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The Future of Semiconductor Packaging

Volume 21, Number 6

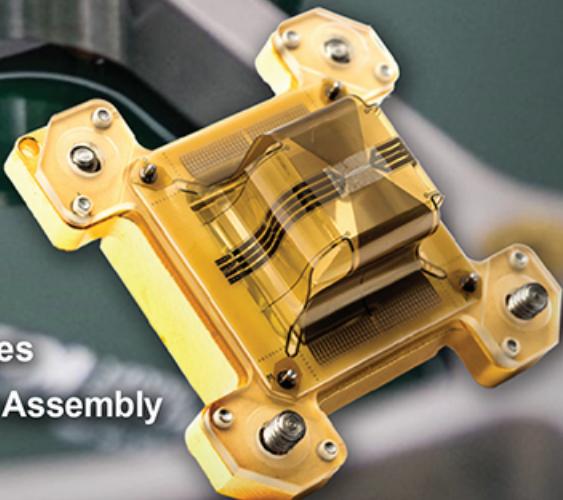
November • December 2017

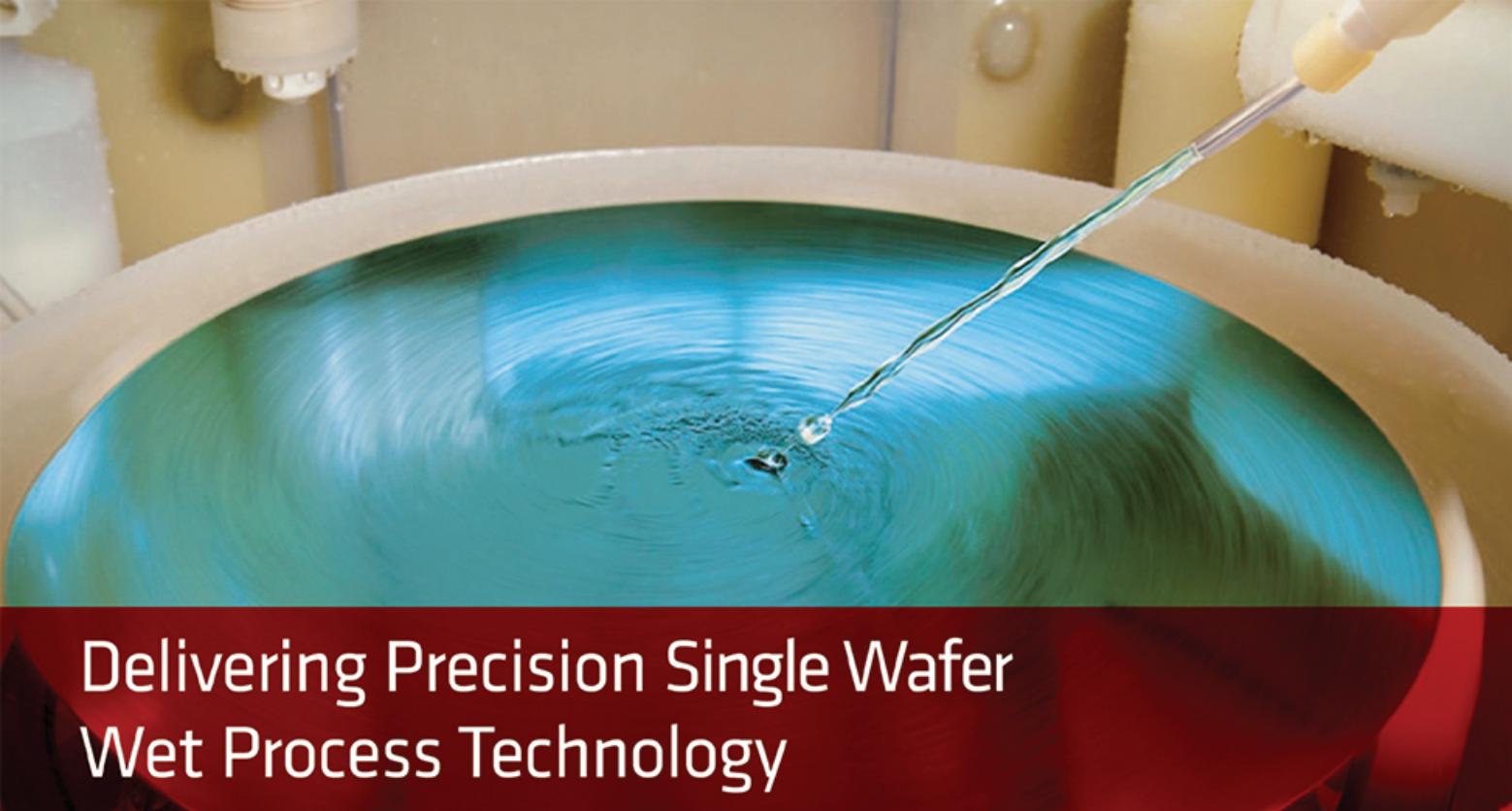
Probe technology for advanced 3D chips

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- Thermocompression bonding
- Optimizing fan-out die placement
- Testing of automotive electronic ICs
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Flux Clean	✓			
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The photo shows a close-up of a FormFactor Pyramid Probe® Rocking Beam Interposer (RBI) probe core. Clearly visible is the tip-layer membrane on top of the space transformer membrane, which connects to the core-I/Os on the four edges of the probe core's metal frame. The background photo depicts the probe core screwed into its 300mm probe card in the test system for evaluation of large-array fine-pitch micro-bump probes in Fab-2 at imec.

Photo: Fred Loosen; Photo composition: Ferenc Fodor and Erik Jan Marinissen – imec, Belgium.

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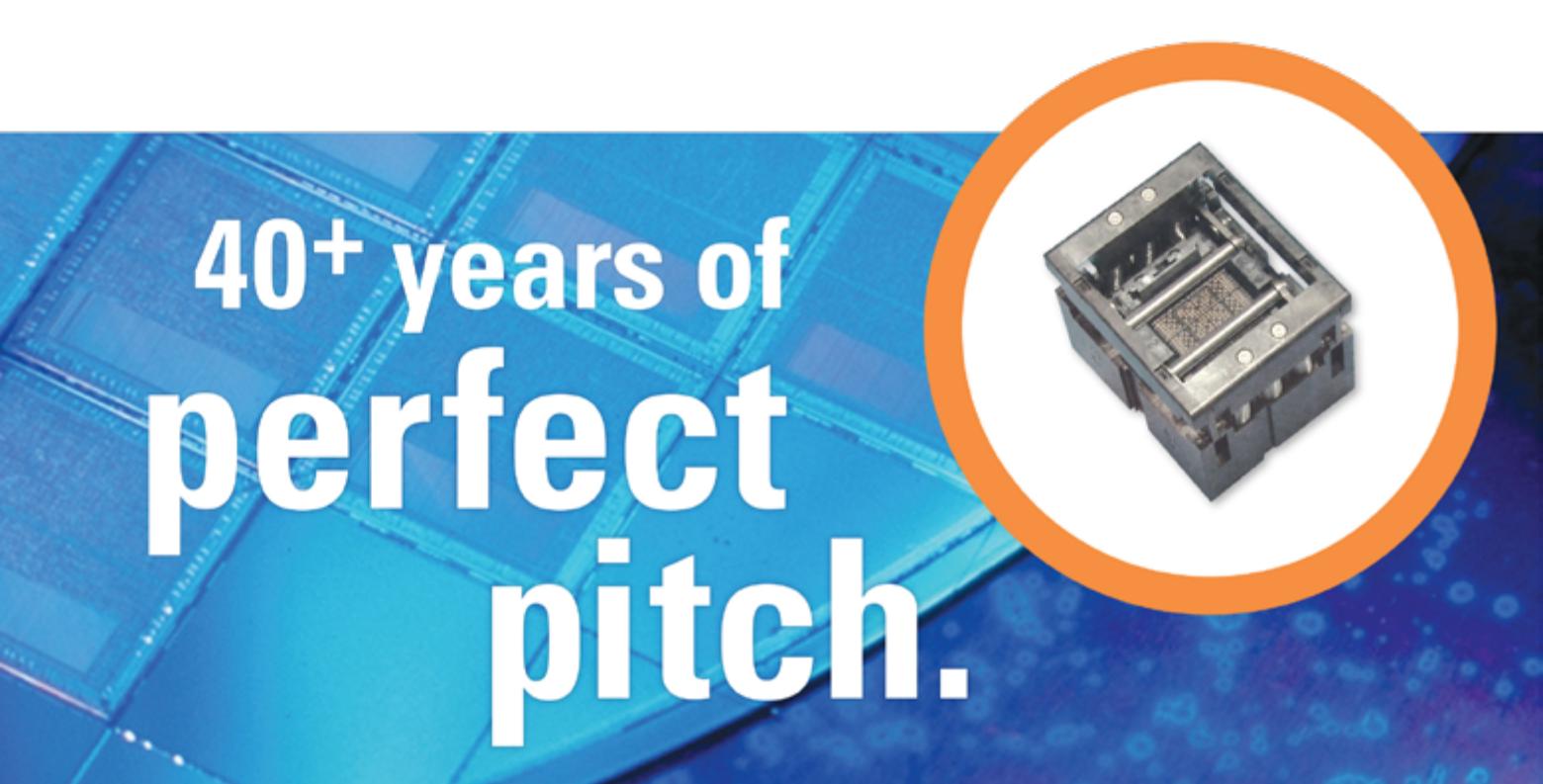
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STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Lawrence Michaels Managing Director/Editor

lmichaels@chipscalereview.com

Debra Vogler Senior Technical Editor

dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Roger H. Grace - MEMS

rgrace@rgrace.com

Dr. Ephraim Suhir - Reliability

suhire@aol.com

Steffen Kröhnert - Advanced Packaging

Steffen.Kroehnert@amkor.com

EDITORIAL ADVISORS

Dr. Andy Mackie (Chair) Indium Corporation

Dr. Rolf Aschenbrenner Fraunhofer Institute

Joseph Fjelstad Verdant Electronics

Dr. Arun Gowda GE Global Research

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Advertising Production Inquiries:

Lawrence Michaels

lmichaels@chipscalereview.com

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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. In the U.S. subscriptions by first class mail are \$125 per year. Subscriptions outside of the United States are \$225 per year to other countries.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine P.O. Box 2165, Morgan Hill, CA 95038

Printed in the United States

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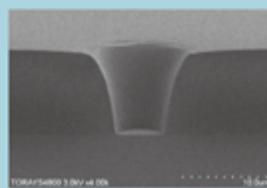
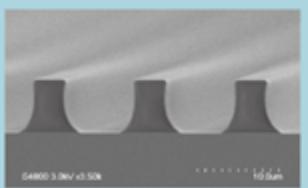
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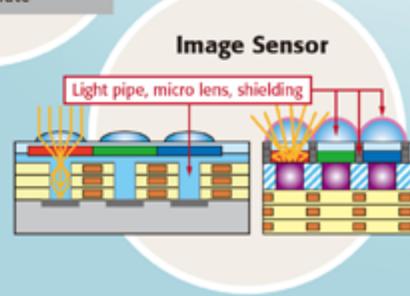
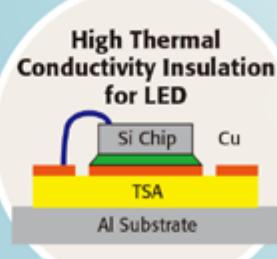
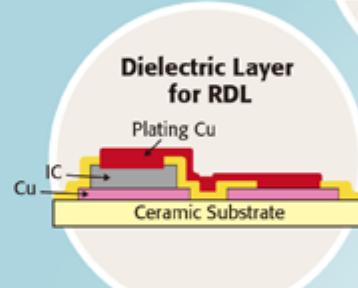
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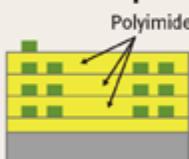
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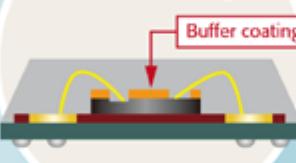
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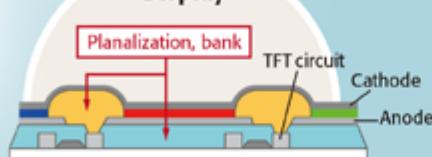
Redistribution Layer



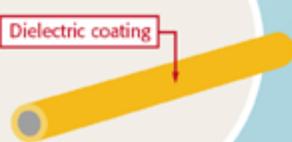
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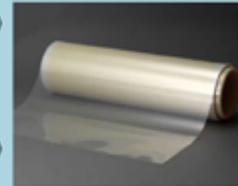
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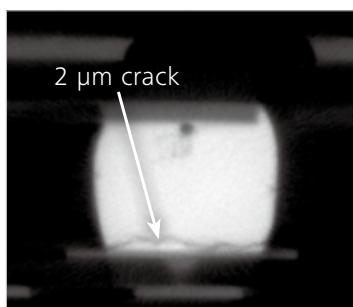
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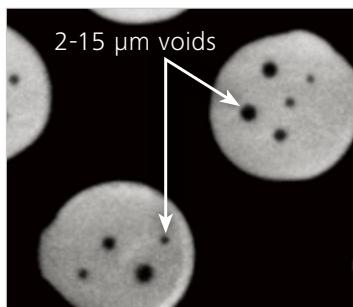
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Executives Speak Out at IWLPC

By Debra Vogler, senior technical editor [[Chip Scale Review](#)]

Panel-based fan-out packaging? Not so fast!

Panel-level based packaging might be the topic du jour, but IWLPC keynote speaker, Han Byung Joon, Chairman of STATS ChipPAC, made the case for tempering the industry's expectations for introduction of the technology. His cautionary take on the matter is not because of the technical challenges so much as for the lack of a sufficient number of killer applications that can provide the volumes needed to make panel-based packaging cost-effective. "We do not see technical problems as being the real inhibitor to panel-level processing."

Han told *Chip Scale Review*. "We already have a proven process with an associated tool set in which we have high confidence in being able to yield high quality and a very cost-effective product. The issues are really supply chain and market related." He believes the industry would need to see maybe one or two emerging applications capable of driving volumes to the levels needed to support panel-based packaging. Han also told *CSR* that the company is participating in the A*STAR Institute of Microelectronics (IME) consortium in Singapore that will be further developing panel-level processing.

To further emphasize his point of view, Han pointed out that if one reviews smartphone forecasts from around 5 years ago, they had led some to believe that panel-based processing would be necessary to meet the volumes required by market demand by this point in time. "But the market

has been disappointing in terms of finding that much volume," said Han. "So unless we see the [semiconductor industry] growth we saw a decade ago, it will be difficult for us to have volume-based cost reduction [brought about by panel-based processing]." Putting an even finer point on his contention, Han told *CSR* that, unlike with fan-out wafer-level packaging (FOWLP), there is no consensus on an industry-winning approach to panel-based processing. He also observed that an outsourced semiconductor assembly and test (OSAT) supplier would need to have a very strong order book to fully load both the existing embedded wafer-level ball grid array-based (eWLB-based) infrastructure, and the additional massive capacity in the form of panel-based processing. "Even incremental capacity in the panel space is massive," said Han. "So the industry overall needs to get comfortable that the top OSATS have sufficient capacity to be reliable suppliers of FOWLP in general (which they do), and then start mapping new product introductions into it in increasing numbers." He further asserts that although this is indeed happening, it is not occurring at a pace that is going to necessitate panel-based process investment in the near future.

In addition to the above considerations, Han said the industry would need to take into account silicon-related aspects of panel-level process qualification. "To qualify a process for production, you would need to fully populate the panel with die – often at the leading-edge process node — so this is very expensive," Han told *CSR*. "It requires a great number of wafers' worth of die given the large panel format, but having access to such a large number of wafers is not always a given." He

further observed that in order to achieve a good time-to-market, one would need to launch a new product based on a round wafer-based format and then quickly follow with a panel-based format as a major cost reduction. "Therefore, the solution provider needs to have both wafer-based and panel-based capabilities, which has implications regarding who is best suited to succeed." Given the above considerations, Han estimates that the industry may be at least 3-5 years away from meaningful panel-based fan-out volume production. "Again, not due to technical constraints, but much more to do with supply chain and market considerations."

Moving beyond the topic du jour, Han believes the industry should keep its focus on wafer-level packaging and making even greater progress with respect to heterogeneous integration, which he believes will be a growth area in the next few years. Han's nickname for the kind of Internet of Things (IoT) applications that will need even greater heterogeneous integration in the near future is "mini-me." These are the kinds of applications that enable us to "participate" or "be present" in events going on in different locations at the same time. Examples include seeing or hearing what is going on inside your home while you are away, or having access to data occurring in a factory thousands of miles away—basically, having access to information that enables you to be more efficient. "Those kinds of applications will be more prevalent, and the industry is not really ready to come up with the integration that will be needed," said Han. He further observed that the so-called "mini-me" applications, though individually do not represent the level of volumes seen with the smartphone, their variety is many. "When you combine them together, it could be significant for a manufacturer."



Han Byung Joon, Ph.D.,
Chairman, STATS ChipPAC

Tackling NRE costs and time to market with heterogeneous integration

In his keynote address at IWLPC, Subramanian S. Iyer, Distinguished Chancellor's Professor at UCLA's Henry Samueli School of Engineering and Applied Science, made the case for addressing out of control non-recurring engineering costs and increased time to market as system-on-chip (SoC) devices have become larger and more complex. While the industry has made some progress with respect



Subramanian S. Iyer, Ph.D.,
Distinguished Chancellor's
Professor, UCLA

to tackling these issues by using 3D stacking of dies and wafer-level fan-out processing, Iyer wants to see these evolve so that heterogeneous integration becomes the backbone of a new SoC methodology that extends to inte-

grating entire systems-on-wafers (SoWs). Iyer described an integration scheme developed at UCLA, called SuperCHIPS (or Simple Universal Parallel intERface). This is a fine-pitch integration scheme (i.e., dielet to interconnect fabric assembly) on a silicon interconnect fabric (Si-IF) [1; and see sidebar "SuperCHIPS in brief"].

The SuperCHIPS approach provides significant value at the system level while lowering the barrier to entry compared with a chip-based SoC approach that is currently used, noted Iyer. "More importantly, it will allow us to re-architect systems in a very significant way," said Iyer. "This transformation is already underway with 3-D stacking of dies and wafer-level fan-out processing, and will evolve to make heterogeneous integration the backbone of a new SoC methodology, extending to integrate entire systems-on-wafers (SoWs)." He also explained that this scheme will help redefine the memory hierarchy in conventional systems and in neuromorphic systems. In such systems, Iyer explained that

the memory is distributed in a nonhierarchical manner. One could, for example, distribute memory so that it is intermingled with the processors in a multi-core system — in a sort of checkerboard pattern — as opposed to traditional memory that is distributed much farther away from the processors. Furthermore, the method described above can be extended to flexible and biocompatible electronics with medical engineering applications into what Iyer refers to as truly three-dimensional systems, meaning systems in which communication is more like the human brain (i.e., any portion of the system can communicate with any other part of the system).

Reference

1. S. Jangam, et al., "Latency, bandwidth and power benefits of the SuperCHIPS integration scheme," ECTC, 2017 IEEE 67th.

SuperCHIPS in brief

As indicated in [1], SuperCHIPS has shown improvements in bandwidth, latency, and power. The dielets range in size between 1-25mm² and are attached to a rigid Si-IF with a pitch ranging from 2-10μm and a short inter-die distance of between 50-500μm using solderless metal-to-metal thermal compression bonding (TCB). The UCLA group's simulations [1] show that links in the Si-IF have a 5-25x improvement in data bandwidth, which can improve system performance (>20x) when compared to PCB-style integration and may even approach single die SoC metrics in some cases. According to Iyer, this method enables heterogeneous system integration and provides significant reduction in design and validation cost. Iyer also emphasized that one of the advantages in building systems by putting multiple dies together heterogeneously rather than monolithically is that they don't have to be in the same technology. "One of the dies could be in 45nm technology, another in RF, and still another using III-V materials," Iyer told *Chip Scale Review*. "You optimize all of these technologies to be at the right price point and the right cost point for these applications."

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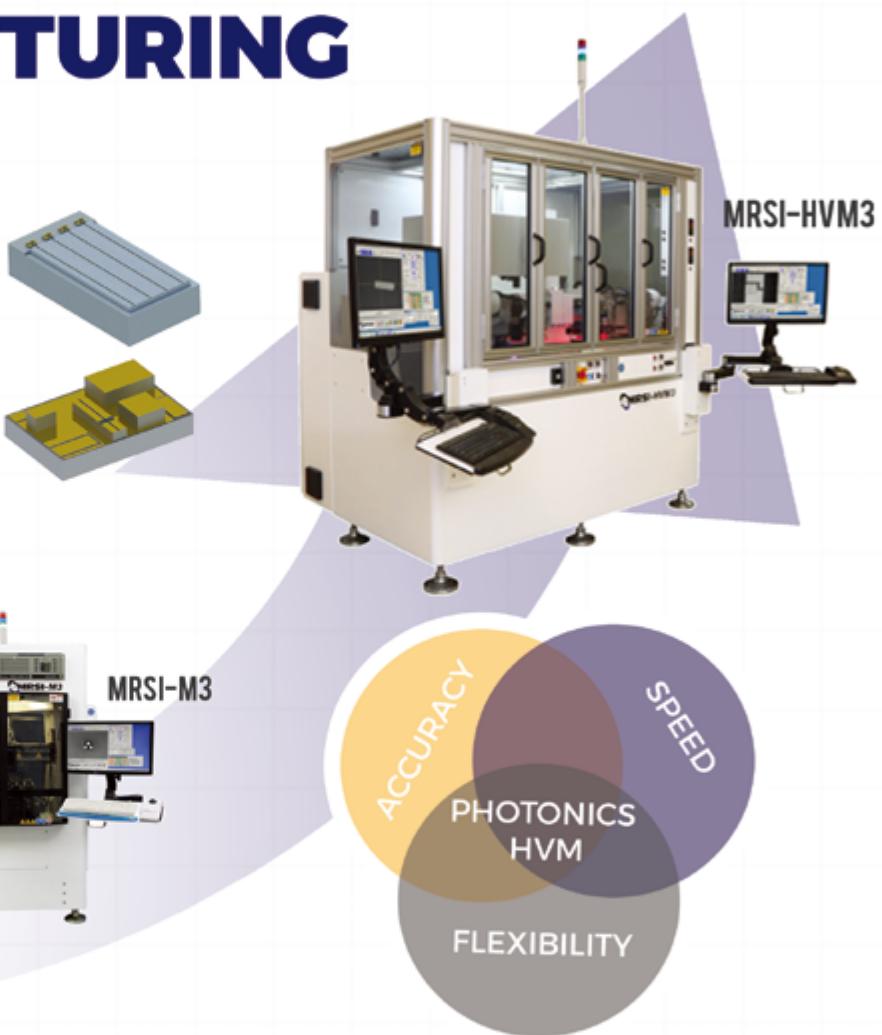
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GUEST EDITORIAL



Heterogeneous integration paving the way beyond silicon scaling limits

By Louis Burgyan *[LTEC Corporation]*

As in prior years, the in-depth presentations at this year's IWLP, covering a broad array of the industry's critical challenges, did not disappoint. A series of keynote presentations and papers included a couple of major announcements that will be discussed below. Of special note, several keynote speakers focused on heterogeneous integration and the added complexities of migration to large rectangular panels. The session presentations reported impressive progress in material science, manufacturing processes, new equipment, metrology, and testing. A few selected

is expected to grow 4%, while the fan-out wafer-level packaging (FOWLP) market is expected to grow 36%. How will the packaging industry and its supply chain keep up? There is no simple answer to



Panel Discussion - Scaling Up Panel Level Processing, Challenges and Opportunities

this multi-faceted question, however, the various keynote speakers and panelists provided attendees with excellent insights.

Naturally, the question of "round vs. rectangle" was in the minds of many presenters, panel members, and attendees alike. Will FOWLP technology remain on round wafers or migrate over to large rectangular panels? Will the success of one approach lead to the eventual demise of the other? The consensus is that both FOWLP and large FOPLP ($600 \times 600\text{mm}^2$ or similar) will coexist for the foreseeable future. There are good reasons for this: migration from WLP to PLP must be an evolutionary step. You start on WLP and move on to PLP after successful production experience is gained on the WLP line, with high yield and proven reliability. Several speakers alluded to the point citing similarity of the technical requirements and challenges along both paths. Some noted it would be a huge risk to commit to build a billion-dollar PLP fab line without prior WLP experience. The technical challenges, the large diversity of the integration tasks, potential fluctuations in customer demand,

all represent enhanced risks, highlighting the need for careful assessment of market persistence and product selection. Currently, various sensor products, HDMI modules, optical communication modules, etc., appear to be viable candidates for fan-out packaging (FOP) or FOPLP, perhaps later followed by 5G antenna modules, RF system-in-package (SiP), even LED modules. The latter is a potentially very large market. Hopefully, in the coming years, we will see customer demand emerging from a broadening range of industries; however, for now, handset demand remains in the driver's seat.

FOPLP at the verge of volume production

Over the years, the industry became accustomed to Apple being tight-lipped about giving forward-looking guidance concerning its packaging needs. Only benchmarking and deep analysis can tell us what kind of packaging technology it actually did deploy. All the more reason to thank **Richard (Kwang Wook) Bae**, VP, Corporate Strategy & Planning Team at Samsung, who outlined the company's vision for moving forward with heterogeneous integration in his keynote. Samsung is developing its own in-house packaging technology—working on homogeneous and heterogeneous fan-out SiP solutions using redistribution layers (RDL).



Keynote audience

The company anticipates a gradual disappearance of current package-on-package (PoP) solutions from the mobile space. Depending upon specific applications, both die-first and die-last approaches are envisioned. As other speakers, Bae stressed the many potential benefits offered by large panel FOPLP. For example, normalized to the throughput of a 300mm wafer line, up to 5.1x improvement can be achieved on large panels (no exact size was given), leading to significant cost savings. In addition, improvements in electrical, thermal performance, and form factor are also expected. Two processes, ePLP (chip first) and PLP-m (chip last) were mentioned by Bae, the latter intended for side-by-side multi-die SiP (**Figure 1**). Samsung is developing chip-first and chip-last FOPLP depending on the die size, number of dies and package structures (PoP, side-by-side, etc.). It has already developed key FOPLP technologies and plans for mass production early next year starting with chip first (**Figure 1**).

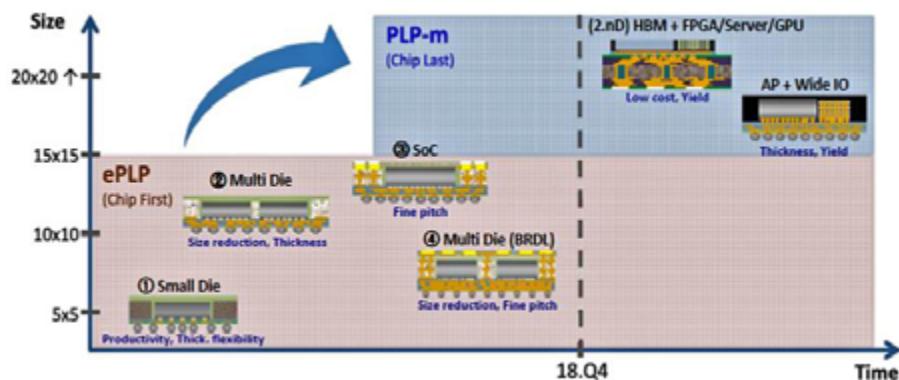


Figure 1: Samsung's FOPLP roadmap. COURTESY: Samsung



Richard (Kwang Wook) Bae - Samsung Electro-Mechanics

The ePLP version, intended for small dies, demonstrated good reliability results with RDL having 5µm L/S. My interpretation of the hints is that the initial product launch is likely to have 10µm L/S, perhaps less. Production starts next year on 510x500mm² panels. Other process varieties and possibly larger panel sizes will follow later.

Construction of a 600x600mm² panel assembly line, also aiming for volume production next year, was disclosed by nepes Corporation. According to **Jay Kim**, presenting for **Lewis (In-Soo) Kang**, the company was able to leverage its considerable experience in 650x750mm² LCD panel fabrication, now in its fourth generation. He is confident that all major issues have been resolved. For example, warping is held below 1mm, and die shift is <10µm in the X direction and <5µm in the Y direction. The company prefers a large panel size and might consider upgrading to 650x650mm².

Tanja Braun of Fraunhofer IZM, presented the results of fabricating advanced LED devices on 457x305mm² panel for now, while aiming to upscale to 610x456mm² panel size later. This R&D feasibility project was initiated by the government of Germany for obvious reasons: 1) the LED lighting market is huge—LEDs enable energy savings and promote a green economy; and 2) large panel embedding, if successfully developed, could open the door for cost reduction thereby spurring wider adoption of LED lighting. Like other presenters, Braun's team also followed the “predictable” path by first implementing the project on 200mm wafers and then transferring it over to large panels. An “on-panel” die-shift measurement algorithm was used for die placement error correction including Θ correction. Double-sided Cu plating, 355nm picosecond laser via drilling, liquid molding, and other innovative techniques were used and evaluated in this project.



Tanja Braun, Ph.D. - Fraunhofer IZM



Jay Kim, Ph.D. - nepes Corporation

In his keynote presentation, **B. J. Han**, Chairman of STATS ChipPAC, offered a realistic assessment of the current state of wafer- and panel-level packaging technology, including his vision of the future. He noted that multi-layer RDL with 40-50µm bump pitch eliminates the need for the interposer, and can incorporate thin-film and other passive components; it is expected to remain the dominant approach for creation of 2D and 3D SiP solutions. Han suggested the vast majority of applications do not require 2µm L/S—what's needed on large panels are 5µm L/S and 100% yield. Han highlighted the simplicity of the chip-first, die face-

down approach of the company's eWLB process supported by a solid supply chain. He further noted that the technology is easily scalable to any wafer size from 5in to the current 12in to 450mm if needed, on the same line. Having shipped over 1.5 billion units, eWLB serves as a solid foundation to expand into eWLB FOSiP. Currently, the company is starting to ship in the millions of FOSiP devices and expects significant growth in the coming years.



B.J. Han, Ph.D. - STATS ChipPAC

Materials and hardware

Overall, given the presentations and discussions at the conference, I saw signs of intense activity and progress all along the manufacturing ecosystem from materials research to lithography, wafer handling, plating equipment, and metrology, just to mention a few, as noted below.

Daisaku Matsukawa of Hitachi Chemical DuPont Microsystems reported on the development and evaluation results of a new low-temperature curable (200–225°C) polyimide/poly-benzoxazole (PI/PBO) that reliably supports 5–6µm L/S vs. the conventional material having 15µm capability and a 375°C cure temperature, resulting in lower shrinkage and less warpage. The new material shows improved flatness and chemical resistance.



Daisaku Matsukawa, Ph.D. - Hitachi Chemical DuPont Microsystems Ltd.

Hitoshi Araki of Toray Industries reported the development of the LT-58000 low-temperature curable positive-tone photosensitive dielectric material having high elongation (40%) and low cure temperature (225°C) for wafer and large panel-level applications as an RDL dielectric. Both properties are essential for warp reduction. The material was thoroughly tested and proven reliable. It demonstrates 300mJ/cm² (i-line) sensitivity, good chemical resistance, good uniformity on 650x550mm² glass panels and supports 5µm L/S.



Hiroshi Matsui - SCREEN Semiconductor Solutions

Hiroshi Matsui of SCREEN Semiconductor Solutions reported on the development of direct-write lithography equipment designed for patterning at 5µm L/S and beyond. This system measures the actual die location and applies corrections accordingly, including global Θ compensation.

James Welsh of Atotech discussed a new Cu electroplating method and associated tool for dual-side copper termination of power semiconductor devices for electro-mobility applications. A unique feature of the approach is its ability to enable simultaneous Cu plating on both sides of the power semiconductor device while maintaining independent and uniform thickness control on each side. Warpage-free dual-side Cu plating was produced using a thin Taiko wafer [<http://www.discousa.com/eg/solution/library/taiko.html>] with continuous Cu plated on the back side. Up to 50µm continuous plating thickness was demonstrated. The dual-side method is significant in that it will lead to improved thermal electrical performance. The company estimates that the reduced process steps enable 26% wafer cost savings.

Christian Ohde reported on Atotech's newly developed electroplating tool, which was designed to meet the needs of large panel embedding up to 600x650mm² and presented results obtained on a 370x470mm² panel. The system uses multiple segmented anodes (not consumable) with reverse anode/cathode pulsed plating and adjustable current distribution. An iron redox system delivers the Cu from a separate reservoir. Cu plating results using 8/5µm L/S showed improved panel-scale uniformity at 1µm/min deposition rate.



Christian Ohde, Ph.D. - Atotech Deutschland GmbH

Justin Oberst of Lam Research Corporation introduced the company's SABRE® 3D front-end/back-end electro-deposition system that enables the use of a thin seed layer of 600Å and a fine-line RDL with 2µm L/S and 4/2µm via aspect ratio. Used in conjunction with Ultratech equipment, a uniformity of <0.2µm was reported over the entire wafer.

Heard at the show

Aside from the many informative presentations, the Exhibitor Hall, networking breaks, and interactive presentations offered many opportunities to engage and learn.



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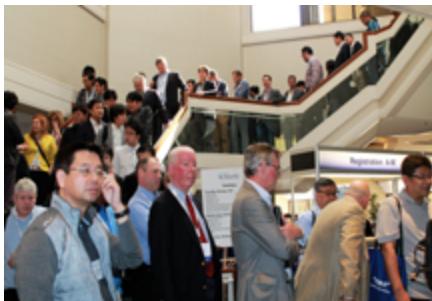
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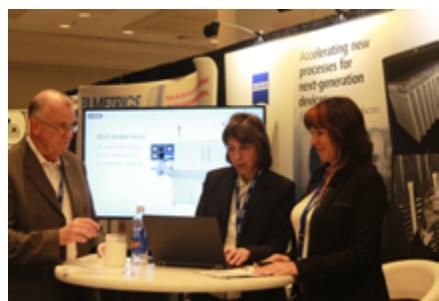




Expo - Canon USA, Inc.



Networking break



Expo - ZEISS Semiconductor Manufacturing Technologies



Interactive Presentations (Posters)

As explained by **Keith Best**, Director of Application Engineering, Rudolph Technologies developed lithography equipment with an improved stage.

The system is capable of handling large panels having warpage as high as 15mm, by multiple means: mechanical, and electro-optical. The application of mechanical force and vacuum reduces warpage during the lithography process to conveniently manageable levels. The residual warpage is handled by dynamic focus adjustment. Position errors of the die are handled by applying feed-forward metrology followed by dynamic error correction. The company also developed a method for detecting non-visual killer defects from transparent films such as photoresist (PR), polyimide (PI) and poly-benzoxazole (PBO) on wafers and panels. Its ultrasonic metrology equipment has capabilities suitable for back-end metrology. A picosecond laser is used to excite the area under test, and the reflected ultrasonic waves are captured for imaging.

Summary

All in all, the IWLPC 2017 reported an impressive array of progress throughout the manufacturing ecosystem, and many of the presenters reported significant advances in various aspects of packaging technology. The keynote presentations offered a reassuring perspective of the future of wafer- and panel-level packaging technology near term, as well as long term. For the first time ever, we could hear loud and clear from industry leaders the long-awaited confirmation that new components and subsystems manufactured on 600x600mm² panels will finally begin to roll out of the assembly lines next year. That will mark 2018 as a major milestone in heterogeneous integration. With these developments as a backdrop, next year's IWLPC (October 23-25, 2018; San Jose California) will surely be another exciting event, promising to offer valuable insights into the unfolding "more than Moore" era of heterogeneous integration. Mark your calendar!

Biography

Lajos (Louis) Burgyan received his Master's in Electrical Engineering from the Polytechnic U. of Budapest and is a retained consultant and technical advisor to LTEC Corporation; email louis.burgyan@ltec.biz

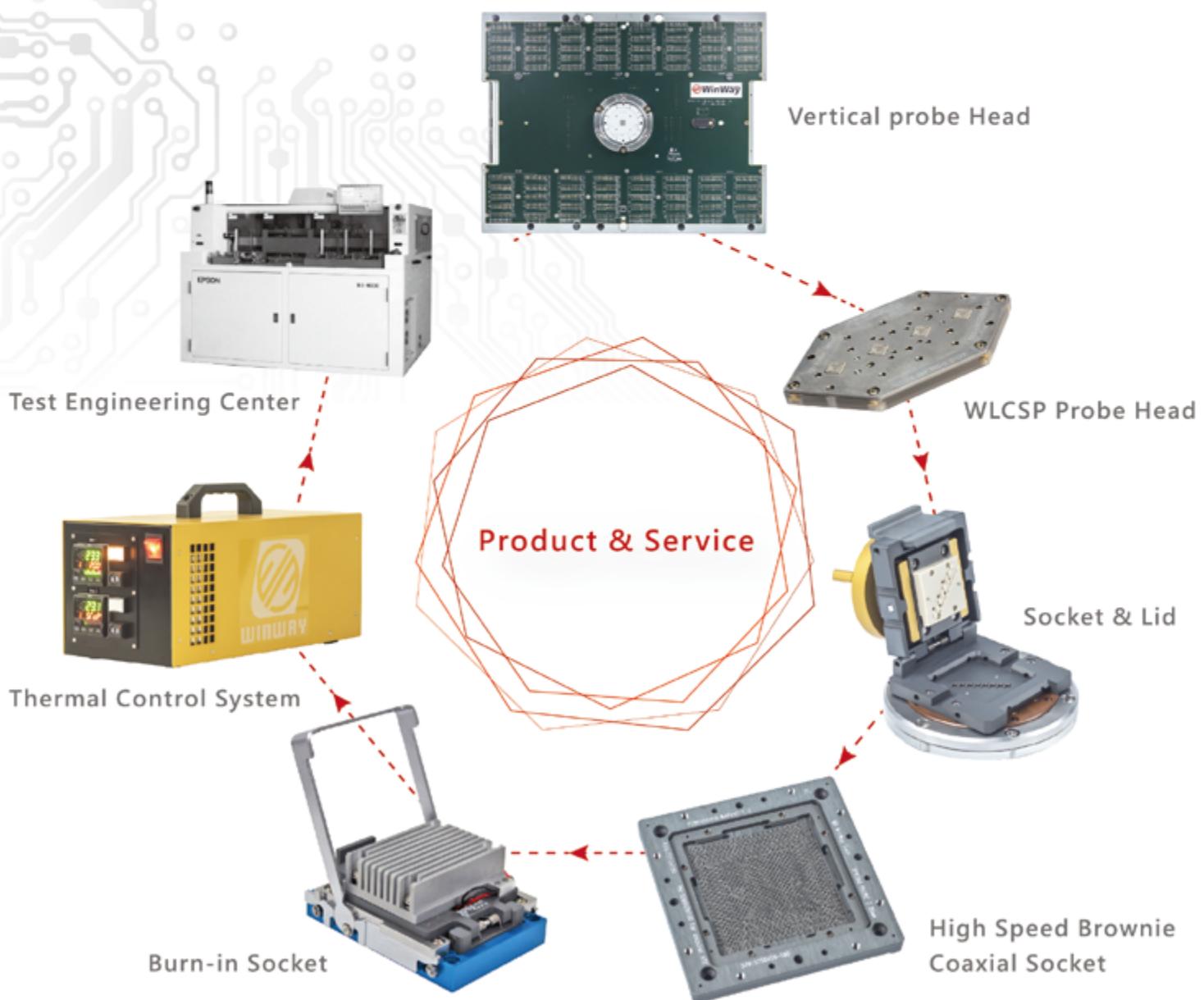
Visit the website for the slide show and video from this year's IWLPC. www.iwlpc.com

An advertisement for Plasma Etch. The top half features the company logo "PLASMA ETCH" with the tagline "PROGRESS THROUGH INNOVATION". Below this is the headline "PLASMA IMPROVES BONDING!". The middle section shows a white plasma cleaner unit with a control panel and a circular port. To the left, text lists benefits: "Our fully automated plasma cleaners offer:" followed by a bulleted list: "Improved Markability", "Enhanced Adhesion", "Better Bonds", "Easier Assembly", and "Surface Modification". Below this is a claim: "100% removal of organic contaminants with a low environmental impact!". At the bottom, it says "STARTING AT ONLY \$ 5,900 USD" and "TO LEARN MORE, VISIT www.PlasmaEtch.com OR CALL 775-883-1336".



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Evaluation of advanced probe cards for large-array fine-pitch micro-bumps

By Erik Jan Marinissen, Ferenc Fodor, Bart De Wachter [[imec](#)] and Jörg Kiesewetter, Ken Smith, and Eric Hill [[FormFactor](#)]

Vertically-stacked multi-die assemblies are a cost-attractive alternative to keep the momentum of Moore's Law going now that technology-node scaling becomes increasingly difficult and expensive. Such assemblies come in many flavors: 2.5D- and 3D-stacked ICs, fan-out wafer-level packages (FOWLP), etc. The stacked components are often large dies in leading-edge technology nodes. Consequently, their yields require testing before stacking (so-called "pre-bond test"), to prevent low compound stack yields and associated high costs. These products have in common that their inter-die connections are implemented with large arrays of fine-pitch micro-bumps. For the non-bottom dies in a die stack, these micro-bumps are the only available wafer-probe interface for pre-bond testing.

Until recently, probing large-array fine-pitch micro-bumps to get wafer-level pre-bond test access into the dies was considered "impossible;" conventional cantilever-type probe cards cannot cover the large arrays, and vertical probe cards do not offer the required fine pitch. This has changed with the arrival of advanced MEMS-type probe cards that offer large fine-pitch probe arrays that match the micro-bumps. In this article, we describe the process and results of the evaluation of such advanced probe cards at imec. For this purpose, we have manufactured dedicated micro-bump test wafers and developed and installed inside our $\varnothing 300\text{mm}$ Fab-2 clean room a new test system with dedicated hardware and software.

Probe targets

Today's most challenging micro-bump probe targets are specified by JEDEC memory interface standards: High-Bandwidth Memory (HBM2) has the largest array (~4,900 micro-bumps) and

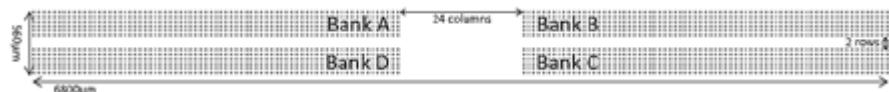


Figure 1: JEDEC's WIO2 micro-bump array [1].

Wide-I/O Mobile DRAM (WIO2) has the finest pitch ($40\mu\text{m}$). In our experiments, we have used WIO2, as it has the most aggressive pitch. A WIO2 interface (**Figure 1**) consists of four banks of $73 \times 6 = 438$ micro-bumps each (hence, a total of 1,752 micro-bumps) with bank gaps of two rows and 24 columns [1].

Imec's process-of-reference (PoR) micro-bumps at $40\mu\text{m}$ pitch are representative for the industrial state-of-the-art. The landing bumps are made of copper, have a diameter of $25\mu\text{m}$, and a height of $5\mu\text{m}$. The top bumps are made of copper, nickel, and tin, have a diameter of $15\mu\text{m}$, and a height of $5+1+3.5 = 9.5\mu\text{m}$.

For characterization purposes, imec designed dedicated test wafers containing only micro-bumps which are all shorted by an underlying blanket copper layer. We named the die design "BMB:" blanket micro-bump. Each of these $\varnothing 300\text{mm}$ wafers contains over 9.4M probe-target micro-bumps, in addition to dummy, identification, and alignment micro-bumps. The 93 dies per wafer contain, among others, 27 WIO2 arrays. We have manufactured these BMB wafers with micro-bumps varying in diameter and metallurgy, including our PoR micro-bumps.

Automatic test system

The automatic test system we have built up for micro-bump probing in the clean-room of imec's Fab-2 in Leuven (see

Figure 2) consists of the following components: 1) test instrumentation consisting of a digital multi-meter and a wide switch matrix, contained in 2) a hard-docking test head with manipulator, which connects through an interface with spring-loaded contacts to 3) an advanced MEMS-type probe card, which is placed in 4) a fully-automatic probe station with wafer loader; the system is completed by 5) in-house developed software for automatic test generation and result data visualization and analysis. The various system components are described in more detail below.

The probe station is FormFactor's fully-automatic Cascade CM300 in dual configuration, i.e., two probers sharing a central material handling unit (MHU), a.k.a. "auto-loader." The two probers are largely identical. Both can automatically load wafers from the shared MHU, but also have a front-side manual load port that accepts $\varnothing 200\text{mm}$ and $\varnothing 300\text{mm}$ wafers as well as large SEMI G74-0669-compliant tape frames for wafers up to $\varnothing 300\text{mm}$ [2,3].



Figure 2: Test system for evaluation of micro-bump probe cards installed in Fab-2 at imec.

Both probers feature an anti-vibration table, a thermally-controlled wafer chuck (between -60 and $+200^{\circ}\text{C}$), and a general-purpose interface bus (GPIB) command interface. The probers support vertical, non-see-through probe cards through software overlay of the wafer image from the downward-looking platen camera and the probe-card image from the upward-looking chuck camera.

The left-hand prober has been adapted to work in conjunction with a hard-docking test head. To make space for the test head, the default microscope bridge and top-view camera have been removed. Fortunately, the (also downward-looking) platen camera is still available. A Reid-Ashman manipulator lifts the 165kg test head and allows it to gently lock into the docking mechanism on the probe station. Once docked, the tester channels connect to the probe card via a spring-contact interface.

The test instruments are based on National Instruments' (NI) PXI series. An NI STS T2 test head holds two PXI racks. Rack 1 is primarily used for parametric and functional testing, while Rack 2 is dedicated for WIO micro-bump probing. Rack 2 contains a PXI-4072 digital multimeter (DMM) that drives nine concatenated PXIE-2535 switch matrix modules, constituting a wide switch matrix with $9 \times 136 = 1,224$ output channels. These output channels ultimately connect to probed micro-bumps and by appropriately configuring the switch matrix, we can allow the DMM to perform two- and four-point resistance measurements between any of the micro-bumps.

The probe card routes the test signals to its center, where we are employing as probe head a Pyramid Probe® Rocking

Beam Interposer (RBI) "probe core" from FormFactor (see Figure 3). A probe core is a rectangular metal frame with a "plunger" that sticks face-down through a rectangular hole in the probe card and touches the wafer. On its four outer edges, the probe core makes electrical contact to little pads on the probe card. A thin-film membrane patterned with conductive traces is attached across the plunger and serves as a space transformer between the core-I/Os and the dense array of probe tips. The RBI probe tips are part of a coupon of a second thin-film membrane, which is affixed on top of the aforementioned space transformer membrane. The tip area is $6 \times 6\mu\text{m}^2$. As the probe tips rock during wafer contact, the actual physical contact to the wafer is made only by the "heel" of the tip, which gives probe marks of $\sim 6 \times 1\mu\text{m}^2$ (see Figure 8).

Imec developed in-house software, both for automatic generation and operation control of the tests, as well as for test data analysis and visualization. A test executive program in LabVIEW controls the NI test instrumentation and, through GPIB commands, the Velox operating system of the Cascade CM300 prober. Test programs are generated automatically based on input files describing: 1) the test system, and 2) the requested measurements for the device-under-test (DUT). The former remains stable over time, while the latter are chip-design specific. The test system description is essentially a look-up table that associates the various probes, via core-I/Os and spring-loaded contacts, to output channels of the wide switch matrix. From these inputs, the test generation software creates a list of switch matrix settings that connect the DMM channels to the proper probe tips. Typical measurements are two- or four-point resistance measurements between specified micro-bumps (that respectively,

include or exclude the parasitic resistances in the test system itself), and the so-called "probe-check" routine (see sidebar, "Probe check routine").

The system's raw measurement data consists of a list of time-stamped resistance values R (in Ohms). These resistance values R are classified as: 1) pass ($R \leq R_{\text{threshold}}$), 2) fail ($R > R_{\text{threshold}}$), or 3) open ($R > R_{\text{max}}$), where $R_{\text{threshold}}$ is determined via a cumulative distribution function (CDF) plot and R_{max} represents the measurement range. Typically, we extract large amounts of raw data out of even a single wafer, and so there is a need to abstract and visualize that data. Our software in LabVIEW and Excel generates wafer maps, micro-bump maps, probe maps, core-I/O maps, and spring-contact maps of single touch-downs, as well as aggregate versions of such maps for multiple touch-downs. These maps are "clickable" to allow the user to drill down during data analysis. While for the evaluation of a new probe card, the probe maps are most interesting, core-I/O maps and spring-contact maps allow us to monitor the health of the test system itself. A probe map can, for example, be used to identify a probe that consistently does not make

Probe check routine

This routine checks for every probe in a given probe set P whether it makes proper electrical contact to the wafer. In an iterative loop over all probes $p \in P$, a two-point resistance measurement is performed between probe p and all other probes $(P \setminus \{p\})$ ganged. These measurements require that all probes are electrically shorted, e.g., by probing on a blanket conducting wafer or on a dedicated "probe check short" structure on a patterned wafer. Our BMB wafers are perfectly suited for the probe-check routine, as all their micro-bumps are shorted. The measurement results include the parasitic resistances of the connections in the test system and probe card from the DMM to probe p , but, provided $P \setminus \{p\}$ is large enough, excludes the parasitic resistances of the connections in the test system and probe card from the DMM to all other probes.

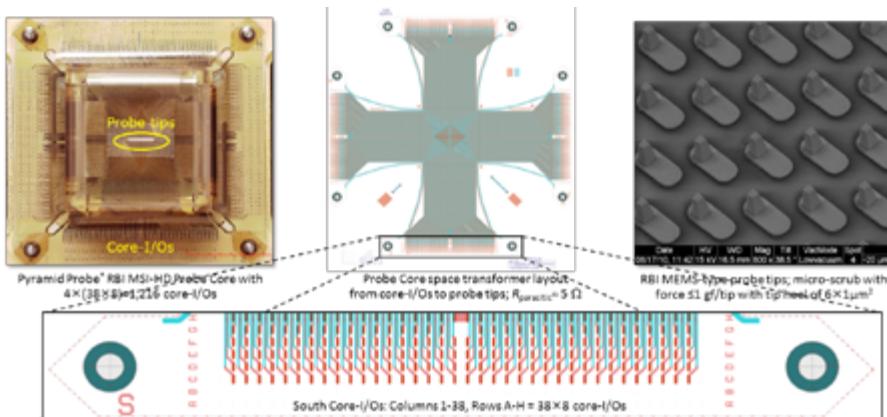


Figure 3: FormFactor Pyramid Probe® RBI "probe core:" from core-I/Os via the space transformer to the probe tips.

contact, e.g., because its tip sits higher than its neighbors, the tip needs to be cleaned, or there is an open contact in the space transformer. A core-I/O map can be used to identify opens or poor contacts at that interface. A spring-contact map can, for example, be used to identify non-functional spring-loaded contacts, a tilted test head, or an issue with the dock's locking mechanism.

Probe card evaluation results

The purpose of wafer probing is to make a proper electrical contact, through which the die in question can be tested. Our incoming inspection procedure is performed routinely on new probe cores that arrive at imec. It consists of an iterative execution of our probe-check routine on a blanket copper wafer while increasing the chuck over-travel from 0 μm (= first physical contact) to the maximum as specified by the probe-core supplier. This procedure identifies possible mechanical and/or electrical issues with the new probe core, if any, and allows us to confirm the supplier-specified recommended chuck over-travel.

Figure 4 shows the results from the incoming inspection of a WIO2-1Bank probe core with 438 probes, for which the maximum over-travel was specified at 150 μm . As can be seen,

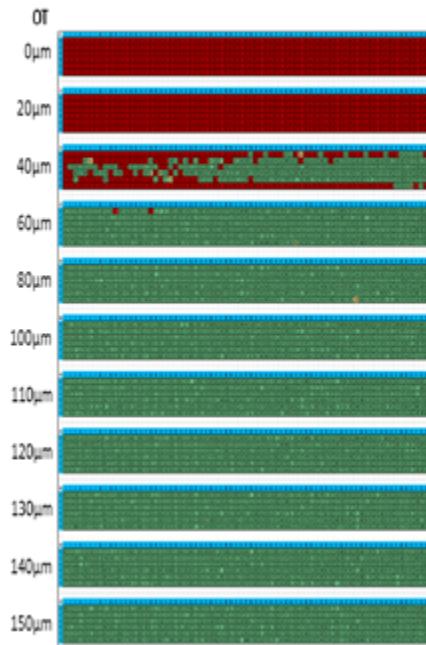


Figure 4: Probe map results of incoming inspection for a WIO2-1Bank probe core.

this probe core operates as expected. It starts making contact at 40 μm over-travel and reaches its best electrical contact at 80-150 μm over-travel. At 150 μm over-travel, $R_{\text{avg}}=20.6\text{ Ohm}$; most of this is the parasitic resistance in test instrumentation, cabling, probe card, and probe core (with $\sigma=2.1\text{ Ohm}$, mainly on account of resistance variation due to the module number of the selected output channel of the wide switch matrix).

We successfully used the FormFactor Pyramid Probe® RBI probe cards with the test system on our BMB wafers with micro-bumps of various diameters and metallurgies. The first thing we wanted to check was if the probe tips indeed landed on the micro-bumps. As

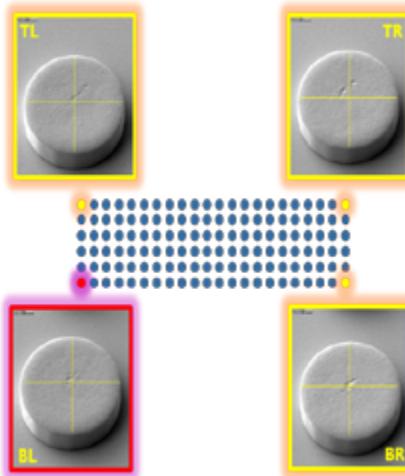


Figure 5: Approach for attribution of probe misalignment to 1) the prober's inaccuracy at specific chuck locations, and 2) the probe core inaccuracy.

depicted in **Figure 5**, we analyzed this by taking scanning electron microscope (SEM) pictures of probe marks at all four corners of the micro-bump array at diverse wafer locations. Ideally, the probe marks are in the center of the micro-bump. For each probe mark, we determined how far it is off-center by measuring its (x,y) coordinates relative to the center of its micro-bump. The probe-top-pad alignment (PTPA) accuracy is affected by both the probe station and the probe core. We attribute the misalignment in the bottom-left corner of the probe array to the probe station, as that bottom-left corner was the focus of the probe station's probe-card training. The PTPA inaccuracy

caused by the probe station varies with the chuck position, and therefore is depicted in a wafer map. Next, we translate the four coordinate pairs such that the bottom-left corner matches the center of its micro-bump. The remaining misalignment of the other three corners indicates to what extent the probe core's tip array is off with respect to the micro-bump array grid.

Figure 6 shows PTPA accuracy results achieved on BMB wafers with a WIO2-1Bank probe core; the misalignment is separated out for probe station and probe core. The probe station is rather accurate: over the entire wafer chuck, the maximum error is 2.5 μm . The probe core tips are positioned very accurately: over the entire array, the maximum error is 1.33 μm (top-left corner). Note: such satisfactory results require regular calibration of the prober's chuck

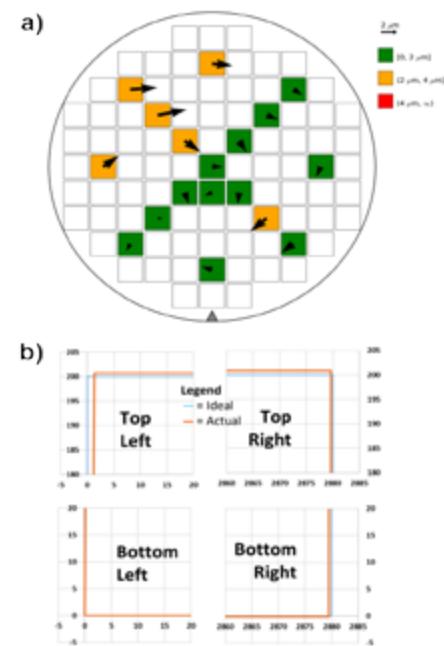


Figure 6: Measurement results of probe-mark misalignment due to: a) the CM300 prober's inaccuracy at specific chuck locations, and b) inaccuracy of the WIO2-1Bank probe core.

positioning system and usage of the prober's thermal-control system to keep the system and test wafers at a constant ambient temperature.

Electrical measurement results depend strongly on what type of measurement is requested and on the metallurgy of the to-be-probed



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micro-bump surfaces. Example results for various wafers are depicted in **Figure 7**. The type of measurement determines which parasitic resistance contributions from the test system itself are included in the measurement result. For a two-point measurement, all parasitic resistances are included in the measured resistance value. Typically, these parasitic resistances are significantly larger than the resistance of the micro-bump to micro-bump connection through the wafer – cfr. the large green arrow in **Figure 7**. And then there is the contact resistance between probe tip and micro-bump. The latter is small, but unmistakably varies with the metallurgy of the micro-bump's probe surface – see the smaller purple arrows in **Figure 7**.

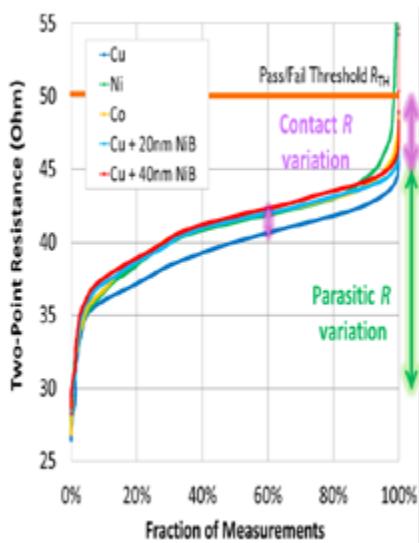


Figure 7: Cumulative distribution function plots of two-point resistance measurements between shorted micro-bumps with varying metallurgies at their probe surface.

Probe marks on Cu micro-bumps are small (see **Figure 8a**), and therefore, we do not expect a negative impact on the interconnect yield after stacking despite the probe mark. For Cu/Ni/Sn micro-bumps, the probe marks are relatively larger (see **Figure 8b**) because these micro-bumps are smaller and so the probe tip is relatively big, but mainly because Sn is a much softer material than Cu and easily deformed. Fortunately, Sn is very forgiving when it comes to stacking. Experiments in which we compared all four cases of yes/no probing the bottom/top micro-bumps, followed by stacking did not

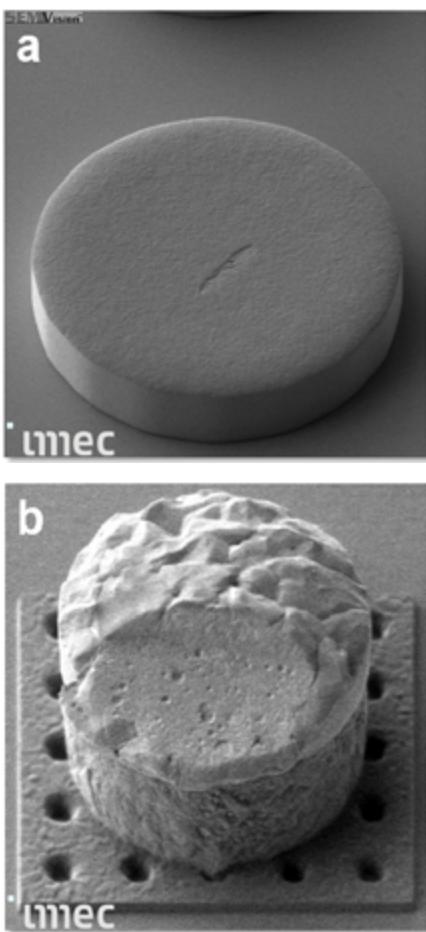


Figure 8: Probe marks on micro-bumps with different dimensions and metallurgies: a) $\varnothing 25\mu\text{m}$ Cu micro-bump; and b) $\varnothing 15\mu\text{m}$ Cu/Ni/Sn micro-bump.

reveal any impact of probing on the interconnect yield [4]. Optionally, the Sn micro-bumps can be reflowed after probing, to restore the Sn cap, remove the probe mark, and thereby prevent particle entrapment.

The data presented above highlights factors that impact the industry's bottom line concerns. Probe cards are consumables with a limited number of touchdowns. The advanced FormFactor Pyramid Probe® RBI probe cores are not inexpensive, so every touchdown adds cost. However, comparisons with the cost analysis tool 3D-COSTAR from TU Delft and imec [4-6] revealed that using these expensive advanced probe cards to probe on micro-bumps is still significantly cheaper than its alternative: providing a limited number of large, easy-to-probe pre-bond probe pads, as this will increase the test time significantly and still leaves the micro-bumps untested.

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Biographies

Erik Jan Marinissen received his MSc and PDEng degrees in Computing Science and Software Technology from Eindhoven U. of Technology, the Netherlands and is Principal Scientist at imec in Leuven, Belgium; email: erik.jan.marinissen@imec.be.

Ferenc Fodor received his BSc degree in Industrial Automation from the Technical U. of Cluj-Napoca, Romania and is Test Engineer at imec.

Bart De Wachter received his BSc degree in Electrical Engineering from Odisee U. in Ghent, Belgium and is Test Engineer at imec.

Jörg Kiesewetter received his PhD degree in Mechanical Engineering from the Technische U. Dresden and is Director of Engineering at FormFactor GmbH.

Ken Smith received his BSc degree in General Engineering from Oregon State U. and is Principal Engineer at FormFactor, Inc.

Eric Hill received his BSc degree in Engineering and Applied Science from the California Institute of Technology and is Director of Technology at FormFactor, Inc.

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Cleaning fine-pitch copper pillar flip-chip packages

By Mike Bixenman [KYZEN Corporation]

The miniaturization of modern electronics continues to challenge the effectiveness of common cleaning processes and the ability to obtain desired cleaning performance and optimal yield. When soldering the flip-chip die to the ball grid array (BGA) interposer, water-soluble paste fluxes are used to ensure a strong metallurgical bond. Ineffectiveness in removing flux residues can lead to contamination, underfill voiding, poor yield, and reliability issues in the field.

Devices utilizing copper pillar technology have more interconnects per surface area, which results in tighter pitch and lower standoff gaps. As standoff gaps lower, flux residues have less area to outgas during reflow. This results in more active residues under the die. A longer wash time using water with a low concentration of cleaning agent is typically required to properly clean die under these lower standoff gaps.

Aqueous saponified cleaning agents diluted in deionized (DI) water have commonly been used to remove flux residues under the flip-chip bottom termination. Saponified cleaning agents are mildly alkaline to form an attractive force to the flux residue. However, alkaline cleaning agents can react, consume and corrode reactive metals. Longer time in the cleaning solution increases chemical attack, which can cause failures due to mechanical stresses. Potential metal incompatibilities and insufficient rinsing represent the most common challenges for engineering improved cleaning agents for cleaning copper pillar flip-chip packages.

Current saponified cleaning solutions adversely react with many metals (Al, Cu, Sn, Ag, Ni, etc.) that are present on the copper pillar die. Especially in alkaline solutions, Al is readily attacked causing galvanic corrosion reactions. Also, there is the potential for defects and discoloration on Cu and SAC alloys during the cleaning process. Crevice corrosion from cleaning solution reactions with exposed metals can weaken interconnects and reduce mean time to failure.

Cu pillar technology

Copper pillar bumping is a growing design trend in electronics packaging. Copper

pillar technology offers many advantages in speed and line pitch. Building integrated circuits with copper and aluminum reduces the potential for electromigration while improving current carrying capacity. Likewise, copper pillar is more cost effective than Au stud bumps for high bump designs. Finer pitch can be achieved, which translates into higher performance over a smaller surface area (Figure 1).

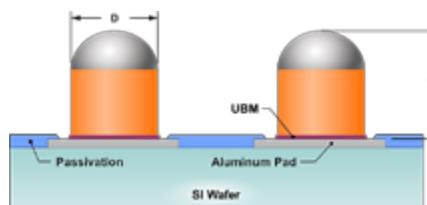


Figure 1: Copper pillar design.

Unlike the traditional bumping process, the copper pillar design exposes a number of reactive metals to the cleaning process. Many of these metals react and dissolve when exposed to saponified cleaning agents. Corrosion inhibitors can reduce, and in some cases, prevent this interaction. The challenge is designing cleaning agents that are effective at inhibiting the different exposed metals with which the cleaning agent comes in contact. If longer cleaning time is needed, the risk of metal interaction is greater.

Aluminum is highly reactive when exposed to alkaline cleaning agents. Common saponified aqueous cleaning agents that are used to clean traditional bumped die work well. These cleaning agents are not suitable for cleaning copper pillar die due to their propensity to attack aluminum and copper. Aluminum is a diffusion barrier metal for copper. Common alkaline cleaning agents can attack, dissolve and crack the aluminum pad. Figure 2 is an example of how a traditional saponified cleaning agent attacks, corrodes and dissolves the aluminum pad. Copper is also reactive when exposed to alkaline cleaning agents. Cleaning solutions with poor copper inhibition will tarnish and oxidize the side of the copper pillar (Figure 3).

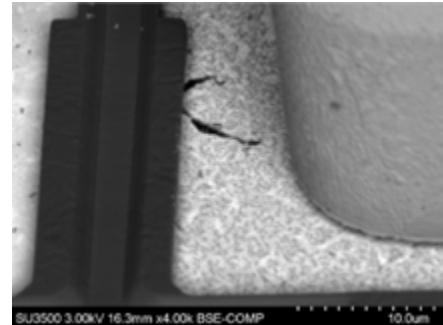


Figure 2: Al pad dissolves, cracks and turns white.

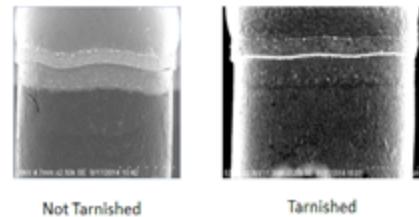


Figure 3: Copper pillar oxidation.

Nickel functions as the intermetallic layer between the copper pillar and SAC305 alloy. Cleaning agents high in alkalinity have been shown to undercut the copper/nickel adhesion layer (Figure 4). SAC305 alloy can pit and darken when exposed to highly alkaline cleaning agents. Longer

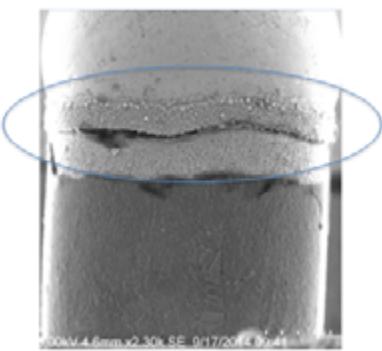


Figure 4: Nickel adhesion layer undercut.

exposure time increases the interaction (Figure 5). The problem is that cleaning agents that react with the exposed metals result in various forms of pitting, galvanic and crevice corrosion. The corrosion effect not only affects electrical performance

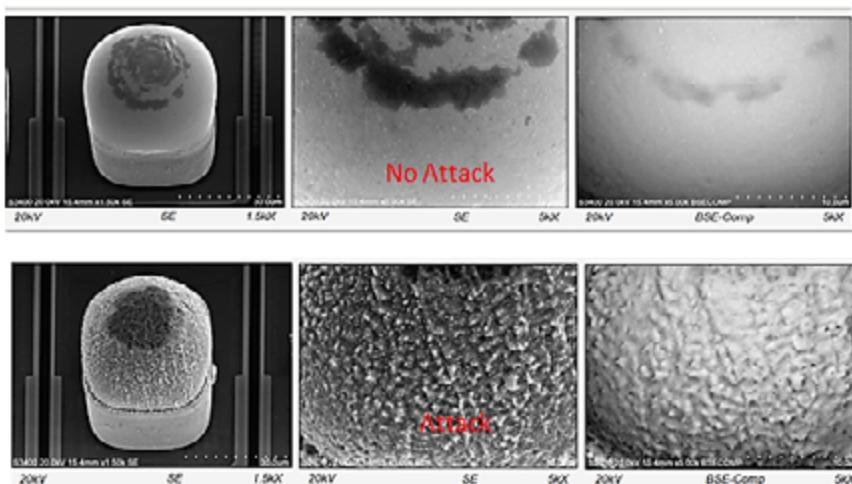


Figure 5: Solder alloy pitting.

but also reduces adhesion. Weakened intermetallic layers compromise the integrity of the copper pillar design.

Balanced cleaning agent design

A well-designed cleaning agent must be capable of removing process residues without causing material compatibility issues. The functions of the flux engineered into solder pastes, paste fluxes and liquid fluxes are many and include:

- Remove oxide layer from pad and solder alloy;
- Protect solderable surfaces during reflow;
- Consume the flux just as the solder begins to melt;
- Be active at 130°C for SnPb and 150°C for SAC;
- Remain active for 90-120 seconds;
- Leave a benign residue;
- Leave a residue that repels (hydrophobic) moisture;
- Provide excellent solderability; and
- Reduce other defects such as head-in-pillow, graping and bridging.

Engineered water-soluble paste fluxes are used to join the interposer with the copper pillar preformed bumps. The flux removes oxide layers from the solder cap and placement pads. During solder reflow, the flux improves wetting to enable a strong metallurgical bond from the flip-chip die to the substrate. During reflow, the flux residue will accumulate under the die and feature out near the edge of the die. At the edge of the die, flux can become depleted to the point where the use of water only is insufficient to clean the edge of the die (Figure 6).

Alkaline saponified cleaning agents commonly are used at low concentrations in DI water, ranging from 3-8% to improve wetting and removal of charred water-soluble flux residues. An alkaline cleaning agent exhibits a strong intermolecular force for the water-soluble flux residue. This cleaning agent design worked well when cleaning a traditional bumped die that only exposed the SAC alloy to the cleaning process. As illustrated in the introduction section of this article, these alkaline cleaning agents are highly reactive to other exposed metals that make up the Cu pillar design.

An effective cleaning process requires both chemical and mechanical forces to rapidly clean the flip-chip BGA package. The packages are placed in a fixture and cleaned at high throughput rates through the cleaning process (Figure 7). If either the chemical or mechanical forces are not balanced, parts will exit the cleaner with residue remaining, which impacts yields. The

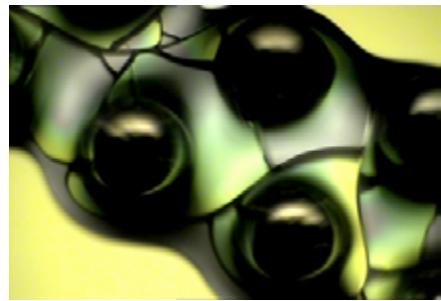


Figure 6: Flux depletion at the edge of the die.

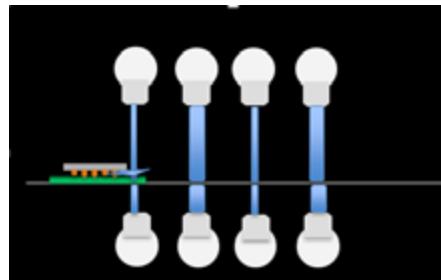


Figure 7: Cleaning process illustration.

job of the cleaning agent is critical in that it must rapidly wet and dissolve flux residues quickly. Other critical properties are materials

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P0.4mm 81GHz**

The advertisement features a black rectangular test socket with a central circular opening. The text "TTS BGA 22" and "TTSCF22T4B2.3-2.4HM35" is printed on the top left. On the bottom left, it says "SO2.4mm" and "P.0.4mm". The background is a green hexagonal grid pattern.

Test Tooling Solutions Group

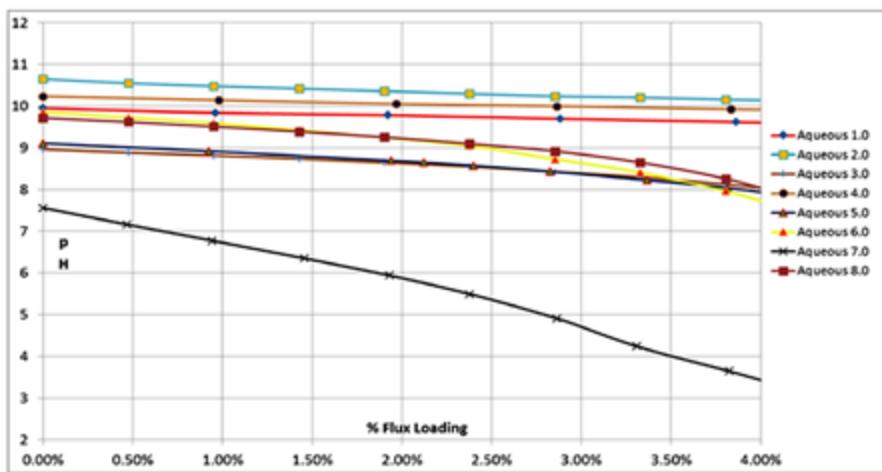


Figure 8: Cleaning agent pH as a function of bath loading.

compatibility, in the case of the Cu pillar with exposed metals, and low foaming.

If the exposed metals on the Cu pillar are contacted with a cleaning solution that reacts with a metal, metal ions will be lost from the metal into the aqueous cleaning solution, leaving electrons behind on the metal. A metal that is attacked by the cleaning solution loses some of the metal electrons through a half cell electrochemical oxidation. The aqueous cleaning agent solution where metal electrons are gained is the reduction electrochemical half cell. A number of issues can occur, such as deformation, cracking and weakened bonds. When exposed to mechanical stresses, the package can cause an in-field failure.

A balanced cleaning agent must work as well as the traditional alkaline cleaning agent for cleaning Cu pillar die. One approach is to design a cleaning agent that is neither alkaline nor acidic. The intermolecular cleaning forces using a neutral cleaning agent will not form as strong of an attraction to the flux residue. To overcome this issue, the cleaning agent can be built with functional additives that dissolve instead of saponifying the residue. Potential tradeoffs when cleaning a water-soluble residue are bath life due to a pH shift into the acidic range, higher operating concentration to clean the residue, and poorer rinsing effects. This option provides better materials compatibility on Cu pillar exposed metals but gives up some of the cleaning performance that has commonly been experienced with alkaline cleaning agents.

A truly balanced cleaning agent has the chemical forces needed to remove the flux residues without giving up on the common benefits found with the traditional alkaline cleaning agents. The engineered cleaning composition requires the following properties:

- Solvents and activators that provide dispersion and intermolecular forces of attraction;
- Both polar and non-polar solvents are needed;
 - o Non-polar solvent to facilitate dissolution of resin and rosin polymeric soils
 - o Polar activators to induce both Van der Waals and London Dispersive Forces
- Low surface tension to penetrate low standoff gaps;
- Low foaming under pressure; and
- Broad material compatibility
 - o Mixed metals
 - o Plastics
 - o Part marking
 - o Board laminates
 - o Bonding and stacking materials

The next-generation cleaning agent designed to clean Cu pillar die is formulated to rapidly clean water-soluble flux residues and to not interact with (or attack) exposed metals. The cleaning agent is mildly alkaline to provide needed intermolecular forces of attraction. This feature provides excellent cleaning, holding the soil in the cleaning agent, improved rinsing and long bath life by stabilizing the pH as flux accumulates into the wash bath. **Figure 8** illustrates this point. Notice how the Aqueous 7 pH drops as the bath loads with flux. This pH drops affects both cleaning and rinsing. Aqueous 8 is a truly balanced cleaning agent that cleans well, holds the soil, and does not attack metallization.

The SEM image of the Cu pillar die exposed to the next balance cleaning agent design shows no material effects on the exposed metals (**Figure 9**). The balanced

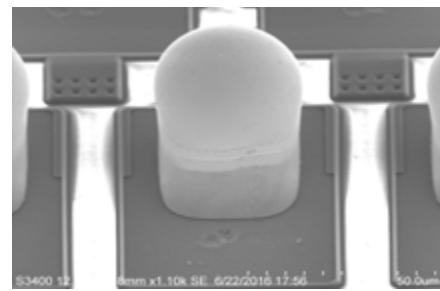


Figure 9: Next-generation cleaning agent that does not attack exposed metals.

cleaning agent hits the design criteria of both cleaning and protecting the Cu pillar die. Some alkaline builder is used to achieve high-performance cleaning while addressing the tradeoffs. The cleaning agent is a drop-in to the current process with comparable performance at the designed concentration, temperature, throughput and mechanical impingement settings. The cleaning agent has no foam issues when sprayed at high impingement energy. The product rinses cleanly with DI water.

Summary

Copper pillar flip-chip has moved into a market leading position on account of its ability to reduce pitch and increase I/O. Improperly cleaned devices can result in poor interfacial bond strengths, electrochemical migration, and failures at the interconnect. Cleaning the package following assembly is a defined and common practice.

Traditional alkaline cleaning agents attack exposed metals on the Cu pillar design. This quality issue can result in field failures. A next-generation balanced cleaning agent design that is a drop-in replacement for the current alkaline cleaning agents was needed. These cleaning agent designs do not materially attack the exposed metals on the Cu pillar design. They are a drop-in replacement for the traditional alkaline cleaning agents with no performance drop off.

Biography

Mike Bixenman received four earned degrees: Chemical Engineering Technology from Nashville State Technical College, Accounting/Chemistry from David Lipscomb U., Masters of Business Administration from Capella U., and Doctorate of Business Administration from U. of Phoenix School of Advanced Studies. He is CTO at KYZEN; email mikeb@kyzen.com

High-performance insulating adhesive film for high-frequency applications

By Junya Sato, Shin Teraki, Masaki Yoshida, and Hisao Kondo *[NAMICS Corporation]*

In today's information society, communication technology is rapidly developing. The use of computing devices, such as various types of smartphones and tablets, has grown significantly. This requires technology that enables high-speed, high-volume data batch transferring and processing with image and video data. High-volume data transferring requires higher frequency application, while high-speed processing and low transmission loss require low dielectric constant (D_k) and low dielectric loss tangent (D_f).

Rising transmission demand in the higher frequency range causes higher transmission loss on the printed circuit board (PCB), leading to delayed or weakened signals. Therefore, a circuit designed to minimize transmission loss in the high-frequency application is necessary. As noted above, this requires insulating materials with low D_k and low D_f .

Furthermore, multilayered substrates have been developed for higher performance. The new film must eliminate substrate warpage and delamination between a conductor and an insulating material to ensure high reliability on a multilayered substrate. Minimizing the difference of expansion coefficient between raw material and substrate is also considered critical for the film.

Challenges

Assuming use in a range of up to several hundred GHz, a low transmission loss in a high-frequency range is expressed in a simple general equation as:

$$\text{Transmission loss } (\alpha) = \text{Conductor loss } (\alpha_c) + \text{Dielectric loss } (\alpha\delta)$$

With respect to conductor loss, it is commonly known that due to the skin effect, the higher the frequency, the current signal flows closer to the surface of the conductor. On a conductor with a rough surface, the current signal is presumed to travel a substantially longer distance on the surface, which leads to greater transmission loss. From this, it can be inferred that enhancing the adhesive strength of the film would reduce conductor loss (caused by the skin effect) on a conductor with a rough surface. An adhesive material is essentially required to provide sufficient adhesive strength on a smoother conductor. On the other hand, the dielectric loss can be reduced by lowering the material D_k and D_f as follows:

$$\text{Dielectric loss } (\alpha\delta) \approx A \times f \times \sqrt{D_k} \times D_f$$

where:

A = Constant number,

F = Frequency,

D_k = Dielectric constant, and

D_f = Dielectric loss tangent.

We have been investigating and developing a material that reduces D_k and D_f . When an insulating film is used as an interlayer adhesive for a multilayer substrate for high-frequency application, the gap of the coefficient of thermal expansion (CTE) between the film and the core substrate causes substrate warping and interlayer delamination between a conductor and the film, thereby leading to poor reliability. The film requires an approximately 20 ppm CTE to minimize the CTE gap between that of the substrate and conductor, respectively.

This paper also examines filler

selection to establish a stable dielectric property performance of the film without reducing current performance, and a resin combination that will afford low dielectric property and good adhesiveness. The paper also reports our achievement of a low linear CTE and low dielectric properties while maintaining high adhesion strength through an investigation of filler selection and resin combination.

Testing

Key factors in the development of this material are presented in the subsections below.

Key factors in the development. It is generally understood that the molecular structure of an adhesive film material has polarity. It is also known that the larger the polarity, the larger the D_k —a result of the orientation polarization of polarized molecules. We therefore developed a film focusing on using a resin with a low polarity molecular structure.

Materials having a chemical structure with low polarization density have low D_k —we considered a desirable material formulation. The study suggests that a rigid main chain backbone and a bulky substituent can effectively reduce D_k , and functional groups with a low polarity molecular structure have positive effects in lowering D_f . Elimination of functional groups having larger polarity is essential to provide a lower D_k ; however, the functional groups affect the adhesion strength. The material selection was carried out in consideration of bringing out the best balance of performance.

Test results: Film A. The test pieces were prepared by vacuum heat molding formulated thermosetting resin composition (under 200°C/1 MPa for 1 hour). The properties of the test

pieces were then determined. The thermosetting film was developed with properties shown in **Table 1** (Film A).

	Film (A)
Dk (2GHz)	2.5
Df (2GHz)	0.0025
Tensile modulus (MPa)	873
Copper peeling strength (N/cm)	11
Copper mat side	
CTE(ppm/deg.C)	120
Tg (deg.C) /DMA	105

Table 1: Properties of the developed Film A.

The results show that Film A exhibited an excellent dielectric property with low Dk and low Df and strong adhesion, however the CTE was too high. This raised concerns of a conduction loss caused by substrate warpage and delamination between a conductor and the insulating film (when forming a circuit substrate). The film CTE for a multilayer application must be lowered to match that of the object on which the film is applied. The desired low CTE is not achievable only by designing the resin backbone—it requires selecting an inorganic filler with lower CTE. Next, the focus was to develop a film with a clear focus on lowering the CTE.

Investigation of fillers. Adding an inorganic filler with a low Dk and low linear CTE is considered to be effective in achieving a lower linear CTE in the film. **Figures 1** and **2** show the Dk and linear CTE of each filler. The results show that silica (SiO₂) filler is suitable for lowering a Dk and

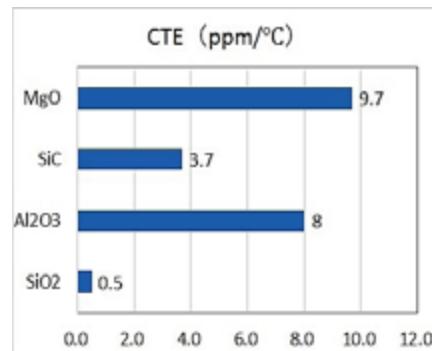


Figure 2: Linear CTE of each filler.

a linear CTE. Therefore, we selected silica as a filler to provide a low CTE for the adhesive film.

The film requires a smooth surface to lower the conductor loss in multilayer applications. With that in mind, we selected a uniform spherical silica particle filler. The filler was then dispersed uniformly in the film to further smooth the surface. We configured the new film to balance the performance of all ingredients by carefully evaluating their respective properties. As a result, we successfully developed Film B using a resin composition with low dielectric property, low CTE, and strong adhesion.

Test results: Film B. The film requires flexibility to be applied on substrates during the multilayering process without breakage. **Figure 3** shows the appearance of Film B. Film B maintains sufficient flexibility while having a low CTE resulting from the added SiO₂. This confirmed that Film B has excellent workability with easy handling when placing it on a substrate.

The test pieces were prepared by vacuum heat molding (under 200°C/1MPa for 1 hour) using the

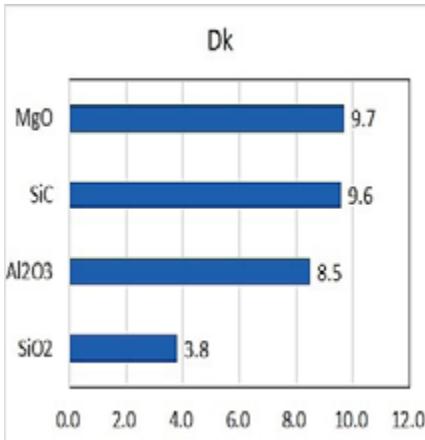


Figure 1: Dk of each filler.

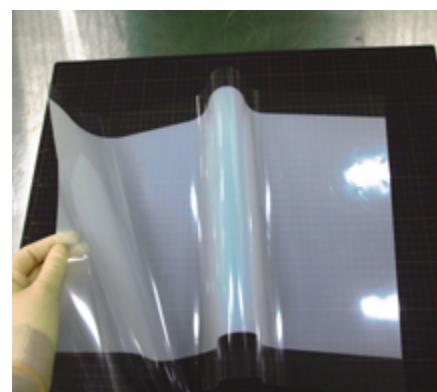


Figure 3: Appearance of Film B.

optimized resin composition. The properties of the test pieces were then determined. **Table 2** shows the results.

	Film (B)
Dielectric constant (2GHz)	3
Dielectric loss tangent (2GHz)	0.0025
Tensile modulus (MPa)	630
Copper peeling strength	
Strength(N/cm)	7
Copper mat side	
Copper peeling strength	
Strength(N/cm)	5.5
Copper shiny side	
CTE(ppm/deg.C)	25
Tg (deg.C) /DMA	150

Table 2: Properties of Film B.

Film B maintained both a low Dk of 3.0 and a low Df of 0.0025. The results show that the CTE was sufficiently lowered to 25 ppm/°C. Adding a filler raised concerns about lowering peel strength, however, our test results achieved high peel strength not only on the rough surface side of the RA copper foil film (1.8 μm), but also on the shiny side of the RA film (0.25 μm). This was achieved through selecting a uniform spherical silica particle filler, optimizing the amount of filler added, dispersing filler uniformly, and selecting a resin with optimal amount of functional groups. The results confirmed the developed insulating adhesive film has low Dk, low liner CTE, and strong adhesiveness, while maintaining low Dk and low Df through regulating CTE.

Dielectric properties depend on frequency. **Figures 4** and **5** show Dk

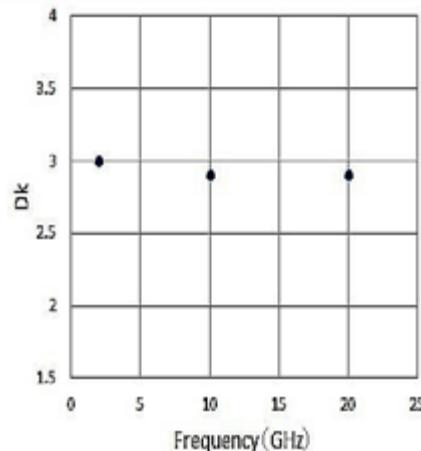


Figure 4: Dk vs. frequency (GHz).

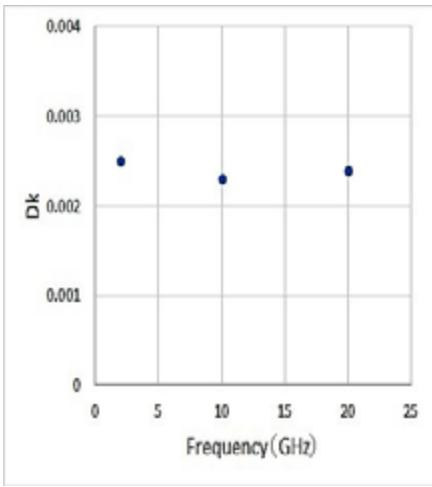


Figure 5: Df vs. frequency (GHz).

and Df in different frequencies. The results confirm that Film B maintains a low Dk and low a Df without any frequency-dependence. This implies that Film B performs reliably even in a high-frequency range.

Transmission loss. We determined if the low dielectric property of Film B can achieve low transmission loss in a circuit through a simulation test. The transmission loss was simulated with the data shown in **Table 3** by using Advanced Design System (ADS) momentum application software. The test also involved a polyimide (PI) microstrip, the current standard material for substrates as a reference.

The tested circuits were 30mm in length with an electrical resistance of 50Ω . The transmission loss (S21) results on Film B and PI were: Film B, -1.0dB and PI, -1.8dB at 20GHz; and Film B, -1.5dB and PI, -2.8dB at 40GHz. The results confirmed that Film B had lower transmission loss than PI. The performance gap between Film B and PI was larger as the frequency increased (**Figure 6**).

Reliability test on the film. Considering the use of Film B on a substrate, we determined the adhesion strength of the film over time under conditions of high temperature, and then constant temperature and humidity; **Figures 7** and **8** show the results for each condition. Both resulted in sufficient adhesion strength with little deterioration even after 1000 hours.

Figure 9 shows the changes of Dk and Df under the constant temperature

	ϵ	$\tan\delta$	t	H	W	Line length
Film(B)	3	0.0025	28μm	50μm	107μm	
Polyimide	3.4	0.014	28μm	50μm	98μm	30mm

Table 3: ADS input data.

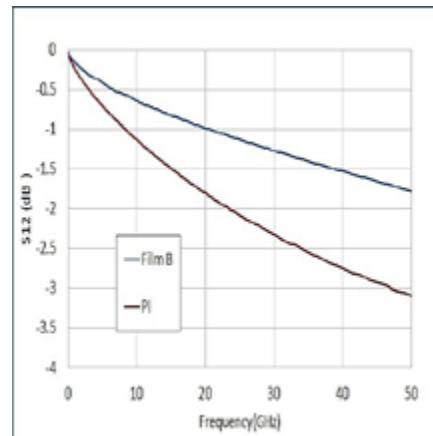


Figure 6: Transmission loss (S21): Film B vs. PI.

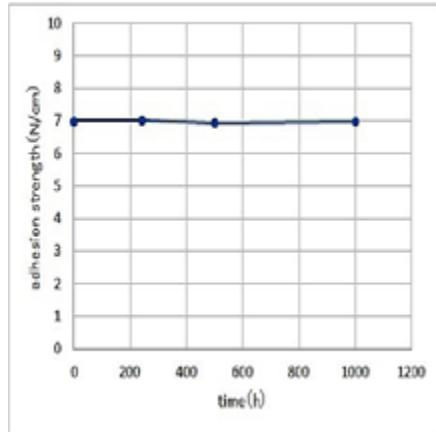


Figure 7: Adhesion strength vs. time at 125°C.

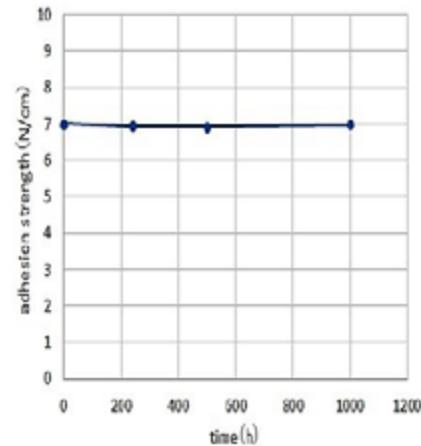


Figure 8: Dk, Df vs. time at 85°C/85% relative humidity.

and humidity conditions. The results proved the desired reliability of Film B showing the lower Dk and Df under constant temperature and humidity.

Melt viscosity curve. Film B demonstrated excellent flowability when heated due to its thermosetting property (**Figure 10**). Film B is cured at a lower temperature of 200°C than the liquid crystal polymer (LCP). In particular, Film B begins to melt at approximately 100°C and hits the lowest melt viscosity at approximately 120°C. The resin flowability increased by melting the resin in Film B while heating it up

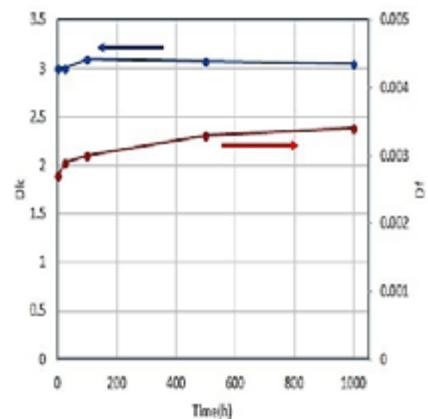


Figure 9: Transmission loss (S21): Film B vs. PI.

to 200°C. This result allows Film B to be better applied to fine circuit patterns. When curing is completed, the resin provides strong adhesion to build a rigid structure.

Evaluation of multilayered substrate. Film B achieves a low linear coefficient of expansion for multilayered substrates. A simple multilayered substrate was prepared using Film B to determine the coverage of copper wiring. Multiple layers of Film B were applied to form a multilayer structure on an FR-4 substrate, a patterned substrate, and copper foils, and then cured at 200°C

for 1 hour. **Figure 11** is a cross-sectional view that shows Film B attached to each layer uniformly.

We were able to create the multilayered substrate using Film B with good bonding between the substrates and Film B and without warpage. We also conducted a solder float test and reliability test under constant temperature and moisture conditions to confirm that the multilayered substrate did not exhibit any swelling or delamination.

Summary

We developed a film that has excellent low D_k and linear CTE performance in a high-frequency range yet provides strong adhesion. By designing a resin focusing on polarization density of molecular composition, employing a uniform spherical silica particle filler in an optimized amount, and dispersing the filler uniformly, we successfully developed the film.

The reliability of the film was evaluated under conditions of high temperature, and constant temperature and humidity. The results show good adhesion strength and good

reliability of D_k and D_f. These results confirm that we have successfully achieved a defect-free substrate with low transmission loss for high-frequency applications. The results of S parameter simulation testing confirmed the higher performance of

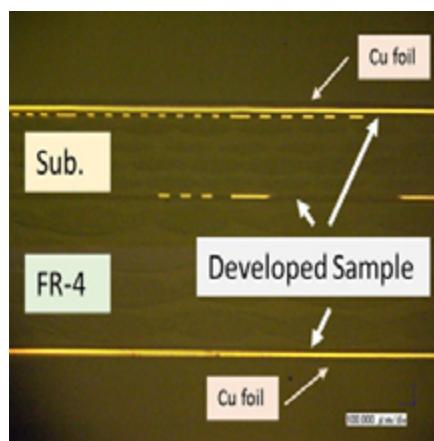


Figure 11: Cross-sectional view of multilayered substrate with Film B.

the developed film compared with PI, exhibiting lower transmission loss on a substrate circuit. The film also has the advantage of being able to

serve as a substrate material with its good adhesion and CTE to PI. One of the film's promising uses is to be a component material for fine wiring and devices such as a multilayer substrate for high-frequency range applications. The film also has great potential to be employed on a millimeter-wave antenna substrate for on-vehicle applications that require high-speed communication.

Acknowledgements

The authors are grateful to Fukuoka U. for its support. We also extend our appreciation to NAMICS managers and colleagues for their useful discussion.

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Biographies

Junya Sato received his MS in Inorganic Material Chemistry from Nagaoka U. of Technology; he is an engineer at NAMICS Corporation; email jsatou@namics.co.jp

Shin Teraki received an MS in Organic Chemistry from Niigata U. He is Group Manager, ADFLEMA R&D at NAMICS Corporation.

Masaki Yoshida received an MS in Mechanical Engineering from Nagaoka U. of Technology and is Team Leader, ADFLEMA R&D, at NAMICS Corporation.

Hisao Kondo received his MS in Chemical System Engineering from Niigata U. and is an engineer at NAMICS Corporation.

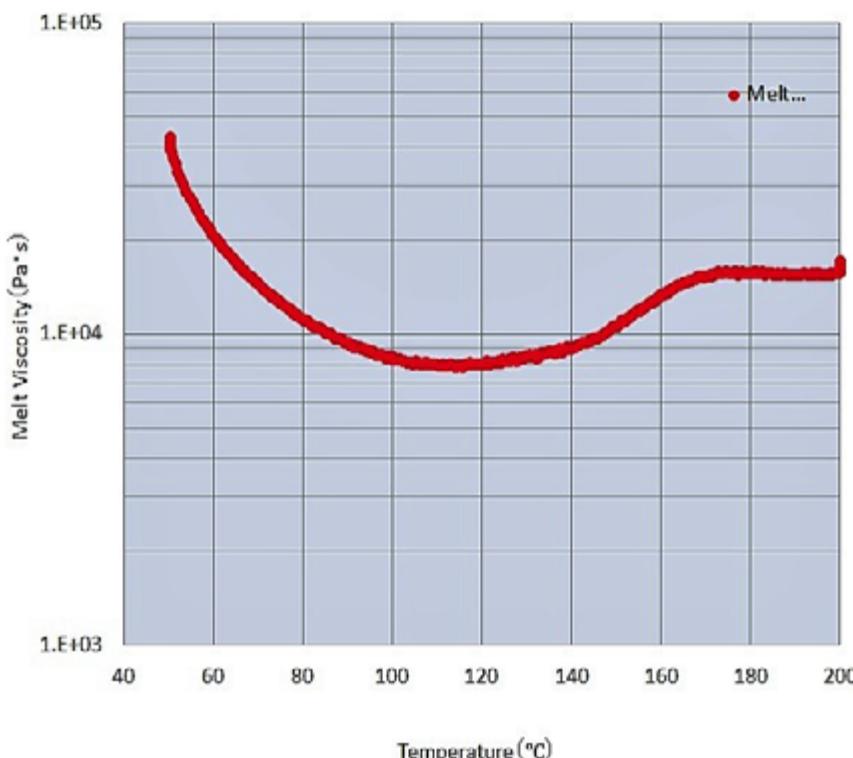


Figure 10: Melt viscosity curve.

Core capabilities of thermocompression bonding

By Hugo Pristauz, Alastair Attard, Andreas Mayr [Besi Austria GmbH]

Part 1 of this article was published March April 2017 (http://fbs.advantageinc.com/chipscale/mar-apr_2017/#16) and focused on an overview of different thermocompression approaches and the technical challenges that can be solved by this technology. Understanding the crucial requirements led us to four core capabilities of a thermocompression bonder, which are discussed in detail in this second part.

To review the points made in part 1, the four core capabilities of a thermocompression bonder (TCB) are: 1) accuracy, 2) coplanarity, 3) bond control, and 4) temperature uniformity.

Accuracy

For a better understanding of the error chain of placement accuracy, the following pragmatic approach, illustrated in **Figure 1**, is useful. It starts with a listing of independent challenges to be mastered for achieving the accuracy targets. In this example, a target is set at $2\mu\text{m}@3\sigma$ for a TC bonding process at the chip-to-wafer (C2W) level with matrix-based bond locations, including temperature ramps, with considerable bond force.

These challenges are listed in the right-most (5th) column in **Figure 1**, which stands for target process requirements. Subsequently, a sequence of simplified reference processes is defined wherein one challenge is eliminated in each step. Because the accuracy target should be easier to achieve after each elimination step, a more challenging accuracy specification can be claimed until the simplest reference application is reached on the left-most side (1st

column) with the most challenging accuracy specification.

Following the approach described above, the first simplification is to move from the real product die application (5th column) to a glass die on glass substrate placement (GoG – 4th column), which eliminates material variations and vision errors, thereby giving more precise post-bond metrology. As a kind of “compensation” for this simplification, the accuracy requirement is enhanced to $2\mu\text{m}@4\sigma$. In a similar manner (3rd column), by moving from high (e.g., 250N) to low bond force (e.g., 30N), the accuracy demand is increased to $2\mu\text{m}@5\sigma$. This scheme can be continued by transitioning from hot to cold process (2nd column), demanding $2\mu\text{m}@6\sigma$, and finally ending at a so-called basic machine capability test (BMC), repeating single-position glass die placements with low bond force without utilization of thermal profiles (1st column). Our demand for BMC placement accuracy is $2\mu\text{m}@7\sigma$, which is equivalent to $0.86\mu\text{m}@3\sigma$.

Having split up the accuracy chain in this way, one can cross-check whether the formulated requirements can actually be

met (**Figure 2**). For the reference process of column 4, the specification of $2\mu\text{m}@4\sigma$ can be slightly out-performed (the actual accuracy reached is $2\mu\text{m}@5\sigma$), but for the easy BMC test with a $2\mu\text{m}@7\sigma$ specification, we can achieve significant out-performance of $2\mu\text{m}@11\sigma$, which relates to $0.55\mu\text{m}@3\sigma$. Obviously, some of the reference accuracy processes are easier to achieve, while others come with significant challenges.

Exercising the kinds of studies described above extensively, most of the attention is ultimately paid to one particular step: moving from a cold (or constant temperature process) to a temperature ramping process because it brings about most of the placement inaccuracy. In this case, it is possible to encounter the abnormal accuracy behavior shown in **Figure 3**. In this example, placement accuracy is close to staying within specification for half of the observation time, but then the process suddenly runs out of control in one direction. It is interesting to understand the root cause of such behavior. Because of the coefficient of thermal expansion (CTE) mismatch between the tool holder (bright green part) and the nozzle (yellow part), it can happen that the

nozzle makes relative movements during the temperature ramps, which can exceed rates of $300^\circ\text{C}/\text{s}$.

Because TC bonders typically use a method to align a die on a bond head nozzle relative to the substrate in a cold or moderate temperature level, any misalignment of the die relative to the bond head during temperature ramping has to be avoided. This is not

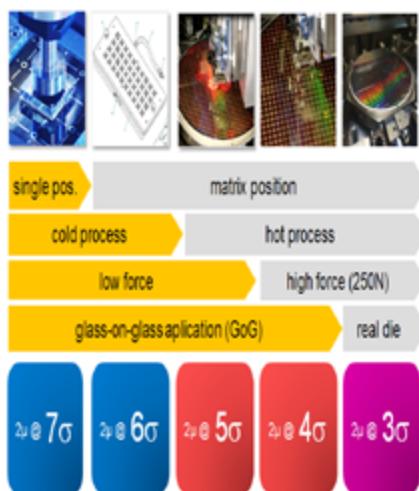


Figure 1: Breaking up the accuracy error chain.

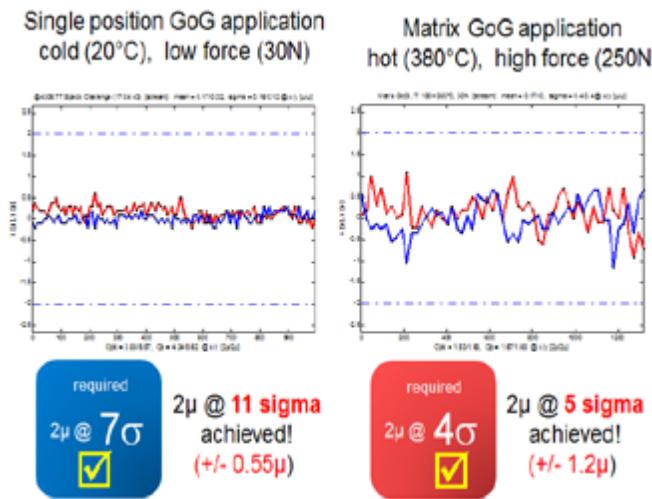


Figure 2: Accuracy performance results.

Essential - Accuracy

Maintain position accuracy while ramping from cold to hot state

Or: bring accuracy from bond head down to die

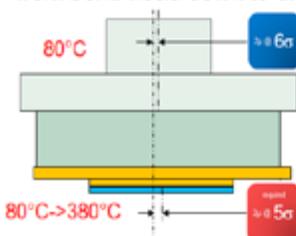
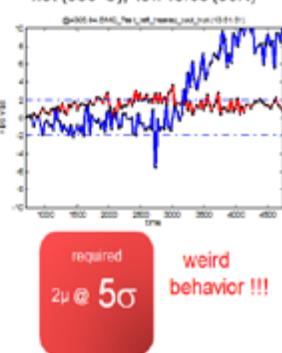


Figure 3: Accuracy challenges of a thermocompression bonder.

Potential Issue

single position GoG application hot (380°C), low force (30N)



Tool Holder: Material A

80°C

isolator

CTE = 3 ppm/K

380°C

Tool Holder: Material B+C

70°C

any, CTE = 9-12 ppm/K

80°C

isolator, CTE = 0.6 ppm/K

380°C

Issues:

- expansion on bottom: 13.5µ/15mm
- Loss of planarity
- Thermal stress
- life time issues
(cracks after >30.000 cycles)

Benefits:

- stays highly planar
- life time: >2 Mio cycles

Drawback

- CTE mismatch between nozzle & tool holder (Si: CTE = 2.6 ppm/K)
- relative movements !!!
- 15 mm Si die: $\Delta 11.7\mu$ @ $\Delta 300^\circ\text{C}$
- isolator: $\Delta 2.7\mu$ @ $\Delta 300^\circ\text{C}$

Figure 4: Different choices of material CTE for the tool holder.

a trivial task considering the fact that the nozzle CTE, which needs to be matched to the die CTE, differs from the tool holder CTE. Such a design approach might be criticized, because it raises the challenge to maintain excellent positional accuracy while ramping from cold (moderate) to hot temperature!

To justify the CTE mismatch between nozzle and tool holder let us compare two different tool holder design approaches (**Figure 4**). In the first approach, the tool holder CTE is matched to the silicon die CTE (about 3ppm/K). Because the tool holder material is thermally insulating

(otherwise it would act as a heat sink and impact the rapid heating rates), there is a large vertical temperature gradient of around 300°C across the tool holder. This results in a thermal expansion mismatch of around 13.5µm over a die size of 15mm, which causes considerable deformations, induces large thermal stresses, and negatively impacts tool holder life time (tool failure after around 30,000 thermal cycles).

The second approach of **Figure 4** targets very low tool holder CTE (0.6ppm/K) with the effect of negligible tool holder deformation and a life time improvement greater than two million cycles. As a drawback, however, there will be relative movements between the nozzle and the tool holder: between tool holder expansion (2.7µm@15mm @300°C) and die expansion (11.7µm@15mm @300°C), a mismatch of around 9µm@15mm will cause relative movements of the parts. These movements can be quite uncontrolled due to other effects such as friction, making it challenging to reach the high placement accuracies required, especially when roadmap accuracies of 0.2µm@3σ are targeted.

How can such challenges be mastered? The actual approach works for 2µm@3σ accuracy and is based on controlled relative movements due to proper design. These details, however, are beyond the scope of this article and it is actually unclear whether this approach is feasible to meet ten times higher placement accuracy specifications.

Coplanarity

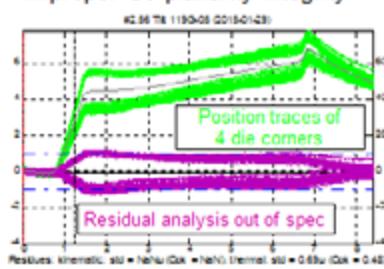
The second TCB core capability is coplanarity, which is important for fine-pitch applications because bump solder cap volume scales down with the 3rd power of pitch,

Figure 5: Coplanarity adjustment mechanism.

Essential: Coplanarity Integrity

„Maintain co-planarity during temperature ramp!“

Improper Co-planarity Integrity



Proper Co-planarity Integrity

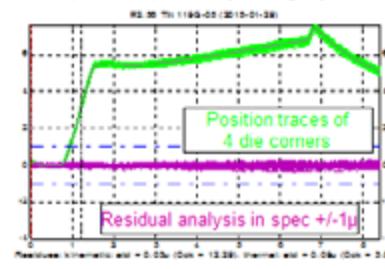


Figure 6: Coplanarity integrity during thermal transients.

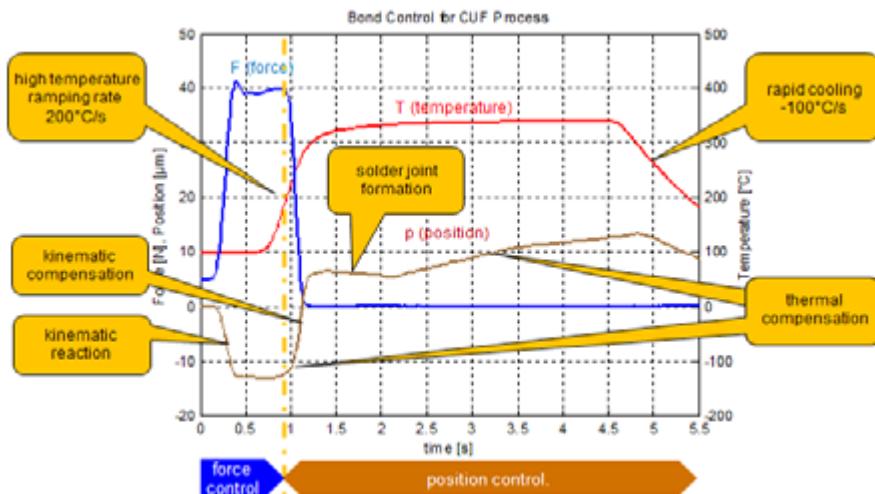


Figure 7: Hybrid bond control for TC-CUF.

which subsequently tightens tolerances for coplanarity mismatch. There is a special approach to establish high coplanarity between bond head and stage. The approach (**Figure 5**) uses a pendulum-based bond head shaft with a pivot point at the top. The pendulum tilt is controlled by two orthogonally arranged microactuators that allow tilt adjustment in the range of $\pm 1\mu\text{m}$ @ 10mm in any direction. This mechanism also allows active tilt compensation, although this capability is beyond the current scope [2].

The real challenge is to maintain coplanarity integrity, i.e., to maintain coplanarity especially during transient thermal phases. In **Figure 6**, the bottom left diagram shows loss of coplanarity integrity during temperature ramping. The green plots are traces of four corner z-positions during a $300^\circ\text{C}/\text{s}$ ramp. Subtracting the z-plots from the average leads to insufficient z-residuals, which should stay within $\pm 1\mu\text{m}$ @ 10mm tolerance for through-silicon via (TSV) memory production. Reasons for a lack of coplanarity integrity can be asymmetric hardware design, as well as asymmetric air flows that cause differential thermal effects. The bottom right diagram of **Figure 6** shows a well-designed system being able to stay within required coplanarity specifications.

Bond control

As mentioned in the introduction, bond control is simple for TC-processes based on nonconductive paste and nonconductive film (TC-NCP and TC-NCF) where epoxy in the bond line gets sufficiently rigid during the ongoing curing process in order to prevent solder joint collapse when solder starts melting. As a consequence, bond

control does not have to consider potential collapse. This is not the case, however, for a TC process based on capillary underfill (TC-CUF), where sophisticated hybrid bond control needs to be considered to achieve a typical bond line thickness of $\pm 1\mu\text{m}$. The time plots of temperature, bond force and z-position for a representative TC-CUF process are shown in **Figure 7**.

The term hybrid refers to the necessity of bond control being partly in force control and position control mode. As shown in **Figure 7**, z-position control is sophisticated, as it has to incorporate three tasks: 1) kinematic compensation, 2) thermal expansion compensation, and 3) solder joint formation.

The z-movement behavior of the bond head is well-described by the metaphor of a “turbulent airplane ride,” so let us “fasten our seat belts” and join this “turbulent airplane ride.” It starts in force control mode with bond force being ramped rapidly to a high value in order to coin bumps for compensation of small bump height variations and coplanarity mismatches, thereby achieving well-defined thermal contact between die and substrate. In direct correlation with raising bond force, the z-position sinks rapidly down (“our airplane passes through the first turbulence”). This rapid z-movement is called the kinematic reaction (**Figure 7**) according to compression of an elastic stack comprising machine parts, substrate and bumped die.

After a small delay (which might be zero), temperature ramping is started concurrently. Because temperature increase induces a thermal expansion of machine parts, bumped die and substrate, the bond head position needs to lift accordingly (**Figure 7**, thermal compensation), otherwise bond force would

increase. This thermal expansion effect, however, will imply an automatic upward move of the bond head caused by the feedback loop-based force controller, in order to keep the bond force at a constant level.

As bond head temperature further increases and the interface temperature approaches the melting point, our “airplane ride” is facing a critical phase. To avoid solder joint collapse during solder liquification, we need to prepare a switch of force control to position control in order to perform so-called kinematic compensation, a rapid upward movement of the bond head during bond force breakdown (“our airplane rides through the next turbulence” – see **Figure 7**).

Why is a suitable kinematic compensation so important? Remember that by raising bond force, an elastic stack has been compressed. By reaching the solder melting temperature, the compressed elastic stack will relax, causing a rapid upward movement of the substrate’s z-position. If the bond head (and die) would not concurrently rise, the solder joint would be smashed, thereby bringing with it the danger of solder bridges, solder climbing and “squishes,” as explained in the introduction.

Kinematic compensation, however, is not the only thing with which we have to be concerned. Because temperature is still in transient behavior and thermal expansion effects are progressing, there needs to be compensation, which is accomplished by additional z-movement (thermal compensation – see **Figure 7**) on top of kinematic compensation. In order to get a clearer picture of the situation, the actual bond head position (p-position – in **Figure 7**) is decomposed into a sum of two position signals, the first one representing kinematic compensation and solder joint formation (denoted as “w-position” in **Figure 8**), and the second representing the thermal compensation movements (denoted as “z-position” in **Figure 8**). In **Figure 8**, The separate contributions of kinematic and thermal compensation can now easily be studied.

After mastering the “upward turbulence” by performing the kinematic compensation, one should realize that the solder height is still maintained at the coining level (same as it was immediately after application of the bond force ramp). For a reliable solder joint, however, the solder height needs to be lowered to a suitable level. This is done with a slow ramp lowering the w-position signal (**Figure 8** – labeled as “ $-7\mu\text{m}$ @ 2s”). At the end of this solder joint formation ramp, the w-position stays at (constant) target level. This requirement will

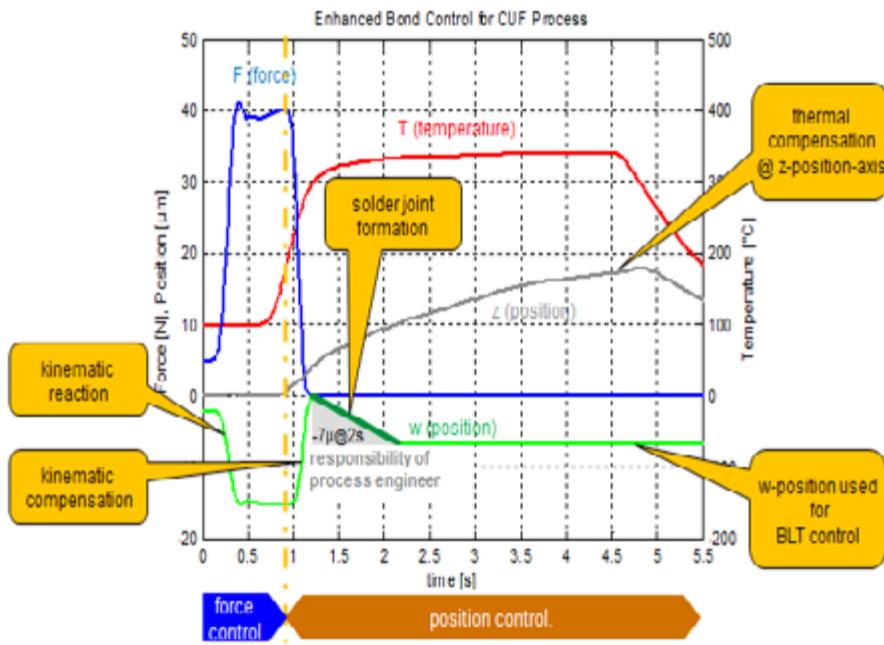


Figure 8: Hybrid bond control for TC-CUF by decomposing bond head position $p = z + w$.

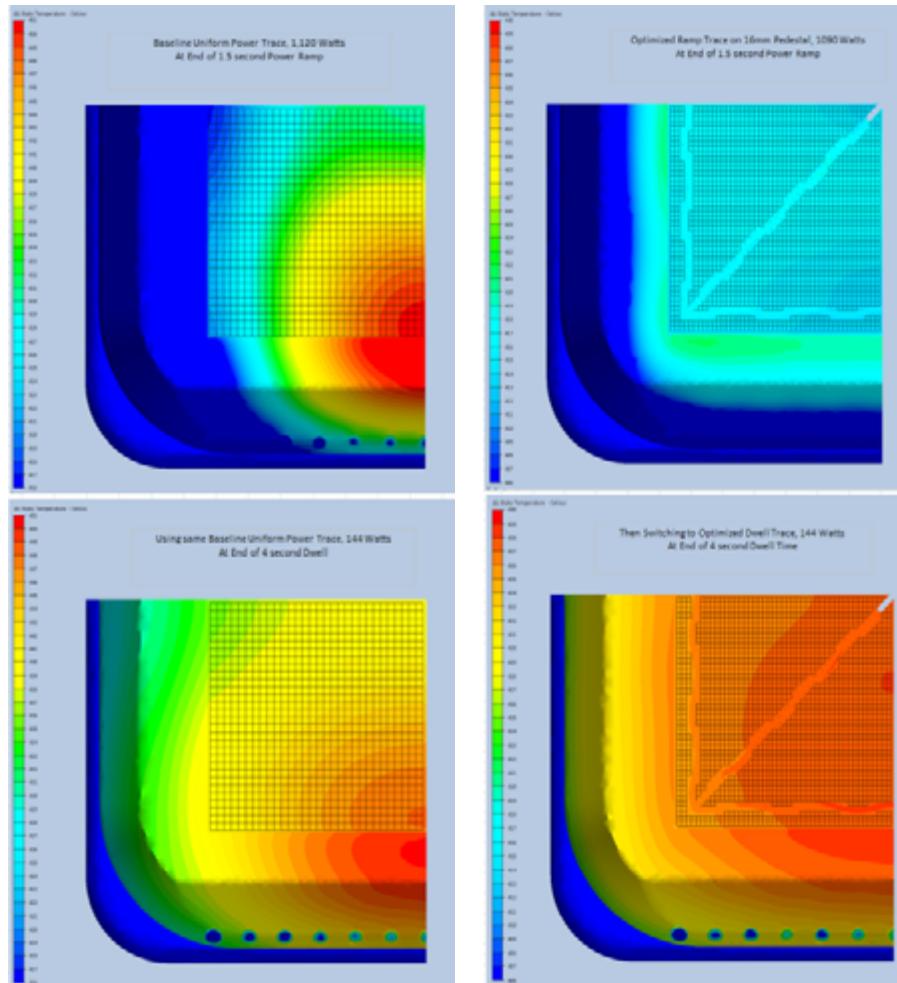


Figure 9: Temperature distribution of a non-optimized (left) versus an optimized tool design (right).

only be fulfilled, if in parallel, the z-position signal is adopted according to a proper compensation of the thermal expansion, until the TC bonding phase has been completed, and the bond head releases the die.

A TC bonder can learn kinematic and thermal compensation properly by running an automatic identification procedure. The only phase that needs intervention of a process engineer is the solder formation phase comprising two values: ramp height and ramp duration. A sophisticated position profile for a TC-CUF process is thereby reduced to essentially two values, because the rest can be automatically identified by the machine.

Where are now the challenges of bond control? Challenges are moderate in the first phase with feedback control-based force control, sensing the bond force with a force sensor integrated into the bond head. The real challenges are related to position control because of the difficulties of distance sensing between the die and the substrate surface, and this is exactly the reason why current TC bonders are running the complete second phase of the bond profile on the basis of a memorized behavior. It should be emphasized that full bond control in position control mode is based on a feed-forward principle, not making use of sensing any actual behavior. As a consequence, this approach requires a very high repeatability of all process variables concerning tight tolerance windows, but also precise timing.

Finally, the question arises why so much attention is payed to TC-CUF, even if TC-NCF will most likely replace TC-CUF. There is one aspect that has not been highlighted so far: we claimed that the bond profile for either TC-NCP or TC-NCF is defined with the goal that epoxy is already cured and rigid—when the interface temperature reaches the melting point. This is one possible way to run the process. An alternative would be to run those processes with hybrid bond control (making the “turbulent air plane ride”). This approach would benefit higher productivity because bond control does not have to wait for sufficiently cured NCP/NCF before starting solder reflow.

Temperature uniformity

Excellent temperature uniformity is required to guarantee a stable and robust TC bonding process. First, having good temperature uniformity ensures that all bumps are exposed to the same temperature profile, and therefore, all the joints are formed in a repeatable manner.

This allows for better joint formation and also improves reliability by avoiding cold joint creation or excessive intermetallic compound (IMC) formation as a result of large localized temperature excursions.

Second, lack of temperature uniformity can also result in lower process throughput. Typically, temperature nonuniformity can be compensated by increasing the process dwell time to allow the tool temperature to homogenize. However, this can result in excessively long process times, which are undesired from a throughput perspective. Furthermore, long dwell times also leave the solder in a liquid state for a longer time, which further promotes IMC growth.

The key challenge from an equipment supplier point of view is the ability to deliver a heated tool that is able to ramp up and down at very high rates, while at the same time being able to minimize temperature nonuniformity. **Figure 9** shows simulations that have been performed for various tool designs. The image on the left of **Figure 9** shows the temperature distribution of a tool with non-optimized heater design. In this case, the tool temperature uniformity was within $\pm 15^\circ\text{C}$ at the end of the transient phase, and $\pm 12^\circ\text{C}$ after a 3s dwell time—too large values, not sufficient to guarantee good and stable reflow conditions at all bump locations on the chip.

The heating structures have then been modified in order to provide much better temperature uniformity (**Figure 9** right). In this case, the heated tool was equipped with multiple heating elements being regulated by more sophisticated control. With this optimized design, the tool was significantly improved with the temperature distribution being brought within $\pm 1.5^\circ\text{C}$ at the end of the transient phase, and $\pm 1.0^\circ\text{C}$ after 3s dwell time. These results have also been verified on actual tools. **Figure 10** shows infrared images of tools whose temperatures were measured after a 1s dwell time following the heating ramp. The top image shows a tool on base of the non-optimized design with a temperature distribution of $\pm 15^\circ\text{C}$, while the bottom image shows a tool utilizing an optimized design with a temperature distribution of $\pm 1.5^\circ\text{C}$.

Summary

TC bonding is a key technology for current 2.5D/3D chip-to-substrate (C2S) and C2W packaging, and there

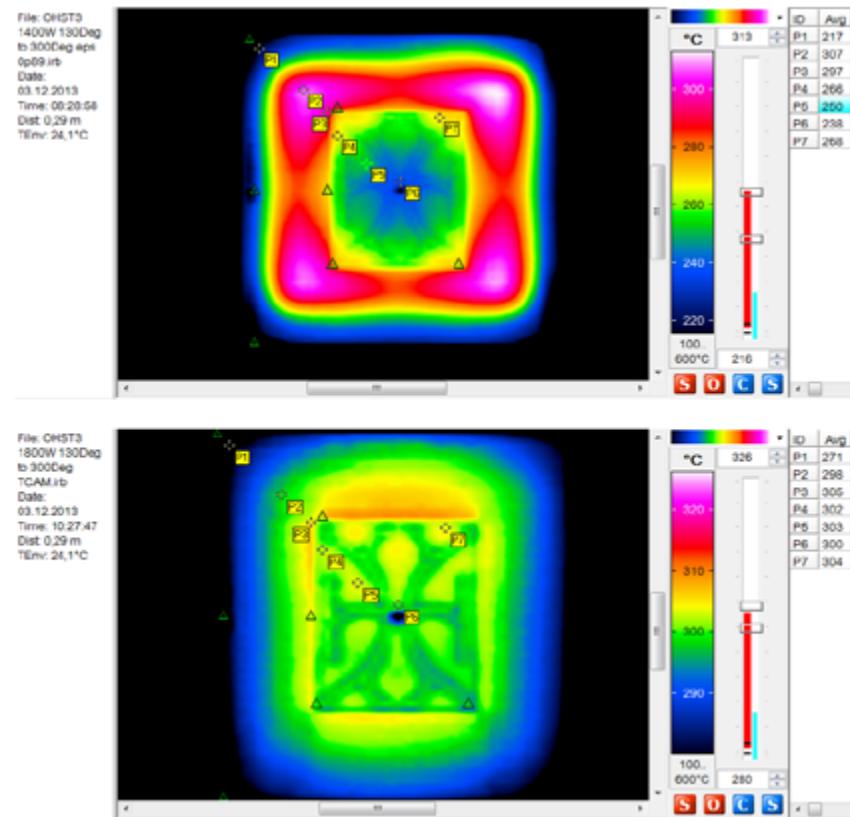


Figure 10: Actual temperature distribution measurement of a non-optimized tool design (top) versus an optimized tool design (bottom).

are mainly three different process flows. Because heterogeneous integration roadmaps are demanding mid-term pitch scaling of a factor five to ten for 3D-SICs (system-in-chips) and 3D-SoCs (system-on-chips), the challenges of TCB core capability improvement have been studied. While the complexity of TC-CUF bond control might vanish by moving to a TC-NCF process, the remaining core capabilities of accuracy, coplanarity and temperature uniformity are facing major challenges due to rapid temperature ramping demands.

Replacing TC bonding technology by a highly productive two-step bonding process based on high-accuracy tacking at constant temperature with subsequent annealing to form the final interconnection, as it is seen with hybrid bonding processes, would work around the major obstacles associated with the rapid temperature ramping requirements of a high productivity TC bonding process.

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Biographies

Hugo Pristauz received his PhD in Control Engineering at the Technical U. of Graz and is VP Technical Development Advanced Technology DA at Besi Austria GmbH; email hugo.pristauz@besi.com

Alastair Attard has a Bachelors degree in Mechanical Engineering and received an MBA from the U. of Malta; he is Manager, Process Development at Besi Austria GmbH.

Andreas Mayr received his Bachelor of Industrial Engineering at the Technical U. of Graz and is a Director, Technical Program Management at Besi Austria GmbH.

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SUSS MicroTec SE Schleißheimer Straße 90 85748 Garching Germany Tel: +49 89 32007 0 Fax: +49 89 32007 162 www.suss.com	 Permanent wafer bonders Temporary wafer bonders Debonders	Mask aligner, coater/developer, projection scanner, laser ablation stepper, nanoprint equipment, photomask cleaning equipment
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Testing of automotive electronic ICs

By Davide Appello *[STMicroelectronics]*

In the five years since my previous editorial contribution [1], the most consolidated applications segments existing at that time evolved without major discontinuities with respect to the offered performances. Key trends identified, such as functional safety and security, took place, thereby definitively setting new standards and methods. In contrast, new applications driven by the booming advanced driver assistance systems (ADAS) segment require disruptive changes in some of the traditional automotive paradigms. This paper provides more details about the key factors driving the various application segments and also analyzes the consequences of the front-end and back-end technologies necessary to accomplish the relevant objectives, as well as on the tools and methods needed to effectively test ICs.

Key factors

With respect to automotive electronics, and more specifically of ICs developed for automotive applications, we have often reported as key factors and keyword attributes such as quality, extended temperature range and lifecycle duration, burn-in, robust design, and design for reliability. **Figure 1** qualitatively shows the incidence of the cost of electronics with respect to the overall value of a car throughout the years. To project the number of components and overall number of applications in the car, the reader should also consider the significant reduction of application service providers (ASPs) per IC year over year as a natural consequence of increases in volume.

The increasing quality requirements, which translated into longer test times and multi-temperature coverage, determined the need for countermeasures to reduce costs as well as the cost of test (CoT). Because of this need, automotive testing adopted several test cost reduction methods from other market segments; these methods were used to push development of more advanced technology despite being at a lower level of maturity. Very high parallelism probing is one example, accompanied by high multi-site testing at the package level. This forced the development of customized ATE cells offering relevant

instrumentation and configuration options.

Additionally, a great deal of effort has been spent to improve design for testability (DFT) by pushing on few key techniques such as memory built-in self-test (BIST), limited pin count test ports, compression, and more recently, logic BIST. DFT methods have been challenged not just to achieve very high coverage indexes, but also to offer diagnostic capabilities to enable high accuracy and resolution diagnostics for reliability learning.

Progress doesn't end here and indeed, as has happened several times in this field, we have signals showing radical changes in past paradigms. To be more specific, the requirements are not changing, instead, they are advancing relentlessly and without major gaps.

Table 1 gives the time horizon for these changes in requirements. The most relevant and potentially disruptive changes concern the conditions in which requirements can be satisfied. Many of the methods used with a good degree of success in the past, appear to be no longer sufficient to meet the goal. Let's review how and why.

Applications

The following quote from [2] succinctly summarizes what has happened in the last few years: "The auto industry is lost in translation between evolutionary, revolutionary and disruptive key trends that all need to be managed at the same time." Some of the applications followed an evolutionary path (see **Figure 2**). Powertrain, braking, and transmission applications evolved

seamlessly—progressively integrating new features mainly driven by safety and security requirements. These features are not major performance-eaters and are instead leveraging robust development methods, verification, and traceability. Quality and reliability performances demand, increased despite starting from already severe conditions.

Body and dashboard applications,

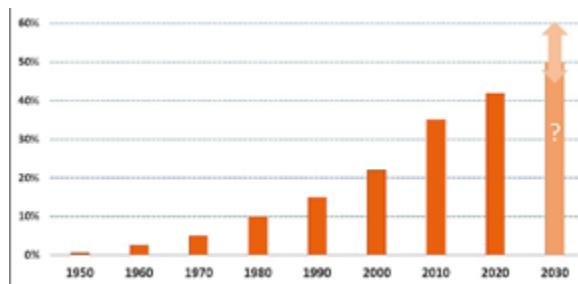


Figure 1: Electronic content in the car.

IC characteristics trend: how these features will impact test requirements

Node	Unit	50nm	65nm	40nm	28nm	16nm	7nm
Power	W	1	2	3	6	8	15
Speed	MHz	200	250	350	1000	1600	2400
Dominant Package type		QFP	QFP	BGA	FCBGA	FCBGA	FCBGA
Dominant Pad technology		AI Pad	AI Pad	AI Pad	SB/CP	SB/CP	SB/CP
(Package Rev'd) Test complexity index*		1	2	2	5	6	7

* Qualitative, considers signal count, bonding technology, materials, mission profile

Table 1: IC characteristics trend: how these features will impact test requirements.

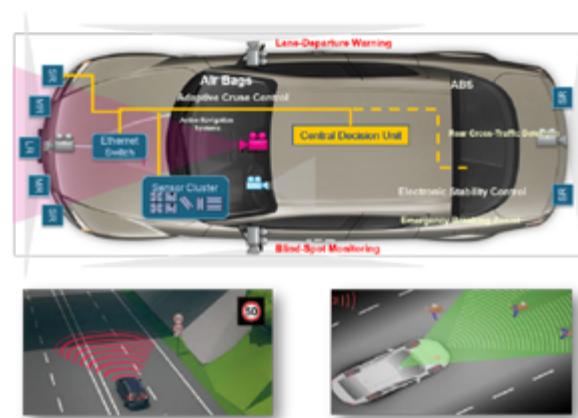


Figure 2: ADAS applications.

entertainment, positioning and radar products for active safety, however, can be categorized as revolutionary for different and multiple reasons. The exponentially increasing number of ICs on board necessarily pushed the price down in some cases. On the other hand, the integration in the dashboard raised the quality requirements to a level closer to under-the-hood applications. Many of these ICs were inherited from consumer domains and non-negligible efforts are expended to make them fit the new style. Finally, millimeter-wave applications and some high-speed link intellectual property (IP) have been integrated into ICs.

Autonomous driving and all ICs supporting such functions (e.g., vision and object recognition, car connectivity, in-car high-speed link) are also revolutionary and are breaking old paradigms (see **Figure 3**). Effects on front-end and back-end technologies adoption will be discussed in the next chapters. These effects have been driven by the characteristics of the IP integrated into these ICs. Multi-core processors running at GHz frequencies to deliver enough computation power, high-speed interfaces to link with memories and surrounding ICs and sensors. But even more relevant, we adopted the most updated versions of these IPs, often before their adoption in some of the consumer/mobile applications.

Adoption of new technology nodes

For many of the ADAS applications, the automotive industry has de facto abandoned a traditional approach to the adoption of new technologies. Until recently, a new technology platform (e.g., foundations and IPs) had been adopted for developing automotive products after having already been used to manufacture high volumes for other market segments. ADAS required breaking this rule because the performance requirements demanded it and the development pace for new applications could not withstand that rule.

The situation discussed above posed several new challenges [3]. Testing and testability are on the critical path of these challenges. The sensitivity to reliability fails requires a statistical visibility of parts per million (PPM). The electrical detection of reliability-dependent failure modes happens concurrently with the detection of t0 fails, driven mostly by defectivity. In the case of new product introduction (NPI) (e.g., on the new technology of early adoption), it is very common to be at the beginning of the yield learning curve, where reliability fail signatures may alias with t0 fails.

Figure 4 shows the typical defectivity learning profile

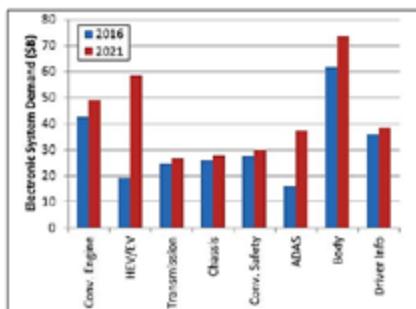


Figure 3: Booming market segments.

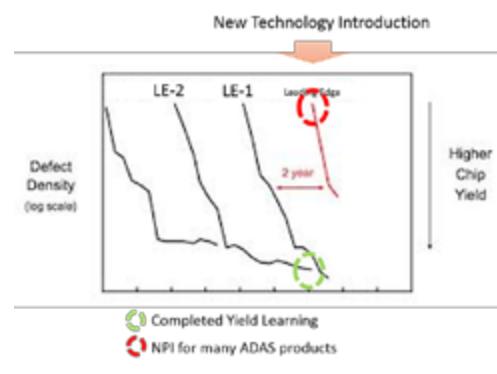
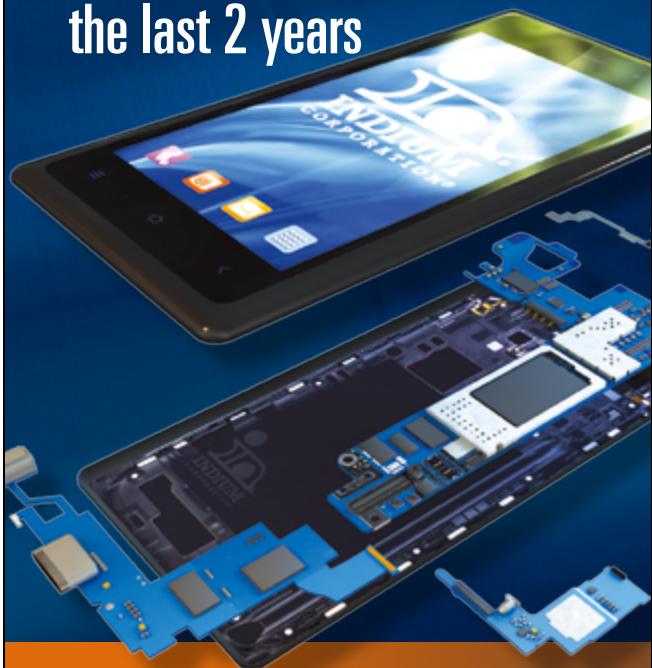


Figure 4: NPI vs. fab defect density.

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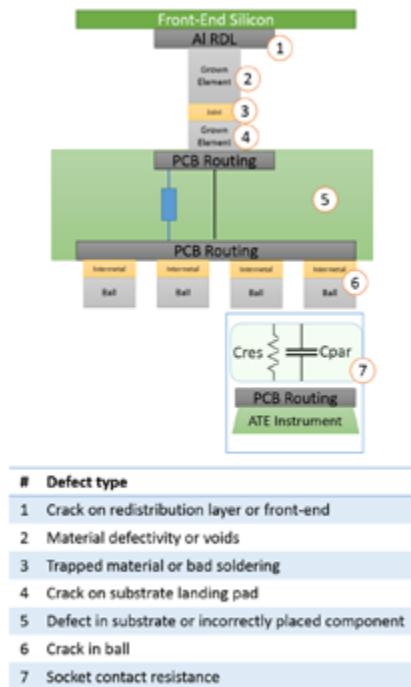


Figure 5: A simplified construction analysis of a flip-chip BGA package.

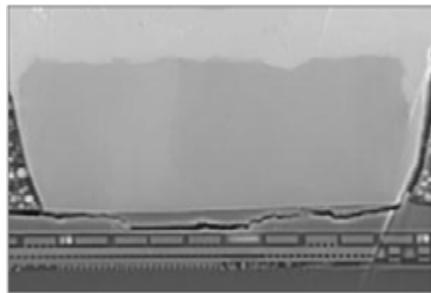


Figure 6: Crack detected on a copper pillar after thermal cycling.

in the fab and highlights a typical ADAS development case compared with a more traditional development condition for automotive applications.

Back-end technology (assembly)

The test industry often linked package test step requirements such as multi-temperature testing and contacting technologies. Similarly, the wide array of literature on testing and testability occasionally described the problem of detecting defectivity introduced at back-end manufacturing. In the majority of cases, the modeling of defects adopted a simple taxonomy. T0 defect detection was possible with simple bonding integrity testing and through the observation of drifts measured through parametric tests. Other defects that are non-detectable electrically should be eradicated through

manufacturing process improvements. This approach is turning to be critical for many reasons that are outlined below.

Technological features. The following have been utilized: multi-die/stacked dies, passive components on substrate, fine-pitch bumps, multilayer substrates, multitude of materials (substrates, lids, molding and filling compounds, silicon, bumps).

Back-end assembly thermomechanical sensitivity. The material stack and the thousands of electrical joints determined at the assembly, are sensitive to the thermomechanical stress applied during testing, during soldering reflow, and finally by the thermal cycles determined by application activity. A specific consideration should be taken for products targeted to segments such as automotive, with demanding requirements with respect to extended temperature ranges.

Product sensitivity. The progressive adoption of high-speed interfaces increases the sensitivity on small impedance variations of signal and power/ground paths.

Test sensitivity of package electrical performance variations. The sensitivity of small impedance variations available during test is limited by some intrinsic characteristics such as socket and PCB load-board track lengths. An interesting exercise is to review the possible defectivity sources of a package implementation, which is utilized by a device whose electrical performance has high sensitivity to even small impedance variations. **Figure 5** shows a simplified construction analysis of a flip-chip ball grid array (BGA) package. Each of the identified potential defects may contribute to a change in the impedance network going from silicon to the package ball. The detection of such an impedance change requires the detection through an ATE and a board and a socket into which the device is placed during test.

Unfortunately, the task outlined above is limited by the contact resistance offered by the socket elements. In **Figure 6**, the reader will find the schematic of the equivalent circuit shown in **Figure 5**. From that and from the value of the described component, the detection challenge is evident. Because these defects might also arise from thermomechanical stress, they can be of an intermittent nature [4]. This complicates the requirements for their detection and, as a consequence, the possibility of testability intervention.

Testability, tolerance and reliability

The introduction of testability, which looks at package defectivity, implies the inclusion

of more activation factors. Mechanical effects become very relevant, together with thermal effects. The utilization of different material types in packages leads to increased sensitivity on material deformation under thermal cycling, which determines mechanical stresses. These types of phenomena and conditions pervade the entire manufacturing process. The assembly step itself manages pressure and temperature to determine electrical connectivity between the different elements. During end-of-line testing, the ICs are soaked at the test temperature and concurrently plunged to achieve adequate electrical contact. After that, the soldering reflow process applies a thermal stress with extreme conditions. Finally, because of power consumption and operating environment, the IC undergoes a number of thermal cycles during the operative life in the application.

The modelling of these stresses is not trivial. An incorrect evaluation of the phenomena may lead to inadequate reliability assessments that are not effectively activating the relevant defect mechanisms [5]. At the same time, the activated mechanisms can be difficult to detect because it might not be possible to recreate all the required conditions or to achieve the needed statistical visibility. Reference [6] reports results of the study performed on a defectivity type activated by thermal cycles. **Figure 6** shows the effects of thermal cycles applied to a copper pillar structure. Cracks leading to connectivity failures were induced by the stress, requiring process improvements to match with the application mission profile.

The kind of failure mode described above opens up very interesting considerations and needs. The reader may easily recognize how the crack shown in **Figure 6** is very subtle in nature. Very often, this type of phenomenon is associated with intermittency of the connectivity depending on the pressure that is locally applied. Pressure is thereafter linked to temperature and to the thermal deformation coefficient of the involved materials. The detection of this failure mode through electrical tests can be very tricky as it may imply repetitive signals, long signal evaluation time, and a high signal-to-noise (SNR) ratio. Despite the fact that the literature in this field is very limited, some examples exist to explain the possible solutions that are intended to improve detection. Reference [7] describes the characteristics of an intellectual property (IP) that has been useful to activate intermittent defects in combination with automated test

equipment (ATE) methods. Beyond end-of-line testing, devices developed for safety applications demand additional capabilities. Some of the package features are necessarily a part of the safety-critical IP of an IC and of the entire system.

Based on the above discussion and along with the recommendations and requirements of the related standard ISO 26262 [8], the IC developer will have two possible directions. In one case, it will be adding redundancy to protect from the evaluated FIT rate. This approach, especially at the package level, may lead to a serious impact on cost. A more tricky and challenging option, however, concerns the detection and diagnosis of performance drifts critical for safety. The detection of drift impacting the package feature may necessarily lead to the need to extend the reciprocal awareness of safety requirements to the interconnected IC on the application board.

Summary

New automotive applications are driving not just the adoption of advanced front-end technologies, but also, packaging technologies are being pushed forward as ever more complex and well-performing package solutions are adopted. This trend puts serious challenges with respect to reliability and quality of the whole IC. This paper provided examples of how the fault induction and design for testability can be extended from the front-end silicon to the package. Similarly, an exhaustive review of functional safety will address the hazards present in the package and define suitable countermeasures for redundancy, repair and/or tolerance.

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Biography

Davide Appello received his laurea in Electronic Engineering at the U. of Pavia in Italy and is Director of Product Engineering for the automotive digital division at STMicroelectronics; email davide.appello@st.com

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Optimization of speed and accuracy for fan-out die placement

By Tom Strothmann *[Kulicke & Soffa]*

Fan-out processes represent the fastest growing segment of electronics packaging market with a projected compound annual growth rate (CAGR) of nearly 50% for the period of 2016 through 2020. The rapid increase in volume has primarily been driven by the mobile space where fan-out packages offer the most compact form factor and low cost. One of the key enabling technologies for fan out is the die placement process, however die placement requirements for fan-out wafer-level packaging vary widely based on the process flow selected. Fan-out process flows can require die placement to be done face up or face down and alignment schemes for die placement can include global alignment, local alignment, or a combination of both methods. In some flows, heat may be required for the carrier or the die and placement force must be carefully controlled. Each process flow has attributes that define the challenges and requirements for die placement conditions, but machines with heat, force and local align capability have higher cost and lower units per hour (UPH). These factors contribute to a higher depreciated cost applied to each unit produced, as well as a higher initial capital cost, and must be considered when selecting the best fan-out flow for a given product.

Accuracy requirements are driven by the photolithography steps done after reconstitution and steppers are commonly used with the assumption that die-to-die spacing is repeatable within a given field area. Die spacing will inevitably be somewhat irregular on account of normal process variation in the placement and reconstitution processes, although variability can be reduced with the proper selection of placement equipment and molding materials. Die placement accuracy in conjunction with die shift during the reconstitution process must accommodate the design rules for redistribution layer (RDL) via size, passivation opening size, and pad pitch for the intended devices. The selection of die

placement equipment is important because equipment optimized for the best accuracy may not have the highest UPH. This trade-off between speed and accuracy should be considered in the selection of the fan-out process to ensure the final product can be produced with the most competitive cost. It is important for manufacturers to understand the interaction of these factors in the selection and optimization of their fan-out process flows because the choice of the process flow imposes constraints that affect the final cost of the die placement process.

FOWLP standard process flows

Three basic process flows have emerged in the industry. The diagram in **Figure 1** graphically represents the options in high-volume manufacturing (HVM) today and some of the die placement requirements for each. Although the TSMC integrated fan-out (InFO) flow has garnered the most attention recently, the embedded wafer-level ball grid array (eWLB) process flow licensed by Infineon has by far the highest volume in production today. The eWLB process flow is currently offered by STATS ChipPAC, ASE, and NANUM S.A. (now Amkor Technology). The products using the eWLB process flow are typically single-die products with low I/O counts such as PMICS, audio codecs, and RF. These “low density” products represent about 75% of the total fan-out wafer-level packaging (FOWLP) volume and that percentage is expected to remain relatively stable as volumes increase through 2020. The three standard fan-out process flows supporting these options are shown in **Figure 2**.

Die placement accuracy and alignment schemes

The two alignment methods used for die placement in fan-out processes are global alignment and local alignment. For global alignment, all die are aligned to a common Cartesian reference frame determined by two or more global fiducials placed on the edge of the carrier. Global alignment provides the fastest die placement and therefore the lowest cost. This method typically requires careful mapping of machine axes to ensure accuracy is maintained over the full work area. Accuracy achieved with this method is typically limited to 5µm for the highest speeds. Global alignment is predominantly used in the eWLB process flow with face-down chip-first placement, but it can be used in other flows as well. Global alignment is depicted in **Figure 3** where a carrier is shown with placed die and global fiducials.



Figure 1: HVM FOWLP process options.

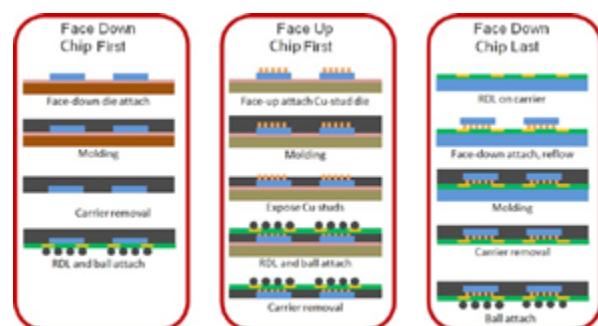


Figure 2: Standard process flows for FOWLP.

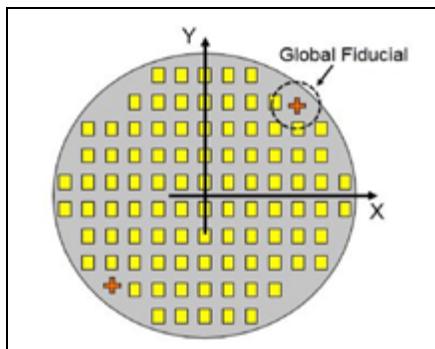


Figure 3: Global alignment fiducials.

Local alignment is slower, but is able to achieve much higher accuracy. With local alignment, each die is individually aligned to local fiducials at the location where the die is placed. This alignment method does not need the machine mapping and characterization required for global alignments. The alignment method also enables very high accuracy thermocompression bonding (TCB) die alignment and accuracy of 1.5-2.0 μm is possible, however at the high speeds required for fan-out placement, 3 μm is more typical. Local alignment fiducials at each die location on a carrier are depicted in **Figure 4**.

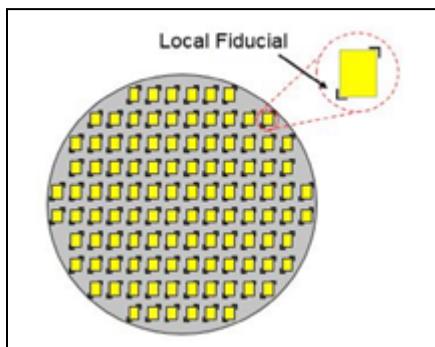


Figure 4: Local fiducials.

There is another method possible for face-down global alignment schemes where RDL layers require accurate alignment in multi-die applications. A method for more accurate alignment of "B" die to "A" die is shown in **Figure 5**. Using global alignment for both "A" and "B" would roughly increase "A" to "B" placement error by $\pm 4\text{-}7\mu\text{m}$. Better die-to-die placement accuracy to support the multi-die RDL connections can be achieved if "A" die can be placed globally and "B" die can be placed locally, relative to "A" die. In this

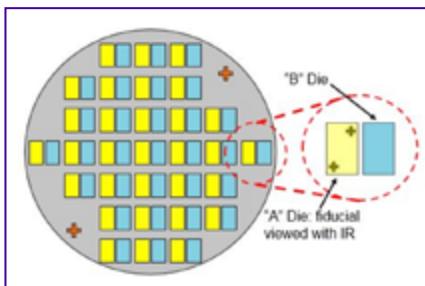


Figure 5: Method for multi-die alignment.

example, accuracy is limited if aligning to the backside of "A" due to the 3-5 μm variation in the dicing cut relative to the active die edge. An alternative method is to use an infrared (IR) camera to look through "A" die to detect die fiducials on the front of the die. The result is more accurate die "B" to die "A" alignment, however the local alignment method for "B" die will impose a lower UPH than can be realized with just global alignment.



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Accuracy challenges with fan-out die placement

Die that are initially placed accurately for a fan-out process have the potential to shift position during the reconstitution process due to several competing factors. In a round format, this shift is typically a radial function from the center to the edge of the carrier as shown in **Figure 6**. As the carrier heats up during the reconstitution molding process, it will expand and affect the relative die position. Carrier material must be selected carefully to minimize the effect. A 300mm

silicon carrier with a coefficient of thermal expansion (CTE) of 3ppm/ $^{\circ}\text{C}$ will shift the outer die position by 37.5 μm if the carrier is heated to 100 $^{\circ}\text{C}$. If a stainless steel carrier is used with a CTE of 17ppm/ $^{\circ}\text{C}$, a 50 $^{\circ}\text{C}$ carrier temperature will shift the radial position by 190 μm . Carrier temperature in the machine must be controlled to support consistent carrier expansion performance during die placement. Thermal expansion of the carrier material during molding must also be characterized and combined with shrinkage of the mold compound during cooling to accurately predict final die position. Selecting materials to minimize these effects will substantially reduce the final variation in die position. Considering these factors, die placed with an accuracy of 3-5 μm may have final position variation of 7-10 μm after reconstitution molding. Most eWLB product designs will have acceptable yield variation if the final die position is <10 μm .

Face-down chip-first process flow requirements

Face-down, die-first process flows used for eWLB and similar processes represent the highest volume and most widely used group of fan-out technologies in production today (**Table 1**). This process group places the die face down onto an adhesive surface during the reconstitution process and may achieve high yield for the intended products with a die position accuracy just under 10 μm after reconstitution.

Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Alignment	Die Value	Typical Flow	Applications
>10k	Face Down	low	low	< 5N	No	Global/ Local	Low	eWLB	Baseband, Power Mgmt, RF, Analog, BT

Table 1: Critical requirements for a face-down chip-first process flow.

A round carrier is used today with a maximum diameter of about 330mm. The process flow is typically used for single-die products with lower I/O counts designed into mobile applications including audio codecs, power management, baseband processors, RF analog and Bluetooth®. The process flow is also a good choice for Internet of Things (IoT) and system-in-package (SiP) low-cost products. Very high-speed placement is required for the process to ensure the lowest cost, and the larger passivation opening size used on the products enables a lower accuracy requirement. Key requirements for die placement in this process include very high speed, face-down placement, no die heat, no carrier heat, and low placement force. Because each die is placed face down on adhesive applied to a carrier that is common to all products, there are no local fiducials for pattern alignment. Global alignment schemes are used to place the die onto the carrier in a virtual Cartesian matrix that is referenced to global fiducials placed at the perimeter of the carrier. Although the flow is most commonly used for single-die products, it can also be used for multi-die products with a few products requiring higher placement accuracy extending down to 3-5 μm . These multi-die applications may also require higher relative placement accuracy where the position of the second die is judged relative to the first die placed.

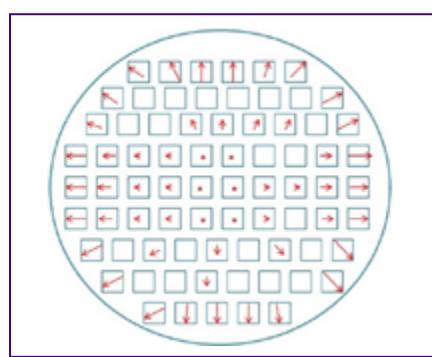


Figure 6: Radial expansion of carriers.

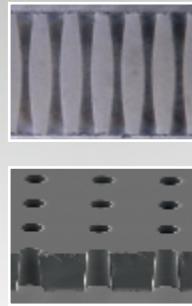
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The capability for placement of passive components prior to reconstitution is useful to enable some SiP and IoT products. Given the low cost of the final product, UPH of the placement process is the key attribute for this process flow to enable cost reduction and a UPH of more than 10k is desired for a competitive process. Placement force in the process must be well-controlled to avoid the die embedding too deeply in the adhesive material, with a resultant step formation at the die edge during the molding process. Die shift after placement is driven by previously discussed factors including composition of the carrier material and the mold compound shrinkage during cure. If die shift is well-characterized, the die placement position can be adjusted by the equipment to compensate for the anticipated shift in position. To enable the most repeatable process, the temperature of the chuck is typically held at a high ambient set point to ensure repeatability.

Face-up process flow requirements

Face-up process flows are used for TSMC InFO and similar processes (**Table 2**). These process flows can be used for high-value die requiring fine line and space and pad pitch. The process flow can support both 2.5D and 3D process options and has received much attention for its use in packaging Apple A10 processors. There are several variations of the process from different suppliers that combine carrier or die heat up to 150°C and force up to 100N. The use of heat and higher force can fix the die position to have very little movement during the reconstitution process, but the longer process time comes at the expense of reduced UPH and higher cost.

2.5D versions of this process flow typically use global alignment schemes, whereas 3D versions of the process flow create an RDL layer and Cu pillars prior to die placement, and may require local alignment. High-accuracy placement is used for all versions of the process flow and accuracy requirements of 3µm are typical. Round carriers are typically used with a standard diameter of 300mm. The process flow is well-suited for high-value die requiring fine-pitch and multi-level RDL because die shift is well-controlled. The key requirements for this process include high accuracy, moderate speed, face-up placement, die and/or carrier heat and controlled placement force up to 100N. Typical products are high-density products with higher I/O counts and can include application processors, memory or multi-die products with silicon partitioning. Accuracy of the placement process is a key attribute to ensure high yield with fine line and space RDL and a UPH value between 4-6k is currently possible.

Face-down chip-last process flow requirements

Face-down, RDL first process flows used for Amkor's Silicon Wafer Integrated Fan-out Technology (SWIFT®) and similar processes represent the most recent addition to the portfolio of fan-out process flows (**Table 3**). It is a unique process in that it uses a conventional Cu pillar bump structure formed on the die prior to the fan-out process. This process flow places the die face down on a pre-formed redistribution layer on a temporary carrier and typically uses a local or mass reflow process to form the required interconnect metallurgy. Underfill is used prior to reconstitution to secure the die position and protect the interface. Round carriers are used today with a standard diameter of 300mm. Once die placement and reflow is finished, the die is underfilled and molding is completed. The temporary carrier is then removed and solder balls are attached.

The process flow is a good choice for high-value die requiring fine-pitch and multi-level RDL with high yield because it is a chip-last process. The key requirements for this process include: high accuracy, moderate speed, face-down placement, flux dip, low die heat, low carrier heat, and low placement force. Local alignment schemes are used to accurately place the die on a carrier with 3-5µm accuracy. The process is well-suited for high-value die or high-density interconnect multi-die products. Typical products have higher I/O counts and can include application processors, memory or multi-die products with silicon partitioning. Accuracy of the placement process is the key attribute to ensure high yield and a UPH of 4-6k is currently available.

Consideration of product requirements

Value of the die to be placed is one of the key considerations in choosing a fan-out process flow. If the value of the die is high, it is preferable to ensure the RDL processing has been successfully completed prior to die placement. This favors a chip-last process or a process where die shift has been minimized and is well-characterized. From an equipment perspective, high-accuracy placement can be achieved with single- or multi-head systems placing one die at a time, and die with high-density

Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Align	Die Value	Typical Flow	Applications
>5k	Face Up	<150C	<150C	<100N	No	Local / Global	High	InFO Like	Mobile application processors

Table 2: Critical requirements for a face-up chip-first process flow.

Speed UPH	Face Up / Face Down	Die Heat	Carrier Heat	Place Force	Flux Dip	Alignment	Die Value	Typical Flow	Applications
>6k	Face Down	No	No	< 10N	Yes	Local / Global	High	SWIFT Like	Mobile application processors, DRAM

Table 3: Critical requirements for a face-down chip-last process flow.

I/O can use die placement with either local or global alignment schemes. For the lowest manufacturing cost, the eWLB process flow should be selected if the product design can tolerate the lower accuracy constraints. High-value die are not good candidates for chip-first processes like eWLB. With this consideration in mind, it is important to realize the chip-last fan-out processes are also the most expensive. When choosing a fan-out flow for the lowest cost, a decision must be made at the start for the accuracy that is required for the intended product. As is common in all die placement machines, accuracy is directly related to the placement speed and consequent cost.

The advertisement features the TTS logo and website (www.tts-grp.com) in the top left corner. The main headline reads "CMOS Socket Testing for Image Sensor". Below the headline are two images of a CMOS socket: a front view showing a green PCB with a central cavity and a back view showing the underside with mounting holes. At the bottom, the text "Test Tooling Solutions Group" is displayed over a stylized green circuit board graphic.

Panel or round format for fan-out processes

Wafer-level fan-out dominates processes today and high-volume panel processing continues to be at least two years out. Panel size has not been finalized and there are many versions in development but panels commonly leverage the flat panel display (FPD) industry. There is alignment to Gen 2 (360x465mm), Gen 2.5 (400x500mm) and Gen 3 (550x650mm) with the largest panel size in the range of 650x650mm. This creates a challenge for equipment suppliers since both size and accuracy requirements are in flux.

Yield is critical for fan-out processes and reconstitution with mold compound is not a clean process. To ensure high final yield, a greater than 98% yield is required for each RDL layer. Compounding yield loss from multiple RDL layers rapidly erodes margins and therefore fewer redistribution layers are better. Product allocation to panel and line utilization is challenging and product mapping to the panel line must ensure full utilization to offset the line investment. It is estimated that the green field cost for a low-volume panel line will be in the range of \$100M. Some of

the specific challenges for a high yielding fan-out panel line are listed below:

- High-speed die placement is absolutely required for reduced cost;
- Placement accuracy is very important;
- Panel warpage is a problem that can complicate die placement;
- Die shift can occur as molding compound cures;
- Die shift becomes critical as $L/S \leq 10\mu m$;
- New dielectric dispense methods and materials are required (slit coating or dry film lamination); and
- Plating uniformity is difficult on a large area rectangular panel.

Although it is intuitive to assume large die will drive the move to a panel format, large high-value die will also require the finest line/space multi-level RDL. It is unlikely panel lines will be able to support these requirements at high yield for several years. Therefore, it is likely high-value die will remain in a round format to leverage existing material sets and process knowledge. If size expansion is required for these products, it may drive a move to 450mm round products. The fan-

out process most likely to first move to a larger panel format will be the eWLB process flow with less demanding die position and alignment requirements.

Summary

Products going into fan-out packages are generally divided into two groups: low-density, low-value, low I/O products, and high-density, high-value products requiring fine line and space attributes. Fan-out processes are grouped into three major process flows and each flow has specific requirements for die placement to reduce cost, optimize yield and improve capability. The highest volume is driven by the lower accuracy eWLB-type products for the mobile market. The eWLB process flow is the lowest cost fan-out process and should be selected if product requirements can support lower I/O count and low-density RDL. This category of product is most likely to be the first to go to a panel format instead of the round format used today.

Both InFO and SWIFT type processes are competitive high-density fan-out flows capable of providing fan-out solutions for high-value products in 2.5D and 3D packages. These process flows are more expensive but can be used for complex packages supporting high-value application processors and memory. Regardless of the process selected, the lowest cost for the process will always be supported by the use of die placement equipment that provides the highest UPH consistent with the placement accuracy required by the process. UPH can be limited because of process conditions such as placement dwell time and high-accuracy alignment, and in the example of InFO-like process flows, the throughput may be limited to a range of 6-8k UPH due to these requirements.

We are developing the next generation of die placement equipment suitable for all fan-out process flows in HVM today. Typical eWLB die placement throughput provided today is about 6k UPH, but the next-generation die placement throughput for eWLB is expected to approach 15k UPH. Typical SWIFT-like process flows today also have a die placement throughput of about 6k UPH, but the next-generation die placement equipment is expected to exceed 10k UPH. This higher UPH will help to reduce the cost of fan-out applications and optimize the die placement segment of the process.

BiTS Workshop

Tom Strothmann received his BA from the U. of Kansas and is Director for Next Generation AP Products at Kulicke & Soffa; email tstrothmann@kns.com

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INDUSTRY NEWS

A*STAR IME announces a multi-chip FOWLP development line



Institute of Microelectronics (IME). The objectives of the group are to develop cost-effective advanced packaging solutions and to spur high-volume manufacturing of next-generation Internet of Things (IoT) technologies. Its members span the industry value chain.

The development line, which is built upon existing infrastructure at IME's facilities at Singapore Science Park II, and its new facilities at Fusionopolis Two, will allow IME and its partners to develop technologies that serve a wide range of markets such as consumer electronics, healthcare, and automotive. Members of the new consortium named in the release include the following: Applied Materials, Asahi Kasei Corporation, Dipsol Chemicals Co., Ltd., ERS Electronic GmbH, Fujifilm, JSR Corporation, Kingyoup Optronics, Kulicke & Soffa, Nordson Corporation, Open-Silicon, Orbotech Ltd, STATS ChipPAC Pte. Ltd., Toho Kasei Co., Ltd., and TOWA Corporation.

The activities of the consortium come at a time when IoT is set to become the next growth driver for the semiconductor industry, as demand for internet-connected devices continues to soar. According to A*STAR IME, FOWLP is an emerging breakthrough chip packaging technology platform aimed at meeting the technology requirements of next-generation electronic devices that require ultra-low power consumption rates, smaller package profiles, higher performance—all made at a lower cost.

The development line is equipped with fully automated tools that can perform the mold-first and redistribution layer (RDL)-first method in multi-chip fabrication. The RDL-first method is expected to achieve a higher reliability rate compared to the conventional mold-first method used by the semiconductor industry, according to the announcement. IME and its partners will jointly develop tools and processes for next-generation FOWLP technologies such as high speed copper (Cu) pillar plating, physical vapor deposition (PVD) processing to control the wafer warpage, moldable underfilling for chip-to-wafer, as well as over molding on wafer with vertical Cu pillar/Cu wire interconnections using wafer-level compression molding, plasma descum of small vias and warpage adjustment, etc.

A*STAR IME emphasized that the FOWLP development line consortium will allow members across the value chain to co-share resources on an open innovation platform and draw upon a rich portfolio of advanced packaging capabilities to address the complexities in system scaling and heterogeneous system integration. Furthermore, the development line will be a test-bed platform through which consortium members can gain new insights on requirements of FOWLP by testing and developing new processes, paving the way for high-volume manufacturing.

The FOWLP development line utilizes tools already in use by major OSATS, and will allow processes, materials and integration flows developed at IME to be smoothly transferred. The consortium anticipates that fabless companies will also be able to make quicker decisions on package structure, integration flows, processes, and materials and equipment for their new products. Materials and equipment suppliers will thereby be able to expedite the development of their products and increase their adoption.

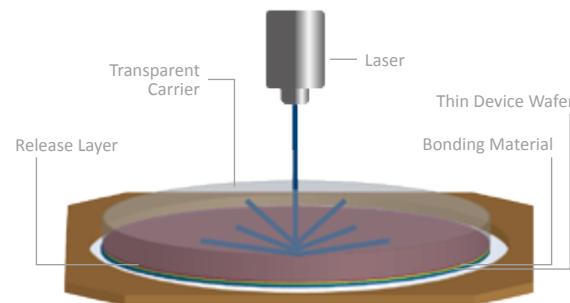


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Ratio 6
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the Netherlands

T: +31 26 319 4500
F: +31 26 319 4550
sales@besi.com

learn more on www.besi.com

