

Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 19, Number 1

January • February 2015

3D lithography distortion control

Page 16

- Advances in test and burn-in
- Achieving a 75GHz test socket
- Ablative DPSS UV laser process
- Optimizing TSV processes and integration
- Reducing the cost of probe card test and repair
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CONTENTS

January • February 2015
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After removal from the FOUP, a 300mm wafer undergoes alignment prior to loading into the Ultratech Superfast 4G Inspection system's coherent gradient sensing (CGS) interferometry module that will perform full-wafer topology measurement for 3D lithography distortion control. The systematic in-line inspections of the latest technologies, such as second-generation VNAND, 25nm DRAM, and 14nm FinFET, have benefited significantly.

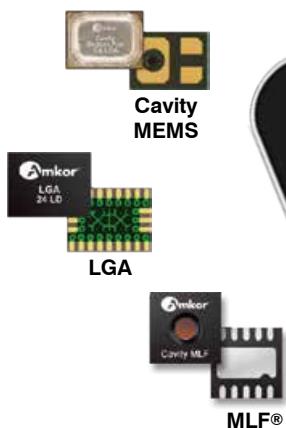
Photo courtesy of Ultratech, Inc.

DEPARTMENTS

Market Outlook Cyclical upturn to continue in 2015 Bill McClean <i>IC Insights, Inc.</i>	5
Guest Editorial The next wave in semiconductor packaging Brandon Prior <i>Prismark Partners LLC</i>	9
Tech Briefs • Indium Corporation to present at IMAPS France workshop • Fluxes and head-in-pillow defects tech sessions to be featured at IPC APEX EXPO Debra Vogler <i>Sr. Technical Editor, Chip Scale Review</i>	14
Guest Editorial Achieving a 75GHz test socket Ila Pal <i>Ironwood Electronics</i>	40
International directory of test & burn-in socket suppliers	42
Industry News SEMI European 3D TSV Summit 2015	53
Advertiser Index, Advertising Sales	56

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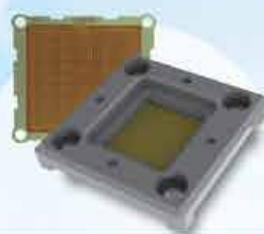
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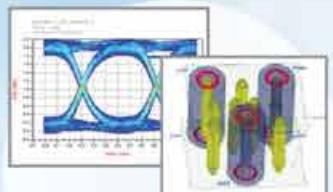
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IN THIS ISSUE

Bonjour 2015!

We open our first issue of 2015 with greetings from Grenoble. Located in southeastern France at the foot of the French Alps, Grenoble was once again chosen for SEMI's third rendition of the European 3D TSV Summit (Jan. 19-21). Staff from *Chip Scale Review* attended the Summit as publication/media sponsor. The themes of "smarter integration" and "enabling smarter systems" played out through the entire event. For more on the conference, visit the "Industry News" section inside this issue.

A portion of this issue is devoted to the test and burn-in socket side of the industry. The upcoming Burn-in & Test Strategies workshop is gearing up for its annual event dedicated to this technology sector. To coincide with this, *Chip Scale Review* annually updates and publishes the international directory of socket suppliers. Buyers and specifiers worldwide reference this guide and will specify and buy directly from suppliers on this list.

Debuting with this first issue of 2015 is a new editorial section consisting of Tech Briefs – short articles written by Senior Technical Editor, Debra Vogler. The new section will feature select quotes, commentary, and data based on questions posed to industry technologists. If your company has significant technical news to announce and you're invited to participate in these interviews, be prepared to discuss the science behind your latest breakthrough, the R&D challenges that have to be solved along the way, and the industry challenges driving the need for the technology. Send your technology news releases to editor@chipscalereview.com.

FEATURE ARTICLES

3D lithography distortion control Jeffrey Mileham <i>Ultratech, Inc.</i>	16
Optimizing TSV processes and integration for volume manufacturing David J. Erickson, Isaac Ow, Sesh Ramaswami <i>Applied Materials</i>	18
Versatile stacking process for heterogeneous 3D integration Thomas Uhrmann, Jürgen Burggraf, Julian Bravin, Markus Wimplinger, Paul Lindner <i>EV Group</i>	24
Reducing the cost of probe card test and repair Greg Olmstead, John Strom, Bill Favier, Foster Lin, Brett Strong <i>Rudolph Technologies, Inc.</i> and Simon Algaier <i>FEINMETALL</i>	29
UV solid-state laser ablation for embedded fine-scale circuitry Dave Myles, David Milne <i>M-Solv</i>	32
Advances in test and burn-in Colin Koh, Muhammad Syafiq <i>Test Tooling Solutions Group</i>	36
Coplanarity analysis and control of spring probe heads for wafer testing Jiachun Zhou (Frank), Cody Jacob, Daniel DelVecchio <i>Smiths Connectors</i>	48

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MARKET OUTLOOK



Cyclical upturn to continue in 2015

By Bill McClean [IC Insights, Inc.]

As IC Insights has emphasized over the past few years, since 2009, there has been a very strong correlation between worldwide GDP growth and worldwide IC market growth. The total worldwide GDP increased 2.8% in 2014 and is forecast to increase 2.9% in 2015, only 0.4 points above the global recession threshold.

With regard to worldwide GDP growth, one of the biggest potential negatives for 2015's growth is the weak Eurozone economy. IC Insights forecasts that the Eurozone economy will grow by 1.0% in 2015, up only slightly from 0.8% growth in 2014.

In 4Q14, the German government forecast that the German economy would grow by only 1.3% in 2015, up from 1.2% growth in 2014 (down from its earlier forecast of 2.0% growth for 2015). This lackluster outlook is significant considering that Germany is the largest economy in the Eurozone. Thus, it currently appears that the Eurozone, with weak growth expected in Germany, France, and Italy, will be the biggest drag on total worldwide GDP growth in 2015.

Japan's economy is also very weak (after registering a negative GDP in 2Q14 and 3Q14, Japan officially entered a recession last year) and is forecast to grow less than 1% in 2015. However, because the Eurozone economy represents twice the share of worldwide GDP compared to Japan (16% for the Eurozone vs. 8% for Japan), its weakness is expected to have more of a negative impact this year.

Historically, there has been a good correlation between oil prices (U.S. dollars per barrel) and worldwide GDP growth. One positive factor for the worldwide economy in 2009 and most of 2010 was the relatively low price of oil. Having the exact opposite effect of rising oil prices, low oil prices have always helped set the stage for a rebound in the worldwide economy. With the average price per barrel of oil declining 31% in 2009 as compared to 2008, the price of oil transitioned from being a "headwind" on the fortunes of the worldwide economy to a "tailwind." Partially driven by lower oil prices, 2010 registered a very strong 4.1% increase in worldwide GDP. Given the forecast of \$58 per barrel of oil for 2015, an 38% decline from 2014, oil prices have the

potential to once again be a "tailwind" for worldwide GDP growth this year.

In summary, the steep decline in oil prices in 2014 gives credible upside potential to IC Insights' current expectations for 2.9% worldwide GDP growth in 2015, which could also lead to stronger 2015 worldwide IC market growth than the 7% increase now forecast. Overall, the price of oil will be one of the most important factors to watch with regard to worldwide GDP and IC market growth in 2015.

IC market forecast

In 2014, the worldwide IC market grew by 8% with a 7% increase forecast for 2015. From 2013-2018, the total IC market is forecast to grow at an average annual rate of 5.4%, more than triple the 1.7% average annual growth rate for the IC industry over the previous five-year span from 2007-2012.

In 2014, total IC unit growth was 9% up from an 8% increase in 2013. Total IC unit shipments are forecast to show a CAGR of 6.4% from 2013 through 2018, compared to the 4.0% average annual unit growth rate from 2007-2012. Meanwhile, after several years of sharp declines, the total IC average selling price is forecast to decrease at a slower average annual rate of 1% from 2013 through 2018.

IC Insights anticipates that the total IC market will surpass the \$300 billion sales level in 2015 (\$307 billion) and the \$400 billion level in 2020. As a point of reference, the IC market first topped the \$10 billion mark in 1980, first exceeded \$100 billion in sales in 1995, and first topped the \$200 billion mark in 2005.

With average annual growth of 11%, the MOS memory segment is forecast to have the strongest growth rate, in dollars, among major IC product categories from 2013 through 2018. Through the forecast period, the MOS memory (11%) and analog IC markets (6%) are forecast to grow at a faster rate than the total IC market, while the MOS logic and microcomponents segments are forecast to have average annual growth of only 3% and 4%, respectively, from 2013 through 2018.

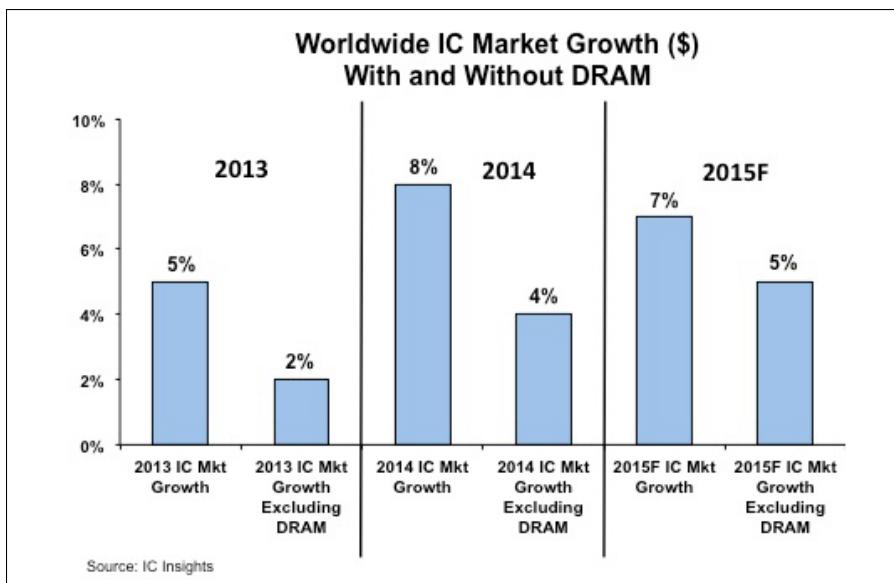


Figure 1: Worldwide IC market growth (\$) with and without DRAM. SOURCE: IC Insights



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IC sales growth in 2014 was slightly more broad-based compared to recent years. DRAM once again led the way in 2014 with 31% annual growth, but other areas also did well, including application processors and many segments within the analog market. Of the 33 major IC product categories IC Insights follows, 13 grew at least as fast as the total IC market increase of 8%. Moreover, 26 IC product categories are forecast to enjoy positive growth in 2015 compared to 25 in 2014 and only 16 in 2013. In 2014, eight IC product categories grew 10% or more as compared to six categories registering double-digit growth in 2013. In 2015, seven IC product segments are forecast to show double-digit growth.

The DRAM market reappeared among the top-growing IC markets in 2013 with a 32% increase. For 2014, DRAM led all IC product categories with 31% growth. In 2015, the DRAM segment is once again expected to register the biggest increase at 15%. DRAM sales growth over the past couple of years has been based on very strong increases in average selling prices (48% in 2013 and a 23% increase in 2014), which have more than offset declines or low single-digit growth rates in DRAM unit shipments.

Figure 1 shows how dramatically the surging DRAM market has affected worldwide IC market growth. In 2013, worldwide IC market growth excluding DRAM would have been only 2%. Moreover, in 2014, total IC market growth excluding DRAM was half the rate (4%) of the total IC market when including DRAM (8%). For 2015, IC Insights forecasts that DRAM market growth will slow to about half of what it was in 2013 and 2014 (to a still strong 15%), which is expected to lessen its positive impact on the total IC market growth rate. However, as shown, the 2014 non-DRAM IC market grew twice as fast as compared to 2013 (4% versus 2%) and is forecast to show slightly better growth in 2015 (5%).

TSV progress to continue in 2015

Through-silicon vias (TSV) and 3D packaging are expected to be hot topics in IC packaging in 2015. Progress is forecast to continue with the development of commercially viable solutions to vertically interconnect two or more ICs using through-silicon vias. TSVs allow for all the chips to be connected in such a way that they function like a single three-dimensional block of multi-layered circuitry (i.e., a 3D IC).

TSVs first appeared on the market in late 2007 in the form of backside vias in CMOS image sensors for the creation of digital camera modules. Assuming the industry can solve some testing issues, drive down costs, and apply new design software for 3D products, image sensors will be only the first of many types of devices to use TSVs. The hybrid memory cube technology being developed by the HMC Consortium utilizes TSVs to interconnect multiple DRAMs on top of a logic chip such as a complex field-programmable gate array (FPGA). Micron claims that HMC will be available as an alternative to DRAM modules in early 2015. AMD and SK Hynix have been working on a similar technology called high bandwidth memory (HBM).

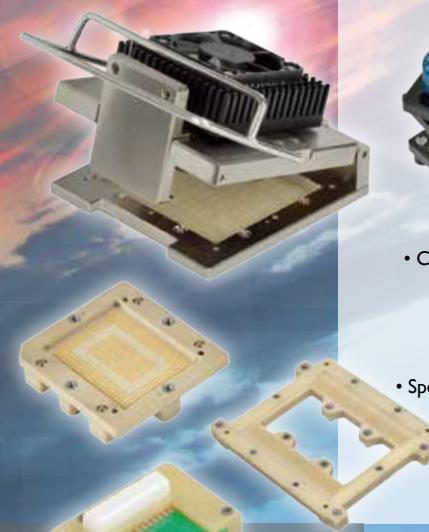
More widespread use of TSV-enabled 3D IC technology for heterogeneous stacks of logic, memory, analog, and/or MEMS-based devices is on the way, but not any time soon. Success with implementing so-called "2.5D" technologies has delayed the need for true 3D IC solutions for heterogeneous stacks. 2.5D involves stacking and interconnecting

chips using silicon interposers with TSVs and is seen as a bridge to full 3D ICs. For now, the only mixed chip-type 3D ICs in high-volume production are image sensor products from Sony with imager and DSP chips, with the HMC and HBM technologies supposedly close to mass production status.

The main challenges holding back 3D IC technology have to do with the need for better EDA tools, the lack of standards, the complexity of designs, and the extra costs associated with TSV technology. High cost is seen by many to be the biggest stumbling block, but the ability to justify the cost of using TSVs will depend on the cost/performance ratio in each application area.

Biography

Bill McClean received his BS in business administration and an Associate Degree in aviation from the U. of Illinois; he is President of IC Insights, Inc.; email info@icinsights.com

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GUEST EDITORIAL



The next wave in semiconductor packaging

By Brandon Prior [Prismark Partners LLC]

The past twenty years have seen an enormous shift in packaging approaches used for integrated circuits (ICs). In that time, we have moved from over 95% of die going into lead frame packages to about 60% of units today. From a revenue perspective, 85% of all package assembly is into package types that did not exist 20 years ago. This column reviews the changes in the last two decades and what package approaches in production or development today are expected to be more widely adopted in the coming decade.

IC packages come in a wide range of formats that continue to evolve. In very simple terms, an IC can be delivered as a bare die or wafer-level chip-scale packaging (WLCSP), in a lead frame package, a ceramic package, or on a substrate-based package. Substrate-based packages first emerged twenty years ago as an alternative to lead frame packages, and since that time have grown to represent 18% of IC package units, but closer to 70% of all IC package value. Substrate packages offer three significant advantages over lead frame packages: 1) Substrate or array packages can have I/O under the package, allowing for

much higher I/O counts. Lead frame packages today generally are limited at 240 I/Os, whereas substrate-based packages can have over 2,000 I/Os. 2) Substrate packages can route signal lines through many layers, adding both flexibility and function beyond what an etched or stamped lead frame can offer. 3) Substrate packages can have better electrical conductivity because of a shorter interconnect path.

The emergence of substrate-based packages

Substrate-based packages have grown from being a niche segment in 1995 to being the dominant package for devices with >100 I/Os. In addition to offering more functionality, substrate-based solutions have become the most cost-effective solution for any semiconductor device with more than 150 I/Os.

In 2013, organic substrate-based packages represented 18% of the total 202Bn packages shipped globally. The balance is either as a bare die, or more likely in a lead frame package construction. When viewed in revenue terms, substrate-based packages represented over 67% of the \$34Bn in total IC package value-add for 2013.

The substrate value for a substrate package can represent 15% to 60% of the total package value (excluding die), but on average represented 34% of the package value in 2014, or \$7.7Bn. Although production of BGA packages began as early as 1993, the organic package substrate

market was quite small until 1997 when Intel began its transition from ceramic to organic solutions.

Organic substrates act as the interconnect interposer and supporting platform in semiconductor packaging assembly. Due to different performance requirements, form factor specifications, and cost considerations, a variety of rigid organic substrates have been developed to meet industry needs.

The initial solution was a wire bond plastic BGA (PBGA) substrate, using two- to four-layer designs. From this original concept, a number of alternatives have emerged, including: 1) CSP or fine-pitch BGA: basically a smaller version using fine-pitch for mobile applications; stacked CSP was also included. 2) Flip-chip versions using build-up substrates; 3) Various system-in-package (SiP) or module solutions such as RF module, camera module, and memory card module; and 4) Package-on-package (PoP).

Because it is impossible to track all of the different configurations, we have categorized them into six major types of organic substrates (**Table 1**). Each has its unique focus of applications, and thus, the supply chain and performance requirements differ. Several of the substrates listed in **Table 1** are discussed in the sub-sections below.

Flip-chip ball, pin, and land grid array (FCBGA/PGA and LGA). These are the packages of choice for high I/O count complex MPU, GPU, and logic devices. The substrates are similar in LGA, BGA, and PGA; however, they require different interfaces to the main board. PGA and LGA require sockets, mainly for MPU. Flip-chip interconnect, rather than wire bond, is used for all of these packages. Package sizes range from 20mm–55mm on a side and substrates can have six to sixteen total layers. Packages smaller than 20mm

Substrate	Application	Major Users*	Leading Substrate Suppliers
Flip Chip PGA/BGA/LGA	MPU, GPU, Chipset, ASIC	Intel, AMD, NVIDIA, IBM, various ASIC suppliers	Ibiden, Shinko, NanYa, SEMCO, Kyocera, Unimicron
Flip Chip CSP and PoP	Baseband/Apps Processor	Qualcomm, TI, Samsung, Apple, Intel, Broadcom, Renesas	SEMCO, Kinsus, Unimicron, Kyocera, Ibiden
Wire Bond PBGA	Logic, MCU, DSP, etc.	Intel, MediaTek, TI, Samsung, Freescale, Renesas, STMicro, Broadcom	Nan Ya, Unimicron, ASEM, SEMCO, LG Innotek
Wire Bond CSP (includes stacked die)	Baseband/Apps Processor, Flash	TI, Qualcomm, STMicro, Broadcom, NXP, Samsung, Infineon	SEMCO, Unimicron, Kinsus, Eastern
Wire Bond BOC or Flip Chip CSP for DRAM	DRAM	Samsung, Hynix, Micron	SEMCO, ASEM, Nan Ya, Unimicron, Simmtech
RF Module	PA, Connectivity, Transceiver, other	Qorvo, Skyworks, Avago, Murata, Taiyo Yuden	SEMCO, Unimicron, Kinsus, Simmtech, ACCESS

*Major users also include OSATs: ASE, Amkor, SPIL, STATS ChipPAC, and PowerTech

Table 1: Organic substrate supply chain.

are included in the next segment: flip-chip CSP (FCCSP). The FCBGA category remains the package of choice for high lead count devices requiring high performance. However, it remains limited to these devices.

Current mainstream capabilities for advanced FCBGA/PGA/LGA can accommodate 130 μm bump pitches, use up to 6-4-6 constructions, have 10 μm -12 μm L/S, and are on package body sizes from 27mm-55mm. Nearly all companies are using the semi-additive build-up process with the latest versions of the Ajinomoto build-up dry film dielectric (ABF). The challenge with broader adoption has historically been the considerably more expensive substrates and limited bumping and assembly infrastructure required to accommodate demands for companies moving to flip-chip.

Figure 1 shows Intel's Haswell i5 notebook processor using an 8-layer

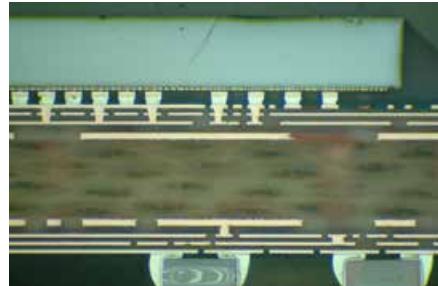


Figure 1: Intel Haswell i5 4250U substrate. SOURCE: Prismark/Binghamton U.

substrate. Intel continues to lead the substrate technology requirements, for now, with few companies to date requiring sub-15 μm line/space.

Flip-chip CSP and PoP. These packages offer a lower profile, better electrical performance, and slightly higher I/O than a conventional wire bond CSP package. FCCSP differs from FCBGA only in body size (<20mm), package pitch (typically CSP is <0.8mm ball pitch), and will usually have from 60-1,300 I/O. The market for FCCSP packages has grown from 100M in 2007 to 5Bn packages in 2013. Looking out five years, FCCSP is forecasted to reach 14Bn units, with strong growth from mobile processors, DRAM and other segments. While application processors from Apple, Samsung, and Qualcomm

are using four- to six-layer substrates, lower-end processors from MediaTek and HiSilicon are often just two-layer designs.

Wire bond PBGA. These packages continue to be the workhorse for 200-800 I/O pin count needs. Extreme price declines have caused many substrate companies to exit this slow growth business. PBGA will continue to lose share to flip-chip at the high end and lower-cost CSP packages at the low end. Therefore, a market decline of 4% per year is expected for PBGA. The leading users of wire bond PBGA substrates remain the merchant package assemblers, although many captive operations have significant volumes. The top subcontractors consuming PBGA substrates include ASE, SPIL, STATS ChipPAC, J-Devices, and Amkor. Other leading users include captive operations such as Freescale, Renesas, Toshiba, Fujitsu, Infineon, and many others.

Wire bond CSP. These packages emerged soon after PBGA packages in the late 1990s. CSPs are effectively wire bond PBGA packages with tighter ball pitches (0.8mm and below), hence the term fine-pitch BGA, or FBGA. An improved definition includes all substrates with package sizes of <20mm. CSPs were initially targeted toward lower lead count devices, but they have now expanded to accommodate 700 I/Os and above.

Total demand for wire bond CSP continues to grow in line with the semiconductor market. It is also losing share to the fast growing FCCSP, but will continue to be the cost-effective approach for many devices with 20-500 I/Os. Initially driven primarily by the high-volume mobile phone market,



Figure 2: Three-layer wire bond CSP substrate for the SK Hynix NAND device.

today most other portable as well as non-portable applications are now using CSP packages for both their smaller size and better electrical performance. Nearly all NAND Flash is packaged in a wire bond CSP package. **Figure 2** shows a three-layer substrate now commonly used for mobile DRAM and NAND packages.

RF modules. RF modules include a range of solutions, often incorporating one or more active power devices along with passive components. The most common RF modules using organic substrates include power amplifier (PA) and power amplifier duplexer (PAD) modules. Connectivity modules for WLAN/Bluetooth® and/or GPS are also common. RF modules are usually 3mm-8mm in size, and typically can incorporate one to four active CMOS or GaAs die, with as many as forty discrete passive components.

The next wave of package evolution

We will continue to see improvements and evolution in substrate-based packages, and they will remain the packages of choice for most all advanced requirements. However, as we look forward, there is

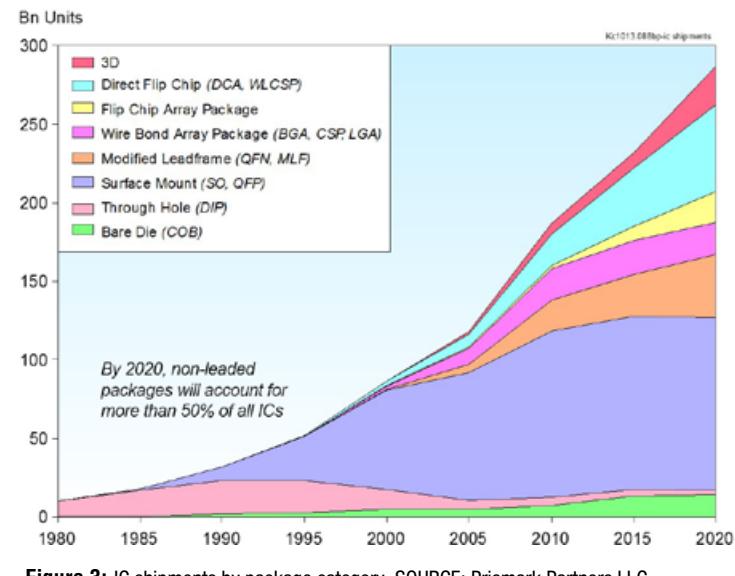


Figure 3: IC shipments by package category. SOURCE: Prismark Partners LLC



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Typical Applications

Semiconductor Packaging

- Medical Imaging
- Multichip Modules
- 3D / 2.5D Packaging
- Wafer Scale Packaging
- RF / Microwave Modules

Photonic Packaging

- Optical Engines
- LED Assemblies
- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

significant interest in alternative packages to meet the ongoing demands of smaller, faster and more economical electronics systems. **Figure 3** shows that 3D and direct flip-chip (WLCSP) will be two of the most notable trends in the coming years. While these are not necessarily new package technologies, they do offer notable improvements to current approaches, and will take us to 2020 and beyond.

WLCSP. As a package concept, WLCSP has been around almost 20 years, and unit volumes are already significant. WLCSPs offer the smallest package size possible, with the package equal to the die size. Recent mobile product tear downs show a significant switch toward the use of WLCSP for nearly all devices with only a few, but important, exceptions still using substrate packages. Even more critical is that WLCSP packages can be less than 0.4mm thick, and this is now being requested by leading mobile phone designers.

WLCSP use today, however, is still largely driven by portable electronics. Going forward, we expect further adoption outside of mobile products (**Figure 4**). This adoption will be enabled by the second-generation of WLCSP package approaches, including, but not limited to:

- **Fan-out WLCSP:** These offer significantly added flexibility with multi-chip, PoP, and broader final pitch configurations that can be built.

While no longer a die size package, the redistribution layer (RDL) processing is still wafer-based, and already offers thinner packages and finer routing capabilities than substrate-based solutions of today.

- **Protected or enhanced WLCSP:** These offer protection on 5 sides of the die, which should enable improved package reliability and easier handling for surface mount technology (SMT) assembly.

- **WLCSP without RDL:** Die designed for flip-chip attach without RDL keep the cost of WLCSP low. Many companies have been using this “bump on pad” approach for years.

3D-TSV and silicon interposer.

These approaches are still in development, with high-volume products expected within the next year. While some companies continue to struggle with whether these

solutions can be made cost effective, a select few have embraced them. Select examples of successful adoption include:

- Image sensors: Most leading players utilize TSV for backside access, while Sony has moved into volume production of 3D TSV stacking.
- RF and MEMS: Many players are using TSV through the wafer caps of MEMS, as well as backside access for RF devices. A few companies such as STMicroelectronics and Bosch are in production of TSV through active silicon in MEMS designs shipping today.
- The silicon interposer approach from Xilinx is perhaps the most well documented example, and has been in production since 2012. Many other companies are looking into this, but so far, production using an interposer approach is still expensive and therefore limited to the highest end FPGA designs from Xilinx.
- DRAM stacks: SK Hynix, Micron and Samsung will all be shipping stacked TSV DRAM die for high bandwidth memory for ultra high-end server and datacom equipment. Samsung and SK Hynix have also shown TSV stacks for high-end servers. Many products will be available in 2015.

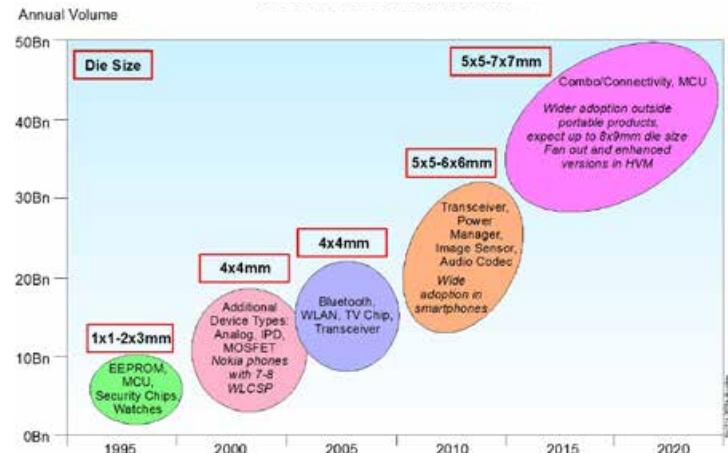


Figure 4: WLCSP/DCA timeline. SOURCE: Prismark Partners LLC

The DRAM examples are expected to be the highest volume in wafer terms, and will also set the stage for further development and wider adoption. However, significant ongoing work needs to address remaining issues, some of which include: 1) Overall process integration challenges from fab to assembly; 2) Wafer-level testing at fine pitches; 3) Die-to-wafer assembly; 4) Thin wafer handing; 5) Materials compatibility; and 5) Thermal management of performance silicon.

Summary

We have seen an enormous shift in packaging approaches used for ICs in the past twenty years. From a revenue perspective, 85% of all package assembly is into package types that did not exist 20 years ago. The next wave of packaging is already upon us. Although we do not expect a significant amount of truly new packages to emerge beyond 3D-TSV, improvements in existing substrate, wafer-level and even lead frame packages will enable the ongoing functional improvements and size reductions that are expected in IC packages in the years to come.

Biography

Brandon Prior received his BA and BE degrees from Dartmouth College and the Thayer School of Engineering, Hanover, NH, respectively. He is a senior consultant at Prismark Partners LLC; email bprior@prismark.com

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TECH BRIEFS

by Debra Vogler, Sr. Technical Editor

Indium Corporation to present at IMAPS France workshop

Indium Corporation's Graham Wilson, an Applications Engineer, is scheduled to present his paper entitled "Sn+ Heat-Spring® Solder TIMs for Superior Thermal Management," at the IMAPS France Workshop on Thermal Management (La Rochelle, France, 2/5/15) at the time of this writing. The paper explores how Heat-Spring thermal interface materials (TIMs) perform against phase change materials and thermal greases under a variety of conditions. Comparative results as they relate to power cycling and bake testing will be presented and the advantages of using the technology will also be discussed.

To get a perspective on the topic, *Chip Scale Review* asked Indium to comment on select aspects of metallic thermal interface performance. Tim Jensen, Senior Product Manager, Engineered Solders, told *CSR* that the TIMs used in the company's new Heat-Spring meet specific thermal performance requirements, which are measured as thermal resistance for the TIM with the application parameters of clamping force applied, finish and flatness of the contacting surfaces, and mounting orientation. Long-term product life requirements are also a consideration. "Operation at an elevated temperature is a primary determinant of failure over time of a semiconductor," explained Jensen. "The purpose of a TIM material is to avoid an increase in the temperature of the die to the threshold temperature for failure." Jensen further noted that moving heat from the critical die surface through the package to an external heat sink is a critical design element used to improve package performance and eliminate thermal constraints on operation, while improving system reliability. "A significant percentage of package thermal

resistance is found in the thermal interface materials, therefore, improvements obtained by specifying a TIM with demonstrated performance that exceeds that of the best traditional material, such as a silicone-based thermal compound, is a first step in design."

Awareness of the need to eliminate silicone compounds is increasing, commented Jensen, with some major power semiconductor manufacturers specifying that no TIM may be used that contains a silicone oil carrier. "Metallic TIMs, such as the Heat-Spring and associated indium alloy shims, also meet other system-level requirements," said Jensen. Included in these requirements are: elimination of the use of a thermal compound that contains silicone oil, a very common carrier; elimination of any concern for outgassing of the silicone; re-deposition on sensitive electrical interconnects and optical lenses and components; and removal of concerns for what is termed "dry-out" within the interface. "The condition termed "dry-out" occurs as both outgassing and physical migration of the silicone oil carrier that occurs over time, and with temperature and cycling."

Other relevant material properties for TIMs include surface contact and improvement with cycling and temperature. "Unlike many other TIMs, such as graphite sheets and die-cut preforms of several types, the Heat-Spring product demonstrates thermal resistance improvements with time and temperature," Jensen told *CSR*. "Silicone-based thermal compounds frequently have been shown to demonstrate a worsening of thermal resistance in the interface over time and temperature because of silicone outgassing, migration, and pump-out." **Figure 1** compares four types of TIM products, including two different commercial brands of relatively high-performance silicone-based thermal grease and two metallic TIM materials, an indium metal flat foil with no patterning (0.003"-thick) and an Indium Corporation Heat-Spring® patterned metallic indium foil (0.003"-thick). Jensen explained that the two metal TIMs perform better than either thermal grease, above 140PSI applied clamping force. "The Heat-Spring patterned metallic TIM outperforms both of the well-known thermal greases at any clamping force greater than approximately 45PSI (.3MPA). Jensen further noted that the Heat-Spring makes intimate contact with the two contacting (source and heat sink) surfaces, and the pattern or texture (visible to the eye) is not a cosmetic enhancement. "The patterning of the Heat-Spring provides an array of compressible columns in the metal, and each of these columns conforms to the roughness and geometry of the mating contact surfaces within the interface."



Tim Jensen, Senior Product Manager, Engineered Solders, Indium Corporation

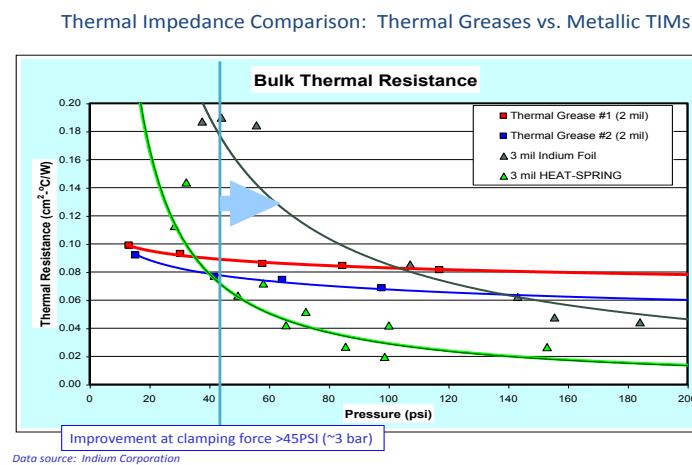


Figure 1: Thermal impedance comparison: thermal greases vs. metallic TIMs. SOURCE: Indium Corporation

Fluxes and head-in-pillow defects tech sessions to be featured at IPC APEX EXPO

Industry experts will tackle the topics of fluxes and ball grid array (BGA) head-in-pillow defects during technical sessions at IPC APEX EXPO 2015 (2/22-2/26/15; San Diego, CA). Alpha's Jason Fullerton, Customer Technical Support Engineer for the Americas Region, will moderate two of these sessions. The "Fluxes I" session focuses on the makeup and performance of the flux component of solder paste. The BGA "Head in Pillow" session discusses the defects of the same name on BGA packages.

Fullerton told *Chip Scale Review* that in the sessions he is moderating there will be multiple examples of new research that will be presented including: 1) A study of how solder paste storage conditions can affect surface insulation resistance (SIR) performance; 2) A case study of a method of designing solder paste stencils to eliminate head-in-pillow defects caused by component warpage; and 3) An experiment to quantify the effect of component contamination with NaCl and its impact on the incidence of head-in-pillow defects.

"The head-in-pillow defect is an excellent example of an area where the industry is still trying to fully understand the condition and all the influences on its formation," Fullerton told *CSR*. While the company does formulation and performance testing to ensure its solder paste products are as robust as possible to this defect type, he explained that there are conditions that lead to head-in-pillow defects that solder paste cannot be expected to completely eliminate. One such cause is component warpage. "Some solder pastes are more robust to this condition than others. But there are cases where assemblers don't have the freedom to change products and have to adapt to the performance provided by the paste in use." He noted that one paper to be presented in the "Head-in-Pillow" session describes a means to optimize the amount of solder paste used by varying the design of the stencils used in the process to eliminate the occurrence of head-in-pillow defects when the warpage of a component is known and consistent. "The work presented demonstrates a deeper understanding of all of the mechanisms involved in the formation of this type of defect than is commonly seen in the industry."

Component contamination is another condition that can cause head-in-pillow defects, commented Fullerton. "Although many assemblers may initially suspect that the cause is some sort of performance deficiency in the solder paste used, one paper in the "Head-in-Pillow" session shows the results of an experiment designed to demonstrate the correlation between contamination and incidence of head-in-pillow defects." Fullerton further added that providing the data to show that

contamination can be a significant factor in forming these defects is important to the industry because it provides additional avenues of investigation to be pursued when trying to troubleshoot their cause.

Fullerton believes that there is a great deal of value in these kind of technical sessions if one can transfer what is learned to the production floor. As an example, he offered up one paper in the "Fluxes" session that describes a number of tests that can be used to evaluate the performance of solder paste. "When users set out to test solder pastes, there are a variety of potential test methods that can be included in their overall test plan," said Fullerton. "Many solder paste manufacturers, Alpha included, can provide technical resources to assist in defining an appropriate test plan for evaluation of current and candidate solder pastes." That said, he noted that some users prefer to perform their testing without involving the material suppliers, while others desire simple tests that can be repeated periodically to ensure the performance of their chosen solder paste is consistent over time. "In these situations, this paper is an excellent resource for practical tests that can be performed on the factory floor with equipment that is typically available to the manufacturing engineer."

Looking ahead, Fullerton sees the industry's major challenge as the continuing reduction of package form factors and the impact on the interconnect materials and processes used to assemble ultra fine-pitch components to PCBAs. "For example, the evolution of passive component packages from 0201 to 01005 to even smaller packages is pushing the limits of solder paste materials and deposition methods," said Fullerton. "Solder paste manufacturers are now manufacturing and providing solder paste particle distributions that didn't exist when I started my career, and developing no-clean flux materials that are capable of performing at the ultra-small circuit spacing typical of modern electronics." He also observed that solder paste stencil printing has enjoyed decades as the primary application method, but that method is now challenged by the viability of jetting technology. "Given the current trends in hand-held electronics and the continuing demand for more performance in these small form factors, I expect the assembly challenges due to miniaturization of electronics to be an important consideration for the foreseeable future."



Jason Fullerton,
Customer Technical
Support Engineer,
Alpha, an Alent plc
Company

3D lithography distortion control

By Jeffrey Mileham [Ultratech, Inc.]

As Moore's Law becomes increasingly difficult and expensive to maintain through two dimensions (2D) all CMOS industry technologies have started to migrate to 3D. Flash NAND has started migrating to vertical NAND (VNAND), DRAM is implementing UHAR (ultra high-aspect ratio) capacitor structures to extend 3D, and logic is preparing for the FinFET ramp. In all cases, these new device paradigms represent a significant departure from the original CMOS planar technology where structures were thin and material engineering was mostly related to the silicon crystallography.

The challenges

The industry has reported the manufacturing challenges associated with this 3D conversion and it is worth pointing out that the two critically needed technology solutions are related to 3D material distortion. The two major issues are directly due to the increasing height of the 3D structure. The first one is that built-in stress non-uniformities in the 3D stack translate to in-plane distortions. The in-plane distortions compromise the ability of lithography to align successive pattern elements of the 3D structure. The lithographic scanner is only able to read patterns and cannot necessarily anticipate material distortion, leading to large misalignments and lower yield. The second is the increasing non-uniformity in surface planarity due to the complex and thick 3D stack. The CMOS processing techniques have to rely on a planar structure to insure integrity of patterning. Given the increasing non-uniformities, focus during lithography becomes increasingly difficult to maintain. As a result, the pattern-critical dimensions as well as connectivity continuity are affected, representing another large source of electrical performance drops or failures.

Collaboration

In leveraging two years of working with leading-edge memory and logic customers using our Superfast 3G inspection systems,

we gained a clear understanding of the industry challenges and the technology needed to enable in-line inspection tools to further advance the 3D manufacturing industry. As a result, the Superfast 4G in-line, 3D topography inspection system was designed with advanced technology to solve the challenges and meet the needs to enable high-volume, 3D manufacturing.

The Superfast technology is based on patented coherent gradient sensing (CGS) interferometry. A schematic of the system is shown in **Figure 1**. The system starts with a relatively low-powered HeNe laser that is expanded to a diameter greater than the

for each pixel of the camera. There are two sets of diffraction gratings and cameras simultaneously collecting slope information in both the x-direction and the y-direction in order to construct a complete slope map of the wafer in parallel. Finally, the slope data derived from the interference patterns is integrated numerically to generate the surface shape, or topography.

An important part of the CGS technology used in Superfast is that it can be used with all types of wafers, including patterned wafers. Several factors contribute to the ability of the CGS technique to measure patterned wafers. The first is that the interference is self-referencing in contrast to other technologies that utilize a reference beam, for example, from a flat mirror. As a result, the two images used to generate the interference pattern in the new technology are of similar intensity and exhibit excellent fringe contrast regardless of the reflectivity of the surface under investigation. Second, a series of interferometric images are collected in both the x and y directions to obtain phase-shifted data with controlled increments of phase. The dark and light fringe contrast bands move dynamically as the phase is shifted, thus allowing the interference pattern be effectively separated from the static pattern contrast. Third, for typical wafer deformations of tens to hundreds of microns, the CGS fringes have a width and spacing much larger than typical pattern features. Such fringe patterns are much more robust for common fringe analysis techniques because the fringes are reasonably smooth and continuous across the entire wafer. Traditional interferometers may have fringe patterns that become discontinuous and difficult to resolve in the presence of wafer patterns, making fringe analysis challenging if not impossible.

The Superfast 4G leverages the single topography inspection to derive through algorithms the flatness, stress and displacement components of the 3D distortion (**Figure 2**). The general approaches for deriving stress and displacement are based on fundamentals of plate mechanics. Stress can be computed from the local surface

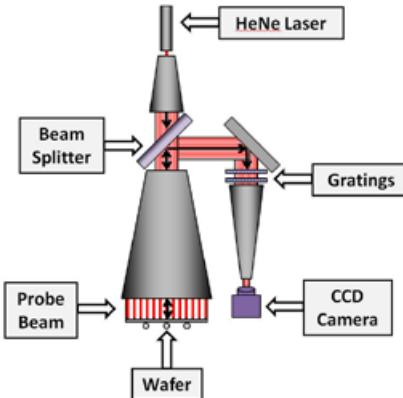


Figure 1: CGS interferometry module for full-wafer topology measurement.

wafer (>300mm), and illuminates the entire wafer at once. The beam that reflects off the wafer surface is distorted in accordance with the local height variations of the wafer, and this reflected light is directed towards two parallel diffraction gratings, which create copies of the surface reflection separated by a fixed distance, ω , called the shearing distance. These copies create an interference pattern that is then imaged onto a CCD sensor that maps a 300mm wafer with greater than 3,000,000 data points with measurement times of a few seconds. The interference pattern contours are areas of constant slope on the wafer and the image is analyzed to provide slope information

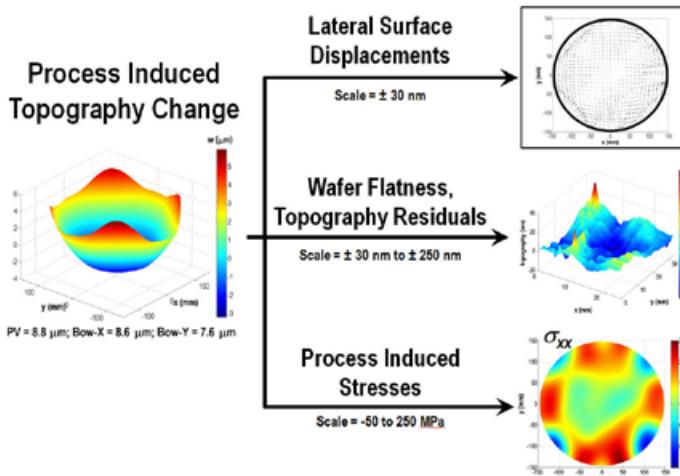


Figure 2: Components of 3D distortion derived from the front-side topography inspection with the Superfast 4G.

curvatures (second derivative of topography) using the well-known Stoney formula. The calculation of surface displacements is rooted in the basics of Kirchhoff plate theory that relates surface slopes to in-plane displacements. The 3G predecessor has been used extensively to measure process-induced topography changes and characterized these distortions. By utilizing such measurements, pilot production of the latest technology has benefited significantly (from 2nd generation VNAND to 25nm DRAM to 14nm FinFET). The systematic in-line inspections of topography coupled with the analysis of the various components of the 3D distortions has resulted in overlay improvement and yield gains. By fingerprinting the full process flow, leading-edge device manufacturers have been able to quantify and prioritize the requirements by identifying critical process steps and their associated deformation signatures. This information was used to develop the high-volume production 4G system.

Memory market leaders, which are further along in their 3D ramp, clearly confirmed that the first and most important contribution to enabling 3D manufacturing is to use distortion measurements to help the lithographic scanner anticipate the material distortion and improve alignment performance. In VNAND, it was found that wafer distortion is now the major contribution to misalignment, which limits the density of the VNAND array design. Medium quantity production showed the ability to reduce misalignment between 20% and 80% depending on the thickness of the stack, and significantly improve overlay and yield especially in VNAND. Furthermore, in addition to displacement feed-forward, measurements of process-induced distortion

automation, and the approach to feed-forward this information to the scanner (**Figure 3**). It is now a proven architecture for production ramp at multiple sites.

Advanced technology

A robust advanced process control (APC) module was designed into the 4G system due to wafer-to-wafer and lot-to-lot variations requiring extensive inline sampling with 30% of wafers and 100% of the lots becoming the sampling standard. As a result, the yield benefits are significant, and to further lower the cost-of-ownership, an advanced, front-end wafer handler was added, which significantly increases the throughput to the highest in the industry (75wph for the 3G, 125wph for 4G with roadmap to 150wph).

To facilitate a smooth manufacturing ramp and risk-free transition from Superfast 3G to the high-volume Superfast 4G, the two inspection systems have identical process modules retaining all critical optical components and stage. This insures a perfect matching of the measurement module of the two tools, bringing lower

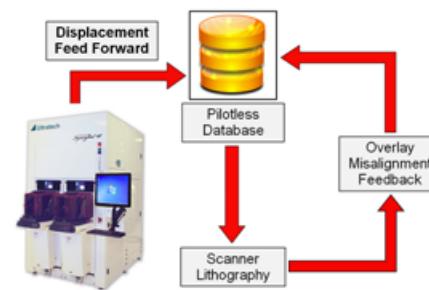


Figure 3: Superfast 4G, front-side, 3D wafer in-line inspection system using the feed-forward approach to send information to the lithography scanner.

are being used for upstream process control, allowing device manufacturers a method for early detection of severe process excursions that cannot be corrected in the scanner.

These collaborative efforts have enabled the rapid development of the complex algorithm, the factory

CoO benefits without the cost of technical risk. Innovation at the system engineering level centered around active isolation of the optics and stage to enable a decrease in noise and vibration. This has produced industry-leading repeatability with Angstrom-level displacement capabilities used for overlay control.

The direct, front-side 3D topography measurement capability is well suited for patterned wafer applications such as feed-forward overlay distortion control, 3D topography measurement for focus control, and high-stress process control (bow, warpage, breakage) (**Figure 4**). Ultratech

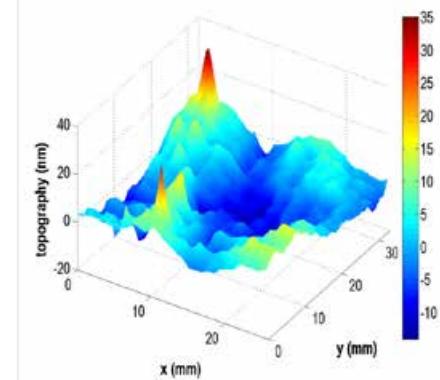


Figure 4: Example of localized chip-level topography map. The height scale runs from -10nm (blue) to 35nm (red).

invested heavily in algorithm and factory automation capabilities and made significant improvements to the new inspection system, resulting in increases of 2.5x in performance and 65% in throughput, as well as a 30% reduction in edge exclusion, compared to the 3G system.

Summary

For applications beyond lithography, material deposition and polishing are noted as the second most important contributors to 3D distortion yield challenges. The technology described above is already being considered for thin and planarization applications. Through additional collaborative efforts, the 4G system will address these in the near future.

Biography

Jeffrey Mileham received his BS and MS degrees in Mechanical Engineering from SUNY at Buffalo and his PhD in Materials Science and Engineering from the U. of Florida and is the Senior Applications Manager of Inspection Systems at Ultratech, Inc.; email jmileham@ultratech.com

Optimizing TSV processes and integration for volume manufacturing

By David J. Erickson, Isaac Ow, Sesh Ramaswami [Applied Materials]

Through-silicon via (TSV) technology creates new opportunities for numerous high-performance and/or form factor conscious applications and is used for devices such as DRAM, logic, and sensors, as well as for advanced silicon interposer applications in GPU, wireline communications, and high-performance computing.

In both 3D and 2.5D architectures, the central element is the TSV itself, whose fabrication has been subject to many unit-process and process-integration challenges [1-4] that have now been largely resolved. The primary steps in forming the via are deep silicon via etch, chemical vapor deposition (CVD) of an insulating oxide liner, physical vapor deposition (PVD) of a metal barrier and seed layer, electrochemical deposition (ECD) of Cu, and chemical-mechanical planarization (CMP) as shown in **Figure 1**. TSV aspect ratio (AR) typically ranges from 5:1 to 12:1.

In the via-middle flow, TSVs are created after transistor formation but before the formation of all or some of the back-end-of-line (BEOL) damascene interconnect layers. Via-reveal is a companion process to via-middle and is done on the backside of wafers after thinning. In the via-last flow, TSVs are created from the backside of thinned wafers. Many applications integrating TSVs must also adopt new bumping approaches to meet the more challenging pitch and density requirements. TSV enabled die-to-die stacking of chips such as DRAM requires very high density bump arrays, presenting unique within-die co-planarity challenges.

Etch technology requirements

Deep reactive ion etch (DRIE) technology is required to etch through the silicon. It involves a combination of dielectric etch and deep silicon etch. To enable downstream processes and seamless product integration, the TSV etch process must deliver smooth sidewalls, minimal reentrancy or undercut between layers, all-in-one etching of dielectric and silicon, high resist selectivity, and depth uniformity

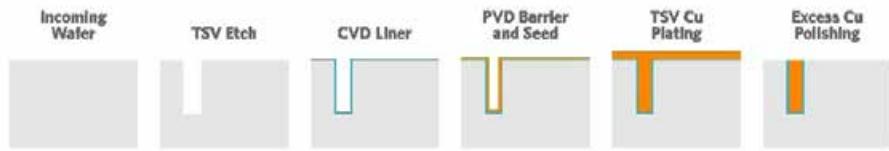


Figure 1: Typical integration flow for TSV creation and fill is very similar to the BEOL sequence.

across the wafer. The TSV is etched by a process of alternating chemistries that etch the silicon and then deposit a protective passivation coating through polymerization reactions. Advanced etch reactor design, modulating source and wafer bias power, and special gas switching techniques enable smooth sidewalls at high etch rates in increasingly high aspect ratio (HAR) structures.

Insulator deposition with CVD

Following etch and post-etch clean, the TSVs are lined with an SiO_2 dielectric deposited using a CVD process. Sub-atmospheric CVD (SACVD) deposition is best suited for schemes that can

accommodate temperatures of approximately 400°C. SACVD O_3/TEOS chemistry exhibits 100% sidewall coverage in HAR structures. The high SACVD step coverage enables continuous PVD metal barrier and seed layers critical for void-free Cu fill.

Advanced metal liner/barrier deposition with PVD

The unit process following TSV insulation is critical. Cu diffusion barrier and Cu seed layer deposition quality directly impact ECD gap fill, electrical performance, and reliability of the integrated TSV structure.

Figure 2a shows a dimensional comparison between BEOL and TSV

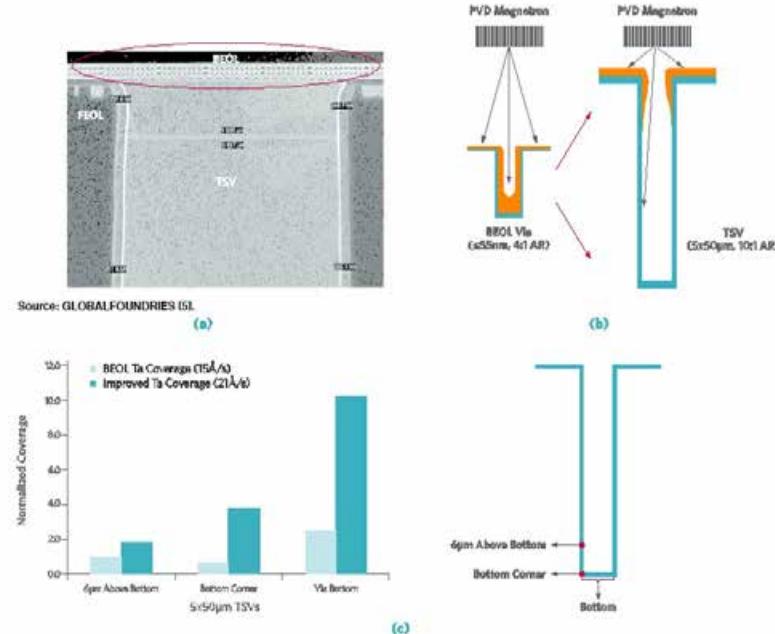


Figure 2: a) SEM image shows vast scale difference between BEOL structures (circled) and a single TSV (courtesy of GLOBALFOUNDRIES); b) Relative scale of BEOL vs. TSV structure makes BEOL PVD inappropriate for TSV applications; c) Improved magnetron design and optimized directionality result in TSV-optimized PVD outperforming BEOL PVD.

When Socket meets Pin...

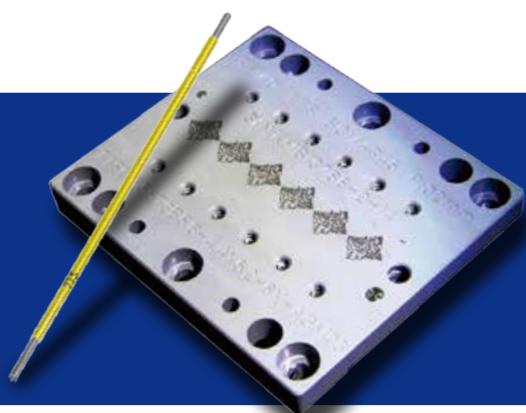


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features. As shown in **Figure 2b**, step coverage in a PVD chamber is a strong function of the neutral/metal ion ratio. Neutrals have high angular distribution and follow line-of-sight deposition. For HAR TSV structures, the result is overhang buildup at the via opening and poor sidewall coverage. Ion energy is also important, as only high-energy ions can reach the bottom of the TSVs. Several technology refinements have greatly improved PVD capabilities for TSV fabrication (**Figure 2c**). Magnetron design [6] is important in establishing the ionization level in a PVD chamber for sputtering metals. To improve directionality of the ions, a potential difference/bias must be established at the wafer level to impart high energy levels to the ions and “pull” them into the TSVs.

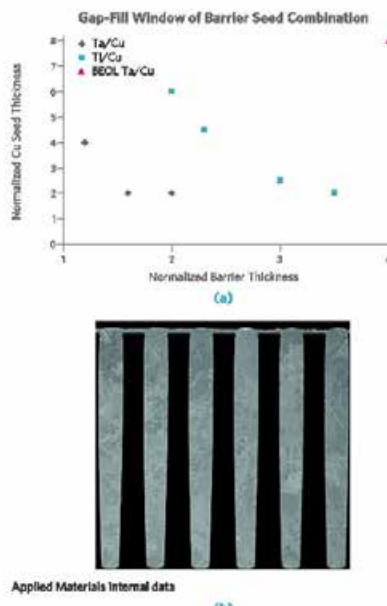


Figure 3: TSV-optimized Ti/Cu and Ta/Cu PVD results are significantly superior to those of BEOL PVD.

Thickness of the barrier/seed layers correlates strongly with the quality of gap fill. The range of barrier/seed thicknesses that results in void-free gap fill can be defined as a gap-fill window. With the enhanced design described above and additional PVD and ECD parameter tuning, much thinner barrier/seed layers are possible. These thinner layers minimize metal buildup around via openings, thereby promoting void-free gap fill (**Figure 3**) in addition to improving productivity and reducing production costs.

The industry is also considering a transition from tantalum (Ta) to titanium (Ti) barriers. This trend is based on manufacturing considerations as well as on Ti's material properties. As shown in **Figure 3**, using TSV-optimized PVD for Ta and

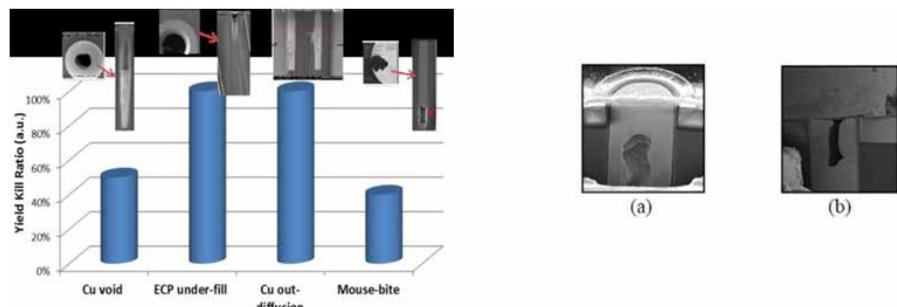


Figure 4: Recent publications [7, 8] highlight gap-fill related yield challenges that must be addressed as the industry transitions to volume manufacturing.

Cu barrier/seed results in gap fill up to four times better than that obtained with BEOL PVD. The Ti/Cu combination improves gap fill approximately two times over typical BEOL Ta/Cu technology. Given that the lighter mass of Ti results in poorer coverage than Ta, the Ti/Cu gap fill window results are exceptional.

Via fill by Cu ECD

As recent publications [7,8] indicate, the Cu TSV gap fill (**Figure 4**) and micro-pillar formation processes have presented significant challenges in terms of yield, reliability, and cost. Many of the TSV fill challenges are related to the choice of hardware, chemistry, and process control capabilities. Micro-pillar, required to enable high-density I/O in 3D DRAM, also has unique challenges such as bump co-planarity to enable high yield die-to-die stacking. Fortunately, many of the key TSV gap fill and micro-pillar coplanarity challenges have been addressed through advancements in hardware, process control, and chemistry design.

The TSV gap fill process is similar to but also very different from the BEOL damascene Cu gap fill process. Both processes involve full-face Cu deposition, require super-conformal deposition to achieve void-free fill, and rely on CMP to remove excess field Cu. However, the processes are very different with respect to dimensions, pre-wet requirements, seed layer sheet resistance, applied current density, process times, impact of bath control, process windows for gap fill, and organic additive design, among others.

The optimal

TSV gap fill process requires bottom-up, super-conformal filling technology, in which deposition at the bottom of the feature is accelerated while that in the field and on the TSV sidewall is suppressed (**Figure 5**). This is achieved primarily through chemistry design and control, but is also greatly influenced by current density control.

If the plating chemistry and the gap fill recipe are not designed correctly, the resulting process will have very narrow windows for void-free gap fill. For non-optimized processes, small variations in incoming wafer conditions or small variations in bath concentrations result in voiding during the gap-fill process. Such voiding issues are costly and have a negative impact on productivity in a high-volume production environment. **Figure 6** shows windowing data from a gap-fill process that has been designed for manufacturing with specific focus on ensuring wide performance margins.

The critical balance between field/sidewall suppression and via bottom acceleration can be easily disturbed by the buildup and accumulation of accelerator byproducts (**Figure 7**). Accelerator byproducts will complex with cuprous ions, forming species more active than the original accelerator. These complexes are unstable, extremely difficult to measure, and interfere with the

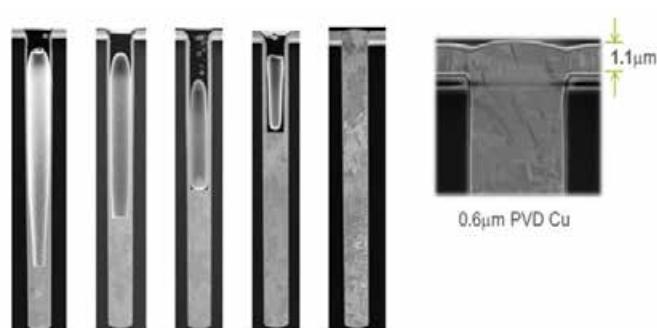


Figure 5: Partial fill cross sections showing an optimized 5x50μm TSV gap-fill process from initiation through complete via fill with slight over filling. For this wafer, the gap-fill time is 19 minutes with a total overburden of 1.1μm after plating.

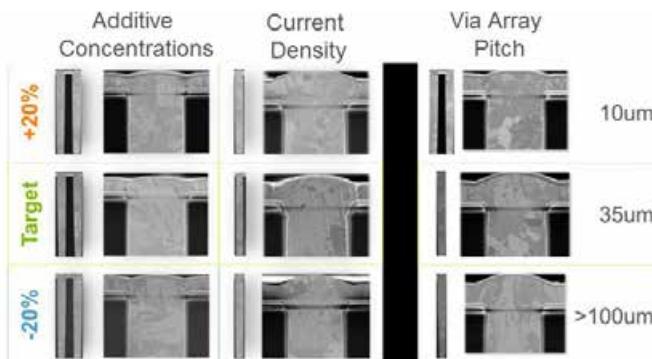


Figure 6: FIB/SEM cross sections of 5x50 μm TSV wafers showing stable, void-free gap fill for wide variations in additive concentrations, current density, and pattern density. Gap-fill process time is 19 minutes.

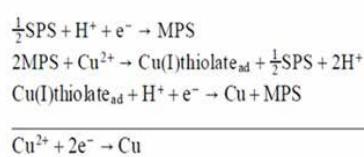


Figure 7: Accelerator facilitated intermediate reactions for Cu deposition showing formation of MPS and cuprous thiolate complex. Also shown is the TSV gap-fill response to MPS dosing.

suppressor and leveler polymers, blocking field and sidewall deposition, and disrupting the balance needed for reliable fill. Ignoring or mismanaging these byproducts results in yield loss and scrap because of unpredictable TSV underfill and voiding. Accelerator stability and the generation rate of accelerator byproducts are functions of the process design and control, and must to be accounted for early in the design.

A common approach to byproduct management is to increase chemistry bleed and feed

rates to counter byproduct accumulation. This is expensive, and does not address the real issue. A lower cost and more effective approach to the gap-fill yield and reliability challenge is to design the chemistry for accelerator stability, design the plating process and recipe to minimize accelerator breakdown, and incorporate hardware for continuous monitoring of the health of the plating bath. The results of this combination are a reliable, stable gap-fill process that will deliver high tool uptime, high productivity, and low cost for volume manufacturing (**Figure 8**).



Figure 8: Center and edge FIB/SEM cross sections from 10x100 μm TSV wafers processed at plating bath ages of a) 0 days, b) 10 days, c) 20 days, d) 30 days, and e) 40 days or ~4,000 wafers showing TSV gap-fill process stability on a production system out to a steady-state bath condition using a 10% daily bleed and feed.

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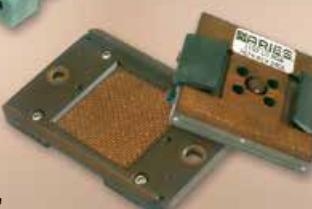
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Additional module cost savings can be enabled through optimization of the PVD and plating processes. As mentioned earlier, advancements in PVD technology have enabled higher step coverage in HAR TSVs. In addition to PVD advancements, Cu thickness requirements can be further reduced by controlling the oxidation rate of the Cu seed layer during the pre-wet process prior to plating and by increasing the nucleation density during the initial stages of Cu plating. Reducing oxygen in the pre-wet helps control corrosion, thereby reducing the PVD Cu thickness requirements. During the first several minutes of Cu plating, nucleation on and thickening of the sidewall Cu film are necessary to enable fast bottom-up, void-free fill. Optimization of the nucleation process has been shown to enable much thinner PVD Cu, delivering savings at PVD and CMP. CMP costs are a direct function of the amount of material being removed, so any reduction in field Cu is beneficial for overall module cost and helps reduce waste. **Figure 9** illustrates the thin seed capabilities and the reduction in total Cu overburden enabled by an optimized gap-fill chemistry and process.

Planarization by CMP

The polishing process removes Cu, barrier metal, and dielectric layers while maintaining tight control over topography

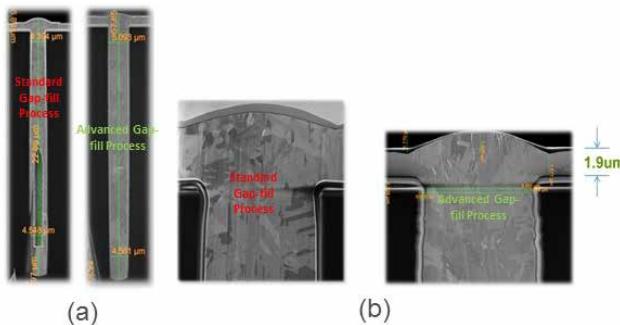


Figure 9: FIB/SEM cross sections of a) 5x50 μm TSVs with 200nm Ti/300nm Cu PVD illustrating how modifications to the gap-fill process can enable thinner PVD, and b) 10x100 μm TSVs with PVD Ti barrier showing a 40% overburden reduction with optimized PVD and ECD.

and defects. Although the typical post-ECD Cu overburden in TSVs can be an order of magnitude thicker than conventional BEOL Cu, Cu slurries for TSV operate at a high polishing rate, thereby lowering costs. The primary process criteria [9] for TSV CMP include profile control at high planarization efficiency, endpoint detection capability with tunable topography, high removal rates, and in-line cleaning capability. Full module integration is key and optimization of the plating process specifically can help

lower CMP costs by enabling lower PVD thicknesses and lower plated Cu overburden.

Co-optimization of unit processes

TSVs created in the middle-of-the-line are exposed from the backside of the wafer to allow connections to be made. This process is the companion to via-middle TSVs. Wafers are first bonded face-down on a temporary carrier and then mechanically thinned by grinding. The first challenge is managing the total thickness variation (TTV) of the bonded stack and the thinned device wafer. This variation can emanate from the non-uniformity of one or all of the following: 1) carrier thickness, 2) adhesive thickness, 3) via-middle etch depth, and 4) grind thickness. Hence, backside via integration requires that the process chosen accounts for these variations. Silicon CMP can be used to improve TTV and create a smooth, defect-free surface. More commonly, backside wafer thinning stops short of the TSV; the TSV remains below the surface of the thinned silicon wafer to ensure that Cu is not exposed. After CMP, highly selective silicon recess etch exposes the TSVs without damaging the liner oxide encasing them.

After the TSVs are revealed, low-temperature CVD nitride/oxide layers are deposited for isolation/passivation (**Figure 10**). The nitride serves as a Cu diffusion barrier and stress compensator, and the oxide provides strength to avoid potential pillar knock-off during the downstream dielectric CMP step.

In an optimized via-reveal sequence, the dielectric CMP process planarizes the resultant pillar and exposes the Cu TSVs with minimal

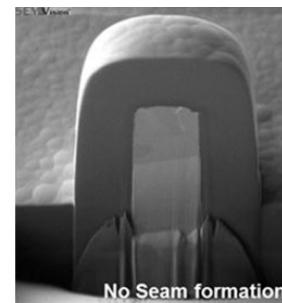


Figure 10: FIB/SEM cross-section showing improved nitride/oxide process (no seam at pillar base corner).

defectivity and smooth tunable topography, leaving a robust matrix of dielectric insulation between them for the subsequent RDL/bump process.

Micro-pillar formation

To facilitate high-density I/O on stacked silicon chips, new packaging approaches and technologies such as micro-pillar are necessary (**Figure 11a**) [8]. Several challenges directly associated with productizing a high-yield micro-pillar module include managing micro-pillar height uniformity or coplanarity to ensure robust connections at each and every I/O, controlling bump metallurgical and thermal mechanical properties through intermetallic compound engineering, and preserving bump adhesion through underbump metallization (UBM) wet etch optimization. UBM undercut is controlled during the low-cost wet etch process through the use of precision etch technology combined with advanced chemical development (**Figure 11b**).

Summary

Extensive co-optimization between TSV unit processes in etch, CVD, PVD, ECD, and CMP has led to an understanding of process trade-offs and integration knowledge necessary for successful volume ramp of TSV products. Specific focus on PVD and ECD TSV gap-fill and micro-pillar formation

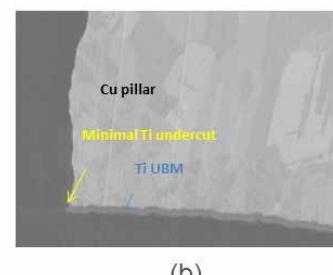
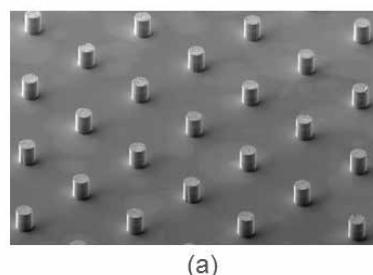


Figure 11: SEM images of a) electroplated Cu/SnAg micro-pillar array and b) FIB cross-section of the UBM/Cu pillar interface showing optimized undercut.

technologies has resulted in processes and hardware optimization that address key yield and defectivity challenges. Future work will continue to focus on extending these processes to smaller, higher aspect ratio TSVs and micro-pillars to meet device scaling requirements.

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Versatile stacking process for heterogeneous 3D integration

By Thomas Uhrmann, Jürgen Burggraf, Julian Bravin, Markus Wimplinger, Paul Lindner [EV Group]

3

D-IC stacking utilizing through-silicon via (TSV) technology holds the key to extending Moore's Law by enabling greater semiconductor device performance in smaller form factors without further lithographic scaling, and is moving closer to high-volume production for several applications. Multiple TSV processing flows, such as via-middle and via-last, are being considered based on the target application and functionality of the stacked IC layers. With both process flows, TSVs are formed after finishing the front-end device and metallization processes, where the electrical connection is done on a micrometer or tens of micrometers scale. This approach, however, limits integration density and bandwidth. For this reason, the call for further upstream integration schemes is getting louder and more specific.

In addition to density and integration, another driver for alternative integration concepts is the lack of cost-efficient patterning to enable the further progression of Moore's Law, which has led to a rise in transistor costs at the most recent lithographic patterning nodes [1]. As a consequence, 3D integration at the front-end manufacturing stage (often referred to as monolithic 3D devices or heterogeneous integration) is moving to the center stage of interest. In this case, functionality is added to the device layer by layer. This stacking can be accomplished by two methods: sequential epitaxial growth of silicon layers and fusion bonding.

The sequential epitaxial growth of silicon layers has been considered for heterogeneous integration because 3D devices are stacked bottom-up in a layer-by-layer fashion, which goes hand-in-hand with today's epi process flows. However, it requires high-temperature annealing, which causes considerable stress on the underlying device layer that can lead to diffusion and yield challenges.

In contrast, fusion wafer bonding enables much greater process flexibility in terms of temperature stress and process

separation. Both wafers are individually processed, which means that normal temperature restrictions apply without the need to consider thermal budget or history of the underlying layer. In addition, process recipes and wafer characteristics remain the same when manufacturing each transistor layer on a prime silicon wafer, which helps maintain high process control and yields. In the case of silicon thin-film transfer or epitaxial techniques, however, the underlying transistor and interconnection layers influence and change the substrate characteristics with each added film or layer. This causes process engineering costs to multiply and the cost of yield loss to be detrimental.

Fusion wafer bonding schemes

Several 3D integration schemes at the front-end manufacturing stage are feasible using fusion wafer bonding, as shown in **Table 1**. A principle differentiator is the orientation of the transistor layer after bonding. The first integration method is silicon thin-film bonding, where a thin silicon film is transferred without any active areas. This is a straightforward process with similar steps compared to epitaxial growth. However, whereas with epi it is difficult to grow defect-free crystalline silicon films, the transferred silicon film is as good as the wafer from which the film came. No epitaxial defects arise because of restricted growth temperature, which results in a high-quality layer of silicon. At the same time, however, these temperature restrictions create their own challenges to

Front-End Stacking by Wafer-Level Fusion Bonding					
	Face-to-Face			Face-to-Back	
	Si film transfer (Via-Last)	Full Area Fusion Bond (Via-Last)	Hybrid Bonding	Full Area Fusion Bond (Via Last)	Hybrid Bonding
Device Layer Stacking	No	Yes	Yes	Yes	Yes
Integration Density	Medium	Medium	High	Medium	High
Process Temperature	400-600°C	200-300°C	300-400°C	200-300°C	300-400°C
Bond Alignment	μm-scale	<200nm	<200nm	<200nm	<200nm
Temporary Handling	No	No	No	Yes	Yes

Table 1: Comparison table of potential front-end 3D stacking processes by fusion bonding.

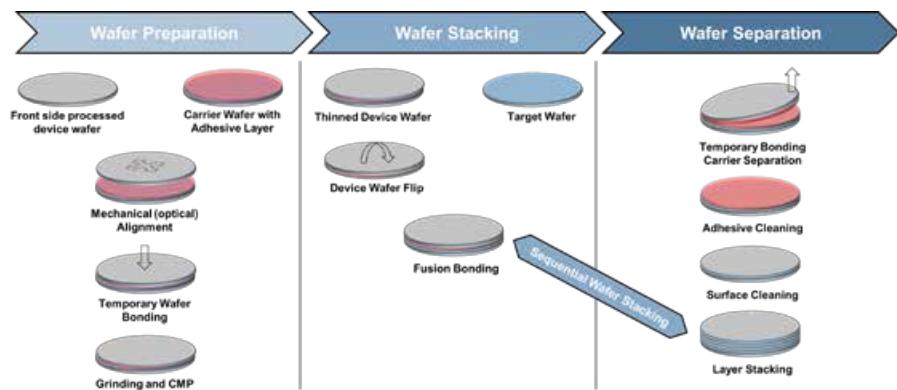


Figure 1: Schematic process flow for heterogeneous face-to-back integration using a temporary carrier wafer for thinning and subsequent stacking.

the underlying transistor layers by limiting the temperature budgets allowed for dopant activation.

A second integration method is full-area transfer of a thin-processed semiconductor film using a face-to-face full-area dielectric bond, where the fully processed transistor wafer is thinned after bonding. With this scheme, a via-last conduction process is needed to connect the transferred semiconductor film to the underlying device layers. Transistor process steps are separated and no additional thermal processes are added to the target wafer other than for TSV interconnects.

A third integration flow is face-to-face hybrid bonding, where a dual damascene copper and silicon-oxide hybrid interface serves as both the full-area bonding mechanism and the electrical connection. Hybrid wafer bonding process flows are gaining considerable attention as critical supporting technologies for TSV processing, because wafer bonding simultaneously enables both the mechanical and electrical connection between individual chip layers.

Several device architectures would benefit if the transferred film has the same orientation as the base substrate, also referred to as face-to-back integration. In this case, the orientation of the wafer remains the same throughout the entire process flow—face up from the thick processed wafer until the stacked device. One clear advantage of the face-to-back approach is the possibility of stacking multiple wafers with the exact same layout, while for face-to-face stacking the layout needs to be mirrored. The risk of wafer damage and scrap during wafer thinning is reduced with face-to-back integration, because thinning is done on an intermediate carrier before being stacked on the final device. Lastly, and most importantly, less real estate of the circuit is being consumed by interconnect structures. For downward-facing transistors, two separate vias need to be etched and filled, leading to a U-shaped interconnect structure.

Temporary carrier mounting of the device wafer

Temporary bonding is the first key process step for face-to-back 3D integration. Special bonding adhesives are used to attach the device wafer to a suitable carrier wafer temporarily in order to ensure stabilization during thinning and backside processing of the device wafer. In this way, standard semiconductor equipment

and process solutions can be applied for further processing of thin wafers. Because semiconductor processing involves a variety of different chemical, thermal and plasma processes, the selection of the right adhesive is essential and material properties and functions are often contradictory.

Figure 1 shows a general process flow for temporary carrier mounting. The device wafer is mounted face-down onto a carrier wafer. Rigidity of the adhesive system is fundamental for this process flow. For

this reason, thermoplastic adhesives, which offer high mechanical rigidity at room temperature and good cleaning properties, have been used [2]. Curing of thermoplastic adhesives is highly important to drive out all containing solvents from the adhesive layer. Samples have been cured at three different curing temperature levels of 120°C, 150°C and 180°C for three minutes each.

Figure 2a shows a thickness map obtained by IR interferometry using

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the inline metrology module on the EVG850TB automated temporary bonding system [3], which reveals a total thickness variation (TTV) after coating and baking of 400nm for an adhesive thickness of 20 μ m. In a subsequent step, the device wafer is aligned mechanically onto the wafer carrier, typically leading to an accuracy of around 50 μ m. Alignment for temporary bonding is much less critical compared to stacking; however, it needs to be good enough to provide support of the valuable device wafer at any time during grinding,

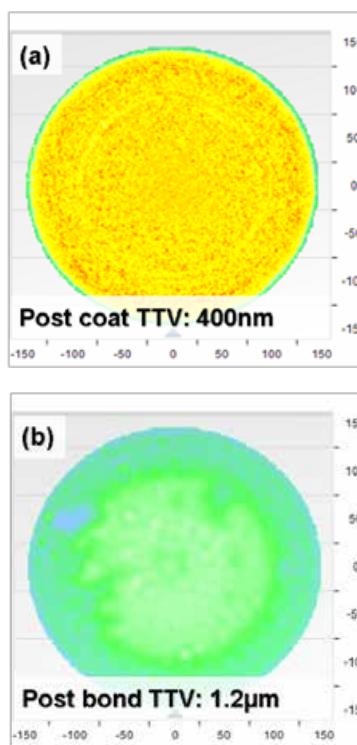


Figure 2: Adhesive thickness map of a 300mm carrier wafer coated with 10 μ m-thick thermoplastic adhesive, qualified with the in-line metrology module on the EVG850TB bonder: a) adhesive thickness map after coating and baking, revealing a TTV of 400nm; b) post-bond thickness map of carrier and device wafer showing a stack TTV of 1.2 μ m.

polishing and backside processing. Subsequently, both wafers are bonded under vacuum applying standard conditions for thermoplastic adhesive [2]. By applying heat above the glass transition temperature, the adhesive film is able to reflow and bond to the carrier. Due to the reflow, the TTV after bonding is slightly increased to 1.2 μ m, as shown in **Figure 2b**.

For wafer back-grinding, an industry-standard multi-spindle grinder has been used to remove most of the wafer thickness using coarse grinding. In a subsequent fine

grind and concluding chemical mechanical polishing (CMP) step, the wafer backside shows sufficient minimal surface roughness suitable for direct wafer bonding. For this experiment the TTV of the device wafer is 2.0 μ m for a device thickness of 10 μ m on 20 μ m-thin thermoplastic adhesive. We note TTV evolves during processing because of multiple factors such as spin coating and baking, which largely determine the flatness and subsequent TTV. Furthermore, during bonding, the adhesive re-melts and pressure is applied to both wafers, which in turn means that pressure and temperature uniformity are crucial. Even prime silicon wafers already contribute up to 2 μ m TTV. Alternatively, silicon-on-insulator (SOI) wafers can be used for transferring the thin silicon film because the surface layer of silicon can be manufactured more precisely and back-grinding can be stopped within the buried oxide layer.

Wafer stacking

As noted earlier, oxide-to-oxide fusion bonding and hybrid bonding with oxide/copper interfaces are two processes that can be used to stack multiple device layers. The main advantage of hybrid bonding is the considerable savings in silicon real estate that are achieved as a result of the connection already being embedded in the interface. For via-last connections, etching and keep out zones for vias consume a considerable amount of the substrate.

Both hybrid and full-area oxide bonding are achieved in two steps. First, hydrogen bridge bonds are formed between both substrates. Next, an annealing step converts instantaneously formed hydrogen bridges into permanent covalent bonds. This transfer normally requires annealing temperatures between 700°C and 1100°C, which would prevent its use in CMOS processing where process temperatures are restricted to a maximum of

400°C for logic device wafers, and less than 300°C for memory wafers. However, plasma treatment of both wafers lowers bonding temperatures to the required range [4-7]. Furthermore, surface roughness needs to be well

below 1nm to achieve good fusion bonding yield. In this study, CMP led to a roughness of 0.26nm. Both polished wafers were subjected to a 30-second plasma activation step. Prior to bonding, both wafers were rinsed with deionized water to ensure particle-free wafer surfaces. Furthermore, the rinse provided a water termination on the wafer's surface, which is essential to form hydrogen bridges between both wafers. Further insight and detailed modeling of fusion bonding has been published [6,7]. Previous experiments have shown that a suitable plasma activation step results in an initial bond strength between 0.2 and 0.6 J/m² [7]. Such high bond strength enables the safe detachment of the temporary carrier wafer in the subsequent process steps.

High alignment accuracy of both wafers is a key step for heterogeneous device integration using via-last or hybrid bonding. Depending on the level used for interconnection and the transferred device layer thickness, via diameters can range from a few hundred nanometers to several microns. Highly accurate wafer-to-wafer alignment enables the accurate overlay between contact pads for via-last TSV etching or landing-pads for hybrid bonding interconnect structures. Alignment accuracies down to 200nm (3 sigma) have been shown by face-to-face bond alignment [7-10].

Carrier separation

After the thin device film is bonded to the device wafer, the carrier wafer is separated from the stack, which opens the surface for the next layer. Thermoplastic adhesives offer the advantage of solvent cleaning after debonding to remove adhesive residues prior to stacking additional layers. In fact, cleaning the temporary bonding adhesive is an essential step, since fusion bonding is highly sensitive to contamination, which can lead to decreased bonding yield. In this study, thermal-slide debonding has

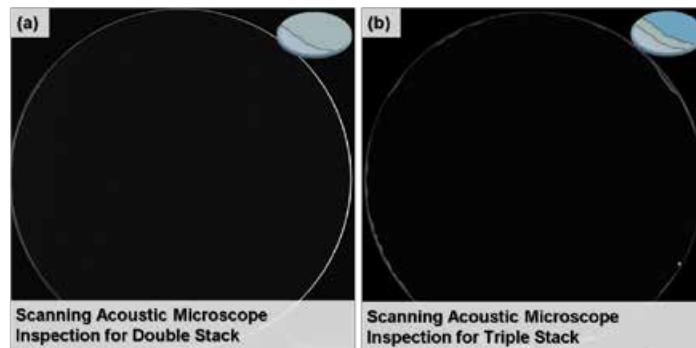


Figure 3: Scanning acoustic microscopy (SAM) measurement of a single transferred silicon layer a) and two stacked silicon layers b) on a 300mm silicon target wafer.

been applied for carrier debonding. Slide-off debonding makes use of an inherent property of thermoplastic adhesives, which is decreasing rheology as temperature increases. Carrier detachment is achieved by heating the wafer stack to 180°C on the thermal-slide debonding module, where the carrier is separated by applying shear force. A final solvent cleaning step is used to remove residual adhesive from the device wafer stack.

Several experiments have been carried out to transfer thin carrier-mounted silicon layers onto a 300mm target wafer by fusion bonding. Fusion wafer bonding yield has been investigated using surface acoustic microscopy (SAM), enabling the inspection of the bonding interface in a non-destructive way (**Figure 3**). All investigated samples show a high bonding yield without any voids at the bonding interface. Furthermore, several wafer stacks have been diced and the cross-section has been further analyzed using standard optical microscopy and scanning electron microscopy (SEM) techniques (**Figure 4**).

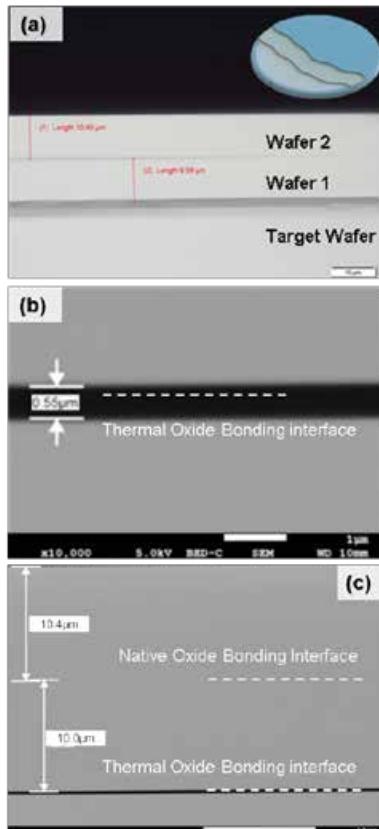


Figure 4: a) Optical microscope cross section through a bonded triple stack; b) high magnification scanning electron microscopy (SEM) image of the bonding interface between a thick target wafer with 0.55µm thermal oxide and the first stacked thin wafer; c) low magnification SEM image of the whole stack.

It should be noted that the first plasma activation and bonding step has been carried out on a landing wafer with a 0.55µm-thick thermal oxide layer on top. The second stacking process has been carried on two native oxide interfaces. Even in the case of very native oxide films, a high bonding yield has been achieved with no visible voids present across the 300mm bond area.

Summary

Heterogeneous or monolithic integration processes offer great potential to increase semiconductor integration density. Full-area fusion and hybrid bonding techniques are under development and alignment accuracy is crucial to precisely stack individual transistor layers and ensure minimum via keep out zones to achieve the highest levels of integration. Traditionally, face-to-face alignment and stacking of

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two individual wafers has been applied. However, the possibility of applying face-to-back stacking of devices using an intermediate handler for wafer thinning and stacking opens up further integration options. Processing and stacking of ultra-thin carrier-mounted device layers on thermal oxide has been shown. Fusion bonding on cleaned temporary bonding interfaces is very promising for sequential stacking of additional device layers. Face-to-back process flows in combination with

high-accuracy bond alignment open the gates for more flexible integration of next-generation 3D-ICs.

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Reducing the cost of probe card test and repair

By Greg Olmstead, John Strom, Bill Favier, Foster Lin, Brett Strong [Rudolph Technologies, Inc.] and Simon Allgaier [FEINMETALL]

As integrated circuits (IC) have continued to grow more powerful and more complex, the number of connections required to provide communication between the circuit and the outside world has increased rapidly. A single die may now have over a thousand such connections. A 300mm wafer contains many die, resulting in over 100,000 total connections per wafer. Automatic test equipment (ATE), used by IC manufacturers to measure the performance and functionality of their products, may be designed to test many die (up to a full wafer) simultaneously, in order to reduce the time required for testing. ATE uses probe cards containing precisely positioned probes, one for each contact, to provide electrical and mechanical connections between the tester and the circuit.

A single probe card may contain over 100,000 probes, each of which is spring loaded to provide reliable contact when it is lowered to the surface and then “overtraveled” to create a forceful scrubbing action on the contact surface that breaks through the surface oxidation layer. Each probe must be checked periodically to ensure it is properly positioned and free of contamination. Probe card analyzers provide high-speed automated test and repair capabilities for probe card maintenance. The analyzer requires a customized interface to provide electrical and mechanical connectivity between itself and the card being tested. The cost of these interfaces has increased dramatically with the increasing number of probes. An important consideration driving this increasing cost is the requirement that the card is not deformed by the forces applied to it as the probes are moved to the overtravel position. Although the force on each probe is small, the total force can be quite large when many probes are tested simultaneously. Probe card interface (PCI) manufacturers make great efforts to insure that any deformation that occurs in the probe card analyzer (PCA) models precisely the deformation that occurs when the card is used in the ATE.

While automated, high-throughput PCI-based probe card test and repair may be warranted in a high-volume production environment, there are many other use cases where the cost of maintaining an inventory of PCIs is economically burdensome, including: 1) Probe card manufacturer production: new tester interface introduction and other low-volume manufacturing; 2) Probe card manufacturer service center: probe card repair; 3) Probe card customer: incoming QA, troubleshooting; and 4) Probe card manufacturer/customer: R&D testing.

Is there a test strategy that can deliver the required test and repair capability at a lower cost in the use cases listed above? More specifically, can the cost of probe card test and repair be reduced by eliminating the PCI? Basic mechanical test requirements include measuring of the planarity of the free probe tips and the alignment of each tip with the test pad in free and overtraveled positions. Electrical tests include component testing, leakage/capacitance, contact resistance, primary channel wiring, and the detection of short circuits in the wiring. We have developed a testing approach that replaces the conventional probe card interface with a simplified, low-cost probe card holder (PCH). The PCH positions the probes in a plane parallel to the reference plane (check plate), supplies minimum hold down force to prevent movement of the card during test, and holds the card so that it can be flipped when a probe needs to be cleaned or repositioned. In addition, the holder provides a single electrical connection to the ground plane of the card. As the results presented below demonstrate, we were able to meet most of the basic test requirements using this approach.

Mechanical testing

The essential compromise, made to accommodate the lower volume applications targeted by this development effort, was to reduce throughput to save cost. Rather than testing a large number of probes simultaneously, the PCH approach tests probes individually or in small groups

(Figure 1). In the PCI approach, the planarity of a large number of probes is measured simultaneously by reducing the distance between the card and a conductive

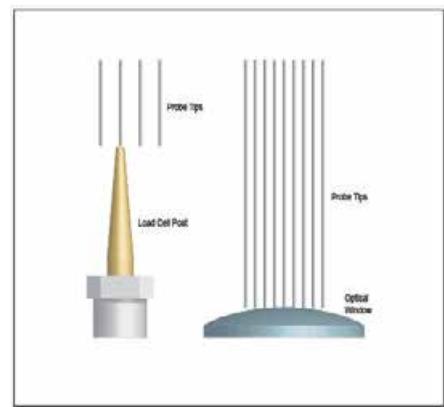


Figure 1: The PCH approach uses a load cell to provide force-based measurements of probe height for planarity. For alignment measurements, a slightly raised window contacts only a small number of probes at any time.

check plate and noting the distance at which each probe makes electrical contact. With the holder approach, the free height of each probe is measured individually using force-based contact detected by a precisely positionable load cell. This avoids the requirement for a large number of electrical connections between the card and the analyzer and reduces the force exerted on the card to a negligible level.

Planarity is tested first since good planarity is required to ensure accuracy in the subsequent optical measurements of alignment and scrub. These measurements are made using a small optical window that contacts only a limited number of probes at any time. The alignment of each probe is measured just before contact with the window (free position), and when the window has been raised to the specified overtravel position. From these basic measurements the system can calculate various characteristics of probe alignment and scrub, including X error, Y error, scrub length, scrub area, scrub angle, probe diameter, probe force, spring rate, and more.

To confirm the validity of the measurements we compared results obtained with a PCI and PCH using a

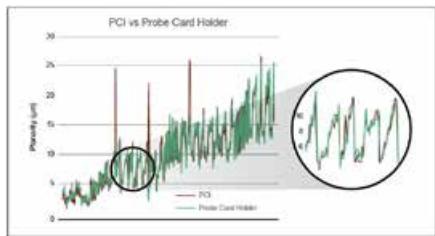


Figure 2: Comparison results of PCI (red) and PCH (green) planarity measurements. The magnified view demonstrates the close agreement of the measurement approaches.

Rudolph PrecisionWoRx® VX4 PCA on a Feinmetall ViProbe® probe card having a 35mm X 35mm active area with 3508 probes (2484 bussed). Results are shown in **Figures 2, 3 and 4**. Agreement between the measurement results of the two approaches is very good. The force-based planarity measurements made with the PCH show less sensitivity to contamination than the electrical planarity measurements made with the PCI.

Electrical measurements

After the mechanical testing described above, we evaluated the ability of the PCH

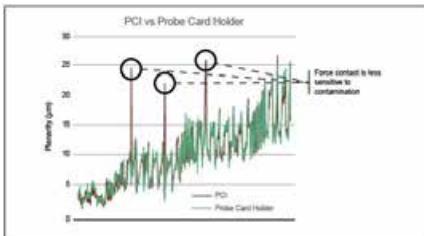


Figure 3: Electrical planarity measurements are more sensitive to errors caused by contamination on the probes.

approach to provide the required electrical measurements. The holder provides a single electrical connection to the ground plane of the card. In addition, the load cell post can be programmed to move automatically to any probe to provide electrical contact. Finally, the operator can use a handheld device to achieve electrical contact to any channel on the tester side of the card. These contacts can be combined to provide almost all of the electrical test capabilities available with a PCI.

Component testing. Component testing involves a combination of the ground connection and individual probe contacts. Selected probes permit automatic testing of all components

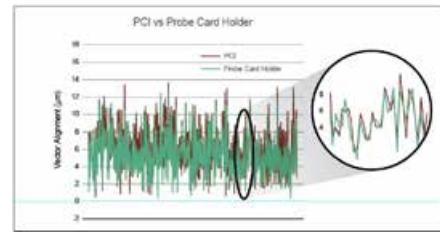


Figure 4: A comparison of PCI (red) and PCH (green) alignment measurements also shows good agreement.

connected to the ground plane.

Leakage/capacitance. The ground connection and individual probe contacts can be used to automatically evaluate leakage and capacitance to ground of all probes.

Contact resistance and primary channel wiring. By moving the “ground” connection to selected contacts on the tester side of the card, and the load cell connection to the corresponding probe, the operator can manually measure contact resistance and confirm the primary channel wiring. Bussed probes, which typically constitute a large proportion of probes, can be measured automatically without

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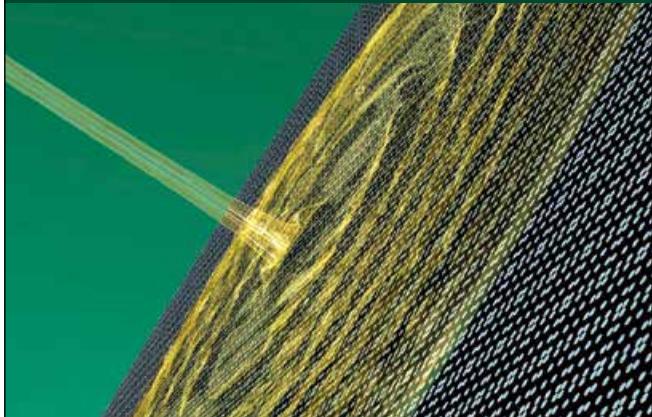
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repositioning the tester side connection. For pathways that do require tester side contact selection, a “User Assist” capability provides a visual representation of the tester side contacts to guide the operator to the appropriate location. In our testing, we found that with “User Assist,” operators could reliably measure non-bussed probes at a rate of 20 to 30 per minute.

Wiring short circuits. Wiring short circuits proved to be one area where the holder approach had difficulty. In the PCI approach, where all channels are monitored simultaneously, a short circuit can be readily detected. The same is not true with the single tester side contact provided by the holder approach, and it is not practical to test a large number of tester side contacts manually. It is an area we are continuing to investigate for holder-based solutions.

Test	PCI	Probe Card Holder
Planarity	Yes - Electrical	Yes - Force
Alignment	Yes	Yes
Components	Yes	Yes
Leakage/Capacitance	Yes	Yes - To ground plane
Contact Resistance	Yes	Yes - Semi-automatic
Wiring - Primary Channel	Yes	Yes - Semi-automatic
Wiring - Shorts/Opens	Yes	No
Cost	High	Low

Table 1: Summary of comparison of PCI and PCH test capabilities.

Summary

Table 1 summarizes our conclusions regarding the capabilities provided by PCI and PCH approaches to probe card testing. PCH provides complete coverage of all mechanical testing requirements and also matches most of the electrical testing capabilities of the PCI approach. Automation of the probe side connections and the User Assist feature deliver faster measurements than might otherwise be expected from a single contact, interactive method.

In addition to broad coverage of basic test requirements, the PCH approach offers other advantages. The holders are easy to make and can often be manufactured in-house with very short lead times. The approach allows simplified probe card definitions. No printed circuit board (PCB) is required for measurements of planarity and alignment. The holder does not require a PCA with Pogo blocks – potentially reducing the cost of the PCA. The cost of a holder is very low compared to the cost of an interface.

Biographies

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UV solid-state laser ablation for embedded fine-scale circuitry

By Dave Myles, David Milne /M-Solv/

Miniaturization in the semiconductor industry continues to be driven by Moore's law, but current manufacturing technologies for IC substrates and interposers are unable to meet the feature size requirements of next-generation advanced packaging architectures at the right cost. Laser embedding conductors within a dielectric offers a number of advantages for patterning fine-scale circuitry when compared to conventional printed circuit board (PCB) manufacturing technologies. Ablation of features down to a resolution of 2µm L:S, and vias down to 5µm diameter allows more signal routing per layer and addresses the technology gap between semiconductor and PCB manufacturing technologies. A new technology has been recently introduced to the market, called Scanned Mask Imaging (SMI) that enables high-resolution, direct laser etching of 3D structures in organic dielectrics through use of cost-effective, low maintenance, ultraviolet (UV) solid-state lasers.

The technology gap

There are many advantages in being able to manufacture IC substrates and interposers with circuitry defined at the few microns scale. More routing can be included per layer, reducing the number of layers required. This not only reduces the height profile of the package, but also the path length of the conductor through the package, thereby reducing signal latency. Fine-scale circuitry in organic substrates enable 2.5D interposer architectures that are able to operate faster and at reduced power consumption, as well as reducing the footprint of the package. The infrastructure already exists for the production of silicon interposers using semiconductor manufacturing technologies, however these have not been widely adopted because of their high manufacturing costs and the poor electrical properties of silicon. The infrastructure for IC substrate and PCB manufacture is well developed and has the potential to provide solutions at the right cost. Current manufacturing technologies, however, are unable to produce feature sizes below 10µm, falling short of the requirements

dictated by IC circuit designers for next-generation organic interposers and advanced chip packages.

Laser embedded conductors (LEC) offer a solution to address this technology gap, enabling the cost-effective production of circuitry with feature sizes in the range of 1-10µm. LEC uses pulsed lasers to create 3-dimensional relief structures in the surface of a dielectric substrate, into which copper is plated to form the circuitry by a sequence of electroless and electrolytic plating steps. The process flow can be seen in **Figure 1**. By using laser ablation in this way, a technique is realized that avoids the less environmentally friendly, multi-step lithographic processes currently used in IC substrate manufacture. LEC can also take advantage of the variety of low-cost, low-k, organic dielectrics already

also improves co-planarity between layers in the package, thus improving layer-to-layer alignment. Embedded conductors are also better adhered to the substrate, enhancing peel strength, due to having a contact area with the substrate approximately 3 times greater than that of a conductor of the same width formed on the surface of a dielectric.

Laser processing for high-resolution patterning

A variety of laser sources exist with a broad gamut of properties, used in a diverse range of applications. For high-resolution ablation of organic dielectrics, short-pulse lasers that emit light in the UV region of the electromagnetic spectrum are most suitable. This is on account of a number of reasons. Firstly, the minimum feature size resolvable by an optical system is directly proportional to the wavelength of light used to illuminate it, so short UV wavelengths enable the machining of smaller features. Secondly, absorption of light in organic materials is usually stronger at shorter wavelengths. A schematic of UV laser ablation can be seen in **Figure 2**. The high absorption coefficient (α), or short optical penetration depth, shown in many materials in the UV, means that most of the laser energy directed at the substrate is absorbed in a very small volume at the irradiated site. This also limits the heat affected zone (or HAZ, usually associated with deleterious thermal effects). As well as the requirement to emit light in the UV, the laser source must also deliver the light in short pulses to limit the thermal penetration depth in the material. Finally, the laser needs to have a high average power, since the throughput of such a laser process is largely proportional to the total average laser power available.

The requirements noted above greatly restrict the laser sources suitable for high-resolution, high-throughput patterning of organic dielectrics. There are currently two main contenders in this market: excimer lasers and frequency tripled, diode-pumped solid-state (DPSS) lasers. Excimer lasers are gas lasers that can emit light at different wavelengths in the UV range depending on the gas used as a gain medium. The gases with the longest lifetime and highest

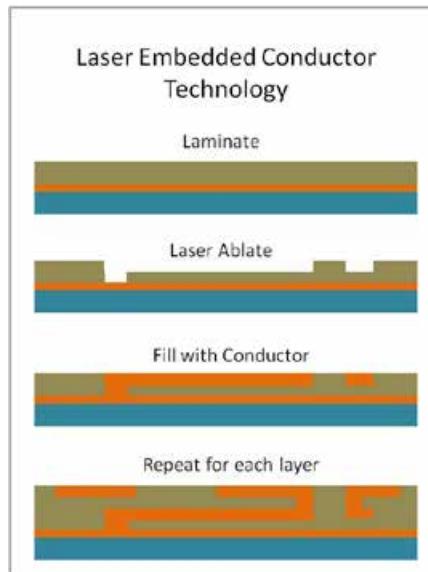


Figure 1: The process flow for laser embedding conductors within an organic dielectric by direct laser ablation.

available on the market. By laser drilling vias in the same process step as laser ablating the circuitry, excellent registration between the two types of features is implicit and no additional laser blind micro-via drilling equipment is required. Embedding the conductor in this way, as opposed to forming a raised conductor on the surface of a dielectric,

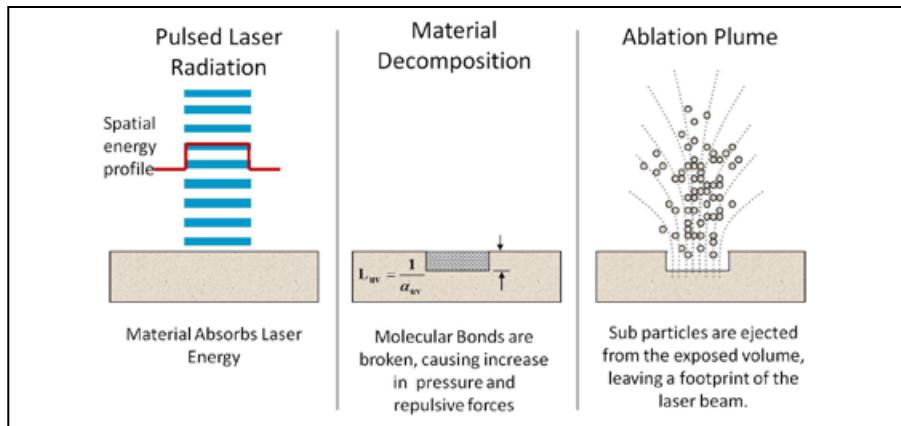


Figure 2: The mechanism of pulsed UV laser ablation of organic materials.

average power, and therefore the lowest cost per watt, emit light at 308nm and 248nm. Excimer lasers produce low-coherence light that is well-suited to imaging applications, so these lasers are often used to illuminate a photomask, which is subsequently imaged and de-magnified onto the substrate by a projection lens. The photomasks are typically a reflective chrome or aluminium coating on a quartz substrate. The metal layer is patterned such that the energy from the laser

only reaches the substrate via the transparent areas of the photomask. Excimer lasers have the highest average power available in the UV range, and are known for their excellent process quality. This quality, however, comes at a cost. As well as the high purchase price of the laser, excimer lasers require a maintenance schedule involving frequent servicing and replacement of costly components. Stainless steel gas lines must be installed in the factory to safely deliver the

toxic and corrosive gases used by these lasers. The high pulse energy and short wavelength can also shorten the lifetime of beam delivery optics. All of these factors combine to create a relatively high cost-of-ownership compared with a UV DPSS laser.

The high coherence of single-mode UV DPSS lasers make them well suited to focusing the beam down to a small spot. The beam can then be deflected across the surface of a substrate by a galvanometer scan head to ablate features in “direct write” mode. The ablated pattern is defined by a CAD file sent to the scan head, so changes to the design can be made on the fly – making these systems very flexible. However, because these systems mark every vector in the CAD file sequentially, complex designs can be time consuming to process. Complicated control systems are required to keep the focused beam speed constant across the substrate in order to achieve good depth uniformity. It is also challenging and time inefficient to ablate large features and ground plane regions with a small focused spot, placing restrictions on the circuit design. These systems, although having the right capital cost, are thus too slow for high-volume manufacture of feature dense advanced packages.

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Scanned Mask Imaging: the alternative

Multimode, nanosecond, UV, DPSS lasers have higher average powers than their single-mode counterparts, however the beam properties make them better suited to imaging rather than focusing. These lasers produce pulses at a much higher frequency than excimer lasers, and subsequently have much lower pulse energies. Therefore, to use these lasers to illuminate a photomask, the beam size at the photomask must be much smaller than for the excimer laser to achieve the

same fluence (energy per unit area). The novel solution is to use a galvanometer scan head to raster scan the UV DPSS beam across the photomask at high speed to illuminate the pattern of the circuit layer, which is subsequently de-magnified through a projection lens and ablated into the target material. This scan process is shown in **Figure 3**.

Although the mask is static as it is scanned, the mask is mounted on a linear stage to allow the overlay of two separate images at the substrate. This allows the machining of different features

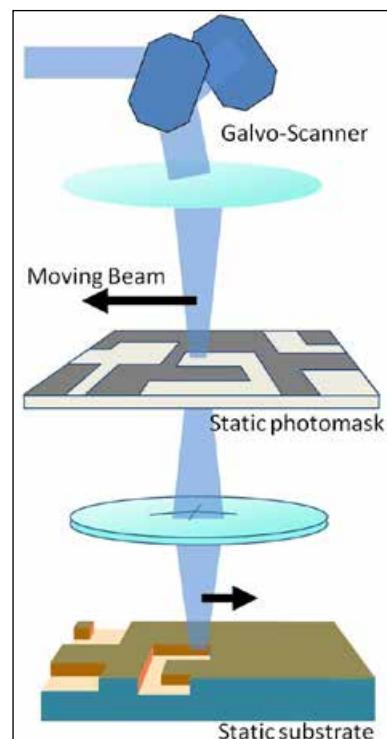


Figure 3: Scanned Mask Imaging system schematic. The static photomask is raster scanned by a galvanometer scan head. The image of the photomask is relayed and de-magnified onto the substrate by a projection lens.

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to different depths, for example the machining of tracks, pads and ground planes to one depth, followed by the drilling of micro-vias down to the layer below. The illumination pattern, which is commonly a simple raster pattern of parallel lines, is defined by a list of vectors sent to the scan head. The ablated depth of the features can easily be tuned by changing the pattern and beam speed at the mask. This tuning controls the number of pulses each area of the substrate receives, and with each pulse removing a finite amount of material, accurate depth control is possible. The illumination can be varied in many ways so as to allow the user full control of the process. For example, the user could elect

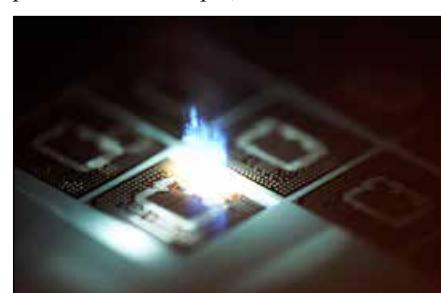


Figure 4: Photograph of SMI ablation part way through the scanning of a chip-scale package device layer.

to illuminate the mask slowly in a single pass, or quickly with multiple passes, and thereby optimize the quality and ablation rate in the material. A snapshot of the process at the substrate can be seen in **Figure 4** midway through scanning the photomask.

Although multimode, UV, DPSS lasers still have a lower average power than excimer lasers, the cost per watt of laser power is much lower. By multiplexing, M-Solv's MSV-302C production tool uses multiple laser sources to illuminate two optics heads, processing panel size substrates up to 20x24" in parallel with a throughput exceeding that of a single-head excimer system. Because of the lower capital cost and running cost of UV, DPSS systems, all this can be achieved with a cost-of-ownership that is a fraction of that of an excimer system.

Results

The quality of the SMI direct ablation process can be seen in **Figure 5**, where 3 μm L:S features have been patterned

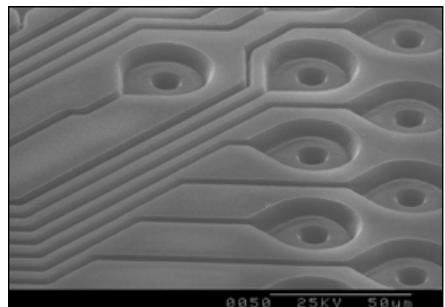


Figure 5: SEM micrograph of an exemplar fan-out device ablated into polyimide. The diagonal lines are 3 μm L:S. The micro-vias are 10 μm in diameter.

and well registered to 10 μm vias. **Figure 6** shows the ablation of 10 μm line width and space features with 33 μm vias ablated down to the visible copper layer below. The registration of the pads with the vias highlights the potential to reduce the capture pad size to give more routing space. **Figure 7** shows the ablation of an exemplar fan out device with 3 μm L:S tracks and 10 μm vias. This process quality, previously only achievable by excimer laser ablation, can now be accomplished with a more cost-effective laser source.

Through the use of high-resolution optics, it is possible to machine features down to 2 μm L:S. Increasing the fluence at the substrate steepens the side walls of the ablation, giving some control of feature profile and maximum aspect ratio.

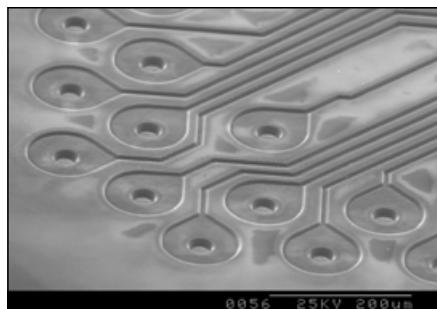


Figure 6: SEM micrograph of a fan-out device with 10 μm L:S diagonal lines. The micro-vias are 33 μm in diameter, and it can clearly be seen that they have been ablated down to the copper layer below.

Summary

Laser embedding conductors offers a solution to the technology gap that has emerged between IC and PCB manufacturing technologies. Fine line patterning of features down to 2 μm in standard, low-k, organic dielectrics meets the demands of next-generation chip packages, while avoiding the multi-step, wet chemical processes associated with lithography. Laser drilling vias in the same process step as laser ablating redistribution layers removes the need for additional micro-via drilling equipment, while also improving the registration between the two features. UV excimer lasers are able to meet the desired quality of process, the technology, however, has not yet satisfied the economics of production. By utilizing UV DPSS lasers, SMI technology is able to reduce the cost of the ablation process significantly, thereby increasing the probability that laser embedded conductors will eventually be realized in a production environment.

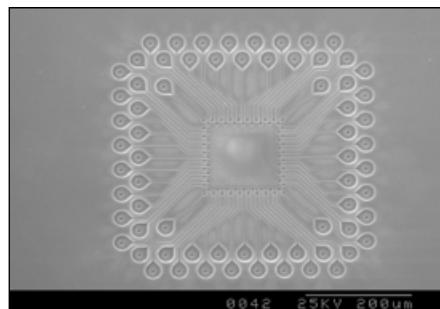


Figure 7: SEM micrograph of an exemplar fan-out device with 3 μm line widths and 10 μm diameter micro-vias.

Biographies

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Advances in test and burn-in

by Colin Koh, Muhammad Syafiq [Test Tooling Solutions Group]

The need for thinner and wider smart hand-held devices with increased capabilities has pushed the boundaries of chip testing. Two fast moving trends are wafer-level chip-scale packaging (WLCSP) and full-function probe testing. The implementation of WLCSP has helped to reduce the cost of packaging by simplifying device packaging. Ironically, the use of simplified assembly structures and processes for WLCSP has increased the demands placed on testing, necessitating upgrades to the test system and its ancillary components.

One main difference between testing at the wafer-scale package level and traditional “single-part” testing is the signal specifications, which have now been moved to the wafer-level environment. Multi-site final test is critical in achieving the best economy of scale without degrading the signal performance requirements. Note that, with multi-site testing, design engineering of the pin to pad alignment has to take on greater precision. It also means that conventional single-part testing is not very useful during the manufacturing process. The challenge for wafer-scale package level testing involves variation in the coplanarity and the stack-up heights that become amplified as WLCSP devices are final-tested on a common wafer.

The conventional single-part test allows a high quality of mixed-signal system-on-chip (SoC) devices to be tested. In addition, there is a legacy methodology of probing that is used for pure digital and memory testing. Therefore, multi-site final testing calls for wafer-scale testing that allows for efficiency in testing without frequent change and reconfiguration of the automated test equipment during high-volume manufacturing (HVM).

WLCSP with multi-test site contactor

The test process begins with a 1.0mm pitch fuse test contactor (Figure 1). The figure shows a 4 by 6 matrix multi-site

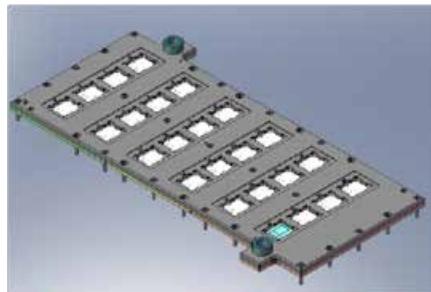


Figure 1: A 1.0mm pitch, 4 X 6 matrix multi-site fuse test contactor. SOURCE: Test Tooling Solutions Group.

test contactor. The key to the solution is that it must overcome variations in the planarity of the test “runway.” Breaking up the approach to the solution into multiple pieces poses a dilemma. This piece-meal approach impacts the overall power integrity because the individual components of spring force, resistance and compliance are related, as shown in Figure 2.

The birth of a 0.2mm multi-site test contactor

The main considerations in developing a 0.2mm multi-site test contactor were similar to those for a 1.0mm contactor, but with a greater need for precision.

There is already an existing solution with the multi-site 1.0mm fuse socket, but to match the downward trend, there is a new market need for a 0.2mm fuse socket. The successes of a strip test socket for memory (for example, the X32 to full wafer one touch probing) will increase designers’ confidence that there is a workable solution. Figure 3 shows a strip test socket for use with memory devices. To achieve the efficiency of a multi-site test contactor, it is paramount that the design engineer consider the following factors for the device under test: 1) Contactor test probe design; 2) High-volume manufacturing (HVM) needs; and 3) Repeatable and rapid changeover.



Figure 3: A strip test socket for memory. SOURCE: Test Tooling Solutions Group.

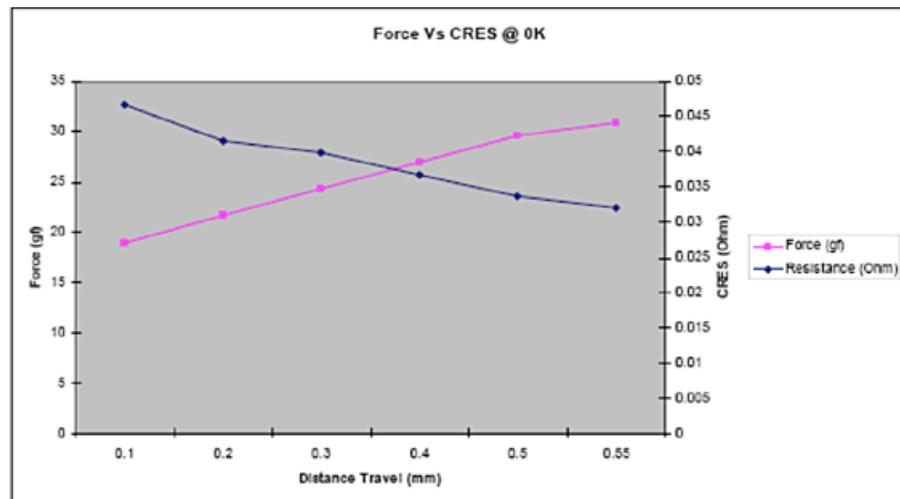


Figure 2: Graph showing the relationship of spring force, resistance, and compliance and its impact on power integrity.

These factors are discussed in the sections below.

The contactor test probe debate

The debate with respect to contactor test probes has been long vs. short. A standard wafer sort (i.e., wafer-probe docking) stack up consists of a pogo tower sandwiched between a probe-interface-board (PIB) and probe card. However, the interconnect height, as described, can effectively be reduced by 30% with a multi-test site contactor. To achieve this 30% reduction, a tradeoff is made. A probe with minimum height also minimizes inductance and yields a very good result. The z-height compliance of a short probe, however, is limited (**Figure 4**). This also means that the multi-site contactor using short probes has to have extremely high z-height accuracy to keep its range compliant within the stack-up.

A contactor test probe has to accommodate a floating socket architecture with strict compliance. Such compliance, coupled with careful

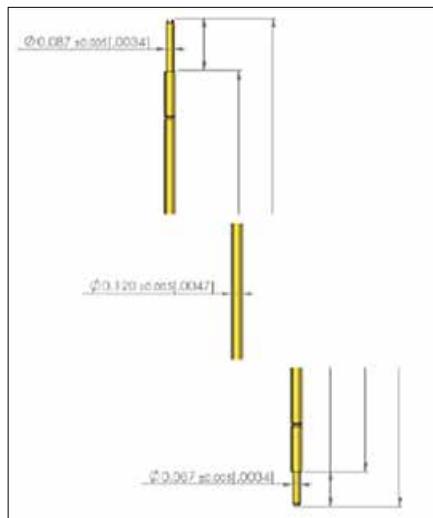


Figure 4: Z-height compliance.

material selection, will enable the solution to be ready for high-volume manufacturing (HVM). Due to imprecise alignment of longer probes, a socket alignment plate, which allows tighter centers, is encouraged. It is also essential that the preload force not be too great for the supporting mechanical

structure. The insertion force of a multi-site socket when making contact with the wafer requires a counter force, to rigidly support and maintain accuracy sufficient to maintain good contact.

Additionally, material selection cannot be overlooked because of the minute feature sizes of the 0.2mm pitch test probe (**Figure 5**). There is no space for additional processing when making the contact (e.g., such as plating on the pin base material) because the finished part is already so small. Thus, one has to have as few process steps as possible

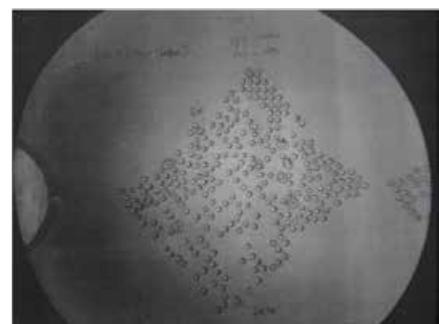


Figure 5: This is a 0.2mm pitch pin with a 0.12mm diameter barrel.

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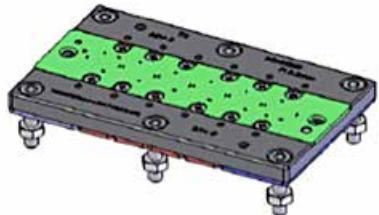


Figure 6: Inspection of a multi-site contactor using a microscopy system. The contactor illustrated is a 5.0 X 8.0 WLCSP 395L P0.2mm, 6-site multi-site test contactor. The drawing shows the pins of site 1. SOURCE: Test Tooling Solutions Group.

from the starting raw material to the final pin rod assembly process.

The ideal material is one that can be readily formed. Another gating factor – as much of a consideration as ease of processing – is in the material’s ability to navigate and pierce through both the oxide layer and lead-free wafer bumps. Care should be taken so that the spring’s counter force is strong, but not forceful enough to deform the solder balls, nor damage the die (buried in the pads of the wafer).

High-volume manufacturing (HVM)

An essential part of all HVM activities is the true-fit check. A lot of time and resources can be recovered during HVM by conducting a true-fit check prior to using the contactor under real test conditions.

First, we need a micro hole. This hole (between the contactor and board) allows the engineer to examine the assembly using an optical microscope. This is a true-fit check prior to loading of the automatic test equipment, and acts as a quick measure of the alignment between the circuit board and the multi-site test contactor. The increase in manpower efficiency during high-volume manufacturing is substantial. The operator can position the wafers precisely under a set of fine contacts in an assembly in 5 minutes versus 45 minutes of possible re-positioning, fitting and removal of the manipulator in the test equipment system without using true-fit.

The use of the micro hole increases the precision of alignment between pad and contactor. Next, we need to look at the tilting angle of the pin, which is restrained by the test contactor. The tilting angle of the pin in the contactor must be kept to an absolute minimum, ideally zero.

Tilting angle. For the 0.2 mm

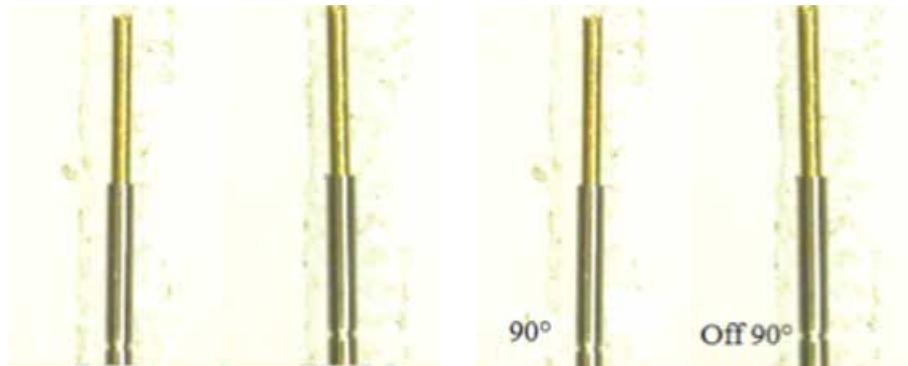


Figure 7: Measurement of the tilting angle of a 0.12mm diameter probe. The left side of the figure shows the pre-measurement configuration; the right side shows the final measurement taken from under the microscope. The figure shows that the pin is bowing in the contactor.

application, it is vital that the x- and y-axis true center remain within the allowable range so that the contactor/pin plunger (top side) cradles the ball grid of the wafer-scale package (**Figure 6**). **Figure 7** shows the pin bowing in the socket, which the design engineer needs to avoid as it is detrimental to the first pass yield.

Analysis of the mechanical system. With a multi-site test contactor, the devices under test (DUTs) are no longer mechanically decoupled or stand-alone because testing is carried out at 2 to 6 sites at one time. The planarity and alignment errors become cumulative with a multi-site test contactor (**Figure 8**). The following discussion describes the summation of variables that comprises the stack-up height error.

Stack-up height error. The stack-up height error can be minimized by using a large frame, with interchangeable inserts, that sits on the same plane as the DUTs, but is not necessarily of the same height. One option is to review the “island design,” which will have an effect on the footprint. There is also another school of thought in which all fabricated piece parts are already permanently deformed. Use of this technique, however, becomes a tricky

proposition when parts are assembled into one.

Piece-part level. At the piece-part level, much consideration is given to deeper barrel hole and counter bore depth. If not considered appropriately, these factors will have an adverse effect on the stiffness of the material as well as the pin tilting angle (see previous section re: tilting angle).

Planarity of the test “runway” and surface flatness. Planarity of the test “runway” and surface flatness are also of concern. To make matters worse, all parts come with their own individual error contribution that will have a cumulative effect due to bowing during post-assembly.

Tightening the screws. Even stress and strain from the pull of the screws will have an impact on the performance stability of the multi-site contactor assembly. An offset as small as +/- 6% could disrupt the best case scenario.

Losses vs. compliance. Power and signal integrity losses will occur if a very long pin is used. However, a short pin will have a shorter lifespan. There is a very fine balance to be established between, on the one hand, losses and z-compliance (if

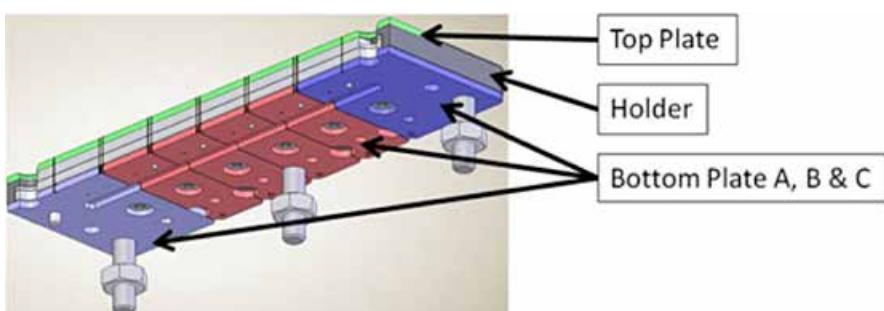


Figure 8: The probability of stack-up height error for a multi-site test contactor.

you put together a solution that needs to last long enough for HVM applications), but on the other hand has a low profile pin for low inductance and other electrical performance considerations.

Repeatable changeover

The alleviation of downtime is becoming a major driving factor to be considered when developing wafer-level chip-scale test processes and set-ups. With the market demanding lower costs, a large increase in the amount of Wi-Fi chip testing could provide a future for high-volume devices. For example, a defective contactor must be easily serviced with maximum equipment utilization time. The greatest fear for any socket maker is a pin being stuck, jammed or bent during the pin insertion process. This concern has resulted in the design of a cost-effective solution for the replacement of pins for HVM applications.

A multi-site contactor typically consists of 4-6 sites (Figure 6) and all the factors (stack-up height error and piece-part level) need to be considered. The

sites are arranged in one column with one site for each DUT, where each site must have the flexibility to be removed and serviced with minimum downtime on the test floor. To achieve that, the inserts, which hold the pin together, are affixed to the multi-site contactor mainframe. The whole structure must be rigid enough to sustain much longer use than that for interchangeable inserts. The standard for the structure is a life cycle of up to a million cycles. Therefore, a large frame made of stainless steel (grade 304) is adopted for several reasons: mainly to improve the top plate warpage, and maintain overall dimensional stability for the required number of cycles. The large frame with inserts has to maintain coplanarity of 0.03mm from pin 1 to the last pin.

Summary

The most important point to remember is that a multi-site test contactor must work right out of the box. A contactor can contain thousands of contacts, each of which must be reliable – with tight centers and excellent yield.

Next, set up must be easy; the micro hole is instrumental to rapid set-up of the test cell. Third, the concept of interchangeable inserts from a large frame should allow the contactor to be serviced off-line without changing the whole assembly system. Finally, with all of the above factors taken into account, wafer-level chip-scale test will allow both the manufacturers and test partners to realize a major cost savings.

Biographies

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Achieving a 75GHz test socket

By Ila Pal *[Ironwood Electronics]*

For over half a century the semiconductor industry has been governed by a commonly known principle described as Moore's Law. This "law" predicts that through technological advancement, a doubling of the number of transistors per integrated circuit (IC) will occur within a given geometric area at regular 18-24 month intervals. The realization of this doubling effect over time has resulted in an ever-widening range of semiconductor devices exhibiting increases in functionality and processing speed combined with an increased demand for power and effective thermal management. This doubling effect has also driven a matching rapid evolution in IC package types and I/O interface configurations. Typical ICs are tested using sockets and the current testing needs exceed 70GHz performance. This article will describe an IC socket contact technology that can reach 75GHz performance without compromising other electrical and mechanical requirements of typical IC applications.

Socket function

Testing can be classified into two categories: IC-level and system-level. IC-level testing involves evaluating the life and performance of IC devices such as microprocessors, ASICs, and chipsets. System-level testing involves evaluating the functional application of those devices under different environments. Both kinds of testing need different sets of criteria for validating the final product. The function of a socket is to provide a connection mechanism from the IC to the circuit board with as little electrical load as possible. This allows the IC to function as it is soldered into the PCB (printed circuit board) but can be replaced by another IC to upgrade or test multiple ICs. **Figure 1** shows a typical BGA socket mounted on a test board.

A 75GHz elastomer socket (GT)

Ironwood Electronics has developed a sequel to the standard GHz socket that

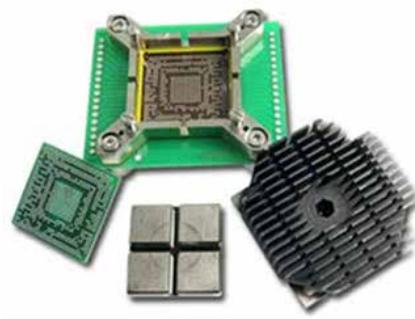


Figure 1: A 75GHz BGA socket with a heat sink.

can test IC packages up to 75GHz. GT elastomer provides a range of high-speed, high-density socket solutions from very compact production sockets to robust test and prototype applications. A magnified photograph revealing a GT contact is shown in **Figure 2**. The sockets are designed such that the force is evenly distributed on the top of the IC thereby pushing the solder balls into elastomer buttons with a silver particle. GT contact technology has 2-3 μ m silver particles held together by a proprietary conductive formulation. These conductive buttons (the diameter is optimized for a 50 ohm impedance) are suspended in a non-conductive polyimide substrate for enhanced durability and reliable performance

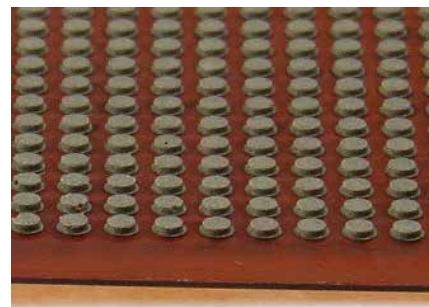


Figure 2: An elastomer contact showing silver buttons for interconnecting individual IC pins.

over time, temperature and cycles. The elastomer is the only medium between the IC package and the circuit board. Precision guides for the IC body and solder balls position the device on the elastomer for a good connection.

Electrical characterization

Electrical requirements are generally stated in terms of the bandwidth. Measuring bandwidth determines if this contact technology is right for particular test application that requires performance at a specified frequency. Bandwidth is typically specified in terms of insertion and return loss. Because the commonly available network analyzers can handle up to 40GHz only, CST microwave

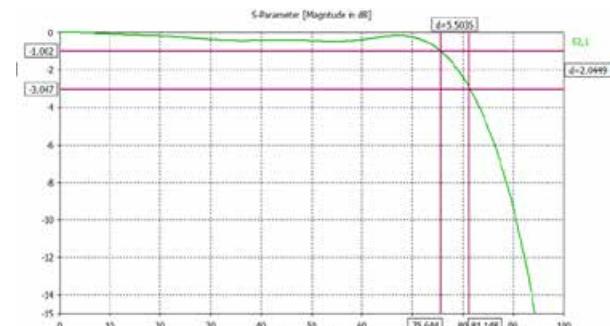


Figure 3: S-parameter curve showing frequency on the x-axis and signal loss in terms of decibels on the Y-axis.

studio software was used to simulate electrical performance. The silver button with polyimide substrate was modeled. Key input values include silver button conductivity and polyimide dielectric loss. A signal is sent from port 1 (top of the contact) and received at port 2 (bottom of the contact). Signal reflections are measured and reported as S21 curves shown in **Figure 3**.

An insertion loss of -1dB @ 75GHz is interpreted as 90% of the signal passed through the interconnect medium and only 10% of the signal was lost through the interconnect transition at 75GHz. This is very critical for the test engineer

because the IC functionality is being verified at this specific frequency.

Mechanical characterization

Removable interface requirements are generally stated in terms of the insertion/extraction force and number of insertion/extraction cycles a socket can support without degradation. Insertion/extraction forces become increasingly important as the pin count of the device increases, as well as the more delicate the ICs become. The mechanical test described below examines the relationship among the deflection of the contact, the force, and the contact resistance.

A displacement force (DF) test station was used to measure the contact deflection and its corresponding force. Force increases linearly as the displacement increases. Similarly, the contact resistance decreases as the force increases. Stable contact resistance has to be identified based on the minimum force

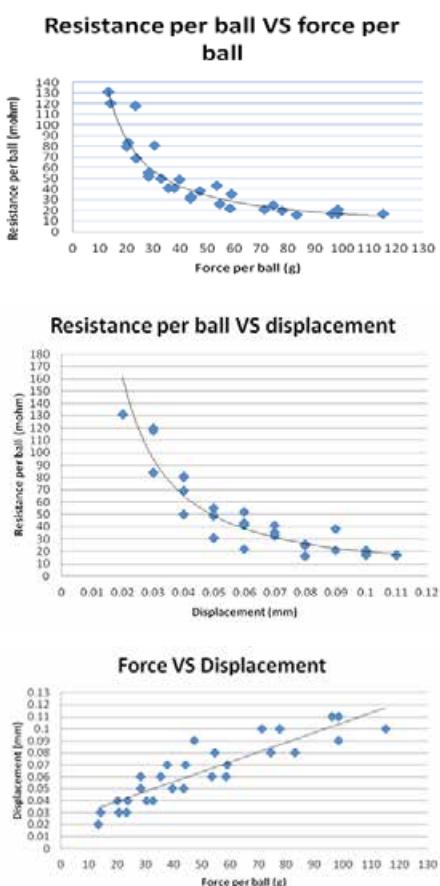


Figure 4: Force deflection resistance curve for GT elastomer contact.

required. A desired displacement has to be identified based on the compliance requirement of each device/application. This information is very important for the test engineer to establish failure criteria when performing device tests using this contact technology. **Figure 4** shows force vs. deflection vs. resistance of the elastomer contact.

From the resistance vs. force graph, it can be seen that in order to achieve a 30mOhms contact resistance, the force needed is 50g per pin. From the resistance vs. deflection graph, it can be seen that in order to achieve a 30mOhms contact resistance, the deflection needed is 0.065mm. From the force vs. deflection graph, it can be seen that a force of 50g per pin causes a deflection of 0.065mm. A test engineer uses these values to determine if the particular contact is suitable for IC testing.

Summary

A single contact technology cannot satisfy all requirements for IC testing throughout its life cycle. The GT elastomer contact has a bandwidth of 75GHz, but the required force of 50g per pin may not be suitable for thin wafer-level packages. The new contact technology has a wide operating temperature range from -55C to +160C, however, it is suitable for low endurance testing because the suspension elastomer contact is rated for 1000 cycles. A primary concern for anyone utilizing high-speed ICs is that the socket must provide a high bandwidth. GT elastomer sockets solve such concerns and provide a solution for high-speed, high-density, high pin count application needs. The test results share the electrical and mechanical characteristics of the contact interface. The simple design of the socket makes it cost efficient and allows assembly to the target board using existing hardware. This socket also has separable components that can be easily replaced and reused.

Biography

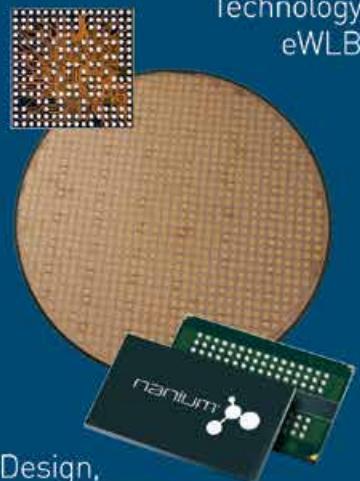
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Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to +260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to +125°C FQ < 30 GHz CF & CR = CM
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AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 4 Merrill Industrial Drive Hampton Beach, NH 03842 Tel: +1-603-926-2517 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
Aries Electronics, Inc. 2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to 155°C CL, FQ, CF & CR = CM
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Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
C2WIDE Co.,Ltd Rm705,84,GaSanDigital 1Ro, GeumCheonGu Seoul, Korea(153797) Tel: +822-364-1878 www.c2wide.com	B, D, P, T	BA, LA	CP = 0.4/0.5/0.65/0.8/1.0mm CL = 300,000 OT = -55° to 130°C FQ > -0.63dB@20GHz CF = 25~35g CR = 3A Continous
Cascade Microtech, Inc. 2430 NW 206th Avenue Beaverton, OR 97006 Tel: +1-503-601-1000 www.cascademicotech.com	D, P, T	BA, LA, SM	P > (0.35 - 0.8) mm CL > (50 - 300,000)x OT = -45°C to +175°C FQ < (9.4 - 40.0) GHz CF < (15 - 55) g CR < (1.0 - 4.0) A
C.C.P. Contact Probes. 5F, No. 8, Lane 24, Ho Ping Rd., Panchiao District, New Taipei City 220, Taiwan R.O.C. Tel +886-2-29612525 www.pccp.com.tw	B, D, P, T		CP = > 0.2 mm CL = > 500k OT = -40~170 FQ = > 10 GHz CF = 15~45 grams CR = > 3A

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Cohu Semiconductor Equipment Group (SEG) 12367 Crosthwaite Circle Poway, CA 92064 USA Tel: 1-858-848-8000 www.cohuseg.com	D, P, T	BA, BD, LA, SM, TH	CP = Contact Pitch > 0.35mm CL = up to 1 Million OT = Temp range -60°C - 175°C FQ = Frequency = <24GHz CF = Contact Force 20 – 40 gram Current rating / pin = < 3A
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com	B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A
Custom Interconnects 2055 S. Raritan Street, Unit A Denver, CO 80223 Tel: +1-303-934-6600 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz CF = CM CR < 5.0 A
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com	B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Enplas Tesco, Inc. 765 N. Mary Avenue Sunnyvale, CA 94085 Tel: +1-408-749-8124 www.enplas-ets.com	B, D, T	BA, LA, SM	CP > 0.4 mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14 - 35) g CR < (0.5 - 1.0) A
Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3 mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30 GHz @ -1dB CF < (15 - 40) g CR < (0.5 - 1.0) A
E-tec Interconnect Ltd. Industrial Zone C Forel (Lavaux) CH-1072, Switzerland 	D, P	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (100 - 10,000)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40 g CR < (0.5 - 3.0) A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4 mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40 GHz @ CM CF < (10 - 12) g CR = CM
Gold Technologies, Inc. 2360-F Qume Drive San Jose, CA 95131 Tel: +1-408-321-9568 www.goldtec.com	B, D, T	CM	CP > (0.4 - 0.5) mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6 - 16.0) GHz @ -1dB CF & CR = CM
High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > (0.5 - 0.8) mm CL > (50k - 250k)x FQ < (4.4 - 10) GHz @ -1dB CF < (30 - 50) g OT & CR = CM
High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5 mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0 A

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HSIO Technologies, LLC. 13300 67th Avenue North Maple Grove, MN 55311 Tel: 763-447-6260 www.hsiotech.com	D, P, T	BA, BD, LA, SM	CP = ≥ 0.3 mm CL = Product Dependant OT = -55° to 155°C FQ > 15-40 GHz @ -1dB CF = Product Dependant CR = 2-4A
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	P	BA, LA	CP > 0.8 mm CR < 10 A CL, OT, FQ, CF = CM
Incavo Otax, Inc. 2205 Harbor Bay Pkwy Alameda, CA 94502 USA Tel: 1-510-675-0688 USA - Japan - China - Malaysia - Singapore - Taiwan www.incavo.com	INCAVO B, D, P, T, CM	BA, BD, LA, SM, TH	CP > 0.01 mm CL = 300K to 1000K OT = -55°C to 155°C FQ = 3.0 ~ 40 GHz @ -1dB CF = 6g to 50g CR < 6.0 A
Ironwood Electronics 1335 Eagandale Ct Eagan, MN 55121 Tel: +1-800-404-0204 www.ironwoodelectronics.com	 B, D, T	BA, LA, SM	CP > (0.25 - 0.4) mm CL > (2K - 500K)x OT = -70°C to +200°C FQ < (6 - 40) GHz @ -1dB CF < 50 g CR < (2.0 - 8.0) A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	 D, P, T	BA, BD, LA, SM	CP > 0.3 mm CL > (300K - 1,000K)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A
Leeno Industrial Inc. 10 105 beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea 408-313-2964(US)/82-51-792-5641 www.leeno.com	 B, D, P, T, CM	BA, BD, LA, SF, TH	CP > 0.1 mm CL > 200K OT = -55°C ~ 150C FQ = 6ghz ->50ghz@ -1db CF = 6g - 50g CR = <-3.0 @ 0.4p
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25 - 0.4) mm CL = CM OT = CM FQ = CM CF = CM CR = CM
M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjc.co.jp	B, D, T	BA, SM	CP > 0.2 mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM
Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25 - 50) g CR < (1.0 - 3.0) A

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Modus Test LLC P.O. Box 56708 Atlanta, GA 31156 Tel: +1-678-765-7775 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3 mm CL > 1,000,000x OT = +200°C Max. FQ < 20 GHz @ CM CF < 35 g CR < 5.0 A
Multitest Electronic Systems 4444 Centerville Road, Suite 105 Saint Paul, MN, 55127-3700 Tel: 1-651 407 7726 www.multitest.com	D, T	BA, LA, SM	CP > (0.25 - 0.5) mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5 - 40) GHz @ CM CF < (26 - 55) g CR < (1.8 - 4.6) A
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong, Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0 - 12.4) GHz @ -1dB CF < (7 - 15) g CR < (0.5 - 1.0) A
Paricon Technologies Corporation 421 Currant Road Fall River, MA 02720 Tel: +1-508-676-6888 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1 - 0.4) mm CL > 1,000,000x OT < 150°C FQ < 40 GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtest.com	D, T	BA, LA, SM	CP > 0.4 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < 25 g CR < 3.5 A
Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
ProFab Technology Inc. 41817 Albrae Street Fremont, CA 94538 Tel: +1-925-600-0770 www.profabtechnology.com	D, T	BA, LA	CP > (0.26 - 0.45) mm CR < 7.0 A CL, OT, FQ & CF = CM
Qualmax, Inc. IT Castle, 1-dong, 1101-ho 550-1 Gasan-dong, Geumcheong-gu Seoul, Korea 153-768 Tel: +82-2-2082-6770 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5) mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0 - 4.0) A
R&D Altanova 3601 So. Clinton Avenue, South Plainfield, NJ 07080 Phone: 732-549-4554 Fax: 732-549-1388 www.rdaltonova.com	D, P, T	BA, BD, LA, SM	CP < 0.3 mm CL = 150,000x OT = -40° to 150°C FQ > 38GHz @ -1dB CF = 15g CR = 4A
Rika Densi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36 GHz @ -1dB CF < (15 - 30) g CP & CR = CM

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Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0 A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35 mm OT = -55°C to +150°C FQ < (9 - 10) GHz @ CM CR < (1.0 - 15.0) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Avenue, Suite 100 San Jose, CA 95120 Tel: +1-408-269-2800 www.sanyu-usa.com	CM	CM	CP > 0.2 mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15 - 25) g CR < (4.0 - 5.0) A
Sensata Technologies, Inc. 529 Pleasant St, P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10 - 25) g CR < 1.0 A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3 - 0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5- 20) GHz @ CM CF & CR = CM
Smiths Connectors 5101 Richland Avenue Kansas City, KS 66106 913-342-5544 www.smithsconnectors.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 250k - 1M OT - 40° to 150°C FQ < 25GHz @ -1db CF 8 - 85 grams CR 1.5 to 5 Amps
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3, 11900, Bayan Lepas, Penang, Malaysia. Tel: 604-646 6966 www.tts-grp.com	D, T, P	BA, BD, LA, SM, TH	CP ≥ 0.2mm CL > 200k - 500k OT = -40°C to +180°C FQ < 30GHz @ 1dB CF = 8 to 45g CR < 6.0A CF & CR = CM
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: +1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5 - 1.0) A
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com	D, T	SM	CP > 0.4 mm OT = -40°C to +150°C FQ < (6 - 8) GHz @ CM CL, CF & CR = CM

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WinWay Technology Co. Ltd. No. 68, Chuangyi S. Road, Second District of Nanzih Export Processing Zone, Nanzih Dist Kaohsiung City 81156, Taiwan Tel: +886-7-361-0999 www.winwayglobal.com	B, D, T	BA, BD, LA, SM	CCP > (0.2 - 0.4) mm CL > (50k - 500k)x OT = -50°C to +150°C FQ < (0.2 - 30) GHz @ -1dB CF < (10 - 41.3) g CR < (1.5 - 7.0) A
Yamaichi Electronics Co., Ltd. 3-28-7 Nakamagome, Ota-Ku Tokyo 143-8515, Japan Tel: +81-3-3778-6111 www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4 mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM

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8-slot • single zone



32-slot • multiple temperature zone



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Coplanarity analysis and control of spring probe heads for wafer testing

by Jiachun Zhou (Frank), Cody Jacob, Daniel DelVecchio [Smiths Connectors]

The applications of wafer-level chip scale package (WLCSP) and micro chip scale package (MicroCSP) technologies have grown significantly in recent years, particularly as consumer electronics have driven down the size of devices. The tight pitch requirements of device leads become one of challenges in device manufacturing. As traditional IC packages have pitches $>0.4\text{mm}$, many WLCSP devices boast pitches of $\leq 0.4\text{mm}$. The trend away from singulated package test toward wafer-level test requires new equipment investment, including probe heads and related contactors, to match the mechanical and electrical performance requirements of the device in wafer testing.

Many WLCSP tests employ conventional front-end contact techniques, either cantilever needles or “vertical probe cards,” based on buckling beam technology. Both techniques have limitations in performance. Cantilever cards are incapable of RF testing that is required in final test of WLCSP devices. Difficulties in maintenance and complexity in repair result in high tooling costs for these types of probe cards. Another major limitation with a cantilever card is a result of its structure, which is suitable only for low pin count devices testing 1-3 devices in parallel. Vertical probe cards with short signal paths are more reliable in making contact and offer better RF performance. The typical weakness of these techniques is their lack of compliance. The WLCSP bump structure usually requires significant compliance for reliable contact when employing high parallelism testing.

As an alternative contactor technology, spring probe heads have grown in popularity in wafer testing because of their advantages over cantilever needle and buckling beam technologies. Spring probe heads provide increased compliance as well as the benefit of field serviceability through individual contactor design structure. Tip coplanarity is a frequently raised concern when utilizing a spring probe head in

wafer testing. This paper offers an analysis of tip coplanarity analysis and proposes approaches to ensure optimal design and performance of a spring probe head.

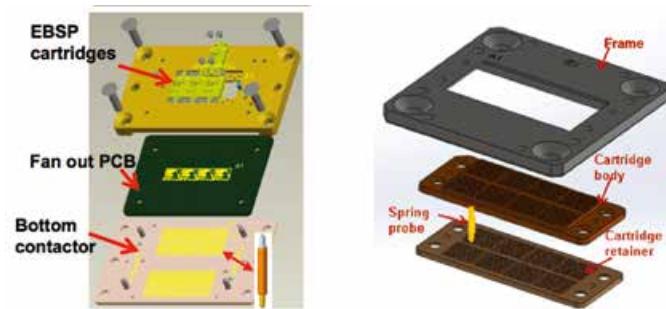
Basic structure of a spring probe head

Typical WLCSP probe head and spring probe contactors are presented in **Figure 1**. Embedded Barrel Spring Probe (EBSP) contactor probe head (P/H) is a new contactor technology developed by Smiths Connectors. With the specific spring probe structures, EBSP P/Hs are typically used for small pitch ($\leq 0.3\text{mm}$) applications.

Traditional spring probe are used in contactors for $>0.3\text{mm}$ pitch applications. The traditional spring probe may be used in $<0.3\text{mm}$ pitch P/Hs, but it is discouraged as its RF performance deteriorates in such applications. This deterioration is due to the additional length ($>5\text{mm}$) required to provide enough compliance in a small diameter ($<0.25\text{mm}$) probe.

As shown in **Figure 1**, the spring probe head structures are completely different from those of traditional cantilever needles and vertical probe cards. The compliance of a spring probe contact tip on device balls/pads is driven from compression of the spring, while other techniques depend on compliance of the signal beam.

Spring probes consist of four components while other contactors have one contacting component. Generally, wafer or WLCSP testing set ups require very tight control on contactor tip coplanarity. The unique structure of spring probes with multiple components requires additional considerations in probe head structure, manufacturing processes, and material selection to control the tip coplanarity and



a. EBSP contactor (Monet) P/H. b. Traditional spring probe P/H.

Figure 1: Typical structures of spring probe heads.

ensure adherence to technical specifications of the wafer tester probe header.

Determining spring probe head tip coplanarity

It is well known that the function of the interconnect is to provide reliable connection with enough probe tip compliance (or travel) to absorb the flatness tolerances of wafer balls/pads and other related components in probe head structures. The state of spring probes inside the probe head body is described in **Figure 2a**. The “free” state refers to the spring probe head placed on the board at free state. When the spring probe head is mounted on a test board or space transformer (fan-out PCB), the bottom plunger is compressed to achieve the “preloaded” state. The spring force is applied on the board. The wafer ball/pad contacts and compresses the spring probe

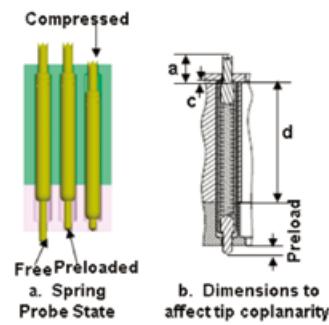
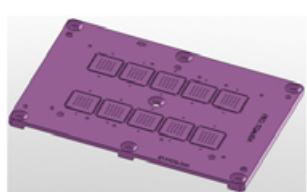
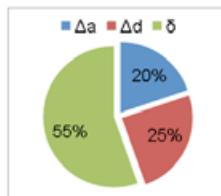


Figure 2: Spring probe state and dimensions that affect coplanarity.



a. Probe head



b. Tip coplanarity

Figure 3: Example of spring probe head tip coplanarity distribution.

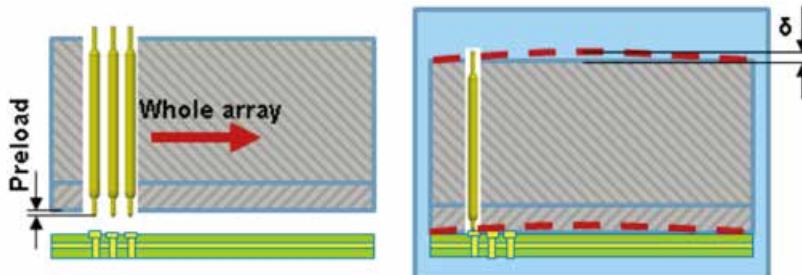


Figure 4: Spring probe preload and probe head bowing.

tip or crown down to testing condition in the “compressed” state.

As shown in **Figure 2b**, the tip coplanarity of the spring probe head is primarily determined by a couple of factors: 1) The accumulated tolerances of the dimensions, a, c, and d, and 2) The bowing (or warpage) generated by preloading of the spring probes. The dimension tolerances are controlled by manufacturing processes of the top plunger and probe body. At the current machining capability, the plunger tolerance is $\sim +/- 20\mu m$ (dimension “a” in **Figure 2b**) and counter bore depth tolerance of $+/- 25\mu m$ (dimension “d” in **Figure 2b**). The probe head body bowing is dependent on the preload force of spring probe, pitch, quantity of spring probes, and body material. The tip coplanarity of a probe head can be calculated with this formula:

$$H = \Delta a + \Delta c + \Delta d + \delta$$

Where:

H = tip coplanarity of whole probe array;

Δa = top plunger neck tolerance, $\sim +/- 0.02mm$;

Δc = barrel crimping thickness tolerance, negligible;

Δd = counter bore depth tolerance, $\sim +/- 0.025mm$, and

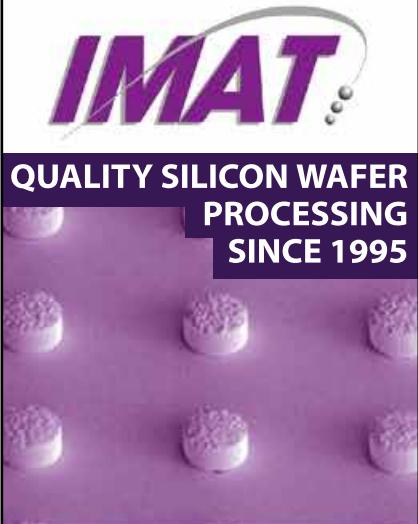
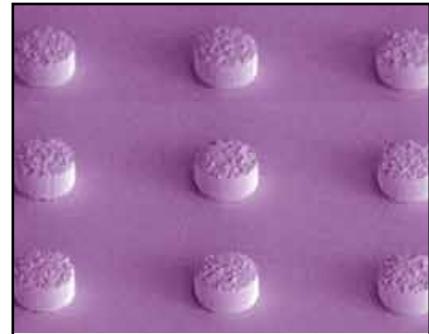
δ = cartridge bowing due to preload.

As an example, **Figure 3** shows

coplanarity of a 10 WLCSP site spring probe head (0.4mm pitch, ~ 200 pins/site). For the worst case scenario, the maximum coplanarity is $\sim 200\mu m$. Dimension tolerance contributes $\sim 50\%$ and probe head bowing about 50% . This probe head uses traditional spring probes with top side compliance $\sim 350\mu m$. Although spring probe compliance can withstand the tip coplanarity variation, wafer testing set ups cannot accommodate such significant variation. Generally, it is not easy to improve tolerances of structural dimensions because of manufacturing process limitations. The improvement or reduction in probe head bowing becomes a major factor in spring probe head development.

Probe head body bowing and body material selection

As mentioned previously, the coplanarity of a spring pin probe head is primarily affected by accumulated tolerances of spring probe components and probe head bowing. The components’ tolerances are determined by manufacturing processes. Probe head bowing is generated by the preload of spring pins at the test board side. Being different from cantilever and vertical probe head contactors, the compression spring of a spring probe is usually pre-compressed, or preloaded, when a probe head is mounted on the mother test board. This preload is about 20 to 30% of the total compliance with a force of $8 \sim 12gf$. Under this spring force,



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Material	Flexural Modulus	
	English, kPSI	SI, Gpa
A Ceramic Filled PEEK	650	4.482
B MDS 100	1420	9.791
C New Thermoplastic Material	2465	17
D New Ceramic material	18853	130

Table 1: Spring probe head body materials.

# of sites	8
Pitch, mm	0.4
Pin count, per site	137
Pin count, total	1096
Preload/pin, gf	12
Total preload, kgf	13.15

Table 2: Spring probe head example for FEA.

the probe head is deformed into a bridge shape, with the middle area raised. Bowing of the probe head can contribute up to 50% of the total tip coplanarity variation of a probe head (**Figure 4**). In addition to spring preload force, the material stiffness, or flexural modulus of elasticity, significantly impacts probe head bowing as well. **Table 1** is a list of flexural moduli for different thermoplastic materials.

To compare the bowing of probe heads with different materials, structures, and pin counts, a series of finite element analyses (FEA) were performed with one 8-site probe head (PH). This is a conventional WLCSP

PH (previously referred to as a socket). The structure and other parameters of this PH are listed in **Table 2**.

The FEA results on a solid model with four different materials are shown in **Figure 5**. According to basic principles of structural mechanics, the flexural modulus elasticity of the material is the primary factor that determines material bending. A higher flexural modulus material has less deformation under external force. For this particular probe head model, FEA results show the center area has the greatest bowing or deformation. Ceramic PEEK is commonly used in package test sockets and is also applied in WLCSP probe heads. With the use of Ceramic PEEK, the maximum bowing at the PH center is up to 0.26mm for this specific 8-site PH. Usually, the preload travel length of a spring probe is about 0.12mm. Under 0.26mm maximum bowing, some spring probes in the center area lose their preload, which can cause increased contact resistance (CRES) due to unstable contact with the test board. Therefore, this design with Ceramic PEEK may not have proper performance and should be redesigned.

Using materials with a high flexural modulus of elasticity, probe bowing can be greatly reduced as presented in **Figure 6**. With doubled flexural modulus in material B, the maximum deflection is reduced to 0.173mm, which is still greater than the preload travel of a spring probe. When using material C, the flexural modulus is four

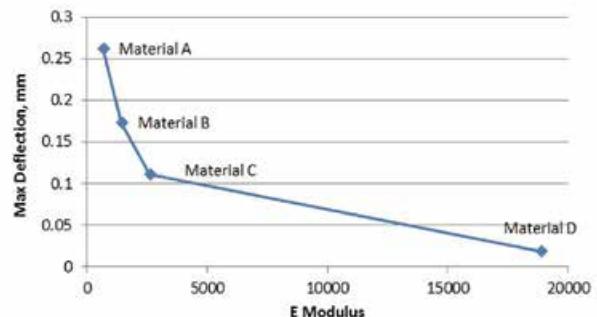


Figure 6: Probe head bowing vs. materials.

times greater than Ceramic PEEK, and the maximum deflection is 0.11mm, which is less than the preload travel of typical spring probes. For material D, which has an extremely high flexural modulus, the maximum deflection is only 0.019mm and could be considered with no bowing for the PH.

Usually, tip coplanarity is the primary technical specification of a probe head in WLCSP and wafer testing. The impact of PH body bowing on tip-to-tip coplanarity of the pin array can be calculated with the formula:

$$\text{Tip coplanarity} = \frac{\text{Max Deflection} - \text{Min Deflection}}{\text{Total Preload Travel}}$$

As shown in **Figure 7**, the maximum deflection is at the center and the minimum deflection is located at the edge of the spring probe arrays. **Table 3** lists the coplanarity values affected by PH bowing for four different PH materials. The material with higher flexural modulus has the best coplanarity

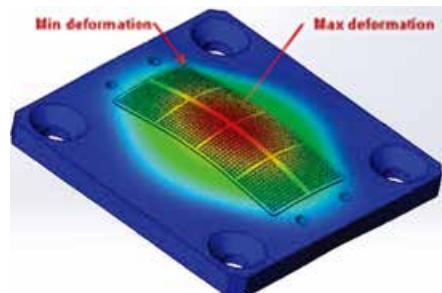


Figure 7: Maximum bowing in the center of the probe head center.

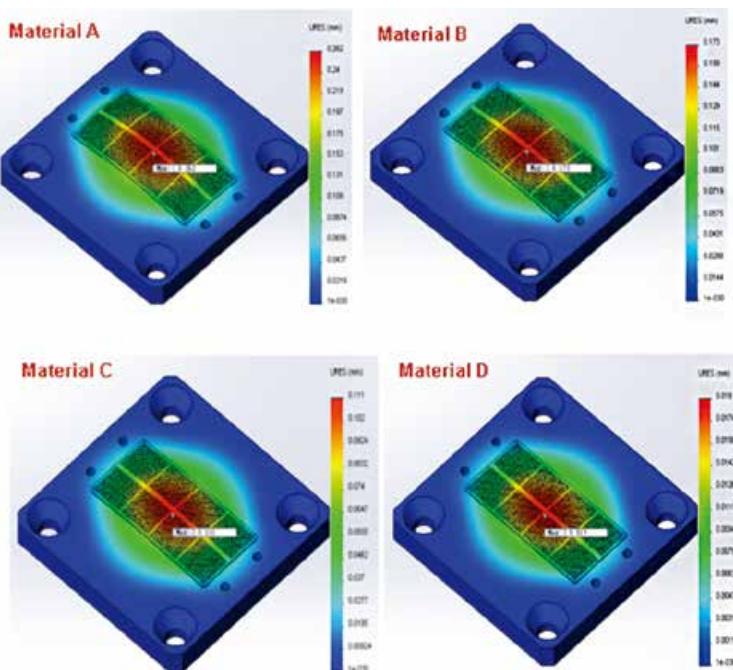


Figure 5: Spring probe head bowing in FEA.

Material	PH Bowing, mm		Co-Planarity mm
	Max	Min	
A Ceramic Filled PEEK	0.261	0.054	.207
B MDS 100	0.172	0.033	.139
C New Thermoplastic Material	0.110	0.020	.090
D New Ceramic material	0.019	0.016	.003

Table 3: Coplanarity vs. probe head bowing.

if all other component tolerances are the same.

Probe head structure on spring probe tip coplanarity

The availability of high strength thermoplastic composite materials is very limited in this industry, which may be the result of a narrow pool of manufacturers and challenges in developing high flux modulus thermo-plastic materials. Optimization of the probe head structure is another approach to reduce spring probe PH bowing and improve tip coplanarity. Among various PH structures, spring probe cartridges with frames are one commonly deployed option.

Figure 8 presents an 8-site probe head designed with one spring probe cartridge and a stainless steel (SS) frame. The FEA simulation results, shown in **Figure 9**, indicate the cartridge with an SS frame structure can reduce maximum deflection from 0.262 mm to 0.124 mm—an improvement of over 50%. The PH bowing of this cartridge with frame design is less than the typical spring probe preload travel, and therefore, it maintains reliable contact of the probe to the test board pads for low CRES.

The mounting screws on a probe head

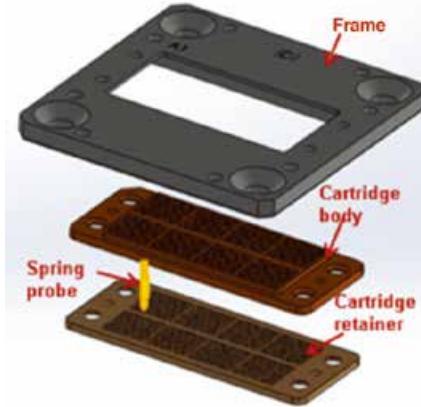


Figure 8: Probe head with frame.

can also affect PH bowing. Although the mounting locations of screws are primarily determined by the test board design, it is always beneficial to have the location close to the spring probe array. **Figure 10** shows an example of how mounting screw distance impacts probe head bowing. As this distance varies from 44.6mm to 24.6mm, the maximum deflection is reduced from 0.329mm to 0.262mm.

Summary

Spring contact probes have been established as one of the major contact

technologies for WLCSP device testing. In pursuit of a stable contact, the preload travel of spring contact probes against the test board can result in probe head bowing and affect contactor tip coplanarity. To minimize the impact, higher stiffness materials should be selected to reduce bowing and improve coplanarity. Enhancements in probe head design structure, such as cartridge and frame methods, can also reduce bowing significantly and ensure better coplanarity of probe head tips.

All simulation results and measurements presented in this paper are based on worst case design scenarios. Considering all design structures and manufacturing improvements, the tip coplanarity of spring probe heads can typically be controlled in the range of <80 μ m in WLCSP and wafer testing technical specifications.

Biographies

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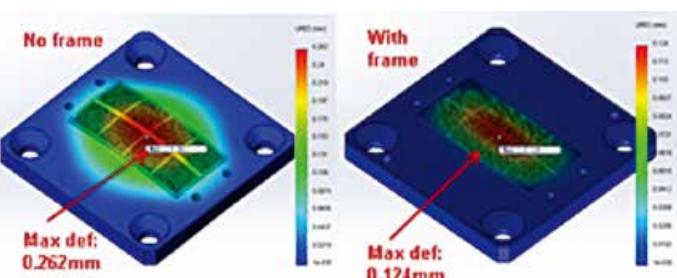
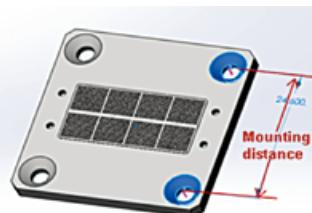


Figure 9: Max deflection comparison: with and without a frame.



Mount Distance, mm	Max Deflection, mm
44.6	0.329
39.6	0.317
34.6	0.301
24.6	0.262

Figure 10: Body bowing vs. probe head mounting location.

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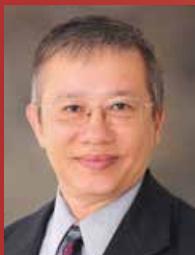
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INDUSTRY NEWS



SEMI European 3D TSV Summit 2015

By Yann Guillou [SEMI Europe]

In January 2015, Grenoble hosted its third edition of the European 3D TSV Summit—SEMI Europe's flagship event focused on 2.5 and 3D integration. Attracting 250 executives and experts from 22 countries to discuss the latest updates in the realm of TSV, the event was a veritable success with more than 9 out of 10 participants rating the event as “good” or “very good.”

Over the course of the two-day summit, attendees had the opportunity to hear from three keynote speakers, 21 invited speakers, and an expert panel discussion. In addition to the high-caliber conference program, attendees were able to visit an industry exhibition focused uniquely on 3D TSV, schedule 1-on-1 business meetings, visit CEA-Leti's 300mm TSV cleanroom, and benefit from the numerous networking opportunities offered to them. The event was sponsored by 20 important actors in the industry.

SEMI kicked off the summit on January 19 with a dedicated market briefing session, where attendees were presented with the market trends to expect for 2.5 and 3D technologies. Of particular note, two presentations made by market experts Barnett Silver of ATREG and Scott Jones of AlixPartners approached TSV and advanced packaging with a fresh perspective.

On day two of the summit, Bryan Black from AMD and Timo Henttonen from Microsoft delivered keynote addresses. In the morning, Black announced that 3D stacking “is happening” and that AMD is now launching new products that integrate TSV technology. In the afternoon, Henttonen was a bit more measured, expressing that from his viewpoint, many issues still need to be tackled in order to integrate 2.5 or 3D products using TSV

technology in consumer products like smartphones. He insisted that yield and test pose the greatest challenges to the development of the technology. Qualcomm, ams, CEA-Leti, imec, Fraunhofer, and many equipment and materials companies also shared their perspectives and their recent progress in the realm of 3D TSVs.

On the closing day of the summit, the third and final keynote speaker took the stage: CP Hung from ASE Group. Hung explained how TSV technology is being assimilated into packaging's DNA. Also on this last day, SEMI chose to highlight two topics that are ever more important to the 3D TSV industry: interposers and silicon photonics. The first session on interposers hosted Corning and Asahi Glass, who presented both glass and silicon interposers from a technological perspective. STMicroelectronics gave the networking processor product perspective, and Rudolph Technologies addressed the topic from a business and supply chain perspective. For the second session on silicon photonics, IBM and HP explained what advantages TSV and 2.5D integration could bring to next-generation photonics products and the business opportunities it would create.

The Gala Dinner – one of the “non-technological” highlights of the Summit – took place in a French Chateau this year. Attendees enjoyed a friendly atmosphere, good French food and wine, and a relaxed setting that lent itself to networking and the development of business relationships.

All proceedings of the SEMI European 3D TSV Summit can be purchased online on the event's website (www.semi.org/european3dtsvsummit). Next year's edition of the event has already been announced for January 18-20, 2016 in Grenoble (France).

Contact author

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Minatec campus - Grenoble, France



Panel discussion: Moderator: Jean-Christophe Eloy, Yole Développement, Panelists Ron Huemoeller, AMKOR, Mustafa Badaroglu, Qualcomm, Martin Schrems, ams AG, Bryan Black, AMD



Guénael Ribette and Gilles Fresquet of Fogale nanotech



Jürgen Wolf, Ehrenfried Zschech of Fraunhofer IZM & IKTS, Eric Beyne of imec, Lawrence Michaels of Chip Scale Review

BiTS 2015 turns up the Irish!

By Chip Scale Review staff

The BiTS Workshop and *Chip Scale Review* are pleased to announce the program for the 2015 BiTS Workshop, which takes place March 15-18, 2015, in Mesa, Arizona. This year, BiTS bumps into St. Patrick's Day, so plan on breaking out your green and orange, because the beer and Irish whiskey will surely be flowing, along with the blarney.

2015 marks a new beginning for BiTS, as Ira Feldman, Feldman Engineering, takes the helm as General Chair. Fred Taber, former BiTS General chair, passed the baton to Feldman at the close of BiTS 2014.

In keeping with BiTS' tradition of excellence, the BiTS leprechauns



Left to right: Morton Jensen, Valts Treibergs, Owen Prillaman, Rafiq Hussain, Fred Taber, Mike Noel, Ira Feldman, Marc Moessinger, John Moore (BiTS 2014 committee), Ila Pal. Not pictured: John Hartstein, Paul Boyce

have been working overtime to bring you eight jam-packed technical sessions, plus a poster session with presentations by test and burn-in

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experts from around the world. This is complemented by Sunday's tutorial, global marketing reports, an inspiring keynote talk, and enough networking opportunities to satisfy your sales manager.

The festivities kick off on Sunday with a hands-on, half-day workshop, *How to Make a High Frequency Transparent Socket*, led by Heidi Barnes, Senior Applications Engineer, Keysight Technologies. Barnes will guide attendees through the basics of simulation and measurement techniques for ensuring signal integrity (SI) of test sockets. Space is limited, so sign up early to secure your spot.

Prismark Partners' Brandon Prior returns as the distinguished speaker for the Sunday night welcome dinner. His presentation will focus on the

impact and growth of small form factor packages such as multi-row QFN, WLCSP, Fan-Out WLCSP and MIS BGA on the electronics industry infrastructure. He will use tear downs of products from early adopters such as Apple, Samsung, Huawei, and Xiaomi to illustrate the rapidly occurring changes.

By Monday morning, BiTS will be going full tilt, beginning with an inspiring keynote by Babak Taheri, VP and General Manager, Sensor Solutions Division, Freescale Semiconductor. Taheri will explore the *Internet of Tomorrow*, by sharing his thoughts on microelectromechanical systems (MEMS) sensing technology and its end applications that include everything from automobiles to smartphones. He will also explore the

Internet of Things (IoT), which will connect all these devices.

In addition to all this top-notch content, be sure to spend some time exploring the BiTS EXPO to see what's *Now & Next* in the test and burn-in of packaged semiconductors. Top off your BiTS experience by participating in the annual social event. This year, we'll celebrate St. Patrick's Day in style with traditional Irish fare and a Casino Night to test your Irish luck and maybe win that pot o' gold.

For more information on BiTS 2015, including the full agenda, registration, and hotel information, visit www.bitsworkshop.org. **Chip Scale Review readers save \$50 on Professional Registration by using Registration Code 50CSR.**

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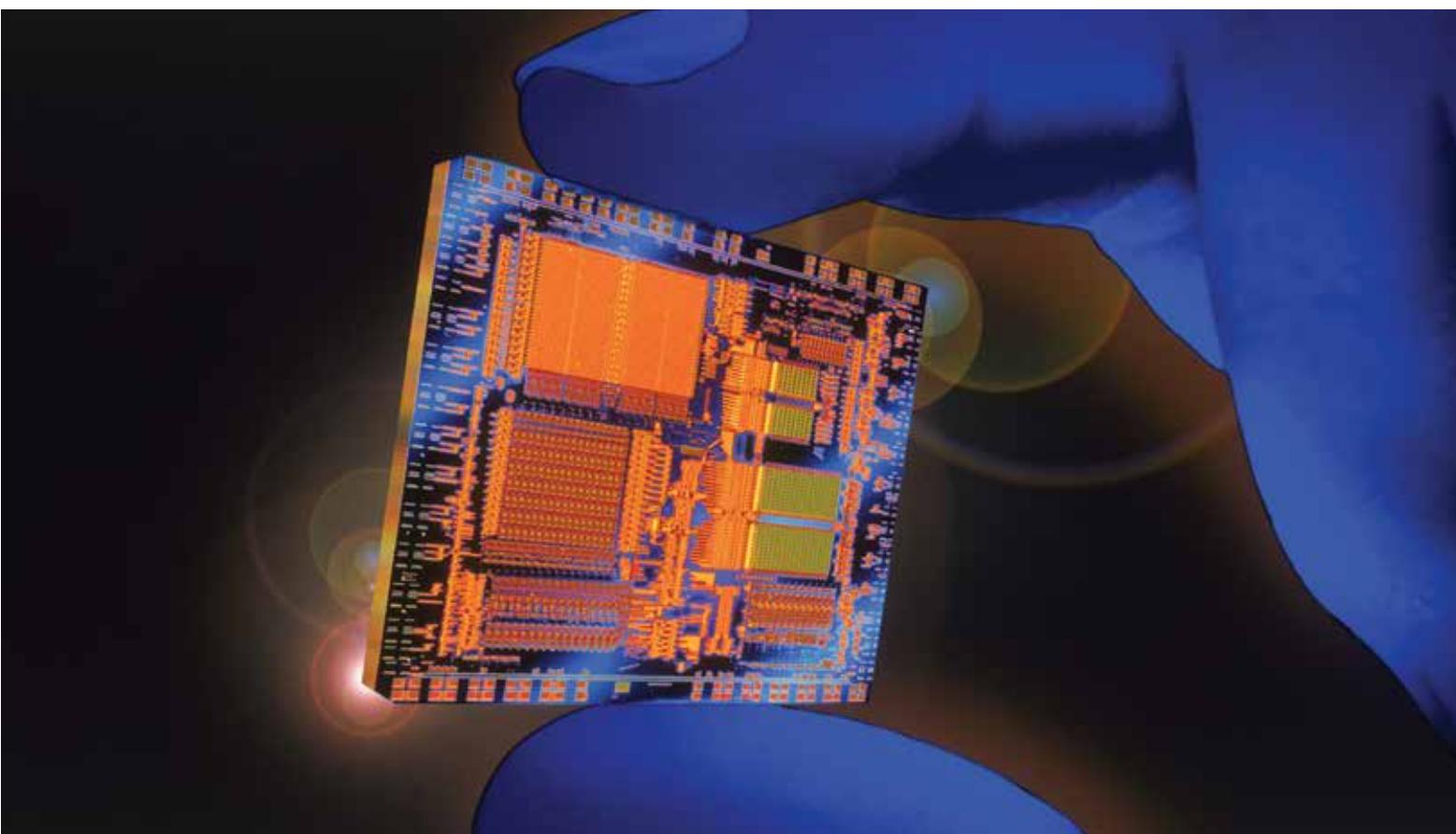


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