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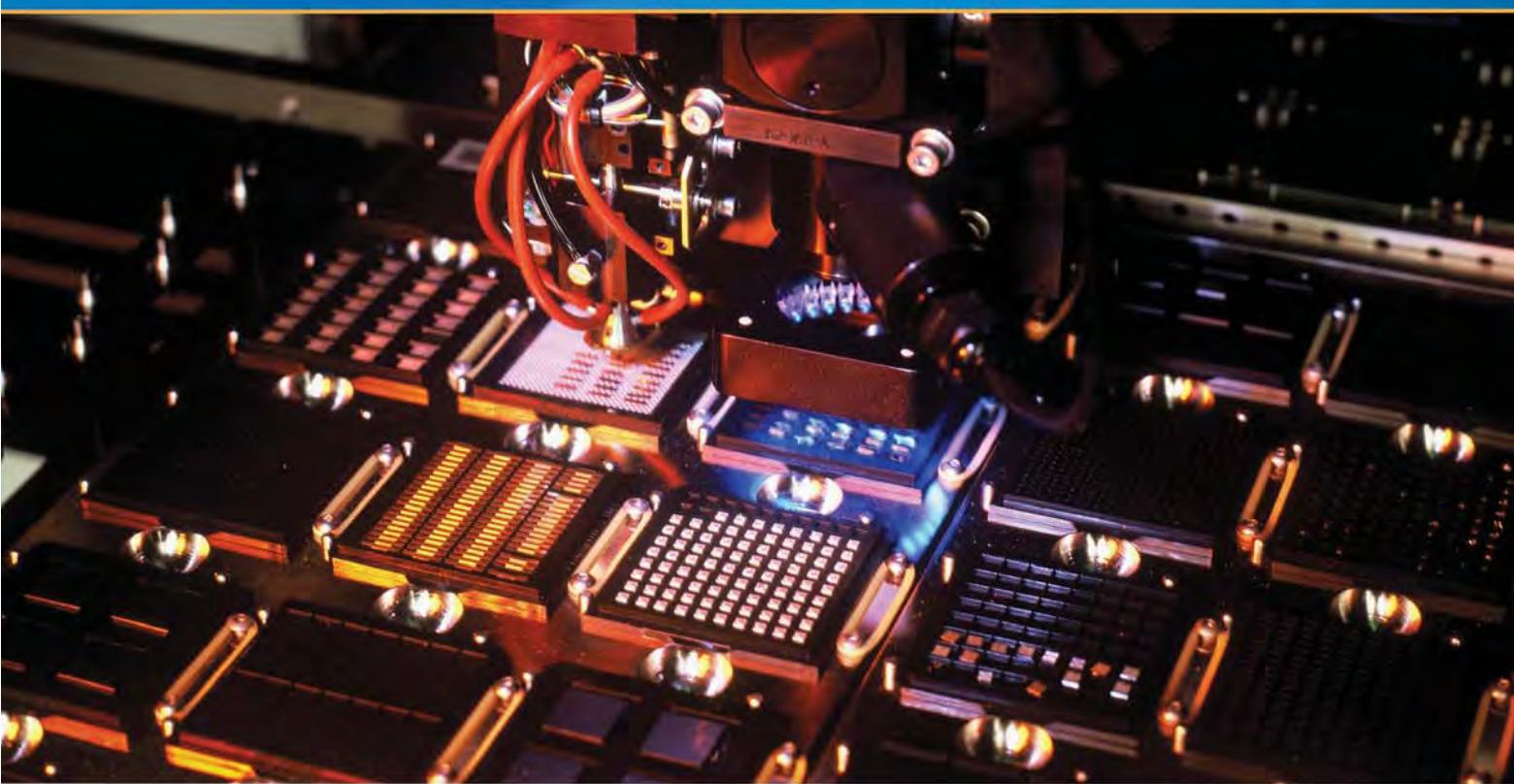
REVIEW®

The International Magazine for the Semiconductor Packaging Industry

Volume 15, Number 2

March - April 2011

- Worldwide IC Packaging Foundries
- WLCSP Market Technology Solutions
- Reliable Low Cost for QFNs
- Die Bonding in a Mobile World
- TSVs in MEMS Development



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March-April 2011

Volume 15, Number 2



March - April's cover represents a global view of the worldwide market for the semiconductor assembly and test services (SATS). The latest market update is presented in this issue's editorial lineup with Integrated Circuits (ICs) Out Pacing the Economy. The top ten OSATS are evaluated in conjunction with the annual International Directory of IC Packaging Foundries.

Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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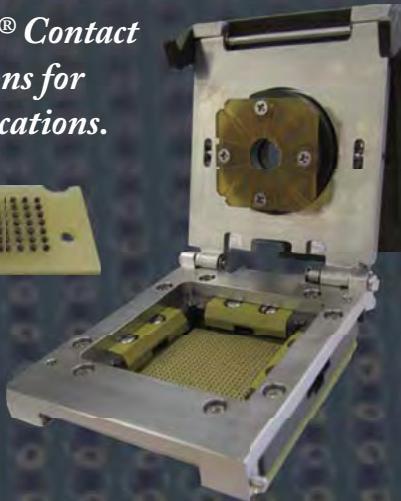
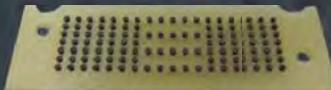


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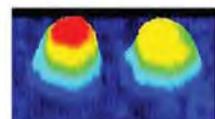
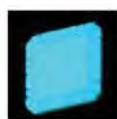
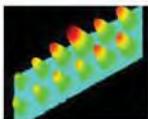
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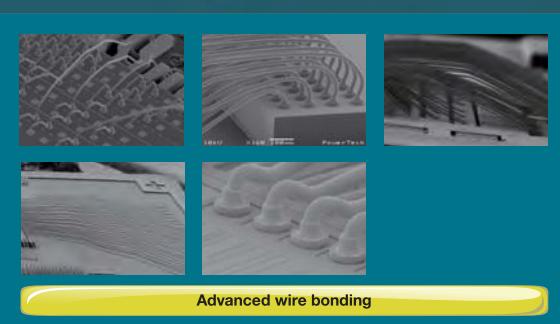


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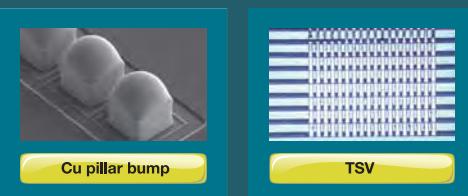
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FROM THE PUBLISHER



Mother Nature Devastates a Country and Impacts an Industry

On behalf of the entire Chip Scale Review team, I'd like to send our thoughts and prayers to all of those whose lives have been affected by the earthquake and tsunami in Japan.

For the second time in a year, I find myself scrapping the original version of the publisher letter and rewriting it just in time to go to press. Last time was in October to celebrate the happy news of the Giants winning the World Series. Unfortunately this time it was because I went to sleep last night after returning from BITS Workshop and IMAPS Device Packaging Workshop with a pretty optimistic feeling about the packaging industry only to wake up to the devastating news of the earthquake and Tsunami in Japan. In barely the blink of an eye, the third largest economic power in the world was hurled into its greatest crisis situation, and things may never be the same.

While many of our colleagues in Japan cared for their families and friends, the analysts were starting to assess the impact this natural disaster will have on the semiconductor industry. Initial concerns were a potential shortage of silicon, and memory components such as DRAM and NAND flash. A preliminary report from Jon Cassell of IHS iSuppli predicts that "the major impact on Japan's semiconductor production is not likely to be direct damage to production facilities, but disruption to the supply chain."

Before the disaster, I had OSATS on the brain because this is our annual OSATS issue. In it you'll find an interview with Scott Jewler, President of Powertech Technologies USA, an award-winning technical feature by Amkor, and a directory of packaging foundries with an introductory report from contributing editor, Sandra Winkler.

There are a lot of them out there, so how is it that it's always the same top four companies that trade off their positions, yet together control the majority of market share? Ask anyone in the know and they'll rattle them off: ASE, Amkor, SPIL, and STATS ChipPAC.

Last year, ASE took the lead, presumably because of its decision to invest in copper processes. Another contributing factor is that while they're diversified, most manufacturing takes place in Taiwan and China. Amkor, on the other hand, is widely diversified, adding to operational cost. They've changed strategy to focus on debt reduction rather than capex spending. However, they are technology innovators and are in the forefront visually. SPIL had a good run in first position (2005, 06, 07) thanks to being a fast follower on technology, low overhead, being a megasite operation with a controlled geographical footprint and strong customer relations. Unfortunately, they seem to have lost the recipe in the last few years, dropping off 10-15%. Some attribute it to lost business to ASE and being slow to adopt copper. Currently in fourth place, STATS ChipPAC is privatized, and is therefore constrained on capex although not as excessively as Amkor. Still, I'm told that the company seems to struggle to execute at high level. I'm curious to see if this ranking gets shaken up as next-generation technologies come to market; both on the WLP and 3D front.

Kim Newman

Publisher

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Patent Reform Legislation: A Reality in 2011?

By Contributing Legal Editors, Jason Mirabito and Carol Peters [[Mintz, Levin, Cohn, Ferris, Glovsky and Popeo PC](#)]

By the time you read this article, Congress will have been debating and arguing over the content of long-awaited comprehensive patent reform legislation for nearly two years. Two reasons that such legislation has not passed include partisanship (which is probably not a surprise) and the opposing positions of high-tech companies vs. pharmaceutical companies on this legislation. However, a new bill entitled **The Patent Reform Act of 2011**, recently approved by the Senate Judiciary Committee and on its way to the Senate, promises to be an acceptable bi-partisan bill with decent hopes of being passed. While the legislation is far-encompassing, we direct your attention to the more important provisions in the present bill.

Change from "First to Invent" to "First to File" System

In the United States (and only in the United States), a patent grants to the entity "first to invent" a particular invention. In almost all, if not all other countries, the entity that beats it to the door of the patent office first, or, in other words the entity "first to file" a patent application, is considered to be the first inventor. The proposed Patent Reform Act will harmonize U.S. patent law to that of other countries and will switch the U.S. patenting system from a "first to invent" to a "first to file" system.

This change has been a relatively controversial subject, and small companies and others have alleged that larger companies have better ability (more money, engineers, and infrastructure) to file their patent applications first. However, adoption of the "first to file" system will eliminate the very complex and expensive interference

procedure available within the U.S. Patent Office to determine inventorship.

Third Party Review of Patent Office Decisions

Under present U.S. patent law, once the Patent Office issues a patent, the public has the ability to file a request for re-examination of the granted patent. The re-exam request is based on and limited to printed "prior art," including patents and publications that a re-exam requester alleges invalidates one or more claims of the patent. Also, depending on the vintage of the patent, the requestor's participation in the re-exam process may be permitted under present law.

Under the proposed new legislation, the rights of third parties will be further expanded and a third party post-grant review process will be available. This is primarily based on the belief that third parties have more incentive to weed out "bad" patents. Thus, in addition to the current reexamination procedures, third parties will be permitted to request review of the granted patent through the post-grant review process. It is expected that the post-grant review will be broader than the present scope of re-examination procedures, which are limited to prior art patents and publications. In addition, the legislation would allow third parties to send prior art to the Patent Office during the pendency of a patent application prior to its issuance as a patent. Presumably, third parties will have become aware of a competitor's potential patent once the Patent Office has published the corresponding application. The main purpose of adding greater third party participation in both the pre-grant and post-grant era is to ensure that weak patents are eliminated. The proposed legislation is in response to third party

criticism, whether deserved or not, alleging that the Patent Office is not "doing its job."

False Patent Marking

In an earlier column, we discussed the relatively recent spate of false marking suits that have been brought under the false marking provision of the patent statute. These cases allege that certain products have been marked with patent numbers representing patents that are either expired or do not cover the product. Penalties are available under the false marking provision, and any penalty that a court grants or that parties settle upon is split between the plaintiff and the U.S. government. Presently, anyone may bring a false marking action. The proposed legislation would not remove the false marking provision from the statute, but, rather, would require that the entity bringing the action demonstrate that it has actually been harmed by the alleged false marking.

Controversial Provisions

One of the reasons patent reform legislation has bounced around Congress for so long is due to the presence of a number of industry-dividing provisions. Earlier versions of the legislation would have imposed limitations on damages for patent infringement. Industries are divided on this issue. High-tech companies were in favor of the proposed limitations, while pharmaceutical companies were against such limitations. Rather than let these provisions torpedo the remainder of the legislation, the Congress has removed them from the current bill. These changes should increase the chances of the new legislation becoming law in the current Congress and, if passed, such legislation will probably be the most comprehensive reform of U.S. patent law since the 1952 Patent Act, almost 60 years ago. 



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INDUSTRY NEWS

Announcing IWLPC Platinum Sponsors

As plans for IWLPC's 2011 technology program are well underway, *Chip Scale Review* magazine and SMTA are pleased to announce this year's Platinum Sponsors, Amkor Technologies and EV Group.



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products include wafer bonding, lithography/nanoimprint lithography (NIL), metrology, photoresist coating, cleaning and inspection equipment. Founded in 1980, EVG is headquartered in St. Florian, Austria, and operates via a global customer support network, with subsidiaries in Tempe, AZ.; Albany, NY; Yokohama and Fukuoka, Japan; Seoul, Korea and Chung-Li, Taiwan. [www.EVGroup.com]



Press lunch panelists, left to right, Dirk Hilbert, Alain Astier, Heinz Kundert, André-Jacques Auberton-Hervé, Jens Drews

SEMI ISS Europe: Capitalizing on European Strengths in the Supply Chain

The SEMI Industry Strategy Symposium (ISS) focuses both on strategy and technology, exploring how to best position the unique added value of Europe's semiconductor industry on the global market. Held at different locations each year, the 2011 event took place in Grenoble, France from Feb 27-March 1. During the press luncheon, European industry executives offered their perspectives. Here are some highlights:

- Heinz Kundert, President, SEMI Europe and moderator of the press conference, reported that that SEMI has made progress in getting the European Commission and EU States to recognize the semiconductor industry as strategic for Europe, and make it a priority to maintain Europe's competitiveness.
- Alain Astier, Group Vice President, Industrial Strategy, STMicroelectronics and member of the SEMI Europe Advisory Board talked about Europe's strengths, most notably the ability to work together in partnership across the value chain.
- Jens Drews, Director Government Relations, GlobalFoundries talked about the company's investment in Dresden, where they are hiring 80 new employees a month. He said this is proof that Europe can be competitive in the microelectronics industry.
- André-Jacques Auberton-Hervé, President and CEO, SOITEC, and chairman of the SEMI Europe Advisory board addressed the need to support those European businesses capable of creating and mass-producing new products in order to create a virtuous circle of growth in their ecosystems. Three competitiveness pillars for Europe include applied

research to set up the required technology platforms, industry consortiums to build pilot demonstrator production lines, and competitive, solidly-anchored local businesses with mass production capabilities.

- Dirk Hilbert, Deputy Mayor, Dresden, Germany gave some interesting statistics about how Germany's public investment in the industry has achieved returns in excess of 100%, and means that the tax revenues generated actually outstripped the initial investments.

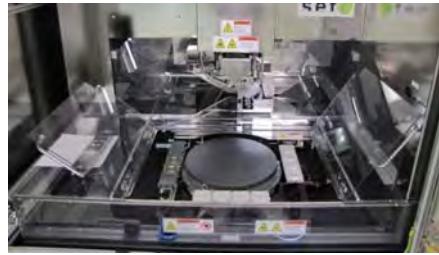
Henkel and Hitachi Chemical Sign License Agreement for Die Attach Film

Henkel Corporation announced it has entered into a license agreement with Hitachi Chemical Co., Ltd. for the worldwide manufacture and sales of certain dicing die attach film. In this agreement, Hitachi Chemical has granted Henkel a worldwide license under the technology described in Hitachi Chemical's Taiwanese Patent No. 303454, and all related counterpart patents to manufacture and sell dicing die attach film.

Leti Develops C2W Direct Metallic Bonding Technology

CEA-Leti has established a multi-partner project to demonstrate high-alignment-accuracy (<1µm) chip-to-wafer (C2W) structures made by direct metallic bonding. Such structures are required for high-performance 3D integrated circuits and could enable a wide range of applications in microelectronics as well as in optoelectronics or MEMS.

Leti developed this C2W direct-metallic-bonding technology to break through certain 3D-integration limitations. For example, the technology allows chips to be attached to a substrate at low temperature and with low bonding pressure. This technology also allows for interconnecting



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the chip and the substrate electrically through local metallic bonding.

To demonstrate the technology, Leti acquired a customized 300mm FC300 pick-and-place tool from Smart Equipment Technology (SET). The equipment was developed by SET based on its high placement accuracy FC300 system to adapt it to direct-metallic-bonding requirements. It will be used by the Minalogic PROCEED project, a •4.2M 24-month project supported by French Fond Interministeriel Unique (FIU). Partners also include STMicroelectronics, ALES and the CNRS-CEMES.

"This collaboration puts Leti in a very good worldwide position for 3D-technologies development," said Leti CEO Laurent Malier. "We will identify the key challenges of 3D product engineering, and C2W strategy with direct-metallic bonding is a very promising option for overcoming those challenges."

Alchimer's Wet Deposition Products Licensed for MEMS 3D Research

To support its metallization processes for 3D MEMS, the Centre de Collaboration MiQro Innovation/MiQro Innovation Collaborative Centre (C2MI), located in Sherbrooke, PQ, Canada, has licensed Alchimer's suite of electrografting products. Alchimer provides nanometric deposition technology for through-silicon vias (TSVs), semiconductor interconnects, MEMS and other electronic applications to the semiconductor and MEMS industries. Electrografting is Alchimer's breakthrough electrochemical process that enables the growth of extremely high-quality polymer and metal thin films.

The C2MI, which includes a state-of-the-art MEMS facility, was launched in 2009 by Université de Sherbrooke in Bromont Technoparc, Quebec, Canada. The center's 200mm MEMS and 3D wafer-level-processing (WLP) equipment will enable its members to test a variety of materials for MEMS production.

"Alchimer's Electrografting technology dramatically increases yields in MEMS, 3D-IC and on-chip interconnects, and provides strong support for work in

advancing the technology for 3D MEMS manufacturing with a cost-effective approach," said Luc Ouellet, vice-president of R&D at pure-play MEMS foundry, Teledyne DALSA Semiconductor.

"The MiQro Innovation Collaborative Centre and its members are at the leading edge of 3D integration in MEMS," said Alchimer CEO Steve Lerner. "They are pushing the design rules in this space, and we are excited that they have chosen our products to support this work. This is another solid technical validation for Alchimer's products and wet deposition technology."

Worldwide IC Packaging Market, 2011 Edition, to be Released in May

The semiconductor industry has been cyclical since its inception, but the general trend for the industry is upwards. The downturn of 2009 reversed itself by the second half of the year, catapulting 2010 into a year of tremendous growth.

As soon to be released report, The Worldwide IC Packaging Market, 2011 Edition, offers an in-depth look at the worldwide integrated circuit (IC) packaging market. The forecasts of individual IC device markets are provided, for units, revenue, and ASP, from 2008 through 2014, with package solutions for each of these markets broken down into I/O ranges. Additionally, package types are rolled up to deliver an overall worldwide forecast of IC packages, divided into 12 different package families, plus bare die solutions.

The contract IC packaging market is forecast and supplied in a separate chapter. Units and revenue are analyzed by package family. Forecasts are computed by compiling information obtained from each individual contract assembly company. Pricing information is provided by I/O count and price per I/O, and when multiplied by units, yields revenue. Profiles of individual contract IC package assemblers are also provided, as is a chapter on the state of the industry.

The IC packaging market is evolving to keep pace with other changing markets. Through extensive primary and secondary research, this report presents an objective look at the world of IC packaging. [\[www.newventureresearch.com\]](http://www.newventureresearch.com)

(continued on Page 45)

Through Silicon Vias in MEMS Product Development

By Carolyn White and Alissa Fitzgerald [AMFitzgerald & Associates]

The demand for smaller, faster, and more powerful integrated circuits (ICs) has fueled aggressive development in the areas of materials, thin film deposition, lithography, etching, and packaging. While many of the fundamental designs were introduced decades ago, microelectromechanical systems (MEMS) and the concept of silicon as a mechanical material as a field did not mature into its own until the fabrication methods developed for ICs provided a platform for development.^{1,2} As it has developed, MEMS technology has tapped into the analog roots of ICs as well as pushed the boundaries of how we interact with the physical world. Along the way, MEMS engineers developed methods for deep silicon etching, thick film deposition, and wafer bonding. Many of these MEMS-specific processes are now finding their way back into ICs in the form of through silicon vias (TSVs) and wafer level package (WLP).

The advantages of TSV are well documented and include decreasing die size, allowing denser interconnect layouts, providing more reliable electrical connections, and hermetic cavity electrical feedthrough.^{3,4,5,6} Their benefits in WLP are especially attractive to MEMS and IC designers and manufacturers: simplified dicing, no wire bonding, and surface mounting without additional packaging.

In the IC world, TSV technology is providing a path beyond that defined by Moore's Law.⁴ It is enabling heterogeneous integration of memory, RF, logic, etc. and providing shorter, better insulated interconnects, which leads to increased data transfer speeds, decreased parasitic capacitance and increased bandwidth.^{5,6}

TSV can also improve integration of MEMS devices with ASIC chips. At one point, the holy grail in MEMS product development was a one-chip MEMS+ASIC solution. That approach proved to be cost prohibitive because of the discrepancy between the production yield of ICs

(>99%) and MEMS (>80%, if you are lucky!) and has mostly been abandoned in favor of a two-chip module. The need for smaller packaging (originally the motivator for the one chip solution) remains, especially for applications related to consumer electronics. TSV now presents an elegant solution to this problem.

TSV Type	Metal	Silicon
Conductor	Tungsten or copper	Highly-doped silicon
Insulator	Silicon oxide, silicon nitride, other dielectrics and proprietary materials	Silicon oxide, proprietary materials
Form factor	Deposited plug or sidewall coating	Formed from substrate material
Process order	Via first or last	Via first
Advantages	Lower resistance, higher density	Higher aspect ratio
Disadvantages	Lower aspect ratio, requires diffusion barrier layer	Higher resistance, lower density

Table 1. Summary of Metal vs. Silicon TSV Properties.

Types of TSV

There are many types of TSVs, but the overall components are the same: a conductive path through the wafer that is isolated from the rest of the substrate. The conductive path is usually supplied by metal (tungsten or copper) or doped silicon. The insulator ranges from oxide to proprietary films developed by TSV suppliers or individual manufacturers (**Table 1**).

Most TSV processing falls into two major categories, via first or via last, which refers to whether the via is done before or after device process steps, respectively.^{7,8,9} The CMOS compatibility of a process, the via fill factor and aspect ratio, wafer thinning, and thermal budget usually play a role in determining which TSV process is best for a particular device design.

The challenges of implementing TSV are real and can be daunting. Forming the via, or hole, is often the easiest part of the processing. Providing a reliable dielectric and/or conductive material fill — free of voids and with structural integrity — is the tricky part and can require significant development. Vias may be fully plugged with metal, or just sidewall coated; either way, subsequent thermal exposure during processing can cause metal to expand and contract, inducing strain in the substrate and sometimes resulting in failure of the TSV or the wafer.^{7,10} Thermal cycling can also affect the planarity of the metal fill and even the wafer, in turn affecting subsequent processing and/or wafer

bonding. Wafer thinning to reveal the TSV can also result in significant wafer warping or cracking.

Silicon vias use the substrate material as the conductive path, which needs to be isolated from the rest of the substrate and neighboring vias using a trench etch. The aspect ratio of the trenches around these types of vias is often quite large, and providing a conformal, mechanically sound dielectric fill requires considerable development and often pushes the limit of existing fabrication tools.

Progress has been made in finding solutions to these technical challenges with considerable development. Companies that have successfully developed TSV for MEMS and who provide foundry services include, but are not limited to, Austriamicrosystems, ALLVIA, IMT, IPDiA and Silex Microsystems.

Advantages of TSV for MEMS

In MEMS devices, TSVs can enable improvements at three levels: package, chip, and device. Some examples illustrating these improvements are described here.

Package Level Improvements: TSV for Medical Devices

The benefits of TSVs at the package level can be illustrated by a catheter pressure sensor, used in many medical procedures. The extreme form factor restrictions of catheters strongly affect the sensor design. Reduction in sensor size can allow for data collection where it previously was not possible, or allow the

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space to be repurposed for sensor improvements (e.g. increased range/sensitivity, temperature compensation).

The image on the left side of **Figure 1** illustrates a MEMS pressure sensor with conventional packaging components. Space on the silicon sensor must be allocated for bond pads. The bond pads are typically connected to a package substrate using wire bonds that have both vertical and horizontal space requirements and can make hermetic sealing difficult due to their surface area and fragility. The package substrate must then connect to a wire harness that relays the signal to an external data acquisition system.

TSVs can provide significant space and packaging improvements for catheter applications by eliminating the need for bond pads and enabling a direct connection to a much thinner flex circuit, as shown on the right hand side of **Figure 1**. Smaller die and smaller catheters can immediately enable new medical applications simply by being able to move into smaller spaces. For example, a femoral artery catheter is typically 4F-10F (1.3-3.3 mm in diameter), but a 3F catheter (1 mm) or smaller can fit into a coronary artery.

Chip Level Improvements: TSV in WLP

The benefits of TSVs at chip level can be illustrated by a WLP example, where a top cap wafer is applied to the device wafer to create hermetic cavities. **Figure 2** illustrates the footprint reduction that can be achieved using TSV to bring

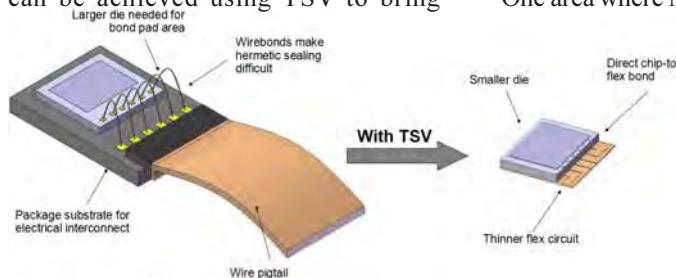


Figure 1. Package Level Improvements.

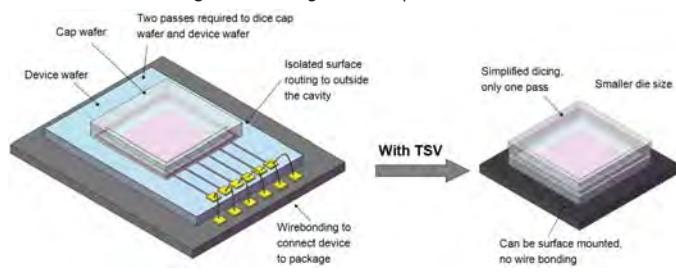


Figure 2. Chip Level Improvements.

electrical signals out from a hermetic cavity. Without TSVs, electrical connections must be made using lateral routing, which requires more surface area and extra process steps of masking, deposition and planarization. With TSVs, electrical connections can be made through the backside of the wafer.

In addition to saving silicon area costs, packaging costs can be reduced. In the first scenario, two wafer dicing passes must be completed, one to cut through the top wafer only and one to cut through the entire stack. This is required to have access to the electrical contact on the top surface of the bottom wafer. Once diced, standard wirebond techniques are used for interconnect, which take up package space.

With the TSV, only one dicing pass is needed though the entire wafer stack. The die can now be surface mounted with technology such as solder ball joints, saving time, space and cost.

Device Level Improvements: TSV for Bolometer Arrays

In some cases, TSV can improve the operation of the MEMS device itself. (A few of these benefits for ICs have been outlined previously in this paper.) In the field of MEMS, imaging technology has proven to be a beneficiary of the technology. For example, Toshiba was able to achieve a 55% reduction in volume and 36% in footprint in their chip scale camera by implementing TSVs.¹¹

One area where MEMS-based imaging technology is becoming increasingly prevalent is uncooled infrared imaging. MEMS fabrication techniques are used to produce bolometer arrays, which measure electromagnetic radiation by sensing small changes in temperature, usually by resistive means. MEMS bolometer development has enabled concurrent improvement of device performance and cost reduction

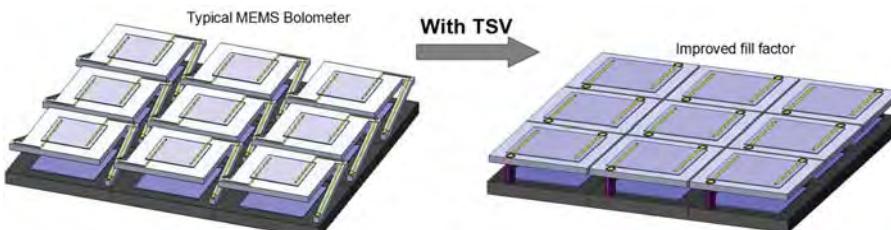


Figure 3. Device Level Improvements.

because the 3D fabrication techniques result in suspended sensing membranes with superior thermal isolation. In addition, MEMS-based WLP in vacuum has improved the performance of MEMS bolometers because the vacuum eliminates the thermal conduction of air between the device and the surrounding package.¹²

Another important contributing factor to MEMS bolometers' performance is the pixel fill. On the left hand side of **Figure 3**, a sketch of a typical MEMS bolometer design with space dedicated to electric interconnects and routing, is illustrated. Even in the best layout and processing situations, up to 25% of the imaging area can be consumed by these connections. When this routing is replaced by TSV, the area consumed by routing can be greatly reduced, improving optical fill factor and increasing pixel density. TSV also makes it easier to use wafer level packaging to package the bolometers in a vacuum.

Including TSV During MEMS Development

Until recently, TSV was only available to foundry customers, in other words, MEMS devices that were already being produced in volume. Integration of TSV could therefore not be considered nor implemented until the MEMS device was fully mature. However, an all too familiar situation for companies is to find themselves, after working hard to develop their core MEMS technology, having commercialization efforts delayed by packaging challenges, many of which could be easily solved with TSV.

Successful leverage of TSV benefits requires integrating and testing the technology early in the MEMS development cycle, not tacking it on later as an afterthought. TSV should be considered early in the overall MEMS design, since it may simplify MEMS design or possibly

create process issues that impact MEMS process flow. Likewise, the presence of TSV strongly influences package and assembly design. If a company waits until after MEMS development to consider TSV, they will likely discover that the pain, time, and cost of re-designing their MEMS device and package to accommodate TSV will more than neutralize the potential benefits of the technology.

Recognizing this important need for TSV during MEMS development, a MEMS development firm* and a pure play MEMS foundry† have teamed up to enable customers to integrate and evaluate proven foundry TSV technology in prototypes. Product cost, time, and risk may be reduced by identifying and solving package and process issues early, simplifying system design and reaping the benefits of TSV integration much sooner in the product roadmap.

Standardized TSV Technology

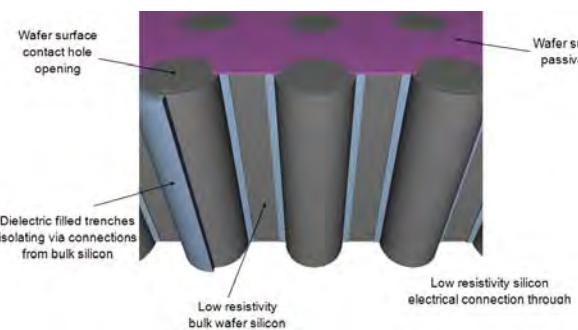


Figure 4. Cross-section of Sil-Via® Substrate. (Courtesy of Silex Microsystems)

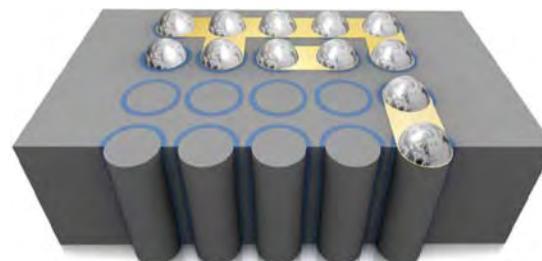


Figure 5. Surface Electrical Routing and Solder Bumps. (Courtesy of Silex Microsystems)

Sil-Via®, a proprietary silicon via technology provided by the MEMS foundry, has a proven history of volume production supply into a wide range of MEMS applications, including the cellular handset market.¹³ It is a via-first process and therefore must be considered in the MEMS design process.

The vias are formed by etching an annular trench into low resistivity silicon. The trench is then filled with a dielectric to isolate the silicon via from the substrate (**Figure 4**). The resulting via is mechanically stable and robust across a wide temperature range. Electrical connection to the via may be made using solder balls, gold stud bumps or similar technology (**Figure 5**). Sealed MEMS chips with TSVs may be directly mounted to circuit boards or flex circuits by surface mount techniques.

Methodology for Prototyping

Two possible options have been created for incorporating these silicon vias into MEMS prototypes. The first option uses a standard TSV pattern—similar in layout to a breadboard—that is available at lower cost and shorter lead time. Depending on the MEMS device design, an interconnect routing layer may be needed to integrate the device design with the TSV pattern. Such prototypes will likely have a less-than-ideal form factor, but for early stage development that may not be important.

The second option is a custom TSV pattern. This option incurs higher costs and longer lead times, but allows the TSV pattern to be built to the customer's specifications.

Figure 6 outlines the method for incorporating TSVs during the MEMS development process. Initial device design, modeling and layout occurs with silicon via design and fabrication rules in mind. During prototype fabrication, the TSVs are created first by the MEMS foundry, and then the MEMS development firm completes the device processing. Small wafer batches (10 wafers or more),



Figure 6. TSV Prototype Development Method.

which are essential during early stage development, are available. When prototyping is completed, the MEMS design can be quickly ramped up to volume, having been developed on a standardized TSV process platform.

Summary

Many MEMS devices can benefit from the use of TSV to meet performance demands, challenging form factors or packaging requirements. Too often, TSV is not considered until late in the development process or after the product design is finished. Integrating a standardized TSV during the prototyping stage provides a strategic advantage in terms of reduced timeline, risk, and cost. In particular, evaluating packaging solutions early on allows new MEMS designs to move faster and with more confidence into volume production.

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Sil-Via® is a trademarked and patented process developed by Silex Microsystems

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Technology Solutions for a Dynamic and Diverse WLCSP Market

By Ravi Chilukuri, *[Amkor Technology]*

The advent of wafer level chip scale packaging (WLCSP) in the semiconductor industry was driven by a strong push for cost reduction and miniaturization. The primary utilizers of this technology have been handheld or portable products, such as cell-phones, ipods, laptops, and netbooks. However, more recently, WLCSPs are gaining foothold in other industries, such as servers and automotive electronics. Initially, reliability performance limited the use of WLCSP to smaller die sizes (<2.5mm), lower pin counts (<25), and mature silicon technology nodes, making WLCSP an excellent match for the analog/mixed signal space. With the maturity of WLCSP in this market, WLCSP has transitioned from an advanced package to a commodity product. Lower cost WLCSP solutions have become a requirement due to growing price pressure and cost inflation of materials and equipment. The cycle time pressure has increased due to the changing business models and supply chain strategies in the new economic environment. To meet these growing market demands, WLCSP providers are faced with the challenges of providing faster cycle times and higher capacity without significant increases in capital expenditure.

Simultaneously, several recent technology advances have enabled WLCSP use in products with pin counts up to 200 and die sizes up to 7mm, opening the application space to RF, high speed, broadband, and memory components as well. Consequently, WLCSP is expanding to markets and applications previously supported by QFN and flip chip CSP. This expansion puts additional price and cycle time pressure on WLCSP manufacturing. Further, many of the above applications require advanced silicon technology

nodes using low-*k* dielectrics, which present unique challenges of their own. Unlike the QFN and fcCSP packages, where the low-*k* silicon die is fully encapsulated and supported by underfill/overmold, the WLCSP has exposed die in which the fragile low-*k* layer needs to withstand higher effective mechanical stress and the die chip-out needs to meet more stringent criteria. To address these concerns, there has been development involving new materials, processing techniques and design rules.

Hence, WLCSP technology development has focused on cost reduction as well as on functional integration. The focus on cost reduction applies more to the mixed signal/analog space using 200mm wafers primarily where WLCSP has become a commodity. The focus on functional integration has involved developing technologies compatible with advanced silicon nodes (90nm down to 45nm), technologies for die with higher pin count (~200) and fan-out wafer level (FOWL) technologies. Much of this application space uses 300mm wafers.

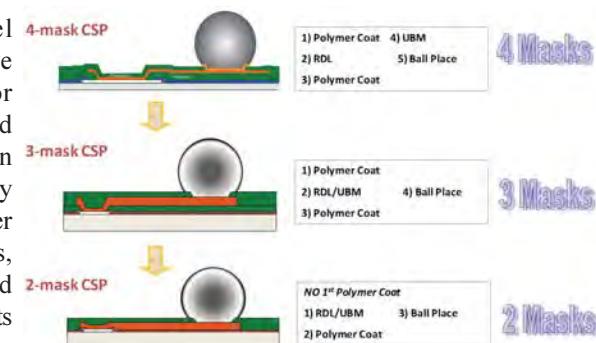
In addition, board level reliability requirements have become more stringent for both temperature cycling and drop tests. With miniaturization and addition of functionality for the smart phones and other advanced electronic gadgets, power management and thermal dissipation requirements have increased. Thereby, significant improvement in temperature cycling requirements have become a primary concern for many applications. Further, with the introduction of WLCSPs into the smart power IC space involving memory components, there has been a need for polymer materials with lower cure temperatures that preserve the programming of

memory components during WLCSP processing. The RF and high speed devices benefit from having polymer layers with low dielectric constant and high breakdown strength. Many of these needs can be catered by the use of PBO based polymers.

This paper examines material options i.e., polymers and solder alloys for new lower cost WLCSP structures as well as the effects of die sizes and I/O counts on product reliability. In some cases, typical failure modes are also presented.

Background

There are currently several flavors of WLCSP technologies in the industry, most of which use a 4-mask approach consisting of 2 layers of polymer, a redistribution layer and a UBM (under bump metallurgy) under the solder bump.* As discussed previously, the recent focus has been to develop cost effective RDL based WLCSP options** that meet the reliability requirements for most WLCSP applications.¹ Both of these



technologies are derivatives of the current HVM offering. A comparison of these technologies is provided in **Figure 1**.

Unlike the 4-mask approach, the three mask stack-up provides cost and cycle time savings through elimination of process steps and lower material costs. Further cost reduction can be

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realized through a two-mask approach, where the first polymer layer is left out of the device stack-up. Early data demonstrated that the board level reliability (BLR) performance of the above three technologies is comparable and meet the generally accepted guidelines for reliability performance.² the 3-mask CSP has since been tested for package level reliability using PBO, in addition to Polyimide (PI). Extensive BLR studies have also been done comparing PBO to PI. Solder alloy comparisons have been done using BLR on both the three- and two-mask CSP.

Package-Level Reliability

A number of package-level reliability tests were performed on parts built using the 3-mask structure with PI for both the first and second polymer level (**Table 1**). The die design used was a

Test Item	Test/Pass Condition
Multiple Reflow	260°C, 5X
Preconditioning at Level 1	85°C/85%, 168hrs, reflow @260°C peak
Preconditioning at Level 3	30°C/60%, 192hrs, reflow @260°C peak
Autoclave (PCT)	121°C, 2 atm, 100% RH, 168 hrs
Unbiased HAST	130°C, 85% RH, 168 hrs
Temp Cycle (TC)	-55°C/+125°C, 1000 cycles
High Temp Storage (HTS)	150°C, 1000 hrs

Table. Package level reliability tests performed on Polyimide and PBO based 3-mask CSP structures

5.5mm x 5.5mm x 0.28mm die with a 10 x 10 full bump array at 0.5mm pitch.

All the parts were preconditioned at MSL1 requirements. Parts were electrically and optically tested prior to preconditioning, after preconditioning, and after reliability testing. Bump shears were also performed following the reliability tests. The same process and tests were repeated on parts built using PBO for both the first and second polymer levels.

PI vs. PBO BLR Comparison on 3-mask CSP

In addition to the package-level reliability, board level reliability (BLR) was also evaluated for PI-based 3-mask CSP vs. PBO-based 3-mask CSP. The die design used for the BLR tests was a 5.3mm x 5.3mm die with a 12 x 12 full bump array at 0.4mm pitch. The solder alloy used was SAC405. JEDEC drop test and thermal cycling were evaluated. The drop test board was an 8-layer board, and the thermal cycle board had 4 layers. The boards used were NSMD with 250µm diameter Cu pads.

The JEDEC thermal cycling condition used for this study was JEDEC JESD22-A104C, Condition G.3. Parts were cycled between -40 to 125C at 1 cycle/hour. The temperature ramp was 18min. and the dwell time at temperature was 12min. Three boards with 15 mounted WLCSP devices were used for each test case. The comparison of PI-based 3-mask CSP versus PBO-based 3-mask CSP shows >2X improvement in the mean life with the use of PBO (**Figure 2**). With the PBO, mean life was greater than 1000 cycles for this 144 I/O die with first fails of greater than 600 cycles. The failure modes for both the PI and PBO versions were noted to be in bulk solder.



Andy Mackie PhD, MSc
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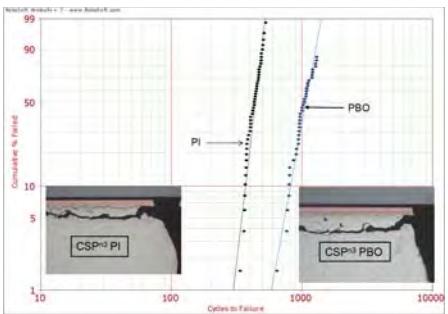


Figure 2. Temperature cycling performance comparing PI and PBO versions of 3-mask CSP

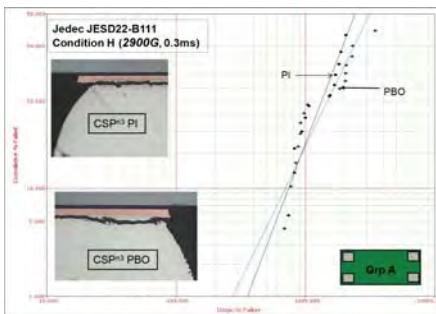


Figure 3. JEDEC drop test performance comparing PI and PBO versions of 3-mask CSP

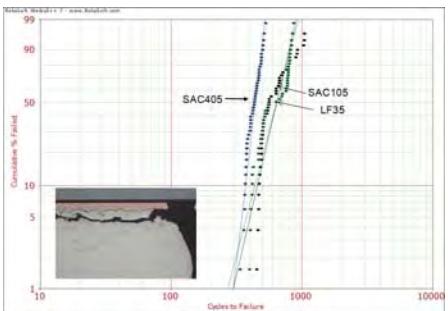


Figure 4. Temperature cycling performance comparing solder alloys on PI based 3-mask CSP

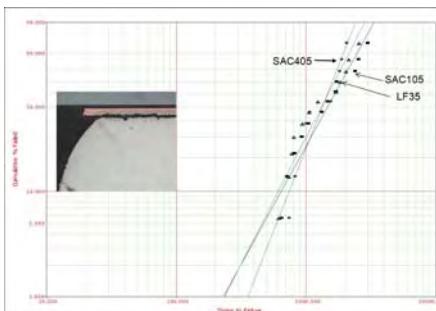


Figure 5. JEDEC drop test performance comparing solder alloys on PI based 3-mask CSP



Figure 6. Temperature cycling performance comparing solder alloys on PI 2-mask CSP

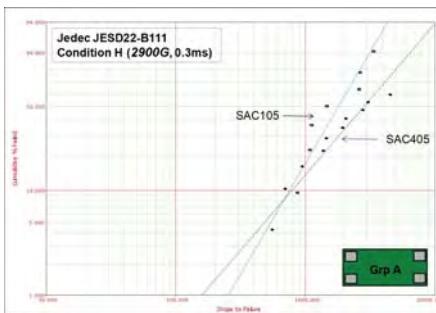


Figure 7. JEDEC drop test performance comparing solder alloys on PI based 2-mask CSP

The setup of the board level drop tester follows the guidelines of JEDEC drop test standards, with 15 WLCSP devices (3 x 5 matrix) assembled on a test board (132 x 77mm).⁴⁻⁶ The testing described in this paper applied the aggressive JEDEC condition H (2900G/0.3ms). The widely used JEDEC condition B (1500G/0.5ms) proved to be impractical for these parts due to the extensive testing time required to collect sufficient data for statistical analysis. Four boards per test case were utilized for drop testing.

Previously, the drop performance of the 3-mask CSP for both JEDEC drop condition H (2900G/0.3ms) and condition B (1500G/0.5ms) was compared.¹ From failure analysis, the primary failure mode was found to be the separation through the IM at the Pb-free/Cu interface. The

acceleration factor between the two different drop conditions for this type of IMC failure was 3 x. A comparison of the condition H drop test for PI versus PBO shows no difference in the drop test performance (Figure 3). For both cases, the mean life was > 1000 drops at condition H indicating an expected life of >3000 drops at the industry wide typically used condition B using the above acceleration factor.

Solder Alloy BLR Comparison

BLR was also evaluated for multiple solder alloys for the PI-based 3-mask CSP. The solder alloys compared were SAC405, SAC105 and LF35. The die design used for the BLR tests was a 5.3mm x 5.3mm die with a 12 x 12 full bump array at 0.4mm pitch. The boards

used were NSMD with 250 µm diameter Cu pads. The BLR test conditions used were the same as those described in the previous section.

There was no significant difference in the thermal cycling mean life with different solder alloys on the 3-mask CSP (Figure 4). The plots for SAC105 and LF35 overlapped, as may be expected due to the similar silver content in these two alloys. Interestingly, the SAC405 performance was equivalent to SAC105 for the 3-mask CSP structure, within the limits of standard test variation. Failure modes for thermal cycle stressing were typically bulk solder failures.

Likewise, the drop test performance of the different solder alloys on the 3-mask CSP was equivalent (Figure 5). Despite using the more aggressive drop test condition H, the first fails were at > 600 drops. This performance far exceeds the typical industry requirements for drop tests. The primary failure mode for drop was noted to be at the copper solder intermetallic layer.

Solder Alloy BLR Comparison on 2-mask CSP

BLR was also evaluated for multiple solder alloys for PI based 2-mask CSP. The solder alloys compared were SAC405 and SAC105. The die design used for the BLR tests was a 5.5mm x 5.5mm die with a 10x10 full bump array at 0.5mm pitch. The boards used were NSMD with 235um diameter Cu pads.

There was no significant difference in the thermal cycling mean life with different solder alloys on the 2-mask CSP (Figure 6). The SAC405 performance was equivalent to SAC105 for the 2-mask CSP structure as well, within the limits of standard test variation.

Likewise, the drop test performance of the different solder alloys on 2-mask CSP was equivalent (Figure 7). Despite using the more aggressive drop test condition H, the first fails were at >500 drops. This performance far exceeds the typical industry requirements for drop tests.

Bump Pitch/Height BLR Comparison

The most common bump pitches used for WLCSP are 0.4mm and 0.5mm. The 0.5mm pitch is fairly common on the

analog and power management ICs, and on devices going into lower-end phones. The 0.4mm pitch has become main stream in the last couple of years for WLCSP with its growth in RF/high speed devices. For testing the impact of the different pitches on the 3-mask CSP, test vehicles were chosen with the same bump array at both 0.5mm pitch and 0.4mm pitch. The bump height for 0.5mm pitch and 0.4mm pitch devices was 250 μ m and 210 μ m, respectively. The BLR was evaluated for above test vehicles built using PI and SAC405. The 0.5mm pitch die design used was a 5.5mm x 5.5mm die with a 10 x 10 full bump array. The boards used were NSMD with 235 μ m diameter Cu pads. The 0.4mm pitch die design used was a 4.5mm x 4.5mm die with a 10 x 10 full bump array. The boards used were NSMD with 250 μ m diameter Cu pads.

There was no significant difference in the thermal cycling performance of the two test vehicles on 3-mask CSP. Both samples exhibited first fails close to or greater than 1000 cycles, with mean life close to 2000 cycles. However, the drop test performance of the 0.4mm pitch device was better than that the 0.5mm pitch device. Despite using the more aggressive drop test condition H, the first fails were at > 400 drops for both samples. The mean life for 0.4mm pitch devices was however 2xX greater than the 0.5mm pitch devices.

Conclusion

The BLR drop and thermal cycling data for 3-mask CSP and 2-mask CSP position these technologies as cost effective and viable WLCSP options. A comparison of PBO and PI based 3-mask CSP technologies exhibited >2 x improvement in thermal cycling life and comparable drop performance using PBO. With different solder alloys, both 3-mask CSP and 2-mask CSP exhibited equivalent TC and drop performance. The 0.4mm and 0.5mm pitch devices showed equivalent TC performance.

* Amkor's WLCSP offering, CSPn1 .

** Amkor's CSPn3 and CSPn2

Acknowledgements

Appreciation is extended to our colleagues from the R&D group of

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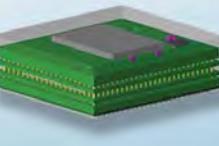
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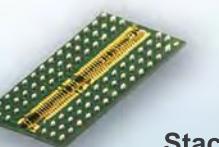
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Co-design Optimizes System Interconnect Paths from ASIC to Package to Board

By Real Pomerleau [Cisco Systems, Inc.] and Carlos Moll [Cadence Design Systems]

Historically, a semiconductor chip and the package and PCB that house it have all been designed independently. One design is completed and “thrown over the wall” to the next design team. Quite often, the PCB designer is challenged with the task of untangling interconnect that would have been better organized to connect to other devices on the PCB. A number of different design challenges, such as faster data transfer speeds, reduced overall product cost, and miniaturization of the final product size, have complicated the design process to the point where an over-the-wall approach is no longer a viable strategy. Chip, package, and PCB design must be a collaborative project to meet final product design goals.

In the absence of such a collaborative process, the package designer often finds himself caught in the middle and sometimes becomes the scapegoat when a design requires a re-plan or a re-spin. For example, if package skew was not properly planned for in the overall interface timing, a chip with a high speed DDR3 interface may not be able to meet timing at the fastest memory speeds. However, if the package had been optimized within the context of the chip and the PCB, meeting timing requirements could have been much easier.

Cisco and Cadence have spent the last couple of years developing a methodology that enables a package to be optimized within the context of the chip and PCB. This process was developed out of necessity when signal and power integrity issues were becoming almost impossible to resolve strictly as a PCB issue. Together, the companies found that with the right tools and methodology, time and expense can be reduced while design quality is increased.

SI and PI problems haunt both the electrical and physical domains. When designs are “thrown over the wall,” the design is typically done by someone with

little knowledge of the overall system constraints. With such a “siloe” design, the IC package designer may be forced to deal with a die design where the padding and bump array (for flip chips) or passivation openings (for wire-bonded chips) are located sub-optimally from a packaging perspective. Package-level signals may be routed underneath and straight across the die core—potentially causing signal and power integrity problems—and parallel bus interfaces may have different routing lengths—causing signal skew across the bus. Signal wires may be scattered around the package footprint with little regard to return current causing more problems. Differential pairs are also sensitive to skew.

Ideally, these signals should have matched physical and electrical lengths. At lower interface speeds, there’s enough timing margin to overcome such mismatches, but with GHz+ signaling rates, there is literally no margin to correct these mismatches on the PCB. Signal quality, crosstalk, and timing are all significant system-level challenges even with an optimized package. Trying to correct the effects on the board of a poorly designed IC package on GHz+ interface speeds is close to impossible.

When power-delivery systems at the die, package, and board levels are designed separately by different design teams, there is no opportunity to optimize the power-delivery network (PDN). Lack of, or improper use of package decoupling capacitors can possibly be fixed with additional PCB decoupling for slower-speed board designs, but today’s high-speed systems require far better, more integrated PDN design to avoid severe PI problems. Separately designed PDNs at the PCB, package, and die levels can produce some unexpected results once they’re coupled together. Integrated co-design of all three PDNs is clearly the right approach.

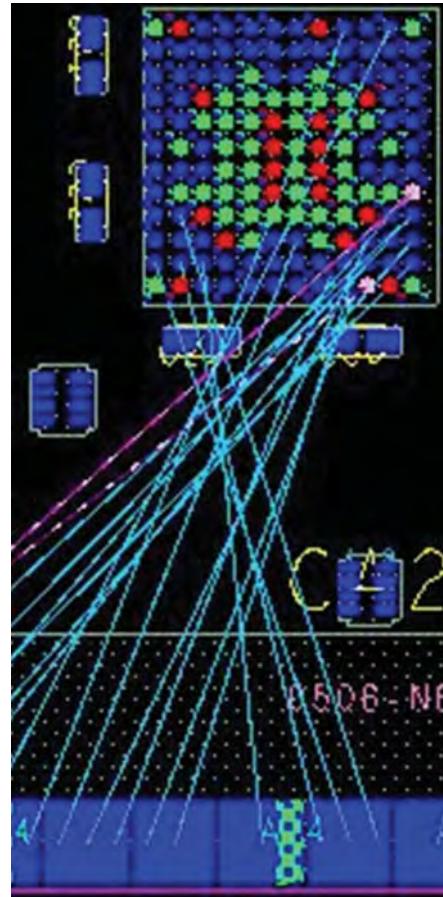


Figure 1. Un-optimized connectivity between a BGA package and a connector on a PCB

Co-Design Reduces Package Costs

Integrated co-design at the die, package, and board levels can also help reduce the IC packaging cost. ASIC packages come in two types: ceramic and organic. Ceramic packages have a large number of layers to distribute die signals, but they cost more and are generally single-sourced. In contrast, cheaper organic substrates are typically limited to fewer signal layers, complicating the efforts to break signals out of the die.

There are also practical limits to the number of PCB layers. Engineering teams often find themselves up against the maximum number of layers for a given board thickness or cost. High ASIC pin counts complicate matters because the

large number of I/O signals must escape the ASIC's shadow on the board, which often consumes many board layers.

When an overall system design is driven by components with predefined pin-outs, it is possible to end up with an interface where all the assigned signal pins are the mirror image of what is desired. **Figure 1** shows the multiple "rat's nests" that can result from such a constrained design approach. Connecting components with multiple rat's nest interconnect problems is a nightmare for board-layout engineers. Un-routed signals that cross over each other will increase PCB layer count and consume most if not all of the available routing channels, making the routing of other interface signals all the more challenging.

Microsoft Office Applications Aren't Design Tools

Several years ago, Cisco started to look at system-level interconnect design optimization. Early approaches required frequent meetings, emails, and re-purposed office applications such as Microsoft Visio, PowerPoint, and Excel to manage design data. Graphical data was communicated between teams using Visio and PowerPoint and netlist data was managed with Excel. Change requests from the IC design team were common and merging these changes into one Excel spreadsheet, which also tracked package and the PCB changes, was a manual and error-prone process. There was constant concern that something would go wrong and the only verification available was manual, line-by-line checking that verifies signals match from chip to package to board.

In the past, designers used separate package and board design tools. As a result, coming up with an optimized overall solution was a struggle. Large-scale changes, such as moving a bus from a package's North to South side, were fairly straightforward but without an integrated view of chip, package, and board, it was difficult to see problems such as a parallel bus mirrored between devices (which creates crossing rat's nest on the PCB).

These problems drove the need for an integrated board, package, and die design environment. Collaboration among chip, package, and PCB designers was clearly necessary to build a reliable and cost-

effective product, and automation was also required. EDA companies were already aware of the need for each of these three design groups to communicate more effectively, and addressed the issue by developing a full co-design solution. On the physical side, the capability existed to import the chip's I/O pad-ring definition into the package-design tools. Package

and PCB designs were also optimized in one tool. However, before collaboration, these were separate steps and what was needed was a seamless flow.

In-House Package Design is a Strategic Advantage

During this collaboration, the advantage of bringing the package design internal

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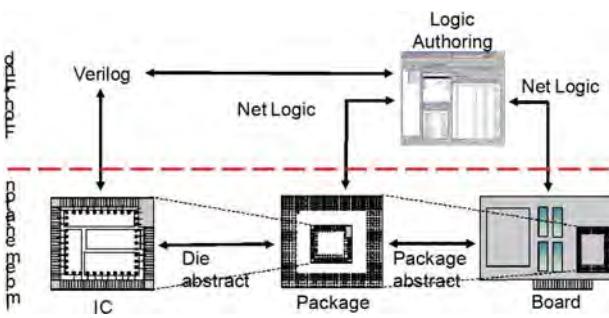


Figure 2. Using System Connectivity Manager to author hierarchical IC-Package-PCB netlist

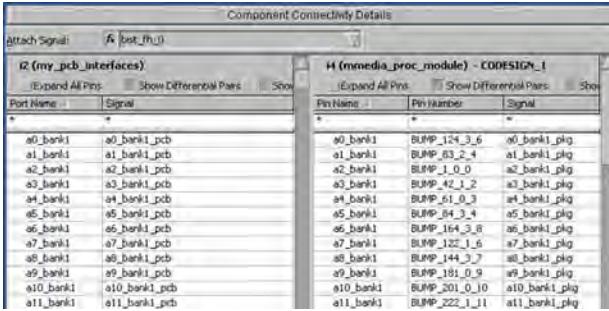


Figure 3. The System Connectivity Manager (SCM) component connectivity pane can maintain different name spaces between PCB, package, and IC environments

to the end-user became clear, especially when considering the power and signal requirements for the company's latest ASICs. Designing the IC package and board together gives better control over the package footprint, which can save layout engineers a lot of board-routing time. Focusing on the PDN and optimizing the distribution of decoupling capacitors allows a reduction in overall capacitor count. This, in turn, reduces the overall product cost.

While in-house package design makes it possible to work efficiently, it's beneficial to also have the option of outsourcing package design to a third party. However, this is only possible through a distributed methodology where abstract information about chip, package, and PCB can be communicated bi-directionally with the third party.

A pure vendor-supplied EDA flow is preferable because it is both expensive and risky to maintain in-house tools and software solutions. The latest versions of EDA tools provide netlist management* as well as a single-window view of chip, package, and PCB (see **Figure 2**) for implementation. Putting all three views together makes optimization and signal management much easier.

One major difficulty in the past was managing netlists across entire systems and

keeping track of net names as a signal traverses various design hierarchy levels. The netlist management tool has been a great help in managing this hierarchical connectivity maze. Its ability to map net names among the PCB, package, and IC environments has proven quite convenient. It's easier to define and maintain connectivity definitions in connectivity pane tables. Because it is only a logical tool the nets can be connected to the new ASIC knowing that they will be physically optimized later in the flow.

Die footprint and bump connectivity can be brought into the netlist management tool in several

ways. It was designed to take advantage of the implicit hierarchy that exists between PCB, package, and die, allowing for maintenance of three different name spaces that are displayed simultaneously (see **Figure 3**).

The connectivity flow across the design hierarchy must be untangled before any physical implementation tasks begin and optimally untangling connectivity across multiple hierarchy levels is complicated. At this time, this tool implements some simple heuristics to help untangle pin assignments but there's no guarantee that physical implementation of the result is possible. The capability of iterating between logical and physical tool set helps zooming in on a solution.

At any point in the flow, the netlist management tool can import the current status of the PCB or package tool database to synchronize it with the logical definition. Because the BGA is being co-designed with die and PCB, pin optimizations to the

BGA automatically propagate to the PCB as well. A simple ECO process propagates pin-out changes through the system if the co-designed BGA package or die changes.

Co-Design Promotes Design Reuse

The co-design solution further enhances the overall design productivity process by allowing design reuse of both logical and physical data. The integration of die, IC package and PCB at the logic level allows the reuse of blocks, library components, and fabric dependent signals. At the physical level, design reuse provides a mechanism to reuse IC place and route, package and PCB power, ground, and signal distribution. It may also include routing and optimal return path via reference locations for high speed signal reference.

Importing parts of existing designs, such as a memory complex from Design

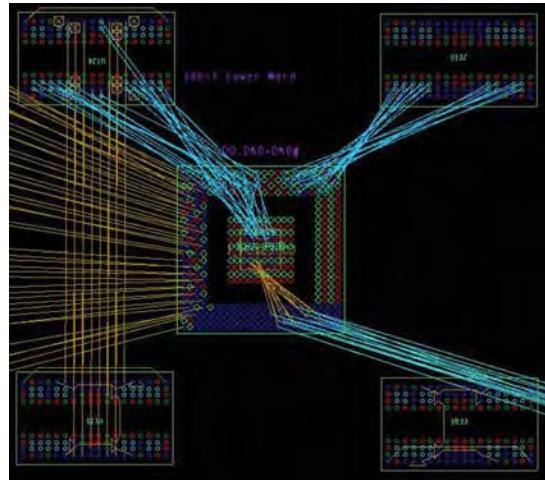


Figure 4. Single-canvas interconnectivity view including PCB, package, and IC (before optimization)

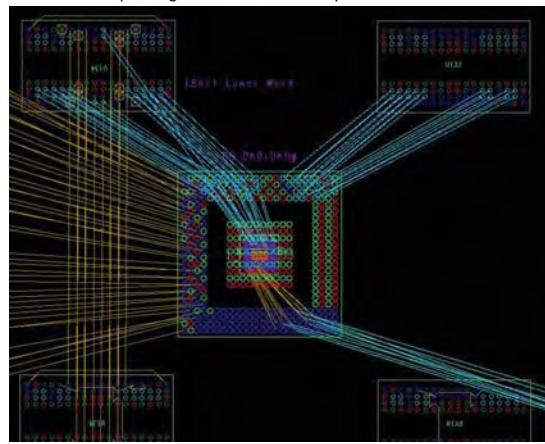


Figure 5. Single-canvas interconnectivity view including PCB, package, and IC (after optimization, no rat's nests)

A or a processor complex from Design B and several custom ASICs from Design C into a new design is tremendously useful and significantly speeds design. The netlist management tool is an ideal place to support these types of transactions.

Knowing the components on the PCB, BGA pin-out can be defined on the PCB to optimize board routability. Then, the BGA footprint can be driven into the IC package and then into the IC pad-ring, which gives a very clean data path through the interconnect design. This path makes the PCB easier to route so that focus can turn to optimizing the electrical performance of high-speed interfaces such as a SerDes differential pair or wide, high-speed, source-synchronous buses. In cases where an IP block on the die has a fixed pin-out, the pin-out can be mapped up through the package to the board and resolve any tangled nets at the PCB or package levels.

The layout of the PCB, package, and IC pad ring is now viewed in a single canvas. Although this tool flow is still a work in progress, it provides a first-cut mechanism to optimize data paths through board, package, and chip (see **Figures 4** and **5** for before-and after-optimization views).

Summary

Automatic pin optimization permits global pin-assignment changes among PCB, package, and IC. Individual pin-swap capabilities allow quick fine-tuning of assignments (see **Figure 6**). Once optimizations are complete the results are read back into the netlist management tool, then export individual board and package files for physical layout. IC pin definitions are written from the single-canvas view and then imported directly into an implementation system for the IC design.^{**} This design flow preserves net names for each of the three design spaces.

By designing the IC package in-house, it's possible to be more pro-active in the design of the system-level PDN, which gives a strategic advantage over getting the package design done outside. Delivering reliable power to the chip requires management of the path from the voltage regulator module, through the board, and through the package. Proper use of decoupling capacitors throughout the entire path is essential to an optimized PDN. Today's high-frequency designs have far less design margin with respect to the power-supply rails and there's great benefit in optimizing the PCB and package PDNs together. An added benefit, PDN optimization can

reduce the required number of bypass capacitors, which lowers overall product cost while improving system reliability.[●]

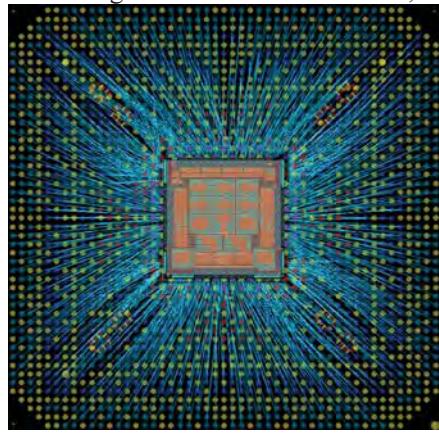


Figure 6. Optimized package and co-design die connectivity. Note the lack of crossing rat's nests



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A Reliable Low Cost Assembly Technology for QFN Packages

By WL Law, Nicole Yong, SH Liew, Daniel Phuah, KF Chung and PN Ng, [Carsem (M) Sdn. Bhd]

More and more, product demand and technological developments are being driven by portable consumer electronic devices like notebooks, GPS, multimedia players, digital cameras, camcorders, cellular phone handsets and accessories. Each succeeding product generation is expected to be smaller and lighter in weight, driving the needs of miniaturization technologies.

There are several options available for such technologies. One of the most cost effective and reliable options, sawn QFN packages, use almost the same assembly line infrastructure as typical leadframe based packages, and do not require totally new assembly technologies or un-established production technologies or material. This article describes process flow and development methodologies for key areas, outlining criteria adopted for materials selection, as well as reliability testing results.

Sawn QFN has become a popular and fast growing package, penetrating and absorbing the current lead package and even BGA device market because of its flexibility in body sizes, high productivity, and good reliability. Regardless of the QFN package size, function can be higher than that of the leaded platform. Additionally, due to the QFN leadless profile, it can be shrunk to thinner and smaller package sizes as compared to the current leaded packages of the same pin count.

In **Figure 1**, an ultra-small package, close to the size of fine sand, measuring only $0.3 \times 0.6\text{mm}$ in a thickness of 0.3mm has been developed as a 0201 SMD package-size-compatible sawn QFN product named X3 Thin QFN. It is mainly to be used as transient voltage suppressor (TVS) in ESD sensitive equipment such as mobile phones, digital cameras, camcorders, MP3 players and notebooks, as some of the examples. TVS is an electronic component used to protect

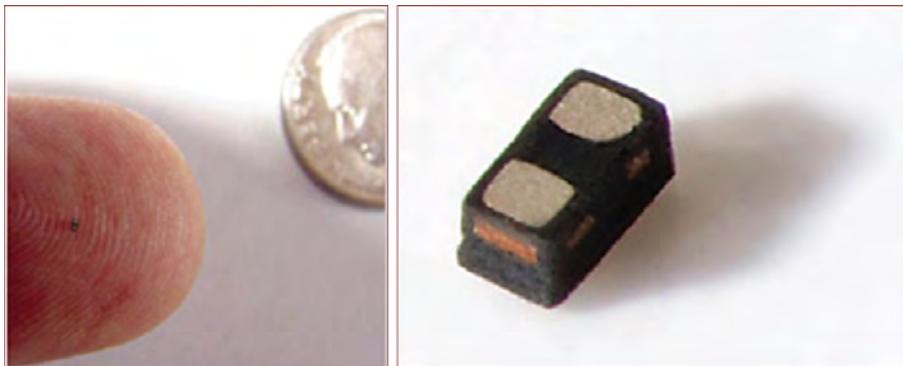


Figure 1. Actual and blown up size of an X3 MLP

electronics devices from very fast and often damaging voltage spikes induced on connected wires. Due to its extremely small footprint, it fits into the requirement of miniaturizing the size and weight of the small hand held electronic devices.

Package Size Requirement

Figure 2 shows a basic internal structure of a QFN TVS comprising a plastic molded package with a diode die attached to a leadframe (LF) using die-attach adhesive (epoxy) internally and a wire connecting the diode die to the external package. As the package gets smaller and thinner to an intended package size of $0.6 \times 0.3\text{mm}$ and thickness 0.3mm , all these aforementioned elements need to be reduced to compatibly smaller and thinner dimensions to fit into the ultra-small package. The die thickness, epoxy, and LF would have

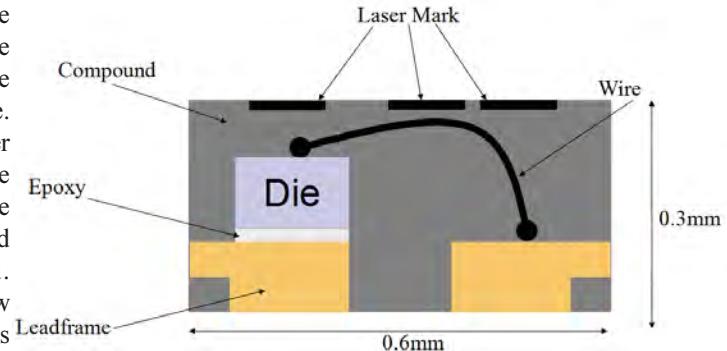


Figure 2. Schematic of X3 Thin QFN Package Construction

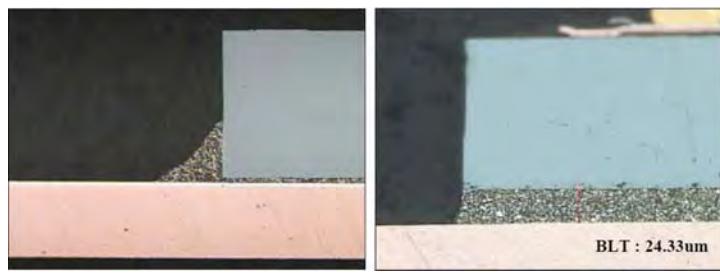
and processes when dealing with the reduced dimension of the various elements in order to build a good, reliable, ultra-small thin package. The materials and the processes may need to be reestablished to accommodate these new requirements.

Materials Requirements

The standard LF thickness used for QFN packages ranges from 5 - 8 mils to cater to package thickness of $0.4 - 1.0\text{mm}$. To shrink packages further to thicknesses of 0.3mm , the LF thickness also needs to be reduced to $<5\text{mils}$. Based on the availability and readiness of the LF supplier as well as the compatible assembly technologies, the conventional QFN leadframe format with $<5\text{ mils}$ thickness was selected.

Because the material thickness is lower but the frame size is similar to thicker LF,

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Die Edge with Epoxy Flow and Fillet Die Edge with No Epoxy Flow nor Fillet
 Figure 3. Schematic of X3 Thin QFN Package Construction

characterization studies on its rigidity and warpage throughout the processes needed to be performed.

Die must be thin and small to fit into the package but not too thin and too small that the assembly processes are unable to be performed or are difficult to handle. The die, usually a diode, requires conductive epoxy to provide the electrical conductivity between the die and the die pad.

For the small die size of the X3 Thin QFN, it is important to prevent any die tilt that may cause an inconsistent wire loop height during wire bonding. Due to the small package size, there is insufficient clearance to accommodate epoxy flow as commonly available in the larger QFN packages. Therefore, it is preferably to select epoxy type with no epoxy fillet after die attach as described in **Figure 3**. Eutectic die attach or die attach film are options that meet these requirements. However, they were discarded due to several constraints. Instead, wafer backside coating (WBC) was selected.

Wire must be conductive, of suitable thickness and properties to form ultra low loop to provide sufficient wire to package top clearance to prevent exposed wire after molding or laser marking.

It is essential to select a fine filler compound to completely fill the narrow space within the ultra-small thin package. The flexural strength and modulus are also important so that the compound is able to provide appropriate mechanical strength when dealing with thin and flimsy strips prior to the singulation process.

Processes Development Study

Along the assembly front end of line (FEOL) and back-end of line (BEOL) processes, we have carried out many characterization studies to create a robust X3 product including die attach characterization study, compound selection, laser mark study, saw singulation process optimization and offloading.

Die Attach Characterization Study

As the die size gets smaller, it becomes a challenge at die attach. The pick-up tool needs to be small enough to grip the die effectively but the small size tool would lead to low vacuum performance as well as short tool life. Die ejection is also critical since the needle needs to be small enough to have good ejection but its small size can easily lead to indentation on the die back. However, it is also important to ensure that the die attach bonder motion of the pick-up and ejection are synchronized to have a good pick up and die placement as well as enabling the bonding tools to achieve acceptable tool life.

Effect of Die Attach Bond Parameter

Bond force, time, and temperature must be evaluated to ensure sufficient die adhesion to the pad and minimal epoxy spread. For



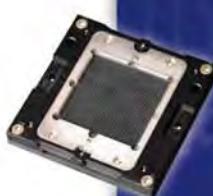
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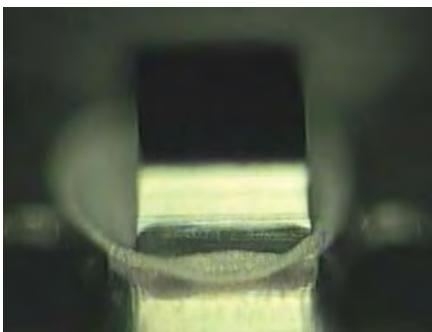


Figure 4. Abnormal epoxy spread

small die size used in this package, it is possible to obtain abnormal epoxy spread as shown in **Figure 4** if the bond parameter is not well optimized.

Compound Selection Study

During the process of identifying a suitable compound type, various compound types data sheets were reviewed carefully. **Table I** depicts the shortlisted compounds based on the critical properties versus the standard compound for the larger & thicker QFN. Additionally, an actual moldability test and c-sam delamination check was performed to identify the best suitable compound type (**Figure 5**). Although compound C gave highest warpage on molded leadframe, it was disqualified after PMC for subsequent moldability tests. Based on the results, we have chosen D to be the molding compound for this package.

Laser Mark

Finding a laser system that can mark character sizes no larger than 0.2mm with the marking alignment of $< 0.05\text{mm}$

	Unit	Std	A	B	C	D
Filler Sieved Size	um	55	45	55	32	30
CTE1	ppm/degC	7	8	9.1	8.8	9
CTE2	ppm/degC	34	43	34.7	30.2	32
Tg	degC	130	150	115	104	135
Flexural Strength	RT	N/mm ²	180	160	130	140
	260degC	N/mm ²	25	23	9	12
Flexural Modulus	RT	N/mm ²	28000	26000	26000	22800
	260degC	N/mm ²	900	900	650	800

Table I. Compound Type Comparisons

throughout a high density leadframe was a challenge. Currently, the smallest character laser mark size is 0.4mm and the highest density leadframe is only half of the density in this new package. Several vendors were reviewed in terms of their respective capability in the marking character size and alignment. A vendor whose buy-off and prototype build showed mark font size as small as 0.147mm and good marking alignment was selected.

leads upon singulation versus regular QFN packages 4mils around the leads. This can lead to poor compound locking or compound drop if the materials and processes are not well taken care of. It is shown from earlier compound studies that compound type is significant to preventing compound drop. Dicing saw optimization on blade type, thickness, and speed are able to provide minimum lead fly-off, compound drop, and offset package. The dicing tool capability also needs to be reviewed or upgraded to cater to a very high-density fine pitch strip-singulation process.

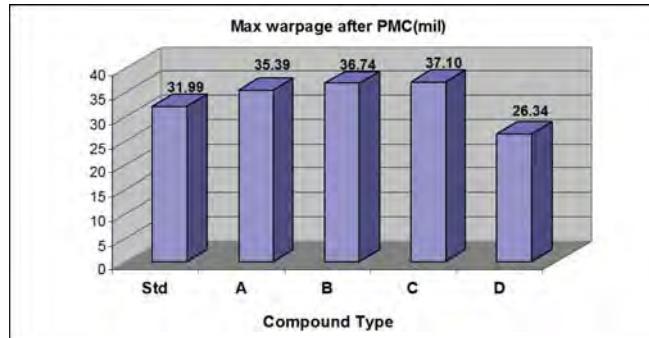


Figure 5. Warpage Comparison for Different Compound Type

Saw Singulation Characterization Study

In the average scenario, there is only about 1.5mil of compound left around the

the dicing process with partial/fully populated molded strip on the saw singulation ring frame was conducted. Both methods provided the final sawn

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Figure 6. Laser mark with font size < 0.15mm in height

products per the Package Outline Drawing (POD). Full strip singulation was selected because it gains higher productivity and lower cost versus single panel singulation.

Offloading Study

Once singulation is completed, units on the dicing tape need to be offloaded into a canister. It is found to be challenging to ensure 100% off-load of the units to the canister from the dicing tape. This could be due to various reasons such as small size, light-weight, static charge, dicing tape properties, and more. Actions evaluated and taken to improve offloading performance included anti-static tape type, ionizer installation and a combination of air and vibration assisted procedures.

Reliability Test Data

Three batches of functional packages were assembled, and subjected to MSL1@260°C reliability testing. No failures were observed during the testing.

Conclusions

A new small package, X3 Thin QFN, of 0201 SMD package-size-compatible diced QFN product has been successfully developed through material and process optimization on similar infrastructures currently used to build the existing QFN packages. In some cases, new developments or capabilities of the assembly equipment is needed to achieve the packaging requirement.

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- 1) JMP Statistical Software / Manual
- 2) Jedec specs
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Die Bonding in a Mobile World

By Steven J. Adamson, James Klocke, Gareth DeSanctis, Alemu Dejene, [Nordson Asymtek]

Packaging has reached its Golden Age. Never in the history of packaging design has the package assembly played such a dynamic role in device performance. Die bonding has advanced from simple dots of epoxy or solder to very thin adhesive films that are applied in exacting dimensions for 3D stacked assemblies.

With over 60% of electronics going into mobile devices, heat sinking for these devices is not typically a challenge. Density is today's engineer's challenge, putting more memory into a package or adding memory to logic devices.

Die are thinner through back grinding to the point where a 300mm wafer is practically transparent after grinding. With die in the 25 to 60 μm thickness range, the glue lines that bond die together must be in the range of 10 to 20 μm thick. Die bonding tapes have been very popular for this application for several years. However, tape comes with a waste factor of at least 25%, which is reflected in its cost. Traditional spin-on methods of applying fluid coatings to wafers can have material losses of up to 80%.

Liquid die bond materials can be applied to wafers with much lower waste factors and hence lower costs. The driver for our work is to develop methods of applying fluids to wafers with much lower waste factors with a target of less than 15%. So far, good quality films in the 10 to 60 μm range have been deposited with minimum edge bead. This article reviews a new process for applying liquid die bond materials to wafers and compare it to tape and screen printing application methods.

Die Bonding History

In the last 30 years die bonding has progressed from gold silicon eutectic bonds through silver glasses and polymer materials. Polymer materials have been available as liquids such as silver epoxies and/or preform epoxies. While preforms have always been an easy simple method of die bonding, they come at a cost premium when compared to using liquid materials.

Liquids or pastes used in die bonding have typically been silver epoxy materials applied by high speed dispensing equipment. This worked fine for many years, but it is difficult to utilize with 3D assemblies. In the last few years, as wire bond die stacking has increased in popularity, the preferred method of applying a die bond material has been tape or film applied materials. These die attach films (DAF) are laminated onto the back of a wafer that has been ground to a desired thickness. This two-layer film is diced through the adhesive layer during wafer dicing without cutting through the carrier layer. The diced adhesive layer is used at the next stage as the die bond adhesive. While this provides a simple clean solution to applying an adhesive, it comes at a price premium compared to liquid materials. The process is called Dice After Grind (DAG). (Figure 1).

Recent Developments in Die Bonding Materials for Stacked Die

A liquid wafer backside coating (WBC) material* has been developed for die bonding stacked die. This is a 100% solids material with no solvent to drive off in the process so is considered a green approach. The material has a viscosity of

about 1000cps and has a UV B-stage cure to provide easy handling after coating. In the die bonding stage, it is heat cured to bond die to substrate or die-to-die. It is a particularly attractive material for use in a process known as Dice Before Grind (DBG). In the DBG process a wafer is diced partially through before back grinding. Back grind (BG) tape is laminated to the active side of the wafer, and the wafer is ground down to a desired thickness. The WBC adhesive is then sprayed onto the back of the wafer. It coats the individual die surfaces, but does not fill or impair the diced streets of the wafer. An inexpensive carrier tape on a wafer frame is laminated over the WBC film and the BG tape removed. There are much lower chipping levels with the DBG process when compared to the DAG process. This is a result of the grinding process removing silicon from the back of the wafer until the slots that were diced in the wafer prior to grinding are opened. Because the adhesive is applied with a spray, the sharp edges of each die are protected with a small amount of adhesive. In addition, there are no small flaps of adhesive materials left at the edges of die that can interfere with die alignment (Figure 2).

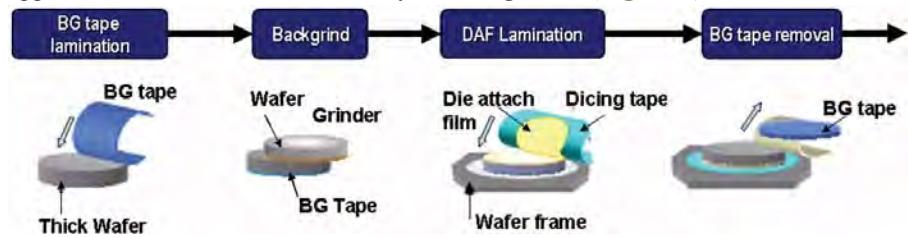


Figure 1. Typical Process for back grinding a wafer and applying DAF tape



Figure 2. Process flow for Spin/Spray application of die attach adhesive

Print, Spin or Spray Application Methods for Die Bonding Coatings

Early WBC coatings were applied by screen printing. This worked well when wafers were of the order of 75 to 100 μm thickness after grinding. Since wafers are now much thinner, the current feeling is that screen printing is a contact method and this can cause wafers to crack when the pressure from the squeegee is applied to the fluid and the wafer.

Spin coating is a standard process used in applying photoresist to wafers. Exceptionally thin films of materials can be formed on a wafer surface with great uniformity across a wafer. The fluids tend to be low-viscosity, solvent-filled materials. The concern is that a large percent of the fluid evaporates into the surrounding atmosphere. Government agencies are now regulating use of these materials. In addition, spin-coating is extremely inefficient, with approximately 48% of the material being spun off a 200mm wafer and around 75% waste on a 300mm wafer. Plus, the physical dynamics of wafer spin coating often leaves a rim of the material at the edge of a wafer.

Spray coating wafers has many advantages over screen printing and spin coating. There is no contact with the wafer, thus it eliminates cracking. The spray can be applied to the wafer with less than 18% loss of fluid, which is much more efficient than spin coating, and because the spray pattern can be tailored to the position on the wafer, edge bead can be minimized.

Spray Equipment Currently in Production Environment

Spray equipment** has been developed to handle these fluids for the WBC process. At 1000cps, it is one of the thicker sprayable fluids, but spraying has been done on thicker materials with a viscosity of 4000cps and higher. However, the requirement to have thin coatings in the 10 to 20 μm range is somewhat more challenging. Also, the uniformity across a 300mm wafer has to be within +/- 10%.

This spray tool has been sold for many years to put down films of anywhere from 5 μm thickness or greater with good uniformity. The new challenge was to

develop a spray pattern that would give good uniformity across a 300mm wafer. This was achieved using an arcing spray head motion across the wafer as the wafer is rotated to create micro overlapping coated areas (**Figure 3**).

Uniformity of the coated films on 300mm wafer using the above coating method is excellent. As seen in **Figure 4**,

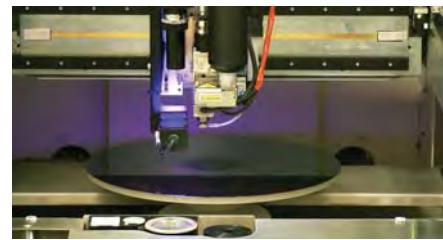


Figure 3. DJ-2200 Spray moving across the wafer in an arc pattern

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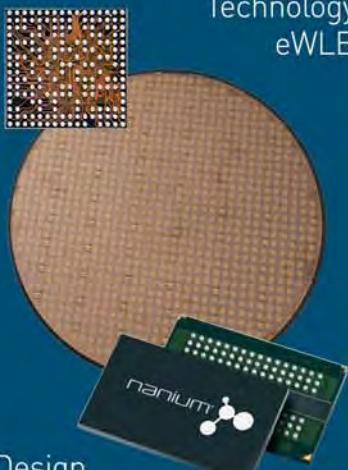
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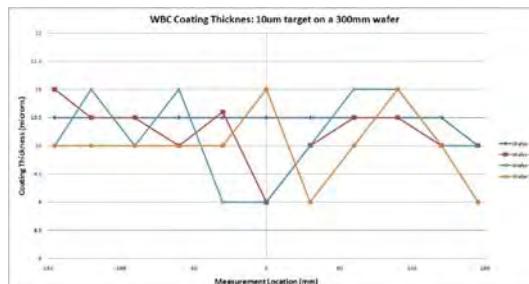


Figure 4. Thickness results from four 10 micron wafer coatings with 10μm films the uniformity meets the +/- 10% thickness specification.

The edge bead problem was resolved by a combination of edge coating pattern and spin speed to allow fluid to flow across the wafer, but not push the fluid to the edge, where surface tension forces can cause a bead to develop. This operation is a carefully balanced procedure to get coating to the edge and at the same time not to spray significant amounts of fluid over the edge of the wafer as waste. **Figure 5** shows the edge bead for a 20μm coating on a 200mm wafer. There is no edge bead for a 10μm coating.

Following wafer coating, the film has to be B-staged to allow for handling. UV lights usually give off large amounts of heat. Because the WBC film will be heat bonded in the die bonding process it is important to keep the film cool, below 50°C, until the die bond stage. To reduce heat at the UV B-stage, a Xenon light source was used for this part of the coating process. This type of lamp still has significant cooling requirements, but the on-time can be controlled to very exacting limits and, if required, can be used in a pulse mode so is a much cooler light source when compared to other UV sources.

In any operation where thin wafers are handled or transported between stations, the cost of these handling systems can be greater than the cost of the fluid application equipment. This is true if using spray coating equipment, screen printing, or applying tape to wafers. The dispensing equipment referenced in this article has built-in handlers that use a simple track system to move not only the wafer but also the wafer chuck. Once a wafer is loaded

onto the wafer chuck it is not released until the film has been UV cured and returned to the load station. The timing of the whole operation is set up to match the output of the wafer grinding system. The system in **figure 6** shows a manual loading system, coating area, and UV cure station. There are automated shutters between the UV station and the rest of the system to avoid curing at the coating stage. The system has been designed to interface with back grinder systems for fully automated operations. The current system design returns the cured wafer back to the load area, but could be easily adapted to allow pick up of the wafer at the UV module.



Figure 6. This systems shows a manual loading system, coating area, and UV cure station

Summary

Simple dispensing of silver epoxy material cannot meet the stringent requirements for 3D assemblies. Traditional methods of applying adhesive layers have been shown to have deficiencies, namely contact to thin wafers and price. It has been shown that liquid adhesives sprayed in a controlled process can achieve the goal of good quality thin adhesive films and at a significant cost reduction to a standard film or tape process. Now that these wafer backside coating systems are being deployed in production environments significant cost savings can be realized.

*WBC-8901UV, by The Henkel Corporation, Irvine, CA

** Nordson ASYMTEK DJ-2020 flux spray was selected by Henkel to spray its WBC material.

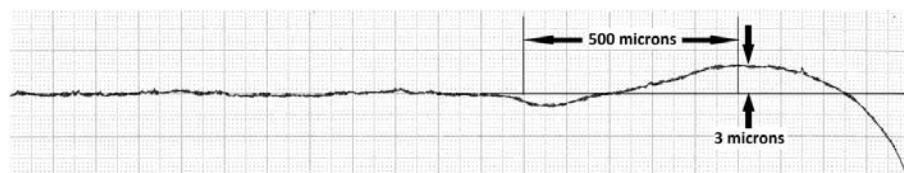


Figure 5. Edge bead for a 20 μm coating on a 200mm wafer

Integrated Circuits (ICs) Out Pacing the Economy

By Sandra Winkler [New Venture Research]

With consumers demanding handheld electronics such as smart phones and tablets, the semiconductor industry rebound that began in the second half of 2009 turned into a boom in 2010. Auto sales also improved, in part due to stimulus packages in several nations. Sales of integrated circuits (ICs) experienced a robust 28.9% growth in units in 2010 over 2009, totalling 41,768 million units. Thus, sales of ICs were 186,398M in 2010. Revenue growth was an even healthier 31.3% between 2009 and 2010, or a growth of \$59,567M over 2009 to \$249,909M in 2010.

The outsourced assembly market rebounded similarly. After a -0.6% revenue decline in 2008 and -15.8% in 2009, revenue experienced a whopping 33.8% growth rate in 2010, to more than \$13B in package assembly revenue. (These figures are for assembly only, not test or other sources of revenue.)

Outsourced units experienced a similar pattern. After falling -1.2% in 2008 and -11.9% in 2009, the contract or outsourced assembly market exploded 30.8% in 2010, to more than 54B units assembled. The contract IC package assemblers captured 28.7% of the packaged units in 2009, which grew to 29.1% in 2010; its usual uphill climb. Contractors have gathered more of the package, assembly, and test business annually from both fabless and fab businesses alike.

Top OSATS Evaluated

The top ten outsourced IC package assemblers differ whether you refer to units or revenue. When referring to outsourced IC package assembly exclusively, the top ten producers in terms of revenue are:

1. ASE, Inc.
2. Amkor Technology, Inc.
3. Siliconware Precision Industries Co., Ltd. (SPIL)
4. STATS ChipPAC, Ltd.
5. PowerTech Technology Inc.
6. Signetics

7. United Test and Assembly Center (UTAC), Ltd.
8. Unisem Group
9. Carsem
10. Orient Semiconductor Electronics (OSE)

Since the package mix differs company by company, some making their profits on the multitude of smaller packages that require assembly, ordering by units, provides a different picture. The grouping by IC package assembly units is:

1. Amkor Technology, Inc.
2. Carsem
3. ASE, Inc.
4. Lingsen Precision Industries, Inc.
5. SPIL
6. UTAC
7. PowerTech Technology Inc.
8. Tianshui Huatian Technology Co., Ltd.
9. Orient Semiconductor Electronics (OSE)
10. Unisem Group

The most successful outsourced IC package assembly companies offer a diverse array of package options that match the overall proportions of the IC packages being assembled worldwide. While DIPs are neither elegant nor profitable to assemble, there is still a market for these hand-inserted packages and contractors will often assemble them at cost in exchange for obtaining other, more profitable, package assembly business.

FBGAs, BGAs, stacked packages, and SiP solutions are more complex and thus offer higher levels of revenue per unit. SOs and TSOPs are smaller, established leadframe packages that offer higher volumes and thus turn a profit out of sheer volumes. Quad flatpack no-lead (QFN) and DFNs are newer to the market and offer an even smaller footprint to the board. QFNs are able to extend lead counts to higher levels by coming in multiple rows of leads of two or three rows, in a perimeter array pattern. This extends its reach into a broader range of I/O counts, pulling at the bottom of the chip carrier and QFP markets. Wafer level packages (WLPs)

are doing the same thing with its overmolded package by extending the surface available for land pads.

ASE was once behind Amkor in terms of revenue, but toppled the leader a few years ago. While offering a mix of all IC package types, they focus heavily on FBGAs and multichip options, such as stacked packages. Bumping for flip chip and final test are also offered through ASE. The company's vertical integration includes design services and substrate manufacturing for its array packages.

Amkor Technologies, for years the leader in both units and revenue, is now in second place in revenue. They also offer a broad portfolio of packages and are pioneers in new package development. Wafer bumping for flip chip and final test are among its breath of services.

SPIL also offers a wide range of both leaded and substrate-based packages. Its turnkey solutions include design consultations, modeling and simulations, wafer bumping, wafer probe and sort, package assembly, final test, burn-in, and drop shipment.

STATS ChipPAC is a merger of STATS, predominately focused on final test, and ChipPAC, a package assembly outfit that spun out of Hyundai. The company has been heavily focused on stacked packages assembly, and more recently flip chip packages after bringing bumping in-house. It's latest package technology being developed is the fcCuBE™, an advanced flip chip packaging technology that features copper (Cu) column bumps, bond-on-lead (BOL) interconnection and enhanced assembly processes.

PowerTech Technologies offers a number of FBGA packages in both single chip and stacked package options. The company also offers TSOP and QFN package solutions, but not the variety of package solutions offered by the other top ranking companies. Services include IC chip probing, packaging, final testing, and burn in to end products. They recently

announced a collaboration with UMC and Elpida to develop 3D integration processes for DRAM and wide I/O DRAM on logic.

Signetics began semiconductor assembly and test operations in Korea in 1966 as part of Signetics Corporation, based in Sunnyvale, California. It was acquired by Philips Semiconductor in 1975, and became an independent subcontract service provider in 1995. Today, Signetics is a subsidiary of Young Poong Corporation.

UTAC provides test and assembly services for a wide range of semiconductor devices that include memory, mixed signal/RF, analog, and logic integrated circuits. UTAC offers full turnkey services that include wafer sort/laser repair, assembly, test, burn-in, mark-scan-pack, and drop shipment, as well as value-added services such as package design and simulation, test solutions development and device characterization, failure analysis, and full reliability test.

Unisem offers an integrated suite of packaging and test services such as wafer bumping, wafer probing, and wafer grinding, a wide range of leadframe and substrate IC packaging, including leaded, QFN, BGA, and flip chip packages, and high-end RF and mixed signal test services. The company's turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization. A majority of Unisem's business is leadframe packages such as SOs, QFNs, QFNs, and TSOPs.

Carsem comes in number 2 in units, but 9th in revenue. It specializes in very small package form factors. They also offer a full range of turnkey test services for RF, mixed-signal, analog, digital and power devices. Carsem also offers system-in-package (SiP) and flip chip on leadframe FCOL™ process technology for various package types.

Orient Semiconductor Electronics

(OSE) predominately assembles leadframe packages. The company provides IC packaging and testing services and Electronics Manufacturing Services (EMS/CEM).

Lingsen Precision Industries, Ltd. (LPI) was founded in 1970 to be the captive assembler for a joint venture between Mitsubishi Electric Corp. and Dahsen Electronic Industries, Ltd. in Taipei, Taiwan. In 1973, Lingsen Precision Industries, Ltd. was reorganized as a wholly owned and independent contract assembly company. The company was moved to the Taichung Export Processing Zone (T.E.P.Z.) in Taichung, Taiwan. The company offers a wide array of packages, mostly leadframe based.

Tianshui Huatian Technology Co., Ltd. assembles primarily DIP and SO packages. The company was chosen as one of the top ten fastest growing packaging and testing corporations in China in 2004.

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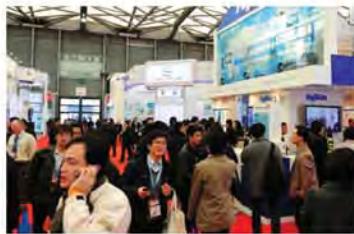
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Powertech's Eye on the Prize

Chip Scale Review Staff



Headquartered in Taiwan, Powertech Technology Inc (PTI) ranks number five overall for major OSATS and number one for OSATS in the memory market (**Figure 1**). So why is it we hardly ever hear about them? Easy, they've been keeping a fairly low profile for the past few years. But this young company, established in 1997, is ready to make its move, investing in next-generation 3D packaging and expanding its presence in the US. Chip Scale Review met with Scott Jewler, President, PTI - USA, to talk more about the company's latest endeavors and strategies to become the number 3 OSAT overall.



Figure 1. PTI Headquarters

CSR: How did PTI come to own such a significant portion of the memory market share?

Jewler: PTI's roots were originally in Powerchip Technology's assembly and test. The company was spun out in 1997 and in 2001, DK Tsai was named as PTI chairman and CEO. He came out of Kingston Technology, the largest memory module manufacturer in the world where he was responsible for worldwide operations. PTI became a publically traded company in Taiwan in 2003 and now handles assembly and test operations for leading memory makers such as Toshiba and Elpida, who count Kingston among their customers. Over the last five years, PTI's memory assembly and test business has exploded; achieving over 30% CAGR.

CSR: Considering the downturn and the overcapacity in the memory market during part of that time, that's a pretty impressive number. Can you explain a little about the reasons for PTI's success at that time?

Jewler: PTI has developed some the most efficient assembly and test operations in the world. We weren't unaffected by the downturn; 2008 was basically a flat year for us. But memory and logic fabs tend to operate differently. Memory fabs produce to capacity while logic fabs produce to demand. While there was some average selling price (ASP) erosion that affected revenue, in terms of units sold we actually grew in '09. That's how we withstood the downturn better than some other packaging houses.

CSR: What's been your technology focus?

Jewler: From a technical standpoint, our focus has been on wire bond, some flip chip and system-in-package (SiP) with a heavy emphasis on wire bond die stacking (**Figure 2**). We're quite competitive in the



Figure 2. PTI's Assembly floor

world, especially in the NAND flash area. We ship 8-9 die stacks in high volume (**Figure 3**). What's critical here is yield.

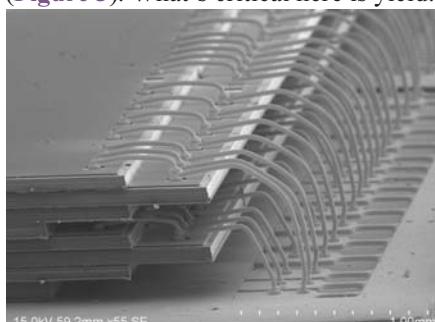


Figure 3. NAND Flash 8 die wire bonded stack

Our strength has been in wafer-level burn in and sorting for known good die (KGD) through our JV company TeraPower, extremely tight assembly process control and memory testing (**Figure 4**). Our focus for the past



Figure 4. DRAM Test line

five years has been mainly on die thinning and stacking technologies to achieve high yield products. We're shipping volume production of 40µm thickness products. **CSR:** You mentioned that up until recently, PTI hasn't had much of a presence in the US. Can you explain why?

Jewler: PTI is a very manufacturing and engineering oriented company. We haven't had a presence in the US because we were running full speed to support growth from our existing customers. Up until now, thanks to direct interaction with customers, we've grown by word of mouth. DK Tsai has the company set up to be extremely efficient, using the best infrastructure. We have about 6000 employees, and generated about 1.2B\$ in revenue in 2010; that's the highest revenue per employee in the industry. Our lines, operator efficiency, the way the factories run — people are amazed at how good PTI is.

CSR: PTI recently announced a collaboration agreement with UMC and Elpida to develop TSV and die stacking technologies. What's that all about?

Jewler: We believe homogeneous stacks

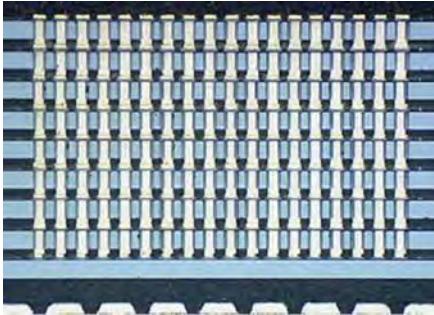


Figure 5. DRAM Stack with TSVs

of DRAM (**Figure 5**) are going to be early adopters of TSV technology, with memory and logic stacks to follow. In this collaboration, we believe we've established a highly innovative model. Partnering with memory maker, Elpida, will enable PTI to be in volume production early while other OSATS are waiting for logic to be involved. By bringing UMC into it, we'll have a structure that already supports logic + memory applications. This way, we're well positioned to scale for pure DRAM stacks and will be able to deploy technology for logic + memory. *CSR: What strategy is PTI employing in preparing for next-gen technologies? For example, what sorts of capex investments are planned?*

Jewler: We're investing in a dedicated 300mm pilot production line (plating, lithography, deposition, cleaning, stacking, etc.) now with capabilities that are cumulative to build up to TSV (**Figure 6**). We'll be able to support 300mm copper pillar bumping, WLCSP, and RDL for both TSV and other applications. We're focused on chip-to-chip (C2C) stacking because that's what Elpida's TSV DRAM process calls for. We don't intend to get into traditional C4 bumping; there's not much need for a new entrant to support this mature technology. Our focus is being prepared for next-generation technologies. For example, when high speed DRAM goes to flip chip,



Figure 6. Tokyo Electron Coater

we'll start right with copper. We're targeting high efficiency high volume the middle-of-line processes; the gap in tools between front-end process and wafer bumping. *CSR: Where will this line be located? When do you expect it to be ramping to production?* Jewler: We are installing our pilot line now for TSV that can handle 10,000 wafers per month in terms of space capacity. This facility is in our Hsinchu Science Park facility. We also intend to break ground on a new factory next to our Hukou headquarters building in March of this year. The plan is to optimize the first two floors of this approximately 500,000 sq ft. building with middle-of-the-line technology to handle next-generation technologies (**Figure 7**). Our 2011 capex plan is 300M with about a third of this going towards next generation technologies. We



Figure 7. MTI Building, site of future 3D assembly expansion

believe that's significantly more than anyone else is doing. We're basically in the mode of executing as fast as possible. We're not relying on existing resources. We're hiring people who are highly experienced in wafer bumping and fab BEOL processes. We believe we'll be the leading OSAT coming out of this for next generation, high-volume memory stacks. We'll leverage that to go to volume in logic + memory.

CSR: What would you say are the biggest challenges the industry is facing in transitioning to 3D integration?

Jewler: Specifically with regard to heterogeneous 3D stacking, the business model solutions in place aren't ideal. The market is looking for the deployment of TSV to enable wider I/O bus communications between logic and memory chips. Performance gains from faster and more parallel processors and denser and higher speed memories are not enough. The technology

of interconnect between devices also needs to move ahead to enable performance. There's a lot of focus on the technology solution but it's also a supply chain challenge: Who buys what from whom to create this integrated memory/logic TSV wide I/O solution. System makers want to buy an integrated solution. Logic companies are doing that for lower density stacks, but it's difficult for them to mark up memory. That's one of the reasons that inspired package-on-package (POP) adoption. In some ways it was a technical solution to a commercial problem. We have to solve the business model problem to enable wide adoption of TSV of heterogeneous devices. *CSR: With regard to these supply chain challenges, how is PTI positioned to handle them?*

Jewler: PTI is in a unique situation. We're partnered with Kingston, the largest semiconductor memory distribution company in the world. We're not constrained by 30 years of packaging business process history. We're open to progressive models, and our business model is in a good position to create solutions to that commercial problem. We're focusing a lot on that in cooperation with our partners. Our strategy is to come up with something attractive to others in the supply chain and pull together resources to come up with a commercial model that works for everybody. We see 2011 as a transitional year for us. In the future we'll be competing with the next-generation of interconnect technology technologies for business at leading semiconductor companies around the world.

CSR: Does PTI have any plans to increase your visibility outside of your traditional markets?

Jewler: We certainly hope to do so. We recently joined SEMI and plan to participate in SEMI Taiwan's 3D packaging forum. We also had several papers accepted into ECTC this year and will be sharing more details about our activity during this conference in booth 310. We are on the web at wwwpti.com.tw and I can be reached at scottjewler@powertech-usa.com. 2011 is going to be an interesting year in the industry and a very exciting one for PTI.

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INDUSTRY NEWS

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BiTS Featured Speakers Enlighten Burn-in and Test Community

By Francoise von Trapp, contributing editor

From the glorious weather and fabulous fare, to the increased number of participants (~350) and a sold-out exhibition, BiTS Workshop 2011 reflected the optimistic attitude that seems to be touching all segments of the semiconductor market as forecasts for continued growth ignite industry-wide enthusiasm.

In addition to a robust technology program of 26 papers and 6 posters and lots of new innovation being showcased on the EXPO floor, four featured speakers enlightened attendees about other areas of the market that their technologies serve. Opening up the event on Sunday evening was Al Crouch, Chief Technologist, Core Instruments at ASSET InterTech, who explained his concerns that ultimately the cost of test, if not handled properly, could kill 3D TSV integration. Luckily it's not too late, if awareness is raised and the proper steps are taken with developing test methodologies.

One important take-away for the test and burn-in community to consider is that with the adoption of 3D TSVs, the PCB world will have to start paying attention to Moore's law, just like the rest of us. In the past, board pin-out didn't change along with the functionality of the package being mounted on it. But with 3D, there are whole systems of logic on each of those stackable die and each of those die have tons of test and debug requirements that will require test from the inside out rather than outside in.



At the BiTS Poster Session, attendees and authors interact directly



Test Tooling Solutions Group showed their products and services at the BiTS EXPO

Board testers will need to test that the devices are communicating with each other as well as performing their functions.

In his Keynote Address on Monday, Roger Schmidt, IBM Fellow and Chief Engineer - Data Center Energy Efficiency drew some interesting parallel trends between the test and burn-in world and the challenges of thermal management in an age where energy use has skyrocketed due to all the data transfer generated by internet usage. For example, there is an increased emphasis on energy efficiency of Test and Burn-In equipment, as well as power delivery, thermal management and utilization rates. There's also an emerging trend of green initiatives and marketing from test equipment vendors. Increasing power density in silicon and packaging, as well as the trend towards fewer components of higher complexity and computing capability are having an impact on trends for both test and burn-in and data centers. Low-power silicon technologies and power/performance trade-offs are also affecting both, and managing heat from the die level through the package level all the way to the data center environment is impacting both test and burn-in and data center energy efficiency.

Brandon Prior, Senior Consultant, Prismark Partners, returned for a follow-up to last year's Market Update to brief the test and burn-in community on IC Package Miniaturization and System in Package (SIP) Trends. Prior talked about



The Multitest team exhibited a wide variety of products at the BiTS EXPO

the transition to 0.4mm pitch package and beyond, forecasting 20% of FBGA/WLCSP to be 0.4mm or less pitch by 2015. However, challenges remain with PCB routing and assembly yield/process/materials at 0.3mm pitch and below.

In addition to fine-pitch array packages, other trends enabling miniaturization include stacked-die memory, and logic/memory package on package (PoP) stacks, and wafer level CSP (WLCSPs). Prior also discussed developing technologies for TSVs and silicon interposers, that he predicted will reach volume manufacturing in the next 8-12 months, and echoing Crouch, said this could pose some major challenges with die level test at pitches <80µm. Test before die-to-die and die-to-wafer stacking will likely be required.

Fred Taber wrapped up the featured speaker talks with a summary of the Socket Marketplace based on data reports from Fleck Research. He said that the world wide socket market has recovered from a drastic 16.6% drop in 2008/09 to a forecasted 53% five year growth rate. The survey included 83 socket companies, representing 82.3% of the test and burn-in socket market revenue.

For further review of this year's BiTS Workshop, visit the organization's website at www.bitsworkshop.org to view video interviews of the featured speakers. The 2012 BiTS Workshop is scheduled to take place from March 4-7, 2012. Hope to see you there.

WHAT'S NEW!

Jet Dispensing for Side View LEDs

At SEMICON China, Nordson Asymtek introduced jet dispensing for manufacturing side-view LEDs, which are used to illuminate displays in devices such as tablet computers, smart phones, and e-readers. The slimmer the LED, the greater the challenge to dispense specialized fluids like silicone phosphor into these tight spaces. ASYMTEK's Spectrum™ S-920N jetting system reportedly jets 0.1 to 0.2mm dots through windows as small as 0.4mm into the LED cavities. It automatically maintains a consistent shot weight with software-managed dispense parameters. Closed-loop



dispensing eliminates the need for time-consuming operator adjustment.

Unlike needle dispense systems, this jet dispense provides non-contact dispensing. It retracts much less for silicone break off and therefore shoots multiple shots faster, increasing speed and throughput. The jet's small, controlled drops of fluid reach tight cavities consistently and reliably, unlike needles which have orifices larger than the cavity windows of side-view LEDs. [\[www.asymtek.com\]](http://www.asymtek.com)

Pick-and-Place Handler offers Improved Production Flow

Test handler manufacturer, Multitest, went to the drawing board to come up with a handler that offers improved jam rates and an optimized production flow. The result is the MT2168, a true all-in-one platform. The company claims it has the best jam rate statistics and has proven high production performance in the field.



The design concept of the MT2168 is optimized for five handling steps, rather than the 10 steps required by traditional pick-and-place handlers. The result is a non-complex architecture for improved material flow. The tool's novel design is said to be an advantage to high-volume production sites as well as sites dealing with small slots and frequent package changes. MT2168 conversion kits are less comprehensive and more cost-efficient. Additionally, kit prices are low and the kit exchange is fast and easy. [\[www.multitest.com\]](http://www.multitest.com)

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High Performance WLCSP Socket

The SG-BGA-7203 socket from Ironwood Electronics was designed to test two different WLCSPs side-by-side in a single socket side while operating at bandwidths up to 10 GHz with less than 1dB of insertion loss. This high performance WLCSP socket is intended to accommodate a 0.5mm pitch 40 ball WLCSP and 0.4mm pitch 30

ball WLCSP in the same socket. The contact resistance is typically 20 milliohms per I/O. Reportedly using the smallest footprint in the industry, the socket connects all pins with 10 GHz bandwidth on all connections and is mounted using supplied hardware on the target PCB with no soldering. It also incorporates a novel quick insertion method using shoulder screws and swivel socket lid so that IC's can be changed out quickly. [\[www.ironwoodelectronics.com\]](http://www.ironwoodelectronics.com)

Virtual Fabrication Software

SEmulator3D® 2011 from Coventor is the latest version of its virtual fabrication software for semiconductor and MEMS process development organizations. The new release reportedly provides a three-fold performance boost in model building time and new robust 3D mesh generation capabilities that create silicon-accurate meshes for physics-based simulations used to optimize the performance and manufacturability of semiconductor and MEMS devices. It comes with the first release of SEMulator3D Reader, a downloadable interactive 3D model viewer that streamlines communications among process development team members and with suppliers and customers.

The company claims that SEMulator3D 2011 is more than three times faster for a 25nm flash memory application. It detects incremental changes to the process description and automatically re-builds only subsequent process steps, saving on average 50% or more in model development time. [\[www.coventor.com\]](http://www.coventor.com)

Enhanced Flip Chip Packaging

fcCuBE™ technology from STATS ChipPAC is an advanced flip chip packaging technology that features copper (Cu) column bumps, Bond-on-Lead (BOL) interconnection and enhanced assembly processes to deliver high input/output (I/O) density, high performance and superior reliability in advanced silicon nodes. It addresses a complex set of current packaging challenges and is said to deliver such benefits as ultra high I/O escape routing density, scalability to very fine bump pitches of 80 μ m and below with finer effective pitches, significant and proven stress reduction on Ultra low-k (ELK/



ULK) down to 45/40 nm and 28nm silicon structures, broad fab node compatibility, higher resistance to electromigration, and

is a lead-free alternative to conventional lead-free bumps and solder-based bumps. [\[www.statschippac.com\]](http://www.statschippac.com)

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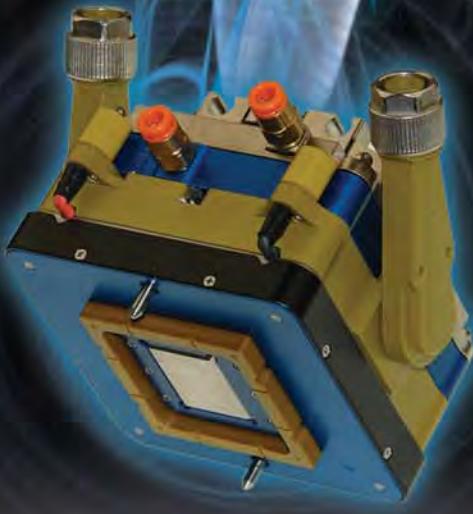
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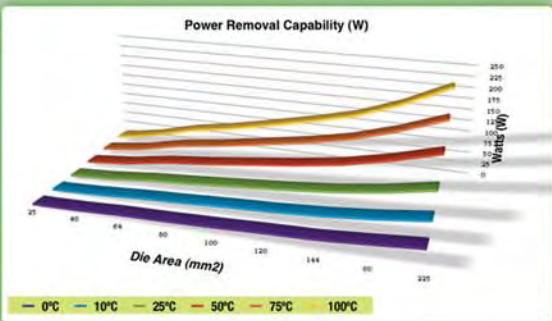
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