

# Chip Scale

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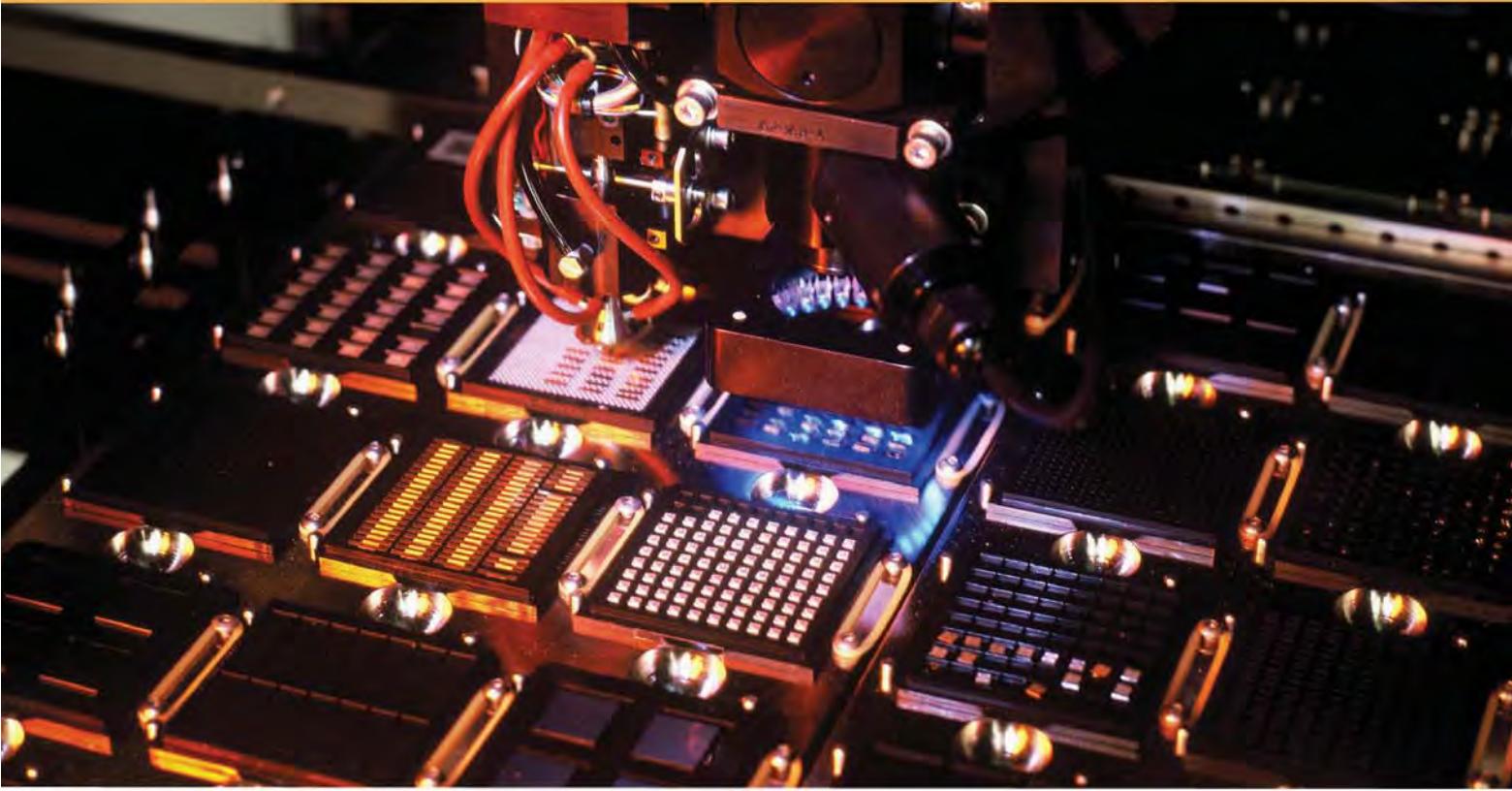
REVIEW®

Volume 14, Number 4

July-August 2010



- State-of-the-Art Thin Wafer Processing
- Solder Paste Properties for Die-attach Processes
- Ga Tech's Vision for Ultra-miniaturized Packaging
- Combined Clean Rooms Creates Efficiency
- International Directories:
  - Automated Encapsulation Systems
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July-August 2010

Volume 14, Number 4



Photograph Courtesy: EV Group Europe & Asia/Pacific GmbH. Thin wafer processing is a key enabling technology for TSV's and 3D interconnects. By adding only 2 process steps, temporary bonding and debonding, every existing fab can be upgraded for thin wafer handling capability. In the picture a process engineer in EV Group's application lab inspects a 50µm thin 300mm wafer on a film frame.

## Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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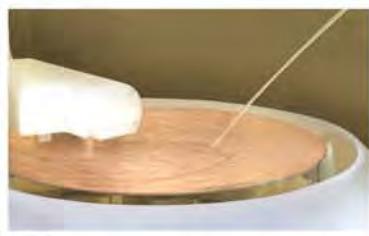
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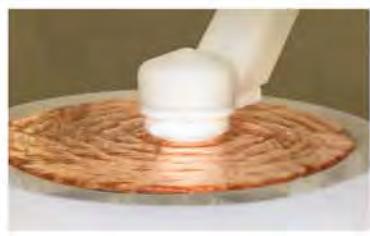


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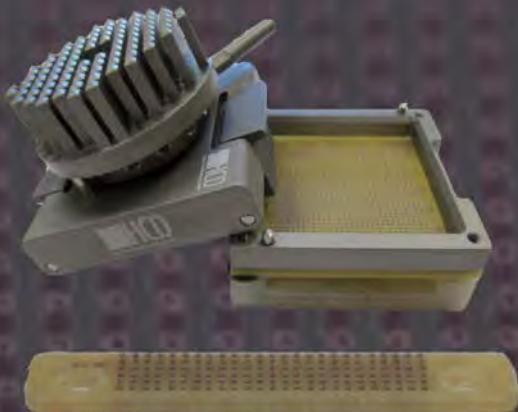


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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$85 per year to Canada or \$95 per year to other countries. In the U.S. subscriptions by first class mail are \$75 per year.

*Chip Scale Review*, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to *Chip Scale Review* magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

# FROM THE PUBLISHER



## Business . . . . . The Fair Exchange of Values!

By Kim Newman

**T**

here continue to be interesting discussions and articles that have helped me to better understand the electronics industry and business in general. One of these discussions, with basis in a recent article, centered around the quote, "Business ... The Fair Exchange of Values." As I prepared to Google the recent article and 100 year old subject matter for the exact quote, it occurred to me that the verbage "Value" (ie. Price) and "Values" (ie. Morals or Ethics) each play an important role in business success. The global supply chains of businesses, and internet access to information, require that pricing models be competitive based on technology and that these same companies do business ethically and professionally!

Following the significant business challenges in 2009, the majority of companies are now into positive 2010 business upturns. Corporate management and staff can typically outline important business negotiations and key relationships, which allowed companies to position for forecasted and eventual 2010 actual increases. The economic conditions of 2009 exposed both the good and bad (strengths and weaknesses) of companies and the relationships with their customers and/or suppliers. It was an economy that did not "make room for everyone" and serious decisions, heavily based on Value and Values, impacted the ability of many companies to make the necessary financial and strategic adjustments in the short term to position for long term success.

Speaking from a standpoint of direct experience, there is absolutely no question that 2009 was a simple matter of survival for many companies including *Chip Scale Review* magazine, which led to many significant changes within the entire CSR organization. These fundamental changes strengthened the foundation of this publication in 2009, while maintaining the consistent position as the leader in packaging and test publications. There is also absolutely no question that this restructuring would not have been possible without the support of our entire staff, editorial writers, advisory board members and loyal readers and advertisers repeatedly emphasizing that *Chip Scale Review* continues to provide a "valuable service and information" to this global industry.

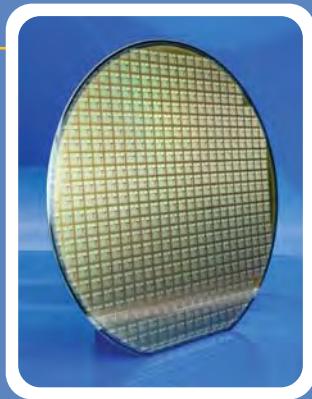
CSR was a media sponsor and exhibitor at the successful ECTC 2010 in June (see the articles in this issue, being distributed at the SEMICON West 2010). Additionally, CSR was an exhibitor & designated "Official Media Sponsor" at the BiTS Workshop conference earlier this year. During several discussions, I did realize that my main responsibility in a "Fair Exchange" of Value / Values, is to manage this publication for continued success, as it is the vehicle allowing technologists to provide information, marketing staffs to promote their products and organizations, to publicize upcoming events. *Chip Scale Review* appreciates your support and the opportunity to be taking part in the current industry momentum. I look forward to seeing you at SEMICON West and the International Wafer Level Packaging Conference (IW LPC) in October as our staff and I are interested in your feedback on this issue as well as your inputs in preparation of upcoming issues for 2010.

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# EDITOR'S OUTLOOK



## Imagine . . .

By Ron Edgar [redgar@chipscalereview.com](mailto:redgar@chipscalereview.com)

**I**magination is the lubricant of research. While scientists, engineers, and technicians can measure, document, and compare, the real breakthroughs are the result of imagination. Where would the genius of Stephen Hawking or Albert Einstein have been without imagination? Astronomy and Theoretical Physics would have been the poorer. For the most part, we all have access to the facts. It is what we do with them that makes us successful or not. The ability to imagine new combinations of the facts, or to imagine something completely new, marks the way forward.

In the Chip Scale arena, there is no lack of ideas. Recent research by Semiconductor Research Corporation (SRC) and Columbia University is providing insight into how electronics fail. As interconnecting wires became smaller, the SiO<sub>2</sub> used for insulation resulted in a slowing of the circuit and, in some cases, excessive power consumption. Replacing this with low-k dielectrics (LKD) seemed to solve the power and performance issues but, unexpectedly, shortened life spans. New ideas to understand the reasons were required. Research focused on optical and electrical studies of charge transport and trapping in LKDs. By using optical excitation techniques, researchers are able to determine electron barrier heights, trap levels and trap densities in LKD and the interfaces between other materials. "These data will help meet an industry-wide need to understand conduction mechanisms in low-k films, particularly those leading to leakage, time dependent dielectric breakdown (TDDB) and reliability concerns," said Dr. Scott List, director of Interconnect and Packaging Sciences at

SRC. "The problems associated with traps in LKD films are expected to increase in importance as the push to even smaller circuitry and lower dielectric constants continue, and these measurements provide us the best insight available to help solve these problems." The work continues.

All sorts of astonishing ideas flow from the hallowed halls of the Massachusetts Institute of Technology (MIT). But self-assembling computer chips? This idea sounds too good to be true. The thrust is this; the processes used for making chips have scarcely changed in 50 years. As features get smaller, now smaller than the wavelength of the light used to make them, the process is out of steam. Its replacement, electron-beam lithography, is significantly slower and more expensive than its predecessors. The MIT approach is to use electron-beam lithography to create tiny posts on a silicon chip. They then deposit specially designed copolymers on the chip. The copolymers spontaneously 'hitch up' to the posts and, by using a copolymer, the joined polymers arrange themselves into predictable patterns. This approach greatly reduces the need for electron-beam lithography. The research is a long way from producing viable chips, but the work holds promise of greatly reduced feature size.

Rao Tumalla and his teams at Georgia Technology have been doing a lot of imagining recently. This edition's article, *Georgia Tech's Vision for Ultra-miniaturized Device and Systems Packaging*, is a must-read article. Matthias, Kim, Burgstaller, Wimplinger, and Lindner of EVG review *State-of-the-art Thin Wafer Processing*. They address many of the key issues including

handling, tracking, measuring, carriers, adhesives, and debonding. The advantages of having a facility that combines a wafer fab clean room with assembly and test clean rooms may not be immediately obvious. TI thought it a good idea and went ahead with their Clark project in the Philippines. The article *Combining Fab and Assembly/Test Clean Rooms for Environmental and Operational Efficiency* is a retrospective on the project and serves as a case study. Well worth the read. AZ Tech Direct, LLC, has again prepared two directories for us, *Directory of Adhesives and Epoxy Suppliers* and *Directory of Encapsulation Systems*. This continues our series of directories which we hope provides you with useful references.

Our contributing editor, Françoise von Trapp, an expert follower of 3D technology, takes a look at the increasing momentum of 3D technology and concludes there *Ain't no stopping it now . . .* We have our usual sections on *Industry News* and *What's New*, with the latest announcements and new products.

International Wafer-level Packaging Conference, IW LPC, sponsored jointly by SMTA and CSR, is pleased to announce its fourth Gold Sponsor, EVG. They join Amkor, PacTech, and Nexx as major conference supporters. If you are interested, IW LPC is looking for Wi-Fi and Reception sponsors. The conference will be held October 11-14, 2010, in Santa Clara, CA, USA.

Keeping your mind stimulated is the best way of keeping your imagination sharp. We hope we offer you the information to do just that. That brilliant new idea may just be enough to make you the market leader — I hope so! ☺

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# INDUSTRY NEWS

## ECTC 2010 Expands and Focuses on 3D Packaging

By Ron Molnar, AZ Tech Direct, LLC, [r.molnar@aztechdirect.com](mailto:r.molnar@aztechdirect.com)



**J**ointly sponsored by IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and the Electronic Components Association (ECA), the 2010 Electronic Components and Technology Conference (ECTC) celebrated its 60<sup>th</sup> anniversary in grand style at the Paris Las Vegas Hotel from June 1 - 4, 2010. It's considered by many to be the premier international conference on packaging, components, and microelectronics systems technology.

This year the event consisted of 36 technical sessions organized in 6 parallel tracks, a special RFID session, 4 poster sessions, 16 professional development courses, and 3 evening programs that included a panel discussion on the emergence of medical devices, a plenary session on the evolution of mobile processing architectures, and a seminar on advanced interconnection technologies. It was quite a challenge for one to attend those technical presentations

and posters of interest without a scheduling conflict and still meet with exhibitors.

As in past years, students were encouraged to attend and participate in the conference. In fact, an ECTC Student Reception was



hosted by IBM on opening day. Additionally, Intel Corp. sponsored this year's award for the Best Student Paper.

The 14 member Executive Committee led by General Chair, Jean Trewella of IBM, Vice General Chair, Rajen Dias of Intel, Program Chair, David McCann of Amkor, and Assistant Program Chair, Wolfgang Sauter of IBM, did an outstanding job of planning the 2010 event with help from over 195 volunteers from around the world. A concerted effort was made to focus on 3-D packaging technologies and to bridge the different functional



Rajen Dias, Jean Trewella, Wolfgang Sauter and David McCann

groups, such as reliability, interconnect processes, and materials, which all play critical roles in advancing new technologies. David McCann added, "A significant portion of the technical presentation at the conference focused on how to solve the challenge of increased density requirements for new products while approaching limits in current interconnect and packaging technologies. Technical depth of the presentations was strong and triggered significant discussion by attendees."

### Attendance Rebounds

Signs of recovery in the technology sector of the economy were evident. Overall, 844 conference attendees, representing 15 countries, had the

opportunity to listen to and learn from a selection of 344 presentations and posters on a wide range of topics that included advanced packaging, modeling and simulation, optoelectronics, interconnections, materials and processing, applied reliability, assembly and manufacturing technology, components and RF, and emerging technologies. Attendance increased more than 50% over the 551 attendees at the 2009 event held in San Diego, CA.

The 16 professional development courses, which included 10 new courses, drew 340 attendees this year. This figure included 58 walk-in attendees who had not pre-registered. A good selection of topics may have accounted for the 84% increase in PDC attendance over the 2009 event which drew 185 attendees.

### Special Events

The featured speaker at the annual ECTC Luncheon was Dr. Tien Wu, Chief Operating Officer of Advanced Semiconductor Engineering (ASE) Group. Dr. Wu joined ASE in March 2000 and assumed the position of Chief Executive Officer at ISE Labs, an ASE testing and engineering subsidiary, in March 2003. He also serves on the ASE Board of Directors. Dr. Wu offered a glimpse of the future in his presentation titled "Semiconductor Business Evolution."

At this luncheon, the authors of the Best and Outstanding Papers from last year's 59<sup>th</sup> ECTC received their awards.

Three evening sessions, open to all attendees, included an ECTC Panel Discussion with five distinguished speakers discussing "The Emergence of the Medical Devices Industry through the View-glass of Microelectronic



Dr. Tien Wu, COO of ASE Group

Packaging Innovation, an ECTC Plenary Session with five industry leaders addressing “The Evolution of Mobile Processing Architectures”, and a CPMT Seminar with five researchers describing “Advanced Bump and Bump-less Interconnection Technologies.”

### Annual CPMT Awards

The IEEE Components, Packaging and Manufacturing Technology Society sponsored a luncheon for conference attendees and presented a number of annual awards. Herbert Reichl, an IEEE Fellow and professor at the Technical University of Berlin, Germany, received the prestigious *2010 IEEE Components, Packaging and Manufacturing Technology Award* for contributions to the integration of reliability in electronics systems and leadership in research and education in electronics packaging.

William Chen of ASE was awarded the *2010 IEEE CPMT David Feldman Outstanding Contribution Award* for leading the CPMT Society in defining the value propositions and executing strategic outreach to CPMT stakeholders in



Rolf Aschenbrenner, Herbert Reichl, and William Chen

the major microelectronics development and manufacturing regions around the world.

Frank Shi of UC, Irvine received the *2010 IEEE CPMT Outstanding Sustained Technical Contribution Award* for his accomplishments in multiple fields including optoelectronic packaging technology development, device and packaging materials development, electronic packaging and manufacturing technology development, and his leadership in the technology transfer of these developments from a research environment to an industrial commercialization and production environment.

Michael Pecht of University of Maryland was awarded the *2010 IEEE CPMTExceptional Technical Achievement Award* for his seminal contributions in the area of electronics reliability from which he developed the new and significant field of prognostics for electronics.

Ning-Cheng Lee of Indium Corporation of America received the *2010 IEEE CPMT Electronics Manufacturing Technology Award* for being a driving force in removing the ‘art’ of SMT assembly and replacing it with science.

Shaw Fong Wong, of ATD-Malaysia was honored with the *2010 IEEE CPMT Outstanding Young Engineer Award* for his contributions in the area of component level solder joint reliability for flip chip packaging, as well as his development of a reliability degradation model for thermal interface materials.

Jorma Kivilahti of Aalto University School of Science and Technology in Finland was awarded the *2010 IEEE CPMT Regional Contributions Award – Region 8* for establishing the IEEE CPMT Finland chapter, developing programs to serve local CPMT members and the profession and building strong collaborations and networks within the region.



Technology Corner Exhibit Hall

### Exhibition Hall

The exhibit hall featured 65 companies this year, including 10 new exhibitors, for a 25% increase over last year. The I-Therm conference was co-located with ECTC this year, and this may have accounted for the increased number of exhibitors offering thermal solutions.

Also, four Poster Sessions were held in the Exhibit Hall over the two day period that the Technology Corner was open. Attendees could interface directly one-on-one with each of the authors of the 71 posters.

### Closing Remarks

Program Chair, David McCann hosted the luncheon on the final day and paid tribute to the numerous people that volunteered their time to make the 2010 event a complete success. Jean Trewella of IBM was presented with a plaque, the *General Chairman’s Award*, in appreciation for her outstanding leadership as General Chair 2010. Nine volunteers received the *ECTC Volunteer Award* for their dedication and length of service. In particular, Albert Puttlitz was recognized for his 25 years of volunteer service. Those contributing 10 years of service were Dan Baldwin, L.J. Ernst, Ceferino Gonzalez, Beth Keser, S.W. Ricky Lee, Li Li, Sylvain Ouimet, and Jean Trewella.

At the close of the program, it was announced that Rajen Dias of Intel will be the General Chair of the 61<sup>st</sup> ECTC to be held in Orlando, FL from May 31 to June 3, 2011.<sup>Sp</sup>

(continued on Page 22)

# GUEST EDITORIAL



## 3D Integration: Ain't No Stopping It Now. . .

By Françoise von Trapp, Contributing Editor [*3D InCites*]

**H**ave you noticed? 3D integration is steadily gaining in the popularity polls as the solution to microelectronics manufacturing issues. Sure, there are many front-end fans of CMOS scaling and those advocating 450mm, but more and more we're seeing all eyes turning to 3D as the answer for concerns ranging from the chip and package to whole system.

Take MEMS, for example, after attending the 8th Annual MEPTEC MEMS Symposium-MEMS and IC System Integration: from Sensing to Awareness, May 20th, in San Jose, Paul Werbaneth reports an increasing enthusiasm for 3D WLP technologies. Jeff Perkins of Yole Developpement reportedly said there's room in the industry for monolithic integration of ICs, the hybrid approach, and 3D WLP w/ TSV MEMS. Specifically with regard to the latter, availability of 3D WLP services and other 3D WLP w/ TSVs at OSATS allows for low-cost, MEMS/IC integration solutions for the sought-after size reductions in MEMS products like microbolometers on Read-Out-ICs, which are packaged using 3D WLP w/TSV. And in Roger Grace's opinion, monolithic integration of MEMS and CMOS system components is declining, while 3D chip stacking is increasing. He cites commercial drivers such as gesture recognition systems, analytical instruments that are hand-held portable, and mesh-network autonomous sensing seismic detection platforms, all of which benefit from

the building block approach of 3D chip stacking.

Indeed, for an industry not known for moving ahead at warp speed, the progress in 3D seems to be picking up momentum as the word of its benefits spread across the supply chain. I'm starting to see articles in design journals touting the benefits of 3D similar to those that we saw three years ago in those publications devoted to processes and technologies. Process folks have been screaming for the design and test community to dive in for at least two years now (I first noted the call at SEMICON West 2008 during its Packaging Summit devoted to TSV processes), but at that time, EDA vendors weren't quite convinced that 3D was a worthy investment. Now, the big design houses are throwing their hats in the ring, and test standards are now a main focus for IEEE. Why? Two reasons. Market demand has arrived, and processes have been sorted out to the point that design rules can be determined and implemented.

### Designing in 3D

Here's where 3D progress is destined to digress from the path 2D emerging technologies followed. Now that we've got the attention of the design community, it's clear that adapting 2D approaches to achieve market adoption isn't a viable option any longer. 3D calls for a whole new protocol. SEMI's Tom Morrow

predicted it two years ago in an interview with me when he said "The great supply chain that worked in the past is going to be dysfunctional in the future. It's a new world. The next era will be driven by the end system-level designer." That era starts now.

As Ahmed Jerraya, research director and head of strategic design programs at CEA-Leti recently explained to me, the existing 2D design architecture is not sufficient for designing 3D systems. In defining a new 3D architecture, it's necessary to develop software in several layers. To achieve this, it's critical to simultaneously develop the architecture and software. That's why Leti, with the support of ST Microelectronics, has spearheaded the European PRO3D Consortium. "Each of the partners in the consortium has existing technology to cover the food chain. The idea is to align all the technologies to create a holistic solution," said Jerraya. 3D processes are not the issue here. While some technology issues will be addressed by the consortium, Jerraya said it will mainly focus on two software-related projects: developing a 3D architecture exploration environment; and development of a software environment for 3D cooling.

Georgia Tech's 3D Systems Packaging Research Center also advocates the holistic approach, drawing inter-disciplinary resources from its engineering department to fuel 7 core research technologies, namely electrical design, mechanical design, nano-materials, nano-scale components,

interconnections, assembly and reliability, thermal technologies, and systems integration. You can read more in this issue's feature, Georgia Tech's Vision for Ultra-miniaturized Device and Systems Packaging.

### Non-Traditional Market Indicators

While analysts analyze historical market data, comparing trends based on past emergent trends (is that an oxymoron?), consumer spending habits, etc, I tend to look at what I call "non-traditional market indicators" to evaluate 3D's progress. For example, you can see telltale signs simply by paying attention to conference agendas. Last year's technology limitation and bottleneck becomes this year's main attraction. I've noticed that papers being presented are shifting in focus from processes themselves to test, measurement, inspection and reliability of said processes. Design and test conferences are adding 3D workshops, and the design and test communities are presenting at conferences previously considered to be process and technology focused. Sounds pretty holistic to me.

For the past two years, SEMICON West's Packaging Summit was devoted to 3D processes. This year, there's no summit, but there IS an exhibitor pavilion devoted to 3DICs, two TechXpot packaging sessions on 3D process technologies; a TechSite session titled 3DIC-Co-design Challenges: How to Speed 3D IC Deployment; a half-day workshop being run by SEMATECH on 3D Interconnect Metrology, and a half-day workshop co-sponsored by SEMI and SEMATECH titled 3D Interconnect Challenges and Need for Standards. That's right. Standards. While a lack of standards still isn't considered a show-stopper for 3D, calling for them is a sure sign that we're closer to market adoption.

When you think about it, SEMICON West's agenda provides a good benchmark of 3D's progress. For an organization traditionally devoted to front-end technologies, their continued expansion into 3D, beyond

conference topics and into exhibition space, is a testament to the growing marketability of the concept itself. Its official; across the board from the chip to the system, 3D sells. What more do we need to say? ☺



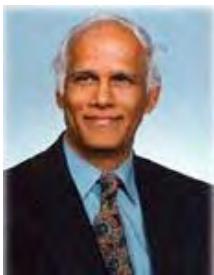
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# Georgia Tech's Vision for Ultra-miniaturized Device and Systems Packaging

## Encompassing R&D, Inter-disciplinary Education and Global Collaborations

By Rao R. Tummala, Venky Sundaram, P. M. Raj, Raghu Pucha, Tapo Bandyopadhyay,

Nitesh Kumbhat, Vivek Sridharan, Traci Walden-Monroe, Dean Sutter

[Georgia Tech Microsystems Packaging Research Center]

**M**oore's Law began with transistor integration at IC level in the late 1940s. Georgia Tech's 3D Systems Packaging Research Center (GT PRC) has launched a new era of Moore's Law for system integration with the system-on-package (SOP) concept.

There are two primary reasons for SOP. First, is functionality and miniaturization at package and system levels. There has been phenomenal progress made at the IC level from 2500nm technology in 1970s to 32nm and beyond, resulting in a billion transistor IC. However, the packages and system boards that house these and other devices and components are almost a billion times bigger in lithographic ground rules than the ICs themselves.

The second reason for SOP is lack of quantum jump in electrical performance or functionality at the system level. The SOP vision eliminates the IC-system gap (**Figure 1**) using nanoscale materials, processes, and unique properties that they produce for every component of the system. This includes interconnections; thermal interfaces; passive components such as capacitors, resistors, filters; and batteries. The SOP concept is expected to revolutionalize system functionality in smallest size and at lowest cost, thus

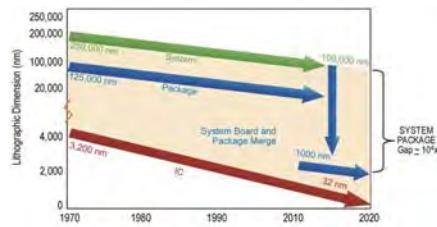


Figure 1. SOP merges package and board close to IC ground rules

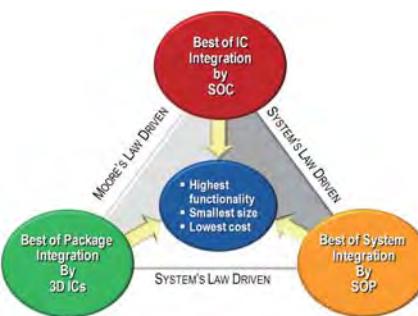


Figure 2. SOC for ICs, 3DICs for modules and SOP for systems

complimenting system-on-chip (SOC) at the IC level and 3D integrated circuits (3D ICs) at module level (**Figure 2**). **Figure 3** is PRC's vision of SOP-based system with all its nanoscale system technologies.

In contrast to traditional academic research by faculty and graduate students alone, Georgia Tech PRC has pioneered an integrated approach with cross-discipline education of students at BS, MS and Ph.D levels and industry collaborations with more than 70 companies from US, Europe and Asia – all in SOP.

### SYSTEM-ON-PACKAGE (SOP)

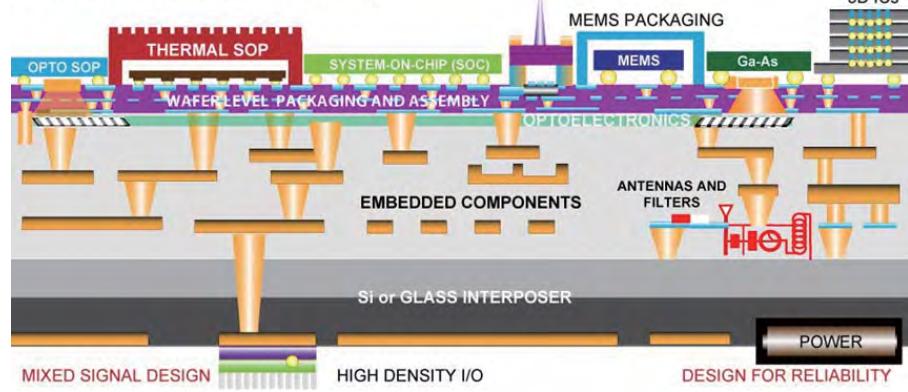


Figure 3. PRC's vision of SOP with the necessary core technologies

### Seven core packaging technologies

To explore and demonstrate a futuristic system, PRC focuses in seven core research areas including electrical design, mechanical design, nano-scale materials and processes, nano-scale components, advanced substrates, interconnections, and system integration.

### Electrical design

The electrical design team vision and strategy is to model and design ultra-miniaturized modules and systems using SOP technologies (**Figure 4**). The research focus includes electromagnetic modeling; signal and power integrity modeling and analysis, and design of embedded actives and nanoscale digital and RF passive components; ultra miniaturized pad-to-pad interconnections; low-loss dielectrics; and high-speed signal channels in electronic, optical, and MEMS packages. The electrical design is aimed at a wide range of packaging technologies such as organic, glass and silicon packaging.



Figure 4. Electrical design focus

Currently, two focus areas include electrical design of ultra-miniaturized and high-density organic packages with chip-last embedded MEMS, actives, and passives (EMAP). The actives include multiple embedded digital, analog, RF, and MEMS. The electrical design team has demonstrated high Q ( $Q>100$ ) inductors (1-10GHz) in 100 $\mu\text{m}$  thick (2-metal layer) and 160 $\mu\text{m}$  thick (4-metal layer) low-loss organic substrates; as well as band pass filters (2.4 and 5.8 GHz bands) with insertion loss  $<1\text{dB}$  and rejection 25dB. In development are solutions for power integrity, electromagnetic interference and noise coupling problems in packages with embedded active chips.

The electrical design of low-cost silicon and glass packages to package 3D ICs is supported by a global industry consortium of approximately 10 companies. The focus here is in the development of high-performance and ultra-miniaturized packages with highest through-package-vias (TPVs) and highest I/O density. Accurate electrical models for TPVs in silicon substrates have been developed.<sup>1</sup> Novel electrical designs for power, signal, and clock distribution are being developed utilizing the semiconductor effects.

## Mechanical design

Up-front mechanical design from first principles coupled with experimental reliability assessment is the PRC's strategy for mechanical design in a systematic flow, beginning with process modeling (Figure 5).

For example, in the development of silicon and glass packages with TPV technology, up-front physics-based process mechanics and design-for-reliability models for various failure mechanisms are developed to evaluate various design, material, and process

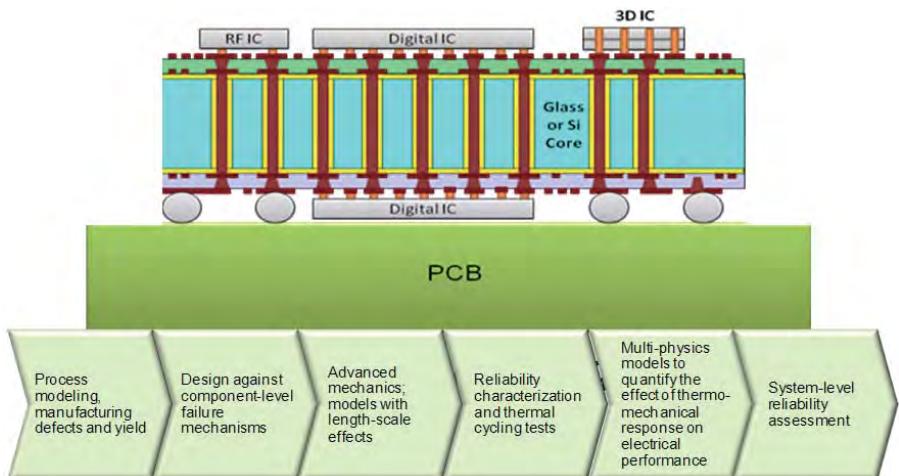


Figure 5. PRC's systematic process for mechanical design

options even before the prototypes are made. Materials display strong scale effects when the characteristic length scale associated with non-uniform plastic deformation is on the order of microns. For example, in the mechanical design of copper TPVs with the diameter in the order of 10-25 $\mu\text{m}$ , the traditional continuum-based modeling techniques need to be augmented with models that incorporate the copper micro-scale hardening effects.<sup>2</sup>

## Nano packaging materials

Traditional packaging materials such as dielectrics and thermal interfaces; and passive components such as capacitors, filters, and antennas, have fundamental limitations in achieving the best property in smallest size. Over the past five years, PRC has explored a number of nanomaterials to address these two barriers (Table 1).

## Nano-scale components

Electronic systems require many components including actives, passives, thermal structures and batteries, as well as interconnections to interconnect all these and more to form systems. The current approach uses bulky milliscale components and are therefore the biggest bottlenecks for enhancing system functionality per

unit area, performance as defined by speed or bandwidth, and power consumption as defined power losses. Figure 3 illustrates some key component technologies in the SOP concept, and a brief description of PRC's nanocomponents focus in power supply components is provided here.

Thin-film capacitor for decoupling and voltage regulation has been one of the greatest barriers for system miniaturization and enhanced-digital performance. This is due to lack of low-cost, low-temperature, thin-film material and process technologies with high permittivity at high frequencies compatible with silicon and organic substrate technologies. Over the past decade, GT-PRC has advanced high-density thin-film capacitors using low temperature, organic or IC-compatible

Components	Today's materials	Nanomaterials research at GT PRC
Capacitors	Sputtered and solgel thin films 1-2 $\mu\text{F}/\text{cm}^2$	<ul style="list-style-type: none"> <li>Nanoscale electrodes</li> <li>Conformal nanodielectrics</li> <li>100 <math>\mu\text{F}/\text{cm}^2</math></li> </ul>
Inductors	Sputtered and plated metals 100 nH/mm <sup>2</sup> , 10 MHz	<ul style="list-style-type: none"> <li>Magnetic nanocomposites and nanowire arrays</li> <li>1000 nH/mm<sup>2</sup>, 100-1000 MHz</li> </ul>
RF dielectrics	LTCC, LCP, PTFE, BCB Permittivity: 2.5-8 Permeability: 1	<ul style="list-style-type: none"> <li>Nanoscale super-paraelectric and super-paramagnetic materials</li> <li>Multiferroic materials</li> <li>Permittivity: 20-100</li> <li>Permeability: 5-100</li> </ul>
Interconnections	Solders 150 $\mu\text{m}$ -pitch reliability	<ul style="list-style-type: none"> <li>Nanometal and nanocomposite interconnections</li> <li>20-50<math>\mu\text{m}</math>-pitch reliability</li> <li>150-250°C processing</li> </ul>
Batteries	LiCoO <sub>2</sub> , LIPON, Li-C 0.1 mAh/cm <sup>2</sup> $\mu\text{m}$	<ul style="list-style-type: none"> <li>Nanoelectrodes</li> <li>Super-ionic conductors</li> <li>1 mAh/cm<sup>2</sup> <math>\mu\text{m}</math></li> </ul>
Thermal Interfaces	Thermal grease, solders 0.1°C cm <sup>2</sup> /W	<ul style="list-style-type: none"> <li>CNT based and nanocomposite TIM</li> <li>0.001°C cm<sup>2</sup>/W</li> </ul>

Table 1. Focus of Nanopackaging Materials Research at GT PRC

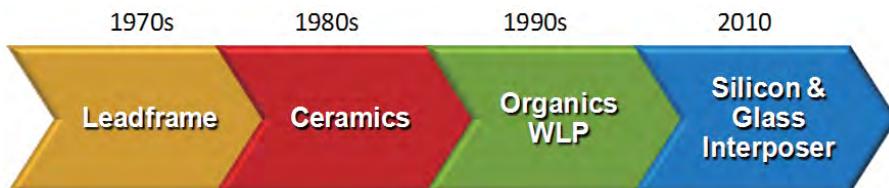


Figure 6. Evolution of packages for increased I/Os and lower cost

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processes.<sup>3</sup> High-permittivity, thin-film dielectrics by themselves are not adequate to achieve higher capacitance densities with high reliability, so the industry is shifting to trench capacitors. To address the cost and throughput limitations of these approaches, PRC has pioneered novel nanostructured electrode and conformal dielectric technologies to achieve capacitance densities around 50-60  $\mu\text{F}/\text{cm}^2$  at high voltages. This exceeds what has been achieved with trench and tantalum capacitors in terms of volumetric efficiency. Power conversion for portable applications demanding high current supply with high efficiency largely depends on inductive energy storage elements. At this time, inductors on silicon do not meet the Quality Factor (Q), size, magnetization, and frequency requirements for many power electronic applications. Novel magnetic nanocomposite cores with innovative silicon and organic substrate-compatible 3D fabrication techniques for enhanced inductance densities and magnetization are being developed by PRC to miniaturize inductors while retaining their high frequency stability and high Qs.

## Package substrates

Substrate technology is the first building block with which to integrate all other system components. **Figure 6** illustrates the trend beginning with leadframes and plastic packages in the 1970s, high temperature co-fired ceramics (HTCC) in the 1980s, glass-ceramics or low temperature co-fired ceramics (LTCC) in the 1990s, and most recently build-up thin-film organic packages.

Organic packages, currently considered the most leading-edge, are reaching limits in I/Os because of poor dimensional stability, thus requiring large capture pads for layer-to-layer interconnections. These problems are easily addressed by silicon interposer technology developing worldwide using 200 and 300mm wafers. While silicon interposers solve the I/O density problem, it is not at a low enough cost per I/O to be a pervasive technology (**Figure 7**). The GT PRC proposes to solve both the I/O density and cost problems by panel-based, low-cost

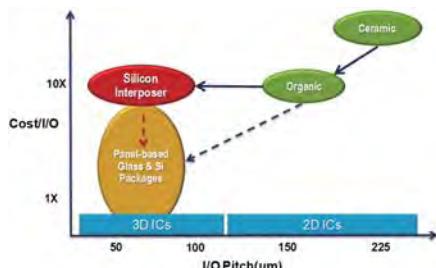


Figure 7. GT PRC's approach to low-cost Si and glass packages

material and process approaches with both silicon and glass packages.

Glass as a package substrate material provides excellent dimensional stability, highest electrical resistivity (insulator), si-matched CTE and is available in thin and large panel format. Non-CMOS grade panel-based silicon is also an excellent package substrate with high thermal conductivity and dimensional stability, as well as matched CTE to Si. A double-side, panel-based fabrication approach using low-cost materials is being developed with optimal electrical, mechanical, and thermal performances. The main challenge with both Si and glass is how to form through vias at low cost.

### Interconnections, assembly and reliability

The main drivers for innovation in high-reliability device and system interconnections are increased I/O density, high-throughput tools, and low-cost materials and processes. Therefore, interconnection research at PRC focuses on ultra-miniaturized, highly reliable, fine-pitch, low-profile and low cost materials and processes (Figure 8). This research falls into two major areas: chip-to-package and package-to-board.

The PRC strategy in chip-to-package interconnection is to design from first principles to achieve 10-40x higher I/O density than traditional flip-chip assembly in two ways:

- Chip-last copper-to-copper interconnections:* The goal of this research is to explore and demonstrate highly reliable ultra-fine pitch ( $\sim 30\mu\text{m}$ ) Cu-Cu interconnections bonded to organic substrates at low temperatures ( $160^\circ\text{C}$ ). The interconnect structure has been shown to pass reliability tests such as thermal cycling test (TCT), high

temperature storage test (HTS) and unbiased highly accelerated stress test (U-HAST), as well as 2000 thermal cycles from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .<sup>4</sup>

**2. Reactive nano-particle based pad-to-pad interconnections:** The objective of this project is to enable extremely fine ( $<10\mu\text{m}$ ) pitch pad-to-pad interconnections at low-temperatures ( $<250^\circ\text{C}$ ) using ultrathin

“bumpless” thin metal as the reactive bonding layer. The nano-metal layer enhances the reactivity, thus lowering the bonding temperature. This research addresses several of the fundamental limitations of today’s flip-chip technology such as pitch, processing cost, thermo-mechanical reliability and electromigration resistance. It also overcomes the challenges

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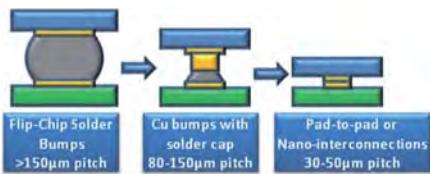


Figure 8. PRC strategy for interconnection research

of direct Cu-to-Cu bonding technology requiring high-temperature ( $400^{\circ}\text{C}$ ) bonding, plasma cleaning of surfaces and long annealing times.

In the package-to-board interconnections, PRC's strategy is to explore and demonstrate SMT-compatible interconnections for silicon-to-board or glass-to-board interconnections. This research is being performed with a variety of options that include low-modulus solders and zero-stress interconnections. (Figure 9).

## Systems integration

The system integration research at PRC aims to integrate all these novel technologies into first proof-of-concept packages or modules.

The PRC strategy in system integration begins with design from first principles leading to a set of research targets for materials, processes, and structures. Miniaturization challenges addressed include isolation of components at close proximity, high reliability interconnections at fine pitch, thermal dissipation of embedded active and passive components, and involvement of supply chain companies for materials and design tools to provide a path for manufacturing infrastructure.

Going well beyond fundamental research and individual leading-edge technologies, PRC has assembled an inter-disciplinary team of academic and

research faculty, industry engineers serving as mentors to BS, MS, Ph.D students to demonstrate the first-of-its-kind digital-RF-optical integrated system to transmit and receive on a single module called Intelligent Network Communicator (INC). This demonstration of 3.1 Gbps digital data rate, 5.8GHz RF front end, and 10Gbps optical data rate was achieved in a small form factor SOP package of 50mm x 75mm (Figure 9).

## Interdisciplinary education

The ultimate goal of PRC's educational vision is to produce "cross-discipline individuals."

Georgia Tech's comprehensive and inter-disciplinary educational programs in packaging include courses, curricula, textbooks, certificates and degrees. Each PRC student is educated with an interdisciplinary focus combining electrical, mechanical, chemical and materials sciences and engineering knowledge because electronic systems are interdisciplinary by nature.

## Global Industry Collaborations

The PRC's vision for industry collaboration includes not only R&D but also intellectual property development, manufacturing infrastructure development involving supply chain companies, facilities-usage, and human resource development at the BS, MS and Ph.D levels. In contrast to the industry's internal R&D that focuses on the three-to-five years prior to manufacturing, industry collaborations at PRC focus

beyond five years because most new technologies take longer than five years of R&D before being ready for manufacturing. This process starts with exploration of new ideas by PRC's research team before coupling with the industry for their strategic technologies in one of two ways: through establishment

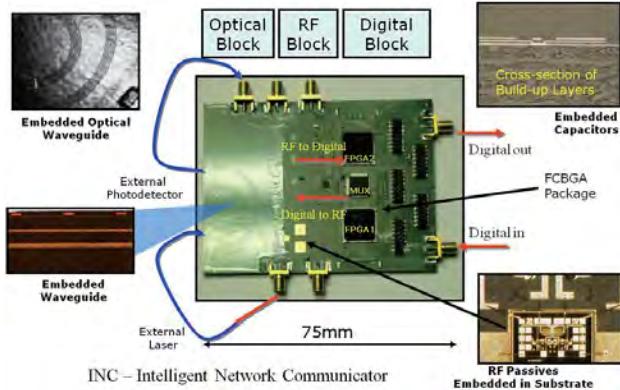


Figure 9. First Digital-RF-optical SOP demonstration at PRC

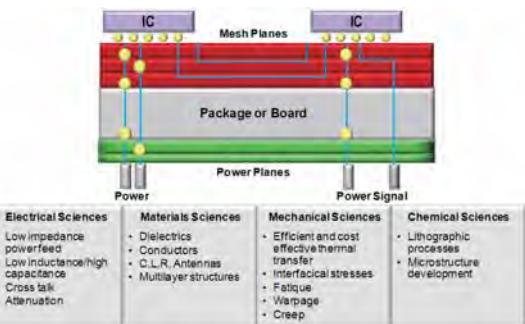


Figure 10. Cross-discipline education at GT PRC

of research consortia for strategic technology developments; and infrastructure and network consortia for all others. Currently, there are two primary industry research consortia involving more than 25 global companies at the PRC: one in Embedded MEMS, Actives and Passives (EMAP) and the other in panel-based, low cost silicon and glass packages. A third and soon-to-be-launched program, called Industry Partnership in Packaging (IPP), seeks to involve more than 50 global-networked companies to develop infrastructure needed for future of packaging industry.

- 1) T. Bandyopadhyay, R. Chatterjee, D. Chung, M. Swaminathan and R. Tummala "Electrical modeling of Through Silicon and Package Vias," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, 2009, pp. 1-8.
- 2) Pucha, R.V., Ramakrishna, G., Mahalingam, S., and Sitaraman, S.K., "Modeling Spatial Strain Gradient Effects in Thermo-Mechanical Fatigue of Copper Micro-structures", *International Journal of Fatigue* 26(9), 2004, pp 947-957.
- 3) Isaac Robin Aboodu, P. Markondeya Raj, Jin Hyun Hwang, Manish Kumar, Mahadevan Iyer, Hiroshi Yamamoto and Rao Tummala, "Electrical reliability of embedded ultra thin-film ceramic capacitors in organic packages fabricated via chemical solution processing on bare copper foils", *IEEE Electronics Component and Technology Conference, ECTC 2007*, Reno, Nevada, pp. 1014 – 1018, May 2007.
- 4) Nitesh Kumbhat et al, Proceedings, Electronic Components and Technology Conference, 2009, pp. 1479-1485.

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# TEST PATTERNS



## Through Silicon Vias (TSV) Bring New Test Trade-offs

By Paul Sakamoto, Contributing Editor [*DFT Microsystems*]

One of my favorite old TV series is "The Hitch Hiker's Guide to the Galaxy" from the BBC. The story starts out when an average guy named Arthur Dent wakes up to find out that his home is about to be demolished to make way for a motorway. He is then informed by his friend Ford Prefect — who is actually an alien travel book researcher — that the Earth is about to be vaporized as part of a "Hyper-Space bypass" for extra terrestrial, faster than light-speed travelers. Many of you must now be wondering how this can possibly relate to test. Well, I think it reminds me of some of the trade-offs we face in the design and test of three dimensional (3D) stacked packages with through silicon vias (TSVs). To make TSVs some silicon territory is being literally vaporized to make way for direct pathways between circuits on different die. A TSV might be ten or more microns in diameter, so the resulting area is large enough for a lot of digital mission-mode gates to occupy. This valuable space is sacrificed to save package and board space as well as to increase chip-to-chip signal performance; to create an effective "Hyper-space bypass" of sorts.

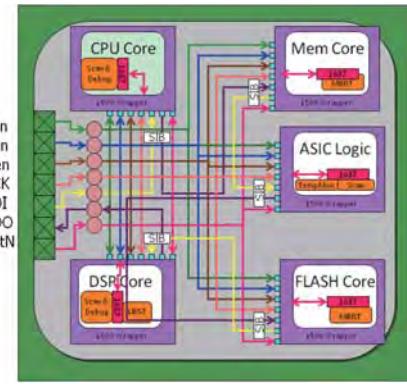
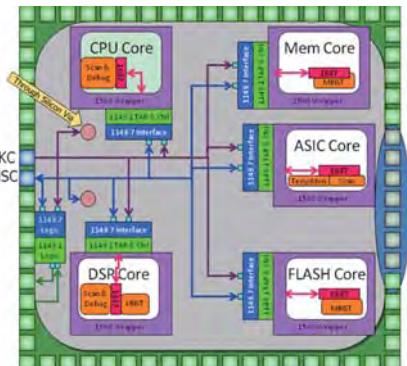
Today, the benefits of the TSV similarly overcomes many of the evils that the process brings, including loss of silicon real-estate, because of the product benefits that come with them. However, when TSVs need to be placed for test access, the reception is not always so great because the test access path, often related to JTAG based scan architectures, does not have a lot to do with the mission mode of the devices in the stack. That is, the manufacturer doesn't get to charge

anybody for the silicon used for test access port space. It is viewed as "cost" or "expense" rather than "value added." The result is that it makes sense to reduce the number of TSVs for test access and use the savings to reduce the area of the resulting chip design or to use the space for money-making circuits. The test access standard chosen for stacked die access will determine how much area is used for TSV connections, the physical layer of the TAP (Test Access Port), the type of ATE equipment needed, the ability to test in parallel, and the speed of test among other factors. Because the subject is evolving, complex and there are competing ideas, there is no agreed upon standard as of yet.

To help me through the fog of "if, what and maybe" for 3D testing, I called upon my old friend Al Crouch who is part of several groups who are wrestling with this topic. As always, Al overloaded my shrinking cranial capacity with masses of great information. We don't have the space to cover it all in detail here, but what it comes down to is a couple of big architectural choices. The first choice is, given a fixed amount of test data and instructions, do you run more test access pins at moderate speed as 1149.1 JTAG tends to do today or can we find a way to run fewer pins faster? Depending on the choice made, it's possible to have as few as 2 pins, which connect through the stack as TSVs, or there could be more than 7 at the other extreme. Additionally, some of the architectures that use more pins require chip enable connections to select or deselect the die or function in the stack. This results in not only more area lost to TSVs, but the possibility of non-uniform test access footprint in the die stack since the

enable signal might not be routed to all the die. As such, the higher pin count solutions tend to add pins to the TSV test access bus as the stack of die gets more layers. The two pin scheme can potentially stay limited to two pins in the stack because it will use packets to send test information to and from the appropriate circuit. Depending on who you talk with, packets in the test bus are either a simplification or a complication with respect to the test access circuitry. From an area standpoint, it's quite likely the SERDES (serializer-deserializer) circuits in the two wire scheme will take up a lot less space than the TSVs of the full 1149.1 ports.

Other advantages of the two wire, packet transmission approach come at wafer sort. In some cases, the 3D device



components at wafer sort may have almost no mission-mode functionality at all and scan based testing ala 1149.1 may be the only real test method for these known good die (KGD) before ... assembly. That is, depending on how functionality is partitioned among the die in the stack, structural test is likely to be the only tool for creating the KGD test. Having only two pins per access port would allow more die to be tested in parallel, it reduced the probe card pins per die, and has other benefits. In fact, with some standardization of the test access and power supply pins, it may be possible to use one probe card for all the die in a stack. The more pins you use, the less likely this is. Also, remember that any pin to be probed needs to have a bonding pad as well as a TSV. This is another serious area hit.

I was able to speak with another friend who is in charge of the design of extremely large, high-performance chips at a large systems company. His chips will not have a high stack due to power, but will still use TSV for performance. Since these chips already have a couple of thousand pins and associated TSVs, the addition of a few extra TSV connections does not create an issue. However, the scalability of addressability native to packet signaling solutions still work out well in his case. Each of his chips might have many cores and a well designed packet architecture will help standardize the test access on each die and yet provide the flexibility to have sufficient test coverage.

In the accompanying illustration, you can see the difference in complexity between the two approaches. I am sure that a compromise will be reached by the time 3D becomes a larger percentage of shipments.

So, now you know some of the trade-offs of TSVs for test access, hyper-space bypasses and silicon motorways. Just remember, stay tuned for more developments here and as "The Hitch Hiker's Guide to the Galaxy" said on its cover, "Don't Panic."

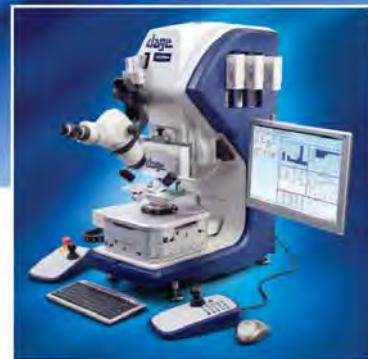
A proposed access solution using two

TSV connections for test in the 3D stack and two pads for wafer sort. The connections are simpler at some expense in circuit and signaling complexity. Area is conserved relative to the insertion of more TSVs.

An example of a chip with a more traditional 1149.1 JTAG implementation adapted for 3D stacks. The result is more connections and more area lost, but the fundamental designs and tools are legacy in nature. Illustration courtesy of Al Crouch.<sup>8</sup>

## New Horizons in Bond Testing

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# INDUSTRY NEWS

(continued from Page 11)

## Tarzwell Outlines Low-cost, Multilayer PEC Substrate Technology at 2010 PEAMS Symposium

PCB industry veteran Robert Tarzwell, of DMR Ltd., kicked-off the 2010 Printed

 **SGIA Printed Electronics & Membrane Switch Symposium**

Electronics and  
Switch (PEMS)  
Symposium

with a keynote describing a novel Printed Electronic Circuit (PEC) manufacturing technology, dubbed Silver Bullet, which may propel printed electronics beyond simple, single-sided, flex circuits. The



event, organized by the Specialty Graphic Imaging Association (SGIA), was held May 18-20 in Phoenix, AZ and drew 20 exhibitors and more than 220 attendees.

According to Tarzwell, working with Taiyo America and Caledon Controls, he developed a liquid photo-imageable dielectric and a high conductivity, silver ink that allowed for the manufacturing of multilayer PECs using an additive trench technique with embedded, 25 $\mu$ m-wide traces and spaces. The traces can range in thickness from 12.5 to 100 $\mu$ m and achieve resistivity comparable to copper foil.

A couple of years ago, Amkor Technology recognized the need for an advanced high density interconnect (HDI) technology to support the needs of multilayer IC package substrates and embarked on a program with partners Atotech and Unimicron to develop fine line, embedded copper traces using laser-ablated trenches. While Silver Bullet may not displace the Amkor approach, it has some advantages that are worth investigating.

The PEC technology requires little investment in capital equipment — essentially a screen/stencil printer and an image exposure/developer unit. No drilling is required. It's an environmentally-friendly

process conducted at relatively low temperatures. The silver-filled ink is solderable and can be plated-up with electroless Cu, immersion Ni, and immersion Au, Sn, or Ag. Stacked and filled, blind and buried, microvias, as small as 50 $\mu$ m diameter, have been demonstrated. Potentially, the fabrication cost can be much less than conventional, subtractive Cu-etched PCBs and still suitable for most applications.

Some issues to be investigated for IC package applications are wire-bondability of Cu/Ni/Au-plated, silver-filled ink traces, overall substrate yield as a function of layer count for the additive layer process, and the thermo-mechanical properties related to warpage and stress. However, Silver Bullet and printed electronics may find early adoption for flip chip substrates where HDI is required to route high I/O dice. It may also gain traction for HB-LED substrates and wafer level packaging. —

**Ron Molnar, Az Tech Direct, LLC**  
[\[www.aztechdirect.com\]](http://www.aztechdirect.com)

## 3D TEST Workshop Announces Call for Papers

While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop, taking place in conjunction with IEEE International Test Conference (ITC) Nov. 4 and 5 in Austin TX, offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

The workshop will focus exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including systems-in-package (SiP),

package-on-package (PoP), and especially 3D-SICs based on through silicon vias (TSVs). The program committee is currently seeking contributions. For submission details, please visit <http://3dtest.ttc-events.org> or email Erik Jan Marinissen, at [erik.jan.marinissen@imec.be](mailto:erik.jan.marinissen@imec.be). Deadline for submission is August 23, 2010.

## Fraunhofer IZM-ASSID Selects EV Group Equipment for Developing 3DIC HVM Processes

ASSID (All Silicon System Integration Dresden), a new project group of Fraunhofer IZM, has ordered two temporary bonding and debonding (TB/DB) systems from EV Group, with the intention of using them for advanced 3D wafer-level process integration flow development for Fraunhofer's industrial partners.

3D ICs require the use of much thinner wafers of about 100  $\mu$ m or less. Given the inherent fragility of these ultra-thin wafers, processing requires TB/DB technology to ensure the structural integrity of the wafer — particularly when it undergoes high-temperature, high-stress processes such as etching and metallization. By temporarily bonding the ultra-thin wafer to a carrier substrate and then leveraging a stress-free debonding approach after back side processing, TB/DB technology offers integrity-assured processing, which results in higher yield.

According to Jürgen Wolf, manager and coordinator of ASSID, the Fraunhofer IZM-ASSID develops highly tailored processes for semiconductor manufacturers with very different requirements, and therefore need flexible and scalable process solutions. "EV Group's temporary bonding and debonding platforms enable seamless development and evolution of the 3D integration processes and technologies for our customers," he said.

Both systems will be installed later this year at ASSID's state-of-the-art facility in Dresden — the first Fraunhofer Center with a 300-mm line dedicated to developing



processes for high-volume manufacturing of 3D ICs. This takes EVG's worldwide install base for its temporary bonding and debonding systems to more than 60 systems. [[www.evgroup.com](http://www.evgroup.com)]

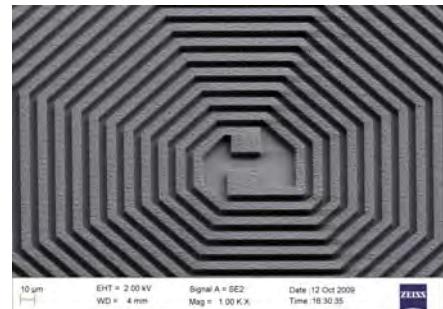
### OSEO Assigns 9M Euro to Support CUIVRE Project

Smart Equipment Technology (SET), Replisaurus Mastering, and research partner, CEA-Leti, were awarded a package worth 9.9 M euro from OSEO's Strategic Industrial Innovation Program to fund CUIVRE, a three year collaborative project aimed at the simplification and shortening of the metallization steps in the microelectronics fabrication cycle, while simultaneously improving the electrical performance.

Certified by the Minalogic Competitive Cluster, CUIVRE (French for "copper") aims to further develop the electrochemical pattern replication

process (ECPR) for the deposition of copper patterns on wafers. This environmentally friendly process provides a simpler way to apply copper interconnect patterns and certain types of components, ensuring better form factors and increased geometrical accuracy, and is a direct response to changes in the semiconductor market needs thanks to the uniformity.

CUIVRE's goal is to stabilize process performance then industrialize the process by effectively integrating it into an actual fabrication process. "The support provided for the CUIVRE project forms part of the Industrial Strategic Innovation (ISI) program, which aims to support collaborative projects containing at least two French SMEs, which must also contribute to creating or strengthening new European or World champions," explained Claude Pinault, Director of the ISI Program.



"This project was ideally matched with the required criteria. We are very pleased to be able to contribute to the progress of this program which we believe to be very promising."

The CUIVRE project brings together SET, manufacturer of high accuracy device bonders; Replisaurus Mastering, a start-up created to develop masters – key components for ECPR technology; CEA-Leti Institute; and four major industry leaders.

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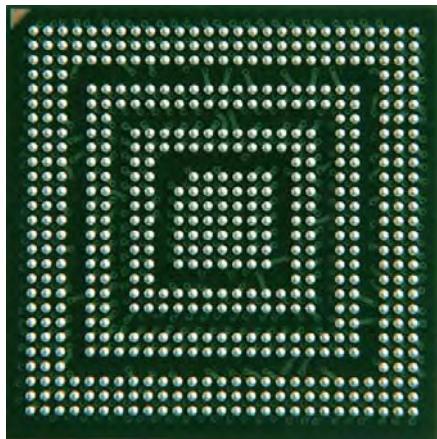
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## **STATS ChipPAC puts Copper Column Bumps to Work**

As of May 25, 2010, STATS ChipPAC's low cost flip chip (LCFC) technology utilizes copper column bump, in an effort to enable low cost flip chip packages with higher routing densities and finer pitch between the columns than standard solder bumps.



Although copper column is a hard bump material that can typically cause damage to low-k (ELK) layers in finer silicon nodes, the LCFC interconnect structure is said to reduce mechanical stress on silicon sub-surface layers, resulting in the elimination of the low-k damage phenomenon commonly observed in sub-45 nm silicon nodes.

"By incorporating copper column bump into our low cost flip chip technology, STATS ChipPAC has expanded the range of applications for which high end flip chip technology can be deployed," said Dr. Raj Pendse, Vice President of Technology.

"Utilizing a copper column interconnect in LCFC packaging achieves a lead-free solution that is reliable and scalable to very fine pitches and provides a natural migration path to solutions such as 3D, Through Silicon Via (TSV), micro bump and green solutions for the future." [\[www.statschippac.com\]](http://www.statschippac.com)

## **Collaboration with Huali Jump Starts imec China**

Imec kicked off the official establishment

of imec China on May 25, 2010, announcing a joint development project (JDP) with the Huali, an advanced chip manufacturer invested in primarily by the Shanghai government. The collaborative effort will focus on fine-tuning imec's 65nm base process at imec's research facilities in Leuven, Belgium, to meet the specifications defined by Huali.



Luc Van den hove, President and CEO of imec (center) is flanked by the Flemish Minister and China's Pudong Government representatives at the opening of imec China

Headquartered in Shanghai's Zhangjiang High-tech Park, imec China's purpose is to facilitate collaboration between imec and Chinese semiconductor and system companies, universities and research institutes in the area of technology transfer, licensing, joint development and training.

"This collaboration with Huali proves that our technologies are valuable for the Chinese market," said Luc Van den hove, President and CEO of imec. "I would like to thank the Zhangjiang High-tech Park for their support in establishing imec China." Van den hove added that China's high-tech potential will likely expand the research organizations collaborative efforts there. [\[www.imec.be\]](http://www.imec.be)

## **STMicroelectronics licenses OptimalTest for Test Floor Monitoring**

OptimalTest, supplier of enterprise-wide test management optimization software, announced a licensing agreement with ST Microelectronics to provide its proprietary adaptive test software for test floor monitoring and control. The system has been deployed on more than 60 testers at two STMicroelectronics sites, and will be

implemented in real-time for wafer sort and final test.

Devices being tested at these sites include complex SoCs and mission-critical devices for high-reliability applications. The software is said to address improved quality, data integrity, yield and test efficiency while reportedly minimizing cost of test for devices aimed at price-sensitive markets.

Using OptimalTest's "lite" adaptive test engine, STMicroelectronics intends to enhance its test floor monitoring and control with no need to revise and re-document how test operations are run.

"OptimalTest's solution will help us achieve even greater consistency and control of our test operations, while allowing us to achieve greater efficiencies in hardware, software and manpower," said Geoff West, VP and General Manager for Manufacturing and Technology Execution, STMicroelectronics. "The solution's high value proposition and cost effectiveness will allow us to compete better while maintaining the highest production standards." [\[www.optimaltest.com\]](http://www.optimaltest.com) [\[www.st.com/stonline/\]](http://www.st.com/stonline/)

## **Vi Technology Names Koen Gutscoven, VP Sales Worldwide**

Vi Technology welcomes Koen Gutscoven as Worldwide Sales VP, to lead Vi TECHNOLOGY global sales activities. Formerly VP sales worldwide for ICOS Vision Systems, Gutscoven brings industry experience, knowledge of customers, products and process to this rapidly expanding company. Jean-Yves Gomez, CEO, Vi Technology says Gutscoven will be a key player in establishing the company's foundation.

While with ICOS, Gutscoven was responsible for customer application support and internal sales administration for the Americas, South East Asia, Japan, Korea, China, Hong Kong, Taiwan, Philippines and Europe. As a result, he's experienced in streamlining feedback

*(continued on Page 29)*

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# State-of-the-art Thin Wafer Processing

By Thorsten Matthias, Bioh Kim, Daniel Burgstaller, Markus Wimplinger, and Paul Lindner  
[EV Group Europe & Asia/Pacific GmbH]

**T**hin wafer processing is a key enabling technology not only for through-silicon-via (TSV) fabrication and 3D chip stacking, but also for power devices, LEDs and MEMS. For handheld applications, the small form factor alone adds value. For device cooling, a thinner wafer brings the heat sink closer to the transistors, thereby improving cooling performance. The performance advantage of TSVs vs. wire bonds has been widely acknowledged by the industry. However, the adoption of this technology for new devices and products is still limited by its cost.

The EMC-3D consortium has carefully analyzed cost-of-ownership (CoO) for TSVs.<sup>1</sup> The costs for etch, barrier/seed layer deposition, and electroplating correlate with TSV depth, diameter and aspect ratio. Reduced wafer thickness enables reduced aspect ratios of the vias, which results in shorter cycle times and lower cost, as well as reduced via diameter, which reduces the silicon real estate consumption. The EMC-3D consortium currently evaluates via-last (pTSV™ 20µm x 80µm) and via first (iTSV™ 5µm x 20-50µm). In July 2009 the partnering companies extended the consortium life by 2 years with the goal to aggressively push the CoO below \$150 for Cu vias.

## The Challenge is in the Handling

Simply speaking, wafer breakage is the thin wafer handling challenge. Mechanical rigidity is not sufficient to store thin wafers in standard cassettes. Various films stress the wafer, causing serious wafer bow and warp. The thin wafer edge is the most critical part of the wafer, and any mechanical contact with the edge at all can nucleate a wafer crack. Single point contact, e.g. due to standard loading pins, can be enough to break a thin wafer. Fully front side processed device wafers are valuable because they are far along the value

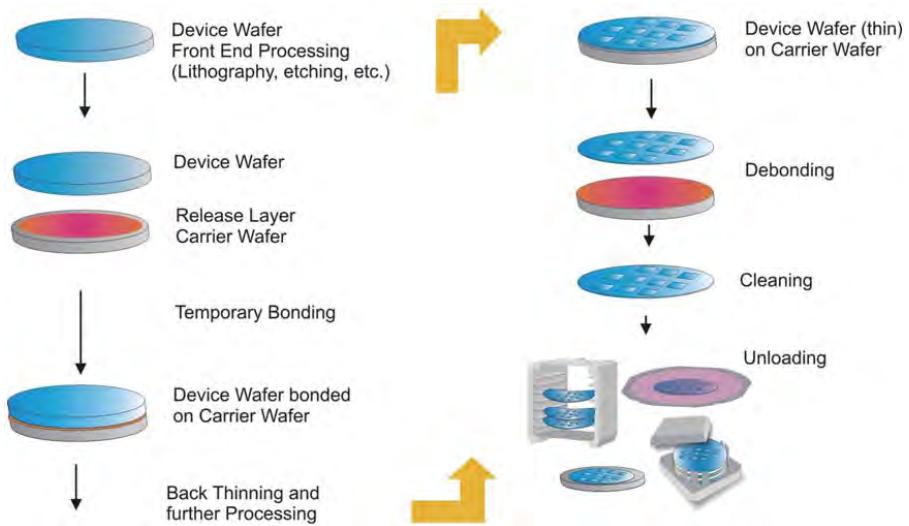


Figure 1. Thin wafer processing based on temporary bonding and debonding

chain. Therefore, the cost of yield can be high, outweighing CapEx and consumables by several orders of magnitude if sub-optimal processing solutions are being used.

Processing of front- and backside of a thin wafer can be implemented by two ways. The first approach is to handle the thin wafer directly. This requires addressing the problem on each individual piece of equipment, with specialized wafer cassettes, robot end effectors, pre-aligners and process modules. However, to minimize the CoO for TSV it is imperative to use the existing foundry and packaging infrastructure as much as possible. Therefore, the second approach is to temporarily bond the thin wafer to a carrier wafer. The carrier wafer provides mechanical stability to the thin device wafer. Temporarily bonded wafers can be handled

and processed like standard bulk wafers. Adding two process steps, temporary bonding and debonding, enables thin wafers to be run in existing fabs with existing equipment.

**Figure 1** illustrates the general process flow for thin wafer processing with temporary bonding and debonding. First, the fully-front-side-processed device wafer is temporarily bonded face down to a carrier wafer. Next, the device wafer is thinned to the desired thickness. The



Figure 2. Thin wafer processing can be implemented in every existing fab with the addition of two pieces of a temporary bonding system and a debonding system

carrier wafer gives mechanical support for the device wafer during thinning as well as all subsequent process steps like etching, deposition or plating. Once the backside processing is finished, the thin device wafer is debonded from the carrier wafer and either put on a film frame or immediately bonded to another device wafer for wafer-to-wafer (W2W) stacking.

This generic process flow must support wafers that have a variety of surface properties and topography. Depending on the wafer topography, the adhesive layer has a thickness in the range of 20-100 $\mu\text{m}$ . Dedicated process modules for coating, baking and wafer bonding ensure that the adhesive film has very low total thickness variation (TTV) after bonding. Adhesive layer non-uniformities would be directly transferred to device wafer thickness non-uniformities after backgrinding.

#### **Tracking and Measuring**

For high-volume manufacturing (HVM), wafer ID tracking is a necessity. However, after temporary bonding, the initial wafer ID is either buried in the bonded interface (in case of wafer ID on device wafer front side) or will be ground away during thinning (in case of wafer ID on device wafer backside). The way to maintain trackability is to link the device wafer ID to the carrier wafer ID within the fab automation software.

Another important feature for HVM implementation is in-line wafer thickness measurement. Modern backgrinding equipment can precisely control wafer thickness, but these tools detect the thickness of the whole wafer stack. To minimize the CoO, low-cost silicon wafers are typically used as carriers. The SEMI standards for wafer thickness are quite loose. Therefore it is necessary to measure the thickness of carrier and device wafer, to calculate the desired final thickness and communicate this thickness via SECS GEM interface to the backgrinding equipment. EV Group manufactures a high volume temporary bonding system that provides modules for coating,

baking, wafer bonding, wafer ID tracking and wafer thickness metrology (Figure 2).

#### **Silicon vs. Glass Carriers**

The described process flow can be used with either glass or silicon carrier wafers. Silicon carriers are 100% compatible with standard equipment, whereas glass carriers can pose issues for electrostatic chucks and can slow

down throughput for some processes due to the lower thermal conductivity of glass. Based on this, silicon carriers provide lower CoO than glass carriers. In the past, glass carrier were recommended for front-to-backside lithography processes. However, due to recent advances on infrared alignment technology there is no longer any difference between glass and silicon carriers.<sup>2</sup>

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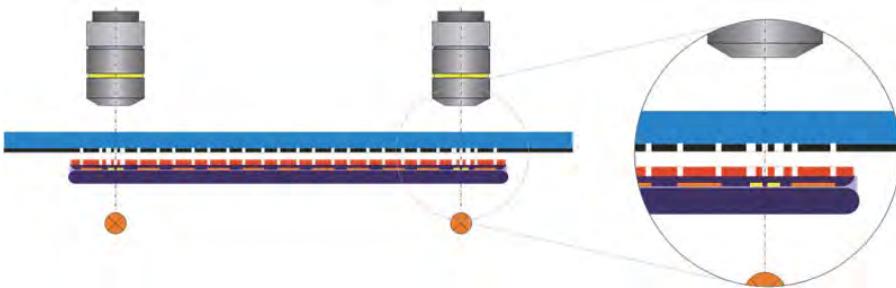


Figure 3. Front-to-backside lithography for a thin device wafer bonded to a carrier wafer. The alignment keys on the device wafer front side are buried in the bond interface. The alignment to the mask is performed with infrared (IR) alignment

## Of material importance

Temporary adhesive must fulfill many different requirements. The material has to work with a variety of surface properties and films. The coating method has to be compatible with high wafer topography and bumps. The material has to be rigid at room temperature for backgrinding, resist high temperatures and typical back-end chemistries, and must not out gas in vacuum. On top of that after all the backside processing is complete the adhesive has to be debondable and cleanable. This list of requirements explains why extensive material and process qualification is so important.

The EMC-3D consortium has qualified an adhesive from Brewer Science Inc. for the complete via-last TSV process.<sup>3</sup> A state-of-the-art CMOS image sensor wafer was used as the test vehicle. The integration of the following process steps was successfully qualified.

- Temporary bonding
- Backgrinding + stress release
- Litho + via etching (Via ratio 2:1)
- TEOS PECVD @ 255°C
- Via metallization (plating)
- BCB passivation
- Backside interconnect creation (solder bumps)
- Debonding + cleaning

Evaluating and assessing the impact of thin wafer technology on device performance is far from trivial. In a joint study, Qualcomm, Amkor, IMEC and EVG investigated the impact of wafer thinning on the transistor performance of a 65nm low power CMOS device. The study concluded that even though the impact of temporary bonding, thinning and debonding resulted in shift for some parameters the overall product performance did not change.<sup>4</sup>

## Debonding is the Cornerstone

The debonding technology is the cornerstone of thin wafer handling.

EVG's production debonding system integrates debonding of the thin wafer, cleaning and film frame mounting within one system. Alternatively the thin wafers can be loaded into coin stacks or put onto single wafer carriers. For thermoplastic adhesives, a slide-off debond process is used. Because it's a thermal release process, slide-off debonding enables both usage of a silicon carrier (as compared to UV debonding which requires glass carriers) as well as non-perforated carriers (compared to solvent debonding). Slide off debonding enables a low-cost carrier – basically a standard silicon wafer. The debonding process itself happens within the adhesive layer, with zero force exerted on the device wafer surface during debonding. After debonding, the residual adhesive layer is cleaned with a single wafer solvent cleaning.

The ability to clean the adhesive after debonding is another key specification for a temporary adhesive. It makes the thin wafer handling solution compatible with undercut bumps in the interface. Mechanical debonding would create significant force on the bump with the risk of ripping the bumps off or leaving residue on the wafer. Slide-off debonding works well for wafers with bumps or pillars on the front- as well as backside of the thin wafer (**Figure 4**).

The limits of thin wafer handling

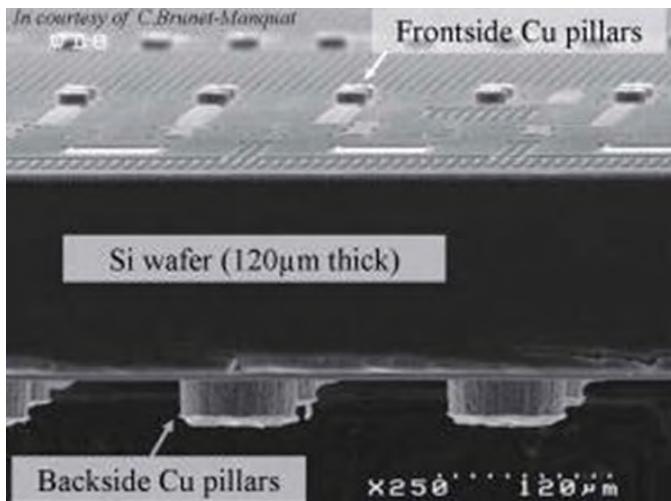


Figure 4. SEM cross section of a 120 μm thin wafer with Cu pillars on the front- and backside.<sup>3</sup>

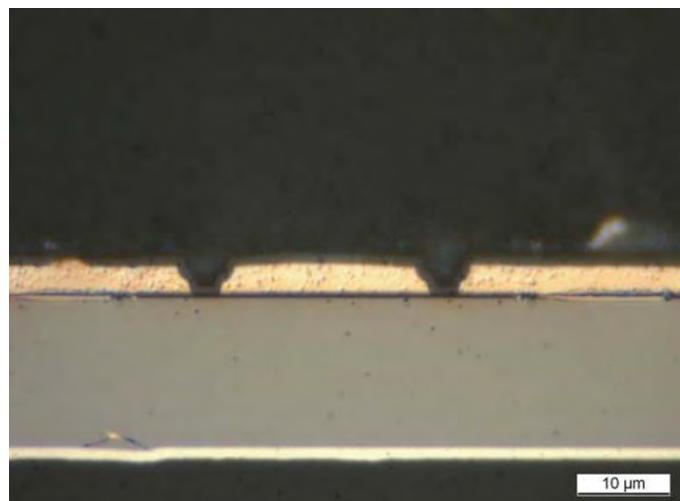


Figure 5. 16 μm thin silicon PowerMOS with 4 μm front side metallization and 2 μm backside metallization<sup>5</sup>

with a rigid carrier have been analyzed in several projects. PowerMOS with wafer thicknesses below 20 $\mu\text{m}$  have been successfully qualified in a project led by Fraunhofer ISIT.<sup>5</sup> **Figure 5** shows a wafer cross-section with 16 $\mu\text{m}$  silicon thickness and a total wafer thickness of 22 $\mu\text{m}$  including top and bottom metallization. M. Duemling et al. took this approach even one step further for the manufacturing of ultrathin RFID devices.<sup>6</sup> The buried oxide layer of a SOI wafer was used as etch stop layer. The entire bulk silicon was removed resulting in a silicon wafer thickness of only 1.5 $\mu\text{m}$  and a total device thickness of only 10 $\mu\text{m}$  including 5.5 $\mu\text{m}$  of interconnects and 3 $\mu\text{m}$  of polyimide layer.

## Summary

In this paper, state-of-the-art thin wafer processing has been reviewed. Adding two process steps, temporary bonding and debonding, enables processing of thin wafers in existing fabs with existing equipment. Materials, process and equipment are closely linked to each other. Temporary bonding/debonding has been successfully qualified for current CMOS devices. 

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*(continued from Page 24)*

about customer requirements, market trends and competitive products, and prioritizing future developments. [[www.vitechnology.com](http://www.vitechnology.com)]

## Joe Midili Honored as Aries Electronics' Rep of the Year

Joe Midili of JMA Inc. was recognized by Aries Electronics' as its 2009 Representative of the Year award after nearly doubling his 2008 sales, reportedly outperforming other members of Aries' representative network for overall sales. Midili, owner and president of the Oceanside, CA-based JMA Inc., has been working with Aries for nearly 14 years. [[www.arieselec.com](http://www.arieselec.com)]



## STATS ChipPAC Honors 2009 Supplier Excellence Award Winners

The recipients of STATS ChipPAC's annual Supplier Excellence Awards were announced May 19, 2010 in Singapore, at the company's annual Supplier Day Celebration. Samsung Electro-Mechanics Co., Ltd, Tanaka Kikinzoku International K.K., and Verigy Ltd. received Best Supplier Awards. Nitto Denko Corp. and Teradyne, Inc. were recognized for Excellence in Service. STATS ChipPAC's Supplier Excellence Awards honor materials and equipment suppliers who provide exemplary services and performance to STATS ChipPAC and its customers by demonstrating excellence in quality, on-time delivery, technology, service, flexibility and cost competitiveness.

Offering his congratulations to the winning companies, Wan Choong Hoe, Executive Vice President and Chief Operating Officer of STATS ChipPAC said, “We would like to recognize those suppliers who have consistently demonstrated a strong level of

collaboration and shared commitment to enable STATS ChipPAC to deliver high quality, cost-effective packaging and test solutions to our customers.” [[www.statschippac.com](http://www.statschippac.com)]

## Fraunhofer ENAS Turns to AltaTech Semiconductor for Precursor Deposition

Silicon stressor materials are used to increase the channel mobility of transistors, enabling higher processing speeds. As called out in the International Technology Roadmap for Semiconductors (ITRS), virtually all of the next-generation precursors required for advanced wafer processing, such as 3D integration, are available only in liquid form. This includes ruthenium (Ru), hafnium (Hf), copper (Cu), and a ternary alloy of germanium, tin and tellurium (GeTeSn).

Therefore for the purpose of depositing these materials on 200 mm wafers, semiconductor and microsystems research organization, Fraunhofer Research Institution for Electronic Nano Systems (Fraunhofer ENAS) in Chemnitz, Germany, turned to Altatech Semiconductors, ordering a AltaCVD system to do the job. The AltaCVD system creates uniform thin films via direct injection of liquid precursors and an advanced flash-vaporization system in processing wafers up to 300 mm.

A previously installed system is being used to deposit diffusion barrier and copper layers for advanced copper damascene interconnects and through-silicon-via (TSV) features.

According to Stefan E. Schulz, who leads back-end-of-line operations at Fraunhofer ENAS, the CVD tool will be used in the development of nanometric thin films to advance the state of semiconductor processing. “The use of liquid-phase precursor injection and evaporation is a key enabling technology for this work,” he explained. Fraunhofer ENAS is scheduled to install the new AltaCVD system in its back-end-of-line (BEOL) cleanroom facility in Chemnitz during the second quarter. Applications support will be provided by Altatech Semiconductor in Berlin. [[www.altatech-sc.com](http://www.altatech-sc.com)]

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- 2009 EXHIBITOR

# Combining Fab and Assembly/Test Clean Rooms for Environmental and Operational Efficiency

By Edwin Feeny, Michael Piscopo, Terry Dalton, and Erwin Estepa [Texas Instruments]

Once Texas Instruments (TI) decided to build a facility that combined a wafer fab clean room with assembly and test (A/T) clean rooms, not even the earthquake potential could deter the construction of the Clark facility in the Philippines. Besides the shaky ground beneath it, building a facility in that region of the world presented numerous challenges, many of which were tied to TI's efforts to achieve several tough environmental and operating efficiency goals to meet our needs, and the needs of our customers.

TI had some important factors in its favor. For example, there was already a facility in Baguio, Philippines, providing a wealth of internal resources to draw from for a construction project of this magnitude. Additionally, the company had been through this exercise a few times before over the last 50 years. Still, every clean room facility is different and the 780,000 sq. ft. Clark building held true to form.

## Deviating from the Norm

It is unusual for TI to combine a wafer-scale packaging fab with its many clean room requirements with an A/T facility that has a different set of must-haves. Benefits to the customer proved to be the overriding factor in this decision. Instead of shipping wafers halfway around the world from a fab facility to an A/T factory, the wafers are moved from one section of the Clark facility to another, saving a tremendous amount of time and expense in shipping and handling. Customers reap the benefits of reduced time-to-market and greater responsiveness from TI.

The Clark project was designed with four manufacturing modules, an administrative wing and another section devoted to the building's mechanical services. (Figure 1) One of the manufacturing modules was dedicated to wafer-level packaging and bumping

processes. Bumping an entire wafer rather than individual die offers significant advantages, such as the elimination of various conventional packaging steps like die bonding, wire bonding and die level flip chip attach.

The other three Clark modules perform assembly, test and probe. Following the bump wafer-scale processes, the wafers are moved across the building to the assembly and test modules where they are diced, packaged and tested for electrical functions and reliability. This is a far cry from the path of some TI chips. A typical round trip for a chip might begin in a wafer fab in Germany before heading to Dallas for chip-scale packaging and test, and then eventually to a plant in Malaysia for assembly. Consolidating some of these processes under one roof improves operations and benefits the customer.

Still, addressing requirements of both a wafer-scale packaging fab and assembly and test in the same facility had its challenges. A wafer fab clean room involves special chemicals, high-purity gases, special exhaust systems, high-purity air

management systems, more sophisticated waste treatment processes and other infrastructure service requirements that an A/T clean room does not. Therefore, designing and building a facility with A/T clean rooms is more straightforward than a facility with fab clean rooms.

## Clean Room Considerations

Several complicated factors were involved in designing and constructing the clean rooms. The wafer fab clean room, which was placed in its own wing of the building, was designed with three levels: the clean room itself, a subfab and a simple air plenum above the clean room.

The lowest level, or subfab, houses the clean room's utilities and other support equipment. The pipes, cables and ducts for the utilities, and support equipment are all strategically placed so that the equipment in the clean room overhead can be rearranged and still have rapid access to all of their required support services. Additionally, special flooring called a waffle table was constructed in the bump clean room itself (Figure 2).

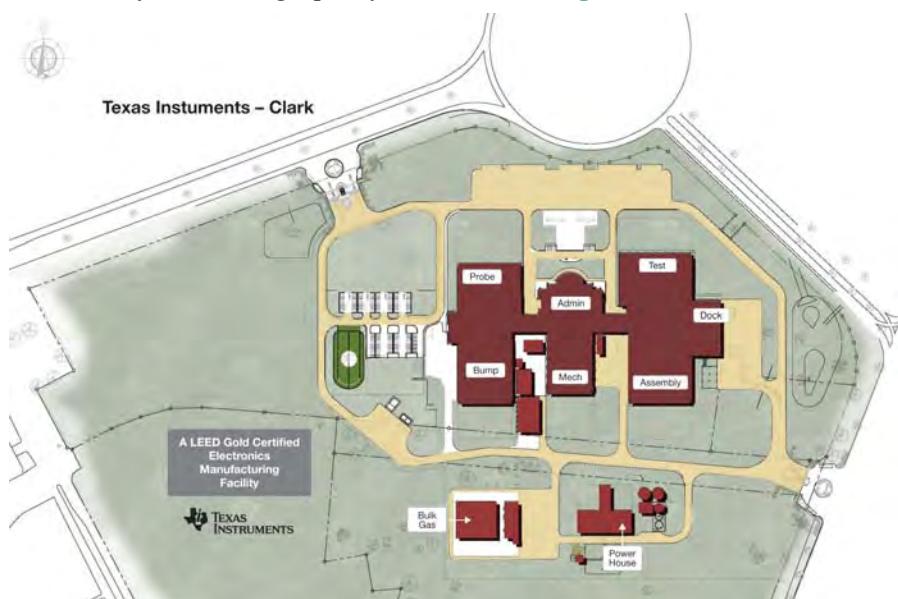


Figure 1. Footprint view of Clark showing modules



Figure 2. Waffle floor table in the clean room



Figure 3. Isolation bearings helps reduce damage from a potential earthquake by 70%

The requirements of a wafer fab clean room are so stringent that air turbulence must be kept to a minimum. The waffle table allows the air in the clean room to flow directly into the subfab with a minimum of turbulence. It also allows for equipment to be installed or moved around the clean room and still have rapid hook-ups to the utilities in the subfab through the holes in the waffle table. The waffle tables' penetrations are circular, rather than the traditional rectangular shape, which improves construction cycle time and reduces costs.

The third level of Clark's bump clean room is a simple air plenum located directly above it. In this plenum, air from the subfab is mixed with air that has been treated and brought in from the outside. This mixture of subfab and outside air is then circulated into the clean room.

All of these items are standard parts of wafer fab clean rooms where spaces are designed to meet certain cleanliness classifications, rated according to the quantity of particles, as small as  $0.5\mu\text{m}$ , measured in the clean room over a certain period of time.

Generally, these classifications are designed into a clean room by varying the amount of ceiling filter coverage. Wafer fabs usually require cleaner environments than A/T clean rooms, which is the case at Clark. The bump wafer fab is Class 1000 while the A/T and probe clean rooms are either Class 10,000 or Class 100,000. The classification requirements are driven by the stage of processing of the product in those spaces and the related risks for

contamination. The closer products get to final state, the less the risk and therefore higher classifications are allowed. For Clark's A/T modules, subfab or air plenum levels were not required because the purity of the environment in these clean rooms was not as demanding as the wafer fab clean room. Accordingly, they require minimal support equipment.

The manufacturing tool mix for the bump manufacturing process included both 200- and 300mm tools to enable wafer scale packaging production and more flexibility for full turn-key production of both analog and digital products of either wafer size. Also, the 300-mm tools have been designed to be flexible for 200mm, allowing maximum asset utilization. These tools are the latest models, providing higher capacity and better process control and include sputter (thin film deposition), resist and polyimide strip, resist and polyimide coater/developer, Cu plating, and wafer back grind tools.

In the end, the installation, configuration and certification of the manufacturing tools in the bump wafer fab clean room went better than was expected due to a great deal of pre-planning and pre-fabrication of utility hook-ups. In fact, most of the utilities were pre-fabricated almost 30 days prior to the arrival of any of the manufacturing tools. In addition, equipment installations average was 3 to 4 per day so that all 97 tools were operational in 30 days — quite an accomplishment for a team of only 10 installation management professionals.

## Feeling the Earth Move

The Clark facility was built in an area with a history of earthquakes. As a result, the design and construction of the building was intended to minimize and protect the facility from any seismic activity. Two approaches to earthquake protection were examined. First, the design of the building could include additional and stronger structural members to withstand the forces of an earthquake, like deeper foundation piers, and a more robust structural skeleton with thicker slab and walls. The second method involved isolation bearings between the foundation and the building itself. The latter technique was chosen, a first for TI.

The Clark facility sits on a single concrete slab with a total of 412 isolation bearings (**Figure 3**) installed between the foundation slab and the building structure. During an earthquake, as the ground shakes, the building structure will slide from side to side as much as 18 inches. In other words, the force of the movement of the earth will be absorbed by the movement of the building across the bearings. These forces will be dissipated as friction at each bearing. Potential damage from an earthquake is estimated to be reduced by as much as 70 %. By absorbing the force of a quake below the structure allows for less damage to the building's internal infrastructure, such as manufacturing tools, facilities equipment and utilities; resulting in a shorter recovery time for the facility.

## Environmentally Friendly

Environment and energy consumption considerations are always a priority for TI when it is designing and constructing a new clean room facility like Clark. In all of its new construction and major upgrades to existing facilities, the company has committed to following the Green Building Rating System known as Leadership in Energy and Environmental Design (LEED). This is an internationally accepted benchmark for the design, construction, and operation of high performance green buildings.

The LEED program provided guidelines and a certification rating system that assures the Clark facility would have a positive and sustainable impact on the ecology of its surrounding region when operational. The LEED guidelines address five key areas: sustainable site development, water savings, energy efficiency, materials selection, and indoor environmental quality. Rather than settle for the minimum level of LEED certification, TI strived for and recently achieved the more demanding ‘gold’ level of certification. Practically all aspects of the Clark facility’s design and construction were affected by the requirements of the Gold LEED certification guidelines, including the following examples.

**Warmer water, lower energy costs:** To improve the energy efficiency of Clark and achieve a sustainable level of overall energy consumption, the efficiency of the facility’s cooling plant was improved. Typically, a factory of this size would be cooled by a chilled water system. Most of these systems maintain the temperature of the chilled water at around 44 ° F. As hot air from inside the plant is expelled as exhaust, fresh air from the environment is brought in, cooled and dehumidified by the chilled air system.

The Clark facility features innovative desiccant wheel technology to improve the efficiency of the dehumidification process. As a result, the water temperature in the chilled water system can be higher than the normal 44 °F. We have been able to increase the temperature of the chilled water at Clark to 50 °F, resulting in energy savings of \$1.50 per cubic feet per minute (CFM). Given the size and complexity of the Clark facility, the energy savings over the course of a year is tremendous.

**‘Green’ starts at the top:** Even though the roof over the Clark facility’s administrative wing is small in comparison to the rest of the building, it is emblematic of what was trying to be achieved with regards to the LEED gold certification. The surface is literally green grass (**Figure 3**), creating a “living roof” that promotes energy savings and

reduces soil erosion around the facility. Instead of heating up in the midday like conventional materials would, the grass surface absorbs and dissipates the sun’s heat. As a result, the office space beneath the roof is kept cooler and less energy is consumed by air conditioning. In addition, the grass and soil roof absorbs much of the rainfall into the grass which

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Figure 4. This "living roof" promotes energy savings and reduces soil erosion

helps reduce soil erosion around the building and its grounds. Additionally, several detention ponds are situated on the Clark grounds to collect water runoff from the rest of the site and to prevent soil erosion that would result from rapid rain water runoff.

Many aspects of the Clark facility contributed to its Gold LEED certification. Other contributing factors included low-purge compressed air

dryers which save \$250,000 per year in reduced power consumption, a water re-use system that collects waste water and re-uses it for irrigation, cooling and exhaust scrubbers, and a daylight lighting scheme that reduces power consumption.

### Local hurdles

Designing and building a complex fab and A/T facility 13 time zones removed from our headquarters would be a challenge for any company, but leveraging previous operational experience in the Philippines helped TI address the hurdles.

Good relations with local and national governmental entities are always critical. Thirty years in the country allowed for these relationships to be firmly developed

before breaking ground for Clark. A list of reliable local suppliers and contractors is also imperative. Fortunately, we were able to draw on the experience of TI's other facility in the Philippines, the Baguio factory, to fill out this list. Lastly supplementing the local TI Philippines technical experts with an international support team was instrumental in keeping the Clark project on schedule as we leveraged a team of offshore experts to help train the local work force and make the new facility operational.

### Delivering the goods

Of course, any complex construction project that stretches over 22 months has its bumps in the road along the way to completion. The Clark facility was no exception. But the ingenuity, resourcefulness, perseverance and dedication of all the people involved contributed to this project being completed on time with best-in-class operational and environmental efficiency. ☀

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# Disposable Solder Paste Properties for Die-attach in Power Electronics

By Albert Heilmann [WC Heraeus GmbH]

The solder joint in power electronics packages, in particular “clip-attach” with soldered copper bridges, is realized with dispensable solder pastes. Aside from typical characteristics expected from a good solder paste – such as good wetting behavior, low void rate, solder joint reliability, and good cleanability – rheological characteristics that ensure a perfect and reliable application of the pastes are of particular importance. Solder pastes syringes, filled and bubble-free, should not separate or change viscosity during shipment, storage, and dispensing process. Even over a long period of process time, a constant dosing of solder paste should be dispensed, and the dispense tool itself should not clog.

These high requirements are necessary in the formulation of the fluxing agent to maintain stability in storage and workability of the solder paste.

## Requirements for flux formulation

Solder pastes consist of solder powder dispersed in a fluxing agent. A fluxing

agent (or flux vehicle) must fulfill several tasks simultaneously, which makes it a complicated material. First it serves as a carrier into which the solder powder is dispersed, and is applied by means of dispensing (or in rare cases by means of pin transfer or screen printing) on the leadframe. It also protects the specific powder surface against oxidation.

The typical sequence of steps in the production of a power transistor is schematically represented in **Figure 1**:

During the soldering process, the fluxing agent must remove the oxides on the surface of the parts and on the solder powder surface to generate a good wetting on substrate and package and form intermetallic phases.<sup>1</sup> The individual formulation's activation temperature must therefore be adapted to the temperature-time profile particular to the solder alloy.

Typically, a fluxing agent consists of solvents (for fluidity adjustment), in which resins (like rosins, or hydrogenated resins), activators, and thixotropic-agents are dissolved. The acid number of the

resin essentially describes the strength of the activation. Natural resins consist of considerable amounts of carbon acids, carbon acid esters, anhydrides and fatty acids. The main components are generally abietic acids, primaric acids and their derivatives.<sup>2</sup>

To increase activation, substances such as acids (e.g. stearic acid, lactic acid, glow amine acid), amines (e.g. dimethylamin, urea, ethyl diamine, tri ethanol amine), or halogen salts (e.g. zinc chloride, ammonium chloride) can be added.<sup>3</sup>

Classification typically goes according to the kind (and/or the degree) of the activation and is fixed in the DIN EN 29454 Table 1, “Organization of solder fluxing agents” based on their main parts.<sup>4</sup> For example:

1.1.3.C: 1 resin; 1 rosin; 3 activated without halogens; C paste

2.1.2.C: 2 organics; 1 water-soluble; 2 activated with halogens; C paste

Since a variety of pastes are also used in the American hemisphere, the fluxing agents in the solder pastes are also frequently classified by the IPC J-STD-004.5

For example:

ROL1: Rosin low activated (< 0.5% Halide)

REMO: Resin moderate activated (0% Halide)

ORM1: Organic moderate activated (0.5-2% Halide)

Rosin-containing fluxing agents form residues that are washable with organic solvents. Water soluble (WS) residues and no-clean fluxing agent residues do not have to be removed because they are not corrosive, do not form an electrically leading layer, and do not negatively affect molding.

## Storage Stability

Flux agent formulation must be optimized to avoid powder sedimentation so that the paste does not separate.

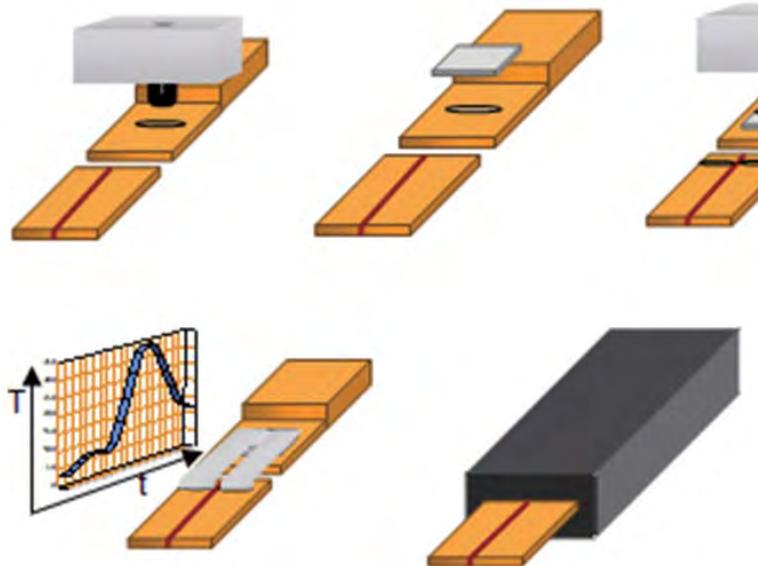


Figure 1. a) Dispensing of a bond pad; b) placement of die; c) dispensing of die and leads; d) placement of clips; e) inline soldering; f) molding

Thixotropic agents are an important factor in this case.

Frozen storage and dispatch are generally recommended, especially for syringes with small needle diameters, because the dispense process often takes several hours at ambient temperature with a high number of pressure-time cycles. This is a serious condition for a solder paste disperse system, and for this reason alone, the solder paste in the syringe must not be able to separate for 24 hours at ambient temperature and perpendicular storage (opening downwards). Good formulations of solder paste fluxing agent are storable for at least 50 hours at ambient temperature.

Furthermore, frozen storage and dispatch is important to prevent paste viscosity change. Freezing also keeps the piston in the syringe from moving to the rear during transport because of vibrations and shock. Due to the compressibility of air in front of the piston, this can lead to paste dripping or variations in the dosing quantity.

## Processability

For volume production in the electronic industry, continuous workability means continuously high throughput in the first place (assuming otherwise identical product characteristics). Rheological characteristics of the paste determine its workability, and through vehicle (fluxing agent) interaction with the type of powder (particle size), the size

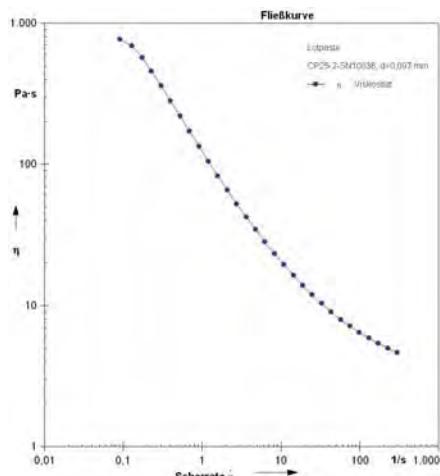


Figure 2. Rotator flow-curve measurement of a solder paste

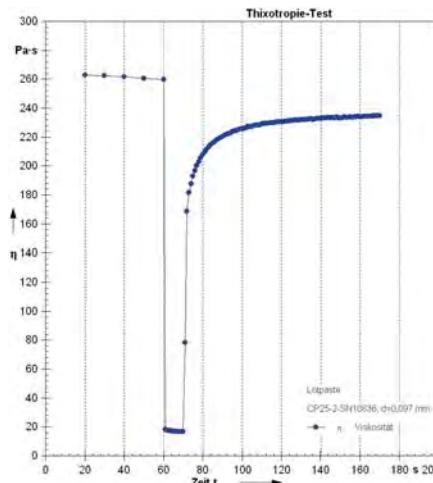


Figure 3. Rotator thixotropic test of a solder paste distribution and metal content (filling degree of the dispersion) is fixed.

A simple way to characterize pastes is with viscometers — which measure the viscosity relative to one of a standard medium — based on spiral pumps (Malcom) or spindles (e.g. T-spindle; Brookfield). Here, a static viscosity value that corresponds to a constant shearing of the paste material is usually indicated. The actual rheological load of the material is not well-known, as mathematical models can only approximately simulate the conditions.<sup>6</sup> (Figure 2)

Multi-range measurements like the so-called “thixotropy test” are also possible. The viscosity is determined in a sequence of 3 loads (Figure 3):

1. Range: constant small shearing, e.g.  $0.1\text{s}^{-1}$
2. Range: constant high shearing, e.g.  $100\text{s}^{-1}$ , destruction of the internal structure
3. Range: constant small shearing as within the 1st range, high measuring point density, pointing out the structural recovery.

Within the first range (from 20 - 60s), the initial viscosity with small shear-values ( $0.1\text{s}^{-1}$ ) are measured. Within the second range (from 60 - 70 s), the internal structure is destroyed with large shear-value ( $100\text{s}^{-1}$ ) and within the third range (from 70 - 170 s with small shear-value) the structural recovery is noted again. The faster the structural build up takes place (i.e. the greater the thixotropy), the smaller the risk of separation.

Furthermore, apart from such measurements with a Rheometer, axletree measurements are also possible and characterize the visco-elastic

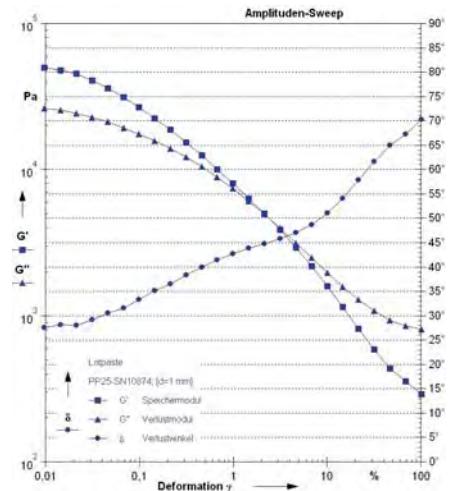


Figure 4. Axletree amplitude sweep of a solder paste

properties of the pasty material. A purely plastic solid offers the largest resistance against a reciprocating deformation at the points of oscillation reversal (according to Hook's law, which states that the largest deflection = largest resetting force). One purely viscose liquid offers the largest resistance in the zero crossover of the oscillation (largest shear-value). Thus the phase angle (loss angle)  $\alpha$  of the complex shear modulus  $G^*$ , which consists of flexible shear modulus  $G'$  (memory modulus) and viscous shear modulus  $G''$  (loss modulus), is between  $0^\circ$  (purely elastic) and  $90^\circ$  (purely viscous).

By means of “amplitude sweep” the yield point of a viscoelastic material can be accurately self-determined. For very low amplitudes, the internal structure is not affected; the memory modulus is larger than the loss modulus. With increased amplitude (shear-value with constant frequency) the internal structure is increasingly disturbed and the value of the memory modulus falls under that of the loss modulus. This “crossover” as a characteristic point is optimally suitable for defining a yield point. This point represents the transition of a visco-elastic gel or solid body to a visco-elastic liquid (Figure 4).

Another axletree measuring methodology is “frequency sweep” (Figure 5). By extrapolating the curves of the two modules  $G'$  and  $G''$  to small frequencies, the storage stability can be forecasted. If the curve of the loss modulus with decreasing frequency (corresponds to

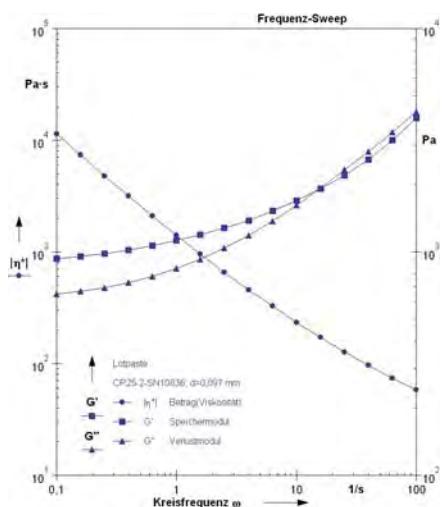


Figure 5. Axletree frequency sweep measurement of a solder paste

longer time interval) rises clearly over those of the memory modulus, then in longer storage times, a sedimentation of the dispersed particles (separation) can be expected.

Thus, good workability means good dispensing behavior, using dispense heads with several openings (so-called "showerheads") until the syringe is emptied without clogging (by separation as consequence of the pressure-time-cycles, or by plating of solder powder particles during the filling up process). Additionally, the applied quantity of the solder paste must remain constant. Bubbles, or micro blisters, are particularly critical here. To compensate for the mechanical stresses caused by false fit of the coefficient of thermal expansion (CTE), a minimum solder layer thickness (bond line thickness) of e.g. 50 $\mu\text{m}$  with 12 x 12mm chips is necessary. A too-small dosing quantity causing a too-thin solder layer endangers package reliability.

## Summary

This article shows that dispensable solder pastes for die-attach applications have substantial differences than solder pastes used for printing applications because of different processing requirements. The rheologic characteristics must be accurately adapted to these requirements. Future die-attach solder pastes should be as residue - free as possible with the same rheologic, processing and soldering characteristics to reduce costs of complex cleaning methods.

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# Next Generation Embedded Wafer-Level BGA (eWLB) Technology

By Seung Wook Yoon, Yaojian Lin [STATS ChipPAC Ltd], V.P. Ganesh, A. Bahr [Infineon Technologies Asia Pacific Pte Ltd], Yonggang Jin, X. Baraton [STMicroelectronics], Pandi Chelvam Marimuthu and Raj Pandse [STATS ChipPAC Inc.]

Integrated circuits (ICs) fabricated on silicon are assembled in different forms of electronic packages and used extensively in electronic products such as personal, portable, healthcare, entertainment, industrial, automotive, environmental and security systems. Current and future demands for increased performance, reduced power consumption, and reliable systems at a reasonable price are met through advanced/appropriate silicon process technology, innovative packaging solutions with use of chip-package-system co-design, low cost materials, advanced assembly and reliable interconnect technologies. This article examines packaging evolution for hand held applications, focusing on next-generation chip embedding technology called embedded wafer-level ball grid array (eWLB).

eWLB offers additional space for routing higher I/O chips on top of silicon chip area that is not possible with conventional WLP or WLB.<sup>1</sup> It also offers improved electrical, thermal, and reliability performance at reduced cost, with the possibility for decreasing technology nodes with low-k dielectrics in SoC (more Moore); and heterogeneous integration of chips with different wafer technology as a system-in-package (SiP) solution in multi-die or 3D eWLB approaches (More than Moore).

This technology combines front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market.<sup>2</sup>

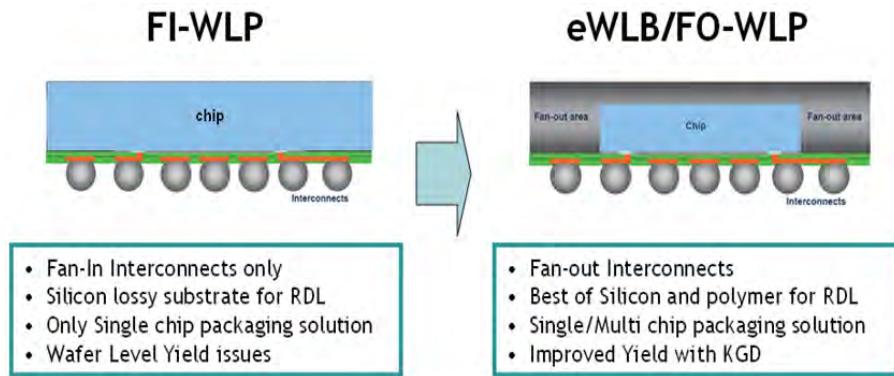


Figure 1. Comparison of FI-WLP and eWLB (FO-WLP)

## eWLB Technology

eWLB technology addresses a wide range of factors. At one end of the spectrum is the packaging with testing costs. Alongside these are physical constraints such as footprint and height. Other parameters considered during development included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency).

eWLB is a fan-out process (Figure 2). The die is surrounded by a suitable material, which spreads the package footprint outside the die. Known good die (KGD) are embedded in an artificial plastic wafer (reconstituted wafer) using a wafer level molding technique. Front end isolation and metallization processes are then used to fan-out the interconnections to the surrounding area with lithography and patterning wafer level processes. Solder balls are applied and parallel testing is performed on wafer. The reconstituted wafer is then sawn into individual units, which are packed and shipped. With the fan-in approach, the number of interconnects and their pitch must

be adapted to the chip's size. eWLB, by contrast, supports a fan out area that is adaptable and has no ball pitch restriction.

## Advantage of eWLB

The advantage of eWLB packaging can be summarized as follows:

- No substrate required
- Miniaturized and high-performance package
- Green packaging (Pb-free and Halogen-free)
- Cu/low-k/ELK compatible packaging technology
- Full module approach with free top surface (thin package-on-package (PoP), SMD compatible)
- Wafer-level batch process including wafer level test

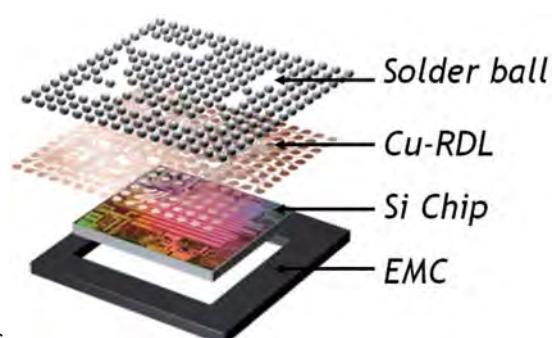


Figure 2. Schematics of construction of eWLB

- Simple logistics and supply chain
- Enabling 3D IC packaging

The current BGA package technology is limited by the organic substrate capability. Moving to eWLB helps overcome such limitations and simplifies the supply chain. Building the substrate on the package itself allows for higher integration and routing density with fewer metal layers. eWLB is a next-generation platform that supports future integration, particularly for wireless devices, and has a number of important features. Transition to eWLB packaging technology enables a significant reduction in recurring costs by eliminating the need for expensive substrates.

BGA packaging also faces a challenge with technology nodes beyond 65nm as the device performance density drives the need for flip chip. But advanced flip chip nodes drive fine pitch combined with weaker low-k dielectric structures resulting in flip chip becoming narrower in terms of process margin. In addition, there is a trend towards being environmentally friendly, driving lead-free and halogen-free, or green, material sets.

### Next-Generation; 3D eWLB Technology

The first generation of eWLB technology was designed for a single side and 1-RDL approach. To address advanced requirements in the market for higher performance and design complexity, new technical items and envelopes should be developed and implemented into the current eWLB technology as shown 6 areas:

#### 1. Multi-layer RDL eWLB packaging

In situations where a device has an interconnect pad arrangement or flip chip or wafer level component, an additional layer of lateral connections may be used to rearrange the connections in a manner suitable for wafer level processing. While RDL is intended for higher electrical performance and complex routing, it also can provide embedded passives (R, L, C) using a multi-layer structure. Further improvement of the integrated capacitors' quality factor by using low-loss thin-film dielectrics on eWLB was also reported.<sup>5</sup> Additionally, a 77 GHz SiGe mixer



Figure 3. SEM micrograph of cross-section of 2 layer RDL eWLB

packaged as an eWLB reportedly had excellent high frequency electrical performance due to short signal pathways which decreased parasitic effects.<sup>6</sup>

#### 2. Thin eWLB packaging

For mobile and handheld applications, portability is a critical factor for product selection. A thinner package provides better board level reliability and a lighter, thinner profile at the system level. Using advanced thinning technologies, eWLB was successfully thinned down to 250 µm thickness. Handling the thin wafer and grinding and removing of Si/epoxy material together using the same process steps were the critical technical challenges. There was in excess of 60% increase recorded in temperature Cycle

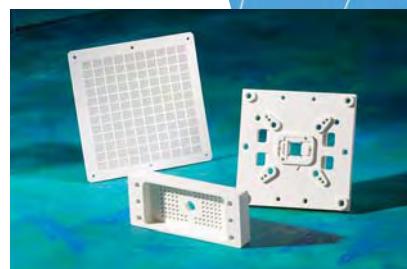
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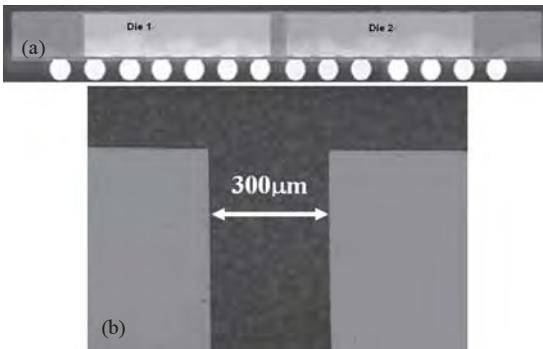


Figure 4. (a) Cross section of 2-die multichip eWLB and (b) SEM micrograph of cross-section of completed mold filling between two chips

on Board (TCoB) performance with thinner eWLB. Drop reliability also improved significantly.

### 3. Multi-chip eWLB packaging

Side-by-side multichip packaging provides more design flexibility for SiP applications because a chip designer has more freedom in pad location as well as circuit block allocation. 3D eWLB technology utilizes very fine-pitch metal line width and space as well as multi-layer RDL processes. It can be used for various

combinations such as RF receiver and digital device, PA (power amplifier) and IPD (integrated passive devices) and memory and controller. eWLB's fine-pitch metallization and well-controlled interconnections with wafer fab lithography processes result in improved electrical performance as compared to wirebonding and organic substrate technology.

### 4. Extra Large(XL) eWLB packaging

FI-WLP is limited to a size of ~5 x 5mm due to board level reliability (BLR) requirements. First gen, 8 x 8mm eWLB successfully passed industry BLR standard tests. Currently, process, assembly and board-level reliability of large-size eWLB up to 12 x 12mm is being studied. So far, XL eWLB passed the drop reliability test. To improve further TCoB reliability, various design, processes, and materials approaches are being explored through computational



Figure 5. SAM (Scanning Acoustic Microscopy) picture of 12x12mm XL eWLB with 3-die multichip eWLB

simulation. With optimized design works, XL eWLB successfully passed TCoB 500 cycles (-40/125C 2cycles/hr.).

### 6. Double-side eWLB packaging

One 3D eWLB approach involves vertical interconnections, in which both sides of the reconstituted wafer has isolation and metal layers, connected using conductive vias. It enables 3D SiP or 3D micro modules. eWLB takes the

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next step, eliminating the PCB and wirebonding or flip-chip bumps to establish electrical contacts. Without a PCB the package is inherently thinner without thinning the die when lower profiles are required. eWLB, therefore has the potential to improve cost effectiveness and reduce entire systems to the size of a postage stamp.

PoP and SOW takes this integration a step further, placing one package on top of another for greater integration complexity and interconnect density (**Figure 6**). eWLB makes it a very flexible choice, and also offers procurement flexibility, lower cost-of-ownership, better total system and solution costs and faster time to market.

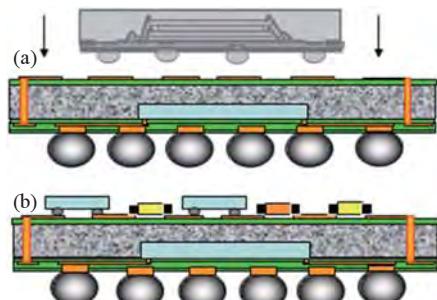


Figure 6. Applications of double-side eWLB packaging; (a) Package-on-Package (PoP) and (b) System-on-Wafer (SOW)

## 7. Large Carrier approach

One challenge and obstacle of a new technology is the cost in early stages of introduction and market penetration. To fabricate more units in one carrier is the most effective production solution. eWLB is moving to production in 300mm sizes, resulting in >2 x units compared to 200mm. There is currently work being done on large panel eWLB with square or rectangular sizes, which can save dead space experienced in circular carrier form and higher units.

## 3D eWLB Package Level Reliability Results

**Table 1** shows the package level reliability result of each next-generation 3D eWLB packages, which have passed JEDEC standard package reliability tests such as moisture sensitivity (MSL) 1 with Pb-free solder conditions. Test vehicles have 8 x 8mm package with 5 x 5mm daisy chain die and 0.5mm pitch. Total ball I/O is 192 and lead-free solder

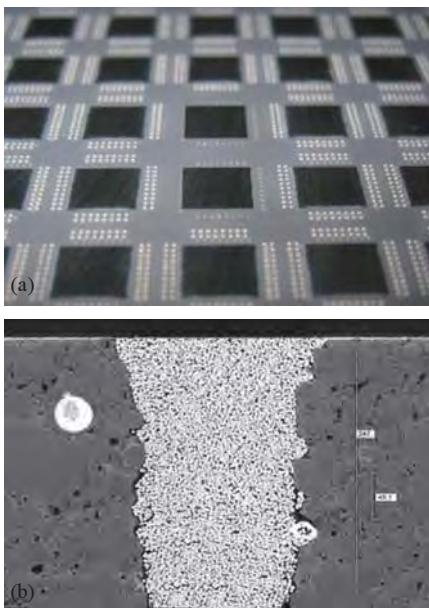


Figure 7. Applications of double-side eWLB packaging; (a) Package-on-Package (PoP) and (b) System-on-Wafer (SOW)

balls are used. All next-generation eWLB packages successfully passed industry standard package level reliability with ball shear tests and OS (open-short) tests.

## 3D eWLB Board Level Reliability Results

For board reliability, next-generation eWLB packages show good TCoB reliability as reported in 1st gen eWLB. **Figure 8** shows a Weibull plot of next-generation eWLB packages as consolidated data. It shows quite comparable TCoB results even for 12 x 12mm XL eWLB. There is continuing work and study to improve board level reliability of large size eWLB packages.

Condition	Status
MSL1 MSL1, 260C - Pass	
JEDEC-J-STD-020D Reflow (3x)	
Temperature Cycling -55C to 125C 1000x Pass	
(TC) after Precon	
JESD22-A104	
HAST (w/o bias) 130C / 85% RH 96hrs Pass	
after Precon	
JESD22-A118	
HighTemperature 150C 1000h Pass	
Storage (HTS)	
JESD22-A103	
BST after 260C Reflow 20x Pass	
Multiple Reflow	

\* Tested by ball shear test and O/S test

Table 1. Package Level Reliability Results of next generation eWLB packages

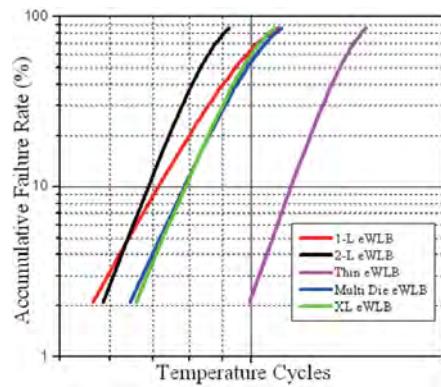


Figure 8. Weibull Plot of TCoB reliability of next generation eWLB Packages

## Further wafer level integration with 3D eWLB for heterogeneous functionality

There is a need for miniaturization at the IC, module (or sub-system), and system levels. At the IC level, scaling continues as it has over the last four decades according to Moore's Law. In addition, 3D chip stacking with TSVs has garnered attention due to its potential in improving the performance, form factor, cost, and reliability at the sub-system or module level.<sup>7,8</sup> There is still a great deal of research and development required to bring this hetero-integration technology to cost-effective implementation with the required reliability and performance needs. In addition to the module level, it needs to focus on performance, form factor, cost, and reliability of the entire system.<sup>9</sup>

Although active and stacked ICs are a highly functional and important component of the overall system, they are only one set of components; many other components including other actives, passives, power systems, wiring, and connectors must be considered in a complete system. As a result, there is a need to think at module and system levels and this need is largely met by the current technology domain in the areas of TSVs, 3D stacking, and WLP. There should be further study on integration, focusing on TSVs, 3D stacking and 3D eWLB with better electrical and thermal performance, greater system reliability, and reduced form factor and overall cost. It will go far beyond this to realize a truly seamless wafer level integrated 3D packaging module that will incorporate aspects of 3D stacking, as well as Si

(continued on Page 54)

# SEMICON WEST SHOWCASE

## Auto Gapping System

At SEMICON West 2010, CyberOptics will showcase WaferSense AGS 300, the latest addition to its WaferSense family that also includes the Airborne Particle Sensor, Auto Leveling System, Auto Vibration System and Auto Teach System. The AGS 300 measures critical gaps such as thin-film deposition, sputtering and etch, allowing engineers to better control gap uniformity and magnitude with high stability over time.

Consisting of three capacitive distance sensors, the system measures gaps between shower heads and pedestals at three points that define a plane to ensure accurate and reproducible equipment setups. It provides wireless measurements

with reported first film check rates to over 99% accuracy. Its wafer-like design and height of only

7.7mm also allows for automatic handling to speed equipment set ups, maintenance and troubleshooting. In addition, the wireless method is repeatable and gives engineers data to optimize preventive maintenance schedules and process controls.

Data can be displayed on a laptop or PC in real-time so that gaps can be quickly adjusted, reducing tool calibration time. Readings can be logged so that the same gap is set across all of tools. **Booth 911** [[www.cyberopticssemi.com](http://www.cyberopticssemi.com)]

## Homogenous Probes

Interconnect Devices Inc. (IDI) announces the development of the



Homogeneous Probe Series, which will be showcased at SEMICON West 2010. This probe series features device contact tips made from a custom developed solid precious metal alloy that is usable

without plating and reportedly offers better hardness and less wear than beryllium copper. Additionally, it reportedly demonstrates electrical conductivity superior to that of carbon steel. The probe's construction methods protect them from the effects of wear and allows them to withstand heavy cleaning. A drop-in replacement for standard IDI (Antares and Synergetix) probes, this probe series is available for all pitches 0.4mm and higher. **Booth 5978** [[www.idinet.com](http://www.idinet.com)]

## Wafer-level Cleaning Solution

At SEMICON West 2010, Kyzen Corp. will feature MICRONOX®MX2302 wafer-level cleaning solution. This engineered semi-aqueous solvent blend is designed to remove difficult flux and paste



residues including lead-free, rosin, no-clean, and tacky flux from wafer bumps found in flip chip, chip scale and µBGA packages. MX2302 accommodates ultrasonic, centrifugal and semi-aqueous spray under immersion cleaning systems. MX2302 is reportedly compatible with all soldering materials, passivation layers (PI, Nitride, Silicon Dioxide, BCB, etc.) and metal layers. **Booth 6356** [[www.kyzen.com](http://www.kyzen.com)]

## AOI System for Camera Modules

VI Technologies will introduce The REVEAL Imagers Series at SEMICON West 2010. Developed with camera module assembly applications in mind, this AOI system optimizes the costs related to assembled materials and process steps by targeting only known good die (KGD). The automated optical inspection accuracy and repeatability levels make for efficient replacement and improvement over manual inspection. AOI capabilities for foreign materials



and process defects ensure the selection of KGD while enabling exact positioning of the image sensor to improve lens-attach process yields.

Designed with a granite-based gantry for stability, REVEAL Imagers Series features high-accuracy axes and a sub-micron pixel size. It detects any foreign material sized above 1-2µm, and checks for process defects such as striations, stain, or watermark. Additionally, it detects defects on naked or glass-capped TSV sensors. Inspection can be performed at pixel level or at the top or bottom sides of the capping glass material for maximum quality.

This turnkey solution allows for either standalone or integrated in-line use with customized handling equipment, and adapts to any products type and size as well as any carriers' kind such as stiffeners, PCBs or strips. **Booth 5377** [[www.vitechnology.com](http://www.vitechnology.com)]

## Sub-micron Bonder

FINETECH will showcase its sub-micron Bonder, FINEPLACER Lambda. This versatile system can be used for precise placement, die-attach and advanced packaging utilizing various bonding technologies — soldering (Eutectic, Au/Sn, Indium), thermo compression, thermo-ultrasonic bonding, adhesives, and curing. It is ideal for low-volume, prototyping and R&D environments requiring precision, advanced technologies and the highest

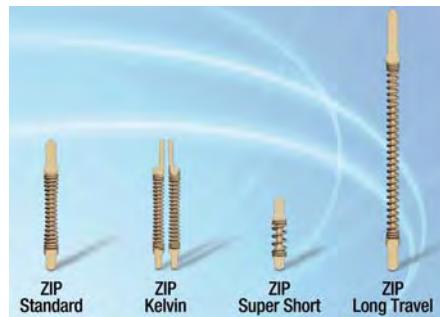


bonding placement accuracy (down to  $\pm 0.5\mu\text{m}$ ).

Applications include flip chip, 3-D packaging, MEMS, wafer level packaging (W2W, C2W), optoelectronic and micro optics bonding and assembly, sensors and more. The system handles component sizes from 0.15mm to 60mm and special tools allow object sizes down to  $5\mu\text{m}$ . **Booth 5570** [[www.finetechusa.com](http://www.finetechusa.com).]

## Contact Technology for Test and Burn-in

Ironwood Electronics will showcase a contact solution for engineering, burn-in and test applications. The XBT product line utilizes a unique contact technology comprising a three-part system that includes top plunger, bottom plunger, and a spring. The brass plungers are machined, plated and assembled to a stainless steel gold plated spring inside a high temperature plastic cavity eliminating the need for an external shell or barrel. A clamshell lid with a wave



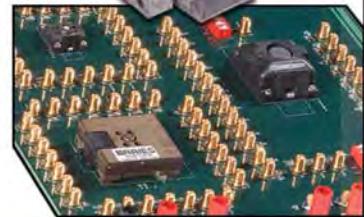
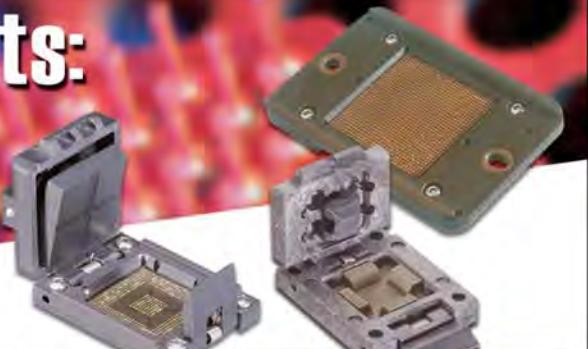
spring provides the compression force on the device to make contact with XBT pins. This mechanism provides easy chip replacement and compatible with the automated handler system also. **Booth 5383** [[www.ironwoodelectronics.com](http://www.ironwoodelectronics.com)]

from 0.8mm down to 0.2mm center spacing. The ZIP SCRUB pin features a positive “scrub-action” pad and ball contact on lead-free plated array and peripheral devices where solder transfer causes frequent cleaning and maintenance cycles. ZIP KELVIN is intended for voltage sensitive device tests on array or peripheral devices requiring sub-1 ohm resistance measurements typical in RDSON and high-power applications. The SUPER SHORT is designed for 0.5nH low impedance, high frequency testing. The ZIP LongTravel, with an OAL up to 6.7mm, was developed for

## "Flat" Technology Pogo Pins

ECT's Contact Products Group's display at SEMICON West will feature the expanded line of its ZIP™ family, “flat” technology Pogo pins, available in pitches

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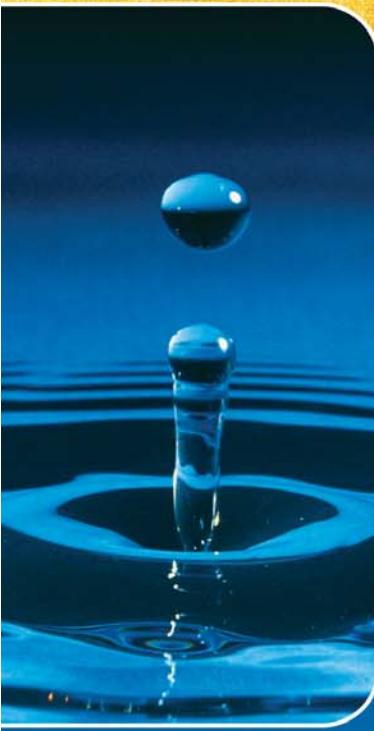
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contacting large devices and strip test where planarity and compliance are an issue. The Z8 is suited for burn-in applications, and combines the performance features of the standard ZIP in a “burn-in-price-point” replaceable compliant pin. The ZIP patented 2-D design features planar contact surfaces fabricated by a unique manufacturing process, delivering performance and cost advantages. **Booth 5870** [[www.ect.com](http://www.ect.com)]

### Full Wafer Test System

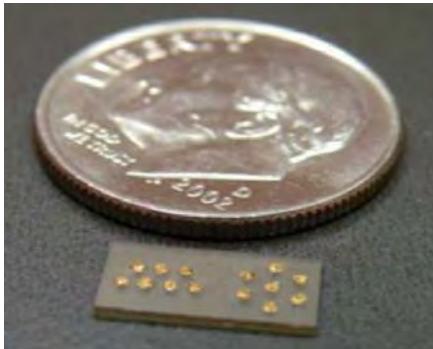
Aehr Test Systems' full wafer 300 mm contactors for its FOX-1 full wafer test systems feature more than 50,000 probe pins and can test an entire wafer with a



single touchdown. This results in higher throughput than the standard testing methodology of stepping across a wafer. Intended to test industry-standard memories such as FLASH and DRAMs, the FOX-1 is optimized to test memory or logic ICs that incorporate design for testability (DFT) or built-in self-test (BIST). **Booth 5756** [[www.aehr.com](http://www.aehr.com)]

### Board-to-board Interposer

To accommodate the challenges of high-density PCB stacking, Custom Interconnects introduces the Thinnerposer, reportedly the thinnest compliant board-to-board interposer available. Targeting



the RF design community for applications such as UAV/UAS, avionics, radar arrays, space probes, and orbital satellites, which are said to be a natural fit for the technology's flexibility, impedance matching, and shock/vibration attributes. Custom Interconnects' general manager, Edward Petsuch explains that the Thinnerposer exploits the potential of the company's core technology, including low signal distortion, robustness, and reliability, allowing them to meet the demands of even the most stringent specification requirements. [[www.custominterconnects.com](http://www.custominterconnects.com)]

### Thermal Conductive Adhesive

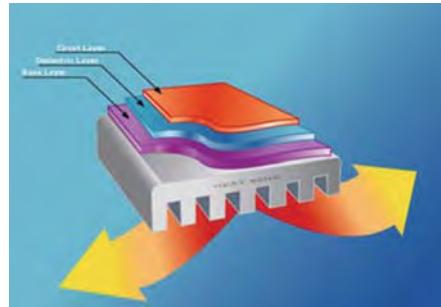
Created in response to a market need for a more flexible, high thermal conductivity adhesive, LORD Corp. introduces MT 815, first in a series of low modulus, thermal conductivity adhesives that can be used as a thermal adhesive for large die, in die attach applications, or as a solder replacement. MT-815 has a modulus of <1 GPa, allowing it to be more flexible and therefore less likely to crack or delaminate under the stresses of temperature cycles. It was formulated to achieve thermal conductivity of >10 W/m-K, establishing a new class of flexible adhesives with high thermal conductivity.

Sarah Paisner, staff scientist for Thermal Management Technology at LORD says "This thermal conductive adhesive combines the advantages of high adhesion and thermal conductivity with the need for lower modulus to accommodate the large stresses experienced by electronic packages." [[www.lord.com/electronics](http://www.lord.com/electronics).]

### Insulated Metal Substrates

AIT's next-generation Cool Clad Insulated Metal Substrates were created to meet the demands industries requiring high-performance circuit substrates, such as high power LED markets. A cost effective thermal design is critical to create a competitive products with a long usable life.

AIT's insulated metal substrate uses an advanced dielectric layer with high temperature stability with a maximum operating temperature of over 300° C;



thermal conductivity of 2.8W/m-k; dielectric strength of 750 V/mil; custom thickness down to 1/2 mil; and matched CTE for reliability after extensive temperature cycling. AIT provides this dielectric on an aluminum heat spreading base plate with custom copper circuit layer thicknesses. [[www.aitechnology.com](http://www.aitechnology.com)]

### Multi-site Testing for High Pin Count Devices

For high pin count devices, the capability of multi-site testing is limited by the required contacting force. In addition, there are complex, integrated ICs with an extremely high pin count for which even single site testing is critical because of too little contact force. Multitest's tri-temp pick-and-place handler, MT9510XP, now offers an option said to substantially increase the contact force, enabling users to test high-pin-count devices in up to eight contact sites in parallel.



Typically, for standard contacting a minimum contact force per pin is required. The new pressure booster option doubles the overall force available, allowing for simultaneous contact on twice as many pins. Overall configuration of the MT9510 remains unchanged for a significant benefit in equipment utilization, return on investment, and cost of test. The new pressure booster option is available for all MT9510 models and can be effortlessly retrofitted in the field. [[www.multitest.com](http://www.multitest.com)]

# EMERGING TRENDS



## ECTC 2010: Plenary Sessions in Review

By Sandra Winkler, Senior Analyst [*New Venture Research, www.newventureresearch.com*]

Once again, this year's ECTC (Electronics Components Technology Conference) didn't disappoint. Hot topics included stacking with through silicon vias (TSVs) / 3D integration, non conductive film (NCF) and non conductive paste (NCP), embedded die solutions to create a SiP, and flip chip and interconnection. Evenings were filled with plenary sessions such as Tuesday's "The Emergence of the Medical Devices Industry through the View-glass of Microelectronic Packaging Innovation", Wednesday's "The Evolution of Mobile Processing Architectures", and Thursday's "Advanced Bump and Bump-less Interconnection Technologies". Here's a review of what the experts discussed during these sessions.

### Medical Device Industry

Medical electronics range anywhere from equipment such as imaging / x-ray to ultra-small devices designed to be implanted such as hearing aids, retinal implants that aid in restoring some form of vision, spinal implant, ingestible chips that send information wirelessly on how the body is reacting to a given medicine, and an implantable drug pump for time-release of drugs.

Other interesting developments discussed included neuroprosthetics in which silicon is fitted with electrodes to interact with the central nervous system, pacemakers, neurostimulator to help with Parkinson's disease, infusion pumps for soldiers, biosensors for diabetics that read blood glucose levels, MEMS pressure sensors to sense the body's fluids, and

devices to measure intra abdominal pressures and pelvic floor disorders.

Robustness, extreme miniaturization, and biocompatibility are required for implantable devices. Wireless technology will be used more frequently to deliver statistical data from these devices to a collection device outside the body available to the doctor and patient.

In these days of soaring medical expenses, reducing costs of medical care is necessary. Smaller equipment, such as handheld ultrasound equipment the size of a cell phone, aids in this effort. Although resolution will not be as good, the device will be portable and low cost. Many devices in medical environments are used once and discarded. Hybrid devices that have multiple uses are another option. Creating standards in medical devices can also lead to reduced costs.

Wafer level packaging, flip chip, SiP, SoC, integrated passives, and 3D integration / TSVs will be used in these markets. More development is needed in the packaging area, as packaging solutions are not keeping up with silicon advancements. Battery power is also not keeping up with current needs. Future challenges will include stretchable substrates with sensors attached to go on shoes or an ace bandage.

### Semiconductor Business Evolution

Dr. Tien Wu of ASE Group, spoke about semiconductor business evolution at Wednesday's business luncheon. According to Wu, semiconductor industry is experiencing a 6 to 7% growth rate, and is greater than the growth in GDP, which is quite positive. For an individual company to obtain a larger growth rate,

it must steal business from competitors, which leads to price wars.

Because he industry invests \$1 billion more in the front end than in the backend, the backend is lagging. Investment in the backend is expected to catch up over the next ten years.

Growth in the semiconductor industry comes in waves focused around specific industries. The PC wave included CPU, memory, and storage devices. The next wave was communications, which encompassed the ideas of connectivity, bandwidth, and people-to-people communications. Information is the next wave, with life sciences also on the agenda. Each wave is higher than the previous one, which indicates more revenue opportunity in each successive wave.

Wu said there are three strategic business plans or directions to take:

- Long Tail — Older technology with lower margins.
- Hyper Jump — New technology with higher margins.
- New Region — Adopt new technology to local ecosystems or new locals.

He predicted that China will or should become the largest consumer economy in the world, surpassing the United States.

### The Evolution of Mobile Processing Architectures

During Wednesday night's "The Evolution of Mobile Processing Architectures", 4G mobile phones of the future were discussed (we are at 3.9G currently). These phones will have data transmission speeds of 50 Kbps (uplink) and 100 Mbps (downlink), requiring increased speeds from baseband processors. Like the medical industry,

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mobile devices will require increased battery life, and running everyday functions will have to consume less power.

While once the corporate market was driving the demand for smart phones, it is now the consumer market driving applications. The user interface is thus critical; that is, human centered. MEMS microphones will be incorporated into smart phones and 90% of future models will have Global video streaming incorporated. Mobile devices must be cloud-ready, which allows for unlimited computing capacity.

There is an obsession with making cell phones as thin as possible; a 1mm IC package height is the Holy Grail. Through silicon vias (TSVs) are already being used in camera phones, as part of CMOS image sensors interconnects. Qualcomm will introduce a chip soon that incorporates TSVs and microbumps with flip chip. Via middle (through silicon vias made in the middle of wafer processing) is taking precedence over via first or last. Stacking using chip-to chip bonding (rather than wafer-to-wafer or die-to-wafer) will be used when a large memory is being stacked with a processor. The dissimilar size of the two dies dictates this.

0.4 mm pitch FBGAs are currently available, with a pitch of 0.3 mm with 1,000 I/O yet to come. Packaging changes will have to accommodate low-k and lower-k dielectrics, shift from wire bond to fine-pitch flip chip to copper pillars, and be lead-, bromine-, and chlorine-free. The baseband module will require shielding, and the RF and digital will have to be partitioned.

A deep understanding of use conditions will be necessary. New failure mechanisms can be expected, not just from the individual elements that must be incorporated within each cell phone, but the interactions of the individual elements.

### Advanced Bump and Bump-less Interconnection Technologies

Non-conductive film (NCF) is needed for wafer level packaging when attaching and bonding a glass substrate. The bumps on the wafer displace the film to achieve electrical connection, and the bump would have a resin core.

When stacking with TSVs, the vias are drilled through the bottom die to interconnect the top die to the substrate below the lower die. Ultra-fine bumps or copper posts are needed for flip chip, with Sn/Ag (tin silver) solder, which would be underfilled. No cleaning is required before reflow, and the IMC (intermetallic compound) is easy to control.

One speaker spoke of creating fine bump joints for TSVs for high speed signal transmission; gold (Au) bumps, or cylinder posts, of 5, 10, or 20  $\mu\text{m}$  are used. Electroless plating is used, a wet fabrication process. Vias are created of 10 $\mu\text{m}$  high, 5 to 20 $\mu\text{m}$  in diameter, with a 30 $\mu\text{m}$  pitch.

### Networking Opportunities

Networking opportunities are always an important part of any conference, providing a chance to feel the “pulse” of what is happening and what is important to the industry.

A total of 844 attendees came to Las Vegas this year; be sure to be counted at the 61<sup>st</sup> ECTC next year in Orlando, Florida's Walt Disney World Swan and Dolphin Resort, May 31 through June 3, 2011.

(continued from Page 47)

package with embedded passive/actives in 3D eWLB packaging with TSV, flip chip, microbump and 3-D WLPs.

## Conclusion

eWLB technology enhances standard WLPs, allowing for next-generation WLP platform due to its fan-out capability. The benefits of standard fan-in WLPs, such as low packaging/assembly cost, minimum dimensions, and height as well as excellent electrical and thermal performance are true for eWLB as well. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SiP) and 3D stacked packaging. Moreover, next generation, 3D eWLB technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to

various types of devices as well as 3D TSV integration for true 3D SiP systems.●

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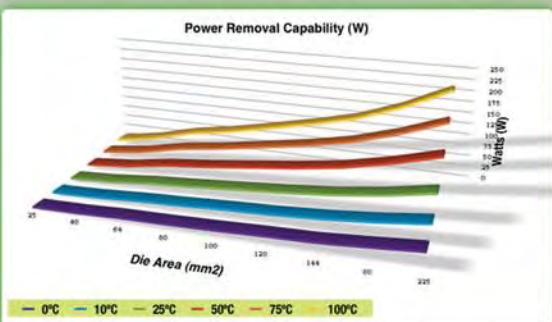
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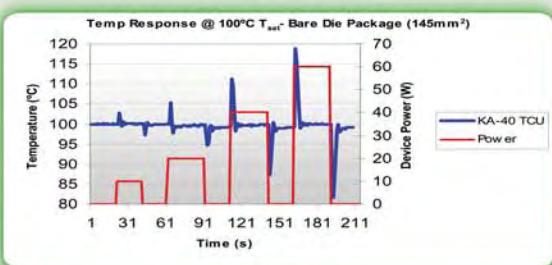
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