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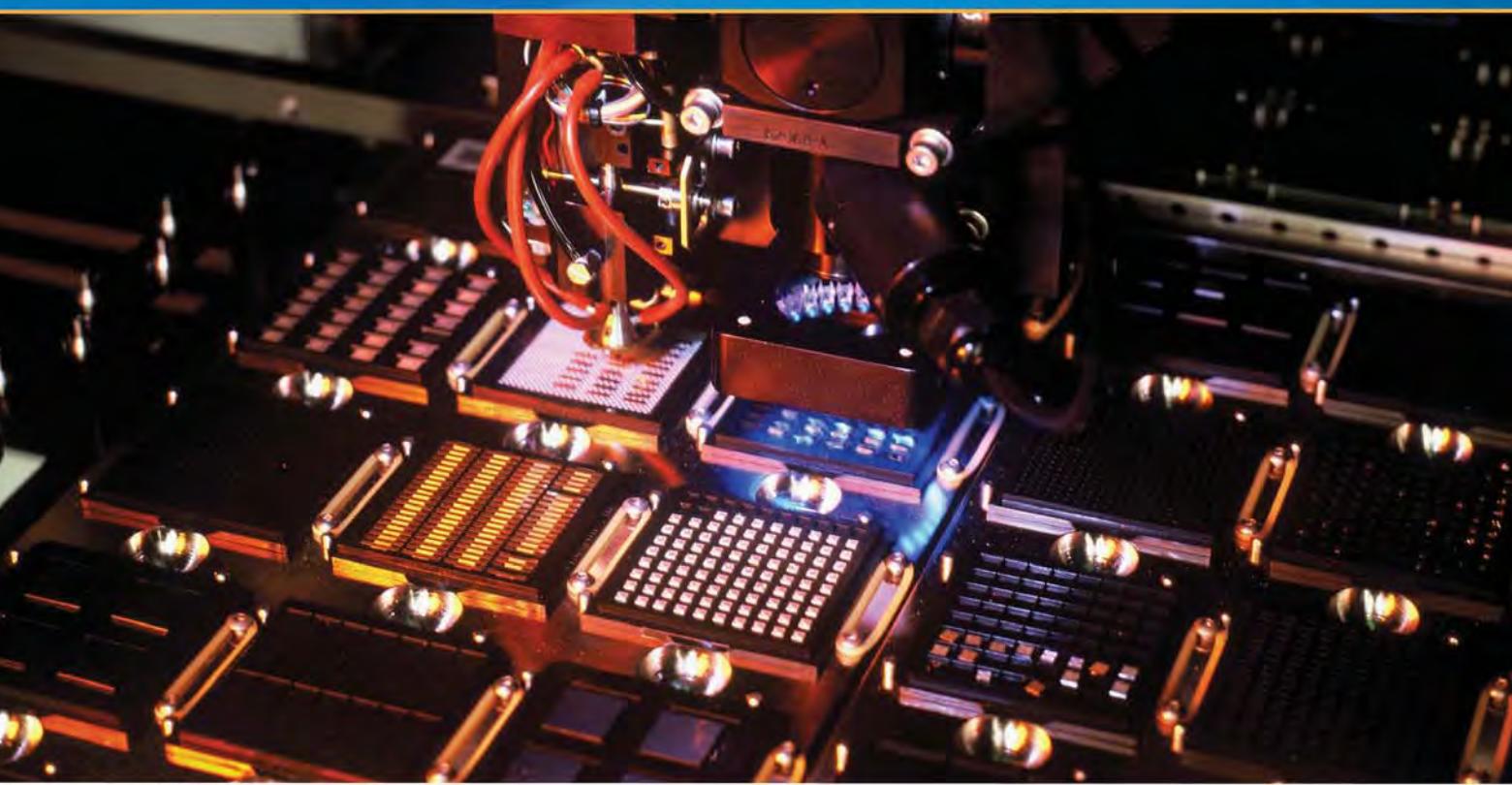
REVIEW[®]

The International Magazine for the Semiconductor Packaging Industry

Volume 14, Number 6

November-December 2010

- Wafer-Level Test
- Design for Reliability
- Fine-Pitch Copper Wire Bonding
- Stress Analysis for 3D Wafer Thinning
- International Directory of Wire Bonders



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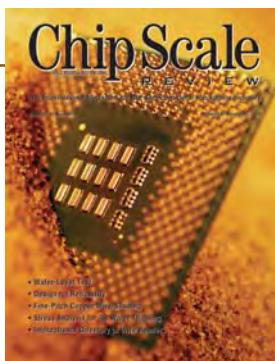
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Nov-Dec 2010
Volume 14, Number 6



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This edition's cover dramatically depicts sand or silica (aka: silicon dioxide) as the raw material for transformation to a silicon wafer. This process is achieved through many steps including the Czochralski process and eventually results as this flip-chip ball grid array. During the manufacturing cycle a number of sequential processes occur to achieve this final step. In this edition of CSR we have assembled a rich set of in-depth articles that unravel a few areas of these complex transforming processes that range from TSV silicon interposers, wafer test probing and the increasing adoption of copper wire bonding, the criticality of emphasis for design and test reliability and the significant challenges of ultra-low alpha emitting solder materials.

Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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Wafer Thinning

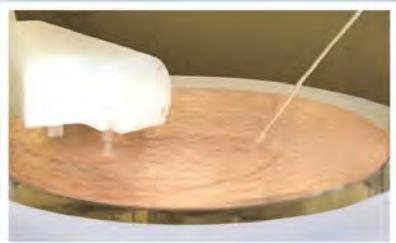


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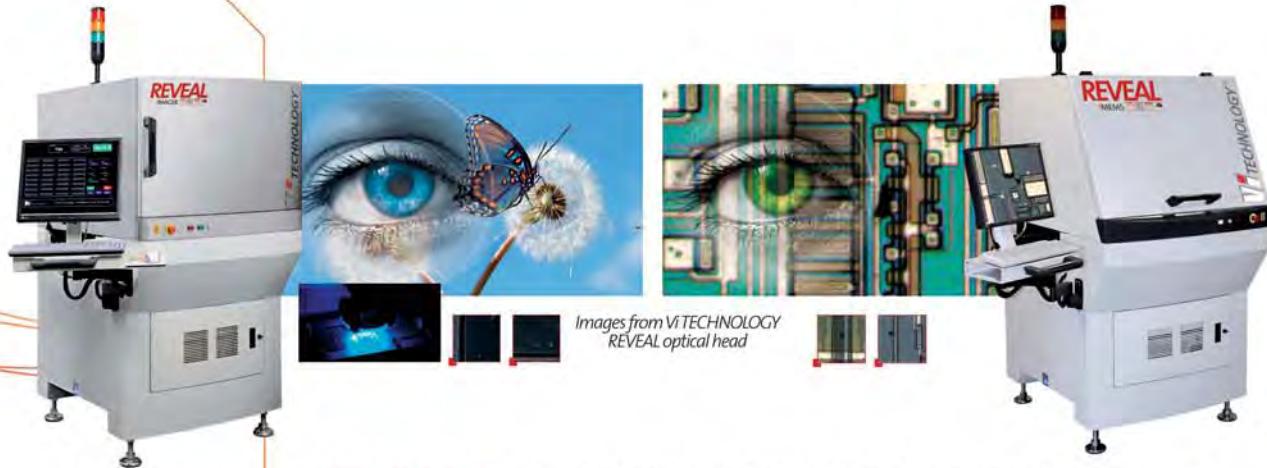
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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Lawrence Michaels Managing Director

lxm@chipscalereview.com

Ron Edgar Technical Editor

redgar@chipscalereview.com

Françoise von Trapp Contributing Editor

francoise@3dincites.com

Sandra Winkler Contributing Editor

swinkler@newventureresearch.com

Dr. Tom Di Stefano Contributing Editor

tom@centipedesystems.com

Paul M. Sakamoto Contributing Editor Test

paul.sakamoto@dftmicrosystems.com

Jason Mirabito Contributing Legal Editor

mirabito@mintz.com

Carol Peters Contributing Legal Editor

cpeters@mintz.com

SUBSCRIPTION INQUIRIES

Chip Scale Review

T 408-429-8585

F 408-429-8605

subs@chipscalereview.com

Advertising Production Inquiries:

Kim Newman

knewman@chipscalereview.com

EDITORIAL ADVISORS

Dr. Thomas Di Stefano Centipede Systems

Ron Molnar Az Tech Direct, LLC.

Dr. Andy Mackie Indium Corp. of America

Dr. Thorsten Teutsch Pac Tech USA

Charles Harper Technology Seminars

Dr. Guna Selvaduray San Jose State University

Prof. C.P. Wong Georgia Tech

Dr. Ephraim Suhir ERS Company

Nick Leonardi Premier Semiconductor Services

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FROM THE PUBLISHER



World Series Champions . . .

The  **Giants**, a Perfect Example of Teamwork !

I actually had my publisher's letter finished ahead of schedule, but then the San Francisco Giants did the unexpected, they won the 2010 World Series! Ever since I can recall, as the daughter of now retired CSR publisher, Gene Selven, there was publishing and baseball. My years watching this sport, and specifically cheering on our hometown favorite Giants, gave me little indication that this seemingly wishful thought for "the Team" would become a reality.

This is historical, at least as far as everyone in this baseball and publishing family is concerned, calling for the immediate and unquestionable need to rethink the publisher's letter for this issue.

Many days and discussions later, amateurs and enthusiasts alike seem to agree on one key point. The Giants won the Championship because they simply performed as a team. This seems to come as a surprise in the era of teams with highly-paid superstars, when it is actually the main premise of team sports, with each player expected to contribute equally to win the championship.

Baseball and publishing . . . I have also relied on the teamwork approach to build momentum and success. With this approach in mind, I would like to share our team line-up for 2011, which will lead to another banner year for *Chip Scale Review*.

Articles, editorials and the supplier directories will continue to be the focus, attracting the widening base of subscribers and advertisers alike. The successful *International Wafer-Level Packaging Conference (IW LPC)*, held in October in partnership with the SMTA Organization, will be enhanced in 2011 with the addition of editorial advisors to expand the technical content. Show dates for the 2011 event are set for October 3-6, 2011 once again in Santa Clara, California.

Chip Scale Review has been selected official media sponsor for the IEEE/ECTC 2011 event and continuing as the BiTS workshop official media sponsor. CSR will also continue ongoing media sponsorships for SEMICON, MEPTEC and SMTA Conferences. Join the CSR Team, as it is never too late to get on the roster for 2011 with your article or advertisement, by contacting our staff. Of course, a big Congratulations to the Giants! 

Kim Newman

Publisher

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EDITOR'S OUTLOOK



A Peek Into Next Year

By Ron Edgar [redgar@chipscalereview.com]

Coming to a close early next year is an interesting 3-year project called dotfive, meaning 0.5THz (500GHz). The project, with fifteen participants from academia and industry in five European countries, aims at developing the enabling technology necessary to move the Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) into the frequency range of 0.5THz at room temperature and evaluate the achievable performance of integrated millimeter wave circuits. Current technology required to achieve these frequencies, based on the more expensive use of III-V semiconductor compounds, does not lend itself to high volume consumer applications. Dotfive hope their technology will enable new applications at very high speed or allow lower speed applications at lower power. Examples include new high-speed interconnects, switches, or ADC/DAC; radar applications such as improved collision avoidance, lane changing, and aviation safety in low visibility; and imaging such as non-invasive imaging, earth sensing, climate control, and medical imaging. The list goes on. To date, 425GHz has been demonstrated and the group is optimistic about achieving the 0.5THz goal within their timeframe. Key functional-block performance has been clocked at 160GHz and shows great promise for many new or improved applications. This certainly might enable some interesting device stacks with technology such as this at the front end for communications or imaging. I think we will see real applications in the not too distant future.

IEEE P1687 is expected to ratify next year. Why should we care? This is the IJTAG standard, aimed at improving testability of single and multiple chips, systems, and boards. It hopes to provide a unified approach to testing rather than the many ad-hoc schemes that exist now, loosely based on JTAG. It aims to improve yields at all levels of system development and provide better debugability. The thrust of the specification is to define "a standard access architecture and protocol, as well as control and automation mechanisms for instruments that are embedded into chips so that these instruments can validate, test and debug chips, circuit boards and systems," according to Glenn Woppman, President and CEO of ASSET InterTech. His crystal ball indicates that the ratification will be "an inflection point because the changes it will bring about in our industry may not be noticeable at first, but over the long term IJTAG will have significant effects." All of us who test chips to systems should take note and if not already aware of what IJTAG offers, should take the time to find out. Improved, more cost-effective testing equals better bottom line.

We have an outstanding set of features for you. Starting with a contribution from the legendary Ephraim Suhir, his article *Probabilistic Design for Reliability* looks at the very real problem of qualification testing and how it could be done faster and better. Wire bonding is our focus in this edition with a directory and two articles on the subject. One is from Horst Clauberg, Ivy Qin, Paul Reid, and Bob Chylak of Kulicke and Soffa, *Fine Pitch Copper Wire Bonding*, and it examines

how copper wire bonding has become an industry reality. The other, *Wire Bonding, It's Not Going Away Any Time Soon* from Gil Olachea of AZ Tech Direct focuses on the machinery and leads into the Wire Bonders Suppliers directory. An interview with Darren James, a product manager at Rudolph Industries, discusses industry trends for probe card test and analysis.

Contactors for Wafer-level Test is the subject of a great article from Jim Brandes of Multitest on the challenges of wafer-level test contacting. He examines the pros and cons of the various available probe types. High-energy sub-atomic particles are the source of many pernicious problems, especially in space and high-reliability applications. Andy Mackie of Indium Corporation and Olivier Lauzeral of iROC Technologies analyze the *Challenges in Supply of Ultra-low Alpha Emitting Solder Materials*. The merits and demerits of *3D Glass and Silicon Interposers* are discussed by Jean-Marc Yannou of Yole Développement who makes the case for a \$950M business by 2015. Stress in thin wafers can be a huge problem. The team of James Hermanowski and Sumant Sood, SUSS MicroTec, Inc.; Scott Sullivan, Disco Corp.; and Hans-Dieter Geiler and Kristian Schulz, JenaWave GmbH have penned a great read, *Stress Analysis of Wafer Thinning Processes for 3D-IC*. So many articles plus our usual Industry News and What's New — what a great line-up. Read them all, you won't be disappointed.

And my crystal ball predictions for next year ... more prosperous than this year and the frenzied pace of development continues with new and exciting technology. I like it! ☺



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INDUSTRY NEWS



IWLP 2010 in Review

Chip Scale Review Staff

This year's 7th annual IWLP, held October 11-14 in Santa Clara CA, set out to connect the future of wafer-level-packaging, 3D, and MEMS with an agenda featuring more than 50 presentations from experts in each area, a marketing panel discussion, a supply chain panel discussion, and a keynote and kick off that tied the whole thing together. The successful event reportedly boasted an increased attendance of 10% with international representation from 13 countries.



European 3D Platform

Opening speaker Peter Ramm, Fraunhofer EMFT, set the stage with a presentation on "The European 3D Technology Platform for Heterogeneous Systems" on Tuesday evening. The 3D program he leads focuses on heterogeneous systems and stacking devices containing MEMS systems. Ramm's presentation featured Fraunhofer's definitions of various 3D configurations. He explained that the choice of 3D technology depends on cost-effectiveness, performance requirements and availability of devices. While through silicon via (TSV) technology is considered one of the most promising, high-performance, and small formfactor 3D technologies today, CMOS Image Sensors (CIS) are the only product on the market using 3D TSV technology. According to Ramm, fabrication of heterogeneous systems often shows the need for post-back-end-of-line (BEOL) 3D integration and mixed approaches.

Among the current projects Ramm's team



is working on is the recently launched eBRAINS, which stands for European Best Reliable Ambient Intelligent Nanosensor Systems. This EU commission-funded consortium picks up where its predecessor, e-Cubes, left off. The latter focused on developing wireless sensor technology integrating ICs, ultra- mini MEMS devices, RF power, memory etc. eBRAIN will focus on improving the reliability of the micro and nano systems themselves. Ramm said since the September 1 launch, he's very happy with the way things are progressing.



Jim Walker



Jan Vardaman



Jean-Marc Yannou

Marketing Panel

Wednesday's Marketing Panel Discussion featured three well-respected industry forecasters: Jim Walker, Dataquest/ Gartner Group, Jan Vardaman, TechSearch International, and Jean-Marc Yannou, Yole Développement. Terry Davis, Amkor Technology, moderated the discussion.

WLP is Pervasive

In her presentation, Vardaman remarked

that WLP is pervasive throughout our industry and increasing over time. She reported a current capacity shortage for 300mm WLPs, but expects that to be alleviated by the end of the year as capital expenditures are expected for additional capacity of both 200mm and 300mm before then. While the majority of demand for WLPs is still driven by the mobile phone market, Vardaman notes other applications are responsible as well. For example, the Apple iPad, of which 2.3M per month are being shipped.



The star of the WLP show is fan-out WLP (FO WLP) and more specifically Infineon's eWLB technology. Vardaman reports that STATS ChipPAC has shipped 35M eWLB packages and more versions of FO WLP can be expected soon including from other manufacturers driven by wireless applications. ASE has licensed eWLP; Nepes bought the RCP line from Freescale and is developing a 3D SiP solution; and Infineon is working to develop a PoP version in its next-generation eWLB.

Solving Problems via 3D

Walker noted that the convergence of bandwidth and speed, design cost and complexity, and time-to-market is driving the 3D packaging market. He said that silicon integration methods take too long, and that packaging is becoming the integrator. "We're lagging Moore's Law. It's taking too long. Design starts are slowing down with regards to advanced feature sizes. There's revenue to be lost by being

late to the market. We are solving problems via 3D and all various derivatives of 3D. Packaging is adaptable to time to market.” notes Walker.

Looking to the future, Walker talks about the internet of THINGS — rather than of computers — to exist by 2021. Future issues include questions like from a manufacturing standpoint, will silicon last beyond 2025? Will consumer applications continue to drive technologies or will it be environmental, governments, military, medical, etc? Will countries form partnerships or will business continue to drive the market? “Whatever it is, it will always be on, and people will always be connected to the man-machine interface,” concluded Walker.

Trends in MEMS Packaging

In his overview of the MEMS market, Yannou began by reviewing the 3 types of MEMS packaging.

First there's the traditional method of packaging individual MEMS in a ceramic or leadframe package that is hermetically sealed. This currently accounts for 8% of the market. Wafer level caps that follow a similar flow is only used for wafer-scale type MEMS devices, such as transducers. A wafer bonding technique hermetically seals the device. This currently accounts for 80% of the market. The remaining 12% of MEMS devices use full WLP processes including interconnections, TSVs, or through glass vias (TGV). He also mentioned an additional emerging technology — thin film capping by deposition of thin films on wafers. This can be done using either silicon or glass. Clearly, the traditional method is being phased out, replaced by WLC and full 3D WLP.

Yannou notes that cost is the main driver for the movement to wafer-level capping and full WLP of MEMS devices. For example, you can place a cap on top of a MEMS transducer and get connections out vertically. The cap only needs to be the size of the MEMS die itself. This way, the MEMS device is smaller and there are more devices per wafer, so the cost is much less.

The IDM View

Keynote speaker, Bradley McCredie, Ph.D., IBM, engaged his audience with his



Bradley McCredie

rousing presentation “Scaling, Packaging and System Integration, Who’s Gonna Carry the Mail?” According to McCredie, classical scaling has reached its limits. The reason is that performance improvements once gained by scaling is now being gained by innovation. But the increased development cost is becoming prohibitive. Using the development of commercial aviation as an analogy, McCredie talked about how reaching peak speed with the Concorde past the exponential and how now it's about taking cost out of manufacturing that sells. The same, he says, goes for the semiconductor industry. What do you do when you've past the exponential? You design for manufacturing. The question in his mind remains, does innovation in packaging technologies take the cost out while adding value? System integration is a time tested cost reduction. “We're going to cross interesting boundaries,” predicts McCredie. “Will packaging play a role?”

WLP Supply Chain Issues

Thursday featured a Supply Chain Panel Discussion by Beth Keser, Qualcomm, Luu Nguyen, Ph.D., National Semiconductor; Takeshi Wakabayashi, Casio; and Matt Kaufmann, Ph.D., Broadcom; moderated by Jan Vardaman, TechSearch International. Much of the discussion during this session revolved around structures needed for new WLPs, who will develop them, what's needed in passivation materials, die sizes and pitch trends, where FO WLP fits, capacity issues and drivers beyond cell phones.

Report from EMC3D

The conference ended with a well-attended presentation by closing speaker, Rozalia Beica, Applied Materials, who discussed “TSV Challenges and Integrated Solutions with EMC3D Consortium.” Interestingly enough, while the EMC3D consortium generally reports on cost of ownership, this time, Beica focused on technical challenges. “Until we solve all technical challenges, we can't implement

the technology,” she explained.

Beica focused on the TSV process sequence where EMC3D has a presence. In the foundry, these include via middle processes, front side redistribution layers (RDL) and bumping, but excludes probe test. In the back-end, it involves everything but final assembly and test. Beica reported successes in improving seed layer coverage, and achieving void-free, conformal deposition. She showcased progress in step coverage, adhesion, and breakdown for the isolation layer. With regards to via fill, the consortium has determined a bottom up approach achieves the best results. Furthermore, optimizing chemistries has proven crucial to 3rd generation ECD processes, resulting reduced plating time, reduced overburden and reduced protrusion, all of which impacts cost.

Conclusion

From WLP to 3D, to MEMS cost, it seems, is still king. However, although Jim Walker cautioned that this doesn't mean always going with the cheapest technology. It really boils down to a combination of cost issues and product life cycle, and will likely involve a combination of silicon package and board level 3D solutions. It's not about being cheapest, but rather meeting consumer needs in the marketplace. Go with the leading-edge technology, says Walker, not the cheapest.



Melissa Serres Director of Education, SMTA



JoAnn Stromberg Executive Administrator, SMTA

Co-hosted by SMTA and *Chip Scale Review* Magazine, the 2010 IWLP was sponsored by Amkor Technology, EV Group, NEXX Systems, Pac Tech USA, and Technic Inc. Plans are now underway for next year October 3-6, 2011.

Visit <http://www.iwlpc.com> for details about the program. Contact Melissa Serres at 952-920-7682 or melissa@smta.org with questions. 

INTERVIEW

Probing Questions for Rudolph Technologies

By Françoise von Trapp, Contributing Editor



Darren James, Product Manager, Probe Card Test & Analysis (PCTA), Rudolph Technologies, Inc. talks with *Chip Scale Review* about industry trends for probe card test and analysis, and Rudolph's approach for addressing these.

CSR: Thanks for speaking with us today, Darren. To get started, could you talk a bit about the product suite that Rudolph offers for probe card test & analysis?

DJ: Rudolph offers several different types of probe card analyzers for testing the whole gamut of probe cards including high performance cards with high density pins for testing devices with a higher number of bond pads that require smaller pitches and smaller probe tips. One-touch memory applications is one area of specialty. The PrecisionWoRx System can be easily configured for a variety of probe card technologies.

The ProbeWoRx300 System is designed for test and analysis of high speed, high force, and high throughput for high pin-count probe cards and features one-touch scan of all probes. The WaferWoRxs tool for probe process analysis measures probe marks.

The industry buzz word right now is “known good die (KGD),” but to get that, you have to start with a known good tester and known good probe card. We provide the mechanism for validating the probe card and probing process, to make sure you have a known good product flow.

CSR: Could you describe the technologies Rudolph uses to evaluate probe cards and how they differ from competing technologies?

DJ: Well, there are a couple of different technologies out there. When you’re testing probe cards, you need to do an optical test to make sure the needles are in the correct position and located in the right place on the wafer. That’s the first part of the test. The second part is to validate the electrical connections from PCB all the way down to needles. In some cases, you have to activate components on the card to establish that it’s a known-good card.

Optics are used for inspecting needles. Rudolph uses a stage-based approach, camera and optic block, measuring the needle in the free-hanging state. It also performs over-travel to measure the needles in the working condition. The center of the scrub is targeted because you want to align the needle so it is not scrubbing off the pad.

Rather than taking a step-and-repeat approach, our optical comparative metrology (OCM) measures the whole surface by moving the camera underneath. It’s a faster, more appropriate process for memory probe cards, where pin counts are moving above 40-50,000 needles. In this case, we use a fixed reference — a fiducial plate — to measure the needle location in X, Y, and Z with a single image scan. This fiducial plate allows us to measure a full 300mm array using a continuous scanning motion for maximum throughput.

Our competitors are using step-and-repeat for all technologies, which is considerably slower on larger array cards and susceptible to more inaccuracies because step-and-repeat measures the needle’s X-Y position relative to stage position, whereas OCM measures relative to the fixed reference grid pattern. Rudolph’s patented 3D OCM distinguishes us from our competitors.

CSR: What are the current economic drivers for probe card test & analysis?

DJ: Probe cards are becoming more of a whole system as more components are being put on the card. In the final test industry, you’re testing tomorrow’s technology with yesterday’s technology, which is always a challenge. To expand capability of the testers, more circuits are being added to the probe card. What drives all probe card analysis is making sure you have a known good probe card; touching down in the right place and making good contact. However, as the industry moves to multi die, scaling to larger and larger needles, it’s difficult to put all those under a microscope manually. You need a tool that will do it for you.

CSR: You talk about Rudolph’s technologies performing both probe mark inspection & probe mark analysis. What’s the difference?

DJ: Probe mark inspection is a “go, no-go” check that is performed as an all-surface inspection just on the wafer. Basically, it ensures contacts stay within the bond pads. It’s an

outgoing quality assurance check used by manufacturers to make sure they have good product going out. Was the mark in the bond pad? If those criteria are met, it's good to go.

Alternatively, probe mark analysis goes beyond inspection to analyze the process and give feedback, giving the end user an opportunity to go back and fix problems. It's a much more in-depth process. At Rudolph, our WaferWoRxs analysis engine can be used on NSX tools, and provides more analysis of the scrub marks and how they relate to each other. It scans across the whole wafer and looks for trends like deflection issues.

CSR: *What kinds of testing process problems can probe mark analysis uncover or provide insight into?*

DJ: With inspection, you see that the mark is off the pad, and the analysis provides the reason why. Then you can make changes to the process to make sure you're putting out good product. Until now, the probing process hasn't had much focus because bond pads were large relative to the needle. All those things have changed. Pads are getting smaller and needles are getting smaller and have circuitry underneath, which contributes to the need for control processes that didn't exist before. It's all about process control.

Probe mark analysis takes the probe card and evaluates how it works in the whole system; how it interfaces with the tester. Without this, you can model some of the behavior but until you actually try and implement it, you don't know how it behaves. Now you can see how it really behaves and where it came from.

CSR: *What is 'predictive scrub' and how can it be used to improve probe card performance?*

DJ: Predictive scrub is a way to improve the whole process. If you look at the whole system, there's a lot of interaction going on. It's hard to dial in on that if you focus on the individual pieces. While predictive scrub can't mimic exactly what's happening in the test cell, what we can do is look at what we expected the results to be from the analyzer and then look at the scrub marks to see what actually happened. Then we work backwards and compensate for that, making improvements to the process along the way.

CSR: *How are increases in sophistication, complexity and cost of packaging affecting your business?*

DJ: Technology moving forward has helped our business grow. 20 years ago there weren't any analyzers, it was all done manually. But as technology reaches 40 and 60 μ m pitch between needles, it's tough for an operator to align. Other methods are

needed to ensure its being done right and that means tools that measure, monitor, and track. That creates more opportunity. Over the last few years, focus on cost has been affecting a number of things. Technology changes mean a need for higher throughput, reduced time on the tools, migration of test area, etc. With the advancement of TSVs, there's a move away from packaging and package test. Rather, there's more focus on sort and testing the wafer itself. Historically it was a two step process. Now, the device becomes the package and that drives more test into the sort area. Part of this is due to customer outsourcing, selling bare die or the wafer itself. The end user is only interested in buying KGD. They want assurances that the die they put in their cell phone is good because the whole package is expensive.

In the sort area, new probe cards allow for higher speeds closer to true operational speeds. If you weed out the bad die in the sort area it minimizes the amount, and therefore the overall cost of final test.

In the 3D integration space Rudolph is doing a lot of inspection work, but on the probe card side, we're still trying to understand what changes this will drive. One option is testing on the lower substrate in the stack rather than the package, and testing bond pads on the package, but only time will tell if that's a viable approach. We're seeing efforts to reduce the force that each needle applies, but there's still a trade-off between force and contact; the more force the better the contact resistance. You need to manage all the tradeoffs. We don't have a really good feel yet for how probing of TSV devices will be implemented.

CSR: *One final question. What future trends do you see on the horizon for probe card testing and analysis?*

DJ: I see three major trends moving forward. First of all innovation in tip technologies for probe card needles will allow for higher densities across the board for DRAM and microprocessors, and more needles in a tighter space. On the other extreme, but driving in a similar direction, I see larger scale across the board with multi-die testing, and bigger arrays. The whole probe process therefore becomes more challenging. As the probe array gets bigger, you still have the same constraints; you have to control surface planarity. How do we go from a small one-inch area, and while still maintaining process, move to a 12" area, all the while increasing force from 60-300kg to maintain planarity across a huge area? That's the challenge moving forward on how to do that.

Additionally, how do we handle the higher temperatures moving forward, for example 190-200°C required in medical and automotive devices? And finally, there will be a trend to reduce cost of test and cost of interconnects.

Stress Analysis of Wafer Thinning Processes for 3D-IC

By James Hermanowski and Sumant Sood [SUSS MicroTec, Inc.], Scott Sullivan [Disco Corp.]
Hans-Dieter Geiler and Kristian Schulz [JenaWave GmbH]

With growing interconnect densities and rising costs of IC manufacturing in leading edge technology nodes, 3D architectures for IC integration and packaging are being adopted by device manufacturers. This drive towards 3D IC and stacked chips requires the thinning of device wafers down to 30-120 μm . A typical 3D-TSV integration process flow involves temporary wafer bonding of a processed device wafer to a supporting carrier wafer and subsequent thinning of the device wafer to the desired thickness. Cracking and chipping are major yield factors for thinned wafers. This article examines the stresses induced as a result of thin wafer processing and discusses a way to measure the stresses using nondestructive techniques while mitigating undesired stresses.

To keep a process in control, measurements must be taken. One key factor in semiconductor devices is stress. There are a number of different methods to measure the stress of devices and surfaces. The challenge is to find a method that measures the stress on the device wafer as a whole, while having the resolution to find localized areas of interest.

In this study, a scanning infrared depolarization (SIRD) stress measurement tool* is used to measure the stress in a wafer as it is processed through edge trimming, bonding, and thinning. The results of the tests show that it is possible to measure while processing; thus controlling the amount of stress the device wafer is subjected to during bonding and thinning.

Micro-Raman spectroscopy is a method well suited for measuring localized stress in silicon wafers. When setting up a wafer thinning process, this destructive test method can be used to measure the stress at the grind mark and find the depth of the resultant stress. On occasion, micro-Raman spectroscopy is used as a process control. Published stress values at the grind marks in silicon are between 25 MPa to 175 MPa

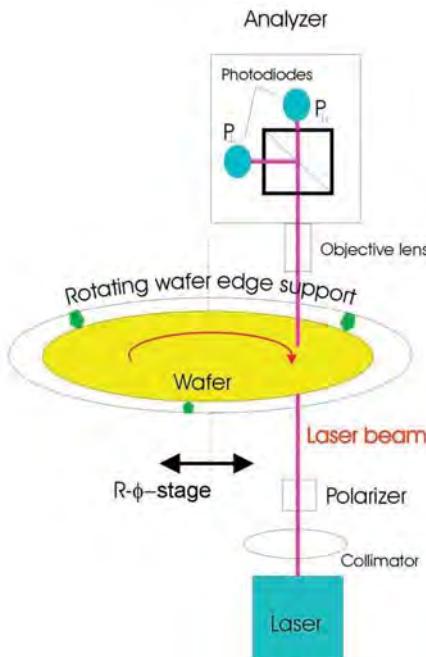


Figure 1. Optical schema of the scanning infrared depolarization imager SIRD with the laser unit, the analyzer unit and the rotation-translation stage where the wafer is placed supported by 3 edge pins

and the effects being observed are up to 10 μm deep. Unfortunately, Micro-Raman spectroscopy does not meet some of this study's requirement for process monitoring. However, the test method does give a good baseline value for stress induced by grinding.

A common non-destructive method for measuring silicon wafers is X-ray diffraction (XRD). With both reflective and transmissive functions, surface stress and internal defects can be measured. Of particular interest to this work was one of the well-known limitations of XRD.

The stress measurement tool, SIRD, represents a full wafer shear stress imager based on an infrared transmission polarimeter. A linear, polarized laser beam of 1.3 μm wavelength penetrates the wafer, and the emitted light is analyzed by use of an analyzer of the polarization state (first Stokes component). The optical arrangement is shown in **Figure 1**. When a wafer is stress-free, the polarization state stays

unchanged during the transition and the depolarization D is zero. If the wafer contains local or global stress fields, the stress-induced birefringence of the crystal causes stress-related depolarization. By scanning the wafer (rotation and translation with polar coordinates) a map is produced and, taking into account the recorded depolarization, the shear stress equivalent G is calculated. This dimensionless equivalent G is proportional to the planar shear stress in polar coordinates. The proportionality is determined by the piezo-optic wafer module M, including the piezo-optic constants of the material and the wafer thickness. Both should be known.

As can be seen by the optical schema of SIRD, the stress-induced phase-shift effect between ordinary and extraordinary beams is integrated across the wafer thickness (integrated photoelasticity). Hence, there is no information about the stress distribution across the wafer thickness. From the remaining 3 plane stress components (radial normal stress σ_{rr} , tangential normal stress $\sigma_{\theta\theta}$, shear stress) SIRD records only one component: the plane shear stress. The sensitivity of the tool allows the detection of stress effects amounting to 0.5 kPa in a wafer of 725 μm thickness.

Because of the short measurement time (about 10 min.) and the noncontact and nondestructive method, the system is capable of in-line control and measurements on product wafers (**Figure 2**). Process control is possible with respect to introduced stress or introduced lattice defects revealed by their stress fields. Quantification of the stress and classification of the defects together with the applicability in all cases where the laser can penetrate the wafer (transmission limit 10-4) allows a broad field of process control tasks starting from wafer manufacturing up to IC-manufacturing and 3D-integration, especially when abrasive and thermal processes are under consideration.

With XRD in the reflective mode, there is some penetration into the sample's

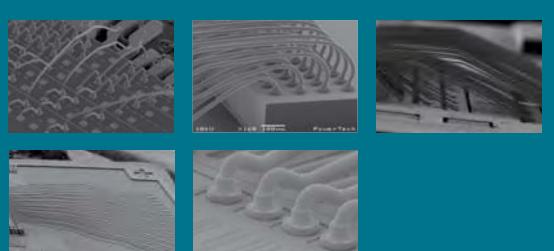
PTI Powers Integration Technology Revolution



wafer thin to 20um



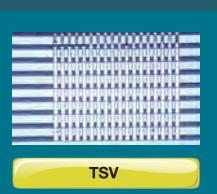
High density chip stacking



Advanced wire bonding



Cu pillar bump



TSV

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Figure 2. SIRD-A300: Fully automated photoelastic measurement system SIRD with handling module, FOUP load port and measurement module (courtesy of PVA TePla AG, Germany)

surface. The result of the penetration can skew results if there is a large variation in the amount of subsurface stress. Surface stress values are a product of the area being measured, as well as the stress due to subsurface damage.

Combining the information from micro-Raman spectroscopy and XRD literature helped decide on the ways to interpret the transmission and reflectance SIRD data. Additionally, when looking at the data from the resolution of the images, it allowed for easy determination of which process induced which stress.

The Process

Performing this process requires six blank 200mm silicon wafers. Two wafers are used as carrier wafers, two are simulated device wafers, and the remaining two wafers are reference wafers. To set a baseline, all the wafers are measured before any processing is done.

Following the baseline measurements, the “device” wafers have their beveled edges trimmed away. Wafers are beveled on the edge for a number of reasons. Two common reasons that affect back-end processing are to allow for easier handling and to keep the edge of the wafer clean during the deposition steps. At the thinning step, the bevel shape of the wafer edge is not a benefit but instead a yield-reducing risk.

As wafers are thinned, the shape of the wafer edge changes, becoming a knife edge at 3D target thicknesses. This thin, sharp edge is more susceptible to damage, while

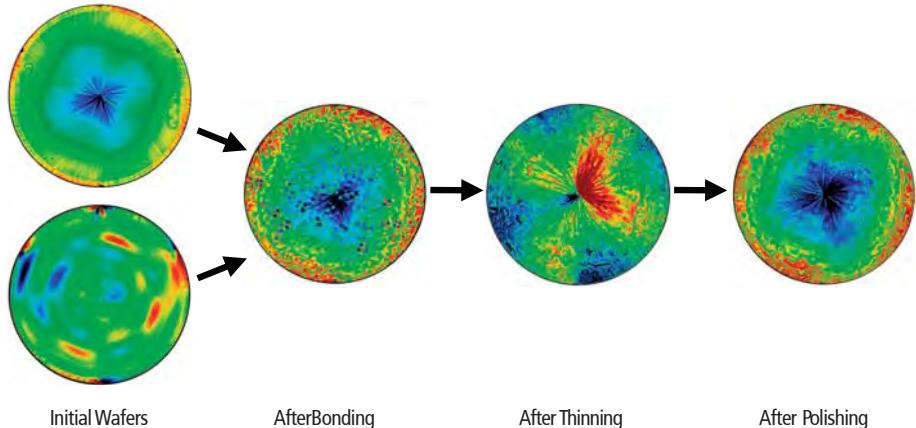


Figure 3. C3 bonded to E4 progesion

at the same time a pocket between the carrier wafer and device wafer exists, which can collect particles during grinding. Trimming away a section of the edge bevel or removing the entire edge bevel prior to thinning reduces the likelihood of damage and eliminates the pocket for particles to become trapped.

The edges are trimmed away by grinding. This can be done with a dicing blade or grinding wheel. For these tests, a grind wheel was used to remove the whole edge bevel. Following the edge trimming, the effect on the wafer is measured prior to bonding.

The 300mm wafers undergo a temporary adhesive bond process** so they can be ground down to approximately 50 μm thickness.

With the “device” wafer bonded to the carrier, thinning can then take place. The grinding is a two step process. First, the majority of the material is removed with a coarse grit wheel. The advantage to using a large or coarse grit is that material is removed quickly. Larger grit has the negative effect of creating a layer of subsurface damage that extends deeper into the silicon. Following the grinding done by the coarse grit wheel, a fine grit wheel is used. The main purpose of the fine grit wheel is to remove the subsurface damage created by the coarse grit wheel.

Grinding with even an extremely fine grit wheel will create subsurface damage. To remove the subsurface stress and subsequent stress from the surface of the wafer the wafers are polished. Final measurements are made on the post-polished wafers.

Results

With grinding and edge trimming, stress is added to the wafer by creating micro-

cracks. These micro-cracks expand the surface exerting a tensile force.

Figure 3(a) shows an as-polished wafer. The stresses in the wafer are circular, possibly from the growth process. Trimming the polished edge changes the stress in the wafer by creating a layer of subsurface damage around the periphery of the wafer. The increase in stress from the edge trim process is from 0.4 kPa to 6 kPa.

Figure 3(b) shows the radial pattern of an in-feed ground wafer. Stress went from 6 kPa to 97 kPa. The increase in stress is as expected. What is also expected is that the larger stress from the grind subsurface damage masks the bulk grown in stress.

Figure 3(c) shows the wafers after thinning with a super fine grit wheel. The grind marks are still visible and less pronounced. The amount of stress has fallen back to the as-polished range.

Figure 3(d) shows the wafers following the polish step. This is done to remove the subsurface damage layer. There is little change in the amount of stress in the wafer.

Conclusions

The SIRD method gives results that allows for high-throughput, non-destructive process monitoring and improvement. SIRD appears to be a highly sensitive technique. The high sensitivity provides a wealth of information regarding the process and equipment, allowing for discovery of critical trends that will be useful for developing wafer thinning processes.

Most importantly, the shear stress pattern on each wafer is tracked as it was processed. Wafer stress increases at the wafer edge due to the edge trimming process. Although the level is relatively low at 5kPa it is

concentrated at the wafer edge. Wafer processing, coating of adhesive and grinding the wafer changes the stress level. Regardless of the processing, it appears that after wafer thinning and polishing the global stress on the wafers is then reduced down towards a neutral wafer.

The final overall image of the shear stress across the wafer is a composite overlay showing the monopoles and patterns from each step, although at significantly reduced stress levels depending on which step of the process the wafers had seen. The high level detail of the images will require more effort to link revealed patterns to physical and process parameters and ultimately to improved process results.

* The JenaWave, SIRD-ARD

** SUSS' XBC300 bond modules using Brewer Science Inc. Waferbond? HT10.10

The authors would like to thank Alain Phommahaxay for providing wafers for this study.^{SP}

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Chip Scale Review Nov/Dec 2010 [ChipScaleReview.com] 17

3D Glass and Silicon Interposers: A \$950M Business by 2015

By Jean-Marc Yannou, [Yole Développement]



Jean-Marc Yannou is in charge of advanced packaging analysis at Yole Développement, including wafer-level packaging and 3D system integration. His 15 years of experience in the semiconductor industry include serving as innovation manager for system-in-package (SiP) technologies at Philips/NXP Semiconductors, and years at Texas Instruments.

3D glass and silicon interposers face fragmented demand and plenty of competition from other emerging solutions, but they're still likely to be a \$950M business by 2015, with a volume of 1.8M 300mm-equivalent wafers. Admittedly, this is a risky forecast for this emerging market, with its wide range of potential applications and different drivers. But it's the best estimate based on close examination of the technology's potential in areas where 3D interposers are a clear solution, and of the trade offs and alternatives in areas where interposers are just one of several potential competing solutions to the looming limits of existing technologies.

A 3D interposer can be defined as a bridge substrate or carrier that connects a die to wider-pitched contacts on another die, package, or board, using vertical through-via electrical connections patterned by photolithography. Currently, 3D interposers are already in volume production for products out of the IC mainstream with unique needs, such as MEMS and high brightness LEDs.

Some MEMS manufacturers use a kind of 3D interposer to reduce the cost of packaging tiny die. Taking electronic connections out through vias formed in a wafer-level cap for attachment to the board allows MEMS chips to be made significantly smaller and thus cheaper, bringing down the cost of the packaged device in spite of the higher cost of through silicon via (TSV) processing.

High-brightness LED manufacturers are choosing 3D silicon interposers for better performance at lower cost. Historically, they have used flip chip attachment to a ceramic sub-mount for heat management, so it's just a question of replacing ceramic with silicon. Though ceramic is the better thermal conductor, silicon can provide better control of electrostatic discharge and allows smaller devices to reduce cost. And with better heat extraction with TSVs, silicon interposers can come close to matching ceramic for thermal management.

Soon, silicon interposers will be manufactured in volume production for CMOS image sensors, RF transceivers, and power amplifiers; again driven by the specific needs of these applications. The next generation of image sensors markedly improve sensitivity at lower cost by using backside illumination, a process that involves thinning the wafer to get the light out the back, and necessitates the use of interposers with vias to get the electrical contacts out the other side. Some power and RF chips will also move to using interposers as a solution for improving heat extraction and adding more integrated passives for better performance at smaller size.

Near term solution for logic and memory stacks

In the mainstream logic and memory IC markets, 3D interposers offer a compelling solution to reduce power

usage in memory stacks and to increase performance of the logic-memory interface. Memory stacks consume a lot of power in the I/O buffers needed to drive the signals out of the IC. Shortening the interconnects by integrating the memory chips with TSVs on interposers can considerably reduce the number and size of the required I/O buffers, thereby considerably reducing power consumption.

For logic-memory stacks, shorter interconnects allow for higher frequency and wider bandwidth for higher speed access to memory. Interposers with TSVs between the chips currently seems to be the easiest way to make these stacks, especially as experience using interposers in other niche markets builds process knowhow and potentially reduces costs.

In the long run, standards for pad placement on logic and memory chips could allow direct chip-to-chip connections without interposers. JEDEC appears to be making a lot of progress on such standards that could eventually make interposers unnecessary. And design software will likely allow fully integrated 3D design, but the tools are far from ready. It is also possible, however, that interposers — like many older IC technologies — will remain a cost-effective solution for some applications.

Finally, interposers are potentially a viable solution to the problem of connecting 28nm generation logic — with its very high I/O density — to the outside world. Chip makers are concerned about the thermal and mechanical mismatch with current laminates causing reliability problems with ultra low-k dielectrics and copper pillar flip chip attachment that will be required at this node. Silicon interposers that match the thermal and mechanical characteristics of the silicon chip provide a clear solution, though at an added cost. So an R&D push is on to find new laminate and underfill materials with lower coefficients of thermal expansion (CTE) that might potentially

solve the mismatch issues at lower cost. But wider experience with 3D silicon interposers and its alternatives — like multicrystalline silicon and volume production on depreciated lines — are also likely to bring down the cost of silicon interposers.

Wide adoption of these 3D interposers will also depend on the development of a reliable and cost-efficient supply chain. The field is wide open for new players and business models to capitalize on the opportunity. IDMs, fabless IC suppliers, wafer foundries, packaging houses, MEMS players, substrate makers, and printed circuit board suppliers are all looking at taking on this part of the value chain. While many companies are in the position to manufacture the interposers, the traditional electronics OEMs aren't likely to be able to assemble the more IC-like devices, nor be able to design them. And who will do the testing and take responsibility for yield and reliability? Successful suppliers will need to figure out the best ways to organize this new

**Summary Table - 2010 Status of 3D Silicon/Glass Interposers
An emerging market**

Interposer type (technology segments)	MEMS and sensor capping interposers	CMOS image sensor interposers	HB LED silicon submounts	3D Power/RF/ analogue integrated passive interposers	Logic only interposers	Logic + memory interposers	Memory stack interposers	Misc. Silicon/glass substrates/packages
Applications	gyroscopes, accelerometers, microphones, pressure sensors, piezoelectric, microfluidic, micro-probes, optical	CMOS in mobile phones, cameras, automotive	HB LED-LHBT-LED (mobile, automotive, general lighting)	RF interposers and power amplifiers (mobile phones, medical & industrial)	High I/O count logic ICs: CPUs, GPUs, FPGAs, application processors	Application processors for mobile phones, CPUs, GPU's	Server farms, computers, both DRAMs and flash memories	Medical, industrial, oil & gas, search, aerospace, defence
2010 status	In Production	Sampling. Will appear with BSI, Sony already in BSI, w/o interposers	Some early production	Sampling (similar interposers, but w/o TSVs are in production)	Proof of concept	In-development, proof of concept	In-development, start of prod by year end	Development of demonstrators
Wafer size	150-200mm	300mm	150-200mm	150-200mm	300mm	300mm	200mm	150-200mm
2010 Wafers	183k (86-inch) 44k (6-inch)	0	50k (6-inch eq.)	A few hundreds	0	0	A few k's	A few hundreds
Players (non-exhaustive)								

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value chain, whether as system integrators or partnerships, perhaps involving specialty design and test services.¹⁸

References

These applications, technologies,

competing solutions, cost issues, likely players and the market size and roadmap are all discussed in detail in Yole Développement's new report 3DSilicon and Glass Interposers: Technologies, Applications and Markets.



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Fine Pitch Copper Wire Bonding

By Horst Clauberg, Ivy Qin, Paul Reid and Bob Chylak [Kulicke and Soffa Industries, Inc.]

Copper wire bonding has become a mainstream packaging technology for high I/O, fine-pitch devices. After over a decade of initially slow-paced R&D, quadrupling of gold prices over the past five years caused the electronics packaging industry to redouble its efforts. This research is now bearing fruit in fully commercialized, high-volume production.

Current market growth in copper wire bonding indicates a revolutionary shift from gold to copper. Until about the end of 2007, the installed base of copper-capable wire bonders represented little more than those used for R&D purposes. Now the number of wire bonders in full production use is doubling every 6 months (**Figure 1**) and the use of copper wire has reached about 20% of the fine-pitch market.

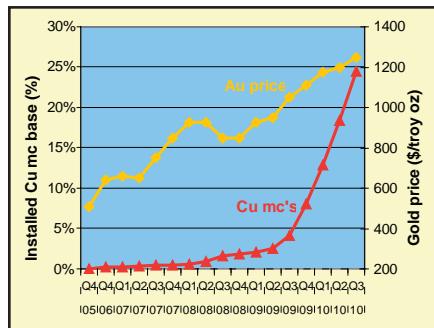


Figure 1. Installed base of Cu wire bonding machines as a percentage of total installed and gold prices for the past five years

The substantial advantages of copper wire including cost (about 15x lower than gold wire), higher thermal and electrical conductivity, and higher stiffness have long been recognized. However, along with those advantages came adverse properties that posed great technical challenges.

Most obvious was copper's propensity to oxidize and corrode. This not only required a means of shielding the copper from oxidizing during the spark that forms the ball, but also caused problems

for the formation of the stitch bond and reliability issues in the final molded packages.

Initially less apparent were problems associated with copper's greater hardness relative to gold. Among gold wire bonding advancements over the past decade was bonding over active circuitry (BOAC). To save die real estate, complex but fragile structures of conductors, dielectrics and even transistors were placed under the bond pad. Bonding on these pads with gold wire was already challenging, and now these same or similar pad structures were expected to be bonded with harder copper wire.

With the advent of copper wire bonding, virtually every aspect of wire bonding required reexamination. As a result, a multitude of process, equipment and material innovations were made in the areas of ball formation, ball bonding, stitch bonding and reliability. Only wire looping was relatively free of challenges, merely requiring a re-optimization of existing processes and providing updated guidelines to achieve loop shapes comparable to gold.

Ball Formation

The inert cover-gas system for protecting the molten copper at the end of the wire during the formation of the ball is perhaps the most readily-apparent modification to the wire bonder. (**Figure 2**) These systems have evolved steadily based on ever-more sophisticated knowledge of the allowable levels of oxygen and the intricate interactions between geometry and gas flow. Today's most advanced cover gas systems are designed using state-of-the-art computational fluid dynamics (**Figure 3**) and advanced Schlieren gas flow visualization techniques. Bonding experiments were carried out in highly controlled environments to determine the levels of oxygen that can cause problems.



Figure 2. Kulicke & Soffa Microenvironment inert cover-gas kit showing the ceramic tube to cover the spark and the Bond Surface tube for covering the bond site

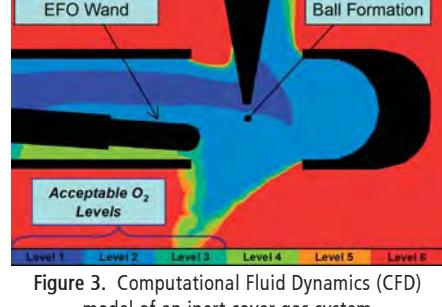


Figure 3. Computational Fluid Dynamics (CFD) model of an inert cover gas system

Currently, the cover systems are optimized to use minimum forming gas (about 0.5 l/min) and usually have an optional gas port that provides forming gas to the bonding surface to increase bond strength. Occurrence of oxidized balls or pointed balls that take place when oxygen levels are slightly too high has been essentially eliminated.

For bare copper wire, the inert cover gas is typically forming gas; a mixture of approximately 5% hydrogen in nitrogen, in which the hydrogen reacts with any residual oxygen in the spark and reduces oxides on the wire. Recently, palladium coated copper wire was introduced, which allows the use of pure nitrogen, presumably because there is no pre-existing oxide layer on the wire surface.

First Bond

The ball bond is the subject of the most intensive R&D efforts. While it is reasonably straight-forward to obtain a

ball bond with high shear-per-area, it is not at all straight-forward to do so without excessively deforming or damaging the bond pad. Not only is copper harder than gold, it usually requires higher levels of ultrasonic motions to make a strong bond. This combination can result in extremely thin aluminum in portions of the bond (**Figure 4a**), excessive amounts of Al splashed beyond the ball radius (**Figure 4b**), or cracks in the dielectric/via structures under the bond pad.

One of the first innovations to reduce the amount of Al deformation was the introduction of softer copper wires.¹ More recently, a greater depth of knowledge about the detailed mechanics of the bonding process has resulted in highly tuned combinations of impact forces, bonding forces, bonding times, ultrasonic motions, and slower high-amplitude motions. These techniques minimize Al splash and provide uniform thickness of Al under the bond, all while maintaining high shear/area (**Figure 4c**).

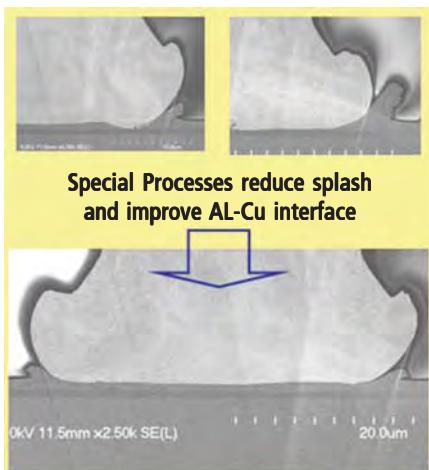


Figure 4. Cross-sections of Cu-on-Al ball bonds showing (a) excessively thin Al under the periphery of the bond, (b) large Al splash and the (c) a well-optimized ball bond

This greater depth of knowledge has recently been implemented into a series of special copper bonding processes² made available on a wire bonder³ specially designed and optimized for copper. The new copper-specific processes provide both improved process results and increased bonder productivity. A direct comparison of traditional bonding results versus the new copper process results are shown in **Figure 4d1** and **4d2**.

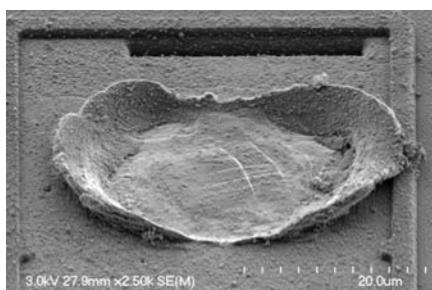


Figure 4d1. Large Pad Splash from traditional bonding process

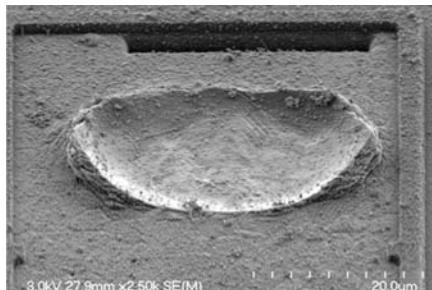


Figure 4d2. Reduced Pad Splash using special Copper Process

As copper wire bonding becomes the preferred process for many devices, the bond pads themselves are being designed to accommodate copper. Fragile via structures are moved out of the highest stress regions to the periphery of the pad, and the Al thickness is being increased to provide more cushioning. The thin Al pads commonly used for gold wire bonding were necessary to limit excessive Au-Al intermetallic growth. Formation of Cu-Al intermetallics is orders of magnitude slower, so thicker Al pads can be used without the risk of Kirkendall voiding.

Second Bond

Although initially quite challenging, most problems associated with the stitch bond have been overcome. Again, the solution involved a combination of innovations in bonding process, bonding wire, and bonding tools. Softer copper wire substantially improves stitch bond performance, and relatively large-amplitude motions, either linear or circular, make good stitch bonds feasible on most surfaces. These motions present fresh, oxide-free copper wire to the lead surface. In addition, they increase the contact area between the wire and lead without introducing excessive vibration from ultrasonic energy. Such vibration can lead to wire sway and poor control

over looping.

The most modern Cu-enabled wire bonders provide a plethora of bonding options and easy user interfaces for implementing a variety of bonding processes. Now the most challenging aspect of developing a stitch bond process can often be how to optimize a process with near-infinite potential process options.

This situation is complicated by the variety of lead surfaces and geometries. In certain package types, such as QFN and some metal lead frames, it is difficult to almost impossible to clamp the leads firmly during bonding. Such packages rely heavily on large amplitude, slow motions for making the stitch bond. With respect to lead surfaces, the most easily bondable surfaces, such as electrolytic Ni - soft Au, are also the most expensive, so that less optimal, less expensive options are often implemented in production.

The thin oxide layer that always exists on copper wire is somewhat slippery, making the ultrasonic motions of the capillary less effective at transferring energy into the weld. Two materials innovations address this problem in different ways. Bonding tools with a granular surface⁴ (**Figure 5**), “bite” into the wire and ensure the effective transfer of ultrasonic energy from the bonding tool to the wire. The other innovation is to coat the Cu wire with a layer of Pd. Although this increases the cost of the wire approximately 3-fold, it is still dramatically less expensive than gold. The Pd surface is free of slippery oxides and typically results in stitch bond strengths that are 50% higher than for bare Cu wire. Unfortunately, Pd-coated Cu wire has one additional down-side: the free-air ball is even harder than that of bare Cu wire and the issues mentioned in the Ball Bonding section are exacerbated.

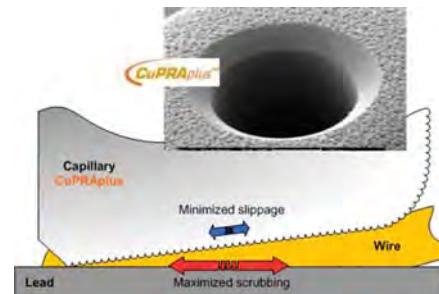


Figure 5. Granular surface K&S CuPRAplusTM bonding tool shown gripping copper wire for improved transfer of ultrasonic energy

Reliability

The use of copper wire bonding in high volume manufacturing demonstrates that confidence in producing reliable packages has been achieved. When they occur, the root causes of failures in copper wire bonded packages are radically different from those in gold wire bonding. In Au-to-Al wire bonds, most failures typically stem from excessive Kirkendall voiding in the rapidly growing intermetallic compounds. Although these intermetallics are somewhat sensitive to corrosion, this aspect of reliability is relatively minor. As a result, accelerated, unmolded baking of the devices provides an accurate prediction of a molded package's ultimate reliability. Intermetallic coverage is a highly useful quality measure for Au-Al ball bonds.

In Cu-to-Al bonds, intermetallics grow slowly, so that void formation is not a serious problem. Historically, the extreme thinness of the intermetallics also prevented the process engineer from performing an easy check of bond quality by measuring intermetallic coverage. More recently useful measurements of intermetallic coverage have emerged.

Further complicating the optimization of a process for good reliability is the fact that the highest shear/area does not correspond to the most reliable Cu bonding process. For Cu ball bonds, shear/area may be well above 10g/mil². In contrast, Au-to-Al bonds usually show a clear maximum near 7g/mil², and the process with the highest shear/ area will typically be the most reliable as well. Maximizing shear/area in a copper wire bond only guarantees badly damaged bond pads. Instead, the optimization has to rely on careful and extensive cross-sectioning and etching to verify an even and continuous bond between the Cu and Al.

The next complexity arises from the high sensitivity of copper and some of its aluminum intermetallics to corrosion. Interaction of moisture from highly accelerated stress tests (HAST) and pressure cooker tests (PCT) with halogens and acidic components in molding compounds are the root-cause of many failures. Since the nature of the mold compound is one of the key aspects for passing reliability tests, the old standby of baking unmolded devices as a quick and relatively easy method of screening

bonding processes before the more involved molded reliability tests has lost much of its value.

Mold compound manufactures have learned much about the reliability requirements for copper wire bonded packages. **Figure 6** shows the reliability

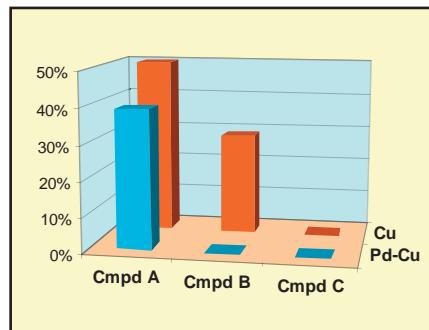


Figure 6. Failure rates after 336 hours biased HAST test for three experimental mold compound formulations with 0.8 mil bare Cu and Pd-coated Cu wire on Al bond pads. (5V bias, 130oC, 85% RH, electrical open/short test. We thank Hitachi-Chemical for sharing this data (These results are not guaranteed.)

performance of the same copper-bonded devices in three different green (i.e., not containing Br/Sb flame retardants) molding compound formulations. Further improvements in molding compounds specifically designed for copper wire bonding are likely to follow. The figure also demonstrates a recent nugget of knowledge that has been gained: Pd-coated Cu wire is somewhat less sensitive to corrosive components in the molding compound.

Conclusion

In-depth re-examination of all aspects of the wire bonding process and a burst of innovation in equipment, processes, tools and materials has made copper wire bonding a commercial reality that is here to stay. The next few years will see copper wire bonding expand into ever more complex and higher I/O devices.

Acknowledgement

The authors would like to sincerely thank Hitachi-Chemical and Hidenori Abe in particular for allowing us to show their molded reliability data.

Reference

1. Heraeus Maxsoft
2. ProCu Bond Process
3. IConn ProCu Wire Bonder
4. K&S' CuPRAplus capillary

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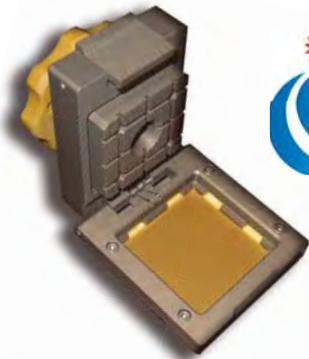
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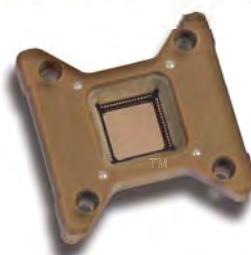
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Probabilistic Design for Reliability (PDfR)

By Ephraim Suhir, [ERS Company, University of California Santa Cruz, University of Maryland College Park]

“ You can see a lot by observing.” — Yogi Berra, American Baseball Player

“It is easy to see, it is hard to foresee.” — Benjamin Franklin, American Scientist and Statesman

Reliability Engineering (RE) is part of the Applied Probability (AP) and Probabilistic Risk Management (PRM) bodies of knowledge.¹ The term reliability includes dependability, durability, maintainability, repairability, availability, testability, and other properties that could or should be viewed and evaluated as probabilities of the corresponding reliability characteristics of a device, system, or process. The use of AP and PRM concepts, approaches, and techniques puts the art and practices of RE on a solid probabilistic and low-risk foundation.

Accelerated Testing (AT)

It is impractical and uneconomical to wait for real-time failures when the Mean-Time-To-Failure (MTTF) of today's highly reliable electronic and photonic systems is many thousands of hours. AT is therefore an inevitable and powerful means for understanding, evaluating, and improving reliability.^{2,3} This is true for Qualification Testing (QT), testing to pass, or Highly Accelerated Life Testing (HALT), testing to fail. To accelerate a device's degradation and failure, one or more conditions that affect functional performance, mechanical reliability, or environmental durability are deliberately distorted. The major AT categories shown in **Table 1** differ by their objectives, end points, follow-up activities, and what is viewed as an ideal test.⁴

QT is the major means through which industry proves that the reliability of their products is above a specified level. This level is measured by the percentage of failures per lot, the number of failures per unit time, or both. QT reduces different products, as well as similar products made by

different manufacturers, to a common denominator. QT reflects the state-of-the-art in a particular field of engineering and the typical requirements for product performance. Although industry cannot do without QT, today's QT and specifications (JEDEC, Telcordia, AEC, or MIL) are only good for what they are intended — to confirm that a given device is qualified to become a product. If a device passes existing QT, it is not always clear why it is good, and if it fails, it is often equally unclear what could be done to improve its reliability. Since QT, ideally, should not lead to a failure, it is unable to provide the ultimate information about reliability — the probability of the field failure.

HALT, unlike QT, is first of all aimed at understanding the underlying Physics of Failure (PoF) by detecting possible failure modes and mechanisms. Adequately planned, carefully conducted, and properly interpreted, HALT provides a consistent basis for the prediction of the probability of failure under given loading (stress) conditions and after a given time in service. HALT information enables effective decisions on what could be changed, if necessary, to design and manufacture a reliable product. A functional, structural, material, or technological improvement can be translated, using HALT data, predictive modeling (PM), and subsequent sensitivity analyses (SA), into a lower probability of field failure. Well-designed and thoroughly implemented HALT can dramatically facilitate the solutions to many engineering and business-related problems associated with cost effectiveness and time-to-market.

It is highly desirable that HALT is conducted in addition to, and preferably before, QT. There might also be situations when HALT can be used as an effective substitution for QT, especially for new products, when suitable QT and standards do not yet exist. It is the HALT that reveals the reliability physics behind the product and, ultimately, to create a product with a low and, if necessary, even specified, predicted, and controlled probability of failure. Technical diagnostic, prognostics, and health monitoring and management can play an important role in such an effort.^{1,5}

Predictive Modeling (PM)

HALT, when aimed at the prediction of the likelihood of the field failure, cannot do without simple and meaningful

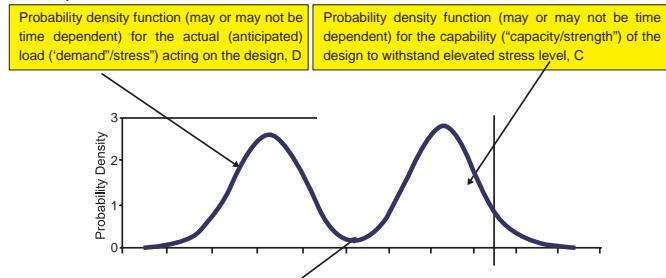
AT Category	Product Development Testing (PDT)	Qualification Testing (QT)	Highly Accelerated Life Testing (HALT)
Objective	Technical feedback to ensure that the taken design approach is viable	Proof of reliability: demonstration that the product is qualified to serve in the given capacity	Understand reliability physics (modes and mechanisms of failure) and assess the likelihood of failure field
End point	Time, type, level, and/or number of failures	Predetermined time, number of cycles, and/or the excessive (unexpected) number of failures	Predetermined number or percentage of failures
Follow-up Activity	Failure analysis, design decision	Pass/fail decision	Failure analysis of the test data
Ideal Test	Specific definitions	No failure in a long time	Numerous failures in a short time

Table 1. Accelerated Test Categories

PM.^{6,7} It is on a PM basis that one decides which HALT parameter should be accelerated, how to process the experimental data, and, most importantly, how to bridge the gap between the HALT data and the likelihood of field failure. By considering the fundamental physics that might constrain the final design, PM can lead to significant savings of time and expense. The most widespread HALT models are aimed at predicting the MTTF. Here are some examples and typical use:

- Power law (used when PoF is unclear)
- Boltzmann-Arrhenius equation (used when elevated temperature is the major cause of failure)
- Coffin-Manson equation (an inverse power law used to evaluate low cycle fatigue life-time)
- Crack growth equations (used to evaluate fracture toughness of brittle materials)
- Bueche-Zhurkov and Eyring equations (used to consider the combined effect of high temperature and mechanical loading)
- Peck equation (to evaluate the combined effect of elevated temperature and relative humidity)
- Black equation (to evaluate the combined effects of elevated temperature and current density)
- Miner-Palmgren rule (to assess fatigue lifetime when the yield stress of the material is not exceeded)
- Creep rate equations
- Weakest link model (applicable to extremely brittle materials with defects)
- Stress-strength (demand-capacity) interference model, which is perhaps the most flexible and well substantiated model (**Figure 1**).

The curve on the right should be obtained experimentally, based on the HALT and on the accumulated experience. The bearing capacity of the structure should be such that the probability of failure be sufficiently low, and the probabilistic SF not lower than the specified value. In a simplified analysis the curve on the right could be substituted, particularly, by a constant value, which, if a conservative approach is taken, should be sufficiently low.



The larger is the overlap of these two curves, the higher is the probability of failure, and the lower is the SF. After these two curves are evaluated (established) for each reliability characteristic of interest and for each moment of time one should evaluate the probability distributing function, $f(\Psi)$, for the safety margin, $\Psi = C - D$, its mean, $\langle \Psi \rangle$, and standard deviation, \hat{s} , and then - the safety factor, $SF = \langle \Psi \rangle / \hat{s}$ that shouldn't be lower than the specified value.

Figure 1. Stress-Strength (Demand-Capacity) Interference model

Various predictive models, whether analytical (mathematical) or numerical (simulations), not only those that are directly related to HALT, can be extremely helpful to understand the PoF and to optimize the performance, lifetime, and cost effectiveness of the item of interest.^{6,7}

Typical HALT

Figure 2 through **Figure 9** illustrate a typical HALT effort.

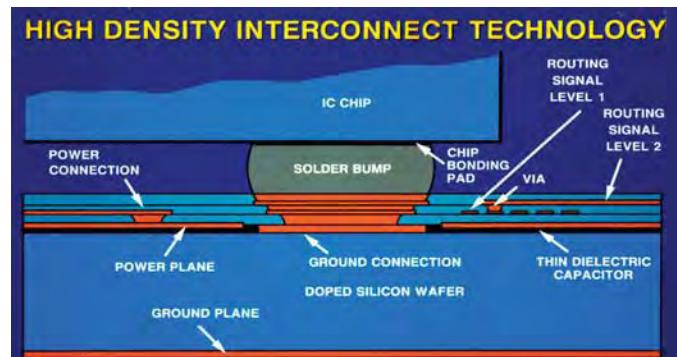


Figure 2. Solder joints are expected to be the most vulnerable structural elements in Si-on-Si high density interconnect technology, but how reliable are they in a thermally matched assembly?

Schematics Showing Locations of Thermal Fatigue Cracks

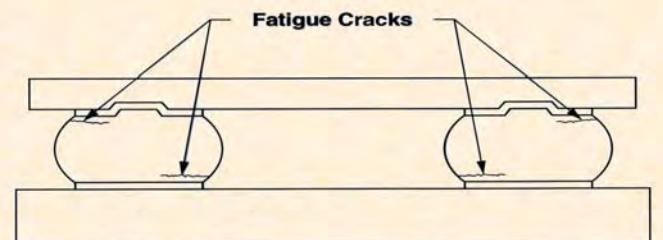


Figure 3. Understanding the reliability physics: low-cycle fatigue in a ductile solder material gets initiated at the areas of high stress concentration

CIRCULAR CYLINDER CLAMPED AT ITS END PLANES

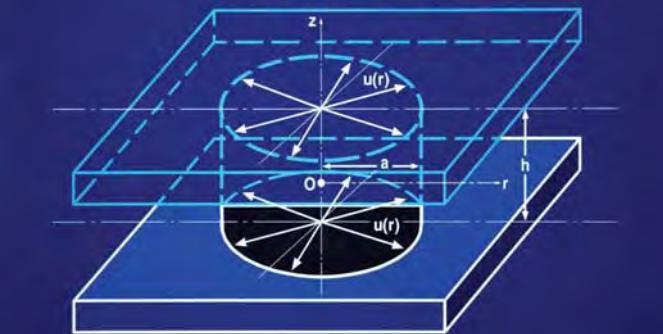


Figure 4. Analytical predictive modeling: a solder bump is idealized as a short circular cylinder

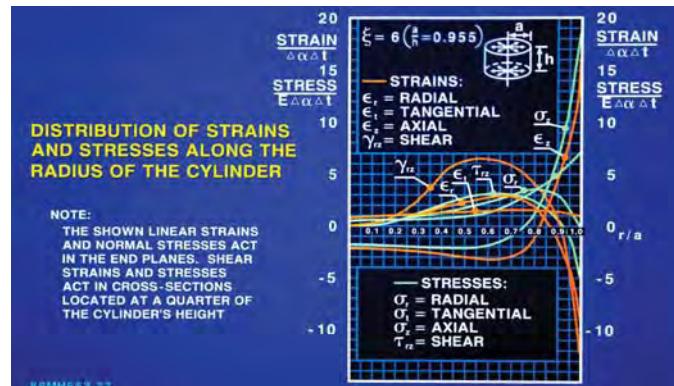


Figure 5. Predicted stresses and strains based on the analytical model

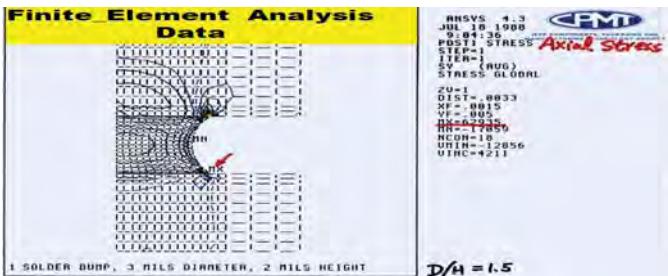


Figure 6. Predicted stresses and strains based on the Finite Element Analysis (FEA) model

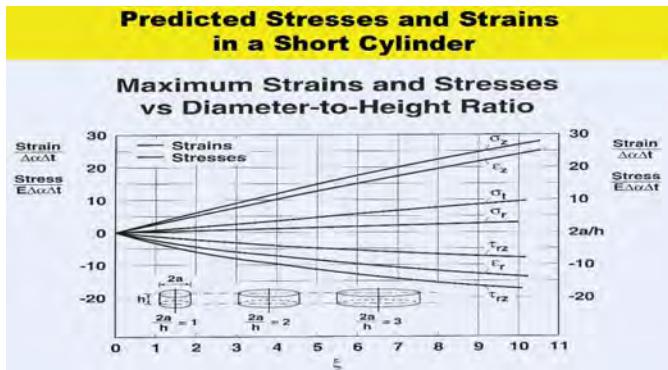


Figure 7. Effect of the solder bump aspect ratio on the stress/strain level as predicted by analytical modeling

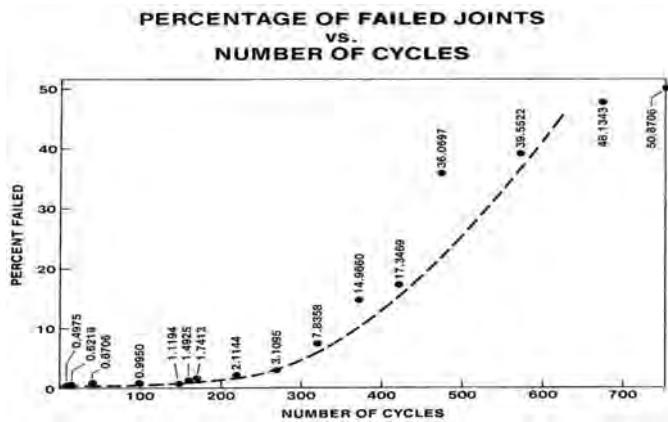


Figure 8. HALT Results

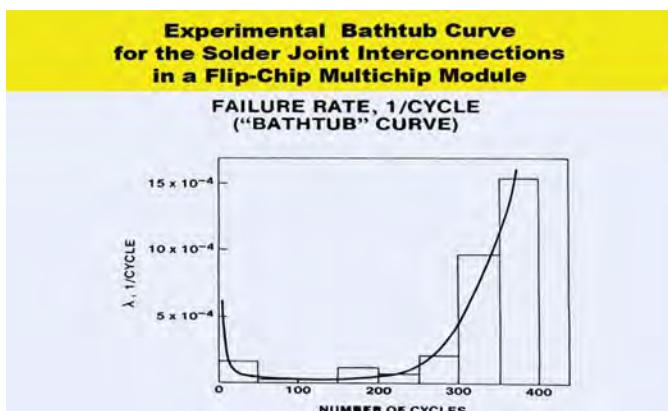


Figure 9. Experimental bathtub curve: about half of the lifetime of the solder joint is in the wear-out phase

Design for Reliability (DfR)

DfR is a set of approaches, methods, and best practices that are intended to be used during the design phase of a product to minimize the risk that the product might not meet reliability requirements and customer expectations. The traditional, deterministic DfR approach proceeds from the notion that reliability can be assured by introducing a sufficiently high Safety Factor (SF), defined as the ratio $SF = C/D$ of the capacity (strength), C , of the item (device, system) to the demand (stress), D . The SF level depends on the consequences of failure, the acceptable risks, the trustworthiness and accuracy of available information about capacity and demand, the possible costs and social benefits, the variability of materials and structural parameters, the fabrication procedures, and perhaps other factors, and is being established from the previous experience for the system of interest considering the anticipated environmental or operation conditions. A PDfR approach brings in the probability dimension to each of the DfR characteristics of interest. When this approach is employed, the reliability criteria are, in effect, acceptable probabilities of failure. Using HALT data and PM techniques, a PDfR approach enables the establishment of such a probability (whatever the definition might be for a particular product or case) for the given operational conditions and for the given duration of operation. After the PDfR predictive models are developed, SA should be conducted to determine the most feasible materials and geometric characteristics of the design, so that the acceptable probability of failure is determined and achieved. In other cases, the PDfR approach can be helpful in establishing the most feasible compromise between the reliability and cost effectiveness of a product. A possible PDfR approach could be based on the stress-strength (interference) model.

The reliability of an item that is discarded when it fails is characterized by its dependability (probability of non-failure). This is defined as the probability $P = P/C \Delta D = P/\psi = C - D \Delta D$ that the item's bearing capacity (strength), C , during the time, t , of operation under the given conditions, is greater than the demand (stress), D . The Safety Margin (SM) $\psi = C - D$ is a random variable. The probabilistic Safety Factor $SF = \frac{\psi}{\sigma_\psi}$ is a non-random reliability criterion defined as the ratio of the mean value, $\bar{\psi}$, of the SM to its standard deviation (STD), σ_ψ , for the particular reliability characteristic of interest. The probability, P , of non-failure, when the SM is normally distributed, is $P = 0.999$ for $SF = 3.090$, $P = 0.9999$ for $SF = 3.719$, $P = 0.99999$ for $SF = 4.525$, and $P = 0.999999$ for $SF = 4.752$. As is evident from this data, the probabilistic SF is more sensitive to the possible changes in the design than the probability of non-failure, and therefore its use is more convenient. In electronic systems, C and D usually change in time. Failure occurs when D becomes equal to or larger than C . This random event is known as the time-at-failure, and the duration of operation until this moment of time is a random variable. The corresponding $SF = MTTF/STD$ is determined as the ratio of the mean value of this duration to its standard deviation.

As a simple example, examine a device whose MTTF, τ , during steady-state operation, follows the exponential law of

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reliability and whose PoF can be adequately characterized by the Boltzmann-Arrhenius equation $\tau = \tau_0 \exp\left(\frac{U}{kT}\right)$. The failure rate is therefore $\lambda = \frac{1}{\tau} = \frac{1}{\tau_0} \exp\left(\frac{U}{kT}\right)$ and the probability of non-failure is $P = e^{-\lambda t} = \exp\left[-\left(\frac{t}{\tau_0} \exp\left(-\frac{U}{kT}\right)\right)\right]$. Solving this equation for the absolute temperature, T , we obtain $T = -\frac{U}{k \ln\left[\frac{\tau_0}{P} \left(1 - \ln P\right)\right]}$. As an example, consider a surface charge accumulation failure for which $\frac{U}{k} = 11600 \text{ K}$, and let the τ_0 value predicted by HALT be $\tau_0 = 2 \times 10^{-5} \text{ hours}$. Suppose the customer requires that the probability of failure at the end of the device's service time $t = 40,000 \text{ hours}$ does not exceed $Q = 10^{-5}$. Then the above formula indicates that the steady-state operation temperature should not be higher than $T = 352.3 \text{ K} = 79.3^\circ\text{C}$ and so the thermal management equipment should be designed accordingly. This elementary example gives a feeling of how the PDfR concept works and what one could gain by using it. Other examples can be found in **Reference 8** and **Reference 9**.

As to the reliability of a complex product (system), it is characterized, first of all, by its availability, which is the probability that the system is available to the user when needed. High availability can be achieved by employing the most feasible combination of dependability on one hand, and repairability, maintainability, and maintenance support on the other.

The most general PDfR approach is beyond the scope of this article. This approach could be based on the use of probability density distribution functions for the probabilistic reliability characteristics of importance (such as electrical parameters, light output, heat transfer capability, mechanical strength, fracture toughness, maximum/minimum temperatures, and maximum accelerations/decelerations) and the factors affecting these characteristics (such as high/low temperatures, electrical current/voltage, electrical/optical properties of materials, mechanical and thermal stresses, and displacements).

New Qualification Approaches Needed?

The short-term, down-to-earth, practical goal of a device manufacturer is to conduct and pass the established QT specification, without questioning whether or not it is perfect. The ultimate,

long-term, broad goal of the industry is to make its deliverables reliable in the field. QT is the major means of making viable-and-promising devices into reliable-and-marketable products. It is well known, however, that devices that pass existing QT often fail in the field. Is this indeed a problem? Are the existing QT specifications adequate? Does the industry need new approaches to qualify its devices into products? If it does, could today's QT specifications and procedures be improved to an extent that, if the device passed these tests, its performance in the field is quantified, predicted, and assured?

We argue that such improvements in QT, as well as in existing best practices, are indeed possible, provided that PDfR methodologies are widely and consistently employed. One effective way to improve the existing QT and specifications is to do the following:

1. Conduct HALT on a much wider scale than today, and, if HALT is aimed at the prediction of a field failure, PM must also be performed.
 2. Carry out, whenever and wherever possible, PM to understand the PoF and to quantify the expected reliability of the product
 3. Revisit, review, and revise the existing QT and specifications based on the HALT data first considering the most vulnerable elements of the device of interest
 4. Develop and widely implement the PDfR methodologies keeping in mind that "nobody and nothing is perfect", that the probability of failure is never zero, but could be specified, predicted, minimized and, if necessary, controlled and maintained at an acceptable low level.
- It goes without saying that these activities should be conducted on an ongoing basis.
- If QT has a solid basis in HALT, PM, and PDfR, then there is reason to believe that the product of interest will be sufficiently robust in the field. In such a situation, the (still non-destructive) QT could be viewed as a "quasi-HALT" or an "initial stage of HALT" that more or less adequately replicates the initial non-destructive stage of HALT. We believe that such an approach to qualify devices into products would enable the industry to

specify, and manufacturers to assure, a predicted and low enough probability of field failure for a device that passed QT. We expect that the suggested approach to the QT will be accepted by the engineering and manufacturing communities, implemented into engineering practice and be adequately reflected in future editions of the QT specifications and methodologies.^{8,9}

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Challenges in Supply of Ultra-low Alpha Emitting Solder Materials

By Andy Mackie, PhD [Indium Corporation] and Olivier Lauzeral [iROC Technologies]

The names of high-energy subatomic particles such as alpha, beta, gamma, heavy ions, X-rays, and cosmic rays are well known to every high-school student (**Table 1**). In aerospace electronics, any of these

Particle Name	Description
Alpha	Helium (He^4) nucleus (2 protons + 2 neutrons)
Beta	Electron or positron
Gamma-, X-rays	Electromagnetic (photon)
Thermal Neutron	Uncharged nuclear particle
Cosmic rays	Mixture of mostly beta, with alpha, gamma and other types
Heavy ions	Charged nucleus

Table 1. Most Common Subatomic Species

particles may be encountered, and each presents a unique challenge for applications such as telecommunications satellites. At sea level, in addition to specific types of cosmic ray (fast neutrons) and thermal neutrons that can directly affect die, semiconductor packaging experts are concerned with alpha particles due to the increasing need for controlled alpha-emissions in materials immediately adjacent to the chip surface. This need is driven primarily by the shrink in individual semiconductor device sizes (characterized by the “equivalent DRAM gate length”¹ present in the active device layers of a semiconductor die.

An alpha particle is an ionized particle that has a high ability to transmit its charge to its environment, creating the condition for ‘single event upsets’ (SEUs) to occur. These particles are emitted spontaneously from the nucleus of a specific, high-atomic-weight isotope (usually >200 Daltons) atom. They can also result from a collision between a fast neutron and a light element’s nucleus, such as silicon (Si) or oxygen (O), or be a recoil product of a fission reaction between a thermal neutron (kinetic energy around 25 MeV) and B¹⁰.

The elements Uranium (U) and Thorium (Th) hold particular interest and concern for semiconductor fabricators, as they both decay to give stable isotopes of lead (Pb),

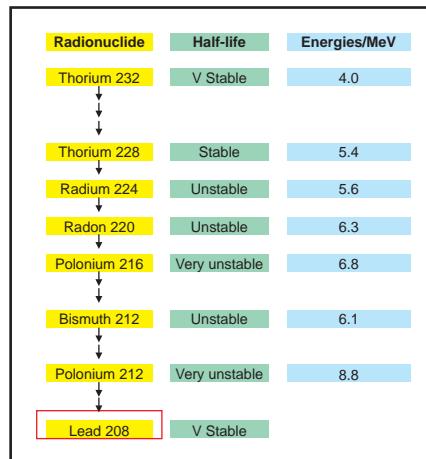


Figure 1. Decay series for Thorium

and so are found associated with lead ore. By decaying, they give rise to alpha particles. The potential energy of the particle depends on the nucleus from which it is emitted. **Figure 1** shows the decay series (only alpha emissions shown) for the isotope Thorium 232. As can be readily seen, the highest energies correlate with greater nuclear instability (shortest half-lives).

The energy (in mega electron Volts, MeV) dictates the velocity — hence the penetration depth — of the alpha particle, which may be traveling at a significant fraction of the speed of light.

Thermal neutrons are also a source of concern in semiconductor applications where B¹⁰ is used, as this isotope can capture thermal neutrons in a fission reaction to produce alpha particles, a gamma ray, and a lithium ion.²

False Protection

Protection against these high-energy alpha particles is often counter-intuitive. As mentioned, the kinetic energy of the alpha particle is (from $\frac{1}{2} m \cdot v^2$) a measure of the velocity. As the particle interacts with the lattice structure, it slows down, creating

pairs of holes and electrons (+ and -), until it finally absorbs two electrons and forms a helium atom. Therefore, it makes sense to put a “protective” layer in the way to shield the active semiconductor layer from accumulating a charge. Unfortunately, this may act to bring the doped-ion wells of the active layer closer, where the slowing alpha particle generates more electron/hole pairs as it slows down (**Figure 2**). Like a firework extinguishing in a final flare of glory, more pairs are generated as the alpha particle’s interactional cross-section grows and finally slows to a stop (red dot in **Figure 2**) in a phenomenon known as the Bragg Peak.³

Over the last several years, JEDEC members have led efforts to determine the extent of semiconductor device sensitivity (specifically memory devices such as SRAM memory and register) to these types of particles and neutrons, using both ambient-level and accelerated particle conditions.^{5,6} Less well-known is the ability of alpha-particles and other high-energy phenomena to cause “latch-up”, where a P-N-P-N junction (effectively two transistors with a common well) are locked into a conductive mode that persists even after the signal is removed. This type of phenomenon is becoming a real cause for concern in high-temperature power semiconductor electronics due to the use of thinner wafers and high-Pb solders (high surface areas) as die-attach materials.

Materials Affected

It is no surprise that materials suppliers for advanced electronics and semiconductor assembly are constantly being asked to meet

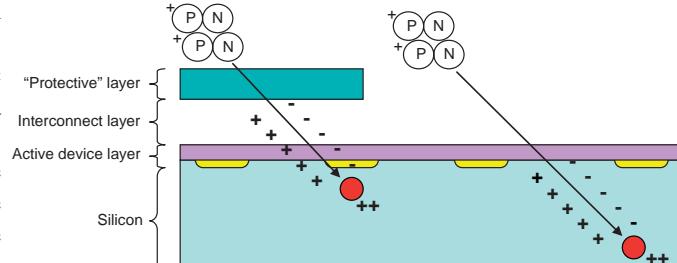


Figure 2. Effect of “protection” on the depth of the Bragg Peak

increasingly stringent requirements for performance criteria as well as adherence to standards. Most readers from a surface mount technology (SMT) background will be familiar with RoHS and similar global requirements for low-lead (Pb) in solders. They may also be familiar with the requirement for low halogen levels, originally driven by environmental needs, and now driven in semiconductor packaging by a requirement for increased compatibility with underfill materials (flip chip) and reduced damage to bondpads (power die-attach applications). Low-alpha emitting materials are the latest addition to that list of customer requirements.

For flip chip and similar applications, the primary low alpha and ultra-low alpha (ULA) emitting materials of interest are those immediately adjacent to the chip surface. With the move from solder bumps to copper pillar for sub-100 μm chip-attach designs, these materials include:

- Organics such as capillary underfills, wafer-level underfills (polymer-collar), photoresists, ABF, solder mask, substrate epoxy, fluxes, and molding compounds.
- Inorganics such as dielectrics, fiber filler in substrate, and “filler” in capillary underfills.
- Metals such as solder, UBM, and copper traces.

Although materials sent for testing to iRoC Technologies are occasionally found to be “hot” (exhibiting high alpha emissivity), the usual assumption is that organic materials are relatively easy to obtain free of uranium and thorium isotopes. Therefore, solder is the key focus-point for spontaneous energetic particle emissions. Experiments have shown that even low levels of lead (Pb) in a tin/silver/copper (SAC) alloy can emit levels of alpha as high as 0.3cph/cm²; or over 2 orders of magnitude higher than the increasingly accepted ULA of 0.002cph/cm².

Note that emerging copper-pillar applications, such as Tessera’s microPILR™, also use solder as a means of attaching the copper pillar to the land on the substrate⁷ and will need to be carefully selected and specified for ULA emissions.

Measurement of Alpha Emissions

Clear test method definitions⁸ are forthcoming from JEDEC, although some companies (both materials suppliers and users) have set their own specifications for terms such as “low alpha” and ULA. The work by JEDEC and associated industry groups indicates that a level of 0.002cph/cm² is considered an acceptable level and should be designated ULA.

Equipment that allows an investigator to determine the energy of a particle, and therefore more accurately “fingerprint” the source of the particle, is becoming available. However, in current state-of-the-art analytical equipment, the accelerating voltage used to detect alpha particles is balanced to ensure on the one hand that low-energy alpha particles are detected, but also to ensure that other particles are not detected or are at least minimized. This usually means that the sensitivity of the detector is reduced by around 10%, and has to be accounted for in the final calculation of the particle flux.

If the signals detected were known to originate from a single known source present only in the material under test, then it should be possible to eliminate any need for background measurements. However, for such a sensitive test method, “false positives” are a frequent occurrence, classified as either from:

- Interfering high energy sub-atomic particles like cosmic rays or stray neutrons
- The measurement system itself due to RF interference or voltage spikes in the supply voltage
- Naturally-occurring Radon gas
- Cross-contamination from other sources, such as dust or previous studies

Specimen Preparation

Accurate measurement of particle alpha emissions relies on a large surface area of the material under study. Typically, a large metal pan of around 1,000cm² forms the bottom of a hermetically-sealed unit, with a cleanable plastic tray that fits inside the pan to hold the material that is under test. The material is spread into a thin film in the tray. A thin plastic (usually 0.002” thick Mylar) film is then stretched over the tray, with care taken to minimize air entrapment between the material in the tray and the plastic film (**Figure 3**). The metal pan is



Figure 3. Material specimen ready for alpha emission study

then sealed into the alpha-counter, and a flow of P10 gas passes over the surface of the plastic film and out into the counting chamber. P10 contains a combination of 90% argon and 10% methane, called the “counting gas”, and is used because it ionizes to CH₄⁺ and Ar⁺ very easily (low ionization energy).

Sensitivity of Alpha Emission Measurement Methodology

The test method’s sensitivity depends greatly on the extent of the measured background radiation. The latest gas flow proportional counters on the market have ultra-low background (as low as 2cph) thanks to a constant improvement in materials and manufacturing processes. However, this best-case background signal is equivalent to 2cph/1000cm² or 0.002cph/cm²; the same level as the highest allowable ULA emission level. The best-case signal/noise ratio for ULA materials is therefore less than 1:1, which severely limits the sensitivity of the analytical methodology and necessitates long periods of study to ensure precision. Even then, precision to four decimal places (such as 0.0020cph/cm²) is impossible to guarantee. Note that the forthcoming JEDEC document discusses the statistical analysis of the data, and best analytical practices in great depth.

It is also important to reliably quantify the background level of radiation both before and after every single measurement to ensure that cross contamination, background radiation shifts, and analyzer sensitivity drift are accounted for accurately.

Manufacture of ULA Materials

Each time a ULA-material (especially metal in molten state) is exposed to other materials, the chance of diffusion, and hence contamination, increases. Alpha-emitting materials range from ambient Radon gas

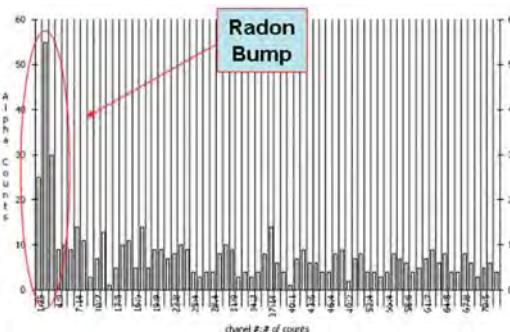


Figure 4. Alpha emission reading vs. time

(Rn), which is a natural breakdown product of specific uranium and thorium isotopes, to dust with adsorbed radon, and other materials that can contaminate. Experience at Indium Corporation has shown that all potential sources of alpha-emitting isotopes need to be accounted for and eliminated either by prudent choice of materials of construction of manufacturing equipment, or (in the case of ambient radon) by purging.

Because it is a non-persistent gas and because its half-life is short, Radon is not considered a legitimate source of concern for ULA materials usage, and test labs in both Asia and in the US do not control for Radon in the environment during sample preparation, although it naturally purges

from the system as the P10 gas flows over the Mylar film covering the test specimen (**Figure 4**). Therefore, key gating alpha-emissions test points need to be set up for consistent supply of low-alpha material. For a manufacturer of solder pastes there are four separate critical points:

1. Incoming raw materials (flux ingredients and solders)
2. Solder powder
3. Flux
4. Final solder paste

If each separate ingredient (1-3) is below the desired limit, then that is a good indicator, but not a definitive one, that the material is suitable for use. Particularly for a no-clean solder paste where the residues are not cleaned, measurement of the alpha emissions for the outgoing paste are the final guarantee of the alpha emission level of the product.

Another critical factor for maintaining total control of alpha emissions is purchasing materials from suppliers whose materials are in “secular equilibrium”. That is, that the alpha emission is from an isotope at the bottom of the decay series that is not increasing in concentration as a result of a

faster-decaying parent isotope. A material in secular equilibrium therefore has maximum particle emission at time zero, and the alpha emissions will then only decrease over time. ☀

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Sensible Solutions... Fast!

Wire Bonding . . . It's Not Going Away Any Time Soon

By Gil Olachea [AZ Tech Direct, LLC]

Of all the topics that appear to be perennial, one must be wire bonding. So, in this brief presentation, what aspect of the subject do I ignore, neglect, or obfuscate? The intent of this piece is not to distinguish the merits or demerits of one process or material to another, but rather to expose the industry's present and future growth of the most common second-level interconnects in semiconductors — wire bond.

Let's state the obvious and then dive into the areas that are of real interest. Today, gold wire ball bonding owns approximately 85% of the second-level interconnect market (it's only been about 3-5 years since copper wire bond was primarily an R&D "toy"). The balance is shared by a combination of aluminum-stitch, solder-bump, ribbon, and (the hot topic) copper. I'll touch on a couple of these, yet focus on the increasingly popular copper wire-bond technology. We know the traditional market drivers and trends like the 7 dwarfs: smaller, thinner, faster, portable, modular, scalable, and cheaper. But here are a few I've encountered that are attracting greater attention:

- Electric vehicles and control modules
- High-power LEDs
- Renewable energy (solar, wind, "green" power)

An Overall Assessment

During the first half of the calendar year, we witnessed a robust growth in wire-bond equipment acquisition, copper wire implementation, and a continued focus on cost reduction. Despite the ebb and flow of the electronics markets, advancing handheld electronics, and sophisticated components and materials, products are continuously seeking cost-effective, profit-building solutions. The predictable evolution of new products driven by portability, weight, and size has accelerated, and continues to accelerate, the need for a high-performance inter-connect — wire bond. This mode of connection between chip and board dominates the market for



Figure 1. Ultra-fine-pitch, 35 μm Ball Bonder (Courtesy: KnS)



Figure 2. Gold Ball Wire Bonder (Courtesy: Shinkawa)

very compelling reasons such as overall cost, installed equipment base, available materials, support, and adoption level.

A variety of industry research firms claim that today's entire market utilizing ball-bond technology is well over 10 trillion bonds. If copper wire bond represents 10% (yes, a debatable number) of the market, that is a sizable market; and it's growing. Therefore, how can this dynamic and upwardly moving market be neglected?

"Copper ball bonding has reached critical mass, although gold ball bonding continues to dominate the market," states Doug Day, General Manager, Shinkawa USA, Inc. He continues, "In the IC arena, copper bonding has become widely accepted and is maturing, both in terms of new equipment sales and conversion of existing equipment."

Copper Wire Bond

An inevitable migration, copper wire bonding represents many benefits, and drawbacks. The most obvious of benefits

is the dramatic reduction in cost of material (today, about a factor of 12 that of gold), followed by improved thermal management, higher power capability, increased electrical performance, high I/O capability, and fine pitch, to list a few.

A number of years ago, copper was touted as the rapid replacement for gold wire but prices of this precious metal kept copper at bay. However, the huge increase in gold prices in the past few years has accelerated the market readiness for, and adoption of, copper. A tremendous amount of time and money has been invested in cultivating copper wire-bond technology to create a viable contender to gold wire bond. The primary issue in implementation of copper wire is the material itself and the resultant bond integrity. Much time and financial resources have addressed the largest of obstacles, excess oxidation. A micro-environment of "forming" gas is created around the bond capillary. This is, simply put (yet a technical success), a micro-sphere of nitrogen-doped gas to

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inhibit oxidation of the interconnect surfaces at the moment of bond. Once the bond has been formed, the oxidation issue has dissipated. While additional focus is being placed upon copper wire improvements to reduce the need for this forming-gas environment, the immediate performance increases in cost, electrical, thermal, and reliability are being heralded, but not without compromise. Among the challenges are bond pad deformation, ultra-sonic pressure, increased wire stiffness, higher potential for destroying active under-bond structures, mold compound interaction, wire shelf life, capillary life, and ensuring bond integrity as good as gold.

Copper wire bond has two major drawbacks: reduced wire-bonder throughput and material shelf life. Though these two problem areas will be resolved, they are apparent today. The aforementioned forming-gas environment requires time and that spells reduced productivity. Due to the rougher surface texture of copper wire, capillary life is roughly 30-50% that of a gold wire capillary. New wire alloy formulations, capillary technology, and bond pad structures will resolve these matters.

Shelf life will also become a moot issue. Today, however, gold wire can be securely stored for about a year and possibly longer with recertification. Copper wire in proper environments will store for three to six months. Additionally, the exposure of



Figure 3. Dual Bond Head Ball Bonder (Courtesy: ASM Pacific)

copper wire spools while on the bonder quickly exacerbates the oxidation issue and the useful life of the spool. These are minor setbacks today and will be resolved in the very near future.

Chip Challenges and Equipment Advancements

Copper formed wire is not the only problem area for this bond technology. The ICs that utilize this technology also present their set of issues, among which are bond pad sizes and structures, pad metallization schemes, under-bond active areas, and low-k dielectrics. Additionally, requalification of chips for bond pad metal schemes represents a costly endeavor and thus makes for questionable adoption of a harder copper wire to form a cost-effective, reliable bond. Many chip manufacturers are holding out for a new device rather than invest now for a copper wire-bond conversion.

At the bonder system level, equipment manufacturers must implement a sophisticated cross section of technologies that weave software, electronics, and mechanical design. It's an art in choreographing the various technologies employed in bonders to achieve the end result of a reliable wire bond, gold or copper.

Advances such as on-the-fly capillary offset adjustment and automatic free-air ball size and sphericity control have improved bonding quality without time consuming inspection or adjustment. An example of a machine that addresses many of the above challenges is the Shinkawa UTC-3000 (**Figure 2**).

The ideal solution is a bonder that uses a capillary which can accommodate copper and gold wire on-the-fly. We'll see who the first manufacturer will be to introduce that capability.

Copper Wire Bond for All IC Packages?

As much euphoria as this may generate, copper is not the answer for everything. As is the case with other bonding solutions, copper wire bond is not the panacea for all packaging styles. There are some high-power ICs and modules where aluminum wire simply makes for an easier outcome at a favorable price point. Ribbon bonds (**Figure 4**) are designed to reliably handle massive amounts of current, improve electrical parasitics, and increase throughput, whereas



Figure 4. Ribbon Bond versus Wire Bond (Courtesy: Orthodyne and Semelab, PLC)

a multiple wire-bond equivalent increases opportunity for wire-bond failure or fusing (electrical current surge induced) while under operation. “The continuing trend to miniaturize power semiconductor packages has led to interconnect challenges. Traditional large diameter aluminum wires that carry high currents may not fit into the space constraints of low profile packages, such as PDFN, PQFN, and SO-8. We've produced various bond solutions for the power demanding portable markets . . .” shares Gary Silverberg, Semiconductor Product Marketing Director, Orthodyne Electronics.

Some IC packages that require precise, specialty work holders for the “fingers” of the lead frame pose a challenge to wire bonders, whether gold or copper, yet with greater demands for ultrasonic coupling and contact time, copper presents increased variables. An example of these type packages are QFN, ultra-fine pitch second bond geometries, and stacked chips. Shinkawa has invested heavily in mechanical and software solutions to overcome these challenges. Adds Doug Day, Shinkawa, “WLPs now form a major part of the (wire bond) market, and have created wire bond difficulties due to the popularity of QFN lead frames which defy wire bond conventions through the existence of large sections which cannot be clamped. We've developed solutions to bond QFNs with high quality and without sacrificing throughput.”

Aluminum wire-bonded products are of a special nature and cost constraints



Figure 5. Orthodyne's 7600 HD MA (Courtesy: Orthodyne)

keep this product area at arm's length from copper wire. Aluminum is still much less expensive than copper and, until the favor swings in the direction of copper, will remain king when it comes to an ultra-low cost interconnect material.

And the Rest of the Story . . .

The advanced technologies, such as 3-D, MEMS, and LEDs, truly have challenged the wire-bond manufacturers. Listing the many issues these products have presented would exhaust the scope of this article. Here are the top problems, past and present, facing equipment, software, and materials manufacturers:

- Looping control (software)
- Loop heights (ultra-low)
- Varied die thicknesses
- Scrub pressure and time
- Under-pad active circuitry
- Bond pad pitch
- Various pad metal schemes
- Die size/stacking
- PRS inaccuracies
- Reverse bonding
- Work clamping
- Metal alloys
- Encapsulant composites
- Increased inspections
- Chip-to-chip bonding
- Multifocus optics

An interesting point, LED market opportunities are fueling immediate growth demands on copper wire bonding. These semiconductor products are driven by growths in the range of 15% (annually) projected for the next 3 years. The various and vast lighting and flat screen (television, monitor, display, projector) end products are the primary absorbers of these items.

Conclusion

I am very optimistic about the future of copper wire bonding. Significant growth opportunities exist for very fine pitch, high I/O devices. Many IC assembly and packaging houses are quickly acquiring copper wire bonders to be aptly prepared to accommodate the expected swell in demand for this support. There will be obstacles in qualifying some products, packages, and molding materials, but (think of this, boys and girls) what has our business been doing the last 50 years but solving problems and bringing innovation to market! ☺

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Hesse & Knipps GmbH Vattmannstrasse 6 Paderborn D-33100, Germany Tel: +49-5251-1560-0 www.hesse-knipps.com				WM: Al WD: 17.5 - 500 BA: 380 x 500 Max. BF: 0 - 4,000 BR: > 120 mS at 2 mm PA: ± 3.0 um ZT: 30 - 110 Max.
Hybond 330 State Place Escondido, CA 92029 Tel: +1-760-746-7105 www.hybond.com	WM: Au WD: 12.7 - 76.2 BA: CM BF: 12 - 250 BP: 0 - 2.0 BT: 0 - 900 ST: < 250	WM: Al, Au, Other WD: 12.7 - 76.2 BA: CM BF: 12 - 250 BP: 0 - 2.0 BT: 0 - 900 ZT: 12 - 19 Max.		
Kaijo Corporation 3-1-5, Sakae-cho, Hamura-shi Tokyo 205-8607, Japan Tel: +81-42-555-2244 www.kaijo.co.jp			WM: Au WD: 15 - 75 BA: 56 x 80 Max. WP: 35 Min. BR: > 48 mS at CM PA: CM ST: CM	
Kulicke & Soffa Industries, Inc. 1005 Virginia Drive Ft. Washington, PA 19034 Tel: +1-215-784-6000 www.kns.com	WM: Au WD: 17 - 76 BA: 152 x 152 Max. BF: 10 - 250 BP: 0 - 2.5 BT: 10 - 1,000 ST: < 250	WM: Al, Au WD: 12.7 - 76 BA: 135 x 135 BF: 10 - 160 BP: 0 - 2.5 BT: 10 - 1,000 ZT: 12.7 Max.	WM: Au, Cu WD: CM BA: 400 x 330 Max. WP: 35 Min. BR: 48 mS at 2 mm PA: > ± 2.0 um @ CM ST: CM	WM: Al, Au, Cu WD: 18 - 76.2 BA: 406.5 x 355.6 Max. BF: 10 - 300 BR: > 183 mS at 2.5 mm PA: > ± 2.5 um @ CM ZT: 12.7 - 25.4 Max.

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INTERNATIONAL DIRECTORY OF WIRE BONDER SUPPLIERS

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COMPANY HEADQUARTERS	MANUAL/SEMI-AUTOMATIC		FULLY AUTOMATIC	
	BALL BONDER	WEDGE BONDER	BALL BONDER	WEDGE BONDER
Company Street Address City, State, Country Telephone Website CM = Contact Manufacturer	WM - Wire Material WD - Wire Dia. (um) BA - Bond Area (mm) BF - Bond Force (g) BP - Bond Power (W) BT - Bond Time (mS) ST - Stage Temp. (°C)	WM - Wire Material WD - Wire Dia. (um) BA - Bond Area (mm) BF - Bond Force (g) BP - Bond Power (W) BT - Bond Time (mS) ZT - Z-axis Travel (mm)	WM - Wire Material WD - Wire Dia. (um) BA - Bond Area (mm) WP - Wire Pitch (um) BR - Bonding Rate/Wire PA - Pl. Accuracy @ 3σ ST - Stage Temp. (°C)	WM - Wire Material WD - Wire Dia. (um) BA - Bond Area (mm) BF - Bond Force (g) BR - Bonding Rate/Wire PA - Pl. Accuracy @ 3σ ZT - Z-axis Travel (mm)
Orthodyne Electronics Division of Kulicke & Soffa Industries 16700 Red Hill Avenue Irvine, CA 92606 Tel: +1-949-660-0440 www.orthodyne.com		WM: Al, Au WD: 25 - 75, 100 - 500 BA: 250 x 150 Max. BF: 10 - 3,500 BP: 0 - 80 BT: 0 - 255 ZT: 50 Max.		WM: Al, Au WD: 25-75, 100-500 BA: 70 x 70 Max. BF: 10 - 3,500 BR: CM PA: ± 8 - 12 um ZT: 50 Max.
Palomar Technologies, Inc. 2728 Loker Avenue West Carlsbad, CA 92010 Tel: +1-760-931-3600 www.palomartechologies.com			WM: Au WD: 17.8 - 44.5 BA: 305 x 152 Max. WP: 50 Min. BR: 125 mS at CM PA: ± 2.5 um ST: CM	
Planar Corporation 2 Partizansky Ave. Minsk 220033, Republic of Belarus Tel: +375-17-223-7211 www.planar.by	WM: Au WD: 17 - 75 BA: 65 x 65 BF: 10 - 150 BP: 0 - 4.0 BT: 10 - 250 ST: < 300	WM: Al, Au WD: 17 - 500 BA: 100 x 200 Max. BF: 10 - 1,000 BP: 0 - 4.0 BT: 1 - 999 ZT: 6 - 14 Max.	WM: Au WD: 18 - 50 BA: 50 x 50 WP: CM BR: 100 mS at CM PA: ± 4.5 um @ CM ST: < 400	WM: Al WD: 10 - 500 BA: 60 x 60 BF: 150 - 3,000 BR: 800 mS at 5 mm PA: ± 15 um @ CM ZT: CM
Questar Products International, Inc. Santa Rita Road, # 270 Pleasanton, CA 94566 Tel: +1-925-461-0100 www.questarproducts.com	WM: Au WD: 17.8 - 76.2 BA: 101.6 x 101.6 BF: CM BP: CM BT: CM ST: CM	WM: Al, Au WD: 17.8 - 76.2 BA: 101.6 x 92.7 BF: CM BP: CM BT: CM ZT: CM		
Shinkawa Ltd. 2-51-1 Inadaira, Musashimurayama-shi Tokyo 208-8585, Japan Tel: +81-42-560-1231 www.shinkawa.com			WM: Au WD: 15 - 38 BA: 66 x 80 Max. WP: CM BR: > 50 mS at 2 mm PA: ± 2.0 - 3.5 um ST: 300 - 320	
TPT GbR Lärchenweg 59a Karlsfeld D-85757, Germany Tel: +49-8131-58604 www.tpt.de	WM: Au WD: 17 - 76 BA: CM BF: 15 - 150 BP: 0 - 2.0 BT: 15 - 5,000 ST: < 250	WM: Al, Au WD: 12.5 - 75 BA: CM BF: 15 - 150 BP: 0 - 2.0 BT: 15 - 5,000 ZT: 15 Max.		
Ultrasonic Engineering Company, Ltd. 1-6-1, Kashiwa-cho, Tachikawa Tokyo 190-8522, Japan Tel: +81-42-536-1212 www.cho-onpa.co.jp		WM: Al WD: 25 - 50, 75 - 500 BA: 104 x 104 BF: CM BP: CM BT: CM ZT: CM		
West-Bond Inc. 1551 S. Harris Court Anaheim, CA 92806 Tel: +1-714-978-1551 www.westbond.com	WM: Au WD: 17.8 - 50.8 BA: 152.4 x 231.8 Max. BF: 10 - 250 BP: 0 - 5.0 BT: CM ST: CM	WM: Al, Au, Other WD: 17.8 - 152.4 BA: 152.4 x 231.8 Max. BF: 15 - 908 BP: 0 - 20 BT: CM ZT: 12.6 - 14.3 Max.		

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Contactors for Wafer-level Test

By Jim Brandes, Multitest

Wafer-level test is a relatively new paradigm for integrated circuit (IC) test. Simply put, it is final test that is performed on a wafer prober. Wafer-level test is made possible by wafer-level packaging (WLP), which adds a redistribution layer (RDL) to the surface of each die on the wafer. The redistribution layer routes signals from the bonding pads to larger pads to which solder balls are added (**Figure 1**). The redistribution layer also creates a hermetic seal on the die's active surface.

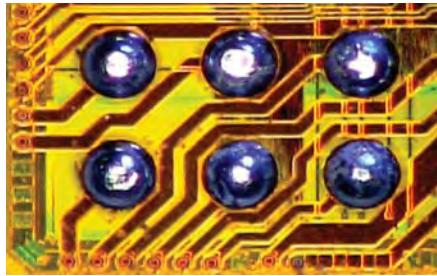


Figure 1. Corner of a WLP, showing bonding pads, redistribution layer, and solder balls

Wafer-level test is mechanically similar to traditional wafer probe. The machine used to manipulate the devices to be tested (the prober) is the same, and the devices are still attached to one another on the wafer. The addition of the redistribution layer and solder balls create some mechanical differences (described later).

Electrically, wafer-level test is quite different than traditional wafer probe, which is typically an abbreviated test performed to confirm that the dice are functional and worth packaging. In recognition that packaging affects performance (and also due to the limitations of most traditional probe interfaces) a more thorough final test was traditionally performed after packaging. Since wafer-level devices are packaged at the wafer level, the test performed on them is the final test, and therefore must be as thorough and complete as the traditional package test.

Electrical Challenges of Wafer-level Test Contacting

When compared to traditional wafer probe, wafer-level contacting presents

several electrical challenges for the contacting hardware. In many cases, the contacting medium must conduct more current than required for wafer probe. This includes the steady-state current required for the device's power and ground, as well as the higher momentary currents that individual tests might require. To properly understand the ability of the contacting media to meet these requirements, they need to be thoroughly characterized by the supplier; tested in the material that is used (not in free air), at DC and various duty cycles; and with a reasonable temperature rise.

Second, since the wafer-level test must be thorough, the contacting medium needs low inductance to ensure power and ground stability while the device is switching under load. For power delivery, the lower the inductance of the path, the better it will perform.

There is often a misunderstanding that lower inductance means better high-frequency performance. This idea results from the fact that for decades, contact media had several nanoHenrys, if not tens of nH, of inductance. At those levels, decreasing the inductance improved performance. Once inductance is reduced to the point that it balances capacitance to create a matched-impedance environment, there is no benefit—but rather a detriment—to further reduction.

For high-frequency performance, impedance and bandwidth are more important characteristics. Once again it is critical that the supplier thoroughly characterize the contact media for a complete understanding of the high-frequency characteristics, as well as the parasitic inductance and capacitance. The characterization must also describe the test conditions, which includes the proximity of signal and return paths, path pitch, and dielectric material at a minimum. It is important to confirm that the WS test characteristics match the conditions under which the contactor is tested.

And finally, the contact medium must present a low, consistent resistance to

ensure accurate parametric measurements. In cases of extreme sensitivity to contact resistance (resistance measurements below an Ohm, critical voltage measurements, or voltage measurements taken under high current loading) Kelvin contact capability is also an important consideration.

Mechanical Challenges of Wafer-level Test Contacting

There are also mechanical challenges when comparing wafer-level test to traditional wafer probe.

In traditional wafer probe, contact is made to relatively clean, extremely coplanar contact pads on each die. Adding the RDL and solder balls greatly increases the coplanarity deviation of the die. Additionally, the solder balls are not as clean and have a thicker oxide layer than aluminum or copper bonding pads.

To properly function, the contact medium must have adequate compliance to compensate for the coplanarity deviations. (The wafer probe world uses the term overdrive, which is roughly equivalent to compliance.) Traditional probe media might have tens of microns of overdrive. Wafer-level test requires hundreds of microns of compliance.

The contact medium must also be presented with sufficient force to penetrate the tin oxide on the typical WLCSP device's solder balls. Where 6-10g was sufficient force for wafer probe, 20-30g is more appropriate for wafer-level test.

A contact tip geometry that presents a sharp profile also aids in the penetration by creating more pressure per unit of contact force, and a sharp geometry tends to remain freer of debris between cleanings. It is important to use the proper cleaning

Performance at WS test	Cantilever Probes	Vertical Probes	Membrane Probes	POGO-type Probes	Flat Probes
Inductance	5nH	2 nH	0.2 nH*	1.5 nH	1 nH
Conductance	0.4 A	0.5 A	0.2 A	1.7 A**	1.8 A**
Bandwidth	2.1 GHz	1.3 GHz	22 GHz	5.5 GHz	18 GHz
Compliance	0.05 mm	0.25 mm	0.25 mm	0.5 mm	0.5 mm
Force	6 - 10 g	6 - 25 g	16 g	20 g	25 g
Initial Cost	\$	\$\$	\$\$\$	\$\$	\$
Field-Servicable	Never	Sometimes	Never	Always	Always
* tip only					
** Steady-state current. Pulsed current higher.					

Table 1. Comparison of basic parameters of wafer-level probe technologies

medium and algorithm to keep the contact tips clean while maintaining their geometry.

Economic Considerations

The costs-of-ownership (CoO) of a wafer-level contactor falls into four primary areas. The first and most easily recognized is the initial price of the contactor. This includes both the durable and replaceable (wear) items in the contactor, as well as any non-recurring engineering (NRE) charges associated with the design of the semi-custom contactor. (Contactors are typically designed using a standard contact medium, but configured to match the device contact pattern and site spacing, as well as other user-dictated requirements.) While this is the easiest cost to use for comparison, it is not enough information to accurately and thoroughly understand CoO.

The next two items — long life and reasonable maintenance cost — are very closely related. To achieve a low CoO, an ideal contact medium allows field replacement of the individual conductive paths through the contactor. This replacement should not require special tools or extensive training. And the replacements should not be required frequently. The cost of the replacement and the time between replacements (expressed as number of touchdowns) taken together and added to the initial cost give an idea of the CoO over the life of a high-volume device. A simplified example is that a contact medium that costs twice as much is cheaper to use if it lasts three times longer.

High test yield is likely the most important cost-of-test item. A low-price contact solution becomes very expensive if it does not provide a high first-pass yield. Retests are expensive and even more so in the case of wafer-level test, which typically has high parallelism. If one failing device in a sixteen-site setup must be retested, all sixteen must be re-contacted.

Comparison of Available Probe Technologies

A number of available probe technologies were evaluated according to these electrical, mechanical and economic requirements (**Table 1**). These included cantilever-beam, vertical-probe, membrane-probe, traditional spring probe, and flat-technology probes.

Cantilever beam probes are the original wafer-probe technology. Although good for single-site wafer probing of perimeter

bonding pads, they're not suitable for wafer-level test because they are not readily capable of contacting arrays or multiple sites. The long, narrow circuit paths that the needles provide have mediocre to poor electrical performance. Their inductance and resistance are higher than ideal, they have poor bandwidth, and relatively low current carrying capacity. Additionally, cantilever beam probes have very little

compliance and lower force than is considered ideal.

Cantilever beam is a mature technology, and the prices of simple probe cards benefit from significant competition. If the application requires array contact, multiple sites, and/or Kelvin contact, the prices increase significantly. Cantilever beam needles can't be replaced individually in the field, and repair requires specialized

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Figure 2. Drawing of traditional POGO-type spring pin (*courtesy of Everett Charles Technologies*)



Figure 3. SEM photo of a flat probe: (*Courtesy of Multitest*)

equipment and expertise. Except for the simplest examples, the CoO of cantilever beams for wafer-level test is not good.

Vertical probe is also a mature technology. Unlike cantilever-beam, vertical probe does allow access to arrayed contact points, readily supports multiple sites, and allows Kelvin contact. It is probably the most commonly-used technology for wafer-level test today.

Vertical probe also has long, narrow paths to the target device, so suffers from mediocre-to-poor electrical performance, similar to cantilever-beam. It exhibits higher inductance and resistance than is ideal and lower bandwidth and conductance than is ideal.

The contact force for some of the vertical probe offerings is good at 25g, while for others it is too weak at 6g. They have poor-to-mediocre compliance of 125 to 300 μ m.

Vertical probes also suffer from a higher-than-ideal initial price. In many cases they are not field repairable, but when they are, individual probes can be replaced. (Typically, the finer the pitch the less likely the probes can be replaced in the field. Therefore Kelvin contacts are rarely field-repairable.)

Membrane probes have the best electrical performance of all the traditional wafer-probe technologies, matching the capabilities of many package-test contactors. Their bandwidth reaches up to over 20 GHz in some applications. Their inductance is offset by the fact that decoupling capacitors can be placed within the contact set close to the device. Contact resistance is mediocre at <200 mOhm, and conductance is poor at 200 mAmps.

Mechanically, membrane probes have good force capability at about 25g. They have reasonable compliance (250 μ m) but with a significant caveat; adjacent-contact variation cannot exceed 50 μ m. Further deviation will not only prevent contact, it can actually damage the probe set. This deviation could easily occur in the case of a missing solder ball.

CoO is the biggest drawback to membrane probes. They have the highest

initial price of all the contact technologies described here and while they can last a long time if they are not damaged, they are not field-repairable and usually not factory-repairable.

Traditional POGO®-type spring pins are another fairly mature technology that has been used to test packaged devices for over twenty years (**Figure 2**). Spring pins have evolved with package testing needs and are fully capable of final test. However, the smaller-diameter probes required for finer pitches tend to also be longer, which has a negative effect on all the electrical parameters: bandwidth, inductance, resistance, and conductance all suffer.

Traditional spring probes are up to the task mechanically, having been used to contact BGAs as long as there have been BGAs, and have plenty of compliance. However, smaller-diameter probes tend to have less force than is ideal.

Traditional spring probes also benefit from the maturity of the industry and the resulting competition. However, finer-pitch probes tend to be more expensive. Spring probes are almost always field-replaceable. And their straight-through design ensures footprint compatibility, allowing the user to switch from one vendor to another to find the best electrical performance, mechanical performance, and ultimately lowest CoO.

Flat-Technology Spring Probes

Flat-technology probes are emerging as the contact technology-of-choice for both package test and wafer-level test (**Figure 3**). They were developed in response to the demand for high performance probes with a lower price point and have only been available for the last few years.

There is no real secret to making a contact technology with high electrical performance. The path through the contactor cannot add to the signal integrity; only detract from it. So keeping the path as short as possible gives the highest possible performance. Flat-technology spring probes are a barrel-less architecture. The two plungers contact one another directly within an external spring.

The direct contact creates multiple parallel contact points, rather than the two serial

contact points in a traditional spring probe. This reduces contact resistance. The fact that the conductive elements have all external surfaces results in excellent plating quality — another factor in low resistance and long life. And the external spring provides the highest force relative to the probe length.

Flat probes provide excellent electrical performance; bandwidth to 25 GHz, inductance around one nH, conductance to several Amps, and resistance around 50 mOhms.

Mechanically, flat probes have compliance of 500 μ m and force up to 25g. They can be made with tip geometries to best match the application. And because of the design flexibility inherent in the technology, they can be designed with offset tips for Kelvin applications.

Like other spring pins, flat probes are field-replaceable without special tools or training. They have been proven to last 500 k — 800 k insertions in high-volume, production environments. And they are footprint compatible with other spring probes, so they can be dropped in to existing applications that are currently using spring pins (**Figure 4**).



Figure 4. Example of flat-probe technology in a wafer-level contactor

Flat probes are not without their shortcomings. They are currently limited in pitch to a minimum of 0.4 mm. 0.5 and 0.4 pitch are the WLCS mainstay today, but the trend over the next few years is finer pitches. (Finer-pitch flat probes are in development). And even though there are only a few vendors for flat probes, the materials and manufacturing techniques are different for each, resulting in different performance for each. They need to be researched individually to find the best solution for high-volume wafer-level test applications.

Conclusion

Of all the traditional and newer device contacting solutions, flat probes provide the best combination of mechanical, electrical, and CoO performance. 



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INDUSTRY NEWS

SEMICON Europa Awards Recognize Industry Veterans

Each year SEMI Europe awards individuals for their efforts in the advancement of semiconductor technologies and their contributions to the industry organization. This year at SEMICON Europa, which took place Oct. 19-20 in Dresden Germany, the following individuals were honored.

European SEMI Award 2010

Established more than two decades ago, the European SEMI Award recognizes individuals and teams who made a significant contribution to the European semiconductor and related industries. Prof. Dr. Herbert Reichl was honored as recipient for the European SEMI Award 2010.



Reichl is being recognized for over 20 years of contributions to advanced semiconductor packaging technologies. He started researching silicon sensor technology in the early 1980s. Reichl recognized the importance of research and development in the area of "Electronic Packaging," founding the "Research Center Microperipheric Technologies" in 1986 in cooperation with the Technical University of Berlin. He also played a pivotal role in establishing the Fraunhofer Institute for Reliability and Microintegration in 1991.

"Prof. Reichl is a driving force in the field of semiconductor advanced packaging. He has made impressive contributions to advances in technology," said Heinz Kundert, president of SEMI Europe. "We are pleased to recognize him for his significant industry accomplishments."

SEMI Europe Lifetime Achievement Award

Peter Woditsch, CEO of Sunicon AG and former CEO of Deutsche Solar AG, was awarded the SEMI Europe Lifetime Achievement Award for his work in Photovoltaics. "Prof Woditsch is one of the real European pioneers in Photovoltaic. He exemplifies the qualities of a SEMI Lifetime Achievement Award recipient and it is an honor to grant him the SEMI Europe Lifetime Achievement Award for 2010," said Kundert.

Woditsch has 40 years of experience with Bayer AG and SolarWorld AG in a variety of key positions. He founded Bayer Solar Lim in 1994 in Freiberg, Saxony. Since 2007, he has been the CEO of Sunicon AG, an affiliate of SolarWorld, responsible for silicon feedstock supply and recycling in the photovoltaic business. He holds a doctorate degree in chemistry from the University of Erlangen and gave lectures as a professor at the University of Münster in industrial inorganic chemistry.

SEMI Europe Standards Awards

It has been said, "Standards are like your heart beat, when it's there, you don't notice it. When it's not there, you have a problem." At SEMICON Europa 2010, Oct. 19-20, SEMI honored two individuals with International Standards Awards.

Paul Williams of the University of Liverpool received a Standards Leadership



Award for his dedication in leading the SEMI Standards Precursors Task Force. Roland Bindemann of Freiberger Compound Materials received a Standards honor award for his dedication to the advancement of SEMI Standards. The SEMI International Standards Program was established in 1973 and benefits the worldwide semiconductor, photovoltaic and emerging markets industries by helping to increase productivity and reduce costs.

"Paul Williams and Roland Bindemann received these Standards awards for exceptional commitment to the advancement of SEMI International Standards," said Kundert. "SEMI is grateful for their commitment to the SEMI International Standards Program."

Formerly with SAFC, Williams has led the SEMI Standards Precursors Task Force since 2005. He consistently built consensus while setting guidelines and seeking input from interested parties. Under his leadership, four major documents were published and four draft documents are almost ready for balloting.

Since 1993, Bindemann has been involved with standardization efforts in Europe. In 2003, Bindemann was appointed as co-chair of the SEMI Europe Compound Materials Standards Committee. Now retired from Freiberger, Bindemann continues to be sponsored by the company to support SEMI European Standardization activities. 

Georgia Tech's PRC establishes UnITE PAC Web Portal

3D Systems Packaging Research Center (PRC)



UnITE PAC, which stands for University-Industry-Technology-Ecosystem PACkaging, is an industry-academia-government electronics packaging technology ecosystem established by the 3D Systems Packaging Research Center at Georgia Tech. UnITE PAC is designed to advance electronic packaging education, technologies, infrastructure, and commercialization via information dissemination and global networking.

Guided by a board of technical visionaries, UnITE PAC was founded on 2 simple strategies supported by 3 key elements in providing world-wide access to packaging information and resources. The first strategy is to use the internet to provide individuals, companies and organizations with a simple, individually-

relevant portal tool where participants can easily view public domain information specific to their posture and needs in the Electronics Packaging Ecosystem. Second is to establish a series of e-Media and traditional media communications mechanisms leveraging the Internet so participants can showcase new information, and learn about emerging technologies, global events, announcements, and resources. The key elements to the program include a web portal, webinars and conferences. For more information visit unite.globalgtprc.org/about-unite-pac.

Imec sets up R&D activity in Taiwan

Imec Taiwan has signed a co-funding contract with the Taiwanese Ministry of Economic Affairs (MOEA) for its R&D activity, Imec Taiwan Innovation Centre (ITIC). ITIC's goal is to expedite applied research projects with industry and academia that will result in electronic designs, components and technology

solutions. The new R&D center will focus on a variety of innovative applications in bioelectronics, MEMS and "green" electronics that are enabled through 3D system-package co-design and system-level evaluation.

Due to the worldwide impact of the Taiwanese semiconductor and consumer electronics industry, it is an important market for a nanoelectronics R&D center such as imec. As imec's local R&D center, ITIC will reportedly facilitate and intensify the collaboration between imec and the Taiwanese industry and academia. "The creation of ITIC, two years after having established a representation office in Hsinchu, Taiwan, is essential in our continued efforts to create value for our current and future partners in Taiwan, to leverage our global partnerships, and to actively interact with the Taiwanese ecosystem," said Luc Van den hove, CEO and President of imec and member of the Board of imec Taiwan. "An R&D

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initiative such as ITIC will intensify imec's interaction with the local semiconductor and system-level companies and academia."

"As a semiconductor innovative applications center, ITIC will support the upward shift in Taiwan's technology value chain and contribute to the realization of Taiwan's strategic Innovation Plan. It will accelerate open innovation that will result in locally owned IP in the area of intelligent electronics," says Jung-Chiou Hwang, Vice Minister of Economic Affairs. "The presence of ITIC - the local branch of the world-famous R&D center imec - will improve Taiwan's position against its peers in Asia, and result in attracting more European companies to invest in Taiwan."

John Snyder Appointed VP Business Development for AMTECH Solder Paste

In a move expected to grow and expand its AMTECH brand, SMT International,



LLC, manufacturer of AMTECH solder paste and process support products, appointed John Snyder as VP, business development. Leigh Gesick, President of SMT International, says Snyder is a vital addition to the organization.

"We are honored to have John Snyder join our organization, as he brings invaluable experience as a successful business executive and as a pioneer in the development of SMT solder paste technology," notes Gesick. "Mr. Snyder will assist us in the areas of product development, marketing/branding, technical support, and territory management."

"The AMTECH line already contains some very high quality products and is supported by strong technical service capabilities managed by very capable and experienced people, says Snyder. "I want to take it to another level by helping us focus on the medical and defense

markets, where domestic demand is still strong and product quality and performance are critically important. Specifically, I want to apply my expertise in new product development by utilizing statistically designed experiments to create a more dynamic product line able to respond quickly to customer needs."

An industry veteran with over 30 years of experience in polymer chemistry, coatings, powder materials and soldering technology, Snyder comes to SMT International after a nine year tenure at Heraeus, Inc., where he managed Research and Development then the operating group for the Americas, helping the company expand its market share, and opened a new world class production area. Prior to that, he was VP of Global Technology at Alpha Metals, where he had been since 1989. He's a graduate of The University of Illinois majoring in Chemistry and Mathematics, and has a long history in new product development at various organizations including De Soto Inc, Glidden Coatings, and SCM Inc.

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COMPANY HEADQUARTERS	WAFER SCRIBING SYSTEMS	SAW DICING SYSTEMS	LASER DICING SYSTEMS
Company Street Address City, State, Country Telephone Website	Method L - Laser, M - Mechanical P - Plasma, S - Saw Automation LU - Loading & Unloading WA - Wafer Alignment CD - Cleaning & Drying Specifications (Max.) WD - Wafer Diameter FR - Feed Rate / Speed	Method L - Laser, M - Mechanical P - Plasma, S - Saw Automation LU - Loading & Unloading WA - Wafer Alignment CD - Cleaning & Drying Specifications (Max.) WD - Wafer Diameter FR - Feed Rate / Speed	Method L - Laser, M - Mechanical P - Plasma, S - Saw Automation LU - Loading & Unloading WA - Wafer Alignment CD - Cleaning & Drying Specifications (Max.) WD - Wafer Diameter FR - Feed Rate / Speed
Note: CM = Contact Manufacturer	Models (Qty)	Models (Qty)	Models (Qty)
Veeco Instruments Inc. Terminal Drive Plainview, NY 11803 Tel: +1-516-677-0200 www.veeco.com	Method: Laser Automation: LU, WA WD: 200 mm FR: 600 mm/s Models (2)	Method: Saw Automation: LU, WA WD: 200 mm FR: 600 mm/s Models (2)	Method: Laser Automation: LU, WA WD: 200 mm FR: 600 mm/s Models (1)

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The listing data for Veeco Instruments Inc was inadvertently omitted from the Sept/Oct International Directory of Wafer Scribing & Dicing Systems Directory.



- > RF and high power applications
- > Leaded and leadless devices: SO/QFN/QFP
- > Pb-free packages
- > Small pad sizes and lead pitches down to 0.25 mm

Multitest ECON® -

cost efficient solution for high power plunge-to-board applications

The ECON® socket combines the most efficient cost of test ratio with high power and high frequency capabilities for small size and small pitch devices (QFN).

Best cost of test: The ECON® socket accomplishes this favourable cost of test by a maintenance friendly contact spring block design, special Dura® and Forta® coatings for long life times, a dedicated contact spring geometry and a new kind of plastic material avoiding thermal expansion.

High power performance: The ECON® supports a maximum peak current of 25 A/ms and a maximum continuous current of 2.5 A. A high contact force of 0.45 N per spring ensures repeatable electrical behaviour.

Compatible interfaces: The ECON® socket is load board compatible to existing RFC sockets and third party socket types. It supports plunge-to-board as well as standard applications in the full temperature range from -60°C to +160°C.

The ECON® is available for SO, QFP, and QFN packages with a lead pitch down to 0.25 mm.
www.multitest.com/ECON



ECT Mercury™

- > BGA, LGA, QFN, WSCSP, QFP...
- > Pitches down to 0.4 mm
- > Excellent RF performance
- > Singulated, strip or wafer-level test

ECT Mercury™ Test Socket -

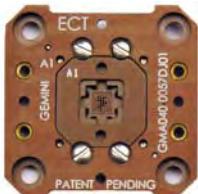
for optimized yield and test cell uptime

The ECT-Mercury™ family of test sockets is the next generation solution for optimized yield and test cell uptime. The ECT Mercury™ offers the answer to today's needs and future challenges. The twofold trend for finer pitches and higher RF capabilities brings standard probes to their limitations regarding length, contact force and bandwidth. The innovative architecture of the Mercury™ overcomes the physical constraints of these standard probe technologies. The ECT Mercury™ test socket ensures:

Best contacting yield based on stable and high contact force, repeatable resistance, accurate positioning and outstanding capability to compensate package tolerances and board flex.

Highest test cell uptime achieved by optimized maintenance and cleaning cycles as well as easy set-up, alignment and cleaning procedures.

Full support of your IC test roadmap: with solutions for singulated, strip and wafer-scale test the Mercury™ covers a comprehensive package range of array and in-line packages including Pb-free applications and small pitch sizes. Its excellent electrical behavior makes the ECT Mercury™ the first choice for advanced RF and high current test.
www.multitest.com/mercury



ECT Gemini™

- > 500K cycles typical lifetime
- > 40GHz 1dB 0.5mm pitch GSG
- > > 0.4mm pitch QFN
 > 0.5mm pitch BGA
- > 1.5mm test height

ECT Gemini™ -

robust and cost effective solution for high frequency test applications

High Frequency: ECT Gemini™ contactors offer the electrical performance required by today's most demanding applications. The combination of short test height and impedance match allow this technology to reach frequency ranges higher than any other pogo pin solution. The unique dual fork design results in an extremely robust mechanical solution typically impossible with other high frequency fine pitch solutions.

Low inductance: Consistent power is a must for integrated devices. Placing both fast switching circuits and power delivery circuits in the same device can wreak havoc on the stability of the device. Inductance in the power delivery network exaggerates this instability. The short test height of Gemini™ contactors minimizes the additional inductance added by the contactor and solves the power delivery issues found with other solutions.

Cost Competitive: The success of the Gemini™ manufacturing process has created an economy of scale. Combining the long lifetime and the low price point of Gemini™ makes it an easy choice.
www.multitest.com/gemini

WHAT'S NEW!

BGA Sockets

The Ultra Slim socket series from E-tec Interconnect offer high speed socketing solutions for BGA, QFN, and LGA packages. The sockets are capable of performing high insertion/extraction



cycles, and feature a very small socket outline, requiring little real PCB real estate. Easy open and close locking methods are part of the series' low-profile locking system. An open top allows for improved heat dissipation. Available with elastomer interposer or probe pins, the sockets can be adapted to any chip style or pin count, and come in either screw lock or fast lock configurations. [\[e-tec.com\]](http://e-tec.com)

Ellsworth Expands Dispensing Product Line

Ellsworth Adhesives, distributor of adhesive and sealing dispensing solutions, has expanded its dispensing equipment and supplies product line with the addition of several hundred new products from Fisnar, Sulzer MixPac, Semco, Techcon , in addition to its lines from Sealant Equipment, 3M, Loctite, Cox, Bostik, Sulzer MixPac, Semco and many others. As a result, Ellsworth Adhesives reportedly offers nearly 1000 dispensing products for sale online

through its US site and a growing number of products on its Canada and UK sites.

"Ellsworth is excited to expand its dispensing product line. The product expansion allows us to better serve new and existing customers in a variety of industrial and electronics markets," stated Mike McCourt, Global President of Ellsworth Adhesives - Specialty Chemical Distribution. [\[www.ellsworth.com\]](http://www.ellsworth.com)

SMT Perimeter Connectors

Advanced Interconnections introduced a line of customized surface mount connectors that reduce board space by utilizing the perimeter of circular and other



odd-shaped PC boards. SMT Perimeter Connectors are created from easily customized FR-4 insulators on in-house driller/routing machines and incorporate high quality screw-machined, solder ball terminals (available down to 0.50mm pitch) on both the male header and the mating female connector (socket). Vertical integration including precision CNC machining and hundreds of existing screw-machined terminal designs reportedly eliminate the need for expensive tooling and set-up costs such as stamping dies.

The semi-circle design maximizes space when stacking circular printed circuit boards and features an integrated keying/

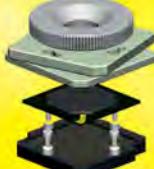
polarization feature. The light-weight, low profile FR-4 insulator can be transitioned to a molded design. Typical applications include military and medical equipment where mission-critical reliability and the ability to provide custom designs in low volumes are required. [\[www.advanced.com\]](http://www.advanced.com)

A*STAR IME Launches Copper Wire Bonding Consortium

The Institute of Microelectronics (IME), a research institute of the Agency for Science, Technology and Research (A*STAR), has launched the Copper Wire (Cu-Wire) Bonding Consortium to tackle existing Cu-Wire bonding issues of quality and reliability, and improve existing measurement systems. This joint effort will be spearheaded by IME in collaboration with multinational companies including ASM Technology Singapore, Freescale Semiconductor, GLOBALFOUNDRIES, Infineon Technologies Asia Pacific, UNISEM and Atotech S.E.A.

Through this initiative, IME will fill the gap in current techniques by developing micro-sensor based methodology to measure the wire bonding stress and perform reliability characterization of wire bonds. These novel sensors will allow the measuring of the stress beneath the wire bonding pad, catalyzing the investigation of potential wire bond damage, and identifying a reliable bonding process for copper wire, including bond pad structures and metallization. Further, the consortium will also cover corrosion study and bond

FastLock Sockets



- Simple open/close = no screws – no tools!
- Adjustable pressdown forces
- Open top for heat dissipation and access to top of the chip
- Low profile retainer solution
- 10'000 cycles min.
- Available with probe pin and elastomer interposer sockets in SMT, thru-hole and solderless versions

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degradation study related to copper wire bonding in harsh environments.

Electronics Cooler from Nextreme

The eTEC™ HV56 module from Nextreme Thermal Solutions, is the next product in the company's high-voltage (HV) line of thin-film thermoelectric coolers (TECs) designed to address electronics cooling applications with larger heat pumping requirements. At 0.6mm high, Nextreme claims it to be the thinnest, highest heat pumping TEC on the market.

"Many of our customers have been asking for a higher wattage device in a single package," said Dave Koester, vice president of engineering at Nextreme. "The eTEC HV56 has four times the heat pumping capacity of our HV14 module and operates at higher voltages, making it easier to drive. The introduction of the HV56 also demonstrates our ability to scale up our technology in a variety of configurations based on customer requirements."

At 85°C the eTEC HV56 can reportedly pump 6 watts or 58 W/cm² of heat in footprint of only 11 mm². This creates a temperature differential of up to 60°C between its hot and cold sides, and operates at a maximum voltage of 10.8V, making it compatible with commonly found board-level currents and voltages. The eTEC HV56 is RoHS-compliant and is manufactured using gold-tin (AuSn) solder, which enables assembly temperatures as high as 320°C , making it compatible with industry standard processes for packaging electronic devices that require tight tolerances. [www.nextreme.com]

AOI and X-ray Inspection

Viscom's X7056 inspection system combines automatic optical inspection (AOI) with in-line X-ray inspection in one single system to detect concealed defects while also simultaneously performing selective verification (AXI-onDemand). It's particularly suited to inspection tasks that require an AOI with high throughput. Additionally, it is said to reduce false alarms while enhancing defect detection capabilities.

Both AOI and X-ray inspection procedures can be quickly and easily performed using the same user interface without needing to transport assemblies into a second inspection system. The



system allows for flexibility in meeting inspection requirements. The system's X-ray unit can be used to selectively verify individual defects during inspection tasks that primarily require an AOI with high throughput, ensuring compliance of tight AOI tolerances.

AXI reportedly provides manufacturers with an effective quality control because of additional images provided by the AXI help to reliably assess quality. It can also be used for QFN components, where high resolution images improve the user's ability to reliably evaluate the components. [www.viscom.com]

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Korea

 **Keon Chang** Young Media [\[ymedia@ymedia.co.kr\]](mailto:[ymedia@ymedia.co.kr])
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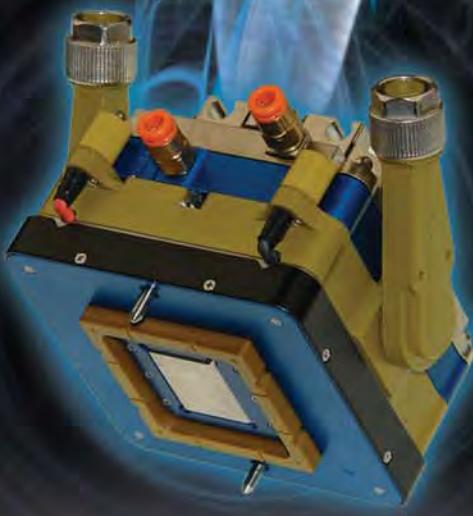


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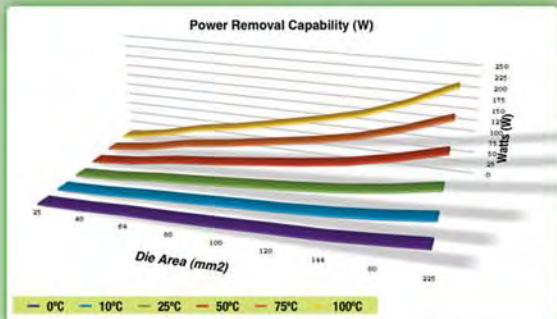
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