

ChipScale

REVIEW

ChipScaleReview.com

The International Magazine for the Semiconductor Packaging Industry

Volume 18, Number 1

January • February 2014

Probing 25µm-diameter micro-bumps for Wide-I/O 3D SICs

Page 20

- 3D ICs
- The future of interposers
- MEMS sensors for mobile devices
- Next-generation TSV filling by electroplating
- Enhanced WLCSP probe card performance at sub-300µm pitch





invent

innovate

implement

www.EVGroup.com

MID-END LITHOGRAPHY SOLUTIONS ARE READY!

Advanced Resist Processing

Thick Resist and Dielectric Layer Coating
Conformal TSV Coating and Polymer Via-Filling

Vertical Thick-Resist Patterning

Large Depth-of-Focus Imaging for 3D Applications
High Exposure Dose Processing

Ultra-Thin, Warped and Carrier-Mounted Wafer Handling



GET IN TOUCH to discuss your manufacturing needs

www.EVGroup.com



CONTENTS

January • February 2014
Volume 18, Number 1



Experimental test set-up for pre-bond probing of 25µm-diameter 40/50µm-pitch micro-bumps for Wide-I/O three-dimensional stacked ICs. Shown is a MEMS-type vertical probe core on a probe card in an advanced engineering probe station. Underneath the probe card adapter is a 300mm test wafer.

Photo: Bart De Wachter/Fred Loosen – imec, Leuven, Belgium

Chip Scale
REVIEW
ChipScaleReview.com

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

FEATURE ARTICLES

Probing 25µm-diameter micro-bumps for Wide-I/O 3D SiCs

Ken Smith, Cascade Microtech; Erik Jan Marinissen, imec

20

Conformal barrier/seeds for next-generation TSV filling by electroplating

Stephen N. Golovato, Tyler Barbera, Keiichi Fujita, Tokyo Electron NEXX; Takashi Tanaka, Tokyo Electron Kyushu Ltd.

24

Diamond: ultimate temperature control material for 3D ICs

Mario M. Pelella, Jerry W. Zimmer, sp3 Diamond Technologies; Thomas S. Tarter, Package Science Services, LLC

28

The future of interposers for semiconductor IC packaging

John H. Lau, ITRI

32

Copper Pillar µBumps

VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

www.amkor.com

PRESENTING THE EVOLUTION OF THE FLIP CHIP BUMP

From the diverse solder bumping solutions of the last decade to the large scale production of today's fine pitch copper pillar bumps, Amkor will provide a solution for your packaging challenges.

Amkor remains at the forefront of semiconductor packaging development and performance.

ELIMINATE THE GUESSWORK

and talk to us today about our extensive offering of next generation design, assembly, and test solutions.

Amkor
Technology®

LEENO has 100% in-house manufacturing to provide our customers with the best Quality & Delivery”



**Logic Test
Socket**



RF Coaxial Spring Probe & Impedance Controlled Socket



**PoP Test
Socket**



Probe Head



**Wafer Level CSP
Probe Card**



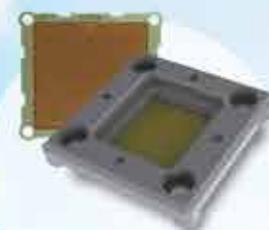
**Memory
Socket**



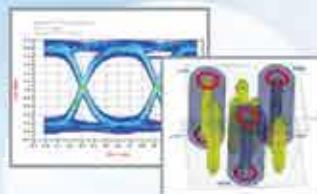
**Spring Contact
Probe**



SLT Socket



**Elastomer
Socket**



Electrical Analysis
CCC Test, HFSS, TDR
Eye Diagram
4Port VNA Test



The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

STAFF

Kim Newman Publisher
knewman@chipscalereview.com
Lawrence Michaels Managing Director
lxm@chipscalereview.com
Debra Vogler Senior Technical Editor
dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Dr. Thomas Di Stefano Contributing Editor
tom@centipedesystems.com
Jason Mirabito Contributing Legal Editor
mirabito@mintz.com
Paul M. Sakamoto Contributing Editor Test
paul.sakamoto@comcast.net
Dr. Ephraim Suhir Contributing Editor Reliability
suhire@aol.com
Sandra Winkler Contributing Editor
slwinkler@newventureresearch.com

EDITORIAL ADVISORS

Dr. Andy Mackie (Chair) Indium Corporation
Rolf Aschenbrenner Fraunhofer Institute
Dr. Thomas Di Stefano Centipede Systems
Joseph Fjelstad Verdant Electronics
Dr. Arun Gowda GE Global Research
Dr. John Lau Industrial Tech Research Institute (ITRI)
Dr. Venky Sundaram Georgia Institute of Technology-
3D Systems Packaging Research Center
Fred Taber BITS Workshop
Dr. Leon Lin Tingyu National Center for Advanced
Packaging (NCAP China)
Francoise von Trapp 3D InCites

SUBSCRIPTION--INQUIRIES

Chip Scale Review
Effective immediately
All subscription changes, additions, deletions to any and
all subscriptions should be made by email only to
subs@chipscalereview.com
Do not leave subscription inquiries on the company
voicemail system.

Advertising Production Inquiries:

Kim Newman
knewman@chipscalereview.com

Copyright © 2014 Haley Publishing Inc.
Chip Scale Review (ISSN 1526-1344) is a registered trademark of
Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified
individuals in the electronics industry. Subscriptions outside of the
U.S. (6 issues) by airmail are \$100 per year to Canada or \$125 per
year to other countries. In the U.S. subscriptions by first class mail
are \$95 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a
year with issues in January–February, March–April, May–June, July–
August, September–October and November–December. Periodical
postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review
magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER

In not one, but two columns on market trends, top analysts Bill McClean of IC Insights, and Dan Tracy/SEMI and Jan Vardaman/TechSearch International, enlighten us on the major drivers of the semiconductor industry as a whole, and those related to materials used for packaging and assembly. Authors from diverse companies such as Tokyo Electron NEXX, ITRI, and sp3 Diamond Technologies, provide detailed perspectives on 2.5D/3D technologies. And in this first issue of 2014, we start a new series about R&D institutes; imec in Leuven, Belgium, is the first to be profiled.

Kim Newman,
Publisher

FEATURE ARTICLES

Packaging of integrated MEMS sensors for mobile devices Yan Loke, Jay Esfandyari, Antonio Cirone, <i>STMicroelectronics</i>	37
Enhanced WLCSP probe card performance at sub-300µm pitch Jon Diller, <i>Smiths Connectors - IDI</i>	42
A 20GHz pluggable 0.5mm pitch BGA connector simplifies test/verification by Ila Pal, <i>Ironwood Electronics, Inc. USA</i>	48

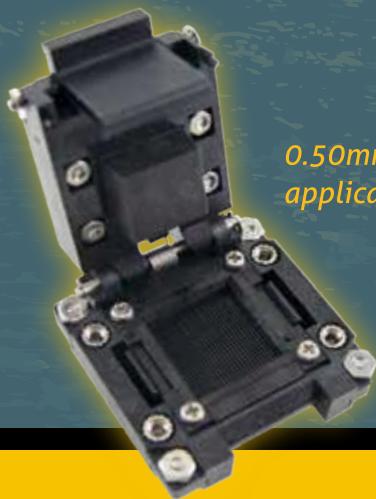
DEPARTMENTS

Market Trends Semiconductor market and packaging trends Bill McClean, <i>IC Insights</i>	5
Guest Editorial Packaging tomorrow's devices: an equipment vendor's perspective Kevin Crofton, <i>SPTS Technologies</i>	8
Market Trends Mobile products: driving developments in materials for packaging and assembly Dan Tracy, <i>SEMI</i> ; Jan Vardaman, <i>TechSearch International, Inc.</i>	12
Guest Editorial Putting 2.5D in perspective – an overview of a budding technology Joseph Fjelstad, <i>Verdant Electronics</i>	14
Profile: imec performs world-leading research in nanoelectronics <i>Chip Scale Review Staff</i> interviews Eric Beyne, Program Director 3D System Integration, <i>imec</i>	18
Guest Editorial Bringing new electronic materials to market Alan Rae, <i>NanoMaterials Innovation Center LLC</i>	46
Industry News <i>Chip Scale Review Staff</i>	53
Advertiser Index, Advertising Sales	56

*Oh
Snap*

We've done it again

INTRODUCING THE M-SERIES SOCKET-
*the first product from our
innovative new SnapFit Process.*



0.50mm BGA burn-in
applications



Now H-Pin Burn-in Test Performance is Faster and Easier.

Once again, we've created a testing solution to make your life easier. SnapFit products deliver superior reliability and performance while significantly reducing product cost and production time.

Let us make your burn-in test a snap. Call 972-258-2580 for a quote.

www.plastronics.com
email us: sales@plastronics.com



Semiconductor market and packaging trends

By Bill McClean [IC Insights]

The “worldwide economy driven” IC industry cycle model is expected to greatly influence the IC market over the next five years. As a result, the annual global IC and semiconductor market growth rates are expected to closely mirror the performance of the worldwide economy (i.e., GDP) throughout the forecast period. In the worldwide economy driven IC industry cycle model, global financial considerations such as oil prices, interest rates, and fiscal stimulus are expected to be the primary drivers.

It should be noted that 2.5% or less worldwide GDP growth is typically considered a global recession. Moreover, worldwide GDP growth in 2013 was only 2.8%. Although this figure is higher than the 2.7% growth rate of 2012, it was still 0.6 points below the long-term average annual global GDP growth rate.

In 2014, worldwide GDP is expected to grow 3.3%, just under the long term average of 3.4%. One of the key aspects of the 2014 forecast is that the Eurozone returns to positive growth. It is IC Insights’ opinion that worldwide GDP increases will not return to at least average long-term growth rates without the Eurozone exhibiting some form of recovery (i.e., positive GDP growth) from its 2012-2013 downturn.

China’s GDP growth rate dropped to 7.6% in 2013 with about the same growth forecast for 2014 at 7.8%. While many developed countries would welcome 7% or higher GDP growth rates, for China, this figure is significantly below the 10% and greater annual GDP increases logged from 2002-2009.

Although the vast majority of economists expect China’s economic

growth to be about 7.5-8.0% in 2014, there are increasing rumblings about the possibility of a “hard landing” for the Chinese economy due to the possible bursting of its over-inflated property market (i.e., housing bubble) and a slowdown in growth for exports. It should be noted that a hard landing for China’s economy in 2014 would be defined as GDP growth of anything less than 7.0%.

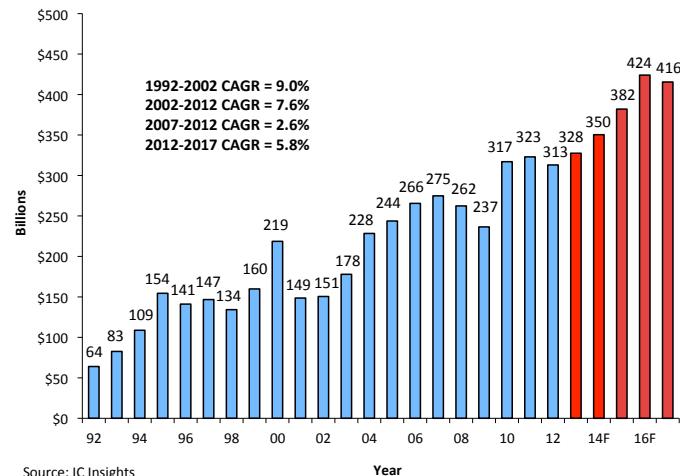
In the past, when confronted with a slowing of GDP growth, China’s government would step in with various investment stimulus programs. However, China’s new leadership is attempting to shift the country’s GDP growth from being highly dependent on investment in infrastructure (i.e., housing and other construction projects) and exports, to one that relies more on consumer consumption. Thus, unless quarterly GDP growth drops below the Chinese government’s official 7.5% target, most economists do not expect significant new stimulus to be forthcoming from China’s new leadership.

Although China represented only 8.8% of worldwide GDP in 2013, driven by its “number one” consumption ranking in so many important electronic system categories like PCs, TVs,

automobiles, and cell phones, the “final consumption” value of ICs (i.e., IC value in electronic systems that are purchased and stay in the country and not exported) in China was about \$50 billion in 2013. This figure represented about 19% of the 2013 worldwide IC market of \$268.9 billion — more than double the country’s percentage share of worldwide GDP. Thus, not only is China increasingly important in driving worldwide GDP growth, it is also increasingly important in driving the “final consumption” value and market growth for ICs.

Overall, there is an extremely high level of uncertainty with regard to the worldwide economy heading into 2014. This high level of uncertainty is expected to continue to cause hesitation with regards to spending by consumers and businesses worldwide. This conservative spending environment ultimately negatively impacts economic

Worldwide Semiconductor Market History and Forecast (1992-2017F)



Source: IC Insights

Year

Figure 1: Worldwide semiconductor market history and forecast (1992-2017F). SOURCE: IC Insights

growth, which is evident in the lackluster forecast for worldwide GDP growth for 2014.

Semiconductor market history and forecast

The worldwide history and forecast of the semiconductor industry for the 1992-2017 time period is depicted in **Figure 1**. As shown, the worldwide semiconductor industry is forecast to reach over \$400 billion in 2016 (\$424 billion), after first breaching the \$300-billion level six years earlier in 2010. The \$78 billion increase in the 2010 semiconductor market still holds the record as the largest annual increase in the history of the semiconductor industry. Moreover, the worldwide semiconductor industry is forecast to reach \$416 billion in 2017, just over 50% greater than the semiconductor market ten years earlier in 2007.

From 1992-2012, the semiconductor industry posted a healthy CAGR of 8.3% — more than double the CAGR for worldwide GDP over this same time frame. However, the semiconductor industry CAGR declined from 9.0% in the 1992-2002 time period to 7.6% from 2002-2012, and only 2.6% from 2007-2012. With relatively stable IC ASPs expected over the next five years, the semiconductor industry CAGR is expected to rebound to 5.8% over the 2012-2017 time period, more than double the 2.6% in the 2007-2012 time frame.

IC packaging trends

SO-type packages were the most widely used in 2012. However, primarily as a result of booming demand for quad flat no-leads (QFN) packages, the FP/CC category exceeded the SO category in 2013 for the first time ever.

The QFN package category in the JEDEC standards includes a variety of manufacturer-specific designs such as the MicroLeadFrame (MLF) package from Amkor, Fujitsu's bumped chip carrier (BCC) and small outline no-lead (SON) packages, Carsem's Micro Leadframe package (MLP), and ASE's microchip

carrier (MCC). There are similar JEDEC standards for dual flat no-leads (DFN) packages that have external bond pads or "lands" on two sides instead of four like the QFN. QFNs and DFNs are part of a larger group of packages called lead frame chip-scale packages (CSPs).

QFN and DFN packages are inexpensive to manufacture—they typically don't have solder balls, are targeted at low-I/O applications (typically <85), and make use of pre-plated lead frames. Either wire bonds or flip-chip bumps are used to attach the IC to the lead frame. Versions like the MLF and BCC have an exposed die attach paddle on the bottom of the package, which serves as an excellent thermal path away from the chip as well as a good ground plane if the pad is grounded on the circuit board. That, in conjunction with the high electrical performance offered by short I/O connections, has made these lead frame CSPs attractive for use in packaging RF circuits for cell phones and other wireless and portable product applications. Many companies have migrated from SOIC packages to QFNs and DFNs. There are also a growing variety of QFNs/DFNs, such as versions with dual rows of lands for as many as 180 I/Os, ones with multiple chips stacked inside, or types that have an air cavity designed into the package for high-frequency microwave applications.

2.5D packaging

In October 2010, Xilinx brought into the spotlight the idea behind using a silicon interposer with TSVs to achieve some of the improvements in circuit density and multi-functionality promised by true 3D IC technology, but without many of the technical challenges and infrastructure issues that have delayed high-volume manufacturing of TSV technology for 3D ICs. This method of using a passive silicon interposer with TSVs was given the obscure name "2.5D" mostly because it was initially seen as a stepping stone to reach true 3D IC technology, which is much different than

the 3D-stacking of chips and/or packages that is already a mainstream technology.

While the first version of Xilinx's "stacked-silicon interconnect" technology didn't stack any ICs in the vertical direction, the 4-layer-metal silicon interposer with TSVs used for the company's Vertex-7 2000T allowed for the combination of four 28nm-fabricated FPGAs mounted side-by-side on the substrate with >10,000 inter-die connections, resulting in a total of two million logic cells in the "package." From a system's point of view, the 2000T appears to be a single super-high-density FPGA chip. Xilinx followed up the homogeneous 2000T with the heterogeneous Vertex-7 HT, which features three FPGA chips with 13G transceivers mounted along with two 28G SerDes transceivers all side-by-side on the passive silicon interposer, giving the HT performance of up to 2.8Tb/s total serial data bandwidth.

Other companies such as Altera, Cisco, Huawei, and IBM have revealed similar 2.5D chip products or concepts, mostly for high-performance networking-related applications. While 2.5D technology was initially viewed as a short-term bridge to full 3D ICs, it is now believed that 2.5D and 3D will coexist. 2.5D is well suited for products like Xilinx's Virtex-7 devices that are commonly used in networking applications, but in systems requiring a large amount of memory operating at the highest level of bandwidth possible, 3D IC technology is needed. There will also be solutions combining 2.5D and 3D technologies where a logic chip might be mounted next to a stack of TSV-interconnected memory chips, and possibly even with supporting analog and passive components, on a silicon interposer having TSVs to connect all the chips together.

Biography

Bill McClean received his BS in business administration and an Associate Degree in aviation from the U. of Illinois; he is President of IC Insights, Inc.; email info@icinsights.com



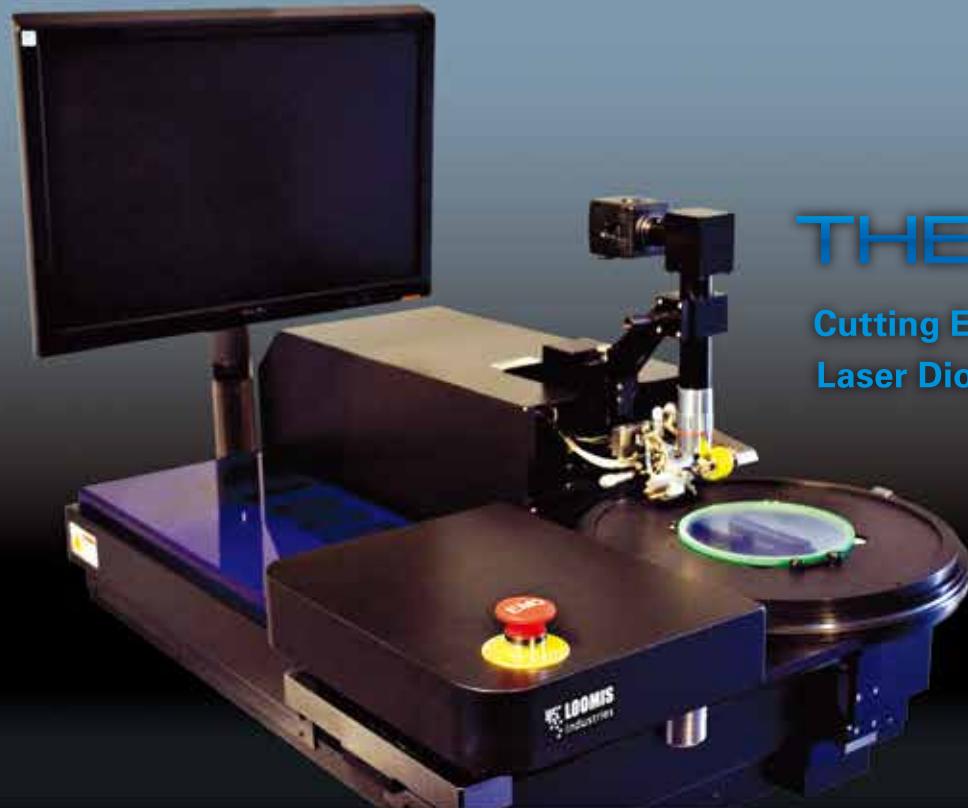
Patented Scribe and Break Dicing Technology

Loomis Industries, Inc.

1204 Church Street
St. Helena, CA 94574

T. 707-963-4111
F. 707-963-3753

info@loomisinc.com
www.loomisinc.com



THE LSD-155

Cutting Edge automated III-V
Laser Diode and Wafer Processing

KEY ADVANTAGES:

- Increased Operator Productivity
- Integrated Scribe and Break Capabilities
- Bar Array Dicing (Grids of Laser Bars)
- Multiple Cleaving Options
- Multiple Wafer Holding Media Options
- High Resolution Optics
- Pattern Recognition with Micron Level Accuracy
- Cleaved Edge, Vision, When standard pattern alignment is not good enough.

EASE OF OPERATION:

- Easy to Navigate User Interface
- Password Protected Levels of Access
- Hands-Off Media Rotation
- Software/Recipe Controlled Process Parameters, Pressures, and Speeds

LOOMIS LSD-155

Speed, product quality and yield speak for themselves.
Contact Loomis Industries for information or a demonstration.

GUEST EDITORIAL



Packaging tomorrow's devices: an equipment vendor's perspective

Kevin Crofton [SPTS Technologies]

The demand for faster, thinner, smaller devices has fundamentally changed the shape of our industry. Chip makers have realized that the opportunities to improve performance by following Moore's Law are becoming fewer, and attention has shifted to the packaging arena as one of the means of delivering on roadmap commitments.

Starting with flip chip, and now 2.5D, and soon 3D designs, this sea change means that front-end equipment is now a staple part of packaging. In the past, there was a clear dividing line between front-end and back-end; front-end foundries and IDMs made the device, and then dies were separated and packaged in the back-end. There is now a new mid-end space where wafer-level packaging occurs; be it backside processing to expose through-silicon vias (TSVs), or where vias can be formed in finished devices, so-called via last TSVs. Ownership of the mid-end space is still in debate; the device maker and packaging specialists both see it as an area where they share in the value of the final device. This new advanced packaging landscape also impacts equipment makers. As we ring in 2014, I'm sharing an equipment provider's perspective in this packaging race, drawing from our extensive work across a broad customer spectrum (i.e., OSATs, foundries, and IDMs).

Advanced packaging takes center stage

For an equipment vendor, the term "advanced packaging" means that front-end plasma etch and deposition equipment are used after the device is completed. Flip chip was the first example of this, where high I/O count

devices were connected via intra-die bumps to relieve the congestion of traditional wire bonding at the die edge. Scaling and performance demands have now moved us into the era of stacking; first, with die positioned on an interposer (2.5D) and soon, die on top of die (3D IC). The benefit of such designs is neatly summarized by work done by Samsung [1] (Figure 1).

While the jury is still out on exactly when 3D IC will move into high-volume manufacturing (HVM), there is no doubt that it will be the packaging method of choice for high-performance devices by the turn of the decade. According to market analyst firm Yole Développement, the market value of all the devices using TSV packaged in 3D in the 3D IC or 3D wafer-level packaging (i.e., wafer-level chip-scale packaging, WLCSP) platforms will hit almost \$40 billion by 2017, representing 9% of the total semiconductor value. There are various views on the true value of the 3D IC market size, but there is no doubt it will gain importance in the coming years — it is not a question of 'if,' but rather 'when,' it will become the primary interconnect scheme in the industry.

Today, flip chip is fast replacing wire bonding in sub-2Xnm devices; 2.5D interposers are already in volume manufacturing, and true 3D technologies continue to mature and move towards volume production readiness. According to Yole, 2.5D interposer underneath

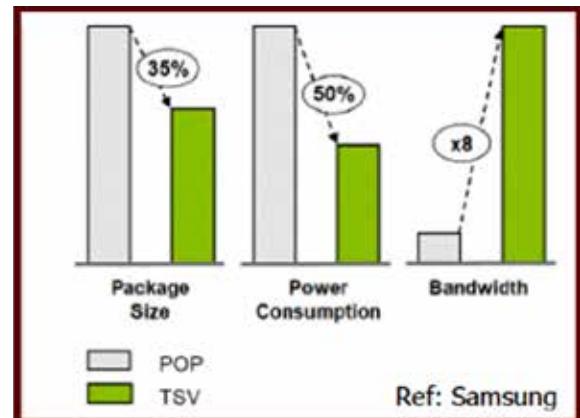


Figure 1: TSV packaged devices deliver smaller packages, reduced power consumption and greater bandwidth [1].

a graphics processing unit (GPU) is especially significant for enabling high clarity 3D imagery in gaming consoles as evident in the latest Sony Playstation 4 released in November 2013. Yole also projects the market for interposers to hit \$1.5 billion through 2017 — about 15% of the overall packaging substrate market value [2].

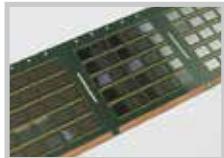
For the advanced packaging community (device makers and equipment makers alike) the inflection point is the ultimate convergence of heterogeneous stacking, which is the promise of 3D interconnection (Figure 2).

Early in the TSV development phase, it became clear that it was an integration challenge where each process step influenced the next. Since that time, SPTS and other equipment vendors like us began offering etch, CVD, PVD (and in some cases, thermal processing) solutions that would work together (i.e., etching high-aspect ratio vias that could be covered with insulators, and

FLIP CHIP BONDER

All New “10” Advanced Features!

- High Productivity
- Precision Bonding Capability
- Flux Vision Inspection Function
- Auto Flatness Check Capability
- Wafer Map Shift Prevent Function
- Foreign Material Detect Inspection System
- Chip Out Detect Inspection System
- Lower Vibration Control System
- User Friendly MMI for Easy Operation
- Lower Temperature Control



FLIP CHIP BONDER-A110



■ General Specifications

SECTION		FLIP CHIP BONDER-A110
PRODUCTIVITY	UPH	15,000 (Based on Dry Run)
ACCURACY	X-Y PLACEMENT	$\pm 6\mu\text{m}$ @ 3 σ
	CHIP ROTATION (θ)	$\pm 0.1\mu\text{m}$ °@ 3 σ
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)
FOOTPRINT	DIMENSION (L x W x H)	1,600(L) x 2,200(W) x 2,000(H)
	WEIGHT	2,600kg



Semiconductor

#532-2, Gajwa-Dong, Seo-Gu, Incheon, 404-250, Korea
TEL. +82-32-571-9100 www.hanmisemi.com

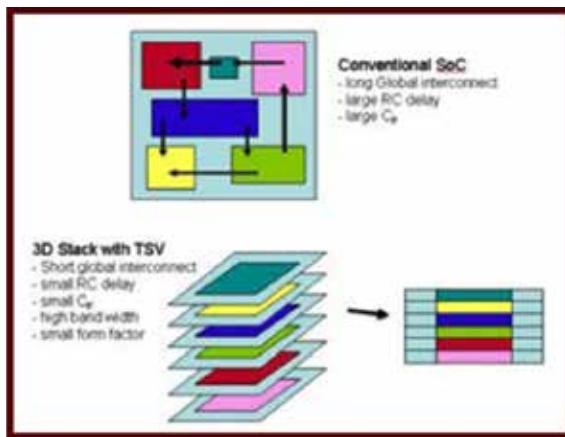


Figure 2: The benefits of 3D-IC die stacking are not in doubt.

then lined with ionized PVD metals offering sufficient sidewall coverage without closing off the via opening). More recently, via reveal technology has become a focus where the backside of the wafer is ground and then etched back to reveal the tips of the metal filled TSVs, ready for connection. It's a different type of silicon etch, but in its own way as challenging as forming a deep via; 100% open area etching at high rate requires a highly uniform plasma with high dissociation characteristics. In addition, high-volume manufacturing (HVM) TSV reveal is best served by in situ endpointing, and an etch process that can accommodate incoming nonuniformities created by mechanical grinding. The second part of the reveal step is to deposit passivation oxides and nitrides by CVD at <200°C: a temperature limit imposed by the temporary bonding layer between the device wafer and the carrier. Depositing low current leakage, stable stress dielectric films at such low temperatures is a science in its own right.

Another packaging application gaining momentum is to use plasma dicing techniques to improve die yield and the number of die per wafer. This is especially critical for chip card, power device, MEMS,

and LED manufacturers. As device trends move to thinner silicon, smaller die or applications grow to include invasive biomedical MEMS devices, conventional approaches (such as mechanical saw, stealth or laser dicing) are beginning to show limitations in capability and cost effectiveness. By applying a well-established semiconductor etch process to this final fabrication step, the advantages gained in

die density per wafer, pattern layout, throughput, yields, and costs are increasingly compelling.

Covering the bases

The early days of TSV development were challenging when the industry (IDMs and equipment suppliers alike) explored ways of solving an integration challenge — we were trying to get to the same endpoint through various technical avenues. Various schemes were under consideration, often resulting in complicated roadmaps with multiple outcomes depending on which scheme triumphed. This situation was clearly untenable in the cost focused world of advanced packaging. Then, market dynamics took over and as the industry nears HVM for 2.5D and 3D, we see consensus appearing. For instance, in the middle of the last decade, the industry debate formed

around the use of a via-first, via-middle or a via-last process approach. Today, it is clear that 3D die stacking will use either via-middle or via-last.

- Via-middle: vias are formed during the making of the actual device; must be formed by the foundry or IDM;
- Via-last: the vias are added after the device is finished by etching Si from the backside of a thinned wafer to contact metal pads on the front (device) side. This can be done by the device maker or by the OSAT.

The probable ratio of via-middle versus via-last is 60/40 or even 70/30 — the choice of process type will be determined by the strategy of the OSATs, integrated device manufacturers (IDMs) and foundries who have to decide on the stage of the TSV insertion.

With the technology ground rules (for the most part) worked out, the new industry challenge is determining where the work will be done. **Figure 3** highlights the creation of the mid-end — the area that exists between formation of the device and dicing. OSATs and some foundries/IDMs see this as an area where they can add value. This is particularly attractive to the OSATs for reasons of both margin, and technical advancements as OSATs now want to move up the technology food chain into a more lucrative market segment.

Partnership

At the recent SEMICON Europe Fab Managers' Forum keynote, I presented on the importance of a strong collaboration between device manufacturers and their equipment vendors. As device manufacturing becomes more demanding, relationships in the supply chain must evolve into a true partnership, where each party understands the challenges faced by the other. Through leveraging an integrated process approach using etch



Figure 3: Emergence of the new competitive landscape between traditional FEOL and BEOL.

Dispensing Control

Enhanced Dispense Process Control



Fluid Pressure Control (FPC) maximizes the dispense capabilities of your pump. Through engineering and software, a constant supply of fluid is delivered to the pump displacement mechanism – not too much and not too little, regardless of fluid level in the reservoir.

With a constant supply of fluid, you'll see repeatability in dispensing like never before. Your dispense process could use an FPC injection!

Consistent & Reliable Process Results

MAX Series Precision Dispensing Systems will improve the reliability of your dispense process. Standard features of 0.0254 mm (0.001") accuracy, close-loop nozzle calibration, and nozzle cleaning eliminate setup variations between operators. MAX Series systems will compliment your micro-electronics and semiconductor dispense processes.



With a wide range of available dispense pumps, the MAX Series will take you to the next level.

Supplying a full range of precision dispense products.

GPD Global
Precision Dispensing Systems

+1.970.245.0408 • request@gpd-global.com • www.gpd-global.com

and deposition steps (including flexible systems that can combine different process steps), we are helping to solve the most difficult process issues at the R&D level. This positive learning will be crucial for transition-to-production scenarios. Close collaboration between vendors and OSATs, IDMs or foundries, with common roadmaps and mutual goals, is the key ingredient to lowering the cost and technical hurdles for next-generation packaging methods.

Summary

The era of 2.5D is here and packaging of true 3D die stacking will start soon. This is perhaps the biggest change in the industry since the introduction of copper (Cu) interconnects in the late 90s. It has been an enormous undertaking, touching all steps of the device manufacturing process from end-to-end. However, although near, there is still work to be done before TSV packaging becomes the industry standard. By adopting a more open working model with equipment vendors and leveraging their knowledge, I believe that the time to HVM can be reduced.

References

1. Samsung Wide IO Memory for Mobile Products - A Deeper Look, Yole Développement Feb 2011 (<http://www.i-micronews.com/lectureArticle.asp?id=6503>).
2. 3D Glass & Silicon Interposers report, Yole Développement Sept 2012 (http://www.i-micronews.com/upload/Rapports/3D_Silicon_&Glass_Interposers_sample_2012.pdf).

Biography

Kevin Crofton received a bachelor's degree in Aerospace Engineering from Virginia Tech and has an MBA with a concentration in international business from American U. He is EVP and COO at SPTS Technologies; email kevin.crofton@spts.com

MARKET TRENDS



Mobile products: driving developments in materials for packaging and assembly

By Dan Tracy [[SEMI](#)] and Jan Vardaman [[TechSearch International, Inc.](#)]

Semiconductor packaging materials are forecast to grow from \$18.7 billion in 2013 on a global basis to almost \$20.0 billion in 2017, according to the latest Global Semiconductor Packaging Materials Outlook (GSPMO) jointly published by SEMI and TechSearch International. This represents a compound annual growth rate (CAGR) of just 1.3%. Excluding gold wire, CAGR increases to 3.6%. Downward pricing pressures, cost reduction activities, growth in smaller and thinner packages, and modest overall semiconductor unit growth all contribute to the revenue growth outlook for packaging materials.

Advanced packaging remains the main driver for materials consumption and new materials development, and the outlook for these packages remain strong. These packages include ball grid array (BGA), chip-scale packaging (CSP) (including lead frame-based), flip-chip, WLPs, and various 3D packages such as stacked-die and PoP. Flip-chip packaged units will grow at a CAGR of 25% between 2012 and 2017 with wireless products driving the growth. Over the same timeframe, WLP, which has already experienced strong growth in unit shipments, is forecasted to grow at an 11% CAGR because of the strength in the mobile sector. Stacked-die packages will grow at a CAGR over 5%.

It's a mobile world

Mobile devices such as smartphones and tablets are driving both the package development and unit volume growth in the semiconductor industry. Today's wafer-level packages (WLPs), package-on-package (PoP), and stacked die chip-scale packages (CSPs) will remain

popular — along with a number of others, such as QFNs and FBGAs. Ever demanding requirements for thin packages are creating challenges for semiconductor makers and the companies that assemble their packages.

Organic substrates: mobile growth saves the day

Organic substrate packages remain one of the largest segments of the semiconductor packaging materials market. Flat to declining growth in the PC industry, coupled with silicon integration and the use of multiple die in a package resulted in slower growth in large body size flip-chip substrates. Because substrates account for 50 to 70% of the total assembly, cost reduction remains a goal. Yields have improved for flip-chip substrates, but as a result of price pressure and an oversupply of capacity resulting from reduced demand in the PC sector, prices have seen a dramatic decline from 2012 to 2013. Greater consolidation in the number of suppliers for flip-chip BGA substrates is expected. The trend is expected to be similar to the decline of companies offering PBGA substrate for wire bond packages because of the low margins. The bright spot, however, is the flip-chip CSP (FC-CSP) segment. The strong growth in mobile products with the increased use of flip-chip calls for a projected 20% market growth rate in the market for FC-CSP substrates.

Underfill material trends

The growth in flip-chip is also driving the demand for underfill material. There

are three primary types of underfill processes in production today: capillary, molded, and pre-applied. Interest in pre-applied materials is strong given the challenges in dispensing underfill as bump pitches and heights become finer. While non-conductive paste (NCP) has been introduced for FC-CSP applications, there is also strong interest in non-conductive film (NCF) materials. New suppliers and formulations of NCF materials are anticipated over the next few years. These materials are expected to see expanding use with the introduction of micro bumps for 3D-IC stacked die with TSVs.

Wafer-level packages: the lowest profile

Wafer-level packages (WLPs) continue to be one of the solutions adopted by many product makers, but the increasing I/O counts are driving the need for new material developments. Much of the growth in WLP remains driven by the demand for low profile packages. Historically, the devices packaged in WLPs were small die sizes with low pin counts (<100), but new product introductions having higher pin counts (up to 500) and 8mm x 8mm die sizes are available. Interest in fan-out applications is growing, though lower cost solutions are desired to drive a broader adoption of this WLP technology.

Wire bond: still here!

The demise of wire bond has been predicted for the last 20 years, but the technology remains the workhorse of the industry. Despite the strong growth in

flip-chip and WLPs, there are still many wire bond packages in production today and the materials used for these packages continue to see strong growth, especially with the growth of quad flat no-lead (QFN) packages and stacked-die CSPs. The die attach film (DAF) market continues to experience strong unit growth, though revenues have weakened with more competition in the market. Improved thermally conductive pastes and films are desired in the market, and suppliers continue to focus on material advancements to enhance such performance. The die attach materials market will reach \$665 million in 2013 and is expected to see growth through 2017.

Summary

The years ahead for semiconductor packaging materials promise to be exciting. As packages evolve to meet the needs of high-growth areas such as smartphones and tablets, new material needs will drive continued material developments. Major findings from the GSPMO report point out the advancements and changes expected in the semiconductor packaging materials market over the next several years. Opportunities include:

- Cost reductions across all material and process sets;
- Fine feature substrates to support bump pitch reductions corresponding with the introduction of 14nm node silicon;
- Thinner core substrates will be needed to meet the demands of low profile packages;
- Substrate materials that provide a low coefficient of thermal expansion (CTE) are required to help address warpage issues;
- Softer Pd-coated copper wire for circuit under pad applications;
- Mold compounds, liquid encapsulants, and die attach materials with low ionic levels compatible with copper and silver wire bonding;
- Moisture level sensitivity 1 mold compounds and encapsulants for bare copper wire, Pd-coated copper wire, and silver alloy wire;
- Better/more thermally conductive

mold compounds and die attach materials for power devices; for die attach, this includes conductive die attach films;

- For mold compounds, low α_1 materials with high thermal conductivity properties; and
- DAF materials with thickness 10 μm and under.

In conversations between material suppliers and their customers, cost issues will continue to dominate the conversation as the end electronics market demands low-cost solutions for the consumer. Gold metal pricing has driven the movement to copper wire and, more recently, silver wire, and even with slight declines in the price of gold, the direction has not changed. Low-cost solutions also call for high-density laminates, matrix lead frame design, underfill material, and die attach film. Suppliers and customers continue to look for solutions to reduce material usage and to improve manufacturing throughput

and efficiencies. Companies across the supply chain will need to collaborate to balance the needs of new materials development and cost reduction efforts.

Acknowledgment

For more information about the SEMI packaging reports, visit: www.semi.org/en/MarketInfo/PackagingMarket.

Biographies

Dan Tracy received his PhD in Materials Engineering from Rensselaer Polytechnic Institute, an MS in Materials Science and Engineering from Rochester Institute of Technology, and a BS in Chemistry from SUNY. He is Senior Director of Industry Research at SEMI.

E. Jan Vardaman received her MA in Economics from the U. of Texas at Austin and is President and founder of TechSearch International, Inc., which has provided analysis on technology and market trends in semiconductor packaging since 1987.



Advanced Packaging ECD & PVD

Beyond
Imagination.



Stratus ECD



Apollo PVD

Over 7M wafers per year
plated & sputtered worldwide in
high volume manufacturing

total.support@us.tel.com
www.TEL.com

GUEST EDITORIAL



Putting 2.5D in perspective – an overview of a budding technology

by Joseph Fjelstad [*Verdant Electronics*]

Anyone with any interest in the field of electronic packaging has doubtless run across the term 2.5D many times over the last few years. It is a curious term, as it would likely leave a first term geometry student scratching his or her head. In geometry (and for the purist) 2D is very simple to understand as a two-dimensional structure is simply a plane having X and Y dimensions only. It is useful for circumscribing an area in standard and agreed upon units for many possible practical uses from defining a plot of land (hectares) or the footprint of a house (square meters), to providing standard units for the purchase of a generally planar material of any imaginable sort. In our physical world, however, everything is actually three-dimensional as there is always a Z element present even in a piece of paper, for example. (The possible exception is the recently announced single atomic layer sheet of graphene, which begs the question are atoms three dimensional constructs?)

Thus, 2.5D has been set up to provide a shorthand way of describing something that resides somewhere between a plane and a solid. Somehow, however, it still seems inappropriate when applied to physical reality as artificial construct, but it is one that nevertheless serves to describe and provide some practical purpose in certain cases. For example, the term 2.5D has proven a useful term in

describing certain generally planar technologies, and most specifically, it seems to have been one that plays well within the electronic gaming industry. If one does a little digging on the internet, one will find that (according to Wikipedia) the term 2.5D originated within the video game industry and has been used to describe either: 1) 2D graphical projections and techniques that cause a series of layered images or scenes to appear to be three-dimensional (3D), when in fact they are not, or 2) gameplay in an otherwise three-dimensional video game that is restricted to a two-dimensional plane. With some loose interpretation, both of these definitions can be construed as being somewhat applicable relative to the run-up of attention given 2.5D in recent years relative to the matter of electronic interconnections at the chip in package level, in that 2.5D is fundamentally a construction comprised of 2D interposers that remain physically indistinguishable from 3D to the untrained observer. In truth, at least to this observer, it appears that the only distinguishing factor for 2.5D in present usage within the electronics packaging industry is that the interposer substrate most often cited and used, is largely silicon or glass (however, organic/PCB technology also finds its way into the mix) and the chosen substrate is normally supplied with TSVs or through-silicon (or silica) vias to allow for connection from the upper surface

of the interposer to the backside. (Obviously, the term TSV is unsuitable for organic/PCB constructions.)

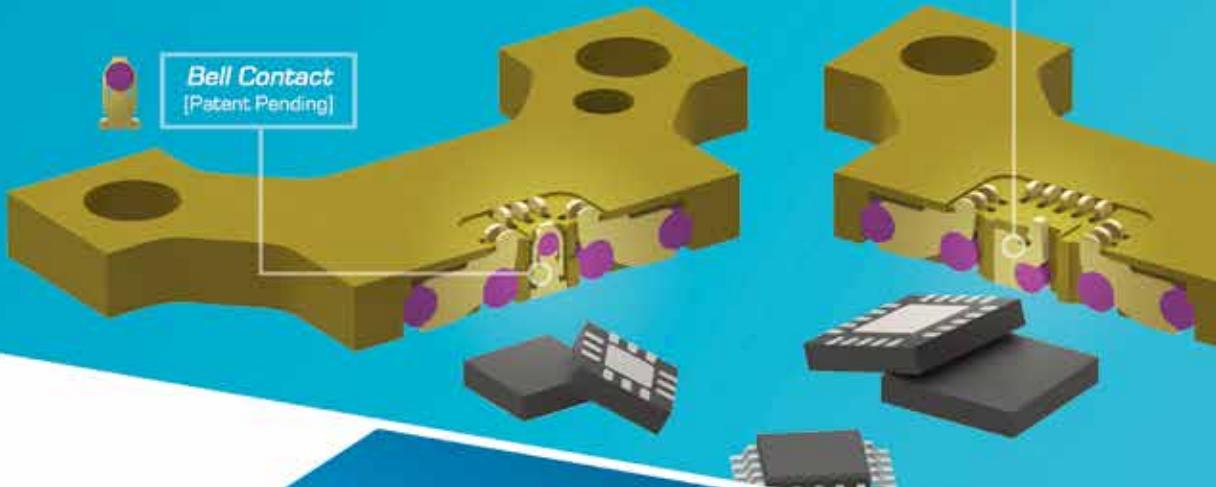
These 2.5D enabling structures are also provided with interconnection paths and terminations to manage the redistribution of I/O from the upper surface to the lower surface to provide an interconnection interface that is more manageable than might otherwise be achieved using bare die. Thus, 2.5D is, at the end of the day, fundamentally an interposer on interposer construction that is populated with semiconductor chips having a mix of functions. Curiously, such constructions are in many ways indistinguishable from the multi-chip modules (MCM) introduced to the market with a great deal of fanfare in the late 80s and early 90s. So why is there such attention given to this intermediary concept?

There are a number of possible and practical reasons for using these so-called 2.5D structures. One of the first benefits of using silicon or glass as an intermediate and interposing substrate is that there is an established base of prospective manufacturers of 2.5D interposers that can make the substrates using semiconductor manufacturing techniques. This allows the producers to create circuit patterns and holes of extremely fine dimension opening the doors to the possibility of attaching chips in flip-chip fashion where the terminations are on a much finer pitch than might be achieved using more



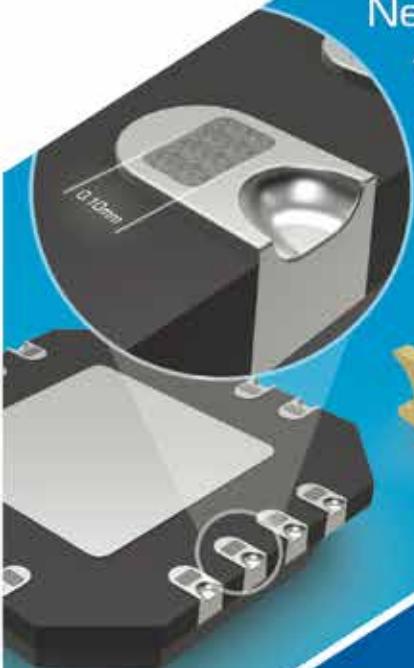
Need Compliant Grounding for
small packages of 2x2 and above?*

We have the solution.



Need Short Wiping of 0.1mm
for your wettable/dimple pad?*

We have the solution.

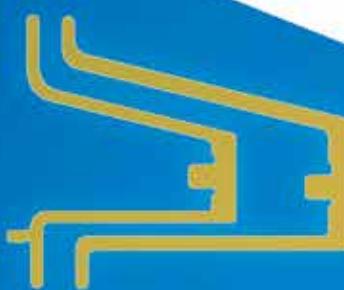


Zigma
[Patent Pending]

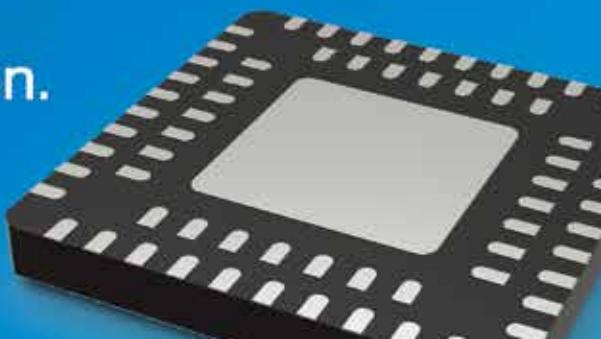


Need Scrubbing
Solution for Dual
Row packages ?*

We have the solution.



Alpha
[Patent Pending]



traditional interposer substrates. By way of example, in a 2.5D assembly, the flip-chip devices are attached first to an interposer using micro-bumps (on the order of 10-25 μm in diameter) that redistributes the terminations from the chips with fine-pitch wiring to the opposite side using TSVs fanning out to a coarser pitch with appreciably larger solder balls (nominally 100 μm in diameter). From a performance perspective, the structure can offer a significant improvement in performance over wire bonded 3D alternatives, but it appears more a stop gap solution at present because of the added cost.

While the semiconductor technologies employed to make 2.5D interposers excel at making the fine features required for dealing with fine pitch flip-chip assemblies just discussed, another key distinction and benefit of 2.5D appears to be the technology's ability to address coefficient of thermal expansion (CTE) mismatch with the silicon chips that are attached to a surface. Dealing with CTE mismatch has been one of the important roles that IC packaging of every sort has been tasked with since the earliest days of the semiconductor industry. Two elements from the periodic table

stand out in the world of electronics manufacture; those two are silicon used for IC manufacture, and copper used for nearly all interconnections. These two elements have an appreciable difference in CTE at $\sim 3\text{ppm}/^\circ\text{C}$, and $18\text{ppm}/^\circ\text{C}$, respectively. Getting these key materials to work to in proximity to one another over a range of temperatures is an important task of the IC packaging designer. Interposer solutions have long served this function and with 2.5D, the need remains and it is accomplished by means of solder balls that connect flip chips to interposer and interposer to package substrate. The general plan of a 2.5D construction using current understanding and definitions can be seen in [Figure 1](#) and an insert is provided to allow comparison with an assembly that is generally considered representative of a 3D construction.

In summary, whether 2.5D is an appropriate and accurately descriptive term or not, is perhaps moot since it already has standing. In that regard, it is a matter perhaps best left to those trying to differentiate and market the various competing concepts that have come into being to address the significant challenges facing those tasked with bringing ever higher performance chip set solutions to market in a timely manner. Whether or not the industry will rally around a single 2.5D solution, or embrace multiple methods, remains to be seen. One thing that does seem certain is that 2.5D is likely to see increased use in appropriate applications on a continuing basis into the future.

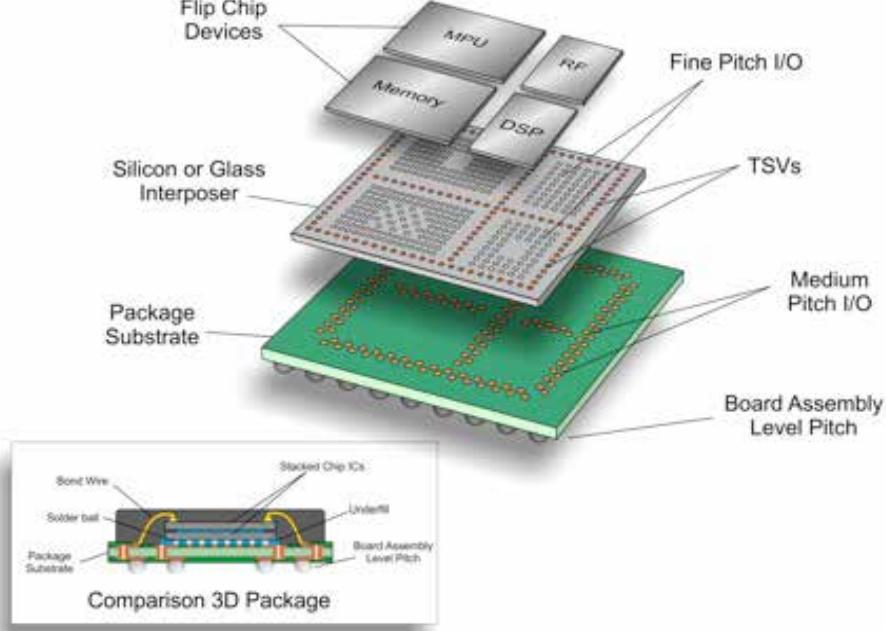
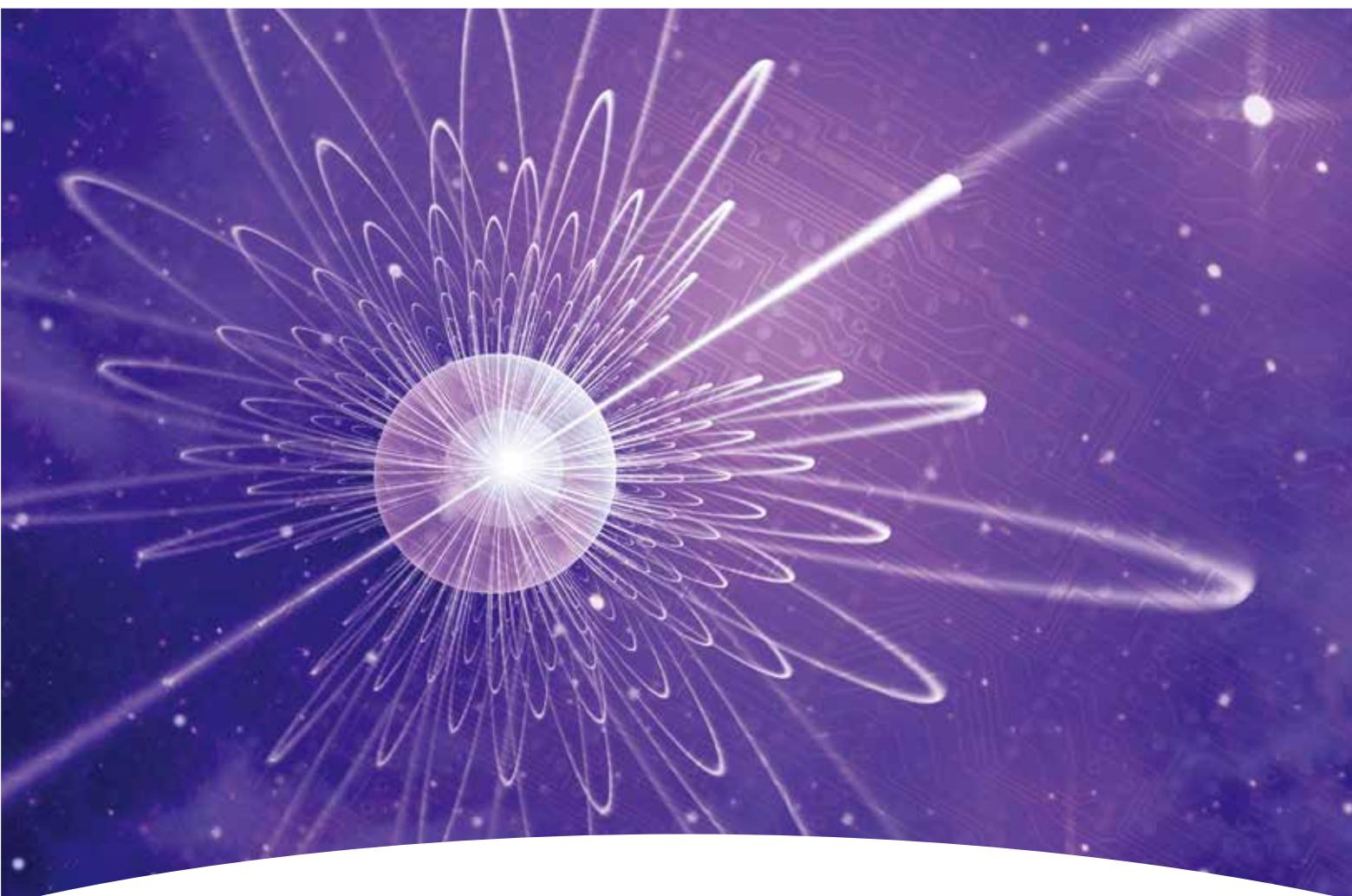


Figure 1: 2.5D package construction. This exploded view of 2.5D technology illustrates how the technology serves to bridge the gap between the ultra-fine pitches used on flip-chip devices by means of an interposer, which helps to translate the pitch to one more easily handled both as a package and ultimately, at board-level assembly as illustrated. A representative 3D package assembly is shown in the insert for comparison.

Contact author

Joseph Fjelstad is CEO and founder of Verdant Electronics.
joe@verdantelectronics.com

reduce soft errors



Deliver more density on your IC packages without soft errors.

Honeywell RadLo™ low alpha packaging materials help eliminate soft errors and single event upsets by reducing alpha emissions, a significant source of these problems. This is becoming increasingly important as chip dimensions and designs continue to miniaturize. Our leadership

and expertise in low alpha refining and metrology mean that Honeywell can help you meet critical alpha emission levels.

Honeywell reliability. Reliable low alpha. Make sure to ask your suppliers if they are using Honeywell RadLo low alpha materials for their chip packaging processes.

Honeywell

Find out more by visiting us at www.honeywell-radio.com

imec performs world-leading research in nanoelectronics

imec
Kapeldreef 75
B-3001
Leuven, Belgium
Tel: +32 16 28 12 11
Fax: +32 16 22 94 00
info@imec.be



Headquarters and main campus - Leuven, Belgium

About

imec performs world-leading research in nanoelectronics and leverages its scientific knowledge with the innovative power of its global partnerships in ICT, healthcare and energy. The consortium delivers industry-relevant technology solutions, and in a unique high-tech environment, its international top talent is committed to providing the building blocks for a better life in a sustainable society. Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China, India and Japan. In 2012, imec's revenue (P&L) totaled 320 million euro.

Background

imec was founded in 1984 as a non-profit organization, led by Professor Roger Van Overstraeten. It has a staff of more than 2,000 people, including more than 650 industrial residents and guest researchers. Imec has grown to be a multi-disciplinary expertise center in the fields of semiconductor chips and systems, electronics for life sciences, body area networks, energy, photovoltaic, sustainable wireless communication, image sensors and vision systems, and flexible electronics and displays. Through innovations in nanoelectronics, imec has collaborated with numerous partners from universities, research institutes and top companies, creating solutions and developing emerging technology for a sustainable environment.

In the domain of semiconductor technologies, imec has enabled notable advancements in global semiconductor chip manufacturing in the three decades since its founding. At the forefront in advancing immersion lithography, EUV, and double patterning, imec has driven lithography as a key solution to overcome the challenges in scaling down features in silicon chips. In 2013, imec and ASML broadened their partnership with the launch of a Patterning Center. When complete, this Center will offer the global semiconductor ecosystem the most advanced patterning knowledge for sub-10nm technologies, crucial to addressing future scaling and infrastructure challenges. This Center will be extended through partnerships with other suppliers into a 'Suppliers Hub,' to collaborate on the development of next-generation process technology solutions.

Mission statement

imec aims to shape the future through world-leading research in nanoelectronics. With imec's global research partners, it leads the development of nano-enabled solutions that allow people to have a better life in a sustainable society.

Board of directors and executive management team

Since 1984, imec has been led by Roger Van Overstraeten, Gilbert Declerck (June 1999), and Luc Van den hove (July 2009).

imec's 3D systems integration technology solution

imec's industrial affiliation program on 3D-IC technology explores technology options to define innovative solutions for cost-effective realization of 3D interconnect with through-silicon-vias (TSV). Imec's 3D integration processes are completely executed on 300mm. To give our partners maximal information, we integrate and test baseline 3D-processes and flows on functional circuit demonstration vehicles. Imec also explores 3D design to propose methodologies for critical design issues, enabling effective use of 3D interconnection on system level.

Chip Scale Review staff interviews Eric Beyne, Program Director 3D System Integration, imec

Eric Beyne is an imec fellow and director of the 3D system integration program. This team performs R&D in the field of high-density interconnection and packaging techniques focused on 3D-interconnectivity.

Eric obtained a degree in electrical engineering in 1983 and a PhD in applied sciences in 1990, both from the University of Leuven (KU Leuven). He has been with imec since 1986. He also serves as president of the IMAPS - Benelux committee.



Given the state of the semiconductor packaging industry - including all the technical and financial challenges associated with R&D for advances - what are the top one or two issues the industry must tackle over the next 18-24 months and why? Do you have proposed solutions for these challenges?

For 3D integration, the focus will be on improving technology readiness: in particular, thin-wafer carrier bonding and debonding, and 3D stacking. Business aspects of availability and testability are also becoming increasingly important. Electrical testing of TSV-based 2.5D and 3D-SICs to guarantee outgoing product quality to the customer is expensive because of the complexity of the advanced design and the many possible steps for testing in the manufacturing flow: pre-bond (before stacking), mid-bond (on a partial stack), post-bond (on a completed stack), and final testing (on a packaged device). It is, however, critical to save costs later on in the production process.

How will your company participate in addressing the issues you raised in your response to question #1?

We are collaborating with both material and equipment suppliers to improve the technology readiness of thin wafer carrier solutions. With respect to 3D assembly, we are studying integration and reliability challenges for microbump pitch assemblies scaled down to 20 and 10µm pitch. In particular, the use of wafer-applied underfill and high-throughput thermocompression bonding is studied. We're also looking into the scaling potential of alternative, direct metal chip-to-chip interconnections. Thermal management issues – caused by the use of bonding adhesives with poor thermal conductivity, by the vertical stacking of the chips and by the reduced thermal spreading due to the aggressively thinned dies — are considered one of the major challenges for 3D integration. We are also collaborating with partners worldwide to develop standardized automated test solutions to bring 3D stacked IC technology to high-volume manufacturing. Non-destructive test methods such as SAM, or probing solutions, are also being developed to detect voids and defects, to test for connection quality, or electrical performance.

How is your participation in standards activities, as well as your research activities as a consortium, helping to meet the technology challenges that lie ahead in the next 2-5 years?

Within the imec 3D research program, a large number of companies are aligned through collaboration, which helps drive conversion of technology routes. In some cases, standardization may be too restrictive in a new application field such as 3D integration, so convergence in technologies and approaches is therefore of equal importance. We're also directly involved in IEEE's standardization efforts on design for 3D test.



Recent significant technology developments

Imec presented a paper at IEDM 2013 providing, for the first time, comprehensive and early guidelines for TSV integration in 10nm node FinFET technology. Imec studied both direct 3D and interposer-based integration, and demonstrated several test vehicles with active silicon die. This allows in-depth study and validation of electrical, thermal and mechanical models. One example is the validation of thermal modeling by FEM, or by the much faster compact thermal model approach using a high power 3D test vehicle, "PTCQ." This chip stack allows for programmable power dissipation locations ("hot-spots") and comprehensive thermal characterization through build-in CMOS temperature sensors. An excellent agreement between experiments and modeling was demonstrated.

Probing 25µm-diameter micro-bumps for Wide-I/O 3D SICs

by Ken Smith [Cascade Microtech] and Erik Jan Marinissen [imec]

Three-dimensional stacked integrated circuits (3D SICs) are emerging as a solution to the speed, power and density requirements demanded by future mobile electronics, as well as high-performance and networking platforms. Through-silicon vias (TSVs) used in 3D SICs shorten interconnects between integrated circuits (ICs), thus reducing power while increasing performance. The electrical inter-die interconnects are typically implemented by means of large-array small-diameter micro-bumps. Wide-I/O DRAM on logic has been identified as a key application for the commercialization of 3D SICs. However, compound product yield conspires to delay full adoption of 3D SICs.

Probe test is essential to improving final stack yield by preemptively identifying the defective devices so they are eliminated before being integrated into otherwise good stacks. Increased test has incremental cost at the die level, but increases yield at final assembly. However, the small dimensions and large array sizes of micro-bumps have made probe test difficult to perform. Researchers at imec have been working in imec's Industrial Affiliation Program on 3D Integration with probe technology partner Cascade Microtech to meet these challenges. They have successfully probed imec test wafers containing a JEDEC Wide-I/O compliant array [1] with 25µm-diameter micro-bumps with a high level of accuracy due to the probe-to-pad alignment features of the probe system and the probe card technology used. This article will discuss the large-array, fine-pitch, low-force requirements specific to probing 3D SICs, and detail the methods and tools developed specifically to meet them.

3D SIC assembly test points

Four test points have been identified in the 3D SIC assembly flow. Test point #1 takes place pre-bond, prior to stacking. If the stack consists of three or more die, there is also a mid-bond, partial-stack test. Third is a post-bond test of the completed stack, and lastly is final test performed on the packaged device.

Pre-bond tests may vary in test quality. Virtually all cost modeling exercises agree that some level of pre-bond testing is required to achieve acceptable stack yields. The ultimate in pre-bond testing is known-good die (KGD) testing. KGD testing is a pre-bond test with a quality level equal to final testing, including coverage of at-speed defects and burn-in. KGD testing is especially important when the die or wafers are procured by one manufacturer from another, as the manufacturer procuring the KGDs does not want to pay for bad dies.

Test access for pre-bond testing of the bottom die, as well as mid-bond and post-bond testing of the stack, is through the external I/Os of the bottom die. These I/Os are implemented as large Cu pillars or controlled collapse chip connection (C4) bumps, and therefore probing them is relatively easy. Pre-bond testing of middle and top dies of the stack requires probing on the large-array fine-pitch micro-bumps, and that is where the challenge comes in.

The current workaround

Major semiconductor device manufacturers are already engaged in production of 2.5D and 3D SIC devices, yet they are unable to probe bumps below 50µm pitch. They have developed a workaround by using additional, dedicated test pads to facilitate pre-bond testing (**Figure 1**). Unfortunately, dedicated probe pads come at the expense of increased design effort, more silicon real estate, additional processing steps and test

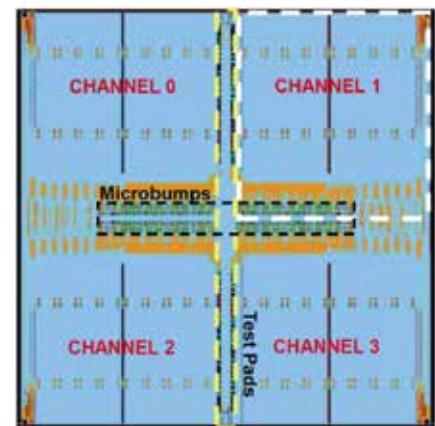


Figure 1: Dedicated test pads are used as a workaround for probing on fine-pitch microbumps. SOURCE: Kim et al., Samsung – ISSCC 2011, reprinted courtesy of ISSCC.

application time, as well as extra capacitive load on the micro-bump I/O during post-bond functional stack operation. Moreover, testing through dedicated test pads still does not prove the functionality of the micro-bumps themselves. What is best is a solution that allows direct probing on the micro-bumps.

Probe requirements

The target micro-bumps dictate that the metallurgy to be probed is either Cu or Cu (Ni) Sn. For this work, the existing JEDEC Wide-I/O standard of 25µm/15µm diameter, 40-50µm pitch, with an array size of 4x (6 x 50) was used (**Figure 2**).

Allowable configurations include up to four DRAM “ranks” stacked either on top of the logic die to achieve true 3D, or next to the logic die on an interposer for 2.5D structures. The logic/memory footprint consists of four channels with 300 micro-bumps per channel. Each channel has 128 bi-directional data bits to create the wide I/O, as well as an independent address, control and clock. The interface has shared power and ground.

To perform the pre-bond test by

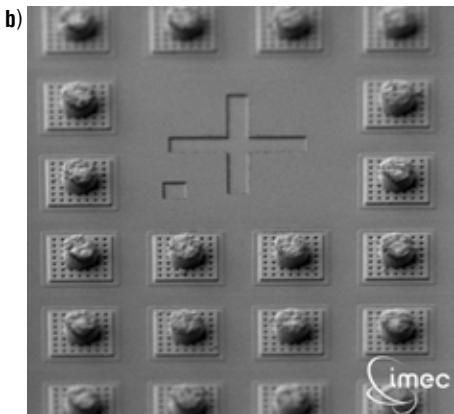
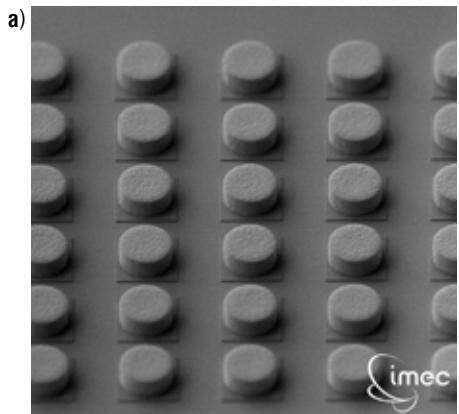


Figure 2: a) (left) 25µm-diameter Cu micro-bumps, and b) (right) 15µm-diameter Cu/Ni/Sn micro-bumps.

directly probing micro-bumps, three key requirements have been identified: good electrical contact; limited probe marks; and acceptable cost. Electrical contact calls for low resistance ($<5\Omega$) so as to not impair pre-bond testing of the die. The probe mark profile must be kept under 500nm to keep from impairing downstream bonding. Lastly, the costs of probe cards and stations need to be reasonable.

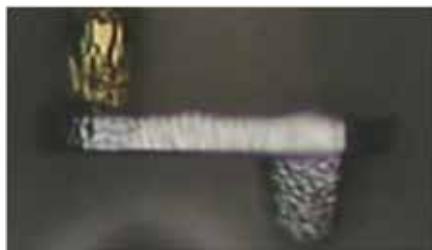


Figure 3: Rocking beam interposer Pyramid Probe®.

The right tools for the job

For its development work, imec partnered with Cascade Microtech to evaluate an advanced version of its Pyramid Probe® technology, and performed probe testing on the company's CM300 probe station, currently installed in imec's 300mm clean room.

This second generation of the MEMS vertical probe separates the probe tip from the interconnect and puts routing in a separate layer to provide finer pitch and replaceable contacts with more compliance. The probe requires significantly lower force—1g instead of 10g—to achieve adequate contact. Additionally, the probe tip pitch is scalable down to ~20µm (Figure 3).

An accurate probe station is required to ensure that the probe card contactor consistently lands in the right spot. Dual cameras align the wafer with the probe card to achieve the necessary alignment accuracy. The wafer moves in the z-direction and comes in contact with the vertical probe card, which remains stable. As this pre-bond step takes place in the clean room environment, the probe station

CSP Test Sockets

**Now Available
Down to 0.2mm Pitch!**

**A lot more of
what you need...**

**...a lot less of
what you don't!**

MORE PERFORMANCE
High-frequency (>40 GHz) sockets with a variety of materials to meet diverse testing requirements from Bench Characterization to Fully Automatic Handlers (>500k cycles) delivering what you need.

MORE CHOICES
Industry's widest available DUT interfaces – Spring Probes, Microstrip™ Contacts and two types of Conductive Elastomers.

LESS COST
All DUT interface materials available in off-the-shelf molded plastic for a fraction of machined housing cost.

LESS WAIT
Aries can deliver the exact sockets you need in four weeks or less! So why settle?

**ARIES®
ELECTRONICS, INC.**
Bristol, PA 19007-6810
Tel 215-781-9956 • Fax 215-781-9845
Email: info@arieselec.com
www.AriesElec.com

*The Evolution of
Interconnect Innovation*

must be clean room compatible.

Probing 25µm-diameter micro-bumps

The goal of this work was to probe fine-pitch micro-bumps without causing damage, while establishing good electrical contact from the test equipment to the device-under-test, and vice versa.

The wide-I/O probe card touched down on channels A and B to check landing for daisy-chain resistance and probe marks. The aim was to check the influence of probing on stacking. The test demonstrated identical probe marks and a smooth contact resistance profile. The probe mark consistently measured 6µm, which corresponds to the heel of the diagonally-placed square 6×6 µm² probe tip. From the very shallow probe mark, no negative stacking yield impact is expected (**Figure 4**).

Probing 25µm Cu micro-bumps has been successfully achieved, and imec researchers are in the process of probing 15µm Cu Sn-capped micro-bumps, which requires even greater accuracy.

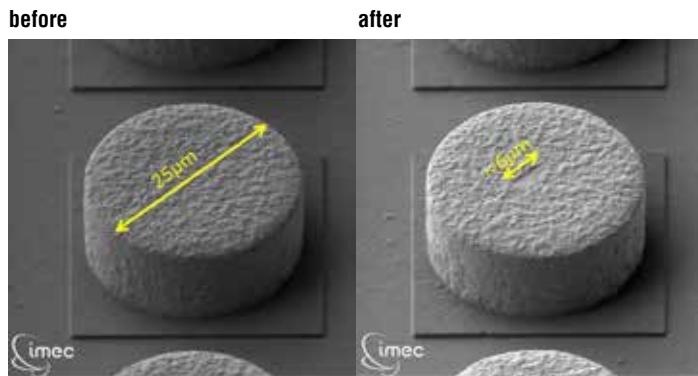


Figure 4: Example of a 25µm-diameter bump before and after probing.

Cost modeling [2] of probing micro-bumps directly versus using dedicated pads indicates that probing on micro-bumps is a lower-cost alternative to testing through dedicated probe pads. The main differentiator is the reduction in test time by avoiding the slow data rates associated with driving data through

the reduced set of dedicated test pads, which would make test a significant contributor to the overall cost. Die yield works as a multiplier (at 50% yield, two dies must be tested to find one good one). Comparatively, the cost of probe cards is minor.

Next steps and ongoing work

All the work thus far has been performed on an imec test vehicle dubbed Vesuvius, which was set up for both 3D tests and 2.5D with a passive interposer. The first phase involved interposer wide-I/O probing. The second phase was Vesuvius wide-I/O probing, and the third phase was a 2.5D stack to check daisy-chain bond yield.

While there are four channels to be tested, today the wide-I/O probe card only covers a single-channel (300 micro-bumps) per touch-down (**Figure 5**). This probe card allows for the study of probe mark impact on the stacking yield, by probing Channels A and B on the (bottom) interposer and

Channels B and C on the (top) Vesuvius dies. However, this is in the scope of the experimental test chip only. On a real wide-I/O product chip, all four wide-I/O channels would be probed and would require four

subsequent touch-downs. Development of a probe core that covers all four channels in a single touch-down is underway.

The drive to finer pitch micro-bumps

Today's micro-bumps come in large arrays at 40-50µm pitch. Pitch

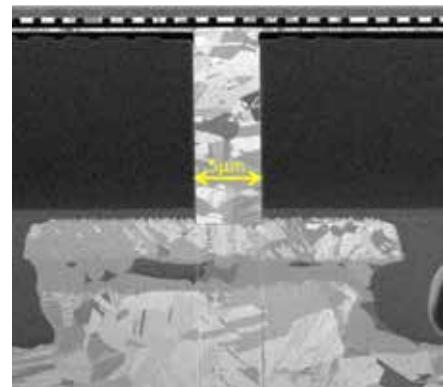


Figure 6: Micro-bumps determine pitch, not TSVs. This SEM photo shows a TSV of 5µm diameter by 25µm height on top of a much larger Cu/Sn micro-bump.

is determined by the sum of the bump diameter and the space in between. Typically, bump diameters are 50% or less of the bump pitch. Conventional probe technology can probe 90µm pitch arrays, which have 40-50µm-diameter bumps. They cannot handle 40-50µm pitch bump arrays with bump diameters of 15-25µm. Cascade Microtech's advanced probe technology has been shown capable of successfully probing 25µm-diameter bumps and 40-50µm micro-bump arrays.

In the near future, there will be pressure to further reduce the micro-bump pitch. Although there isn't any JEDEC standard for finer DRAM pitches, logic-to-logic partitioning will assuredly drive the industry to finer pitches. Because 10µm TSV pitches can already be achieved, the burden of increased interconnect density falls to the micro-bumps, and pressure is on to further shrink that pitch to 20µm and even 10µm (**Figure 6**). Test chips with 20µm-pitch micro-bumps are already available, but it will be an uphill battle to follow the shrinking pitches of the micro-bump roadmap. This push to finer pitches is putting pressure on probe test methodologies, as well as contactors and equipment suppliers to find solutions that enable fine-pitch, low-force probing.

Work is also underway to address the issue of signal integrity. Three elements to

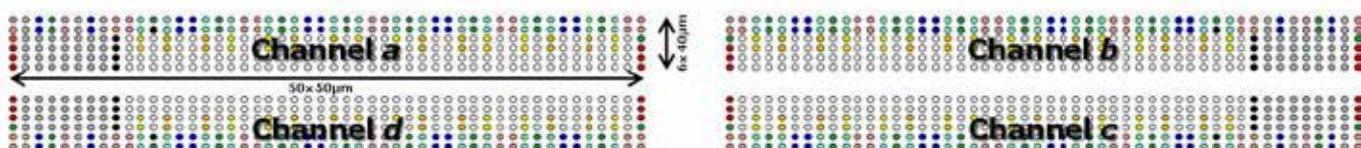


Figure 5: Wide-I/O DRAM interface is laid out in four channels, tested in pairs.

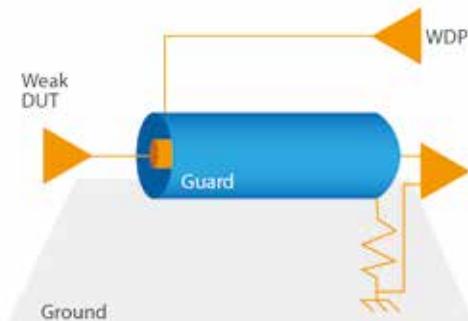


Figure 7: Schematic of the weak driver pre-charge concept.

manage this have been identified, including signal routing density, clean power delivery, and weak I/O driver limitations. The wide bus and the I/O are not designed for driving current to automated test equipment (ATE). Weak driver pre-charge (WDP) is a recent breakthrough that involves pre-charging the tester interconnect to a large percentage of the predicted output level. **Figure 7** shows a guarded ground reference for the weak I/O signal lines that is charged by an additional pin driver. The guard is charged in time with the expected output

of the weak driver so that there is no voltage differential between the signal and guard, which essentially eliminates the capacitive load of the interconnect. Simulations indicate the expected improvement in rise time and prototype experiments are underway to validate the approach.

Summary

3D SICs are rapidly developing and have attractive benefits. While test challenges remain, work is progressing, particularly in the area of probe technologies and pre-bond test. Direct micro-bump probing is proving to be a more cost-effective and technologically complete method than dedicated pre-bond probe pads. However, it requires advanced probe cards and probe stations. Recent work on test wafers has resulted in successfully probing single-channel wide-I/O micro-bumps at 25 μ m diameter. Work continues to further prove out this methodology on actual wide-I/O DRAM.

References

1. Wide I/O Single Data Rate (JEDEC Standard JESD229); JEDEC Solid State Technology Association, Dec. 2011; <http://www.jedec.org>.
2. M. Taouil, S. Hamdioui, E. J. Marinissen, S. Bhawmik, "Using 3D-COSTAR for 2.5D Test Cost Optimization," IEEE International 3D Systems Integration Conf. (3DIC'13), San Francisco, CA, Oct. 2013.

Biographies

Ken Smith received his BS in General Engineering from Oregon State U., and is a Principal Engineer at Cascade Microtech; email kens@cmicro.com

Erik Jan Marinissen received his MSc and PDEng degrees from Eindhoven U. of Technology in Eindhoven, the Netherlands and is a Principal Scientist at imec.



BPS-7200HD

Solder ball Attachment System for All kinds of BGA Packages on PCB Lamination Strip Form.

- Max Substrate capacity(mm) : 95x260
- Cycle time : 12~14sec
- Fine Pitch capability(mm) : 0.15ball & 0.30pitch.



BPS-7200FC

Solder ball Attachment System for Flip Chip Package on Unit PCB Form with Matrix Boat.

- Max Boat capacity(mm) : 150x310
- Cycle time : 15~28sec
- Fine Pitch capability(mm) : 0.20ball & 0.40pitch.



ASA-7200

Stiffener Attachment system for Thin Unit PCB and Warpage Free operation.

- 4 Chase Press by Servo Motor with Easy Conversion
- Stiffener handling : Tube or Tray
- UPH : 1300units.

"For additional information, Please visit our website or contact us."

www.sspinc.co.kr sale@sspinc.co.kr +82-32-822-0881~4

Conformal barrier/seeds for next-generation TSV filling by electroplating

Stephen N. Golovato, Tyler Barbera, Keiichi Fujita [Tokyo Electron NEXX] and Takashi Tanaka [Tokyo Electron Kyushu Ltd.]

T

he first-generation of through-silicon via (TSV) designs for interposer and die stacking (3D) concentrated on TSV features with an aspect ratio (A/R) on the order of ten. Typical via sizes are 10 X 100 μm (diameter X depth) for interposer and 5 X 50 μm for 3D applications. Ionized physical vapor deposition (IPVD) has been successful in depositing barrier and seed layers in these A/R=10 vias that allow efficient “bottom-up” filling by electroplating (ECD) using available chemistries. While these applications are currently moving to pilot lines and low scale production, development has already begun on the next generation of TSV structures for interposer and die stacking. These may be via-middle (front end) or via-last (back end) designs; they are expected to increase in aspect ratio for denser TSV arrays while maintaining a similar wafer thickness. Structures with A/R in the range of 15-20 are being designed and produced. A typical structure for interposer might be 8 X 120 μm and 2 X 40 μm for 3D. These structures will challenge all TSV formation processes, including etch, dielectric liner deposition, barrier/seed deposition and TSV fill. This article will focus on barrier/seed and

TSV fill processes. These two processes are tightly coupled since the quality of the seed has a strong impact on the ECD filling process. This impact can be on the chemistry requirements, particularly the additives that drive bottom up filling of the TSV, as well as the plating time.

The drivers for higher A/R in the next generation of TSV structures include the difficulty in processing thinner wafers, increased I/O requirements and device shrink, which require higher TSV density, and keep out zones around active devices, which will be reduced for smaller vias. These new high-A/R structures challenge our process technologies and the cost requirements to bring 3D into mainstream semiconductor production. The challenge for IPVD as the barrier seed for A/R>10 is that it is not a conformal process, but rather is thick on the top surface and becomes thinner from top to bottom inside the TSV. A perfectly conformal process would deposit an equal thickness on all surfaces. This is illustrated in **Figure 1** where coverage achieved by IPVD is compared to perfectly conformal coverage.

The thinnest area inside the via for IPVD is the bottom sidewall, so achieving the minimum required coverage for

ECD on this surface drives the process requirements. Every other surface must have thicker coverage than necessary. The ratio of sidewall seed thickness to top thickness, known as the step coverage, is minimum on the bottom sidewall and decreases with A/R. The minimum seed thickness requirement leads to higher top coverage (overburden) with higher A/R and the tendency to pinch off the smaller opening of the higher A/R via, as shown in **Figure 1a**. Thicker overburden increases the CMP removal requirement while pinch off reduces the metal flux into the via. To control these effects, etch back steps within the IPVD process to reduce overburden and pinch off are needed. Etch back occurs as part of the IPVD process because the substrate is biased producing sputtering of the surfaces. However, at A/R>10, additional etch-only steps are required. It may even be necessary to add intermediate CMP steps. All of these additional process steps drive up cost. This is illustrated by the per wafer cost-of-ownership analysis (CoO) shown in **Figure 2**. Included process steps are barrier seed deposition, ECD TSV fill and CMP. At A/R=10, single IPVD and CMP steps can be used. At A/R=20, 2-3 times longer IPVD-CMP processes may be required. The cost of the conformal barrier/seed as shown is an estimate for the three concepts to be discussed in the next section. The cost can vary $\pm 40\%$ depending on the concept. The cost consequences of the scaling of IPVD from A/R=10 to A/R=20 provide incentive for an alternative lower cost, production-worthy solution to barrier-seed requirements at A/R=20.

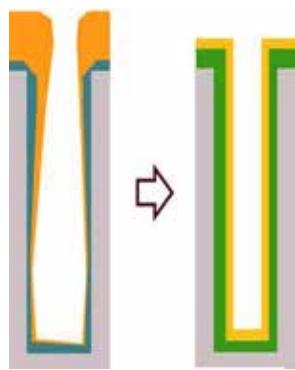


Figure 1: Barrier/seed coverage in a via a) Uneven coverage, pinch-off and thick overburden with IPVD, and b) Example of 100% conformal coverage.

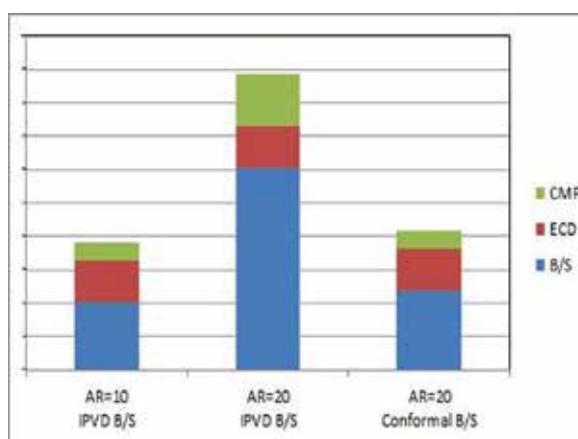


Figure 2: Cost-of-ownership analysis for barrier/seed and fill processes.

Conformal barrier/seed concepts

Key requirements for a conformal barrier/seed process include adequate step coverage, seed properties that allow efficient bottom-up ECD via fill with current chemistries, cost-of-ownership significantly lower than the competing IPVD process and readiness for high-volume manufacturing.

Another important property is the deposition temperature. For via last applications on bonded and thinned wafers where the TSV is etched from the back side, the bonding adhesive will fix the maximum process temperature to <150-300°C, depending on the adhesive. IPVD can meet this criterion. Deposition process technologies that provide good step coverage include dry processes such as chemical vapor deposition (CVD) and atomic layer deposition (ALD), and wet processes such as electro or electroless chemical deposition. All of these approaches are potential solutions for barrier/seed deposition at high A/R and have been investigated for feasibility. Examples of an ALD/CVD process, a conformal wet seed process, and an electroless process will be described here.

ALD/CVD barrier-seed. ALD and CVD are prime candidates to replace IPVD barrier/seeds at A/R>10 because of their inherent conformality. At A/R =20, an ALD barrier metal and a CVD seed metal have been tested successfully. Without the IPVD Cu seed layer, successful nucleation of Cu ECD for TSV fill has been achieved directly on a CVD metal layer that is not Cu. This direct plating is done in a conventional TSV plating solution with comparable deposition times to the conventional TSV fill on an IPVD Cu seed. The process flow is shown in **Figure 3**.

The ALD and CVD deposits are very thin with a target of 3-6nm. The depositions have conformal coverage of 100% and 80%, respectively. Although the coverage is very good for these layers, the thin seed has higher resistivity than Cu, though much lower than the barrier metal, resulting in a “terminal” effect at the TSV fill step. The terminal effect causes a voltage drop from edge to center on the wafer that leads to varying deposition rates across the wafer during the ECD process causing some voiding toward the wafer center. Several pre-treatments have been developed to compensate for the terminal effect, enabling direct void-free ECD filling of through-silicon vias up to A/R=20 using standard bottom-up chemistry. An optimized process was implemented in a Tokyo Electron Stratus ECD system. **Figure 4** shows a focused ion beam (FIB) cross section image of a filled 2 X 40µm via.

The process temperature for ALD is generally 350-400°C and for CVD can be as low as 190-210°C. For a via last application after bonding and thinning, the ALD process

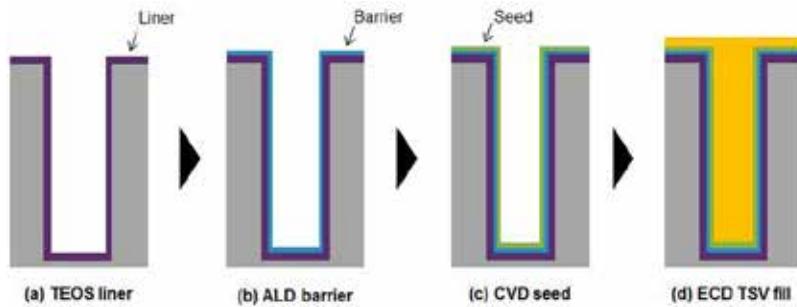


Figure 3: TSV fill process flow using ALD barrier CVD seed: a) TEOS liner; b) ALD barrier; c) CVD seed; and d) ECD TSV fill

Accurately Hit 25 µm-diameter Micro-bumps

Breakthrough technology on the CM300 Probe System lets you probe directly on Cu pillar micro-bump wafers, enabling test of 3D-TSV architectures.

The Cascade Microtech CM300, with advanced Pyramid Probe® technology, provides a solution for 3D SICs that works with “Through Silicon Vias” and allows probing of micro-bumps down to 25 µm-diameter.

Achieve greater probe-to-pad alignment precision and consistent, accurate measurements to increase performance and yield while reducing overall costs. Only Cascade Microtech delivers reliable light-touch measurement on delicate micro-bumps.

Find out more about Cascade Microtech’s breakthrough technology* at cscd.co/csr-3dtsv

CM300 Probe System
Pyramid Probe

The CM300, together with the advanced Pyramid Probe card, achieves accurate measurement on a wide I/O test wafer using a single-channel probe card with an array of 6 x 50 tips at 40/50 µm pitch.

CascadeMicrotech®

*Results achieved in collaboration with imec

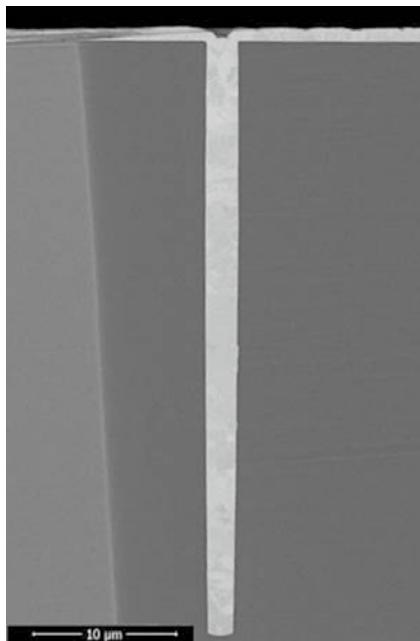


Figure 4: 2 X 40 μm via filled directly on a non-Cu CVD seed.

would be too hot but CVD is usable.

ALD barrier/conformal wet seed. Cu electrodeposition on an ALD barrier has been tested on a high-aspect ratio TSV structure. Applying high overpotential in the specific solution enables Cu nucleation directly on the barrier metal. In this case, the ALD barrier was deposited on a wafer with 5 X 50 μm TSV structures with TEOS oxide liner. The barrier thickness was 3nm and was 100% conformal, that is, equal thickness on all surfaces. Then a Cu seed was deposited on the barrier by electroplating using an additive-free conformal plating chemistry. The process is implemented by Tokyo Electron in a Stratus ECD Microstrike module. Following the conformal seed deposition, the TSV is filled using standard bottom-up chemistry in a Stratus ECD plating cell. **Figure 5** shows a schematic view of the process flow for a TSV structure.

A key feature of the process [1] flow is the addition of a standard PVD (not IPVD) Cu “conductivity” layer in the wafer surface, as illustrated in **Figure 5b**. In this case, the Tokyo Electron Apollo PVD system was used to deposit a 100-200nm thick layer. By using standard (not ionized) PVD, the Cu extends into the via only up to A/R~3. Non-uniform deposition associated with the terminal effect, which is strong for the highly resistive barrier metal, is eliminated by

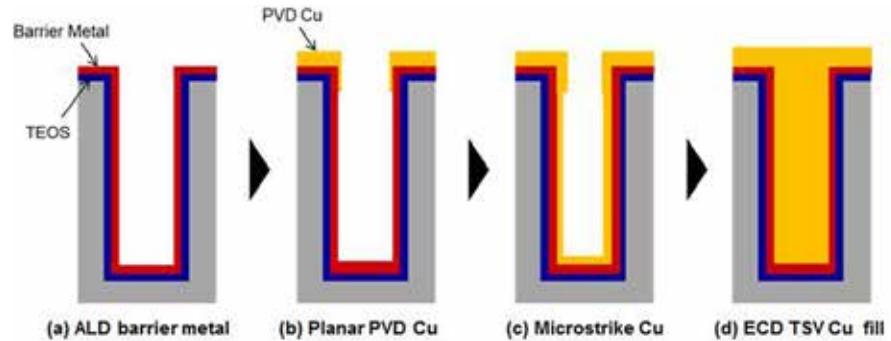


Figure 5: TSV fill process flow using conformal ECD Microstrike seed: a) ALD barrier metal; b) Planar PVD Cu; c) Microstrike Cu; d) ECD TSV Cu fill.

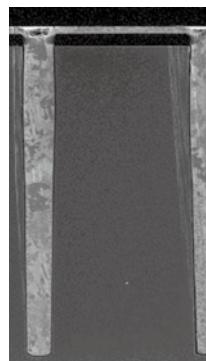


Figure 6: A 5 X 50 μm via filled directly on a Microstrike conformal ECD seed.

the PVD Cu layer. Using a simple low cost blanket PVD film only adds a small amount to the TSV cost: ~1%. After depositing PVD Cu on the field, the Microstrike process provides the conformal Cu seed (**Figure 5c**), followed by the typical bottom-up TSV Cu electroplating process (**Figure 5d**). Microstrike and TSV fill processes are performed sequentially in the same ECD tool. The current waveform applied in the conformal Cu bath was optimized in order to enhance the Cu nucleation and to promote adhesion on the ALD barrier. Filled 5 X 50 μm structures were cross-sectioned by FIB. The successful filling on the Microstrike Cu seed layer deposited in Cu citrate bath is shown in **Figure 6**.

The same process recipe for TSV bottom-up fill that had been optimized for an IPVD Cu seed worked well for the vias covered

with Microstrike Cu seed. The same TSV plating time of 22 minutes resulted in the complete fill. Because the fill time is the same as for IPVD, the Microstrike seed does not appear to have any properties that impede the bottom-up fill. Though scaling this process to aspect ratio A/R>10 has not yet been tested, there are no fundamental reasons to prevent this scaling. However, since the ALD barrier is deposited at >300°C, this process flow would not be appropriate for a via-last TSV process.

Electroless barrier/seed

Electroless Cu plating is well established for printed circuit boards (PCB) but has not been used for semiconductor interconnect applications. In PCB applications, electroless Cu is used as a standalone conductor or a seed for electroplated Cu where thicker films are required. In particular, electroless Cu is used to plate the surfaces of through holes between layers in PCBs, a similar function to the TSV seed application though at a smaller A/R. It has several features that make it attractive for seed deposition in high-aspect vias including conformal coverage and low temperature for via-last processing. In the example discussed here, an electroless barrier metal

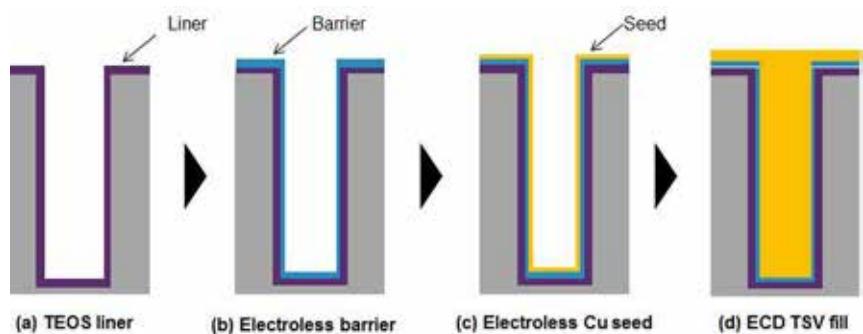


Figure 7: TSV fill process flow using electroless barrier seed: a) TEOS liner; b) Electroless barrier; c) Electroless Cu seed; and d) ECD TSV fill.

layer is followed by an electroless Cu seed layer. The process flow is shown in [Figure 7](#).

For the case discussed here, a 65nm barrier was deposited by electroless plating on a TEOS liner in 5 X 50 μm vias. This was followed by a 35nm electroless Cu seed. These layers are deposited sequentially in the same system. The step coverage for each layer is $\geq 75\%$. Successful bottom-up electroplated Cu TSV fill has been demonstrated using this barrier/seed combination. [Figure 8](#) shows an FIB image of a 5 X 50 μm via filled by standard bottom-up fill chemistry in a Tokyo Electron Stratus ECD system using the electroless barrier/seed.

Electroless barrier/seed deposition is not a high-temperature process and will be suitable for via-last application. Being highly conformal, it is expected to scale successfully to higher A/Rs.

Summary

There are several candidate process flows for conformal barrier/seed processes with potential for use in the next generation of higher aspect ratio through-silicon vias. Three examples have been reviewed here with data showing their feasibility. Key requirements for adoption will be compatibility with downstream processes after filling of the TSV by ECD, compatibility with the TSV scheme, whether it be via-middle or via-last, before or after bonding and thinning of the wafer and, of course, cost. The slower than expected roll out of interposer and 3D packaging has been attributed mainly to the high cost relative to other wafer-level packaging choices. Any new process will be evaluated for cost with the goal of lowering overall cost per wafer for 3D packaging. At some point in the near future, the size, speed and power saving advantages of 3D will intersect the cost requirements of a large number of semiconductor products and 3D packaging will take off. In the meantime, developments in 3D continue to advance the technology and reduce cost. Higher aspect ratio and new conformal barrier/seed options have the potential to play an important role.

Reference

1. Keigler et al., US Patent Application US20110240481, Apr. 6, 2010.

Biographies

Stephen N. Golovato received his PhD in Electrical Engineering at the U. of Wisconsin and is Director of Process Technology at Tokyo Electron NEXX; email Stephen.Golovato@us.tel.com

Tyler Barbera received his BS in Chemical Engineering at the U. of Massachusetts-Amherst, and is a Process Engineer at Tokyo Electron NEXX.

Keiichi Fujita received his Master of Engineering in Material Science at Kyoto U. and is a Process Engineer at Tokyo Electron NEXX.

Takashi Tanaka received his MS in Chemistry at Kwansei Gakuin U. and is a Process Group Leader at Tokyo Electron Kyushu Ltd.

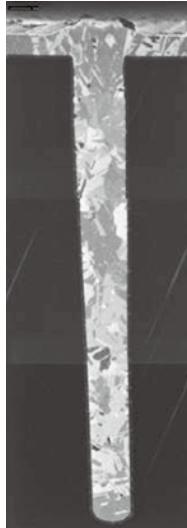
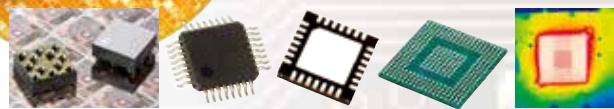


Figure 8: A 5 X 50 μm via filled directly on an electroless Cu seed.

Johnstech®



Wafer & Package Final Test



- **High Performance, Low Force Probe Array & Test Contactors**
- **Characterization, Production Floor, and Test Cell Integration Services**

Johnstech®

www.johnstech.com/connected

Find out more and win an iPad

Diamond: ultimate temperature control material for 3D ICs

By Mario M. Pelella, Jerry W. Zimmer [sp3 Diamond Technologies] and Thomas S. Tarter [Package Science Services, LLC]

Once thought to be a bridge to full 3D IC stacks, 2.5D/3D interposer technologies have emerged as a solid presence in the semiconductor industry because of such performance advantages as smaller footprint, reduced interconnect delays, lower power, and higher bandwidth. Applications targeted for 3D interposers include MEMS and sensors 3D capping, system partitioning, CMOS image sensors, 3D LED silicon substrates, and 3D integrated passive devices. Market research firm Yole Développement predicts that by 2017, 2.5D/3D interposer revenues are expected to reach 15% of the packaging substrate market value.

Finding ways to manage thermal dissipation in these 2.5D/3D interposer packages, however, is a major challenge facing technology developers. According to Yole, thermal management could well be the barrier to entry for 3D if the industry cannot figure out how to dissipate heat throughout the entire package.

Both silicon (Si) and glass are being considered as interposer material. Unfortunately, neither of these exhibits favorable thermal conductivity. Recent studies examining chemical vapor deposition (CVD) diamond films as a viable alternative to glass and Si are showing great promise because of diamond's high thermal conductivity, a coefficient of thermal expansion (CTE) that matches silicon [via a composite stack with copper (Cu)], and compatibility with existing Cu damascene processing. This article will also introduce the idea of using silicon-on-diamond (SOD) substrates as the ultimate solution for 3D interposer technologies.

Interposer material options

Current 2.5D and 3D interposer configurations rely on Si as the interposer material because of its availability on the market, the established infrastructure for Si, performance benefits and its coefficient of thermal expansion (CTE) match to active die. Particularly in high frequency applications, Si is the better performer compared to glass. The downside of Si is the cost of Si interposers themselves and the lack of Si interposer suppliers [1]. For these reasons, glass and organic interposers are both under development as alternatives. The benefit of glass is mainly cost, the ability to reach fine pitches, and the fact that it is a CTE match for the printed circuit board. However, glass has been shown to have impedance issues and is a poor thermal conductor. Additionally, the manufacturing infrastructure for glass interposers has not yet been developed, and until it is, manufacturers are unlikely to embrace glass as a viable interposer option. Organic interposers are showing progress for coarser pitch 2.5D interposers, but can't achieve the

line widths and spacing necessary for high-density through-silicon via (TSV) applications. Additionally, organic interposers don't exhibit the same CTE match as glass or Si.

One option that has been given little consideration as an interposer material is diamond. CVD diamond films offer all the advantages of Si and glass, and more. Diamond exhibits a number of unique physical properties that make it an attractive alternative to Si or glass as an interposer material. Diamond exhibits the highest known thermal conductivity; much higher than Si and glass, and 2-3x higher than Cu. Its CTE is substantially lower than that of glass and it demonstrates both chemical and biochemical inertness. Most importantly, as the hardest substance ever discovered by man, it exhibits the highest Young's Modulus; 10x that of Si. As such, it is a much easier material to handle regardless of thinness. Because it is a very rigid material, 5µm of diamond is as manageable as 50µm of Si, allowing for extremely thin stacks (**Table 1**). Diamond is compatible with

Material Property	Cu	Glass	Si	sp3 CVD Diamond
Thermal Conductivity (W/mK at 25°C)	300-398	0.9	120 -150	800 - 1400 ¹
CTE (ppm/ $^{\circ}$ C@30-200 $^{\circ}$ C)	17.8	6	4.1	1.5 - 1.8
Young's Modulus (GPa)	117	50-90	130 -185	1200

1 – sp3 measured (Graebner, Rev. Sci. Instrum., Vol. 64, No. 11, Nov. 1993, Bell Labs TC technique)

Table 1: Material property comparison of Cu, glass, Si and diamond films.

conventional CMOS process integration, so no changes need to be made to the infrastructure to accommodate diamond films into 2.5D and 3D process flows.

Traditionally, CVD diamond has been known to be a very expensive material and up until recently, it was considered too costly an alternative to Si or glass, regardless of its benefits. But in thin film applications, the cost is following the curve of integrated circuits (ICs). If the cost per cubic millimeter keeps declining as it has been, it will be economically feasible to use diamond in thermal applications for 3D ICs. Moreover, high-volume manufacturing of CVD diamond films will also drive down diamond's cost structure.

Thermal modeling analysis

For the purpose of demonstrating the differences between the thermal conductivity and dissipation capabilities of Si, glass, and CVD diamond, a basic thermal modeling analysis was performed using a simple stacked chip assembly consisting of four active-side down ICs with three interposer layers placed on a face-up ‘logic’ chip. While this configuration is not standard for 2.5D and 3D interposers, the goal is to show relative improvements in temperature and temperature distribution when replacing glass or silicon interposers with CVD diamond material.

The model contains TSV arrays in two areas in the stack with a total of three hundred fifty-two 30 μm vias represented. The basic pitch of the TSV is 100 μm . TSVs propagate from the face of the top IC (active side down) to the face of the logic IC (active side up) for a total length of 240 μm . Quarter symmetry is used in this model set. **Figure 1** shows the stack-up for Case 1. The chip sizes represented are: 1) Chip 1-4: 5 x 10mm x 50 μm thick; 2) Interposer: 5 x 10mm x 30 μm thick; 3) Logic: 6 x 11mm x 50 μm thick; and 4) Substrate: 6 x 11mm x 200 μm thick.

Two sets of data are presented. The first case study includes power dissipated in specific areas on each of the chips. The second case study keeps these power dissipation areas and adds

hot spots in three 100 μm^2 areas. Figure 1 also shows the power dissipation area (1/4 symmetry) detail for each chip. The total power dissipated in the assembly is 112W.

Thermal conductivity values for the materials in the model are shown in **Table 1**. For both cases the exposed surfaces of the model (except for symmetry planes) have a convective heat

	Diamond	Silicon	Glass
Tmax (°C)	98.38	103.6	106.5
ΔT	16.73	27.08	33.4

Table 2: Case #1 Tmax result.

	Diamond	Silicon	Glass
Tmax (°C)	98.9	107.9	115.6
ΔT	16.9	31.2	41.0

Table 3: Case #2 maximum temperature.

Semiconductor

Advanced Packaging for 3D Integration Spherolyte Copper for Through Silicon Via (TSV)

Variety of TSV structures plated with Spherolyte Cu

Bottom-up filling mechanism left: initial stage; right: final stage

2 μm x 40 μm TSVs with ruthenium seed layer plated and filled with Spherolyte TSV III

Spherolyte TSV III is the latest generation of Atotech's Through Silicon Via process. It is designed to fill a variety of different TSV dimensions for both the 2.5 and 3D TSV technology. Even the most demanding aspect ratios of 1:20 on Ru seed layers are accessible.

Bottom-up Filling Process

- Growth initializes at via bottom
- Minimal overburden and protrusion

Features and Benefits

- Void-free filling of high AR structures
- Applicable on ruthenium seed layer
- Uniform copper thickness distribution
- Homogenous grain structure
- Successful plating on a variety of feature sizes
- Lowest copper impurity level
- Low temperature copper to copper direct bonding

Atotech Headquarters
P.O. Box 21 07 80 · 10507 Berlin · Germany · www.atotech.com
Tel. +49 30-349 85-0 · Fax +49 30-349 85-777

 **ATOTECH**

transfer coefficient of $10\text{W/m}^2\text{K}$ applied. A fixed temperature of 60°C is applied to the exposed surface on the bottom of the substrate layer. The models are solved for steady-state temperature.

Case study #1. Solutions are generated for three interposer materials: CVD diamond, silicon and glass. **Table 2** shows the maximum temperature for each case 1 result. ΔT represents the maximum difference in temperature across the IC stack from the coldest point to the hottest point.

Figure 2 shows temperature contour plots for the materials with a temperature scale limited to a range of $85\text{-}100^\circ\text{C}$ for comparison. **Chart 1** is temperature plotted as a function of distance from the edge along the (long) symmetry plane.

From **Table 2**, the reduction of temperature from the worst-case shows a modest improvement due to limited heat removal directly from the exposed faces of the interposers. However, the data in **Figure 2** shows that the reduction in temperature delta across the IC stack is significant. The use of CVD diamond interposers reduces the temperature difference across the assembly by 50% compared to glass interposer material and 38% over Si.

Case study #2. Case #2 includes additional power dissipation to simulate

hot spots in the stack. Power dissipation of 0.2W is applied in each of three $10\mu\text{m} \times 10\mu\text{m}$ square areas (**Figure 3**). **Table 3** shows the maximum temperature result for the case with hot spots. ΔT represents the maximum difference in temperature across the IC stack. **Figure 4** shows cross sections at the hot spot location and temperature profiles bisecting a hot spot at the surface of chip #3.

For case #2, the benefit of CVD diamond is evident when hot spots are present. The temperature uniformity is significant with the utilization of CVD diamond films. The temperature difference (ΔT) is 59% (16.7°C) less than glass material and 46% (9°C) less than Si.

Figure 3 shows that the use of CVD diamond material for interposers almost eliminates temperature peaks from hot spots. The benefit of using high-thermal conductivity CVD diamond material is shown through reduction of maximum temperature and temperature distribution.

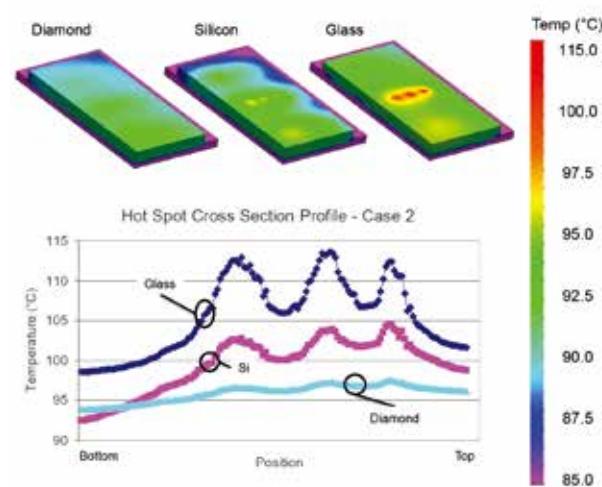


Figure 3: Case #2 temperature distribution and profile at hot spot.

Implementing CVD diamond films

There are several different ways CVD diamond can be implemented. One way is to use a solid diamond interposer with Cu vias. This provides the highest thermal conductivity but also has the highest cost and does not perfectly match the CTE of the silicon chip. A better approach is to use a diamond/Cu/diamond interposer. Diamond is very compatible with Cu. By applying a titanium tungsten adhesion layer, Cu will adhere to diamond. By selecting the correct structural configuration of Cu and diamond, one can provide a perfect CTE match to the silicon, maintain the

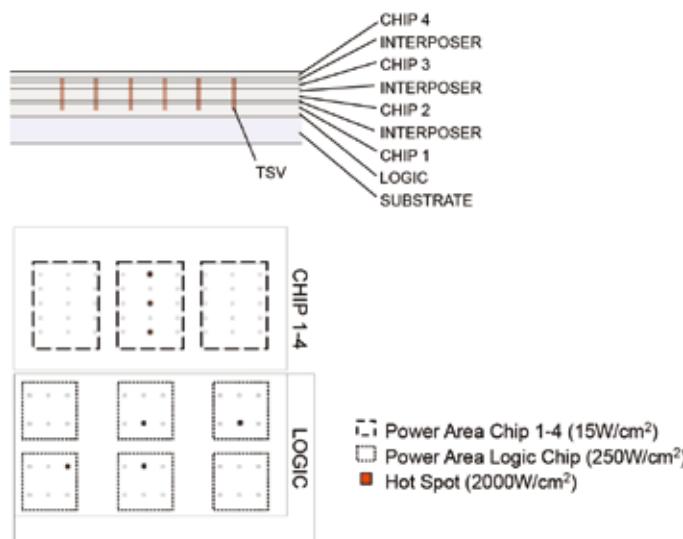


Figure 1: Model stack-up and power dissipation detail.

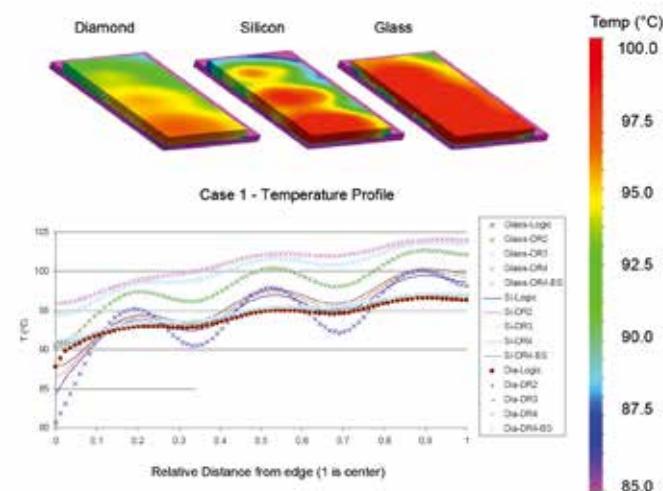


Figure 2: Case #1 temperature profiles and distribution.

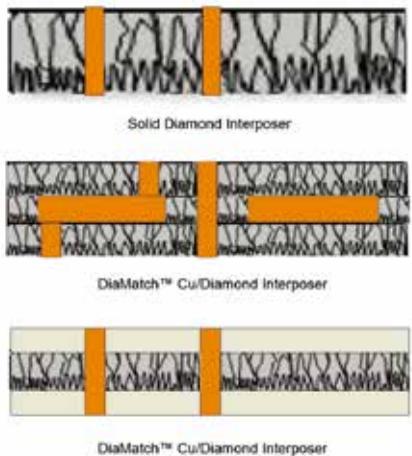


Figure 4: Methods to implement CVD diamond interposers.

stiffness advantage of diamond, reduce the overall cost relative to solid diamond and provide an RDL capability built into the interposer. A third method is to apply the CVD diamond film to thin Si to create a Si/diamond/Si interposer that would achieve compatibility with existing silicon interposers at the expense of lower thermal conductivity than pure diamond or a diamond/Cu/diamond. Laminate cross sections of these approaches are shown in **Figure 4**.

The ultimate 3D IC (**Figure 5**) would not use an interposer at all, but would build the CVD diamond film right into the substrate platform for the devices, in the same manner that silicon-on-insulator (SOI) wafers are manufactured, replacing the oxide layer with diamond to create an SOD stacked substrate. The CVD diamond layer does not need to be thick due to its high Young's modulus.

CVD diamond can be treated like any other CVD film grown on silicon.

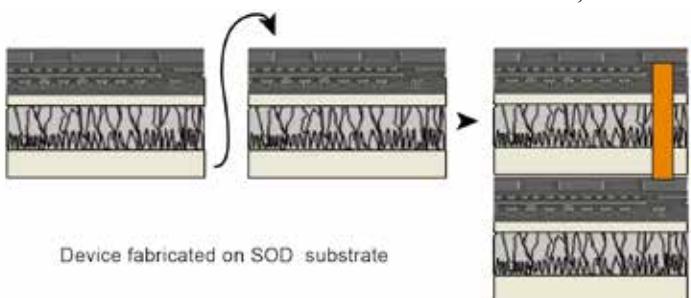


Figure 5: The ultimate 3D IC with silicon-on-diamond substrate.

It can be patterned using photoresists and hard masks, etched using oxygen RIE etching and subjected to CMP processes without fear of damage to the film. All of this can be done on standard CMOS equipment.

Summary

While 3D ICs are thought to enable heterogeneous super systems of the future, CVD diamond films can provide the ultimate solution to address the thermal management issues associated with them. Diamond/Cu/diamond, diamond/silicon/diamond, and Si/diamond/Si are potential interposer solutions. A stacked SOD substrate solution, integrating CVD diamond, provides the ultimate use of diamond films for applications without interposers. With the falling cost of CVD diamond and the increasing thermal management needs of the semiconductor industry, it's time to incorporate CVD diamond into mainstream products.

Reference

1. F. von Trapp, "The flip side of the glass interposer coin," <http://www.3dincites.com/2012/07/the-flip-side-of-the-glass-interposer-coin/>

Acknowledgements

The author relied on the following resources for experimental data:

1. C. Y. Khor, M. Zulkifly, A. Maejo, "Modeling and analysis of the effect of stacking chips with TSVs in 3D IC package encapsulation process," *Inter. Jour. of Science and Tech.*, 2012.
2. M. Ni, Q. Su, Z. Tang, J. Kawa, "An analytical study on the role of thermal TSVs in a 3D IC chip stack," *DATE 2010 Friday workshop*

on 3D Integration, <http://www.date-conference.com/conference/date10-workshop-W5>, 2010.

3. P. Ramm, "Shrinking 3D ICs – capabilities and frontiers of through-silicon via technologies," *AIDA*, <http://indico.cern.ch/getFile.py/access?contribId=39&sessionId=3&resId=0&materialId=sldes&confId=209454>, 2013.
4. P. Park, "3D integration for mixed-signal applications," white paper, <http://www.ziptronix.com/wp-content/uploads/2011/08/analog-applications1.pdf>, 2002.
5. G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S. K. Lim, R. Tummala, "Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications," *Electronic Components and Tech. Conf.*, 2011.
6. M. Fritze, P. Franzon, M. Steer, "Thermal challenges in DARPA's 3D IC portfolio," *Sematech workshop on thermal & design issues in 3D ICs*, Albany, N.Y., 2007.
7. T. K. Ku, "3D TSV stacking IC technologies, challenges and opportunities," *AMD technical forum 2011*, http://sites.amd.com/us/Documents/TFE2011_026ITR.pdf, 2011.

Biographies

Mario M. Pelella received a PhD in Electrical Engineering from the U. of Florida and his MSEE and BSEE from Clarkson U.; he is VP of Engineering at sp3 Diamond Technologies; email info@sp3inc.com

Jerry W. Zimmer has over 20 years of experience in semiconductor manufacturing in addition to over 20 years of experience in synthetic diamond deposition; he is CTO Emeritus at sp3 Diamond Technologies.

Thomas S. Tarter is a 30-year veteran in the field of electronic packaging and is President of Package Science Services LLC in Santa Clara, CA.

The future of interposers for semiconductor IC packaging

by John H. Lau [ITRI]

In this study, the future of passive interposers (2.5D IC integration) for semiconductor IC packaging will be investigated. Emphasis is placed on: 1) the real applications of interposers, 2) the recent advances of the low-cost build-up package substrates, and 3) the possibility of high-end smartphones use the interposer technology. Some recommendations will also be provided.

Real applications of interposers

More than 20 years ago, IBM in Japan invented surface laminate circuit (SLC) technology [1, 2]. This SLC technology formed the basis of today's very popular low-cost organic package substrates with build-up layers vertically connected through micro vias [3] to support solder-bumped flip chips. As mentioned in [4-8], one of the key reasons to have the intermediate substrate such as the TSV/RDL (through-silicon via/redistribution layer) interposer is created by ever increasing semiconductor IC density and pin-out, and shrinking IC pad-pitch and size; the conventional build-up

package substrate cannot support these IC requirements. A couple of examples are shown in **Figures 1** [9, 10] (Xilinx/TSMC) and **2** [11] (Xilinx/UMC/SPIIL). The sample in **Figure 1** is fabricated/assembled by a turn-key (vertically integrated) manufacturing process called CoWoS (chip-on-wafer-on-substrate) developed and operated by TSMC. Xilinx designed the structure. On the other hand, the sample in **Figure 2** is made by the collaboration of Xilinx (design), UMC (TSV/RDL interposer), and SPIIL (MEOL). MEOL stands for middle-end-of-line, which includes [12] UBM (under bump metallurgy), solder bumping, temporary bonding, backgrinding, TSV Cu revealing (grinding, silicon dry etching, low-temperature passivation deposition, chemical-mechanical polishing), thin-wafer handling, debonding, cleaning, etc.

It can be seen from **Figures 1** and **2** that even with 12 build-up layers (6-2-6) on the package substrate, it is still not enough to support the four 28nm FPGA (field-programmable gate array) chips. In addition, a TSV (10 μ m-diameter) silicon interposer (100 μ m-deep) with four top

RDLs (three Cu damascene layers and one aluminum layer) is needed. Why? As shown in **Figure 3**, in order for better device manufacturing yield (to save cost), a very large system-on-chip (SoC) has been sliced into four smaller FPGA chips made by TSMC's 28nm process technology. The 10,000+ of lateral interconnections between FPGA chips are connected mainly by the 0.4 μ m-pitch (minimum) RDLs of the interposer. The minimum thickness of the RDLs and passivation is ~1 μ m. Each FPGA has more than 50,000 micro bumps (Cu-pillar with solder cap) at 45 μ m pitch as shown in **Figures 1** and **2**, and there are more than 200,000 micro bumps on the interposer. Thus, passive TSV/RDL interposers are for extremely fine-pitch, high-I/O, high-performance, and high-density semiconductor IC applications.

On October 20, 2013 Xilinx and TSMC [13] jointly announced production release of the Virtex-7 HT family with 28nm process technology; the companies claim this is the industry's first heterogeneous 3D ICs (actually 2.5D ICs) in production. The Xilinx Virtex-7 HT FPGAs feature

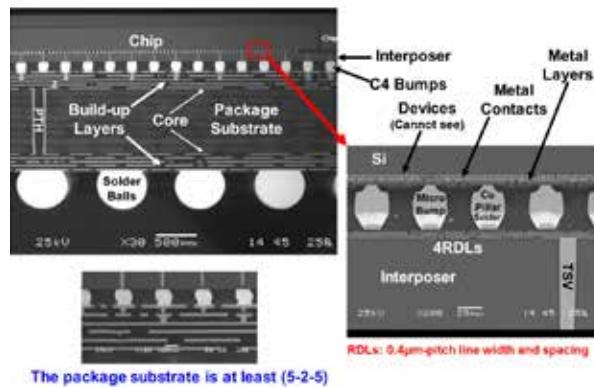


Figure 1: Four 28nm FPGA are micro Cu-pillar solder bumped on a TSV interposer with four RDLs on its topside. The interposer is C4 solder bumped on a package substrate with at least 10 (5-2-5) build-up layers [9, 10].

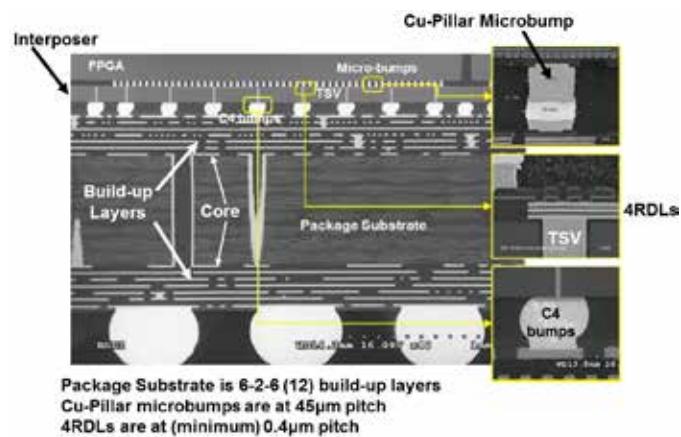


Figure 2: Four 28nm FPGA are micro Cu-pillar solder bumped on a TSV interposer with four RDLs on its topside. The interposer is C4 solder bumped on a package substrate with at least 12 (6-2-6) build-up layers [11].

BiAgX™ High Temperature Pb-Free Solder Paste Technology

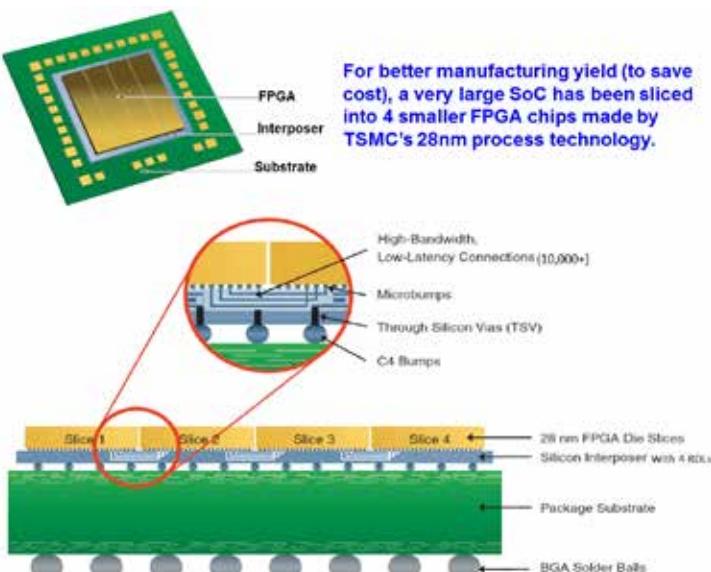


Figure 3: A very large SoC has been sliced into four smaller FPGA chips made by TSMC's 28nm process technology. The lateral communications of the chips are mainly performed by the four RDLs on top of the interposer [9].

up to sixteen 28.05Gbps and seventy-two 13.1Gbps transceivers. In addition to the Virtex-7 HT FPGAs, two other homogeneous devices in the 3D IC family have been in volume production since early 2013: Virtex-7 2000T and Virtex-7 X1140T series. On November 11, 2013 [14], however, Xilinx announced the first shipment of the semiconductor industry's first 20nm FPGA product manufactured by TSMC without a TSV/RDL interposer! One of the reasons could be the 20nm SoC FPGA was not sliced and the build-up package substrate was adequate.

In general, package substrates with 8-build-up-layer (4-2-4) and 25µm line-width and spacing are more than adequate to support most of the semiconductor IC chips. Thus, interposers are seldom needed, unless it is for very fine-pitch, high-I/O, high-density, and high-performance applications.

Recent advances of low-cost build-up package substrates

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates by increasing the number of build-up layers, shrinking the dimensions of the metal line width and spacing, and reducing the pad size and pitch. The most exciting and promising one is Shinko's thin-film RDLs on top of a build-up package substrate.

Figure 4 shows Shinko's integrated thin-film high-density organic (i-THOP) substrate [15] for high-performance applications. It is a 4+(2-2-3) test vehicle (**Figure 4** top- and middle-left), which means there is a 2-layer metal core, three build-up metal layers at the bottom (PCB) side, two build-up metal layers on the top (chip) side, and the first number "4" represents there are four thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer (**Figure 4** top- and middle-left). The thickness, line width and spacing of the Cu RDLs can be as small as 2µm (**Figure 4** bottom-left). The thin-film Cu RDLs are vertically connected



BiAgX™

- Drop-in replacement for high-Pb solder paste
- Pb-free and Sb-free
- Solidus >260°C after reflow
- MSL1 proven per IPC/JEDEC J-STD-020D



Learn more:
<http://indium.us/E036>

From One
Engineer
To Another®

www.indium.com
askus@indium.com



ASIA • CHINA • EUROPE • USA

©2014 Indium Corporation

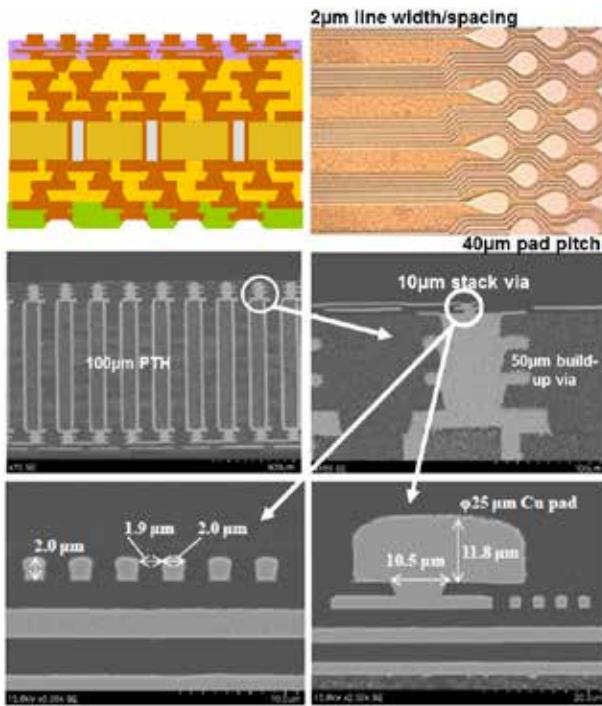


Figure 4: Shinko's thin-film RDLs on build-up package substrate test vehicle (TV). (Top-L) schematics of the 4+(2-2-3) TV. (Top-R) 2μm line width and spacing RDLs and 40μm pad pitch. (Middle-L) Cross section of the TV: 100μm plated through hole at 0.8mm thick. (Middle-R) Build-up layers are vertically connected by micro vias (~50μm) and thin-film RDLs are vertically connected by 10μm stack via. (Bottom-L) 2μm line width, spacing, and thickness RDLs. (Bottom-R) 25μm-diameter pad on 40μm pitch and the pad thickness is 10-12μm [15].

through a 10μm via as shown in **Figure 4** (middle-right). The surface Cu pad-pitch is 40μm (**Figure 4** top-right) and the Cu pad diameter is 25μm with a height of 10-12μm (**Figure 4** bottom-right).

The assembly process of the i-THOP

Then normal processes are applied to open small diameter vias and a Ti/Cu seed layer is sputtered on the resin layer. A photoresist is then spun on and exposed by a stepper to make the 2μm wiring trace (RDL) pattern. The wiring thickness is formed by electrolytic Cu plating. Finally, the Cu pads on the top layer are treated by organic solderability preservative (OSP).

Figure 5 shows the warpage measurement results of the 4+(2-2-3) i-THOP substrate (40mm x 40mm) under a temperature variation from room temperature (RT) to 260°C and then back to the RT. It can be seen that: a) for all the temperatures, the deformed shape (warpage) of the package

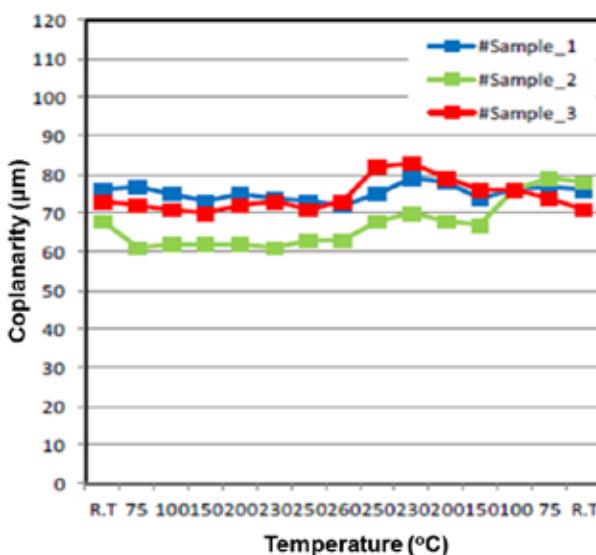


Figure 5: Warpages of the TV vs. temperatures [15].

substrate is followed. First, the conventional build-up layers are laminated on both sides of the 0.8mm-thick core (with 100μm plated through-hole) of the package substrate and the Cu metal build-up layers are formed by the normal semi-additive techniques and vertically connected through a ~50μm build-up micro via [3] (**Figure 4** middle-right). After the backside is coated with a (25μm-thick) solder mask layer for the ball grid array (BGA) solder balls, the topside surface is finished by chemical-mechanical polishing (CMP) to flatten the laser-drilled and Cu-filled vias and to smooth the surface in preparation for applying the fine-wiring insulating resin layers.

A thin-film process is used to deposit the insulating resin layers.

substrate is convex, b) when the substrate is heated to the lead-free temperature (260°C) the warpage increases to only 10μm, and, c) overall, the warpage is stable.

Qualification tests have also been conducted on the i-THOP substrate structure. These tests are: a) precondition: MSL (moisture sensitivity level) 3A and reflow (to 260°C) 3 times; b) thermal cycling (-55°C ↔ 125°C) for 1000 cycles; and c) HAST (highly accelerated stress test): 130°C/85%RH/3.5V for 150h. i-THOP substrate passed the tests and no via delamination was observed.

As a result of the data discussed above, substrate/packaging houses should follow Shinko's lead and commercialize the thin-film RDLs on top of the package substrate with CMP (to perform the planarization) and stepper (to form the 2μm or less RDL pattern) technology. It should be noted that a package substrate is a must. An interposer, however, increases cost and slows down the electrical performance. Try not to use the interposer unless the build-up package substrates are not adequate to support the very high I/O, high-performance, high-density, and fine-pitch chips. Now, with the thin-film RDLs on top of the build-up package substrate, the high-volume production of interposers will be pushed out even further.

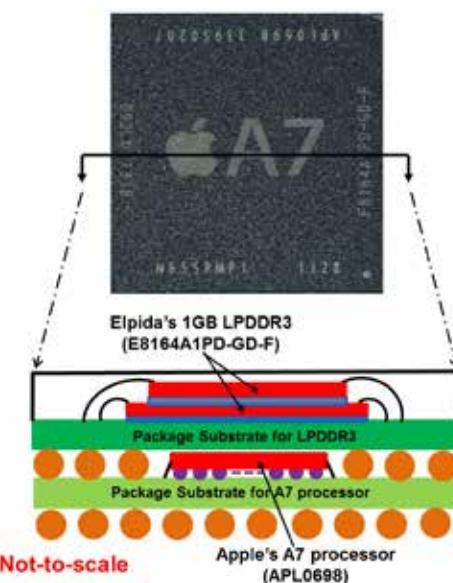


Figure 6: (Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the A7 processor/memory PoP.

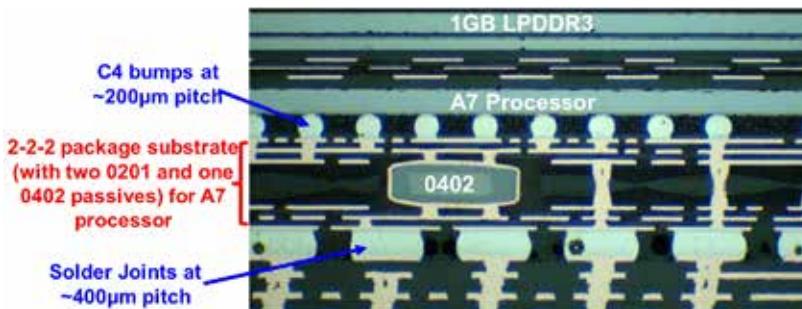


Figure 7: A typical cross section of the package substrate of the A7 processor.

these bare processor and memory chips can be placed side-by-side on a build-up package substrate. The memory chips can be either cross stacked or individually placed by wire bonding. Also, the memory chips can be placed individually by solder bumped flip chips. The memory chips can even have TSVs (perhaps for the future LPDDR4, but unlikely). A package substrate with 3-2-3 build-up and 150 μ m pad pitch should be adequate. Otherwise,

Will high-end smartphones use interposers?

One of the high-end smartphones is the iPhone 5s. **Figure 6** shows the package-on-package (PoP) inside the iPhone 5s. It can be seen from the schematic cross section that the top package is housing the Elpida (now Micron) 1GB LPDDR3 (low power double data rate type-3) mobile random access memory (RAM) chips (~11mm x 7.8mm), which are cross stacked and wire bonded on a FBGA (fine-pitch ball grid array) package substrate and then over molded. There are three rows (456) of solder balls on the FBGA. The bottom package is housing the 64-bit A7 processor chip (~10mm x 10mm), which is a solder-bumped flip chip on a build-up package substrate with 38 x 34 = 1292 solder balls. (It is interesting to note that one of the reasons why the iPad Air is the world's thinnest tablet is Apple dropped the PoP format and put the two packages side-by-side. Because of the horizontal space limitation of iPhone 5s, this, unfortunately, cannot be done.)

Figure 7 shows the cross section of the package substrate supporting the A7 processor. It is a 2-2-2 (two core layers and two build-up layers on its top side and bottom side) simple substrate with two 0201 and one 0402 embedded passives. The pad pitch for the controlled-collapse chip connection (C4) bumped A7 processor chip is ~200 μ m, and for the ball grid array solder ball, the pitch is ~400 μ m. There is no need for an additional interposer and there is plenty of room for the build-up package substrate to grow.

What if there is no PoP? Let's assume all the issues for using the bare solder bumped processor chip (from Apple's foundry) and memory chips (e.g., from Micron) have been resolved. Then, all

WinWay Technology Co., Ltd.
The Partner You Can Trust in Testing
while you are engineering the future

Test Socket for Engineering and High Volume Production

- * PoP Socket
- * Coaxial Socket
- * CIS Module Socket
- * Elastomer Socket

Probe Card for ATE Traditional and Direct Dock Wafer Testing

- * WLCSP Probe Card
- * Direct Dock Probe Card

Active Thermal Controller for Characterizing Your Product in Low and High Temperature

- * Manual ATC
- * Plunger ATC
- * Seiko Epson Handler ATC Changeover Kit

Contact Elements for Satisfying Various Test Requirements

- Spring Probe
- W-Pin

RF Measurement & Simulation

Mechanical Simulation

Thermal Simulation

We Provide Comprehensive Worldwide Support

<http://www.winwayglobal.com>
sales@winwayglobal.com

a 4-2-4 package substrate with 100 μ m pad pitch should be more than enough. An interposer is not necessary!

Summary

The future of interposer for semiconductor IC packaging has been studied. Some important results and recommendations are:

- In general, interposers are for extremely high-I/O, high-performance, high-density, and fine-pitch semiconductor IC applications. Because of its wiring capabilities, such as sub-micron metal line width and spacing, small via forming abilities (5 μ m or less via diameter), and heavy/frequent/consistent use in the semiconductor IC industry (e.g., infrastructure), a Si interposer is the choice!
- Thin-film RDLs on top of the build-up package substrate with CMP (to perform the planarization) and stepper (to form the RDL pattern) technology invented by Shinko is the right way to go. The industry should strive to commercialize it.
- A package substrate is a must. An interposer, however, is a cost adder and slows down the electrical performance. Try not to use the interposer unless the build-up package substrates are not adequate to support the very high I/O, high-performance, high-density, and fine-pitch chips. Now, with the thin-film RDLs on top of the build-up package substrate, the high-volume production of interposers will be pushed out even further.
- The build-up package substrates are more than adequate to support the semiconductor IC chips in high-end smartphones, and an interposer is not necessary.

Acknowledgements

The author would like to thank the VP and Director of Electronic and Optoelectronic Research Laboratory, Dr. C. T. Liu, for his strong support on this project, and the fruitful discussion from his colleagues at ITRI, HKUST, IME, and throughout the electronic packaging

community. Thanks also go to the Ministry of Economic Affairs (MOEA) Taiwan for its financial support.

References

1. Y. Tsukada, S. Tsuchida, Y. Mashimoto, "Surface laminar circuit packaging," Proc. of IEEE/ECTC, May 1992, pp. 22-27.
2. Y. Tsukada, S. Tsuchida, "Surface laminar circuit, a low cost high-density printed circuit board," Proc. of Surface Mount Inter. Conf., Vol. 1, Aug. 1992, pp. 537-542.
3. J. H. Lau, S. W. R Lee, *Microvias for Low Cost, High Density Interconnects*, McGraw-Hill Book Company, New York, NY, 2001.
4. C. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, T. Chai, "Nonlinear thermal stress/strain analysis of copper filled TSV (through-silicon via) and their flip-chip microbumps," Proc. of IEEE/ECTC, May 2008, pp. 1073-1081.
5. X. Zhang, T. Chai, J. H. Lau, C. Selvanayagam, K. Biswas, S. Liu, et al., "Development of through-silicon via (TSV) interposer technology for large die (21x21mm) fine-pitch Cu/low-k FCBGA package," Proc. of IEEE/ECTC, May 2009, pp. 305-312.
6. C. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, T. C. Chai, "Nonlinear thermal stress/strain analyses of copper filled TSV (through-silicon via) and their flip-chip microbumps," IEEE Trans. on Advanced Packaging, Vol. 32, No. 4, Nov. 2009, pp. 720-728.
7. J. H. Lau, Y. S. Chan, R. S. W. Lee, "3D IC integration with TSV interposers for high-performance applications," Chip Scale Review, Vol. 14, No. 5, Sept/Oct, 2010, pp. 26-29.
8. T. C. Chai, X. Zhang, J. H. Lau, C. S. Selvanayagam, D. Pinjala, Y. Hoe, et al., "Development of large die fine-pitch Cu/low-k FCBGA package with through-silicon via (TSV) interposer," IEEE Trans. on CPMT, Vol. 1, No. 5, May 2011, pp. 660-672.
9. B. Banijamali, S. Ramalingam, H. Liu, M. Kim, "Outstanding and innovative reliability study of 3D TSV interposer and fine-pitch solder micro-bumps," Proc. of IEEE/ECTC, May 2012, pp. 309-314.
10. B. Banijamali, C. Chiu, C. Hsieh, T. Lin, C. Hu, S. Hou, et al., "Reliability evaluation of a CoWoS-enabled 3D IC package," Proc. of IEEE/ECTC, May 2013, pp. 35-40.
11. W. Kwon, M. Kim, J. Chang, S. Ramalingam, L. Madden, G. Tsai, et al., "Enabling a manufacturable 3D technologies and ecosystem using 28nm FPGA with stack silicon interconnect technology," IMAPS Proc. of Inter. Symp. on Microelectronics, Oct. 2013, pp. 217-222.
12. J. H. Lau, "Supply chains for high-volume manufacturing of 3D IC integration," Chip Scale Review, Vol. 17, No. 1, Jan/Feb 2013, pp. 33-39.
13. <http://press.xilinx.com/2013-10-20-Xilinx-and-TSMC-Reach-Volume-Production-on-all-28nm-CoWoS-based-All-Programmable-3D-IC-Families>
14. <http://press.xilinx.com/2013-11-11-Xilinx-Ships-Industrys-First-20nm-All-Programmable-Product>
15. N. Shimizu, W. Kaneda, H. Arisaka, N. Koizumi, S. Sunohara, A. Rokugawa, T. Koyama, "Development of organic multi-chip package for high-performance application," IMAPS Proc. of Inter. Symp. on Microelectronics, Oct. 2013, pp. 414-419.

Biography

John H. Lau received his PhD degree from the U. of Illinois at Urbana-Champaign and is a Fellow at the Electronics and Optoelectronics Research Laboratory, Industrial Technology of Research Institute; johnlau@itri.org.tw

Packaging of integrated MEMS sensors for mobile devices

Yan Loke, Jay Esfandyari, Antonio Cirone [STMicroelectronics]

As the number of mobile device users continues to surge, mobile device manufacturers are faced with the critical challenge of how to capture their share in this lucrative market. They attempt to distinguish themselves from their competitors by adding more features and sensors into their devices. It will not be surprising when new sensors measuring pressure, humidity, alcohol content, and IR camera for night vision are included in the next wave of mobile devices. The number of applications available on this next wave of phones continues to surge, and new sensors need to be implemented to “sense” new parameters.

In order for the sensors to fit into ever smaller and thinner mobile devices, the demand for smaller package size has resulted in trends from as large as 7x5mm down to the current 2x2mm (depending on device type) while maintaining or adding more functionality. Package thickness is nominally at 1mm with further reduction in sight. Design, process, and packaging engineers have to work together to address the arduous task of the forever shrinking device size.

Design of MEMS devices

Currently, an individual MEMS sensor such as the accelerometer or gyroscope is capable of sensing three axes simultaneously. This eliminates the need for three identical sensors to be oriented in the x-y-z axes on the assembly board in order to enable the three degrees of freedom. Furthermore, these devices are designed to respond only to the parameter that they are meant to measure and are not affected by other external forces. For example, a gyroscope is designed to measure rate

of rotation and should be immune to vibration or shock. In terms of cross axis effects, a rotation in a particular axis should not affect or result in measurements in the other two axes.

The design of a MEMS device needs to also address other specifications such as on-axis sensitivity, zero level measurement (initial offset), drift of zero level and sensitivity with time and temperature. Presently, most MEMS sensors are based on either capacitive or piezoresistive principles. They detect a change in the parallel plate capacitance or a change in resistance due to an external force such as acceleration or rotation acting on a mechanical structure.

With the market pressure for smaller device size, the dimensions of the mechanical structures have to be further reduced, which inherently results in a more dense design. This in turn can affect the sensitivity of the device as the mechanical structure will now respond less, resulting in a smaller change in capacitance or resistance. This poses a challenging task for the IC engineers to design a circuit that is to be able

to detect the reduced changes with interference from noise and effects of stray capacitance.

Support structures such as wider frames and thicker substrates are important elements in a mechanical structure. This will ensure the MEMS devices are rigid and sufficiently immune to molding and the board assembly stress. However, in line with device shrinkage, these devices will have less of such essential elements, and their performance attributes such as initial offset, sensitivity and offset change with temperature, just to name a few, are affected. A simple phenomenon is that a film of a certain stress will warp a thinner substrate more than a thicker substrate, which will affect the initial gap of the mechanical structures – hence the offset. Front end processes such as film deposition, and backend processes such as the molding, will have to be redialed to take into account the thinner substrate.

Despite the challenges listed above, MEMS designers continue to shine in being able to create solutions for multi axis sensors to measure the

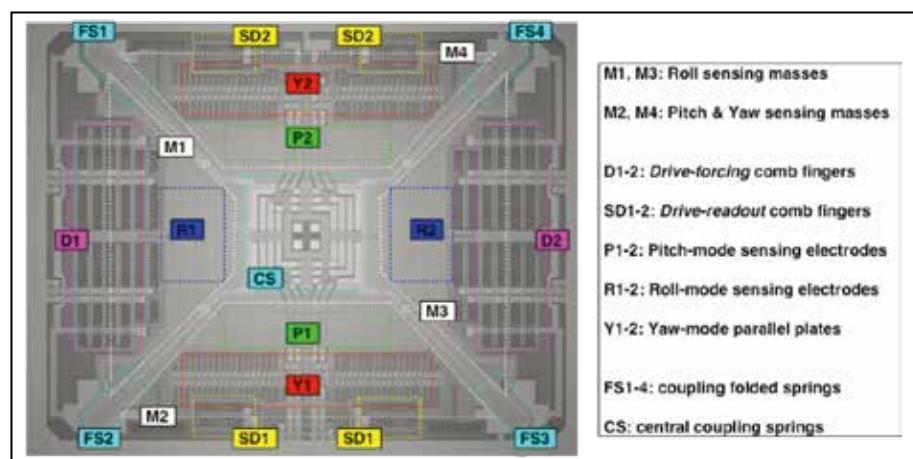


Figure 1: Single mechanical structure to detect rate of rotation in three axes.

parameter that they are designed for while remaining immune to other parameters. For example, a gyroscope design [1] with a single oscillating mass to detect rotation in multiple axes has been developed as compared to one oscillating mass for each axis (**Figure 1**). While it is designed to measure rate of rotation, it is also immune to acceleration and vibration.

MEMS and IC integration

For MEMS sensors in a high-volume industry like the mobile device market, MEMS and IC devices are fabricated on separate wafers. Although there have been trends in the MEMS technology to incorporate device integration on the same wafer, they continue to be done separately for a number of reasons. First, process integration is simpler as there are significant challenges in integrating the MEMS process in the standard integrated circuit flow ranging from process compatibility to temperature constraints. Second, high yield is imperative for these products because of volume demand and pressure to keep price down. It is easier to develop separate MEMS and IC high yielding processes as compared to fabricating them on the same substrate. Robust and scalable processes are keys to sustaining the high demand in the consumer market. Lastly, integrating MEMS devices and integrated circuits on the same substrate will require more real estate in the x-y plane as they need their own space, hence, making it more challenging to shrink the die.

Fabricating the MEMS and IC devices

separately opens up the option to be able to stack the devices vertically, hence reducing x-y dimensions and taking advantage of the available vertical space. However, it is important to note that space in the vertical direction is also limited as mobile devices are getting thinner and thinner. **Figure 2** illustrates a typical process flow from the individual wafer fabrication, testing, integration, thinning, and package assembly to final test.

The majority of the MEMS wafer suppliers are on a 200mm line. Starting thinner wafers in the 400 to 500 μm range from their nominal 725 μm thickness is not uncommon as it will reduce the amount of thinning required at the backend. A thinner wafer, however, will bow more compared to a thicker wafer for the same film stress and is more prone to breakage in the fabrication line when subjected to high temperature processes. The bow alters the overall flatness of the wafer, which in turn causes issues with the automatic wafer handlers and creates havoc for photolithography tools. Ultimately, there is a trade-off between wafer line yield and the thickness of the wafer.

Integration of the MEMS and IC devices is either done on the die or wafer level, depending on the process integration. An example of a die-level integration is shown

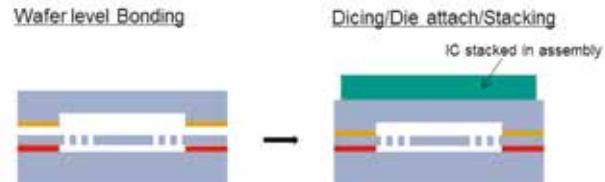


Figure 3a: a) Die-level MEMS and IC integration.

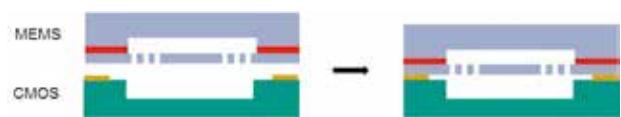


Figure 3b: b) Wafer-level MEMS and IC integration.

in **Figure 3a** where the IC chip is attached to the top of the MEMS device through conventional packaging techniques and wire bonded to make the electrical connection. Because MEMS die consist of moving parts, they must be protected from the environment by incorporating a capping wafer, which is usually done at the wafer level. In addition to protection, it also provides a hermetic environment, which is a necessity for some mechanical operations of the device.

On the wafer level, as shown in **Figure 3b**, the MEMS wafer is bonded to the IC wafer while simultaneously achieving the electrical connection between the two devices. In comparing the two approaches, the die-level approach offers the following advantages: 1) Flexibility in being able to select the appropriate IC for the application without having to do a complete redesign of the components in order that they fit together physically; 2) Scalability enables the modification of the mechanical sensing element without having to modify the IC wafer; 3) No heat dissipation from the IC that will affect the characteristics of the mechanical sensing element, which would have a significant negative impact on the performance of the device; and 4) Does not require a cavity in the IC wafer to accommodate the integration of the MEMS structure.

In either approach, wafer-level bonding is required. Low-temperature bonding techniques such as glass frit to thermo compression (Au to Au) to eutectic (Au-Si to Al-Ge) bonding come to play in assisting such integration. Depending on the process, bonding width from tens to

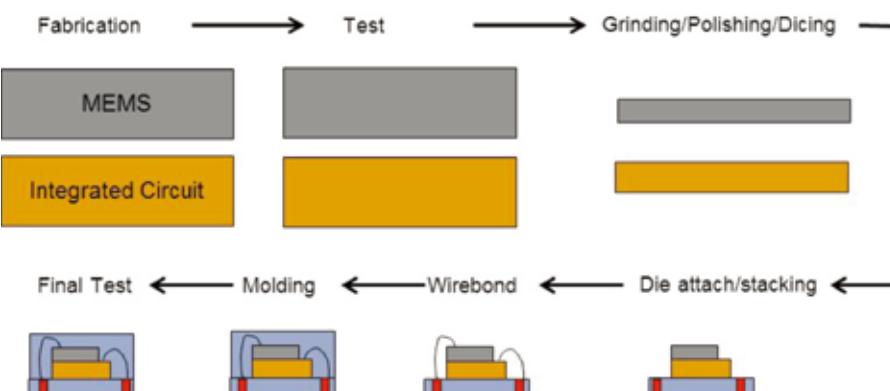


Figure 2: Typical assembly flow of a MEMS device.

hundreds of microns is required to ensure a good mechanical and hermetically sealed bond.

It is clearly evident that the bond area serves no other purpose than space for the two wafers to adhere together. As such, novel bonding techniques have been an area of interest to help reduce the required bond width and thus the overall size of the die. Shrinking a bond width from 300 μm down to 50 μm will reduce overall die size down by 0.5mm, considered a significant ratio of the overall die size.

There is always a challenge to discover new bonding techniques with minimum bond width while maintaining or achieving better than current results. One such viable technology is the room temperature bonding with surface plasma activation that does not require intermediate layers. This promising technology, which is available on a limited commercial scale, is definitely trending, and this will help reduce cost and increase throughput.

To connect to the external world, wire bonds from the MEMS device to the packaging substrate are required. As such, bond pads on the MEMS device are a current necessity, but they occupy precious space because they are located on the same plane as the MEMS structure.

A novel design [2] has been realized where the bond pads are relocated to within the wafer-to-wafer bonding frame and are accessible from the bottom of the MEMS die through the utilization of through-silicon vias (TSVs) as shown in **Figure 4**. TSV technology is instrumental

in device miniaturization and in this design, pillars of silicon that are electrically isolated from the substrate are used as conducting vias.

This approach significantly reduces the complexity of integrating TSVs into the design as incorporating either polysilicon or metal filled vias into the process will be challenging and not cost effective. This solution of using TSVs allows the relocation of the bond pads to be under the bonding frame and has helped further shrink the MEMS die by at least another 0.10 to 0.15mm.

In addition to die size reduction, the TSV will enable the use of small stud bumps to connect the MEMS with the IC, requiring minimal metal



Figure 4: Utilization of a TSV within the wafer bonding frame for electrical connection to the MEMS device.

High Speed / Low Cost Development, Test & Burn-In Sockets

Compression, SMT, & Thru-Hole PCB Mounting

Lead pitches as low as 0.4mm, up to 125,000 insertions.



Quick
On/Off Lid



Easy Screw - Lid
removed to show detail.



Easy Knob
configuration

Multi-Cavity Sockets

Significantly reduce your socket & labor costs with these multiple IC test and burn-in solutions.



Custom Test Fixtures

Fully automated or manually operated solutions to test any lead pitch & IC package

Quick Turn Low NRE



ET® **EMULATION
TECHNOLOGY, INC**

1-800-232-7837

www.emulation.com

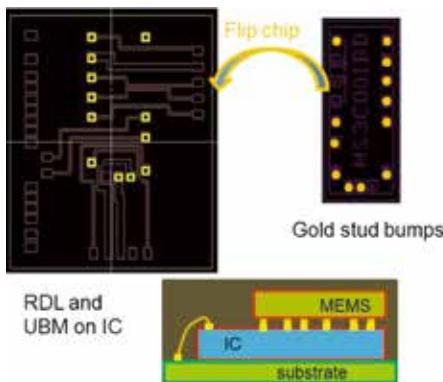


Figure 5: Utilization of TSV in a MEMS device to enable stud bumping to an IC.

connection modifications in one of the two parts. As shown in **Figure 5**, the IC is fabricated using under bump metallization (UBM) and redistribution layers (RDL) to move the connections from the boundary to the center of the device. This will not only streamline the assembly process, but also significantly reduce the length of the bonding required to electrically connect the two devices.

Assembly and packaging

As indicated before, die stacking is a norm, and it is not uncommon to find between 2 to 4 chips stacked vertically within a 1mm package. Regardless of how thin a wafer can be processed successfully through the fabrication line, further reduction in the thickness of the wafer through lapping and polishing in the backend is still required.

In a three-level stack, the typical thickness of each substrate is 0.2mm. With a 200mm diameter wafer, this results in a diameter to thickness ratio of 1000:1. This will require extremely delicate wafer handling protocols to ensure the thin wafers can survive subsequent processes such as dicing and die attach. Inappropriate wafer handling results in micro cracks and wafer warpage that are the top failure modes leading to wafer breakage during the assembly process.

The conventional technique has been to lap and polish the wafer to the required thickness before dicing. There is, however, an emerging technology whereby the process is reversed. The wafer is first pre-cut half way in the front and lapped and polished from the backside. This subsequent process simultaneously

singulates the wafer and thins the die to the required thickness, thereby eliminating the need to handle very thin and fragile wafers.

Continuous innovation has introduced the availability and implementation of new films that function both as dicing tape and die bonding material. This has helped simplify the backend process with the omission of die attach film lamination, and wafer damage caused by heat treatment during adhesion is reduced, if not eliminated.

With sensors designed to measure parameters in three axes, alignment accuracy of the MEMS die to the x, y, and z axes of the package substrate is critical. While the orthogonality between the 3 axes within a die is defined by the lithography and etch process of the wafer fabrication process, the orthogonality of the MEMS die with respect to the package is defined by the rotational alignment capability of the pick and place tool. Furthermore, the parallelism of the MEMS die with respect to the surface of the substrate will also affect the performance of the device. As the devices get smaller, the capabilities of assembly tools are being challenged.

The last major step in the backend assembly that finalizes the dimension of the device is molding. This is where the device is encapsulated in a protective environment. To reduce the overall thickness, the technique of exposed silicon has been discussed in the MEMS industry. As the name itself suggests, there is no molding material on the top surface, thus, exposing the silicon. In the absence of the top molding material, the top silicon surface works as the mechanical element of the MEMS device and acts as a protective structure as shown in **Figure 6**. Obviously, this approach is only conducive to a non-harsh working environment, which is in line with what mobile devices are designed to operate. Further steps are required to ensure that the integrity of the hermetically sealed cavity is not compromised because of permeability effects when one side of

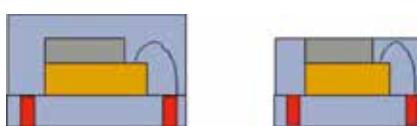


Figure 6: Concept of exposed silicon packaging.

the silicon is exposed to the environment.

It is expected that in the very near future, thickness specifications will be further reduced. The development of new materials and novelty in packaging in order to be able to achieve such specifications will be an enduring challenge.

Summary

As MEMS devices shrink with growing functionality and capability, MEMS designers, together with process and packaging engineers, have to work in unison to tackle this challenge. Decisions cannot be made in isolation – they affect all parties. The bar is continuously rising. Novelty in designs, from fabrication processes to packaging schemes, are a must in order for suppliers to stay ahead of the competitors.

Parallel to adding more functionality to MEMS sensors, the trend is to make the sensors smarter. Smart sensors incorporating dedicated microprocessors will play an important role in the Internet of Things that is on the horizon as a hub of intelligence and a gateway between different sensor nodes and the clouds.

References

1. B. Vigna, "It makes sense: how extreme analog and sensing will change the world," Hilton Head 2012 Workshop.
2. M. Ferrera, "3D integrated solution for motion MEMS," SEMICON West 2012,; http://www.semiconwest.org/sites/semiconwest.org/files/docs/Marco%20Ferrera_STMicroelectronics.pdf

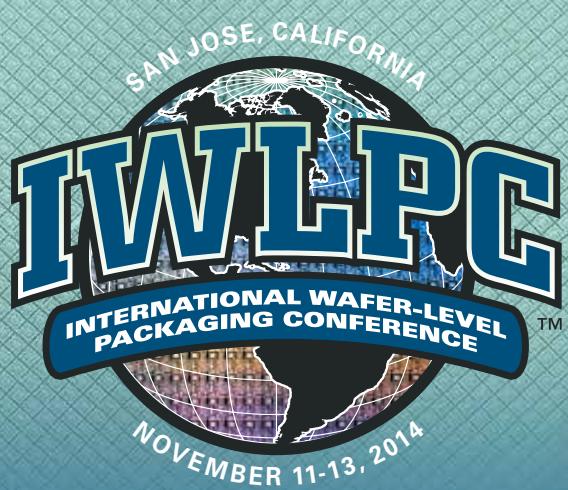
Biographies

Yan Loke received his MS degree from the U. of Alberta, Canada, and a Bachelor of Engineering from Carleton U., Canada. He is a Product Marketing Principal Engineer at STMicroelectronics; email yan.loke@st.com

Jay Esfandyari received his Masters and a PhD in Electrical Engineering from the U. of Technology of Vienna, Austria and is a MEMS Product Marketing, Senior Manager at STMicroelectronics.

Antonio Cirone received his Masters degree in Electronic Engineering at Polytechnic of Milan, Italy and is a Marketing Engineer at STMicroelectronics.

www.iwlpc.com



11th Annual International Wafer-Level Packaging Conference Exhibitor & Sponsorship Opportunities

November 11-13, 2014

DoubleTree Hotel, San Jose, California

IWLPC Conference: November 11-13

IWLPC Exhibition: November 12-13

WHAT IS THE COST TO EXHIBIT?

	Before Sept 7th	After Sept 7th
SMTA Member	\$1,150	\$1,300
Non-Member	\$1,300	\$1,450
Electricity	\$50	\$50

WHAT IS INCLUDED

- 8' x 10' or 8' x 8' booth space
- Electronic Attendee List
- Directory Listing
- Two Free Lunches Per Day
- Company Sign
- IWLPC Proceedings
- One Conference Pass

SPONSORSHIP OPPORTUNITIES

Command the attention of the IC Packaging Industry!
Several levels of Sponsorships are available:

PREMIUM SPONSORSHIP LEVELS

Platinum Sponsor (Limit 4)	\$4,800
Gold Sponsor (Limit 4)	\$3,200
Silver Sponsor (Limit 2)	\$2,000

ADDITIONAL OPPORTUNITIES

Reception Sponsor	\$5,000
Flash Drive Sponsor	\$2,500
Lanyard Sponsor	\$2,500
Tote Bag Sponsor	\$2,000
Hotel Key Card Sponsor	\$2,000
Lunch Day 1 or 2 Sponsor	\$1,500
Luggage Tag Sponsor	\$1,400
Charging Station Sponsor	\$1,200
TV Monitors Sponsor	\$1,200
Refreshment Day 1 or 2 Sponsor	\$900
Show Directory Advertising	\$200 - \$400

 **SMTA** Surface Mount Technology Association and  **Chip Scale Review** are proud to present the leading industry event for designers, users, and suppliers of 2.5D & 3D integration, flip chip, and wafer-level packaging equipment, materials, and services.

LOOKING FOR AN ALTERNATIVE SPONSORSHIP OPTION THAT YOU DON'T SEE LISTED ABOVE?

Contact one of the representatives below to create a customized sponsorship package for your company!

FOR MORE INFORMATION, PLEASE CONTACT:

Patti Coles patti@smta.org | 952-920-7682 | Questions on the Conference or Exhibition

Kim Newman knewman@chipscalereview.com | 408-429-8585 | Sponsorships and exhibits

Ron Molnar rmolnar@chipscalereview.com | 480-215-2654 | Sponsorships and exhibits

Enhanced WLCSP probe card performance at sub-300µm pitch

by Jon Diller [Smiths Connectors - IDI]

There are lots of good reasons that spring contact probes have dominated package test for decades: their high degree of compliance, maintainability, and ruggedness make them easy to use and relatively trouble-free. However, the pitch of wafer sort has generally prevented the full application of these advantages to front end test.

The growth of wafer-level chip scale packaging (WLCSP) has begun to change that. For the most part, WLCSPs have been at a spring probe-friendly 500 and 400µm pitch since their inception. The testing performed on WLCSPs is essentially a final, functional test, and package test engineers who are familiar with spring probes have often been at least partially responsible for test development. As spring probe manufacturers have begun to develop product specifically for the WLCSP market, a significant amount of effort has been devoted by many to the development of product to meet the roadmap extension of many device manufacturers below 350µm pitch.

This article attempts to consider the totality of the WLCSP probe card market, to understand why spring probes are attractive, and why such drive exists for reliable spring probes at finer pitches. It then turns to a consideration of what makes spring probes (and their interposers) challenging at those pitches. Finally, it describes a couple of ways probe card suppliers are moving those barriers, making high performance, easy-to-use probe cards a reality at near-future pitches.

WLCSP probe cards today

When WLCSPs were developed, the instinctive approach of most sort engineers was to use probe card

technologies that work for flip-chip bond pads, which present a similar-seeming array of targets. Cantilever probes, buckling beam structures, micro springs, and membrane contacts are known approaches with which these engineers were comfortable.

These contact technologies, however, exist for a fundamentally different purpose than WLCSP test, and are designed to a significantly different scale. While variations on these technologies are available that can manage a certain amount of mechanical compliance, power handling, or RF signal integrity, the performance demands of the final functional test that WLCSPs require can be quite different from wafer sort. Further, contact technologies designed to work well on 100µm pitch bond pads are much more fragile and difficult to maintain than they need to be for 400µm pitch, not-very-coplanar bumps.

By contrast, spring contact probes for 400µm pitch had already been developed and refined for small BGAs and QFNs by the time WLCSPs began to evolve, and were offered by a comfortable range of probe card and test contactor manufacturers. These probes were short enough to have bandwidths of several gigahertz, bulky enough to tolerate continuous currents as high as three amps, and significantly less expensive than the vertical probe card technologies developed for sort.

The factories that used spring probe contactors for WLCSP loved them, because they last for as much as a million cycles and are

very easily maintained when they do fail. The automatic cleaning techniques used with conventional probe cards work well with spring contact probes, especially where a homogeneous precious metal tip material is used. A manufacturer who used membrane or cantilever probe cards might have to maintain one spare for every two probe cards in active use, with cards going back (often across oceans) to their manufacturer for maintenance. By contrast, spring probe contactors can be repaired in minutes in the field; a lone spare can keep an entire line up in complete safety.

In addition to the impetus from the factory, test engineers were increasingly drawn to switch from conventional vertical probe technologies to spring contact probes by test requirements. Higher device currents exceed the limits of many buckling beam technologies. The demand for increased parallelism and signal integrity requirements have edged out cantilever cards in some applications, particularly large-scale mixed signal and system-on-chip (SoC) applications.

All of this has made spring contact probes the preferred contact technology

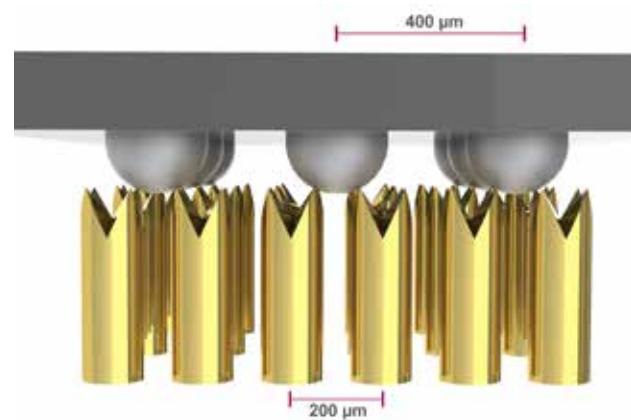


Figure 1: Kelvin contact of a WLCSP at 400µm pitch.

for many WLCSP manufacturers. However, the technical challenge of making spring probes of fine diameter that retain their advantages over other technologies has limited this in two different ways: following device pitch roadmaps, and dealing with Kelvin contact.

Chasing the roadmap

WLCSP pitch is constrained primarily by its application; if all else were equal, end users would generally prefer greater density and smaller packages. There are, however, limits on what can be successfully soldered down on the final product's PCB. Pitch packages of 350 μm were therefore until recently a rarity, and smaller packages, while talked about, were rarely in evidence. However, in this decade, WLCSPs have been fielded with features as fine as 200 μm . Manufacturers see practical requirements at 180 μm and below in their near-term requirements.

The aforementioned near-term requirements would present no issue, of course, to the extant vertical probe technologies long since developed for flip chip. However, as device pitch marches downward, expectations in terms of device speed and current handling are formed by what was possible at 400 μm . Having worked with spring probe contactors for larger devices, production test engineers are loath to give up easy, cheap, and simple spring probe solutions in the face of finer devices.

In addition to these factors, makers of power management devices are deeply interested in using Kelvin (four wire) test. Where device design for QFNs is slowly permitting test engineers to move away from Kelvin, the techniques designers rely on are unavailable in WLCSP designs. As Kelvin declines in prominence in QFNs, it is rising with respect to WLCSPs.

Kelvin test of a WLCSP requires getting two electrically isolated contacts on a bump, which, at 400 μm pitch, is 230 μm in diameter; in other words, the contacts must be on at most 200 μm pitch (Figure 1). Again, this is easy with some WLCSP technologies – but these same makers of power management devices that are driving toward Kelvin are also trying to reach higher pulse and constant currents, and the same factories that love probes for their usability are frustrated by complex

Kelvin solutions based on vertical probe technologies. Kelvin, thus, is as significant a driver toward finer pitch spring contact probes for WLCSP as is the natural pitch of the devices themselves.

So what makes it so hard?

The ‘end of roadmap’ for spring contact probes with respect to pitch has been predicted many times: first 1mm, then 0.5, and down each step

incrementally. With enough momentum from the market, spring probe manufacturers have consistently found a way to redefine what’s possible, and deliver products that remain attractive to users for their capabilities and usable in production through their robustness. To understand the limitations that resist miniaturization of spring probes, a brief review of spring probe design and terminology is in order.

SUBMIT ABSTRACT ONLINE

www.iwlpc.com

General Conference Chair:
Keith A. Cooper, SET North America

Technical Conference Chair:
Steven Xu, Qualcomm

>> Call For Papers

SMTA and **Chip Scale Review** are pleased to announce plans for the 11th Annual International Wafer-Level Packaging Conference and Tabletop Exhibition. This premier industry event explores leading-edge design, material, and process technologies being applied to Wafer-Level Packaging applications.

The **IWLPC Technical Committee** would like to invite you to submit an abstract for next year's program.

Deadline for submittal is April 18th, 2014.

Suggested Topics to Submit

WAFER LEVEL PACKAGING

- Wafer Level Chip Scale Packaging (WLCSP), Flip Chip, Fan-Out and Redistribution, Wafer and Device Cleaning, Nanotechnology, Quality, Reliability, and COO

MEMS PACKAGING

- MEMS Processes and Materials, MEMS Design Tools or Methods, Nano-MEMS and Bio-MEMS, Integration, MEMS Integration and Interconnects, RF/wireless, Sensors, Mixed Technology, Optoelectronics

3-D PACKAGE INTEGRATION

- 3D WLP, Thru Silicon Vias (TSV), Silicon Interposers, Stacking Processes (W2W, D2W, D2D), IC Packaging Substrate, Embedded Die and Passives, TSV Integration: FEOL vs BEOL

ORGANIZED BY

SMTA
Surface Mount Technology Association

Chip Scale Review

FOR MORE INFORMATION, PLEASE CONTACT:

Patti Coles patti@smta.org | 952-920-7682 | Questions on the Conference or Exhibition

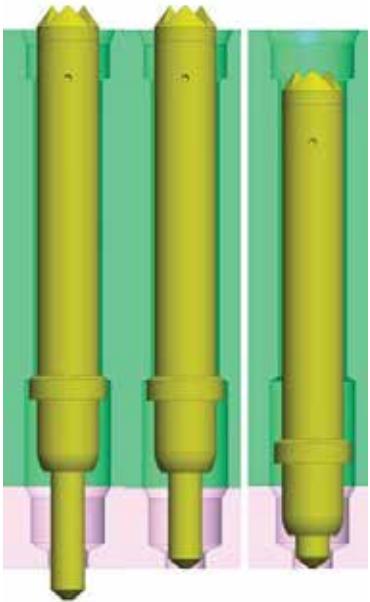


Figure 2: (Left to right) Floating spring contact probe at rest, preloaded against the probe card, and in the test condition.

A spring probe normally consists of at least one plunger, the portion that moves; a coil spring, which provides compliance; and a barrel, which holds the other two components. In some archetypes, the barrel floats in the interposer, and contacts the device under test (**Figure 2**). In others, the barrel is restrained, and a second plunger is used to comply to the bump (**Figure 3**). Current flows from the bump, to the barrel or plunger, through the barrel, and through the second plunger to an interface printed circuit board. The current does not normally flow through the spring because it is a long thin piece of wire with relatively high bulk resistance. The barrel is a much larger piece of metal, and generally has at least two orders of magnitude less resistance.

In addition to the bulk resistance of each component, the current encounters contact resistance (C_{res}) at each interface. Contact resistance at the bump is driven by oxides that coat the surface of the tin alloy; the tip must penetrate this film to make contact, and the degree to which C_{res} is mitigated at this interface is driven by how much penetration can be achieved, which in turn increases the surface area of contact between the bump and the probe. Penetration of the oxide layer is a function of the sharpness of the probe tip and the motive force of the spring, which combine to form a given

force per square area. As either sharpness or force is increased, the tip penetrates more deeply, creating a larger intersection of noble materials and lowering constriction, and thus, contact resistance.

The current next encounters C_{res} between the plunger and barrel, which is driven by force per square area as well. In the case of the plunger to barrel interface, the components of this relationship are the size of the interface between the plunger and barrel and the lateral force exerted between those two components. The plunger and barrel are each plated with a noble metal, which, in most cases, can be expected to last for the life of the probe (as limited by other failure modes, q.v.). The surfaces of the plunger and barrel each have microasperities that constrict current transfer. Lateral force – sideload – applied to the plunger either by the design of the probe, or by the application, crushes these microasperities and reduces C_{res} .

Signal integrity in non-coaxial spring contact probe structures is primarily a function of their length with respect to the wavelength of the signal, and their

characteristic impedance. At reasonable lengths (e.g., 3mm) and appropriate diameters, spring probe interposers are capable of bandwidths as high as 15GHz without special design considerations.

When diameter is reduced, several of the mechanical relationships that drive spring probe performance are compromised. Maintaining the same compliance and contact force with a smaller spring coil invites designers to increase the length of the probe, which both limits signal integrity and makes manufacture of the barrel more challenging because of increasing aspect ratios. Barrels and plungers are most commonly screw machined from nonferrous metals like beryllium copper and phosphor bronze; when driven to finer pitches, the plunger can become so small in diameter that it lacks robustness when made by common methods. The barrel becomes more difficult to plate internally, and to maintain its robustness, the wall thickness must be increased, which further constrains the diameter of the plunger. It's harder to form precise, sharp features on the tip of a smaller plunger, which can limit penetration; force is also difficult to maintain, and these two issues can significantly decrease the reliability of contact at the bump. Finally, fine parts are significantly more difficult to place in the socket without breaking, thereby limiting field maintainability.

Solutions

A proven way to address some of the mechanical compromises normally forced by tighter pitch is to omit the barrel of the probe. The probe then consists solely of two plungers and a spring, generally held together by force fit (**Figure 4**). The hole in the interposer thus takes the role of guidance and constraint that is normally filled by the barrel. With the diameter of the barrel subtracted, the spring and plunger can be made commensurately greater in circumference. This produces a more robust plunger and a more compliant, more forceful spring.

However, the other function of the barrel as a low resistance current path is

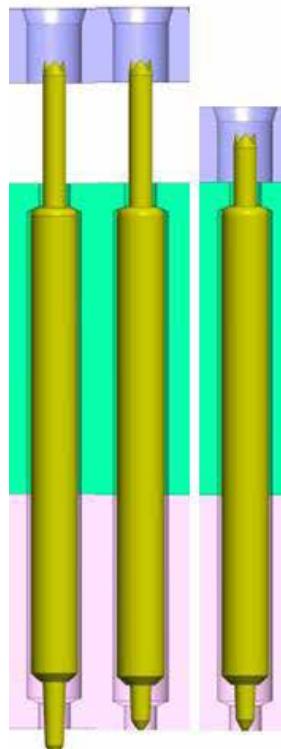


Figure 3: (Left to right) Double-plunger spring contact probe at rest, preloaded against the probe card, and in the test condition.



Figure 4: Spring contact probe without a barrel.

not filled in this design. As a result, basic resistance is high, and signal integrity can be challenged by the flow of current through a coil. This limits the application range of this approach; it is often unsuitable for power management, mixed signal, and RF devices. One solution is to use an arrangement of extensions of the plungers that pass through the spring to carry the current. This helps with resistance, but does not address signal integrity; it also significantly increases the cost of the probe. Power management devices are thereby addressed to some degree, but RF and mixed-signal application range remains an issue.

Another approach is to line the hole in the contactor body with metal (**Figure 5**). The lining can be quite thin, so the increase in plunger and spring robustness is retained as an advantage. The current flows through the lining, which addresses both basic resistance and signal integrity. The lining can also help protect the integrity of the hole when the probe is exposed to side load. This approach is able to address the full range of WLCSP applications, and has already been fielded to below 200 μm pitch.



Figure 5: Probe card with metal-lined holes taking the role of the probe barrel.

Summary

The development of robust spring probes for 200-350 μm pitch has extended the roadmap of spring contact probes in WLCSP test and has been driven by the customers for these probe cards. The market has a strong attraction to spring probes as a technology, and has expended significant energy in driving probe card

manufacturers to adapt to its changing test conditions.

Biography

Jon Diller received his Baccalaureate from the U. of Iowa and a Master's degree in Business Administration from Ottawa U. He is a Global Account Manager at Smiths Connectors - IDI; email Jon@idinet.com

Our Point Is... DL Technology Needles Work Precisely For Any Application.



DL Technology needles are designed and crafted to dispense material accurately, efficiently and to provide for better material release. Our needles are constructed in a variety of sizes, configurations, and patterns to meet your needs for any application.

EZ-FLO needles available in footed and non-footed surface mount, encapsulation, luer, and cone. Designed to provide precise, repeatable volumes. Stainless steel and ceramic needles available.

Easy Release Luer-lok dispense needles available in stainless steel and plastic. Used for applications such as epoxy, solder paste, solder mask and a variety of other materials.



Custom Needles can be designed according to unique requirements and specifications.

DL Technology has been the leader in micro dispensing technology for over 15 years. For more information, or for size or specifications on our line of needles, pumps or valves, visit www.dltechnology.com.

DL Technology

216 River Street, Haverhill, MA 01832
P: 978.374.6451 | F: 978.372.4889
sales@dltechnology.com



GUEST EDITORIAL



Bringing new electronic materials to market

By Alan Rae [NanoMaterials Innovation Center LLC]

Although our industry's products evolve very rapidly, especially in handheld consumer electronics, new materials introductions are carried out with a high level of caution – and for good reason. Seemingly "simple" materials substitutions such as the introduction of lead-free solder or halogen-free laminates have created new and challenging failure modes (and job security for process engineers!). Materials and process are always inseparable.

What is evolving most rapidly in our industry is system design and software—the challenge is when system design starts to impinge on materials properties, for example, when semiconductor nodes at 20nm and below demand copper pillars and thermocompression bonding rather than solder bumps and reflow. Environmental pressures, economics and materials scarcity can also act as triggers for a materials or process change. This evolution will bring new processes, new materials, new

challenges and new opportunities!

In terms of new materials and processes, there are two pathways to product acceptance, one fast-track, and the other more measured as described below.

Pathway 1. "Drop-in" products, for example: nano-coated stencils for fine-pitch deposition or nano fillers in underfills. This situation 1) Applies to an application that can use existing IPC and other standards and test methods; 2) A product is developed with significant cost/performance advantages; 3) A robust supply chain is put in place, often using existing trusted sales channels; 4) The product is qualified using 3rd party or consortium data wherever possible; e) Commercialization can be relatively rapid. These products can see commercialization in less than five years from launch.

Pathway 2. "Radical" products, for example graphene-based interposers. This situation includes all of the above items listed in pathway 1, plus: 1) Requires a major change to manufacturing processes and infrastructure and creation of a new supply chain; 2) Not all standards and test methods exist, needing the development of national and international standards by IPC, IEC, ISO. These products might take 10 years or more to gain market traction.

So, for a new product to gain rapid acceptance, the following considerations are important:

1. The material has to be readily processable using existing equipment and design rules;

E-tec
Interconnect

**Sockets, Contactors & Adapters
for Prototype Development & Test**

- Compatible with virtually any footprint
- Probe-pin & Elastomer solutions
- Pitch range from 0.30mm to 2.54mm
- Pin counts up to 2000
- Bandwidth to 40GHz
- SMT, thru-hole & solderless options
- Several socket closure styles available
- Custom requirements are welcome
- Competitive pricing
- Expedited delivery

For further information visit www.e-tec.com

or contact us directly for immediate attention
E-Tec Interconnect Ltd, USA Marketing & Sales
E-mail: info-US@E-tec.com, Telephone: +1 408.746.2800

- a) Rapid deployment: nano fillers in underfills; b) Slow deployment: embedded capacitors (largely because of design rule development in the early days); and c) An end run is possible when the process equipment doesn't exist, e.g., Novacentrix copper oxide ink for printed copper circuit formation linked with photonic curing equipment – but this can also add significant time to the commercialization process.
- 2. The material has to give a significant performance advantage, a significant cost advantage, or be dictated by end product evolution.
- 3. Developing the right partnerships can be critical. Many innovative small companies cannot afford to set up expensive production facilities or distribution systems in the current financial climate. They need to partner with an existing production or distribution partner and/or get funded by licensing out specific market sectors.
- 4. Qualification times can be long and arduous. Third-party verification by independent entities can be extremely valuable. Consortia data produced by organizations such as iNEMI, AREA, HDPUG, etc., are a rapid and cost-effective way to evaluate new materials and processes.
- 5. The biggest issue: there has to be a real and significant “pain point,” i.e., a compelling market need. One of the biggest barriers to the large scale deployment of printed electronics noted in the last two roadmap cycles by iNEMI roadmap writers is lack of market pull, except in displays.

Many new materials under development in the USA are

nanomaterials spinning out of projects funded by various agencies under the National Nanotechnology Initiative (NNI). The commercialization and technology transfer challenges faced by new companies spinning out of universities or government laboratories are considerable and reviewed at length in a recent National Academies Triennial Review of the NNI (available free from www.nas.edu).

Once the product is ready to go, the combination of lack of venture funding, the diversion of angel funding towards software app startups, and the current government funding sequestration means that the current climate is very new-business unfriendly. For example, SBIR (Small Business Innovation Research) grant funding is critical to small business survival in the early product development stages, but the recent U.S. Department of Defense 2013.3 solicitation published in July 2013 included less than five solicitations from the Army and Navy — and none from the Air Force.

Fortunately, the world is full of inventors and entrepreneurs (as well as inventors and intrapreneurs working in established companies) who won't take no for an answer and still find a way to make things happen. The electronics industry will depend on them to feed innovation to the larger companies that will supply the materials and processes we all need in the electronics industry. This is perhaps the most exciting time in decades in the materials industry, with new families of materials — for example graphenes and other 2D compounds — as well as new processes, such as 3D printing. Expect to see both evolutionary and revolutionary changes in the way we put together packaging!

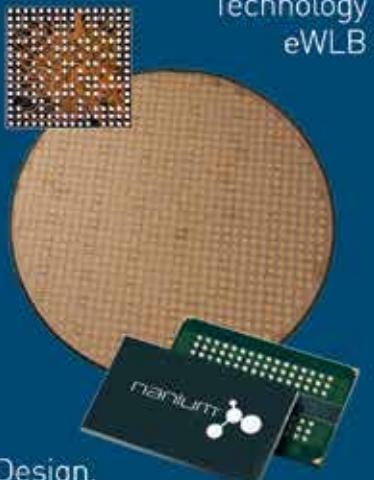
Biography

Alan Rae received his BSc from Aberdeen U. and his PhD and MBA from the U. of Newcastle Upon Tyne; he is CEO, NanoMaterials Innovation Center LLC; email arae@nanomic.org



Semiconductor Packaging, Assembly and Test

Leading Edge
Fan-out WLP
Technology
eWLB



Design,
Development,
Engineering and
Manufacturing Services



www.nanium.com

A 20GHz pluggable 0.5mm pitch BGA connector simplifies test/verification

by Ila Pal [Ironwood Electronics, Inc. USA]

IC socket industry trends are impacted by a combination of technology and market-driven factors. Technology-driven factors include miniaturization, increased pin counts, faster operating speeds, higher operating temperatures, and higher current carrying capabilities. Market-driven factors include increased durability, shorter development cycles, and the need for more cost effective solutions. For many products designed with today's high-performance integrated circuits, ball grid array (BGA) socketing systems are an essential option during the design, testing, and/or production phases of the new product development process.

An IC socket is an electromechanical device that provides a pluggable interface between an IC package and a system circuit board or subassembly. This interface must be accomplished with maximum repeatability and minimal effect on signal integrity. Providing for a removable interface is a major reason for using a socket and may be required for ease of assembly, upgradeability, maintainability, and cost savings. A cost advantage may be possible by eliminating the need to directly attach the IC to the printed circuit board (PCB). The socket is permanently (soldered) attached to the PCB, while the IC device can be inserted into or removed from the socket without disturbing the connections to the PCB. This allows the IC to function as it is soldered into the PCB, but also to be replaced by another IC or multiple ICs. Sockets also aid in the ability to test, evaluate, and inspect the complete system. In the field, a socket provides enhanced capability for maintenance, testing, replacement or upgrades, which may become a critical factor in product life cycle because of technology evolution and IC availability.

In high performance end-use product applications, the requirement for directly

attaching the device to the board is often critical. The consideration of a pluggable small footprint socket is made as an option to facilitate product replacement, upgrade, and repair in the field. The direct component replacement requirements result in the need to solder the socketing system directly to the target board. Solderability, in terms of meeting co-planarity requirements and in the prevention of solder wicking into the contact interface, is especially important. Key to success is the ability to withstand multiple reflow cycles without loss of reliable contact because of substrate warping and wicking of solder into the contacts. High-performance integrated circuits with pitches down to 0.5mm are becoming common. Because of the high density, a low insertion force (force per square area) is important criteria for usability. This paper will discuss mechanical and electrical characterization of pin and socket interconnects that are pluggable in a 0.5mm pitch array format.

Giga-snaTM BGA socketing system

The system consists of two modules. The base module has socket pins arranged in a polyimide substrate with solder tails on the backside for attaching to the target PCB. The top module has terminal pins arranged in an FR4 substrate with a round head pressed flat against the substrate. This round head acts as a PCB pad to receive the actual BGA device. The BGA device soldered onto the top module and plugged into the base module, which is soldered onto the target PCB, completes the interconnect system.

Figure 1 shows both the top and base module of the BGA socketing system. Removable interface requirements are generally stated

in terms of the insertion/extraction force and number of insertion/extraction cycles a socket can support without degradation. Insertion/extraction forces become increasingly important as the pin count in the socket increases or the pitch decreases.

Socket pin anatomy

The socket pin is a single piece integrated clip design and is made of heat-treated beryllium copper alloy 172 with 30 micro inch of gold over 100 micro inch of nickel finish. The socket pin is press-fit into the polyimide substrate directly. The adapter pin is a machined round pin and is made of brass alloy 360 with 30 micro inch of gold over 100 micro inch of

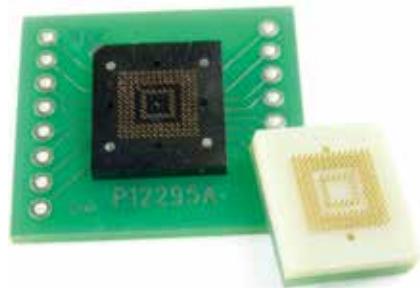


Figure 1: Giga-snaTM BGA socketing system.

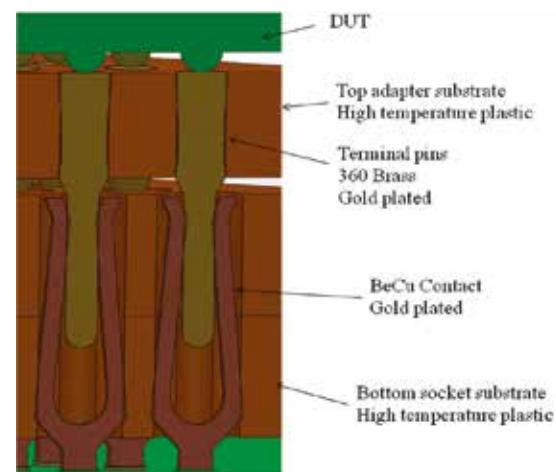


Figure 2: Socket and adapter pin cross section.

nickel finish. The adapter pin is press-fit into the FR4 substrate directly. **Figure 2** shows socket and adapter pin cross section details.

Contact force

The main function of the socket pin is to provide the required contact force for signal transmission with minimal loss. Material properties and contact geometry play a major role in determining the contact force. The contact clip has two fingers positioned in a diagonal fashion inside the drilled hole. Each finger is a cantilever beam; for a cantilever beam, the force versus deflection equation is shown below.

$$F = (D/4) E W (T/L)^3$$

Where, F = force due to deflection of the beam

D = deflection

E = elastic modulus

W = width of beam

T = thickness of beam, and

L = length of beam.

By optimizing the contact geometry and elastic modulus, appropriate contact force is provided over the full range of operation conditions. Another important material property relevant to contact force is stress relaxation. Stress relaxation causes reduction of stress in the beam under load as a function of time and temperature, thereby causing insufficient contact force over time, which results in system failure. Heat-treated beryllium copper possesses high stress relaxation resistance.

Mating mechanism

There are two phases to the mating process: initial deflection of the beam (phase 1) and sliding to the final position (phase 2) after the beams are fully deflected. Therefore, the total force per contact depends on contact force (described in the previous paragraph) and the coefficient of friction due to this sliding action. The total mating force between the two modules (top and bottom) depends on contact force, coefficient of friction, the additional force

necessary to overcome misalignment of mating halves, and dimensional variances of the substrate. It is very important to consider total mating force of mating halves as opposed to individual contact force.

Experimental setup

Figure 3 shows the experimental setup. BGA socketing modules were developed for a 153-pin BGA device (0.5mm pitch). The base module was soldered onto a daisy-chained PCB. An alternate daisychain BGA device was soldered onto the top module. Both modules were attached to the fixture set inside the Imada DPS-110R force gauge, which measures



Figure 3: Insertion/extraction test setup.

HPB-4



High-Power Burn-In with Test System

MEETING the CHALLENGE

- Individual temperature control for each device up to 600 W
- Test devices at a maximum temperature of 150°C with a liquid-cooled heat-sink per device
- Programmable clocks with leading and trailing edges per pin, one-nanosecond resolution, and 8 on-the-fly timing sets
- System capacity of 14 burn-in boards (112 devices)
- 12 vector formats per-pin per-cycle with memory testing extensions
- 128 I/O signals per board
- High-speed clock range of 2 to 400 MHz
- 64M vector memory, 8G scan
- 19 programmable voltage regulators provide 2060 amps of device current per burn-in board
- 16 high-current supplies
 - (0-3.2 Volts up to 125 Amps each)
- 3 low-current supplies
 - (0-6 Volts up to 20 Amps each)


MICRO CONTROL COMPANY





7956 Main Street NE, Minneapolis, MN 55432 • Phone: 763-786-8750 • Toll Free: 800-328-9923 • Fax: 763-786-6543 • www.microcontrol.com

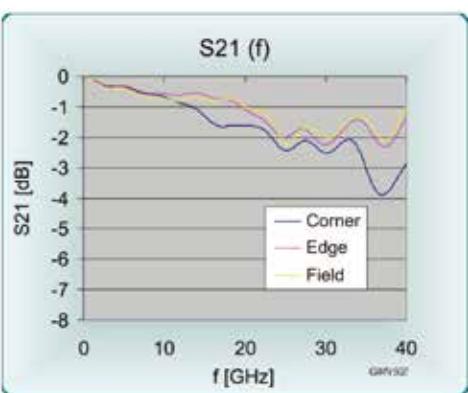


Figure 5: S-parameter data for corner, edge and field array pins.

force when the modules are inserted and extracted. A Metra HIT 30M four-lead ohmmeter was used for all resistance measurements. The resistance averaged 0.018ohms/contact.

Test results

A relationship between the insertion/extraction forces versus the number of cycles is shown in **Figure 4** for the BGA153 socketing system. From the

graph, it can be seen that insertion force for the complete 153BGA system averages 4.5 lbs and it is repeatable over 10 cycles. The extraction force for the complete 153BGA system averages 2lbs and it is repeatable over 10 cycles.

Electrical requirements are generally stated in terms of the bandwidth. Bandwidth is typically specified in terms of insertion and return loss. A vector network analyzer is used for this experiment. A signal is sent from port 1 (top of the contact) and received at port 2 (bottom of the contact). Signal reflections are measured and reported as S21 curves shown in **Figure 5**.

An insertion loss of -1dB @ 20GHz is interpreted as 90% of signal pass through the interconnect medium and only 10% of signal is lost through the interconnect transition at 20GHz. Also, it can be noticed that both edge pins and field array pins show -1dB@20GHz, and the corner pins show -1dB@13.5GHz. This data shows that in addition to contact geometry, the location of the contact pin plays a significant role in RF performance.

This is very critical for the test engineer because the specific pin functionality in the IC is being verified at a specific frequency.

Summary

A primary concern to anyone utilizing high-density devices is that the socket must provide a high-performance, low and stable value of resistance while meeting mating requirements; in particular, it must meet requirements for the mating force and the number of mating cycles it must withstand without degradation. The test results presented for the Giga-snaP™ socket system share the electrical and mechanical characteristics of the contact interface. The simple design of the socket makes it cost efficient and allows assembly to the target board using a standard reflow process. The electrical path of the BGA socket adapters is a high priority performance issue; the physical length from the top connection point on the male adapter to the solder tail on the female socket is 3mm. This is the shortest connection length by far for interconnect pin sockets, therefore providing better transmission of high-frequency signals.

Acknowledgment

The author would like to thank Vinayak Panavala for his assistance with sample preparation and testing.

Biography

Ila Pal holds an MS degree in Mechanical Engineering and an MBA degree; he is VP of Marketing at Ironwood Electronics Inc., USA; email ila@ironwoodelectronics.com

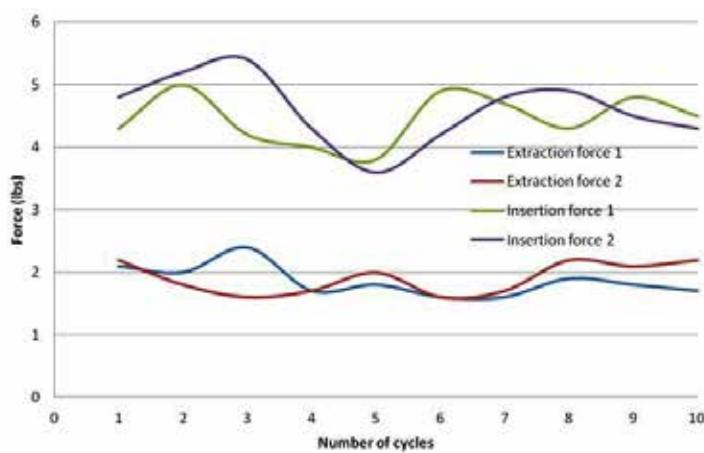


Figure 4: Insertion/extraction data.

INDUSTRY NEWS

SEMICON China 2014 - Shanghai New Exposition Convention Center March 18-20

Held at the Shanghai New Exposition Convention Center from March 18-20, SEMICON China features five theme pavilions, a host of concurrent programs, conferences, and exhibits. Last year, the conference hosted almost 57,000 attendees and exhibitors and over 2900 booths.



The Advanced Packaging Technology Forum will be held on Thursday, March 20 from 13:00-18:00 (1:00 – 6:00pm) at the Kerry Hotel in Pudong, Shanghai. The forum will discuss solutions to advanced packaging issues — including 2.5D/3D packaging, wafer level packaging, copper pillars, high-density TSV technologies — and will analyze the market trends of these technologies. This forum provides an exceptional platform for executives, engineers, researchers and other industry professionals to discuss advanced engineering and scientific information, ideas, and solutions in the industry, and offers an opportunity to reach customers from the local China IC industry.

Topics include:

- Market Analysis of Advanced Packaging
- Approaches Overview of Advanced Packaging Technologies
- New Materials in Advanced Packaging Integration
- Testing of Advanced Packaging Integration
- Modeling of Advanced Packaging Integration
- Roadmap Discussion of Advanced

Packaging in China

- Challenges of Advanced Packaging Development in China
- EDA Tools Support for Advanced Packaging
- Panel Discussion

The “More than Moore” Technology Forum is Wednesday, March 19, from 8:00am-12:30pm. This session covers Advanced Packaging Technologies and RF/mmWave Technologies; CMOS Image Sensors; High voltage, High

FAST & ACCURATE

Accurate Dual Valve Dispensing

Self-Actuating Tilt Jetting

Nordson ASYMTEK's Spectrum™ II

high-speed, high-accuracy dispensing platform sets a new standard for precision dispensing applications in microelectronics & semiconductor manufacturing and MEMS & LED assembly. Jet small dots and thin lines into tight spaces with Tilt Jetting and Precision Z-gap Control. Maximize productivity with Dual Valve Dispensing while saving manufacturing floor space with Spectrum II's small footprint.

 www.NordsonASYMTEK.com/highaccuracy
Watch the Video or contact us at
info@nordsonasymtek.com

See Nordson ASYMTEK
at SEMICON China
booth #3239





Power, LED; 2.5D/3D and 3D-IC topics; IP issues; and EDA Tools.

SEMICON China theme pavilions include: LEDs, MEMS, Secondary Equipment Applications, Service and Fab Productivity Solutions, TSV, and Smart Life. All attendees are invited to the opening keynote event, moderated by Allen Lu, president SEMI China, and Jay Chen, president and COO of Tokyo

Electron (Shanghai) Ltd.

To register or get more information, visit www.semiconchina.org or contact:

SEMI China
Tel: 86.21.6027.8500
Email: semichina@semi.org

Besi and imec Collaborate on Thermocompression Technology for High-Accuracy Narrow-Pitch Bonding of 3D ICs

Grenoble, France at the SEMI European 3D TSV Summit, world-leading nanoelectronics research center imec and Besi, a global equipment supplier for the semiconductor and electronics industries, announced they are joining forces to develop a thermocompression bonding solution for narrow-pitch die-to-die and die-

to-wafer bonding with high accuracy and high throughput. Through this collaboration, imec and Besi will pave the way to industrial adoption of thermocompression bonding for 3D IC manufacturing.

3D IC technology, stacking multiple dies into a single device, aims to increase the functionality and performance of next-generation integrated circuits while reducing footprint and power consumption. It is a key technology to enable the next generation of portable electronics, such as smartphones and tablets, which require smaller ICs that consume less power.

One of the key challenges to making 3D IC manufacturing a reality is the development of high-throughput automated process flow for narrow-

Join your colleagues at the World's Premier Event for What's **NOW & NEXT** in Burn-in & Test of Packaged ICs

Register Online at BITSWORKSHOP.ORG

©2014 BITS WORKSHOP LLC PHOTO: Bee-Creative/iStock

Fifteenth Anniversary

BITS
Burn-in & Test Strategies Workshop

March 9–12, 2014
Mesa, Arizona

Technical Program
EXPO 2014
Social Events

Sign up now for EXPO & SPONSORSHIPS

Chip Scale

pitch, high-accuracy die-to-die and die-to-wafer bonding. Flip chip and reflow soldering, which are currently combined for bonding, require lenient bonding accuracy on large bump pitches (around 150-50 µm bump pitch). Bump pitches need to further scale down to 40-10 µm to realize a sufficiently high performance. This needs high accuracy in bonding within the range of 1-2um @3sigma. Moreover, an automatic process flow is essential for industrial adoption. Thermocompression bonding is a method that enables this high bonding accuracy on narrow bump pitches, although with this comes long cycle times due to temperature and pressure profiles and processing methods which hinder industrial adoption of this technology up to now.

imec and Besi will conduct joint research to develop a high-throughput thermocompression bonder in an automated process flow, with high accuracy and shorter cycle times, paving the way to enabling a manufacturable 3D, 2.5D and 2.5D/3D hybrid technology.

"We are excited to work with a key research center such as imec and leverage its expertise in fine pitch bonding materials and processes to increase the yield and reliability of our equipment," said Richard Blickman, CEO at Besi. "This collaboration will enable us to benchmark our Chameo tool to meet the industrial needs of the semiconductor industry, offering our customers a viable and effective solution for 2.5D/3D IC manufacturing."



Celebrando BiTS - 15 Anos!

The BiTS Workshop is pleased to announce the advance program for the 2014 conference, which takes

place March 9-12, 2014, in Mesa, AZ. This year, BiTS celebrates its 15th anniversary, and plans are in place for a big celebratory splash.

Fred Taber, BiTS general chair, attributes the conference's 15 years of success to the quality technical programs put together by a dedicated committee of volunteers who endeavor to make every BiTS experience unique. Year after year, the conference features leading edge technology presentations, interesting and engaging guest speakers, feature segments, a top notch EXPO, and a healthy dose of networking. This year's lineup of what's NOW and NEXT in burn-in and test of packaged ICs promises to deliver all of the above and more.

Building on last year's Talking Points topic, 'Interconnectology,'

BiTS has invited Simon McElrea, president of Invensas Corporation, a wholly owned subsidiary of Tessera Technology, to deliver the keynote address. Invensas has branded itself as "The Interconnectology Company" to help foster the idea that the future of computing lies in an interconnected supply chain and interconnect technologies as a value-add to the end product. This concept resonated with the BiTS community last year, so Simon was asked to provide the back-story and big picture of how the concept of Interconnectology will enable the future of computing.

Prismark Partners' Brandon Prior returns as the distinguished speaker. He'll provide an overview of the global packaging market, with a focus on emerging and fast-growth package solutions.

This year's Tutorial and Tech Talk

KYEC
Your Strategic Partner for Testing MEMS and CMOS Imaging Sensors
www.kyec.com

- HQ in Taiwan & Worldwide Offices, covering USA, Japan, Europe, China and Singapore
- Over 2000 sets of test systems and growing
- Professional testing services, covering Wafer probe, Final test, Pre-Assembly, Burn-in, Back-end
- Complete testing Solutions and equipment , such as Memory, Logic, SOC, RF, CIS, MEMS

Address: 101 Metro Dr. #540 San Jose, CA 95110 Tel: 1-408-452-7680 Fax: 1-408-452-7689

sessions have been designed to fit hand-in-glove. Peter Ehlig, a Texas Instruments Fellow teaches this year's tutorial. In "Test 101: A Holistic View of Test," Ehlig looks at test from the

perspective of all its stakeholders, and will lead a discussion on how test works or doesn't work. The tutorial dovetails with this year's TechTalk, led by Jeffrey L. Roehr of Texas

Instruments. Roehr will address "The Most Common Mistakes in Test" made by product and test engineers during test program development, characterization, and limit setting, and how to avoid them.

Determined not to take things too seriously, BiTS always tries to deliver information with a twist. Last year, it was under the guise of a 'talk show.' This year, two leading socket companies have been invited to participate in the ultimate workshop game show. "BiTS Feud" pits the two companies head-to-head in a face-off about who knows the most about packaging trends, as determined by the BiTS Workshop membership. This one will be sure to keep you on the edge of your seats!

All of this, plus seven technical sessions, two poster sessions, socket market updates, lots of new products to check out in the EXPO, and the highlight of the week, Celebrando BiTS - 15 Anos!, will be sure to keep attendees busy. This year's party will be a fiesta like no other, complete with authentic Mexican cuisine, frosty margaritas and cerveza, sombreros, and a Mariachi band.

For more information on BiTS 2014, including the full agenda, exhibiting, sponsorships, attendee registration, and hotel information, visit www.bitsworkshop.org

Texas Instruments acquires UTAC facility in Chengdu, China

CHENGDU, CHINA – As a follow-on to plans announced earlier this year, Texas Instruments Incorporated (TI) (NASDAQ: TXN) today announced it has acquired a building in the Chengdu Hi-Tech Zone from UTAC Chengdu Ltd. Earlier this year, TI announced its investments in these operations could total up to

For Any PCB - GHz Bandwidth BGA/QFN Sockets

Quick-Turn Custom Sockets

- Use on any existing PCBs
- No mounting holes
- No soldering
- Patented placement/epoxy system
- 0.32mm larger than IC (per side)
- Bandwidth to 40 GHz
- 0.3mm pitch & up



Ironwood
ELECTRONICS

1-800-404-0204

www.ironwoodelectronics.com

\$1.69 billion over the next 15 years, further demonstrating its long-term investment strategy in this important region.

The new 358,000 square-foot facility will become TI's seventh assembly/test (A/T) operation. Located on the same property as TI's existing wafer fab in Chengdu, the site will become the company's only end-to-end wafer fabrication and A/T facility.

"TI's operations in China play a significant role in supporting TI's customers, today and well into the future, and we're excited to build the company's only fully integrated fab and A/T facility in Chengdu," said Kevin Ritchie, senior vice president of TI's Technology & Manufacturing Group. "The addition of this back-end capacity further enhances TI's global manufacturing footprint, enabling us to better ensure continuity of supply to our customers and support their growth."

TI will immediately begin updating and equipping the facility while simultaneously running a small production line in the new building. In accordance with TI's commitment to preserving the environment across its global footprint of manufacturing operations, reducing water, energy and waste will be given priority consideration as the building is refurbished. TI plans for the A/T site to be equipped and in production in 4Q 2014.

This investment plan does not change TI's 2013 capital spending forecast. The company continues to expect its capital spending levels to remain about 4 percent of revenue until revenue exceeds \$18 billion and should then range between 4 to 7 percent of revenue over the long term.

TI has served a broad array of

customers in China for more than 27 years and has established 18 offices for sales and applications support, in addition to its wafer fabrication plant in Chengdu and its product distribution center in Shanghai.

TI has manufacturing operations throughout the world, including the United States, Mexico, Germany, Scotland, China, Malaysia, Japan, Taiwan and the Philippines.

Save the Date Device Packaging 2014!



10th International Conference and Exhibition on Device Packaging

**Radisson Fort McDowell Resort and Casino
Scottsdale/Fountain Hills, Arizona - USA**

March 10 - 13, 2014

**Conference Details On-Line at:
www.imaps.org/devicepackaging**

Featuring Topical Workshop Tracks:

- Advanced 3D Packaging;
- Flip Chip and Wafer Level Packaging; and
- *Packaging Innovations & System Challenges for: Microsystems & Devices; Photonics Packaging*

Device Packaging Exhibit and Technology Show

Device Packaging Professional Development Courses (PDCs)

**Conference and
Technical Workshops
March 11-13, 2014**

**Exhibition and
Technology Showcase
March 11-12, 2014**

**Professional
Development Courses
March 10, 2014**

**GBC Spring
Conference
March 9-10, 2014**

Sponsored by IMAPS
International Microelectronics Assembly and Packaging Society
Bringing Together the Entire Microelectronics Supply Chain!

**Please contact Brian Schieman by email at
bschieman@imaps.org or by phone at 412-368-1621
if you have questions about the technical program, exhibits, golf or PDCs.**

The only event
that encompasses
the diverse world
of integrated
systems packaging!



May 27-30, 2014

The Walt Disney World
Swan & Dolphin Resort
Lake Buena Vista
Florida, USA

For more
information, visit:
www.ectc.net

Don't miss out on the industry's premier event!

ECTC 2014

The 64th Electronic Components
and Technology Conference

MORE THAN 300 TECHNICAL PAPERS COVERING:

- 3D/TSV
- Advanced Packaging
- Modeling & Simulation
- Optoelectronics
- Interconnections
- Materials & Processing
- Applied Reliability
- Assembly & Manufacturing Technology
- Electronic Components & RF
- Emerging Technologies

Conference Sponsors:



HIGHLIGHTS

- 41 Technical Sessions including:
 - 5 Interactive Presentation Sessions, including one featuring student presenters
- 18 CEU-approved Professional Development Courses
- Technology Corner Exhibits, featuring more than 95 industry-leading vendors
- 5 Special Invited Sessions
- Several evening receptions
- Wednesday luncheon keynote speaker
 - Peter L. Bocko, CTO, Corning Glass Technologies
- Multiple opportunities for networking
- Great location

ADVERTISER INDEX

Amkor	www.amkor.com	1
Aries Electronics	www.arieselec.com	21
Atotech	www.atotech.com	29
BiTS	www.bitsworkshop.org	52
Cascade Microtech	www.cascademicotech.com	25
DL Technology	www.dltechnology.com	45
ECTC	ectc.net	56
Emulation Technology	www.emulation.com	39
E-tec Interconnect	www.e-tec.com	46
EV Group	www.evgroup.com	IFC
GPD Global	www.gpd-global.com	11
Hanmi Semiconductor	www.hanmisemi.com	9
Honeywell	www.honeywell-radio.com	17
IMAPS DPC	maps.org/devicepackaging	55
Indium Corporation	www.indium.com	33
Ironwood Electronics	www.ironwoodelectronics.com	54
IWLPC	www.iwlpc.com	41, 43
JF Microtechnology	www.jftech.com.my	15
Johnstech	www.johnstech.com/connected	27
KYEC	www.kyec.com	53
Leeno	www.leeno.com	2
Loomis Industries	www.loomisinc.com	7
Micro Control	www.microcontrol.com	49
Nanium	www.nanium.com	47
Nordson Asymtek	www.nordsonasymtek.com/highaccuracy	51
Plasma Etch	www.plasmaetch.com	50
Plastronics	www.plastronics.com	4
Sensata	www.qinex.com	OBC
Smiths Connectors IDI	www.idinet.com	IBC
SSP Inc	www.sspinc.co.kr	23
TEL	www.tel.com	13
Winway Technology	www.winwayglobal.com	35

ADVERTISING SALES

USA West, USA-North Central

Kim Newman

P.O. Box 9522 San Jose, CA 95157-0522
T: 408.429.8585 F: 408.429.8605
ads@chipscalereview.com

USA-East, USA-South Central

Ron Molnar

13801 S. 32nd Place Phoenix, AZ 85044
T: 480.215.2654 F: 480.496.9451
rmolnar@chipscalereview.com

International

Lawrence Michaels

2259 Putter Court
Brentwood, CA 94513
T: 408.800.9243 F: 408.429.8605
lxm@chipscalereview.com

Korea

Young J. Baek

407 Jinyang Sangga, 120-3 Chungmuro 4 ga
Chung-ku, Seoul, Korea 100-863
T: +82.2.2273.4818
ymedia@chol.com



Introducing Our Advanced

QFN TEST SOLUTIONS

The leading provider of high performance test sockets has expanded its offering to include two new QFN testing solutions. Archimedes for peripheral test and the patented Celsius for tri-temp peripheral package test are both examples of what you have come to expect from Smiths Connectors | IDI, great value and leading edge technology. By combining proven scrubbing contact technology with our global manufacturing and distribution capabilities, testing QFN devices is now more affordable than ever.

Our renowned quality and reliability make Smiths Connectors | IDI your worldwide partner for the next generation of test solutions.

40+ years of perfect pitch.



And now, the perfect name



Qinex [kuh-nekts] 1. Over 40 years of reliable burn-in and custom connections; 2. Quality interconnects for **nex**-gen solutions.

Introducing Qinex, the new brand name for superior interconnection solutions from Sensata Technologies. Qinex, the new word in perfect pitch.

QUALITY. High-value interconnection solutions since 1970.

- 24/7 global engineering
- 24/7 global support teams
- Local engineering and sales
- Six Sigma quality management
- Proven, reliable high-volume manufacturing
- Expert molding, design, and customization

INNOVATION. More I/O choices, smaller form factors, superior performance in less time.

- Latest 3D design tools
- On-site model shops
- Rapid prototyping
- Advanced thermal analysis
- Design on demand
- Broad range of innovative contact designs



PARTNERSHIP. In a fierce global market, only Qinex reliably supports the innovation, reputation and competitiveness of your business. We'll work with you to get it right, the first time.

**40+ years of perfect pitch.
And now, the perfect name.**

WEB www.qinex.com

EMAIL qinex@sensata.com

CALL 1-508-236-1306

