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The Future of Semiconductor Packaging

Volume 19, Number 6

November • December 2015

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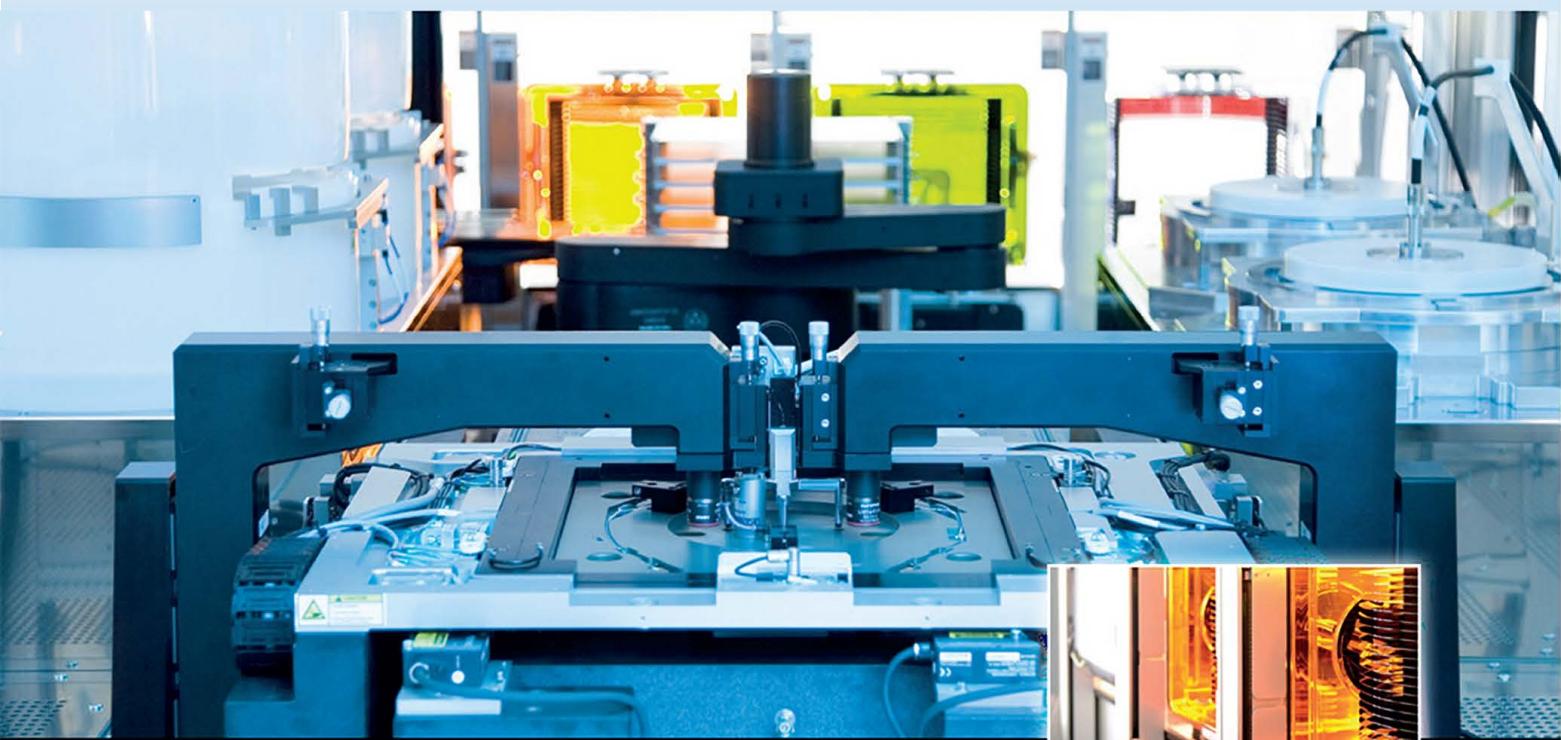
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Chip-to-wafer stacking enabled by 3D integration has significant potential to improve device performance while reducing power consumption. There are many possibilities for collaboration between foundries and OSATs, specifically with ultra-precise stacking ($<1\mu\text{m}$). Leti's roadmap calls for developing fine pitch, from classical thermocompression stacking with copper pillar, to ultra-dense bonding using Cu-Cu technology. Ultra-precise C2W is a promising possibility for the next generation of 3D-ICs. Photo courtesy of CEA-Leti

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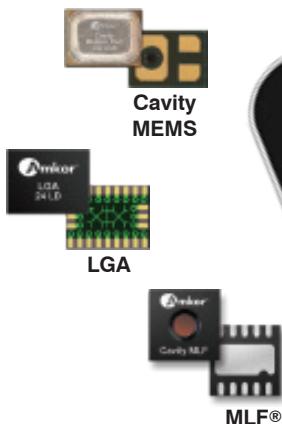
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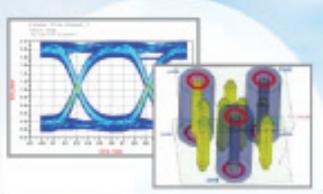
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The (r)evolution of wafer-level packages

By Andrej Ivankovic [Yole Développement]

The latest events in the technology market indicate that 2015 marks the beginning of an exciting new era for the IT and electronics industries. At the semiconductor supply chain level, the industry entered a profound consolidation phase with high M&A activity reshaping the business landscape. As the smartphone market matures, new forces are appearing in the form of the Internet of Things (IoT). While the mobile sector continues to drive the market, the scent of IoT is already spreading in the consumer sector with products such as wearables and the first smart home appliances. IoT market, application and technology segmentation has begun. Companies across the industry are restructuring, merging and acquiring in order to adjust their portfolios, enable a complete platform offer, and establish leading positions in the market.

At the level of technology, as profitability of front-end-of-line (FEOL) scaling options remains uncertain and IoT promises application diversification, the spotlight is now turning to advanced packages for: 1) Cost reduction, 2) Performance boost, and 3) Functional integration. In order to answer market demands, the advanced packaging segment focuses on integration and wafer-level packages (WLP).

Fan-in vs. fan-out: complementary or competing?

According to Yole Développement (Yole) estimates, advanced packaging services revenue will increase by US\$11.5 billion from 2014 to 2020 at a CAGR of 8%, in majority due to high-volume adoption of fan-out WLP, 2.5D/3D and evolution and growth of fan-in WLP and flip chip [1,2]. Compared to substrate-based flip-chip packages, wafer-level packages excel in cost and form, as illustrated in **Figure 1**. Their unmatched

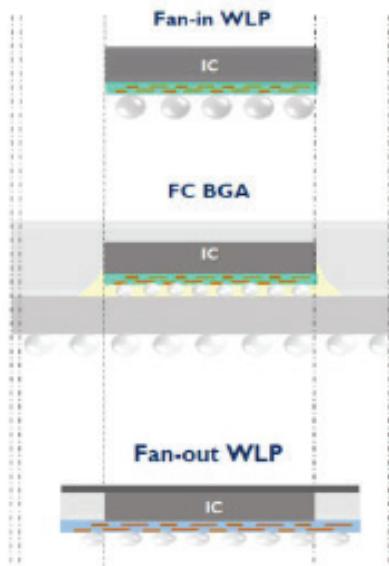


Figure 1: Comparative size illustration of fan-in WLP, fan-out WLP, and flip-chip BGA packages. SOURCE: [6]

appeal lies in the capability of assembling small to medium pin count ICs in the smallest possible footprint and thickness (substrate-less packages) at low cost. In addition, shorter interconnect paths lead to an overall boost in electrical performance.

Fan-in and fan-out WLP act as complementary, rather than competing, technologies. When bump count, size and pitch requirements exceed the available fan-in surface under the Si die, fan-out acts as a natural extension. While the current package size sweet spot for fan-in WLP lies up to $7 \times 7\text{mm}^2$, the fan-out package sweet spot is found at up to $12 \times 12\text{mm}^2$. Technologies such as sub- $10\mu\text{m}/10\mu\text{m}$ L/S (line width/space) and bump pitches as low as $0.35\mu\text{m}$ can already be found in both package types, with total package thicknesses reaching $600\mu\text{m}$ and below. While scaling of these package parameters continues, package sizes and pin counts keep increasing. When it comes to single dies, a clear quantitative line between fan-in and fan-out cannot be drawn,

because the final packaging technology chosen is product requirement dependent. Furthermore, the applications of fan-in packages are extended beyond the typical 200 I/Os. TSMC announced its plans to increase pin count capability up to 800 I/Os within a year and this year, NANUM S.A. introduced the largest fan-in package on the market: a $25 \times 23\text{mm}^2$ package incorporating 1188 balls and utilizing $700\mu\text{m}$ bump pitch.

While fan-out single-die packages will fundamentally always have the capability of incorporating several tens to hundreds of pins more than fan-in, it has other significant advantages that it can bring to a package: higher board reliability, lower thermal resistance, backside protection, and the potential for increased integration of multiple dies, system-in-package, and 3D integration.

Market penetration

Smartphones are by far the leading WLP market. More than 90% of fan-in and fan-out wafer-level packages are estimated to be in cell phones and tablets. Recent teardowns by Yole and its sister company, System Plus Consulting, of three high-end smartphones indicated a high penetration rate of WLP, 30% on average [3-5]. **Figure 2** illustrates current WLP penetration in smartphones by IC device type, with WLP illustrated in shades of red and orange.



Figure 2: Current WLP penetration in smartphones by IC device type (WLP in red and orange). SOURCE: [6]

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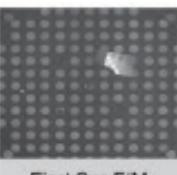
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Wafer Ejector Pin Marker Inspection



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ACCURACY	X-Y PLACEMENT	5µm @ 3σ / 6µm @ 3σ	10µm @ 3σ
	CHIP ROTATION	±0.05 °@ 3σ	
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)	
FOOTPRINT	DIMENSION(Wx Dx H)	1,600mm x 1,230mm x 1,600mm	
	WEIGHT	2,600 kg	



Figure 3: Fan-out WLP revenue forecast following Apple/TSMC entry with inFO technology. SOURCE: [6]

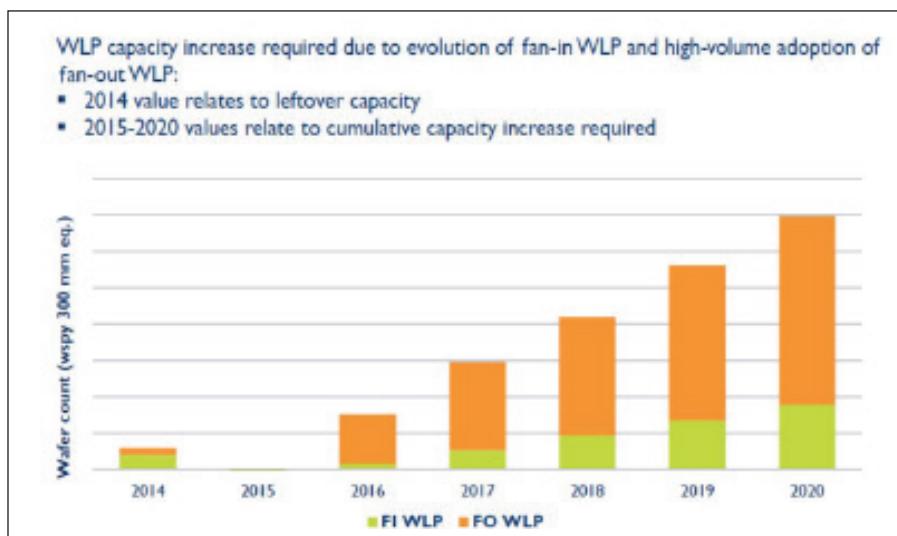


Figure 4: Leftover capacity in 2014 and required capacity increase forecast: WLP capacity increase required due to evolution of fan-in WLP and high-volume adoption of fan-out WLP. The 2014 value relates to leftover capacity, and 2015-2020 values relate to the cumulative capacity increase required. SOURCE: [6]

The fan-in WLP is a mature market estimated to cross the US\$3 billion line of packaging services in 2015, an order of magnitude larger than the current fan-out market, which was estimated at US\$174 million in 2014. However, from 2016, with the adoption of fan-out WLP for application processors (APUs), packages previously addressed by flip-chip/PoP technologies, a high growth for fan-out WLP is expected.

Impact of inFO PoP and capacity increase

TSMC has been developing WLP technologies for several years and has already established a presence in fan-in WLP. The news is that its fan-out based inFO platform might be ready for prime time. Apple needs innovative packaging solutions to follow its progressive A10 mobile processor, and TSMC seems to have the cutting edge technology to address Apple's needs. While Samsung

and Intel are circling around the same area, TSMC seems to be favored, with its inFO PoP and 16nm node technology, as the first choice for Apple's A10 processor for 2016 editions of the iPhone 7 and 7+ series. Whether the A10 will be partly split with Samsung, or all the volume will go to TSMC and supporting outsourced semiconductor and test suppliers (OSATs) licensing inFO, remains to be seen. The TSMC inFO is not just about winning high volume from Apple, it represents a gateway for other fan-out technologies, and manufacturers as well. Furthermore, with this grand market opening, a beginning of real competition between TSMC and OSATs will be initiated where differences in CAPEX power, innovation pace and new partnerships will be key. With TSMC's push, and with fan-out generally stepping into the flip-chip domain, since the fan-out WLP approach in most cases does not utilize a flip-chip type substrate, the demand for flip-chip substrates could be negatively impacted. Therefore, 2016 could be that game changer where the industry will see inFO penetrating into iPhones and iPads followed by an awakening of competitive fan-out SiP/PoP solutions spreading into other high-end smartphones, APU/memory, FPGA, and GPU packaging.

According to Yole's analysis, Apple/TSMC inFO adoption will transform the fan-out market and result in a revenue increase from US\$174 million in 2014, to US\$2.4 billion by 2020, as shown in Figure 3. The transition phase growth of 10% from 2013 to 2014 will be modified to a 32% compound growth after the 2016 jump [6].

Along with steady growth of fan-in packages, fan-out adoption relates to stringent demands in capacity increase, as indicated in Figure 4. According to projected demand and current capacities, Yole estimates that 2014 leftover WLP capacities are enough for only one-third of the additional demand expected in 2016. Furthermore, 2014 leftover capacities are estimated to be an order of magnitude lower than the cumulative capacity increase that will be required by 2020.

Summary

Although a mature platform, fan-in WLP is on an evolutionary path. Due to its major advantages, low cost and thickness, fan-in is expected to further grow, its adoption being further expanded to higher pin-count packages. Fan-out WLP is expected to make a major breakthrough within the next year, likely led by TSMC inFO PoP and followed by other fan-out multi-die solutions. Furthermore, looking at the long term, a bright future lies ahead for wafer-level packages with respect to IoT requirements as they are well positioned to answer related cost, form and functional integration demands.

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Biography

Andrej Ivankovic received a master's degree in Electrical Engineering, with specialization in Industrial Electronics from the U. of Zagreb, Croatia, and a PhD in Mechanical Engineering from KU Leuven, Belgium. He is a Technology & Market Analyst, in the Advanced Packaging and Semiconductor Manufacturing team, at Yole Développement; email ivankovic@yole.fr

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Overview of 3D-integration activities at CEA-Leti

By Séverine Chéramy [\[CEA-Leti\]](#)

CEA-Leti has focused on 3D integration at the architectural and technological levels for many years. In 2007-08, Leti inaugurated its 3D and MEMS 200mm line and added a 3D 300mm line in 2011 to meet the needs of its industrial customers. Dating back to 1975, the relevant patent portfolio has grown to more than 100 patents.

Today, Leti's 3,000m² 3D-300mm cleanroom, focused on back-end technologies, has more than 40 process and metrology tools that are either dedicated to 3D integration, or shared with other platforms. These support advanced developments on a range of technologies and processes, from through-silicon vias (TSV) to wafer-level packaging (WLP). The objectives are both to base developments on a state-of-the-art line and to work in parallel on innovative bricks. For example, Leti is equipped with a state-of-the-art deposition tool from SPTS Technologies. This equipment comprises an industrial mainframe surrounded by several deposition chambers for barrier and seed, ionized physical vapor deposition (iPVD) and chemical vapor deposition (CVD) layers. A complete lithography line is also available, including a 3D stepper from Canon. For packaging, two fine-pitch pick-and-place tools from Panasonic and SET are available to focus on chip-to-wafer integration (thermocompression and direct bonding).

Metrology, defectivity and inspection also play an important role in 3D process development. Leti collaborates with leading equipment suppliers such as Rudolph Technologies and Fogale nanotech to address important challenges in this

area and reduce time to development. The two complete 200mm and 300mm manufacturing lines have allowed Leti and its partners, throughout the years, to develop pioneering demonstrators. This article describes some of the recent development advances and key successes.

Advanced technology boxes

Leti is working on each of the 3D challenges: temporary bonding, interconnection, TSVs, packaging, and thermal and mechanical management. This section focuses on TSV and chip-to-chip interconnection.

TSVs. The multiplicity of possible final applications for 3D integration creates a very wide range of specifications, specifically with TSVs. Specifications for the first TSV technology that was developed, for CMOS image sensors (CIS), were for medium interconnect density with a TSV-last approach (70μm diameter for an aspect ratio of 1:1). Today's specifications for interposer and high-performance computing (HPC) applications require a high interconnect density, while managing interposer warp. This leads to the highest possible aspect ratio of TSV-middle (diameter 10μm and aspect ratio of more than 10:1). Another example with a very dense 3D logic stack: the smallest-possible TSV with a small keep-out-zone (KOZ) will be preferred (diameter 1μm, aspect ratio of about a few microns). Leti continues to work on a wide range of TSVs to meet all those challenges, and the TSV-middle and TSV-last strategies are continuously reviewed, because both types of interconnects present advantages and drawbacks.

Our work on fine-pitch TSVs (typically less than 30μm) and wide

I/O for application processors led in early 2010 to the development of TSV-middle, mainly for high-bandwidth requirements. Following that, we used a similar process for 2.5D interposers, but the current trend is to increase the aspect ratio with the same diameter. The objective is to make thermal and mechanical management simpler by increasing the silicon thickness, which is the first requirement to address thermal dissipation and warp issues. Our current work led us to focus on barrier and seed deposition (iPVD, CVD and wet), as well, and TSV filling. Advanced work on dielectric deposition, low temperature and low stress that is nonetheless compatible with very high aspect ratios, such as 20:1, is underway (**Figure 1**).

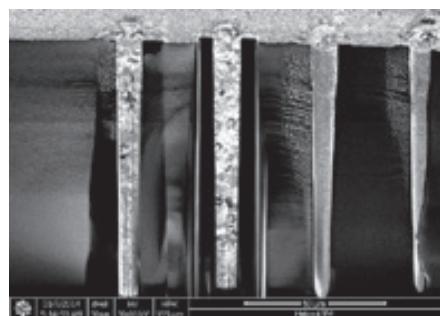


Figure 1: TSV 10μm *120μm.

Finally, we believe that some very different applications will require a very dense TSV matrix to connect, for instance, more than two logic dies, or when partitioning logic, analog and memory functions. Some simulations suggest that a pitch of 1μm would be required in case of partitioning. Advanced work is underway to achieve that challenging goal, with a strategy



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of integrating both TSV-last and TSV-middle (**Figure 2**).

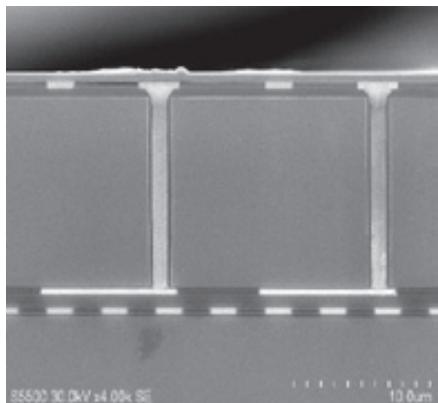


Figure 2: TSV 1μm *10μm.

Silicon-to-silicon interconnection. Copper pillar technology with a pitch of 40μm is now state-of-the-art and available for industrial applications. Leti's current work on copper pillar, pushed by the requirements of HPC, is focused on obtaining a very dense matrix of copper pillar, at the finest pitch possible (**Figure 3**). Our target is 20μm, but it is important

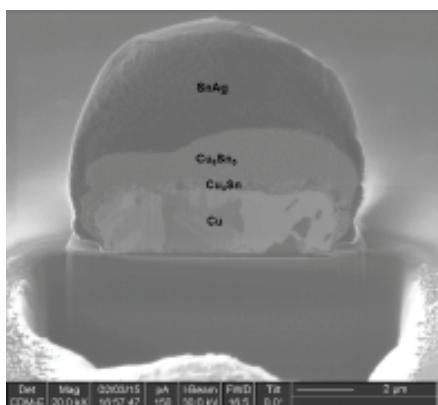


Figure 3: Copper pillar diameter 10μm.

to note that our specification uses a very similar process to the one currently used in production, which makes our process easily transferable. Underfill and stacking are included, mainly by working on pre-applied underfill at both chip and wafer levels.

As the need for shrink will undoubtedly continue, we have been developing an alternative approach in parallel to our pursuit of copper pillar diameter reduction. This copper-copper direct-bonding approach combines the excellent advantages of a room-temperature, no-pressure process that does not require any underfill. This technology, described in many papers, has proven to be feasible for wafer-to-wafer bonding. A pitch of 7μm has already been achieved on 200mm and 300mm wafers (**Figure 4**). Extensive electrical and reliability data complete this

about the process if you consider stacking a 200mm wafer on a 300mm wafer? What would be the yield when stacking two advanced-node wafers together? Will copper-to-copper bonding be limited to similar die-size bonding? Will it be suitable also for the interposer? Given these limitations to wafer-to-wafer bonding, chip-to-wafer bonding is an interesting alternative, but it requires supplementary work on equipment, process and full integration, which also is underway at Leti. We are also considering chip-level self-alignment to improve both alignment and throughput.

Some key successes

Ramp-up of 3D developments started after the success and transfer of the TSV-last approach for CMOS image sensors at STMicroelectronics. Since then, Leti has been convinced that complete demonstrators are key to validating the interest of 3D integration. As a result, Leti and ST showed with set-top-box applications in 2011 (**Figure 5**) that:

- Replacing wire bonding with TSVs has no impact on the performance of the digital part; and
- Partitioning the analog and digital parts has no impact on the performance. This was demonstrated to be technically viable and economically interesting by focusing the analog part on the 130nm node, while the digital part can scale to 28nm or lower.

Obviously, this proof of concept exceeded the application of the set-top box and could be a very effective way

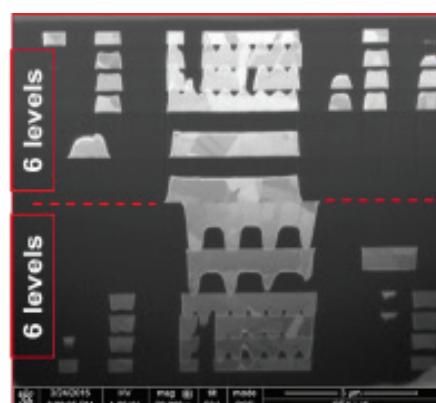


Figure 4: Copper-copper hybrid bonding, pitch 7μm.

work and position this technology as the main driver in several product roadmaps, such as for imaging applications. Our roadmap anticipates a pitch of 1μm within two years.

While wafer-to-wafer integration technology is nearly transferable, it nevertheless already shows some limitations that raise questions: what

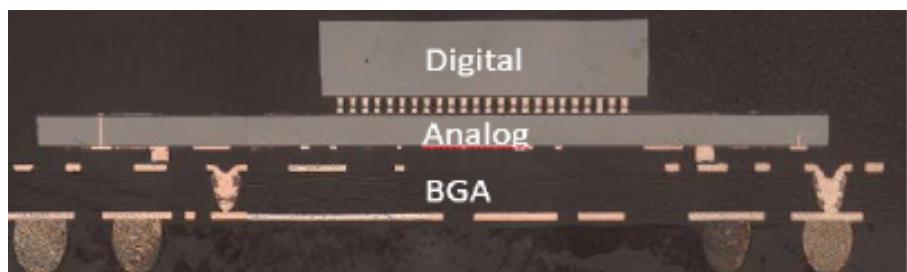


Figure 5: Logic/analog partitioning. SOURCES: STMicroelectronics/Leti

BETTER TECHNOLOGY STRONGER TOGETHER

JCET Completes Acquisition of STATS ChipPAC to Ascend to a Leading OSAT Player Globally

China's leading semiconductor packaging and testing company, Jiangsu Changjiang Electronics Technology (JCET, SHE: 600584), successfully completed the acquisition on Aug 5 2015 of STATS ChipPAC, a leading provider of advanced semiconductor packaging and test services headquartered in Singapore. This USD 780 mn transaction was originally announced on Dec 30 2014, and was conducted through JCET-SC (Singapore) Pte. Ltd., a subsidiary of JCET.

This acquisition will escalate the combined entities to one of the world's top outsourced semiconductor assembly and test (OSAT) players. As a combined group of companies, JCET and STATS ChipPAC offer a broader technology portfolio with significant manufacturing scale in key semiconductor geographies. The acquisition will also improve the competitiveness of the Chinese semiconductor packaging and test industry with a strong intellectual property (IP) and innovation portfolio built around advanced technologies acquired by JCET.

"The completion of our acquisition of STATS ChipPAC is an important step for us, and it presents an exciting win-win opportunity for both companies, supporting our long-term success," said Xinchao Wang, Chairman of JCET. "Post acquisition, the combined entities will provide one of the most extensive product/service portfolios to a highly diversified customer base with wide geographical coverage. Our leadership position in advanced packaging technologies will be further strengthened through the acquisition. JCET and STATS ChipPAC are working together to deliver the substantial revenue and cost synergies for our investors."

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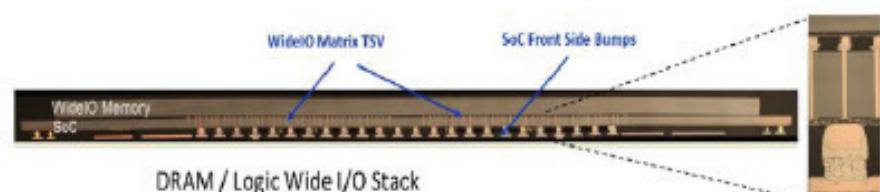


Figure 6: Wide I/O DRAM/logic demonstrator using a TSV-middle process at the 65nm node in a face-to-back approach. SOURCES: STMicroelectronics/Leti.

to reuse technology for mature fab lines that cannot scale.

Beginning in 2010, Leti, along with its partner, SHINKO, realized the passive interposer for HPC applications on 200mm and 300mm wafers. It was also the time that the wide I/O approach (DRAM/logic) gained favor. In July 2012, ST-Ericsson released the first wide I/O demonstrator, realized with a TSV-middle process at the 65nm node in a face-to-back approach, working with STMicroelectronics and Leti (**Figure 6**).

This list is not complete, of course. We also should cite what we call “vehicle test wafers” or “technology wafers,” which denote our developments to guide designers with design rules. For instance, we developed a dedicated 3D thermal die containing more multiple sensors and hot points to characterize the thermal mapping in a 3D stack.

New developments

Convinced that 3D integration has reached sufficient maturity to be considered for other applications, Leti, STMicroelectronics and Mentor

Graphics, through the IRT Nanoelec program, designed and realized 3DNoC demonstrators in 2015. They demonstrate the use of 3D stacking technology in scalable, complex digital systems-on-chip (SoC). This two-die logic stack connected by a network-on-chip (NoC) not only again proves the viability of the integration, but above all proves with real data that 3D stacking can improve the performance of the package. Extensive data on this will be provided at ISSCC 2016 (**Figure 7**).

Exploring alternatives. Leti has also used its 3D 300mm line to recently demonstrate what is believed to be a first for the MEMS industry: fabrication of MEMS on 300mm wafers (**Figure 8**). The announcement was made on September 17, 2015 during the European MEMS Summit in Milano, Italy. The demonstration was Leti’s proprietary M&NEMS (micro and nanoelectromechanical systems) platform that allows fabrication of a variety of sensors currently integrated in smartphones. This manufacturing

concept enables the design and fabrication of combo sensors, such as three-axis accelerometers, three-axis gyroscopes, and three-axis magnetometers on the same chip, as well as pressure sensors or microphones. The M&NEMS technology is currently being transferred to an industrial partner through a non-exclusive agreement.

In addition to lowering costs, manufacturing MEMS with 300mm technology enables 3D integration with MEMS CMOS processes in more advanced nodes than on 200mm wafers, and the use of 3D TSVs, which is already available in 300mm technology.

Summary

At Leti, we compare 3D integration to assembling bricks, like LEGOS®, in its design and technology potential. We have a strong base to develop any new architecture, and we continue to push the limits.

The next demonstrator “IntAct,” scheduled in early 2016, is an active C65nm interposer for all high-performance applications: it combines design partitioning, power management embedded in the C65nm interposer and design-for-test features. The technology includes chip-to-chip connection pitch <20µm, high aspect ratio TSV-middle and warp management.

We are already thinking about 3D-stack fine-pitch using copper-copper bonding pitch at 1µm.

Acknowledgement

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Biography

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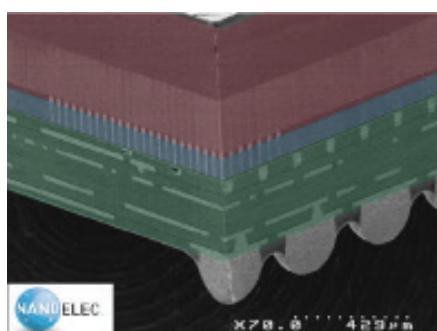


Figure 7: 3DNoC demonstrator from the IRT Nanoelec program.

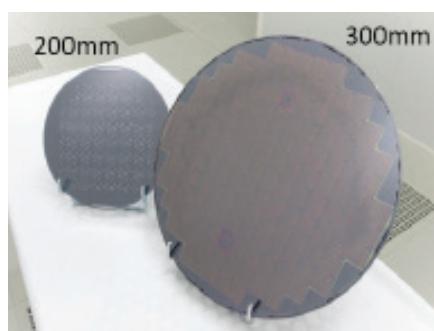


Figure 8: 200mm and 300mm wafers with MEMS devices.

Chip package interaction for advanced nodes: a holistic approach for foundries and OSATs

By Jae Kyu Cho, Frank Kuechenmeister, Dirk Breuer, Jens Paul, Michael Thiele [GLOBALFOUNDRIES Inc.]

For more than half a century, advancement of silicon process technology has tried to keep pace with Moore's law. The main focus was device down-scaling, focusing on processing power improvement for high device density, high clock speed/bandwidth, and low power consumption. The recent dramatic changes in front-end-of-line (FEOL) technologies in silicon, from conventional Poly/SiON gate to high-k metal gate and nonplanar transistors (FinFET), are widely known. Another important change to note for the packaging industry is that back-end-of-line (BEOL) in silicon is also experiencing striking change from conventional silicon dioxide (SiO_2) dielectric material to ultra low-k (ULK) dielectric material in order to achieve low RC delay, reduced power consumption, and less crosstalk.

In a similar manner, the packaging industry introduced various innovations such as thermocompression bonding, wafer-level packaging, and 2.5D/3D technologies. These packaging industry efforts equally contributed to the technological advancements with performance boost, high I/O counts, small footprint, and a high level of integration. However, ULK dielectric material in a silicon BEOL stack is porous and brittle, and widely known for its inferior mechanical properties. Therefore, the combination of the recent industry trends of a larger die size and ULK dielectric material, especially in advanced Si nodes with advanced packaging technology, imposes significant chip package interaction (CPI) challenges. CPI became one of the critical reliability issues that needed to be addressed to avoid electrical or mechanical failure in products. When addressing CPI challenges, different areas have to be considered, ranging from silicon processing, package assembly processing, assembly material, and substrate technology. To better understand, identify, and overcome unprecedented

CPI challenges, a holistic effort between foundry and outsourced semiconductor assembly and test providers (OSATs) is required, and this article mainly focuses on GLOBALFOUNDRIES' overall CPI analysis approach, consisting of CPI test vehicle chip design, BEOL stack analysis, and CPI reliability stress testing.

Chip package interaction (CPI)

The growth of microelectronic technology to fulfill ever-increasing various market demands requires creative silicon/package technology. In turn, there is always the potential to bring up unprecedented CPI challenges in the industry. The main goal of CPI analysis is to maintain the structural integrity of packaged parts through various stress tests and to prevent any potential manufacturing or reliability related issues [1]. As the industry faced several CPI-related failures over the last decade, CPI qualification became one of the prerequisites for technology qualification before a product tape-out. Unfortunately, each package type faces unique CPI challenges, so it is important to qualify each package type independently. The first step to fully appreciate CPI challenges is to understand their origin and underlying contributing factors. For instance, the main CPI challenge for a wire bonding device comes from thermomechanical stress during the wire bond (thermosonic) process on a bond pad in BEOL, while the biggest challenge for flip-chip devices comes from the mismatch of the coefficient of thermal expansion (CTE) of the individual package components after chip attach, as shown in **Figure 1** [2].

The nature of CPI challenges is very complex and needs extensive attention from various points of view as shown in **Figure 2a**. Failure of proper CPI management often results in catastrophic failure, as shown in **Figures 2b-e**. The critical factors contributing to the CPI-related thermomechanical stress can be categorized as follows:

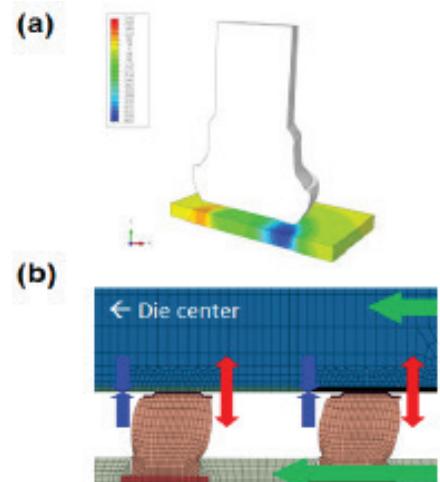


Figure 1: Illustration of CPI challenges at the package level: a) wire bond case [3], and b) flip-chip case.

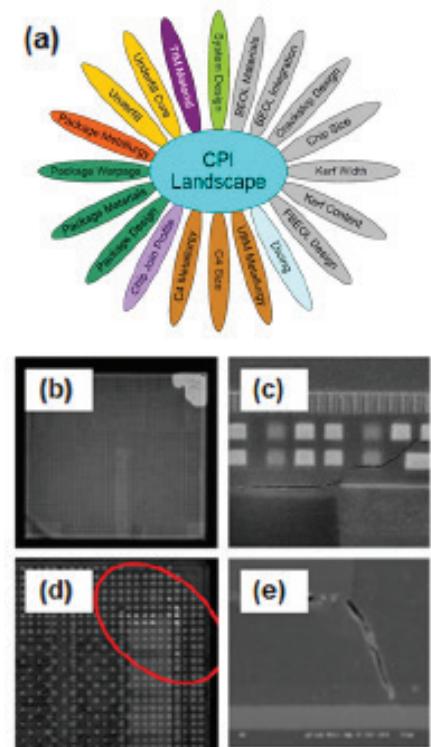


Figure 2: a) Various components affecting CPI result for flip chip [4]. Common CPI-related failures: b) Corner delamination, c) BEOL stack crack, d) White bump, and e) Underfill crack.

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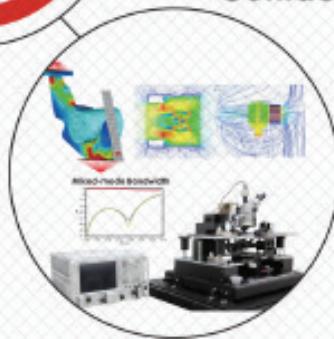
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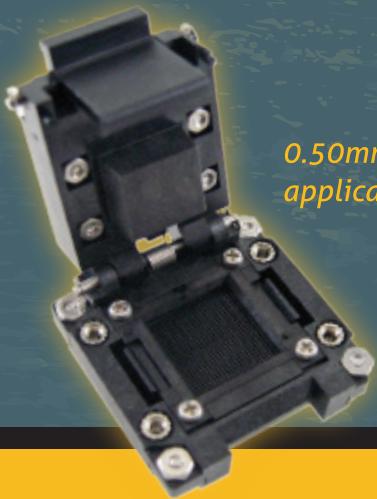
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- Silicon processing, especially BEOL/FBEOL (far-back-end-of-line) layer processing involving multiple layer deposition and high-temperature curing/annealing, results in intrinsic stress in the thin films.
- Package processing, including chip attach, wire bonding, or dicing processes, introduces stresses from their environmentally harsh processing conditions in the final package configuration.
- Lay out design, size, and metal/via density in silicon and substrate affects effective modulus; and co-planarity, in turn, affects the structural integrity of materials.
- CTE mismatch of adjacent package materials (silicon, underfill, molding compound, thermal interface material, and substrate) introduces mechanical strain/stress in the system.
- Any defects introduced during processing are the weakest in structure and can be an initiation point for CPI-induced failures and therefore, need to be controlled.

CPI test vehicle

In order to understand CPI-related thermomechanical stress on a package, a CPI test vehicle (TV) is designed and verified before product tape-out at each silicon technology node. Die size and the BEOL stack are two of the critical factors for CPI TV design. Other factors such as FBEOL interconnect option and substrate types are also taken into account. In general, GLOBALFOUNDRIES aims to design a CPI TV to be the most representative of future product lines. In that sense, the CPI TV die size should cover most of future products' die sizes as a larger die size imposes a higher CPI related-risk. The CPI TV contains several CPI macro structures that are electrically accessible. In CPI analysis, it is well known that the distance to neutral point (DNP) is a critical element for CPI-related risk. It is also widely known that higher DNP imposes higher CPI-related risk, so most of the CPI macro structures are predominantly located near the four die corners and periphery domain, as shown in **Figure 3**. After silicon wafer processing, the CPI TV goes through the final package assembly process. The CPI macro structures inside the CPI TV are sensitive enough to measure any structural integrity impact during package assembly or reliability testing. The JEDEC standard deals with several examples of CPI structures [1]; however, in most of the cases, depending on the package type, application, and market,

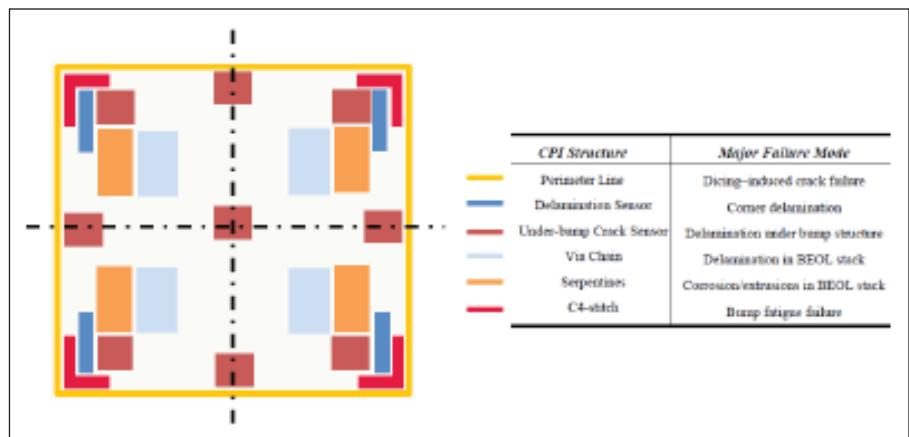


Figure 3: Schematic of CPI TV design layout for flip-chip application.

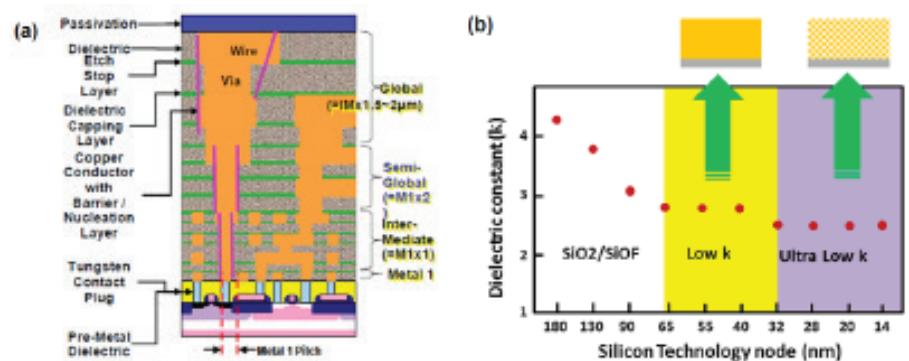


Figure 4: a) Schematic illustration of a cross section of a BEOL stack [5], and b) The general trend in dielectric material in the BEOL stack.

additional types of CPI macro structures need to be considered in CPI TV design.

Back-end-of-line (BEOL) stack in silicon

To better understand the structural integrity between chip and package, it is crucial to understand how the BEOL stack in silicon plays a role in CPI risk assessment. In integrated circuit (IC) fabrication, individual devices such as the transistor and static random access memory (SRAM) are constructed on a silicon substrate and multiple metallization layers along with the insulating interlayer dielectric (ILD) layers consisting of a BEOL stack. The BEOL stack is a wiring layer to transmit signal and power between devices and the substrate/board, as illustrated in **Figure 4a**. With the BEOL stack residing on top of devices, the electric performance of the devices is often limited by the RC time delay of the ILD layers. In order to boost electric performance in the BEOL stack, various efforts were focused on reducing the effective dielectric constant (k) of the ILD layers. As shown in **Figure 4b**, in the 1990s and early 2000s, efforts were focused on introducing

various chemical components in the BEOL stack, and these efforts successfully resulted in a scale-down of k in the ILD layers. Sub-100nm Si technology required a different approach, and the industry figured out an innovative one by physical modification of the ILD layers. The first physical modification was realized by the reduction of density in ILD—the so-called low- k (LK) dielectric. Further reduction of k was achieved by introducing nanopores (essentially nano air bubbles) in ILD, and this approach, known as ultra low- k (ULK or extreme low- k : ELK) ILD, has been rapidly adopted in the industry and successfully used for advanced silicon technology nodes. However, continuous reduction of k in ILD resulted in the modulus reduction of the ILD, which in turn, resulted in the deterioration of the BEOL structural integrity. To minimize the use of ULK/LK dielectric, therefore, it is common practice in the foundry industry to utilize ULK/LK layers in lower metal layers with fine metal pitch, and to utilize SiO₂ layers in upper metal layers with loose pitch. Therefore, the stack trends of ULK/LK in BEOL stacks and the role of ULK/LK in BEOL structural integrity have been attracting various efforts from a CPI point of view.

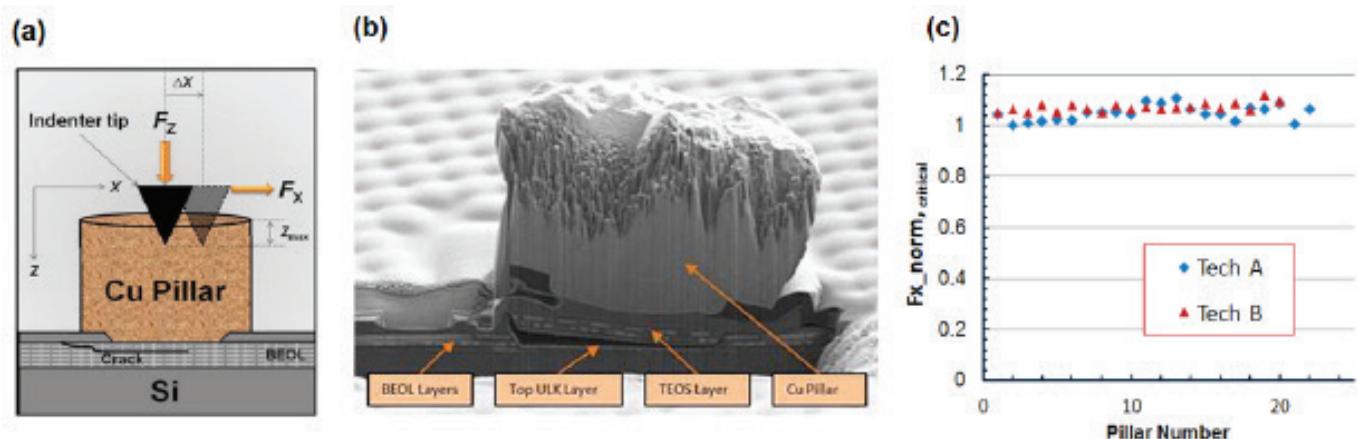


Figure 5: Description of BABS test: a) Schematic of the BABS test. Critical force is monitored in situ while a nanoindenter indents a bump in the z-direction and shears off in the x-direction. b) A cross sectional view after the BABS test. c) Critical lateral force (F_x_{norm}) comparison between Tech A and Tech B.

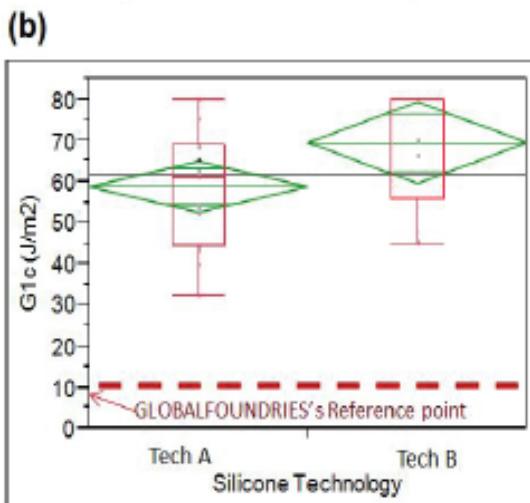
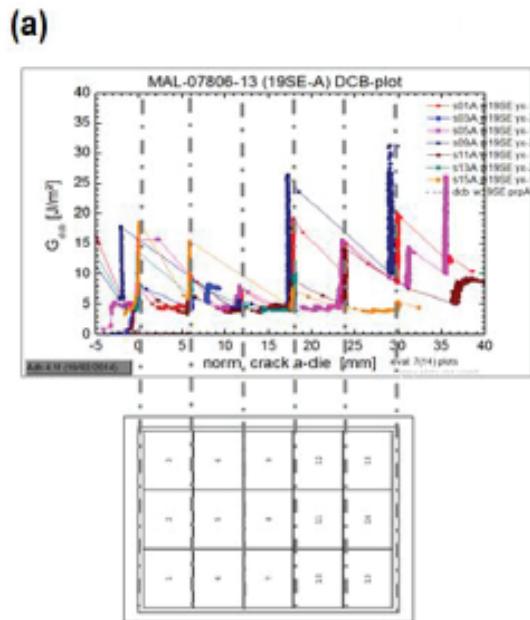


Figure 6: DCB test result: a) Critical energy release rate (G_c) converted from load-displacement data. b) Critical energy release rate (G_c) comparison between Tech A and Tech B.

Analytical methods for BEOL stack structural integrity

At GLOBALFOUNDRIES, three analytical methods are commonly used to characterize the mechanics of a BEOL stack: bump-assisted BEOL stability indentation (BABS), double cantilever beam (DCB), and four-point bending. The microelectronics industry has adopted various concepts from structure/fracture mechanics, and many analytical methods have been modified/developed for microelectronic applications. The BABS test is GLOBALFOUNDRIES' patented technology and specifically provides information on BEOL stability at the silicon level without package assembly. The DCB test provides information on the critical energy release rate of BEOL and is useful to characterize crackstop structure bond-strength in the BEOL stack. The four-point bending test is used to measure interfacial properties of thin films. In particular, BABS and DCB are useful for full BEOL stack construction; the following paragraphs describe BABS and DCB in more detail.

BABS testing. In BABS testing, a bumped wafer is indented vertically and sheared off horizontally by a nanoindenter. **Figure 5a** describes how the BABS test is performed, and more detail can be found in the

reference articles [6, 7]. The external shear stress, induced by the nanoindenter, initiates a crack in the BEOL stack that continuously propagates through the ILD/metal layers. The post-test cross-sectional view (**Figure 5b**) shows how a typical crack propagates, and which interlayer has a weakness or a reduced interfacial adhesion. As expected, BABS test results showed that the uppermost ULK layer was most prone to crack failure. The plot in **Figure 5c** shows a comparison of the critical lateral force (F_x_{norm}) between BEOL stack options of two advanced silicon nodes. Tech A is a silicon technology in high-volume manufacturing (HVM) and used as a reference for the BABS test. Silicon Tech B is a technology under development and this data indicates that both silicon Tech A and silicon Tech B with a different BEOL stack showed equivalent BEOL stack strengths.

DCB test. For the DCB test, two parallel silicon strips are bonded together using epoxy with an artificial initial crack present. By opening up the pre-existing crack with known crack length, load-displacement behavior can be monitored (**Figure 6a**), which provides the critical fracture energy release rate (G_c) (shown in **Figure 6b**). This analytical method is a complementary method with BABS to characterize BEOL structural integrity, and it is also a very useful method to characterize crackstop strength in the BEOL stack. **Figure 6b** shows the critical energy release rate data for die crackstops in two different GLOBALFOUNDRIES' advanced silicon technology nodes. In both cases, the crackstop (G_c) meets GLOBALFOUNDRIES' internal requirement to ensure adequate protection of the die from edge cracking or delamination under external thermomechanical stimuli.

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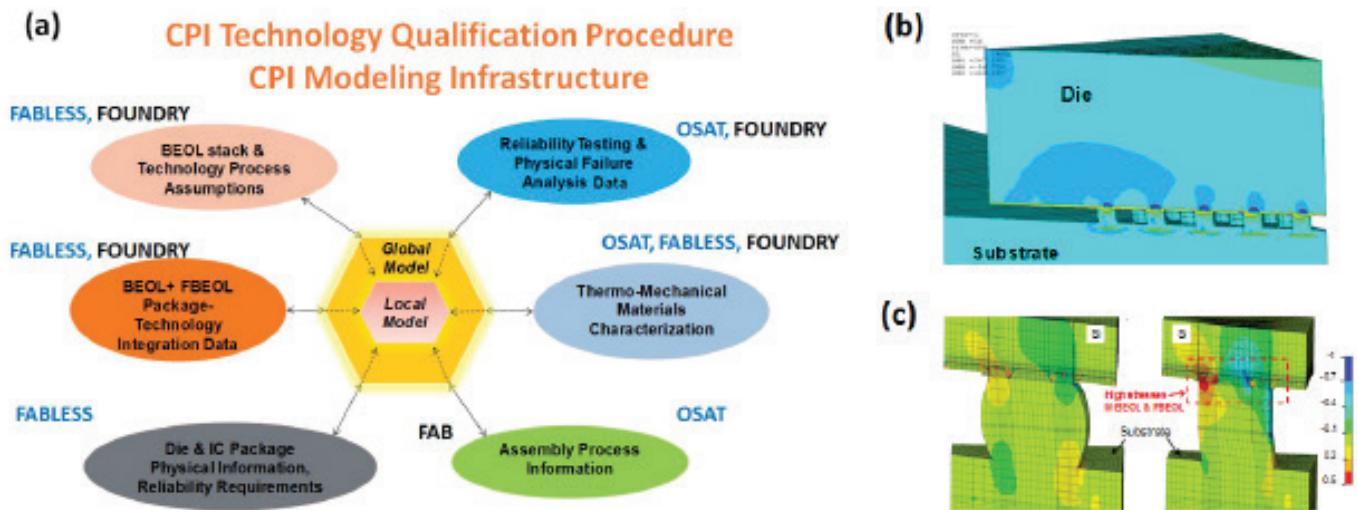


Figure 7: a) CPI FEA modeling infrastructure, b) Typical FEA simulation result for the global model, and c) Typical simulation result for the local model.

Stress Test	Test condition	Target	SAM
Pre-conditioning (MSL3)	Pre-bake 125 °C/24 hr Moisture soak 30 °C /60 %RH/192 hr 3x Reflow – peak temperature 260 °C	0 eTest failure	0 failure
TC	-55 °C/125 °C, 1000 cycle	0 eTest failure	0 failure
mHAST	130 °C/85 %RH, 96 hr	0 eTest failure	0 failure
HTS	150 °C/1000 hr	0 eTest failure	0 failure

Table 1: Component-level CPI qualification reliability tests and conditions.

Finite element analysis

Once CPI TV design and layout is complete, and the target packaging option is determined, it is critical to analyze its thermomechanical behavior by simulation in advance. Even in the same silicon technology, depending on the target market and performance requirement, there are several different BEOL stack options. Qualifying all available BEOL stack options through CPI reliability testing is costly and practically impossible; therefore, finite element analysis (FEA) simulation can be used as an effective tool to predict/analyze thermomechanical behavior of a package with various BEOL stacks and package options as a first screening step [7]. For the BEOL stress analysis that is performed in CPI modeling, there exist three to six orders of dimensional differences between features in the BEOL level (nanometer scale) and package level (millimeter scale) that cause significant computational challenges in determining the stress levels of the various elements. Therefore, a global model is typically first constructed based on several elements as shown in **Figure 7**. Once the global model is completed, a localized sub-model is created to determine BEOL layer stresses based on a refined subset of boundary conditions from the

global model. For advanced silicon node chips utilizing flip-chip packaging, it is well known that the ULK layer is one of the weakest points from a CPI perspective. Therefore, the main areas of interest are ULK layers in the BEOL stack and solder joint domains, which is where the localized sub-models are focused. In general, based on these FEA simulation results, the BEOL stack with the highest CPI risk is chosen for package reliability testing using the CPI TV.

CPI reliability testing

After full package assembly, the CPI TVs undergo reliability testing, as shown in **Table 1**. GLOBALFOUNDRIES follows JEDEC standard reliability stressing conditions for each of the tests performed. CPI reliability testing starts with “known good packages,” and resistance/leakage changes of the CPI macro structures are measured at several read-outs. Resistance changes greater than $\pm 20\%$, and leakage currents greater than $1\mu\text{A}$ are considered a failure. As a final step, all stressed packages undergo scanning acoustic microscopy (SAM) inspection after electrical verification to check for any indication of layer delamination or mechanical failures [8, 9].

Future CPI challenges

From a foundry industry perspective, reducing the dielectric constant (k) in a BEOL stack is a major challenge to boost electrical performance, and the next potential movement is to introduce air gaps in the ULK BEOL stack because air has the lowest dielectric constant on earth. However, it would result in an even lower modulus BEOL stack, and in turn, maintaining the structural integrity is likely to be very challenging. From an OSAT perspective, flip-chip with a coreless substrate, or fan-in/fan-out wafer-level packaging (FOWLP), is becoming more popular as a cost-effective option with a smaller footprint. However, the current packaging trends of minimizing CTE mismatch, maintaining warpage control, and bigger die size add additional challenges. Moreover, the microelectronic industry is moving toward 2.5D/3D integration with through-silicon via (TSV) and integration with photonics. It is important to note again that CPI challenges are caused by the outcome of interplay between the chip and package. Therefore, to overcome these significant CPI challenges and to successfully implement technological achievements into high-volume manufacturing, the holistic approach between foundry and OSATs from a chip design to final package assembly is a crucial factor, and GLOBALFOUNDRIES has been actively collaborating with various OSATs to achieve these goals.

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3D packaging and system integration

By Hamid Eslampour, Goo Lee, Seung Wook Yoon, Dongkai Shangguan /STATS ChipPAC

The emergence and evolution of any package technology is driven by market trends as experienced by the end application. With the maturing of the mobile market, the trends for smartphones and other mobile devices are more than ever for lower cost. Meanwhile, a higher degree of functionality and performance, thinner devices, and longer battery life are some of the additional market drivers seen in these devices. The implications of these market drivers on the packaging content of mobile devices are higher performance packaging, lower cost, smaller form factor, and a higher level of integration.

System-in-package (SiP) technology has been evolving through utilization of various package technology building blocks to serve the market needs with respect to miniaturization, higher integration, and smaller form factor as cited above, with the added benefits of lower cost and faster time-to-market as compared to silicon (Si) level integration, which is commonly called SoC or system-on-chip. As such, SiP incorporates flip-chip (FC), wire bond (WB), and fan-out wafer-level packaging (FOWLP) as its technology building blocks, and serves various end applications ranging from RF, power amplifiers (PA), MEMS, and connectivity, into more advanced application processors (AP), and other logic devices such as GPUs/CPPUs. The specific SiP technology used in each application varies in complexity based on the number of components and the pin count of each component as defined by each application. For example, while an AP SiP package may utilize the more advanced 3D SiP type, the relatively less complex RF SiP may utilize laminate-based FC technology or an FOWLP.

According to Prismark Partners, by 2019, SiP packaging TAM will be exceeding 39 billion units (Bu) encompassing various market segments including mobile, automotive, computing, Internet-of-Things (IoT), wearable electronics (WE), and medical. While the package form, fit, and functionality requirements for each of these

market segments varies, mobile, IoT, and WE segments, which constitute the bulk of the TAM, have a few drivers in common including: a small form factor, a high level of integration,

and low power consumption as needed for longer battery life. These drivers collectively promote the adoption of FOWLP as one of the ideal SiP solutions in these market segments. In general, the increased popularity of SiP is also based on other drivers in addition to those cited above, including: 1) the added design flexibility, 2) better electromagnetic interference (EMI) isolation and cross-talk control, 3) lower total product cost due to avoidance of costly SoC integration, 4) simplification of the end application's electronic manufacturing service (EMS) surface mount technology (SMT) process with fewer components, and 5) the enablement of plug-and-play solutions.

Integration technologies

SiP by definition constitutes a number of components that are all packaged together to form a sub-system. Depending on the end application they serve, these components could comprise passives, RF filters, power, sensors, and/or logic chip in packaged or bare die form. The form of integration of all these components together in one module or package as SiP is determined not only by the technologies used in fabrication of the individual chips, such as WB or FC, but also by the level of form factor reduction that is to be achieved. An SiP containing chips using WB technology cannot attain the same form factor as the SiP using FC technology, or WL technology, on account of the routing requirements imposed by the interconnect schemes. A greater level of integration can also be attained by replacing the passives with integrated passive devices (IPDs), or the

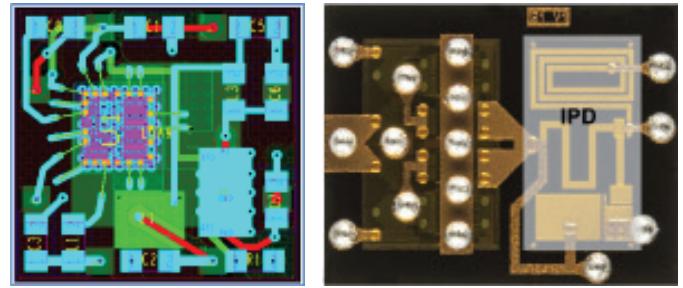


Figure 1: Conversion of laminate SiP (left) to eWLB SiP (right).

use of embedded passives in substrate (EPS) technology.

Figure 1 is an example of a PA module that was initially designed in an 8x8mm² SiP with passives and a CMOS chip using an SMT process on laminate, which was later converted to FOWLP or embedded wafer-level ball grid array (eWLB) package resulting in a 4x5mm² package size, and a 70% package body size reduction.

The SiP consists of an integrated passive device (IPD) that has replaced all the passive components as shown in the original laminate design, in addition to a PA CMOS chip, all integrated into the 4x5mm² eWLB package outline using one redistribution metal layer (RDL). The 4x5mm² package contains the IPD die measuring at 2.9x1.7mm² and CMOS PA die measuring at 3x2mm², one RDL metal, and two passivation layers, with BGA balls facilitated through the ball-drop process.

The general integration concept described above is used in conjunction with the given package technology with key benefits of faster design cycle time, quick assembly turnaround time, and faster time-to-market, by enabling various subsystems such as RF front-end modules (FEMs), antenna switch modules (ASMs), and connectivity modules, containing many components such as filters, switches, transceivers, sensors, and micro-control units (MCUs) [1]. Depending on the end application and overall system constraints, the integration can be done through FOWLP or other package configurations as shown in **Figure 2**.

As cited earlier, RF systems are one of the main beneficiaries of SiP technology because of the inherent nature of the various

heterogeneous components that they incorporate in enabling their end function. **Figure 2** shows a chip-scale module package (CSMP) for a WLAN modem application, which consists of an IPD as the substrate, a baseband (BB) chip, RF chip, EEPROM, and a number of passive components, assembled in an SiP. The value proposition for this

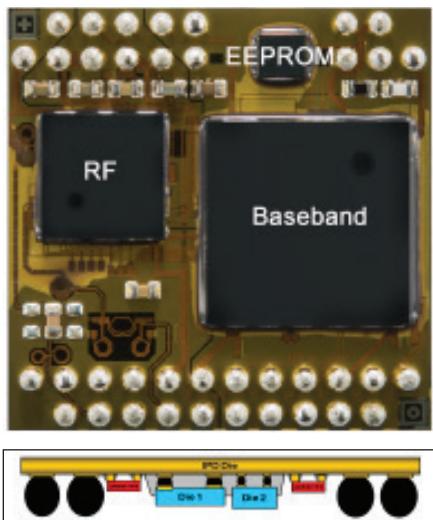


Figure 2: WLAN, CSMP SiP.

package technology is the smallest form factor enabled for the product by using conventional SMT processes for component attach, and the integration of an IPD acting as the substrate.

The IPD measures at $9 \times 9 \text{ mm}^2$ and 0.45mm in thickness, and has the RF, BB and EEPROM flip-chip attached, along with 9 passives that are mounted using an SMT operation. More specifically, chip-to-wafer (C2W) FC and SMT processes are used for the fabrication process, followed by wafer-level BGA attach, and the final wafer saw singulation process.

3D integration

Higher levels of integrations can be achieved through adoption of 3D packaging technologies to combine various functional blocks together in creating the SiP module. The 3D packaging technologies generally include package-on-package (PoP) and either utilize laminate-based FC or WB technology, or FOWLP technology. The latter results in further form factor reduction compared to the laminate-based PoP through the elimination of the substrate and implementation of more advanced routing densities. **Figure 3** depicts this 3D eWLB PoP with logic die in the

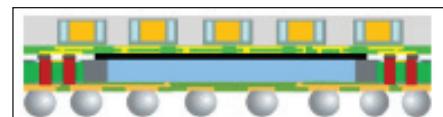


Figure 3: eWLB PoP SiP with passives and logic die.

bottom eWLB package, and the collection of passives and filters in the top package.

The bottom eWLB package measures only 470 μm in height including the BGA balls, and the top FBGA package with passives measures at about 810 μm in thickness, primarily driven by the thickness of passives and the mold cap used in the top package for encapsulation. One example of the end application or device benefiting from such a 3D packaging concept could be an RF-FEM where the CMOS die is located in the bottom eWLB package, and other components including SAW filters, passives, duplexer, and low-noise amplifier (LNA) located in the top FBGA package. In this package, the $3.8 \times 3.8 \text{ mm}^2$ die fits in the bottom eWLB package outline of $5.3 \times 5.3 \text{ mm}^2$ with one RDL and 0.4mm pitch vertical interconnects that facilitates the connection between the top and bottom packages [2]. This 3D structure would have a compelling value

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proposition as an SiP design in applications where quick turnaround solutions are needed with a high degree of design flexibility for product implementation, while achieving the smallest height profile and package body size. These attributes are due to the utilization of the existing packaging infrastructure for the top package and the use of well established eWLB processes for the bottom package.

Alternatively, the top mold cap could be entirely removed and a passive-attach performed using a conventional SMT process directly to the bottom eWLB PoP with an interposer as depicted in **Figure 4**. This package fully passed JEDEC L3 reliability tests including 1000-hour TC-B, 1000-hour HTS, and uHAST 192 hours. The subsequent board-level reliability (BLR) evaluations showed no failures after a 300-cycle drop test and a temp-cycle-on-board (TCoB) of up to 950 cycles.

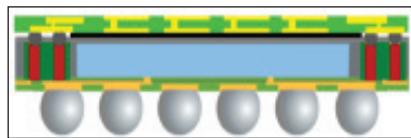


Figure 4: eWLB PoP with interposer.

More advanced 2.5D SiP package technologies used for high-end computing applications where CPU/GPU computing power requires high-bandwidth memory and a high data rate transfer to the processor, can benefit from eWLB technology to form the fine lines/spaces (L/S) routing that is needed for the high-speed I/O connection between the processor and memory. In such cases, eWLB eliminates the need for a costly interposer and is directly attached to the substrate, while also accommodating the space for IPDs and passives on the same substrate adjacent to the processor for better power delivery and voltage droop control [3].

MEMS and sensors are other applications where SiP packaging benefits from FOWLP technologies mainly for cost and form factor reduction. These devices have historically been packaged using traditional WB laminate technologies, where the more advanced FOWLP technologies such as eWLB, offer further and significant form factor reduction. An example device for a pressure sensor application is shown in **Figure 5**. The bottom eWLB package that houses the logic die measures at $1.6 \times 2.1 \text{mm}^2$, while the top pressure sensor in a WLCSP measures $1.2 \times 1.2 \text{mm}^2$.

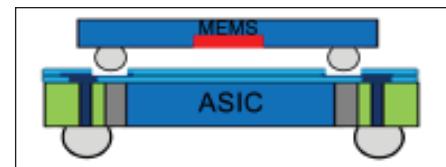


Figure 5: MEMS pressure sensor in an eWLB SiP.

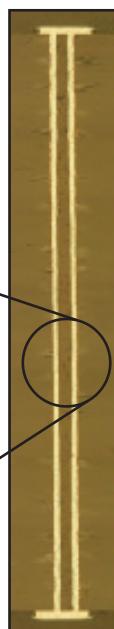
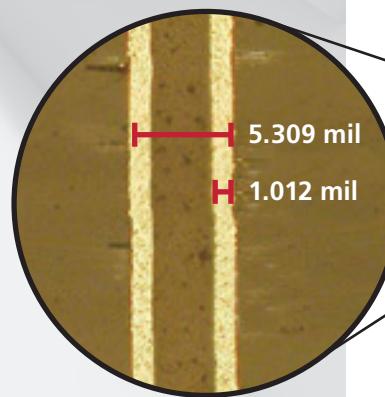
Miniaturization

In order to meet the market trends and keep pace with a higher level of integration, FC package technologies are also transformed to enable a higher level of heterogeneous device integration in the package. Here, the advancements are made through refinement of assembly processes and design rules to enable further reduction in keep-out-zones (KOZ) required for placement of various components, and through refinement of the molding process to achieve a lower mold cap height, and enhancement of the molded underfill (MUF) process to achieve filling through a smaller component stand-off height. Also, dual-sided assembly and packaging concepts are used to enable active device placement on both sides of the package to facilitate

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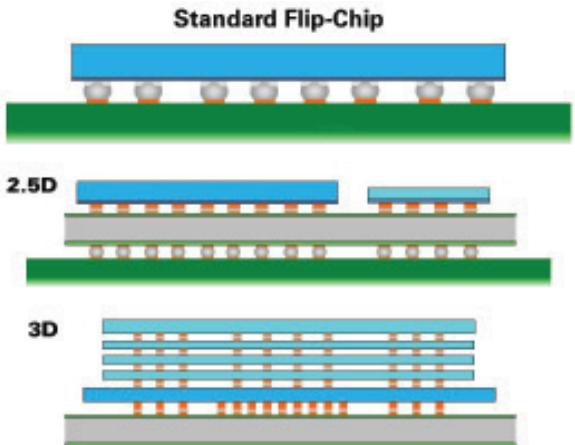


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further integration. **Figure 6** shows such a package concept utilizing dual-sided assembly, while the die located on the BGA side is also molded for further protection.

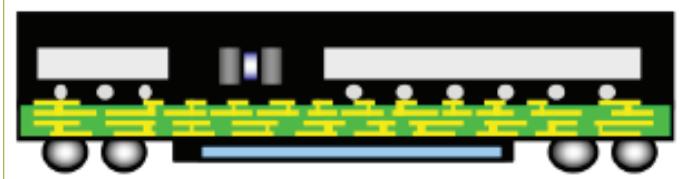


Figure 6: Dual-sided fcFBGA SiP.

Naturally, different molding technologies are used for the top side and bottom side molding processes; furthermore, X, Y, and Z-height constraints on the bottom side should all be considered as applicable to allow for a proper BGA attach process and the subsequent PCB mounting process. In this package process flow, the top side assembly is accomplished by solder paste printing of the passives' terminal pads, placement of passives by a chip shooter, flux dipping, and placement of FC bare dies, followed by a one-step reflow process.

Summary

Going forward, with the continuous push for higher integration and a smaller form factor at the end device level, it is expected that there would be a wider adoption of this modularized packaging concept as a means for more efficient and streamlined system-level assembly. This trend, if it holds true, will have technical and business implications for both outsourced semiconductor assembly and test suppliers (OSATS) and electronic manufacturing services (EMS).

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Advances in wire bonding to lower the cost of interconnect

By Ivy Qin, John Foley, Bob Chylak, Nelson Wong [Kulicke & Soffa]

The desire of providing more functionality at lower cost has driven the growth of the semiconductor industry since its inception. Wire bonding has been the work horse of the industry for the last 70 years and will continue as such. Other technologies, such as tape-automated bonding (TAB) and flip chip, have been developed. Among all the interconnect technologies, wire bonding is almost always the lowest cost and the most flexible interconnect solution. Therefore, it remains the most popular interconnect method. Around 85% of the semiconductor packages are wire bonded today. Lowering the cost of wire bonding technology is vital to the continuing growth of the semiconductor industry.

There are different cost models to compute the packaging cost. One model uses activity-based cost modeling, which decomposes the manufacturing process into a sequence of activities, and sums the cost of each activity [1]. Some of the main cost components are material, labor, time to complete the task, tooling cost, depreciation of the equipment, and cost due to yield loss. In this paper, we will discuss how advances in wire bonding help to further reduce the cost of packaging. We will look into several key areas including cost of material, cost of labor and time, and productivity and yield improvements.

Reduced material cost

Material cost is often the biggest cost component; it comprises more than 60% of the package cost in the example given in **Table 1**. **Table 1** shows the packaging cost comparison for a 500 I/O package using a 2-layer substrate. Material cost consists of 67% of the package cost for the Au wire example in **Table 1**. The two largest material cost contributors in wire bonded packages are the substrate and wire. There have been a few key advances in wire bonding to reduce the cost of materials. The most significant cost reduction is the introduction of Cu wire to replace the expensive Au wire. As the example in **Table 1** shows, by going to Cu wire, the package cost can be reduced from \$0.86 to \$0.69.

Not all the cost savings from the transition to Cu wire can be realized, however. For Cu wire bonding, the bonding process tends to be more challenging with lower yield and throughput, which is reflected in a \$0.04 increased wire bonding cost in **Table 1**. During the last few years, efforts in R&D to improve Cu wire bonding have come to fruition. For example, a more robust cover gas system inert gas delivery system was developed to reduce the level of oxygen to be well below 1%. During the ball formation process, Cu wire needs to be protected from oxidation because oxidized balls cause bonding issues, such as bond pad damage and ball lift. When the Cu ball is better protected from oxidation, it is easier to bond to it, resulting in a shorter bond time, higher bond strength, and less pad damage. All of these features translate to higher throughput and higher production yield, therefore lower cost. This is one example of how wire bonder hardware improvements have led to greater cost reduction.

Another example of cost reduction is the introduction of optimized Cu processes in the form of model-driven, response-based processes. Au wire bonding is relatively easy; there are normally two to three critical parameters that need to be optimized to achieve a robust process. Cu processes are much more complicated and often involve optimization of over 10 bonding parameters. By leveraging R&D, models were developed and implemented with simplified response-based inputs, such as the desired bonded ball diameter. The ProCu™ process for first bond and the ProStitch Plus™ process for second bond are processes that have demonstrated

	Au Wire Bonding	Cu Wire Bonding	Flip Chip
Wire	\$0.28	\$0.07	-
Wire Bonding	\$0.20	\$0.24	-
Bumping	-	-	\$0.15
Underfill	-	-	\$0.10
Other Package	\$0.08	\$0.08	\$0.20
Substrate	\$0.30	\$0.30	\$0.35
Total	\$0.86	\$0.69	\$0.80

Table 1: Packaging cost comparison for a 500 I/O CSP package with a 2-layer substrate. SOURCE: Prismark

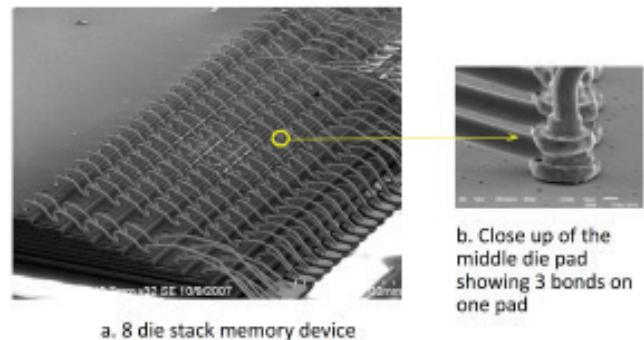


Figure 1: Multiple stacked die with stand-off stitch (SSB) bonds.

improvements in yield performance and throughput [2,3].

With today's advanced Cu wire bonding technologies and well-controlled manufacturing environments, the cost saving from transitioning to Cu wire are more fully realized [4]. For example, the average production yield is reported to be 99.88% for fine-pitch, high-density devices using 28nm wafer technology (source: ASE).

NAND memory is one area in packaging that has not adopted Cu- or Pd-coated Cu wire bonding due to a few challenges. The bond pads on memory devices are thin, usually only 0.6µm. This thin pad coupled with low-k dielectrics makes Cu wire bonding more challenging. NAND memory can be stacked vertically such as 4, 8, 16 or even 32 die stacks (**Figure 1a**). In this wire bonding configuration, the bonds are strung or cascaded down the stair case of devices using stand-off stitch bonding (SSB). In order to accomplish this

string of wires, first, a bump is bonded on the pad, and then a wire is bonded with its second bond placed on the bump. Lastly, the first bond of the next wire is bonded on top (see **Figure 1b**). This method has implications for Cu wire bonding. There are three bonds made on each pad compounding the forces to which the pad is exposed; this makes controlling pad damage even more difficult. An attractive alternative for these devices is Ag wire. Ag alloy wire is more expensive than Cu wire, but can still offer more than 80% cost savings compared to Au wire. Ag wire hardness is in between Au and Cu, so it is a bit easier to optimize than Cu wire; it may, therefore, be a good first step in reducing the cost of memory packages. Ag wire bonding has some issues that need to be overcome. Free air balls need to be formed in an oxygen-free environment similar to Cu. Forming repeatable and symmetric free air balls for Ag wire is not as easy as for Au wire and Cu wire, so the free air ball formation and bonding process recipe for Ag wire needs to be optimized differently. By leveraging technologies already developed for Cu wire bonding, the transition to Ag wire becomes a lot easier. **Figure 2** shows results for 15 μm Ag wire using ProAg™ (a K&S

proprietary process) for first bond and ProStitch Plus-Ag™ for second bond processes. All process specifications such as shear strength, pull strength, intermetallic coverage, and looping, met specifications with the same or better performance than Au wire.

For fine-pitch Cu wire production, Pd-coated Cu (PdCu) wire is normally used today. 15 μm PdCu wire is in limited production, and even 13 μm PdCu wire demonstrated robust process capabilities in R&D studies (**Figure 3**). This shows the maturity and capability of Cu wire

bonding today. PdCu wire is still 1.5X-2X the cost of bare Cu wire, so there is still significant cost savings by going to bare Cu wire. The main issues with bare Cu wire are the molded reliability and second bond robustness. With new high-reliability alloyed Cu wire and better second bond process, bare Cu wire for fine-pitch devices is a good possibility for future cost reduction [3,5].

Another material cost reduction is the development of lower cost substrates and lead frames such as pre-plated frame (PPF) QFN.

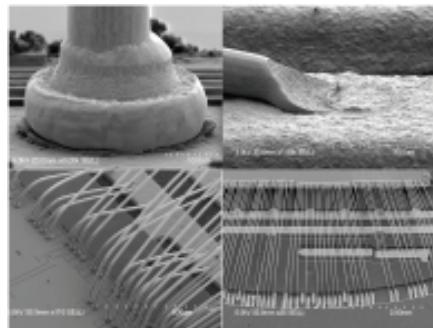


Figure 2: A fine-pitch 15 μm diameter Ag wire bonding process using ProAg™ and ProStitch Plus™ processes (32 μm bonded ball diameter).

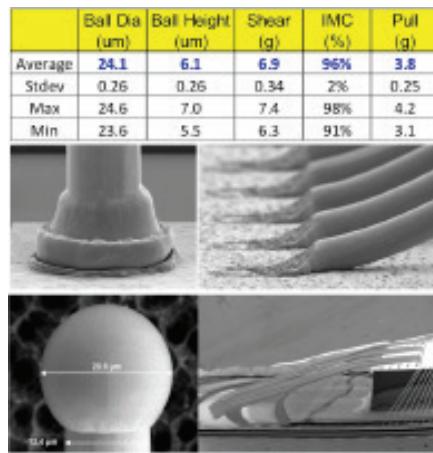


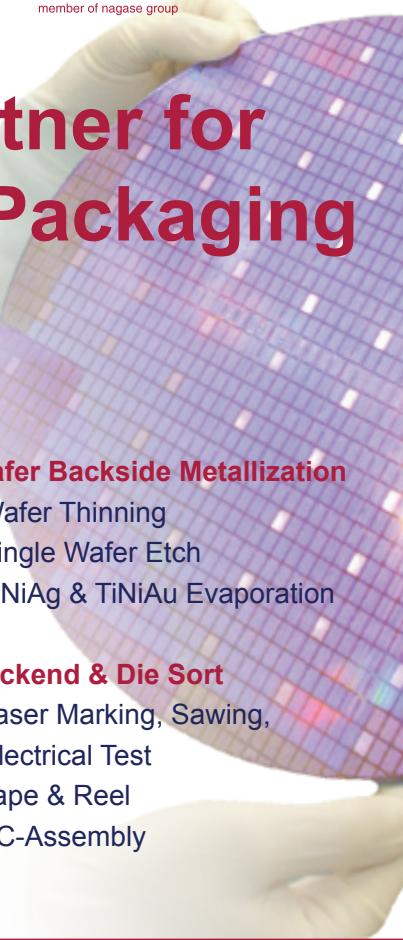
Figure 3: Fine-pitch 13 μm diameter PdCu wire bonding, using ProCu™ and ProStitch Plus™ processes with a 24 μm bonded ball diameter.

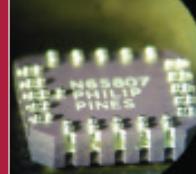
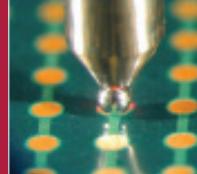


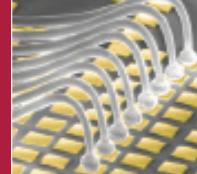
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PPF QFN offers reduced cost and simplified assembly by eliminating deflash and Sn-alloy plating steps. However, some of the low cost PPF QFNs are more difficult to wire bond due to thinner coatings, rougher surfaces and in some cases, inconsistent plating quality. In the example shown in **Table 2**, bare Cu wire produces 100% non-sticks, and PdCu wire can bond, but has unacceptable pull strength values. When using the new ProStitch Plus™ process, the bonding met specification with high pull strength and good Cu remains. New processes such as this, can enable a robust process and realize a material cost savings from both bare Cu wire, and low-cost PPF QFN.

Reduced time and labor

Time-to-market is the key to survival in our industry. New products need to be developed and produced in a short time period to capture market share. The major smartphone producers offer a new phone platform every two years. Wire bonding technology is an intrinsic fan-out technology because the wire loops connect

the I/O on a small chip to the lead fingers on a bigger substrate. The presence of wires makes the package design more forgiving and allows flexibility of the pad and substrate layout. In other words, wire bonding is more tolerant of less optimal chip and substrate designs as the bonding wire can be formed into different shapes to clear other wires and other components. These attributes can benefit the design cycle because of less stringent design requirements and the reuse of existing chip and substrate designs. Fan-out wire layouts can also accommodate more I/O counts and allow high-density devices (>1000 I/Os) to be wire bonded. This is normally done using a multi-tier pad layout as seen in **Figure 4a**. Die can also readily be put in a stack with wires interconnecting them (**Figure 4b, c**). These configurations enable more functionality in a small package size and provide a low-cost solution for advanced devices.

Another benefit from switching to Cu from Au wire is that the mechanical strength of Cu wire is much stronger. This increased strength enables taller loops and long wire spans needed for high I/O count, multi-tier devices. However,

programming these high-density devices can be time consuming and may require design iterations. 3D looping software has been in development and is in the early phase of product introduction. The new 3D looping

tool has two components. The front-end component is a 3D design, visualization and clearance check tool that is embedded in a CAD program. It can design the multiple loop tiers according to the package requirements, such as the number of pad rows, and the maximum allowable package height. The loop profile for each wire is automatically designed based on its desired shape. A clearance check is then performed for the whole package. Wires that are too close are flagged for further optimization. The back-end component is the software on the wire bonder that calculates the looping motions to reproduce the wire loops designed and verified during the package design phase. 3D looping software helps the designer to check package performance, optimize pad layout and substrate layout, shorten the design cycle, and achieve a more optimal wire bonded package. **Figure 5** shows a complicated wire bonded package that was designed using 3D looping software. With the 3D programming capability of realistic and reproducible loops in the CAD program, and the looping software on the bonder to produce the loop shape as designed, the development cycle time can be reduced by half, and product yield can also be improved with less yield loss caused by wire shorts.

As mentioned before, the substrate cost can be a significant part of the package cost. Substrate costs can be reduced by having fewer layers. Wire bond loops can replace wiring in the substrate to reduce the number of layers in the substrate as well as the cost. The added wire loops increase the complexity of the package, which can be mitigated by using more optimal loop shape designs.

The cost of the devices can be reduced if the time to produce each unit is shorter. By improving the net UPH (units per hour) by 20%, packaging cost can be reduced by about 7% when using Cu wire. Optimal processes can provide a higher UPH too. ProCu™ and ProStitch Plus™ processes have demonstrated over 20% UPH gain because of shorter bond time and fewer assists [3].

Another example of UPH improvement is the multi-stitch process for stacked die packages as shown in **Figures 1** and **4c**. Traditional wire bonding processes break the wire after each second bond and form another free air ball for the next loop. For multi-stacked die with multiple pads connecting to the same lead, multi-stitch processes use one wire chain to connect multiple pads to the lead. This process can shorten the wire cycle by 15% and more. It also reduces the number of times the pad is bonded.

Process type	Traditional 2 nd bond Process		New ProStitch Plus Process	
Wire type	Bare Cu	PdCu	Bare Cu	PdCu
Non Stick on Lead	100%	0%	0%	0%
Pull Average (g)	4.11	5.60	5.96	
Pull Minimal (g)	2.24	4.70	5.16	
Pull Std Dev (g)	1.04	0.39	0.45	
Pull Cpk (Isl=2.5)	0.52	2.65	2.56	
After pull test Cu Remain	0% Cu remain	0% Cu remain	>80% Cu remain	>80% Cu remain

Table 2: Comparison of wire type and process type for low-cost PPF QFN with 20µm wire.

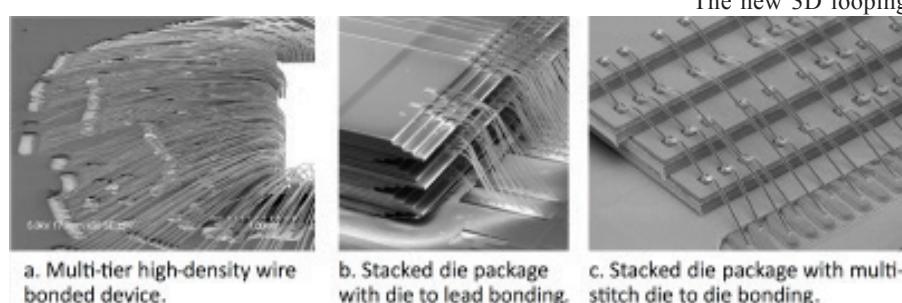


Figure 4: Complex wire bonded packages with multi-tier and multi-die stack configurations.

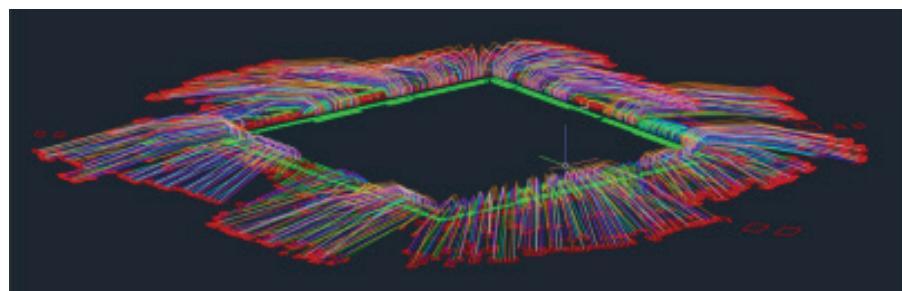


Figure 5: Offline 3D looping software-designed wire loops (>1000 wires).

Improving wire bonding yield

Improving wire bonding yield is another effective way to reduce the package cost. An advanced recovery tool on the wire bonder, such as the automatic recovery from short tail and non-stick on lead, can reduce the yield loss caused by operator error and improve net UPH. The more robust processes and better oxygen-free environment have all demonstrated improved package yield. Machine-to-machine portability is also important for good production yield. Because one recipe is normally used across a large population of machines, bonder portability can ensure optimal performance on all of the machines. A lot of effort has been expended to develop tools on the bonder to automatically calibrate key subsystem performance. One patented technology performs on-bonder ultrasonic current calibration to ensure that the same ultrasonic energy can be output from each wire bonder. With all these processes and tools, wire bonding yield can be maintained at 99.9%, even with the most complex packages.

Summary

Wire bonding is a mature technology that makes more than 10 trillion bonds each year. New technologies continue to extend the life of

wire bonding by further reducing the cost and providing more capability. For cost reduction, alternative wires such as Pd-coated Cu wire, Cu alloy wire, Ag alloy wire, and lower cost substrate technology, such as PPF QFN, should be considered. Advanced equipment and process technologies such as those discussed here can help retain the material cost savings by ensuring robust and fast bonding processes. For today's advanced node devices with complex looping requirements, the 3D looping tool can help shorten the design cycle, reduce costly redesign, and improve wire bond yield, which in turn, enables wire bonding more complicated advanced node devices at a lower cost.

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Biographies

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Advancing fan-out wafer-level packaging for mobile applications

By Steffen Kroehnert [NANIUM S.A.] and Long-Ching Wang, Lijuan Zhang [Marvell Technology Group Ltd.]

I

In the second half of 2013, Marvell Technology Group Ltd. and NANIUM S.A. created a semiconductor supply chain collaboration that has continued to prosper. Understanding the need for close collaboration along the supply chain, co-designing and co-developing solutions are essential elements to achieving time-to-market, quality, and cost targets dictated by the extremely fast and volatile semiconductor and technology markets in which both companies are engaged.

Focusing on mobile and wireless communications markets, but also looking forward to the needs of upcoming Internet of Things/Internet of Everything (IoT/IoE) applications, both companies identified fan-out wafer-level packaging (FOWLP) as a promising packaging technology suitable to better serve those needs compared to other packaging technologies, such as organic laminated substrate-based flip-chip ball grid array (FCBGA) and lead-frame-based quad flat no-lead package (QFN). The substrate-less fan-out wafer- and panel-level packaging (FOWLP/FOPLP) technologies developed during the last decade show great potential. The FOWLP market is forecasted to be \$200M in 2015 with 30% CAGR in the coming years [1]. This growth can also be explained by the wide design flexibility and system integration capability of FOWLP technologies, which provide a small, thin package performing as an active interposer.

A deeper look into the various potential semiconductor applications, namely for mobile, wireless communications and IoT/IoE devices, and their packaging requirements have been discussed in previous *Chip Scale Review* articles [2,3]. A driving force and significant advantages of FOWLP, namely embedded wafer-level ball grid array technology (eWLB) invented by Infineon Technologies AG, are the superior electromagnetic performance of the package compared to similar package types, as well as offering higher levels of dense system integration.

An eWLB package has very short connections between die pads and the package I/Os. This results in extremely low package parasitic values, especially in terms of inductance, and a good matching network for high-frequency applications with superior electromagnetic performance and low loss. Because of the much lower package parasitics compared to laminate substrate or lead-frame-based packages, eWLB offers excellent RF performance. Applicability of the eWLB package is proven in high volume for high-frequency applications. It has become a standard package for RF/baseband system-on-chip (SoC) for the mobile communication market and is taking over market share for automotive and non-automotive millimeter wave and radar applications [1]. Higher frequencies up to 80GHz millimeter-wave radar applications have been demonstrated [4]. The feasibility of packaging solutions up to 120GHz is also under investigation.

For modules that need superior electromagnetic performance and dense system integration, especially where a high level of miniaturization is required, the eWLB-based wafer-level fan-out (WLFO) technology platform, such as that offered by NANIUM, shows the greatest potential. Desired technology features and technology bricks are either available in the eWLB tool box or in development. Already developed WLFO-based 2D constructions, like wafer-level system-in-package (WLSIP)

with embedded active multi-die, discrete passives, already packaged components, sensors and optical elements, and WLFO-based 3D constructions, such as wafer-level package-on-package (WL3D/WLPP), can achieve the highest integration density. Several WLSIP products, of low and medium complexity, are already in volume production. An increasing number of products with higher levels of system integration are getting qualified and ready for volume production.

NANIUM's business model promotes long-term collaboration with intensive data and know-how exchange in the day-to-day work between its R&D engineers and the customers' counterparts. This fosters success and allows for efficient co-design and co-development of new products that result in first-time-right and fast time-to-market. After the first products have been developed together, development of new products comes about more quickly. As with Marvell, the collaboration started with one product, but today has more than 10 products that have been, or are currently, co-developed and qualified for volume manufacturing.

We have chosen the first joint development product by Marvell and NANIUM as an illustration of a successful collaboration. The product, the Marvell power management unit PM820 with integrated audio codec, is shown in **Figure 1** with views from the top side,

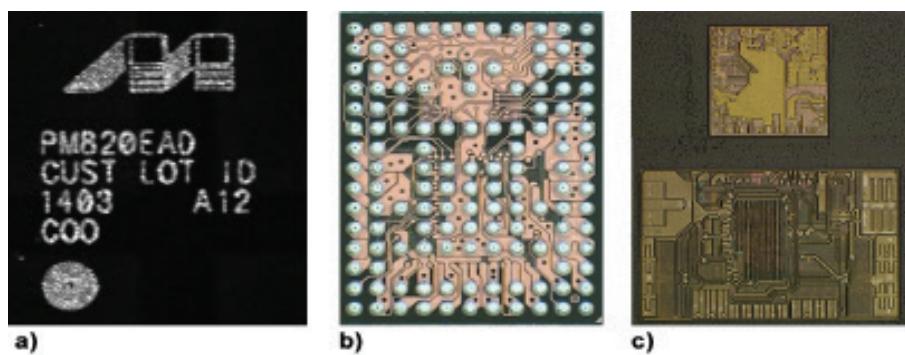


Figure 1: Product PM820, PMU + audio codec dies integrated side-by-side in a WLFO package
a) package top side, b) bottom side with BGA solder balls, and c) inside with two different dies embedded.

bottom side and inside. Inside the unit are two different dies, a power management unit (PMU), and an audio codec, side-by-side integrated in an WLFO-based WLSiP package. Some of the design features include: 1) A single RDL for competitive manufacturing cost; 2) A 6.3x4.7mm² package size at a 0.765mm thickness including the BGA solder balls; 3) 133 package I/Os at 0.400mm BGA pitch compatible with a low-cost standard PCB; 4) No underfill required to achieve specified board-level reliability; and 5) Low-temperature cure polyimide (PI) dielectric passivation layers.

The design described above achieved some NANIUM firsts and got qualified for high-volume manufacturing in a very short timeframe. Firsts include: 1) Cu-RDL line/space width of 10µm/10µm; 2) First wafer-level system-in-package (WLSiP) with two different dies in high-volume manufacturing; and 3) Laser grooving for separation of 28nm CMOS technology node based dies.

To meet the tight time-to-market expectations, NANIUM needed an approach that was fast and flexible to answer the customer needs. Always pushed by the supply chain to be faster and even more flexible, NANIUM had an aggressive time-to-samples schedule — just two weeks after initial set up, as well as accelerated manufacturing cycle times. While keeping a strong engineering focus to identify and reduce risks while achieving the most reliable package construction and process for volume manufacturing, the time from project start to engineering samples to qualification and ramp-up to a volume of four million components-per-month was achieved in less than four months. Reasonable volume of that product continued to be produced through mid-2015.

This speed required new ways to learn and stabilize manufacturing and yield in the line. The ability to scale to a high volume very quickly while keeping costs low was important to overall success. Other key elements of a successful collaboration included: 1) Short response times; 2) Effective data provisioning and reporting; 3) Profound design assessment and recommendations with short iteration loops; and 4) Joint development of the optimum solution.

The result was seen in the August 12, 2014 announcement by Marvell [5] that Samsung would be using its ARMADA

mobile LTE solutions in Samsung's new 4G LTE Smartphone and Mobile Hotspots. The PM820 example used in this article was also specifically noted in the announcement and is discussed in more detail below.

PM820: WLSiP package construction. The WLFO process basically consists of reconstitution and redistribution. After the known good dies (KGD) are ground to the required thickness still in wafer format and

separated from their original wafer, they are picked and placed face-down on the thermal release tape on the temporary mold carrier in the configuration required. In this case, it is a WLSiP configuration with two different dies: a PMU and audio codec of significantly different sizes side-by-side, as seen in **Figure 2**. This configuration is then overmolded with epoxy mold compound in a compression mold process resulting in the new self-sustaining reconstituted round

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panel as shown in **Figures 3** and **4**. That round panel then gets processed in the thin-film line with dielectric layer 1 (DL1), Cu-RDL, dielectric layer 2 (DL2) and Cu-UBM before it is sent to laser marking, solder ball attach, and package singulation from the reconstituted round panel (**Figure 5**).

PM820: WLSiP package reliability. Reliability of system-in-package (SiP) has always been a challenge because of the heterogeneous integration of different elements with different interconnect

technologies in 2D and 3D construction due to the large number of interfaces, different materials and their coefficients of thermal expansion (CTE), complex process flows, and temperature budget applied during processing. This is also challenging for WLSiP, but seems be less critical on account of the thin-film processing used instead of wire bond and flip chip, and the usually smaller package dimensions. The package design and bill of materials of the PM820 WLSiP, namely selection of the solder ball alloy and the decision to apply an under bump metallization (UBM), was optimized to compromise between temperature cycling on board (TCoB) and drop test (DT) reliability requirements—the most significant board-level reliable (BLR) tests for products targeting the mobile market.

The positive effect of an UBM on BLR is well known. However, applying UBM requires extra process steps. Therefore, both cases, UBM and non-UBM, have been investigated to find out the level of the improvement achievable with UBM for this specific product. A summary of the BLR tests

for the UBM case can be seen in **Table 1**. The TCoB according to the JEDEC standard (-40 to 125°C), but customized in terms of cycling speed (2cy/h instead of the typically applied 1cy/h) with pass criteria: <5% failure rate @ 500x, passed with the first fail >600x. DT according to JEDEC JESD-22-B111 with pass criteria: failure rate <30% @ lowest drop count >700, passed with the first fail at >1,000 drops. **Table 2** shows the considerably worse results that were achieved for the non-UBM case.

For PM820 WLSiP volume manufacturing, it was decided to apply UBM. DT passed with no fails before 1,000 drops. That is 10x better than the non-UBM case. The Weibull projection of the DT comparing UBM and non-UBM package version is shown in **Figure 6**.

Increasing the number of mobile applications in WLFO

So what is next in advancing FOWLP for mobile applications? We see the beginning of widespread acceptance of FOWLP technology into different markets and applications. Superior electrical performance due to very short

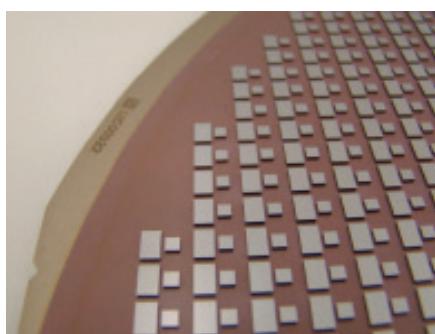


Figure 2: Panel reconstitution, with dies placed face-down on thermal release tape on a temporary mold carrier (dummy dies).

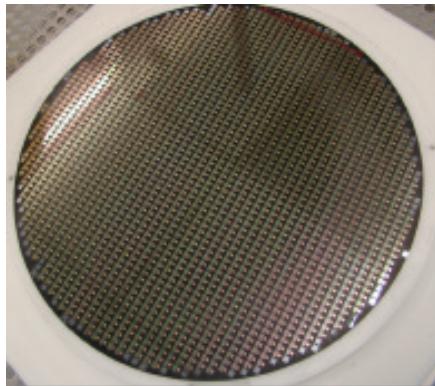


Figure 3: A fully populated reconstituted 300mm round panel after molding (productive dies).

TEST	SPECIFICATION	PASS CRITERIA ACHIEVED
Temperature Cycling on Board (TCoB)	Customer specific -40°C / +125°C, 2cy/h	< 5% failure rate @ 500x FF>600
Drop Test (DT)	JEDEC JESD-22-B111	0 Fails @ 1,000 drops and Failure rate < 30% @ lowest drop count > 700

Table 1: Board-level reliability of WLSiP with UBM.

TEST	SPECIFICATION	PASS CRITERIA ACHIEVED
Temperature Cycling on Board (TCoB)	Customer specific -40°C / +125°C, 2cy/h	< 5% failure rate @ 500x FF>500
Drop Test (DT)	JEDEC JESD-22-B111	0 Fails @ 100 drops and Failure rate > 30% @ lowest drop count < 700

Table 2: Board-level reliability of WLSiP without UBM.

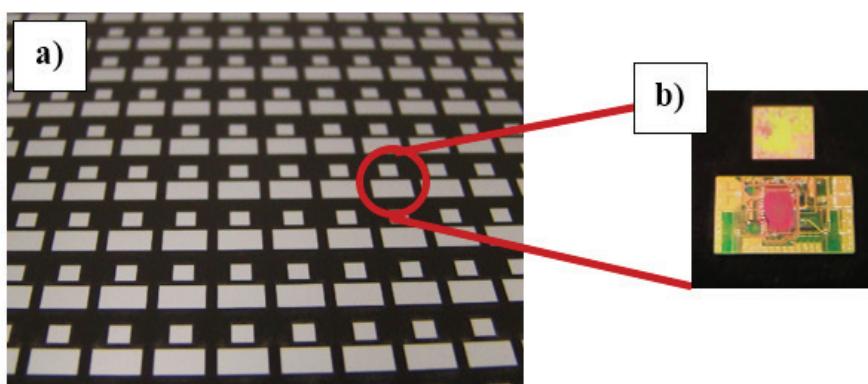


Figure 4: A reconstituted wafer after wafer molding and removal of the temporary mold carrier and thermal release tape; the active side of the die is getting exposed for thin-film processing: a) dummy dies, and b) productive dies.

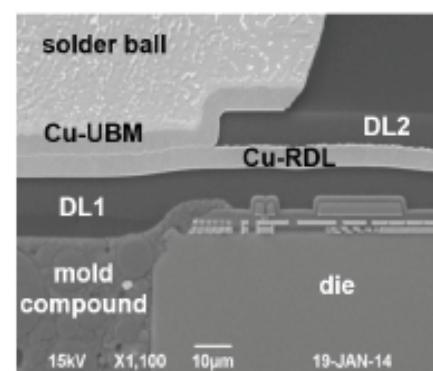


Figure 5: Cross section of the final package showing the die, molded fan-out area, RDL-stack with UBM, and solder ball.

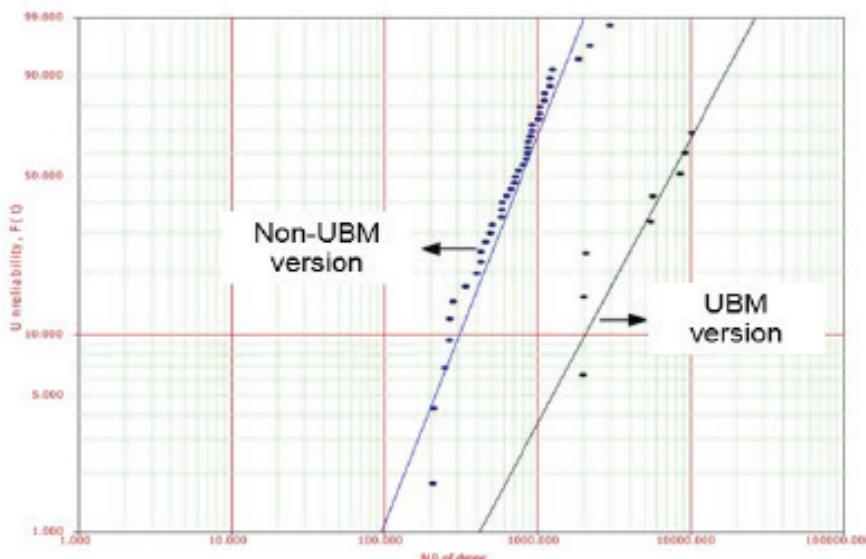


Figure 6: Weibull projection of the PM820 WLSIP drop test for UBM vs. non-UBM package versions.

connections between die pads and package I/Os, as well as the small, thin package outline is inherent in WLP. Providing a fan-out zone to accommodate the required number of I/Os within the required BGA pitch on small SoCs was the original driver of the development of FOWLP technologies in order to overcome the space limitations of conventional fan-in WLP (FIWLP) and WLCSP. Today, the manifold opportunities for dense system integration in a small thin wafer-level package provided by FOWLP technology become increasingly important and attracts an increasing number of customers and variety of applications. This is especially true for the eWLB-based WLFO technology platform because of its system integration-favorable package construction concept, process flow and manufacturing cost efficiency, mainly in batch processes on large format round or rectangular panels.

The use of FOWLP for its products is a key strategy for Marvell. Other mobile and wireless market products we see using eWLB-based WLFO today or in the near future include: 1) PMU; 2) audio codec; 3) GPS; 4) PMIC; 5) RFIC; 6) Bluetooth®; 7) NFC; and 8) WiFi.

Integration for miniaturization and performance improvement is another strategic use of eWLB-based WLFO. For example, about half of the 10 products Marvell is coproducing with NANIUM for package design, development and manufacturing are multi-die products, combining different functionalities in the same package.

In conclusion, we believe that FOWLP technologies in general, and eWLB-based WLFO specifically, are packaging technologies that are enabling efficient design and faster

time-to-market for the growing number of mobile, wireless communications and IoT/IoE devices. Co-development efforts such as these by Marvell and NANIUM are the wave of the future where packaging becomes a chief enabler of innovative product design.

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Assembly design kits: the next big thing

By John Ferguson, Tarek Ramadan [*Mentor Graphics*]

Traditional system-on-chip (SoC) design processes contain fully-qualified verification methods for integrated circuit (IC) designs in the form of process design kits (PDKs) from the foundries. IC designers use these PDKs to not only reduce their risk, but also improve overall productivity by implementing repeatable, proven verification techniques. Chip design companies and outsourced semiconductor assembly and test companies (OSATs) have no corresponding sign-off verification process to ensure that an IC package meets manufacturability and performance requirements.

The lack of qualified verification processes puts package designers at a significant disadvantage compared to their IC design counterparts. Package die are often produced using die from multiple processes and multiple foundries, which not only raises the level of complexity, but also increases the need for a process that ensures these disparate products can be manufactured within a single package. Package designers must often work with poorly-documented and/or inconsistent processes each time they submit a package design. In addition, the new class of packages now coming into the market enhances the interactions between the layers, so there is no clear separation between the traditional die and package.

Package design strategy

By placing ICs into protective physical packages (IC packages), not only are the devices better protected against damage and exposure, but downstream users can more easily manipulate them during assembly onto printed circuit boards (PCBs). There are many types of IC package designs, some with standardized requirements that are registered with trade industry associations such as JEDEC and Pro Electron, and others that are proprietary designs made by one, or only a few, OSATs.

The need for a formal package verification strategy. The challenges of verifying IC packages are numerous. Die design teams often have very different goals from the package design team, which creates unforeseen integration issues. Chips often come from different foundries, and are verified using different processes, making package failures hard to identify and fix. There isn't even a formal verification process to ensure that the connectivity from a single die to the ball grid array (BGA) of the package is correct. The industry simply doesn't have good characterization of package processes and requirements, leaving chip designers and OSATs to muddle through. Not that the industry isn't trying. OSATs have built and manufactured packages for years and developed a variety of tools to help in the process. However, they must write their own rules for each assembly, with no reference sign-off deck that ensures the manufacturability and performance of the package. In addition, OSATs rarely hold their customers to a hard and fast rule deck like foundries do.

The purpose of an assembly design kit (ADK) is similar to that of the PDK—ensure manufacturability and performance. What makes that happen, in both PDKs and ADKs, are things like standardized rules that ensure consistency across a process, qualified tool flows, interface formats, input/output formats—in short, everything a designer needs for successful design—in the form of tested, qualified, and proven methods that produce working designs. An ADK could provide many benefits to the industry: reduced risk of package failure, increased packaging business, and increased use of 2.5/3D packages.

Why existing verification flows cannot be used. There are multiple reasons why IC-centric verification solutions do not work for package verification. Physical verification (PV) tools rely on GDSII, or similar layout formats, for their inputs. Because these formats contain no data

about a geometry's vertical placement, that information is inferred through layer mapping and the use of typical layer-naming conventions. For example, PV tools infer that metal2 is vertically higher than metal1 and lower than metal3, and establish the layers' electrical connectivity through the appropriate via layers. All geometries mapped to the same layer are considered to be coplanar, and any geometries that overlap or abut are treated as if they are a single polygon, as they will be merged during the mask generation process. However, there is generally little to no commonality in layer mapping from one foundry to another, and in some cases, even from one node to another at the same foundry. The design rule checking (DRC) tool would interpret the geometries located on the same layer as the geometries from the package redistribution layer (RDL) as coplanar, and consider those geometries as if merged, when in reality there is a significant vertical displacement between them. For this reason, traditional IC PV tools do not easily lend themselves to this kind of packaging task.

An entirely new approach is needed for sign-off quality physical verification of packages. One component of an ADK would be sign-off checks for the package layers and interacting die layers, without reference to any kind of layer mapping. Such checks would include ensuring that connections are intact within the package (die-to-die) and from the package to the outside (die-to-BGA). Electronic design automation (EDA) vendors that support the ADK would need to enhance their tools to implement these checks and enable debugging of any errors.

Next is validation of the electrical connectivity across the assembly. In the IC space, designers rely heavily on standards, such as SPICE—a standard that represents connectivity all the way down to each individual device component. By associating device components with their corresponding

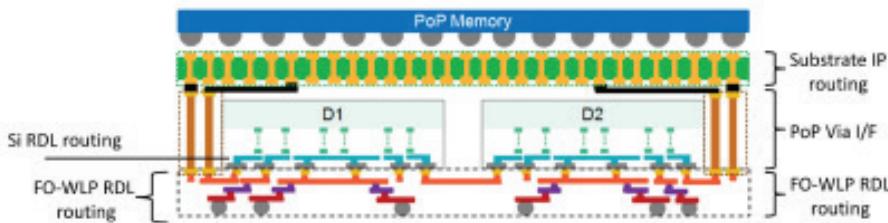


Figure 1: Fan-out wafer-level package design.

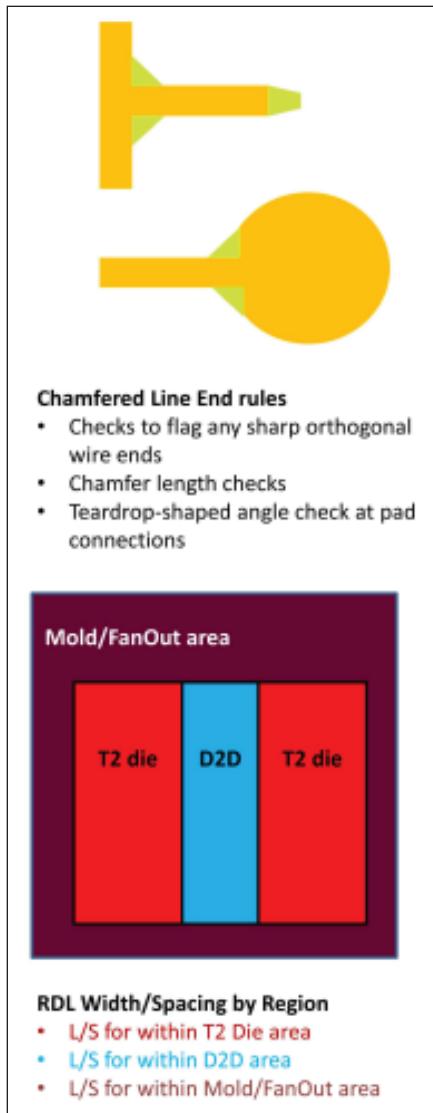


Figure 2: Design rule checks in an assembly design kit target specific geometries found in package designs.

device models, and tracing their connections to all other devices in the circuit, they can perform electrical simulations. Unfortunately, despite being called a “netlist,” SPICE does not actually contain direct information on connections. Instead, it is a list of devices and device pins from which connections are inferred. This inference

does not work in the package assembly space because package design tools do not deal with data down to the transistor level. With no true devices, a traditional layout vs. schematic (LVS) tool relying on a SPICE-style netlist has nothing to check in a package. Other file formats, such as AIF [1], are used to represent the connections from the pins of one die to its surroundings.

Envisioning an ADK

So, what should an ADK include? Obviously, it must include both physical verification and extraction sign-off solutions for a start. A verification engineer must be able to verify each component independently and at the interfacing level (die-to-die, die-to-package, etc.). All processes should be independent of any specific design tool or process used to create the assembly. In addition, a complete ADK must work across both IC and packaging domains, meaning the flow must support multiple formats—IC layout design formats (LEF/DEF, Open Access, and GDSII/OASIS), as well as package formats (AIF, CSD, MCM, SiP, ODB++, and Gerber)—although existing conversions between formats may help simplify the flow. In fact, there is really nothing in the package space that can't be represented in IC space formats and vice versa. In other words, we do not need new standard formats—we need existing tools to expand their format capabilities, or we need to validate format translation tools. Finally, all of these verification processes must be validated by the OSAT.

To prove the feasibility of an ADK that enables packaging rules independent of any specific package design or die process, Mentor Graphics collaborated with an electronic design company and an OSAT to develop a prototype ADK for 2.5/3D IC packages. We selected a chip-scale package (CSP) design, which must be a single-die, direct surface-mountable package [2], with an area no greater than 1.2 times that of the die, and a ball pitch maximum of no more than 1mm. Initial steps

included the definition of requirements and responsibilities, and the development of specific checks and flows to create a method for verifying a fully-stacked system that included both DRC and LVS performed on each component independently and at the interfacing level, as well as support for assembly and stress rule checking.

The actual design was a side-by-side package using an embedded fan-out wafer-level packaging (FO-WLP) technology to support multi-die integration (**Figure 1**). This wafer-level package (WLP) is a type of CSP that enables the IC to be attached face down to the PCB using conventional surface mount technology assembly methods. The chip's pads connect directly to the PCB pads through individual solder balls. The die may be mounted on an interposer on which pads or balls are formed, or the pads may be etched or printed directly onto the silicon wafer, resulting in a package very close to the size of the silicon die. WLP technology differs from other BGA, leaded, and laminate-based CSPs, in that no bond wires or interposer connections are required. The main advantages of the WLP are a small package size, a minimized IC-to-PCB inductance, and a shortened manufacturing cycle time.

Defining requirements and responsibilities

The OSAT determined what was needed to perform DRC and LVS comparisons on packages, and created design rules addressing package-specific requirements. For example, package wire widths vary depending on whether they are over die, between die, or completely outside the die, so rules were needed to govern the design of wires in the package, including specifics such as size, distance, etc. Design rule checks were then implemented to ensure all requirements were satisfied in the package. Typical checks (**Figure 2**) included:

- Verify DRC and LVS across interface boundaries between package and dies;
- Perform DRC checks on RDL layers
 - Avoid orthogonal/90° angles on RDL geometries
 - Area-dependent line width and spacing (L/S) checks; and
- Perform metal density checks
 - Fill check for floating metal fill pattern and/or biased metal plane with slotting
 - Local-based density checking.

The OSAT also wrote rules for the types of elements and configurations permitted in the package:

- Assembly rule checks
- Die-to-die edge;
- Die-to-package edge;
- Die-to-package alignment;
- Corner rules;
- Landside caps to BGA spacing; and
- Mechanical stress checks
- Die-package fan-out ratio.

The Calibre® 3DSTACK tool was used to implement the package verification. Syntax in the tool was enhanced to combine the two rule sets and provide rule checking capabilities (**Figure 3**). To eliminate layer mapping issues, the tool automatically re-assigns all layers for each component (die, interposer, packaging layers, etc.) to separate layers. This reassignment must be done per placement to avoid problems caused by multiple placements of the same die. However, reassignment alone is insufficient. DRC is typically coded for the process layers available in a chip die, but because these layers are now

all reassigned to unique names, the implication is that assembly checking will always require a unique rule file specific to the die layers in the specific configuration. Instead, the tool provides the rule writer a level of abstraction to indicate types of layers (pads, bumps, RDL, etc.), so rules can be associated with these types.

When the Calibre 3DSTACK process is run, the platform can associate the specific layers of each die or package component to the appropriate layer type. Knowing where each component interacts with others allows the tool to automatically regenerate a detailed set of checks between the appropriate layers from each component, independent of how the design is configured, how many dies are placed, or for what processes those dies are targeted.

For LVS, the first challenge was the absence of a traditional source netlist for a package. We determined that the de facto industry substitute, a common spreadsheet format, was satisfactory (**Table 1**).

Figure 4 shows the ADK LVS process. LVS connectivity through the package RDL is verified by confirming the

physical connections between external pins to the die. To enable designers to check the connectivity of a standalone package design (no devices), as well as improve the existing solution for capturing the netlist (connectivity intention) for a fully-stacked system (IC + package), virtual die are generated from the spreadsheet netlist pin coordinates.

The Calibre 3DSTACK tool can perform a kind of black-box connection checking without going to the transistor level. Connections from the package source netlist, including those from package formats, can be compared to a black-box SPICE netlist extracted from the assembly layout. The physical connections through a passive interposer or package level RDL can be verified for shorts or opens to the pin labels to which they connect in the layout.

Using the System Netlist Generator tool associated with the Calibre 3DSTACK tool, we can combine the extracted black-box netlist with the previously-generated transistor-level netlists for each die, forming a full transistor-level netlist for the entire assembly. This netlist can be used for detailed SPICE analysis or other

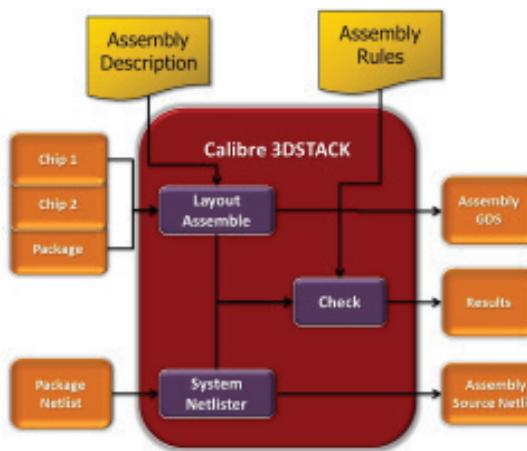


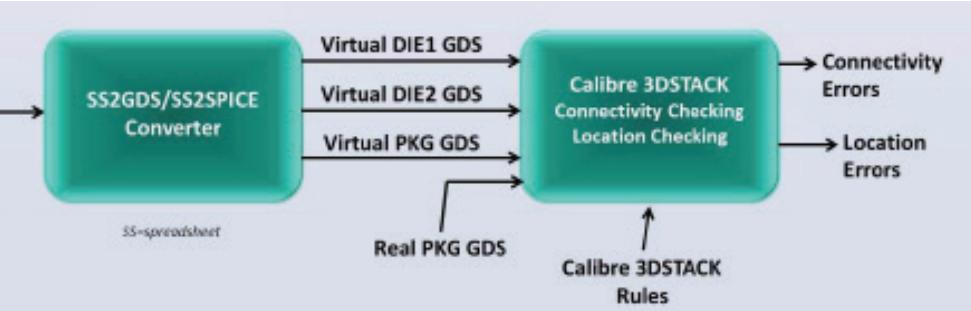
Figure 3: The Calibre® 3DSTACK tool is used to process the package-specific rule checks and circuit comparison.

#REFDES	PIN_NUMBER	PIN_X	PIN_Y	PIN_NAME	NET_NAME
DIE1	core_ubump_1	3062	11952	sig_1	NC_1
BGA	L35	4802	11618	L35	CHAIN1_IN
DIE1	core_ubump_2	3274	11952	sig_2	CHAIN1_IN
DIE1	core_ubump_3	3486	11952	sig_3	CHAIN1_IN
DIE1	core_ubump_4	3698	11952	sig_4	CHAIN1_4_5
DIE1	core_ubump_5	3910	11952	sig_5	CHAIN1_4_5
DIE1	core_ubump_6	4122	11952	sig_6	CHAIN1_6_7
DIE1	core_ubump_7	4334	11952	sig_7	CHAIN1_6_7
DIE1	core_ubump_8	4546	11952	sig_8	CHAIN1_8_9
DIE1	core_ubump_9	4758	11952	sig_9	CHAIN1_8_9
DIE1	core_ubump_10	4970	11952	sig_10	CHAIN1_10_11
DIE1	core_ubump_11	5182	11952	sig_11	CHAIN1_10_11
DIE1	core_ubump_12	5394	11952	sig_12	CHAIN1_12_13
DIE1	core_ubump_13	5606	11952	sig_13	CHAIN1_12_13

Table 1: A spreadsheet serves as the package source netlist in the assembly design kit.

#REFDES	PIN_NUMBER	PIN_X	PIN_Y	PIN_NAME	NET_NAME
DIE1	core_ubump_1	3062	11952	sig_1	NC_1
BGA	L35	4802	11618	L35	CHAIN1_IN
DIE1	core_ubump_2	3274	11952	sig_2	CHAIN1_IN
DIE1	core_ubump_3	3486	11952	sig_3	CHAIN1_IN
DIE1	core_ubump_4	3698	11952	sig_4	CHAIN1_4_5
DIE1	core_ubump_5	3910	11952	sig_5	CHAIN1_4_5
DIE1	core_ubump_6	4122	11952	sig_6	CHAIN1_6_7
DIE1	core_ubump_7	4334	11952	sig_7	CHAIN1_6_7
DIE1	core_ubump_8	4546	11952	sig_8	CHAIN1_8_9
DIE1	core_ubump_9	4758	11952	sig_9	CHAIN1_8_9
DIE1	core_ubump_10	4970	11952	sig_10	CHAIN1_10_11
DIE1	core_ubump_11	5182	11952	sig_11	CHAIN1_10_11
DIE1	core_ubump_12	5394	11952	sig_12	CHAIN1_12_13
DIE1	core_ubump_13	5606	11952	sig_13	CHAIN1_12_13

Figure 4: The LVS process uses virtual die to examine package connectivity and circuit location in standalone mode.



electrical analyses, such as reliability checking for electrostatic discharge (ESD) or electromigration (EM) with tools like the Calibre PERC™ tool.

Results

Using the Calibre 3DSTACK tool, the OSAT created a rule file for the FOWLP process that can be used by any designer targeting this package technology at that OSAT, regardless of what processes were used for the dies, or how many dies are in the package. The rule file checks the manufacturing constraints of the package RDL and the die-to-die constraints, and verifies the connectivity through the package from die-to-die and die-to-BGA. It is entirely independent of any specific design tool used to generate the package. Designers applying this rule file can leverage traditional Calibre functionalities for debugging and review.

Summary

Beginning with physical and electrical verification, Mentor Graphics collaborated with a design company and an OSAT to develop and test the concept of an ADK. Initial results show that while creating an ADK is a non-trivial effort and requires cooperation and collaboration between design houses, OSATs, and EDA vendors, using an ADK can reduce the risk of package failure, while also reducing turnaround time for both the component providers and OSATs.

But a design kit is much more than just basic sign-off requirements. Designers need validated technology files for the design creation tools, just like we have for place-and-route and custom design tools in the IC space. These files usually coincide with the development of a reference flow by the foundry. The IC world also has the concept of intellectual property (IP) cells that can be reused in many designs. Perhaps the package assembly world should consider die-level IP that can be reused in specific design packages. Future work might include thermal and/or stress sign-off solutions, as well as design-for-test strategies. Such strategies could help trace back to the root cause of failure should an assembled package fail.

The initial ADK has already proven to be a valuable resource for the OSAT and its customers. A fully-realized ADK could provide a standardized process that both chip design companies and OSATs can use to ensure the manufacturability and performance of IC packages.

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Temporary bonding and thin wafer handling strategies for semiconductor device processing

By Ramachandran K. Trichur, Tony D. Flaim [Brewer Science, Inc.]

Consumer electronics such as smartphones, tablets, and handheld devices are driving the demand for thinner, smaller, and more highly integrated semiconductor packages. Wafer-level packaging (WLP) is evolving rapidly to shrink package sizes for easier integration into mobile electronic devices. As die sizes have continued to decrease, the bandwidth and number of inputs/outputs (I/Os) required have been increasing, creating the need for innovative advanced package designs to maintain high bandwidth and manage higher I/O counts at the chip, package, and board levels. Historically, the packaging industry has relied on flip-chip processing for most WLP applications. Over the last few years, many new forms of WLP have been developed to enable higher-density applications, namely fan-out WLP (FOWLP), fan-in wafer-level chip-scale package (FI-WLCSP), 3D FOWLP, 2.5D integration with interposer technology, and true 3D IC integration using through-silicon via (TSV) interconnects. Many of these WLP technologies involve processing of thin wafers that must be mechanically supported during the manufacturing flow. Carrier-assisted wafer handling is proving to be a reliable method for processing thin device substrates. In this method, a device wafer is temporarily bonded to a rigid carrier substrate with a polymeric material that controls the overall stability of the structure during thinning and other processing.

Temporary bonding process

The temporary bonding process consists of reversibly mounting a device wafer to a carrier substrate with a multilayer polymeric bonding material system. The bonding materials and the carrier substrate mechanically support the device wafer during thinning and subsequent backside processing. Because the primary bonding material and its ancillary layers control the bonding and debonding characteristics, as well as the in-process stability of the structure, they must be carefully designed to withstand the high

stresses created by thermal cycling, coefficient of thermal expansion (CTE) mismatch, and a host of other factors while remaining easily separable at the end of the process.

Temporary bonding technology has been implemented in a variety of high-volume manufacturing environments for handling ultrathin wafers through standard fab processes such as deposition, dry and wet etching, plating, cleaning, and so on. The general process flow for temporary bonding and carrier-assisted thin wafer handling is illustrated in **Figure 1**. New handling challenges continue to arise as the industry moves toward greater heterogeneous integration, larger packaging substrates such

as panels, and even thinner die and package dimensions. As a result, temporary bonding solutions and wafer support systems have to keep pace with these challenges to serve the growing needs of the industry.

Key challenges

Many segments of the semiconductor industry including FOWLP, power devices, MEMS, 2.5D and 3D IC, and compound semiconductors utilize temporary bonding technology for handling ultrathin wafers. While each of these device segments presents a unique set of challenges for temporary bonding, there are also common challenges, as the summary in **Table 1** explains.

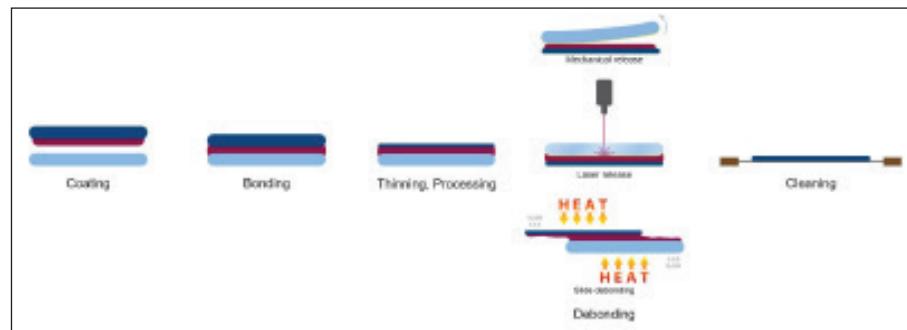


Figure 1: General schematic of thin wafer handling process flow.

Market Segment	Characteristics of the Process	Key Challenges and Expectations for Temporary Bonding Material
FOWLP	<ul style="list-style-type: none">Highly stressed heterogeneous substratePanel-type substrates and reconstituted 300-mm wafers less than 400 µm thick require wafer support systemsDouble-sided RDL processing, SiP, and PoP packages may require temporary wafer bonding processes	<ul style="list-style-type: none">Large area/panel processesHigh-stress substratesLow-temperature bonding/debonding processes
Power Device	<ul style="list-style-type: none">Device wafer thinned to much less than 100 µmHighly stressed device wafersProcess temperatures 350°C+ for dopant activation	<ul style="list-style-type: none">Ultrahigh temperature (350°C+)High-stress substrates
2.5-D and 3-D IC	<ul style="list-style-type: none">Ultrathin wafer handling (wafers ~30 µm thick)Highly stressed device wafers with TSVs and interposers	<ul style="list-style-type: none">High-stress substratesLow-temperature bonding/debonding processes
MEMS and III-V	<ul style="list-style-type: none">Extremely fragile and sensitive substrates at low thicknesses which require wafer support systemPost-thinning process temperatures could reach 350°C+ for certain annealing processes	<ul style="list-style-type: none">Ultrahigh temperature (350°C+)High-stress substrates
Other Commonalities for All Above Segments		<ul style="list-style-type: none">Increase process throughputSimplify process stepsRoom, temp./low temp. bonding processLow outgassing in vacuumHigh yield, low CoO

Table 1: Key challenges for temporary bonding materials in various market segments.

FOWLP technology. The market for FOWLP reached \$200M in 2014 and is expected to grow at a rate of 30% CAGR in the future [1]. FOWLP technology utilizes a wafer reconstruction process in which known good dies from the original device wafer are picked and placed on a substrate and then over-molded with an epoxy molding compound and cured to create a heterogeneous substrate known as a reconstituted wafer. Subsequently, the reconstituted wafer is temporarily bonded to a carrier before being further processed to fabricate redistribution layers (RDLs) on one or both sides of the wafer. The bonded wafer typically goes through dielectric deposition, metallization, and photolithography processes to fan-out interconnections from the die area onto the epoxy molding area surrounding the die. The reconstituted wafer then goes through normal wafer-level bumping and singulation processes.

The dies in the reconstituted wafer are made predominantly of silicon, which has a CTE of 2-3 ppm/ $^{\circ}$ C, while the over-molding compound has a CTE of 7-8 ppm/ $^{\circ}$ C. Depending on the die size and density, the effective CTE of the heterogeneous substrate will lie somewhere within this broad range. The inherent CTE mismatch of the silicon die and the epoxy molding compound creates high residual stress and significant bowing of the substrate. Several design regulations and limits have to be met to minimize this bow.

FOWLP packages are predicted to become thinner and thinner to meet market needs, and as 300mm reconstituted wafers become thinner, they are no longer self-supporting and require a wafer support system for handling. The same holds true as FOWLP packaging moves from single-die FOWLP to double-sided RDL, package-on-package (PoP), and system-in-package (SiP) FOWLP architectures. **Figure 2** shows the expected evolution of package type and substrate size for FOWLP.

Current high-volume production is based on 200 and 300mm reconstituted wafers, and it is predicted that a more than 2.5x cost reduction can be obtained by moving to Gen 2 panel-sized reconstituted substrates [2]. These larger panels and thinner package sizes have significant internal stresses that result in bow and warp of the substrates. Temporarily bonding a panel-sized substrate to a carrier substrate such as a sheet of glass will become the preferred route for processing thin, large-area panels, although a simplified process for

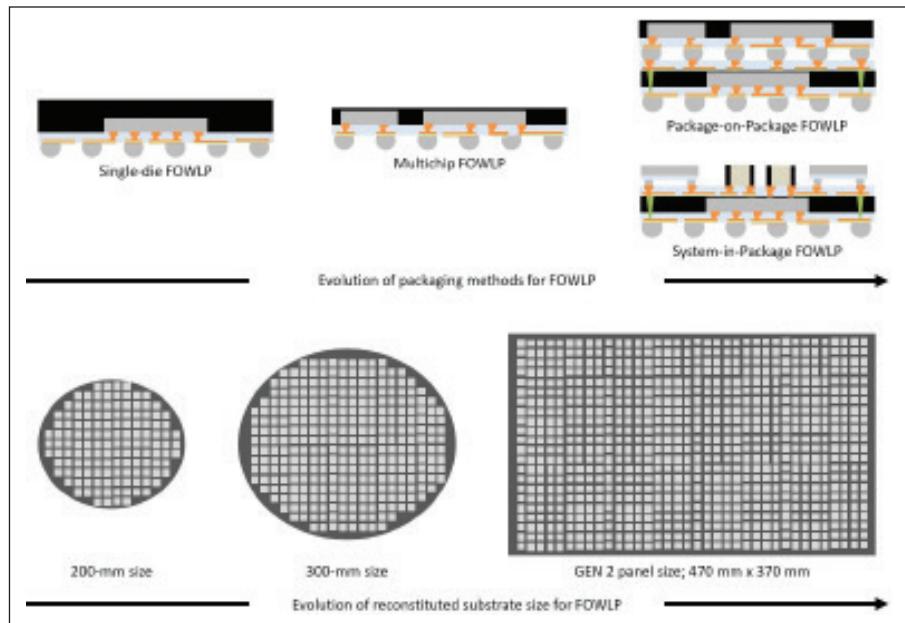


Figure 2: Evolution of package type and panel size for FOWLP.

bonding and debonding large-area substrates will be sought eventually.

Power devices. The fabrication of power devices such as insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) involves thinning to far less than 100 μ m to enable better heat dissipation and higher power densities. At these thicknesses, the device wafers easily warp due to high intrinsic stresses in the structure. Moreover, unlike CMOS device wafers where active elements are on the front side of the device wafer and fabrication is completed before temporary bonding, in IGBT and MOSFET devices, the wafer requires ion implantation and dopant activation on the backside of the wafer to create backside drain contacts after temporary bonding and backside thinning [3,4]. The dopant activation step requires temperatures as high as 350 $^{\circ}$ C to 400 $^{\circ}$ C, and, therefore, the temporary bonding material needs to survive such high temperatures without decomposing and remain soluble for later cleaning. **Figure 3** depicts a simplified thin wafer handling flow for power device fabrication. It is an exceedingly difficult challenge for a temporary bonding material to survive 400 $^{\circ}$ C treatment successfully. Fortunately, a few pre-commercial platforms with ultrahigh-temperature (UHT) capability are yielding encouraging results in current field trials.

2.5D and 3D IC integration. Thin wafer handling and temporary bonding are now well-established processes for 2.5D interposer fabrication and DRAM

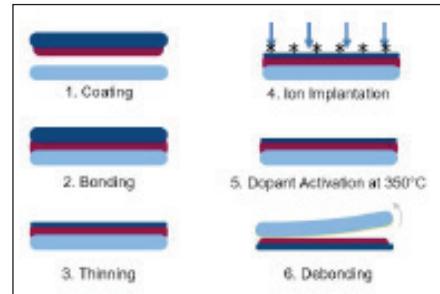
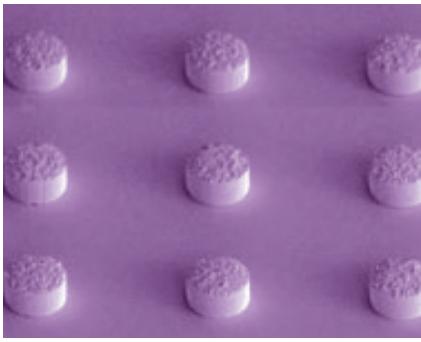


Figure 3: Simplified schematic representation of thin wafer handling in the power device fabrication process.

3D stacking. For interposer fabrication, the device wafer is usually temporarily bonded to a supporting wafer and thinned down to the required thickness to expose the TSVs as the first step in building the backside interconnect. Correspondingly, the temporary bonding materials must be able to withstand the high-vacuum conditions and temperatures up to 250 $^{\circ}$ C required for dielectric and metal deposition. After separation from the carrier, the bonding materials remaining on the device wafer must be removed completely and easily by solvent cleaning. It is typical for device wafers to be thinned to less than 50 μ m for wafer sizes up to 300mm. The bonding material must achieve a post-bond total thickness variation (TTV) of less than 5% in order for the TSVs to be revealed uniformly across the wafer. It must also stabilize the device wafer against cracking and edge chipping throughout the entire backside process. Because 2.5D and 3D devices often have solder



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bumps up to 85 μm tall, the temporary bonding material thickness must be about 100 μm for successful processing. Like all areas of advanced packaging, 2.5D and 3D IC device fabrication is very sensitive to cost-of-ownership, throughput, and yield.

C o m p o u n d semiconductor (III-V) and MEMS devices. A wide variety of device substrates are encountered in the III-V market. The common substrates are gallium arsenide (GaAs), silicon carbide (SiC), indium phosphide (InP), gallium nitride (GaN), and complex epitaxially grown compositions on silicon or sapphire. Substrate sizes vary from 2 inches up to 8 inches depending on the end product and the existing capability for growing epitaxial layers on different wafer sizes. Most of these substrates are brittle and very susceptible to breakage when thinned below 150 μm , and some exhibit high residual stresses that can lead to warping, making a carrier support system necessary. While waxes or tapes have been the traditional choice for temporary bonding, polymeric bonding material systems have now been developed to withstand the higher stresses and temperatures encountered during thinning and downstream processing of III-V substrates.

Thin MEMS device wafers can suffer from much of the same fragility, and MEMS packaging often requires very high-temperature processing steps such as hermetic sealing or prolonged exposure to high-energy reactive ion etching. New, specially designed polymeric bonding material systems are being developed to provide stable temporary bonding under these harsh conditions.

	HT High-temperature-compatible materials	VHT Very high-temperature-compatible materials	UHT Ultra-high-temperature-compatible materials
Max. process temperature	225°C	350°C	400°C
Bonding temperature	150°–180°C	High, Low, Room Temp.	Low, Room Temp.
Debonding temperature	~180°C	Room Temp.	Room Temp.
Stability at max. temperature*	1+ hour	1+ hour	1+ hour
Debonding methods	Silic., Mechanical, or Laser	Mechanical or Laser	Mechanical or Laser
Bond line thickness	10–100 μm	10–100 μm	10–100 μm
Oxidizing	Stable in low vacuum	Stable in low vacuum	Stable in low vacuum
Platform names	BrewerBOND® 220 material and other products	BrewerBOND® 305 material and other products	Developmental products

* Stability at max temperature is dependent on specific product; some products are stable up to several hours.

— Pre-Commercial / Developmental —

Table 2: High-level classification of temporary bonding materials.

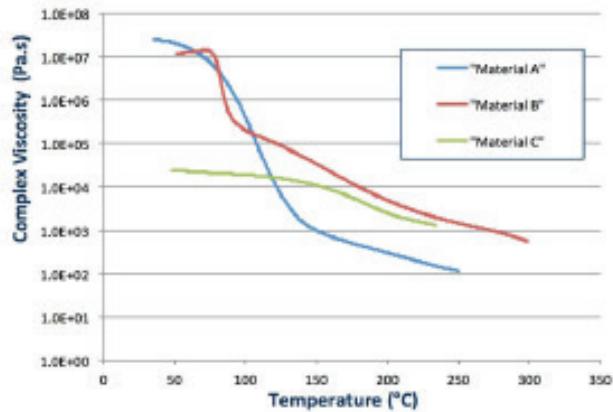


Figure 4: Comparison of melt-viscosity properties for three temporary bonding platforms.

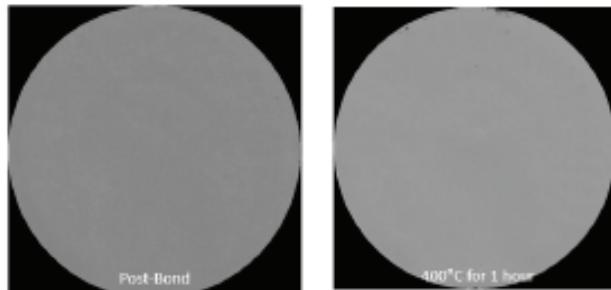


Figure 5: Scanning acoustic microscopy image of UHT material, a) post-bonding and b) after 400°C exposure for 1 hour.

Temporary bonding materials

The information in **Table 2** represents a high-level classification of the temporary bonding materials that are available and being developed for different applications. Several of these platforms are already used in high-volume production, while others are pre-commercial and developmental materials that are currently undergoing field testing and customer evaluations in advanced applications.

Viewed from a high level, it is clear that the industry is moving toward higher-temperature processing of thinner, more highly stressed, larger-area substrates and panels. All the while, the expectations for temporary bonding materials are moving toward more simplified bonding and debonding processes at lower temperatures and with less force to improve yields and throughput and reduce process cost-of-ownership. Consequently, we expect to see dynamic changes in the roadmap for temporary bonding materials and process development over the next few years.

Temporary bonding materials can be largely categorized by their maximum in-process use temperature, as shown in **Table 2**. In our experience, three main-use temperature ranges exist: high temperature (HT, 175°–225°C), very high temperature (VHT, 225°–350°C), and ultrahigh temperature (UHT, 350°–400°C+). Within these classifications, one can select specific products for compatibility with different bonding and debonding methods, tool designs, and other process flow requirements. Most of the platforms have been developed for room-temperature debonding using laser-assisted release or mechanical (peel-type) release.

Figure 4 displays the plots of melt viscosity versus temperature for three bonding material platforms at temperatures from 50°C to 300°C. At 200°C, the melt viscosity of Material B is ~15 times greater than that of Material A. Melt viscosity at a given temperature is indicative of the amount of stress a bonding material can handle without delaminating, voiding, or deforming. Based on the melt viscosity characteristics and other physical parameters such as adhesion strength, material platforms can be chosen and optimized for temporary bonding applications in which the range of stress varies from low to high. **Figure 5** shows a scanning acoustic microscopy image of a wafer pair bonded with the UHT material platform listed in **Table 2**. Even after heat treatment at 400°C for 1 hour, the bonded pair survived fully intact with no defects occurring in the material bond line.

The road ahead for temporary bonding materials

The market continues to push technology boundaries to create smaller, faster, and more highly integrated devices at lower cost. Device makers and advanced packaging manufacturers are employing all the design

and processing tools at hand to meet this need. Temporary bonding technology is one of the critical new processes for continuing progress. Our bonding material and process development roadmap has anticipated the ever more demanding needs of the industry and, in fact, is leading users toward more cost-effective and reliable thin substrate handling technologies.

As an example of the above, our new materials are being developed to allow bonding at low temperatures or even room temperature, which will translate to reduced baking and bonding times. When this feature is combined with room-temperature debonding, wafer throughput can begin to approach more than 30 wafers per hour. We believe that these simplified bonding and debonding methods will also be applicable to panel-based processing. At the same time, continuous improvements in thermoplastic bonding material platforms are reducing cleaning times and solvent consumption. Lastly, unique combinations of thermoplastic and thermosetting bonding materials are being employed to create a UHT platform that is truly capable of operating at or above 350°C.

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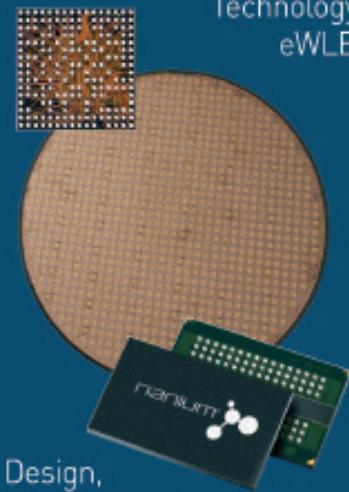
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Patent issues of fan-out wafer/panel-level packaging

By John H. Lau [ASM Pacific Technology Ltd.]

In the industry, research institutes, and universities, there are many engineers, researchers, students, and professors working on fan-out wafer/panel-level packaging. In order to avoid the granted and pending patents in this area, they are trying various methods such as die up, die down, die first, die last, RDL (redistribution layer) first, RDL last, mold first, mold last, round temporary carrier, and rectangular temporary carrier. In this study, the patent issues of fan-out wafer/panel-level packaging will be investigated. Emphasis will be placed on the claims of the granted patents and making some recommendations. The patents that impact semiconductor packaging the most will be briefly mentioned first.

Patents impacting semiconductor packaging

There are many significant patents such as the solder bumped flip-chip and through-silicon vias that impact semiconductor packaging. However, based on the author's opinion, the following four patents are the most important so far.

Lead frame. On July 17, 1967, Kauffman of Jade Corporation [1] proposed the use of a lead frame (see items #14, 16 in **Figure 1**) having terminal ends (item #18, **Figure 1**) to fan-out the circuitry from a chip (item #20) as shown in **Figure 1**, to a printed circuit board (PCB). Today, just about all electronic products use lead frames such as the gull-wing lead, J-lead, and/or through-hole lead to fan-out the circuitry from a chip to a PCB. In the past almost 50 years, the lead frame patent has had the most impact on semiconductor packaging.

Organic substrate with solder balls. On March 2, 1992, Paul Lin, Mike McShane, and Howard Wilson of Motorola proposed [2] the use of an organic carrier or substrate (item #12 in **Figure 2**) with area-array solder balls (item #26 in **Figure 2**) (instead of lead frames) to fan-out the circuitry (items #22, 30, 33 in **Figure 2**) from a chip (item #18 in **Figure 2**) to a PCB, which is called a plastic ball grid array (PBGA) package. Also referring to **Figure 2**, item #22 is a wire bond and item

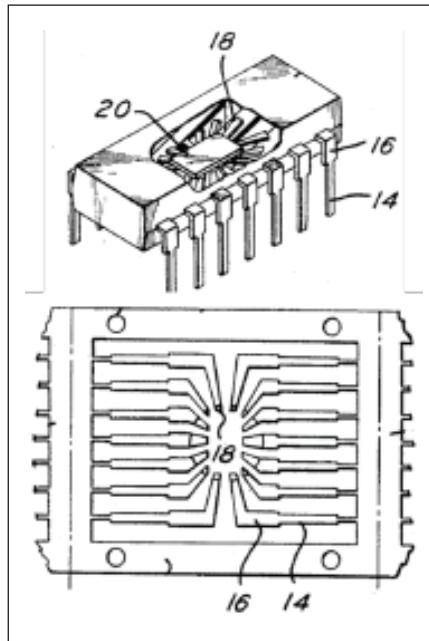


Figure 1: Lead frame patent [1] proposed by Jade Corporation.

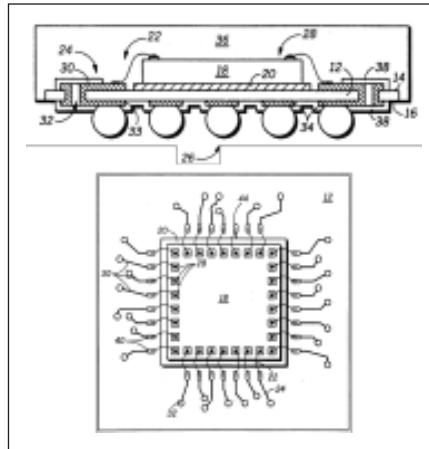


Figure 2: Organic substrate with area-array solder balls patent [2] proposed by Motorola.

#32 is a via in the substrate connecting the upper wiring layer (item #30) to the bottom wiring layer (item #33). It should be pointed out that in 1989, Motorola and Citizen Watch announced the over molded pad array carrier (OMPAC) package, which is the first PBGA.

Amkor (1993) led the outsourced semiconductor assembly and test suppliers (OSATs) to license this packaging technology from Motorola—and the BGA era began. Since then, hundreds of patents such as solder bumped flip-chip on organic substrate have been granted in the related area. However, they are incremental patents and Motorola's [2] is the fundamental patent.

Today, PBGA packages have been used for housing just about any (low-end to high-end) semiconductor ICs (from 4 to 625mm²) with solder balls ranging from 10s to 1000s and their pitch ranges from 0.5, 0.65, 0.8, 1, to 1.27mm. The sizes of the PBGA packages range from 10mm x 10mm, to as large as 55mm x 55mm. The organic substrate with solder ball patent ranks second in terms of impact on semiconductor packaging, so far.

Fan-in wafer-level packaging. On July 13, 1998, Peter Elenius and Harry Hollack of Flip Chip Technologies proposed [3] the use of RDL (see item #30 in **Figure 3**) to fan-in the circuitry from the peripheral bond pads (items #18, 20, **Figure 3**) of a chip (item #10, **Figure 3**) on a wafer (item

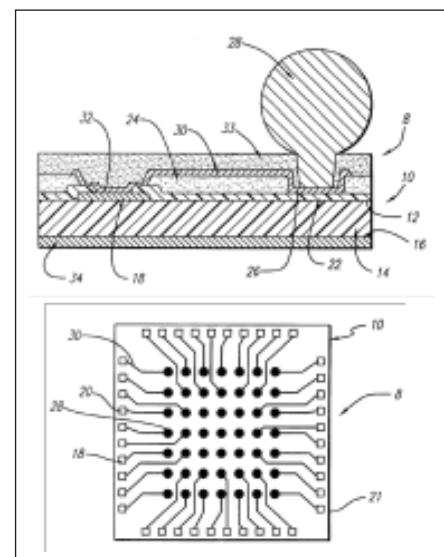


Figure 3: Fan-in WLP patent [3] proposed by Flip Chip Technologies.

#14, **Figure 3**) and of solder balls (item #28, **Figure 3**) to connect to a PCB without underfill. The RDL (item #30) is connecting the electrical contact (item #32) on the peripheral bond pad (items #18, 20) to the solder bump pad (item #26). Large solder balls (item #28) can be fabricated within the chip (item #10) on a wafer (item #14). Lead frame, substrate, and underfill are eliminated.

It should be pointed out that the concept of fan-in wafer-level packaging (WLP) was first proposed by Flip Chip Technologies [3,10,14]. However, the knowledge in this area has been mentioned/demonstrated by many others such as Mitsubishi [4,8], Marcus [5], Sandia [6], ShellCase [7], Fraunhofer IZM [9,11], DiStefano [12], and EPIC [13]. The packages made by the fan-in WLP are called wafer-level chip-scale package (WLCSP)

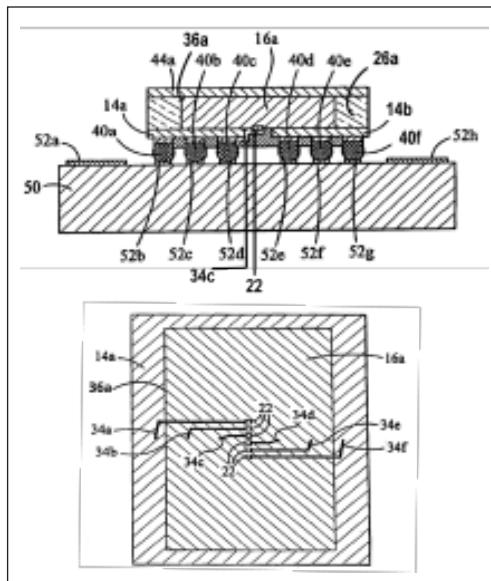


Figure 4: Fan-out WLP patent [16] proposed by Infineon.

and one of the most famous is UltraCSP [15] developed and patented by Flip Chip Technologies [3]. In 2001, again Amkor led the OSATs and foundries to license the UltraCSP, and the WLP era began.

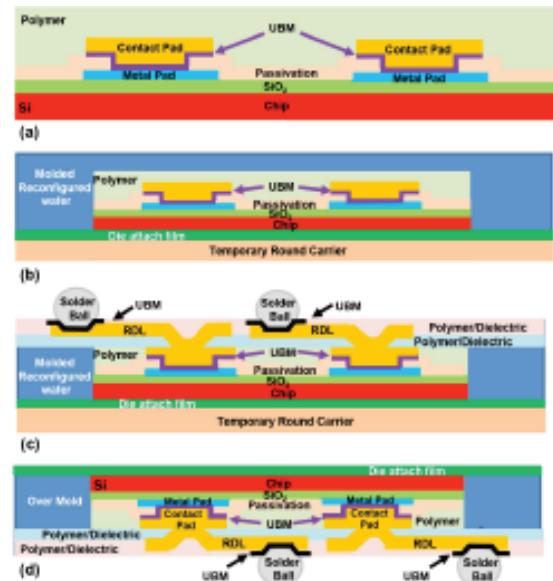


Figure 5: Integrated fan-out (InFO)-WLP patent [21] proposed by TSMC.

In the past 15 years, WLCSP has been used mainly for low-cost, low-end, low-profile, low pin count, small form factor, and high-volume applications such as mobile (smartphones and tablets) and portable (digital

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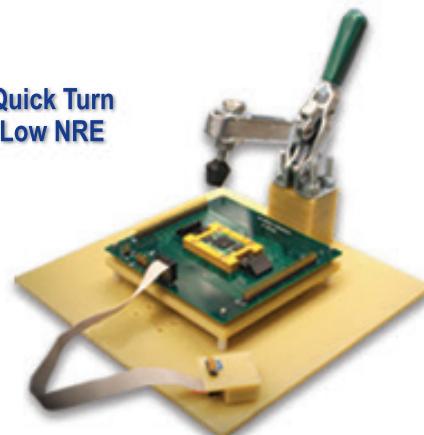
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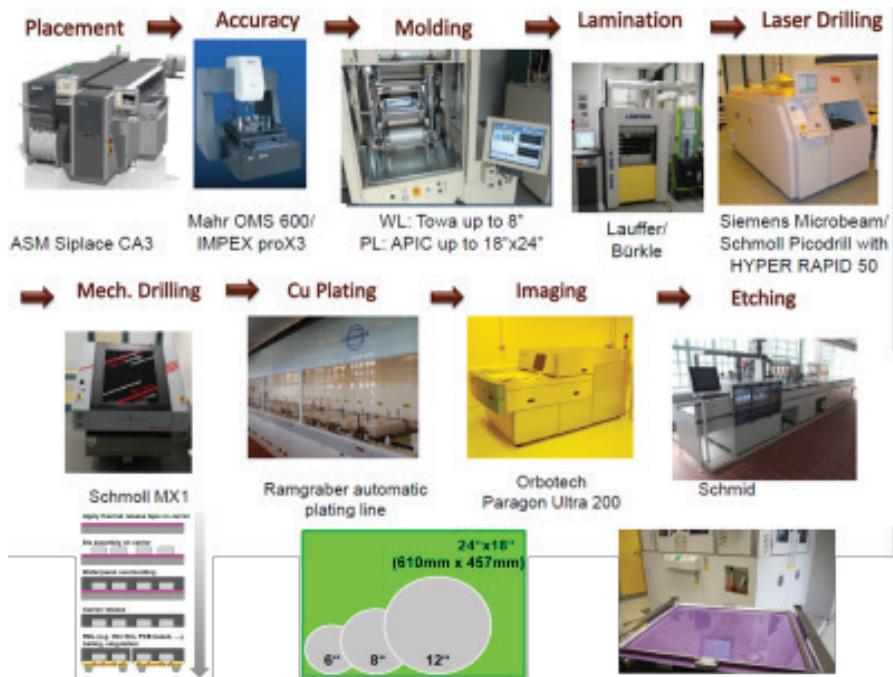


Figure 6: Fraunhofer IZM's fan-out panel-level packaging (FOPLP) integration line and process flow.

cameras and notebooks) products. The fan-in WLP patent is the third most impactful one in semiconductor packaging, so far.

Fan-out wafer-level packaging. On October 31, 2001, Harry Hedler, Thorsten Meyer, and Barbara Vasquez of Infineon proposed [16] the use of RDLs (items #34a-f in **Figure 4**) to fan-out the circuitry from the metal pad (item #22) of the chip (item #16a) on a wafer and solder ball (items #40a-f) to the metal pads (items #52b-g) on a PCB (item #50) without underfill (**Figure 4**). Some of the RDLs (items #34a, 34f) having a portion that extends beyond (fan-out) the edges (item #36a) of the chip (item #16a). Item #26a is the encapsulant (molding compound). Items #14a-b are the dielectric layer.

It should be pointed out that the concept of fan-out WLP was first proposed by Infineon [16]. Even though some of the knowledge of this technology has been patented by General Electric [17,18] and EPIC [19], Infineon's patent [16] specifically pointed out the use of RDLs to fan-out the circuitry from the metal pad of the chip on a wafer and solder ball to the metal pads on a PCB (**Figure 4**). Infineon also specifically pointed out that some of the RDLs have a portion that extends beyond (fan-out) the edges of the chip. These are the major claims in [16], which were not claimed by GE and EPIC.

The advantages of fan-out WLP over PBGA packages with solder-bumped flip chip are: 1) lower cost, 2) lower profile, 3) eliminating the substrate, 4) eliminating the

wafer bumping, 5) eliminating the flip-chip reflow, 6) eliminating the flux cleaning, 7) eliminating the underfill, 8) better electrical performance, 9) better thermal performance, and 10) easier to go for system-in-package (SiP) and 3D IC packaging [20].

The advantages of fan-out WLP over fan-in WLP are: 1) the use of known good die (KGD), 2) better wafer-level yield, 3) using the best of silicon, 4) multi-chip, 5) embedded integrated passive devices, 6) more than one RDL, 7) higher pin counts, 8) better thermal performance, 9) easier to go for SiP and 3D IC packaging, and 10) higher PCB-level reliability.

Today, Infineon's fan-out WLP technology is licensed by ASE, STATS ChipPAC, NANIUM S.A., and STMicroelectronics. Even fan-out WLP is not in very high-volume manufacturing yet, however, because of the important advantages over the fan-in WLP and PBGA, it has the potential for substantial growth. Therefore, this author considers fan-out WLP as the fourth most impactful for semiconductor packaging in the near future.

The claims of Infineon's patent

The major claims of Infineon's patent [16] are the use of RDLs to fan-out the circuitry from the metal pad of the chip and solder ball to the metal pads on a PCB (**Figure 4**). The company also claimed that some of the RDLs have a portion that extends beyond the edges of the chip. As a matter of fact, the company [16] didn't

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Temporary carrier	Appl.	Line width/spacing	Line Thick.	Dielectric Mat.(Thick.)	Litho.	Proc./Equip.
	High-end	$\leq 2 - 5\mu\text{m}$	$1 - 2 \mu\text{m}$	$\text{SiO}_2 (1\mu\text{m})$	Stepper	<u>Cu damascene</u> <u>Semi. Equip.</u> <u>High-Precision P&P</u>
	Middle-end	$5 - 10\mu\text{m}$	$3\mu\text{m}$	Polymers ($4 - 8\mu\text{m}$)	Mask aligner	<u>Cu plating</u> <u>Packaging Equip.</u> <u>Ordinary P&P</u>
	Low-end	$10 - 20\mu\text{m}$	$5\mu\text{m}$	Resin ($15 - 30\mu\text{m}$)	Laser direct imaging	<u>PCB Cu plating</u> <u>PCB Equip.</u> <u>SMT P&P</u>

Table 1: Geometry, material, process, and equipment for fan-out wafer/panel WLP.

claim anything such as die first or last, die up or down, RDL first or last, mold first or last, and reconfigured wafer or panel at all. It is a “structure” patent.

TSMC InFO-WLP

One of the most famous fan-out WLPs is TSMC’s integrated fan-out WLP (InFO-WLP). **Figure 5d** schematically shows a typical cross section of the InFO-WLP [21]. It starts off by KGD testing of a device wafer. Then, under bump metallization (UBM) is performed by sputtering (e.g., Ti/Cu) with physical vapor deposition (PVD), and the Cu contact pad (or post) accomplished using electroplating. These steps are followed by spin coating a polymer (e.g., polyimide (PI), benzocyclobutene (BCB), or polybenzo-bisoxazole (PBO)) on the whole wafer and then singulating it into individual dies (**Figure 5a**). The individual KGD is placed (face-up) on a temporary round carrier with a die attach film as shown in **Figure 5b**, and then over molding is done on the whole temporary carrier with KGDs to form the molded reconfigured wafer. It is followed by backgrinding the reconfigured wafer to expose the Cu contact pad, building up the RDLs, and mounting the solder ball (**Figure 5c**). Finally, remove the temporary carrier and singulate the reconfigured wafer into individual units, and then we have the fan-out package (**Figure 5d**) by InFO-WLP. Comparing the cross section of **Figure 5d** with that of **Figure 4**, it can be seen that they are similar, i.e., the RDLs fan-out the circuitry beyond the chip edge.

TSMC have been working on a new package-on-package (PoP) called InFO-PoP

for the application processor (AP) chipset (mobile DRAM + AP SoC (system-on-chip)). Just like TSMC’s CoWoS (chip-on-wafer on substrate) technology, they called this PoW (package-on-wafer) technology [22]. PoW means the mobile DRAM package is stacked on the AP InFO reconfigured wafer and the connection between the memory package and the AP InFO package is by through-InFO-via (TIV). If this happens, then the wafer bumping, flip-chip assembly, flux cleaning, underfill, and package substrate are eliminated, and it results into a lower profile and cost PoP.

Fraunhofer IZM’s FOPLP

During 2015 IEEE/ECTC, Fraunhofer IZM presented a paper [23] that summarized its 3-year development on fan-out panel-level packaging (FOPLP). They showed that with surface mount technology (SMT) equipment for picking and placing the dies and integrated passive devices and PCB technology for making the RDLs, they are able to fabricate FOPLP at a very low cost (with a large panel instead of a wafer) for low end, low pin count, small chip sizes, and high-volume applications. A complete Fraunhofer IZM FOPLP integration line is shown in **Figure 6**. It can be seen that there is not any semiconductor foundry equipment. Their test vehicle is a standard PCB size (610mm x 457mm) rectangular panel and the process flow is also shown in **Figure 6**. Comparing the cross section of the fan-out package with that of **Figure 4**, it can be seen that they are almost the same, i.e., the RDLs fan-out the circuitry beyond the chip edge.

Summary

The patent issues of fan-out wafer/panel-level packaging have been investigated in this study. Some important results and recommendations are as follows:

- As of today, the patents impacting the semiconductor packaging industry the most are: 1) lead frame, 2) organic substrate with area-array solder balls, 3) fan-in WLP, and 4) fan-out WLP.
- Fan-out WLP and fan-out PLP can do the same things fan-in WLP can: such as, for low cost, low end, low profile, low pin count, small form factor, and high-volume applications.
- Fan-out WLP can do most of the things PBGA can; such as, for middle-end to high-end microprocessors, ASICs, and memory applications. However, some of the things PBGA can do, but fan-out WLP cannot are: 1) large die size ($\geq 12\text{mm} \times 12\text{mm}$) and 2) large fan-out package size ($\geq 25\text{mm} \times 25\text{mm}$). These are due to the thermal expansion mismatch and warpage limitations of the fan-out WLP.
- Infineon’s patent [16] is a “structure” patent. The major claims are the use of RDLs to fan-out the circuitry from the metal pad of the chip and solder ball to the metal pads on a PCB; some of the RDLs have a portion that extends beyond the edges of the chip.
- If the cross section of an individual fan-out package (no matter if it is made from die first or last, die up or down, RDL first or last, mold first or last, and reconfigured wafer or panel) looks like the one in **Figure 4** (RDLs fan-out the circuitry beyond the chip edge), then it is subjected to Infineon’s patent [16].
- Instead of trying to avoid Infineon’s fan-out WLP patent [16], the focus should be on the development of new and innovative applications such as TSMC’s low-profile and low-cost InFO-PoP and Fraunhofer IZM’s low-cost and high-volume FOPLP with SMT and PCB technology.
- The geometry, material, process, equipment, and application of fan-out wafer/panel-level packaging are recommended as follows (**Table 1**).

- a) For reconfigured wafers for high-end applications (e.g., high-end APs), the RDL line width/spacing and thickness are, respectively, $\leq 5\mu\text{m}$ and $2\mu\text{m}$ right now. But very soon they are going down to $\leq 2\mu\text{m}$ and $1\mu\text{m}$, and the lithography process is accomplished using a stepper. They are fabricated by the Cu damascene method. The dielectric layer (SiO_2) is $1\mu\text{m}$ thick and fabricated by the plasma-enhanced chemical vapor deposition (PECVD) method. A high-precision pick and place (P&P) bonder is needed for die placement.
- b) For reconfigured wafers for middle-end applications (e.g., low-end APs, ASIC and memory), the RDL line width/spacing and thickness are, respectively $5\text{-}10\mu\text{m}$ and $3\mu\text{m}$, and the lithography is accomplished using a mask aligner. They are fabricated by the electrochemical deposition method. The dielectric layer comprises polymers (e.g., PI, PBO or BCB) and is $4\text{-}8\mu\text{m}$ thick. An ordinary P&P bonder should be able to perform the die placement.
- c) For reconfigured panels for low-end applications (e.g., WiFi/Bluetooth®/FM module, RF transceivers, PMIC, and the power management unit), the RDL line width/spacing and thickness are, respectively, $10\text{-}20\mu\text{m}$ and $5\mu\text{m}$. They are fabricated using PCB technology. A resin-coated copper (RCC) sheet is laminated on the reconfigured panel. Microvias are drilled through the RCC layer to the die pads and electrically connected by Cu plating. RDL formation is done by laser direct imaging in combination with a dry film resist and copper etching. The dielectric layer (resin) ranges from 15 to $30\mu\text{m}$. An SMT P&P is more than adequate for die placement.
- d) There is a small overlapping area between the high-end and middle-end, and the middle-end and low-end.

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Biography

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Bosch Sensortec enables sensor fusion with new sensor+software development package

By Debra Vogler, Sr. Technical Editor

Bosch Sensortec recently announced the release of a compact 9-axis motion sensor — the BMF055 — along with a software development package that enables customized sensor systems to be programmed for specific applications. The new sensor is part of the company's Application-Specific Sensor Node (ASSN) family and combines an accelerometer, a gyroscope and a magnetometer with a Cortex M0+ processor from Atmel's SAMD20 microcontroller family. The device is in a 5.2 x 3.8 x 1.1mm³ package.

The company says that the new sensor is well suited to the needs of users developing advanced application-specific sensor fusion algorithms, adding sophisticated motion sensing capabilities, and replacing multiple discrete components with a single package. Among the market segments being targeted are robotics, gaming, remote controls, navigation systems, drones, and human interface devices for Internet of Things (IoT) projects.

The software development package includes a precompiled BSX Lite fusion library with integration guidelines, API source files for individual sensors and example projects as a plugin for Atmel Studio. The Atmel toolchain can be downloaded from Atmel's website. The company noted that this software development package will enable end users to develop their own application-specific firmware for the BMF055 sensor without requiring an additional application processor.

Chip Scale Review asked Divya Thukkaram, Product Manager at Bosch Sensortec, to discuss some of the requirements and challenges the company had to address to develop the new sensor, and to provide context for it within the ASSN family. "The target was to build an ASSN small enough to fit into wearables and IoT devices," Thukkaram told *CSR*. "The BNO055 delivers fused orientation data that is required by many IoT and wearable applications, while the BMF055 is the flexible programmable version of the BNO055."

Regarding the technical challenges that had to be overcome to meet the customized SiP requirements of the new sensor's package,

Thukkaram said that the big challenge for the hardware was the integration of six different chips with more than 90 bond wires in one single package. "The duration and complexity of the product qualification rise together with the integration of increasing hardware components," said Thukkaram. "Of course, the software development was also a big challenge, first of all because of the complexity of the fusion algorithms, and certainly also due to the flexibility we set as a target from the very beginning." Thukkaram further noted that an advantage of the sensor and the software development package is that the device takes care of the complete sensor fusion, "so the designer can concentrate on the application development." She added that the industry trend is to further miniaturize package technology and integrate more sensors into an SiP package to meet the requirements of wearable devices, as well as IoT applications.

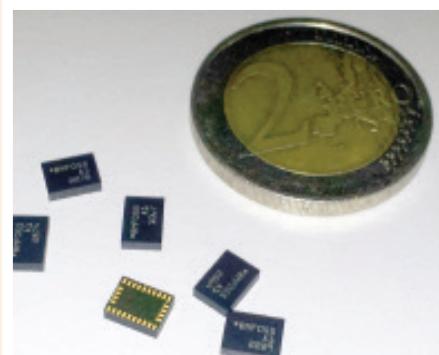


Figure 1: The BMF055 sensor.

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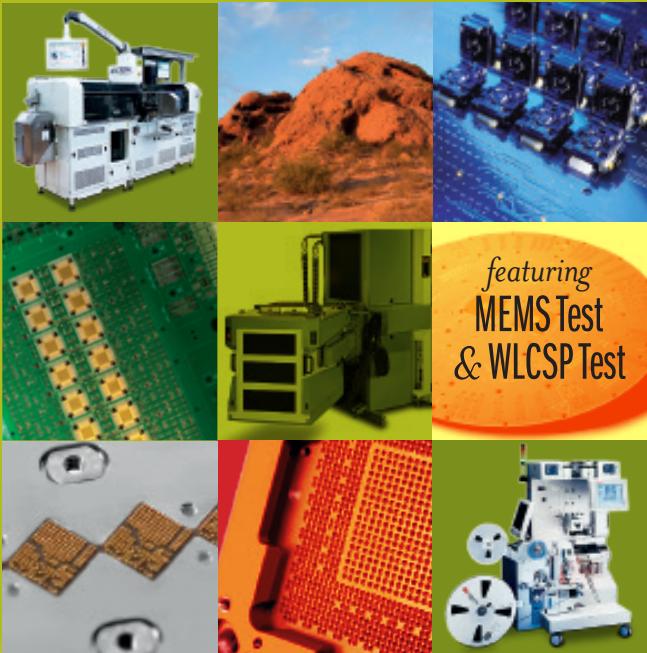
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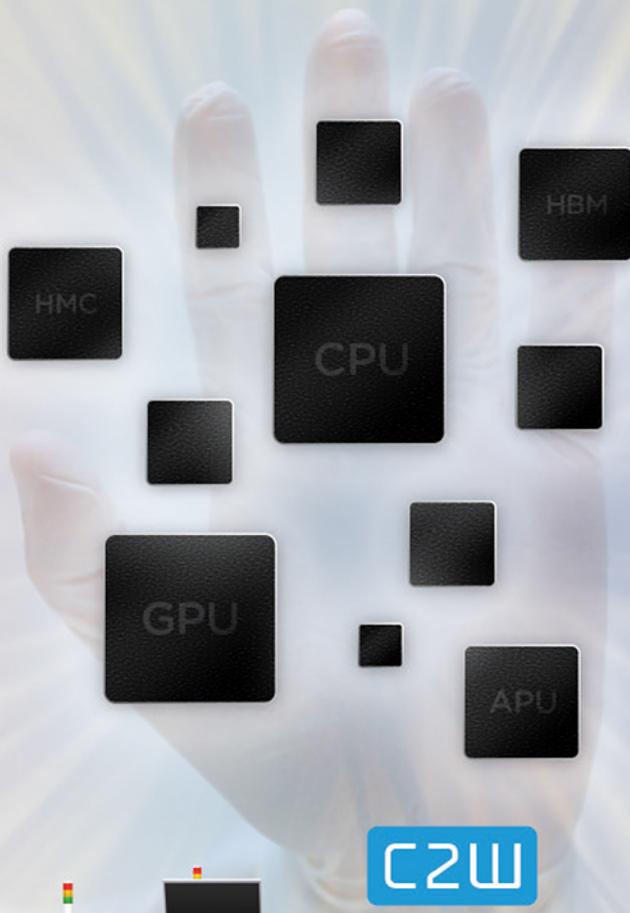
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