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R E V I E W

*The International Magazine for the Semiconductor Packaging Industry*

Volume 16, Number 6

November - December 2012

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- **Lessons for 3D IC Adoption**
- **3D IC Thin-Wafer Handling Materials**
- **Maximizing the Value of Silicon Interposer Technology**
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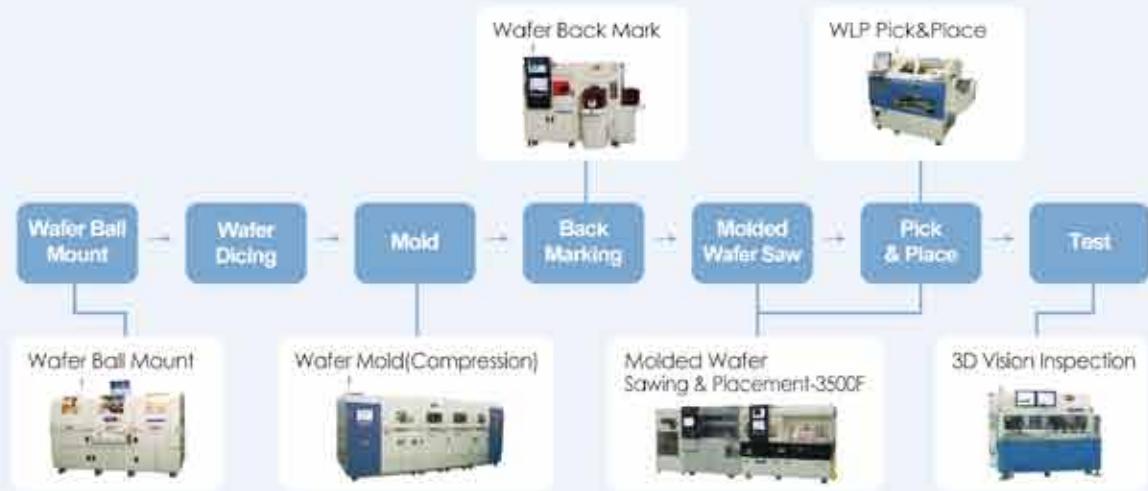
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# FROM THE PUBLISHER



## Amid Economic Weakness, Europe Flexes Its Muscles at SEMICON Europa

**S**EMICON Europa 2012 unfolded this year amid continuing economic woes and uncertainties for the region. Chip Scale Review asked Steffen Kroehnert, Technology Director, Nanium S.A. to share his observations of the event with our readers. He told me that business in Europe has short visibility and investment in equipment in Europe is about 3.5 billion dollars, with the economy in general being flat. But with some 344 exhibitors at the event, and the chance to talk to visitors from all over the world and make new contacts - he said it was great for networking and the show's theme, "Building on the strength of Europe," was apropos. He found the most compelling technology topics of discussion to be the 450mm wafer transition, EUV lithography, and 3D/TSVs, along with system integration.

As further evidence of Europe pulling itself together, Steffen pointed out that SEMICON Europa was well supported by Saxony (i.e., Saxony Economic Development Corporation), whose VIP reception and networking event, "Saxony! - Get Together," brought about 450 entrepreneurs and researchers from the microelectronics and IT branch to the world-famous Semperoper in the heart of the ancient center of Dresden. Steffen told CSR that with 20% more attendees compared to last year, the 40 programs and events with 210 speakers increased the value of the show for both visitors and exhibitors. As an example, he points out that during the committee debriefing of the Advanced Packaging Conference (APC), the conference chair, Andy Longford (Panda Europe), declared this years' conference as the most successful in many years, a statement, which the almost 100 participants definitely shared, noted Steffen.

David McCann of Globalfoundries gave a keynote to the APC entitled, "Product Drivers and Process Advances for 3D and 2.5D." McCann had made the observation that several technical presentations covering the topic of TSV-enabled interconnect in 2.5D and 3D technologies probably represented the primary theme heard at the show. Among the solutions discussed by process and metrology companies where those involved in the formation, isolation, and filling of high-aspect ratio vias, as well as leakage between vias and via contact resistance. It was also observed by McCann that, given the challenging economic environment in Europe and worldwide, it was not surprising to hear a lot of discussion about how to drive down the cost of TSV formation.

What can we take away from Steffen's observations? With strong participation in the technical sessions and exhibits at SEMICON Europa, semiconductor industry participants are not taking the region's economic troubles lying down, but instead, are flexing their networking and problem-solving muscles in a show of strength. Get together indeed!

*Kim Newman*  
Publisher

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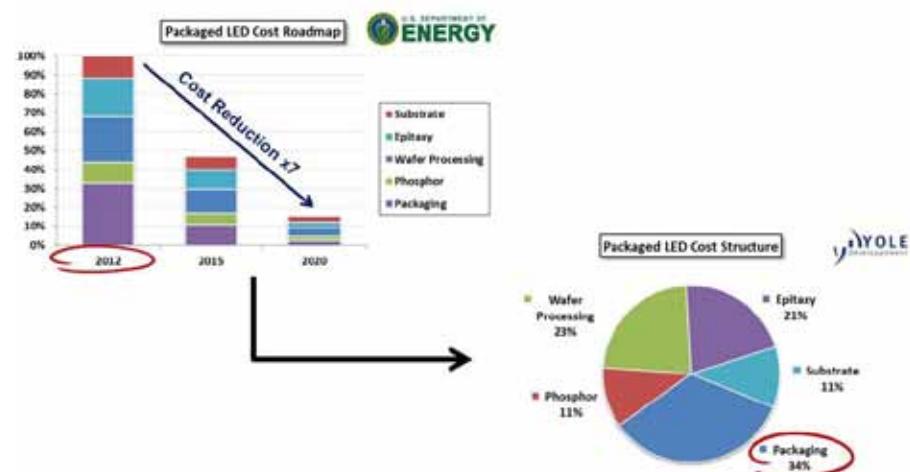


## Cost Reduction Drives LED Packaging Towards New Technologies

By Pars Mukish *[Yole Développement]*

**O**ne key to the growth of the LED lighting sector over the next few years will be how successfully it can drive down packaging costs. That naturally means more pressure on margins, but it also means opportunities for dedicated higher throughput, higher yielding equipment, even at higher initial cost. It means changes for the package substrate market as well, as the incursion of mid-power LEDs from the display sector into lighting applications spurs demand for chip-on-board (COB) solutions on the one hand, and high-power applications move to AlN substrates on the other. The upside is potential 5X growth in demand in LED die area to package, which Yole Développement projects could reach 80 billion mm<sup>2</sup> a year in five years as LED lighting becomes more cost-competitive.

Major improvements in LED technology over the last couple of years have enabled a real volume market for specialty solid-state lighting, but the mass penetration of the general lighting market still depends on further major cost reductions. The U.S. DOE roadmap targets a 6X reduction in packaged LED die cost by 2020 to enable wide adoption (**Figure 1**). We think that these cost reductions are possible, and that many of the key opportunities are in packaging, which accounts for a significant ~35% of LED costs on average (**Figure 2**). We expect major manufacturing changes in the next two years to propel sales of LEDs for lighting to surpass sales of LEDs for displays by 2014, driving strong market growth. Yole projects the total LED market will pick back up this year from last year's oversupply bloodbath to some \$11.4 billion, and climb at ~7% CAGR to a peak of \$17.1 B in 2018 (**Figure 3**). This forecast factors in a big drop in ASPs—the growth translates into ~23% CAGR in



**Figure 1:** Cost Structure of Packaged LED. SOURCE: Status of the LED Industry, Yole Développement, 2012



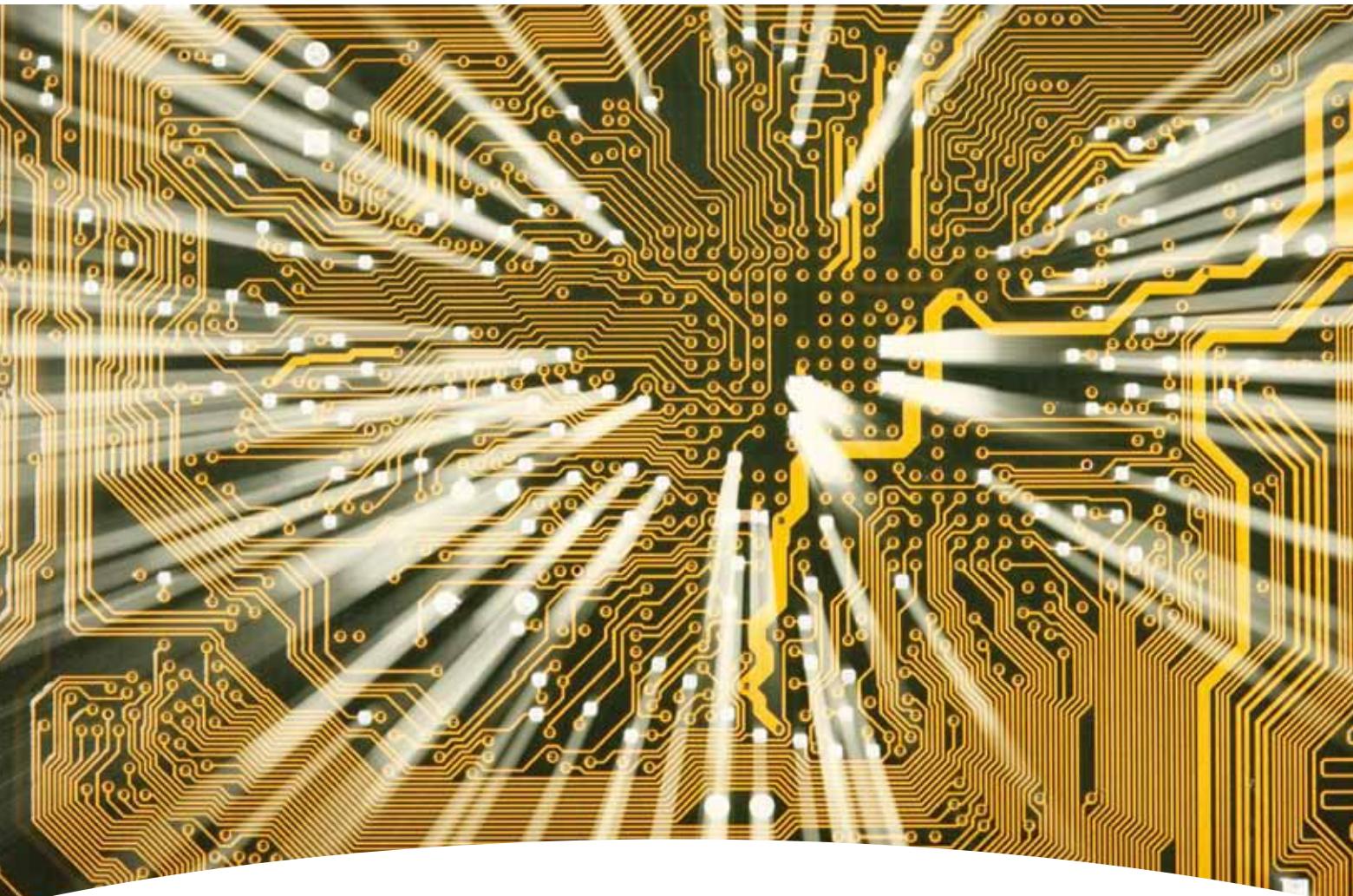
**Figure 2:** 10 Key Technologies & Research Areas at Packaging Level; Relative Impact on LED Cost-of-Ownership. SOURCE: LED Packaging, Yole Développement, 2012

die area to be packaged, from 22.5 billion mm<sup>2</sup> in 2012 to 80 billion mm<sup>2</sup> in 2018. Note that this is the net surface area of die to be packaged—the processed wafer area less losses from yield and dicing street width. After 2018 the market will likely start to decrease, as slow replacement cycles for the long-lasting LED bulbs limit demand, while prices continue to decline.

We are now seeing a real mind shift at LED makers and users towards even

more emphasis on driving down costs, which will have a global impact on equipment and technology. Cost reduction is becoming one of the main drivers for the adoption of new chip and packaging technologies. The economic downturn has turned even commercial and new construction users of LED lighting to focus more on upfront costs instead of longer term cost-of-ownership, just as consumers always have. Early adopters

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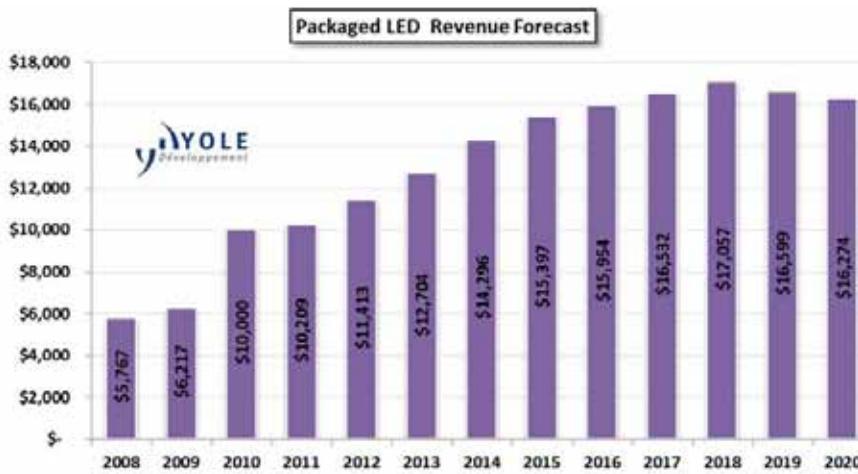


Figure 3: Packaged LED Revenue Forecast. SOURCE: Status of the LED Industry, Yole Développement, 2012

and niche lighting applications, where LEDs have clearest advantages, have already converted, moving the competition towards more mainstream markets where steadily improving fluorescents offer stiffer competition. Maturing technology means device efficiencies may be closing in practical limits, and more players can produce products with acceptable performance.

### Influx of Mid-Power LEDs from Display Side Will Impact Substrate Market

The influx of mid-power LEDs from the display market into the lighting market is driving down packaging costs. As recently as last year, the general lighting market meant high-power LEDs. But the volume ramp up of mid-power LEDs for LCD TV backlights drove down prices, and the slowing of the TV market created an oversupply. So lighting suppliers have found ways to use these lower cost, mid-power LEDs instead that allow simpler packaging solutions for thermal management. They can be mounted on a metal lead frame or a low cost plastic substrate, or mounted directly COB on metal-core PCB without use of an additional package substrate or sub-mount. Use of COB-mounting, not only for mid-power, but also for high-power chips for lighting applications, is growing rapidly, and will likely take an increasing share of the market. This may actually delay

cost reduction of ceramic substrates and other more complex thermal management solutions, as the increasing volumes of COB devices eat into the potential volumes needed to provide economies of scale to bring down costs of the competing packaging solutions (Figure 4).

Of course, as always with LEDs, no one solution fits every application, and the mid power devices can't match the color consistency and quality of the high power devices, and the COB mounting doesn't offer the directional performance of traditional packaging. But for many applications, multiple designs and package choices will be possible, not only COB vs. traditional packaging, but arrays vs. discrete packaging, or conformal vs. remote phosphors.

For high-power devices, direct-plated ceramic alumina (DPC Al<sub>2</sub>O<sub>3</sub>) remains the most commonly used package substrate material, as the best balance of cost and performance. But small markets exist for

a wide range of options, depending on the demands of the application, and the manufacturing culture of the maker. Low temperature co-fired ceramic (LTCC) or DPC Al<sub>2</sub>O<sub>3</sub> have the advantage of lower costs, while DPC AlN or silicon substrates offer better thermal conductivity. Silicon offers total package thermal resistance lower than DPC Al<sub>2</sub>O<sub>3</sub> and close to that of DPC AlN, with a good thermo-mechanical match with the LED, better adhesion of silicon encapsulant and lenses, and potentially low cost batch wafer-level assembly processes than could compensate for the higher cost of the substrate. Silicon, however, also requires more costly additional steps of deposition of insulator, barrier and seed layers in the vias, before copper filling. Demand for more expensive and more thermally conductive DPC AlN will see strong growth, as improved manufacturing processes and higher volumes drive down costs. Ceramic substrates remain the substrate of choice in high-end lighting to handle the high lumens per Watt devices. Metal lead frame substrates are still a significant 5%-10% of the total volume, but that will decrease, as the size is large and reliability is limited with large die sizes.

Though the LED market has so far had little interest in wafer-level packaging, as a major change with high upfront cost, the entry of IC makers into the LED business could bring some adoption of this approach with potential for good thermal performance for small die at low cost in volume. TSMC has said it intends to redistribute the die onto a silicon wafer for further processing. The IC giant started to ship its first small volumes of LED devices

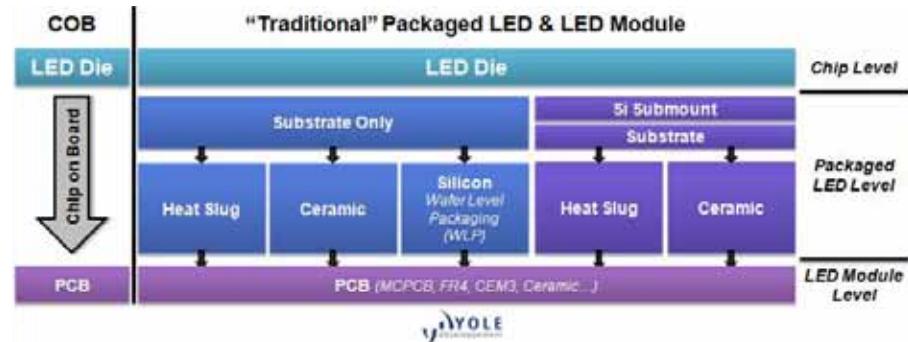


Figure 4: Trends in Packaging Substrates. SOURCE: LED Packaging, Yole Développement, 2012

this spring.

## Die Singulation Moves to Laser Processes

The drive to lower costs and higher volumes is driving the industry from mechanical towards laser dicing, even though the required upfront investment may be higher. Mechanical dicing causes a relatively higher degree of damage, and bad die in this early packaging step still bear the full cost of the rest of the packaging process. Inspection of die before packaging is, to date, only a very small trend, as dedicated equipment is not available, and it may seem more sensible to invest directly in improving the singulation process instead.

Though both the initial cost and operating costs are higher for laser than mechanical dicing, the clean edges with no kerf loss and no debris even on thick substrates give better light extraction and higher yields, so ROI is better as volumes increase. Demand is growing particularly strongly for stealth laser dicing developed by Hamamatsu, despite its nearly 5X higher initial cost, for the better throughput and yields at higher volumes. These stealth tools, supplied primarily by Disco, have been accounting for more than 35% of laser dicing equipment sold. Low cost blade dicing continues to dominate in volume, especially among new Asian entrants. Though the LED industry's excess production capacity has slowed LED tool sales in general, the shift to more expensive laser tools that can both scribe and dice has mitigated the slowdown in revenue for the singulation sector.

As usual with LEDs, the lack of standardization resulting in a wide variety of die sizes, substrates, and types of structures mean different tools will be best for different applications. Mechanical dicing solutions continue to improve, with new blades and processes, and will continue to be used for their low cost, good performance on GaAs-based LEDs.

Mechanical solutions — or new types of laser technologies entirely — may be the best solution for the increasingly common vertical LED structures, that may

sometimes be more difficult to dice with conventional laser tools, depending on the complexity of the structure. These LEDs can extract more light by removing the processed layers from the original sapphire substrate and bonding them instead to a conductive metal or silicon substrate, so the diode connections can be made on the top and bottom of the die, instead of side-by-side on the top surface and its mesa layer stack. Laser dicing through this bonded stack can impact the interior materials and reduce performance. Potential new solutions include serial multi-beam laser dicing (ALSI), parallel multi-beam laser scribing (Uni Via Technology), and thermal laser separation (Jenoptik), as well as some novel approaches to etching through the wafer. As with other LED process tools, most of the gains will likely go to the first successful supplier of a solution, and the rest to the second entrant; the market probably has room for at most two equipment makers in each niche.

## Profit Will Move Upstream in the Value Chain

We estimate that packaging currently accounts for a major part of the profits in the LED value chain, but the value opportunities will increasingly move upstream, from the die and the package, to the LED module and the LED-based lighting product. As has happened on the display side, LED die and packaging for lighting applications will likely become more standardized, and more new entrants from Asia will drive down margins, making LED die packaging into more of a commodity. But luminaires and systems will move to add new functionality, creating opportunities for suppliers of packaging materials such as optics and PCB materials at the module level. ☀

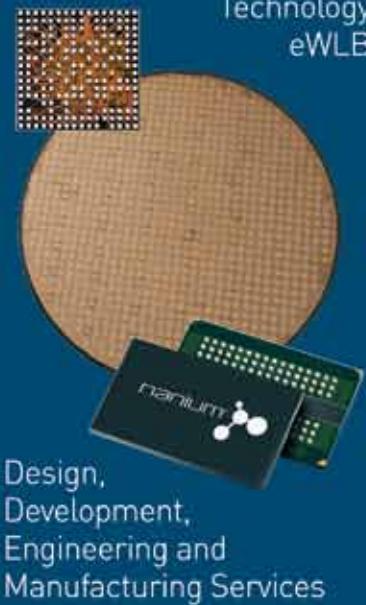
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# GUEST EDITORIAL



## Why Does it Take So Long to Introduce New Technologies? - A Lesson for 3D IC Adoption

By E. Jan Vardaman, Linda C. Matthew [[TechSearch International, Inc.](#)]

The demand for 3D ICs remains driven by performance such as high bandwidth between memory and processor and the need for lower power. While the drivers for 3D ICs remain constant, the time line for its adoption keeps shifting out. Why does it take so long to adopt a new technology? This article examines historical adoption of new technologies and looks at the specific case for the 3D IC with through-silicon via (TSV) technology. Technological and business issues are discussed.

### A History Lesson: Adoption of Flip-Chip Interconnect

Flip-chip interconnect was first introduced by IBM in the 1960s with the first application mounted on a ceramic substrate for a high-performance application. Automotive suppliers Delco in North America and Denso in Japan also adopted flip-chip in the same era. Mainstream flip-chip adoption, outside of captive operations, required the development of the industry infrastructure and introduction into a high-volume application to provide economies of scale to lower the cost of the technology. In the early days, barriers to the adoption included the availability of low-cost bumping services, difficulties with underfill, the availability of low-cost substrates, flip-chip bonding equipment, and merchant bump, assembly, and test service providers. Substantial improvements in industry infrastructure and process maturity, coupled with volumes driven by Intel's adoption of flip-chip on laminate substrates removed many of the barriers to widespread introduction of the technology. Infrastructure developments included the introduction of new, low-cost methods for wafer bumping,

an increasing number of subcontract assembly services with growing capacity, laminate substrate providers, and bumping for 300mm wafers. With substantial price declines for wafer bumping, assembly services, and laminate substrates, flip-chip moved into high-volume manufacturing[1]. The process took time and considerable resources from equipment and material companies. In 2002 flip-chip using solder bumps accounted for ~1.2% of total IC shipments and it has taken 10 years to reach a 5% market share (excluding wafer-level packages and gold bumping). Parallels in the adoption of flip-chip technology and the adoption of TSV technology have been drawn. A new technology introduction requires several steps: feasibility, niche applications, reliability, cost reduction, and high-volume production [2]. The availability of EDA tools is required for commercialization and in the case of flip-chip, designers had to learn to design in an area array layout instead of a peripheral layout to take full advantage of the technology. Fortunately the timeframe for new technology adoption is faster today, but it still requires time and resources. Adoption does not happen overnight.

### Early Adoption: A Case Study

In October 2010, Xilinx became the first company to announce a 3D IC product with the introduction of its 28nm Virtex-7 LX200T field-programmable gate array (FPGA). The high-capacity FPGA with 6.8 billion transistors was made possible by placing four FPGA slices side-by-side on a 65nm passive silicon interposer with through-silicon vias (TSVs). The new stacked silicon interconnect (SSI) provided an FPGA solution with lower latency, higher system bandwidth, and reduced

power through the elimination of I/O interconnect. The technology introduction allowed a faster time-to-market for a competitive product solution with more features and a longer lifetime. With the portioned design of four slices instead of a large single monolithic die, higher yield at the wafer-level was also achieved.

Development and product introduction required the commitment of time and resources over a five-year span ([see Figure](#)). The initial work for the Xilinx SSI technology started in 2006 as an R&D program. With management commitment, the work moved into the product group in 2008 and real product plans started. A major selling point was the idea that this would allow the company to reach a technology node with more features earlier than its competitors. Goals were established and careful thought was given to the project milestones. As each milestone was met, the plan moved forward.

One of the keys to the success of the SSI was the commitment to the design software. In conjunction with EDA tool vendors, Xilinx rebuilt development tools from the ground up. This included acquisitions of tools and internally rebuilt software. Reusable software IP is also attributed to the successful development to this product. It is also important to note that an FPGA is a unique device type that lends itself to partitioning, and as configurable logic, the ability to have a lot of testing inside the device. Along the way, the development team found solutions to challenges they were not expecting at the outset of the project. The moral of the story is that the management, resource, and time commitment paid off, but it did not happen overnight. Since the time for first introduction, Xilinx has introduced several successful new products

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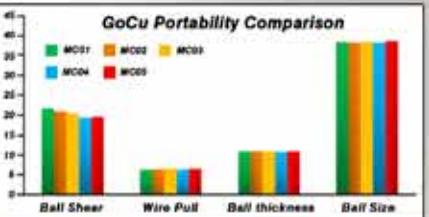
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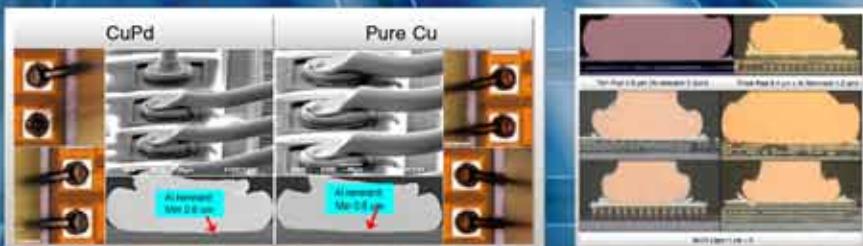
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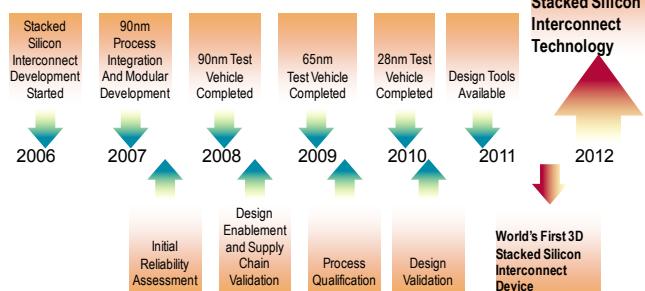
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Progression to Stacked Silicon Interconnect (SSI) Technology. SOURCE: Xilinx

## Moving to High-Volume Manufacturing

Major application areas for 3D ICs include memory stacks, memory and logic stacks, and logic stacks. Device types include flash, DRAM, processors, FPGAs, and other logic devices. Image sensors with backside vias are already in volume production in camera modules. Backside vias have been in production for MEMS for years. Power amplifiers with backside

vias are in production today, and many other device types will continue to make use of backside vias. The timing for 3D IC mass production depends on the development of the industry infrastructure, including EDA tools, equipment and materials to allow a high-yield manufacturing

process, test methodologies, thermal solutions, and a supply base. How the process compares in terms of cost and reliability with existing technologies is also a critical factor. In many cases, this means wire-bonded die stacking. While performance is a driver, cost is a limiting factor. Even with the advantages of 3D ICs, there are several challenges to the adoption of this new architecture. The industry is clearly focused on solving problems associated with improving yield and lower cost. Many standardization efforts are underway. 3D TSV is moving from PowerPoint engineering into real engineering, but it requires time and money before high-volume manufacturing (HVM) can be realized for 3D ICs.

## Obstacles to 3D IC Commercialization

Several technical challenges and infrastructure issues, such as business logistics, are delaying the full commercialization of TSV technology for 3D ICs. The major issues are: 1) EDA tool availability, including the ability to use thermally

aware tools and the ability to communicate between tools; 2) Manufacturing yield in key process steps, such as debonding during wafer thinning; 3) Thermal dissipation and cooling methods; 4) Test methodology; 5) Infrastructure-related issues, including logistic supply chain handoff; 6) Reliability data for a broad range of applications; and 7) Unit device cost compared to alternatives.

## Summary

Once the 3D TSV technical challenges are resolved and the technology becomes cost-effective, business challenges will remain until the industry settles on a model. As the boundary between foundry and assembly processes continues to blur, there will be a struggle to determine which organizations can best meet the customer's needs for assembly and test. Any one of these issues has the potential to limit a full 3D TSV implementation, and these challenges are driving many companies to seek alternative packaging and assembly solutions until they can be solved [3]. 3D ICs will be deployed in commercial products, but realistic expectations are advised and resource commitments are required. ☀

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## Biographies

E. Jan Vardaman received her MA from the U. of Texas and is the president of TechSearch International, Inc.; email [tsi@techsearchinc.com](mailto:tsi@techsearchinc.com)

Linda C. Matthew received her BS and MS degrees in materials science and engineering from the Massachusetts Institute of Technology, and is a senior analyst at TechSearch International, Inc.

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## Happy Birthday AIA: One Year After

By Jason Mirabito [Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C.]

**A**s reported in this column about a year ago, on September 16, 2011 President Obama signed the Leahy-Smith American Inventors Act, known as the AIA. This is the most comprehensive patent reform legislation since 1952. Some of the provisions of the AIA did not come into effect until just recently, on September 16, 2012. This column will concentrate on some of those enactments which may affect a patent both before and after issuance. Among the changes that came into effect on September 16, 2012 are: a) Pre-issuance Submissions, b) Supplemental Examination, c) Post-Grant Review, and d) Inter Partes Review.

The purpose of the above provisions is to assure that patents that are issued by the U.S. Patent and Trademark Office (USPTO) are valid patents. The four provisions aim to promote valid patents by allowing submissions, both by the inventors as well as by third parties, either before or after issuance of the patent to ensure that all relevant prior art has been before and considered by the Patent Office. This is due, at least in part, to a perceived problem that the patent examiners might not have before them the most relevant prior art.

### Pre-issuance Submissions

The AIA allows a third party to submit certain types of prior art to the USPTO to consider and to include in the patent application file wrapper. The scope of the submission is somewhat limited in that only patents, published patent applications and other printed publications may be submitted during the time of the pendency of an

application. The submitter is required to describe the relevance of the submissions, pay a USPTO fee and include a statement by the submitting person that the submission is in accordance with the law and the rules of the AIA. The perceived purpose of this Pre-issuance Submission is to allow the USPTO to decide whether to allow or reject the application prior to its issuance so as to avoid a third party having to go back to the USPTO after a patent has been issued.

### Supplemental Examination

After a patent has been issued, a patentee will now be permitted, again starting on September 16, 2012, to request supplemental examination and present to the USPTO information that may be relevant to the patentability of the invention. For example, if a patentee has become aware of prior art after the patent has issued, the inventor can submit the prior art to the USPTO with the goal of determining whether the recently discovered prior art is relevant or not relevant to its patentability. In order to control the amount of such submissions, the submitter must convince the Patent Office that there is a substantial new question of patentability that is raised by the submission being made. This provision has just come into effect and it will be interesting to see how many submissions will be made under this provision.

### Post-Grant Review

Up until the present time, there has been no comprehensive procedure (with the exception of reexaminations) other than litigation for a third party to

challenge the validity of the patent on any and all grounds possible. The Post-Grant Review procedure, which went into effect on September 16, 2012, allows, for a period of nine months after the issuance of the patent, a third-party to provide any type of evidence why a particular patent should not have issued. This may include prior art but may include other purported frailties of the patent. In order to start a procedure under the Post-Grant Review, a third party must file a petition but also must be able to show that more likely than not at least one of the claims challenged in the petition is not patentable. It should be mentioned that the Post-Grant Review does not really come into operation for a few years, because it only applies to those patents applied on or after March 2013. Since the period of pendency of patent applications is (usually) two or three years, Post-Grant Review petitions will likely not be filed until 2015 or so.

### Inter Partes Review

The Inter Partes Review, as discussed in the earlier column in this review, is a modification of the existing, now superceded Inter Partes Reexamination procedure. Under the Inter Partes Review, petitions may be filed any time following nine months after a patent issues (and thus after the post-grant review period has expired). In the Inter Partes Review, a fast track system has been established by the USPTO so that an Inter Partes Review generally commences and ends within one year. Like its predecessor Inter Partes Examination, the Inter Partes Review is limited to patents, patent

applications and other published prior art that the petitioner seeks to use to invalidate the patent in question. The standard for grant of the petition under the Inter Partes Review is in fact different from that of the Post-Grant Review. In a Post-Grant Review, the petitioner must demonstrate that it is more likely than not that at least one of the claims challenged in the petition is unpatentable. In an Inter Partes Review, the petitioner must demonstrate a reasonable likelihood that the petitioner will prevail as to at least one of the claims challenged. Thus, while it is felt that the standard for the Inter Partes Review is less than that of the Post-Grant Review, only time will tell as the USPTO accepts both of these and progresses with them.

**One final note on Ex Parte Reexamination.** The Ex Parte Reexamination provision, which has been in effect for dozens of years in

the U.S. patent system, is relatively unaffected by these other changes. Under the Ex Parte Reexamination statute, petitioners can petition the Patent Office to open a reexamination procedure, again based, like Inter Partes Review, on printed publications, issued patents and published applications, but the standard of review is in fact different from either the Post-Grant Review standard, or the Inter Partes standard. The standard for Ex Parte Reexamination is whether the petition raises a new substantial question of patentability of one or more claims of the patent at issue.

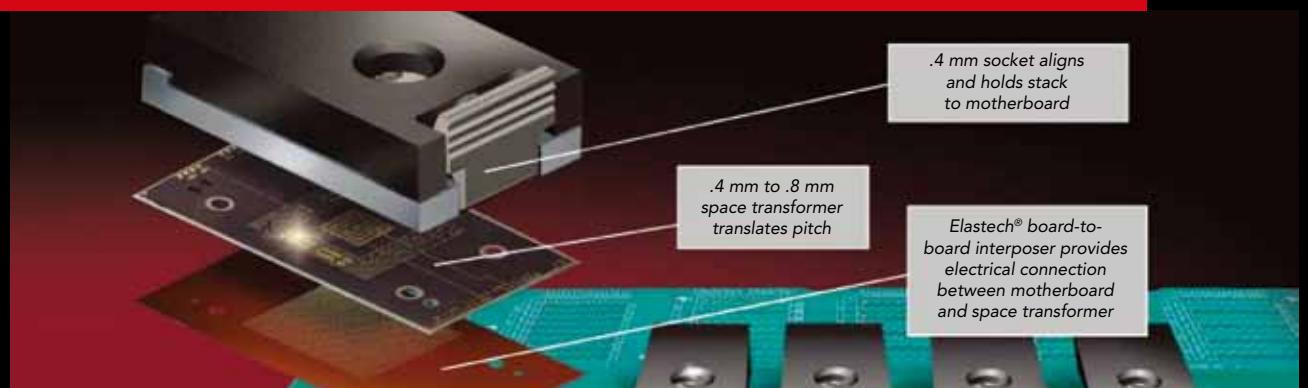
At least one of the purposes of the new provisions (i.e., Pre-Issuance Submissions procedure, Supplemental Examination procedure, Post-Grant Review, Inter Partes Review, and Ex Parte Reexamination) is to shift determinations of validity of a patent from the court system to the USPTO, the presumed expert in determining validity

of a patent. In patent litigations today, invalidity is almost always raised as a defense by an accused infringer, so that now various procedures are available to allow the accused infringer to bring the patent back into the USPTO to be rejudged, so to speak, as to its validity. It will be interesting over the next several years to see how many of these petitions will be filed, but even at this early date, a number of petitions under Inter Partes Review have already been filed, so the USPTO can be expected to be very busy! 

### Biography

Jason Mirabito received his BS degree in engineering physics from New York U., a JD from American U., and an LLM degree from Georgetown Law Center. He is a registered patent attorney and a member of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C.; email JMirabito@mintz.com

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# INDUSTRY NEWS

## STATS ChipPAC Announces Expansion Plans in South Korea

STATS ChipPAC Ltd. announced plans to expand its semiconductor assembly and test operation in South Korea. The company has signed a non-binding memorandum of understanding to invest in a new integrated facility in



Current Stats ChipPAC Facility in South Korea

the Incheon Free Economic Zone, an international business district located in the Incheon metropolitan area that is adjacent to Seoul, South Korea.

The integrated facility will include approximately 95,000 square meters (1 million square feet) of land with options for future expansion. The integrated facility will be used for manufacturing, research and development, and administration. Construction is scheduled to begin in the third quarter of 2013 and the new facility is expected to be operational in the second half of 2015. STATS ChipPAC intends to integrate its existing facilities in South Korea into the new, larger facility to achieve a more efficient, cost effective manufacturing flow and provide flexibility for future expansion.

## Sensata Acquires Wells-CTI's Burn-in Test Socket and Thermal Control Lines

As of October 1, Sensata Technologies acquired the burn-in test socket and thermal control product lines of Wells-CTI. The product lines

will be incorporated into Sensata's Qinex business, which is part of Sensata's Controls business segment. David Barnum, manager of the global Qinex business, told CSR, "We were interested in the product lines because WELLs-CTI's products are largely complementary to BiTS products

produced by Sensata, enabling Sensata to grow its BiTS business and to expand our expertise into thermal controls that are often used in conjunction with current Sensata Qinex BiTS products."

According to Sensata, the purchase combines WELLs-CTI's strength in logic and Sensata's strength in memory, resulting in

a more diversified customer base for the combined business. Sensata was spun off from Texas Instruments in 2006; it went public in 2010 and employs about 11,400 people in 11 countries.

## Save the Date - 2013 BiTS Workshop

Preparations are well underway for the Fourteenth Annual Burn-in & Test Strategies Workshop (BiTS), March 3–6, 2013 at the Hilton Phoenix East/Mesa Hotel.

BiTS is the world's premier event for what's Now & Next in Burn-in and Test of packaged ICs. The Technical Program includes Presentations & Posters covering a range of important topics, a Tutorial and TechTalk featuring expert instructors and renowned Speakers sharing their insights on prominent industry topics. At the BiTS EXPO, attendees can browse, explore and chat with knowledgeable representatives from a collection of global companies showcasing their package burn-in and test products and services.

Networking opportunities are



Burn-in & Test Strategies Workshop

plentiful with numerous meals, breaks, and receptions that give attendees the opportunity to compare notes with colleagues from around the world while soaking up the Arizona sunshine.

EXPO registration is open; attendee registration opens in December. Visit the BiTS website for details – [bitsworkshop.org](http://bitsworkshop.org).

So, save the date: the 14th annual BiTS Workshop – March 3–6, 2013 in Mesa, AZ.

## M+W Group Is Associate Member for Facilities and Infrastructure of Global 450 Consortium

M+W Group (M+W) has been selected by the College of Nanoscale Science and Engineering (CNSE) of the University at Albany, United States, to be an associate member for facilities and infrastructure for the Global 450mm Consortium (G450C). M+W will spearhead development of new facility and infrastructure technologies and manage building and facility suppliers selected to participate in the G450C program.

According to Rick Whitney, CEO M+W US, a safe and sustainable environmental footprint is a key focus area for the facility program. The eco-friendly mandate calls for solutions that reduce energy and water consumption, and minimize the generation of waste throughout the facility life cycle. The G450C partnership enables the company to align on facility standards with other industry forums and drive operational cost and duration improvements that provide a competitive advantage to the consortium members, noted Whitney.

Announced by New York Governor Cuomo in September 2011, the

G450C's main objective is to enable the transition from existing 300mm wafer size production to the new 450mm technology. Managed by New York State through CNSE, the founding members of G450C are Intel, IBM, Globalfoundries, TSMC and Samsung.

M+W Group and the G450C will work with facility suppliers selected from among the top-tier providers of critical semiconductor facility components, systems, and services. These suppliers will be designated as "G450C Affiliate Participants," providing a unique opportunity to leverage the strengths of the broader membership in order to provide facility solutions that are essential to industry growth and the 450mm transformation, and lead to tens of millions in additional private investments in G450C and New York State.

The G450C headquarters and core operations are located at CNSE's Albany NanoTech Complex, within the new NanoFab Xtension (NFX) building that is currently being constructed by M+W. NFX will provide 60,000 square feet of state-of-the-art contiguous cleanroom space, with completion scheduled for the end of 2012.

### Singapore Salutes Scientists at the President's Science and Technology Awards Ceremony

Singapore's highest awards for scientists were presented at an award ceremony for the President's Science and Technology Awards 2012 (PSTA) on October 30, 2012 at Singapore's Ministry of Trade & Industry.

This year, three different awards were presented, among them was the President's Science and Technology Medal (PSTM), which was awarded to Professor Dim-Lee Kwong, Executive Director of the Agency for Science, Technology and Research's (A\*STAR)



Prof. Dim-Lee Kwong

Medal (PSTM), which was awarded to Professor Dim-Lee Kwong, Executive Director of the Agency for Science, Technology and Research's (A\*STAR)

Institute of Microelectronics (IME). Prof. Kwong has played a pivotal role in developing the science and engineering landscape in Singapore since 2001, especially in the semiconductor industry, through promotion and management of microelectronics R&D. As a result of his strategic efforts, IME has attracted collaborations with numerous multinational companies, many of which are global leaders of the semiconductor industry. A major outcome of IME's research is the establishment of the US\$100M Centre of Excellence (COE) in Advanced Packaging in Singapore in 2012. The COE is jointly established by IME and Applied Materials Inc.

### Yole Updates Its Temporary Bonding Equipment and Materials Market Forecast

Yole Développement announced the update of its Thin Wafers, Temporary Bonding Equipment & Materials Market forecast. According to the market research firm, there is definitely a growing need for thin wafers (below 100µm) for numerous applications: 3D ICs, MEMS, CMOS image sensors, power devices, LEDs, RF devices, memory and logic, interposers, and photovoltaics. The firm believes that by 2017, the ratio of thin wafers vs. total

number of wafers (in 300mm eq.) will be 74%, corresponding to >80M 12" eq. wafers (see **Figure**). In particular, Yole pointed out that the CIS BSI application is the big driver for ultra-thin wafers: 2011 was a big year for 300mm wafer bonding tools because of BSI - an application that requires ultra-thin layers (<10µm) on 12".

Yole analysts pointed out that as wafer thickness decreases to 100µm and below, manufacturing challenges arise. Ultra-thin wafers are less stable and more vulnerable to stress, and the die can be prone to breaking and warping—not only during grinding but also during subsequent processing steps.

In 2017, most of the 12" wafers will be 200µm thick for logic application; also, most of the thinned wafers will be in the 10-99µm thickness range. This includes memory, as well as interposers and power device applications.

Currently low in value, the temporary bonding equipment market will reach US\$250M by 2017. According to the research firm, thin wafer handling will enjoy increased importance in the coming years, but as chips get thinner and wafer diameter increases, thinning/handling procedures are required. "This implies development in wafer thinning, wafer dicing and wafer temporary



**Figure:** MEMS & Sensors. Thin wafer shipment 2011-2017 forecast in 300mm eq. by application. SOURCE: Thin Wafers, Temporary Bonding Equipment & Materials Market report, October 2012, Yole Développement

bonding," said Eric Mounier, Senior Analyst MEMS Devices & Technologies at Yole Développement.

Yole's updated temporary wafer bonding equipment forecast shows that 10% of the total thin wafer shipment will experience a temporary bonding step by 2017. So, while temporary bonding equipment is still a small market today, it is expected to grow as the need for thin wafer handling grows. Yole estimates the market for temporary bonding tools to be more than \$250M by 2017. Currently, shipped bonder/debonders are for power and 3D ICs applications. However, the research firm believes that 3D ICs will become the predominant application for temporary bonders beyond 2015.

### Expansion and Planned Acquisition Broaden Horizons for Touch International

Touch International, Inc., announced its planned acquisition of a former Taiwanese touch screen company, as well as the continued expansion of its manufacturing facilities in Zhongshan and Shenzhen, China. The new development will further complement the Austin, Texas facility with added capacity and extended manufacturing capabilities.

The purchase will encompass all of the Taiwanese company's touch screen technology, equipment and raw materials, which will be used in a 5,000 ft.<sup>2</sup> extension of the facilities that will broaden Touch International's value-added enhancement and touch screen manufacturing abilities. Equipped with a Class 10,000 clean room, the new areas will house additional cover lens manufacturing capabilities, a second optical bonding team, and a line designated for contract manufacturing assembly.

Michael Woolstrum, co-founder and CEO of Touch International, noted that the acquisition of these assets will further complement the company's vertically integrated system in its

Shenzhen facility by increasing the capacity of its touch screen, cover glass and LCM (touch screen module) manufacturing lines. He also said that the company will be able to speed up production and reduce cost for its customers in specialized industries. As

part of a \$10 million expansion effort and technology development plan, the progressive improvements are aimed at bolstering touch screen production, reducing prices and shortening delivery times. The continuation of growth is the next step after the complete renovation

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of the Austin factory clean room and the opening of the Shenzhen manufacturing facility in 2011.

According to Woolstrum, touch technology and display enhancements will continue to grow and mature in specialized industries such as military land vehicles, airplane cockpit control, and advanced medical devices. He commented that with the demand in these markets on the rise, the company needs to evolve with the market and position itself to accommodate increasingly strict requirements and regulations.

### ePAK International Enforces Patent Rights Against TexChem Advanced Packaging Products

ePAK International, Inc. has announced that it has filed a lawsuit in California against TexChem Advanced Packaging Products alleging infringement of ePAK's patent related to its line of eLX™ Zero-Movement semiconductor wafer handling and transport canisters.

ePAK has asserted that TexChem's 300mm HWS-RM Horizontal WaferShipper™ infringes ePAK's US Patent 6,988,620 entitled "Container With an Adjustable Inside Dimension That Restricts Movement of Items Within the Container."

ePAK is seeking an injunction to stop TexChem from producing or selling infringing containers.

### Atotech Collaborating with SEMSYS CO on Optimized Electroless Plating

SEMSYS CO and Atotech have collaborated to develop and deliver an integrated solution for optimum electroless plating in advanced packaging technologies. Atotech's Xenolyte product line will be paired with SEMSYS CO's electroless plating system, GALAXY, to deliver a pad metallization process with high throughput and fine line capability.

The goal of the cooperation is to combine the best of two production

methods – the high throughput achieved with wet bench plating and the successful plating of fine lines typically achieved in a batch spray tool. This technology will encompass a spray batch pretreatment, followed by the electroless plating of nickel, palladium and (if needed) immersion gold in a wet bench system. The final rinsing and drying will take place in a designated Spin Rinse Dryer (SRD) chamber. The ancosys ancolyzer on-line system will be used for monitoring and dosing the plating bath compounds. The system will be fully automated and will be optimized for easy maintenance and cleaning.

The first GALAXY test lines have been installed at Atotech's Semiconductor Technology TechCenter in Berlin, Germany. Research and development for the next smaller structures on the electroless modules for nickel and palladium are currently underway. The estimated release date for commercial availability is the second quarter of 2013.

### Soitec and Shin-Etsu Handotai Announce Smart Cut™ Licensing Extension and Expanded Technology Cooperation

Soitec and Shin-Etsu Handotai Co., Ltd (SEH), announced a Smart Cut™ licensing extension and expanded technology cooperation agreement. The new partnership includes an extended 10-year licensing agreement between the two companies and establishes a new level of joint technology cooperation. It will facilitate the development and wafer supply of silicon-on-insulator (SOI) wafers to meet major market opportunities such as SOI for RF devices, FinFETs on SOI, and fully-depleted (FD) planar circuits. According to the companies, the partnership represents a step forward in the supply chain and ecosystem that will enable the next-generation of technologies on an optimized SOI wafer from two independent suppliers collaborating at the R&D level. It will also accelerate

time-to-market for breakthroughs at a material level.

The agreement is a licensing extension that expands the scope of the partnership between Soitec and SEH, including cross-licensing Smart Cut related patents between the two companies. As a result of the agreement, SEH will continue to use Smart Cut technology to manufacture SOI wafers, and now will be able to extend its Smart Cut manufacturing capabilities to other materials, a trend commonly referred to as silicon-on-anything or SOA (any material on top of which there is a thin film of plain silicon), which will allow SEH to further expand its scope of applications.

### NANIUM Passes Production Milestone: 200 Million eWLB Components Shipped in Less than Two Years

NANIUM has announced that it has shipped its 200 millionth eWLB component for wireless communications and other applications - a goal reached in less than two years. The 300mm embedded wafer-level ball grid array technology (eWLB) uses a combination of traditional front-end and back-end semiconductor manufacturing techniques with parallel processing of all the chips on the wafer, leading to more cost-effective manufacturing. With an increased level of integration of the silicon's overall protective package and a dramatically higher number of I/Os per area, this technology provides significant cost and size benefits for manufacturers of cutting-edge wireless and consumer products.

The company has recently adapted its eWLB technology for consumer MEMS, stacked-die DRAM multi-chip packages (MCP) for high-capacity memory applications, mixed-signal RF ASIC with high power dissipation, and heterogeneous integration within system-in-package (SiP).

The 10% year-over-year productivity increase also reflects full conversion

to NANIUM's eWLB over mold technology that allows both thinner and more robust packages. The company completed its ramp up of volume capacity for 300mm eWLB wafers in late 2010.

### Silicon Europe: Cluster Alliance for European Micro-and Nanoelectronics Industry

Four of the leading micro- and nanoelectronics regions in Europe are joining forces to form the transnational Cluster Alliance 'Silicon Europe – The Leaders in Energy Efficient ICT Electronics.' The cluster partners from Germany, Belgium, France, and the Netherlands are linked by a common goal: to secure and expand Europe's position as the world's leading center for energy efficient micro- and nanoelectronics and information and communications technology (ICT). To reach this goal, Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France) and Point One (Eindhoven/Netherlands) are cooperating in research, development and business expertise. Together they represent about 800 research institutes and companies, which account for more than 150,000 jobs. Among the companies are global market leaders such as Philips, NXP, Globalfoundries, Infineon, STMicroelectronics, Schneider Electric and Thales. This makes Silicon Europe one of the largest technology clusters of the world.

### ON Semiconductor Joins imec's GaN-on-Si Research Program

ON Semiconductor (Nasdaq: ONNN) has joined the multi-partner, industrial research and development program at imec to collaborate on the development of next-generation gallium nitride (GaN) on silicon (Si) power devices.

GaN is characterized by superior electron mobility, higher breakdown voltage and good thermal conductivity properties, making it ideal for power and radio frequency (RF) devices that need high-switching efficiencies. Today, GaN-based power devices are too expensive for large volume manufacturing, as they are fabricated on small diameter wafers using non-standard production processes.

Imec's research program is focused on developing GaN-on-Si technology on 200mm wafers, as well as reducing the cost and improving the performance of GaN devices. Last year, the program successfully produced 200mm GaN-on-Si wafers, bringing processing within reach for standard high-productivity 200mm fabs. Moreover, imec developed a fabrication process compatible with standard CMOS processes and tools, the second prerequisite for cost-effective processing.

### Dow Corning Electronics Solutions Reinforces European Services through Expanded Relationship with Biesterfeld and Ellsworth

Dow Corning announced that it has expanded its relationship

The advertisement features the Brewer Science logo at the top, consisting of a stylized hand icon above the company name "brewer science". Below the logo is a photograph of a person's hands carefully handling a thin, curved silicon wafer. The text "ZoneBOND® technology" is overlaid on this image. Further down, the text "The proven thin-wafer-handling solution" is displayed. On the right side, there is a vertical column of headings: MATERIALS, PROCESSES, EQUIPMENT, followed by a downward-pointing arrow, then SILICON, COMPOUND SEMICONDUCTOR, and MEMS, each separated by horizontal lines. At the bottom right is a QR code. The footer contains the text "Contact Brewer Science for your product or process needs" and the website "www.brewerscience.com".

with two proven and longstanding distributors, Biesterfeld SpezialChemie GmbH based in Hamburg, Germany, and Ellsworth Adhesives based in Germantown, Wisconsin, USA. Under the expanded collaboration, Dow Corning is reinforcing the support and value of its electronics portfolio offered to customers in strategic European markets.

According to Jean-Louis Lenoel, Channel Manager Europe for Dow Corning, the company is committed to building strong Pan-European distribution channels.

A rapidly growing European distributor of specialty chemicals, Biesterfeld SpezialChemie is a trusted and longstanding partner of Dow Corning Electronics business. Under its broadened agreement with the company, Biesterfeld will expand its current distribution services to customers in Poland, Ukraine, Bulgaria, Croatia and the Czech Republic, to also offer Dow Corning's solutions to electronics manufacturers in Germany, Switzerland and Austria.

A global corporation specializing in the distribution of specialty chemicals and equipment, Ellsworth has long been a distributor of Dow Corning solutions in the Americas, Greater China, Australia/New Zealand and several Western European countries, including the U.K., France, and Spain. In its expanded role, Ellsworth will deepen access to Dow Corning's advanced product portfolio to customers in the countries of Norway, Sweden, Denmark and Finland.

### **Endicott Interconnect Technologies, Inc. Promotes Rajinder Rai CTO**

Endicott Interconnect Technologies, Inc. (EI) has promoted Rajinder Rai Chief Technology Officer (CTO) reporting to James J. McNamara Jr., President and CEO. In his new position, Rai will be responsible for monitoring new technologies, overseeing the selection of research projects, generating



Rajinder Rai

a technology roadmap and ensuring its progress and assessing the potential of new product introduction.

Rai brings 16 years of experience in the high-tech electronics industry. He has held a variety of senior design and development engineering positions as well as various senior management and executive roles, most recently as Vice President of Engineering at EI. He has been successful and possesses particular expertise in driving new business opportunities, most recently through EI's Integrated Circuit and Assembly Services (ICAS) business.

Rai holds a BS in materials science and engineering from the University of Notre Dame, and an MS in materials science from Stevens Institute of Technology. He has been issued 6 US patents and authored more than 25 technical papers over the course of his career.

EI's former CTO, Voya Markovich, retired on September 28, 2012.

### **Job Elders Joins Xsens**

Xsens has appointed Job Elders as Senior VP Strategic Alliances. Elders joins Xsens as the company expands its business model with focus on sensor fusion software for consumer electronics. MEMS industry

veteran, five-time entrepreneur and MANCEF founder, Job Elders also made a significant equity investment in the company.

Xsens is a supplier of business-to-business motion tracking software and systems, and has a proven track record in mission critical applications in industrial applications, game and film industry, and movement sciences. With Elders on board, Xsens adds the

focus of licensing its motion tracking software to the consumer electronics industry enabling, among others, natural user interfacing, context awareness, and location-based services.

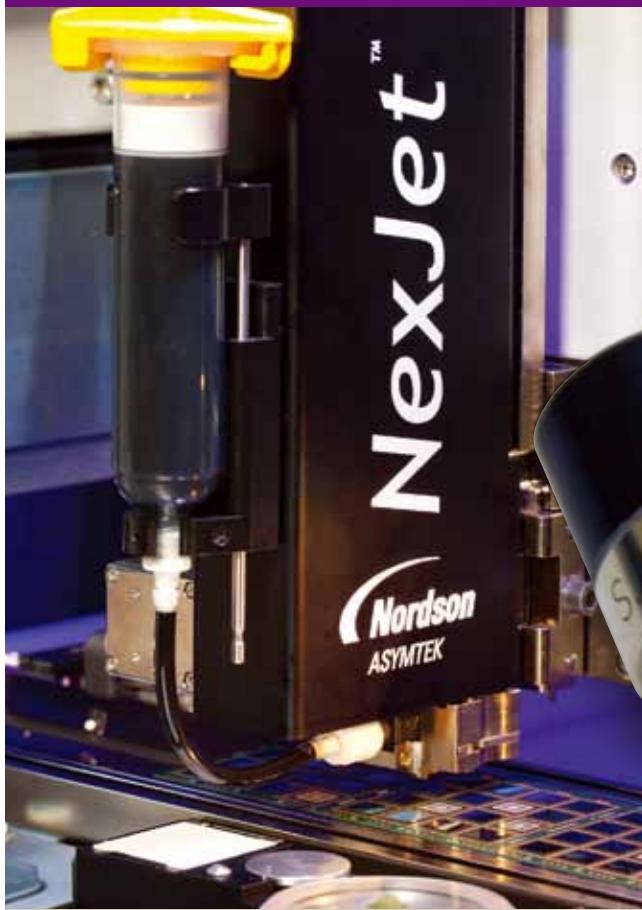
Job Elders is chairman and a board member of several high tech companies and director of Zinnergy innovation fund. Previously, he has founded and developed five MEMS companies including C2V which was acquired by Thermo Fisher Scientific. He was founder of TMP and served as TMP's Managing Director and he served as VP and GM of Alcatel Optronics Netherlands after Alcatel's acquisition of the operations in 2001. Job Elders was founder and board member of the MANCEF foundation, as well as founder of the Point One foundation and member of its board until 2010. He is the author of more than 80 technical and business publications, as well as patents, and has chaired and spoken at several MEMS events. He received his PhD in physical chemistry from the University of Amsterdam.

### **Jonathan Doan Joins Nordson MARCH as Director of Marketing**

Nordson MARCH announced the appointment of Jonathan Doan to the position of Director of Marketing. Doan will drive the product roadmap and develop new marketing programs to promote the company's plasma treatment systems for the semiconductor, printed circuit board, life science, hard disk drive, LED, and solar/photovoltaic industries.

Doan has extensive global technology and marketing experience, most recently as Director of Product Management and Marketing for Excico in Paris, France. He holds an MBA in Global Business from St. Edwards University, a BS degree in Marketing from the University of Texas, and a BS in Chemical Engineering from Texas A&M University. The Texas A&M University logo, which is a blue circular emblem with the letters "TAMU" inside.

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# 3D IC Thin-Wafer Handling Materials Requirements

By Mark Privett *[Brewer Science, Inc.]*

## T

he need for 3D integration has been widely reviewed in the literature for quite some time. Overcoming the challenges for high-volume 3D integration will require cooperation across many functions in the semiconductor supply chain, as well as new technology development in several production areas. Although included within those challenges, materials requirements for thin-wafer handling have had limited review [1]. Industry experts state that the material must survive thinning, passivation, metal layer deposition, and patterning in order to redistribute I/O locations, and then be easily removed for final package assembly. However, these applications requirements do not clearly define what material properties are necessary.

Although several materials and material families meet thinning and removability requirements, process flows between thinning and final cleaning remain inconsistent from fab to fab and from one outsourced semiconductor assembly and test (OSAT) service provider to another. This article describes the base process flow for mounting a wafer to a carrier, final separation of the thinned wafer from that carrier, and cleaning of the wafer. Material requirements for full backside processing are discussed, and the capabilities of the currently available material sets and processing of the same will be demonstrated.

## Overall Process

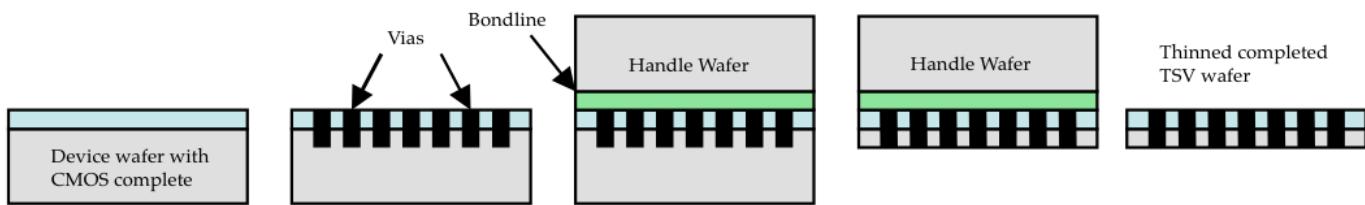
At this time, the most popular way to complete through-silicon vias (TSVs) and enable three-dimensional stacking of chips is the use of a via-middle process flow [2]. The device wafer is finished with completed blind vias in the full-thickness wafer. These vias are etched and filled to a depth equal to or slightly greater than the desired final device thickness. Upon completion of the CMOS circuitry portion of the device and the creation of the blind vias, the device is thinned to expose the blind side of the vias as a copper nail (**Figure 1**). It is critical that the thinned wafer have very uniform thickness because thinning may damage the device. If vias are exposed prematurely during the thinning process, particularly during the grinding process, copper may be smeared across the device and damage it. Manufacturers want thinned wafers to have a total thickness variation of no more than 4 $\mu\text{m}$ , preferably less than 2 $\mu\text{m}$ .

To create through-silicon interconnects, the CMOS device is mounted temporarily to a rigid carrier for thinning and also so that I/O may be routed to match the needs of the chip upon which it will be stacked. The thinning typically starts with a mechanical grinding process to thin the wafer from its standard thickness, e.g., 775 $\mu\text{m}$  for a 300mm wafer, to within 10 $\mu\text{m}$  of the final device wafer

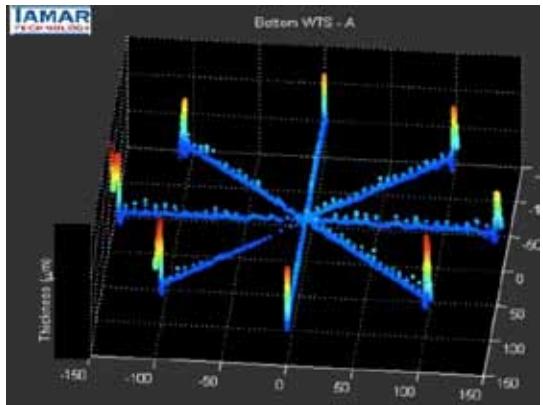
thickness, e.g., 50 $\mu\text{m}$ . Wet etching or deep reactive ion etching (DRIE) processes are used to complete the thinning and expose the copper nails for final re-distribution layer (RDL) creation. Grinding is significantly faster than etching; therefore, manufacturers want to grind wafers as much as possible before etching. However, the grinding wheels must not come in contact with the copper or the copper will be smeared across the wafer.

## Bonding

Materials used to bond the device wafer to the rigid carrier are typically spin applied to the device, which is then bonded to the carrier at a specific temperature and with a specified pressure. Bonding material must cover any topography on the device surface, and the bond line must have very uniform thickness so that the grinding and etching processes expose the copper nails uniformly. Device topography varies significantly from one device design to another and may range from 1 or 2 $\mu\text{m}$ , to more than 80 $\mu\text{m}$  in cases where solder bumps are used as interconnects. To create such thick coatings, bonding materials are generally quite viscous (a few thousand centipoise), and even then slow spin speeds must be used to get desired coating thicknesses. These slow spin speeds result in thick material at the edge of the wafer that may be double



**Figure 1:** Via-middle process.

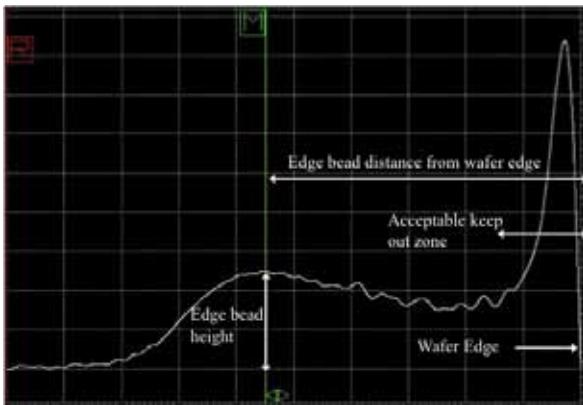


**Figure 2:** a) (left) Edge beads as measured by interferometer, and b) (right) by profilometer. Interferometer photo courtesy of and used by permission of Tamar Technologies.

the thickness of the bonding material in the center (**Figure 2**). The thicker bead of material can cause a greater space between the carrier and the device wafer at this edge and during grinding can cause the edge of the device wafer to be thinned to a greater degree than the center planar area. Vias at the edge may be revealed too soon and may be deformed or smeared by grinding.

Novel dispense, spin, and bake sequences have been developed, and materials suppliers must assist in optimization for the tool of choice to minimize edge bead and move it as far to the edge of the wafer as possible and maximize the wafer utilization. Additionally, next-generation bonding materials and application processes are being developed to simplify the entire process flow for temporary bonding and to significantly reduce bonding material total thickness variation.

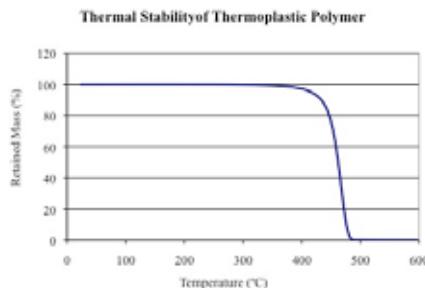
Another critical bonding material requirement is that the bond line must contain no voids. Many of the bonding materials in use for temporary bonding are thermoplastic polymers in a solvent carrier. The solvent must be baked slowly out of thick polymer coatings so the solvent diffuses through the polymer without producing bubbles that aggregate and form a blister in the coating. Bonding material voids resulting from poor dispense setup or rapid baking may cause device thickness non-uniformity to be created during thinning. Even more importantly, air trapped in these voids expands in a high-temperature, low-pressure environment



and can rupture the thinned wafer. Initial bond quality may be tested using scanning acoustic microscopy (SAM) to ensure a void-free bond line.

### I/O Rerouting

After thinning, during I/O rerouting, the thinned wafer undergoes several high-temperature, low-pressure processes such as chemical vapor deposition (CVD) and sputtering [3]. A typical process flow includes surface passivation, metal sputtering, plating, and then etching to reroute I/O, a second round of passivation on the patterned metal, and, finally, interconnect creation with the placement of solder bumps. The bonding material must survive these processes, so the material must be thermally stable, as usually measured by thermogravimetric analysis (TGA; **Figure 3**), to temperatures significantly higher than chamber temperatures. No degradation of the polymer that results in weight loss should occur in these chambers. The material must also be chemically stable to resist degradation by etching chemistries.



**Figure 3:** TGA analysis of a polymer. As temperature is raised, no mass loss is seen until 400°C.

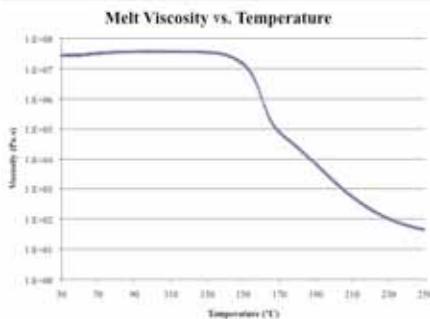
The polymeric bonding material must provide mechanical support for the thinned wafer through all processing steps, from the time the wafer is bonded to the carrier, to the time it is released from the carrier. During initial processing, the wafer undergoes a number

of high-temperature processes to create circuitry and eventually to create the I/O contact points on the device surface. Several layers of metal and dielectric are deposited on the surface of the wafer, often at high temperatures. When the device then cools, these layers become highly stressed because their coefficients of thermal expansion (CTEs) differ from that of the silicon wafer. Metal layers have higher CTE than silicon, while insulating layers have lower CTE. With the full thickness of the wafer, say 775µm, the wafer remains flat when stressed, although some degree of bowing may occur across the wafer. Deposited layers are designed to keep stress low to limit bowing to less than 100µm as well as to permit further wafer handling using edge grip or vacuum end effectors.

To make through-silicon vias cost effective however, the wafers must be made significantly thinner, to about 50µm, leaving significantly less silicon crystal to hold the wafer flat. As an analogy, one could consider this similar to removing 22.5 inches of a 24-inch beam holding up a ceiling or bridge; only 1.5 inches remain to hold that bridge flat. A bridge is held flat and supports the stress created by the weight it bears by using the full 24-inch beam cross section. If the beam was thinned to 1.5 inches, the stress of the weight on the bridge would bend and even break the bridge. The 22.5 inches of material removed from the beam is similar to the 725µm of silicon that are to be removed from the wafer.

Mechanical support for the thin wafer on a carrier may be provided in either of two ways. For a thermoset material, the mechanical support is provided by adhesion to the surfaces of the carrier and the device and the strength of the thermoset layer. Because a thermoset material remains a solid, it must also be compliant enough to allow for some expansion of the thinned wafer on the carrier. These compliant thermoset polymers also expand greatly with temperature and therefore may create an additional stress imbalance.

Conversely, a thermoplastic material allows for some movement as needed at high temperature. Thermoplastic material properties vary with temperature as the material changes from a rigid solid at low temperatures to a soft solid and finally to a highly viscous fluid at higher temperatures, as shown by the melt rheology curve in **Figure 4**. This property change permits rigid support at room temperature and then compensates for the CTE mismatch between the carrier and the device wafer during high-temperature backside processing. The material must provide bonding material support below its softening point and hydraulic support above its softening point.



**Figure 4:** Rheology of a thermoplastic polymer. The example material is solid up to ~150°C and changes to a thick liquid above that temperature.

## Separation from Carrier

Finally, after completion of all thinned wafer backside processing, the carrier and the bonding material must be removed from the thinned device. Three principal methods for this separation are currently in use: using solvent to

soften or dissolve the bonding material, separating the device from the carrier using a thermal slide process, and lifting the carrier away from the device [4]. Each has advantages and disadvantages and the method must be selected based on the user's individual needs.

The first method for carrier release and bonding material removal uses a solvent bath to soften the thermoplastic bonding material through a perforated carrier and then subsequently cleaning with solvent baths. This method creates a very-low-stress release process but requires handling of the thinned, fully processed device wafer in a solvent bath. Separation times are long, but capital investment is low, making this method suitable for specialty wafer production.

Thermal slide separation involves heating the bonded wafer pair to a temperature high enough to significantly reduce the viscosity of the bonding material. Vacuum chucks are used to lock the wafer and the carrier to separate chucks, and then shear force is used to separate the wafer from the carrier. One of the chucks moves parallel to the face of the second chuck's stationary face to complete the separation. The thin wafer is transferred using a special full-face end effector to either a full-surface spin chuck or to a film frame for removal of the bonding material from the wafer using solvent. If the full-surface spin chuck is used, a second full-face end effector is then used to mount the thin wafer to a film frame for dice and test, and then pick and place. The carrier may be transferred for cleaning using a standard end effector, and cleaning may be completed on the standard spin chuck or even in a bath system, if desired. This solvent cleaning method provides a low-stress means of removing the bonding material that remained on the wafer surface and leaves a clean surface ready for connection to chips on which it may be stacked.

In the last separation method, the carrier is lifted off the device in a peel-like fashion. Three variants of this lift-off separation method have been developed. In the first method

introduced, the bond between the bonding material and the carrier is broken with a rastering laser [5]. The carrier is transparent to the laser, but treated on the face inside the bond line to create a heat-affected zone that "unzips" the bond between the carrier and the wafer. The flexible thermoset bonding material used with this technology is left on the device surface and then peeled off this device wafer.

In a second variant of this lift-off separation, a release layer is deposited on the device surface at the very beginning of the process [6]. An uncured thermoset bonding material is then applied to the carrier, the carrier and device are placed tightly together face to face, and the bonding material is thermally cured. For separation, the carrier and the bonding material are peeled directly from the device surface.

Finally, to get the best characteristics of room temperature debonding by lift-off while protecting the surface of the device by subjecting it only to solvent wash to eliminate bonding material, a new bonding technology was introduced. In Brewer Science® ZoneBOND® technology, a high-tack area is created on the carrier, and the center of the carrier is treated to create a low-stiction zone [7]. The wafer is then coated with a thermoplastic bonding material and is bonded to the carrier using time, temperature, and force under vacuum. For separation, the high-tack bonding material area is softened in a special solvent exposure, and the device is mounted to another temporary carrier such as a film frame. The device is held on a full-surface vacuum chuck, and the carrier is lifted off the bulk bonding material layer at room temperature. Separation takes place at the carrier-bonding material interface, keeping the stress on the device to a minimum. The device is then stripped of bonding material using solvent with a puddle-and-spin-dry process. Once cleaned, the finished device wafer may be transported for dice, test, and final assembly.

As 3D IC technology advances and moves into very-high-volume manufacturing, more cooperation

between groups within the semiconductor supply chain will be required. fabs that make chips with different functions such as memory and logic must cooperate to match interconnects for full heterogeneous integration. In addition, to complete the process of thinning and signal rerouting, fabs and OSAT providers will need to work with equipment and materials suppliers to fully enable all processing. Bonding material suppliers have a thorough understanding of the material properties and capabilities and may help accelerate the integration process if consulted for process development and implementation. Although the timeline for 3D IC high-volume manufacturing has slipped from original plans, much like the expected timeline for flip-chip implementation, cooperation across all portions of the supply chain will bring this much needed technology to full maturity in the next few years.

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## Biography

Mark Privett received a BS in mechanical engineering from the U. of Missouri-Rolla, an MS in materials science and engineering from the U. of Florida, and an MBA from Arizona State U. He is the Manager of Technology for the Advanced Packaging Technology Business at Brewer Science; email mprivett@brewerscience.com.

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# System Planning Maximizes Value of Silicon Interposer Technology

By Kevin Rinebold [Cadence Design Systems]

The buzz in the semiconductor industry over 3D-ICs continues to escalate. Today, many designs are implementing through-silicon vias (TSVs) in passive silicon rather than active silicon. Die are being placed side by side on a silicon substrate and connected through interconnect on the silicon. Most of the industry refers to this as silicon interposer or “2.5D” technology.

With the risk and cost of developing systems-on-chip (SoCs) on the latest technology nodes that utilize large, complex flip-chip packages, silicon interposers can be an attractive alternative (Figure 1). They enable multiple die of mixed process technologies to come together on a substrate that provides a greater interconnect density than what's available in the package or printed circuit board (PCB). Use of silicon interconnect to implement high-bandwidth die-to-die connectivity (like Wide I/O memory) can also result in better performance and reduced power consumption.

While much of the discussion on implementing silicon interposers has been related to TSV construction and

manufacturing technology, some are thinking in broader terms and looking at the silicon interposer as a part of the overall system. Considering the silicon interposer in the context of the chip, package, and PCB requires a prototyping and planning solution capable of representing these multiple fabrics in a single environment. A prototyping and planning environment inclusive of the interposer allows designers to make tradeoffs and decisions in the context of the full system, resulting in an optimized system with maximum electrical performance and lower development costs.

The objective of this prototyping and planning is to coordinate device placement with associated pin and net assignments within the chip-interposer-package-PCB system. Once assignments are determined and connectivity is optimized, route feasibility planning can take place. In the case of Wide I/O memory (with its timing and performance constraints), route planning of the memory bus is performed with full system visibility, which in turn enables the necessary system-level signal and power integrity planning. The idea is to perform this

planning and optimization prior to detailed implementation—when the options to make changes are the greatest and cheapest to implement.

Achieving this objective is a multi-fabric balancing act of evaluations and tradeoffs. It requires insight into aspects of the detailed package layout—like flip-chip escape patterns and route feasibility. Visibility into the PCB-level netlist, its influence on ball pad configuration, and its potential impact on socket compatibility is imperative. The ability to understand chip-level logic restrictions (such as hard macros and high-speed interfaces) and their impact on the I/O pad ring and subsequent netlist is also a must. Incorporating a silicon interposer into the system planning equation brings the added dimension of micro-bumps, TSVs, and C4 bumps, all of which factor into connectivity optimization and route feasibility.

Connectivity planning and optimization must work in concert with placement and feasibility functions as part of the system prototyping and planning environment. These are not isolated events but rather pieces in a tightly intertwined puzzle, with the results of one piece impacting the others. Deriving a balanced solution across the fabrics requires a great deal of automation that is highly scalable to adapt to various interconnect schemes.

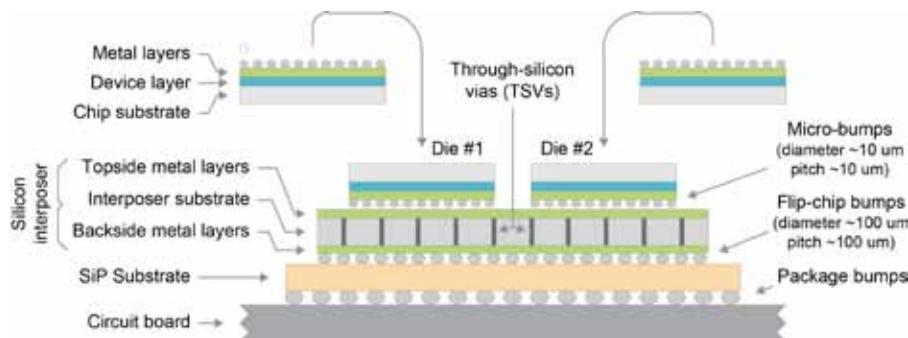


Figure 1: System substrate stack-up including interposer.

## Bottom-up Connection Planning

Consider the scenario of incorporating a new package containing an interposer with multiple die onto a PCB that targets a consumer product for which cost and performance are the primary drivers. While device placement and assignment

decisions made solely in the context of the chip may yield the ideal chip-level design, they could ultimately result in missing the cost and performance targets for the end product. In such a top-down system flow, the chip-level placement dictates the bump and ball assignments in the downstream fabrics. This results in excessive coupling in the high-speed memory interface and a needlessly complex escape routing scheme that requires additional layers in the package and PCB substrates.

A more cohesive approach utilizing system planning and prototyping would establish an initial ball pad assignment that considers the routing and layer constraints of the PCB, and then propagate it into the package to establish the C4 bump placement of the interposer. The C4 bump placement in turn would influence the TSV and micro-bump placement on the interposer and die respectively, and then subsequently the pad ring and device placement at the chip level (**Figure 2**). While it's unrealistic to drive the system entirely from the bottom-up, factoring in aspects of the PCB and package during early planning is a necessity to achieve product cost and performance targets.

System prototyping and planning requires innovative functionality to manage and manipulate a range of data at various stages of completeness and adapt as portions of the design become less abstract during the design cycle. Ease of implementation and usability are crucial to minimize disruption to the overall design flow while still providing fast ramp-up of new users. The ability

to instantiate design information on-the-fly ensures timely planning and feasibility in the absence of detailed content. Solutions must be vertically-aware to support silicon interposer, 3D-IC, and other stacked applications while providing versatility to model various die attach scenarios.

There are numerous aspects to consider when performing system prototyping and planning. Some of these include: data management, system hierarchy, bump and TSV pattern construction, net management, connection optimization, signal integrity (SI), power integrity (PI), and route feasibility.

### System Hierarchy and Data Management

A fundamental aspect of system prototyping and planning is the ability to quickly make placement and net changes in one fabric and immediately see the impact on adjacent fabrics. This requires an environment capable of uniting design data of various sources and formats for the purpose of planning, then communicating the data back to the implementation tools for design completion. Aspects like device scaling for process shrink and instance management must also be taken into account when moving data between environments.

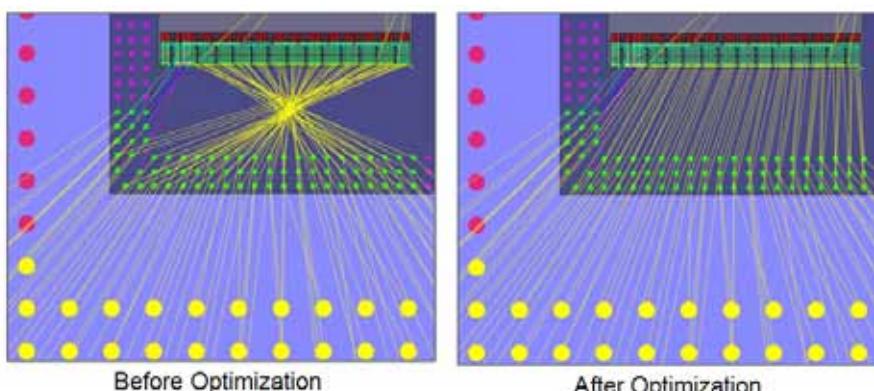
For example, when representing silicon data in the context of the interposer or package, the design content must be represented at its final dimensions while the incoming silicon data will be at the drawn scale.

It's not sufficient to just scale the incoming data—its source must also be tracked so items like bump patterns are properly represented in their respective implementation tools.

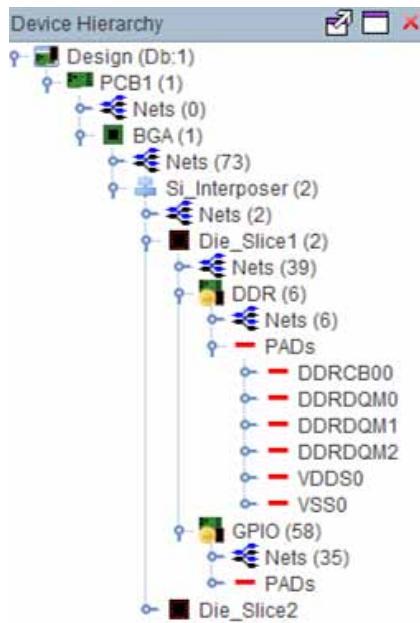
Populating the system prototyping and planning environment is accomplished using various data formats. In some cases they might be industry standards like LEF/DEF or Verilog, or a more generic spreadsheet format. Emerging formats, such as the Die Abstract File from Cadence, may be utilized to create a tighter link between the silicon implementation and the prototyping/planning tools. Package- and PCB-level data may be represented in their native formats or in a reduced representation showing just the critical devices like high-speed memory and connectors.

Once the planning environment is populated, the relationships among devices must be defined and managed—in other words, establish the full system representation. This is accomplished using automated hierarchy management to establish and manage the relationships among the fabrics. It enables representations of the complete system from the chip level to the PCB level while maintaining the integrity of individual design data. Most every aspect of system prototyping and planning will reference the hierarchy before performing a given task. An example of device hierarchy, **Figure 3** illustrates the full system from the PCB through the package and silicon interposer down into the chip-level I/O pads.

When designs from different sources come together, it's not uncommon to encounter syntactical differences in net names. One example of such differences is for a logical net of Address bit 0 to be called ADDR[0] on the chip, A[0] on the package, and AD[0] on the PCB. From a system perspective these are all the same logical net. Before connection planning and optimization can take place, these nets must be mapped and correlated while maintaining the integrity of the source netlist (**Figure 4**). A similar situation exists when there's a need to map several instances from a



**Figure 2:** Bottom-up connection optimization influencing I/O pad-ring placement.



**Figure 3:** Device hierarchy in system prototyping and planning environment.

chip to one instance on the interposer or package. An example of this would be multiple on-chip VDD nets connecting to a common VDD net on the package.

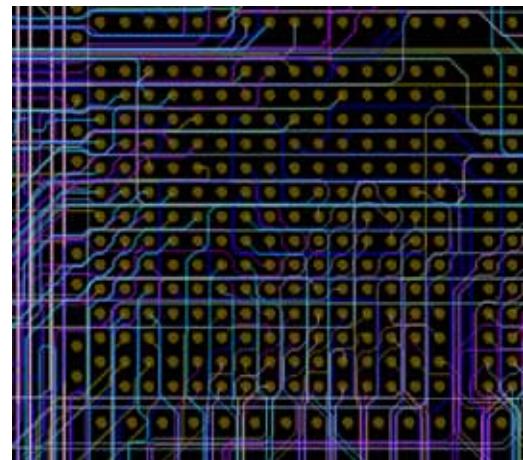
While a silicon interposer requires an additional level of planning, it also serves as a beneficial buffer between the silicon and package/PCB. In many cases the interposer is used as an interconnect redistribution mechanism to resolve and balance conflicting requirements between these fabrics. The

actual size of the interposer is primarily a function of the die it encompasses, so the ability to adjust its size on-the-fly in response to die changes is required. Properly representing die orientation in relation to the interposer is critical since they'll likely be in a face-down orientation—the exact opposite of the representation in the incoming data.

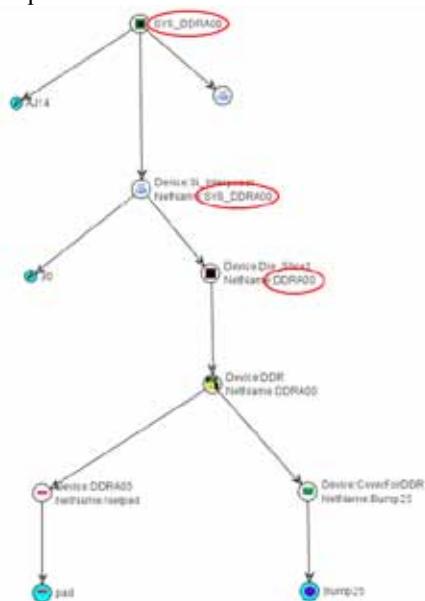
Given the variability and influence from adjacent fabrics, it's most efficient to instantiate the initial interposer layout as part of the system prototyping and planning process. This requires the ability to not only construct the appropriate bump and TSV patterns, but also to properly prepare and manage design content in the appropriate representation for the implementation tool. An example of this is using multiple one-pin instances to represent bumps in the chip implementation tool while presenting the same content to the package implementation tool as one multi-pin instance. Process scaling must also factor into this example. The planning environment should include the capability to incorporate updated content as it becomes available, as well as a verification mechanism to ensure bump pattern integrity across fabric boundaries.

exists between the package ball pads and the PCB substrate. Via placement for escape routes not only impacts routability, but greatly influences connection scheduling and sequencing.

Once escape routing patterns have been evaluated and the connectivity optimized between their respective fabrics, the next step is to evaluate the overall route feasibility of the package and, possibly, the interposer. Route feasibility must account for key constraints like differential pairs, bundles or net groups, and timing targets. The objective is to verify routability within the target layer count and produce initial interconnect layout suitable for preliminary signal integrity



**Figure 5:** Complexity of package escape routing on PCB impacts layer count.



**Figure 4:** Net SYS\_DDRA00 on package maps down to net DDRA00 on chip.

## Performing Meaningful SI/PI Analysis

Flip-chip is the common attachment mechanism used in conjunction with silicon interposers. As a result, requirements for the redistribution layer (RDL) at the chip level and bump escape routing on the package substrate must also be considered as part of system prototyping and planning (**Figure 5**). RDL routing takes place on the outer most layers of the chip and is used to connect the I/O pad cells to their respective bump cells. The required route resources are a direct result of the placement quality of the I/O pad and bump cells. Bump escape routing is performed on the package substrate and directly impacts layer count and design complexity. A similar scenario also

(SI) and power integrity (PI) analysis.

SI and PI are strictly not separable issues—the power delivery network (PDN) is used as a voltage reference for signal nets and therefore any noise on the PDN also appears as signal noise. PI is typically addressed first with DC IR drop, dynamic noise, and impedance analyses. The PDN for an interposer is larger and must handle greater current delivery capacity than a PDN for an individual chip, making these interposer PI feasibility analyses critical to properly assess overall system-level performance.

The electrical parasitics of TSVs and interposer routing are important new concerns relative to conventional 2D-ICs. Resistance, self inductance,

and mutual inductance should be considered. The mutual inductance among TSVs not only couples noise between individual power rails, but also between signals and the PDN. This signal/PDN coupling provides additional incentive to pursue power-aware SI analysis, even at the feasibility stage.

In addition to delay and impedance of interposer signal nets, proximity coupling among these nets must also be considered. Therefore, as for TSVs, the inductance of interposer interconnect routing cannot be ignored. Typical RC on-chip extraction methodologies may be of limited value for interposer SI/PI feasibility assessment, but will definitely be required for subsequent post-implementation verification SI/PI analyses.

These feasibility SI/PI analyses are performed on initial interconnect layouts and preliminary TSV maps. “What if” analyses are performed to judge electrical performance feasibility and develop design-rule constraints for formal physical implementation in more classical IC tools. Though the interposer is an IC environment, it is applied much as a package. Not surprisingly, SI/PI analyses are expected to provide many of the same performance metrics as standard package extraction and assessment tools.

The initial layouts of the interposer are not required to correspond closely to the final implementation to gain meaningful SI/PI performance metrics. In this light, the analyses may bias toward faster speed versus precise modeling. But they must still include all relevant physical effects (e.g., inductance). The results of these analyses, though approximate, are more than adequate to guide any potentially required rebalancing of noise/delay/timing margins across the multiple fabrics of the system to achieve overall electrical performance goals. In the absence of such guidance at the feasibility stage, it may be too late to perform such rebalancing after too many components of the design are finalized.

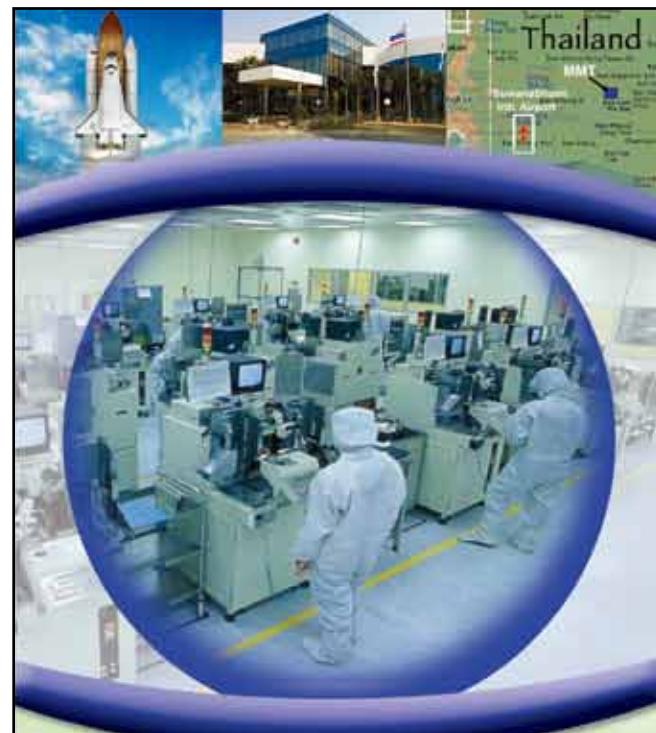
## Summary

Whether a system utilizes silicon interposer technology or not, the goal remains the same—deliver a product that meets or exceeds cost and performance metrics. With products that use high-speed, high-bandwidth interfaces, coordinated planning and analysis across all fabrics—silicon-interposer-package-PCB—is mandatory. Failure to do so results in a needlessly complex system that comes up short against performance and cost targets.

Employing a system prototyping and planning environment that unifies the multiple fabrics and facilitates bottom-up planning is a more efficient path to product realization. It supports critical decision making on issues that impact performance, complexity, and cost at a point in the design process when it's the most practical and economical to effect change.<sup>8</sup>

## Biography

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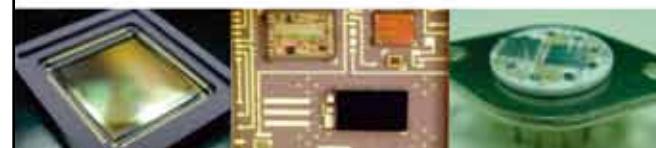
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# Designing and Qualifying Chip-Scale Packages

By Craig Hillman, Nathan Blattau [DfR Solutions]

The continued evolution in semiconductor fabrication, and the expectations that have come with it, has resulted in a revolution in chip-scale packaging (CSP). The tremendous cost and struggles to produce the next-generation integrated circuit, including \$10 billion for 450mm wafer fabs [1] and TSMC's well documented challenges with yield at 28nm [2], have driven significant interest and resources into new materials and new architectures for next-generation semiconductor packaging. These challenges have not only allowed chip-scale packaging to continue its steady improvement in miniaturization and density, but it has also flowered an expansion of the very concept of a chip-scale package. This includes the recent introduction of silicon interposers, through-silicon vias, and embedded die designs.

These changes and improvements create great opportunity for improvements in form, fit and function. The ability of stacked die to provide 16GB of flash memory in today's smart phones are well-documented, as is the thin form factor of the iPhone's package-on-package (PoP) microprocessor. However, every revolution in packaging, from the introduction of the ball grid array (BGA) to the quad flat pack no-lead (QFN) to the PoP, has typically gone through a two stage lifecycle. In the first stage, the high-volume OEMs work with the largest component manufacturers and the outsourced assembly and test (OSAT) vendors to ensure that the new packaging concept is highly compatible with the supply chain's manufacturing process and qualification procedures. Areas of concern are identified based on initial studies, information is

exchanged among the parties involved, and modifications are either made to the packaging or the manufacturing process. After a successful launch, the package lifecycle enters the second stage, where other component manufacturers incorporate the new packaging concept into their technology and then attempt to convince the broader market that the new package is appropriate for their design, manufacturing environment, and end-use application. Unfortunately, as one could guess, the second stage never goes as well as the first.

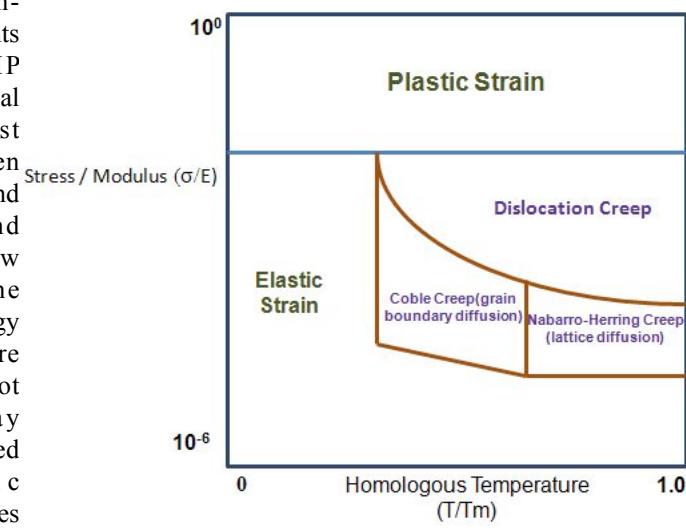
## Reliability Physics

What is often missing from the second stage is an understanding from all parties on how to identify what they don't know they don't know. The high-volume supply chain is rarely representative of the challenges and idiosyncrasies faced by tier 2 and tier 3 component vendors and OEMs and is therefore not necessarily an appropriate staging area to shake out potential issues with the packaging technology. If issues are identified, resolutions can be hidden by non-disclosure agreements and aggressive IP posturing. The critical question that must be asked, and often is not, by this second wave of users and consumers is how the changes in the packaging technology could induce failure in ways that are not relevant and may not even be detected by the classic qualification activities prescribed by either

JEDEC or the Automotive Electronics Council (AEC). And that requires an understanding of reliability physics.

Reliability physics, also known as physics of failure (PoF), is the process of using modeling and simulation based on the fundamentals of physical science (physics, chemistry, mechanics, etc.) to predict reliability and prevent failures. With semiconductor packaging, what this really means is being able to accurately characterize material movement. The majority of the key failure mechanisms of concern (fatigue, creep, electromigration, etc.) relate back to material movement and how it changes as a function of stress. Success in the domain of reliability physics requires an understanding of the stress, the magnitude of the stress, the rate at which this stress is driving material movement, and when this material movement could induce failure.

An example of this structure can be seen in creep. Creep is the tendency of a solid to permanently deform when subject to a fixed load. As seen in **Figure 1**, the presence and type of



**Figure 1:** Schematic of deformation map (Ashby maps) of Sn-based solder.

creep in solder varies depending upon the stress, normalized by modulus, and temperature, normalized by melt temperature. Having this basic knowledge, one can then start to look at the packaging architecture and ask, ‘Is creep a risk in my use environment?’ If the answer is yes, other questions start to naturally fall into place: 1) at the given temperature, which creep mechanism will dominate; 2) what are the potential sources of stresses that will drive creep. The ability to sufficiently answer these questions will then point towards the right combination of characterization, simulation/modeling, and testing necessary to have a robust qualification plan.

## Case Studies

The process of using reliability physics to help design and qualify CSP can quickly become convoluted and academic if every stress, mechanism, and algorithm is presented and explained. It has been our experience that a more insightful approach for the practicing engineer, either at the component manufacturer or the OEM, is to provide case studies relevant to current generation technology. With this in mind, the state-of-the-art packaging of the Virtex 7 2000T was selected as an appropriate guinea pig.

Before moving forward, it is important to note that neither DfR Solutions nor the authors have had any prior engagement with the design, manufacturing, marketing, or assembly of this package and any evaluation of the package does not imply or deny any activity by the manufacturers. Instead, the revolutionary aspects of this package make it an excellent example of the recent changes in CSP beyond the classic memory device or fine-pitch BGA. The 2000T pushes the boundaries of CSP in terms of size and mass. It is a significant package at over 63mm corner-to-corner. And while the 2000T does not fall into the traditional classification of a CSP as per IPC/JEDEC J-STD-012 Implementation of Flip-Chip and Chip-Scale Technology (package area of no more than 1.2X

the original die area), the total volume of silicon, including active die and interposer, may make JEDEC rethink its definition. Most importantly, it is the first known off-the-shelf component to use silicon interposer technology with through-silicon vias (TSV). The silicon interposer, fabricated at 65nm, connects four identical field programmable gate array (FPGA) die fabricated at 28nm.

Before starting the case study, it is important to note that a critical aspect of physics-based design and qualification is linking the knowledge of failure mechanisms and failure drivers back to the manufacturing process. One of the classic limitations of the standard JEDEC qualification process is that sample selection is based on a nominal manufacturing process with the hope that three lots of a sufficient size will somehow magically introduce sufficient variation into the sample population. Reliability physics requires asking what aspect of the manufacturing and assembly processes could be a strong influence on a failure mechanism and what is the realistic worst-case setting that can be reasonably incorporated into the design of experiments.

## Electromigration and HTOL

The case study of the 2000T will focus on three important mechanisms: electromigration, creep and fatigue. Electromigration is the diffusion of material within an interconnect, such as a trace or via or solder ball, due to the flow of electrons. It is dependent upon the current density, temperature, and material/geometry of the interconnect. Black’s equation [3] is the algorithm typically used to describe this behavior

$$MTTF = A j_e^{-n} \exp\left(\frac{E_a}{kT}\right)$$

Equation.1

where A is a constant, j is the current density, n is an exponent (typically around 2), E<sub>a</sub> is the activation energy (typically around 0.8eV for Pb-free solder bumps), k is Boltzmann’s constant, and T is the temperature of the solder bump (NOT the temperature of

the package).

Traditionally, electromigration has been the provenance of die designers, but increasing current densities and smaller packaging geometries have driven the concern to first level interconnects. One of the first things we noticed about the 2000T is the size of the connections between the four FPGA die and the silicon interposers. Described as micro-bumps, their 25μm diameters are a significant reduction from the traditional 75-125μm diameter of solder bumps and even smaller than the familiar 45μm copper columns more recently introduced. Looking at Black’s equation, we can see that this new geometry, for the same current load through the interconnects, would potentially decrease lifetimes by an order of magnitude.

However, recent experiments also tell us that copper columns, by reducing current crowding and potentially driving SnCu intermetallic formation, can increase lifetimes by one to two orders of magnitude over Pb-free solder bumps (which, in turn, were about an order of magnitude worse than the high Pb bumps they replaced). There is also the possibility that current loads through the power connections and bump temperature could be higher compared to previous generations (a typical trend with silicon fabrication).

While a clear answer to electromigration in this particular packaging cannot be provided in this article, the key point about this relatively quick exercise is to demonstrate the ability of reliability physics to bring questions and discussions to the forefront of the design and qualification process. It can also bring out questions regarding the manufacturing process. For example, how sensitive is electromigration through the micro-bump and TSV structures to the manufacturing process? If the TSV is 90% filled, especially near the traces on the surface, how much does that reduce lifetime due to electromigration?

If information obtained through modeling and simulation demonstrates a sufficient level of design robustness,

reliability physics can then be used to design an appropriate qualification test plan. While testing for electromigration is typically a full or partial factorial, if confidence in the constants in Black's equation is high, then only one condition need be selected. In either situation, the conditions must be carefully selected. Again, reliability physics provides clear guidance on this decision. At elevated temperatures (100°C and above), the little tin (Sn) available under the copper column quickly reacts to form SnCu intermetallics that are very resistant to electromigration. However, at lower temperatures, the diffusion behavior of tin changes substantially from bulk-dominated to grain boundary dominated [4] (this has been well documented in tin whisker experiments). This could result in non-relevant extrapolations from standard test conditions.

### Creep and Fatigue and Temperature Cycling

Additional mechanisms of interest for the 2000T or any other similar package architecture would be creep and fatigue of the interconnects. In this case, there are three levels of interconnections (micro bumps, solder bumps, and solder balls). It is well known that temperature cycling is the common JEDEC test used to characterize the creep and fatigue mechanisms of solder in semiconductor packaging. However, this basic approach has been called into question recently by differences in specifications and changes in materials.

To start, creep and fatigue behavior can tend to be captured through quantifying the strain range experienced during a temperature cycle [5]. For most connections, this has been through

$$\Delta\gamma = C \frac{L_D}{h_s} \Delta\alpha \Delta T$$

Equation.2

where  $L_D$  is the diagonal distance,  $h_s$  is the solder joint height,  $\Delta\alpha$  is the difference in CTE between two structures (die and substrate, substrate and board, etc.) and  $\Delta T$  is the change in

temperature. More recently, foundation stiffness models [6] have been added to the mix to capture some of the complex mechanics that influence the stresses

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L_D = F \cdot \left( \frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left( \frac{2 - v}{9 \cdot G_b a} \right) \right)$$

Equation.3

being applied to the solder connections; where  $F$  is the shear force,  $L_D$  is length,  $E$  is the elastic modulus,  $A$  is the area,  $h$  is the thickness,  $G$  is the shear modulus, and  $a$  is the edge length of the bond pad.

The need to understand the physics behind this degradation phenomenon has been recently heightened due to differences between JEDEC JESD47 Stress-Test-Driven Qualification of Integrated Circuits and IPC 9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments. The former specification, favored by the component industry, recommends 2300 cycles of 0 to 100°C. The latter specification, favored by the OEMs, recommends 6000 cycles of 0 to 100°C (if reliability physics has not been used to develop a tailored test plan). One can immediately see that the supply chain is now, potentially, testing under conditions up to two-thirds more benign than the OEM is expecting. On top of this, JESD47 makes no mention of the test board dimensions. Especially for a large component like the Virtex 7, testing on smaller, thinner printed boards could extend times to failure by 2 to 3X.

On top of this discrepancy, there has been a critical change in packaging materials. Because of the brittle nature of low-k dielectric, some OSAT vendors have migrated from

underfills with high glass transition temperatures ( $T_g$ ) (greater than 110°C) to underfills with low glass transition temperatures (less than 80°C). This one

modification, in one packaging material, has in one stroke invalidated the classic approach to temperature cycling.

The reason for this complete rethink in qualification practices is because the underfill does not undergo uniform changes as it approaches its  $T_g$ . As shown in Figure 2, the coefficient of thermal expansion (CTE) increases more rapidly than the elastic modulus decreases. This difference in timing is because changes in the CTE in polymers tend to be driven by changes in the free volume where changes in modulus tend to be driven by increases in translational/rotational movement of the polymer chains. Because lower levels of energy are required to increase free volume compared to increases in movement along the polymer chains, CTE changes before modulus [7].

The downside to this little bit of physics is that the underfill will now expand significantly and have the stiffness necessary to push against the flip chip, causing a significant rise in tensile stresses within the interconnect (Figure 3). The fact that this stress state is over a very narrow temperature

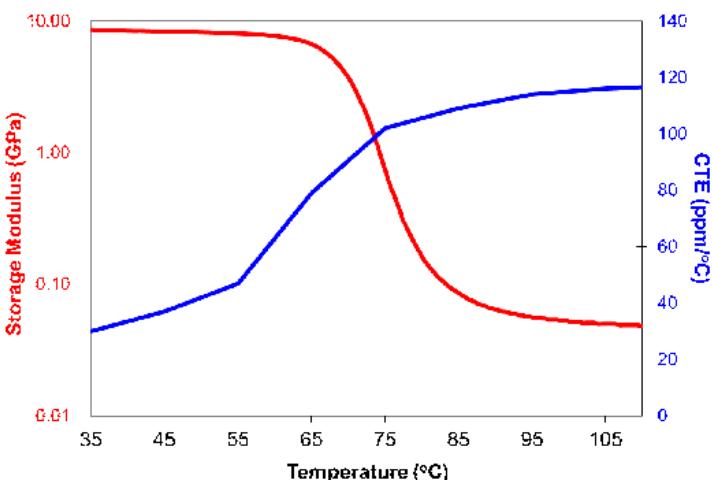
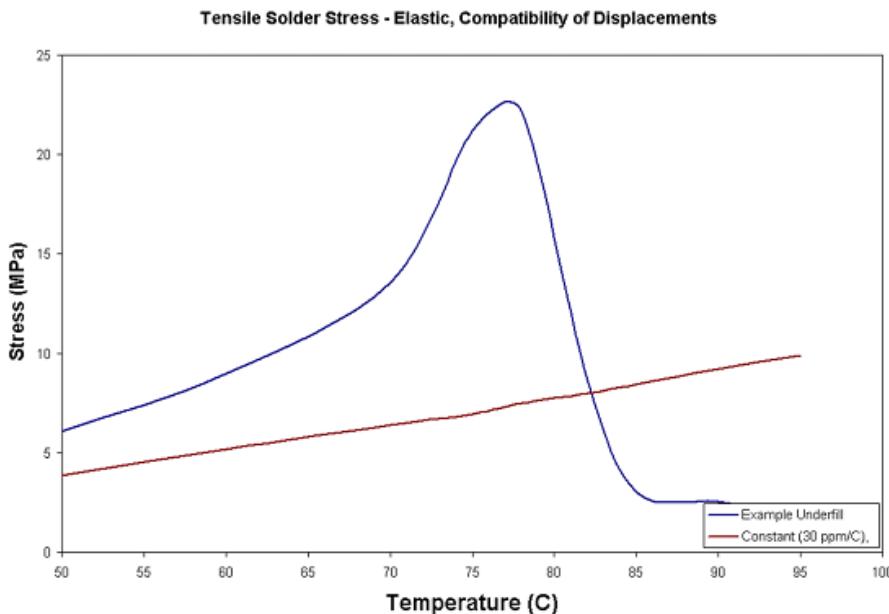


Figure 2: Change in storage modulus and coefficient of thermal expansion (CTE) as a function of temperature for an underfill material with a  $T_g$  of 75°C.



**Figure 3:** Tensile stress in solder bumps encased in low  $T_g$  ( $75^{\circ}\text{C}$ ) underfill as a function of temperature.

range can create situations where small changes in temperature can induce failure in a far shorter period of time than the traditional  $-40^{\circ}\text{C}/125^{\circ}\text{C}$  requirements. In the case of the 2000T, there are two levels of underfill (chip to interposer and interposer to substrate) to consider. The actual underfill material is unknown by the authors, but reliability physics tells us that one or more low  $T_g$  underfills could make a JEDEC temperature cycle test inadequate for some applications.

The appropriate approach in this situation for design verification and qualification depends if you are an eventual user of this technology (component manufacturer) or customer of this technology (OEM). In both situations, you will want to fully characterize the underfill CTE and modulus as a function of temperature. For a user, this can be done by performing thermo-mechanical analysis (TMA) and dynamic material analysis (DMA) on the raw underfill. For the OEM, more sophisticated techniques, such as nanoindentation and digital image correlation (DIC) are required to reverse engineer the key material properties.

Once this information is obtained, simulations need to be performed assuming global and local temperature rise. Local temperature rise, where

power dissipation is constrained over small area, is likely the greater risk as it can induce a complex stress state that may result in tensile stresses being applied to the interconnects. Tensile stresses can reduce time to failure by an order of magnitude compared to classic shear and a deviation from the standard physics of failure formula for solder joint fatigue. The results from these simulations may drive modifications to thermal cycling, including the introduction of mini-cycles around the  $T_g$ .

## Summary

While advances in packaging technology allow for continued progress in Moore's Law, it also requires additional due diligence from users and customers. While in all likelihood this new packaging architecture is very robust, using reliability physics to validate designs and develop qualification plans is a common sense approach for risk mitigation for all customers (reliability is application-specific). By forcing the right questions to be asked, reliability physics can hopefully prevent the industry-wide escapes that tend to periodically plague the electronic industry (see low ESR capacitors, red phosphorus encapsulants, etc.). Always remember: an educated consumer is the best customer. ☀

## Biographies

Craig Hillman received his BS in metallurgical engineering and materials science and engineering and public policy from Carnegie Mellon and his PhD in materials science from the U. of California – Santa Barbara and is CEO at DfR Solutions; email [chillman@dfrsolutions.com](mailto:chillman@dfrsolutions.com)

Nathan Blattau received his BS in civil engineering and his PhD in mechanical engineering from the U. of Maryland and is SVP at DfR Solutions.

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# Metrology and Inspection Solutions for TSV Processes Used to Connect 3D Stacked ICs

By Rajiv Roy, Tim Kryman, Reza Asgari [Rudolph Technologies, Inc.]

The market's seemingly insatiable demand for more power and capability and smaller footprint has led manufacturers to develop advanced packaging and 3D integration schemes that combine multiple stacked die. Most of these schemes use through-silicon vias (TSVs) to route signals "vertically" through the chip stack, combined with layered structures, such as redirect layers and interposers, to route signals "horizontally" on the chip, between chips, and to the package. Typically, these processes operate on fully processed wafers, making process errors extremely costly. Inspection and metrology for process control are indispensable. The TSV process, which must create vias through the substrate, fill them with conductive material and connect them to the next chip in the stack, has a number of unique inspection and metrology requirements.

There are many variations on TSV processes, but all have certain operations in common. In a typical process (grossly oversimplified for this discussion) the via is first etched or drilled through the completed active circuitry layers and into the substrate to a specified depth. The vias are filled with copper, a redirect layer (RDL) may be added to route signals horizontally and bumps are added to facilitate vertical connections to the adjacent chip in the stack. The top surface of the wafer is then temporarily bonded to a carrier and the wafer is thinned from the backside to reveal the filled TSVs. Another redirect layer may be added to the backside, and more bumps. At this point, additional chips or a wafer may be bonded permanently to the exposed surface. Eventually, the

wafer is debonded from the carrier and diced into chips, which may be connected to another wafer or packaged. Each of these steps must be inspected for defects and tightly controlled to ensure good process yields.

## Via Creation

Vias may be etched or laser drilled. They range greatly in diameter, depth and aspect ratio and their dimensions must be carefully controlled. The choice of measurement technology depends on the vias' depth and aspect ratio. Vias up to 270 $\mu$ m deep with aspect ratios less than 10 may be measured with confocal spectral interferometry using a method known as spectral analysis of white light interferograms (SAWLI). The technique analyzes the interference signals observed on a spectrometer in order to measure the air gap thickness between a reference plate and the sample (Figure 1). It is a scanning technique that can provide a detailed profile of the via. Measurements take 10-30s per via, depending on size.

As the via's aspect ratio becomes larger, it becomes more difficult to extract sufficient signal from the bottom to perform the analysis. Infrared interferometry provides a novel solution. Silicon is

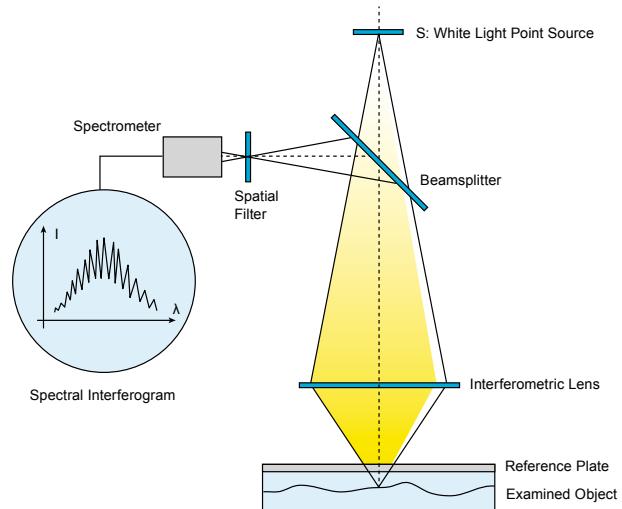


Figure 1: Confocal spectral interferometry for low aspect ratio TSV (LART) metrology. Source: STIL

transparent to infrared light allowing the measurements to be made from the back side of the wafer. The vias appear as columns. The system can measure the thickness of the wafer and the distance from the back surface to the bottom of the via to calculate the via depth (Figure 2). Silicon is transparent to infrared light allowing the wafer to be inspected from the backside, so the system measures the thickness of the wafer and

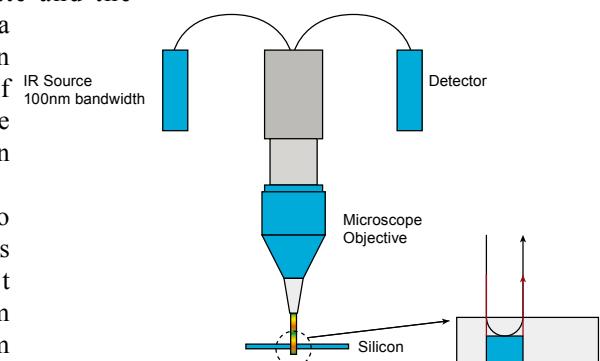


Figure 2: Infrared interferometry-based sensor for high-aspect ratio TSV (HART) metrology. SOURCE: Tamar

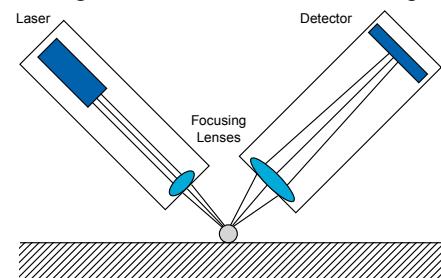
the distance from the back surface to the bottom of the via to determine via depth. It is not limited by via aspect ratio. The technique uses a visible light camera to align the front side of the wafer, then flips the wafer and uses the notch to correlate front to back.

Infrared interferometry can measure single or multiple TSVs. Measurement capability depends on CD size, TSV density, and the objective spot size. It can also measure other features such as trenches. It delivers sub-wavelength

A dual-beam visible light interferometer (VT-SS) measures topography and thickness of transparent layers simultaneously (**Figure 3**). One beam provides direct measurements of the thickness of transparent materials. The other beam measures topography (distance from the sensor) allowing the system to measure the thickness of opaque materials by scanning over the edge of the feature. RDL CDs can be derived from scanned interferometer profiles or camera-based measurements.

as many as 1,000,000 bumps per die and 60 million bumps per wafer.

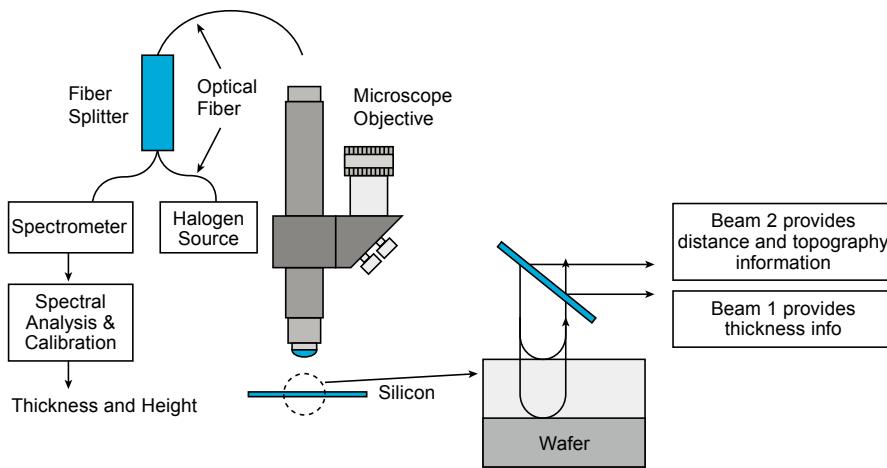
Laser triangulation (LT) provides fast, precise measurements of bump height and coplanarity (**Figure 4**). A laser is directed at the wafer surface at an angle of 45° and focused to a spot



**Figure 4:** Laser triangulation measures bump height.

size of 5 $\mu\text{m}$ . Through a combination of laser scanning and wafer movement, the beam scans the entire wafer surface, completely covering a 300mm wafer at production speeds. A lens collects the reflected/scattered laser light and focuses it on a position-sensitive detector. Changes in the location of the collected light on the detector provide bump height measurements with a resolution of 54nm. The system also includes camera-based technology for defect inspection and 2D measurements of bump diameter and position and RDL CDs.

**Figure 5** illustrates some of the steps in a pillar bump process. In step 1, under bump metal (UBM) and a copper seed layer are deposited over the metal contact pad. Camera-based measurements determine inside and outside CDs. VT-SS or laser triangulation can measure UBM height. In step 2, photoresist (PR) has been deposited, exposed and developed to open a window for copper plating. Camera-based inspection and metrology finds defects, such as uncleared PR, and measures the diameter (D) and location of the opening. VT-SS measures the thickness of the photoresist over the UBM. In step 3, copper has been deposited into the opening. VT-SS measures the thickness of the deposition (H) and the contour of the copper surface. In some cases laser triangulation may be used to make these



**Figure 3:** Dual-beam visible light interferometer for thickness and topography measurements (VT-SS).  
SOURCE: Tamar

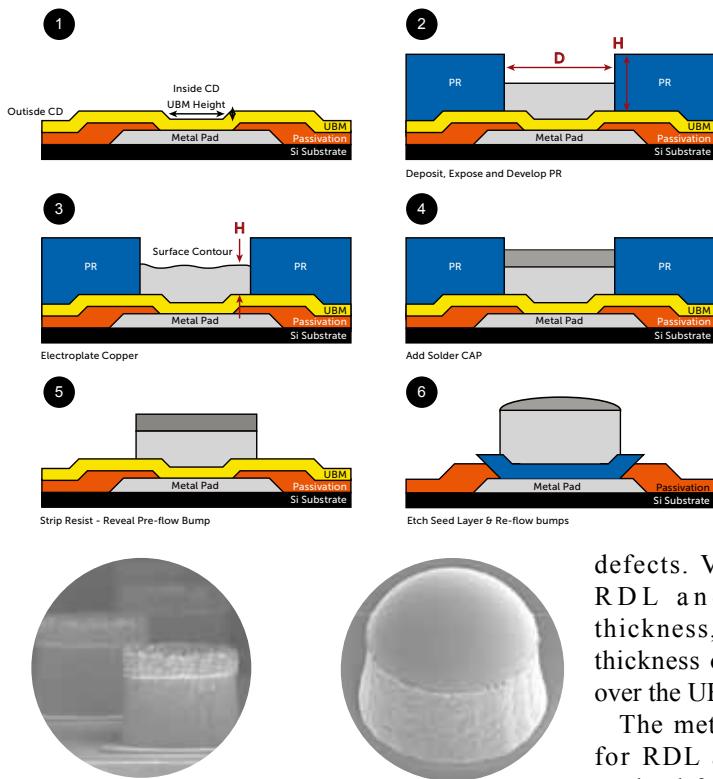
accuracy. An evaluation on 5 $\mu\text{m}$  diameter by 35 $\mu\text{m}$ -deep vias yielded a 3 $\sigma$  precision of 0.17 $\mu\text{m}$ . It is fast (~5 seconds per measurement) and not limited by the aspect ratio of the feature. Infrared interferometry can also be used to measure the thickness of bonded wafers and the adhesive layer, providing the thickness and total thickness variation (TTV) of each layer and the total stack.

### Via Filling, RDL Plating

After vias are created, they are lined with barrier and seed layers, and then filled with copper using a plating process. One or more redirect layers may be added using lithographic processes to route signals horizontally over the surface. Inspection and metrology requirements include post height, RDL plating thickness, RDL dimensions, seed/barrier thickness, copper fill, overburden and via void detection.

### Micro Bump/Pillar Bump

Bumping processes are a critical component of most 3D interconnect (3DI) schemes. Bumps provide the vertical reach required to make connections through the adhesive layer that bonds stacked chips together. Bumps may be applied to pads on the frontside of the wafer or to TSVs on the backside. 3DI bumping processes are largely extensions of processes long used for flip-chips or solder bumps. 3DI bumps are smaller, more closely spaced, and far more numerous. Micro bumps are solder bumps with diameters as small as 20 $\mu\text{m}$  and heights as low as 5 $\mu\text{m}$ . Similarly sized pillar bumps comprise a lithographically-defined metal base (pillar) that may or may not be solder capped. The space between bumps is typically equal to the bump diameter (2:1 pitch). The number of bumps used in 3DI schemes has grown explosively, with roadmaps calling for



**Figure 5:** Pillar bump processes require metrology and inspection at numerous intermediate steps.

same measurements. In step 5, a solder cap is added over the copper and the photoresist is stripped away. In step 6, the solder has been reflowed and excess UBM and seed layer removed at the base of the now completed pillar bump. Camera-based technology inspects for bump and wafer surface defects and measures bump diameter and location. Laser triangulation or VT-SS can measure bump height and volume. Laser triangulation can also evaluate the co-planarity of the bump tops.

### Backside RDL and UBM

When frontside processing is completed, the wafer is temporarily bonded to and thinned from the backside to reveal the filled TSVs. This is often followed by RDL, UBM and bump processes similar to those used on the frontside. After thinning, the wafer is first inspected (camera-based) for defects and damage and to confirm that the TSVs are properly filled and revealed.

RDL and UBM processes are growing more complex and must be

tightly controlled to ensure process yields. **Figure 6** illustrates some of the required measurements. Camera-based technology provides measurements of RDL and UBM feature dimensions ( $X$  and  $Y$ ) and locations, as well as inspecting for defects. VT-SS measures RDL and UBM edge thickness, as well as the thickness of the polyimide over the UBM.

The metal systems used for RDL and UBM have evolved from single layers to multi-layered stacks. RDL may be Cu, Cu over Ti, or Cu/Al sandwiched between layers of Ti. UBM stacks include Ni/Pd, Ni/Pd/Au and Al/Ti/Cu/Ni. Picosecond Ultrasonic Laser Sonar (PULSE™) technology uses a laser-generated acoustic wave to provide non-contact, non-destructive, on-product measurements ( $\leq 30 \times 30 \mu\text{m}$  sites) of single and multi-layered opaque thin films (**Figure 7**).

**Figure 7** illustrates the picosecond ultrasonic laser sonar - a pump/probe technique that uses a brief laser pulse to create an acoustic wave. The wave travels through the stack and is partially reflected at interfaces between different materials. The system detects returning reflections to calculate the thickness of each

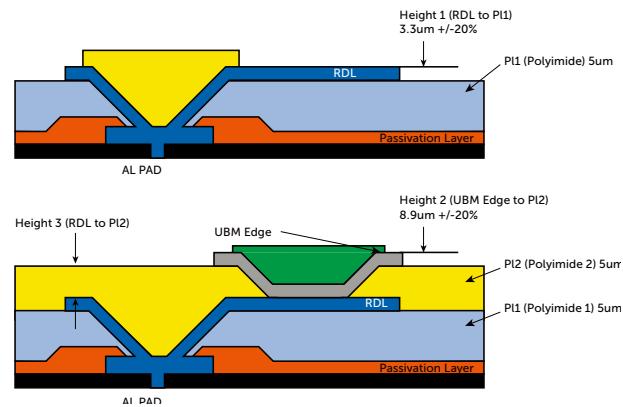
layer. PULSE Technology can measure each layer in the stack. Its small spot size permits measurements on product wafers and can directly measure the

thickness of RDL and UBM film stacks critical to the successful packaging schemes enabled by the TSV process. In addition, PULSE is now being developed to provide TSV metrology (fill/overburden, void detection) as well as stacked silicon/die debond and pillar bump metrology.

### Post-bond

Edge trimming is a technique used to reduce damage at the wafer edge during wafer thinning. Untrimmed wafers have rounded edges. When an untrimmed wafer is bonded to a carrier and thinned, the thin unsupported edge is prone to cracking and chipping, which can easily damage adjacent die. Edge trimming creates a specific stepped profile at the top edge of the wafer (**Figure 8**) before it is inverted and bonded. When a trimmed wafer is thinned, the remaining edge is square and more resistant to chip and crack damage.

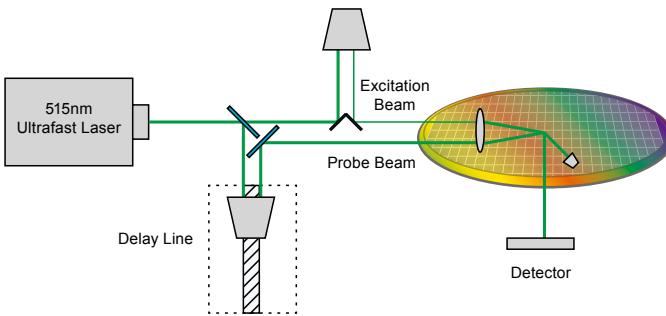
Edge trimming is an aggressive grinding process. Image (camera) based edge inspection combines speed and high sensitivity and allows images of defects to be saved for later analysis. It is important that the edge inspection system provides good coverage of the top surface of the wafer near the edge where delicate circuitry is located, as well as the ability to measure the trimmed edge profile. The notch area is particularly prone to damage. Edge



**Figure 6:** RDL and UBM structures are becoming more complex and require careful control to ensure yields.

inspection can also confirm the overall alignment of the carrier and device wafer.

The wafer shown in **Figure 8** has



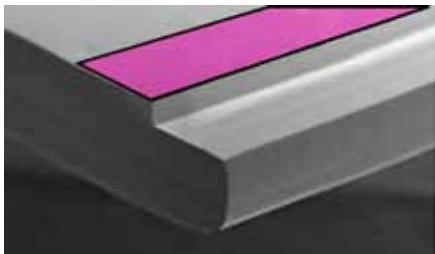
**Figure 7:** Picosecond ultrasonic laser sonar pump/probe technique.

been cross-sectioned to show the profile of the trimmed edge. When the trimmed wafer is inverted and thinned, the remaining squared edge is less prone to chipping and cracking. Trimmed wafers must be inspected and the edge profile measured before bonding, with special attention paid to the top surface near the edge (indicated in the figure in purple) where delicate device circuitry is easily damaged.

Bonded and thinned wafers require thorough inspection before proceeding with backside processing. Bonded wafers are often warped and difficult to pull flat with conventional vacuum chucks. Edge handling and closed-loop vacuum control help to ensure reliable handling. Camera-based inspection can find defects and contaminants on the ground backside surface of the thinned wafer. The backside of the carrier wafer also requires inspection for contamination and damage. TSV protrusion above the wafer surface is readily measured with VT-SS. Infrared interferometry (described previously for high-aspect ratio TSVs) can also be used to measure the thickness of the thinned wafer and the adhesive layer.

## Debond

After thinning and backside



**Figure 8:** Edge trimming reduces chipping and cracking.

processing, the wafer is debonded from the carrier and cut into individual die. Special handling is required for thinned ( $50\text{ }\mu\text{m}$ ) wafers, which are very flexible and easily broken. They may be attached to a flexible film (film frame) for

handling. The debonded wafer must be inspected for residual adhesive and other defects. After dicing, the individual die require a final inspection of defects generated by the sawing process.

The **Table** summarizes the inspection and metrology requirements of TSV-based 3D integration and advanced packaging processes. The table also highlights applications for the following sensors: HART, VT-SS and LART. The system column refers to the inspection platform: F30™ and NSX® 320 are camera-based surface inspection platforms; E30™ is a camera-based edge inspection module; WS 3880™ combines camera-based 2D surface inspection and laser

triangulation for 3D bump inspection. In all cases, these sensors can be readily integrated into existing camera-based inspection platforms to provide robust, reliable production. ■

## Biographies

Rajiv Roy received an MA in marketing and an MS in computer science from the U. of Texas at Dallas, and a BSEE from the Indian Institute of Technology (IIT), Kanpur, India. He is VP of Business Development and Marketing Director for Final Manufacturing at Rudolph Technologies; email rajiv.roy@rudolphtech.com

Tim Kryman received a BS in accounting and information systems from Lock Haven U. and an MBA from DeSales U.; he is the Director of Metrology Product Management at Rudolph Technologies.

Reza Asgari received his post-graduate degree in mechanical engineering from Louisiana State U. and is a Product Line Marketing Manager for the Wafer Scanner 2D/3D inspection solutions for the wafer bump market at Rudolph Technologies.

Process Step	Metrology and Inspection Requirements	System	Flipping	HART	VT-SS	LART
Via Engineering	<ul style="list-style-type: none"> <li>2D CD metrology and defect detection</li> <li>3D via depth metrology</li> <li>Film thickness</li> </ul>	F30 or NSX 320	Yes	Yes	Yes	
Nail Protrusion	<ul style="list-style-type: none"> <li>2D nail protrusion detection</li> <li>3D nail height metrology</li> <li>Film thickness</li> </ul>	F30 or NSX 320			Yes	
Bumping	<ul style="list-style-type: none"> <li>2D surface/bump inspection</li> <li>Film thickness</li> <li>3D bump metrology</li> </ul>	NSX 320 (2D/FT) WS 3880 (3D)			Yes (NSX)	
Edge Trimming	<ul style="list-style-type: none"> <li>Trim metrology</li> <li>Edge chipping</li> </ul>	NSX 320 + E30				
Bonding	<ul style="list-style-type: none"> <li>Wafer to glass misalignment (X, Y, T)</li> <li>Edge defects including notch area</li> <li>Adhesive thickness, TTV</li> </ul>	NSX 320		Yes	Yes	
Back Grinding	<ul style="list-style-type: none"> <li>2D surface inspection</li> <li>Edge chipping inspection</li> <li>TTV</li> </ul>	NSX 320 + E30		Yes		
Backside Bumping	<ul style="list-style-type: none"> <li>2D surface/bump inspection</li> <li>3D bump metrology</li> <li>Litho (Si front and back) alignment verification</li> </ul>	NSX 320 (2D/FT) WS 3880 (3D)			Yes (NSX)	
Chip Attachment	<ul style="list-style-type: none"> <li>2D surface inspection</li> <li>Chip to chip alignment metrology</li> <li>Post mold defect inspection</li> </ul>	NSX 320				
Die Bond and Post Saw	<ul style="list-style-type: none"> <li>2D surface/bump inspection</li> <li>Residue defects</li> <li>Edge defects including notch area</li> </ul>	NSX 320 + Film-frame (XPort)				
Interposer	<ul style="list-style-type: none"> <li>2D CD metrology and defect detection (&lt;10 x AR)</li> <li>3D via depth metrology</li> </ul>	NSX 320				Yes

**Table:** Summary of the inspection and metrology requirements of TSV-based 3D integration and advanced packaging processes.

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# GUEST EDITORIAL

## Die Attach Materials Strategies to Enable IC Package Cost Reduction

By Shashi Gupta, Howard Yun, Victor Aquino, [Henkel Electronic Materials LLC]

**A**s packages have reduced in size, increased in functionality, and continue to incorporate ever thinner die, the need to enable IC package miniaturization has driven advances in electronic materials technology. At the same time, the push for smaller, higher-functioning devices also demands these products at lower cost, presenting even greater challenges to packaging specialists.

To help meet the convergence of higher functionality and reduced cost, conductive die attach film-based materials have been developed and have been proven to lower both materials costs and processing costs, effectively reducing the total cost-of-ownership for certain devices. More robust processing capabilities, high reliability and improved yields, in combination with better process efficiencies and reduced material use, have made these novel materials a welcome die attach breakthrough.

When it comes to process benefits, conductive die attach film provides several. The die attach adhesive is applied at the wafer-level, eliminating the dispensing step along with the set-up process required for die attach paste. This makes the set-up time a lot faster because the operator is not required to change syringes on dispense equipment every four to eight hours, thereby contributing to higher operator productivity. The risk of needle clogging – a major cause of downtime - clean-up and multiple set-up runs throughout a shift, are all eliminated. Potentially, consumables such as different sizes of dispensing heads and the associated maintenance costs can be done away with as well. In addition, dispensing equipment does not have to be procured and, in most cases, packaging firms already have laminators in place so no additional investment is required. Over the long-term, this could lead to capital

investment savings of as much as 50%. In the short-term, manufacturers that don't already own lamination capability would need to invest in laminators but the return on that investment (from additional efficiencies and cost-lowering benefits) would be realized quickly.

The material cost advantages associated with film-based die attach products as compared to paste-based materials are significant for certain die sizes. From a design rule perspective, conductive die attach films offer a high degree of latitude. Film-based materials effectively eliminate the fillet inherent with traditional paste-based products, which enables the incorporation of more die and/or more functionality per package as the die to pad clearance is much tighter. This also means that less silicon, gold wire, lead frame (substrate) and mold compound materials are required, thereby lowering materials cost per unit package significantly. As the market trends toward system-in-package (SiP) technology, using conductive die attach film allows

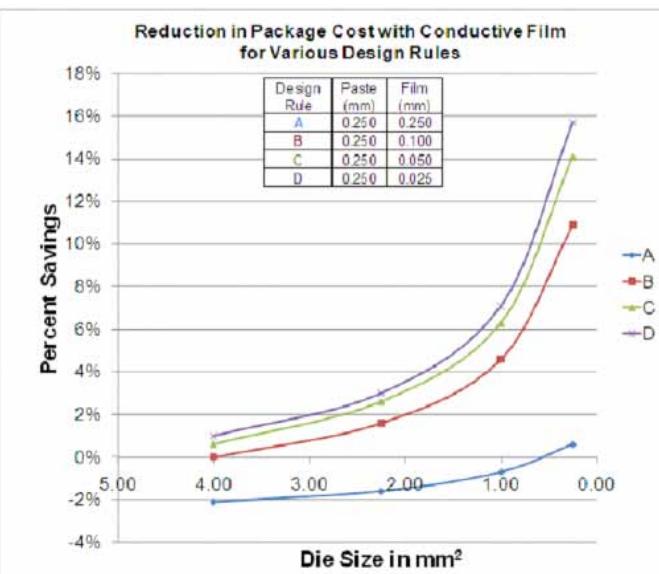
designers to bring multiple die closer to each other so as to reduce cost and footprint. On average, package material cost can be lowered by 2% to 10% for small- to medium-sized packages. Savings for material cost-of-ownership per unit package are greater for packages – particularly those that incorporate small- to medium-sized die – using tighter design rules, enabled by

conductive die attach film (see **Figure**).

Incorporating conductive die attach film does not limit packaging specialists from moving toward cost-effective copper wire and away from higher cost gold wire, as there is no risk of outgassing. Copper wire oxidation may occur from resin-induced outgassing – a condition associated with paste-based materials. Ultimately, oxidation can lead to corrosion and electrical shorts and, to date, has discouraged some manufacturers from moving to lower-cost copper wire from gold. Conductive die attach film now solves this dilemma.

The use of conductive die attach film also reduces material waste. Even though paste typically has a worklife of between 24 and 48 hours, the reality is that once a syringe is opened, anything that remains in the syringe at the end of a shift will typically be discarded. Film, on the other hand, has a worklife of three months and will remain stable at room temperature.

Included in the commercial advantages



Design rules A, B, C and D compare the die to pad clearance capability of paste versus film and how the design latitude afforded by film can reduce overall package costs.

associated with moving from die attach paste to conductive die attach film are improved yield, better quality and storage/shipping cost savings. Internal testing confirms that conductive die attach film offers better moisture sensitivity level (MSL) performance as compared to paste. Eliminating yield loss due to epoxy on die, die tilt, and resin bleed contributes to lower package costs. What's more, the quality and reliability of the device produced with conductive die attach film is expected to be better. Therefore, expenses associated with quality complaint resolution and potential product recall are reduced. Another cost related to MSL performance is the requirement for dry packaging. For devices manufactured with MSL3-rated materials, dry packaging is required for shipping and storage. Conductive die attach film can enable a package to achieve MSL1, so dry packaging isn't necessary and all of these costs are eliminated.

In addition to all of the above cost reduction advantages, the use of

conductive die attach film has a positive environmental impact through the elimination of waste and lower energy consumption. As mentioned previously, unused paste materials are often discarded at the end of a shift and can lead to a significant volume of material waste. Plus, most pastes have to be stored at -40°C while conductive die attach films can be maintained using standard refrigeration (and, again, are stable at room temperature for up to three months), which saves on energy consumption. Finally, all of the desiccants and dry bags used for storage of devices manufactured with MSL3-rated materials that are just thrown away now do not have to be procured or discarded.

All told, package unit cost can be reduced by 10% to 30% by using conductive die attach film as compared to paste for certain applications. When one considers the material cost savings, the process benefits and the commercial advantages – not to mention the environmental impact – conductive die

attach film offers a holistic approach to IC package cost reduction and, in many cases, enables the development of devices that could not be produced with traditional, paste-based materials.

### Biographies

Shashi Gupta received his PhD in polymer chemistry from the U. of Southern California, and BS from the Indian Institute of Technology. He is Director of Global Marketing, Conductive Film at Henkel Electronic Materials LLC; email shashi.gupta@henkel.com

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# Solder Paste Dipping and Reflow Using 0.4mm-Pitch PoP Packages (Part 2)

Christopher Nash, Maria Durham, *[Indium Corporation]*

The electronics industry's trend toward miniaturization of electronic assemblies necessitates smaller pitch and bumps on chip-scale-packages (CSP) and package-on-package (PoP) components. This has led to the need for novel solder paste material characteristics. A solder paste's flux vehicle rheology, powder size, and metal load all play a crucial role in its dipping and reflow performance. It is equally important to understand the role of the actual dipping and reflow processes with regard to performance of the material.

Solder paste, when used in PoP dipping processes, adds volume to the solder joint and acts as a bridge between the warping components and boards, even when the substrate twists and gaps form between the solder ball (sphere, bump) and the substrate [1]. The reliability of a solder joint created with solder paste is greater than that of a solder joint created with just tacky flux because of the extra volume of solder in each joint. "Based on previous works done on the relationship between BGA solder joint quantity and solder joint strength and reliability, greater solder quantities generally result in greater joint strength [2]."

Testing shows the differences between a normal surface mount technology (SMT) solder paste and new solder pastes that are specifically formulated for a dipping process. The testing also shows the performance differences between solder pastes with different flux vehicles, powder sizes, and metal loads. Process set-up also plays a significant role.

## Understanding the Reflow Process

Once the 0.4mm PoP packages have been dipped and placed onto the circuit board, they are ready for the reflow process. This is a challenging step because of the fine solder powder sizes used. A smaller powder size has high surface area to volume ratio

(versus larger particle diameters). This leads to a higher oxidation percentage within the solder powder. If the flux vehicle within the solder paste is not properly formulated, the oxidation can lead to issues like graping, solder balling, head-in-pillow, voiding, non-coalescence, and/or non-wetting [3].

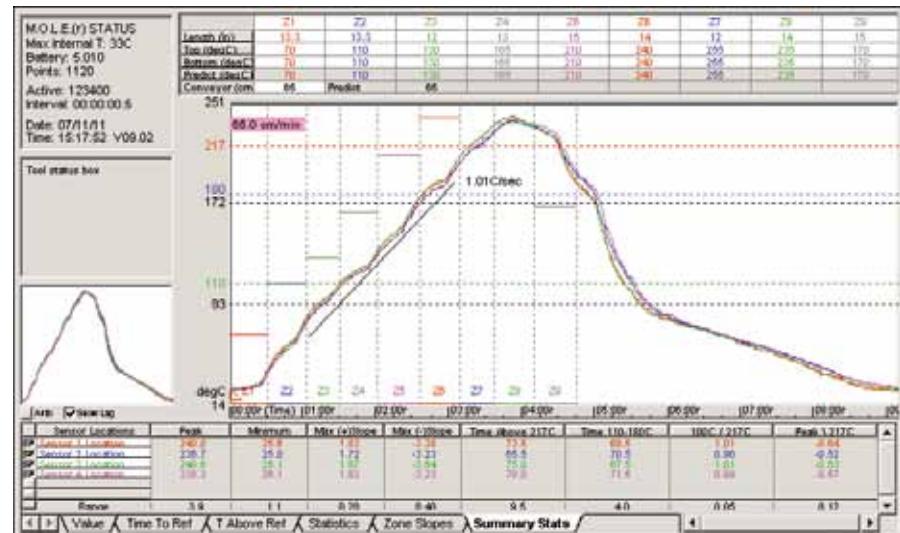


Figure 1: Air reflow profile.

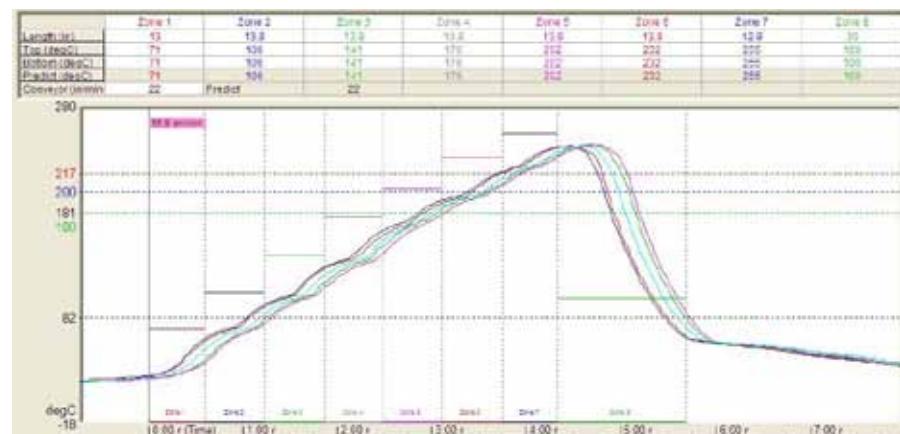


Figure 2: Nitrogen reflow profile.

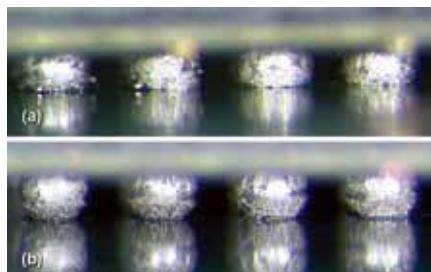
The solder paste materials used for this study were reflowed in both air and nitrogen (~100ppm oxygen) atmospheres (**Figures 1 and 2**). (Paste A was not included in this study because of inconsistent solder bump volume and coplanarity issues.) **Figures 3-6** show the typical reflow results of the solder paste materials.

## Reflow Results

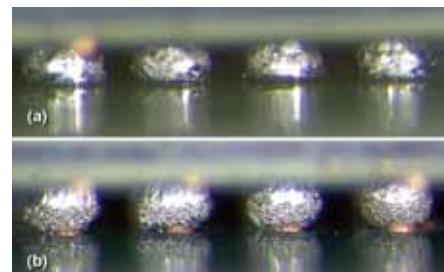
The following results concerning reflow were obtained: 1) Paste B, <20 $\mu\text{m}$  powder, reflowed in air: exhibited solder beading, which may be a lack of coalescence of one or more solder powder particles, and non-wetting to the board pad; 2) Paste B, <20 $\mu\text{m}$  powder, reflowed in nitrogen: solder joints had good coalescence, wetting, and ball collapse; 3) Paste B, 5 $\mu\text{m}$ -15 $\mu\text{m}$  powder, reflowed in air: solder joints exhibited lack of coalescence of more than one powder particle on the same ball, non-wetting to the board pad, and incomplete ball collapse; 4) Paste B, 5 $\mu\text{m}$ -15 $\mu\text{m}$  powder, reflowed in nitrogen: solder joints had good coalescence, wetting, and ball collapse; 5) Paste C, <20 $\mu\text{m}$  powder, reflowed in air: minor solder beading, which may be a lack of coalescence of one solder powder particle, but this was only in a few occurrences. The rest of the solder joints looked good, with good ball collapse and good wetting; 6) Paste C, <20 $\mu\text{m}$  powder, reflowed in nitrogen: good coalescence, wetting, and ball collapse; and 7) Paste C, 5 $\mu\text{m}$ -15 $\mu\text{m}$  powder, reflowed in nitrogen: joints looked very good, with good coalescence, wetting, and ball collapse.

## Reflow Summary

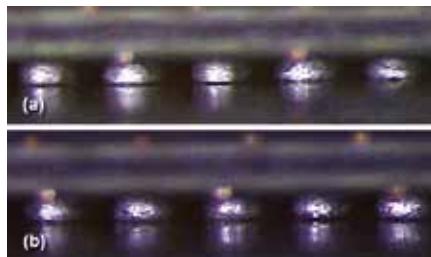
The following observations were made concerning reflow as a result of this work: 1) The best performing solder paste in an air reflow environment was Paste C with <20 $\mu\text{m}$  powder. Except for a few solder joints with minor coalescence issues, the solder joints looked acceptable. The other air-reflowed solder pastes had issues with wetting, coalescence, ball collapse,



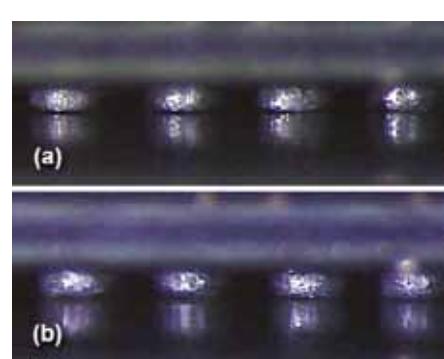
**Figure 3:** Paste B – Air: a) <20 $\mu\text{m}$ ; b) 5 $\mu\text{m}$ -15 $\mu\text{m}$ .



**Figure 5:** Paste C – Air: a) <20 $\mu\text{m}$ ; b) 5 $\mu\text{m}$ -15 $\mu\text{m}$ .



**Figure 4:** Paste B – Nitrogen: a) <20 $\mu\text{m}$  b) 5 $\mu\text{m}$ -15 $\mu\text{m}$ .



**Figure 6:** Paste C – Nitrogen: a) <20 $\mu\text{m}$ ; b) 5 $\mu\text{m}$ -15 $\mu\text{m}$ .

and/or solder beading; 2) All of the nitrogen reflow studies resulted in great solder joint formation; and 3) The results of the reflow experimentation show that solder paste manufactured with either powder size range (<20 $\mu\text{m}$  and 5 $\mu\text{m}$ -15 $\mu\text{m}$ ) will reflow better and provide more acceptable solder joints when reflowed in nitrogen rather than an air environment. A nitrogen reflow environment drastically improved the resulting solder joints versus air reflow.

## Electrical Resistance Measurements

After the components were reflowed onto the boards, electrical continuity analysis was performed by testing the electrical resistance.

Flux	Paste C					
Metal load	79%					
Part	1	2	3	4	5	6
Resistance of <20 $\mu\text{m}$ in Air (on In and Out Pins)	1.7	1.7	1.7	1.7	1.8	1.8
Resistance of <20 $\mu\text{m}$ in Air (on bottom package Daisy Chain)	0.4	0.6	0.6	0.8	0.6	0.8
Resistance of 5 $\mu\text{m}$ -15 $\mu\text{m}$ in Air (on In and Out Pins)	1.5	1.6	1.5	1.4	1.4	1.5
Resistance of 5 $\mu\text{m}$ -15 $\mu\text{m}$ in Air (on bottom package Daisy Chain)	0.5	0.6	0.5	0.5	0.5	0.6
Metal load	79%					
Resistance of <20 $\mu\text{m}$ in N <sub>2</sub> (on In and Out Pins)	0.4	0.4	0.4	0.4	0.4	0.4
Resistance of <20 $\mu\text{m}$ in N <sub>2</sub> (on bottom package Daisy Chain)	0.3	0.4	0.3	0.4	0.3	0.4
Resistance of 5 $\mu\text{m}$ -15 $\mu\text{m}$ in N <sub>2</sub> (on In and Out Pins)	0.2	0.2	0.2	0.2	0.1	0.2
Resistance of 5 $\mu\text{m}$ -15 $\mu\text{m}$ in N <sub>2</sub> (on bottom package Daisy Chain)	0.3	0.1	0.3	0.1	0.1	0.2

**Table 1:** Electrical resistance measurement - Paste C.

Flux	Paste B					
Metal load	79%					
Part	1	2	3	4	5	6
Resistance of <20µm in Air (on In and Out Pins)	1.6	1.7	1.6	1.7	1.8	1.6
Resistance of <20µm in Air (on bottom package Daisy Chain)	0.8	0.7	0.6	0.7	0.6	0.6
Resistance of 5µm-15µm in Air (on In and Out Pins)	1.8	1.9	1.8	1.7	1.7	1.7
Resistance of 5µm-15µm in Air (on bottom package Daisy Chain)	0.6	0.8	0.7	0.8	0.7	0.7
Resistance of <20µm in N <sub>2</sub> (on In and Out Pins)	0.4	0.4	0.4	0.4	0.5	0.4
Resistance of <20µm in N <sub>2</sub> (on bottom package Daisy Chain)	0.3	0.3	0.4	0.4	0.4	0.3

**Table 2:** Electrical resistance measurement - Paste B.

electrical resistance measurement was performed by testing the daisy chain from the in and out pins on the board, and also by testing the daisy chain net that was created just for the bottom package (which can be tested on the back side of the board). These measurements (**Tables 1 and 2**) show that all the reflowed parts had continuity except for one. This component was misplaced on the board (rotated 45°) and the daisy chain did not line up correctly.

Based on this data, the following observations were made. Nitrogen-reflowed boards frequently had a lower electrical resistance than the air-reflowed boards. This lowered resistance may be associated with the fact that the nitrogen reflowed components were dipped and placed with a different piece of equipment than the air reflowed parts, which may have resulted in a less reliable and accurate dipping performance. There is no indication that the resistance is sensitive to the use of two different flux vehicles. It is possible that the flux vehicle formulations were not dissimilar enough to make a difference. It is also possible that there was not enough of a variance between the finished solder joint integrity to

measure from the in and out pins. This is most likely due to the distance the current is traveling. The in and out pins cover more daisy chains than the bottom package daisy chain pattern.

## Future Considerations

During this experiment a number of ideas were considered that would allow for a better understanding of the dipping process and materials used. Among the considerations: 1) New measurement techniques: a) measuring the solder paste on each individual bump, and b) measuring the solder paste thickness within the reservoir; 2) DOE depicting the differences in the dipping reservoir styles (linear vs. rotary); 3) Reliability differences between solder paste and tacky flux: a) thermal cycling and b) drop testing; 4) DOE depicting the effect of smaller component pitches and/or ball/bump sizes, such as 0.35mm and 0.3mm pitch; 5) DOE evaluating the manufacture of PoP components with various pitches and/or ball/bump sizes - making sure that one solder paste material will work well for multiple sizes; and 6) Voiding analysis.

## Summary

The following observations were

noticed a difference in the resistance. The electrical resistance of the 5µm-15µm powder was slightly lower than the resistance of the <20µm powder. This may be because the 5µm-15µm powder delivered a smaller amount of solder to the part than the <20µm powder did, causing less paste to be transferred to the part, as can be seen from the weight measurement results in part 1 of this article. Finally, the bottom package daisy chain resistance is almost always lower than the resistance

made based on the results obtained:

**Solder paste formulation.** Dipping: The best preforming paste is Paste C with the 5µm-15µm powder. This paste provides a more uniform coverage of the dipped solder balls, with a more defined and linear break point than the <20µm powder across all the component bumps. Reflow: When reflowed in air, the <20µm powder in conjunction with Solder Paste C was the best performing paste, producing shiny rounded joints with no evidence of non-coalescence. The use of a nitrogen (low oxygen) reflow environment resulted in drastically improved solder joint formation across all of the reflow studies.

**Assembly processes.** It is important to remember that the dipping and reflow processes play a role that is as significant as that of the solder paste materials that are being used in the development of a successful PoP process. Two assembly processes in particular require attention: dipping and the reflow profile. With respect to dipping: the solder paste dwell time and dip height are the most vital process control parameters. The goal is to achieve optimum dwell time to maximize solder paste coverage of the balls, while allowing the highest UPH (units per hour) throughput. The retraction speed seems to have little effect on the dipping process, from the observations in this set of experiments. However, it has been noted from currently unpublished work that a slower withdrawal speed reduces the incidence of non-pickup from the reservoir. As with the dwell time, this would have to be balanced against the UPH requirement. Regarding the reflow profile: although not studied here, the specific reflow profile is known to have an effect on solder paste reflow [4] and PoP package or board warpage [5], which will impact yields.

## Acknowledgements

This paper appears in two installments. Part 1 addresses the design of experiment, the metrics and data,

and the package-on-package solder paste dipping process. Part 2 addresses the package-on-package solder reflow process, the overall conclusions, and suggestions for future study. ■

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# INTERVIEW

## Direct From IWLPC !

## Electronics Solutions

DOW CORNING

*Chip Scale Review staff conducts an exclusive Interview with Jim Rosson, at IWLPC 2012 Conference & Expo in San Jose, California.*



*Created to explore the endless possibilities of the silicon atom, Dow Corning's expertise, collaboration and broad portfolio of advanced silicone technologies has helped the semiconductor industry overcome challenges and reach new goals for over four decades. The company's proven portfolio offers solutions ranging from die encapsulants for stress relief, to adhesives for sealing and bonding, to thermal interface materials for performance and reliability. Today, Dow Corning has established the global infrastructure to ensure reliable supply, quality and support to its semiconductor manufacturing customers worldwide.*

**Jim Rosson**  
**Market Segment Leader Semiconductor Packaging**  
**Dow Corning Electronic Solutions**

**CSR:** From your perspective, what are some of the major changes underway in semiconductor manufacturing?

**JR:** We've seen the boundary traditionally separating front-end wafer fabrication and back-end packaging operations become increasingly blurred over the past few years. Whereas before, only a handful of IC wafers might have incorporated packaging features processed at the wafer level, leading analysts such as Yole Développement predict that wafer-level packaging will be on nearly a quarter of the 300mm wafers manufactured in 2016.

This so-called "mid-end" has meant opportunities for players at either end of the semiconductor manufacturing value chain, and many of them are rushing to capitalize on this emerging and promising sector. But at the same time, players from both sides have encountered unfamiliar challenges in this evolving space. Namely, they need new materials solutions to address increasingly stringent passivation requirements for power devices, better stress buffers for processing large die

sizes, and they need to support low-heat processing for wafer-level packaging applications.

**CSR:** How is Dow Corning adapting to help customers meet these evolving challenges in the mid-market, and what is driving development of its semiconductor packaging solutions?

**JR:** We're expanding our intellectual resources around wafer-level packaging to develop materials targeting challenges in emerging mid-end applications. For example, the materials typically used for wafer-level packaging applications are conventional dielectric materials, which have weak mechanical strength. That means they can impose unwanted tensile stress on delicate wafers. Meanwhile, packaging manufacturers approaching the middle-market from the back end have sought new processing materials with high-temperature capabilities and broader compatibility with their packaging platforms.

As these two groups have converged in the semiconductor industry's emerging mid-end, there has arisen a strong demand among OSAT

(outsourced semiconductor assembly and test) groups for materials platforms that enable stress reduction and high-temperature performance. Both of those qualities speak to silicone's strengths.

Dow Corning is fortunate to have a long history of expertise as a silicones industry leader to build on in this semiconductor market. Silicones are widely recognized in both the front- and back-end for their excellent thermal and chemical resistance, as well as their optical properties. So, we came to the table with a ready-made platform for innovating new solutions for this sector.

**CSR:** Given its familiarity with the industry, Dow Corning can't be too far behind the curve on emerging demands. Can you discuss any rising challenges and discuss what platforms you're innovating to address them?

**JR:** You raise an important point about platforms. Semiconductor packaging companies competing in this space need robust systems solutions, not just materials. In recent years, Dow Corning has been strategically moving away from its role as a materials supplier in

the traditional sense to more closely collaborate with customers to solve challenges in the mid-end market. Helping to develop cost-efficient systems solutions is one of our top priorities. In this way, we are keeping pace with the curve.

Our collaboration with SUSS MicroTec provides a good illustration of how successful this approach can be. Our two companies worked closely together to develop a new material and equipment system for temporary bonding applications in 3D through-silicon via (TSV) wafer-level packaging. We are now testing it with select beta customers. The technology comprises a simple bi-layer, spin-coated temporary bonding adhesive system. It uses mechanical debond using standard SUSS MicroTec manufacturing equipment, and it's compatible with the thermal and chemical requirements for via middle and interposer TSV processing. In addition, it enables faster room temperature de-bonding for advanced packaging applications.

**CSR:** Earlier you mentioned the need for materials that enable stress reduction and high temperature performance – is there anything under development to meet those demands?

**JR:** Actually, we are here at IWLPC (International Wafer-level Packaging Conference) to give a presentation on recent developments in our photopatternable silicone technology. These aren't new materials. They were introduced a decade ago, and showed some early promise at improving reliability of under-the-bump features thanks to the very low stress they impose.

Unfortunately, these early generation materials had a room-temperature shelf life of a few days, which slowed their

adoption. But, as we mention in our presentation here, we've been able to extend the shelf life of photopatternable silicone technology to five months under room temperature conditions. So, users now have greater flexibility during qualification, prototyping and, most importantly, volume manufacturing.

This advance arrives at a critical juncture for the industry. These materials bring all the thermal stability, low modulus and high flexibility typical of conventional silicones, which enables

enable single, low-stress dielectric coatings on different substrates at thicknesses ranging from 6 to 45 $\mu\text{m}$  that can be patterned using standard photolithographic processes. What makes these materials even more unique is that their required exposure dose is independent of film thickness. As a consequence, the same dose of broadband UV light cures a 10 $\mu\text{m}$  thick film as efficiently as a 40 $\mu\text{m}$  layer, which helps maintain a high process throughput.

**CSR:** Do you have any final thoughts about the larger market?

**JR:** Yes, I'd like to build on what I mentioned earlier about the vital importance of collaborating in this market. One fundamental challenge of the overall semiconductor packaging market – especially for materials companies – is that there are so many companies that all want to solve a problem. As a co-development partner, Dow Corning differs in that we thoroughly review all customer challenges and then determine the best materials solution that will provide the synergies we need to innovate new technologies.

This is a more strategic approach in that it enables us to reach down the value chain and get closer to customer applications to develop system-level solutions in a more collaborative way. This approach has always been part of our company's culture, but we are taking steps today to reinforce it both internally and with customers. Part of our growth plan includes adding and training staff to work with manufacturers in order to develop innovative new solutions, rather than simply supplying off-the-shelf materials. This approach is a win-win for Dow Corning and its customers; and ultimately, it's a win for the semiconductor industry at large.



them to minimize mechanical or thermal stress to wafers during processing. But more importantly, they offer application-specific benefits for large die wafer-level packaging applications.

For example, high-current analog devices are presenting increasing demand for materials that enable passivation layers up to 40 $\mu\text{m}$  thick, which is the sort of application where photopatternable silicones excel. They

# INDUSTRY NEWS

## IWLPC 2012 - Another Smashing Success!

Ron Molnar, *[AZ Tech Direct]*

Interest in Wafer-Level Packaging (WLP) continues to expand as evidenced by the research presented by the early users and suppliers of this IC packaging technology at the most recent International Wafer-Level Packaging Conference (IWLPC) held November 5 – 8, 2012 in San Jose, CA. This premier event, co-organized by SMTA and Chip Scale Review, brought together 500 technologists from around the world to discuss recent advances in wafer level packaging, 3D integration, and MEMS design and assembly.

SMTA Administrator, JoAnn Stromberg noted, “The SMTA continues to welcome the opportunity to work with Chip Scale Review in presenting one of the industry’s strongest events dedicated to bringing together some of the semiconductor industry’s most respected authorities addressing all aspects of wafer-level, 3D, TSV, and MEMS device packaging. From the plenary sessions to the exhibit hall to the conference sessions, we were pleased with the support that was shown for this event as we approach our 10th IWLPC anniversary in 2013.”

This year’s event, led by General Chair, Andrew Strandjord of PacTech USA, and Technical Chair, Luu Nguyen of Texas Instruments, consisted of 29 technical presentations organized in three parallel tracks, two panel discussions, four half-day tutorials, two morning plenary sessions, and was capped off with an intriguing keynote dinner address.

### MORE EXHIBITORS

Although the exhibit hall was expanded this year, it was completely “sold out” again with 52 exhibiting companies as compared to 44 last year. Steady supporters that have exhibited for the past five (5) years included: EV Group, Kyzen Corp., Pac Tech USA, Promex Industries, and TechSearch International.



Sandra Winkler & Karen Williams of New Venture Research



Paula Faria & Auie Sukys of Nanium S.A.



Kim Newman of Chip Scale Review & Jim Rosson & Team of Dow Corning Electronic Solutions



Deborah Patterson & Debi Polo of Amkor Technology



Tim Olson & Garry Pycroft of Deca Technologies

Kim Newman, Publisher of Chip Scale Review, exclaimed, “As the co-organizer, promoting IWLPC is a year long effort resulting in a ‘sell-out’ from the keynote dinner to the exhibits. We



John McCarthy & Rick Trevino of Rudolph Technologies



Hitoshi Yokoyama & Team of Teramikros are pleased that 2012 brought in new faces and companies such as CAD Design Software, Compugraphics, Johnstech, KYEC USA, Sonoscan, and Zymet."

There were actually 20 new exhibitors this year. Other first-timers included Atotech, Deca Technologies, Disco, Dow Corning, Dow Electronic Materials, GDSI, IMT, Milestone, NuSil, Protavic, Rudolph Technologies, SEC, and SigmaTech.

## MORE LEARNING

The four tutorial programs, taught by industry veterans, attracted 90 participants. As was the case last year, the two most popular tutorials once again were "Wafer Level Packaging" by Luu Nguyen, Ph.D., of Texas Instruments and "TSV and Other Key Enabling Technologies for 3D IC/Silicon Integration" by John H. Lau, Ph.D., of the Industrial Technology Research Institute (ITRI).

## MORE SHARING

The morning plenary sessions offered two perspectives on how to attain the many benefits of wafer level packaging. Dr. Nicolas Sillon of CEA-Leti described the 2.5D integration approach using silicon interposers in his presentation titled, "Silicon Interposer:



Keynote Address & Dinner



Dr. Nicolas Sillon of CEA-Leti

Much More than a 'Piece of Silicon.' Dr. Paul Marchal of IMEC described the challenges and benefits of WLP using a complete 3D approach in his presentation titled, "3D Integration – A Corner Technology for Heterogeneous Integration."

The 29 technical talks described many new materials, equipment capabilities, and unique processes developed specifically for the manufacturing of wafer level and MEMS-based IC

products to attain performance goals associated with smaller footprint and shorter interconnects.

## MORE NETWORKING

The sold-out, keynote dinner featured a thought-provoking address, titled "A Trojan Chip in Your Smartphone? It's Coming" by John Ellis, a semiconductor industry veteran turned best-selling author of *Dormant Curse*. He introduced the audience to some of the fictional characters in his novel and warned of some of the dangers that could be exploited in our mobile wireless society.

## MORE CONTRIBUTORS

The success of industry events, like IW LPC, depends on contributions from many volunteers and organizations. In addition to 52 corporate exhibitors, there were 10 corporate sponsors this year led by the three Platinum Level contributors:

Amkor Technology, Invensas, and STATSChipPAC. Kim Newman acknowledged, "We couldn't do it without the support of these various sponsors!"

## ATTEND IW LPC 2013

Planning is already underway for the 10th Anniversary of IW LPC in Fall, 2013. Check the website, [www.iwlpc.com](http://www.iwlpc.com), for more details as they become available.

# Product News

## Ultratech Introduces Superfast 3G CGS Inspection System for Use in Front-, Middle- and Back-end-of-line Production

Ultratech, Inc. introduced an in-line wafer inspection system, the Superfast 3G, which targets a wide range of applications including improved overlay control and enhanced yield. According to the company, the system can be implemented anywhere in the production line—front-, middle- and back-end-of-line. At advanced technology nodes, variations in stress and distortion on a wafer can have a significant impact on device performance and yield. Based on the company's patented coherent gradient sensing technology (CGS), the new system measures over 800,000 points of data per wafer. The system's high data density enables a wide range of applications from one measurement, as within-die, die-to-die and wafer-to-wafer process variations can be characterized quickly and comprehensively. The new system has an edge-exclusion capability of less than 2mm.



Superfast 3G

## Cadence Optimizes Allegro 16.6 Package Designer and SiP Layout Solution

Cadence Design Systems, Inc. announced enhancements to its Allegro® 16.6 Package Designer and System-in-Package (SiP) Layout solution that support low-profile IC package requirements for next-generation smartphones, tablets, and ultra-thin notebook PCs. New features include open cavity support for die placement, a new wire bond application mode that improves efficiency, and a wafer-level-chip-scale-package (WLCSP) capability.

The solution supports a new database

object for open cavity placement that provides enhanced capabilities, such as DRC and 3-D viewing, to support die placement within a cavity of the package substrate. A new intuitive wire bond application mode improves throughput by focusing specifically on the wire bond process. The suite enables WLCSP flow by reading and writing more concise GDSII data. A new advanced package router, based on Sigrity™ technology, accelerates the substrate-level interconnect implementation of a package. Additionally, package assessment, model extraction, signal and power integrity analysis, also based on Sigrity technology, have been integrated into the Allegro 16.6 solution.

## Deca Technologies Unveils New Product Line of Embedded Die Packaging

Deca Technologies has introduced its technology for embedded die packaging, called M-Series™ CSP, which addresses such issues as die shift, package reliability, and cost vs. performance benefits. This new

line is a rugged, fully molded packaging technology that provides popular ball grid array (BGA) style formats while eliminating the need for laminate substrates. It features the company's proprietary Adaptive Patterning™ technology that dynamically creates and implements a unique design for each device during the manufacturing process to adapt for the typical die shift associated with embedded device packaging.

According to the company, Adaptive Patterning allows features such as vias and redistribution traces to dynamically align to shifting die within an embedded device structure. Through the integration of a fixed-design pattern with an adaptive region, the methodology resembles the characteristics of classic wire bonding, yet is realized through a wafer-level build-up flow. With the addition of a dimensional inspection step

and processing through the company's automated design software, it is able to create a unique design for every device within a molded panel, thereby removing the classic barrier of a cost-effective embedded flow.

## New Electroless Copper Process Uses Alternative Reducing Agent

Atotech has introduced a green electroless copper process, called Ecoganth MV, that enables PCB and IC substrate manufacturers to meet technical



and ecological requirements while avoiding harmful substances that are used in conventional

Coverage on ABF-GX 92 processes. The new process is free of formaldehyde, Ni, P, and CN-, making it a biodegradable complexing agent. Furthermore, the alternative reducing agent is compatible with established conditioning and activation processes; its high bath activity also makes it capable for mixed production (ABF resins and cores). The reducing agent has a high throwing power and a deposition rate that is adjustable by temperature and stabilizer dosing.

The process primarily targets the IC substrate manufacturing process based on the semi-additive process (SAP) technology. The development was therefore focused on the ionic activation systems of the company's Neoganth® series. For optimal plating behavior, the process uses a new stabilizer system that enables blister-free deposition on standard base materials such as Tg FR4, halogen-free and BT base materials. It also makes co-deposits such as nickel, superfluous, according to the company.

## New X-ray Inspection System Offers Cloud Inspection and Automation

Creative Electron launched its TruView® Elite X-ray inspection system. The microfocus (90kV or 150kV) x-ray sources in the new system target PCBA analysis, single component failure inspection, medical device quality control, and other applications. The company says that the amount of automation and software enable the full inspection of 22"x22" objects. The system uses a patent-pending reel-to-reel



TruView Elite X-ray inspection system

(R2R) system capable of inspecting thousands of parts per hour. The system's modular design is scalable allowing for the addition of features as necessary over time. The company says its product exceeds all standards, including CCAP101, AS5553, MIL-STD-883C, IDEA STD-1010-A, and the upcoming AS6081 and AS6171. The system's cloud inspection capability allows operation from anywhere in the world. Other system specifications include a 1"x2" or 2"x2" FP field of view (4" diameter IID), a resolution of 1µm, and a magnification of 2,000X.

### High-Performance BGA Socket Operates at Bandwidths Up to 10GHz

Ironwood Electronics has introduced a high-performance BGA socket for 0.8mm pitch 900 ball FCBGA - SG-BGA-8029. The socket operates at bandwidths up to 10GHz with less than 1dB of insertion loss. The contact resistance is typically 20milliohms per I/O. The socket connects all pins with 10GHz bandwidth on all connections and is mounted using supplied hardware on the target PCB with no soldering. The socket also incorporates a quick insertion method using shoulder screws and swivel socket lid so that ICs can be changed out quickly. A heat sink and a fan dissipate 14.55W. The application of the socket is to verify the function of the non-nolatile DRAM controller



SG-BGA-8029 sockets.

that reads and writes data directly into DDR3 DRAM, with a configurable data rate from DDR3-800 through DDR3-1600. The socket also features an independent compression mechanism to accommodate package manufacturing variations. The specific package sizes accommodated by the socket are 0.8mm pitch 25mm x 25mm, 30x30 ball array. The SG-BGA-8029 sockets are constructed with high-performance and

low inductance gold-plated embedded wire on elastomer as interconnect material between device and PCB. The temperature range is -35C to +100C. The pin self-inductance is 0.15nH; and the mutual inductance is 0.025nH. Capacitance to ground is 0.01pF. Current capacity is 2Amps per pin.

### SONIX Introduces Molded Flip-Chip Enhancement

SONIX has introduced its latest

The logo for the International Wafer-Level Packaging Conference (IW LPC). It features a stylized globe with a purple and yellow color scheme. The text "SAN JOSE, CALIFORNIA" is curved along the top edge of the globe. The acronym "IW LPC" is prominently displayed in large, bold, purple letters across the center of the globe. Below the globe, the full name "INTERNATIONAL WAFER-LEVEL PACKAGING CONFERENCE" is written in a smaller, white, sans-serif font.

## >> Call For Papers

SMTA and Chip Scale Review are pleased to announce plans for the 10th Annual International Wafer-Level Packaging Conference and Tabletop Exhibition. This premier industry event explores leading-edge design, material, and process technologies being applied to Wafer-Level Packaging applications.

The IW LPC Technical Committee would like to invite you to submit an abstract for next year's program. Deadline for submittal is March 15th, 2013.

**SUBMIT ABSTRACT ONLINE:** [www.iwlpc.com](http://www.iwlpc.com)

### Suggested Topics to Submit

#### WAFER LEVEL PACKAGING

- Wafer Level Chip Scale Packaging (WLCSP), Flip Chip, Fan-Out and Redistribution, Wafer and Device Cleaning, Nanotechnology, Quality, Reliability, and COO

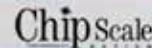
#### MEMS PACKAGING

- MEMS Processes and Materials, MEMS Design Tools or Methods, Nano-MEMS and Bio-MEMS, Integration, MEMS Integration and Interconnects, RF/wireless, Sensors, Mixed Technology, Optoelectronics

#### 3-D PACKAGE INTEGRATION

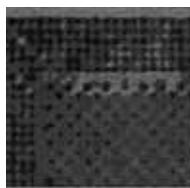
- 3D WLP, Thru Silicon Vias (TSV), Silicon Interposers, Stacking Processes (W2W, D2W, D2D), IC Packaging Substrate, Embedded Die and Passives, TSV Integration: FEOL vs BEOL

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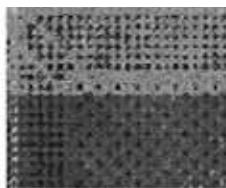


For more information on the conference, please contact Patti Hvidhyld at 952-920-7682 or to [patti@smta.org](mailto:patti@smta.org). For information to exhibit and sponsorship opportunities please contact Seana Wall at 952-920-7682 or to [seana@smta.org](mailto:seana@smta.org).

Molded Flip-Chip Imaging (MFCI™) enhancement that targets improvement of image quality and defect detection in molded flip-chips - including MUF applications - with or without polyimide (PI) layers. According to the company, the enhancement has been designed to reduce the impact of the scattering and attenuation effects of filler particles in mold compounds and PI layers allowing for the use of frequencies up to 200MHz in some cases for improved image quality. Configured through the company's WinIC software, the enhancement improves spatial resolution, contrast, edge definition, and detection of hidden defects when inspecting samples containing materials that scatter or attenuate ultrasonic signals.



Original Image



Improved bump resolution



Hidden defect revealed

### **Qualtera Targets Semiconductor Yield, Product and Test Engineering with Silicodash**

Qualtera unveiled Silicodash, an automated, cloud-hosted decision support system (DSS) for semiconductor test data analysis. The new product rapidly identifies, analyzes, and reacts to test, quality and yield issues. It is being used in high-volume beta trials with major European semiconductor IDMs and is available now.

According to Qualtera, the product is a solution for fabless companies, IDMs, foundries and test houses that need more relevant and timely information from the semiconductor manufacturing chain. Currently, engineers need to compile test data from multiple sources and

then add their own analysis, a process that can take hours or even days. By using the new software, the analysis and reporting processes

are, to a large extent, automated and can be completed in minutes. Designed to handle all types of test data regardless of product type, data source or volume, the new product provides a real-time, detailed overview of the entire manufactured volume, enabling the identification, analysis, and action on quality or yield issues in manufacturing and test processes.

Implemented as a cloud-hosted service, the product does not require software to be installed locally and allows engineers in multiple locations to securely access and share data in real-time, providing full transparency in the semiconductor manufacturing and test processes. It was designed for jobs of all sizes: from just a few wafers, up to analyzing test data for high-volume chip manufacturing. Daily, weekly or quarterly overview reports are generated and updated on a real-time basis along with drill-down features and custom feedback alerts for early problem detection. ●



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### SEMICON Korea 2013

January 30–February 1  
Seoul, Korea  
[www.semiconkorea.org](http://www.semiconkorea.org)

### LED Korea 2013

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[www.led-korea.org](http://www.led-korea.org)

### SEMICON China 2013

March 19–21  
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[www.solarconchina.org](http://www.solarconchina.org)

### SOLARCON<sup>®</sup> China 2013

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[www.fpdchina.org](http://www.fpdchina.org)

### SEMICON Singapore 2013

May 7–9  
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[www.semiconsingapore.org](http://www.semiconsingapore.org)

### SEMICON Russia 2013

May 15–16  
Moscow, Russia  
[www.semiconrussia.org](http://www.semiconrussia.org)

### SEMICON West 2013

July 9–11  
San Francisco, California  
[www.semiconwest.org](http://www.semiconwest.org)

### SEMICON Taiwan 2013

September 4–6  
Taipei, Taiwan  
[www.semicontaiwan.org](http://www.semicontaiwan.org)

### PV Taiwan 2013

October 30–November 1  
Taipei, Taiwan  
[www.pvtaiwan.com](http://www.pvtaiwan.com)

### SEMICON Europa 2013

October 8–10  
Dresden, Germany  
[www.semconeuropa.org](http://www.semiconeuropa.org)

### PE 2013 Exhibition and Conference

October 8–10  
Dresden, Germany  
[www.plastic-electronics.org](http://www.plastic-electronics.org)

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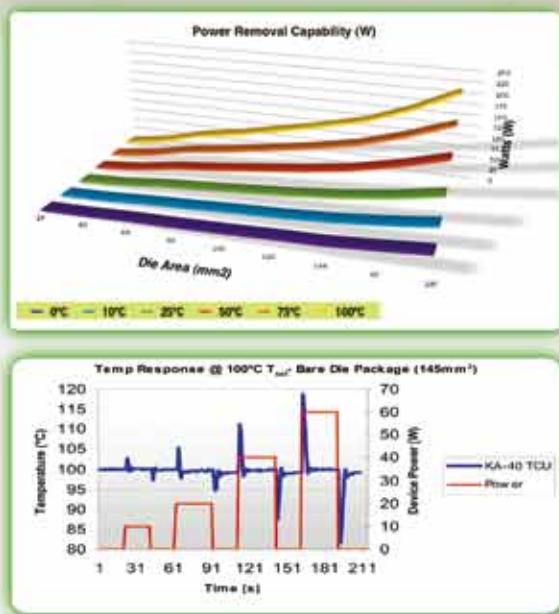
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