

# Chip Scale® Review

ChipScaleReview.com

R E V I E W

*The International Magazine for the Semiconductor Packaging Industry*

Volume 17, Number 6

November • December 2013

**Test sockets for the parallel world**

P. 11

**Failure analysis**

**Ultra-high BW PoP**

**Wet-etch processing for TSVs**

**C4 flux deposition challenges**

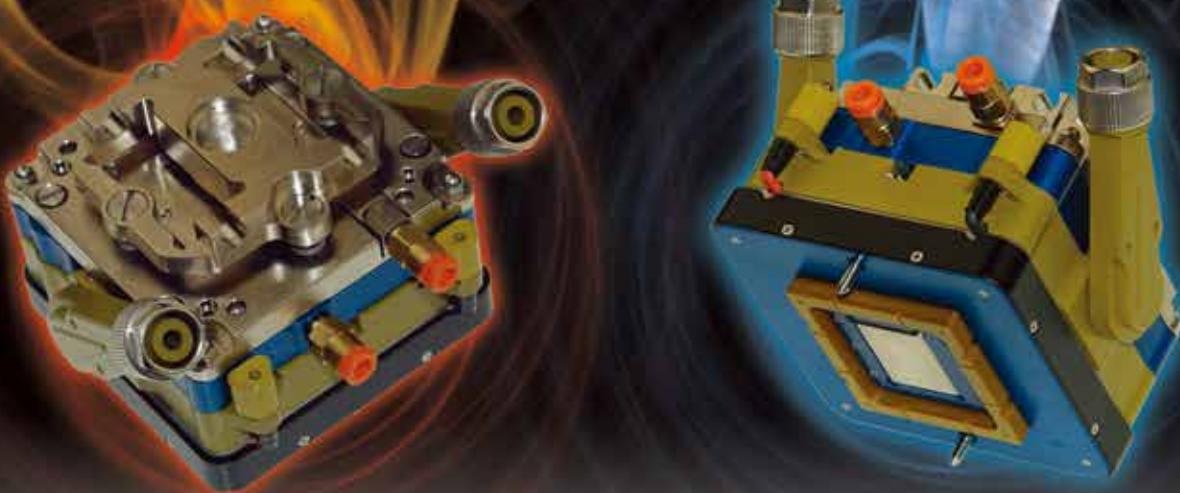
**IC package inspection & metrology**



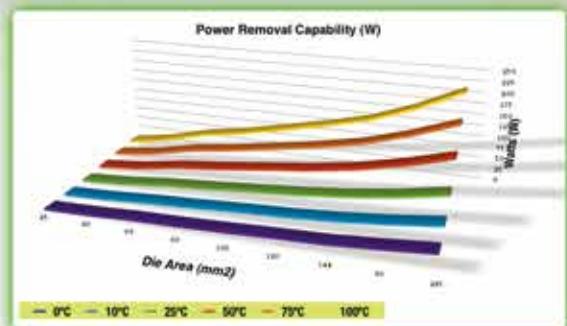
introducing

## Advanced Thermal Management

...it's elemental



**Essai's New Generation Thermal Management Systems Offer Performance & Versatility for I.C. Temperature Testing**



**Highly efficient** thermal response with Thermo-Electric Cooler, Liquid & Heater assist based technologies

**Distributed force** loading between the Die & Substrate that prevents silicon cracking while maintaining proper thermal contact

**Smaller footprint** that can fit in various applications – manual or automated System Level & Final Test handlers

**Integrated vacuum pickup** designed for handler applications

**Cold test capable** with efficient condensation abatement features

Available for **wide range of packages**:  
Bare Die, Lidded, Thin Core, and Ultra Small Form Factor devices

**essai**  
[www.essai.com](http://www.essai.com)

# CONTENTS

November • December 2013  
Volume 17, Number 6



The drive toward increasing parallelism in testing semiconductor devices raises new challenges for test sockets. The front cover shows an assembly of Centipede's contactor cartridges configured to test an array of 40 Greenlant SATA drives at KYEC facilities in Chu Nan. During testing over a full range of temperatures, the contactor assembly is enclosed in a sealed mini-chamber to avoid condensation.

Cover image courtesy of KYEC.

**Chip Scale**  
REVIEW  
ChipScaleReview.com

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging  
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,  
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

## FEATURE ARTICLES

### High-resolution nondestructive 3D imaging

Bruce Johnson, *Carl Zeiss X-ray Microscopy, Inc. (formerly Xradia)* **22**

### 3D IPAC: a new concept in integrated passive and active components

P. Markondeya Raj, Saumya Gandhi, Srikrishna Sitaraman, Venky Sundaram, Rao Tummala,  
*Georgia Institute of Technology* **26**

### C4 interposer requirements driving high-precision flux deposition

Fernando D. González, *Sono-Tek Corp.*; Ricky Bennett, *Assembly Process Technologies LLC*,  
Andy C. Mackie, *Indium Corporation* **32**

### Ultra high-bandwidth PoP infrastructure development

Wael Zohni, *Invensas Corporation* **38**

## Copper Pillar $\mu$ Bumps

VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND  
TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

[www.amkor.com](http://www.amkor.com)

### PRESENTING THE EVOLUTION OF THE FLIP CHIP BUMP

From the diverse solder bumping solutions of the last decade to the large scale production of today's fine pitch copper pillar bumps, Amkor will provide a solution for your packaging challenges.

Amkor remains at the forefront of semiconductor packaging development and performance.

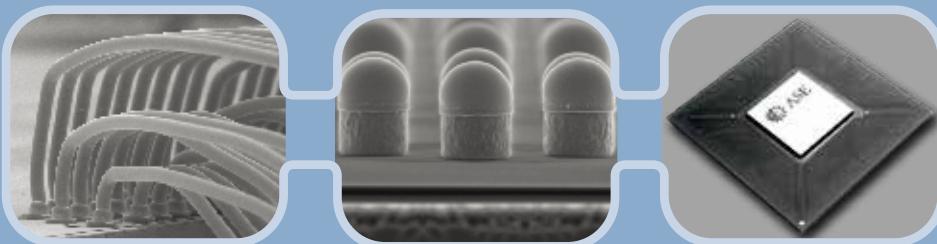
### ELIMINATE THE GUESSWORK

and talk to us today about our extensive offering of next generation design, assembly, and test solutions.

**Amkor**  
Technology®



**ASE Group: The world's largest provider of independent semiconductor manufacturing services in assembly, test, materials and design manufacturing.**



Copper Wire • aQFN™ • a-fcCSP™ • aMAPPoP™ • SiP Module • Cu Pillar



## FEATURE ARTICLES

<b>Lowering cost of silicon etch for revealing TSVs</b> Laura B. Mauer, John Taddei, Ramey Youssef, <i>Solid State Equipment LLC</i>	<b>42</b>
<b>Inspection and metrology in the tape-and-reel process</b> Carl Truyens, Piet Kerckhove, <i>KLA-Tencor</i>	<b>46</b>
<b>Field-driven test contacting solution</b> Shamal Mundiyath, <i>JF Microtechnology Sdn Bhd</i>	<b>50</b>

## DEPARTMENTS

<b>From the Publisher Good-bye 2013!</b> Kim Newman, <i>Chip Scale Review</i>	<b>4</b>
<b>MEMS Market Trends Emergence of the trillion sensors opportunity</b> Janusz Bryzek, <i>Fairchild Semiconductor</i>	<b>7</b>
<b>Test Trends Test sockets for the parallel world</b> Tom Di Stefano, <i>Centipede Systems</i>	<b>11</b>
<b>Industry News</b> <i>Chip Scale Review Staff</i>	<b>14</b>
<b>Tech News Diagnosing component failures often requires a system-level approach</b> Paul Sakamoto, <i>Contributing Editor</i>	<b>49</b>
<b>Product News</b> <i>Chip Scale Review Staff</i>	<b>53</b>
<b>Advertiser Index, Advertising Sales</b>	<b>56</b>

**MICRO  
CONTROL  
COMPANY**

# BURN-IN VALUE MENU

*... satisfy your hunger for low-cost burn-in!*

1) Choose the size of your LC-2 Burn-In with Test System  
 2) Add refrigeration to your order, if it suits your taste  
 3) Enjoy!

8-slot, single-zone reliability burn-in oven

32-slot, multiple temperature zone reliability burn-in oven

64-slot, production burn-in oven

**Nutrition Facts**  
 Serving Size:  
 Choose the Size You Need  
 Servings Per Container: 1

Amount Per Serving	100% Daily Value*
Total I/O	up to 256 channels per BIB.
Total Power	up to 500 Amps of DUT current available per BIB, up to 10 individually programmable power supplies, up to 150 Volt power supply outputs.
Total Flexibility	up to 8M vector memory depth with scan capability per BIB, individual temperature control up to 50 Watts, compatible with many BIB sizes.

\*Micro Control Company  
7956 Main Street NE  
Minneapolis, MN 55432

Phone: 763-786-8750  
Toll Free: 800-328-9923  
[www.microcontrol.com](http://www.microcontrol.com)

Chip Scale Review • November • December • 2013 [ChipScaleReview.com] 5

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

## STAFF

**Kim Newman** Publisher  
[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)

**Lawrence Michaels** Managing Director  
[lkm@chipscalereview.com](mailto:lkm@chipscalereview.com)

**Debra Vogler** Senior Technical Editor  
[dvogler@chipscalereview.com](mailto:dvogler@chipscalereview.com)

## CONTRIBUTING EDITORS

**Dr. Thomas Di Stefano** Contributing Editor  
[tom@centipedesystems.com](mailto:tom@centipedesystems.com)

**Jason Mirabito** Contributing Legal Editor  
[mirabito@mintz.com](mailto:mirabito@mintz.com)

**Paul M. Sakamoto** Contributing Editor Test  
[paul.sakamoto@comcast.net](mailto:paul.sakamoto@comcast.net)

**Dr. Ephraim Suhir** Contributing Editor Reliability  
[suhire@aol.com](mailto:suhire@aol.com)

**Sandra Winkler** Contributing Editor  
[slwinkler@newventureresearch.com](mailto:slwinkler@newventureresearch.com)

## EDITORIAL ADVISORS

**Dr. Andy Mackie (Chair)** Indium Corporation

**Rolf Aschenbrenner** Fraunhofer Institute

**Dr. Thomas Di Stefano** Centipede Systems

**Joseph Fjelstad** Verdant Electronics

**Dr. Arun Gowda** GE Global Research

**Dr. John Lau** Industrial Tech Research Institute (ITRI)

**Dr. Venky Sundaram** Georgia Institute of Technology-3D Systems Packaging Research Center

**Fred Taber** BiTS Workshop

**Dr. Leon Lin Tingyu** National Center for Advanced Packaging (NCAP China)

**Francoise von Trapp** 3D InCites

## SUBSCRIPTION-INQUIRIES

Chip Scale Review

Effective immediately

All subscription changes, additions, deletions to any and all subscriptions should be made by email only to

[subs@chipscalereview.com](mailto:subs@chipscalereview.com)

Do not leave subscription inquiries on the company voicemail system.

Advertising Production Inquiries:

**Kim Newman**

[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)

Copyright © 2013 Haley Publishing Inc.

Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$100 per year to Canada or \$125 per year to other countries. In the U.S. subscriptions by first class mail are \$95 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

# FROM THE PUBLISHER



## Good-bye 2013!

This makes 2013 a wrap for us at *Chip Scale Review*. I would like to extend a heartfelt thank you to the many contributors to this magazine throughout the year—the many authors that spent tireless hours penning for *Chip Scale Review* and the many supporters of advertising! We thank each and every one. If it weren't for the advertising community, there wouldn't be trade publications.

We close out the year with a lineup you won't want to miss. The front cover depicts the column that brings us closer to a parallel world of test sockets. The team at Georgia Tech PRC bring us the latest advances in 3D IPAC – a new concept in integrated passive and active components. A must read is an exclusive feature from KLA-Tencor covering packaging inspection and metrology. If you missed the TSensors Summit at Stanford University in October, Janusz Bryzek of Fairchild Semiconductor will bring you up to date on the trillion sensors market opportunity. Zeiss (formerly Xradia) reports on high-resolution nondestructive 3D imaging. The authors at Sono-Tek Corporation, Assembly Process Technologies LLC, and Indium Corporation cover C4 flux deposition challenges, while Invensas infrastructure development for ultra-high bandwidth for PoP.

Read all about how IWLPC - The International Wafer-Level Packaging Conference unfolded this year on page 18. Be sure to save the date for other upcoming industry events. Chip Scale Review also supports the 3D ASIP Conference December 11-13. Join industry leaders at RTI International's 3D ASIP Conference in San Francisco and explore the latest technologies and market insights into 2.5/3D device and systems integration. Visit [www.3dasip.org](http://www.3dasip.org) for a complete agenda and full program details. The Power of Integration European 3D TSV Summit is the new must-attend event focusing on 3D TSV and the full supply chain taking place January 21-22, 2014 in Grenoble France. Email Yann Guillou with the SEMI Europe Grenoble office at [yguillou@semi.org](mailto:yguillou@semi.org) for further details.

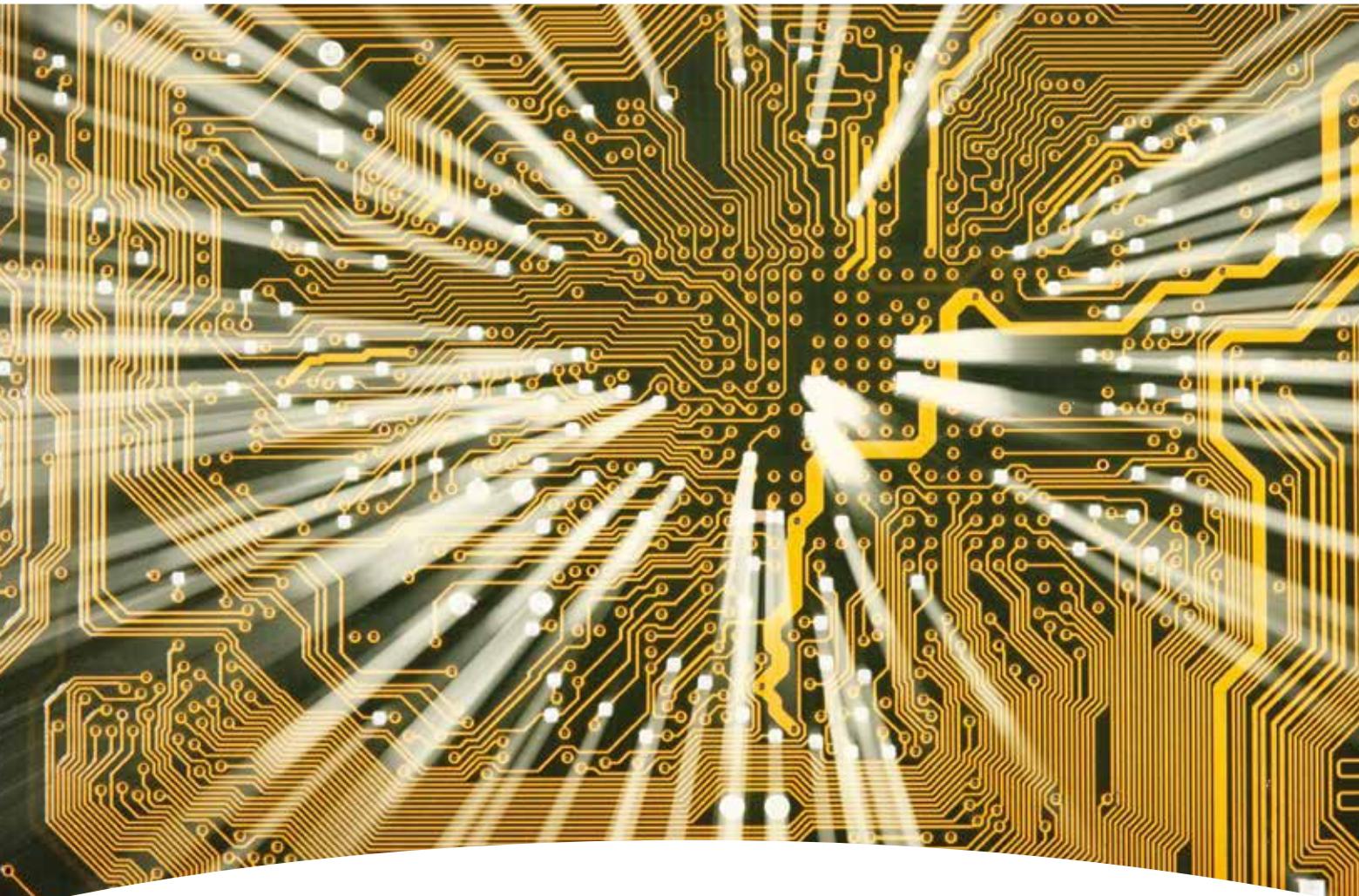
Be sure to inquire about the 2014 Chip Scale Review editorial and issue calendar. Contact your CSR sales representative or the publisher for the e-copy and discover the top challenges the industry has to tackle to enable the advancement of semiconductor packaging.

The end of the year typically is the time for many companies to plan and budget. Save your budget for advertising in 2014 and of course, for Chip Scale Review. There are six issues planned while the monthly e-newsletter carries technical articles, news, products and industry events. The more strategic marcom program will have a combination of both venues.

Here's wishing our CSR community all the best in 2014.

*Kim Newman*  
Publisher

# reduce soft errors



Deliver more density on your IC packages without soft errors.

Honeywell RadLo™ low alpha packaging materials help eliminate soft errors and single event upsets by reducing alpha emissions, a significant source of these problems. This is becoming increasingly important as chip dimensions and designs continue to miniaturize. Our leadership

and expertise in low alpha refining and metrology mean that Honeywell can help you meet critical alpha emission levels.

**Honeywell reliability. Reliable low alpha.** Make sure to ask your suppliers if they are using Honeywell RadLo low alpha materials for their chip packaging processes.

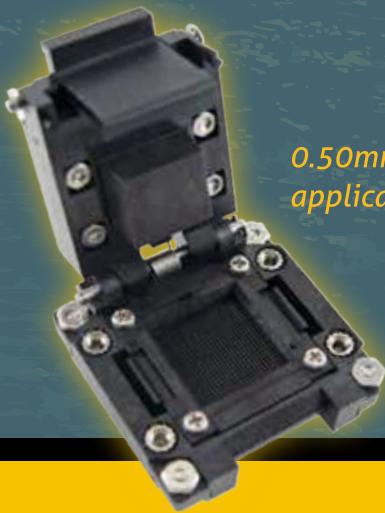
## Honeywell

Find out more by visiting us at [www.honeywell-radio.com](http://www.honeywell-radio.com)

# Oh Snap

We've done it again

**INTRODUCING THE M-SERIES SOCKET-**  
*the first product from our  
innovative new SnapFit Process.*



0.50mm BGA burn-in  
applications



### **Now H-Pin Burn-in Test Performance is Faster and Easier.**

Once again, we've created a testing solution to make your life easier. SnapFit products deliver superior reliability and performance while significantly reducing product cost and production time.

*Let us make your burn-in test a snap. Call 972-258-2580 for a quote.*

[www.plastronics.com](http://www.plastronics.com)  
email us: [sales@plastronics.com](mailto:sales@plastronics.com)

# MEMS MARKET TRENDS



## Emergence of the trillion sensors opportunity

By Janusz Bryzek *[Fairchild Semiconductor]*

Sensors started an adoption of IC packaging technology to enable lower cost and higher volume capability in the 1970s with the first hybrid (ceramic) packages used for pressure sensors by National Semiconductor. This process was accelerated by the emergence of the mobile market (cell phones, tablets, games, cameras, etc.). Absorption of sensors into this segment exploded from 10 million units in 2007 (triggered by the emergence of the iPhone and the Wii gaming console) to 3.5 billion in 2012—primarily in cell phones and tablets.

Sensors in mobile devices (microphones, acceleration, magnetic, gyros, pressure, humidity, proximity, light, IR, etc.) have adopted IC packaging, primarily QFN, LGA and cavity types. What is interesting about this development, is that it represents the first real standardization in the MEMS industry.

Recently, visionary organizations (referenced below) started to forecast the sensor demand growing from billions in 2012 to trillions within the next decade. The demand is expected to be driven by the emergence of sensor-based smart systems. Harbor Research [1] defines smart systems as a fusion of computing, communication, and sensing in the era of the pervasive internet, wherein people, devices, sensors and businesses are connected and able to interact. Harbor Research [1] considers smart systems the biggest business opportunity in the history of business.

High-volume deployment of perhaps 100 new sensors will create demand for new packaging technologies accommodating unique requirements of these new sensors, such as compatibility

with body fluids in mobile devices, compatibility with wet chemicals, disposability, integration of sensor arrays, etc. High-performance sensors will need to address low cost zero stress packaging and hermeticity. Many of the emerging sensor types are likely to be disposable (e.g., for testing body fluids). Low cost interfacing of disposable sensors with mobile devices will require a dedicated development.

A new low cost disruptive technology – 3D printing – has emerged. It has the potential to be massively adopted in the trillion sensor market, as it will allow cost competitive printing of VLSI electronics including radios and antennas, diversified sensor arrays, batteries, energy scavengers, and packages on a single substrate. Another printing technology – paper microfluidics – has the potential to be massively deployed to support digital health applications. New materials that have the potential to migrate either to packages or to sensors have also come to the fore. One such material is graphene. The “buzz” about graphene is coming from a number of sources.

### Pointers to the potential for a trillion sensors

In 2012, only four categories of sensors (microphone, acceleration, gyro and compass) shipped about a billion units each. Now, multiple developments appear to indicate a sensor market growth to a cumulative volume of a trillion units by 2023. Such potential growth is the result of several global “tides” described below along with a number of recent referenced presentations that support this observation.

### Exponential technologies.

Exponential technologies were defined in the book *Abundance* [2] as those enabling the growth of global supplies and services in excess of the demand for them. In just one generation (20 years), they are expected to create abundance and equality between supply and demand on earth. Based on history, eight technologies are classified as exponential: 1) biotechnology and bioinformatics, 2) computational systems, 3) networks and sensors, 4) artificial intelligence, 5) robotics, 6) digital manufacturing and infinite computing, 7) medicine, and 8) nanomaterials and nanotechnology.

Sensors are not only one of the eight exponential technologies, but are also embedded in other exponential technologies. *Abundance* projects the need for 45 trillion networked sensors in about 20 years, helping to solve global problems such as the shortage of food, energy, water, healthcare, education, as well as global pollution.

**Emerging technologies.** Emerging technologies are defined by the World Economic Forum and Cientifica as those that arise from new knowledge or the innovative application of existing knowledge and lead to the rapid development of new capabilities. Emerging technologies also have the potential to disrupt or create entire industries. Such technologies are projected to have significant systemic and long-lasting economic, social and political impacts, as well as create new opportunities and challenges to address global issues.

The Summit on the Global Agenda 2011 in Abu Dhabi led to the compilation of the Top 10 Emerging Technologies

with the greatest potential to provide solutions to the most compelling social, economic and environmental challenges. Among the compilation are the following segments: 1) informatics for adding value to information, 2) synthetic biology and metabolic engineering, 3) Green Revolution 2.0 – technologies for increased food and biomass, 4) nanoscale design of materials, 5) systems biology and computational modeling/simulation of chemical and biological systems, 6) utilization of carbon dioxide as a resource, 7) wireless power, 8) high energy density power systems, 9) personalized medicine, nutrition and disease prevention, and 10) enhanced education technology. While broadly diversified, many of these emerging technologies represent or use smart systems, a fusion of sensors, computing and communication, and therefore represent another potential contributor to the emergence of a trillion sensors.

**Sensory swarms.** Sensory swarms are defined as huge volumes (swarms) of wireless sensor nodes deployed locally or globally. Sensory swarms form a foundation for multiple global tides, such as the internet of things and everything, CeNSE (see below), and digital health. Trillion sensor forecasts for sensory swarms come from several organizations. The Qualcomm Swarm Lab at UC Berkeley projects 1000 radios per person on earth by 2025, with trillions of connected sensor-based devices as the swarm around the edge of the Cloud, to link the cyber and physical/biological worlds. It is reasonable to assume that each radio may support several sensors.

Bosch has presented [3] a vision for 7 trillion sensors (sensory swarms) to serve 7 billion mobile subscribers by 2017. Up to 18 sensors have already been embedded in mobile devices today, with close to 100 in high-end cars, and up to 100 in high-end smart homes. Bosch's vision for 1000 sensors per average person by 2017 seems reachable.

In its presentation [4], Texas

Instruments outlined the vision for growth of internet-connected devices to 13 trillion by 2025, with major markets being fixed and mobile communication, computers, industrial, medical, military and aerospace. TI expects MEMS, specifically sensors, to be the enabling technology for such growth. The “intelligent ambient” (as the company refers to its vision of internet-connected devices), based on wireless sensor nodes, will adapt, anticipate, be transparent, dependable, and autonomous.

**Internet of things (IoT).** IoT [5] is defined as sensors and actuators embedded in physical objects, often using internet protocol (IP) [6]. IoT is starting to gain a momentum and it seems to be crossing the “chasm” in a path to becoming a market “tornado” [7]. Major IoT sensor applications are expected to be focused on information and analysis (such as tracking behavior of persons, things and data through space and time, enhanced real time situational awareness of the physical environment, and sensor-driven decision analytics through deep analysis and data visualization), and automation and control.

Libelium [8] and Beecham Research [9] forecast IoT deployment to create smart cities, and monitoring of the environment, water, materials, energy, agriculture, farming, buildings, retail, transportation, public safety, industrial controls, ehealth and IT. In China's most recent 12th 5-year plan, IoT was promoted to one of the seven strategic emerging industries with about \$1B government funding allocated over the next five years [10].

**CeNSE.** Hewlett Packard, in multiple presentations from 2010 to 2012 [11], introduced a Central Nervous System for the Earth (CeNSE). CeNSE is based on detectors and actuators, and is forecast to reach a trillion units by 2018. Key market segments include climate monitoring, oil exploration and production, assets and supply chain tracking, smart highway infrastructure, tsunami and earthquake warning, smart

grid and homes, and structural health monitoring. The first deployed CeNSE system included 1 million wireless accelerometers on a 10x10km site for Shell Oil exploration.

**Context-aware computing.** Intel has presented [12] the emergence of sensors for context-aware computing. The company expects that sensors supporting such systems will absorb a trillion sensors by 2020-2022. Out of a trillion sensors, 70% will be solving problems and 30% will be enhancing lifestyles. The applications will include sensing all around an individual's needs, and understanding situations (e.g., mood of the person you meet), all-around devices, personal health, social interactions, planet context, and universe context.

**IBM 5 in 5.** IBM unveiled the seventh annual "IBM 5 in 5" – a list of innovations that have the potential to change the way people work, live and interact during the next five years. These five sensor/actuator innovations include touch (ability to touch through your phone), sight (a pixel will be worth a thousand words), hearing (computers will hear what matters), taste (digital taste buds will help you to eat smarter), and smell (computers will have a sense of smell). The IBM 5 in 5 is based on market and societal trends, as well as emerging technologies from IBM's R&D labs around the world that can make these transformations possible.

**Digital health.** Digital health based on a broad range of health sensors connected to mobile platforms (cell phones, tablets, etc.) emerges as a solution to the skyrocketing cost of medical care, aging population and lack of medical care in developing countries.

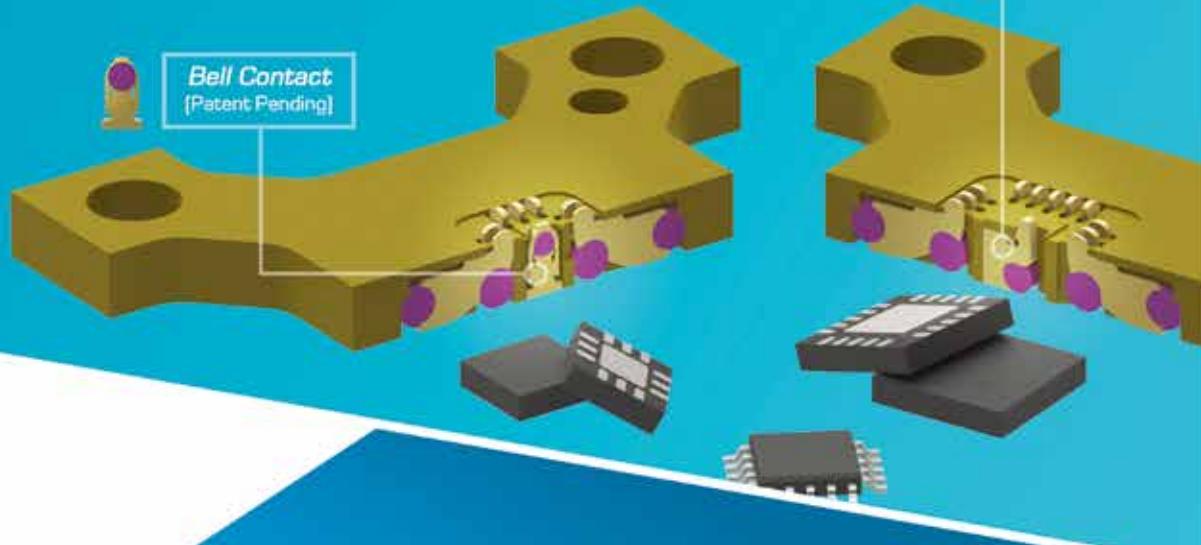
Visible examples of the evolving market include the 2013 CES Show in Las Vegas, where there were 19 Digital Health conference sessions and 350 exhibitors in the Digital Health section. Another example is Qualcomm's \$10 million Tricorder X PRIZE [13], a 42-month competition to bring the sensing of 15 of the most common human diseases to the cell phone. Nokia



We Bring Possibilities

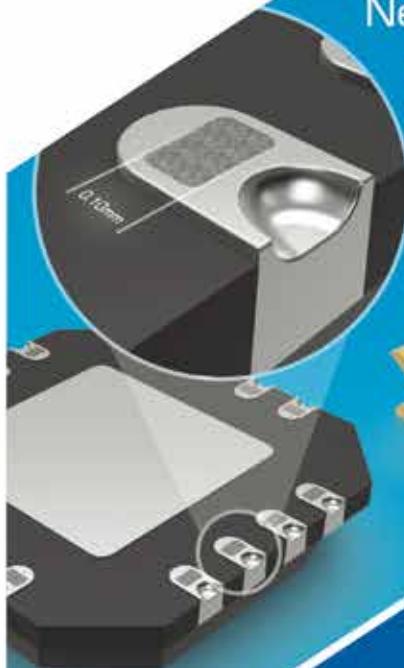
Need Compliant Grounding for  
small packages of 2x2 and above?\*

We have the solution.



Need Short Wiping of 0.1mm  
for your wettable/dimple pad?\*

We have the solution.



Zigma  
[Patent Pending]



Explore these  
new exciting and  
outstanding solutions on  
our website or with our nearest  
sales channel partner today.

Find out more at:

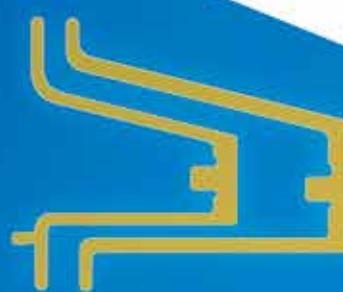
<http://www.jftech.com.my>  
World class company in semiconductor industry

Or e-mail us at:

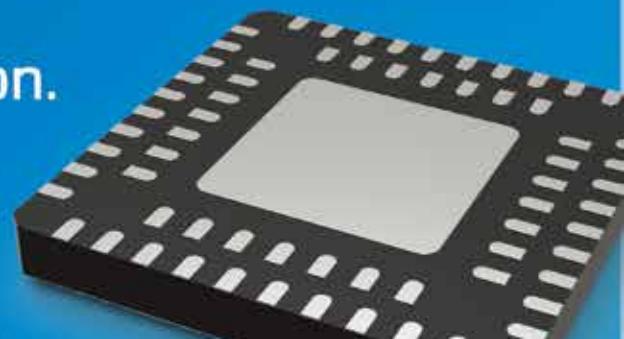
[sales@jftech.com.my](mailto:sales@jftech.com.my)

Need Scrubbing  
Solution for Dual  
Row packages ?\*

We have the solution.



Alpha  
[Patent Pending]



announced a similar competition [14] with a \$2.25M prize. The emergence of location-based advertising as well as activity-based advertising will be based on sensors in the body, on the body, and out of the body. These systems use personal behavior information derived from sensors.

### Trillion sensor vision

Historically, each new sensor type took over 20 years to move from concept prototypes to volume production. To accelerate this cycle, and thereby accelerate solutions to global problems (e.g., hunger on earth, reduction of global warming, development of green energy and clean water, slowdown of global population growth, reduction of skyrocketing cost and lack of medical care, etc.), a Trillion Sensors (TSensors) Roadmap (**Figure 1**) development has been initiated. The first step of this roadmap was the TSensors Summit organized at Stanford University in October 2013 [15]. The objective was to gather emerging sensor applications

from visionaries. At the conference, several organizations presented their visions for a continued growth to trillion(s) of sensors. Market research companies don't yet see this growth (see Yole's forecast in the figure), so the explosion to trillion(s) is likely to be driven by applications not yet envisioned by leading market research organizations. As sensor development has been historically much longer than pure semiconductor technologies, the TSensors Roadmap development is being launched to improve the visibility of future needs to enable accelerated development. Based on these applications, several working groups are planned to be formed, each focused on development of an acceleration strategy for specific ultra high-volume sensor types supporting these applications.

### Summary

The growth of the sensor market from billions to trillions over the next decade will face multiple challenges. One of the most important hurdles to overcome will be the potential for the growth of volumes by three orders of magnitude. Associated with volume explosion, there will be a correlated price pressure and solutions may require disruptive technologies.

Emergence of a trillion sensor potential represents a significant opportunity for the packaging industry. Probably the most important potential is that shipments could grow by perhaps two orders of magnitude in the coming decade. New disruptive technology – 3D printing – has entered the market and may evolve as an instrumental innovation for the trillion sensors vision. The emergence of 3D printing may fuse ICs, sensors, batteries and packages onto one manufacturing platform.

The by-products of the global tides driving market growth will be longer and healthier lives, and the ability for all of us to live in a less polluted and a more energy

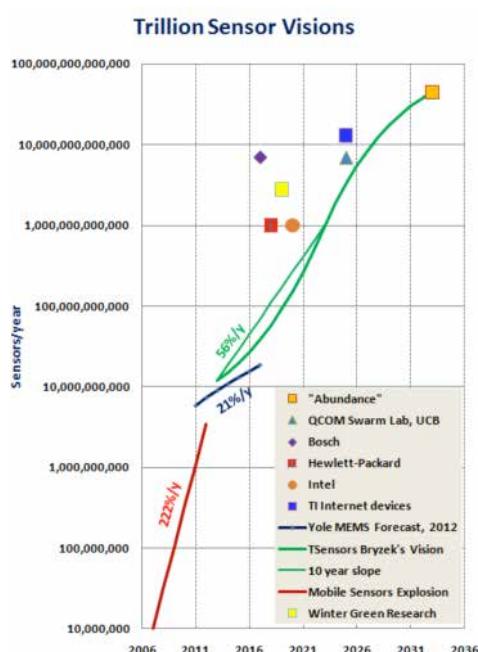
efficient world—and have more fun than ever. Because of the sheer size of the forthcoming changes driven by global tides, the first MEMS billionaires may emerge. 

### References

1. <http://harborresearch.com/smartsystems/>
2. [www.abundancethebook.com](http://www.abundancethebook.com)
3. H. Muenzel, "MEMS from automotive to consumer electronics," MEMS Technology Summit, Stanford U., Oct. 2010.
4. A. Amerasekera, "Ultra-low power electronics in the next decade," 2012 MIG Congress, Oct. 2012.
5. <http://www.technologyreview.com/view/509546/2013-the-year-of-the-internet-of-things/>
6. McKinsey, [http://www.mckinseyquarterly.com/The\\_Internet\\_of\\_Things\\_2538](http://www.mckinseyquarterly.com/The_Internet_of_Things_2538)
7. <http://www.chasmgroup.com/>
8. [http://www.libelium.com/top\\_50\\_iot\\_sensor\\_applications\\_ranking](http://www.libelium.com/top_50_iot_sensor_applications_ranking)
9. <http://beechamresearch.com/article.aspx?id=4>
10. <http://technode.com/2012/05/14/internet-of-things-not-just-a-concept-for-fund-raising/>
11. R. Friedrich, "CeNSE: awareness through a trillion MEMS sensors, the decade of sensing and sense-making, MEPTEC, May 2012.
12. S. Bhide, "Emerging usages & apps for sensors in 2016+," MEMS Business Forum, May 2012.
13. <http://www.qualcommtricorderxprize.org/>
14. <http://www.nokiasensingxchallenge.org/>
15. <http://www.TSensorsSummit.org>

### Biography

Janusz Bryzek received his MSEE and PhD from Warsaw Technical U., Poland, and completed the executive management program at Stanford U. He is VP Development, MEMS and Sensing Solutions at Fairchild Semiconductor; email [janusz.bryzek@fairchildsemi.com](mailto:janusz.bryzek@fairchildsemi.com)



**Figure 1:** The mobile sensor market for volumes not yet envisioned by leading market research organizations in 2007 grew exponentially over 200%/yr between 2007 and 2012.



## Test sockets for the parallel world

by Tom Di Stefano *[Centipede Systems]*

The relentless march of technology toward higher complexity at ever lower cost is felt in the test sector as a move toward parallel test. Memory was the first to go massively parallel starting with X32 wafer probes a decade ago, and progressing rapidly through X64, X128, full wafer, and finally, one touch wafer probes. Parallel testing reached into other sectors of high value ICs where circuit complexity and embedded memory drive up test time, while the market demands lower cost. Massively parallel testing offers a way forward for high-volume devices. The movement toward parallel testing of ICs will impact test sockets, just as massively parallel DRAM testing drove wafer probe technology.

The socket format follows the array configuration as determined by the capabilities of the handler, automatic test equipment (ATE) and contactor. At times, one of the three is the limiting factor in parallelism. Handlers, with their increasing cost and complexity, have been a pacing factor. Now, emerging formats including strip testing and test-in-tray, provide means for handling large arrays of devices, providing virtually unlimited parallelism. Strip test can dramatically increase throughput, in some cases by as much as a factor of three [1]. However, strip test is generally limited to certain package formats only. Emerging technology for test-in-tray and InCarrier test overcomes limitations of strip test while allowing rapid handling of large arrays of devices. ATE capacity is becoming the factor pacing parallelism of test.

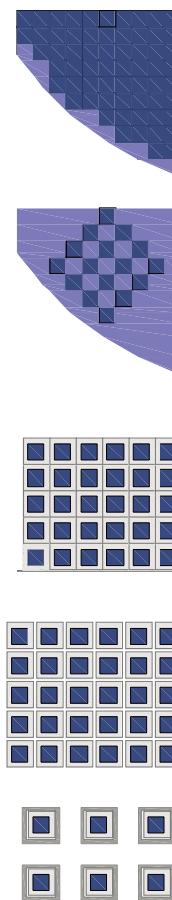
Test electronics is evolving to enable more parallel test in certain applications.

Card-based ATE enables expansion of tester resources to support increased parallelism. In applications where test time is dominated by embedded memory, built-in self test (BIST) and/or test during burn-in (TDBI) facilitate massively parallel testing. TDBI at temperature allows for more efficient screening for latent defects.

As with wafer probe for memory chips a decade ago, contactors for massively parallel test are becoming more important today. The density of devices under test becomes a factor in selecting a contactor strategy. At one extreme, a one-touch wafer probe offers the highest density, with every die tested as illustrated in **Figure 1a**. The one-touch solution comes at a cost due to complexity of the test interconnect, typically going through two levels of escape routing from the densely packed dice. The interconnect bottleneck can be relieved by testing alternate die sites on a staggered pattern as illustrated in **Figure 1b**, in order to reduce cost and complexity of the probe card. The cost of the contactor for parallel test can be further reduced by spacing dice further apart on a regular array, as with eWLP formats.

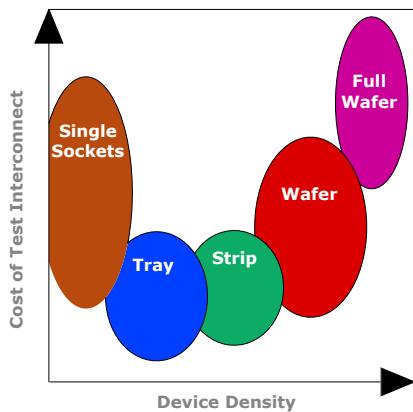
Complexity of escape wiring and associated interconnect is largely

determined by device I/O and spacing between adjacent dice. This complexity is reflected in the total cost of the contactor as illustrated in the cost-density map of **Figure 2**. Although actual costs depend greatly on specifics of the contactor density and performance requirements, the cost of highly parallel contactors generally shows a minimum at moderately spaced sites, with costs rising with increasing density to an ultimate at one-touch full-wafer DRAM probes. At the lower density of individual sockets for highly parallel test, then at low densities the total cost begins to rise because of the physical size of the structure. For any given device and test regimen, there is an optimum device spacing for a minimum of total cost and complexity. As an example, the cost of massively parallel die contactor assemblies could be reduced by increasing the die-to-die spacing by embedded wafer-level packaging (eWLP) or test-in-tray techniques.



**Figure 1:** a) One-touch wafer probe; b) Staggered wafer probe; c) Strip test; d) Test-in-tray; and e) Discrete sockets.

Strip test features a high packing density of devices, allowing for fast index times and high parallelism in a small space. For suitable package types, strip test offers greatly enhanced test efficiency where applicable. Contactor requirements for strip test are somewhat more relaxed than wafer probes because



**Figure 2:** Cost of test interconnect vs. device density for highly parallel testing.

of the added spacing between dice. However, retest in a strip environment is more complex, and highly reliable contactors are at a premium. And for closely spaced contact pads, thermal expansion and dimensional stability limit the size of the strip and test parallelism. Alignment issues can be ameliorated by matching the coefficient of thermal expansion (CTE) of the contactor to the strip. Because the contactor is closely tied to changes and variations in materials and processes, strip test is best suited to manufacturing operations with integrated packaging and test.

Test-in-tray provides the advantages of strip test while overcoming certain of its limitations. Test-in-tray supports all package types from BGA to WLP and flip-chip, while allowing flexibility to determine device spacing independently. Spacing can be set to facilitate board escape wiring as well as contactor design to allow efficient test fixtures. Dimensional stability and CTE control of the tray permit contacting device arrays of virtually unlimited size. The tray and mating contactor are designed as an ensemble to obtain good registration for the test conditions. In a sense, the tray is a part of the contactor assembly. Alignment of device to contactor is achieved in a rapid sequence of first aligning the tray to the array of contactors in x-y-z space. Then, each device is brought into alignment with

a mating contactor. The tray has the flexibility to use the same format for test, re-test, and test of returns, all with the same test configuration.

Overall, device spacing on mating contactors is an important factor for massively parallel test. A compact array simplifies the mechanical design. Thermomechanical stability is easier to control and the job of establishing thermal conditions is simplified. Test efficiency improves with density as index time is reduced. On the other hand, too small a spacing complicates the contactor structure and cramps escape wiring on the board. With increasing parallelism of test, new approaches are needed for large contactor arrays that go beyond the capabilities of individual discrete sockets.

### Contactor configurations

First to go massively parallel, full wafer memory testing is well established. The next challenge, 450mm wafer probes with increased mechanical and thermal stability issues, still lies in the future. Individually registered and leveled tiles may be the answer, or perhaps a new technology is needed.

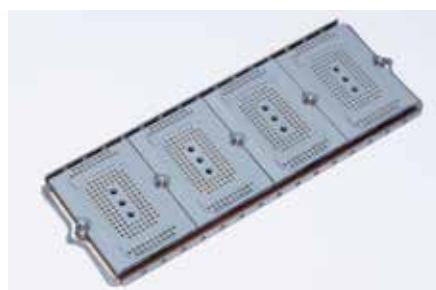
The ongoing drive toward parallel test requires new approaches to sockets and contactors for singulated devices. Highly parallel testing places more stringent requirements on the contactor assembly. A contactor may incorporate thousands to tens of thousands of contacts, each of which must work reliably. Mean time between failure of the assembly scales inversely with the number of devices under test. The cost of ATE down time, equipment utilization, and device retest can become significant compared to the cost of the contactor itself. This means that first, the contact and socketing must be reliable. Second, defective contactors must be easily replaceable in a short time to minimize machine down time. And third, partitioning of the contactor assembly should allow replacement of a defective element without replacing the entire assembly.

The assembly shown in the cover

photo [2] contacts 40 devices in parallel, where the array of devices is held in registration by a tray. A 4mm spacing between devices allows space for sockets as well as for easy escape routing on the board. The 40 sites are arranged in ten columns of four devices each, where each contactor column is a replaceable cartridge. The contactor cartridge in **Figure 3** includes four independently operating alignment sockets for 145 ball BGA devices. The cartridge is retained by spring clips that hold the cartridge accurately in position and maintain that accuracy across a range of test temperatures. The CTE of the cartridge is matched to that of the assembly fixture to maintain dimensional stability across temperature transitions from -55C to +150C. Air channels through each socket facilitate air flow for thermal management.

Cartridges are easily replaceable with an insertion/extraction tool that compresses the retaining springs and brings the cartridge into position in the assembly. A cartridge containing a defective socket can be removed and replaced in less than one minute, minimizing down time. The small thermal chamber enclosing the compact 40-device array is quickly accessed to allow for the fast change over. Cartridges are cleaned and repaired off line.

The specific configuration of contactors for massively parallel test depends upon test conditions, device size, pin count, and ATE resources. Close spacing of devices in the array conserves board space and simplifies interconnect to the ATE. For thermal testing of large arrays, a compact assembly with minimum spacing



**Figure 3:** Contactor cartridge for X4 devices.

between devices greatly simplifies temperature control and minimizes thermomechanical problems because of thermal transients. A compact thermal chamber that can be accessed quickly helps reduce repair and maintenance down time.

Under certain applications, such as sensitive RF devices, an increased spacing is needed for high performance. Individual sockets, such as the 84-pin cartridge shown in **Figure 4**, allow space for shielding and sensitive routing. The single site cartridge is held in position by miniature spring clips, one on each end of the cartridge. Again, the cartridge is quickly replaceable by use of an



**Figure 4:** Single device contactor cartridge for 84-pin RF device.

insertion tool, for either wafer probe or final test on a load board. Contactor probes in the cartridge are self-cleaning to increase the mean time between failure (MTBF).

Monolithic contactor arrays, however complex and expensive, are merited in certain parallel test applications where functional integration is necessary. An example, illustrated in **Figure 5** is an integrated socket for testing 32 MEMS pressure sensors in parallel. The socket includes 64 independently switched



**Figure 5:** Monolithic contactor array for testing X32 MEMS pressure sensors with 64 pressure ports.

gas channels for supplying differential pressure to each of the devices under test. The figure shows the assembly with electrical and pressure contacts under a mating mini-chamber for thermal testing. A monolithic configuration is used to integrate the complex network of pressure channels with electrical contractors in a pressure sealed module. In such cases, a monolithic approach actually simplifies integration. However, where possible, a partitioned configuration is preferable.

### Summary

Parallel testing of high-volume ICs places increasing demands on test contactors. The contactors must be low maintenance, and preferably self-cleaning, to minimize down time. Change-over time for replacing sockets must be fast because of the large number of contact probes. Dimensional integrity of large arrays is an increasing problem

because of high compression forces and thermal transients. And of course – cost. ☺

### Acknowledgment

InCarrier is a registered trademark of Multitest.

### References

1. Chuck Schleigh as quoted in Microconnections V.3, No.2, p.2 (2009).
2. Assemblies of contactor cartridges as illustrated on the cover are used for testing trays of 40 devices in parallel at multiple temperatures.

### Biography

Tom Di Stefano received his BSEE from Lehigh U. and PhD in applied physics from Stanford U. He is President and founder of Centipede Systems; email tom@centipedesystems.com

*Your Best Testing Partner*

KYEC

Address: 101 Metro Dr.#540 San Jose, CA 95110  
Tel: 1-408-452-7680  
Fax: 1-408-452-7689

**Huge test capacities**

- HQ in Taiwan & Worldwide Offices, covering USA, Japan, Europe, China and Singapore
- Over 2000 sets of test systems and growing
- Powerful test capabilities and efficient production logistics

**Wide range of test capabilities**

- Professional testing services, covering Wafer probe, Final test, Pre-Assembly, Burn-in, Backend
- Complete testing Solutions and equipment, such as Memory, Logic, SOC, RF, CIS, MEMS
- Customized test accessories service
- Strong R&D team and advance test technology

KYEC is a leading provider of testing services and solutions to the IC industry

[www.kyec.com](http://www.kyec.com)

# INDUSTRY NEWS

## ADATA Technology To Provide Invensas xFD Memory Modules to Server and Data Center Customers

Invensas Corporation reports that DRAM module and USB flash vendor, ADATA Technology, will design, manufacture, and sell xFD™ based memory modules into the server and data center markets.

xFD is an advanced, high-performance memory interconnect technology that offers comprehensive features for module- and system-level design. It leverages existing wire-bond package assembly infrastructure with an efficient face-down die stacking configuration. In addition to size reduction, xFD is said to offer significantly improved electrical and thermal performance, while reducing component and system hardware cost.

"Invensas has been working with leading server OEMs as well as Internet and social media companies to validate our xFD based memory solutions," said Simon McElrea, president of Invensas. "We are delighted that their positive feedback has allowed us to partner with ADATA Technology to deliver, and work in partnership with our licensees to deliver, xFD based solutions into the server and data center markets."

"xFD technology is an ideal platform to design and manufacture cost effective memory modules while improving performance, signal integrity, and thermal dissipation for our strategically important server and data center markets. We are excited to include this new innovative technology into our memory module product line," said Ted Tsai, Sr. Manager, DRAM at ADATA.

## Yole Développement Reports: Combo Sensors Expected to Triple in 2013

Many saw 2012 as a turnkey year for consumer combo sensors, with high-volume adoption in platforms such as Samsung Galaxy S smartphones. Since then, numerous developments have occurred, and the market acceptance of combo solutions has been extremely

quick, not only for 6-axis IMU but also for 6-axis e-compass. In addition, 9-axis solutions are being introduced to the market and innovative solutions should follow with integration of pressure sensing, processing units, and RF capabilities.

The combo sensor market is estimated to be \$446M in 2013, growing to \$1.97B in 2018. This represents 21% of the global inertial consumer market in 2013, and will grow to an impressive 66% by 2018. "While smartphones and tablets are now driving volume increases and adoption of combos, the picture should be different in 2018," noted Laurent Robin, Activity Leader, Inertial MEMS Devices & Technologies at Yole Développement. "The next market wave should come from wearable electronics, where long-term market potential is huge.

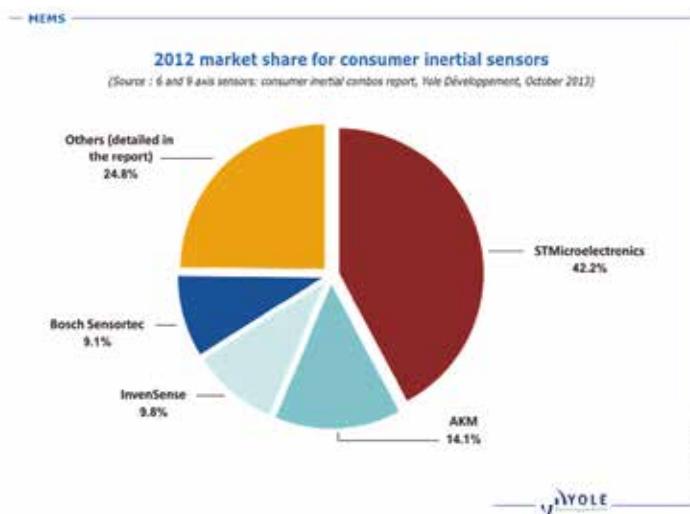
While combo sensors will take a significant portion of total market share, opportunities will remain for discrete sensors: from accelerometers used in basic activity trackers to gyroscopes for camera module stabilization."

The road was not so easy for inertial combos and some challenges still need to be solved. Outside of the offering, which is still smaller than with discrete sensors, combo sensors are sometimes said to be inaccurate or create constraints for board placement. In the past, footprint reduction was the only argument in favor of combos. However significant achievements have been made in the past couple of months. Most of the past yield issues have been solved, leading to lower price. In addition, combo solutions facilitate both qualification and testing at

the integrator level, and development of sensor fusion.

STMicroelectronics is the global leader in the inertial consumer sensor market with 42% market share. Only InvenSense and Bosch Sensortec are able to compete with it today. It is key to be able to control the different technologies or to establish the right partnerships to sell a large range of combo solutions. ST is just beginning to sell its own magnetometer in 2013, while Bosch has been very active in launching new product lines since 2012. InvenSense has just partnered with Melexis as an alternative source to AKM for the magnetometer die in 9-axis solutions, although this is not official information.

Prices are sharply dropping, with IMUs sold to some large volume customers below \$1.00 in 2013. To stay



in the race, the three leaders are going to introduce technical innovations: monolithic integration of 6 to 9-axis, use of TSV, chip scale packaging, and active capping.

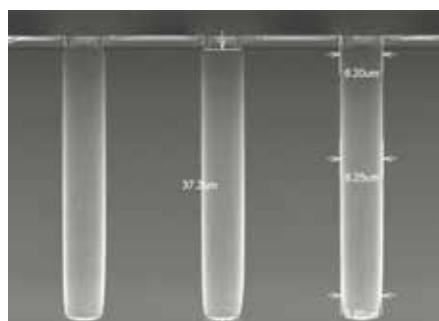
Current challengers and newcomers are eyeing this combo opportunity and expect to take market share while the supply chain is not yet mature. Kionix, Freescale, Alps Electric, Fairchild, Maxim and more than 10 other companies are all targeting this market space. New business models are built and

more fabless companies are likely to be involved in the combo market.

Value is moving to function delivery with embedded sensor fusion. Sensor fusion developments must be taken seriously. There has been hype about it for many years and now we are seeing commercial implementation. The first real products with sensor fusion are already on the market, such as sensor hubs in the latest smartphones and tablets from Samsung and more recently by Apple, with the M7 processor in iPhone 5S. In addition, GPS chipsets with indoor navigation capability relying on MEMS sensors are now available from CSR, Qualcomm and Broadcom.

### Imec and SPTS Partner on Advanced Nanotechnology Applications in BioMEMS

SPTS Technologies, a supplier of advanced wafer processing solutions, and imec, a European nanoelectronics research center, have announced a joint partnership to further advance micro- and nano-sized components for BioMEMS, using SPTS' Rapier silicon deep reactive ion etching (Si DRIE) technology.



Micro and nanotechnologies are fast becoming key enablers in medical research, diagnosis and treatment, with rapid developments in areas like DNA sequencing and molecular diagnostics. Imec, as one of the pioneers in the field, is developing the underlying heterogeneous technology and components as the backbone to these life science tools.

One of the most important process techniques in BioMEMS manufacturing

is deep silicon etching. It can be used to manufacture devices such as microfluidic channels, polymerase chain reaction (PCR) chambers, mixers and filters. Imec is currently developing lab-on-chip technology for fast SNP (single nucleotide

polymorphisms) detection in human DNA and a micro-sized detection system for circulating tumor cells in the human blood stream. The outcome of this research will be products that deliver a better quality of life for current and future generations.



www.EVGroup.com

## MID-END LITHOGRAPHY SOLUTIONS ARE READY!

- Advanced Resist Processing  
Thick Resist and Dielectric Layer Coating  
Conformal TSV Coating and Polymer Via-Filling
- Vertical Thick-Resist Patterning  
Large Depth-of-Focus Imaging for 3D Applications  
High Exposure Dose Processing
- Ultra-Thin, Warped and Carrier-Mounted Wafer Handling



GET IN TOUCH to discuss your manufacturing needs  
[www.EVGroup.com](http://www.EVGroup.com)

"We chose SPTS as a partner after running extensive wafer demonstrations on their tool, challenging them on the demanding structures required by our current projects," says Deniz Sabuncuoglu Tezcan, leader of imec's Novel Components Integration team. "The results convinced us that the Rapier module could help us create the devices we envision. The demos show that the processes will deliver the high throughputs and repeatability necessary for cost-effective volume production."

"We are very pleased to be working with imec, a world-renowned institute with a global reputation for developing cutting-edge technology", said Kevin Crofton, Executive VP and COO of SPTS. "BioMEMS is one of the new frontiers of the MEMS industry and will deliver huge benefits to our health and wellbeing. We're proud that our technology will be used to develop life-changing devices that will benefit this and future generations."

### Delft University of Technology and imec Introduce 3D-COSTAR to Optimize Test Flows of 3D Stacked Integrated Circuits

Delft University of Technology (TU Delft) and nanoelectronics research center, imec, introduced 3D-COSTAR, a new test flow cost modeling tool for 2.5/3D stacked integrated circuits (ICs). 3D-COSTAR aims to optimize the test flow of 3D stacked ICs (SICs), taking into account the yields and costs of design, manufacturing, packaging, test, and logistics.

Due to many high-precision steps, semiconductor manufacturing is defect-prone. Consequently, every IC needs to undergo electrical tests to weed out defective parts and guarantee outgoing product quality to the customer. For TSV-based 2.5D- and 3D-SICs that typically contain complex die designs in advanced technology nodes, testing is even more critical. In addition, there are many possible test moments in the

manufacturing flow: pre-bond (before stacking), mid-bond (on a partial stack), post-bond (on a completed stack), and final testing (on a packaged device). Although testing is expensive, filtering out the bad components in an early stage is critical to save costs later on in the production process.

"There is not a 'one-size-fits-all' test flow that covers all stacked-die products. The test flow needs to be optimized based on yield and cost parameters of an individual product and that is a complex optimization problem," stated Dr. Said Hamdioui, Associate Professor at TU Delft. "And different test flows, executed after manufacturing, may require different design-for-test features, which need to be incorporated in the various dies during their early design stages."

3D-COSTAR uses input parameters that cover the entire 2.5D-/3D-SIC production flow: 1) design; 2) manufacturing; 3) test; 4) packaging; and 5) logistics. It is aware of the stack build-up (2.5D versus 3D, multiple towers; face-to-face or face-to-back) and stacking process (die-to-die, die-to-wafer, or wafer-to-wafer). The tool produces three key analysis parameters: 1) product quality, expressed as defect level (test escape rate) in DPPM (defective parts per million); 2) overall stack cost; and 3) breakdown per cost type.

"3D-COSTAR has proven to be a crucial tool to analyze the many complex trade-offs in 3D test flows, in terms of both cost and DPPM," said Erik Jan Marinissen, Principal Scientist at imec. "Among others, we have used 3D-COSTAR to determine when pre-bond testing of the interposer in 2.5D-SICs pays off and what its maximum-allowed test cost can be. In some cases, the overall stack cost reduction amounts to 40%, showcasing that upstream testing can help avoid downstream costs. The tool also demonstrated under which circumstances mid-bond testing (on partially-completed stacks) can be avoided without compromising a high stack yield."

"Together with imec, Cascade

Microtech has recently demonstrated the feasibility of direct probing large-array fine-pitch micro-bumps to avoid the usage of dedicated pre-bond pads," stated Ken Smith, principal engineer, Cascade Microtech, Inc. "Analysis with 3D-COSTAR clearly showed up to 50% overall cost benefit of doing microbump probing using an advanced probe cell such as was demonstrated with Pyramid Probe® RBI technology on our CM300 probe station."

### Global Semiconductor Sales Increase for Sixth Straight Month in August

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing and design, announced that worldwide sales of semiconductors reached \$25.87B for the month of August 2013, an increase of 6.4% compared to August 2012, marking the industry's largest year-over-year growth since March 2011. Sales in the Americas increased by 23.3% compared to August 2012, while global sales in August were 1.3% higher than the previous month's total of \$25.53B. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"Global semiconductor sales have now increased for six consecutive months, and the industry is well ahead of last year's pace, thanks largely to sustained growth in the Americas," said Brian Toohey, president and CEO, Semiconductor Industry Association. "Strong demand for memory products has driven sales in recent months, but sales were also up in August among non-memory products, demonstrating the breadth of the semiconductor market's strength."

Regionally, August sales topped sales from the same month last year in the Americas (23.3%), Asia Pacific (7.6%), and Europe (5%), but decreased in Japan (-16.4%), in large part because of the devaluation of the Japanese yen. Sales

in August were up across all regions compared to the previous month.

"Semiconductor sales have demonstrated increasing momentum in recent months, thanks in part to stabilizing macroeconomic conditions, but this week's government shutdown and a looming debate over the nation's debt limit threaten to destabilize the economy and disrupt growth," said Toohey. "Congress and the Administration should work together to avoid these self-inflicted wounds and get America's fiscal house in order."

### **Integra Technologies Announces the Purchase of Analytical Solutions, Inc.**

Integra Technologies, provider of integrated circuit test and related services, announced it has acquired Analytical Solutions Incorporated (ASI). Analytical Solutions provides product evaluation services through Destructive Physical Analysis, Construction Analysis, Failure Analysis, Non-Destructive Testing and Counterfeit Device Investigation of semiconductor devices. These services will reportedly complement the electrical test and related services already provided by Integra, and provide a single point of contact for a broad array of semiconductor test and evaluation services supporting the Military, Avionics, Space, Medical, Automotive and Fabless Semiconductor markets. The Trusted Security Analysis portion of the ASI business portfolio, which features the Pix2Net Software, is not included in the purchase and will be added to the newly formed company, MicroNet Solutions Inc, service offerings.

"We are very excited about the combination of Integra and Analytical Solutions," said Becky Craft, president of Integra Technologies. "The Analytical Solutions portfolio of services complements Integra's business and provides our mutual customers with one of the largest semiconductor test and analysis service offerings in the industry."

Ms. Craft added further, "Integra has

been an employee owned company since 2008 and we are pleased to welcome our new employee owners from Analytical Solutions."

"Integra and Analytical are both leaders in their market segments," noted Michael

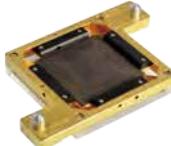
Strizich, former President of Analytical Solutions. "Combining the companies will give our customers an even stronger company to partner with as they continue to innovate with ever-greater levels of semiconductor technology."



# WinWay Technology Co., Ltd.

## The Partner You Can Trust in Testing

while you are engineering the future



**Test Socket** for Engineering and High Volume Production

- \* PoP Socket
- \* Coaxial Socket
- \* CIS Module Socket
- \* Elastomer Socket



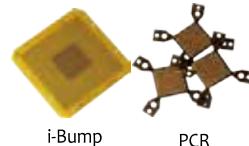
**Probe Card** for ATE Traditional and Direct Dock Wafer Testing

- \* WLCSP Probe Card
- \* Direct Dock Probe Card

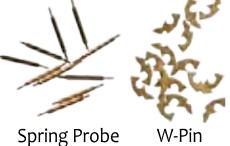


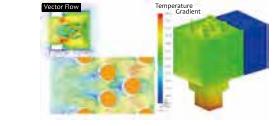
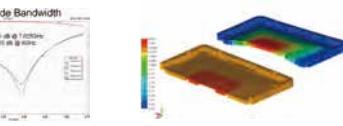
**Active Thermal Controller** for Characterizing Your Product in Low and High Temperature

- \* Manual ATC
- \* Plunger ATC
- \* Seiko Epson Handler ATC Changeover Kit



**Contact Elements** for Satisfying Various Test Requirements





RF Measurement & Simulation      Mechanical Simulation      Thermal Simulation

We Provide Comprehensive Worldwide Support

 <http://www.winwayglobal.com>     [sales@winwayglobal.com](mailto:sales@winwayglobal.com)



# International Wafer-Level Packaging Conference (IW LPC) turns 10!

By Ira Feldman [[Feldman Engineering Corp](#)]

**M**arket adoption is increasing rapidly for wafer-level packaging (WLP) as it is applied to a greater range of applications. The shift of “post-PC” from desktop to mobile devices has driven the development of WLP into the mainstream by providing extremely space efficient and low cost packaging. There has, and will continue to be, many technical and business challenges in packaging devices on wafer (or other substrate) en masse instead of on an individual basis.

Similar to wafer-level packaging technology itself, the 2013 **International Wafer-Level Packaging Conference** (IW LPC) technical presentations covered a large range of applications, challenges, and solutions. This **10th anniversary** event with over six hundred total participants had thirty-nine presentations in three parallel tracks over the two days. In addition to “traditional” applications of WLP for integrated circuits (IC) covered in the “WLP” and “3D” presentation tracks, microelectromechanical systems

(MEMS) WLP applications were highlighted in the “MEMS” track and general sessions this year.

In particular, Marco Aimi (General Electric Global Research Center - GE GRC) provided a high energy plenary on the industrial applications of MEMS. It may be more accurate to say that his was a “high-current” presentation because an application highlighted was metal MEMS cantilever switches for industrial and power grid control handling hundreds of kilo amperes. By solving many of the technical challenges including packaging, not only does MEMS technology enable greater performance, it delivers a competitive advantage.

Rozalia Beica (Yole Développement) kicked off the **MEMS presentation track** with a market overview of MEMS packaging along with what makes it “special”, i.e., higher cost than IC packaging. The application-specific requirements are such that the cost to package and test a MEMS device averages a quarter of the total production cost. As standardization of

MEMS packaging starts, the MEMS rule of thumb (attributed to Jean-Christophe Eloy, Yole Développement) of “1 MEMS Product = 1 MEMS Device = 1 Fabrication Process = 1 Package” requiring extremely high investment cost and development time is starting to weaken.

In “30 Years of Microsystem Packaging: From Automotive to Mobile Electronics and Beyond,” Leland “Chip” Spangler (Aspen Microsystems) traced the development of the MEMS industry from the pressure sensors developed in response to the United States Clean Air Act of 1970 to the present. As each device is truly a microsystem, he highlighted the very specialized packaging requirements of each end application.

Other speakers in the MEMS track also highlighted their application-specific WLP packaging challenges. Noureddine Hawat (MEMSIC) described the challenges of packaging a thermal (instead of capacitive) sensing MEMS accelerometer that requires tight control of a thermal gas for proper operation. Mike Shillinger (Innovative Micro Technology) described the processing challenges of bonding and dicing MEMS systems with three to five different types of wafers stacked to produce the final device. Not



Ron Molnar visits with Barrie Van Devender of Axus Technology



Exhibitor Plasma-Therm

only is process order important, selecting processes to accommodate the different material types is crucial because not all the wafers used are silicon.

Interest in **3D IC packaging** has increased significantly from last year with a total of nineteen papers, resulting in two parallel tracks of 3D papers on day two of the conference, in addition to a single track on day one. For those focused on 3D packaging, it made it even more challenging to decide which one of two excellent presentations to attend. Through the diligence of the moderators, everything was kept on time and switching sessions was easy between the three tracks throughout the conference. The only challenge besides not being able to attend all presentations was finding a seat in the overflowing technical sessions.

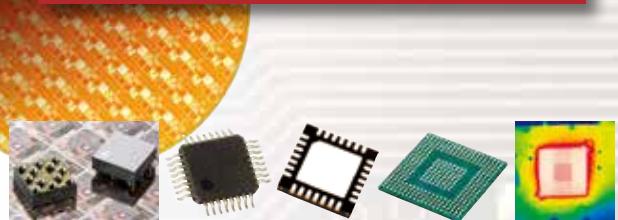
In the **3D plenary**, “A Consumer Driven Market – This Changes Everything,” Simon McElrea (Invensas Corporation) highlighted how technology – electronics and computing in particular – have significantly changed from being government and industry driven, to being consumer driven. Once a market changes to being consumer driven, the volumes skyrocket, while the price per unit plummets. The technology then becomes pervasive and changes not only our expectations, but our behaviors, which further increases consumer demand.

Satisfying the rapid growth of consumer demand will continue to require significant changes in the electronics industry in every area from intellectual

property, to supply chain structure, to energy efficiency. For example, smartphones drove the market adoption of WLP because of the extreme premium on space within the phone. To achieve optimal results with WLP requires even closer cooperation between and across the entire range of design, wafer fabrication, packaging, and test activities. Contrast this situation with the past when each area may have only interacted with its adjacent areas in a limited fashion.

Today, everything from through-silicon vias (TSV) to connectors is considered “packaging.” But Mr. McElrea prefers to use “Interconnectology” (coined by Scott Jewler) since “packaging” sounds like cardboard boxes

**Johnstech®**



# Wafer & Package Final Test



- **High Performance, Low Force Probe Array & Test Contactors**
- **Characterization, Production Floor, and Test Cell Integration Services**

**Johnstech®**

[www.johnstech.com/connected](http://www.johnstech.com/connected)

**Find out more and win an iPad**

and shrink-wrap. And Interconnectology is critical to the success of the end product, especially in consumer driven markets where differentiation, including high performance, at low cost is essential.

Several of the **3D Track** presentations covered interposer technologies from



3D Panel Discussion: Sitaram Arkalgud - Invensas Corp as Moderator, Abe Yee Nvidia Corp., Jim Walker of Gartner Technology, Laura Rothman Mauer of Solid State Equipment, & Suresh Ramalingam of Xilinx.

silicon to alternative materials including through-glass vias (TGV) by Sergio Cadona (nMode) and phase change alloys (PCA) by Semyon Savransky (The TRIZ Experts). These topics were also covered by Professor Rao Tummala (Georgia Institute of Technology) in his well-attended tutorial. Test and metrology for 3D were covered including presentations by James Quinn (Multitest) and Rajiv Roy (Rudolph Technologies).

The **3D Panel** of Laura Rothman Mauer (Solid State Equipment), Suresh Ramalingam (Xilinx), Jim Walker (Gartner Technology), and Abe Yee (NVIDIA Corporation) explored how close 3D packaging is to mainstream applications. Sitaram Arkalgud (Invensas Corporation) moderated this lively discussion with varying degrees of "readiness." It is true that Xilinx is



Shekar Krishnaswamy of Applied Materials presents "Overcoming the Productivity Challenges in Wafer-Level Packaging"

shipping production quantities of 2.5D based product. Several issues remain, however, thereby "blocking" technical progress for 3D devices, with thermal issues being the biggest impediment. With 2.5D, there is not likely to be large-scale adoption beyond specialty devices until the cost is significantly lowered. As Mr. Yee said, companies will pay slightly more for increased performance, but they won't pay significantly more unless there is no other choice. So 3D or large quantities of 2.5D will not happen unless a bold company decides to "invest" (read: spend far more than normal, possibly losing money) to push technology ahead, or has no other choice in how to implement a product.

Presentations on automation, test, materials, processes, and new technology comprised the **WLP Track**. Many of the presentations had new solutions or twists on existing technology. For example, William Rogers (DECA Technologies) discussed how DECA was fabricating WLP using continuous flow equipment



## E-tec Interconnect

### Sockets, Contactors & Adapters for Prototype Development & Test

- Compatible with virtually any footprint
- Probe-pin & Elastomer solutions
- Pitch range from 0.30mm to 2.54mm
- Pin counts up to 2000
- Bandwidth to 40GHz

- SMT, thru-hole & solderless options
- Several socket closure styles available
- Custom requirements are welcome
- Competitive pricing
- Expedited delivery

**For further information visit [www.e-tec.com](http://www.e-tec.com)**

or contact us directly for immediate attention  
E-Tec Interconnect Ltd, USA Marketing & Sales  
E-mail: [info-US@E-tec.com](mailto:info-US@E-tec.com), Telephone: +1 408.746.2800

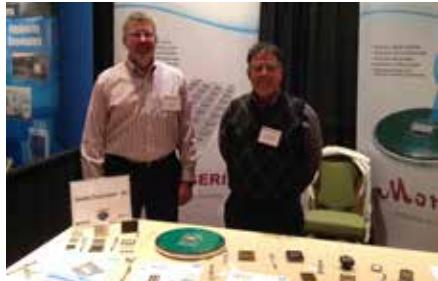




(www.e-tec.com)

Jim Walker of Gartner & Chris Scanlan of Deca Technologies

22 Chip Scale Review • November • December • 2013 [[ChipScaleReview.com](http://ChipScaleReview.com)]



Peter Ursu & Ali Hassanzadeh of Smiths Connectors -IDI

on larger panels based upon processes and equipment developed for solar panels. The continuous flow and larger panel sizes allow them to significantly reduce their costs and to improve the processing with innovations such as adaptive patterning.

In the exhibit hall, the **fifty-five exhibitors demonstrated a large variety of equipment, software, and services related to WLP**. Everything from enabling technology, to process inspection, to test equipment, to consumables, to turnkey services for WLP was represented. If you are a customer needing, or a vendor providing, WLP services, there was certainly something of interest on exhibit. The show floor was busy throughout the conference and a number of exhibitors commented on the increased level of interest.

IWLPC opened with a fascinating history lesson on the **origins of Silicon Valley** by Paul Wesling (IEEE Components, Packaging, and Manufacturing Technology Society CPMT Distinguished Lecturer). Mr. Wesling's keynote described how the ecosystem of companies of the vacuum



Paul Wesling gives the keynote address

tube era collaborated and prospered. This lead to the rise of Silicon Valley from these garages and sheds to that of the familiar Hewlett-Packard and Apple garages and well beyond. **It is clear that the WLP ecosystem benefits from**

**similar collaborations that are enabled by the IWLPC.**

#### Save the Date

November 11-13, 2014 DoubleTree Hotel San Jose, California.

## LEADERS IN MICRO DISPENSING TECHNOLOGY

SMALL REPEATABLE VOLUMES ARE A CHALLENGE, BUT NOT IMPOSSIBLE IF YOU HAVE BEEN CREATING THEM AS LONG AS WE HAVE.



### TO DO IT WELL, WE PROVIDE THREE THINGS:



**Dispensing Expertise** in a variety of microelectronic packaging applications.

**Feasibility Testing & Process Verification** based on years of product engineering, material flow testing and software control.

**Product Development** for patented valves, dispensing cartridges, needles and accessories.

Our Micro Dispensing product line is proven and trusted by manufacturers in semiconductor, electronics assembly, medical device and electro-mechanical assembly the world over.

#### DL Technology

216 River Street, Haverhill, MA 01832

P: 978.374.6451 | F: 978.372.4889

info@dltechnology.com

[dltechnology.com](http://dltechnology.com)



# High-resolution nondestructive 3D imaging

By Bruce Johnson [Carl Zeiss X-ray Microscopy, Inc. (formerly Xradia)]

## I

It's no secret that modern electronics are becoming increasingly complex as end users demand faster, more powerful and portable devices that do more, and do it longer. To meet demand, package complexity continues to spiral upward. For the device manufacturer, this increased complexity has the effect of making it harder and harder to identify the source of failures, and to hone cost-efficient process workflows that improve quality and speed time to market of new package designs.

An integral part of failure analysis and advanced packaging process development is imaging features that are buried within complex 3D structures. More and more often, in order to obtain sufficient information, physical destruction of the sample is required. Sample destruction is generally undesirable so there is a continuing need for effective non-destructive imaging methods. This article will provide an overview of the evolution of 3D XRM as a high-resolution non-destructive imaging method and the increasing role it will play in advanced packaging applications. Two application areas will be highlighted: failure analysis and wafer-level packaging process development.

### Nondestructive high-resolution 3D imaging

To date, physical cross-sectioning remains the most widely used imaging technique in failure analysis and development of semiconductor packages. Cutting into samples and using scanning electron microscope (SEM) and optical micrographs to capture images delivers high resolution and contrast in side-view images and

provides the detail needed to measure critical structures and defects. However, the technique has its drawbacks. Chief among them is the fact that physical cross-sectioning is destructive, meaning the fault dynamics within a particular sample can be studied objectively only once. The process may also introduce debris or damage soft layers and create stress relief that actually obfuscates clues about the root cause of defects. In other cases, defects may be missed completely if the incorrect polishing orientation is chosen. And from an efficiency standpoint, the technique proves relatively time-consuming.

For the reasons stated above, engineers have sought to incorporate nondestructive techniques such as X-ray imaging wherever possible. Two-dimensional (2D) X-ray and conventional 3D micro computed tomography (micro-CT) technologies have been used in the development of ball grid array, thermal compression bonding, and flip-chip technologies. They are capable of delivering sufficient resolution and quality for imaging large voids, rough misalignments, and non-contact opens from top-views of first- and second-level interconnects. However, as more layers with smaller feature sizes are stacked on top of each other in multi-chip packages, interposers, and through-silicon vias, conventional techniques prove inadequate [1].

### Enter 3D XRM

Recently, a more powerful, three-dimensional X-ray variant technique has proven to be a successful alternative to physical cross sections in failure analysis (FA) labs. Known as XRM, or X-ray microscopy, this next-generation

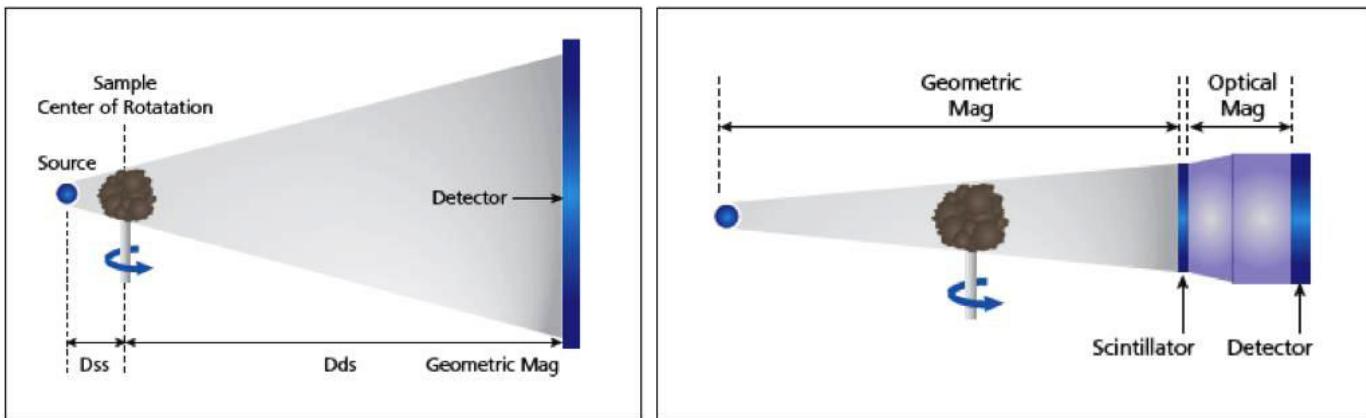
approach shows potential to bridge the gaps in 3D IC production metrology [1,2].

Micro-CT was developed to achieve micrometer voxel (the 3D analog of a 2D pixel) resolution, but trade-offs exist between sample size and achievable spatial resolution. Micro-CT relies on maximizing geometric magnification, with resulting limitations in source-to-object distance that prevent high-resolution imaging of larger samples.

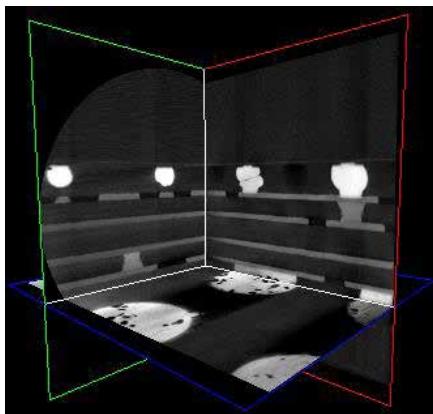
In contrast, and key to this new XRM technology is its dual magnification parameters. Unlike conventional 2D X-ray and micro-CT techniques, which rely solely on geometric magnification, XRM employs geometric and optical image magnification based on scintillator-coupled optics to achieve higher spatial resolution over a larger working distance. Because of this unique architecture, resulting 3D XRM images are comparable in quality to those obtained by SEM, even for larger samples, thus providing a viable nondestructive alternative to physical cross-sectioning for FA and process development workflows (Figure 1).

### Virtual cross-sectioning

Virtual cross-sectioning is now routinely being used by the majority of leading semiconductor manufacturers to augment or improve upon physical cross-sectioning for imaging complex multi-layered 3D IC packages. XRM produces a 3D data set that the user can slice into "virtual cross sections" of any plane—X, Y or Z—running through the volume (Figure 2). By utilizing tomography to generate 3D virtual models of internal structures from 2D X-ray projections, these virtual slices are collected in small intervals over a



**Figure 1:** Comparison of micro-CT architecture a) (left) and XRM architecture b) (right). With dual stage magnification, XRM maintains high resolution across a range of package sizes, even for larger packages.

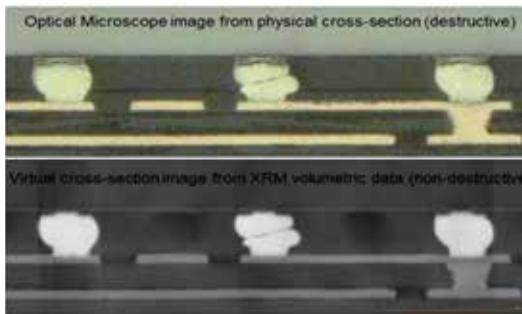


**Figure 2:** Virtual 3D model of internal structure with FOV 0.7mm<sup>3</sup> and spatial resolution of 0.7μm/voxel. Three colored boxes represent orthogonal virtual cross-section planes through the volume. The resulting volumetric data shows non-wet defects as well as large voids in the BGA bumps.

range of angles, typically 180° or 360°. A filtered back projection model is used to reconstruct a virtual 3D image of the sample.

High-resolution volumetric data allows engineers to review an unlimited number of virtual cross sections in any orientation through the volumetric dataset. This reduces the time needed to isolate a defect and determine the cause of package failure.

As an illustration of how the image qualities compare, **Figure 3** shows a virtual cross section image compared to the same location after physical cross-sectioning. By comparison, features of the main non-wet defect are clearly visible in both images.



**Figure 3:** Comparison between images collected with an optical microscope and XRM computed tomography. In addition to the non-wet defect in the center of the image, the red arrow points to a ~2μm void between the Cu pad and solder bump missed by physical cross-section

### Application of XRM in failure analysis

The failure analyst's job is getting tougher. For failure analysis, samples are frequently considered irreplaceable; thus, it is usually more desirable to preserve the sample as long as possible so that the maximum information about the failure can be obtained. While the sophistication of techniques for failure location isolation is increasing, it is getting more difficult to characterize and diagnose failure morphology without resorting to destructive methods. Part of the problem is that insight into failures may be buried deep within advanced, multilayered structures such that exploring them is increasingly difficult to do with traditional nondestructive methods. Techniques such as scanning acoustic microscopy, time domain reflectometry, 2D X-ray imaging and

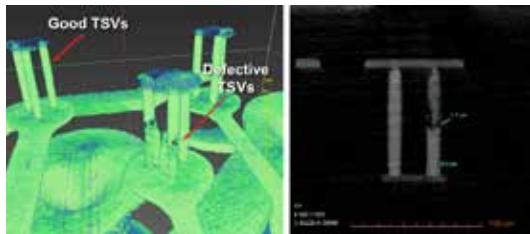
thermal imaging, have proven useful in nondestructively isolating the general vicinity of failure modes, such as bump cracks and voids, but they generally do not provide sufficient information to fully characterize the failure. Hence, the next step following localization is to use some form of destructive physical analysis to attempt to visualize the failure and, hopefully, determine the root cause.

Examples of destructive techniques include parallel de-processing, laser/chemical de-processing, mechanical cross section, de-capsulation or FIB cross-sectioning. In each of these techniques, the part is physically cut open to reveal the location of the failure. If the failure is located and the cause is still unknown, further testing, such as elemental analysis, can be performed. However, if the failure is not located, the conclusion will most likely be "no defect found" since the action of cross-section or de-capsulation has destroyed the sample. Following fault localization, XRM offers a viable high-resolution non-destructive alternative for characterizing the failure, either instead of, or to complement physically destructive methods.

**Figure 4** is an example of XRM used to image the location of an electrically open failure. On the left is the 3D rendering of the failure. One benefit of working with a 3D dataset is that it may be "segmented" by material

density. In this example, only the copper is revealed, making it easy to see the morphology of the failure. On the right is a virtual cross section taken at the failure location from the same dataset. In many cases, these images may be enough to diagnose the cause of the failure. However, in those cases where diagnosis requires more information, additional testing may be performed on the chip because the sample has not been destroyed. If destructive analysis is still required, the XRM 3D dataset may also be used to guide the best way to perform that physical analysis.

Another notable example of where XRM has proven useful in failure analysis is for imaging failures in circuit



**Figure 4:** Images of a TSV failure taken by XRM on a 4mm x 4mm intact package without destroying it. a) (left) XRM 3D rendering of electrically open TSV fault. TSVs are 10µm in diameter; and b) (right) virtual cross section taken from 3D rendered image at the failure location.

boards (**Figure 5**). In this example, it was believed that there was a crack in a copper trace where the ball grid array (BGA) attaches. Because of its ability to maintain resolution over large working distances (**Figure 1**), XRM renders it possible to image a 2µm trace crack in a 4" by 8" circuit board without destroying it. Similar to the case presented in **Figure 4**, if destructive physical analysis is still required then the XRM dataset may be used as a guide for how to best accomplish it.

Throughput of acquiring XRM data sets will depend upon physical properties (materials, feature sizes, and outer dimensions) and the necessary image quality required to visualize a defect. For the circuit board presented in **Figure 5**, images that clearly reveal the crack were obtained in as little as 1.75 hours as shown in **Figure 6**. However, recent advances in XRM enable high-

quality cross-section images to be obtained in as little as 30 minutes per measurement.

### Application of XRM in WLP process development

#### Wafer-level packaging

(WLP) is an advanced packaging technology in which the die interconnects are manufactured and tested on the wafer, then singulated by dicing for assembly in a surface mount line. WLP effectively extends front end wafer processing into a realm that was previously accomplished post-singulation. The motivation for this is to enable a higher density of interconnects in smaller packages by using similar processing techniques to those that are used in front end processing. The goal is to increase the bandwidth or data handling capacity and speed of communications between system components, for example

I/O between processor and memory, while at the same time using less power and fitting into smaller and smaller end products, such as mobile devices.

Here is where TSV technology comes into play. In TSVs, vertical interconnects are running through the dies. When TSV-enabled die are stacked on top of each other and interconnected with bumps, they form 3D integrated chips. This technology can be used for stacked DRAM, stacked NAND, or a processor-DRAM stack in mobile applications. TSVs have replaced peripheral wires that are millimeters in length with vertical

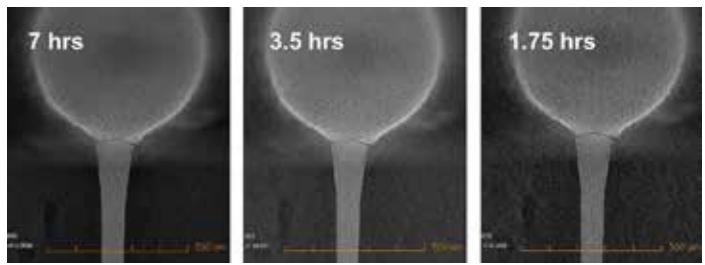


**Figure 5:** Virtual cross sections of a crack in a copper trace taken by XRM on a 4in by 8in circuit board without destroying it. In spite of the board's size, the XRM is still able to clearly image the 2µm crack.

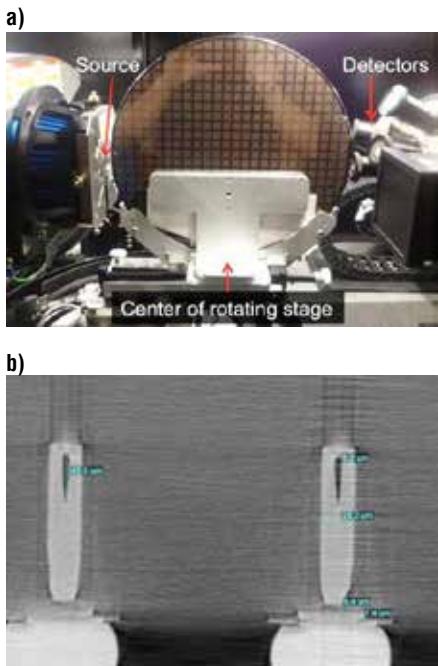
connections that are just microns in length. They contain thousands, not hundreds, of inter-chip connections, enhancing their bandwidth. Connections are now microns long and are situated over the entire area of the chip to enable faster data exchange and lower operating power.

As the resulting structures get smaller and more "3D," there remains a need to image subsurface structural details: defect locations for failure analysis and structural integrity for process development. As described above, for advanced 3D IC packages it is becoming more challenging to image important details of subsurface structures by traditional techniques without physically cutting the wafer. This is where, with the latest advances in XRM, high-resolution 3D data sets can provide a solution.

Similar to the circuit board example presented in **Figure 5**, the unique XRM architecture enables high-resolution 3D datasets to be acquired, even for large samples such as 300mm wafers. Wafers are manually loaded onto the XRM rotating stage using a specially designed wafer holder (**Figure 7**). Tomographies of any location on an intact 300mm



**Figure 6:** Examples of the virtual cross section image quality from **Figure 5** as a function of 3D dataset acquisition time. For cases where throughput is the highest priority, lower signal to noise but adequate images may be obtained in much shorter time frames.



**Figure 7:** XRM use for WLP: a) wafer sample holder mounted on the rotating stage within the XRM; b) representative virtual cross section from tomography taken on wafer. The XRM can image intact 300mm and 200mm wafers with ~1µm voxel size anywhere on wafer.

destructive SEM imaging techniques and low-resolution, non-destructive micro-CT capabilities while improving time to results, for which X-ray is not traditionally known. Capable of achieving high spatial resolutions in intact packages and circuit boards, XRM is now routinely being used by the majority of leading semiconductor manufacturers to augment or improve upon physical cross-sectioning for failure analysis and advanced packaging process development. Because of XRM's architecture, it is possible to acquire high-resolution 3D datasets for complex multi-layered 3D IC WLP packages prior to singulation in significantly reduced time frames.

As the reach and impact of XRM technology grows within FA labs, studies correlating XRM with SEM and optical images will underscore the value of nondestructive techniques as a workhorse for advanced packaging failure analysis and development facilities. 

[http://www.zeiss.com/xrm\\_electronics](http://www.zeiss.com/xrm_electronics)

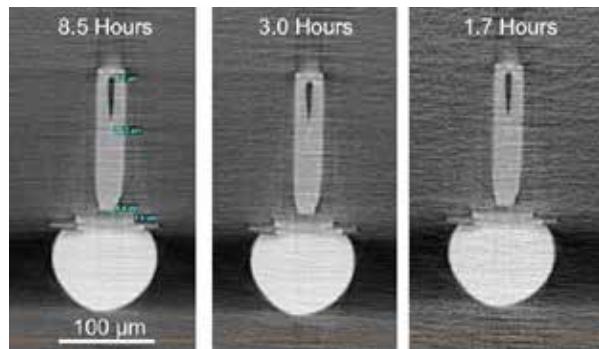
## References

1. K. Fahey, R. Estrada, L. Mirkarimi, R. Katkar, D. Buckminster, M. Huynh, "Applications of 3D X-ray microscopy for advanced package development," IMAPS 2011, 44th Inter. Symp. on Microelectronics, Oct. 9-13, 2011.
2. A. Merkle, J. Gelb, "The ascent of 3D X-ray microscopy in the laboratory," Microscopy Today 21(2) 2013, pp. 10–15.

wafer may be acquired with 1µm voxel resolution to observe and quantify TSV morphology and characterize processing quality on wafers prior to chip singulation (**Figure 7b**). The user has the flexibility to optimize required image quality and data acquisition time (**Figure 8**) similar to the circuit board example presented in **Figure 6**.

## Summary

The latest advances in X-ray microscopes bridge the gap between high-resolution,



**Figure 8:** Tradeoff of signal-to-noise ratio vs. image acquisition time. Virtual cross sections from the same point on a wafer at varying tomography acquisition times.

## Biography

Bruce Johnson received his Bachelor's degree in Physics from the U. of California at Berkeley, his Master's degree in Applied Physics from Rice U., and of Electrical and Computer Engineering from the Georgia Institute of Technology, and a Diplôme de Spécialisation in Signal Processing and Information Theory from the Ecole Supérieure d'Electricité in Metz, France. He is a Manager of Semiconductor Product Marketing at Carl Zeiss X-ray Microscopy, Inc. (formerly Xradia); email bruce.johnson@zeiss.com

# Venus Series

## New Line of Low-Cost Plasma Cleaners

Plasma Etch, Inc. is proud to introduce the Venus series to our line of low cost plasma cleaners. The Venus comes standard with computer control and mass flow controllers for added precision.



**Venus Features:**

- Computer Control
- Process Data Acquisition
- Process Data Archiving
- Dual Sequence Programming
- Hardcopy Process Data Recording
- On-Screen Process Trend Plotting



Visit [www.PlasmaEtch.com](http://www.PlasmaEtch.com)  
or call today at 775-883-1336

# 3D IPAC: a new concept in integrated passive and active components

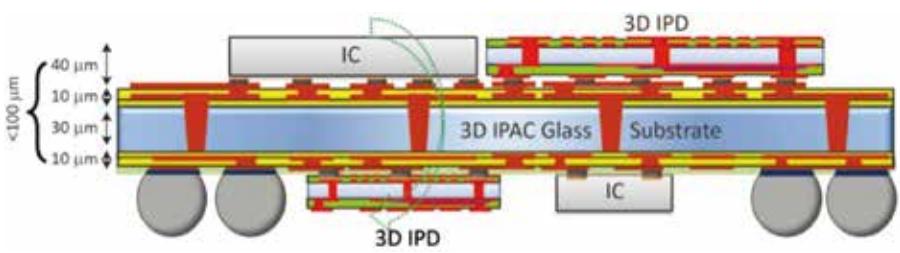
By P. Markondeya Raj, Saumya Gandhi, Srikrishna Sitaraman, Venky Sundaram, Rao Tummala  
[Georgia Institute of Technology]

**E**lectronic systems are comprised of various active and passive components, often packaged as individual components and interconnected on a system board. There has been an evolutionary trend to miniaturize both packages and interconnections. This is one approach to system miniaturization, however, that will eventually reach limits in package miniaturization, passive component miniaturization, component properties and assembly processes. In addition, the long interconnect length between active and passive devices inherent with this approach, limits system performance. There is yet another factor that also limits both the signal speed, driven by the dielectric constant of the medium in which the interconnection is embedded, and the power consumption, driven by the electrical loss of the medium.

A new concept, referred to as 3D integrated passive and active components (IPAC), being developed by Georgia Tech's Packaging Research Center (PRC), addresses all the above shortcomings in achieving miniaturization and performance. This technology can also lead to lower production costs than those seen with today's approaches.

## 3D IPAC concept

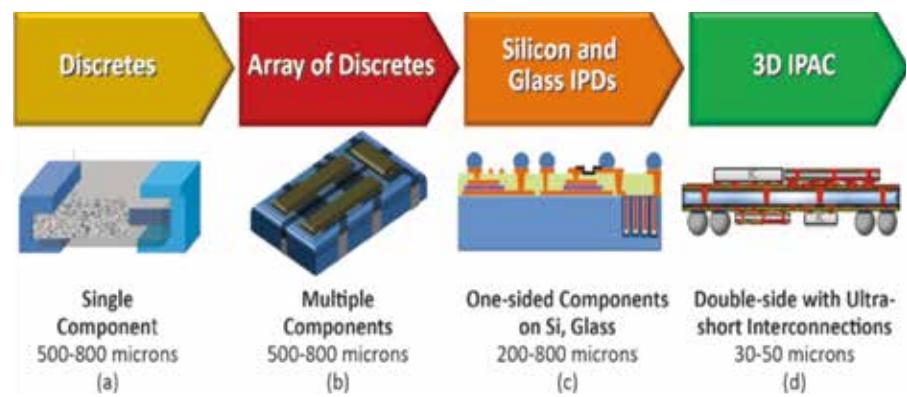
The 3D IPAC concept comprises an ultra-thin glass substrate as the low loss and low dielectric constant medium ( $\sim 30\mu\text{m}$  thickness) with low-cost through-package copper vias and double-side RDL wiring layers. This configuration allows assembly of both active and passive components on both sides, as illustrated in **Figure 1**. Such



**Figure 1:** 3D IPAC and 3D IPD concepts.

a concept has many advantages. It is ultra-miniaturized in both XY and Z dimensions. For example, in the XY dimension because of the double-sided assembly of active or passive components, the result is a cutting of the size almost in half. Furthermore, in the Z direction, ultra-miniaturization is realized because of the use of an ultra-thin glass substrate ( $30\mu\text{m}$ ) and ultra-short ( $10\mu\text{m}$ ) interconnections to both active and passive devices. The total thickness of the completed substrate is less than  $100\mu\text{m}$ . In this approach, unlike in current and other approaches, the interconnection distance between active and passive

components is only about  $50\mu\text{m}$  (curved arrow in **Figure 1**), which gives rise to the highest performance levels. The passive and active components can also be embedded in the cavity of the glass substrate, or in its wiring layers, for additional thickness reduction and performance enhancements. The 3D IPD (integrated passive device) concept, shown in **Figure 2**, is similar to 3D IPAC except that it is used for passive components only. These 3D IPD components are formed as ultra-thin discrete devices, ready for testability, with multiple passives, as films or layers on an ultra-thin glass substrate with through-vias.



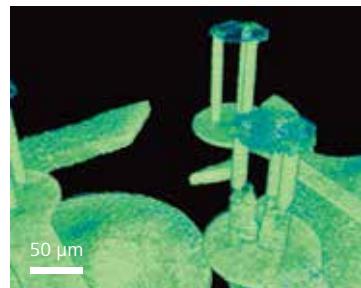
**Figure 2:** Evolution of passive components to the 3D IPAC concept for active and passive integration of functional modules.

The moment "I think" becomes "I know".

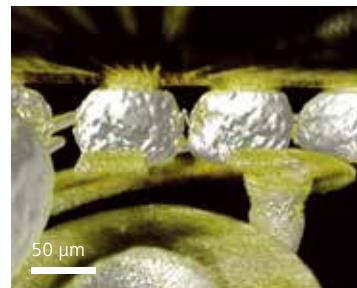
**This is the moment we work for.**

// TECHNOLOGY

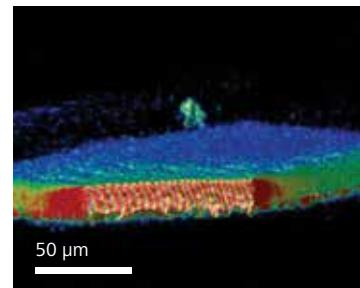
MADE BY CARL ZEISS



Defective TSV



Bump Short from Electromigration



Copper Dendrite



**What are you learning from your defects?**

As the industry strives for ever increasing performance and efficiency, semiconductor packages are becoming ever more complex with associated failures more difficult to determine. See inside your intact complex IC packages with non-destructive 3D X-ray at high resolution. The new Xradia 520 Versa from ZEISS provides you with higher throughput for faster time to results with the power of full volumetric data.

 **xradia®**

**is now**

[http://www.zeiss.com/xrm\\_electronics](http://www.zeiss.com/xrm_electronics)



## Component integration

**Substrates.** Current, leading-edge RF modules are mostly based on either low-temperature co-fired ceramics (LTCC) or low-cost organic substrates. The LTCC substrates provide the best loss and quality factor at GHz frequencies for RF interconnections and embedded RF passives, but do not typically meet the reduced thickness and lower cost needs of smart mobile devices. Traditional organic substrates, fabricated on large panels using low-cost glass-epoxy laminates, do not have the required RF characteristics. However, they can be fabricated with advanced dielectrics, such as liquid crystal polymers (LCP), to achieve the desired RF properties. This fabrication process, however, results in high costs and an inability to shrink lithographic dimensions with tight tolerances. Organic substrates also have challenges in achieving fine-pitch, chip-level interconnections with high reliability because of the TCE mismatch to ICs. Silicon substrates have high electrical loss and high wafer fabrication costs.

**Modules with discrete passive components.** Today's functional modules utilize discrete passive components manufactured separately and assembled onto the packages or boards. These components are typically 0.3–0.5mm thick, as shown in **Figure 2a**, resulting in module thicknesses >1mm. Over the past 10 years, these devices have been successfully integrated as component arrays (**Figure 2b**) and thinner IPDs for some applications [1]. As these components are large and mounted far from the active ICs in 2D side-by side configurations, they add parasitics that scale with interconnection length, unlike the 3D IPAC module described here [2].

**Modules with embedded discretes.** To address the above limitations of discrete passives, there is an increasing trend to bury the passives in the substrate core or as a part of the build-up layers [3,4]. This approach reduces the distance to active devices to less than 200 $\mu$ m, improves the module performance, and saves the package and

board space. This approach is, however, limited by the component thickness (0.3–0.5mm) and in the number of components as well as their testability and thermal issues.

**Modules with thin-film components.** These modules suffer from other limitations such as achieving good tolerance levels, testability, reworkability, and defect-driven yield losses.

RF components in organic substrates depend on low-loss polymers, but their low dielectric constants and permeability lead to relatively large component designs. Any increase in the dielectric constant is accompanied by a strong dependence of capacitance with temperature, frequency, voltage bias and film thickness. Components with standard organic substrate technologies also do not achieve the required tolerances for precision components. Their poor dimensional stability and warpage, as well as their moisture uptake, pose challenges for miniaturizing RF devices.

Thin-film components on silicon IPDs have many advantages [5–7] (**Figure 2c**) but suffer from low Qs (less than 10) and expensive processes, in addition to low inductance densities. To overcome these challenges, IPDs are also made of glass, which enhances their Q factor [8]. However, these thick glass or silicon IPDs are surface-mounted on the board as passive modules, far away from active ICs, and are not typically integrated with actives and passives as complete, functional modules. Further, they only have components mounted on one side. High-density inductors with magnetic films on these IPDs [9] help to improve the inductance density but do not meet the frequency stability above 1GHz unless novel nanomagnetic structures are invoked. These silicon and glass IPDs, therefore, differ from 3D IPDs being developed by GT-PRC.

The 3D IPAC concept described in this paper goes beyond the state-of-the-art passive technologies described above in many ways. The GT-PRC 3D IPAC design includes novel thin-film materials and processes for improved

properties: ultra miniaturized and testable RF and power 3D IPD modules and high-performance by virtue of closest proximity between actives and passives.

In contrast to flip-chip and wire bond device-to-package interconnections, the 3D IPAC concept uses ultra-short copper interconnections, formed with low-temperature and low-pressure processes, with the best electrical and thermomechanical reliability. All these benefits are expected to result in 3D IPACs with 2X improvement in performance levels and 2–5X reductions in size compared to current modules.

## 3D IPAC advances at GT

**Glass-based 3D IPAC substrates.** GT-PRC has been pioneering innovative glass substrates as a superior and low-cost alternative to ceramic, silicon and organic substrates. By developing a new set of low-cost panel-based processes such as laser via processing, polymer build-up layers and wet metallization, it has recently demonstrated the first generation of through-via glass substrate technology in thicknesses of 100–150 $\mu$ m, 60 $\mu$ m TPV diameters at 100 $\mu$ m pitch, 5 $\mu$ m wiring traces, resulting in 50 $\mu$ m pitch Cu-micro-bump interconnections [10]. In the next generation of glass substrates, advances will be made to reach 30 $\mu$ m glass thicknesses and TPV diameters scaled down to 10–15 $\mu$ m with 20–30 $\mu$ m pitch and chip-level interconnections with heights up to 7 $\mu$ m. These substrates, for the first time, enable ultra-thin functional modules with double-side actives and passives displaying the best performance, miniaturization and cost reduction.

**RF inductors.** GT-PRC and its material partners have demonstrated major fundamental and technological advances in the design and fabrication of high-frequency inductors. RF inductor design libraries for high-density, Q>200 and SRF>10GHz were developed with various substrate geometries and design rules [11]. Using advanced inductor fabrication processes

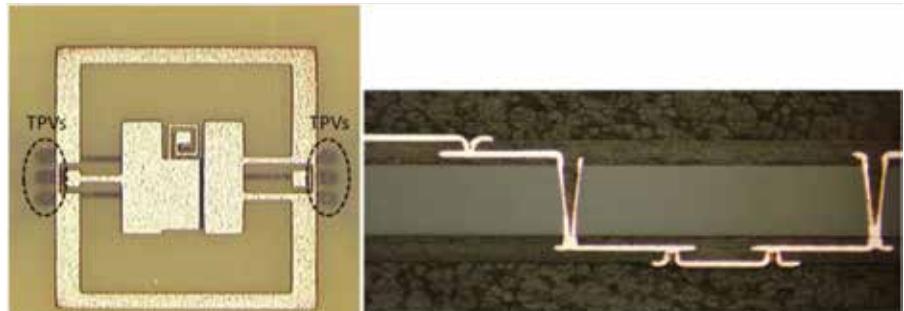
on glass with high coil densities, an inductance density of  $50\text{nH/mm}^2$  with Q above 60, has been demonstrated [12].

**RF capacitors.** The 3D IPAC glass substrate in development at GT-PRC provides unique opportunities to integrate a new class of low-loss and high permittivity dielectrics with high precision and low tolerance, unlike with ceramic or traditional organic laminate processes. By incorporating paraelectric fillers into the low-loss build-up layers, composites with permittivity 3-4X higher than with the polymer matrix, with low TCC has been achieved [13]. GT-PRC is also pioneering innovative high K thin-film RF dielectrics based on glass-compatible nanostructured super-paraelectrics that can enhance the permittivity without compromising frequency stability and loss [14].

**Filters.** A new class of glass-based 3D IPD filters with double-side inductor and capacitor components, going beyond today's silicon IPDs, improving the component properties and component densities were recently demonstrated [12,15]. Through-via formation using high throughput tools and processes such as laser-via ablation and wet metallization techniques were utilized for interconnecting the components on both sides. An example of a 3D IPD filter fabricated with these processes on glass is shown in **Figure 3**. This filter shows an insertion loss of 0.6dB and return loss of above 25dB.

### 3D IPD for power components and other passives

**Thin-film capacitors.** GT-PRC has also been pioneering advances in thin-film decoupling capacitors [16-17] for more than a decade. These include the design and fabrication of power distribution network prototypes with power-ground planes and thin-film capacitors using ceramic thin films and ceramic-polymer composites, in partnership with several companies [18]. In spite of these and other advances, embedded thin-film decoupling capacitors still face manufacturing



**Figure 3:** 3D IPD filters on glass. (Courtesy: Vijay Sukumaran, GT-PRC)

**Expanded Fluid Dispensing Capabilities with Higher Precision**

**Accurate Dual Valve Dispensing**

**Self-Actuating Tilt Jetting**

**Nordson ASYMTEK's Spectrum™ II**

high-speed, high-accuracy dispensing platform sets a new standard for precision dispensing applications in microelectronics & semiconductor manufacturing and MEMS & LED assembly. Jet small dots and thin lines into tight spaces with Tilt Jetting and Precision Z-gap Control. Maximize productivity with Dual Valve Dispensing while saving manufacturing floor space with Spectrum II's small footprint.

[www.NordsonASYMTEK.com/highaccuracy](http://www.NordsonASYMTEK.com/highaccuracy)  
Watch the Video or contact us at  
[info@nordsonasymtek.com](mailto:info@nordsonasymtek.com)

**Nordson**  
ASYMTEK

challenges because of yield, testability and repairability issues. The 3D IPAC approach comprehensively addresses these challenges by forming a separate, testable component before assembly. Further, this approach yields better performances than embedded thin-film decoupling capacitors because of the close proximity (<40 microns) between the active and 3D IPD passives, as shown in **Figure 1**. GT-PRC demonstrated such advanced glass-based 3D IPDs with high dielectric constant thin films using glass-compatible processes [18-19].

**Power capacitors.** For power supply applications that need much higher volumetric capacitance densities, a new class of 3D IPD capacitors is being developed. The high capacitance density in this case is achieved by simultaneously increasing the dielectric constant, reducing the dielectric thickness to the nanoscale range and exponentially improving the area, using nanoporous electrodes (30–75 $\mu\text{m}$ ) and conformal dielectrics (30–40nm). The electrodes provide very high surface areas per unit volume from the nanoscale porosity. These high-density capacitors advance beyond the leading-edge trench capacitor IPDs by improving capacitance density by a factor of 10X, while simultaneously reducing the cost by using large area processes materials and tools [20]. In these approaches, capacitance densities >400 $\mu\text{F}/\text{cm}^2$  have been demonstrated with break down voltages exceeding 15V.

**High-density inductors.** A new class of magnetic-based inductors with high permeability, field anisotropy, low coercivity and frequency stability are being developed as well. Today's magnetic materials for power inductors face several shortcomings to meet these requirements. A novel approach that achieves the best permeability with frequency stability, and yet produces thick films in an economical way, is being developed at GT-PRC [21]. Novel nanomagnetic films with high permeability of 100 and low coercivity of 0.1Oe have been developed by

creating magnetic anisotropy in the films.

### Summary

A new 3D IPAC concept for passive and active component integration, advancing beyond today's discrete, embedded and IPD components, is currently in development at GT-PRC. The new concept starts with ultra-thin glass substrates with the lowest loss, followed by low-cost through-via formation and double-sided thin-film wiring for assembly of active and passive components with ultrashort interconnections. In addition, the concept of 3D IPD is being developed for ultra-miniaturized and high-performance passives.

We have been able to demonstrate technology breakthroughs in many of the key 3D IPAC building blocks. These include panel-based 3D IPAC glass substrates with small diameter TPVs and RDL wiring layers, 3D IPDs with precision RF components that include inductors, capacitors and filters, and 3D IPDs for power components with high volumetric capacitance density, high efficiency and low loss, as well as short interconnections between devices. 

The 3D IPAC described in this article is funded by an industry consortium consisting of many end-users and supply-chain companies. Those interested in knowing more or joining the Georgia Tech consortium are encouraged to contact: Dr. P. Markondeya Raj  
raj.pulugurtha@ece.gatech.edu.

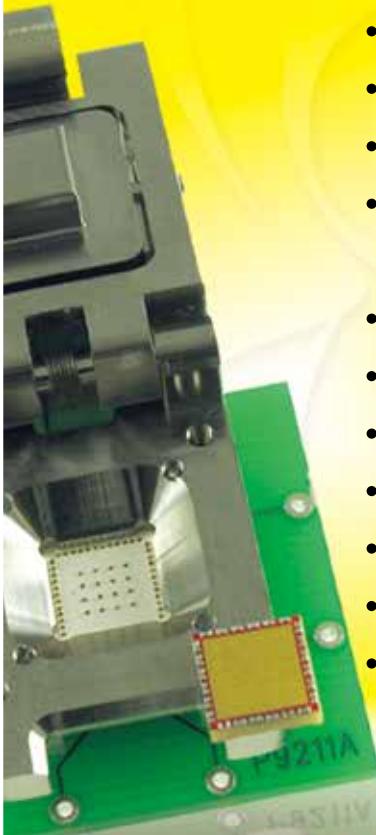
### References

1. "Murata's New ESR Capacitors Tackle Anti-Resonance," <http://www.murata.com/products/article/pdf/ta1082.pdf> [Feb. 21, 2013].
2. S. Gandhi, S. Xiang, P. M. Raj, V. Sundaram, M. Swaminathan, R. Tummala, "A low-cost approach to high-k thin-film decoupling capacitors on silicon and glass interposers," *Electronic Comp.* and Tech. Conf. (ECTC), 2012 IEEE 62nd, pp. 1356-1360.
3. R. Aschenbrenner, A. Ostmann, "The evolution and future of embedding technology," International Conf. on Electronic Packaging Tech., ICEPT 2013.
4. [http://www.i-micronews.com/upload/Rapports/Yole\\_FOWLP\\_EMBEDDED\\_die\\_package\\_2012\\_Sample.pdf](http://www.i-micronews.com/upload/Rapports/Yole_FOWLP_EMBEDDED_die_package_2012_Sample.pdf)
5. F. Murray, et al., "Silicon-based system-in-package: Breakthroughs in miniaturization and "nano"-integration supported by very high quality passives and system level design tools," Proc. Mater. Res. Soc. Symp., 2007, Vol. 969, pp. 27-36.
6. A. Polyakov, S. Sinaga, P. M. Mendes, M. Bartek, J. H. Correia, J. N. Burghartz, "High-resistivity polycrystalline silicon as RF substrate in wafer-level packaging," *Electronic Letters*, vol. 41, no. 2, Jan. 20, 2005, pp. 100–101.
7. K. Zoschke, J. Wolf, M. Töpper, O. Ehrmann, T. Fritzsch, K. Scherpinski, et al., "Fabrication of application specific integrated passive devices using wafer-level packaging technologies," Proc. 55th Electronic Components and Tech. Conf., 2005, pp. 1594–1601.
8. C. Nopper, "Glass for IPD applications," First International Global Interposer Tech. Workshop, Nov. 15, 2011, Atlanta, GA.
9. D. S. Gardner, et al., "Integrated on-chip inductors using magnetic material (invited)," *Jour. of Applied Physics*, Vol. 103, p. 07E927, 2008.
10. V. Sukumaran, T. Bandyopadhyay, Q. Chen, N. Kumbhat, F. Liu, R. Pucha, et al., "Design, fabrication and characterization of low-cost glass interposers with fine-pitch through-package-vias," in Proc. IEEE 61st Electronic Components and Tech. Conf. (ECTC), May 31–June 3, 2011, pp. 583–588.
11. S. Dalmia, F. Ayazi, M. Swaminathan, S. H. Min, S. H.

- Lee, W. Kim, et al., "Design of inductors in organic substrates for 1-3GHz wireless applications," Microwave Symp. Digest, 2002 IEEE MTT-S International, Vol.3, 2002, pp. 1405-1408.
12. V. Sridharan, et al., "Design and fabrication of bandpass filters in glass interposer with through-package-vias (TPV)," ECTC 2010 Proc. Vol. 60, pp. 530,535.
13. J-H. Hwang, P. M. Raj, I. R. Aboothu, C. Yoon, M. Iyer, H-M. Jung, et al., "Temperature dependence of the dielectric properties of polymer composite-based RF capacitors," Jour. of Microelectronic Eng., Vol. 85, Issue 3, March 2008, pp. 553-558
14. P. M. Raj, K. P. Murali, S. Gandhi, R. Tummala, K. Slenes, N. Berg, "Integration of precision resistors and capacitors with near-zero temperature coefficients in silicon and organic packages," Electronic Comp. and Tech. Conf. (ECTC), 2012 IEEE 62nd, pp. 910-914.
15. Y. Sato, S. Sitaraman, V. Sukumaran, B. Chou, J. Min, M. Ono, et al., "Ultra-miniaturized and surface-mountable glass-based 3D IPAC RF modules," 63rd Electronic Comp. and Tech. Conf. (ECTC), 2013 IEEE.
16. H. Windlass, M. Raj, D. Balaraman, S. Bhattacharya, R. Tummala, "Polymer-ceramic nanocomposite capacitors for system-on-package (SOP) applications," Adv. Packaging, IEEE Trans., vol. 26, pp. 10-16, 2003.
17. P. Muthana, K. Srinivasan, A. E. Engin, M. Swaminathan, V. Sundaram, B. Wiedenman, et al., IEEE Trans. on Adv. Packaging, 31, 234 (2008).
18. P. M. Raj, S. Xiang, M. Kumar, I. R. Aboothu, J. H. Hwang, Y. Liu, et al., "Leakage current suppression in solution-deposited barium titanate films on copper foils," Jour. of Materials Science: Materials in Electronics, Vol. 23, No. 4, pp. 901-908, 2012.
19. S. Gandhi, P. M. Raj, V. Sundaram, M. Swaminathan, R. Tummala, "A new approach to power integrity with thin-film capacitors in 3D IPAC functional module," 63rd Elec. Comp. and Tech. Conf. (ECTC), 2013 IEEE.
20. H. Sharma, K. Sethi, P. M. Raj, R. Tummala, "Fabrication and characterization of novel silicon-compatible high-density capacitors," Jour. of Materials Science: Materials in Electronics, Vol. 28, No. 2, pp. 528-535, 2012.
21. P. M. Raj, R. Tummala, N. Kumbhat, V. Sundaram, S. Uppili, J. Ellul, "Magnetic devices utilizing nanocomposite films layered with adhesives," WO/2013/025878; filed at the USPTO on 8/16/2012.

## Burn-In & Test Sockets 0.4mm to 1.27mm

### Industry's Smallest Footprint



- Up to 500,000 insertions
- Bandwidth 23 GHz
- 2.5mm per side larger than IC
- Ball Count over 3500, Body Size 2 - 100mm
- <25 mΩ Contact Resistance
- -55C to +180C
- 4A to 8A @80C rise
- BGA, LGA, QFN, QFP, & SOIC
- Optional heatsinking to 100W
- Six different Lid options
- Quick Turn Customs



**Ironwood**  
**ELECTRONICS**  
[www.ironwoodelectronics.com](http://www.ironwoodelectronics.com)

1-800-404-0204

# C4 interposer requirements driving high-precision flux deposition

by Fernando D. González [Sono-Tek Corporation.]; Ricky Bennett [Assembly Process Technologies LLC]; and Andy C. Mackie [Indium Corporation]

Upcoming interposer design for the flip-chip electronics packaging process may result in several challenges related to the overall assembly process. One of these is the need for high-precision fluxing. To better understand how the industry got to this point, it is helpful to go back to the fundamentals of wire bonding vs. flip-chip. The older and primary method of die-to-printed circuit board (PCB) interconnect, known as wire bonding, works by making connections from the integrated chip (IC or die) to the PCB via extremely thin wires (in the order of 15 to several hundred microns in diameter). In some cases, it can also incorporate an interposer, which acts as a medium between the die and PCB. The purpose of the interposer is to mechanically support the die while it distributes inputs/outputs (I/Os) to the package pins. This technology has been able to remain prevalent for today's packaging needs because of its flexibility and cost-effectiveness.

Driven by a market demand for smaller, faster electronics with a higher number of I/Os, an alternative electronics packaging method, by the name of flip-chip, was born. In this process, an interposer is always used. Solder bumps are deposited onto the die's metallized pads and then flipped onto the contact pad of the interposer. When ran through a reflow oven, the solder bumps melt and serve as connections to the interposer. An injection of underfill (a highly viscous epoxy) succeeds in filling in the empty gaps between the solder bumps, which aids in providing additional mechanical strength to the assembly and reduces

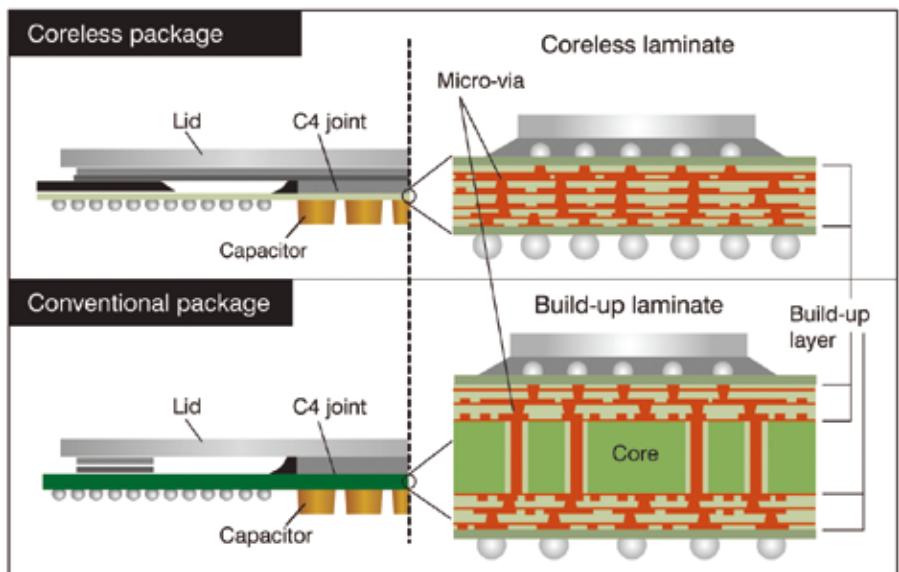


Figure 1: Thickness comparison of conventional vs. coreless interposers.

strain on individual solder joints by creating a structure that warps as temperature changes. The interposer can then be mounted onto the PCB via a pin grid array (PGA) or ball grid array (BGA). The flip-chip method is costlier and requires a higher level of optimization, but its advantages over wire bonding are too great to ignore. For high-speed applications, small solder bumps add minimal parasitics and propagation delays to the electrical signal path. It is also the most rugged interconnection method available due to the aforementioned underfill injection. Lastly, as die I/O continues to increase, perimeter electrical interconnection by wire bonding becomes limited, whereas for flip-chip, I/O can be arrayed over the entire surface area of the die.

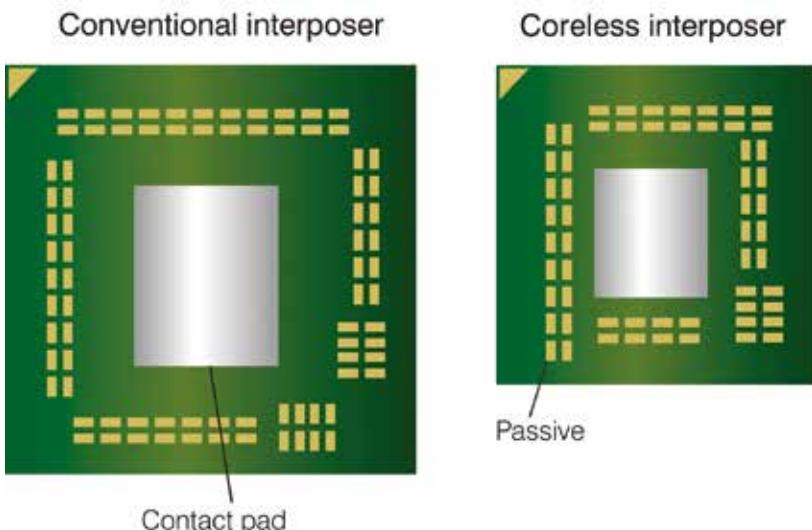
## Upcoming interposer technology

To enable electronic consumer

products to be designed smaller, lighter and thinner, improvements to die geometry are required. This requirement leads to a need for a thinner, less rigid interposer. Current, conventional interposers are approximately 1mm thick. Upcoming interposers, known as being either thin-core or coreless, are approximately 0.6mm and 0.4mm thick, respectively. **Figure 1** illustrates a conventional and coreless interposer package.

As the name indicates, the coreless package eliminates the need for a core, unlike the conventional interposer. This enables the build-up layer to be much thinner. Another advantage seen is high-speed transmission characteristics.

In addition to a significant reduction in thickness, these interposers are also required to have less surface area. A typical interposer's surface contains a contact pad (where the die will be



**Figure 2:** Surface area comparison of conventional vs. coreless interposers.

attached via solder bumps) and passive components (or passives) that are typically spaced approximately 3mm away from the contact pad. To reduce the surface area, the passives on coreless interposers are brought inwards, so there is a smaller gap between them and the contact pad. **Figure 2** compares the

typical surface of a conventional and coreless interposer.

#### New interposer design challenges

Because of the challenging requirements for new interposer designs, it is inevitable for new manufacturing issues to arise, the first being related to

the interposer thickness. The 40-60% decrease in thickness causes it to be slightly flexible. When a die has been flip-chip processed onto the interposer and run through the reflow oven to induce connections, the high heat can promote warping of the interposer, which leads to rework and possible scrapping of the expensive die.

Another issue arises due to the passives' closer proximity to the contact pad. An important process step prior to the actual flip-chip process is to apply a thin, uniform layer of flux to prevent oxidation and promote bonding. Current flux deposition methods face challenges that need to be addressed. New demands to the specification have led to the need for higher precision in the fluxing process.

#### Flux deposition techniques

The first approach to applying this layer of flux was done by a method called dip coating. In high-volume production, the die (with solder balls attached) is dipped into a small plate of

# CSP Test Sockets

**Now Available  
Down to 0.2mm Pitch!**

**A lot more of  
what you need...**

**...a lot less of  
what you don't!**

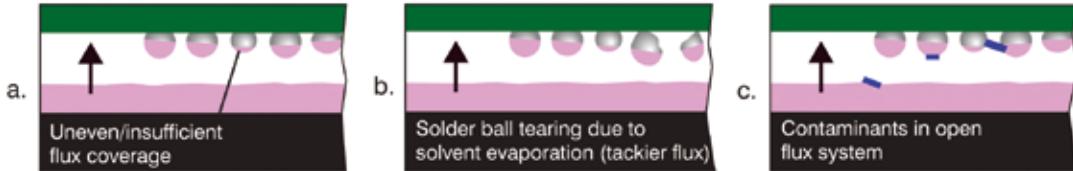
**MORE PERFORMANCE**

High-frequency (>40 GHz) sockets with a variety of materials to meet diverse testing requirements from Bench Characterization to Fully Automatic Handlers (>500k cycles) delivering what you need.

**ARIES®**  
ELECTRONICS, INC.

Bristol, PA 19007-6810  
Tel 215-781-9956 • Fax 215-781-9845  
Email: info@arieselec.com  
[www.AriesElec.com](http://www.AriesElec.com)

**The Evolution of  
Interconnect Innovation**



**Figure 3:** Dip coating process issues.

liquid flux. A rotating doctor blade controls the flux level on this plate. The flux thickness is determined by varying the solids concentration. A higher concentration would yield a thicker layer and vice-versa. The disadvantage with this process is that the flux thickness, which is a highly desirable variable to control, is reliant on the liquid and not the deposition application itself. In addition, since the solder balls are not 100% identical in pitch, some may not get adequately coated, resulting in a weak joint (**Figure 3a**). Evaporating solvent because of the flux plate being constantly exposed to an ambient environment results in a solids concentration increase. This increase must be monitored and compensated for by a solvent injection method for maintaining the flux's specific gravity specifications. A stickier flux (with higher than preferred concentration) ran the risk of pulling the solder balls off the die (**Figure 3b**). Furthermore, dust particles that fell in the flux could attach themselves to a short ball and prevent contact with the substrate (**Figure 3c**).

Ultimately, the multitude of issues listed above in addition to high maintenance and low flux thickness deposition flexibility (layers only as thin as 25 $\mu\text{m}$ ) led to manufacturers seeking a more robust and reliable flux deposition method. It became evident that the open flux system associated with dip coating could not be a long-term solution and that a non-contact deposition method was required. Following experimentation with a variety of methods, a more sophisticated technique, known as jetting, was adopted as the industry standard. This pressure spray method emits droplets (several hundred microns in size) onto the substrate that are flattened by a successive coaxial air assist that

causes the dots of flux to flow together and form the film. This method has been shown to significantly improve throughput time and consistently results in 100% coverage of the contact pad with pure, uncontaminated flux. There are, however, some obstacles to overcome as discussed below.

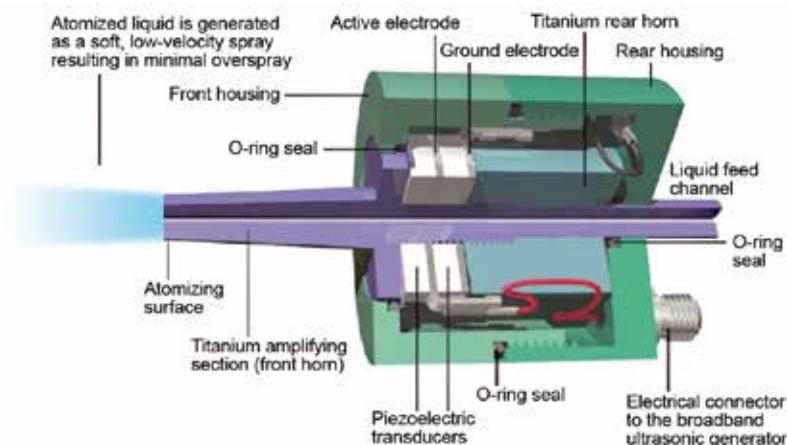
The first obstacle is caused by excessive flux deposition that leads to flux residue. Although significantly less than the residue seen in dip fluxing, excessive flux from jetting can lead to a problem known as "hot spots." When the die has been fully processed and is being tested, there is a noticeable temperature spike in the area where the flux is thickest. This spike leads to an unreliable final product. Another problem is the inability to consistently provide uniform thin-film layers. A non-uniform wet layer of flux may lead to an issue known as "die float," which refers to the die drifting off-center with respect to the flux pad. Therefore, when ran through the reflow oven, a significant number of connections will not be made. Finally, flux droplets can bounce off the surface of the flux pad because of the high speed at which they are being emitted. These resulting

satellite droplets can make contact with the surrounding passives that can lead to another issue known as "tombstoning." Since the passives are resting on wet solder paste, when the assemblies enter the reflow oven, the mix of spray flux and solder flux causes the passives to shift due to an imbalance of surface tension. In a worst case scenario, the component can stand up on one end (resembling a tombstone). Of course, all of these issues require that the manufacturer either implement rework, or scrap the interposer and die. Rework clearly wastes time and if unsuccessful, scrapping the die is an unfortunate financial consequence.

### Boat positioning

For optimal use of real estate versus units per hour (UPH), an array of substrates is positioned within a JEDEC format boat/carrier. A typical array would consist of two rows by five columns. However, any kind of array is acceptable providing that the standard format is maintained. Usually smaller substrates are positioned within the standard format to maximize the UPH, which could be as many as three rows by 9 columns, giving an array total of 27 parts. These are typical configurations, but could be more or less, depending on the factory configuration.

The boats used for substrate



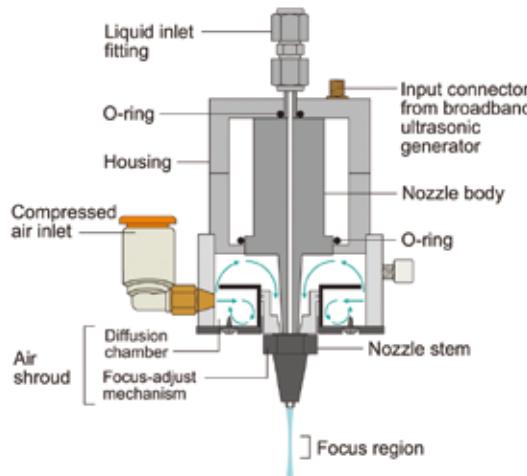
**Figure 4:** Ultrasonic nozzle cross-sectional view.

transportation are typically not manufactured to high tolerances. This will lead to boat positioning variation as well as individual part positioning within the boat. For example, the outer dimensions of the boat will have a sized tolerance, the position of each substrate pocket will have a positional tolerance, the size of the pocket will have a tolerance, and the substrate itself will have a tolerance. If each of these were held to  $\pm 0.05\text{mm}$ , the stacked tolerance would look more like  $\pm 0.2\text{mm}$ . In reality this is tight, and may be closer to greater than  $\pm 0.5\text{mm}$ .

Depending on the type of equipment used, mechanical and/or vision controlled systems can compensate for these errors, but it comes with a UPH overhead. To keep up with the UPH requirements, it is common practice to configure a spray pattern that compensates for the positional variations. This will lead to a larger than needed spray area. This is perfectly acceptable providing that there is available real estate so that flux does not cross contaminate on surrounding passives. With the demand for higher performance smaller packages, this ultimately becomes a serious problem, and therefore tighter spray processes are critical.

### Tailoring of flux for the deposition technique

To be able to form a solder joint onto the substrate metallization, it is necessary to have a solder alloy above its liquidus (upper melting point) and a metallization capable of forming an intermetallic with at least one of the component metals of the solder. One of the confounding factors is the presence of oxides (usually tin oxide for Pb-free solders) on the surface, which can cause a variety of issues. These range from very simple concerns such as poor wetting and voiding, to more serious defects such as head-in-pillow (HIP). HIP defects can sometimes occur when a physical contact is made between the oxidized solder and the metal contact, but without the solder, does not form a true metallurgical joint. To remove the



**Figure 5:** AccuMist cross-sectional view.

oxides and enhance wetting, a film of flux is used at the interface between the solder and the metallization.

The evolution of flux formulation and its rheology and the myriad methods for flux deposition have occurred in tandem. For this reason, flux and equipment manufacturers work hand-in-hand to supply the industry with materials and equipment that complement each other. In flip-chip processes, liquid fluxes may be either sprayed or jetted onto the surface of the substrate in precise locations (as with Indium Corporation's Flip-Chip Flux WS-575-SP), or the flip-chip itself may be dipped into a tray of more viscous flux (such as Indium's Flip-Chip Flux WS-575-A). Dipping fluxes tend to be used in high UPH operations using large die with large pitch, while spraying or jetting is used for smaller, fine-pitch die where a more precise control of the flux quantity is necessary.

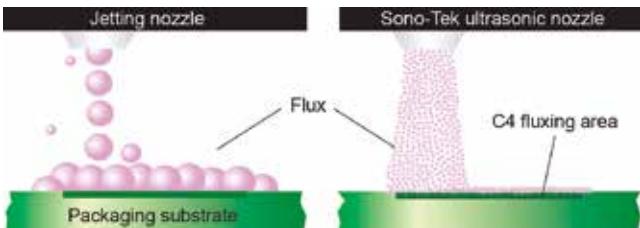
### Ultrasonic spray as an alternative

As can be gathered, increased control and precision is becoming a major topic for future flip-chip flux deposition processing. Ultrasonic spray is a method to address current and upcoming challenges. As the name implies, ultrasonic atomizing nozzles employ high-frequency sound waves—those beyond the range of human hearing. Disc-shaped ceramic piezoelectric transducers convert electrical energy into mechanical energy. The electrical

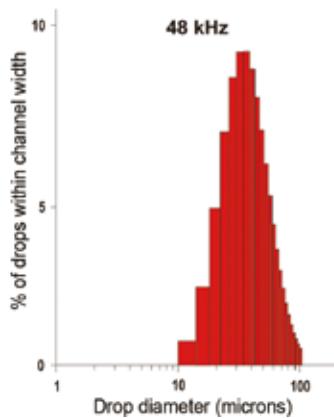
input, in the form of a high-frequency signal from a power generator, causes the transducers to vibrate at the same frequency. Two titanium cylinders magnify the motion and increase the vibration amplitude at the atomizing surface.

**Figure 4** shows a cross-sectional view of a typical ultrasonic nozzle. The electrically active elements, such as the transducers, electrodes and connecting wires, are sealed from external contamination. Chemically impervious o-rings assure the integrity of the seal. Nozzles are typically fabricated from titanium because of its good acoustical properties, high tensile strength, and excellent corrosion resistance. Liquid introduced onto the atomizing surface through a large, non-clogging feed tube running the length of the nozzle absorbs some of the vibrational energy, setting up wave motion in the liquid on the surface. For the liquid to atomize, the vibrational amplitude of the atomizing surface must be carefully controlled. Below the so-called critical amplitude, the energy is insufficient to produce atomized drops. If the amplitude is excessively high, the liquid is sheared, and large, unpredictable droplets of fluid are ejected, a condition known as cavitation. Only within a narrow band of input power is the amplitude ideal for producing the nozzle's characteristic fine, low-velocity mist.

Ultrasonic atomization deposition technology has over two decades of successful implementation with different flux applications. These applications include spray fluxing for PCB soldering and solar cell interconnects (known as bus lines) that can incorporate a variety of flux types and even extremely high solids fluxes. With thousands of machines currently operating in the field, ultrasonic spray has proven to be a precise fluxing deposition method and is considered today's modern established technology for high quality spray fluxing.



**Figure 6:** Jetting vs. ultrasonic spray droplets.



**Figure 7:** 48kHz drop diameter distribution.

Recent advancements in ultrasonic spray shaping control technology have led to the ability of it being a viable flux deposition method for the flip-chip process. The low velocity atomized flux is directed toward the substrate through the use of an air shroud. **Figure 5** illustrates the air shaping device, known as the AccuMist air shroud, which is appropriate for spray fluxing onto the small contact pads of the interposers. Compressed air, at around 0.5PSI, is introduced into the diffusion chamber of the air shroud, which produces a uniformly distributed flow of air around the nozzle stem. The width of the bow-shaped spray plume is controlled by adjusting the distance from the nozzle to the substrate—the typical height being approximately 10-15mm from the surface of the interposer.

### Method of drop formation

Ejected droplets from both jetting and ultrasonic nozzle technology are highly consistent in diameter. For jetting, since the droplet size is a function of the orifice diameter, the droplets tend to be in the range of 200 $\mu$ m or greater; see **Figure 6** for an illustration of this

concept. On the other hand, ultrasonically atomized droplets are a function of the frequency at which the particular nozzle is vibrating. Simply put, nozzles resonating at higher frequencies produce smaller diameter droplets and vice-versa. For example, a typical flip-chip flux atomized by a 48kHz nozzle has a median drop diameter in the range of 30 $\mu$ m. Because of both a slightly higher surface tension and density, the median droplet diameter for water is closer to 38 $\mu$ m. **Figure 7** depicts the log-normal drop diameter distribution for the 48kHz ultrasonic nozzle with water.

Although the sprayed media in **Figure 7** is water, the tight droplet distribution relationship is characteristic of ultrasonic spray and would carry over to a sprayed flip-chip flux. As can be interpreted from the graph, 9% of the droplets have a diameter of 38 $\mu$ m, 8% of the droplets have a diameter of 40 $\mu$ m, 8% of the droplets have a diameter of 30 $\mu$ m, and so on. This droplet regularity is advantageous for producing thin-film layers with high uniformity and avoiding the “die float” issue, which is currently experienced with jetting.

### Ultrasonic spray testing results

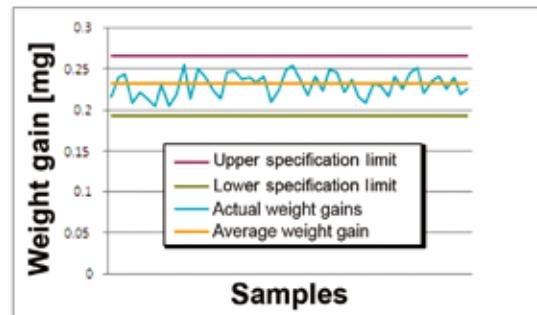
Desirable thin-film flux coatings, generally in the vicinity of 5 $\mu$ m, are determined by interposer weight gains following the coating process. Therefore, qualifying ultrasonic spray involved coating a large sample set of interposers to acquire weight gain information. The desirable coating thickness, which relates directly to a desired dry flux weight gain, was supplied with a permissible deviation percentage (typically around  $\pm 15\%$ ). All testing was able to

be achieved under the industry standard maximum cycle time.

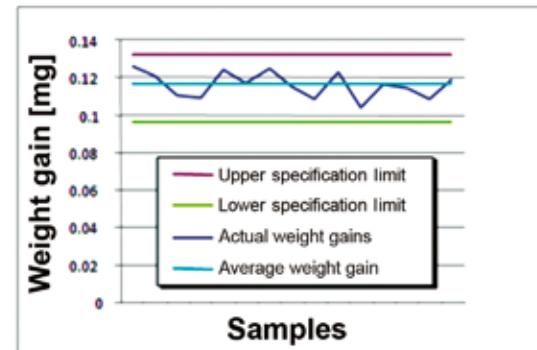
As **Figure 8** shows, over a wide range of samples, the weight gains never surpassed the maximum permissible amount (known as the upper specification limit, or USL) or fell short of the lowest permissible weight gain (known as the lower specification limit, or LSL). In fact, the weight gain deviation was found to be as low as  $\pm 12\%$ . This proven ability to provide consistent weight gains would result in interposers without flux residue, thus eliminating the issue of “hot spots.”

Furthermore, tests were conducted to verify if ultrasonic spray could provide similar results if the operator desired half weight gains (and therefore a thinner layer of flux). **Figure 9** provides these results. As can be gathered, weight gains still fell within the permissible range with even less deviation ( $\pm 11\%$  in this case). With this data, ultrasonic spray proves its flexibility in terms of deposition quantity, and therefore flux layer thickness.

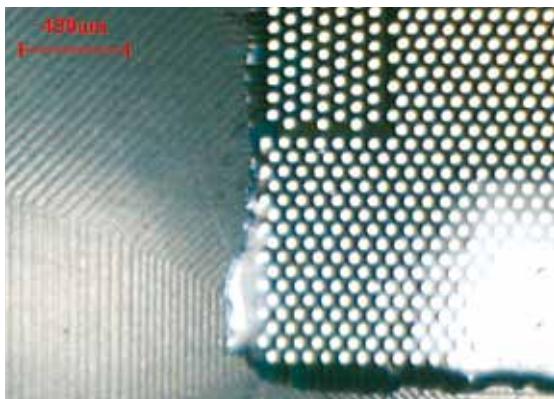
In addition to weight gain tests,



**Figure 8:** Flux weight gain consistency results.



**Figure 9:** Lighter flux weight gain consistency results.



**Figure 10:** Flux coating around perimeter of contact pad corner.

experiments were conducted to calculate transfer efficiency. This involved coating the contact pads of an interposer and measuring the dry weight gains of just the area of the contact pads and comparing it to the dry weight gain of a much larger area. The ratio would then result in the transfer efficiency from the nozzle to the contact pads. This was found to

be over 95%. The other 5% is the intended overspray due to compensation of the stacked positioning tolerance. **Figure 10** depicts a microscopic image of the contact pad on the interposer. What is being shown in this particular image is the bottom left corner of said contact pad. As can be seen, the overspray is minimal. Around the entire perimeter of the contact pad, the overspray was never greater than 750 $\mu\text{m}$ . This reduction in overspray and elimination of satellite droplets would result in tombstoning no longer being an issue since the over-sprayed flux droplets are nowhere close to falling on the passive components, even if they were brought in a couple millimeters closer. This achievement would then motivate interposer designers to be able to make interposers with a smaller surface area.

## Summary

Ultrasonic spray fluxing for the flip-chip process could bring a plethora of benefits for electronic packaging manufacturers. Improving on the advantages brought forth by jetting, ultrasonic spray is capable of not only being a viable coating method for today's flip-chip market, but can also prove to be a solution for tomorrow's upcoming flux deposition packaging needs. ☺

## Biographies

Fernando D. González received his Bachelor of Science in Electrical Engineering from Rensselaer Polytechnic Institute and is an Applications Engineer at Sono-Tek Corporation; email fgonzalez@sono-tek.com

Ricky Bennett is President & CEO of Assembly Process Technologies LLC.

Andy C. Mackie is a Senior Product Manager at Indium Corporation.

## High Speed / Low Cost Development, Test & Burn-In Sockets

### Compression, SMT, & Thru-Hole PCB Mounting

Lead pitches as low as 0.4mm, up to 125,000 insertions.



Quick On/Off Lid  
Easy Screw - Lid removed to show detail.

### Multi-Cavity Sockets

Significantly reduce your socket & labor costs with these multiple IC test and burn-in solutions.



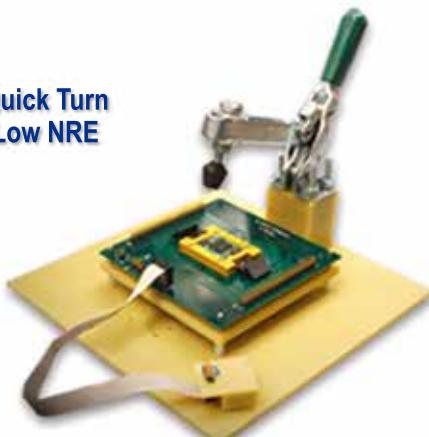
Easy Knob configuration



### Custom Test Fixtures

Fully automated or manually operated solutions to test any lead pitch & IC package

Quick Turn  
Low NRE



**ET®** **EMULATION TECHNOLOGY, INC**

1-800-232-7837

[www.emulation.com](http://www.emulation.com)

# Ultra high-bandwidth PoP infrastructure development

By Wael Zohni *[Invensas Corporation]*

**M**icroelectronics for mobile systems have been miniaturized to the point where they take up a small fraction of the total volume contained by very thin and light phones and tablets. This size reduction leaves more space for the battery and other critical components. These advances have been achieved in large part through chip integration, or the system-on-chip (SoC) approach, where typically two to eight processor cores are combined with two to four graphics processor cores in a single chip. While this has brought large computing resources to low power devices, it has highlighted the lack of memory access.

3D packaging is the norm for electronics densification and offers a platform for a high number of short interconnects between chips. For the processor and memory packaging, package-on-package (PoP) has become the most popular approach. Current solder ball stack or through-mold via (TMV) versions offer a maximum of 300-400 interconnects with up to 64 memory data interconnects, for

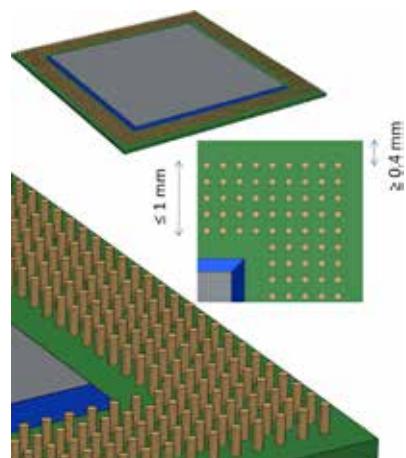
a bandwidth of up to 25.6GB/s at 1600MHz DDR signal speeds. As the SoC processors with multi-core CPU and GPU require more memory bandwidth, these PoP technologies become limiting. To meet high bandwidth requirements, a wide I/O memory industry standard has been proposed with up to 512 memory data interconnects for a bandwidth of greater than 100GB/s even at lower 800MHz DDR signal speeds. Memory devices with 512 data lines require about 1000 interconnects to include associated address, control, power and ground. PoP with 1000 interconnects requires pitch values of 0.24mm or lower to maintain the overall package size of 14mm x 14mm. The industry expectation is for through-silicon via (TSV) technology to offer this fine-pitch solution, but TSV is not expected to be widely available for such applications within the next few years.

In contrast, Bond Via Array™ (BVA™) PoP is a technology that can enable ultra high-bandwidth between multicore processors and high-bandwidth memory much sooner by utilizing

conventional wire bond technology and existing materials and infrastructure. The salient features of BVA PoP are the free-standing wire bonds that act as very fine-pitch vertical interconnects and the stacking of a memory package with the corresponding very fine-pitch ball grid array (BGA) on the logic package. **Figure 1** illustrates the capabilities of different processor-memory stacking technologies. BVA PoP offers TSV-like capabilities utilizing a conventional PoP assembly approach.

## BVA PoP

The BVA wire bond array interconnect concept is shown in **Figure 2**. The BVA interconnects are free-standing wire



**Figure 2:** BVA PoP design.

bonds that extend from the substrate to the top surface of the base logic package. The tips of these wire bonds form land terminals for mounting of a topside memory BGA package. The wire bonding approach offers very fine-pitch capability, using newly developed processes that utilize conventional wire bond equipment. The free-standing wire configuration bypasses existing PoP interconnect pitch limitations by

	BGA	TMV	BVA	TSV
Pitch (mm)	0.5-0.65	0.4-0.5	0.2-0.4	0.05-0.2
IO	200-300	300-500	500-1500	1000+

**Figure 1:** 3D packaging technologies comparison.

# Semiconductor-Grade Fluxes for 2.5D and 3D

Pitch (mm)	No. of interconnect rows				
	2	3	4	5	6
0.50	200	288	-	-	-
0.40	256	372	-	-	-
0.30	344	504	656	-	-
0.24	432	636	832	1020	-
0.20	520	768	1008	1240	1464

Table 1: Number of interconnects as a function of pitch.

Equipment	K&S IConn
Capillary	SU-64165-865E30-ZU34TS-400, H24-CD30-T60-OR12-F20 and 4187T-6023-R33
Wire	50 µm diameter Copper wire
Pad size	160 ± 20 µm
Pad finish	ENEPIG, Ni (5.0 ± 2.0 µm), Pd (0.06 ± 0.02 µm), Au (0.1 ± 0.05 µm)

Table 2: Wire bond details.

Parameter	Measured value	Comments
Ball-bond diameter	101µm-105µm	Design spec.: 90µm-110µm
Ball-bond height	30µm-31.6µm	Design spec: 25µm-35µm
Wire pull test	51.0gm-52.8gm	Failure at stem
Ball shear test	100.4gm-408.8gm	Cohesive failure

Table 3: Wire bond data summary.

decoupling the vertical structure's pitch from its corresponding height. Whereas solder spheres collapse in height with the reduced diameters required for finer pitch, vertical wire bonds can maintain desired stand-off heights while significantly reducing lateral pitch. The interconnect scaling capabilities are tabulated in **Table 1**. For a given 14mm x 14mm package and assuming a 1mm peripheral width for I/O at a distance of at least 0.4mm from the edge as shown in **Figure 2**, up to 1464 interconnects can be formed at 0.2mm pitch. These numbers of I/O are enough to meet future high bandwidth memory requirements.

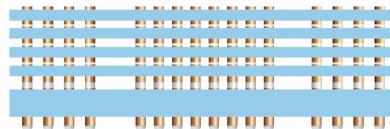
Two assembly methods introduced by BVA include the free-standing wire bonds and memory stacking with fine-pitch BGA. To validate these two processes, high-volume manufacturing (HVM) equipment vendors were engaged. Details of this activity are provided in the following sections.

### Free-standing bond wires formation

BVA PoP features free-standing wire bonds that act as fine-pitch interconnects between the processor and memory. Wire bond pads are patterned on the logic substrate to surround the logic chip. Two test vehicles were evaluated: one with 432 I/O at 0.24mm pitch (2 rows around the logic chip), and 1020 I/O at 0.24mm pitch (5 rows around the logic chip, as shown in **Figure 3**).

Multiple large-scale (over 100,000 continuous bonds)

### 2.5D and 3D Thermocompression Bonding (TCB)



### Applications and Materials

- Bump fusion/wafer fluxes for copper pillar/solder microbump
- Flip-chip fluxes for memory-on-logic and logic-on-interposer

### Attributes

- Process proven in 2.5D/3D server and mobile applications
- Water-soluble or no-clean near-zero residue (NZR)

### Our Products:

- Waferflux WS-3543
- Flip-Chip Flux WS-641
- Flip-Chip Flux WS-3555



Learn more:  
<http://indium.us/E033>

From One  
Engineer  
To Another®

[www.indium.com](http://www.indium.com)  
[askus@indium.com](mailto:askus@indium.com)  
ASIA • CHINA • EUROPE • USA

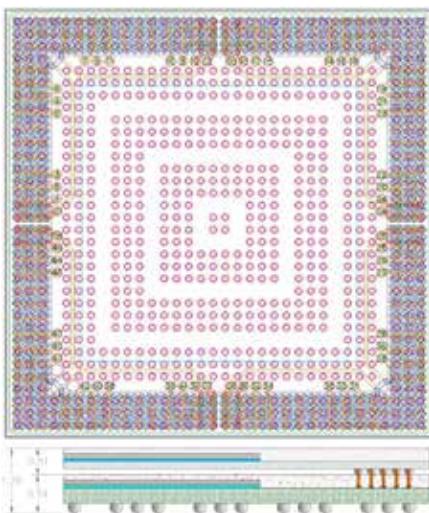


©2013 Indium Corporation

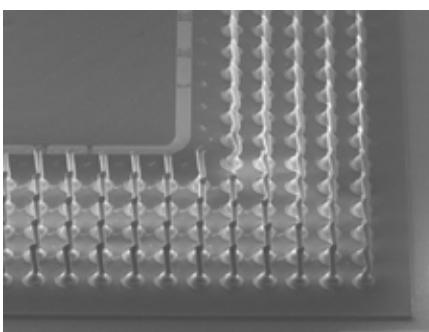
assembly demonstration runs were carried out for these two test vehicles. The wire bonding was carried out by Kulicke and Soffa (K&S), an established wire bond equipment manufacturer. The details of the evaluation setup are given in **Table 2**. The wire bonds for the 1020 I/O test vehicle are shown in **Figure 4**.

As part of these wire bond validation runs, wire bond ball size and bond strength were measured. The frequency plots for both are given in **Figure 5** and the data is summarized in **Table 3**. Results showed all bonding to be within required specifications.

To complete a single run of bonding 117 logic substrates with 432 I/O each for a total of 50,544 wires, the total



**Figure 3:** 1020 I/O test vehicle with 5 rows of interconnects at 0.24mm pitch.

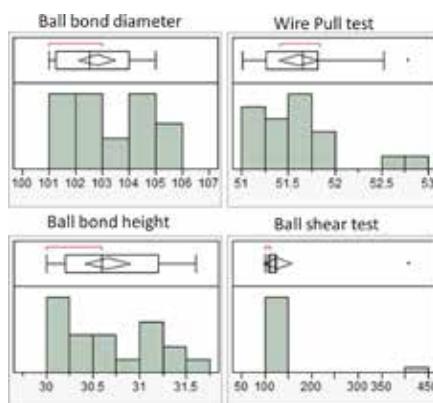


**Figure 4:** Wire bonds on the 1020 I/O test vehicle.

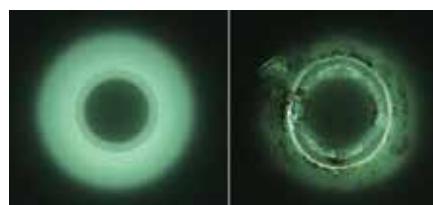
processing time was 1.836 hours. This amounts to an average of 7.65 bonds per second (BPS) and a package unit throughput of 63.7 units per hour (UPH). For another run of bonding 113 logic substrates with 1020 I/O each for a total

of 115260 wires, the total time taken was 4.61 hours. This amounts to an average of 6.95BPS and a package unit throughput of 24.5UPH.

During both runs, only one unit was rejected because of non-stick wire bonds. This defect was linked to wire bond capillary wear. **Figure 6** shows the capillary tip when new and after 103,000 wire bonds. Once the capillary was changed, no non-stick wire bonds were encountered. These HVM runs successfully validate the BVA free-standing wire bond technology for high I/O PoP.



**Figure 5:** Frequency plots of measured wire bond values after multiple 100,000 wire bond runs.



**Figure 6:** The capillary tip as new and after 100,000 wire bonds.

Test	Standard	Test condition	Sample size	Evaluation	Result
Moisture sensitivity Level 3	IPC/JEDEC-J-STD-020C	125°C for 24hrs; 30°C/60% RH for 192 hours, 3X Pb-free reflow	22 logic and 22 memory packages	C-SAM Inspections at T0 and post-MSL3	Pass
High temp. storage	JESD22-A103D-condition B	150°C, 1000 hours	22 PoP off-board	E-test after 168, 500 and 1000 hours	Pass
Unbiased autoclave	JESD22-A102D-condition D	125°C/100%RH/2atm for 168 hours	22 PoP off-board	E-test after 96 and 168 hours	Pass
Drop test	JESD22-B111	>30 drops, 1500 G, 0.5 msec. 20 PoP on board with underfill	In situ monitoring	Pass (125 drops)	
Temp. cycling (board level)	JESD22-A104D Condition G	MSL3 and then -40°C to 125°C, 1000 cycles	45 PoP on board with underfill	In situ E-test up to 1000 cycles	Pass

**Table 4:** Reliability test results.

PoP stacking with the logic-to-memory interconnect pitch at 0.5mm and 0.65mm is routinely practiced by the industry, with 0.4mm pitch emerging as the next step in conventional capability. Although

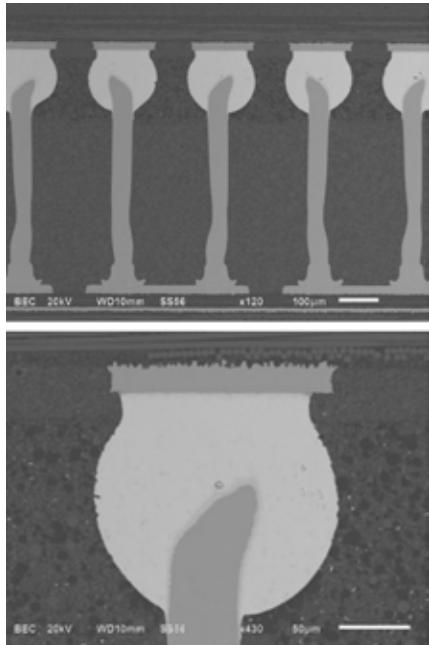
the 0.24mm pitch offered by BVA PoP is significantly finer than the industry norm, stacking these fine-pitch packages was successfully demonstrated by a third party surface-mount technology (SMT) equipment vendor, Universal Instruments Corporation (UIC). The main process steps for BVA PoP stacking are the same as for conventional PoP and correspondingly include flux dipping memory packages, placement on the logic packages, and reflowing the solder interconnects.

For the flux application, a linear thin-film applicator was used. This method offers linear actuation for thickness uniformity and supports a broad viscosity range. It allows for gang or individual dip processing and has quick-release tooling for easy cleaning. These features assure thickness repeatability with the cavity plate, force based dipping, and dip verification based on spindle impact sensing. The memory packages were dipped into tack flux prior to placement on logic units.

Logic and memory packages may be stacked individually or on the printed circuit board (PCB). In this case, individual stacks were assembled. Individual stacks allow for a single component to be supplied to multiple assembly lines, with the trade-off that the parts have to go through an extra reflow cycle and require separate trays for the stacked packages. The individual stacking process is fully automated. The memory packages were picked, vision inspected for 9 solder balls in each corner, for a total of 36 solder balls, and then placed on the logic packages with 30g force. Conventional mass reflow was used. The resulting solder joints are shown in **Figure 7**.

The individual stack assembly yield was 100% with one lot and only one short was reported in a second lot as a result of operator error. These results

validate the fine-pitch stacking of memory packages on the wire tips of logic packages.



**Figure 7:** Cross section SEM of wire bonds to solder interconnects between the logic and memory package.

### Reliability testing

Reliability tests were carried out and the results are summarized in **Table 4**. In situ monitoring of the daisy-chain resistance was done for all tests and no failures were detected. The drop test was continued to 128 drops and no failures were observed. The parts that were mounted on the test boards were underfilled before testing.

### Summary

Small form-factor mobile computing systems require not only microelectronics densification such as PoP, but also high performance to address emerging product needs. BVA PoP technology offers ultra high-bandwidth between the logic and memory packages. With the potential for more than 100GB/s memory bandwidth, BVA offers a compelling solution for next-generation systems. By utilizing free-standing wire bonds as interconnects, very fine pitch is achieved.

To validate this packaging technology, two advanced processes, free-standing

bond wires and fine-pitch memory package stacking were validated for HVM through third party manufacturing equipment vendors. Multiple 100,000 wire bond runs were performed for both 432 I/O and 1020 I/O test vehicles. It was shown that after processing more than 100 devices at a time, a throughput of about 7 bonds per second was achieved with minimal yield loss due to capillary tool life, which can be readily addressed in HVM. Stacking fine-pitch memory packages on top of a BVA logic package was also carried out at nearly 100% yield using available SMT equipment.

Extensive validation of the above featured processes for BVA indicates this interconnect technology is capable of high-yield assembly and offers a compelling near-term solution for achieving high-performance PoP.

### Biography

Wael Zohni received a BSME from Worcester Polytechnic Institute, MA; he is VP at Invensas Corporation; email [wzohni@invensas.com](mailto:wzohni@invensas.com)

### Acknowledgments

The author would like to acknowledge Kulicke and Soffa (K&S) and Universal Instruments Corporation (UIC) for their contributions to this article.

# CONTECH Solutions, Inc.

Contech Solutions has been providing innovative test interface tools to the worldwide semiconductor industry since 1995. ATE contactors • Manual test sockets • Reliability sockets • FA sockets • FA boards • DUT boards BIB probes • Socket receptacles • Adaptors



631 Montague Avenue • San Leandro, CA 94577  
T: 510.357.7900 Ext. 203 • F: 510.357.7600

[www.ContechSolutions.com](http://www.ContechSolutions.com)

# Lowering cost of silicon etch for revealing TSVs

Laura B. Mauer, John Taddei, Ramey Youssef [Solid State Equipment LLC]

## 3

D Integration is becoming a reality for packaging a variety of different integrated circuits. Cost and process controls remain the primary barriers to the introduction of 3D packaging into high-volume manufacturing. Thinning the device wafer is a critical part of the overall process, and using wet etch to reveal the through-silicon vias (TSVs) is one way to dramatically reduce costs. Using an adjustable, automated spin etch tool can significantly improve the process control. Capital costs are further reduced by eliminating the polishing step after the bulk grind of the silicon and by integrating cleaning and silicon thickness measurement into the wet etch system.

The TSV middle process appears to be the preferred integration scenario and the process flow has been discussed previously [1,2]. The device wafer is mounted on a carrier using an adhesive layer. The structure is illustrated in **Figure 1**.

The silicon wafer needs to be thinned to reveal the Cu TSVs so that 3D connections can be made. The overall process currently involves four steps: grinding, polishing, cleaning, and plasma etch.

The bulk of the excess silicon is removed by grinding. Mechanical grinding is the preferred technique for wafer thinning because of its high removal rate [3]. Commercially available grinding systems typically use a multi-step process that starts with a coarse grinding process at very high rates ( $5\mu\text{m}/\text{s}$ ), with a subsequent fine grinding process at a reduced rate ( $\leq 1\mu\text{m}/\text{s}$ ). While the fine grinding step(s) removes most of the damaged layer that is created by the coarse

grinding step, there still remains a defect band near the wafer surface. The thickness of this defect band is dependent on the grinding conditions [4].

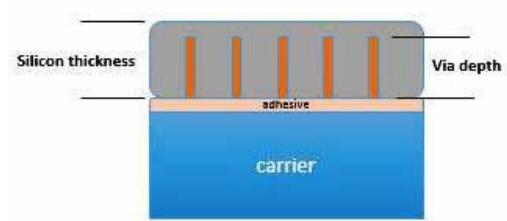
These residual defects can cause stress in the thinned wafer that leads to additional bowing and can result in wafer breakage. The subsurface damage of the coarse grind can be reduced by grinding with finer abrasives, but not removed entirely [5]. This increases the process time and is frequently followed by a polishing process to reduce the remaining subsurface damage and eliminate stress in the wafer. A cleaning process is needed to remove any residual polishing slurry and ensure a clean surface.

Finally, the Cu TSVs need to be revealed. These last three steps (polish, clean, and reveal) can be replaced with a wet etch process that polishes and cleans while it accomplishes the reveal. Furthermore, any variation in the removal of silicon during grinding can be reduced by adjusting the wet etch process. The overall etching is controlled by integrated measurement of the remaining silicon thickness.

## The wet etch process

The wet etch process has the ability to compensate for the non-uniformities of the post-grind wafer, coupled with the via depth variations, in addition to removing the grinding marks and smoothing the surface. **Figure 2** shows the surface roughness after the grinding process.

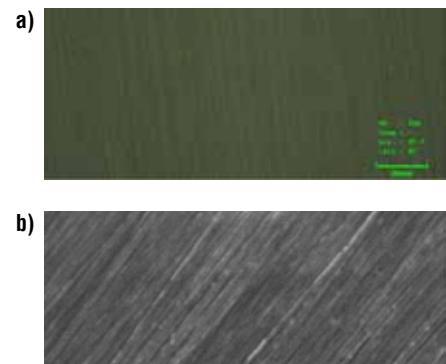
We are using a two-step etch process. The first step is focused on smoothing the surface and eliminating thickness non-uniformities at a high etch rate. The



**Figure 1:** Cross section of a bonded wafer post-grind.

second step must be selective to both the oxide liner and the metal studs.

For the first step, isotropic wet etching of silicon is used to provide a smoothing of the surface roughness, as well as to effect a high etch rate. The etchant contains a mixture of nitric and hydrofluoric acids as active etch ingredients. The nitric acid acts as an oxidizer to convert the surface into silicon oxide and then the HF etches the oxide. For use in a single-wafer spin processor, the addition of chemicals with higher viscosities is needed to provide a more uniform etch of the wafer surface. Phosphoric and sulfuric acids are added for their viscosity and do not chemically participate in the etching reaction. The addition of these viscous acids does not alter the chemical kinetics, but does increase the mass-transfer resistance as a result of the increase in viscosity.



**Figure 2:** Images of the rough surface post-grind a) optical, and b) SEM.

In addition, the ratios of the chemicals can affect the surface roughness. At high HF and low nitric acid concentrations, the process is very temperature dependent. Further, the reaction rate cannot be easily controlled, resulting in unstable silicon surfaces. At low HF and high nitric acid content, smooth, polished surfaces result because of the more diffusion-limited reaction. With the addition of the viscous acids, the surface roughness decreases more efficiently for the same removal rate. The use of a spin etch system allows the optimization of this step. Further, the rate of chemical reaction, along with the spin process parameters, has significant effect on the overall uniformity and surface finish [6]. Process conditions can be selected to tailor the etch rate for a smoother surface and to compensate for the non-uniformities of the post-grind wafer.

For the second step, a selective etch process is used to reveal the metal vias;

the chemistry does not attack the oxide liner or metal of the TSV. Previously, both KOH and TMAH have been used for this etch process and have been discussed in detail [7,8]. These chemistries meet the criteria of being selective to silicon without etching oxide or copper. KOH has a higher etch rate than TMAH, but leaves a potassium silicate residue that must be removed with an in situ post-cleaning process. TMAH has health concerns, which make it less desirable, even though it etches residue free.

To compensate for the deficiencies of both KOH and TMAH, we use a new anisotropic chemistry developed by Sachem. This chemistry, known as Developmental Si Etchant SMC 42-1, has been used for this process with excellent results. This etchant has a higher etch rate than TMAH, does not have the health concerns of TMAH, and leaves a clean, residue-free surface, unlike KOH. The selectivity to oxide is ~10,000:1. This formulation also allows for process

optimization when combined with the process parameters available only in a spin etcher.

The results of the wet etch are illustrated in **Figures 3** and **4**. An AFM image of the rough surface after grinding, but before polish, is shown in **Figure 3a**. The grind marks are clearly visible. The roughness Ra value was 10.2nm after the overall grinding process.

The two-step wet etch process not only compensates for thickness variations, but also smoothes the surface. The final surface is shown in **Figure 3b** and has an Ra value of 1.5nm. **Figure 3b** is at the same scale as the initial measurement in **3a**, while **Figure 3c** provides an expanded scale with higher resolution.

**Figure 4** provides optical and SEM images of the post-etch results at the same magnifications as the post-grind images in **Figure 2**. The oxide-covered Cu vias are revealed and the silicon

**connector capabilities**

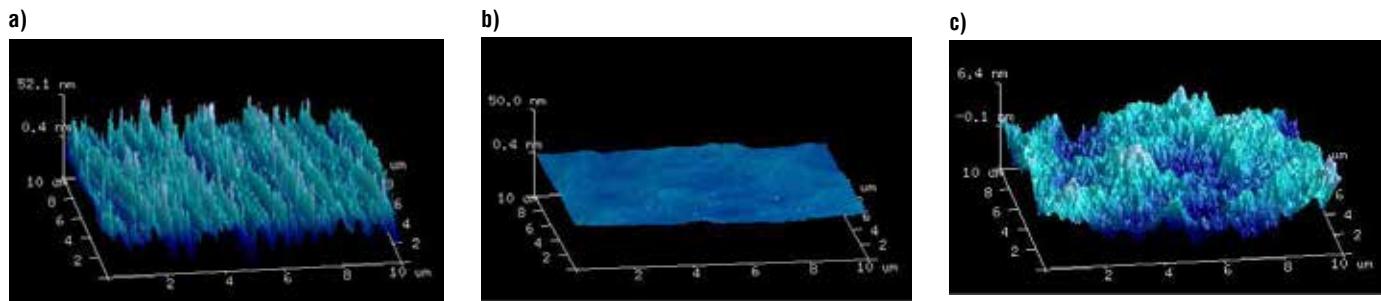
**solutions for your needs**

CCS is your engineering resource. Where other companies are limited to offering standardized products, CCS is uniquely positioned to design integrated solutions that meet your specifications. CCS supports the mid and low volume needs of customers that require design intensive, high compliance, long cycle life connectors.

[www.compliantconnector.com](http://www.compliantconnector.com)

**ECT**  
EVERETT CHARLES  
TECHNOLOGIES  
A DOVER COMPANY

[www.ectinfo.com](http://www.ectinfo.com)  
401-739-7310



**Figure 3:** AFM a) post-grind, b) post-etch with the same scale, and c) post-etch with an expanded scale.

surface is smooth, with no visible grind marks.

### Thickness measurement and profile control

The variation of the silicon thickness after grinding can be up to  $10\mu\text{m}$  radially within a wafer. These non-uniformities come from the variations in the TSV etch depth, bonding adhesive thickness, and grind uniformity. Some of these variations are dependent on each other. For instance, in areas where the bonding adhesive is thicker, the silicon will be thinner after the grinding process. Large variations are also observed from wafer to wafer. Single-

wafer processing in a spin etch tool can compensate for both types of variations.

Single-wafer etch processing can compensate for radial non-uniformities by etching more or less across the wafer, depending on the process parameters. This is achieved using SSEC's controllable nonlinear motion profiles for chemical dispense. In fact, this method of compensation is absolutely necessary in order to provide more uniformly revealed vias after the etch process. SSEC's tools determine the silicon thickness with integrated infrared measurements. The integrated thickness measurement allows a tailored etch recipe to be calculated for each wafer immediately prior to the etch process. The post-etch measurement confirms the proper amount of silicon was etched.

Measurement of the silicon thickness prior to etching is critical to the reveal process, but must be combined with prior knowledge of the depth of the TSV. The manufacturer must have accurate dimensions of the metal stud that forms the TSV. The amount of silicon to be etched is determined based on the depth of the TSV and the desired height of the revealed Cu studs.

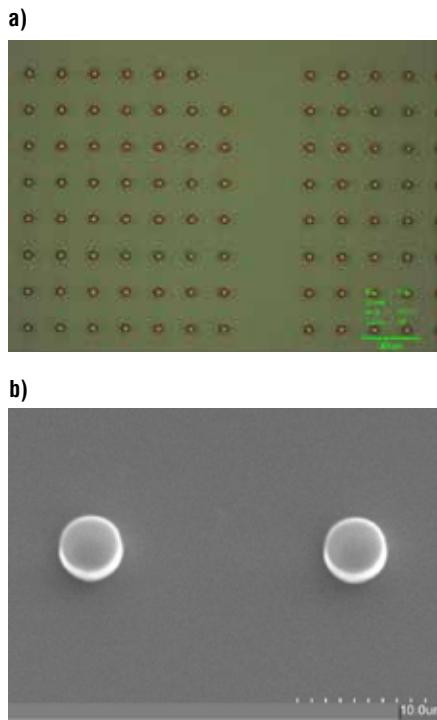
For the tools described above, a wafer thickness measurement sensor has been incorporated in a separate chamber in the system design in order to provide closed-loop feed-forward control of the etching process. The sensor measures the actual thickness of the device wafer, not the entire stack, which includes the carrier and adhesive. Multiple

measurements are taken across the diameter of the wafer. The measurement of the via depth must be done previously in the front end-of-line (FEOL) process when the vias are etched and filled. The data are combined to allow for the calculation of the silicon etch depth and radial profile. An example is shown in **Figure 5**.

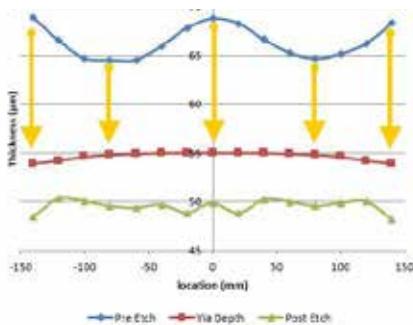
The etch rate in a single-wafer etch tool can decrease over time because of the chemical reactions changing the chemistry. A constant etch rate can be maintained by incorporating chemical replenishment. To ensure the proper chemical replenishment is taking place, the etch rate is monitored by measuring the amount of silicon that was etched on the previous wafer. Thus, the etch rate can be computed and used for the next wafer to provide closed-loop process control. The projected etch time with radial variation is calculated using this etch rate.

The variation in radial etch rate is selected based on the thickness of the silicon wafer, minus the depth of the TSV, plus the amount of TSV to be revealed. The arrows in **Figure 5** indicate the difference in etching that is needed as a function of the radius of the wafer. In this example, the vias were to be exposed by  $5\mu\text{m}$ . The initial thickness variation of the silicon after grinding was  $4.4\mu\text{m}$ . However, the TSV depth variation was  $1.5\mu\text{m}$ , which must also be factored into the etch calculation.

Using the same  $5\mu\text{m}$ -reveal example, if the etch had been done without compensation for the radial variations, the



**Figure 4:** Images of the smooth surface post-etch a) optical and b) SEM.



**Figure 5:** Pre- and post-etch thickness measurements.

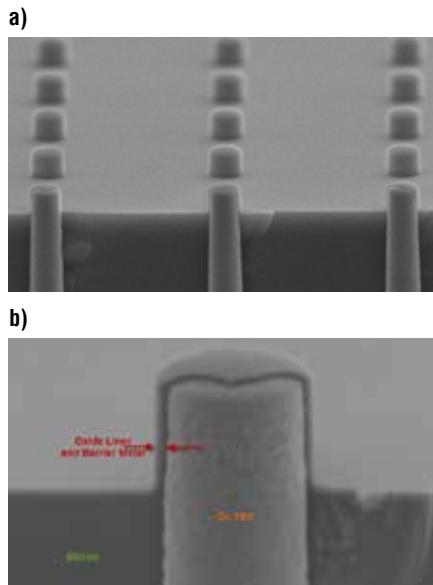
reveal heights would have varied by the initial 4.4 $\mu\text{m}$  of silicon non-uniformity, as well as the 1.5 $\mu\text{m}$  variation of the vias. Some of the vias could be exposed by over 10 $\mu\text{m}$  and could result in mechanical failure during subsequent redistribution layer (RDL) processing [9]. Using an etch profile to compensate for the incoming silicon thickness variation and the known variation of the vias, the resulting reveal heights were within a  $\pm 1\mu\text{m}$  window around the desired 5 $\mu\text{m}$ -reveal height.

**Figure 6** shows a cross section of a revealed TSV. The oxide liner and barrier metal are intact. There is no attack or dishing around the intersection with the silicon.

Continual thickness measurement allows the etch rate to be determined and not only fed forward for the next wafer to be processed, but also factored into the processing of the current wafer. If the final silicon thickness measurement is not within specification, the wafer can return to the etch chamber for further processing.

## Summary

Using a single-wafer tool with adjustable spin etching and integrated thickness measurement, a low-cost process to reveal copper TSVs has been demonstrated. The system described in this article can replace four tools (CMP, plasma, clean, and thickness measurement) with significant capital savings. The silicon surface is clean and smooth, removing the stress related to



**Figure 6:** SEM cross sections of revealed TSVs a) overview of mutiple TSVs, and b) enhanced view of a single TSV.

grinding. Compensation for radial non-uniformities in the silicon thickness and via depths is accomplished by modifications in the radial etch profile. An integrated wafer thickness measurement system provides critical information to control the etching process. The oxide isolation liner remains intact because of the selectivity of the chemical etching process.

## Acknowledgments

The authors would like to thank the following people for their significant contributions to this work: Yongqiang Lu and Sian Collins (Sachem); Willy Krusell, Bill Kalenian, and Thomas Brake (Strasbaugh); and Stephen P. Olson (SEMATECH).

## Biographies

Laura B. Mauer received her BS in Electrical Engineering from New York U. and her MS in Electrical Engineering from Syracuse U. and is Chief Technical Officer at Solid State Equipment LLC; email lmauer@ssecusa.com

John Taddei received his BS in Chemical Engineering from the U. of Pennsylvania and his BS in Physics

from Lebanon Valley College; he is a Process Lab Director at Solid State Equipment LLC.

Ramey Youssef received his BS in Chemical Engineering from Lehigh U. and is a Process Development Manager at Solid State Equipment LLC.

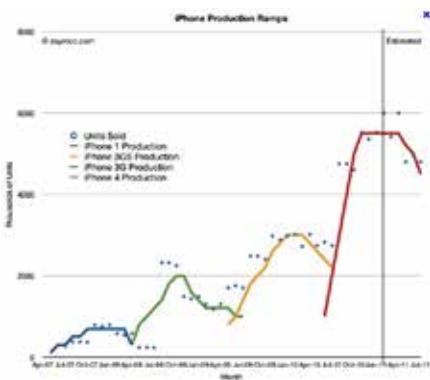
## References

- S. Olson, K. Hummler, "TSV reveal etch for 3D integration," 3D Systems Integration Conf., 2011, IEEE, pp. 1-4, Jan. 31, 2012.
- N. Kumar, S. Ramaswami, J. Dukovic, et al., "Robust TSV via-middle and via-reveal process integration accomplished through characterization and management of sources of variation," ECTC 2012 IEEE 62nd, pp. 787-793.
- M. Reiche, G. Wagner, "Wafer thinning: techniques for ultra-thin wafers," Advanced Packaging, March 2003.
- I. Zarudi, L. Zhang, "Subsurface damage in single-crystal silicon due to grinding and polishing," Jour. of Materials Science Letters, 15 (1996) pp. 586-587.
- N. Watanabe, T. Miyazaki, M Aoyagi, K. Yoshikawa, "Damage evaluation of wet-chemical silicon-wafer thinning process," 3D Systems Integration Conf., 2011, IEEE, Jan. 31, 2012.
- L. Mauer, J. Taddei, R. Youssef, "The role of wet etching in silicon wafer thinning," Compound Semiconductor, 2009.
- L. Mauer, J. Taddei, R. Youssef, "Silicon wafer thinning to reveal Cu TSV," IMAPS Conf., Fountain Hills, AZ, March 2012.
- S. Olson, K. Hummler, "TSV reveal etch for 3D integration," 3D Systems Integration Conf., 2011, IEEE, pp. 1-4, Jan. 31, 2012.
- Ibid.

# Inspection and metrology in the tape-and-reel process

By Carl Truyens, Piet Kerckhove [KLA-Tencor]

**A**s the final step in the semiconductor packaging process, an inadequate tape-and-reel process can substantially affect yield and a manufacturer's bottom line. Once the package has been fully assembled and passed functional test, scrapping a package at this stage is most costly. Maximizing yield becomes of the essence and dictates the need for high accuracy inspection and defect detection. At the same time IC packagers are being confronted with steep ramps driven by an unprecedented rise in consumer demand for mobile products (**Figure 1**). Recent improvements in screening capability to minimize over-rejection while still capturing critical defects, handling reliability, speed and cost-efficiency are being introduced to meet this demand.

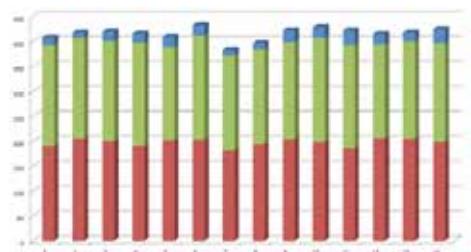


**Figure 1:** iPhone production ramps (courtesy of <http://www.asymco.com/>).

## Mobile products in a high-volume manufacturing environment

The dynamic consumer smartphone market is straining the IC packaging supply chain as never seen before. The product life cycle of a smartphone is shortening and the IC packages that need to be supplied to support a smartphone

generation have very high volume peaks. This creates unprecedented ramps for the IC packaging unit supply chain. The T640 platform has specifically been designed to address this need. Featuring a dual independent taper at a maximum speed of 25k UPH, the T640 has proven capable of reaching 400,000 units output per day consistently (**Figure 2**).



**Figure 2:** T640 daily output (y-axis) achieved over a two week period (x-axis).

To be able to achieve 400,000 units per day output while being confronted with a wide variety of input and output media suppliers, carefully selected to bring down material costs, it is clear that tape-and-reel equipment had to be improved with respect to handling reliability. Next-generation taping technology to cope with such wide product and material variety was introduced on the platform.

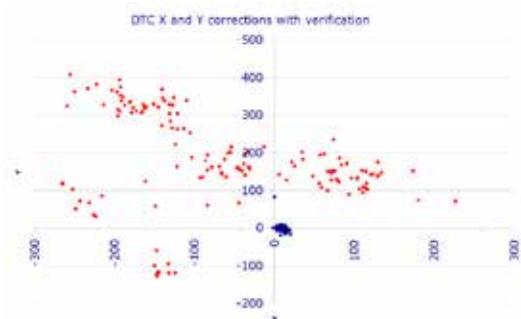
One example of such next-generation technology relies on dynamic tray compensation (DTC). DTC is a proprietary technology, that ensures centered device pick up and handling reliability. Inherent to the technology is vision guidance, which measures each incoming tray and tape to enable correct placement of IC packages in real time without negatively affecting

taping output per day. It has proven to be a key enabler for handling 2x2mm<sup>2</sup> packages with tray-based input, a rising need as bowl feeders have been proven to damage sensitive units such as MEMS. These 2x2mm<sup>2</sup> packages were previously thought incapable of being handled in tray-based media—doing so meant a breakthrough in the MEMS IC packaging industry.

The effectiveness of DTC is shown in **Figure 3**. Red dots represent the absolute pocket positions in X and Y for different trays of the same type – variations commonly encountered in real life production environments.

Blue dots represent the pocket positions when corrected by DTC. A 96% reduction in handling uncertainty was achieved, ensuring centered device pickup and accurate placement in tape.

Another example of next-generation taping technology focuses on flexibility. To optimally support tray-to-tray and tray-to-tape operations, the T640 features a compact tray unit. The design has an input, all pass and reject lane. Optionally, the reject lane can be equipped with two separate reject trays of the JEDEC format. Tray-to-



**Figure 3:** Increase in handling reliability by DTC (measurements in microns).

tape operations combine the tray-side scanning capability with an independent dual taper, providing the flexibility to alternate both tray-to-tray and tray-to-tape operations with minimal loss of productivity. In today's high product-mix environment the dual taper can be equipped with an optional motorized track conversion (MTC).

Taper changeovers have often proved cumbersome because of the requirement for manual adjustments on the positioning of the track and seal shoes (**Figure 4**). These manual



**Figure 4:** Automated MTC changeover using different specifications on seal line positions.

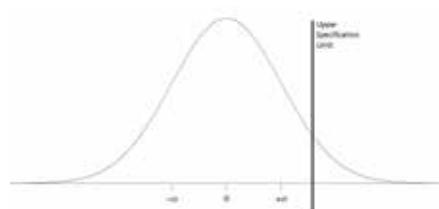
adjustments left room for changeover errors, positioning inaccuracy and potential costly customer returns. Eliminating any room for error, MTC fully automates adjustments of seal shoe and track positions, which can now be programmed into the inspection and handling recipe. When an operator loads the batch or scans a lot traveler card, the taper changeover will be initiated automatically without the need for tools or a technician to attend the taper tool. Following the changeover sequence, an operator immediately proceeds with loading material at minimal loss of productivity.

### Increasing inspection and metrology

Besides cost, there's one recurring theme for IC packages in mobile products: form factor. By definition, the mobile products in which these packages are used, need to fit in end users' pockets. ICs shrink, get faster and less power hungry. At the same time, less space remains in the contemporary

smartphone, thereby driving IC packages to become smaller and thinner.

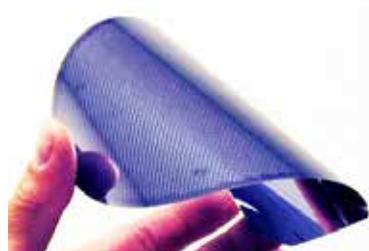
This form factor challenge has rather far reaching implications on metrology. Upper control levels (USL) on total IC package height are being scrutinized and tightened closer to packaging process capabilities (**Figure 5**). To ensure maximum yield, the requirements on accuracy and repeatability for



**Figure 5:** IC package height distribution close to USL.

inspection need to be tightened as well. Total IC package height can optionally be measured on T640 with a capability reaching below 10µm accuracy. The IC package height definition as described

## VORTEX WAFER HANDLING SOLUTION STANDARD AND THIN WAFER SORTING/PACKING



**PRELUDE  
W A F E R  
P A C K I N G  
S Y S T E M**  
Packs/unpacks  
both thin and  
standard wafers



\* For 4"~12", 50 to 800 µm wafers; warped, bumped or perforated

\* Non-contact vortex end effector equipped with Quartet's proprietary Soft Touch mechanism that ensures safe handling of wafers without damage, shift, or rotation

\* Packing/sorting tools, vortex end effectors and manual wands for thin wafer handling available

**Quartet  
MECHANICS**

For datasheet, please contact [inquiry@quartetmechanics.com](mailto:inquiry@quartetmechanics.com) | [www.quartetmechanics.com](http://www.quartetmechanics.com)  
P +1.408.200.8345 | F +1.408.200.8341 | 2343 Bering Drive, San Jose, CA 95131, USA

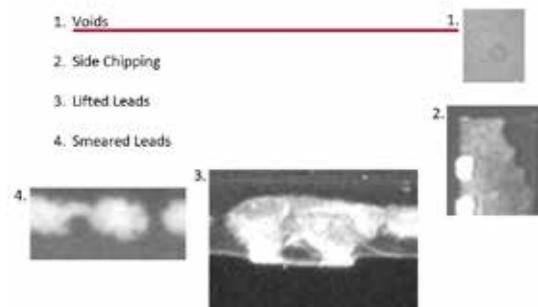
by JEDEC “mounting height” in ref. #1 [1] is used. This definition includes an element of IC package height variations induced by package warpage, which can be a significant contributor to total IC package height variations for these ultra-slim designed packages. For a good read on the maximum permissible warpage, the authors suggest ref. #2 [2].

Besides metrology, defect inspection also gets increased attention. Thinner dies in combination with thinner flip-chip substrates introduce new defect inspection requirements on bare die products. Silicon micro-crack detection at 100% sampling rate and HVM speeds are becoming the norm instead of the exception. Combining these added defect inspection requirements with an effective taper platform is asking for a technological revolution rather than an evolutionary change, typical of the past few years.

Because sub-micron silicon die crack detection is now required, an extension emerged to the widely used advanced package visual inspection (aPVI™) capability. The latter was first introduced to replace manual inspection by automated optical inspection (AOI). While aPVI™ has proven capability on defect catalogs containing a broad variety of defects of interest (DOI), the more recent xCrack™ technology has proven to excel on silicon micro-crack detection (Figure 6) making both capabilities complementary. The new technology also allows detection of

silicon die micro-cracks down to  $0.7\mu\text{m}$  in width at a throughput of 10,000 units per hour.

In consideration of the other side of the packaging scale, where we find quad-flat no-leads packaging (QFN) sensitive to side defects during the singulation process, typical defects to be binned as rejects are displayed in Figure 7. The main challenge with side inspection has always been that implementation typically came at a large loss of throughput/productivity. Because QFNs are on the low-end of the packaging scale, it was not economically viable to implement in practice. Instead,



**Figure 7:** QFN side defects of interest.

the high-speed QFN5S side inspection option on the T640 brings the capability below this cost-of-ownership threshold as it supports HVM throughput of up to 20,000 units per hour. ☺

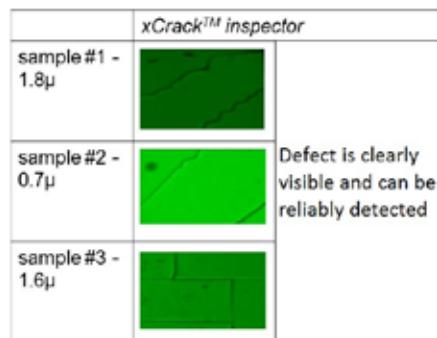
## References

1. JEDEC STANDARD 95 Page 4.17-16/A.
2. JEITA ED-7306: Measurement methods of package warpage at elevated temperature and the maximum permissible warpage.

## Biographies

Piet Kerckhove received his MSc in Electrical Engineering from U. Gent, Belgium and is a Product Marketing Manager at KLA-Tencor; email Piet.Kerckhove@KLA-Tencor.com

Carl Truyens received his MSc in Electro-Mechanical Engineering from U. Leuven, Belgium, and an MSc in Electrical Engineering from Stanford U. He is Sr. Marketing Director at KLA-Tencor.



**Figure 6:** xCrack™ vs. aPVI™ Silicon micro-crack detectability.

## STATEMENT OF OWNERSHIP, MANAGEMENT AND CIRCULATION

1	Publication Title: Chip Scale Review		
2	Publication Number: 1526-1344		
3	Filing Date: 10/04/13		
4	Issue Frequency: Bi-Monthly		
5	Number of Issues Published Annually: 6		
6	Annual Subscription Price: \$95/Year		
7	Mailing Address of Known Office of Publication: 1018 Hazel Avenue, Campbell, CA 95008 Contact Person: Kim Newman, 408.429.8585		
8	Mailing Address of Headquarters: Same as above		
9	Publisher: Kim Newman P.O.Box 9522, San Jose, CA 95157-0522 Editor: Debra Vogler 74-478 Hwy 111 #363 Palm Desert, CA 92260		
10	Owner: Haley Publishing Inc., P.O. Box 9522 San Jose, CA 95157-0522		
11	Known Bondholders, Mortgagors and Other Security Holders Owning or Holding 1 Percent or More of Total Amount of Bonds, Mortgages or Other Securities: None		
12	Tax Status: Has not changed during preceding 12 months		
13	Publication Title: Chip Scale Review		
14	Issue Date for Circulation Data Below: September - October 2013		
15	Extent and Nature of Publication	Average No. Copies Each Issue During Preceding 12 Months to Filing Date	No. Copies of Single Issue Published Nearest to Filing Date
a.	Total Number of Copies (Net Press Run)	15,732	15,500
b.	Paid and/or Requested Circulation	14,274	14,173
1	Paid Requested Outside-County Mail Subscriptions on Form 3541	0	0
2	Paid In-County Subscriptions (Form 3541)	0	0
3	Sales Through Dealers and Carriers, Street Vendors, Counter Sales and Other Non USPS Paid Distribution	0	0
4	Other Classes Mailed Through the USPS		
c.	Total Paid and/or Requested Circulation	14,274	14,173
d.	Free Distribution by Mail		
1	Outside-County (on Form 3541)	0	0
2	In-County (on Form 3541)	0	0
3	Other Classes Mailed Through the USPS	0	0
e.	Free Distribution Outside the Mail	1,385	1,226
f.	Total Free Distribution (Sum of 15d and 15e)	1,385	1,226
g.	Total Distribution (Sum of 15c and 15f)	15,659	15,399
h.	Copies Not Distributed	224	174
i.	Total (Sum of 15g and h)	15,883	15,573
j.	Percent Paid and/or Requested Circulation (15c divided by 15G times 100)	91.16	92.04
16	This Statement of Ownership will be printed in the November - December 2013 issue of this publication.		
17	Signature and title of owner and publisher Kim Newman, Publisher <i>Kim Newman</i>		
I certify that all information furnished on this form is true and complete. I understand that anyone who furnishes false or misleading information on this form or who omits material or information requested on the form may be subject to criminal sanctions (including fines and imprisonment) and/or civil sanctions (including civil penalties).			



## Diagnosing component failures often requires a system-level approach

by Paul Sakamoto, Contributing Editor

**D**evice complexity, functional partitioning, exotic materials, and high performance requirements that result in the lack of a specification guard band are a few of the issues driving component failure analysis (FA) to include system-level investigation. As an industry, we are familiar with the progression of complexity and performance, but what about partitioning and materials issues? A simple example of an issue involving partitioning is a radio frequency (RF) device. Whether it is a Bluetooth port, or the latest cellular radio format, the final system installation and packaging will affect the operation of the device differently than does the manufacturing test. The antenna and other loads are usually contained in the system, not the chip, and will always be subtly different than the test interface in manufacturing.

The most efficient approach to a complete FA flow from system to component would be to keep the whole project under one roof. This is most often seen in large companies. Although they likely use some outsourced labs in their work, the majority of issues can be handled in-house with their vast resources and amortized over their many products. Even for billion dollar companies, the cost of a full FA lab that reaches from system to the guts of an IC is often too high. Usually, smaller companies have to be general contractors that job out almost all parts of the FA task to various labs. This approach works, but it is usually slower due to communication and prioritization overhead. As a result, customers are driving the independent analytical labs to expand their services to yield complete analyses in a shorter time. One example

of this development is Evans Analytical Group (EAG), which announced its “Electronics System Failure Analysis” practice in October of this year. The company created a business practice around the technical resources it has been building over the years to service customer demands for system-level FA. It is probably a harbinger of things to come in the test and FA lab world. EAG has been a big driver of consolidation in the FA lab space and it seems likely that this will cause other labs to join forces to combine and give a similar offering.

According to Aram Sarkissian, GM of the Microelectronics Test and Engineering Division at EAG, as electronics systems become smaller, more complex, and more deeply embedded in our daily lives, the cost of failure has risen exponentially. The company’s failure analysis offering includes both electrical testing and materials characterization and uses the latest high-resolution imaging and electrical localization tools. These capabilities are increasingly important given the growing complexity of electronics systems, rapid pace of miniaturization, special characteristics of advanced technology processes, intermittent nature of system malfunctions, and challenges associated with the exotic materials used to design and manufacture today’s components.

Semiconductor component failure analysis is still one of the larger businesses at EAG. When the investigation narrows down to the component level, the company’s engineers have access to a full list of capital-intensive equipment, which includes X-ray, optical microscopy, laser microscopy, automatic test equipment

(ATE), focused ion beam (FIB) and tunneling electron microscope (TEM), at the junction level. An example of what has become a typical FA case is the marginal solder connection shown in **Figure 1**. Some of this equipment is so expensive that only the largest IC manufacturers have their own labs so equipped. “Most of the sub-billion dollar semiconductor companies do a substantial portion of their FA business with us,” said Taqi Mohiuddin, EAG’s Senior Director of Marketing. “Not only do they avoid the need to fully utilize an expensive piece of gear, but we have engineers on staff who do these jobs full-time and therefore are uniquely experienced.”

EAG announced its system FA services on October 8th of this year. It will be interesting to see how soon others follow with similar offerings. ☈



**Figure 1:** The photo shows a cross section of a pair of non-wetting solder bumps. The poor solder interface was the root cause of a marginal failure in the stacked packages. Several levels of prior investigation involving system-level test, ATE, optical and X-ray examination, were required to get to this pinpoint failure source. (Photo courtesy of EAG.)

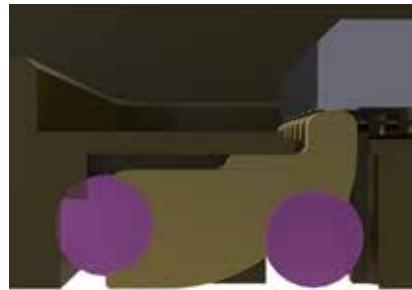
# Field-driven test contacting solution

Shamal Mundiyath *[JF Microtechnology Sdn Bhd]*

## I

In today's semiconductor industry, test technology is improving and moving forward dramatically. With the continuous increase of market needs and complexities, the problem of integrated circuit (IC) testing has become much more challenging and needs an economic solution with reliable and sustainable performance. Various analyses (internal and in conjunction with end users as well as [1]) on test field challenges and customer "pains" revealed that a solution addressing current issues must be designed.

The main objectives of any production test are to be able to rely on test data and not spend time on repetitive tests, and to avoid test failures. To determine the contact resistance of a rigid pin, we need to understand the internal mechanics of the pin assembly as well as the resistance network that allows the flow of current. A new rigid contactor called Zigma (**Figure 1**), which utilizes short wipe stroke (SWS) technology, enables various plated devices to test millions of insertions. This new design addresses the false failure



**Figure 1:** Zigma pin with front and back elastomer.

phenomenon in final production test by virtue of its having increased co-planarity between the front and back elastomer configuration (**Figure 1**). When assembled

with an increased pre-tension, the back elastomer is compressed to the operating height that will accommodate standard pad height variations on the target PCB. Similarly, on the top side, the device compresses the front elastomer to its operating height to accommodate the device's co-planarity. In this compressed state, the tips of the pin penetrate through the layer of oxides of tin on the device under test (DUT) allowing current to flow through the advanced profile. Because the device has wide co-planarity, not all of the pins available in the test industry market today are compressed to exactly the operating height. If the plungers are not compressed to the same operating height, the engagement to the device pads will be different, which in turn results in a large variation in contact resistance. This enhanced feature allows production workers to test and verify without multiple repeat testing.

It is also the contactor designer's duty to ensure that the lifetime of the DUT boards is not compromised, which is one of the most discussed issues in the test industry. The new technology on the contactor surface with its advanced contact finish (ACF) (**Figure 2**) and motion dynamics ensures that the DUT board, even after millions of cycles of insertions, is not degraded.

## Development objectives

There are several factors that need to be taken into account in highlighting product configuration for various plated device applications: first is the contact pin profile itself. A different device plating such as matte tin or NiPd/NiPdAu may require different contact profiles and motion dynamics. For



**Figure 2:** Zigma pin with ACF-advanced contact finish.

matte tin, the contact pin needs to break through the oxides, maintain an effective wipe action, and provide good contact resistance readings.

A second factor is the contact force. The amount of contact force needs to be compatible with the type of plating. For example, the force required for matte tin is different from that required for NiPd-plated devices. Because of the greater hardness of NiPd and prolonged plunger force, the contact tip wears prematurely. Zigma does not use its housing body as a tail end stopper. Instead, the rear elastomer is used as the tail stopper, which helps to dissipate the pressure that builds up at the contact tip and DUT board. This scheme increases the life span of the contact pin.

A third factor is the surface roughness—a key parameter. Contact pins that have a rough surface will tend to fill up with solder material when used with tin-plated devices. A smoother surface will tend to keep the contact tip clean with minimal tin migration. Having a smoother, softer gold finish on the contact will also reduce chafing when in contact with the gold plating of the load board.

## Packaging considerations

Packaging has a number of influences on test methods, one of which is the issue of sawn vs. punched packages for high-frequency devices: one type with burr-free smooth edges; the other with “ragged” edges. Because of tolerance factors on the alignment pocket opening and the DUT, the sharp burrs from the sawn packages hit the contact tip of the pin and get dislodged from the DUT when exposed to vibrations. This situation causes severe damage to the contact tip up. Additionally, the burr particle that falls on the DUT board has a “sand paper” effect leaving the board severely damaged. With the help of SWS technology, the contact tip is placed further inside of the device pad edge, thereby avoiding the sharp burrs that occur with sawn packages. The result is less contamination formation and debris collection and increased pin contact life.

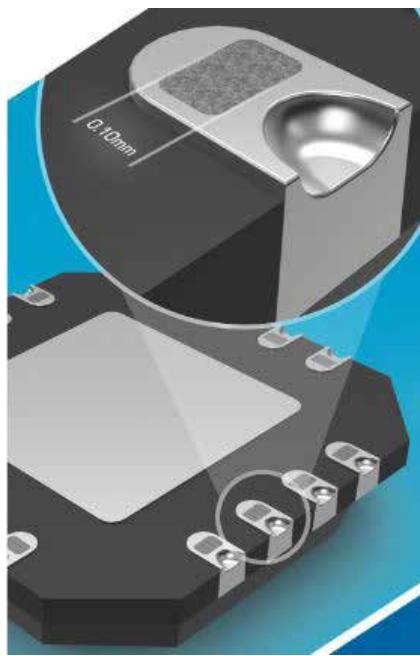


Figure 3: Wettable flank/dimple pad device.

Trends in packaging such as dimple pads/wettable flank (**Figure 3**), corner chamfer pads (**Figure 4**), and short pads are becoming increasingly popular. It is therefore becoming highly challenging to test with the rigid contact solutions currently available as the pad length

needed to make a good scrub exceeds the wipe length, thereby resulting in contact failure. A potential test challenge now facing the industry is the use of devices with corner chamfer pads as shown in **Figure 4**. For such pads, the available pad length is 0.2mm maximum, where the scrubbing should take place without smearing the pads to the die, which will result in either a test failure or a quality rejection. The SWS technology addresses this issue by providing a good wipe length of  $\leq 0.10\text{mm}$  that will land well inside the very short pads of the devices.

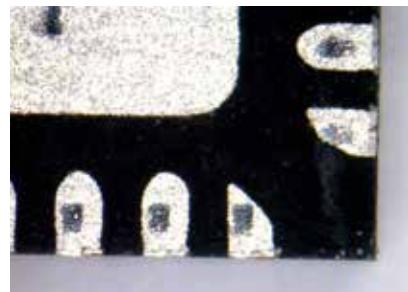


Figure 4: Corner chamfer pads.

## Summary

A new contacting solution is designed to meet several of the most challenging issues facing semiconductor test. The new design provides sustainable performance in terms of less cleaning, reduced cost-of-test, longer MTBA/MTBR, higher overall equipment efficiency (OEE), and high first-pass yield.

## References

1. “The future is the interconnect: IITC,” online, cited Aug. 10, 2012; <http://www.monolithic3d.com/2/category/tsv/1.html>

## Biography

Shamal Mundiyath received his MSc in Engineering and Manufacturing Management from Coventry U. MSRSAS and is Head of the Department-Engineering at JF Microtechnology Sdn Bhd; email [shamal.mundi@jftech.com.my](mailto:shamal.mundi@jftech.com.my)

The advertisement for nanium features a blue header with the company name "nanium" and a stylized molecular structure logo. Below this, the text "Semiconductor Packaging, Assembly and Test" is displayed in a bold, sans-serif font. In the center, the text "Leading Edge Fan-out WLP Technology eWLB" is shown above an image of a square chip with a grid of pads. To the right, the text "Design, Development, Engineering and Manufacturing Services" is listed. At the bottom, there is a photograph of a cleanroom environment where a person in a blue protective suit is working on a large piece of industrial equipment. The website address "www.nanium.com" is prominently displayed at the bottom right.



# EXPAND YOUR BUSINESS WORLDWIDE



## Discover the Power of SEMI® Global Expositions

Whether you are looking to explore new regions, technologies, or markets, SEMI Expositions are the ideal platform to showcase your brand, connect to customers, and grow your business worldwide. Let SEMI help you build an exhibition and marketing program that gains maximum exposure and takes your business to the next level!

For the complete schedule of SEMI Expositions,  
visit [www.semiexpos.org](http://www.semiexpos.org)

## Upcoming SEMI Expositions

**SEMICON Japan 2013**  
December 4–6  
Chiba, Japan  
[www.semiconjapan.org](http://www.semiconjapan.org)

**SEMICON Korea 2014**  
February 12–14  
Seoul, Korea  
[www.semiconkorea.org](http://www.semiconkorea.org)

**LED Korea 2014**  
February 12–14  
Seoul, Korea  
[www.led-korea.org](http://www.led-korea.org)

**SEMICON China 2014**  
March 18–20  
Shanghai, China  
[www.semiconchina.org](http://www.semiconchina.org)

**FPD China 2014**  
March 18–20  
Shanghai, China  
[www.fpdchina.org](http://www.fpdchina.org)

**SEMICON Singapore 2014**  
April 23–25  
Singapore  
[www.semiconsingapore.org](http://www.semiconsingapore.org)

**SEMICON Russia 2014**  
May 14–15  
Moscow, Russia  
[www.semiconrussia.org](http://www.semiconrussia.org)

**SEMICON West 2014**  
July 8–10  
San Francisco, USA  
[www.semiconwest.org](http://www.semiconwest.org)

**SEMICON Taiwan 2014**  
September 3–5  
Taipei, Taiwan  
[www.semicontaiwan.org](http://www.semicontaiwan.org)

**SEMICON Europa 2014**  
October 7–9  
Grenoble, France  
[www.semiconeuropa.org](http://www.semiconeuropa.org)

**PE 2014 Exhibition  
and Conference**  
October 7–9  
Grenoble, France  
[www.plastic-electronics.org](http://www.plastic-electronics.org)

# Product News

## Dow Introduces SOLDERON Tin-Silver Plating Chemistry for Lead-Free Bumping

Dow Electronic Materials introduced SOLDERON™ BP TS 6000 tin-silver plating chemistry for use in lead-free bumping applications. Improved features include enhanced plating performance, bath stability and ease-of-use. The company claims this next-generation formulation enables the industry's widest process window with the most robust process flexibility and a competitive cost of ownership (COO).

"As flip chip packages become mainstream and the industry continues to move toward 2.5D and 3D packaging technologies, there is a clear market requirement for high-performance lead-free alternatives for plating applications," said Dr. Robert Kavanagh, global business director, Advanced Packaging Metallization, for Dow Electronic Materials. "Customers need materials optimized for today's finer bump geometries. This new chemistry achieves significant performance improvements, delivering even faster plating speeds, better uniformity and smoother surface morphology in addition to a smooth, void-free interface when used together with Dow's and other leading copper (Cu) pillar formulations."

With a single formulation, SOLDERON BP TS 6000 Tin-Silver (SnAg) is said to be capable of plating speeds ranging from 2 to 9  $\mu\text{m}/\text{min}$ ., which reportedly creates a significantly wider operating window when compared with other solutions in the marketplace. The tunable nature of the Ag composition in this formulation makes it suitable for a number of applications and eliminates the need to change the chemistry to address different processing requirements. The chemistry has proven to be robust enough for both bumping and capping of a wide range of patterned wafers and it is not restricted for use with specific photoresists. It exhibits with-in die

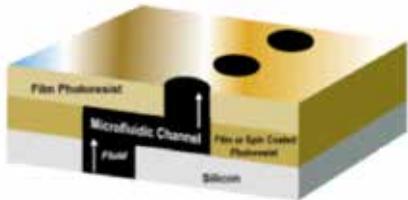
(WID) uniformity after reflow of <5% over a wide range of wafer types, which demonstrates its suitability for high-volume manufacturing. Additionally, it is macro- and micro-void free after reflow for improved yields and reliability.

"One of the most compelling strengths of SOLDERON BP TS 6000 Tin-Silver is the product's enormous flexibility, which allows it to perform exceptionally well in a variety of applications from in-via and mushroom bumping to Cu and micro-Cu pillar capping," added Kavanagh.

SOLDERON BP TS 6000 Tin-Silver plating bath has proven to be both electrolytically and thermally stable, which contributes to the chemistry's competitive COO. Offering an electrolytic bathlife of >100 Ah/L and a ≥6-month pot life, it is compatible with in-line metrology processes. Samples are currently available and in beta testing with multiple customers.

**Engineered Materials Systems Debuted its Dry Film Negative Photoresists at IWLPC 2013**

Engineered Materials Systems, Inc., global supplier of negative photoresist materials for MEMS and IC cooling, introduced its DF-2000 Series Dry Film Negative Photoresists optimized for hot roll lamination and



processing on MEMS and IC wafers.

The films were developed for consistent photo speeds with +/- 3% critical dimension targets and are available in various thickness formats from 5 to 50  $\mu\text{m}$ , +/- 5%. The cured chemistry can reportedly withstand harsh environments including resistance to extreme moisture conditions and corrosive chemicals. The DF-2000 series films are said to be less brittle than most available negative photoresists with a glass transition temperature of 145°C (by DMA Tan Delta) and a moderate

**HCD**

820A Kifer Road,  
Sunnyvale, CA 94086  
(408) 743-9700 x331  
[www.hcdcorp.com](http://www.hcdcorp.com)  
ISO 9001:2008 Certified

Board-to-Board      Package-to-Board      Board-to-Flex

**Featuring HCD Patented SuperButton® and SuperSpring® Contact Elements incorporated into socket and interposer solutions for prototyping, validation, space transformer, and test applications.**

Coming soon to a show near you:

DesignCon  
January 29-30  
Santa Clara, CA

BiTS  
March 4-5  
Mesa, AZ

**HIGH CONNECTION DENSITY, INC.**

*"Our Proprietary Technology,  
Your Competitive Advantage"*

Copyright © 2013 High Connection Density, Inc. All rights reserved. Information is subject to change without notice.  
"SuperSpring" and "SuperButton" are trademarks of High Connection Density, Inc.

# Product News

modulus of 4.5 GPa at 25°C. The cured chemistry is hydrophobic, providing for chemical and moisture resistance. DF-2000 series films are compatible with and can be used in contact with the EMS line of spin-coatable photoresists.

## Plasma-Therm Launches Plasma-based Die-singulation System

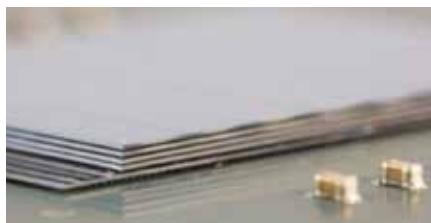
Plasma-Therm launched its MicroDieSingulator (MDS) systems, intended to deliver plasma-based singulation of semiconductor dies from 4-, 6-, and 8-inch wafers mounted on industry-standard tape frames. By using energized plasma, rather than mechanical saws or lasers to dice wafers, the MDS system singulates individual die, leaving streets of 20µm or less — reportedly far smaller than most existing equipment can achieve.

Reducing street size maximizes valuable silicon real estate. Additionally, Plasma-Therm's exclusive MicroDieSingulator technology separates die without causing lateral damage from stress-induced cracking, overheating, or re-deposition of ablated material. Scanning-electron microscope (SEM) images confirm that the process produces separated dies with smooth, vertical sidewalls.

Implementing MDS systems reportedly increases throughput in terms of more wafer-per-hour and die-per-wafer. Additionally, dies are less likely to be chipped during separation and less prone to fracture during packaging.

"With its plasma-based process, MDS outperforms mechanical saws and laser cutting tool," said Ed Ostan, Executive VP marketing, Plasma-Therm. "In addition, IC designers gain the freedom to utilize thinner wafers, design smaller streets, and even create non-rectangular streets and dies." MDS-100 systems are equipped for high-volume production, with automated, tape-frame cassette transfer stations.

## Micron Technology Ships First Samples of Hybrid Memory Cube



Taking a dramatic step forward in memory technology, Micron Technology reports it began shipping engineering samples of the world's first engineering samples of its 2GB Hybrid Memory Cube (HMC) to lead customers. HMC is designed for applications requiring high-bandwidth access to memory, including data packet processing, data packet buffering or storage, and computing applications such as processor accelerators. Micron expects future generations of HMC to migrate to consumer applications within three to five years.

An industry breakthrough, HMC uses advanced through-silicon vias (TSVs) to combine high-performance logic with Micron's state-of-the-art DRAM. Micron's HMC features a 2GB memory cube that is composed of a stack of four 4Gb DRAM die. The solution is said to provide 160 GB/s of memory bandwidth while reportedly using up to 70% less energy per bit than existing technologies.

"The Hybrid Memory Cube is a smart fix that breaks with the industry's past approaches and opens up new possibilities," said Jim Handy, a memory analyst at Objective Analysis. "Although DRAM internal bandwidth has been increasing exponentially, along with logic's thirst for data, current options offer limited processor-to-memory bandwidth and consume significant power. HMC is an exciting alternative."

HMC's abstracted memory is expected to enable designers to devote more

time to leveraging its features and performance and less time to navigating the multitude of memory parameters required to implement basic functions. It also manages error correction, resiliency, refresh, and other parameters exacerbated by memory process variation.

"System designers are looking for new memory system designs to support increased demand for bandwidth, density, and power efficiency," said Brian Shirley, vice president of Micron's DRAM Solutions Group. "HMC represents the new standard in memory performance; it's the breakthrough our customers have been waiting for."

Micron expects 4GB HMC engineering samples to be available in early 2014 with volume production of both the 2GB and 4GB HMC devices beginning later in 2014.

## Aries Electronics Announces Probes On 0.2MM Pitch



Aries Electronics, a US manufacturer of standard, programmed and custom interconnection products and test sockets used worldwide, announces its latest addition to its socket spring probe repertoire with new probes capable of contacting devices on 0.2mm pitch.

These new probes enable socketing (for test and burn-in applications) for many new device packages and bare-die

being designed and made on this pitch. The contact and spring material are gold plated beryllium-copper. The probes are available with either a pointed -tip or crown-shaped termination.

These new probes will yield >100k cycles over a temperature range of -55° to +150°C.. This performance makes these probes ideal for socketing for bench test or burn-in applications. In addition, these probes yield a very low inductance (~0.59nH) signal path making them compatible with testing RF devices at 10 Ghz and beyond. They require about 6g of compression to actuate and can be placed on a .004" diameter PCB pad.

These probes can be used with any of Aries standard molded AND machined CSP socket bodies. This enables the customer to use this socket on any new or previously existing test (or burn-in) board.

### Nusil Technology Presents Low Viscosity, Thermally Conductive Silicone Potting Elastomer

Silicone materials provider, NuSil Technology LLC introduced R-2165, a robust silicone solution intended to protect electronic components and systems such as sensors, relays, and connectors. Market growth in applications requiring silicone due to its excellent ability to perform at elevated temperatures inspired development of R-2165.

"R-2165 is the latest addition to NuSil's diverse portfolio of silicones designed for potting and encapsulating components in need of the high level of power required by many of today's applications, such as data centers and faster data transfer in general," said Bob

Umland, Marketing & Sales Director, Electronics and Engineering.

R-2165 joins NuSil's group of versatile silicone materials for potting and encapsulating that vary in appearance and thermal conductivity yet cure at room temperature. All of these materials are pourable, easy to process, and proven to increase the operation life of electrical components in harsh environments.

R-2165 is gray in color, pourable, and exhibits moderate thermal conductivity of 0.6 W/mK. Similar to its portfolio affiliates for this class of materials, it uses platinum addition cure chemistry, offering minimal shrinkage, no cure by-products, and a cure time that can be accelerated with heat.

WORLD'S PREMIER EVENT  
for what's  
**NOW & NEXT**  
in  
BURN-IN AND TEST OF PACKAGED ICs

Technical Program  
EXPO 2014  
Social Events

Sign up now for  
EXPO & SPONSORSHIPS

**BiTS**  
Burn-in & Test Strategies Workshop™

March 9-12, 2014  
MESA, ARIZONA

Now in its  
Fifteenth Year

Register Online at [BITSWORKSHOP.ORG](http://BITSWORKSHOP.ORG)



Chip Scale  
REVIEW



The Power of [Integration]



## European 3D TSV Summit

### Application Ready

#### EXHIBITION & CONFERENCE

January 20-22, 2014  
Grenoble (France)

The must-attend event focusing on 3D TSV and gathering the full supply chain. In 2013, the 1<sup>st</sup> edition reached 97% satisfaction rate and had more than 320 attendees from 20 countries.

European 3D TSV Summit 2014 features:

- 25 presentations of executives and experts
- Panel discussions & Market session
- 500 m<sup>2</sup> of Exhibition
- Pre-Summit Symposium on MEMS and TSV (NEW)
- One on one business meeting service
- CEA-LETI 300mm TSV line tour
- Cocktail and Networking Dinner



**Save the date. Join us.**

[www.semi.org/european3DTSSummit](http://www.semi.org/european3DTSSummit)  
Contact: Yann Guillou ([yguillou@semi.org](mailto:yguillou@semi.org))

#### ADVERTISER INDEX

<b>Amkor</b> <a href="http://www.amkor.com">www.amkor.com</a> .....	1
<b>Aries Electronics</b> <a href="http://www.arieselec.com">www.arieselec.com</a> .....	33
<b>ASE Group</b> <a href="http://www.aseglobal.com">www.aseglobal.com</a> .....	2
<b>BiTS</b> <a href="http://www.bitsworkshop.org">www.bitsworkshop.org</a> .....	55
<b>Contech Solutions</b> <a href="http://www.contechsolutions.com">www.contechsolutions.com</a> .....	41
<b>DL Technology</b> <a href="http://www.dltechnology.com">www.dltechnology.com</a> .....	21
<b>Emulation Technology</b> <a href="http://www.emulation.com">www.emulation.com</a> .....	37
<b>Essai</b> <a href="http://www.essai.com">www.essai.com</a> .....	IFC
<b>E-tec Interconnect</b> <a href="http://www.e-tec.com">www.e-tec.com</a> .....	20
<b>Everett Charles Technology</b> <a href="http://www.compliantconnector.com">www.compliantconnector.com</a> .....	43
<b>EV Group</b> <a href="http://www.evgroup.com">www.evgroup.com</a> .....	15
<b>HCD Corp</b> <a href="http://www.hcdcorp.com">www.hcdcorp.com</a> .....	53
<b>Honeywell</b> <a href="http://www.honeywell-radio.com">www.honeywell-radio.com</a> .....	5
<b>Indium Corporation</b> <a href="http://www.indium.us/E033">www.indium.us/E033</a> .....	39
<b>Ironwood Electronics</b> <a href="http://www.ironwoodelectronics.com">www.ironwoodelectronics.com</a> .....	31
<b>JF Microtechnology</b> <a href="http://www.jftech.com.my">www.jftech.com.my</a> .....	9
<b>Johnstech</b> <a href="http://www.johnstech.com/connected..">www.johnstech.com/connected..</a> .....	19
<b>KYEC</b> <a href="http://www.kyec.com">www.kyec.com</a> .....	13
<b>Micro Control</b> <a href="http://www.microcontrol.com">www.microcontrol.com</a> .....	3
<b>Nanium</b> <a href="http://www.nanium.com">www.nanium.com</a> .....	51
<b>Nordson Asymtek</b> <a href="http://www.nordsonasymtek.com/highaccuracy">www.nordsonasymtek.com/highaccuracy</a> .....	29
<b>Plasma Etch</b> <a href="http://www.plasmaetch.com">www.plasmaetch.com</a> .....	25
<b>Plastronics</b> <a href="http://www.plastronics.com">www.plastronics.com</a> .....	6
<b>Quartet Mechanics</b> <a href="http://www.quartetmechanics.com">www.quartetmechanics.com</a> .....	47
<b>Rudolph Technologies</b> <a href="http://www.rudolphtech.com">www.rudolphtech.com</a> .....	OBC
<b>SEMI</b> <a href="http://www.semiexpos.org">www.semiexpos.org</a> .....	52
<b>SEMI European 3D TSV Summit</b> <a href="http://www.semi.org/european3dtssummit">www.semi.org/european3dtssummit</a> .....	56
<b>Sensata</b> <a href="http://www.qinex.com">www.qinex.com</a> .....	IBC
<b>WinWay Technology</b> <a href="http://www.winwayglobal.com">www.winwayglobal.com</a> .....	17
<b>Zeiss</b> <a href="http://www.zeiss.com/xrm_electronics">www.zeiss.com/xrm_electronics</a> .....	27

#### ADVERTISING SALES

##### USA West, USA-North Central

**Kim Newman**

P.O. Box 9522 San Jose, CA 95157-0522  
T: 408.429.8585 F: 408.429.8605  
[ads@chipscalereview.com](mailto:ads@chipscalereview.com)

##### USA-East, USA-South Central

**Ron Molnar**

13801 S. 32nd Place Phoenix, AZ 85044  
T: 480.215.2654 F: 480.496.9451  
[rmolnar@chipscalereview.com](mailto:rmolnar@chipscalereview.com)

##### International

**Lawrence Michaels**

2259 Putter Court  
Brentwood, CA 94513  
T: 408.800.9243 F: 408.429.8605  
[lxm@chipscalereview.com](mailto:lxm@chipscalereview.com)

##### Korea

**Young J. Baek**

407 Jinyang Sangga, 120-3 Chungmuro 4 ga  
Chung-ku, Seoul, Korea 100-863  
T: +82.2.2273.4818  
[ymedia@chol.com](mailto:ymedia@chol.com)

# 40+ years of perfect pitch.



## And now, the perfect name



**Qi-nex [kuh-nekts]** 1. Over 40 years of reliable burn-in and custom connections; 2. Quality interconnects for **nex**-gen solutions.

Introducing Qinex, the new brand name for superior interconnection solutions from Sensata Technologies. Qinex, the new word in perfect pitch.

**QUALITY.** High-value interconnection solutions since 1970.

- 24/7 global engineering
- 24/7 global support teams
- Local engineering and sales
- Six Sigma quality management
- Proven, reliable high-volume manufacturing
- Expert molding, design, and customization

**INNOVATION.** More I/O choices, smaller form factors, superior performance in less time.

- Latest 3D design tools
- On-site model shops
- Rapid prototyping
- Advanced thermal analysis
- Design on demand
- Broad range of innovative contact designs



**PARTNERSHIP.** In a fierce global market, only Qinex reliably supports the innovation, reputation and competitiveness of your business. We'll work with you to get it right, the first time.

**40+ years of perfect pitch.  
And now, the perfect name.**

---

WEB [www.qinex.com](http://www.qinex.com)

EMAIL [qinex@sensata.com](mailto:qinex@sensata.com)

CALL **1-508-236-1306**





## Stepper redefined

### MEETING LITHOGRAPHY CHALLENGES HEAD-ON

- Large field of view (52mm x 66mm)
- 30 reticle library with four-reticle wheel
- On-the-fly auto focus for each exposure
- Warped wafer handling
- Superior depth of focus for thick resists
- Substrate and size flexibility  
(450mm, reconstituted wafers, square interposers, etc.)

Advancing Tomorrow's Technology



JetStep™ Advanced Packaging  
Lithography System

**RUDOLPH**  
TECHNOLOGIES

[www.rudolphtech.com](http://www.rudolphtech.com)