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R E V I E W

*The International Magazine for the Semiconductor Packaging Industry*

Volume 17, Number 5

September - October 2013

## Packaging Innovations: Graphene for Next-Generation Electronics Packaging

P. 20

- Acoustic Imaging & Inspection
- Metrology for Bumping Processes
- Wafer-to-Wafer Bonding for 3D ICs
- Thermocompression Bonding (TCB)
- Wafer-Level Fan-Out Packaging (WFOP)

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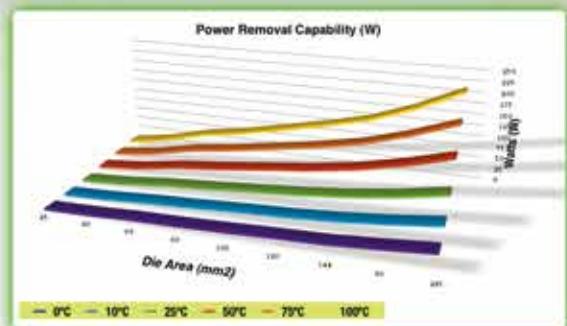
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September October 2013  
Volume 17, Number 5



The integration of different known good dies from different wafers, produced in different technologies and fulfilling different functions is best done by Fan-out Wafer Level Packaging technologies like eWLB. It enables the highest integration density, thinnest package, smallest die-to-die distance and shortest interconnections realized substrate-less by thin-film redistribution layer. The picture shows part of a reconstituted 300mm mold wafer with different dummy dies embedded.  
Source: Nantum S.A.

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REVIEW  
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*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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A scanning electron micrograph (SEM) showing a dense array of copper pillar microbumps. The pillars are raised, rounded structures with a distinct orange-yellow tint, likely due to the imaging process or the nature of the material. They are densely packed in a grid-like pattern across the field of view. In the bottom right corner of the image area, there is a dark green rectangular box containing text and a logo.

## Copper Pillar $\mu$ Bumps

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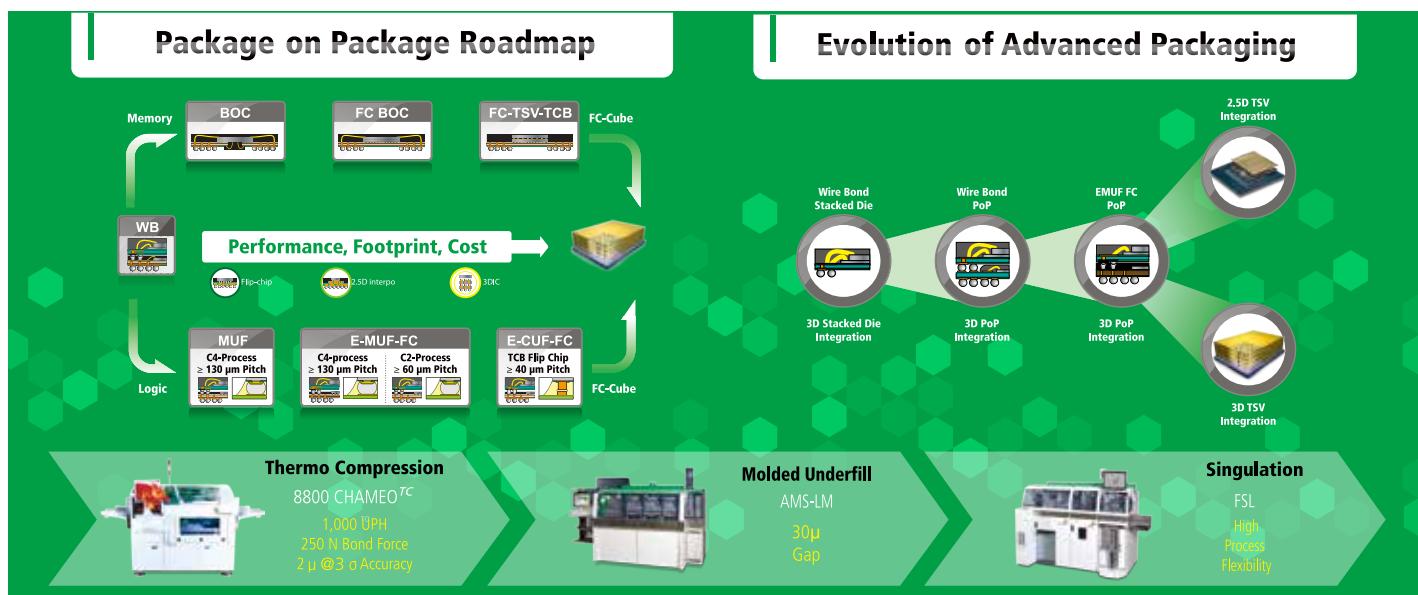
Besi has a broad portfolio of machine range that addresses all the assembly process steps involved in leadframe, substrate and wafer level packaging with applications in a wide range of end-user markets including electronics, computer, automotive, industrial, RFID, LED and solar energy.

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## Highlights

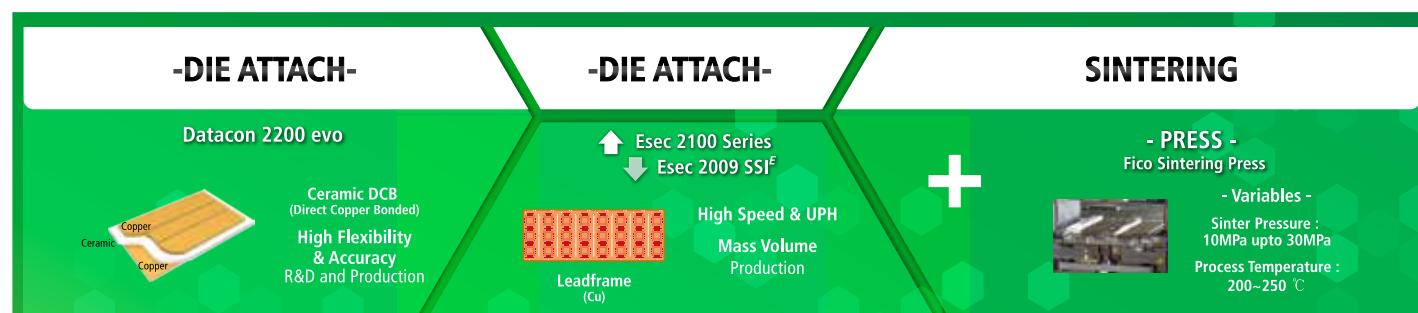
### Thermo Compression Meets Productivity

Thermo Compression Bonding is the breaking through technology for flip chip packaging of silicon based on < 28 nm nodes. It is also the enabling technology for TSV (through silicon via) for 2.5D and 3D integration.



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# FROM THE PUBLISHER



## A Major Milestone for IWLPC!

This year marks a major milestone as the 10th Anniversary for the International Wafer-Level Packaging Conference (Nov. 5-7, DoubleTree Hotel in San Jose, California). All sponsorships and the 50 exhibit spaces are sold out. Highlights will include the Keynote Breakfast Address with Paul Wesling (IEEE/CPMT), a 10th Anniversary Celebration Reception, an exclusive 3D Panel hosted by Invensas, plus two days where 50+ exhibitors will bring their top sales teams and executives to meet with prospective customers during the two days of exhibits.

There is an expo pass coupon for free access to the exhibits taking place Nov 6 & 7 located in the Industry News section on page 9. Take advantage of the Early Bird discounted rates in effect now through October 4. Visit [http://www.iwlpc.com/register\\_now.cfm](http://www.iwlpc.com/register_now.cfm) and register today!

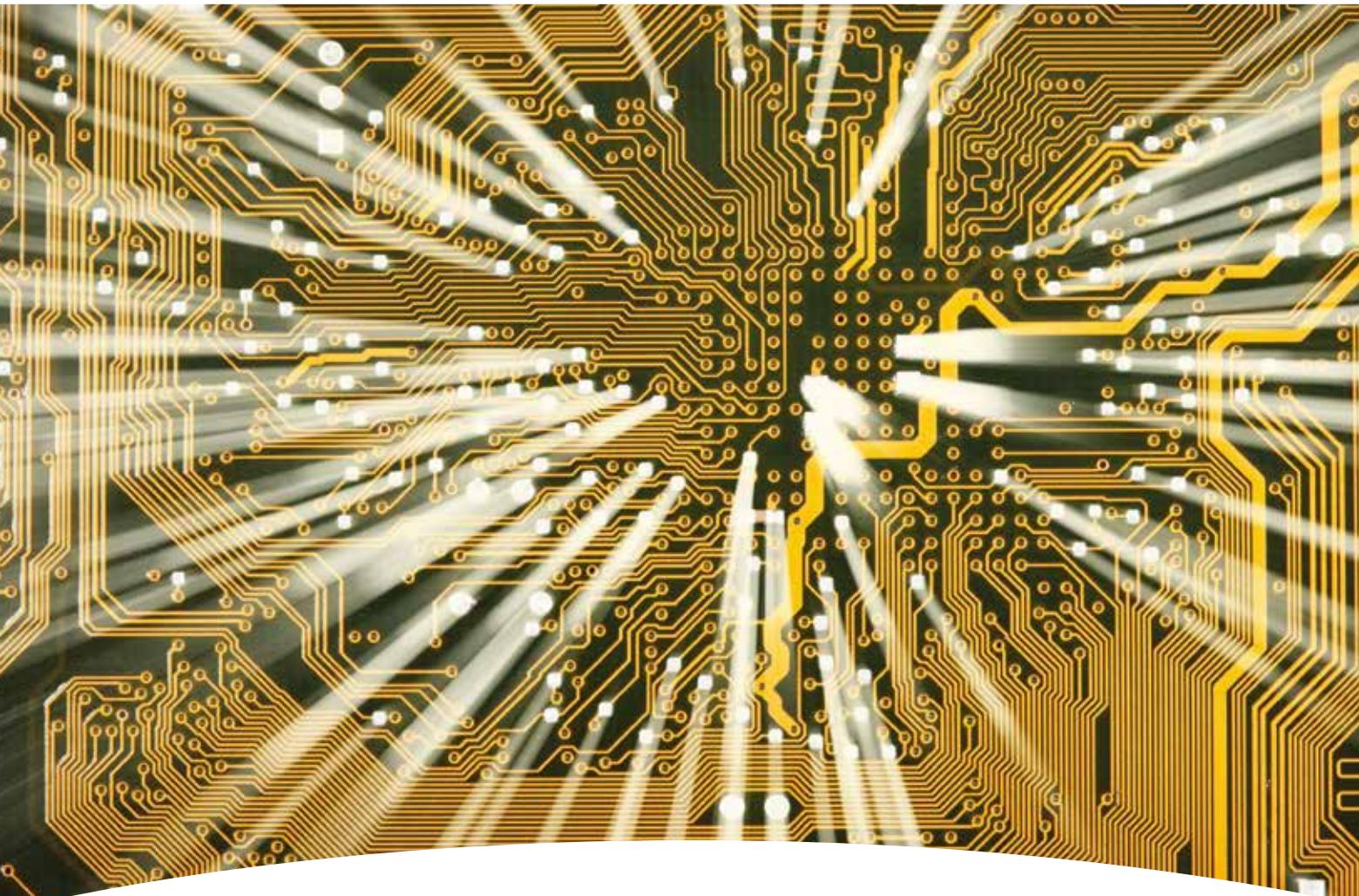
Many companies will also be attending IMAPS Microelectronic Symposium (Sept. 30 - Oct. 3, Orlando, Florida) or the SMTA International Conference (Oct. 13-17, Fort Worth, Texas). On the other side of the world, SEMI will be running SEMICON Europa (Oct. 8-10, Dresden, Germany). Pick up your copy of CSR during the events scheduled during this busy conference season. Visit the Nanium booth at Europa to pick up your copy, or look for it in the media bins at the show.

This issue brings a broad selection of editorial content to satisfy the industry's hunger for the latest developments in packaging technology. High on the list is the International Directory of Bonding Equipment for 2.5D & 3D Assembly teamed with an engaging article on thermocompression bonding. You won't want to miss the discussion of graphene for next-generation electronics packaging presented by the team at GE Global Research. Wafer Test is covered by ERS, the MEMS Packaging feature is co-authored by ePack Inc. and Hanking Electronics Ltd., Metrology for Bumping Processes is addressed by Rudolph Technologies, and Wafer-to-Wafer Bonding for 3D ICs is covered by Brewer Science. Dev Gupta of APSTL reviews TSV-based 3D technologies, and J-Devices contributes the latest on Wafer-Level Fan-Out Packaging.

Lastly, we welcome Lin (Leon) Tingyu to Chip Scale Review's Editorial Advisory Board. Leon received his PhD from the National University of Singapore and is currently a Senior Manager at the Institute of Microelectronics (IME) in Singapore. His expertise is in IC manufacturing processes including TSV/ TSI, Cu wire bonding, high power modules, thermal management, smartphone design and development, product mechanical reliability, module design (FOWLP), and product failure analysis. Welcome Leo!

*Kim Newman*  
Publisher

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# GUEST EDITORIAL

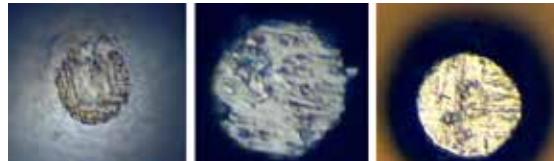
## Achieving First-Pass Test Success on Flip-Chip and Pillar Wafers

By Terence Collier [[CVInc.](#)]

**H**igh-density bumps have a higher propensity for entrapment of contaminants resulting in test failures of known good die. Bumps and pillars provide nesting sites for both surface and subsurface materials that are not typical of standard CMOS wafers.

Building a flip-chip or pillar wafer begins with the addition of a wet or dry resist to a standard CMOS wafer. The resist is processed and patterned in such a manner as to leave openings where a feature will be grown on the wafer. **Figure 1** shows an example of openings in liquid resist that have been spun on the wafer, baked, exposed and developed. While dry resist is applied and processed differently, the wafer will look similar prior to when the lithography process is complete. As a result, similar residues will be trapped on the wafer upon completion. While liquid resists are a bit easier to remove, the pillars and bumps themselves become traps for holding resist, plating and post-etch residues. Smaller form factor geometries add the additional difficulty of reduced bond strength. Where a large geometry feature has more surface adhesion for bond strength, this author has noted that smaller geometry features can be dislodged with the bump and pillars during the clean and saw operation.

If the debris remains and can be dislodged with saw coolant streams and spin rinse dryers (SRDs), probing can become a higher risk as well because probe needles might exert more force on individual bumps than either the saw or the SRD. Providing a wafer that is ready for probe and that simultaneously reduces the necessary force required for good electrical contact and high yield is a challenge.



**Figure 1:** From left to right: a) Original bump with debris, b) Probe tip after a few touchdowns, and c) Probed bump with debris transferred to the bump.

### The Good, the Bad, and the Dirty

The flip-chip process begins at the wafer fab where cleanliness is paramount. Particle-free wafers might still have thin layers of residues on the finished products. In the subsequent stages, those layers are removed so the wafers can be bumped or pilled. For the sake of simplicity and space, this paper will only review the liquid resist process. After wafers are received from the fab, they are prepped for bumping. To simplify, resist is spun on a wafer that has been coated with a seed layer of metal. The resist is processed through bake prior to alignment and exposure. Some resist brands require a post exposure bake after exposure, while others can proceed directly to develop. A descum might be prepared after develop to assure the openings in the resist are completely clear for bumping.

The clean and debris-free openings are the sites where either bumps or pillars will be formed. The next step wafer bumping involves electroplating the under-bump metallization (UBM) stack (or copper pillar) followed by solder bump (or caps for pillars). Next, the photoresist is removed to reveal UBM metal with an initial pillar of solder. This resist removal step is one of the two main contamination sources for bumped wafers. Even with the standard featureless and almost flat surface of a CMOS wafer, contaminants can become

adhered and trapped to the surface. These contaminants can be reaction by-products, residues, or particles, and easily adhere to the surface and cavities of small sub-micron topography.

Understanding that the features and trap sites on bumped wafers are orders of magnitude larger than the typical trap sites on standard CMOS wafers, it is easy to imagine the ease with which debris can be trapped. The surface of a CMOS wafer is typically passivation and aluminum. While the passivation is typically inert (oxides and nitrides), aluminum is a metal and provides a catalyst site for contaminants and corrosion. Aluminum is almost inert to backend processes, but serves as a catalyst for the new layers of Cu, Sn, Ag, Ti, and W, etc., providing for more complex contaminants. Adding resist and strippers for resist removal almost guarantees corrosion and contamination to the final product. The spaces in and around the pre-reflow solder and copper pillars also provide mechanical nesting sites for particles that would be typically lifted and carried away by gases and fluid transfer on a flat surface. Once the solder undergoes reflow, those same layers can now be chemically attached to the surface.

Reflow is assisted with flux and heat. Of course any material “heated” onto a surface is difficult to remove. While flux removers will remove most of the flux, the newly burned on carbon materials are almost impossible to remove. Those residual amounts of flux can be turned into polymers when the wafers are rinsed and dried in organic solvents. The reaction by-product and residual

process materials from resist processing, plating, stripping, ash by-products, and fluxing now support very difficult, if not impossible, layers to remove. The question remains: were metal oxides omitted? Neither organic solvents nor plasmas remove this native oxide that occurs on Cu, Sn, Pb or Ag. Flux will remove the metal oxides, but flux has to be removed, which promotes regrowth of metal oxide. How is this dilemma resolved? The answer is no oxide is ever completely removed in an oxygen-rich environment. Therefore, while one process removes a set of materials, it might exacerbate another problem.

## Test

Electrical test (probe) and assembly performance will be improved by removing native and non-native oxides, etch residues, photoresist and other debris deposits on the surface of bumps/pillars. Most commercial flux and wafer cleaners are moderately effective at removing organic contaminants, but not as effective against burned-on organic residue; most have very limited capability at removing metal oxides. Cleaning "ALL" residue is critical for stable test yield; proper oxide and residue removal improves probe card life and first pass test yield. For example, during "first pass" electrical test, either a sample or 100% of devices are electrically tested. Failures are grouped in bins as opens/shorts, functional and parametric fails. Some of the failures are due to contamination on the bump or probe card that contribute to high contact resistance (CRES) in the test circuit.

Metals have low bulk and surface resistance - typically less than 50 milliohms. The contact area, typically the surface of the bump plus the probe card tip, might have higher than normal surface resistance because of contaminants, oxidation and corrosion. CRES can increase the normally low resistance between the device under test (DUT) and the outside world by up to a few megohms. Since the electrical contact to the outside world is made

at this interface, contact resistance is a critical parameter. Increased CRES impedes electrical contact between the device and tester. Reducing CRES improves yield and extends the life of hardware and preventive maintenance costs.

As a result, CRES can be the root cause of open/shorts and some parametric fails. To recover those failures, a "second pass" and even "third pass" electrical test can be required. This author has seen some wafers have only a 30% success on first pass and subsequently require second and third pass testing to achieve 50% and 85%, respectively. Each probe pass picks a little debris from the bump that then adheres physically or chemically to the probe needles. So the probe needles pick a small amount of debris from the bumps with each pass, until false failures begin to occur.

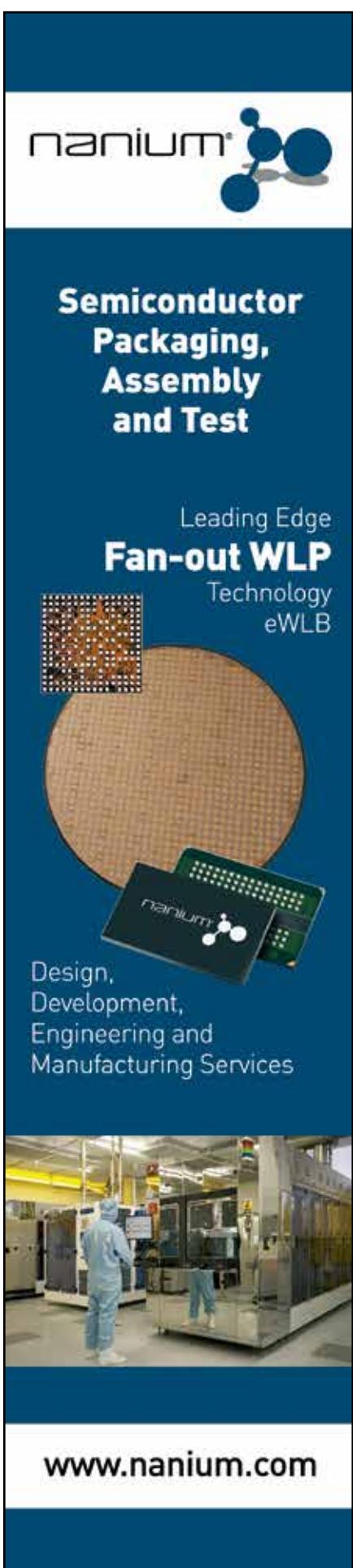
The needles can also deposit some of this debris onto the bumps. If the probe needle contacts a dirty surface, some small amount of material adheres to the surface of the probe tip. The vertical motion of the probe then causes that material to deposit on the next bump until enough material accumulates at either interface where good devices begin to fail. Those failures are the die that require retest to capture known good die.

## Summary

A significant percentage of known good devices require multiple test passes because of contamination and corrosion on bumps and pillars. Cleaning probe needles can temporarily reduce CRES, but if the bumps are not cleaned, the CRES will quickly increase resulting in more false failures. Proper cleaning helps recover yield loss, reduces cycle time, and extends the life of probe needles if the needles don't have to be cleaned as frequently. 

## Biography

Terence Collier is President of CVInc.; email [tcollier@covinc.com](mailto:tcollier@covinc.com)



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A photograph showing a cleanroom environment where a person in a blue protective suit and mask is working on a large piece of equipment. In the foreground, there is a close-up image of a green printed circuit board (PCB) with a grid of gold-colored pads, and above it, a circular wafer with many smaller pads. The overall theme is semiconductor manufacturing and assembly.



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# INDUSTRY EVENTS



## IWLP 2013 Program Finalized and Registration is Open

The SMTA and Chip Scale Review are pleased to announce the presentation line-up for the 10th Annual International Wafer-Level Packaging Conference (IWLP), which will be held November 5-7, 2013 at the DoubleTree by Hilton Hotel in San Jose, California.

Four application-oriented tutorials focused on Interposers, TSVs, Wafer-Level Packaging (WLP), and Choosing Between Technologies are featured on Tuesday, November 5, 2013. They will be instructed by experts in the field including Rao Tummala, Ph.D., from Georgia Institute of Technology, Luu Nguyen, Ph.D., from Texas Instruments, John H. Lau, Ph.D., from the Industrial Technology Research Institute (ITRI), and Herbert J. Neuhaus, Ph.D., TechLead Corporation.

The conference takes place November 6 and 7, and comprises three technical tracks on WLP, 3-D (Stacked) Packaging, and MEMS Packaging. With a record number of abstracts received this year, the technical committee added two technical sessions on 2.5/3D Integration to help accommodate the many topics. A special session for Metrology and Test was created to focus on this under-served area of technology. From the worlds of 3D and MEMS, a line-up of plenary speakers and panelists was assembled to provide success stories and offer a glimpse of new and emerging technologies and applications.

Paul Wesling, a CPMT Society

Distinguished Lecturer, is scheduled to give an exciting and colorful history of device technology development and innovation in his presentation "The Origins of Silicon Valley: Why and How It Happened Here" during the Keynote Breakfast on November 6.

Additionally, this year the exhibition was expanded to include over 50 solutions providers showcasing everything from materials to equipment, market research to metrology, and foundries to OSATs.

The IWLP Registration is now available on-line and Early Bird conference pricing is in effect until October 4, 2013, after which registration prices will go up \$100.

## 3D ASIP 2013 Focuses on the Technology and Market Landscape for Device and Systems Integration and Interconnect



Now celebrating its 10th year, 3D Architectures for Semiconductor Integration and Packaging (3D ASIP), which takes place December 11 – 13, 2013, Hyatt Regency San Francisco Airport Hotel, Burlingame, California,

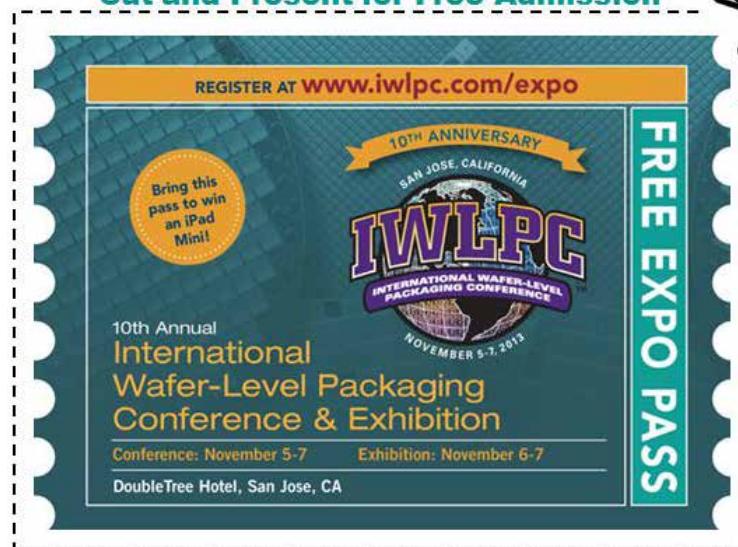
continues to be an ideal venue to meet with leaders from around the world to learn and discuss the latest technology and market insights into 2.5/3D device and systems integration and packaging.

Ever since the first 3D ASIP conference took place a decade ago, the 2.5/3D community and technology have progressed considerably, notes conference co-chairs Philip Garrou, IEEE Fellow and Consultant, and Robert Patti, CTO and VP Design Engineering, Tezzaron. Yet there are still many questions remaining about where the industry will be 10 years from now, what market applications will lead the way, and how each company can best compete in the emerging 2.5/3D device and system interconnect world.

The conference format offers attendees a platform to gain the latest information on technology progress and industry trends that define this sector today and tomorrow. With over 20 invited speakers, the conference aims to provide information critical to planning ongoing and future business and technical efforts impacted by 2.5/3D developments and opportunities.

3D ASIP targets senior-level technologists, managers, and business leaders from the world's foremost companies and research institutions, and

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addresses the interests of the entire 2.5D/3D ecosystem, from technology developers to equipment and materials suppliers to designers, manufacturers, foundries, packaging providers, and end users.

For more detailed information on this year's event, please visit the conference website at [www.3dasip.org](http://www.3dasip.org). Sponsor and exhibit opportunities are available on a first-come, first-serve basis.

### **European 3D TSV Summit: "Application Ready" Theme to Focus on Both Business and Technology Aspects**

The latest TSV product developments and achievements will be discussed at the 2nd European 3D TSV Summit on January 21-22, 2014 in Grenoble, France. Building on the success of the 1st event that attracted almost 320 people from 20 countries, the theme of this year's event is "Application Ready," addressing 3D TSV from both a business and technology perspective. The latest TSV product developments and achievements — including cost, business models, supply chain, manufacturability and technology aspects — will be addressed by executives and experts from global companies.

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as well as equipment and materials suppliers will present during this unique two-day event. More than 25 speakers will share their views during the plenary presentations as well as "round table" discussions. An exhibition zone will be located at the heart of the venue, enabling companies to showcase their products and services to decision makers. The event also includes a unique opportunity to visit the CEA-LETI 300mm TSV clean room. Prior to the event, attendees will be able to prepare their Summit schedule on-site meetings by using a specially developed software tool.

New this year, as an introduction to the event, a Pre-Summit Symposium discussing MEMS and TSV will be held on January 20 in the late afternoon with an invited speaker, roundtable and welcome cocktail.

The event continues to address the hot and controversial topics related to 3D TSV manufacturing and offers unique networking and promotion opportunities. The European 3D TSV Summit Steering Committee includes executives from: ams AG, BESI, CEA-LETI, EV Group, Fraunhofer-IZM, imec, Multitest, Oerlikon Systems, SPTS, STMicroelectronics, and SUSS Microtec.

### **64th ECTC Call for Papers and Professional Development Courses**



IEEE opened up its Call for Papers for ECTC 2014, inviting all companies or individuals interested in presenting at this year's event to submit abstracts

and proposals about new developments and technology related to the following:

- Advanced Packaging
- Applied Reliability
- Assembly and Manufacturing Technology
- Electronic Components and RF
- Emerging Technologies
- Interconnections
- Materials & Processing
- Modeling & Simulation
- Optoelectronics
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There are multiple presentation opportunities at ECTC 2014. Anyone interested in giving oral, interactive presentations, or students interested in presenting a poster session should submit an original, previously unpublished, and non-confidential abstract to the appropriate program chair.

Additionally, the 2014 conference will have a number of Professional Development Programs as part of the

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## 3D InCites and TechSearch International Announce the Winners of the First Annual 3D InCites Awards



The 3D technology focused online community, 3D InCites, and Market Research firm, TechSearch International, have announced the winners of the first annual 3D InCites Awards Program. The program, established to recognize achievements to further the commercialization of 2.5D and 3D IC technologies, benefits the IEEE Frances B. Hugle Engineering Scholarship, which encourages young women to pursue careers in engineering. A panel of nine industry expert judges and an online ‘popular vote’ represented the 10 votes to determine the winners from a field of 25 nominees in five categories.

Xilinx' Virtex 7 H580T won the award for 3D Products Design/Process. Mentor Graphics swept two award categories, winning for 3D Design Tools with its Calibre tool, and the 3D Test and Reliability Tools/Equipment category with its Tessent MemoryBIST product. EV Group's EVG850TB/

DB XT won the 3D Manufacturing Equipment award, and Dow Corning, took home the 3D Materials award with its Temporary Bonding Solution.

Awards were presented at a breakfast ceremony hosted by Impress Labs, Thursday, July 11, 2013 at the Impress Lounge during SEMICON West. During the event, Ana Londergan, Senior Staff Engineer at Qualcomm Technologies—the awards' platinum sponsor, presented a \$5,000 check on behalf of the 3D InCites Awards Program to Jan Vardaman, TechSearch International, representing the donation to the IEEE Frances B. Hugle Engineering Scholarship.

## Applied Materials Names Gary E. Dickerson as CEO



Applied Materials, Inc. Board of Directors has appointed Gary E. Dickerson as president and chief executive officer (CEO) and Michael R. Splinter as executive chairman of the Board of Directors, effective September 1, 2013. Additionally, Dickerson will serve on the Board of Directors. Dickerson is currently president of Applied Materials and succeeds Splinter, who has served as the Company's CEO since 2003.

In a statement, Splinter called Dickerson “an outstanding leader and partner” who is focused on the company’s growth strategies. “I welcome him to the Board and have every confidence that his vision and personal drive will translate into remarkable success in leading Applied

Materials as our next CEO,” he said.

For his part, Dickerson credited AMAT with a strong foundation from which to build, noting the company’s broad technology, deep talent, and passion for driving materials innovation that will provide the device performance and yield solutions needed to advance technology. “Our opportunities have never been greater and I am grateful to Mike and the board for the privilege to lead Applied into a new era of growth and success,” he said.

A long-time industry leader, Dickerson served for seven years as CEO of Varian Semiconductor Equipment Associates, Inc. until its acquisition by Applied Materials in 2011 and spent 18 years at KLA-Tencor Corporation where he held a variety of operations and product development roles before serving as president and chief operating officer. He earned a BS degree in Engineering Management from the University of Missouri, Rolla and an MBA from the University of Missouri, Kansas City.

Splinter was named president and chief executive officer of Applied Materials and a member of its board of directors in 2003, and became chairman of the board in 2009. He is a 40-year veteran of the semiconductor industry and has reportedly led Applied to record revenue and profits during his tenure as CEO. This fall, he will receive the Semiconductor Industry Association's 2013 Robert N. Noyce Award for his outstanding achievements and leadership in support of the semiconductor industry.

## GLOBALFOUNDRIES and Applied Materials Sign Fab 1 Service Agreement

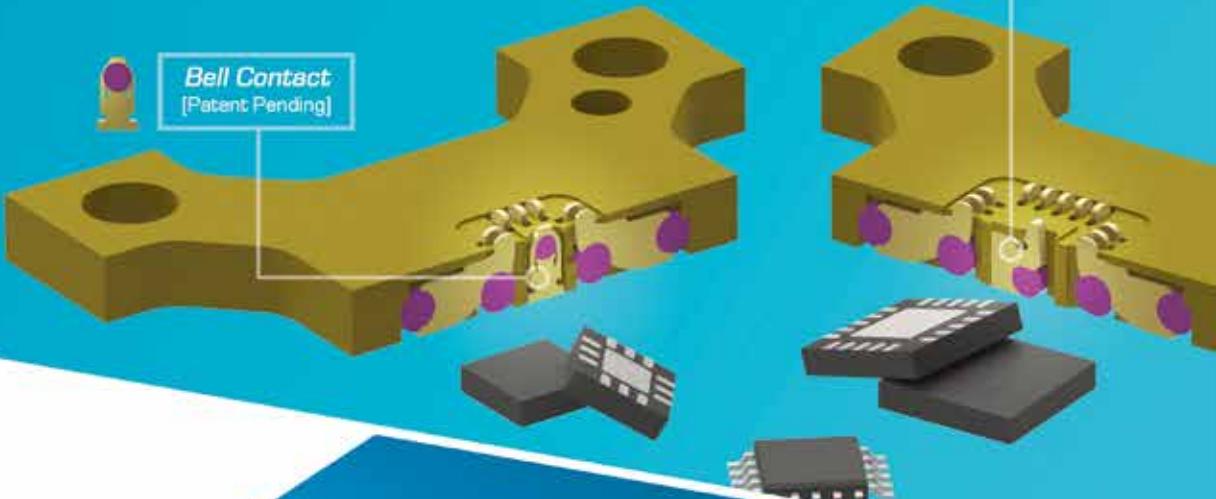
Semiconductor equipment manufacturer, Applied Materials, Inc. (AMAT) has signed an enhanced two-year contract with top tier foundry, GLOBALFOUNDRIES Inc., to service all AMAT equipment at its Fab 1 in



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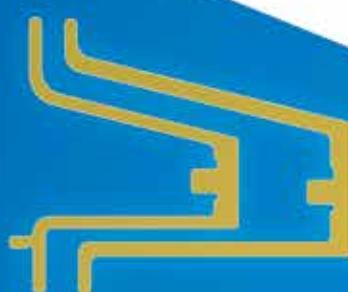
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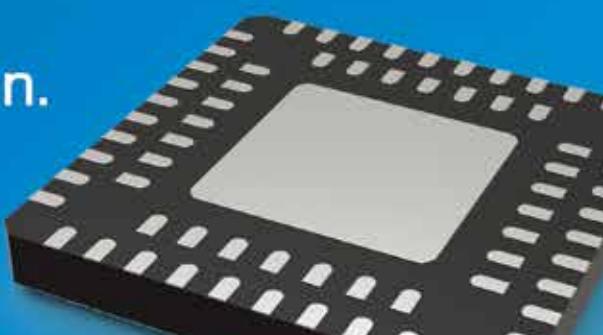
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Dresden, Germany. According to the company, this Applied Performance Service contract extends beyond traditional tool maintenance to support GLOBALFOUNDRIES in optimizing technology ramps, increasing capacity, reducing scrap and improving factory output stability in critical areas.

"GLOBALFOUNDRIES is currently ramping its worldwide capacity, including the build-out of the Dresden site into the largest manufacturing site in Europe," said Kay-Uwe Weber, Director Global Supply Management of GLOBALFOUNDRIES Fab 1. "We believe the spirit of this contract - to have both service teams collaborate even closer using Applied's technical depth and Fab1's manufacturing experience - will provide us with custom-made services to accelerate our success."

Under the agreement, a team of AMAT certified engineers will provide GLOBALFOUNDRIES Fab 1 with 24x7 support in mission-critical areas, using advanced engineering and logistics technologies, including AMAT's remote diagnostic capability and proprietary equipment engineering and diagnostic software. All the AMAT tools covered under the enhanced contract will receive preventive and corrective maintenance, spare parts

management, parts cleaning and coating, and analytical services.

"We are very pleased that GLOBALFOUNDRIES Fab 1 has chosen us as an important collaborator and resource in helping to achieve its aggressive growth and technology goals in Dresden," said Charlie Pappis, group VP and general manager of Applied Global Services. "Together, we've tailored a flexible, wide-ranging Performance Service program that focuses Applied's efforts on solving high-value manufacturing challenges, which will allow GLOBALFOUNDRIES Fab 1 to focus on its core competency of providing high quality, advanced technology to its customers."

#### **SUSS MicroTec Honored with SPIL's Outstanding Performance Award**

Every two years Siliconware Precision Industries Co., Ltd. (SPIL), a top tier outsourced semiconductor assembly and test service (OSATS) provider headquartered in Taichung, Taiwan, honors its most respected suppliers with its "Outstanding Performance Award".

This year, SPIL honored SUSS MicroTec, supplier of equipment and process solutions for the semiconductor and related markets, with its "Outstanding Performance Award". Only one other company was selected out of a field of 500 suppliers to receive the 2013 award. The award, established to acknowledge excellent supplier performance, is based on criteria such as quality, price, delivery, support and technology.

"In the fast-moving semiconductor industry, quality, technology and support are major distinctive features of equipment providers," says Frank P. Averdung, President and CEO of SUSS MicroTec. "We are honored to receive this distinctive recognition of our work from SPIL – one of our most valued customers."

#### **Sono-Tek Corp. Expands In-House Laboratory Testing Facilities**



Sono-Tek Corporation, a global ultrasonic spray technology company, announced the completion of its laboratory testing facility expansion, located at the corporate headquarters in Milton, NY. The recent acquisition of equipment, including an SEM microscope for onsite coatings analysis performed in the lab, led to some reorganization and physical expansion of the facility to provide a better workflow for customers and visitors in addition to some increased elbow room.

"Access to equipment such as this new SEM is beneficial not only to Sono-Tek customers, but to the surrounding community of colleges and other research institutions in New York for advancing research and manufacturing of future innovations in our area," said Steve Harshbarger, president, Sono-Tek. "We envision our lab continuing to grow in the coming years, as new applications for ultrasonic spray coating continue to develop."

Sono-Tek reports that the newly installed equipment, and particularly the SEM microscope, enables the company to gauge process variables by providing immediate onsite analysis of coatings that require very precise deposition characteristics, such as photoresist onto MEMS, fuel cell coatings, medical implantable device coatings and other nanomaterial coatings. Additionally, a new corona surface treatment has been installed to better prepare substrates for improved surface tension characteristics prior to coating. The acquisition of at

least one more surface treatment tool is planned in the future.

### Ultratech/Cambridge NanoTech Expands Operations With New, State-Of-The-Art Facility



Ultratech, Inc., a supplier of lithography, laser-processing and inspection systems to the semiconductor advanced packaging and related markets, has relocated Ultratech/Cambridge NanoTech to Waltham, MA. After acquiring the assets

of Cambridge NanoTech in December 2012, the company invested in a new facility to enhance atomic layer deposition (ALD) development.

ALD technology provides coatings and material features with significant advantages compared to other existing techniques for depositing precise nanometer-thin films. This technology is expected to be in high demand in volume manufacturing environments for integrated optics, micro-electro-mechanical systems (MEMS), implantable devices in the biomedical sector and batteries and fuel cells in the energy market.

The new state-of-the-art facility will reportedly expand its operations for next-generation ALD equipment development to enable leading-edge scientific research.

"The completion of the new facility

marks our successful integration of the Cambridge NanoTech assets into Ultratech's nanotechnology product group," says Arthur W. Zafiropoulo, Chairman and CEO of Ultratech. "By investing in the expansion of these operations, we expect to generate increased revenue in new and existing markets. Ultratech, and our ALD unit, Ultratech/Cambridge NanoTech, will continue to focus on technology solutions that support our global



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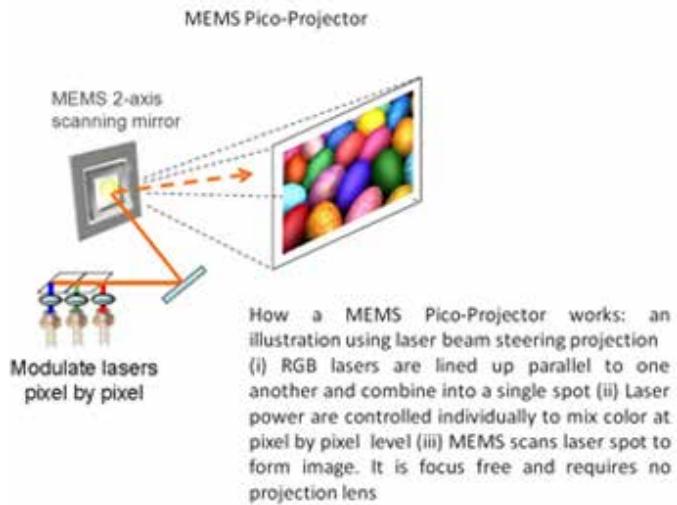
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## Micromirror Technology for Smartphones: The Next Big Thing

With consumers using smartphones as mobile entertainment centers, the ability to project photos and videos on any surface may soon become the norm. A\*STAR Institute of Microelectronics (IME) and OPUS Microsystems Corporation, a Taiwan-based company specializing in Micro-Electro-Mechanical Systems (MEMS) scanning mirror devices, have signed an agreement to refine and develop a MEMS scanning mirror for smartphone applications. This would reportedly



enable phones to project photos and videos on any surface, and with no constraints on the viewing screen size of the mobile devices.

MEMS scanning mirror—or micromirror—technology, which is used in light-modulating devices, has undergone rapid technological progress over the years. This has led high video and image quality in high-definition televisions and more recently, digital cinemas. The market demand for such visual experience expresses itself in portable consumer electronics, such as tablets and mobile phones, in which gaming, photo, and video applications

have become integral. This technology is expected to be a major component in the next generation of smartphones.

To meet this demand, OPUS and IME will work together on the development of an optimized MEMS scanning mirror, which will enable a pico-projector for smartphone applications. Through this project, the two parties aim to achieve a slimmer, smaller, higher-performance MEMS micromirror that offers a compact yet high-resolution pico-projector solution for smartphones, essentially turning any surface into a display.

The project signifies OPUS Microsystems' first research partnership and project in Singapore and will build on IME's experience and knowledge in

the field of MEMS. IME will lead the process design and development while OPUS Microsystems will contribute in the design of the scanning mirror.

"We are delighted that OPUS Microsystems has chosen IME to be their partner for its first research project in Singapore," said Prof. Dim-Lee Kwong, Executive

Director of A\*STAR IME. "The interest in pico-projectors has gained traction in recent years, but the industry challenge remains in achieving a cutting-edge technology that will allow the integration of a small-scale projector into smartphones while maintaining a high resolution output. It is an exciting R&D opportunity for IME to be part of such a project that will potentially lead to a technological breakthrough."

## Hesse Mechatronics Opens Training and Applications Lab in Tempe, Arizona

Hesse Mechatronics, Inc., the



Allan Camp, Technical Support Manager  
Hesse Mechatronics, Inc.

Americas subsidiary of Hesse GmbH, manufacturer of high-speed fine-pitch wedge bonders and fully automatic heavy wire bonders for the backend semiconductor industry, recently opened its newest training and applications lab in

Tempe, Arizona.

The company assigned responsibility for the new lab to Allan Camp, who joined the company as technical support manager in June 2012. Camp brings more than two decades of experience in the semiconductor industry, including his work for Eastman Kodak Company in microelectronics packaging and Xerox Corporation in wafer fabrication.

Camp will oversee technical support and training on Hesse Mechatronics' family of semiconductor packaging equipment both at the training facility and at customer sites. He will also conduct demonstrations of Hesse Mechatronics' wedge bonding equipment, including thin wire wedge bonders and heavy wire wedge bonders, so customers can validate and qualify the equipment prior to making an investment in new technology.

"Allan's knowledge in wafer fab operations, microelectronics packaging, and semiconductor process equipment will serve our customers well as he provides training that addresses their specific equipment and manufacturing requirements," notes Joseph S. Bubel, president of Hesse Mechatronics, Inc.

Camp's role and the new lab are steps in Hesse Mechatronics' strategy to improve customers' experience. Hesse intends for the new lab to increase the convenience of qualifying and learning about their wedge bonding equipment and the convenience of taking advantage of support services.

# Next-Generation Wafer-Level Fan-Out Package

By Akio Katsumata, Tomoko Takahashi [[J-Devices](#)]

**A** new package structure and technology for the next-generation of wafer-level packaging (WLP) is being developed—called wafer-level fan-out package (WFOP). A face-down mounting type, this package uses a metal plate, e.g., stainless or copper, as the base plate of its redistributed interconnection layer. The redistribution traces fan out of the dies, so that the pin count is not limited by die size as in the case with WLP. The redistribution layer is fabricated using the semi-additive method of copper plating. By manufacturing with this large scale panel substrate, we can achieve higher throughput than with the conventional wafer manufacturing method. Moreover, this new package has several additional benefits, including being ultra-thin with excellent thermal characteristics, and a reduced noise level, which are made possible by the metal plate. Additionally, the packaging process using this direct patterning method has the potential for new styles of semiconductor packages. The package structure, process flow, design rules, and package characteristics will be provided in this article.

## Packaging Drivers

Recently, the smart device market has been dominating the electronic device business. Smart devices, such as mobile phones, tablets of various sizes, and e-readers, have multiple features and functions, such as imaging, data processing, 3D graphic engines, MPEG engines, cameras, RF, TV and more. Various system LSI, memories and components are used for those devices. Requirements being placed on semiconductor packages include miniaturization, high wiring density, and thinness. Packages, of course,

must enable high-speed electrical transmission, lower thermal resistance, and multi-function capability.

To meet the requirements listed above, several fan-out packages are being developed. There are some technical issues, however. First, the embedded dies in the mold resin shift their positions because heat processes shrink the resin, and the alignment accuracy of wire bonding or interconnect redistribution is therefore limited. Additionally, in embedded packages, dies are covered by resin, so the heat generated by the devices cannot dissipate efficiently. In fan-in packages, the body size depends on the die size, so their design rules are not very flexible. In response to this problem, we developed a new type of fan-out package, called wafer-level fan-out (WFOP). This new package can overcome these issues and has highly accurate die placement, lower thermal resistance and is capable of placing balls outside of the die.

## The Basic Structure

**Figure 1** shows the cross section of the structure and **Figure 2** the actual view of the distribution layer. The package is one of the face-down mounting types that uses a metal plate, such as stainless steel or copper, as the base plate of the redistributed interconnection layer. The dies are

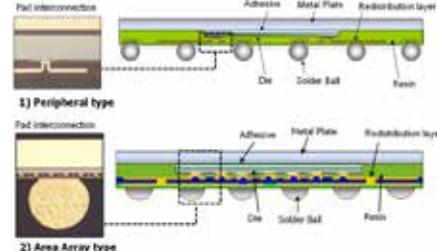


Figure 1: Cross section.

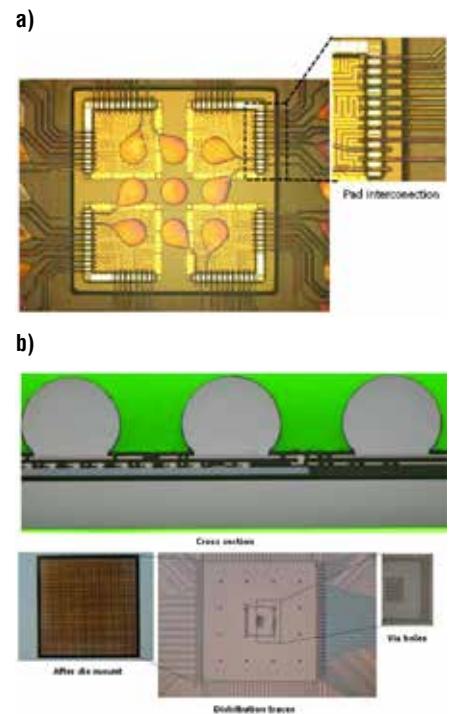


Figure 2: a) Peripheral array distribution traces; b) Area array distribution traces.

mounted on the metal plate, and the resin between the dies acts as a stress buffer and insulator for the interconnections. The distribution layer is fabricated using the semi-additive method of copper plating. In **Figure 1**, there are two layers for the trace, but it is not limited to two. Three layers—two layers for signals, and one layer for the ground plane—will be the typical format. In **Figure 2a**, the contacts between the die pads and distribution layer are leaded. **Figure 2b** shows a cross section of area pads connections and redistribution traces. The solder resist is formed on the interconnection layer and the balls are placed on the solder resist.

## Process Flow

The process flow begins when the

dies are attached onto the metal plate. The placement accuracy is less than  $\pm 5\mu\text{m}$ . After that, the resin is laminated as an insulator for the redistribution layer. Openings are made in the resin in the area of the die pads. Next, using the plating method, traces are formed on the resin layer. In the case of multi-layers, the sequence from resin lamination to plating traces is repeated. The solder resist is laminated on the resin and the traces, and then patterned for solder balls, and the balls are placed on it. Finally, the metal plate is singulated into individual units by dicing, and the packages are completed.

In the process flow, the size of the metal plate is not limited because the process starts with placing dies on it and redistributing wires. In other words, those packages can be fabricated not only by wafer scale, but also by panel scale. This means higher throughput is achieved by leveraging the scale.

## Design Rules

**Table 1** shows some design specification values. There are two options for the die pad array. In the case of the peripheral pad array, the current minimum pitch is  $50\mu\text{m}$ , and we connect redistribution traces and die pads as shown in **Figure 2a**. In the case of the area pad array, the current

minimum pitch is  $150\mu\text{m}$  and  $30\mu\text{m}$  via holes in the pads are created as shown in **Figure 2b**.

One of the benefits of this new package is its thinness; height data for the package is shown in **Figure 3**. The nominal height in design is  $960\mu\text{m}$ , and the average is around  $965\mu\text{m}$ . In this package, a  $50\mu\text{m}$  die thickness, no core, no bumps and fewer build-up layers are achieved.

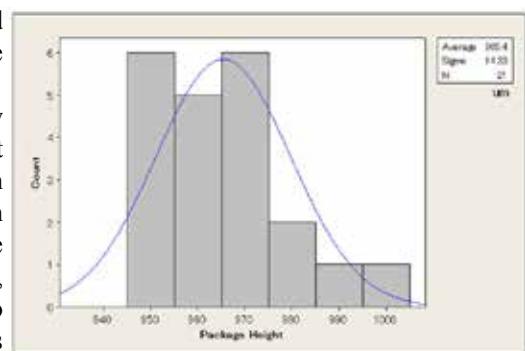
## Package Characteristics

**Figure 4** shows the simulation result of thermal resistance to compare this package and the wire bonding type plastic fine-pitch ball grid array (PTFBGA). Two types of the base plate are simulated, one stainless, the other copper. The x-axis is the die area ratio of the package size. Generally, the smaller the die size ratio, the higher the thermal resistance. But in all ratios, this package's thermal resistance is lower than that of the PTFBGA, by 5% to 15% in the stainless steel base plate type, and by 22% to 45% in the copper base plate type. The temperature contour diagram in **Figure 4** shows that more heat cannot spread on the die in PTFBGA. This means that the metal plate in this package functions as an effective heat spreader.

Item	Design specifications	
	Peripheral Pad	Area Pad
Line width	$20\mu\text{m}$	
Line space	$20\mu\text{m}$	
Pad pitch	$50\mu\text{m}$	$150\mu\text{m}$
Via land diameter on pad	-	$86\mu\text{m}$
Via diameter on pad	-	$30\mu\text{m}$
Via land diameter on RDL	$86\mu\text{m}$	
Via diameter on RDL	$30\mu\text{m}$	
Via land -line space	$20\mu\text{m}$	
Ball land - line space	$20\mu\text{m}$	
Ball land – via land space (Same NET)		$0\mu\text{m}$
Ball land – via land space (Different NET)		$20\mu\text{m}$
Package outline – resist space	$50\mu\text{m}$	
Resist – Copper pattern space	$50\mu\text{m}$	

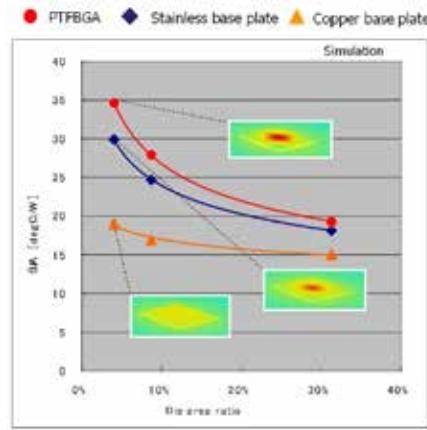
Ball pitch	Ball land diameter	Resist opening diameter	Package height	Stand off
No Ball	-	-	$460\mu\text{m}$ TYP	-
0.80mm	$530\mu\text{m}$	$380\mu\text{m}$	$860\mu\text{m}$ TYP	$400\mu\text{m}$
0.65mm	$480\mu\text{m}$	$350\mu\text{m}$	$790\mu\text{m}$ TYP	$330\mu\text{m}$
0.50mm	$350\mu\text{m}$	$230\mu\text{m}$	$710\mu\text{m}$ TYP	$250\mu\text{m}$
0.40mm	$290\mu\text{m}$	$220\mu\text{m}$	$650\mu\text{m}$ TYP	$200\mu\text{m}$

**Table 1:** Design specifications.



**Figure 3:** Actual package height of the basic structure.

**Figure 5** shows the electromagnetic interference (EMI) test method and results. The models tested were PFBGA, the basic structure of WFOP package (the basic type shown in **Figure 5**), and the type with a grounded metal lid (the grounded type shown in **Figure 5**). Compared to the PFBGA, the output power noise of the basic type (of WFOP package) is lower by 10dB, and the noise of the grounded type is lower by 25dB. The result can be explained



**Figure 4:** Comparison of thermal resistance.

by noting that the metal plate in this package works effectively as a noise shield, even though the metal plate is a floating node. In the grounded type, it works even better.

**Table 2** shows the results of reliability tests for the basic structure. Temperature cycle testing (TCT), pressure cooker testing (PCT), high-temperature storage (HTS) testing, and on-board TCT were carried out. The electrical connection and scanning acoustic topography (SAT) images are checked at each lap. There is no problem.

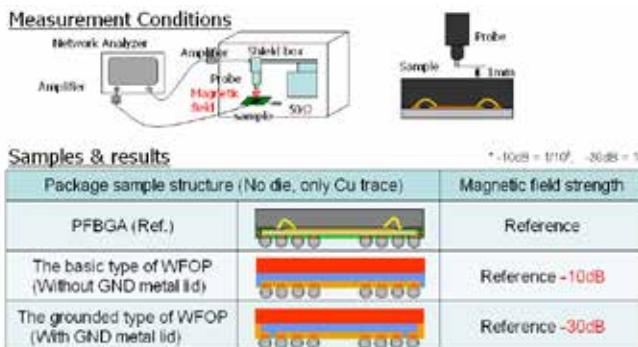


Figure 5: Comparison of EMI.

### 3D Packaging

**Figure 6** shows the cross section of a stacked-die type of WFOP package. The manufacturing process for the stacked-die type is very similar to the basic type. The second die is attached on the resin over the first die, and is covered with resin again, and traces are formed over the resin. This sequence is repeated again for the third and the fourth dies. The TCT result of this package is shown in **Table 3**. No problems are found in electrical tests and SAT images.

The warpage under heating and

cooling can be seen in **Figure 7**. The total warpage value is only around 70 $\mu$ m. Most of the warpage happens around 130°C, which is the Tg of one resin in the package. Over and under 130°C, the metal plate is stiff

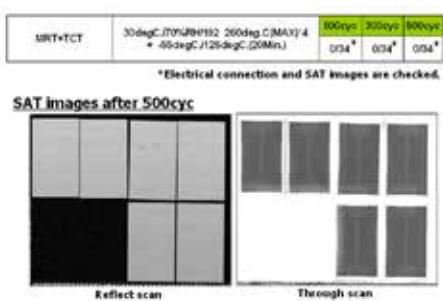


Table 3: TCT result of the stacked die package.

enough to keep the resin from warping. Such stacked-die packages are required for high spec memories. The sample shown in **Figure 6** is for 2CH/4CE. As a next step, we are planning to develop a four die stack and an eight die stack in one package as 8CH/8CE.

### Summary

In this article, we

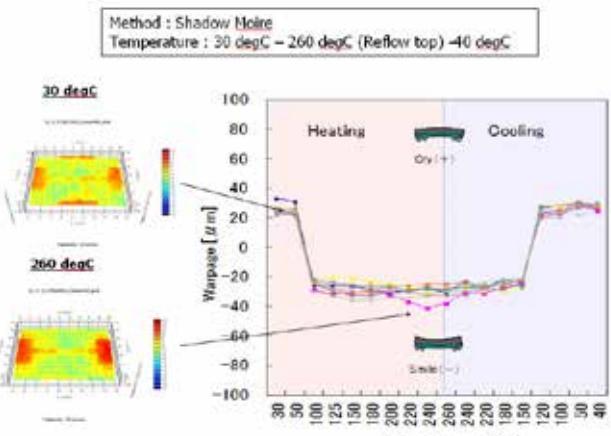


Figure 7: Warpage during heating and cooling.

formats) are CPU and MPU peripherals in smart devices. We are also planning to expand this direct patterning technology to future packages, such as multi-chip module (MCM), stacked-dies, and package-on-package (POP). These structures will provide the solution for system-in-package, and because this package is less susceptible to EMI, it will be a promising solution for RF devices.

### Acknowledgment

The authors deeply appreciate support by the staff in cooperating companies.

### Biographies

Akio Katsumata received his BS in Industry Chemistry from Chiba U. and is the General Manager for the Packaging Research & Development Center at J-Devices; email akio.katsumata@j-devices.co.jp

Tomoko Takahashi received her MS in Material Physics from Osaka U. and is the Specialist for the Packaging Research & Development Center at J-Devices.

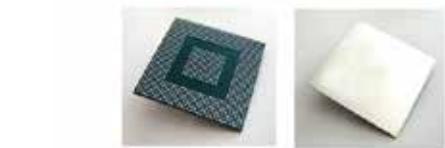


Table 2: Results of reliability tests for the basic structure.

Items	Condition	N	After MRT SAT/TEST	1stLAP SAT/TEST	2ndLAP SAT/TEST	FinalLAP SAT/TEST
MRT1	30C/70%RH/216h 260C*3	32	0/32	-	-	-
MRT2	30C/70%RH/144h → 255C*3 → 30C/70%RH/24h → 255C*1	21	0/21	-	-	-
MRT1+PCT	110C/1.2mm 85%	22	-	0/22(168h)	0/22(312h)	0/22(500h)
MRT2+PCT	110C/1.2mm 85%	10	-	0/10(168h)	0/10(312h)	0/10(500h)
MRT1+TCT	-55C(200h), 125C(200h)	22	-	0/22(100cyc)	0/22(300cyc)	0/22(500cyc)
MRT2+ TCT	-55C(200h), 125C(200h)	11	-	0/11(100cyc)	0/11(300cyc)	0/11(500cyc)
MRT1+HTS	150°C	22	-	0/22(168h)	0/22(312h)	0/22(500h)
On board TCT		22	-	0/22(510cyc)	-	0/22(2000cyc)

Figure 6: Cross section of stacked die package.

introduced a next-generation fan-out package—a new embedded wafer-level package structure and fabrication technology. This structure is a promising solution for a thinner package with more traces, lower thermal resistance, and better electrical characteristics.

Possible applications for this new package (in both FBGA and FCBGA

# Graphene for Next-Generation Electronics Packaging

By Kaustubh Nagarkar, Shakti Chauhan, Faisal Ahmad, Arun Gowda [GE Global Research]

**G**raphene, comprised of carbon atoms bonded in one plane as a honeycomb lattice, reigns supreme in its electrical, thermal, and mechanical characteristics compared to almost any other material in existence. Because of its 2-dimensional nature, graphene has the potential to overcome some of the inherent limitations of other advanced materials like carbon nanotubes (CNTs) to integrate into practical applications. Consequently, graphene and related technologies are increasingly being researched by universities, national labs, and industry alike.

This article provides a review of the progress and gaps in realizing graphene-based solutions for the electronic packaging industry. A brief description of currently available fabrication processes for graphene or graphene-based materials is provided alongside a detailed discussion of several promising application areas (**Figure 1**). The best properties of graphene exist for suspended monolayer configurations, whereas most electronic packaging applications will need to utilize graphene in micro- or macro-structures. The ability to favorably scale graphene's superior properties from nanoscale dimensions to such bulk or 3D structures, and commercially viable manufacturing processes to accomplish this, are identified as key needs for broad applications-impact.

## Graphene Properties

Several researchers have studied graphene's intrinsic properties, i.e., for a suspended atomic monolayer – a peculiar manifestation where no other 3D materials exist. In this form, graphene has demonstrated an array of properties that surpass those of

currently used materials. Balandin, et al., first reported intrinsic thermal conductivity of 4800-5300W/m-K [1]. Most electronic packaging applications today typically deploy metals (Cu – 400W/m-K, Ag – 430W/m-K, Al – 250W/m-K) as heat spreaders or fillers, for solid conduction-based heat transfer. Later studies reported ballistic phonon conduction in graphene with thermal conductivity between 2000-4000W/m-K [2, 3]. The upper end of this range is achieved for isotopically pure graphene (<0.1% C<sup>13</sup> as opposed to 1.1% natural abundance) and with large domain (or grain) sizes. These properties also exceed the reported results for multi-walled and single-walled CNTs (3000-3500W/m-K) and the best bulk crystalline thermal conductor, i.e., diamond (1000-2200W/m-K).

Research has also revealed the superior electrical properties of graphene such as high mobility (~20m<sup>2</sup>/Vs), high current density (~10<sup>8</sup>A/cm<sup>2</sup>), ballistic transport, and low electrical resistivity [4, 5]. From a stand-point of mechanical properties, graphene films have been shown to possess an elastic modulus of ~1TPa and high intrinsic strength (~30GPa), when combined with its low density, making graphene much lighter, stronger and harder than

steel at similar dimensions [6]. With graphene, such strength and stiffness can be realized even with atomically thin sheets thereby allowing remarkable mechanical strength to be combined with geometric flexibility. Atomically-thin graphene-based membranes also offer the promise of an effective barrier i.e., graphene membranes have been shown to be completely impermeable to most liquids and gasses (even helium), while only allowing water vapor to pass through [7].

Graphene also possesses some unique optical properties. It does not have a band gap and therefore can absorb radiation extending all the way into the THz range. Another interesting phenomenon that has been observed in graphene is the ultrafast carrier dynamics that is attributable to its peculiar band structure. This property, in conjunction with Pauli blocking of the carriers, has been exploited for shaping and stabilizing ultra-short (~ picoseconds) pulses in fiber mode locked lasers [8].

The prevailing excitement around graphene stems largely from this array of exciting intrinsic properties of graphene films. Electronic packaging applications, among others, are particularly positioned to benefit from

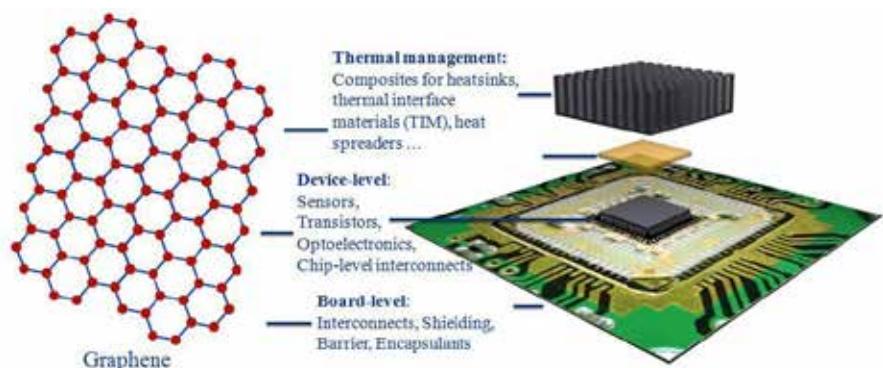


Figure 1: An illustration of the far-reaching potential applications of graphene in microelectronics.

the utilization of graphene as they often rely on a combination of properties (such as thermal, electrical, and mechanical). Graphene-based materials, therefore, can provide a significant leap forward in the performance and reliability of electronic devices and systems.

## Fabrication Routes and Applications

Many processing techniques have been researched to manufacture graphene as summarized in **Table 1**. These can broadly be categorized as top-down or bottom-up approaches [9]. Top-down approaches typically use graphite as the starting material and “exfoliate” it to yield graphene. These processes are capable of producing large quantities of high-quality graphene in flake or powder form. On the other hand, bottom-up approaches create layer by layer of graphene from a carbon source; these are slower but yield continuous large area, single or multi-layer sheets. The table also lists potential electronic packaging applications based on the form achieved by the manufacturing method. The most prominent applications include next-generation nano-electronic (beyond CMOS) and optoelectronic devices, interconnects, and thermal management, ranging from the chip, to the system level [**Figure 1**]. The other key areas that are relatively unexplored include structural (such as encapsulants), shielding, and impact resistance materials. This section outlines the potential of graphene in all the aforementioned areas.

**Optoelectronic Devices.** Graphene finds itself at the center of many optoelectronic applications such as optical modulators and ultrafast broadband photo-detectors. The high carrier mobility would enable such devices to operate at frequencies approaching hundreds of GHz. But the issue of the limited absorption capability of a single monolayer (merely 2.3% at 300nm to 2500nm) will need to be addressed [10]. Graphene could also be integrated in devices such as high power semiconductor lasers to extract light, deliver current, and at the same time, spread out the heat, which could have a remarkable impact on devices such as LEDs, vertical external cavity surface emitting lasers (VECSELs), optical modulators and optical amplifiers and their packaging.

**Interconnects.** Transistors and interconnects are two major areas that could utilize the superior electrical properties of graphene. Graphene-based on-chip interconnects – varying from a few nanometers to microns – are actively researched as they enable miniaturization, compatibility with potential “beyond CMOS” graphene transistors, and excellent thermal performance. Also, issues of electromigration and current density related to today’s metallic (typically Cu) interconnects could be resolved [11]. Graphene nanoribbons (GNRs) have been actively researched for on-chip interconnects because of their compatible fabrication process. In early

studies, their resistivity was measured to be comparable to copper in various nanometer-width scales [5, 12]. Several researchers have already looked into the use of CNTs in combination with graphene for 2.5D/3D through-silicon via (TSV) interconnects [11]. Researchers have also proposed dense vertical and horizontal graphene (DVHG) for TSV filling and horizontal interconnects [11, 13].

The research on graphene for off-chip interconnects primarily spans printable inks, transparent conducting layers, electrodes, and fillers in solder. Early commercialization of graphene-based inks have targeted the replacement of more expensive silver inks with better performance than carbon inks for flexible electronics [14]. An exciting area of development is in the use of graphene for transparent conducting electrodes for flexible/stretchable electronics. Roll-to-roll capable, large area, multi-layer conducting films with greater than 90% transparency and less than 125 Ohm/sq sheet resistances have been demonstrated using a CVD process [15]. Graphene also has the potential for robust, low cost anisotropic conducting films for interconnect applications, especially with transparent conductors in displays [16]. Efforts to make anisotropic conductive films (ACF) with graphene encapsulated magnetic microspheres or graphene-coated polymer spheres have shown promising electrical results [17]. The potential of graphene as an additive in solders has also been explored. Exfoliated graphene oxide flakes (that were subsequently converted to graphene) were incorporated with indium or indium-gallium alloy to form a matrix composition that resulted in lower net thermal and electrical resistivity in the material [18].

**Heat spreading Layers.** Several emerging applications in consumer and military electronics like RF and microwave power amplifiers (Si-LDMOS, GaAs MESFETs, SiC MESFETs and GaN HEMTs), 2.5D and 3D integrated Si microprocessors and memory devices, require the integration of on-chip cooling strategies

Process	Source	Characteristics & Form	Electronic Packaging Applications
Top-Down	Derived from graphite/graphite oxide through exfoliation: Micromechanical, electrochemical, solvent-based, arc discharge	<ul style="list-style-type: none"> <li>Flakes (or powders) with small lateral size</li> <li>Monolayer or Few-layer Graphene (MLG, FLG)</li> <li>Large production quantities</li> <li>Cost-effective</li> </ul>	Fillers in composite materials e.g., inks, thermal interface materials (TIM), encapsulants, barrier layers/coatings
Bottom-Up	Epitaxial growth on silicon carbide; chemical vapor deposition; confined self-assembly, etc.	<ul style="list-style-type: none"> <li>Continuous large area films</li> <li>Higher quality, i.e., fewer defects</li> <li>Deposition on non-planar surfaces</li> <li>FLG, MLG</li> </ul>	Monolithic graphene structures Transparent electrodes, on-chip/off-chip interconnects, heat-spreading layers, barrier coatings, transistor and optoelectronic device layers

**Table 1:** Types of processes used to manufacture graphene and related applications.

to mitigate hot spots. Graphene, due to its inherently 2D nature, offers the promise of an efficient solid conduction heat spreading strategy such that near-junction temperature gradients i.e., hot spots can be minimized without the complexity of on-chip active cooling strategies (microfluidic cooling or thin film thermoelectrics). For example, several approaches with graphene-based heat spreaders have been demonstrated, in MLG and FLG form, to affect temperature reduction in hot spots on MOSFET devices on SOI substrates [19] as well as GaN HEMT devices [20]. With graphene, substantial junction temperature reduction at the hot spots (even for GaN-on-sapphire devices) was reported, with the potential to yield up to an order-of-magnitude increase in device lifetime.

Similar approaches can also be visualized for stacked Si and Si interposers for the emerging 2.5D and 3D packaging approaches. Filled Cu vias or CNT-filled vias could be used for ‘through-thickness’ (or inter-layer) heat transfer (i.e., thermal vias), or play a dual role as vertical interconnects and thermal vias [11]. Graphene (particularly in its FLG form) can realize lateral heat spreading along with lateral interconnects in these devices. In a 3D stack, lateral heat spreading enables utilizing a larger layer-area for inter-layer heat conduction so as to minimize the overall package thermal resistance. Incorporation of h-BN (a 2D material similar to graphene but electrically insulating with thermal conductivity of 300–800W/m-k) as the device dielectric layer can further enhance near-junction cooling through lateral heat spreading in these devices [21].

**Electronic Materials.** Graphene fillers in an organic (polymeric) matrix are being deployed for applications such as conductive inks, thermal interface materials (TIMs), barrier layers, shielding layers, encapsulants, and electrically conductive adhesives. These manifestations utilize graphene flakes or graphene nano-platelets (GNP) in mono- or multi-layer form as fillers in a composite system. Several studies have reported promising

enhancements in thermal conductivity, electrical conductivity, mechanical stiffness and gas barrier properties in polymeric composites with graphene fillers [22]. Shahil, et al., reported up to 2300% enhancement in a graphene-epoxy nanocomposite at 10% loading for TIM applications, outperforming conventional metallic fillers as well as CNT fillers in similar matrix systems [22]. At just 2% loading, they were able to enhance the thermal conductivity of commercial thermal grease from 5W/m-K to 14W/m-K, while preserving all mechanical properties. For electrically conductive polymeric systems, graphene fillers have shown the lowest percolation threshold (between 0.1% - 0.37% weight percent) as compared to conventional fillers [22]. Similarly, elastic modulus and tensile strength can be enhanced by a factor of 2-8 with <3% volume fraction of graphene-based fillers in common polymeric matrix systems such as PDMS, PVA (poly(vinyl alcohol)) and PCL (polycaprolactone) [22]. Graphene oriented parallel to polymer films can reduce gas permeation by as much as 90% at only 3 wt% thereby demonstrating a potential for barrier layer applications [22]. Thus, greater functional property enhancements at comparable loading can be obtained with graphene fillers because of their excellent intrinsic properties and their 2D nature (as opposed to CNTs and other nano-fillers).

### Challenges for Applications and Possible Solutions

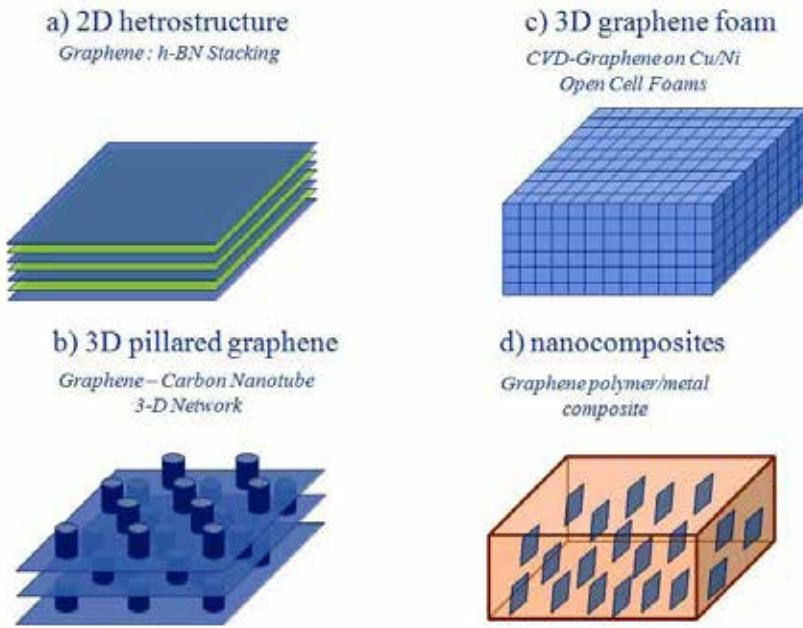
Many challenges need to be overcome in applications utilizing both monolithic as well as nano-composite graphene and graphene-based structures. The challenges discussed below pertain to the fabrication processes, as well as to the inherent structure of the implementations.

**Monolithic - Graphene Implementations.** Currently, high quality monolithic graphene films are grown on metal substrates using CVD processes at temperatures as high as 1000°C and subsequently transferred to the device substrate [23]. During the process, organic residues and etchants

degrade the films’ intrinsic properties. Therefore, the ability to grow and pattern graphene layers directly onto the device substrate (Si, GaN, SiO<sub>2</sub>, plastics, etc.) at CMOS-compatible temperatures is an attractive solution. Alloying of the deposition substrate (Cu or Ni foils) and the use of higher order hydrocarbon precursors gases (benzene, etc.), as opposed to methane, may lower CVD temperatures to 450°C, making graphene CVD deposition a CMOS-compatible process, while retaining adequate quality [24]. Recently, large area surface wave plasma CVD-based graphene films synthesized at ~300°C have also been demonstrated [25]. Also, alternative etchant chemistries and transfer processes (electrochemical transfer process, etc.) to ensure defect-free graphene films are being researched.

From a structure standpoint, the intrinsic properties of graphene monolayers are strongly affected by the choice of substrate and stacking of monolayers. Upon placement on a substrate (typically SiO<sub>2</sub>), the thermal conductivity of graphene monolayers drops to ~600W/m-K and electrical mobility reduces to 4x10<sup>4</sup>cm<sup>2</sup>/Vs [2, 26]. The impact is even higher in encased structures. Similarly, the thermal conductivity and mobility of graphene reduces when it is stacked as multiple layers approaching those of graphite at n = 11 layers [2]. With the present understanding, at dimensions (width and thickness) larger than ~50-100nm, metals like Cu will continue to offer lower electrical and thermal resistance, making monolithic graphene-based structures only suitable for nano-electronics or first-few layers in back-end-of-line (BEOL) interconnects. The high degree of anisotropy because of weak inter-lamellar coupling is also a key obstacle.

**Figure 2** shows an illustration of several emerging solutions to these issues. **Figure 2a** shows a heterogeneous structure with alternative graphene and h-BN multilayers, which seem to allow the retention of in-plane electrical (and possibly thermal) transport properties in substrate and



**Figure 2:** Potential architectures to realize macroscopic (3D) structures with graphene films: a) graphene - h-BN heterostructure, b) pillared graphene with graphene-CNT structures, c) 3D graphene foams, and d) graphene nanocomposite.

multi-layer implementations. Such super-lattice structures could also be used in broadband, high bandwidth

photo-detectors. **Figure 2b** shows a pillared graphene structure that utilizes CNTs as interlayer connections

between individual graphene layers [27]. Such a structure could eventually yield a 3D material without the high degree of anisotropy seen in graphitic structures, while retaining the intrinsic properties. Simulation results suggest that the spacing and length of the CNT connections and the precise nature of CNT-graphene nodes need careful consideration [28]. Both heterogeneous and pillared graphene implementations are inhibited by the lack of a viable fabrication process.

**Figure 2c** shows a graphene foam structure, where an unbroken MLG or FLG film can be provided within a macroscopic structure. Early thermal property measurements of graphene foam structures have shown promising results due to the absence of nodes or junctions, which strongly limit the properties of other 3D manifestations (as in **Figures 2a** and **b**) [29]. Pettes et al., reported an effective thermal conductivity of ~1.7W/m-K of a FLG foam structure with only 0.45% volume

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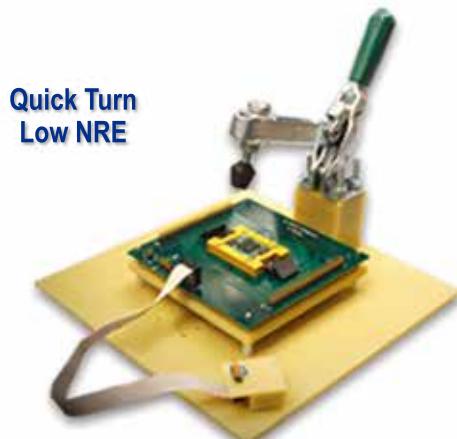


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fraction. With further increase in volume fraction, or surface area to volume ratio in such structures, higher effective properties could be attained.

**Graphene Nano-composite Implementations.** Another strategy to make macroscopic structures with graphene-like properties is through the fabrication of graphene-based nanocomposites (**Figure 2d**). As discussed earlier, such materials can be used as inks, TIMs, barrier coatings, encapsulants, etc. In this context, top-down approaches to manufacture graphene-based fillers (GNP, flakes, etc.) are particularly attractive. While initial results in this field have been quite promising, there is still considerable room for improvement and optimization. The desirable characteristics for the fillers are large domain size, low defect density and appropriate functionalization for interfacial coupling and dispersion. It has been established that production of GNP fillers through the oxidation of graphite and thermal or chemical reduction – the most attractive route for large-scale production of graphene-based nanocomposites – can also adversely modify the mechanical stiffness, electrical transport and thermal properties of the graphene-fillers. For instance, wrinkles and atomic-scale perforations found in thermally reduced graphene (TRG) may make the sheets less stiff, more permeable and reduce thermal and electrical conductivity, but may inhibit restacking, thereby improving dispersions at higher loading. Alternative cost-effective routes to exfoliate graphene layers need to be sought that preserve graphene's intrinsic properties in the nanocomposite system. These would, as an example, involve eliminating the structural deformation or unnecessary functionalization and post-treatments that restore graphitic planar domains.

## Summary

Ever since the discovery of graphene in 2004, there has been a rapid growth in studying its properties, as well as unearthing disruptive applications (such as sensors). Graphene has the potential to offer vast improvements in

microelectronic devices and systems. Today's manufacturing techniques can produce graphene in many forms, at varying scales, as required by potential target applications. Significant challenges, however, exist in the geometric scalability of graphene, while preserving its intrinsic properties for electronic packaging applications. The first commercial implementations of graphene are being realized in the area of nanocomposites. Meanwhile, other 2D materials, such as hexagonal boron nitride (h-BN), whose structures are similar to that of graphene, are already being actively researched [30]. A whole family of graphene-like materials have emerged, which include transition metal dichalcogenides (TaS<sub>2</sub>, WS<sub>2</sub>, MoS<sub>2</sub>, MoTe<sub>2</sub>, NiTe<sub>2</sub>), graphene oxide and reduced graphene oxide, graphane (double-sided hydrogenated graphene) and fluorographene (fluorinated graphene) [31]. The varied but compatible properties of such materials may help fill the gap in the adoption of graphene (or like) materials in electronic packaging applications. <sup>Sp</sup>

## References

1. A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, C. Lau, "Superior Thermal Conductivity of Single Layer Graphene," *Nano Letters*, 8, 902–907, 2008.
2. A. A. Balandin, "Thermal Properties of Graphene and Nanostructured Carbon Materials," *Nature Materials*, 10, 569–581, 2011.
3. E. Pop, V. Varshney, A. Roy, "Thermal Properties of Graphene: Fundamentals and Applications," *MRS Bulletin*, 37, 2012.
4. K. Bolotin, K. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, et al., "Ultrahigh Electron Mobility in Suspended Graphene", *Solid State Communications*, 146, 351, 2008.
5. R. Murali, Y. Yang, K. Brenner, T. Beck, J. Meindl, "Breakdown Current Density of Graphene Nanoribbons," *Applied Physics Letters*, 94, 243114, 2009.
6. C. Lee, X. Wei, J. Kysar, J. Hone, "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene," *Science*, Vol. 321 no. 5887, pp. 385-388, 2008.
7. R. R. Nair, H. A. Wu, P. N. Jayaram, I. V. Grigorieva, A. K. Geim, "Unimpeded Permeation of Water Through Helium-Leak-Tight Graphene-Based Membranes," *Science*, 27, 335, 2012.
8. Q. Bao, H. Zhang, Z. Ni, Y. Wang, L. Polavarapu, Z. Shen, et al., "Monolayer Graphene as Saturable Absorber in Mode-Locked Laser," *Nano Res.*, 4, pp. 297-307, 2011.
9. R. Edwards, K. Coleman, "Graphene Synthesis: Relationship to Applications," *Nanoscale*, 5, 38, 2013.
10. K. F. Mak, M.Y. Sfeir, Y. Wu, C. H. Lui, J. A. Misewich, T. F. Heinz, "Measurement of the Optical Conductivity of Graphene," *Phys. Rev. Lett.* 101, 196405, 2008.
11. M. Nehei, "CNT/Graphene Technologies for Advanced Interconnects and TSVs," SEMATECH Symposium Taiwan, October 18, 2012, Hsinchu, <http://www.sematech.org>
12. R. Murali, K. Brenner, Y. Yang, T. Beck, J.D. Meindl, "Resistivity of Graphene Nanoribbon Interconnects," *IEEE Electron Device Letters*, Vol. 30, No. 6, June 2009.
13. A. Kawabata, T. Murakami, M. Nihei, N. Yokoyama, "Growth of Dense, Vertical and Horizontal Graphene and Its Thermal Properties," *Japanese Journal of Applied Physics* 52 04CB06, 2013.
14. <http://vorbeck.com>
15. S. Bae, H. Kim, Y. Lee, X. Xu, J. Park, Y. Zheng, et al., "Roll-to-roll Production of 30-inch Graphene Films for Transparent Electrodes," *Nature Nanotechnology*, 5, 574-578, 2010.

16. H. Kim, J. Kim, K. Kim, H. Lee, S. Lee, S. Lim, M. Park, "Tailored Anisotropic Magnetic Conductive Film Assembled from Graphene-encapsulated Multifunctional Magnetic Composite Microspheres," US8178201B2.
17. J. Shen, Y. Zhu, K. Zhou, X. Yang, C. Li, "Tailored Anisotropic Magnetic Conductive Film Assembled from Graphene-encapsulated Multifunctional Magnetic Composite Microspheres." *Jour. of Materials Chemistry*, 22, 545-550, 2012.
18. K. Jagannadham, "Thermal Conductivity of Indium-Graphene and Indium-Gallium-Graphene Composites," *Jour. of Electronic Materials*, 40, 1, 25-34, 2011.
19. S. Subrina, D. Kotchetkov, A. Balandin, "Graphene Heat Spreaders for Thermal Management of Nanoelectronic Circuits," *IEEE Electron Device Letters*, 30 (12), 1281, 2009.
20. Z. Yan, G. Liu, J. Khan, A. Balandin, "Graphene Quilts for Thermal Management of High-power GaN Transistors," *Nature Communications*, 3, 827, 2012.
21. I. Jo, M. T. Pettes, J. Kim, K. Watanabe, T. Taniguchi, Z. Yao, L. Shi, "Thermal Conductivity and Phonon Transport in Suspended Few-Layer Hexagonal Boron Nitride," *Nano Letters*, 13 (2), pp 550–554, 2013.
22. H. Kim, et al., "Graphene / Polymer Nanocomposites," *Macromolecules*, 43, 6515–6530, 2010.
23. X. Li, et al., "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science*, 324 (5932), 1312-1314, 2009.
24. Z. Li, P. Wu, C. Wang, X. Fan, W. Zhang, X. Zhai, et al., "Low-temperature Growth of Graphene by Chemical Vapor Deposition Using Solid and Liquid Carbon Sources," *ACS Nano*, 5(4), pp. 3385-90., 2011.
25. T. Yamada, J. Kim, M. Ishihara, M. Hasegawa, "Low-temperature Graphene Synthesis Using Microwave Plasma CVD," *Jour. of Applied Physics*, 46, 2013.
26. J. Chen, C. Jang, S. Xiao, M. Ishigami, M. S. Fuhrer, "Intrinsic and Extrinsic Performance Limits of Graphene Devices on SiO<sub>2</sub>," *Nature Nanotechnology* 3, 206 – 209, 2008.
27. G. K. Dimitrakakis, E. Tylianakis, G. E. Froudakis, "Pillared Graphene: A New 3-D Network Nanostructure for Enhanced Hydrogen Storage," *Nano Letters*, 8 (10), pp. 3166–3170, 2008.
28. V. Varshney, S. S. Patnaik, A. K. Roy, G. Froudakis, B. L. Farmer, "Modeling of Thermal Transport in Pillared-Graphene Architectures," *ACS Nano*, 4 (2), pp. 1153-1161, 2010.
29. M. T. Pettes, H. Ji, R. S. Ruoff, L. Shi, "Thermal Transport in Three-Dimensional Foam Architectures of Few-Layer Graphene and Ultrathin Graphite," *Nano Letters*, 12 (6), pp. 2959–2964 2012.
30. D. Pacile, J. C. Meyer, C. O. Girit, A. Zettl, "Two Dimensional Phase of Boron Nitride: Few-atomic Layer Sheets and Suspended Membranes," *Applied Physics Letters*, 92, 133107, 2008.
31. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, "Single-layer MoS<sub>2</sub> Transistors," *Nature Nanotechnology*, 6, pp. 147-150, 2011.

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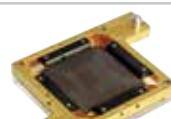


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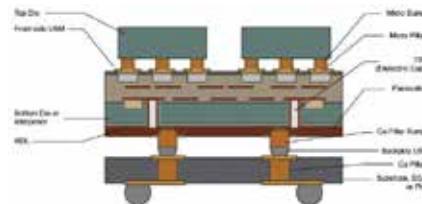


# Controlling Bumping Processes with Picosecond Ultrasonic Metrology

By Johnny Dai, Priya Mukundhan, Tim Kryman [Rudolph Technologies, Inc.]

**A**dvanced packaging processes continue to follow a development path similar to front-end processes, with increasing process complexity and decreasing feature size demanding greater attention to inspection and metrology to control processes and maintain yields. In addition, the high value of the known good die being packaged multiplies the cost of scrap and the benefit of increasing yield. The adoption of advanced packaging has driven an increase in interconnect density with more I/O connections in smaller form factors. Bumps used in fine-pitch, high-density interconnects are now as small as 15 $\mu\text{m}$  diameter at a 40 $\mu\text{m}$  pitch. Importantly, the plating processes used to create these bumps and interconnects exhibit pattern dependent variations that require direct measurements on product wafers to ensure adequate process control.

Bumping processes came into widespread use with the adoption of flip-chip packaging processes. Flip-chip processes generally use solder bumps and can create bumps with pitches down to 150 $\mu\text{m}$ . In response to the demand for higher interconnect densities, manufacturers have developed advanced packaging processes that interpose complex structures between the chip(s) and the package to route electrical signals and secure the chip mechanically to the package (Figure 1). Although there are many different schemes for these interconnects, (commonly referred to as 2.5D packaging) most use some form of bumping to create mechanical and electrical connections between stacked components, i.e., chips, interposers and packages. Typically, these bumps are made of copper and created using a plating process. Copper pillar bumps have reached diameters as small as 15 $\mu\text{m}$  with 40 $\mu\text{m}$  pitch in-line.



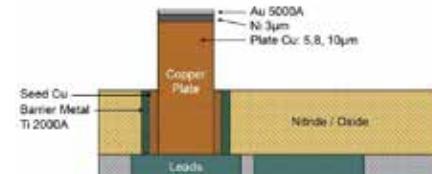
**Figure 1:** Advanced packaging techniques use complex structures to route signals between the chip and the package, allowing more connections in less space. The structures are typically created with wafer-level processing using processes similar to front-end fabrication processes.

The bumps themselves are comprised of a multilayered stack of various metals with the mechanical and electrical performance of the interconnect determined by the physical dimensions and metallurgical characteristics of the individual layers.

As these advanced packaging processes move from development to high-volume production, manufacturers require automated measurement capability with the speed and precision to control the process, thus maintaining both yield and throughput. Automated measurements improve repeatability and reduce labor costs. Given that packaging often occurs at an outsourced semiconductor assembly and test (OSAT) facility using expensive, known good die, a comprehensive interconnect metrology is becoming widespread by OSATs and IDMs who have in-house packaging facilities.

Figure 2 shows the typical layers used in a copper pillar bump interconnect. Each metal layer in a copper pillar bump contributes to the specific mechanical and electrical characteristics of the interconnect. A copper pillar bump may consist of an Al or Cu conductive pad followed by a Ti or TiW barrier layer to prevent diffusion of copper into the pad, a Cu seed layer to ensure proper adhesion, the plated Cu pillar, a Ni or NiV diffusion barrier, possibly Pd over

the Ni to prevent oxidation, and topped off by either a Au flash or a SnAg solder cap. All of these materials are opaque to visible light and thus require non-optical techniques for thickness measurement and proper process control.



**Figure 2:** Bumps provide the mechanical and electrical connections between stacked components. The bumps are themselves complex stacks of multiple layers. The performance of the connection depends on the physical and metallurgical characteristics of the films in the stack.

## Picosecond Ultrasonic Measurements

Picosecond ultrasonic measurement is a non-contact, non-destructive technology that uses an extremely short pulse of intense laser light to heat a very small spot on the sample surface. The expansion that results from the nearly instantaneous heating generates an acoustic wave that travels down through the various layers of the sample. At each interface between layers, the wave is partially reflected back toward the surface. By precisely measuring the time elapsed between the initial pulse and the returning reflections from each interface, one can accurately measure the thickness of each layer in a multilayer stack. Metal films ranging in thickness from a few tens of Angstroms to greater than 10 $\mu\text{m}$  can be measured. Measurements are based on first principles and do not require daily calibrations or reference wafers. The small spot size (5 $\mu\text{m} \times 7\mu\text{m}$ ) allows for measurements directly on product wafers.

Picosecond ultrasonic metrology is well established for metal film thickness metrology and qualified as a process-of-record tool at all top ten IDMs and

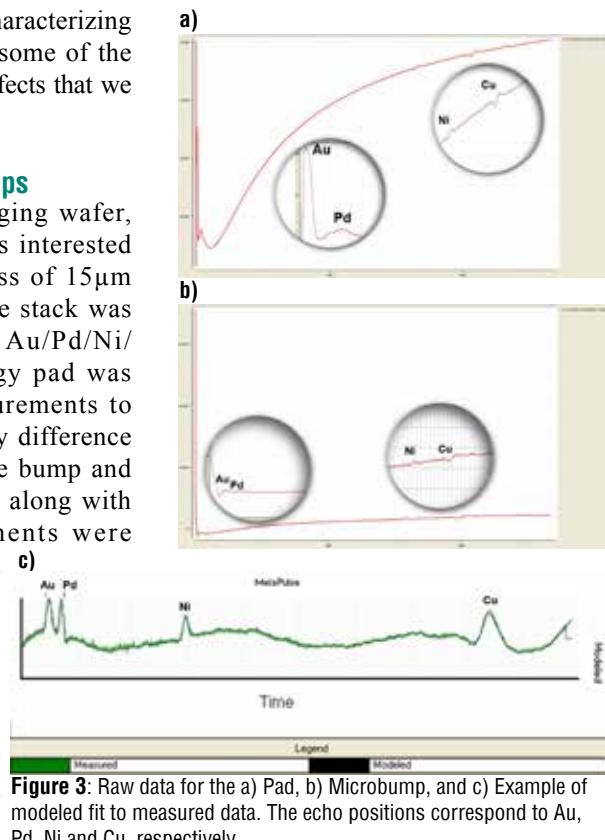
foundries in front-end semiconductor manufacturing. Recently, we have been working with foundries and OSATs to qualify this technology for advanced packaging. To meet the needs of our packaging customers, improvements have been made to the hardware's configuration to extend the upper thickness limits of the films measured, while reducing the measurement site size capability to measure directly on microbumps. Optical techniques exist that can measure physical characteristics, such as bump height, plot uniformity, and coplanarity across the wafer, but picosecond ultrasonic metrology is unique in its ability to measure in sites as small as 15 $\mu$ m and provide multi-layer film specific information. Picosecond ultrasonics is therefore capable of providing the metrology needed to control advanced bumping processes. Measurements of under bump metal stacks (UBM) and redistribution layers (RDL) are routine from a measurement standpoint. In this article we will focus

on selected examples of characterizing microbumps and describe some of the pattern-dependent plating effects that we have observed.

### Characterizing Microbumps

On an advanced packaging wafer, our foundry customer was interested in measuring the thickness of 15 $\mu$ m diameter microbumps. The stack was nominally described as Au/Pd/Ni/Cu on oxide. A metrology pad was also identified for measurements to determine if there was any difference in the process between the bump and the pad. A full wafer map along with repeatability measurements were requested to understand the capabilities of the technology for such measurements and also to help characterize the within-wafer uniformity.

**Figure 3** shows the raw signal obtained from the pad and the microbump. Using



**Figure 3:** Raw data for the a) Pad, b) Microbump, and c) Example of modeled fit to measured data. The echo positions correspond to Au, Pd, Ni and Cu, respectively.

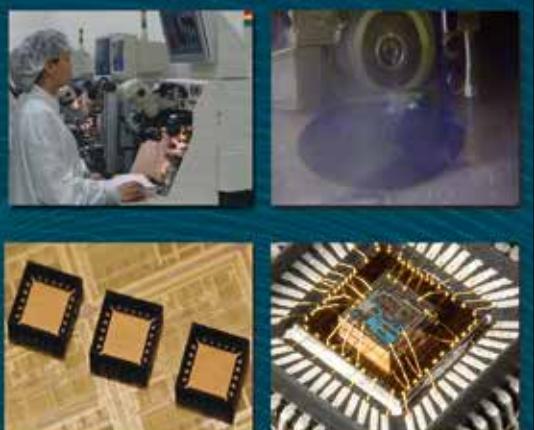


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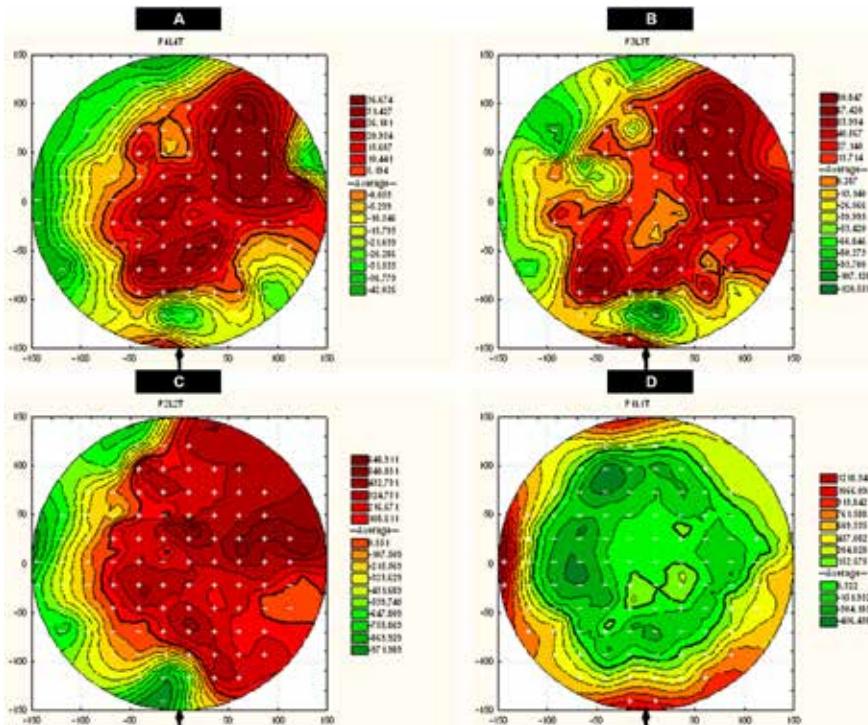
picosecond ultrasonics, we were able to measure the thickness of all the layers simultaneously. The echo positions can be identified unambiguously in the graph and correspond to the various layers of the stack. Using standard speed of sound in the materials, we can calculate the thickness of the films as Thickness=velocity\*echo position/2.

The within-wafer (WIW) uniformity profiles for all the layers measured on both the microbump and pads are shown in **Figures 4** and **5**. The films were nominally measured at 200Å Au/400Å Pd/4μm Ni/1μm Cu. The 1 σ standard deviation for WIW uniformity on the pad was ~7% for Au, 3% for Pd, 0.5% for Ni and 3% for Cu. The bump measurements, in general, showed more variations and the WIW uniformity were much higher than the pad: ~9% for Au, ~9% for Pd, 1% for Ni, and 5% for Cu. The variation in thickness between the pad and the microbump is significant and demonstrates the need for monitoring directly on the microbump instead of the pads in order to get an accurate representation of process variations. In high-volume manufacturing, the ability to consistently and reliably measure these small structures is very important. Precision (30 repeats at wafer center) as well as stability (load/unload, five days, two times a day) measurements were made on both the structures.

Precision measurements for all the layers for both the pad and the bump were <0.1% 1σ standard deviation. The stability plots are shown in **Figure 6** and the 1σ standard deviation is summarized in **Table 1**. The excellent repeatability measurements more than meet the needs for process control.

### Pattern-Dependent Plating Effects

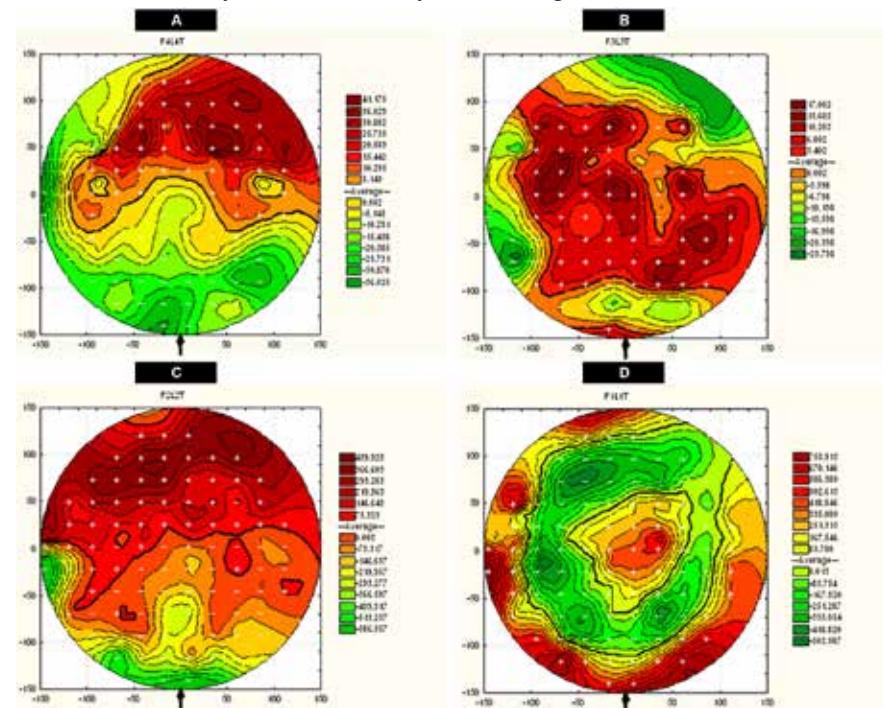
Pattern-dependent plating effects have been studied extensively in the dual-damascene development process. In this study, an under bump metal (UBM) wafer with pads of varying shapes and sizes was identified for measurements to a) determine the technology's capability to measure in these different structures, and b) to determine how significant the pattern-dependent plating effects were across the various structures.



**Figure 4:** The within-wafer uniformity profiles for a) Au, b) Pd, c) Ni and d) Cu from the microbump.

**Figure 7** shows a schematic representation of the structures identified for measurements. Six different sites, ranging in size from 20μm-40μm were selected on a nine-wafer skew. The stack was nominally Ni/Cu. Using picosecond ultrasonics, we measured the thickness of the Ni and Cu layer simultaneously.

Within-wafer variation was ~2-4% for Ni and ~9% on Cu. **Figure 8** shows within-wafer uniformity profiles across each site. As the profiles point out, we were able to identify pattern-dependent plating effects. For example, within the same die, the variation in Ni thickness could be as high as 10%, and the Cu ~6%.



**Figure 5:** The within-wafer uniformity profiles for a) Au, b) Pd, c) Ni and d) Cu from the pad.

## Summary

As the advanced packaging process becomes more complex, metrology requirements are also becoming very stringent. Microbumps are now approaching diameters as small as 15 $\mu\text{m}$  with a pitch less than 50 $\mu\text{m}$ . The materials and thicknesses used in the bumping process are critical to the mechanical and electrical performance of the final package. In this study, we have demonstrated the use of picosecond ultrasonics for the measurement of microbumps (15 $\mu\text{m}$  diameter) and the value in measuring directly on the bumps instead of a metrology pad. The non-contact, non-destructive technique

allows for full wafer characterization at production-worthy throughputs and provides excellent stability for high-volume manufacturing.

## Biographies

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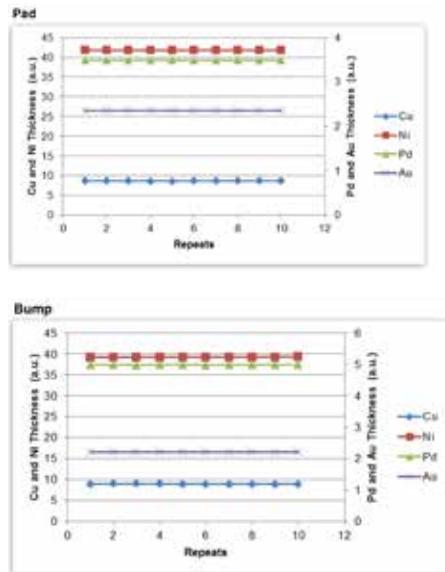


Figure 6: Pad and microbump stability plots.

**Table 1:** Summary of five-day stability data collected on both pad and microbump. Summary of five-day stability data collected on both pad and microbump.

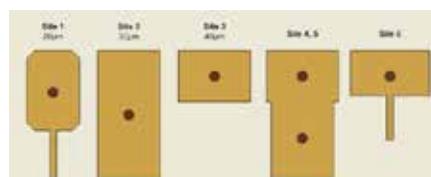


Figure 7: Schematic representation of measurement sites.

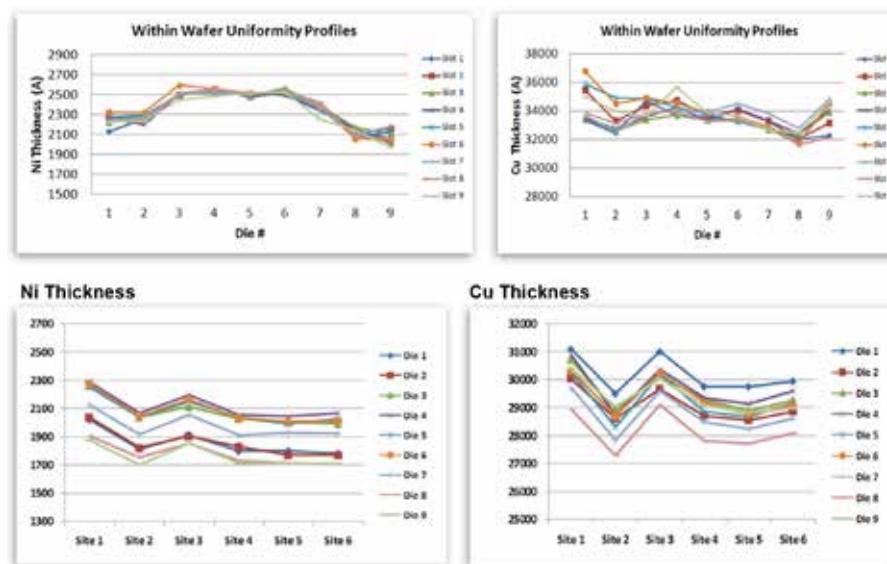
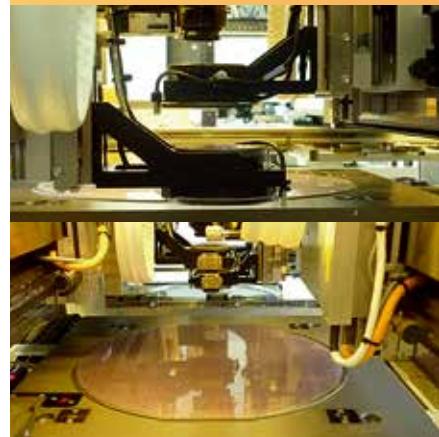


Figure 8: Ni and Cu thickness profiles across the different sites on nine different die that were measured.

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# Bonding Material Properties From a 3D IC Perspective

By Michelle Fowler [Brewer Science]

Wafer-to-wafer bonding with advanced materials is one of the most promising approaches for three-dimensional (3D) integrated circuit manufacturing [1]. Developing new or improved bonding materials for an evolving thin-wafer-handling customer base is an evolutionary process. Most industry experts agree that these materials must survive thinning and backside processing while allowing for debonding and easy removal. Because process flows differ from fab to fab and from one outsourced semiconductor assembly and test (OSAT) service provider to another, various bonding material platforms are being developed [2]. Performance criteria such as improved film uniformity, low-stress films, improved thermal stability, debonding ease, and residue-free cleaning are of primary concern to the end user. From the developers' perspective, these material demands ultimately translate to different bonding material chemistries with differing physical properties.

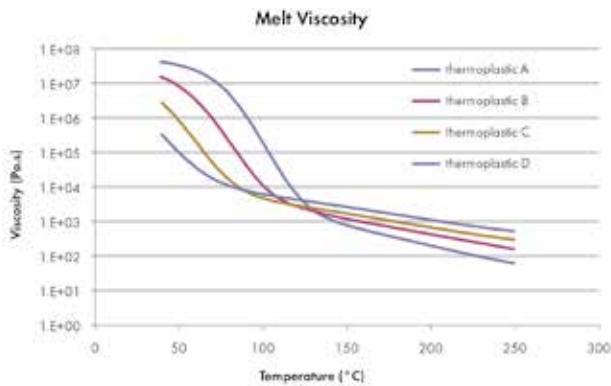
## Film Uniformity and Low TTV

For the past century, synthetic chemistry has been developing new bonding materials, and the technology has accelerated rapidly in recent years. Thermoplastic materials have several desirable properties that make them excellent bonding materials. These materials are used to temporarily bond device wafers that require significant thinning and the creation of an I/O redistribution layer on the backside that will be attached to a support or carrier wafer [2]. Thermoplastic materials are formulated to be non-reactive and cannot be crosslinked by either heat (thermal curing) or light (photocuring). At elevated temperatures they have the ability to melt and reflow, which will enable the material to cover wafer

topography and flow into vias and trenches. Known as the polymer melt rheology or melt viscosity, this property allows the thermoplastic bonding material to planarize the wafer surface when the film is baked above the melt temperature of the polymer. The total thickness variation (TTV) is a measure of the film thickness uniformity across the wafer (maximum film thickness minus minimum film thickness), which is typically reduced during the baking process (Figure 1).

For today's 3D IC devices, severe or extreme topography is driving the need for thicker bonding films. Thermoplastic bonding materials capable of achieving film thicknesses of 50 $\mu\text{m}$  or thicker have become the new standard. When coated using a spin-apply process, the thermoplastic bonding material must cover a substrate 200-300mm in diameter at reasonable spin speeds (<2000rpm) over various topographies while maintaining a film TTV of less than 3 $\mu\text{m}$ . Normally, most of the coating non-uniformity will be located within 10mm of the wafer edge, forming what is called the bonding material edge bead (Figure 2). Spin-coating dynamics and material surface tension all contribute to the buildup of material at the wafer's edge.

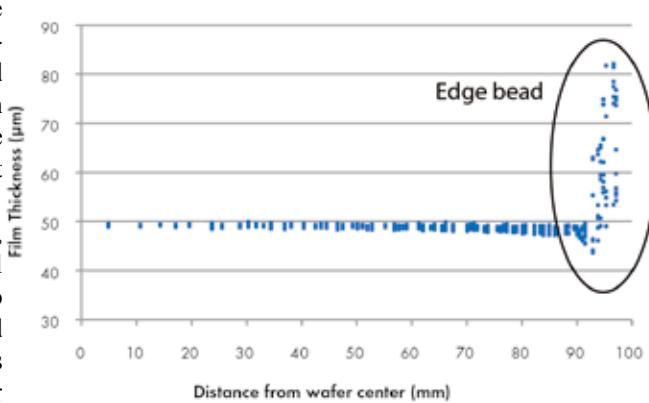
During bonding, this excess material can squeeze out into the wafer bevel and can cause various defects at the wafer edge. Edge bead



**Figure 1:** Graph showing the different melt profiles for various thermoplastic materials. The viscosity drops dramatically with increasing temperature.

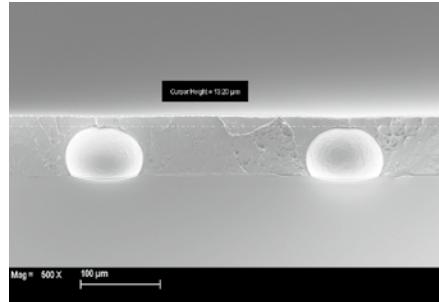
can be controlled through formulation modifications and various process controls during spin coating. A low film TTV will translate to improved wafer uniformity after backside grinding, allowing for thinner device wafers (less than 50 $\mu\text{m}$  thick). For a thick bonding material to fill or planarize wafer topography, the material should also have a low solution viscosity with low film shrinkage during baking [1]. To meet this requirement, the material scientist must balance material viscosity with formulation solids content to maximize film thickness, minimize film shrinkage, and improve coating quality. The casting solvent system and melt rheology during baking will also determine the final thickness of the film and its uniformity (Figure 3). Because

Radial Plot with Edge Bead



**Figure 2:** Radial plot showing film uniformity with a 30 $\mu\text{m}$  edge bead.

of film uniformity limitations caused from spin coating a thick, viscous bonding material, alternative coating methods are also being developed that create very uniform films without an edge bead.



**Figure 3:** Bumped wafer with excellent fill planarized by a thermoplastic bonding material.

### Thermal Stability During Backside Processing

Thermal stability can be defined as the maximum temperature at which a bonding material fails. Delamination defects, deformations around topography, and loss of adhesion to the carrier are all failures related to high thermal exposure. Delamination defects can be caused from volatilization of low-molecular-weight additives at high temperatures and from polymer degradation. At high temperatures, the melt viscosity of the thermoplastic bonding material can become so low that the stress in the bonded stack can overpower the mechanical strength of the material, causing blisters and deformation of the thin device wafer. Many of today's unfilled thermoplastic bonding materials have a maximum use temperature range of less than 300°C.

Thermoplastic bonding materials are non-reactive and are designed to be temporary and removable after the debonding process has been completed. When they are subjected to high-temperature backside processes, they can fail, either by forming voids (delaminations) in the bond line or by becoming soft and reflowing, which can cause wafer misalignment. Unlike a thermoset bonding material, thermoplastic materials are not cured or crosslinked and can be sensitive to moisture, etch gases, and other contaminants they contact during wafer backside processing. Once bonded, the

bonding film is no longer fully exposed to the outside environment; the wafer edge is the only exposed area. Bond failures at the wafer edge can occur when the bonding material absorbs moisture or other contaminants which, when subjected to vacuum or heat, can volatilize and cause failures within the bond line (**Figures 4 and 5**).

For processes where dry-etch removal is possible, a thermoset material offers

distinct advantages over an uncured thermoplastic polymer. These materials are formulated to react and become fully cured once they are exposed to either heat or light. This property makes the bonding material an irreversibly hard film that can only be removed by using harsh cleaning chemistries or by dry-etch processing. A thermoset bonding material can be spin applied and will have good re-flow properties when

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**Figure 4:** Acoustic scan of a bonded wafer with edge delaminations.



**Figure 5:** Enlarged image of flower patterns or delaminations at the bond interface.

processed at temperatures below the cure temperature or before the film has been exposed to ultraviolet (UV) light.

Another material property that affects how well a bonding material performs in a high-temperature application is the glass transition temperature, or  $T_g$ , of the polymer. All polymers have some temperature at which their physical properties are rigid and glassy. When a polymer is in the glassy state, its mechanical behavior is relatively stable, hard, and brittle. With an increase in temperature, the polymer will change from a glassy to a rubbery state. Bonding materials having  $T_g$  values at or below ambient temperature remain rubbery and flexible at lower temperatures but with increases in processing temperature can begin to melt or flow, resulting in a loss of mechanical strength. Ideally, with backside processing temperatures for bonded wafers reaching upwards of 300°C for some applications, a bonding material should have a  $T_g$  below the bond temperature but still high enough to remain flexible but not flowable at elevated temperatures. This property will prevent misalignment between

the carrier and the device wafer. The polymer  $T_g$  can be modified by adding plasticizer or by altering the degree of polymer branching or crosslinking.

With so much of the fabrication process being proprietary to each fab, communicating process specifics such as temperatures, chemicals, and vacuum processes that the bonding material will be exposed to will determine which material will work best for a given application (**Table 1**).

### Low-Stress Debonding

Thinning device wafers to thicknesses less than 50 $\mu\text{m}$  creates a thin and delicate substrate (analogous to heavy-duty aluminum foil). Stacking or bonding together multiple layers and depositing organic (polymers) and inorganic (metals) materials will create stress in the bonded stack, seen as wafer bowing. Bowing of the bonded wafers is caused by a mismatch of coefficients of thermal expansion (CTE) of the substrates or materials that have been deposited onto the wafer (silicon, copper, photoresist, bonding material, etc.) [3]. Each material and substrate in the bonded stack will expand and shrink at different rates when exposed to a certain temperature. Once the device wafer is thinned and various metals have been deposited, stress in the bonded stack becomes critical. Having a bonding material that can remain compliant while offering sufficient mechanical strength to support the thinned device depends upon several mechanical properties of the polymer. The Young's modulus,

tensile strength, and melt rheology of the polymer all play a role in how the bonding material will behave at higher process temperatures and under stress. Being able to bond and debond at relatively low process temperatures will help to minimize stress in the bonded stack, reducing bowing and preventing damage to the thin device wafer.

Single-coat, spin-applied bonding materials are simple and robust and provide the least expensive bonding process in terms of cost-of-ownership. However, using a single bonding material chemistry that can perform and survive all of today's backside processes and then cleanly debond using a sliding, solvent bath, or lift-off method, is becoming a thing of the past. Most of today's sensitive bonding and debonding processes require a bilayer or multilayer approach to temporary bonding. Release layers and laser lift-off layers are now being used extensively with temporary bonding materials. These types of debonding processes can be done at ambient or low temperatures with minimal force needed to debond the carrier from the thin device wafer.

### Solvent Removal/Cleaning the Device Wafer

Once debonded, the carrier wafer can be cleaned using any process the customer chooses. The thin device wafer requires a delicate cleaning process to preserve and protect the expensive die. Solvent removal of the remaining bonding material is the preferred method. Once the device wafer has been mounted to a film frame for support, a

Thermoplastic		Thermoset	
+ temporary/easily removed	- limited thermal stability	+ permanent film	- limited reflow
+ excellent melt/reflow	- moisture sensitive	+ mechanically strong	- difficult to remove once cured
+ good bond strength		+ hermetic	
+ good chemical resistance		+ good bond strength	

Polar		Non-polar	
+ equipment compatible	- can intermix with photoresist	+ excellent chemical resistance	- higher ionic contamination
+ low ionic contamination	- moisture sensitive	+ hermetic	- less friendly
+ friendly			- incompatible with equipment

Low $T_g$		High $T_g$	
+ low temperature process	- limited thermal stability	+ excellent thermal stability	- high bond pressure
+ low bond pressure		+ rigid	

**Table 1:** Properties of bonding materials.

# Semiconductor-Grade Fluxes for 2.5D and 3D

compatible solvent will be used to soften and dissolve the remaining bonding material. The solvent must dissolve the bonding material without damaging the film frame. Most fabs and OSATs are familiar with and use polar materials and solvents in their equipment sets, and their waste streams will be compatible with polar materials. This makes a polar bonding material and solvent cleaning system more attractive to customers with a lower initial cost-of-ownership.

Basic chemistry teaches us that “like dissolves like,” so polar solvents, such as water, will dissolve polar compounds, such as sugar, while non-polar solvents, such as oil, dissolve non-polar compounds, such as waxes. Polar systems will also be “cleaner” and free from high levels of ion contamination. In contrast, a non-polar bonding material and solvent system will not intermix with polar products already in production and will survive harsh wet backside processes, protecting the device wafer from wet chemistries. These types of bonding materials also have fewer problems with absorption of moisture. Because of their propensity to contain benzyl-type structures, bonding materials formulated in non-polar solvents are more likely to be regulated and less environmentally friendly and contain higher levels of ionic contaminants than their polar counterparts.

## Summary

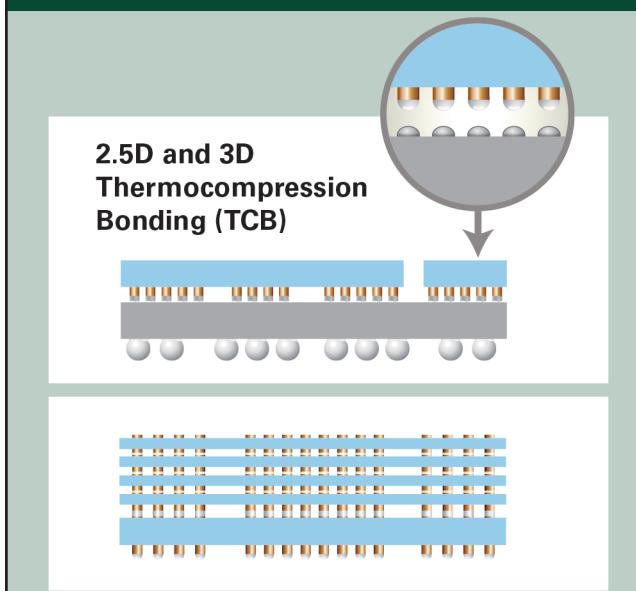
As materials researchers and product developers, we are forever bumping into the laws of physics. Very rarely does one create the perfect, universal product. Product development is done in increments, “baby steps,” while keeping pace with market demand. Materials research is being done to complement new bonding and debonding schemes, which can be done at ambient temperature to minimize wafer stress. Various methods for temporary wafer bonding, which include multilayer and alternative bonding applications, that utilize release and laser lift-off layers are also being explored. Fine-tuning a material chemistry to meet changing industry demands requires the developer to have a thorough understanding of the material’s mechanical properties and the applications in which it will be used. The innovations for tomorrow’s new technologies are being created using materials science, novel engineering processes, and methods development. ☺

## References

1. F. Niklaus, G. Stemme, J. Q. Lue, R. J. Gutmann, “Adhesive Wafer Bonding,” *Jour. of Applied Physics*, 99, 031101, 2006.
2. M. Privett, “3D-IC Thin Wafer Handling Materials Requirements,” *Chip Scale Review*, pp. 24-27, Nov/Dec 2012.
3. Marc J. Madou, *Fundamentals of Microfabrication*, 2nd edition, CRC Press, pp. 262-263, 2002.

## Biography

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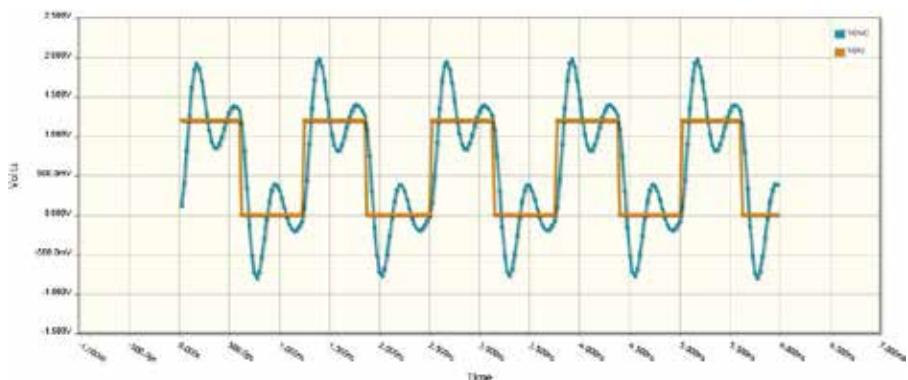
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# Understanding TSVs, Interim Alternatives and Active Interconnects

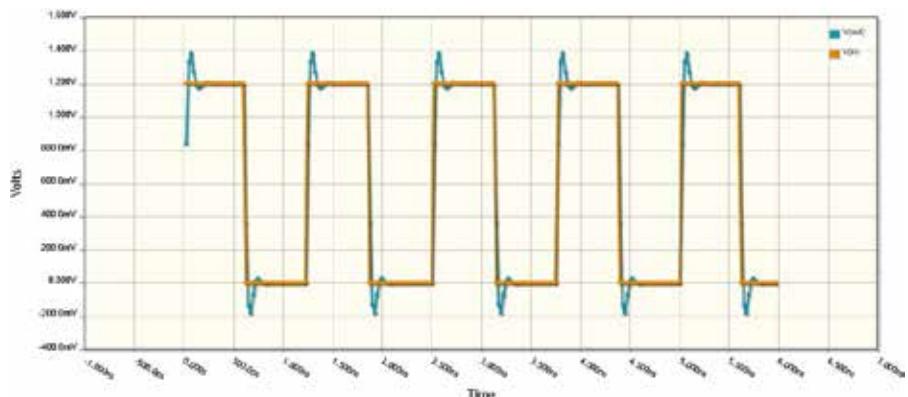
By Dev Gupta [APSTL]

Through-silicon via (TSV) technology is the latest step in the march of advanced packaging technology that started over 20 years ago with flip-chip. Just like flip-chip, the principal motivation for using TSVs to build 3D stacks of chips is the gain in electrical performance. The short solder bumps used in flip-chip technology allow a significant (1,000-fold) reduction in interconnect parasitics (R, L, and C) as well as a 25-fold increase in I/O density compared to the previous generation of interconnect technology, namely, wire bond. Flip-chip in conjunction with build-up organic substrates enabled packaging of 32 and then 64-bit microprocessors that required wide data and address buses, and stable power delivery. However, when multiple dice (e.g., microprocessors and DRAMs) were to be integrated on the same planar substrate, long interconnects on the relatively coarse-pitched ( $15\mu\text{m}$  lines and spaces) build-up organic substrate could not be avoided. This led to limits on the operating frequency due to propagation delay and signal integrity issues, as well as the power lost to drive the signals through the long interconnect lines on the substrate. Tighter integration of multiple silicon chips on fine geometry Si substrate (the so-called multi-chip module-deposited, or MCM-D) found only limited adoption because of its high cost compared to single-chip solutions from wafer fabs able to afford the latest process node.

At last, the advent of TSV technology has made it possible to eliminate long horizontal runs of interconnect lines from chip-to-chip in a 2D MCM. Chips with TSVs are stacked vertically



**Figure 1:** Simulated Input and output (in blue) waveforms in a PoP package at a clock rate of 800MHz. The idealized input waveform is rectangular and varies between 0 and 1.2V. Parasitics of a conventional PoP package make the output oscillatory, thus limiting the data transfer rate between chips connected through such packages.



**Figure 2:** Simulated Input and output waveforms in a 4-die stack with wide I/O using TSVs and buffered on die interconnects at a clock rate of 800MHz (current LP DDR 3). Compared to **Figure 1**, the output waveform (in blue), is sharp even at 800MHz because of the reduced parasitics of TSVs.

and then bonded to provide a large number of short and extremely low loss interconnects between them. When horizontal redistribution layers within a die are minimized through careful floor-planning, very short interconnects result. The parasitics of these short interconnects being orders of magnitude lower compared to even those in a flip-chip package, it becomes possible to get jitter or noise-free signals even at high clock rates – hence faster data transfer rates per line (Gbps), reduction in power

required to drive the signals through the interconnect, and a very high number of inter-die I/O through the TSVs. The impact of package/interconnect parasitics on the shape of output waveform between the processor and memory, and therefore, the data transfer rate, is seen from simulated waveforms of **Figure 1** (for baseline package-on-package, or PoP at 533MHz) and **Figure 2** (for a 4-die stack with TSV at 800MHz).

The sharp waveform possible with TSVs enables breaking the so-called

“memory barrier” (the data rate, or bandwidth in GBps) possible between a CPU and fast memory, which, since the 1980s, has been recognized as a basic limit to computer performance. The other part of the barrier is the power lost in transmitting data through long and lossy interconnects (e.g., in super computers, servers, and even in smartphones), which TSVs can also reduce drastically. This is why there is much excitement and activity about TSVs, and at least until recently, speculation was rife about impending implementation of this novel technology in even cost-driven high-volume consumer electronics (e.g., smartphones and tablets).

An enormous amount of TSV-related activities is now going on around the world at integrated device manufacturers (IDMs) such as, IBM, Samsung, Tezzaron, Micron, etc.), fabless companies (e.g., Qualcomm), IP houses (e.g., Rambus), research laboratories (e.g., imec, Leti, SEMATECH, ASET, ITRI, IME, etc.), academia (e.g., GaTech), leading foundries, and outsourced assembly and test services (OSATs), to name a few. To evaluate the results of all these groups, it is necessary to adopt easy to interpret metrics based on the claimed benefits of TSV technology: high-bandwidth and low power needed to transmit data.

The bandwidth B is calculated from:

$$B = n * T * f \quad (\text{Eq. 1})$$

where n = the data width, or the number of parallel lines, T = the toggle rate, which is 2 for double data-rate (DDR) type memories, and f = the frequency or clock rate.

To take advantage of the large number of I/O lines possible because of the fine pitch of TSVs (typically 50µm), the number n could be as high as 512 (compared to just 64 in baseline 2-channel memory packages), so the same bandwidth B can be obtained at 1/8th the frequency. This approach is used in the wide I/O bus under development for high-speed/low-power memory.

The power, P, needed to drive I/O lines is given by:

$$P = n * T * f * C * V^2 \quad (\text{Eq. 2})$$

where

C = the capacitance of the interconnect lines and V, the operating voltage.

In **Table 1**, the performance of various 3D modules using baseline PoP packaging and using TSV-based stacks are compared on the basis of bandwidth (B) and power (P) as defined above.

Measured data presented in **Table 2** confirms the large improvement in both B and P possible in TSV stacks compared to baseline PoP. However, most of the TSV work reported to date is for small scale development and implementation of even simple memory/controller stacks (no CPU, therefore no redistribution issues) on an industrial scale is eagerly awaited.

#### The implementation of TSV-

based 3D into products has started with sensor/ processor modules, but it has not yet taken off for the much anticipated processor/memory stacks. While much discussion in the industry centers around cost or supply chain, there are unresolved technical issues that need speedy resolution. They are: 1) Local stress fields created by the thermo-compression bonding of dice into a stack that persist and affect device operation; 2) Stress caused by Cu-filled TSVs (large CTE mismatch with Si) affecting electron mobility in transistors surrounding the filled via and causing timing issues; and 3) Nonuniform thermal fields within a stack affecting memory refresh times in an irregular way.

Only now are solutions for the critical issues listed above being explored at various labs. They are:

#### 1. For bonding stress: Non-

3D Packaged Logic & Memory	Physical Details	Bandwidth (GBps)	I/O Power Eff. pJ/ bit	Yield (%)	Remarks
Baseline (WB, FC )					
LP DDR 2/3 in. baseline PoP	2 WB DRAM over FC SoC	<6.4	3.7	high	Billion+ units a year
TSV-based 3D stack					
Memory only					
A. TSV Memory Pioneer	(2004): Cu vias (2007 - ): W vias only 6µm deep 10µm pitch, capped w/Cu bond pad, sequential process	3x	0.6x	NA	4x increase in density, all compared to “baseline,” in small scale production
B. Large Memory Co. (2010- 2011)	Cu vias, 7.5µm dia, AR 10, Wide I/O 4 x 128, 2 memory die stack, 200MHz	12.8	0.78	67-76	Caused much excitement
C. Memory Co. (2012 - )	4 nos. 1Gb DRAM over controller, 1866 Cu vias, 5µm dia 50µm long, 60µm pitch, Cu-Sn reflow	128	10.5	NA	Later claim 70% less energy/bit compared to current DDR 3 tech., uses SERDES link to CPU
Logic & Memory					
D. National Lab (2013) MP-SoC w/only FS RDL & 1016 nos. TSVs/ under 1 no. Wide I/O SDRAM	4x128 bits, 200 MHz through Cu TSVs in SoC only, dia 10µm, length 80µm, pitch 40µm, bumps Cu-Sn-Cu dia 20µm pitch 40µm	12.8	0.9	NA	Custom designed SoC with Wide I/O TSVs located in the center, no redistribution needed on back side of SoC
E. Fabless SoC Co.: SoC w/4 nos. Wide I/O DRAM	Cu vias approx. 30µm long, 40µm pitch, 4 memory dice over Logic, all Wide I/O	NA	NA	NA	Modeled effects of packaging stress on electron mobility. Test after 3D assembly showed no increase in memory bit failure rate

**Table 1:** Electrical performance of various 3D modules (PoP and TSV-based).

Package No.	Interconnect/Package Configuration	Clock Rate (MHz)	Bandwidth (GBps)	Normalized I/O Power (%)	Foot print (%)
1	DIMM: packaged DDR 4 on PCB	800	6.4	100	100
2	CPU & LP DDR 2 or 3 in PoP	<800	< 6.4	24	20
3	CPU on FCBGA w/ 4 nos. Wide I/O Memory chips stacked over it with TSVs	200	12.8	4	10
4	CPU & 3 nos. planar Wide I/O DRAM chips on a 2.5D interposer	200	12.8	14	40
5	CPU & separate stack of 3 nos. Wide I/O DRAM chips with TSVs, all on a 2.5D interposer	200	12.8	19	20
6	CPU & LP DDR3 in Stacked FOWLP with pkg. vias @ 0.3mm pitch	400	6.40	16	20
7	APSTL SuperPoP (baseline PoP modified by inserting active interconnect chip between CPU and DRAM)	800	12.8	8-12	20

**Table 2:** Performance of packages based on 3D TSVs and interim technologies.

metallurgical bonds (not Cu-Sn, not even Cu-Cu thermocompression) but low-temperature and low-pressure Cu-Cu bonding to take advantage of covalent bonds possible (after CMP) at the atomic level.

**2. For TSV stress:** Maintain a keep-out zone around each Cu-filled TSV but lose real estate (for digital, 3x the TSV diameter, for analog even larger). As the stress field depends on the square of the TSV radius, work has only just started to shrink the TSV diameter (from 5 to, say, 2µm) while maintaining its length (development of processes, e.g., for etch, Cu plating to fill vias and reliability for TSVs of AR>10).

**A non-obvious solution from an industry pioneer:** Many of the issues (1 and 2 above) can be avoided if Cu is replaced as a via fill material by materials (e.g., tungsten with a smaller CTE mismatch to Si). For the last few years, a small US-based company has been doing just that, using W as the via fill material. Though W is both brittle and a poor electrical conductor compared to copper, limiting the via diameter to 1.5µm and length to 5 or 6µm does the trick and allows the use of

the standard chemical vapor deposition (CVD) process used to metallize wafers. With W, there are no “copper-pumping” type issues, nor any mismatch stresses, thus freeing the location of TSVs from stress constraints and further improving stack electrical performance because of the shorter interconnects on redistribution layers. Because of its non-obvious advantages, this clever choice deserves more in-depth evaluation as do non-wafer fab type via fill alternatives, such as vacuum filling with molten low stress solders.

**3. For non-uniform temperature fields:** Development of heat spreaders between the dies in the stack, conductive underfill materials.

There are unresolved issues in the TSV process flow as well. One such issue is the need for backup wafers when a parallel rather than sequential wafer thinning operation is carried out to reveal the buried TSVs after which bond pads are plated on them. While the former has the potential of higher yield and throughput, issues with temporarily attaching/detaching the thinned wafers from the backup wafer and subsequent handling damages to the thinned wafer

have been significant. Even as new laser activated adhesives get developed to address the detach stress problem, questions are being raised about the wisdom of the parallel approach when the sequential process (as practiced by A in **Table 1**, which shifted to W vias), though lower in throughput, at least does not require any of these additional steps.

It should be clear that more comprehensive and accelerated development is needed before TSV-based 3D stacking of processor and memory can be ready for even cost-insensitive applications (e.g., supercomputers or medical electronics/implants). Even after the technology is ready and affordable, to get the best performance, it would still be necessary to redesign processor chips so that additional redistribution lines to connect to orthogonal memory chips are minimized. Otherwise, the full benefit of TSVs on electrical performance will not be realized.

### Interim Solutions

While TSV development continues in fits and starts, a whole variety of interim interconnect/packaging solutions are being developed to address the memory bandwidth issue to a varying degree and are discussed below.

**2.5D Si interposer with TSVs.** By using a Si substrate with fine lines and spaces (0.6-1µm), as well as TSVs, and attaching chips on top by fine-pitch (50µm) micro-bump flip-chip, the interchip distance in the module is reduced greatly compared to PCBs, or even organic substrates and interconnects are shortened, thus improving both bandwidth (B) and power (P). Secondary benefits are: 1) the isolation of Si chips with weak extremely low-k (ELK), etc., (as there are no CTE mismatch issues for Si-Si bonds) from second-level organic substrates, 2) the ability to integrate bypass capacitors on the interposer right next to signal bumps so parasitic inductance, L, is minimized, and 3) easy heat removal from the exposed die backside. However, the cost of a large Si substrate processed in a wafer fab is a hindrance just like the

MCM-D from an earlier era and other materials such as improved organic substrates or large panel - processed glass substrates may offer just enough routing density for chips (e.g., graphics processing units (GPUs) that are not as I/O intensive as field-programmable gate arrays (FPGAs).

Buoyed by the adoption of 2.5D interposers for commercial products since 2010 to integrate partitioned FPGAs, and thus maintain high yield in spite of using a then immature 28nm process, many configurations of 2.5D interposer-based modules are now being considered/evaluated. However, not all of them may be able to replicate the yield bonus in case of FPGAs that offset the high cost of the interposer. Before embarking on a 2.5D evaluation/build for a given interposer technology, it would be best to assess the benefits and costs by taking into account appropriate metrics (maximum bandwidth possible, power dissipation, I/O power savings, footprint/interposer area/cost). In **Table 2**, the results of electrical modeling for bandwidth and I/O power are presented for several module configurations: 1 and 2) Board/substrate-based; 3) A true 3D stack using TSVs; 4 and 5) Versions of 2.5D modules (CPU, wide I/O memory) including one that uses stacked wide I/O memory with TSVs; and 6 and 7) Interim solutions derived from traditional packaging.

From **Table 2** it is seen that compared to memory in a DIMM (package #1, used in servers) a true 3D stack (#3) can reduce I/O power (loss in interconnects) by a factor of 25 and the footprint by a factor of 10. Replacing a baseline PoP (#2) as used in smartphones by #3 could cut I/O power by as much as 6-fold, and footprint by 2-fold, rather tempting for battery powered handheld systems like smartphones since the percentage of power lost in the interconnect has been rising with each generation of DRAM in a PoP (**Figure 3**).

A module using 2.5D interposer (#4) technology (which has lower risk because no TSVs are needed in the die) can deliver a 7-fold savings in power but suffers from an increase in cost because of the large Si interposer

with fine (0.6 $\mu$ m) lines that have to be processed by the dual-damascene process. Stacking all the memory chips (#5) would shrink the interposer and its cost, but would still require a mature 3D TSV technology – which, even when available, would do nothing to improve the power loss compared to package #4 (as interconnect runs in the lossy Si substrate, at a minimum half the sum of chip dimensions, would dominate over

the TSV stack).

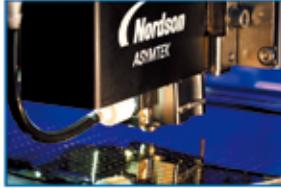
**Double-sided packages using interposers or other substrates.** To avoid using immature TSV technology in active dice, as well as to reduce the size of expensive Si interposers with TSVs, double-sided packages using Si interposers or even the finest pitch organic substrates are being evaluated. To obtain best electrical results, the interconnect length (i.e., redistribution

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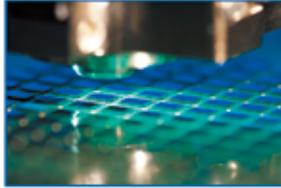


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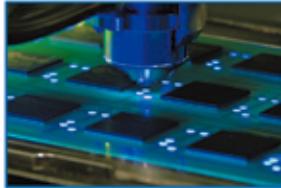
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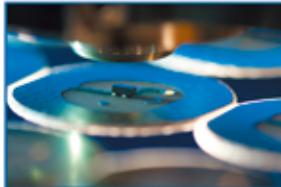
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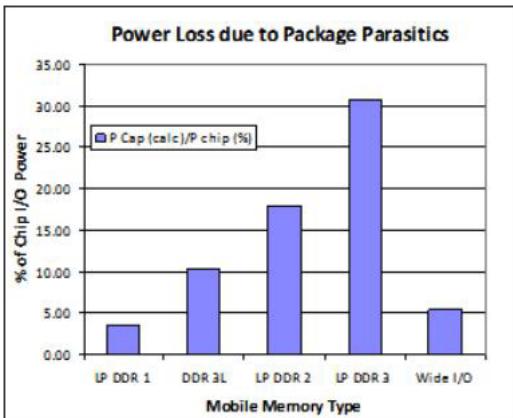
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**Figure 3:** The rising impact of package parasitics in the power required to transfer data between system-on-chip (SoC) and memory in conventional PoP packages. Note the dramatic improvement for wide I/O with TSVs at an equivalent bandwidth.

layers, through-vias, etc.) between the dice on both sides of the substrate needs to be minimized. A memory IP company has built test vehicles using both types of substrates and test chips including a single layer of memory. The company has characterized losses and established design rules for various interconnect features (TSVs, micro-strip lines) using both measurements and modeling.

**Stacked fan-out wafer-level packaging (FOWLP).** OSATs, too, have realized that there are issues with TSVs as developed so far in wafer fabs and are reusing their WLP technology to provide stackable thin packages that combine the traditional virtues of packaging (i.e., protection of bare die, known-good die) with avoiding TSVs in the active dies by offsetting the vertical interconnects to the periphery of the package (as in PoP, but no wire bond used even for memory chips). It is also possible to embed passives for decoupling in the stackable FOWLP thus created. Though the wafer-level redistribution layer necessary in this configuration does add to interconnect parasitics, it is still possible to cut I/O power by 5-fold compared to #1.

**PoP packages with dense vertical interconnect (wire bond, flip-chip).** The typical pitch of vertical interconnects (solder ball, solder filled vias in molded die) today are 0.5mm and they are placed two deep around the periphery of the two vertically connected sub-

packages in a PoP package that is used in every single smartphone and a majority of tablets. Even in the largest PoP in use today (14mm sq.) the maximum number of I/O (DQ) lines cannot be increased much over the current 64 bits for dual-channel memory. The parallel data width can, however, be greatly enhanced by increasing the number of vertical interconnects. Approaches reported so far include replacing the solder balls of vertical interconnects with fine-pitch flip-chip (even Sn capped Cu pillar bumps) or wire bonded Cu pins at a pitch as low as 0.25mm and five deep – giving a total pin count around the package periphery of over 1,000 for a 14sq. package. They mimic wide I/O with TSVs at least in I/O count, and therefore have the potential to deliver even at lower frequencies (where normally inductive noise is lower, signals are cleaner, eye diagrams have larger openings, all lowering the chance of bit errors) a high bandwidth to equal that of 3D TSV stacks. This approach, however, does not address the improved power efficiency possible with wide I/O using TSVs.

$P = B * C * V^2$  (Eq. 2), can be rewritten as directly proportional to the bandwidth, B (Eq. 1), as follows.

$$P = B * C * V^2 \quad (\text{Eq. 3})$$

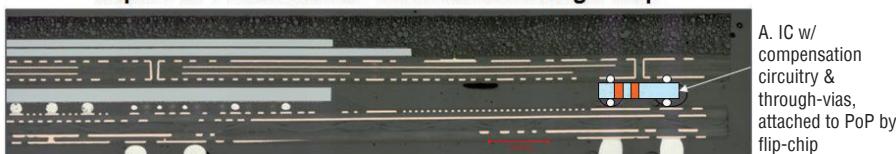
So merely increasing the number of vertical interconnects will not reduce the power loss in I/O so long as the bandwidth, B, stays the same and nothing is done to reduce the capacitance C to approach that of a true TSV (about 50fF). This is the drawback of the approaches to improve baseline PoP technology as described above. Moreover, by shrinking the pitch of the vertical interconnects, these designs would also increase their parasitic inductance (L) and thus run the risk of increasing the induced noise and limiting the maximum permissible clock rate (and bandwidth), perhaps well below the desired 800MHz.

**APSTL's Active Interconnect and Super PoP.** Interconnects are electrical circuits, but until now, interconnect performance has been improved by mechanical means, e.g., by shrinking them. The penalty for taking the mechanical approach has gotten worse with each iteration, e.g., in case of flip-chip, the consequences of changing to less plastic Pb-free solder alloys or the effect of chip/package interaction on ELK dielectrics. With TSV-based 3D stacking, this penalty for inserting the simple-looking TSVs into active dice and then stacking them by using flip-chip bonding only gets worse. At APSTL, we have taken a very different approach to improving interconnect performance, not by physically shrinking the lines, but by inserting compensatory circuitry into them. This is the concept of “Active Interconnects” and patents have been filed to cover this approach and its implementation into a range of applications ranging from servers to smartphones.

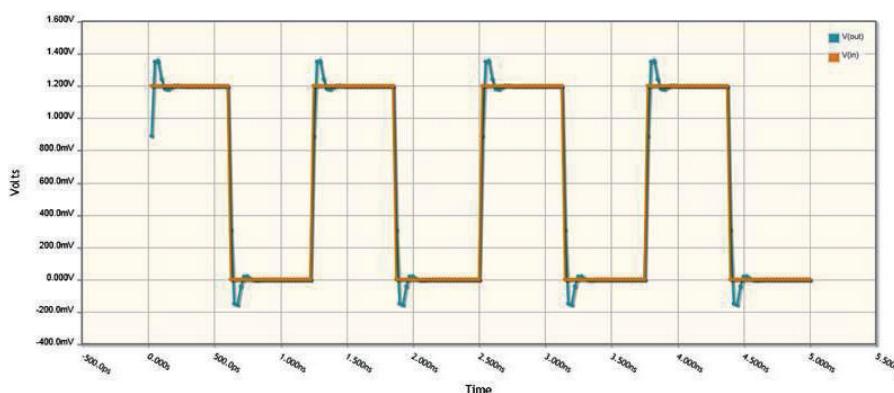
Given the low cost of integrated circuits and the anticipated need for data width not rising above 128 bits (4 channels, each 32-bit wide) anytime soon, it is possible to incorporate the additional compensatory circuitry into chips nestled between the two layers of a PoP package (Figure 4). The resulting waveform (Figure 5) resembles that in a TSV-based 3D stack (Figure 2) with all attendant benefits. This improved PoP package is called SuperPoP [1] and as it uses only existing technologies and avoids yield/reliability risks, the additional cost would be a fraction of the TSV route.

Any serious effort to get TSV-based 3D technology ready for commercial adoption would benefit greatly from technically savvy and confident program management capable of identifying and boldly making the necessary changes to not just solve individual challenges, but also simplify them as a whole – much along the lines of the small US company that switched from Cu to W vias and uses sequential rather than parallel wafer thinning. The TSV approach, however, still remains a very mechanical approach (physical changes to the interconnects)

### Super PoP : Baseline PoP modified with Magic Chip



**Figure 4:** Cross section of a Super PoP, a baseline PoP package that was upgraded for higher bandwidth and lower I/O power loss by inserting compensatory circuitry for each data line. The additional circuitry is contained in 4 ICs, 1 of each (marked A) is assembled at the periphery between the two levels of the baseline PoP.



**Figure 5:** Output for SuperPoP at 800MHz; the output waveform looks like that out of a 3D stack with TSVs (Figure 2).

to solve an electrical problem—an approach that is showing its limits (ever more complex processes, stress effects on device, CPI magnified by stacking, etc.). An alternative is a shift to using electrical solutions (e.g., additional circuitry) to solve electrical problems as realized in the active interconnect concept and Super PoP technologies. ☑

### Reference

1. D. Gupta, "A Novel Non-TSV Approach to Enhancing the Bandwidth in 3-D Packages for Processor-memory Modules," Proc. 2013 IEEE ECTC, pp. 124-128.

For additional references on specific topics please contact the author.

### Biography

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# Comparing Coolant Technologies in Semiconductor Wafer Test

By Klemens Reitinger [ERS electronic GmbH]

T

he need for accurate and reliable temperature control of semiconductor wafers undergoing electrical test is not a matter of “if” but of “when” and “how.” This is true both in laboratories and on wafer test floors at semiconductor manufacturers and at their production partners. The purpose of this article is to outline a short history of how wafer thermal test has changed over the past 40 years, in particular with reference to the cooling method employed, and to promote a discussion of the direction it will take in the future.

## Background

The original wafer thermal chuck was controlled by literally one single Peltier element inside of a 1 ¾” chuck. Our company built it in 1971 for a pioneer in semiconductor manufacturing. It was used in a simple wafer sort application and provided active heating and cooling. A wafer sort application checks the functionality of the chips on a wafer prior to its being sawed into individual devices. This gives the manufacturer the opportunity to discard the bad devices early on in the production process thereby saving the packaging and final test costs for those devices, as well as to match the quality of good devices to markets.

The checks performed during wafer sort ranged from a simple determination of pass/fail to a more complex category sorting of the devices into various levels of “pass,” often temperature related. Devices that passed testing at +25°C, but failed at higher or lower temperatures, could not

be sold at the same price as those that had undergone testing in the upper and lower ranges. Classic applications for devices requiring a “pass” during both hot and cold test were in automotive, space and military applications, as well as high-end logic applications, such as microprocessors and graphics processors. These are extremely attractive markets in terms of their average selling prices and their ability to survive economic down turns.

The simple heating concept behind most hot testing of semiconductor wafers today is the same as we see in everyday cooking applications. A resistance heater is built into a plate (i.e., chuck) that is slightly larger in diameter than the wafer that will rest on it during test. A good “hot chuck” is recognized not only by how hot it can get, but how fast it gets there, how uniform the temperature is across its diameter, how rigid and flat it is, and how electrically quiet it can remain during test. A simple hot chuck is also very reliable and easy to maintain.

As the need for cold test began to increase with the increase of semiconductor devices in automobiles, as well as in space and military applications, a common and very successful solution came to market that combined the resistance heater of the simple hot chuck together with the flow of a coolant through the chuck.

## Cooling is critical

To control the temperature of the chuck - and thus the temperature of the wafer under test - tool designers employ a number of technologies. The

most common ones are Peltier elements, liquids, and gases. Each one has its merits and its drawbacks.

**Peltier elements.** This technology utilizes the known thermoelectric effect. Peltier elements are basically heat pumps: an electric current pushed through the element in one direction causes it to heat up. When current is pushed through the element in the opposite direction, it cools down. Peltier devices can be used to control temperature in both directions - for heating as well as for cooling. How hot or how cold the element becomes is controlled by the amount of current pushed through the element. These properties make Peltier-based wafer chucks both versatile and with a resolution as good as the current control electronics. Peltier-based systems are compact and relatively easy to integrate into test equipment.

But there are drawbacks to using Peltier elements in wafer chuck systems. Because they ostensibly have no moving parts, they carry an inherent promise of reliability attached to solid-state systems. Experience shows, however, that Peltier elements cannot always deliver on this promise of reliability. The strain generated through multiple heat cycles and the resulting mechanical tensions cause mechanical failures. Because Peltier elements are made up of multiple semiconducting elements connected in series, a single interruption causes the entire system to fail. Though the failure rate might not be very high in objective terms, their reliability typically does

not meet the requirements of semiconductor production where failures in the value chain are not tolerated. Another shortcoming of Peltier elements is that they cannot be used for tests where temperatures above 200°C are required; their solder points begin to fuse at these high temperatures. Many test applications, in particular those in laboratory environments, require temperatures of up to 300°C. Thermal systems based on Peltier elements would be disqualified for these applications. Additionally, one would still need some kind of coolant to get rid of the dissipation loss.

**Liquid Coolants.** Pure water is theoretically well suited for the temperature control of chucks. Its limitations are well defined and obvious: at normal air pressures, water cannot be used for temperatures below freezing or above the boiling point. This range of 0°C to 100°C is much too narrow for real-world wafer test operations. In the event of coolant leakage, there is a danger of causing short circuits in sensitive electronics near the coolant hoses. Even distilled water quickly ionizes and readily conducts an electrical current.

A partial workaround for the narrow temperature range problem can be found by using a mix of water and ethylene glycol similar to the antifreeze used in car radiators. Such a mixture can expand the operating temperature range significantly. However, modifying these properties of water also will influence the thermal characteristics negatively. Additionally, the danger of short-circuits in the nearby electronics remain and cleaning of leakage will even get more complicated.

Thermal systems utilizing water or water/ethylene glycol mixtures as the coolant are rarely used in semiconductor testing today. Much more widespread is the use of synthetic cooling liquids such as perfluoropolyether (PFPE), sold under various brand names. These inert liquids are chemically stable as long as the operating limits are not exceeded, and they can be used in a broad temperature range typically from about -70°C to +120°C. Because they are very poor conductors of electric current, they do not pose a danger of short-circuits in the case of leakage. Compared to water,

#### Cooling Power with Typical Boundary Conditions

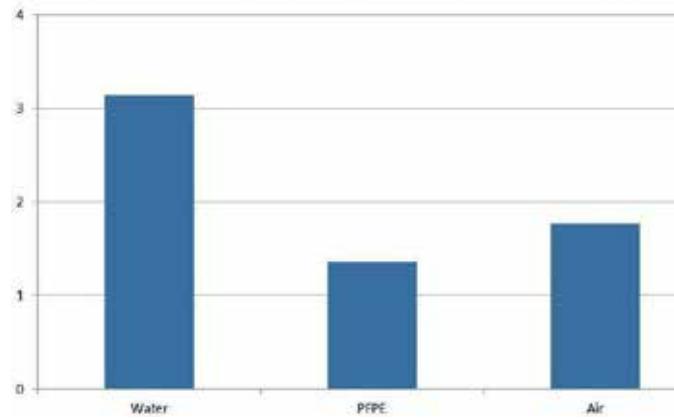


Figure 1: Cooling power with typical boundary conditions.

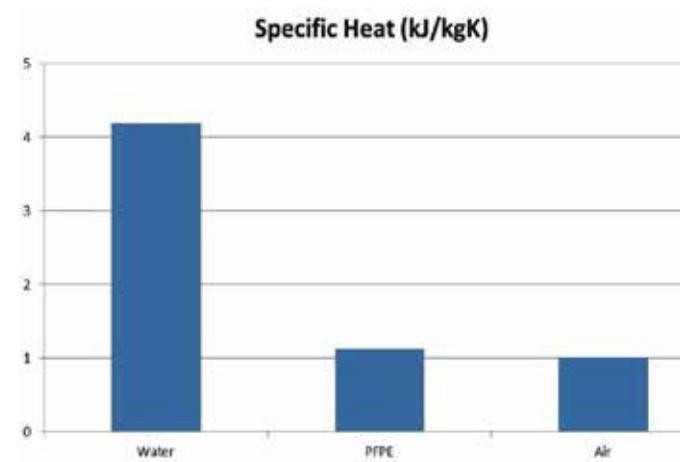


Figure 2: Specific heat conditions for water, PFPE, and air.

the thermal properties of these coolants are less suitable for heat removal. Depending on the type, these coolants are sometimes closer to air than to water (Figures 1 and 2).

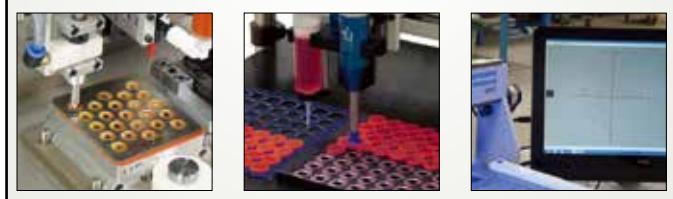
In contrast to water, even to purified water, synthetic cooling liquids, however, are rather costly. Since these liquids evaporate over time even in closed circuits, the systems need regular refills. In addition, they require a complex infrastructure to handle their logistic and environmental implications. Though they are not highly

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toxic, these liquids are subject to hazardous waste legislation that adds to their already high operating costs. In case their operating temperature range is exceeded, there is a theoretical risk that they could disaggregate into their chemical constituents. These can include highly toxic and otherwise hazardous gases such as fluorine or chlorine. This limitation restricts the use of PFPE-based liquids to relative low temperatures; at the same time, their utilization is associated with high costs and technical complexity.

**Direct injection of pressurized gas refrigerants.** Instead of using a refrigeration system to chill a secondary coolant in a heat exchanger and circulating that coolant through the wafer chuck, this method is more direct. The chuck itself becomes the evaporation chamber of a closed refrigeration system as refrigerant gases under pressure are pushed into the chuck where they expand and remove heat energy. Chemically, these gases are functionally identical to the gases used in air conditioning systems and in household refrigerators. While today's commercially available refrigerants are no longer considered harmful for the ozone layer, some are inflammable. This holds true for some of the most popular refrigerants such as butane or ethanol.

The direct injection of refrigerants along with the integration of the evaporator into the chuck opens interesting technology perspectives. Such configurations can handle very high amounts of energy at extremely high levels of


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a)

## Using Cooling Air for Purge

Task	l / min
Cooling Air = Purge Air = Pre-Cooling Air	330
Air Dryer	150
<b>Total</b>	<b>480</b>

b)

## Not Using Cooling Air for Purge

Task	l / min
Cooling Air	330
Purge Air	330
Air Dryer	150
<b>Total</b>	<b>810</b>

**Table 1:** Comparison a) Using cooling air for purge, vs. b) not using cooling air for purge. As can be seen, the usage of cooling air for purge significantly reduces the air consumption of the system.

efficiency, effectively almost 100%. On the downside, these systems are very difficult to engineer into equipment that has moving parts (such as the table that moves a wafer chuck). They require very high gas tightness, which rules out the usage of flexible plastic or rubber tubing. The rigid metal gas pipes needed to hold these gases render the resulting test systems inflexible and clumsy. This intolerance to leakage also translates into relatively low reliability. Every small leak can cause operation interruptions. Typically, direct injection systems have high acquisition and operating costs.

**Air.** Virtually every semiconductor manufacturing line has a ready supply of pressurized clean dry air (CDA) easily accessed at the wall utilities behind the equipment in the factory. In contrast to water, other liquids, and synthetic cooling agents, when air is used as the coolant, it does not impose any limitations with respect to the temperature ranges

required for semiconductor test. In addition to any use as a coolant, large amounts of CDA (or other very dry gas) will be necessary as an environmental purge to prevent frost in the wafer test area inside of the equipment. Failure to reliably prevent frost in the test area can result in the destruction of the very expensive electrical probes used during cold wafer test. That requirement for environmental dry air (or gas) purge exists independent of whatever coolant is used to achieve the temperature in the wafer chuck. The drawback of air as a coolant is its relatively low thermal capacity. However, given the availability and flexible handling of air, this drawback does not have a high material impact.

The heat exchangers used in ERS's AC3 thermal system effectively cancels out the drawback of the lower thermal capacity, while benefitting from the smaller footprint, lower utilities costs and application flexibility associated with using air as the coolant. The patented heat exchanging system on the AC3 extracts maximum cooling from the chilled air and then utilizes that same air to purge the test area. This effectively reduces the consumption of air and mains power (**Table 1**).

### Future Perspectives

Moore's law predicts the continuation of the trend towards smaller device geometries and increasing integration of functions in semiconductor chips. With ever-more functionality and complexity, the test procedures required will also get more complex. Add this to the perspective of manufacturing on 450mm wafers, and you see steeply rising requirements for test systems. For example, multiple concurrent tests on a wafer result in multiplying the mechanical pressure exerted by the test probes. Forces of up to 3000N are absolutely realistic. Under these conditions, the mechanical stability of the chuck must be guaranteed under all circumstances; tolerable deviations are in the single-digit micron magnitude. At the same time, the electric noise

generated by the test equipment must not affect the test results, which means noise levels in the femto-ampere range. Additionally, temperature deviations resulting from the heat generated by the device under test must be corrected within milliseconds. We have already determined that our air cooling concept is scalable for 450mm chucks. The design principle of air as the cooling agent for most use cases enables us to

meet all these challenges now, and in the foreseeable future. ☺

### Biography

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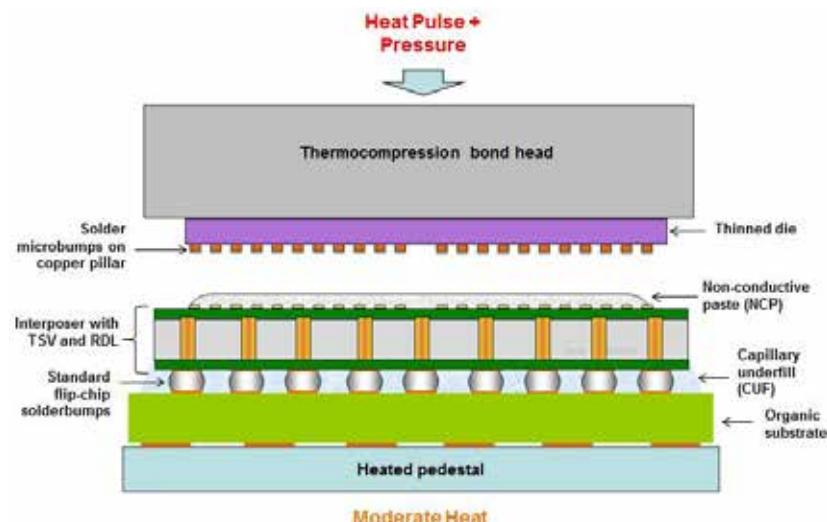
# Thermocompression Bonding (TCB) for Dimensional (2.5D and 3D) Assembly

By Andy C. Mackie [Indium Corporation]

In 2011, Amkor and Xilinx announced [1] the joint development of copper-pillar flip-chip/interposer technology using thermocompression bonding (TCB) assembly processes. A basic schematic of the final TCB joining process is given in **Figure 1**. Flip-chip assembly using thinned die with solder microbumps on copper-pillars is fast becoming a standard process, and is part of the lexicon of “dimensional assembly” (2.5D and 3D). TCB for die onto interposers or coreless substrates is now a critical manufacturing technology, taking over from standard placement and reflow processes.

TCB using non-conductive paste (NCP) combines three processes into a single tool: 1) Precise placement of the die; 2) Dispensing of the NCP; and 3) Reflow of the stacked assembly. TCB is obviously in marked contrast to the standard sequential flip-chip (C4) processes of placement and reflow. **Figure 2** shows a basic flow diagram for the contrasted processes applicable to dimensional assembly. The process flow possibilities increase significantly once 3D processes (die-to-die (D2D), die-to-wafer (D2W) and wafer-wafer bonding) are considered.

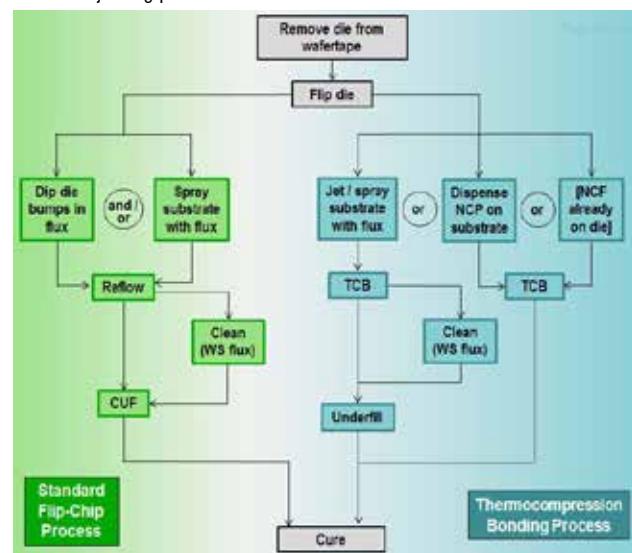
TCB is taking over from standard flip-chip assembly processes (**Figure 3**) as the dominant technology due to two factors: 1) The increasing potential for the unreliability of the final soldered joints (such as bowing due to the use of thinned die), and 2) The inability of the standard process to deal with NCP, non-conductive film (NCF) and similar emerging assembly materials. However, this means that new failure modes in



**Figure 1:** Basic schematic of the final TCB joining process.

equipment, materials, and processes are also emerging. Just some of the issues with TCB with NCP are given in **Table 1**. Please note that some of these issues may also be seen with NCF assembly, which is much less mature than the NCP process.

For packaged devices costing many thousands of dollars, a slow sequential process may be able to successfully balance the reliability needs of large die bearing many tens of thousands of I/Os against low throughput, but for standard copper pillar assembly processes, especially those aimed at consumer applications, speed is of the essence.



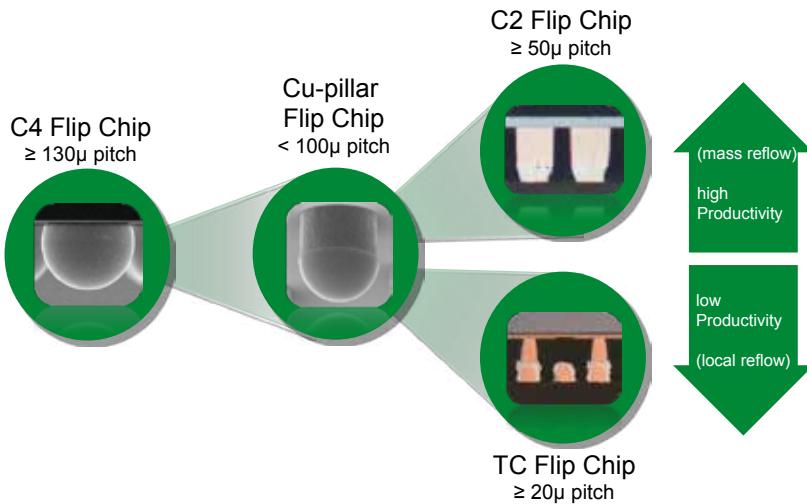
**Figure 2:** Flow diagram for contrasted processes applicable to dimensional assembly.

## Current TCB Equipment

The leaders in TCB equipment for slower, standard 2.5D (copper-pillar/microbump flip-chip-on-interposer) assembly processes in the

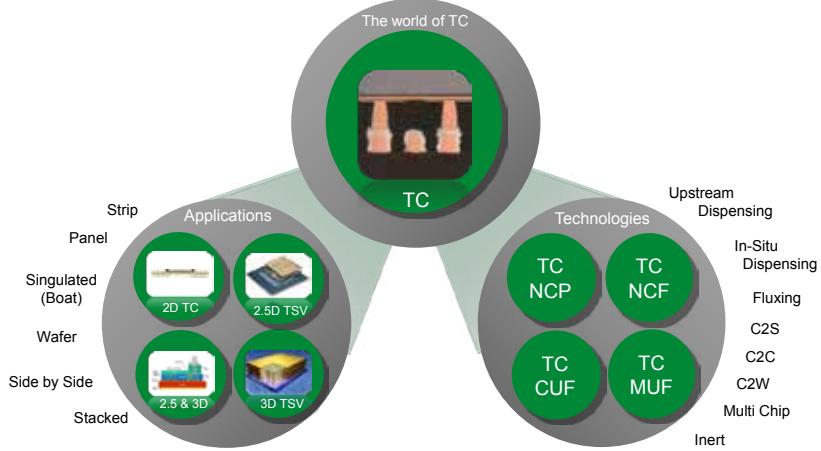
a)

## SOLDER FLIP CHIP EVOLUTION



b)

## THE DIVERSIFIED WORLD OF TC



**Figure 3:** a) The solder flip-chip evolution; b) The diversified world of TC. SOURCE: BESI

last several years have been Japanese manufacturers such as Toray and Shibaura. These companies worked with outsourced assembly and test (OSAT) manufacturers such as ASE, Amkor, and others to adapt standard flip-chip machines, adding in capabilities for

precision placement (often claimed to be down to +/-2µm), along with the ability to provide significant pressure (10kg or more) onto the die, as well as ways to introduce rapid heating and cooling. However, as the 2.5D assembly process has evolved, newer entrants into

the equipment market are emerging, each with its own approach to market needs.

### Interview Questions

There are tens of equipment suppliers selling, or planning to offer, capital equipment into the dimensional assembly market space. The author asked a number of these companies, including some in the development phase, if they would be willing to answer questions about the TCB process. The four respondents who answered favorably were sent a series of questions—and the responses are given below. Those interviewed are therefore just a sampling of the manufacturers engaged in TCB equipment development, and we know that others not mentioned in this article will emerge in the coming months.

### What major challenges with materials for TCB still exist?

**BESI:** TCB is quite a complex process, and the use of proper materials is crucial. If the appropriate design rules are not met, or the manufacturing tolerances of substrates and bumps are not well controlled, then higher bond forces are required to overcome the insufficiencies. However, higher bond force requirements usually make process windows smaller and processes slower, as the process must be given time to smoothly build up the force. Pre-applied NCP (or NCF) materials add significant complexity, as they need to combine excellent properties for adhesion, reliability, wetting, and fast curing. Everybody is looking for fast curing NCP/NCF materials without a compromise in the complementary properties, but looking back to the moderate progress made in the preceding three years, such a fast-curing adhesive seems still to be a major challenge.

**Finetech:** Since Finetech's earliest days 20 years ago, our equipment has been capable of thermocompression bonding for virtually any application. We have helped in so many market

Concern	Description	Potential Causes
Throughput	Units per hour (UPH)	Time of NCP precision dispense; precision placement of die into viscous paste; TCB heat profile time
Voiding	Bubbles in the NCP	Flux reaction products; poor dispense or die-placement process; bubbles in NCP before application
Bridging ("extrusion")	Solder connecting adjacent joints	Overpressure during bonding process; no z-axis control; bubbles in NCP
Slippage	Die misalignment during placement	Radially asymmetrical force in the thinning TCB film; inability of bond head to retain die alignment
Fillet unevenness	Wetting of NCP onto edge of die varies	NCP dispense pattern (asymmetrical); uneven die singulation
Particulate entrapment in solder joint	NCPs all contain solid particulates	Simple capture of particles in solder joint during TCB
Unreliable solder joints	Non-wet opens and incomplete wetting of solder onto metallization	Warpage before or during bonding; non-isobaric compressive force; particles blocking solder joint formation; insufficient pressure during TCB process
Damage to ELK/ULK layers	Thinned die at smaller nodes	Non-isobaric TCB process; high speed die-placement

**Table 1:** TCB/NCP shortcomings.

segments over that time. The areas of challenge almost always come down to process limitations in heat, force, time, or chemistry. First, seeing copper-pillar devices at the R&D level, we have worked to provide the process flexibility needed at that stage. Finetech strives to provide all bonding options for a product being built.

**SET-NA:** Joining materials for TCB face challenges such as price, performance, scalability, and costs. Of these, scalability to true microbump feature size is critical to support shrinking design rules. Upcoming multi-level assembly process flows, such as 3D integration, require special attention to bonding materials that will minimize or even eliminate the temperature excursions required as multiple chips are bonded in succession to a substrate in stacked fashion. The thermal excursions normally required for reflow bonding or high-temperature TCB consume process time, can create misalignments, and materials stresses when joining devices with large differences in CTE. Low-temperature or room-temperature TCB

will be a major milestone in enabling large-scale heterogeneous integration.

**Palomar:** We see two main challenges with TCB process materials: temperature and placement force. TCB is a soldering process and so requires temperatures suitable for solder reflow. TCB processes require a higher thermal profile than conductive paste processes, such as with silver epoxies. Although there have been process advancements toward NCP for flip-chip assembly, conductive paste (such as a cured epoxy) is still a viable option for thermally sensitive assemblies as the curing process requires lower temperatures than solder. There are multiple methods of curing, but typically, thermal curing is at a lower temperature than solder temperatures. The disadvantage to conductive pastes is that these cured epoxies are not as thermally conductive as a solder. NCPs may be used along with conductive pastes to add structural strength, in addition to giving thermal dissipation. TCB typically necessitates a high bonding force (~60g per bump). Material structures need to be adequate

for the higher forces. For example, on a small die, this is not a problem, but in larger die with 50 or more bumps, the combined force can grow rapidly.

### Where do the four major assembly methods: NCP, NCF, and flux with CUF or MUF fit into the needs of different chip markets?

**BESI:** TCB processes using NCP were introduced by Amkor for high-volume chip-to-substrate manufacturing, primarily to overcome the drawbacks of (capillary underfill) CUF for fine-pitch and low bond line (die/substrate distance). NCP gets tricky if dies are getting thin, and thin dies are a key factor for economically-viable TSV. A die thickness of 50µm for logic is now typical, and proper NCP dispensing requires tight process control. The memory industry, which has stacked TSV memory on its roadmaps, are dealing with die thicknesses of 30µm or less, where the epoxy becomes really tricky as the required accuracies of both volume and pattern consistency are at the edge of deposition technology capability. Memory guys are saying, "It took us almost one decade to get the epoxy paste out of memory production, and now, with TCB, it came in through the back door. We hope this time to kick it out a little bit faster!" So many people are working to get the NCF (or pre-applied adhesive on wafer) technology running for thinned die.

In contrast to NCP, the NCF comes with a higher viscosity. Since the glue material has to be squeezed out between the bump and the pad in the initial phase of the TC process, NCF processes need a higher bond force. However, higher bond force for ultra-thin die does not make people feel confident. Another challenge comes with high bump (I/O) count, where NCP/NCF entrapment becomes a serious issue; NCP/NCF may not be completely squeezed out between the bump and the pad, leading to yield loss due to non-wetting.

Thus, a new direction can be seen now. People are again investigating post-applied epoxy processes for TCB packages like CUF and molded underfill (MUF). A common mind-set is that for flip-chip pitches less than 130 $\mu$ m, the CUF becomes tricky (which finally was also leading to pre-applied NCP technology) and needs to be replaced by a new mind set where a new post-underfilling technology might come into place. Datacon TC-bonders provide a fluxer as a standard option, and our sister company, Fico, works on transfer-molding technology for both CUF and MUF. One year ago we demonstrated that copper-pillar flip-chip gaps of 30 $\mu$ m can be filled with MUF without voids, and now 15 $\mu$ m vias with a 1:10 aspect ratio can be filled without voids. This clearly shows that known good technology, such as CUF or MUF for TCB, could enter a new dimension.

**Finetech:** People tend to gravitate toward a “known good” process they are familiar with, and fluxing is a good example. As an equipment supplier and process advisor, we are continually reminding designers that paste and film options are available. I have seen a growth in interest for these adhesive chemistries that had traditionally been used only for chip-on-glass (COG) and chip-on-flex (COF) applications.

#### **What major challenges with the TCB-based assembly process and equipment still need to be overcome?**

**BESI:** Basically there are two challenges: mass production capability and productivity (throughput (UPH = units per hour) and final product reliability). The die processed in a TCB machine are typically expensive, and so any issues associated with yield can result in huge costs. In order to maintain high capability, the throughput is usually compromised, even if the machine could run at a higher speed. The real challenge is to run a robust high-yield process at high throughput.

The reality for many applications is that there are plenty of small pitfalls in mass production, where many of these pitfalls are still waiting to be identified. It took a decade or so for standard flip-chip (C4) production to develop into a robust, well-characterized, process. For TCB we only are at the very beginning. Lab and pilot productions have been completed, but for a variety of products high-volume manufacturing is in its initial phase.

**Finetech:** We offer modules to allow bonding with all these process options, such as controlled flux dipping. Dealing with small pieces of film in a lab is not much different than placing the die. Doing this in a high-volume production environment adds different challenges. Whenever you hold onto a device through the connection process, the equipment cycle time becomes a major factor. However, this thermocompression process has very good yield for finer pitch bonding.

**SET-NA:** Flux with CUF has been used for many years in the assembly of infrared focal plane arrays (IRFPAs). These

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IRFPAs are hybrid structures with thousands to millions of interconnect bumps between detector and readout chips, and represent a logical technology pathfinder for 3D-IC as both pitches and gaps shrink. In IRFPA assembly, bumps as small as 3 $\mu$ m wide have their oxide removed prior to room temperature TCB. This oxide removal reduces the compression force for reliable metallurgical interconnect. Once bonded, many IRFPAs are capillary-underfilled to secure the structure for military and aerospace applications. The hybrid gap is typically too small (3-6 $\mu$ m) for traditional fluxing and subsequent removal, so pre-hybridization etches are often used to remove oxidation from the bumps. As bump diameters shrink down to 3 to 10 $\mu$ m, many IRFPA manufacturers have gone to plasma etching to remove oxidation. SET-NA provides an atmospheric plasma system that quickly removes bump oxidation and passivates the bump surface against re-oxidation so that bond queuing time is not an issue.

**Palomar:** High-force requirements for larger, multiple bump applications (>10 interconnects per chip) can negatively impact product reliability when using TCB. Just as important, process dimensional (x,y,z) precision becomes an issue as the die size and the number of interconnects increase. This is especially true for the challenge of aligning bumps and pads when die and substrates have differing CTEs.

### How is your company addressing these challenges through equipment and process design?

**BESI:** The requirements from our customers are very clear: TCB bonding needs to run robustly with high yield, and it needs to become as easy and productive as C4 flip-chip bonding. Besides the required core equipment capabilities (high accuracy, automated coplanarity, bond control, and thin die handling) one of our focus directions is to provide usability. Our leading TCB

bonder is an evolution of our 8800 platform with the biggest installed base of C4 bonders, so this task has not been too difficult as most of the usability, self-calibration, and auto-diagnostic functions were already in place. Productivity requires high throughput, uptime, and fast time-to-yield. We are using a lightweight construction that can support high placement accuracy, in combination with high bond force based on our patented mechatronic approach (one of our core competencies). The unique machine concept allows for dual head TC bonding on the same strip (or same wafer), and hence, faster substrate throughput to overcome the NCP dry-out issue. The ideal equipment should, therefore, be able to process strips and boats, chip-to-wafer (C2W/D2W) applications, side-by-side or stacked multi-chip, as well as supporting all variants of TCB processes, like NCP/NCF or CUF/MUF, all in a 'tiny' foot print.

**FineTech:** We offer integrated dispense for adhesives, flux, or solder on our bonding systems. A wide range of forces is required for process flexibility. We also developed a special module just for ACF/NCF tack bonding.

**SET-NA:** We are taking a multi-pronged approach. We are maintaining and expanding our historical focus on high-accuracy bonding equipment for critical applications with very small features, and we have also developed an atmospheric plasma system to remove oxides and residual organic films from bonding surfaces, and then passivate them against re-oxidation. This system has proven to be effective on a variety of elemental and alloyed metals, mostly of In, Sn, Ag, and their alloys.

Furthermore, we are also working with key industrial partners to identify and characterize bonding metallurgies that can be quickly cleaned and passivated, and which feature very fast joining processes at very low temperatures to provide connections with high mechanical and electrical integrity for

next-generation applications.

**Palomar:** Flip-chip on a large die (D2D assembly) is supported by a new design using conductive pastes or anisotropic conductive paste (ACP) flip-chip attach processes for radio frequency identification (RFID). Each part requires a bumped 450 $\mu$ m RFID component flip-chip attached onto a PCB array followed by an epoxy underfill. All parts had to be assembled onto a 200mm X 150mm substrate with 179 sites per PCB. Assembly Services supported the RFID die flip-chip attach using the <5um placement accuracy automated 3800 Die Bonder. The underfill step was inherent with the ACP process. Our equipment can support high-precision TCB on small devices with 10 or fewer interconnects, such as high-reliability, high-bright LEDs that commonly require high-accuracy placement of interconnects.

### Acknowledgements

I am indebted to the following respondents who gave a lot of their time to make this article a success: 1) Dr. Hugo Pristauz, better known to the packaging industry as "Dr. Flip-Chip," of Datacon/ESEC ("BESI"); 2) Keith Cooper and Eric Schulte of SET North America ("SET-NA"); 3) Neil O'Brien of FineTech USA ("FineTech"); and 4) David Rasmussen of Palomar Technologies ("Palomar") 

### References

1. <http://www.i-micronews.com/news/Xilinx-2-5D-FPGA%E2%80%99s-coming-off-production-line-closer-look,7717.html>

### Biography

Andy Mackie received his Master's degree from the U. of Bristol (UK) and his PhD in Physical Chemistry from the U. of Nottingham (UK) and is a Senior Product Manager, Semiconductor Assembly Materials, at Indium Corporation; amackie@indium.com

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ASM Pacific Technology Limited 12/F Watson Centre 16 Kung Yip Street Kwai Chung Hong Kong Telephone: 852 2619 2000 Fax: 852 2619 2118/9 <a href="http://www.asmpacific.com">http://www.asmpacific.com</a>	Die Bonders, Flip-Chip Bonders	Various others
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# Acoustic Imaging and Inspection

By Tom Adams [Sonoscan, Inc.]

**S**emiconductor component makers are always interested in ways to improve speed and performance, and to make production easier and less costly. These improvements often change the requirements for the non-destructive acoustic microscope imaging that finds internal structural defects.

In cooperation with manufacturers, we are working to develop new acoustic microscope tools that will provide the inspection that will be needed when new package designs move into production. New tools for automated production inspection, imaging of stacked die assemblies, chip-on-wafer inspection, and imaging of molded underfill flip-chips are reported here.

## Advanced Production Inspection

In many applications, the acoustic inspection of plastic-encapsulated microcircuits (PEMs) and many other component types is performed inline before the components are placed on a printed circuit board. The components are placed in JEDEC-style trays for mass scanning. The purpose of acoustic inspection is to identify components having internal structural defects that may cause an eventual field failure.

The structural defects are voids, delaminations, non-bonds and cracks. Strictly speaking, a delamination is an area where two materials were once bonded but have become separated. A non-bond is an area where the bond between two materials never existed, perhaps because of contamination on one of the surfaces. Although it may be difficult to define the cause of a particular defect when it is seen acoustically, or to distinguish between a delamination and a non-bond, the outcome is still the same – the defect is still a reliability risk.

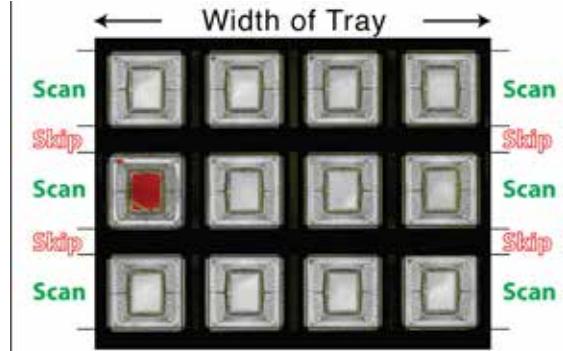
By their type and location, the defects vary in the degree of risk they pose to

electrical performance. A non-bond between the encapsulant and the die face of a PEM is always cause for rejection because when exposed to thermal cycling, it may expand laterally and break a wire bond. Delaminations of the mold compound from the top surface of the die paddle are serious because they may expand laterally under the die attach material. Lengthy delaminations or non-bonds between the top surface of the lead fingers and the mold compound are troublesome because they may increase their length through thermal cycling and open a pathway between the ambient environment (humidity, contaminants) and the die. IPC/JEDEC J-STD 020D makes such delaminations cause for rejection if their length is more than two-thirds the length of the lead finger.

Voids are susceptible to expansion, but to a much smaller degree than, say, delaminations. A small, isolated void in a region of the mold compound that is not near another surface poses a minuscule risk to electrical performance. But a void of the same size that is among the bond wire loops poses a high risk.

All of these defects reflect virtually 100% of the ultrasonic pulse because they are gaps in or between solid materials. Conventionally, the acoustic microscope's transducer scans back and forth across the width of the JEDEC-style tray, moving incrementally along the longitudinal axis after each transit. In this way, the transducer scans the entire area of the tray, including the areas that are between parts and therefore not of interest.

The newly developed system changes the pattern of scanning by skipping over some of the empty areas (**Figure 1**). In addition, it uses two or more transducers instead of one. Suppose



**Figure 1:** Faster acoustic scanning of trays holding parts is achieved when two transducers scan simultaneously and skip over non-part regions of the tray.

that transducer A will first scan a row of four parts stretching across the width of the tray, and that there are seven more such rows in the tray. What happens is this: simultaneously, transducer A scans the first row, and transducer B scans the fifth row. The two transducers then skip over the longitudinal area between the just-scanned row, and goes directly to row 2 (transducer A) and row 6 (transducer B).

The area that is scanned may be further reduced if, for example, only the area of the die in each component needs to be inspected. In this case, the transducer does not sweep across the entire width of the tray at once, but instead stops at each area of interest and just scans that area. Depending upon the size of the interest areas and the blank spaces (non-interest areas) between them in the tray, it could be more efficient for throughput to scan the tray within a single sweep, or to scan each part individually. The critical aspect of the decision is related to how fast the scanner mechanism can ramp up to full speed.

Both conventional and advanced production scanning use a transducer of a given ultrasonic frequency, with parameters such as the gate (vertical extent of the sample from which echoes are used for imaging), gain and other parameters fixed. The overall purpose

is simply to identify those parts that have internal structural defects, and to identify the x-y location of the defect.

In actual practice, the discovery of defects during production scanning often leads to a request for an analytical look at the same parts, preferably without a long wait. The new system therefore includes the full analytical tool set of C-SAM® systems, and is the first production system to have analytical capabilities. These tools include (among others) nondestructive acoustic cross-sectioning of the part, transmission (rather than reflection) mode imaging, measurement and mapping of the thickness of an individual layer within the part, frequency domain imaging, and multiple (poly) gate imaging.

To give one example, here is what can be done with the multiple-gate imaging tool. Ordinary imaging uses a single gate (defined depth) from which echoes are received. If the die face is the depth of interest, the gate will be fairly narrow and will include the die face, but not interfaces above or below this gate.

Multi-gate imaging lets the operator set as many as 200 individual gates. They may be as thin as the material will permit. They are usually adjacent, but they may be made overlapping or separated. All the imaging is performed during one transducer scan, and each gate produces its own acoustic image.

The isolated void mentioned earlier is an example of a situation where this tool might be useful. The production image of the tray will only show that this part has a void at a given x-y location, but does not tell the precise depth of the void. It might be truly isolated and harmless, or it might be among wires. Setting 20 gates would result in 20 images; in one of the images, the void will appear in sharp focus. Its z-location above or below the bond wires can easily be estimated, and it can be clearly identified as harmless or risky.

#### Die Stack Inspection

The acoustic inspection of stacked die to find internal defects is chiefly a concern during development and prototyping, where the goal is to select materials and processes that will make

internal defects very unlikely. By far the most frequent acoustically imaged defects in stacked die are delaminations between the die.

Developed during a multi-year collaboration with the Technical University of Dresden, a new simulation software tool makes the acoustic imaging of stacked die (the test stacks consisted of 8 die) more straightforward and faster. An acoustic microscope

operator without the simulation software faces the almost unsurmountable problem that there are too many echoes to deal with. In reflection-mode acoustic imaging, the scanning transducer sends a pulse of ultrasound into the die stack. It is partly reflected by bonded interfaces, of which there are many. An echo reflected upwards encounters bonded interfaces, and is partly reflected downwards. When you

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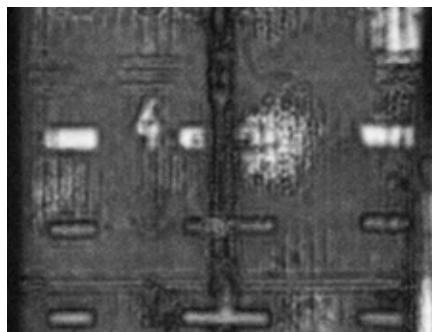
have 8 die in a stack, the number of echoes of varying amplitude reaching the transducer quickly becomes very large. Trying to sort out the echoes to find internal defects becomes extremely time-consuming.

The engineer charged with finding defects in a die stack uses the simulation software before attempting to image the physical die stack. With the simulation software, he/she can create a virtual model of the physical die stack, specifying the thicknesses of the die and of die attach layers, and the physical characteristics (acoustic velocity, density) of each material.

The engineer will also place a virtual defect at the top of each die. The virtual defects will reflect ultrasound with the same very high amplitude as real defects. The engineer now images the top of virtual die #4 (for example) to see the defect that was placed there. When the defect is found, small adjustments to the imaging parameters can be made to optimize virtual imaging for die #4.

When the engineer has done the same for all of the die, he/she uses the imaging parameters derived from the simulation to image the physical die. The echoes can then be gated on, or very near to, each physical material interface, even if no defect is present. The imaging parameters will probably be tweaked based on the results with the physical sample. The engineer may then export the upgraded parameters to the simulation for further refinement before returning to the physical die stack, where the acoustic images can be obtained at the precise depths required to inspect for internal defects.

**Figure 2** shows the results from using this method on a test stack of 8 die. An identifying number has been etched into each die, along with adjacent bars. Both the number and the bars are voids. The parameters established by using the virtual die stack were used to image this physical die stack. The brightness of the number and associated bars indicate that the echoes showing die #4 have been correctly identified. The numbers and bars of adjacent die are faintly visible here, but each die can now be imaged correctly with its own parameters.



**Figure 2:** Stacked-die simulation software lets an engineer use known parameters to create a virtual die stack and perform initial acoustic imaging. Transferring the imaging parameters between the virtual die stack and the physical die stack makes possible accurate imaging – here, die #4 in an 8-die stack.

### Wafer Inspection

The preferred point at which to inspect wafer level packages, MEMS devices, and other devices made by bonding wafers, is at the wafer level. Inspection at this stage lets the manufacturer remove devices that do not meet acceptance standards immediately after dicing, and before further expense is incurred in the processing of worthless devices.

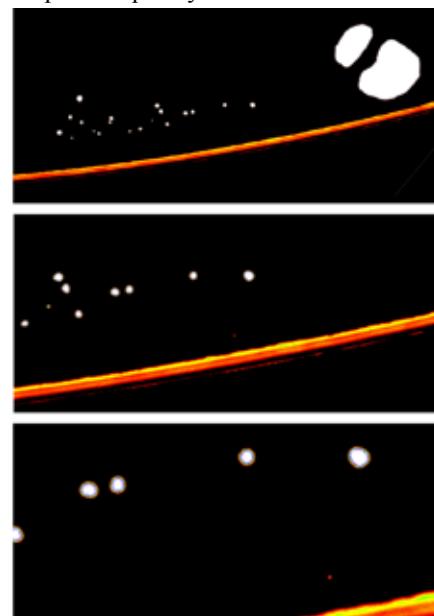
To make wafer inspection more accurate (via higher resolution, **Figure 3**) and faster, an automated, high-throughput wafer inspection system has been developed. It handles, inspects and analyzes 300mm wafers, but can also handle 200mm wafers. The system can be configured with two loadports or SMIFs to increase throughput, and two stages and two transducers, so that two wafers can be inspected simultaneously. Shrinking die sizes and shrinking feature sizes mean that very tiny defects can be fatal. The system images voids <5 microns in diameter, as well as delaminations as thin as 200Å.

High lateral transducer speed (>1m/s) improves the throughput rate, as does the sequencing of tasks (aligning, placing, removing, and drying of wafers) for the robotic arm. A specialized water-jet transducer permits non-immersion scanning to prevent water ingress between the wafer pair. After a wafer has been scanned, the acoustic data is overlaid onto the wafer map for automated identification of rejected devices, which are removed after dicing of the wafer.

### Molded Underfill Flip-Chips (MUFs)

Historically, flip-chips have been imaged acoustically after capillary process underfilling and before overmolding. The ultrasonic transducer scanned the back side of the silicon – meaning that only the acoustically very transparent silicon lies between the transducer and the underfill and solder bumps. Most of the significant structural defects, chiefly underfill voids and bump cracks, occur between the die and the substrate. Because of silicon's transparency, the depth of interest could occasionally, in some very thin packages without overmolding, be imaged using the very high ultrasonic frequencies of 300MHz and 400MHz.

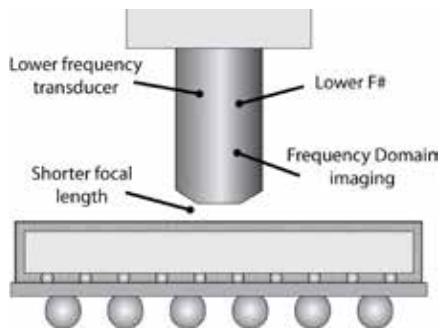
Simultaneous underfilling and overmolding means that the transducer now scans the cured underfill above the die. This adds one material interface – overmold to silicon – to the target, but more importantly, adds a material that tends to absorb ultrasound. The mold compound typically absorbs enough ultrasound to make it necessary to use a lower frequency transducer to penetrate to the depth of interest. Lower frequency means lower resolution. In some flip-chip packages, the mold compound is relatively benign and the loss of resolution minor. In many packages, the drop in frequency and loss of resolution



**Figure 3:** High resolution makes it possible to identify even defects <5µm in size, and to remove components having these defects.

is more significant, although inspection can still be performed. A few mold compounds have been encountered that are so lossy that meaningful inspection is all but impossible.

In most molded underfill samples, imaging is performed by using a transducer of somewhat lower frequency, and the images obtained are suitable for finding defects. In some samples, imaging can be improved by using a transducer that has been customized in order to maximize its performance for a particular geometry and mold compound type. **Figure 4** shows the key techniques for achieving best results:



**Figure 4:** Four considerations that can improve the imaging of molded underfill flip-chips.

**One can use a lower frequency transducer.** The frequencies typically used on bare flip chips, 230 MHz and above, won't penetrate the MUF. The operator might use a frequency such as 50 or 100MHz to determine whether they will penetrate. Very low frequencies such as 20MHz may penetrate through the MUF, but may not be able to resolve the bump bonds.

**One can select a transducer having a lower F#.** The F# is determined by the transducer's piezoelectric element diameter (D) and the focal length (FL). A lower F# means that the ultrasonic beam can be more finely focused, therefore providing better resolution.

**One can use a transducer having a shorter focal length (FL).** A pulse launched from the transducer first needs to pass through the water couplant, which absorbs ultrasound. A shorter FL means that the water path will be shorter, and thus less attenuating. The FL must, however, be long enough to reach the depth of interest.

#### Switch from time domain imaging

**(the usual reflection-mode method) to frequency domain imaging (FDI).** FDI takes advantage of the fact that any given transducer emits ultrasound along a range of frequencies on both sides of its nominal frequency. A 100MHz transducer might emit frequencies from 70MHz to 120MHz. FDI imaging produces an acoustic image for each frequency that returns enough echo signals. Twenty or more images from a single FDI scan is

not uncommon. What matters is that an interface reacts to different frequencies differently, and a feature that is faint at one frequency may be sharp and clear at another frequency.

#### Biography

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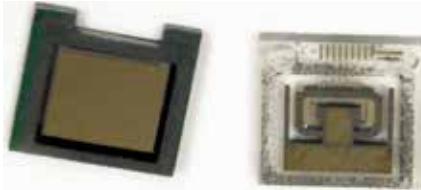

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# Chip Scale MEMS Vacuum Packaging

By Douglas Sparks [[Hanking Electronics Ltd.](#)]; and Jay Mitchell, Sangwoo Lee [[ePack Inc.](#)]

**T**hanks to new consumer applications, billions of MEMS (microelectromechanical system) devices are being fabricated each year. A large percentage of these such as gyroscopes, pressure sensors, bolometers and voltage controlled oscillators, require vacuum packaging. Vacuum packaging reduces damping in resonators, acts as a reference vacuum in pressure sensors, reduces absorption in infrared devices, and in general, reduces hysteresis and often improves sensitivity and resolution.

Vacuum packages have transitioned from discrete metal and ceramic packages to chip-scale devices. A variety of methods have been used to improve vacuum packaging at both the discrete and wafer level. Getters have been employed to lower the cavity pressure from the Torr range into the mTorr range. Integrating a thin-film getter [1-3] into a chip-scale package can greatly reduce the complexity of low pressure (<10mTorr) MEMS vacuum packaging. A capping wafer, generally either silicon or glass, is patterned and etched to form both a cavity that will enclose the active micromachine and often open up access to the electrical bond pads. Next, the getter and the sealing material are deposited in the cap wafer. The sealing material may be made up of a reflowed glass layer, gold or solder. The getter film is generally comprised of a reactive thin-film transition metal, which in some cases does not require activation [1, 2]. Since thin-film deposition techniques are employed in a cleanroom environment, the getter is virtually particle free compared to conventional NEG's formed using powder metallurgy. Adding the thin-film getter does not impact the chip size. **Figure 1** is a close-up of the chips and shows that the



**Figure 1:** Thin film getters patterned on the cap (left) and device surfaces (right).

patterned thin-film getter can be placed on the top cap (left) or active device side (right).

Thin-film getter technology has been applied to chip-scale vacuum packaging of commercially available gyroscopes, accelerometers, pressure sensors, optical devices, infrared sensors, and microfluidic density and chemical concentration meters [4], Pirani gauges [5], biological cell and particle detection [6], micromachined Coriolis mass flow sensors [7], drug infusion systems [8], and RF MEMS resonators [9]. **Table 1** summarizes the cavity pressures obtained with and without getters for a variety of sensors and microstructures.

Packaging Technology	Seal Temperature (°C)	Without Getter	With Getters
TO Can Weld	25	30-50mTorr	NA
Ceramic Solder	250-330	2-4Torr	10mTorr
CSP Anodic Bond	375-500	2-400Torr	1mTorr
CSP Reflow Glass	400-450	1-2Torr	0.8-2mTorr
CSP Metal Eutectic	250-430	1-2Torr	2.5 mTorr
CSP CVD Seal	400	7.5 mTorr	NA

**Table 1:** MEMS vacuum packaging methods without and with getters [1, 2, 5, 7, 12, 17].

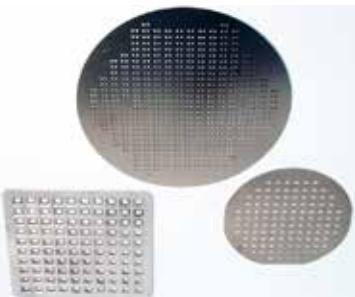
Deposited getter technology offers the flexibility to customize the getter layers used and the thickness employed, which is of great advantage in changing the getter for different MEMS encapsulation processes. The deposition of getters is not limited to MEMS chips. Both MEMS die and conventional metal and ceramic vacuum packages can incorporate a patterned getter on either the lid or other surfaces on the device wafer. Thin-film getters on wafers can be patterned with traditional photo-etch

processes, lift-off resist and shadow masks. Metal photolithography gives the advantage of being able to make small feature sizes, but is limited in the depth of cavity in which the film can be patterned. Shadow masking can be used to place the getter in deep cavities but has coarse line width control. It also provides the best getter surface for improved gas absorption because no chemical processing has been used to pattern the metal layer. **Figure 2** shows an example of shadow masks that have been used with both wafers and metal lids employed with soldered ceramic and welded metal packaging.

These reactive metal getters will not trap noble gases like helium, neon, argon or krypton. These noble gases are used in semiconductor processing for sputtering, reactive ion etching, as carrier gases in CVD, and for backside wafer cooling. It is possible for noble gases to be implanted in the surface of a wafer during plasma etching and sputter back etching, where they can outgas over time.

What are the long-term reliability issues associated with vacuum packaged MEMS devices? Poorly sealed wafers due to particle related voids or misprocessing of reflowed glass or solder can lead to air leaking into the microcavity. Long-term reliability testing is key, prior to product launch, of any new technology to avoid field failures. Several authors have noted MEMS hermeticity problems associated with chip-scale helium and/or hydrogen in vacuum-packaged MEMS.

Kim, et al. [10], found that helium and hydrogen could permeate CVD oxide sealed MEMS resonators at elevated temperatures resulting in a



**Figure 2:** Shadow masks used to pattern thin film getters.

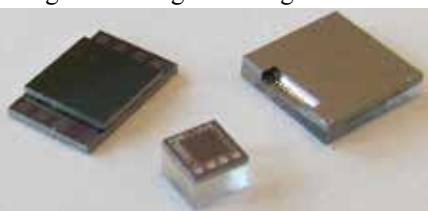
degradation of a device's Q. Hydrogen or helium gas at an ambient temperature of 400°C can reversibly increase cavity pressure. A helium ambient at 170°C could also depress the resonator Q as could a long 100°C bake in air because of the 5ppm helium present in the atmosphere. The gradual cavity pressure increase was not observed after air storage for 3000 hours at room temperature. By sealing the CVD oxide plugs with an aluminum capping layer, the researchers found that they could prevent hydrogen permeation into the CVD sealed microcavities at elevated temperatures.

For wafer-to-wafer vacuum sealing, no change in cavity pressures has been observed after four years at room temperature in air for eutectic sealed Pirani gauges that incorporated thin film getters to lower pressures [11]. Reflowed glass-sealed resonators that also used thin-film getters in the wafer bonding process showed no change in cavity pressure (below 1mTorr) and Q for over 5 years at 95°C in air [11,12]. These studies relied on time and temperature in air to check for leaks and accelerate air or atmospheric helium or neon leakage into the microcavities.

Gas concentration and pressure can also be used to accelerate gas leakage, which is the essence of the helium bomb test MIL-STD 883E required for so many years in electronic package testing [13]. Resonator Q values have been observed to decrease in the presence of pressurized helium at low temperature in sealed microstructures [12]. The reversible effects were seen with MEMS resonators employing wafer-level reflowed glass and/or direct silicon-bonded sealing interfaces. These

effects were seen between 23°C and 100°C after and during helium exposure at relatively low pressures of 140 to 380KPa. Resonator Q changes were not observed for hydrogen, argon, nitrogen, methane, carbon dioxide and air [12,14].

To look at helium-related hermeticity in more detail, several chip-scale vacuum packaged (CSP) devices were tested at room temperature with pressurized helium that was also at room temperature. **Figure 3** shows the Pirani gauge, resonator and absolute pressure sensor chips tested. The commercially available microfluidic resonator chip [15] uses a resonating silicon tube that is vacuum sealed using reflowed glass along with a thin-



**Figure 3:** Chip scale packages that have shown helium permeation in this study.

film getter. Three different pressure sensors were also tested in this study; a Freescale manifold absolute pressure sensor, that is made using two silicon wafers bonded with reflowed glass [16], a Delphi manifold absolute pressure sensor that forms its vacuum reference using silicon to glass anodic bonding [17], and finally, a Delphi differential silicon-on-glass pressure sensor.

The resonator Q value was found to decrease from continued helium exposure at 380KPa at room temperature, as shown in **Figure 4**. This Q change corresponds to a pressure increase from 1mTorr to over 100Torr after just 48 hours of helium exposure. This resonator employed a thin film getter to obtain such low initial cavity pressures (1mTorr) and had silicon cap wall thicknesses of 150 to 200μm.

Both Freescale monolithic absolute pressure sensors and Delphi Wheatstone bridge absolute pressure sensors showed a gradual linear change in the zero pressure offset during helium exposure.

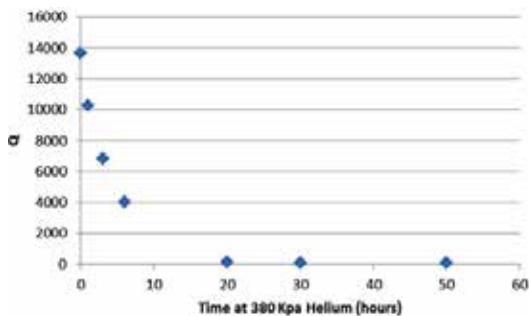
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**Figure 4:** The decrease in resonator Q with time from room temperature helium exposure at 380KPa.

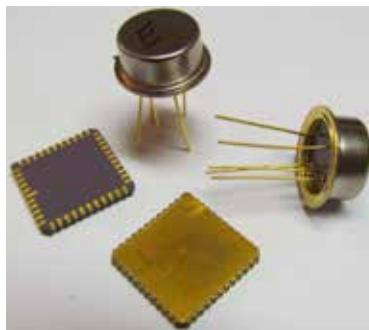
This denotes an increase in the cavity pressure of the vacuum reference, which causes deflection of the piezoresistors in the bridge. Absolute pressure sensors stored in air at the same pressure showed no change in the zero pressure offset. These single-crystal silicon diaphragms had thicknesses of 12 to 20 $\mu\text{m}$ . Differential Delphi pressure sensors showed no change caused by helium exposure. The anodically bonded Delphi absolute pressure sensor is of most interest since there is no sealing material, only the relatively wide glass-silicon anodically bonded interface.

To examine other means of packaging MEMS sensors, Pirani gauges [8] packaged with three different methods, CSP, welded metal TO lids, and ceramic packages with soldered lids, shown in **Figure 5**, were pressurized at 690KPa (100psi) for 400 hours. This helium exposure caused the average cavity pressure of the silicon chip-scale packaged Pirani gauges to increase by 1.471Torr, while the ceramic and metal packages exhibited no significant change in thermal impedance and therefore, internal pressure.

**Table 2** summarizes the different wafer- and package-level vacuum sealing materials examined to date, as well as the bonding methods and results with regard to helium permeation. All

chip-scale vacuum packaging methods eventually had a helium ingress problem, while the two discrete packaging methods using ceramic and metal packages did not. Even wafer-level bonding methods with no sealing material, direct fusion bond and anodic bonding, were not hermetic in the presence of pressurized helium at room temperature. Silicon is the common material (12 $\mu\text{m}$  to 500 $\mu\text{m}$  thick) for the parts showing helium permeation.

While hermeticity problems due to particle-related defects and voids can lead to random leaks, this would not be an expected cause in four different wafer fabs with all four wafer-level bonding methods. The permeation of helium has also been observed with three different MEMS devices: resonators, absolute pressure sensors, and Pirani gauges. Prior work with the same resonating



**Figure 5:** Discrete vacuum packages used for MEMS devices.

devices found no change in Q after long-term pressurization in hydrogen, nitrogen and argon at room temperature [12], as well as methane and carbon dioxide [14].

The comparison between resonators immersed in both hydrogen and helium is the best evidence that a gas leak is not the cause for the Q changing results.

Effusion is the molecular process by which a gas moves through a porous wall or through a narrow channel such as a crack or leaky seam. Thomas Graham noted that the effusion rate of gases is inversely proportional to the square root of the densities or molar masses of gases. Graham's law of effusion explains why a narrow channel or relatively tight seal may be leak proof to air, with a molar mass of about 29g/mole, and yet fail to hold lighter gases like hydrogen, with a molar mass of 2g/mole, or helium, with a molar mass of 4g/mole. The observation that hydrogen did not leak into the vacuum cavity through a wafer-level glass reflow and fusion bond, while helium does [12], suggests that effusion of a gas through a sealing gap is not the cause of CSP helium permeation.

Based on the results of this study it is not currently recommended to use vacuum-sealed MEMS devices such as absolute pressure sensors in helium or a helium gas mixture. Other devices like wafer-level packaged infrared chemical sensors may develop errors associated with helium absorption peaks if operated in this type of medium. Neither passive nor electrically-activated getters can be used to absorb noble gases like helium.

## Summary

Further work is needed to determine if chip-scale MEMS packaging can be developed that does not have a helium permeability problem. As Kim, et al., showed [10], vacuum-sealed MEMS devices can have problems even with the 5ppm helium present in the atmosphere at the high end of the device operating temperature, which can range from 85 to 150°C for automotive, industrial and aerospace devices. While metal and ceramic packages can be used to solve this problem, a reliable chip-scaled part would save size and weight. ☺

## Biography

Douglas Sparks received his PhD from Purdue U. and is EVP of Hanking Electronics; email sparksdr@hanking.com

Jay Mitchell received his PhD from the U. of Michigan and is President of ePack Inc.

**Table 2:** Helium permeation for different vacuum packaging materials and sealing methods.

Sangwoo Lee received his PhD from Seoul National U. and is CTO at ePack Inc.

## References

1. B. Lee, S. Sook, K. Chun, "A Study of Wafer-Level Vacuum Packaging for MEMS Devices," *J. Micromech.& Microengr.*, 13 pp. 663-669, 2003.
2. D. Sparks, S. Massoud-Ansari, N. Najafi, "Chip-Level Vacuum Packaging of Micromachines Using NanoGetters," *IEEE Trans. Adv. Packaging*, Vol. 26, No. 3, pp. 277-282, 2003.
3. M. Moraja, M. Amiotti, "Getters Films at Wafer-Level for Wafer-to-Wafer Bonded MEMS," *Design, Test, Integration and Packaging of MEMS/MOEMS 2003*, IEEE, pp. 346-349, May 5-7, 2003.
4. D. Sparks, R. Smith, J. Patel, N. Najafi, "A MEMS-Based Low Pressure, Light Gas Density and Binary Concentration Sensor," *Sensors & Actuators A*, 171, pp. 159-162, 2011.
5. J. Mitchell, G. Lahiji, K. Najafi, "Long-Term Reliability, Burn-in and Analysis of Outgassing in Au-Si Eutectic Wafer-Level Vacuum Packages," *Solid-State Sensor, Actuator and Microsystem Workshop*, Hilton Head Island, SC, Jun 4-8, pp. 376-379, 2006.
6. T. Burg, M. Godin, S. Knudsen, W. Shen, G. Carlson, J. Foster, K. Babcock, S. Manalis, "Weighing of Biomolecules, Single Cells and Single Nanoparticles in Fluid," *Nature*, Vol. 446, pp. 1066-1069, 2007.
7. R. Smith, D. Sparks, D. Riley, N. Najafi, "A MEMS-Based Coriolis Mass Flow Sensor for Industrial Applications," *IEEE Trans. Indust. Elect.*, Vol. 56, No.4, pp. 1066-1071, April 2009.
8. D. Sparks, A. Chimbayo, J. Cripe, R. Smith, N. Najafi, "Preventing Medication Infusion Errors and Venous Air Embolisms Using a Micromachined Specific Gravity Sensor," *Drug Delivery Technology*, Vol. 4, No.4, pp. 82-86, May 2004.
9. B. Wissman, "Silicon and WLP Enables Commercial-Grade MEMS Resonators," *Solid-State Technology*, Vol. 50, pp. 59-64, June 2007.
10. B. Kim, R. Candler, R. Melamud, M. Hopcraft, S. Yoneoka, H. Lee, et al., "Hermeticity and Diffusion Investigation in Polysilicon Film Encapsulation for MEMS," *J. Appl. Phys.* 105, 013514, 2009.
11. D. Sparks, S. Massoud-Ansari, N. Najafi, "Long-Term Evaluation of Hermetically Glass Frit Sealed Silicon to Pyrex Wafers with Feedthroughs," *J. Micromech. & Microengr.*, 15, pp. 1560-1564, 2005.
12. D. Sparks, "The Hermeticity of Sealed Microstructures Under Low Temperature Helium and Hydrogen Exposure," *J. Micromech. Microeng.*, 23, 015016, 2013.
13. Y. Tao, A. Malsha, "Theoretical Investigation on Hermeticity Testing of MEMS Packages Based on MIL-STD-883E," *Microelectronics and Reliability*, 45 pp. 559-566, 2005.
14. D. Sparks, R. Smith, J. Patel, N. Najafi, "A MEMS-Based Low Pressure, Light Gas Density and Binary Concentration Sensor," *Sensors & Actuators A*, 171, pp. 159-162, 2011.
15. D. Sparks, K. Kawaguchi, M. Yasuda, D. Riley, V. Cruz, N. Tran, et al., "Embedded MEMS-Based Concentration Sensor for Fuel Cell and Biofuel Applications," *Sensors and Actuators A*, 145-146, pp. 9-13, 2008.
16. J. Gragg, "Silicon Pressure Sensor," US Patent 4,317,126, 1982.
17. W. Baney, D. Chilcott, X. Huang, S. Long, J. Siekkinen, D. Sparks, S. Staller, "A Comparison Between Micromachined Piezoresistive and Capacitive Pressure Sensors," *Proc. of the Fall SAE Conf.*, No.973241, pp. 61-66, 1997.



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# Product News

## Mobility Drives Electronics: Multitest's Solutions for Efficient Test

Recently demonstrated during an open house from July 9-11 at their facility in Santa Clara, CA, Multitest reports that its new MT2168 pick-and-place handler is the best solution for the challenges of building small, yet highly integrated, packages for mobile devices.

According to the company, the MT2168 pick-and-place handler offers a variety of smart features that meet special IC requirements for mobile devices. For one, the MT2168 fully supports advanced packaging. To comply with the requirements for functionality and performance, the highly integrated packages used in mobile technology contain heterogeneous stacks. The soft material handling with smooth and shock-proven movements of the MT2168 combined with its controlled plunge avoids damage to such fragile stacked devices.

Additionally, MT2168 can be configured with active thermal control (ATC) to manage power dissipation, which is often an issue with highly integrated ICs. The high plunger force of up to 5,000 N reportedly ensures best contacting performance even for high pin count packages.



Added to the challenge of building the devices, the demand for smartphones, tablets, and ultrabooks requires high volumes of semiconductors and sensors. But, in a fast-changing consumer market ASPs, and therefore the production costs, are critical. Unfortunately, ICs and sensors for mobile applications have special test requirements and test handling needs to ensure high throughput and high yields to achieve best cost of test, and that's where Multitest believes their new MT2168 contains another solution.

According to Multitest, the unique material flow and the capability of the handler to test up to 32 packages in parallel ensure low jam rates and the highest throughput even for the smallest packages. As a result, the MT2168 is a cost-efficient handling solution for high-volume production.

## Nordson ASYMTEK Introduces Batch Fluid Dispensing System for Cleanroom Applications

Nordson ASYMTEK, a supplier of dispensing and jetting technologies, released its Spectrum™ S-820-C stainless steel dispensing system. The system, third party certified for Class 100 cleanroom use, can be used

in applications extremely sensitive to contamination by sub micron-sized particles, such as wafer-level packaging (WLP). It can also be utilized for dispensing a controlled amount of adhesive in precision cleanroom manufacturing operations. The system reportedly provides advanced dispensing process capability and is ideal for use in labs, new product development, and batch production.

According to ASYMTEK, processes developed on the S-820-C can be



transferred to a conveyorized Nordson ASYMTEK fluid dispenser when operations require more than batch capacities. It also claims production can be expanded with minimal configuration downtime in the transition from engineering development to inline manufacturing.

Even the stainless steel enclosure, enclosed keyboard, and special cable design reportedly reduce particle generation. An optional HEPA filter can be added for downward airflow to further minimize particle generation during processing. Other options include a laser height sensor, which helps maintain consistent dispensing height, and a dual-action dispensing head, which can be used to increase UPH.

Additionally, the S-820-C performs with a wide range of fluids, processes and substrates used in electronics packaging and assembly. It is said to integrate easily with most Nordson ASYMTEK jets, pumps, and valves, including the NexJet® NJ-7.

Nordson ASYMTEK's advanced process control capabilities have been incorporated into the S-820-C platform, bringing premium features to this batch system.



10th Annual

# International Wafer-Level Packaging Conference & Exhibition

November 5-7, 2013

DoubleTree Hotel, San Jose, CA

Tutorials: November 5

IWLPC Conference: November 6-7

IWLPC Exhibit: November 6-7

## IWLPC EVENT SCHEDULE

- Nov. 5 Professional Tutorials  
Nov. 6 Keynote Breakfast  
Nov. 6-7 Exhibition, Panel Discussion and Technical Presentations on 3D, WLP and MEMS.

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Paul Wesling, a CPMT Society Distinguished Lecturer

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### Metal Based MEMS Offer New Growth Opportunities

William G. Hawkins, General Electric Global Research Center

### A Consumer Driven Market — This Changes Everything

Simon McElrea, Invensas Corporation

## PANEL DISCUSSION

### 3D High Volume Manufacturing — Are We There Yet?

Hosted by **invensas**

"We have participated in the IWLPC for the last two years and have found that the technical presentations have been very enlightening. IMT, being a MEMS foundry, utilizes wafer level packaging in over 70% of the products that we produce and would not miss this important conference. We also found the exhibit hall experience very valuable."

— Michael Shillinger, Founder, Innovative Micro Technology (IMT), IWLPC Best of Conference 2012

For more information on the conference, or exhibit and sponsorship opportunities please contact Patti Hvidhyld at 952-920-7682 or [patti@smta.org](mailto:patti@smta.org)

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## **Ironwood Electronics Stamped Spring Pin Socket for LGA110**

The LGA110 socket from Ironwood



Electronics was introduced to address high-performance requirements for 0.5mm pitch devices - CBT-LGA-5000. The contactor is a stamped spring pin with 31-gram actuation force per pin and a 500,000 insertion cycle life. The self inductance of the contactor is 0.88 nH, insertion loss of < 1 dB at 15.7 GHz and capacitance 0.097 pF. The current capacity of each contactor is 4 amps. Socket temperature range is -55°C to +180°C. The socket also features an IC guide for precise land grid array (LGA) edge alignment. The specific configuration of the LGA package to be tested in the CBT-LGA-5000 is 25x21mm body size and 0.5mm pitch. This socket can be used for hand test and quick turn custom burn-in applications with the most stringent requirements.

The CBT-LGA-5000 socket features

a unique contact design with outside spring and flat stamped plungers that provide a robust solution for burn-in & test applications including excellent electrical signal integrity to meet the requirements of today's demanding analog, digital, RF, Bluetooth and telecom applications. The socket is mounted using supplied hardware on the target PCB with no soldering, and uses smallest footprint in the industry. The smallest footprint allows inductors, resistors and decoupling capacitors to be placed very close to the device for impedance tuning. The clamshell socket lid incorporates a quick installation method using latch so that IC's can be changed out quickly. These socket product lines have been designed to the JEDEC standard MO-220 and are available for all standard configurations. Custom designs are also available.

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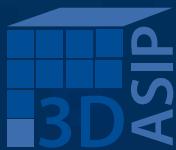
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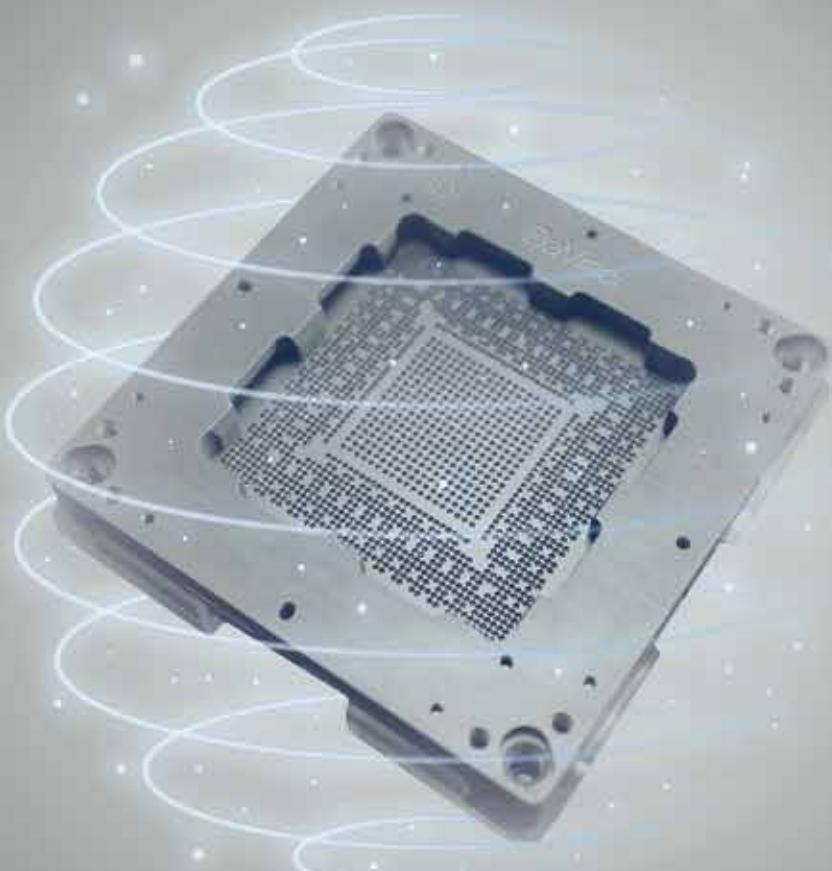
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