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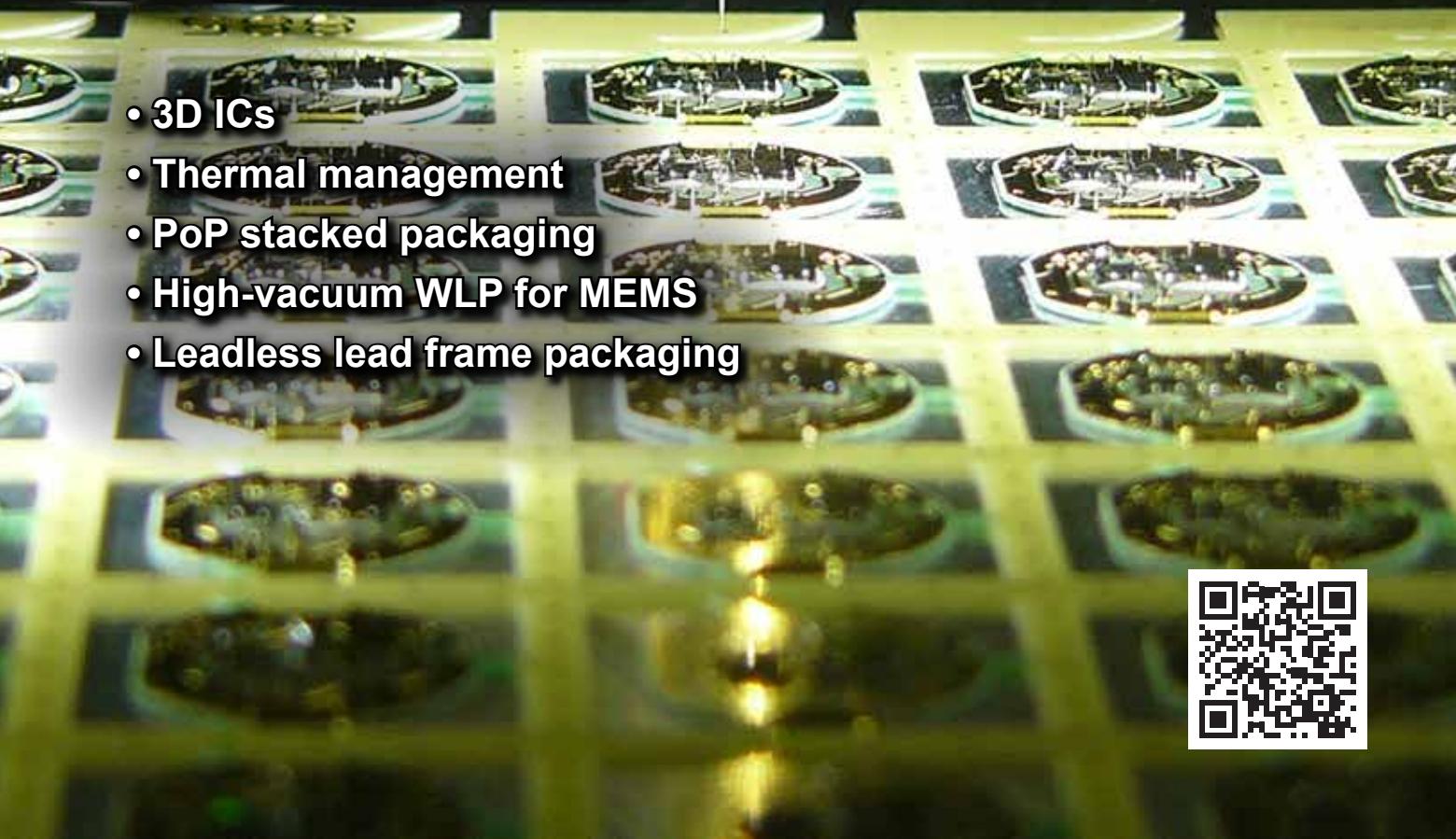
*The Future of Semiconductor Packaging*

Volume 18, Number 6

November • December 2014

## Automation for bond testing of MEMS

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  - Thermal management
  - PoP stacked packaging
  - High-vacuum WLP for MEMS
  - Leadless lead frame packaging
- 





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The photo shows MEMS devices undergoing an automated non-destructive wire pull test on a Nordson Dage bond tester. The addition of high-resolution camera systems has enabled the development of high-performance automated bond test systems. Automation gives significant improvements in repeatability and precision and limits the influence and variation caused by the operator. Camera-assist automation capability is vital in many bond test applications including wafer-level bond and die shear, copper pillar/flip-chip micro bumps, ultra-fine pitch interconnect, wire pull and shear/pull of hybrid devices.

Photo courtesy of Nordson Dage

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REVIEW

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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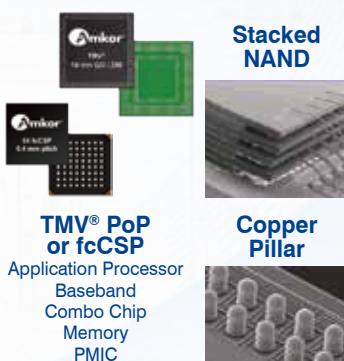
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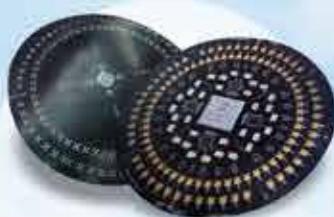
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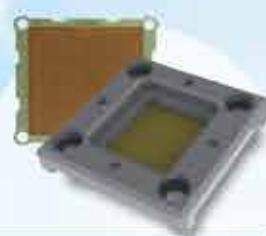
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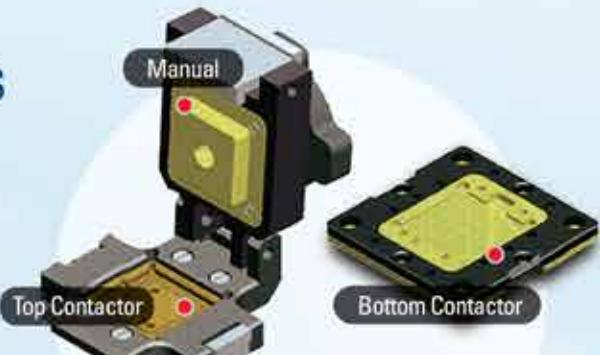
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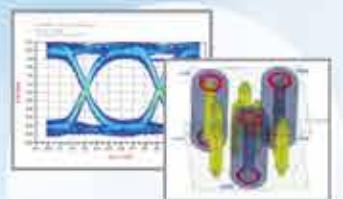
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## FROM THE PUBLISHER

This last issue in 2014 includes insight into the latest work from two leading R&D institutes: CEA-Leti gives readers a perspective on its 3D technology platform, and Fraunhofer discusses its 3D heterogeneous integration strategy. We also bring the year to a close by featuring perspectives on a number of industry events dedicated to the ongoing innovation of the semiconductor packaging industry: SEMICON Europa, IMAPS, and IW LPC.

Looking ahead to the many industry events planned for 2015, the new year will kick off with a spotlight again on world famous Grenoble, France, where the SEMI European office proudly presents its third European 3D TSV Summit (Jan 19-21). Later in the year, SEMI's new flagship event in Milan will be focusing on MEMS at the European MEMS Summit complete with conference, exhibition, and networking opportunities (Sept 17-18).

*Chip Scale Review* offers a physical and virtual platform for the many papers presented at the conferences throughout the year. Increase your company visibility and get your article placed in one of the 6 planned issues in 2015. (Contact the editor for specifics at [editor@chipscalereview.com](mailto:editor@chipscalereview.com)). As we bring this year to a close, many decision makers are planning, forecasting and projecting for the year ahead.

We look forward to hearing from you.

**Kim Newman**  
 Publisher

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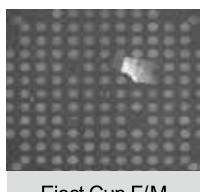
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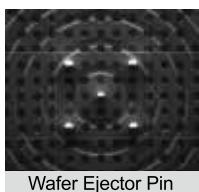
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# 3D MARKET UPDATE



## Moving 3D ICs into HVM: narrowing the gap

By E. Jan Vardaman [[TechSearch International, Inc.](#)]

The wait for the introduction of 3D ICs with through-silicon vias (TSVs) has been a long one, but the time has finally arrived for a number of applications. Backside vias in MEMS, power amplifier devices, and image sensors have been in production for many years. Sony even introduced a via last process where its CMOS image sensor and logic devices provided dramatic improvement in a camera selected for smartphones and tablets. The wait for other applications has not been a patient one. Many companies in the industry have invested time and money into working on equipment, materials, and assembly operations to meet the need for a technology that each year shifts out into the future for high-volume manufacturing. Has the time finally arrived for the introduction of the technology? The answer is “yes.” By moving into production with stacked memory modules, announcements from Micron, SK Hynix, and Samsung have become more than words on cute PowerPoint slides, as engineering samples from some of these memory makers are now in the hands of companies that will be moving into production with real volumes in 2015 (**Figure 1**). It has not been an easy path. Micron first talked about its Osmium process in 2002. Few companies have the patience to wait over a dozen years for technology commercialization. Micron’s process is a special architecture where the logic layer is designed separately with memory layers stacked and connected with TSVs.

Micron, SK Hynix, and Samsung use a bond/debond process for the wafer thinning process that works, but could still use improvements. The first applications will be in network systems products and high-performance graphics solutions, followed by servers. Tezzaron’s new architecture memory solution that uses a permanent bond process has been in production for several years for special high-performance applications.

### Drivers for 3D ICs with TSVs

Bandwidth demands and device latency issues, coupled with power management, delivery and distribution needs, have created drivers for a new integrated circuit (IC) architecture solution. Many semiconductor industry activities point to the adoption of 3D ICs with TSV technology as a possible solution. With the cost of lithography outstripping the budgets of even the most financially fit semiconductor companies, 3D ICs with TSVs offer an option that is under consideration by many companies.

### Gaps

What about other products such as memory and logic, or logic on logic stacks with TSVs? There are gaps in the technology, infrastructure, and logistics that are holding this back. What are these gaps and how can they be solved? Several technical challenges and infrastructure issues such as business logistics are delaying the full commercialization of TSV technology for 3D ICs. Major issues include: 1) EDA tool availability including the ability to use thermally-aware tools and the ability to communicate between tools to design

new architectures; 2) Manufacturing yield in key process steps such as debonding during wafer thinning; 3) Assembly of 3D ICs; 4) Thermal dissipation (especially when logic is in the stack) and cooling methods; 5) Test methodology; 6) Infrastructure-related issues, including logistic supply chain handoff and risk assumption; 7) Reliability assurances; and 8) Cost compared to alternatives.

Any one of these issues has the potential to limit a full 3D IC implementation, and these challenges are driving many companies to seek alternative packaging and assembly solutions until they can be solved.

### Too many choices?

A designer is confronted with many options when selecting the IC design and optimal packaging solution. The use of pathfinding tools will enable better choices when faced with a myriad of options including the use of true 3D ICs, or a silicon interposer solution (or potentially laminate or glass).

A new option is the approach presented by Intel for its foundry customers where a silicon bridge in the substrate allows communication between chips. Or,

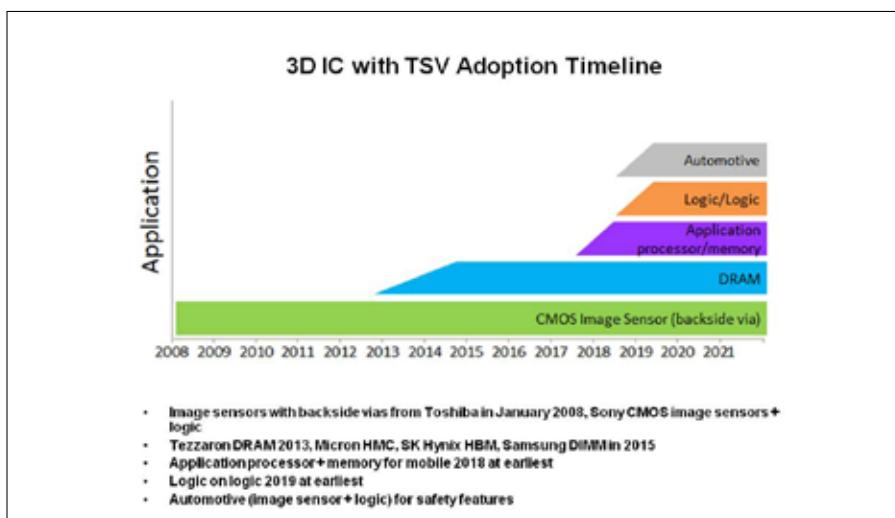


Figure 1: 3D IC with TSV adoption timeline. SOURCE: TechSearch International, Inc.



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maybe some other form of stacking should be considered. Options include package-on-package (PoP) with a flip-chip die or an embedded die in the bottom package substrate, or a fan-out wafer-level package solution (FOWLP). The memory stacked in the top package can be fully tested and standard footprints enable one memory supplier's package to be swapped out for another's package. Decoupling the memory from the logic gives the end user more supply chain options than a 3D IC logic and memory solution where the devices are designed to function with each other.

Multi-chip modules without TSVs in the substrate are also in production and include system-in-package (SiP) solutions. Face-to-face (F2F) stacking technology is another alternative to 3D IC integration.

## Electronic design automation (EDA) tools

One of the major challenges is for developers to be able to design and model the full package and die at the same time. This would include having the ability to model electrical, mechanical, and thermal requirements. Most tools have been focused on 2.5D applications. Companies in the memory market have their own internal 3D IC design capability. One area of critical importance is low-power design, still in its infancy. Currently EDA and other companies are working on developing true 3D IC tools but they are not ready yet for release.

With a true 3D IC with TSVs, design tools will enable the full design, but need to include a thermally-aware component, especially where memory and logic are stacked. Why? Because memory is specified to operate properly at specified temperatures, it will not function properly if it is on top of a logic die with hot spots that create conditions that exceed the thermal limits of the memory.

Helping to design with the understanding of the tradeoffs in the manufacturing process for TSVs will allow the creation of cost-effective designs that can be introduced to the market faster. Support from the EDA tool community is important in the adoption of both 3D IC and 2.5D (interposer) solutions.

## Interposer solutions

The interposer solution is poised to become more than just an interim game as companies find the cost effectiveness and performance gains of partitioning devices. By fabricating only the most critical features on the newest nodes and fabricating other functions in lower cost, older technology nodes, a more cost-effective solution is possible. Design tools are also critical in this area. Companies such as Xilinx pioneered the way for much of the infrastructure development with the introduction of a new field-programmable gate array (FPGA) architecture that has taken advantage of partitioning logic to provide a solution with higher bandwidth, lower power, and higher performance. This infrastructure, combined with supplier base and continued technology improvements to lower cost, will enable others to adopt this solution. The interposer solution is not without its own challenges including multiple vendors with silicon interposers, the development of low-cost interposer solutions, and assembly of die-on-interposers. Challenges for assembly include interposer warpage.

## Micro bump assembly

Another area that is receiving considerable attention is the micro bump assembly process. Making the bumps appears to be less challenging than the assembly process. The typical micro bump pitch today is 40 to 50 $\mu\text{m}$ , but some research organizations are discussing 30, 20, or even 10 $\mu\text{m}$  micro bumps for future structures. How will these bumps be bonded? What level of accuracy will be required for the bonding equipment? Do we even need a bump or should the industry migrate to a copper-to-copper direct bonding process? How do you know the bonds are good? What type of inspection is required? Depending on where the assembly is performed – at the foundry or the OSAT – inspection will be critical in determining who is responsible for defects.

## Test

In 2.5D solutions, the industry expects known good interposers, known

good memory stacks, and probably known good die, as concluded at the recent IEEE 3D Test Workshop. The introduction of 3D ICs requires new developments in test methodologies and strategies in design-for-test. While progress is underway, critical needs must be met in order to improve yields and final assembly, and reduce costs. What EDA tools are available to support test? What standards are available and is more work required? Is built-in self-test (BIST) adequate for most designs? Recent workshops on test indicate that progress is underway in many of these areas, but additional resources are required.

## Summary

The industry still has much work to do to develop true 3D IC processes that are higher yielding and result in lower costs. Progress in via formation and filling continues, improvements in the via reveal step, and improvements in throughput have contributed to a positive direction. But obstacles to high-volume manufacturing of 3D ICs with TSVs remain. Challenges include: cost/yield, design, the debonding step in the wafer thinning process, thermal dissipation where logic and memory or logic and logic are stacked, and test. Much hard work is still required before yields improve sufficiently to reduce the cost of the technology relative to established alternatives.

The casual observer should be reminded that infrastructure developments are key in the adoption of new technologies. In the case of 3D ICs, this means companies that can fabricate 3D IC designs, companies that offer assembly services, and equipment and materials that enable the production of cost-effective solutions.

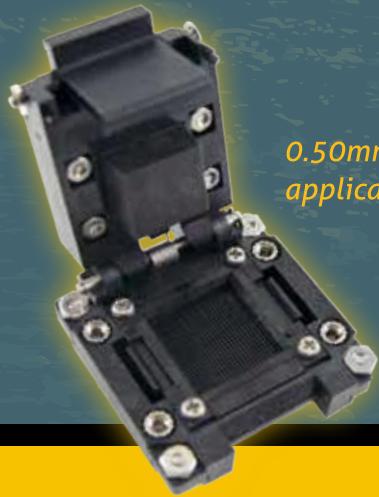
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# GUEST EDITORIAL



## Europe's microelectronics industry - as dynamic as ever!

By Steffen Kroehnert [[NANIUM S.A.](#)]

**S**EMICON Europa is the annual premier event for the global microelectronics industry in Europe. After being hosted in Zurich and Geneva in Switzerland, Munich, Stuttgart and Dresden in Germany, over the last 37 years, SEMICON Europa, one of the 8 SEMICON shows worldwide, in its 38th year took place from October 7-9, 2014, for the first time in Grenoble, France ([Figure 1](#)). From now onwards, the event location will alternate between Grenoble and Dresden.

Heinz Kundert, President of SEMI Europe, said in his welcome keynote address, that it was overdue and time for the move to Grenoble. The location was chosen as the event location based on the strength of its semiconductor ecosystem, with world class universities, R&D institutes and industry clustered around innovation. Along with the Dresden region, the Grenoble region is one of the

largest semiconductor research and manufacturing centers in Europe. Grenoble was indeed a great host of the event. A large majority of the attendees thought that this was a superb show with 300 speakers in 70 conferences or sessions.

Some facts released by SEMI Europe: 5,810 industry experts, professionals and executives attended SEMICON Europa, which makes it the largest industry event in Europe. There was a 28% increase in visitors compared to the previous year. With 424 exhibiting companies, the attendees saw 18% more exhibitors sharing 48% more exhibition space.

One of the reasons for the above statistics can be found in the increased attractiveness of the event, and the higher number and very good quality of the conferences and sessions, which took place in conjunction with the exhibition. Of course, being in Grenoble for the first time also

attracted new and other people to attend the event, and also some exhibitors pointed out that this is exactly the reason why they came to Grenoble, while they skipped exhibiting at SEMICON Europa in Dresden during previous years.

What were the highlights? To the point: it was more "SEMICON than ever." SEMICON Europa 2014 developed into a new platform with an increased spectrum of opportunities. One of the new venues at the conference included the Innovation Village: The Hub for Start-ups, Investors and Innovators, at which 30 start-ups used the chance to present themselves. In addition to the established conferences such as the Fab Manager's Forum, MEMS, Advanced Packaging, Test Manufacturing, Plastic Electronics, 3D IC Integration, 450mm Wafer Diameter, Secondary Equipment and Standards, there have been new conferences and programs including: 1) the Imaging Conference, 2) the Low Power Conference, and 3) the Power Electronics Conference. New topic segments included electronics applications and components, which had 39 exhibitors.

### Market update for Europe

Equipment spending in Europe is forecasted to be up by 48% in 2015 compared to this year (\$2.49bn to \$3.68bn), which is by far the highest growth compared to all other regions. Average growth of all regions is forecasted to be 11%. This data is supported by the European investment strategy and industry programs. Materials spending in Europe is forecasted to increase by 4% in 2015 compared to this year (\$3.13bn to \$3.24bn), which is also the forecasted average growth for all regions.



**Figure 1:** ALPEXPO Grenoble, home of SEMICON Europa 2014. SOURCE: SEMI Europe, 2014.

Talking about Europe, Dan Tracy, Senior Director, Industry Research at SEMI Headquarters summarized during the Global Semiconductor Market & Trends Overview that there are still 200 front-end entities (wafer fabs and silicon foundries) and more than 60 back-end entities (assembly, packaging and test facilities) in Europe. Front-end companies such as Intel



**Figure 2:** SEMICON Europa 2014 Exhibition Floor at ALPEXPO Grenoble.  
SOURCE: SEMI Europe, 2014

Ireland and Israel, STMicroelectronics, GLOBALFOUNDRIES, and Infineon, as well as imec (a major hub for start-ups, innovators and investors) are adding capacity in their lines in Europe, mainly for the 14nm CMOS technology node transition. Some of them, chiefly imec, are also evaluating 450mm wafer transition efforts. Europe is very strong in semiconductor equipment, but the semiconductor materials suppliers that together have more than 50% of the global share of the semiconductor materials market are in Japan, or at least headquartered in Japan. What we see is that the European microelectronics industry is as dynamic as ever, and Europe continues to provide a highly favorable environment for innovation and the development of new technologies (**Figure 2**).

Mid to high single-digit growth of semiconductor revenues is expected in 2014 and into 2015, where mobility, wireless, and connectivity remain the growth engines, especially for leading edge investments and advanced

packaging. The industry perceived a 7.9% market growth in Europe during the first semester of 2014, according to the WSTS association. Remarkable also is the fact that 50% of the semiconductors produced worldwide will be consumed in China. That is where the main markets are.

SEMICON Europa 2014 addressed the latest developments related to the Internet of Things (IoT) in the Electronics Conference, which focused on the automation level in fabs, and smart-connected sensor devices. SEMICON Europa highlights also included electronic applications such as imaging and nanoelectronics for healthcare, and electronic components for low power and power electronics. Consumers

continue to drive an ever increasing demand for mobile electronics and interconnectivity, for both work and play. New devices are being developed and sensor applications are soaring to meet future requirements for processing and transmitting data/information across a variety of applications such as healthcare, industrial, security, entertainment, energy efficiency, and others.

Networking opportunities were numerous (**Figure 3**) and were heavily used by the attendees. Still, the time between conferences, special sessions, supplier presentations and visits to the exhibitor booths at the exhibition floor often has been too short for all the contacts one wanted to make or sustain. That is the only negative side of having – to otherwise great advantage – so many suppliers, customers, competitors, institutes,

academic and political, all together in one place. Fortunately, the evening events allowed one to continue intense talks that began during the day. A highlight was the Gala Evening “Ice & Mountains” on Tuesday, October 7, 2014, at the Grenoble ice rink, Pole Sud, which was part of the 1968 Winter Olympic games. The program included “magic” lighting, ice and snow setting, sculptures from ice, even silicon wafers frozen in ice blocks, and artistic dancers on ice.

### Report from APC

The Advanced Packaging Conference (APC) – co-located with SEMICON Europa – turned out to be one of the best APC events ever. The conference committee comprised packaging experts from APT, CEA-Leti, Fraunhofer IZM, Hesse Mechatronics, IMAPS Europe, imec, Infineon, NANUM, NXP, Oerlikon, OSRAM, PacTech, Panda Europe, Robert Bosch GmbH, STMicroelectronics and YOLE Développement. They, along with support from SEMI Europe, organized a conference that for the first time included poster presentations and a panel discussion.

For its second year, the conference’s theme was “The Power of Packaging.” Two major issues were addressed: 1) The increasing importance of system integration in package, means more powerful value add for packages and systems, and 2) the packaging of



**Figure 3:** Networking opportunities everywhere at SEMICON Europa.  
SOURCE: SEMI Europe, 2014



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### MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

power semiconductors, which is one of the main topics in the European semiconductor industry. Two keynotes, 10 presentations and 6 posters were presented. The keynotes were given by Continental Automotive GmbH and Airbus France and addressed the topics of what is needed to be successful in those markets, and why manufacturing in Europe is one of the keys for this success.

More than 100 people registered for the conference and 89% of the participants ranked the conference excellent or good. Another 93% answered "yes" to the question asking if they learned something that can be applied to their work. This result underlines the value brought to the attendees of the conference.

Some of the main topics at APC were the packaging strategy for power and automotive applications into advanced packaging technologies originally developed for consumer and mobile markets, all kinds of embedding technologies, even embedding of already embedded components into organic laminated printed wiring boards (PWB), new ways of laser and plasma dicing of silicon and compound materials wafers, Ag wire as an alternative to Au and CuPd wire, die attach by Ag sintering for direct copper bonded (DCB) and lead frame-based power applications, which turn out to be two different challenges for the same material.

The highlight of the conference was the panel discussion "Packaging in Europe - Future Opportunities." As shown in **Figure 4** (far left), the panel was moderated by Jean-Christophe Eloy, President and CEO of Yole Développement. The panelists (continue moving left to right in **Figure 4**) came from across our industry: a good mix of OEMs, IDMs and the following OSATs: 1) Philippe Pons/Airbus France; 2) Andreas Fischer/Robert Bosch GmbH; 3) Jean-Marc Yannou/ASE Group; 4) Harald Fritzsche/Continental Automotive GmbH; 5) Armando Tavares/NANIUM, S.A.; and 6) David Clark/



**Figure 4:** Panel session, "Packaging in Europe - Future Opportunities," at the Advanced Packaging Conference. SOURCE: NANIUM, 2014

Amkor. Among the discussion topics: 1) what needs to be done to strengthen semiconductor packaging, assembly and test industries in Europe; 2) where the opportunities are seen, what are the requirements of the customers, and 3) where can Europe utilize its advantages and strengths by reacting to those requirements. All agreed that the current trend for more system integration towards more complex system-in-package, embedding solutions, wafer-level packaging and More-than-Moore realization has potential for our industry in Europe as more innovation and engineering power, very close cooperation in the entire supply chain, co-design and co-development capabilities, and also the close and efficient link between industry and academic and institutes are more important now than ever before.

### ESPAT founding meeting

On October 8, 2014, in the afternoon, the European Semiconductor, Packaging, Assembly and Test interest group (ESPAT) founding meeting took place in the presence of 30 of the approximately 50 companies and associations that had shown an interest in this initiative. During preparations for this meeting, many of these companies already contributed a list of their expectations and possible contributions to the group, which were then discussed during the meeting. The aim of the

group is to strengthen and grow semiconductor packaging, assembly and test manufacturing in Europe by 1) Analyzing what is left in this field in Europe, 2) Identifying gaps that need to be addressed to ensure compliance to international roadmaps, 3) Bringing together the involved community, 4) Stimulate investments, 5) Give ESPAT a voice on both,

the national and European levels, and last but not least in cooperation with other associations, 6) Training and educating the next-generation of packaging manufacturing experts. Of the participants, 70% voted for working towards forming a SEMI Special Interest Group (SIG) out of the industry interest group within the next year. *Chip Scale Review* reported about the plan to set up ESPAT in its March-April 2014 edition ("Semiconductor packaging, assembly and test in Europe," pp.: 46-49).

The next face-to-face ESPAT meeting is planned for June 2015, in combination with the SEMI - Packaging TechSeminar (formerly called "SEMI - Networking Day") Q2/2015 hosted by NANIUM S.A. in Vila do Conde, Portugal. The theme will be: "European ShowCase – Semiconductor Packaging, Assembly and Test."

We all are looking forward to next year's SEMICON Europa in Dresden, Germany, taking place October 6-8, 2015.

### Biography

Steffen Krohnert received his masters degree in Electrical Engineering and Microsystem Technology at the Technical U. of Chemnitz, Germany and is Director of Technology at NANIUM S.A.; email Steffen.Krohnert@nanium.com

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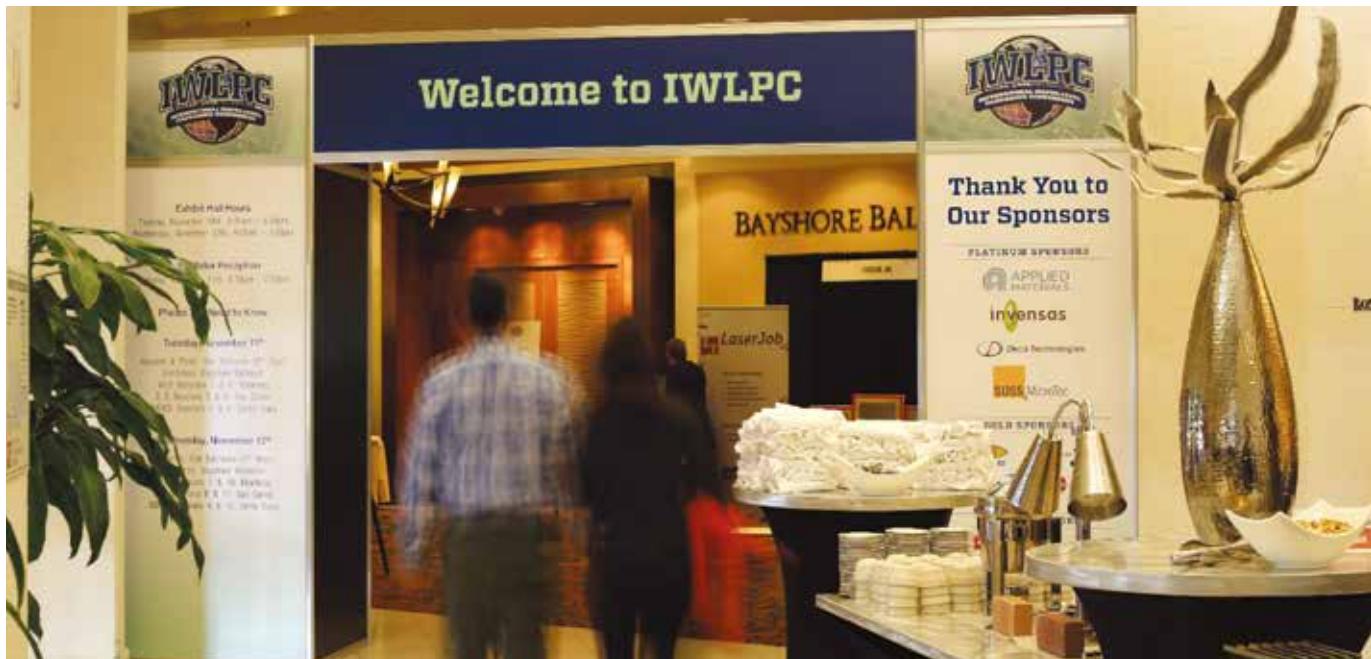
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# INDUSTRY NEWS



## IWLPC – Gateway to 3D, TSV, WLP & MEMS device packaging

By Chip Scale Review staff



The 11th annual International Wafer Level Packaging Conference (IWLPAC) 2014 was held at the DoubleTree Hotel in San Jose, CA on November 11 – 13, 2014.

IWLPC brought together the semiconductor industry's most respected authorities addressing all aspects of wafer-level, 3D, TSV, and MEMS device packaging. The technical program featured 48 excellent presentations organized in three parallel WLP, 3D,

and MEMS tracks over the course of two days.

This event continues to grow every year as wafer-level packaging gains traction in the semiconductor industry. The overall attendance of 839 technologists from 19 countries in 2014 grew to nearly 46% more attendees than the 2013 event.

This year's event opened with the keynote address from Dr. Janusz Bryzek, Chair of the TSensors Summit entitled "Living Connected Through Trillions of Sensors." In addition, there was a MEMS plenary talk by Dr. Mehran Mehregany of Case Western Reserve University entitled "Wearable, Wireless Health Solutions and Related Packaging Challenges" and a WLP plenary talk by Ted Tessier of FlipChip International entitled "Wafer-Level Packaging Innovations to Enable Wearable Electronics." It's apparent that the market for wearable medical electronics devices is the dominant driver of both wafer-level and MEMS packaging in the near-term.



Shekar Krishnaswamy of Applied Materials session Mobile Applications to Enhance Manufacturing Productivity in Advanced Packaging



3D Panel discusses System Level Advantages of 3D Integration

Francoise von Trapp of 3D Incites moderated a stimulating and interactive panel discussion on "System Level Advantages of 3D Integration." Using a cell phone app, about 60 audience members participated by voting on a number of statements regarding the current status and readiness of 3D integration.

One of the distinguished panelists and industry veteran, E. Jan Vardaman, of TechSearch International observed, "The



IWLPC provided a wonderful opportunity for discussion of a variety of topics ranging from WLPs and MEMS to 2.5D and 3D ICs. The excellent networking opportunity with a combination of international participants with an influx of local Silicon Valley companies made it an event worth attending.”



Session attendees



Garrett Oakes of EV Group and Peter Ramm of Fraunhofer Research Institute



Bob Patti Tezzaron meets with Nagesh Vodrahalli of Allvia



Applied Materials Shekar Krishnaswamy & David Hanny



Exhibitor LBSemicon



Paula Faria of NANUM



Richard McKee of Pac Tech, Jaye Hayes of Unisem, Jim Walker - Gartner Research



Session with Maaika M. Visser Taklo, SINTEF

The exhibition hall was “sold out” again this year by 58 companies promoting their products and services, including Platinum-level sponsors, Applied Materials, Deca Technologies, Invensas, and SUSS MicroTec.

Several of the exhibitors mentioned that the narrow technical focus and Silicon Valley location of this event brought them a number of highly-qualified leads.

The third and final day of the conference featured four outstanding tutorials on various aspects of wafer-level packaging and 3D integrated circuits. They were taught by Dr. Luu Nguyen of Texas Instruments, Dr. Ning-Cheng Lee of Indium Corporation, Dr. Leland “Chip” Spangler of Aspen Microsystems, and the ever-popular Dr. John Lau of ASM Pacific Technology.

Keith Cooper of SET North America, and this year’s IWLPC General Chairman, summed it up best when he said, “IWLPC 2014 – Wow, what a great event we had! From the fantastic opening keynote by Janusz Bryzek about sensor proliferation, to all the technical sessions to the four excellent tutorials, I was absolutely delighted with the high quality technical interaction. Not only did we have a panel of industry gurus on stage (and at times on the hot seat) to discuss 3D integration, we also were treated to stimulating plenary presentations on the topics of wireless healthcare devices and wearable

electronics. My heartfelt thanks to all who worked so hard to make this event a grand success! Mark your calendars now for October 13-15, 2015, as we continue to define the future of advanced packaging in the heart of Silicon Valley.”

*(continued on page 51)*

# A 3D technology platform: from process toolbox to functional demonstrators

By Thierry Mourier, Séverine Chéramy, Patrick Leduc [CEA-Leti]

**I**t is commonly established that 3D integration is a key technology for current and future system-on-chip (SoC) designs. The panel of potential applications is very wide, extending from mobile and wearable electronic goods (e.g., medical sensors, watches) to very high-performance servers and micro-servers and automotive products.

Several integration approaches can be considered to realize 3D integrated circuits for these applications. The integration approach is classically driven by the product requirements, but this also is a combination of manufacturability, cost (development, product), time-to-market, investment, supply chain, scalability, etc. In the end, so many factors can lead to many different integration flows.

To ease the transfer from development to industrialization, and to realize these products in a short time-to-market, accessibility to a complete supply chain from design to early integration and packaging is mandatory during the early development phase. This principle is the basis of Leti's 3D platform in Grenoble, France. The concept of the 3D toolbox is defined to accommodate any partner that wants to convert an idea or functionality to a final product.

The technology platform must be as compatible as possible with any requested integrations and partners' equipment. Earlier partners used 200mm fabs. For this, a compatible platform was developed in 2005; but the new generation of products uses mid-process integration on 300mm wafers. For this reason, a complete 300mm pilot line at Leti was also inaugurated in 2011.

Both pilot lines perform state-of-the-art individual processes and modules to ensure standard integration, but also to prepare the next generations and anticipate new processes or new material needed in the roadmap. Examples are listed below:

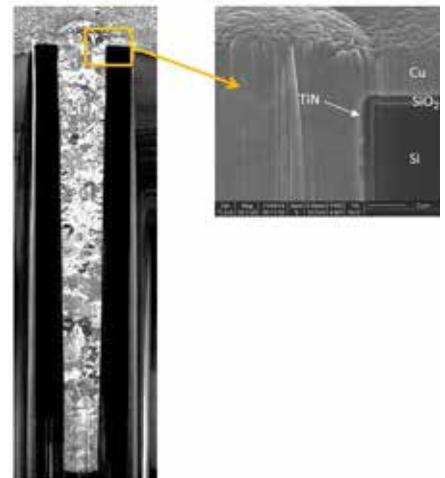
**Through-silicon vias (TSVs).** For mid-process vias, 10 $\mu\text{m}$  (diameter) by 80 $\mu\text{m}$  (depth), and 6x55 $\mu\text{m}$  TSVs were developed (aspect ratio 8:1). New products require aspect ratios of 10:1 and higher. These geometries almost reach the limitations of actual ionized physical vapor deposition (iPVD) barrier and seed deposition and

will require an alternative solution to be quickly developed. Indeed, there is a real need for a higher TSV aspect ratio to keep a sufficient silicon thickness, to reduce the TSV + Keep Away Zone area, or to increase the TSV density, etc. For this purpose, close collaborations with tool suppliers were established. For instance, Leti and SPTS Technologies are working, through a common laboratory, in the field of TSV insulation and metallization – specifically on chemical vapor deposition (CVD) TiN and Cu seed layer deposition. **Figure 1** shows the complete filling of a 10x120 $\mu\text{m}$  TSV (12:1) with the integration of a very conformal (>30% step coverage in 20:1 AR feature) 10nm-thick metal organic chemical vapor deposition (MOCVD) TiN barrier.

Other work is underway on full wet technology, which could also have the advantage of reaching high TSV aspect ratios. This work is being done in collaboration with Alchimer. In parallel, work on dense TSVs (range of diameter about 1-3 $\mu\text{m}$ ) is ongoing. This TSV work highlights Leti's possibility: provide state-of-the-art processes, pushed to their technical limit (iPVD: aspect ratio >10:1), provide advanced developments on alternative technologies and launch a technical benchmark, including equipment, material and processes (CVD/wet).

**Chip-to-chip interconnection.** Copper pillar soldering is the primary choice for micro bump diameters, ranging from 50 to 20 $\mu\text{m}$ , but smaller pitch (<20 $\mu\text{m}$ ) is also addressed. Underfill technology has to be developed in parallel to the chip-to-chip interconnection. Leti focuses its work in this area on pre-applied underfill: chip (non-conductive paste) or wafer-level (wafer-level film). This study takes into account die size, density of interconnections, the gap between chips in the z direction, the gap between chips in the x and y directions, etc.

For this study, a Panasonic FCB3 machine and a vacuum laminator for the wafer-level film are used. As for TSVs, a complete study is proposed, easily transferable, if needed: a material benchmark and associated processes, in this case based on state-of-the-art equipment. A test vehicle is used for the benchmark, and in case of specific needs

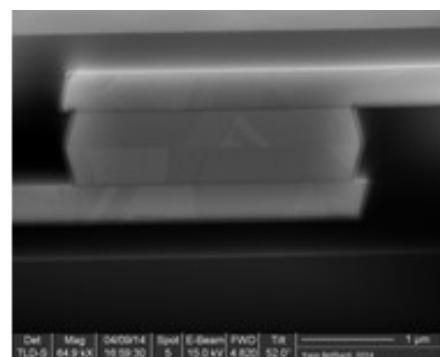


**Figure 1:** A 10X20 $\mu\text{m}$  TSV filled with Cu; the view shows excellent coverage of the MOCVD TiN barrier.

from partners and specific dies to test, it is easy and quick to check their feasibility.

This "copper-pillar + underfill" approach has the advantage of being quite standard in the packaging world, except for the pitch. Two main factors can nevertheless appear as constraints. First, the underfill may be increasingly difficult to dispense and can also bring a possible mechanical constraint to the final stack. Second, the pitch will probably be limited (a 20 $\mu\text{m}$  pitch may be the limit).

When a very high density is needed, or when we need to remove the underfill, Cu-to-Cu bonding is also proposed, as shown in **Figure 2**. This technology is available with a wafer-to-wafer (WtW) approach, and under development and industrialization with a die-to-wafer approach (DtW). Our



**Figure 2:** Cross-section of hybrid direct bonding: Cu/Cu and SiO<sub>2</sub>/SiO<sub>2</sub>.

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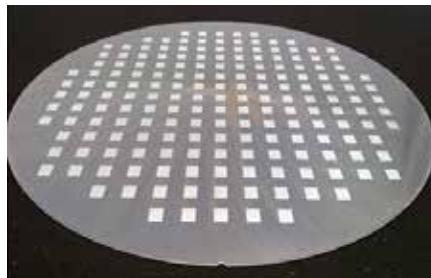
approach on Cu-to-Cu is “techno-push:” develop the technology and the process, provide design rules, provide a pitch that can be obtained for WtW or DtW, provide full characterization (DC and RF) and model. With this approach, many designers have at their disposal the complete library of technological solutions.

**Temporary bonding.** Some 3D integration flows require a temporary bonding process on a carrier or on the stacked die. Depending on the integration scheme, polymer-based temporary or permanent bonding on glass or silicon were developed through strong partnerships with equipment suppliers (EVG, Yushin) and materials experts (3M, Brewer Science, and others) to face any type of integration request. Bonding and debonding are obviously key factors in selecting a material and equipment, but these are not sufficient to prove the full integration. For that reason, Leti has worked on “short-loop” integration batches, including plasma-enhanced chemical vapor deposition (PECVD) deposition, to test the bonding quality and compare the different solutions: laser debonding, wet debonding, mechanical debonding. Comparative data are then obtained and provided to the material or equipment supplier, or foundry and outsourced semiconductor and test (OSAT) facility.

**Wafer-level packaging.** Leti has chosen to work on specific assembly steps that are, or could be done, at wafer level. These steps include handling and dicing of thin wafers, chip-on-wafer stacking, wafer-level molding, and chip-to-substrate bumps. Most of these processes have been developed and are now available. For instance, concerning wafer thinning, a collaboration with DISCO allows our partners access to the most advanced tools and processes. Concerning die-to-wafer stacking, advanced underfill materials are evaluated using the 3D platform.

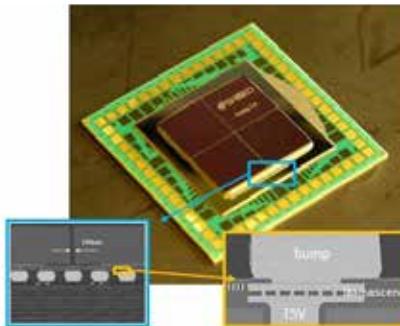
To ensure a low warpage of the chip-on-wafer assembly, specific developments have been done on polymer wafer-level molding used to planarized the assembly. This low-stress process will have multiple advantages by allowing planarization after a die stacking, replacing a temporary bonding in the case of high thickness, stiffening a thin interposer, filling a TSV or a hole, and more. **Figure 3** represents a 300mm wafer with multi-dies stacked, and with a polymer planarization that has been ground to expose the die. The sufficient maturity of the process modules allowed the realization of fully functional demonstrators.

Silicon interposers are known to be a driving application for 3D integration, whether they are passive, RF or, in the future,



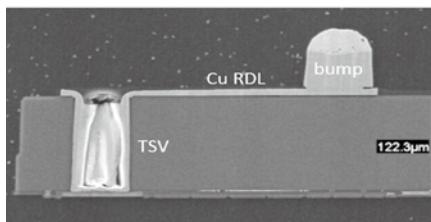
**Figure 3:** Die-to-wafer stacking and polymer planarization.

photonic devices. They were the products on which 3D integration on 300mm wafers was successfully delivered. **Figure 4** shows a global view of four circuits stacked by our



**Figure 4:** Four dies stacked on a 100 $\mu\text{m}$ -thick silicon interposer stacked on a board. (Courtesy of SHINKO)

partner, SHINKO, on a 100 $\mu\text{m}$ -thick silicon interposer stacked on a ball grid array (BGA). It also shows zoomed in areas on the high-precision alignment between each die and the mid-process 10 $\mu\text{m}$ -diameter TSV connected to a copper pillar through damascene interconnections. **Figure 5** shows the cross



**Figure 5:** Cross section of a TSV-last RF interposer.

section of another integration choice for an RF silicon interposer designed to integrate the antennas on silicon for further high-density stacking of RF chips. In this case, the choice was made of a TSV-last option with routing through a copper redistribution layer (RDL) to the micro bump.

The second major application for 3D technology is the heterogeneous integration of system-on-chip (SoCs) ICs made with different technologies to realize a complete function. The example given in **Figure 6** shows a test vehicle, “3D-Learn,” made in the frame of the IRT Nanoelec program.



**Figure 6:** Cross section of the test vehicle “3D-Learn.”

This test vehicle, from its conception to its packaging, was developed to be a source of “3D learning.” It consists of a multi-project wafer, whose fabrication (FEOL, BEOL, 3D, packaging) is representative of a real product, but whose dies are dedicated to characterization: process development, reliability, RF modeling and thermal characterization.

## Summary

Leti is part of the Grenoble ecosystem open to any partners whose goal is to convert ideas to fully functional demonstrators. Partners who want a dedicated study on a specific 3D module, such as temporary bonding, TSV or interconnection, can also take advantage of Leti’s 3D state-of-the-art equipment. This campus includes the modeling and design activities, the clean rooms for the silicon fabrication, and the characterization platforms including testing facilities. It was built to implement various types of integrations on different technologies in close partnership with industrial partners through bilateral or collaborative projects, or in the frame of the IRT Nanoelec 3D program.

## Acknowledgement

Part of this work on 2.5D and 3DIC is funded thanks to the French national program “Programme d’Investissements d’Avenir, IRT Nanoelec” ANR-10-AIRT-05.

## Biographies

Thierry Mourier holds an Engineering degree with a specialty in Electrochemistry from the Conservatoire National des arts et métiers in Grenoble. He is in charge of the development of deposition processes for 3D and WLP technologies at Leti; email thierry.mourier@cea.fr

Séverine Chéramy received her Engineering degree with a specialization in Material Science from École d’ingénieurs Polytech in Orléans, France. She heads Leti’s 3D Integration Lab.

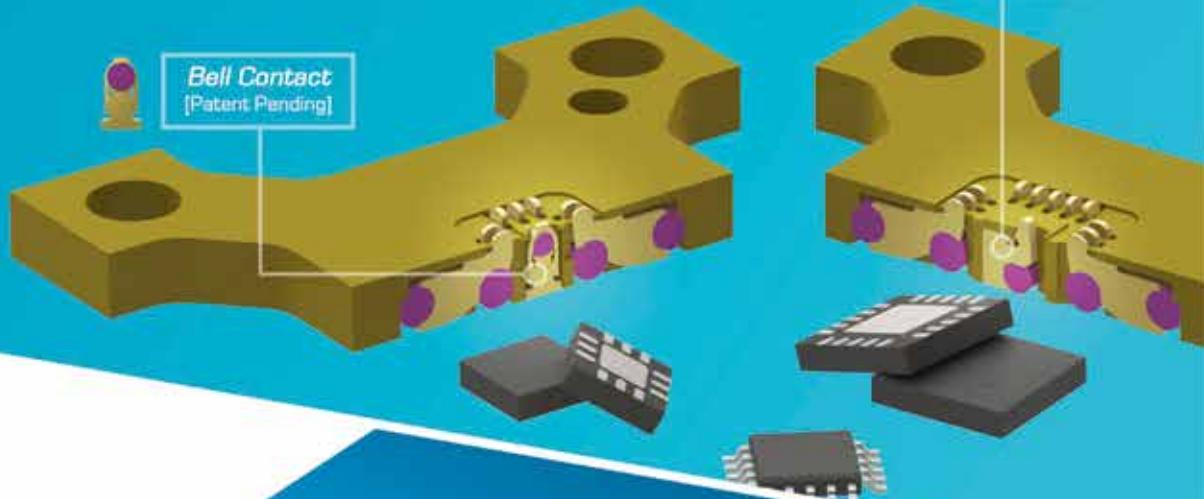
Patrick Leduc received his MS degree in solid-state physics from the Institut National Polytechnique in Grenoble (INPG). He is 3D IC program manager at Leti.



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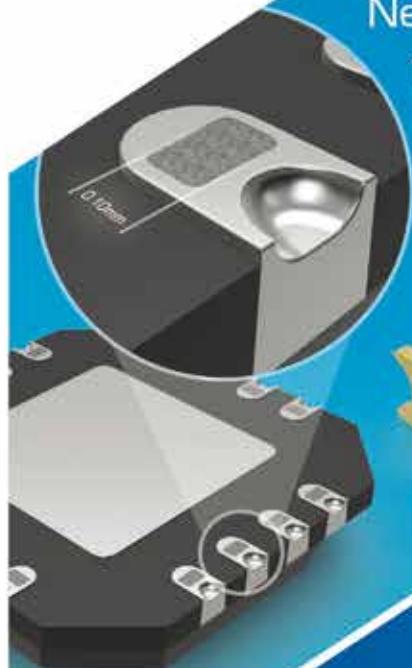
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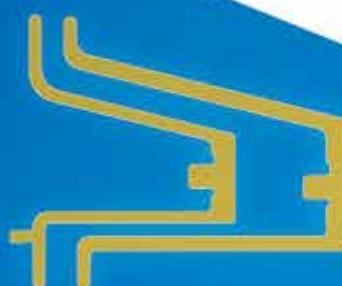
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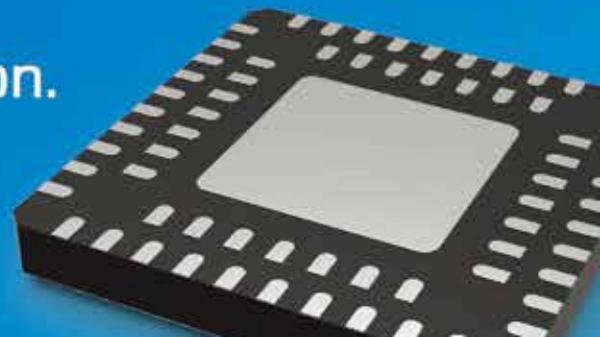
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# Leadless lead frame packaging for automotive and high-density requirements

By Lee Smith [United Test and Assembly Center (UTAC)]

**L**eadless lead frame based packages first saw broad adoption and industry infrastructure development with Fujitsu's introduction and licensing of its "bump chip carrier (BCC)" package in 1997 [1]. UTAC Thailand (previously NSEB) was an early licensee of the BCC technology. Over the past 17 years there have been continuous advancements in density, thickness, reliability and performance, which have resulted in leadless lead frame packages forecasted to be the largest package segment on a unit basis—approaching shipment levels of a billion per week for 2014 [2]. These leadless lead frame based packages may go by different suppliers' names, but the JEDEC designation of quad flat no lead (QFN) is the dominant package type and will be used generically in this article. The vast majority of QFN packages have a single row of perimeter pads limiting their application to low pin count devices – typically below 100.

The broad adoption and rapid growth of QFN packages are due to their cost and size advantages over conventional leaded packages like small outline integrated circuit (SOIC) and QFP. However, harsh environment and high-reliability applications such as automotive, have required advances in the leadless structure to enable a full solder joint fillet to enable automated optical inspection (AOI) systems to validate that all leads have a solder fillet to ensure optimum solder joint integrity to withstand temperature cycle life solder fatigue and mechanical vibration or shock failures. To enable full solder joint fillets, saw and punch singulation processes must be advanced to ensure side wall plating of the perimeter copper lead to enable solder wetting. **Figure 1** outlines the process flow with the addition of a step cut process prior to lead plating to enable plating of the side flank of the perimeter lead. **Figure 2** provides cross section views to verify control of the step cut depth and

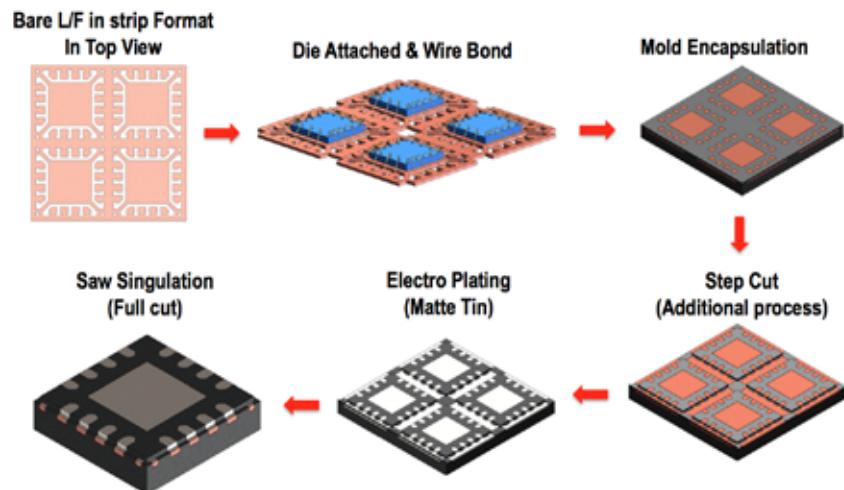


Figure 1: WFN side lead plating flow.

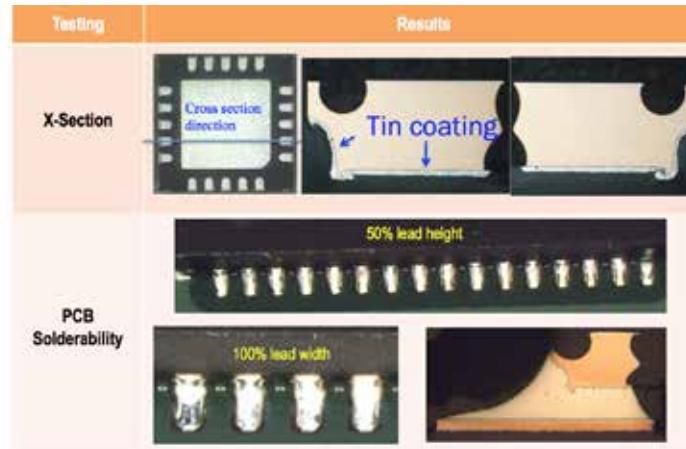


Figure 2: QFN side lead plating cross section views.

uniform thickness of the matte tin plating across the lead base and side wall flank. Cross section views are included after surface mount solderability testing to demonstrate 50% lead height and 100% lead width solder coverage. UTAC QFN packages have utilized an optimized material set and process to ensure JEDEC moisture sensitivity level 1 (MSL1) at 265°C for years. The addition of the step cut and side lead plating has been qualified to MSL1 as well. Full UTAC internal board-level reliability results will

be complete in Q4, 2014. End users for automotive applications have completed their internal qualification and UTAC is in production with side lead plated QFN packages for automotive applications. It is expected that aerospace and harsh environment industrial applications will also see the advantages that side-plated QFN leads can provide in their high-reliability applications.

To address higher I/O density applications, IC designers have been

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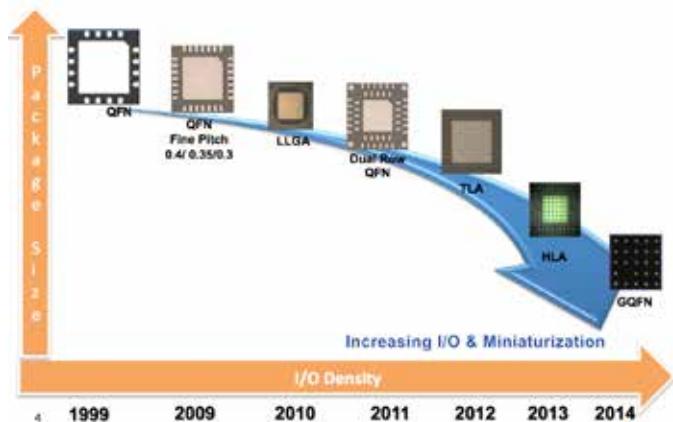


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demanding a low-cost QFN package solution that includes interconnect trace routing to enable multi-row and full array pad configurations. A number of solutions have been developed to achieve multi-row lead density, some of which are in production with some success. **Figure 3** provides a history of the milestones for new leadless lead frame solutions that UTAC introduced since its early success in BCC and adding QFN in 1999. Details of these new higher density leadless lead frame packages such as, the leadless lead frame grid array (LLGA), the thermal leadless array (TLA), and the high-density leadless array (HLA), were reported in industry publications [3–6]. Supply chain, cost, and manufacturability obstacles, however, have limited adoption and scale up of these solutions. Therefore, new approaches that utilize standard assembly processes have been sought to serve applications demanding the highest I/O density with lead frame trace routing technology. Recent advancements at UTAC show promise in overcoming these obstacles and are in the process of scale up for high-volume manufacturing.



**Figure 3:** UTAC leadless lead frame milestones.



**Figure 4:** UTAC GQFN (grid array QFN) process.

The process and materials technology advancements enable multi-row and full grid array pad densities with high-density lead routing and interconnects to serve a wide range of IC designer's single, multi-chip and passives integration configurations; the acronym GQFN will be used for grid array QFN in this article.

## Key processes and GQFN configurations

**Figure 4** illustrates the key process flow and area array configurations enabled with a routable lead frame-based technology. A partially etched and pre-plated lead frame is designed, fabricated and delivered to the package assembly line where die attach and wire bond are performed. (Flip-chip, stacked die, and passive integration options are all supported but not shown here.) Following mold/post-mold cure, two critical processes are used—processes not found if standard QFN process flows are utilized. The two processes are: 1) etch back of the lead frame carrier to complete the trace routing and isolate the pre-plated leads, followed by 2) an insulation mold process to complete the package

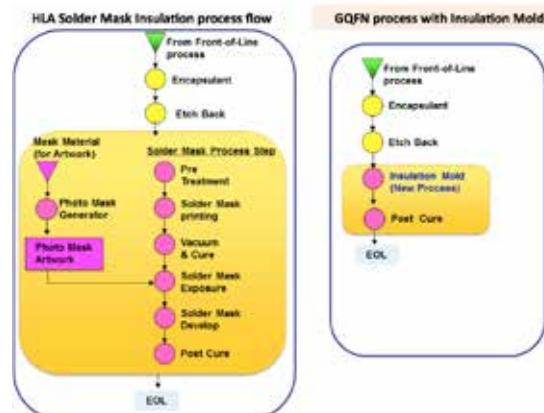
encapsulation. If the product board surface mount assembly dictates, a printed solder bump or ball drop for higher stand-off can be completed before package saw singulation.

Etch back has been used for many years in leadless lead frame production, beginning

with the BCC technology. A solder mask-based lead insulation process has been introduced as a high-density leadless array (HLA) solution for area array QFNs, but as **Figure 5** shows, it requires a complex multi-step process flow vs. the insulation mold process development for the GQFN package. The challenges associated with this solder mask insulation process raises cost and manufacturing challenges that are limiting adoption and scale up of the HLA solution. To address these limitations UTAC evaluated options and focused on development of an insulation mold process for GQFN.

The insulation mold process poses assembly challenges as well, and overall optimization was conducted to address these challenges. A number of process and material factors had to be overcome in the development to deliver a high-volume capable insulation mold process. Factors include: 1) Mold tool design – cavity, gate, runners and air vents; 2) Film assist molding – film material and process parameters; 3) Mold clamp pressure, transfer profile and pressure; and 4) Mold material properties and fine filler technology.

**Figure 6** illustrates the key process options available for wire bond devices. Lead frame options include 4 or 5 mil copper carriers with either NiPdAu or selective Sn plating. Die thickness is 4 mils for epoxy paste or die attach film (DAF), development is underway to enable 2 to 3 mil die thickness with the use of DAF. Wire options include Au, PdCu or Ag alloys in various wire diameters based on die bond pad openings. Mold caps range from 0.75mm for stacked die or thick component system-in-package (SiP) configurations to 0.25mm for thin package applications that require a 0.5mm maximum package



**Figure 5:** Insulation mold vs. solder mask insulation.

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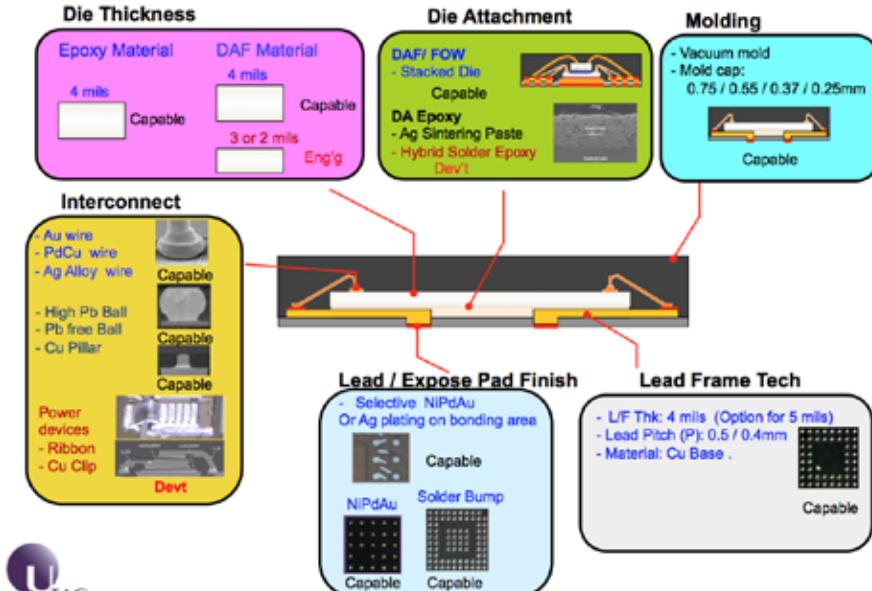


Figure 6: GQFN wire bond process options.

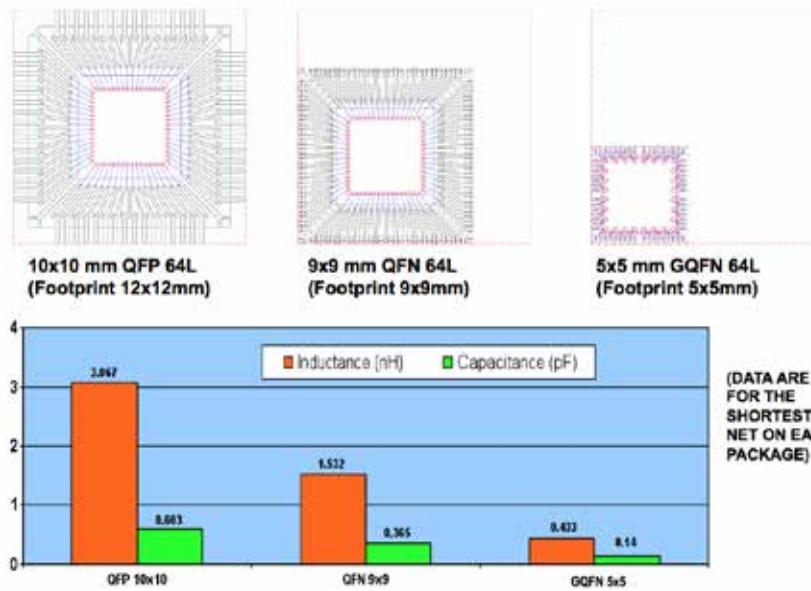


Figure 7: Electrical performance comparison: QFP/QFN/GQFN.

thickness. Development is planned for power devices that require ribbon bonding or copper clip assembly.

Current designs in GQFN technology have enabled 40 to 60% reduction in package size vs. a QFN because of their ability to route leads under the die area. The higher interconnect density of this technology enables bond finger location flexibility to improve wiring diagrams to handle complex die pad layouts and multi-, stacked die, and SiP configurations. Shorter wire lengths

are enabled that can provide improved electrical performance with lower inductance and capacitance as shown in **Figure 7**. Here the package size and electrical performance advantages are shown for GQFN vs. a QFN or QFP package with 64 leads. For RF and power management SiP applications, in addition to lower electrical parasitic performance, GQFN has shown lower thermal resistance offering both improved electrical and thermal performance vs. various design approaches to achieve improved performance in organic substrate-based land grid array (LGA) packages widely used in SiP applications.

## GQFN board-level reliability (BLR)

Mobile applications require new package technologies to retain solder joint integrity over more stringent temperature cycle stress and drop shock use cases. To evaluate BLR for the grid array QFN technology, a 5x5x0.45mm 79-lead GQFN with a wire bonded 2.9x2.6x0.1mm die was tested. Because this 79-lead GQFN design reduces the package size by 60% vs. a QFN, the increased die-to-package ratio poses concerns on board-level reliability as the silicon coefficient of thermal expansion (CTE) mismatch between package and PCB will have a greater impact on solder joints, especially those under the die edge regions. The package structure for GQFN 5x5x0.45mm 79 leads is shown in **Figure 8**.

The 5x5mm extremely thin (XGQFN) packages were surface-mount attached to 200x150mm boards and subjected to accelerated life tests to determine their second-level reliability. The temperature cycling accelerated test condition was -40°C to 125°C with 15mins dwell/ramp. The Weibull plot (**Figure 9**) shows the characteristic life, which is defined as the number of life cycles at which 63.2% of the test components have failed. Although the die-to-package ratio is very high at

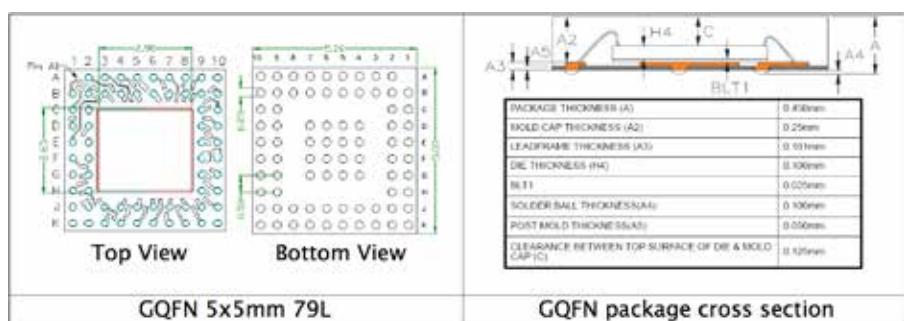


Figure 8: a) (left) Package structure for GQFN 5x5x0.45mm, 79 leads; and b) (right) a GQFN package cross section.

58%, the XGQFN 5x5mm had excellent TCoB performance with the first failure at 2,680 cycles and a characteristic life of 4,600 cycles (**Figure 9**).

### Board-level drop test

Demanding handset use cases are driving mechanical drop shock resistance targets up, with customers requiring

data up to 1,000 drop cycles. XGQFN 5x5mm packages were mounted on a 132x77x1.0mm 8-layer board, which was designed to form an integrated daisy-chain. The test method is composed of free-fall dropping the board using a drop table from a specified height that corresponds to JEDEC Condition B (1500 Gs, 0.5ms duration, half-sine pulse) as listed in JESD22-B110 Table 1. The XGQFN 5x5mm package had excellent drop performance with the first failure at 470 cycles with a characteristic life of 950 cycles that passed mobile customers' harsh test criteria (**Figure 10**).

The density advantages of using flip-chip in QFN packages combined with copper pillar bumping will combine to enable a wider range of devices and applications to take advantage of the size, thermal and electrical performance advantages that are inherent with flip-chip packaging.

**Figure 11** shows a cross section of a design that utilizes flip-chip copper pillars in a GQFN package to provide a unique arrangement of thermal pads and signal lands. The

design achieves a small package with a high die-to-package size ratio along with good thermal and electrical performance.

### Summary

Advances in leadless lead frame assembly, materials and process technologies enable QFN packages to address challenging application and device requirements through improved reliability and higher I/O densities. The addition of a step cut process before lead plating enables plating of the lead side wall flank

to improve solder joint integrity and AOI inspection through the formation of a full solder fillet. This improvement allows QFN packages to be utilized in harsh or higher temperature applications to better serve the high-reliability requirements driven by the automotive market. The development of an insulation mold process addresses and resolves many of the manufacturing challenges that have been limiting the adoption and applications for multi-row and area array QFN packages. The combination of robust etch back and insulation mold processes enable higher I/O density and design flexibility in QFN packages that allow grid array QFN (GQFN) packages to address designs that, to date, have required a 2 to 4 layer organic laminate fine-pitch ball grid array (FBGA) or LGA package. GQFN technology allows flip-chip, stacked die and passive integration into low-cost lead frame-based packaging to fuel continued growth in leadless lead frame applications.

### Acknowledgements

The author thanks Jun Dimaano Jr. of UTAC Singapore, corporate R&D, and Saravuth Sirinorakul of UTAC Thailand, site R&D.

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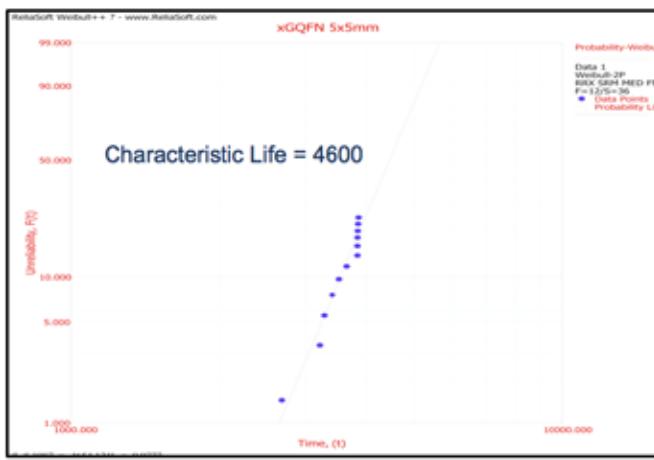


Figure 9: TCoB: Weibull plot.

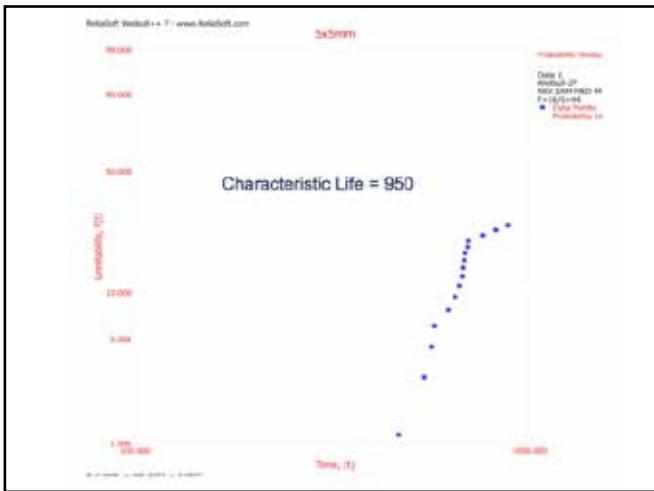


Figure 10: Drop test: Weibull plot.

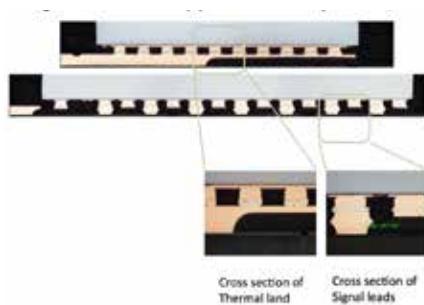


Figure 11: FC with copper pillar bumps in GQFN.

# An alternative PoP stacked packaging solution using an organic substrate interposer

By Steven Lin [Siliconware Precision Industries Co., Ltd.]

Just like CPU architecture drove the semiconductor industry during the PC era, the application processor (AP) is the most important component in every mobile product and therefore, drives the industry. Because of dimension and power limitations, APs require a unique and integrated package solution to meet thermal, electrical and mechanical requirements.

Package-on-Package (PoP) is an integrated circuit packaging method to vertically combine discrete logic device and low power mobile memory packages. Two chip-scale ball grid array (BGA) packages are installed atop each other, i.e., stacked, with a specific interface to route signals between them. This configuration enables a higher component density in devices such as smartphones, tablets, and other hand-held products.

PoP technology was widely used in mobile phones for the bottom flip-chip chip-scale package (FCCSP) digital AP to stack with a top wire bond low power double data rate (LPDDR) chip-scale package (CSP). The bottom FCCSP package form factor and its pin up of top solder balls were limited by the LPDDR BGA matrix, which had been defined by JEDEC. Because of high-bandwidth memory requirements for smartphones, a lot of new PoP solutions to accommodate more I/Os between the top LPDDR memory package and the bottom digital application processor package are becoming a reality.

One alternative PoP, or so-called high-bandwidth (HBW) PoP, is to place an additional routable substrate on the package top as an interposer. This design can be widely connected with LPDDR4, high-I/O memory and other analog/digital devices. The technology can even be regarded as a platform to accommodate non-LPDDR devices such as PMICs, RFICs, etc.

In this study, HBW PoP is a 3D structure that combines an “organic substrate interposer” with an embedded mold compound in the bottom package as the connection interface with the top package is introduced. This design will bring benefits, not only providing more I/Os, but also more

flexibility to accommodate different package sizes to stack on the top, for non-LPDDR devices like PMIC, RFIC, etc., to form multi-functional system-in-package (SiP) modules, or even the increasingly important applications of wearable electronics or the internet of things (IoT). That is, compared with a traditional PoP without an interposer, an additional organic substrate interposer (with full matrix I/O pad layout) can build a fully functional system and achieve the wide I/O memory goal. This structure, however, will bring some major assembly challenges, such as package warpage, mold compound voiding, and in-line process defect detectability issues. The solutions to solve those defects were developed with considerable engineering efforts.

In the study, many mechanical simulation models and design of experiments (DOE) studies were used to address how Cu pillar bump height changed (e.g., solder tip height adjustment in Cu pillar bumps) and how process tooling design optimization (e.g., substrate carrier and cover jig design and material adjustment) can effectively improve the Cu pillar solder joint failure rate. Moreover, mold compound and substrate core material properties (such as the coefficient of thermal expansion [CTE] or modulus property adjustment) can effectively reduce package warpage. Subsequently, improvement of stacking PoP or surface mount technology (SMT) yields were addressed in the study.

## HBW PoP feasibility study

In general, the main attribute of the HBW PoP structure in terms of I/O

count is the interconnection of the Cu ball and Cu stud between the top interposer and the bottom substrate. A Cu stud at both sides can accommodate more I/O counts (over 1000) while a Cu ball and one side Cu stud cause a restriction on the ball pitch and on the substrate aspect ratio (A/R; Cu stud height/diameter). The pitch limitation will therefore be around 0.27mm. However, the two side Cu studs can approach a pitch of 0.2mm (**Figure 1**). Based on the current substrate supplier capability of an A/R>1.25, it will be a challenge in the future as long as data I/O continues to increase along with bandwidth.

For comparison, there are embedded PoP structures such as that shown in **Figure 1**, and non-embedded structures such as the

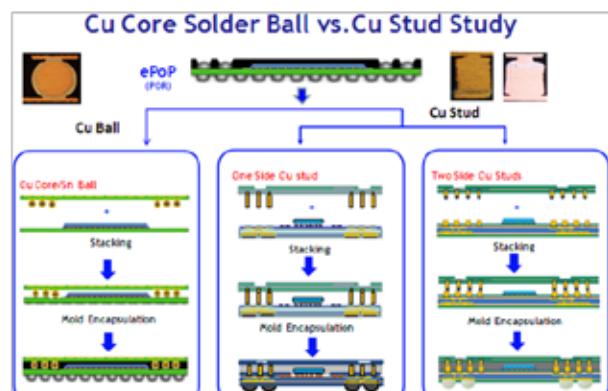


Figure 1: Embedded HBW PoP structure.

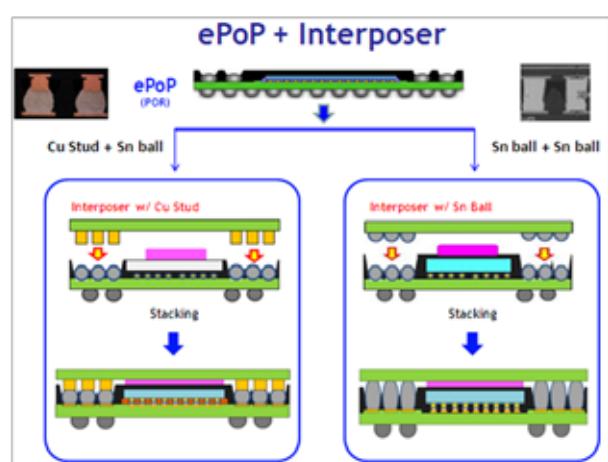


Figure 2: Non-embedded HBW PoP structure.

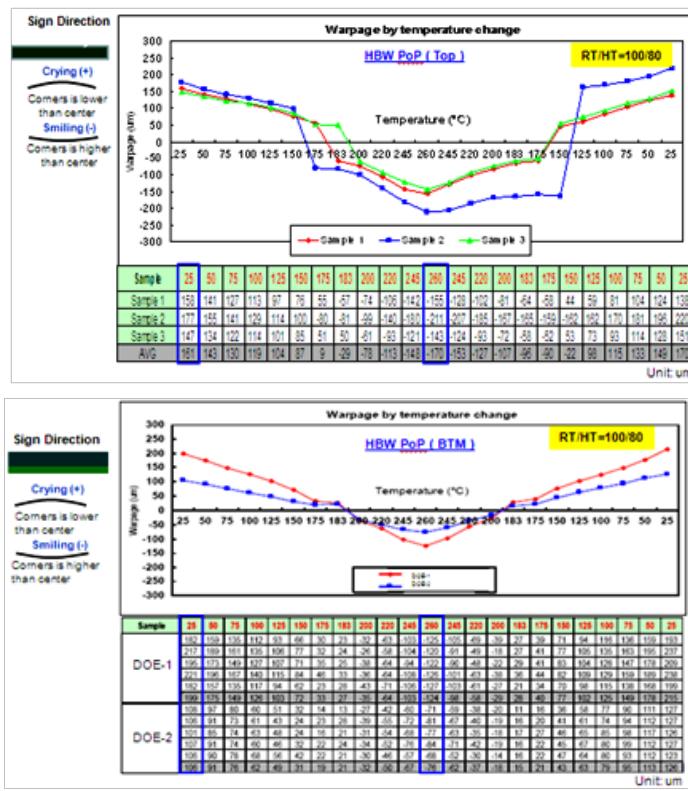


Figure 3: Top interposer and bottom ePoP warpage performance for an HBW PoP non-embedded structure.

ones shown in **Figure 2**. The top interposer will have either a stud or a solder ball to act as the contact.

Differences between the processes used to generate the embedded and non-embedded structures include the molding process. For the embedded package, one must first run the SMT process to connect the top interposer to the bottom substrate and then do the molding on the strip form. On the non-embedded package, however, one must do the ePoP first, and then the SMT process unit by unit.

One challenge with the non-embedded process is ePoP warpage because its structure requires a thinner bottom ePoP thickness than the traditional ePoP structure. The top interposer relies on a 2-layer substrate with a thickness of around 0.12mm and also needs to consider the gap between the top interposer and the ePoP structure. Thus, bottom ePoP warpage will be the major consideration. Moreover, joint stress also needs to be considered with respect to package reliability and board-level test.

On the other hand, there is less concern with bottom ePoP warpage in the

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embedded structure because the molding is processed after SMT processing of the top interposer and bottom package. However, another challenge will be the SMT accuracy and the gap between the die and the top of the interposer.

The top interposer and bottom substrate warpage performance for the non-embedded structure (**Figure 3**) shows that the top interposer and bottom ePoP warpage were out of criteria (RT/HT 100 µm/80 µm). Such warpage performance needs to be improved by using an optimal jig to control the reflow

joint during SMT processing. The major reason for such poor warpage is because of thickness restriction. So, as mentioned previously, the next challenge will be stress during reliability testing. The unit warpage performance, however, can meet the criteria RT/HT 100 µm/80 µm on both the embedded and the non-embedded structure (**Figure 4**).

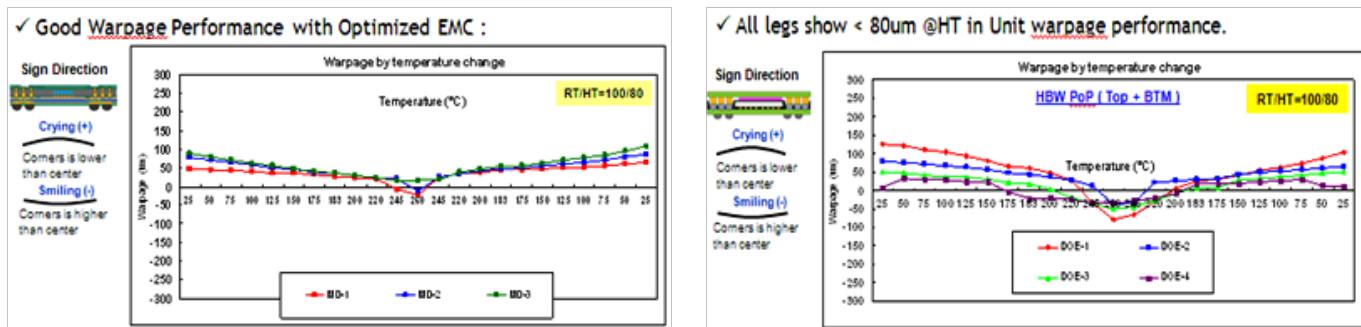
### Summary

The requirements for ever higher resolution images and increased bandwidth in electronic devices/applications will

mean that the number of I/O connections will increase. Our studies have shown that an alternative PoP structure with a routable substrate interposer can meet these requirements.

### Biographies

Jui-Cheng (Steven) Lin received a masters degree in Electrical Engineering from the U. of Southern California and is a technical manager of the Engineering Center at Siliconware Precision Industries Co., Ltd. (SPIL); email Stevenlin4@SPIL.com.tw



**Figure 4:** Unit warpage performance for an HBW PoP embedded (left) and non-embedded structure (right).

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# Camera-assist automation for bond testing of MEMS interconnect

By Alan King, Evstatin Krastev *[Nordson Dage]*

The term MEMS (microelectromechanical systems) appeared and started gaining popularity in the mid-80s. MEMS refers to a complete system on a single platform that consists of both mechanical and electrical/electronic components. This permits the system to incorporate both the sensors (e.g., pressure meters or accelerometers) and the control/reporting electronics on a single chip within the Si wafer. MEMS have enjoyed a tremendous growth in recent years because of the continuing trends for miniaturization and increased complexity that govern the manufacturing output in all fields including consumer products, industrial, medical, military, automotive, and so on. Currently, one can find these tiny devices within any contemporary cell phone or automobile diligently performing their tasks as high-quality microphones, micro accelerometers and gyroscopes, pressure sensors, RF modulators and microfluidic controllers.

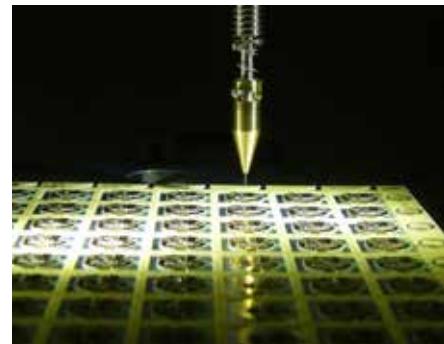
Naturally, the increased complexity and miniaturization poses new challenges for testing equipment and testing methodology in general, and bond testing technology in particular. The need for automation is critical to streamline the testing process and also reduce the influence of human errors. While simple “step and repeat” automation has been sufficient in the near past, currently microelectronic interconnect in general is experiencing a number of changes. Geometries are continuing to shrink and operator manual alignment of the test head to the bonds is becoming more and more difficult. Thus, focus is returning to camera-assisted automation that originates from the Dage BT25/2500 projects in the early 1990s.

In this paper, we present the technology behind the modern fully automated bond testing of MEMS devices using camera assist. The image capture camera that is integrated into the bond tester main

frame is used as the main teaching device, providing the accuracy and ease of programming needed. Various software features come in handy in streamlining the programming and keeping the process within the necessary precision parameters. We find this automation technology to be useful for a wide range of applications, including wafer-level bond and die shear, Cu pillar/flip-chip micro-bumps, ultra-fine pitch interconnect, lead frame wire pull and shear/pull applications of hybrid devices.

In recent years, we have seen a constant increase in the requests and need for automating the bond testing process. The reasons behind this can be grouped in several general categories. First, there is a widespread push in the industry for increased productivity. Replacing the manually performed operations by an expensive operator with an intelligent fully automatic machine performing the same tasks is faster and cheaper. For another group of users, speed and price are secondary to precision. For these end users, performing the test with the highest possible accuracy is of crucial importance. This involves precise alignment and positioning of the test tool before the test, which needs to be exactly reproduced over and over again. Manual tool alignment and test execution is always prone to inaccuracies due to inconsistencies in individual operator performance, as well as the variation introduced by multiple operators using the equipment.

The first principle for automating the bond testing process is to make sure that all the parts that need to be tested are mechanically placed and secured at the same physical location at all times. This is accomplished using precise work holders that ensure placement accuracy. For MEMS devices as shown in **Figure 1**, the sample holder is of comparably simple design as the individual parts have fixed locations within the large printed circuit



**Figure 1:** MEMS devices set up for an automatic non-destructive wire pull test.

board (PCB) assembly. This is also valid for MEMS devices that need testing at the wafer level before being cut and packaged individually.

In the case of individual packages that have the MEMS device already installed within the plastic packaging, however, the requirements for the sample holder are significantly more demanding (**Figure 2**). The sample holder needs to be designed and built allowing for many different parameters, some of which are working against each other. The sample holder needs to accommodate as many devices as possible that need to be loaded as fast as possible and at the same time as accurately as possible.

In cases similar to the one in **Figure 2**, multiple sample holders are suggested so the parts can be loaded at the same time

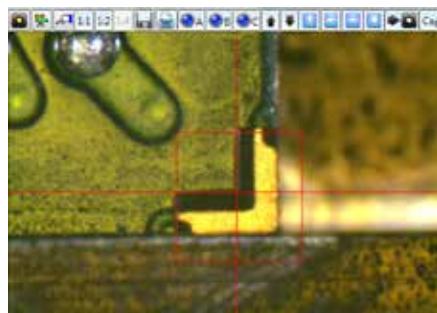


**Figure 2:** Sample holder designed for automatic bond testing of individual MEMS devices loaded into the system.

as the testing is executed. Appropriate fiducials for the camera-assist system need to be identified within the sample itself or machined within the sample holder. In addition to the sample holder accuracy, there are also very stringent requirements for speed and mechanical positioning to the X-Y stage. The stage needs to be as fast and accurate as possible and at the same time not prohibitively expensive in order to accommodate tight budgets typical for current economic conditions.

Once the best possible mechanical alignment and securing of the devices is assured, the rest of the auto programming and execution steps need to be done in an appropriate manner. While auto programming has been accomplished in the past by simply using the test tool as a teaching device, much better accuracy and ease of programming can be achieved by using integrated camera assist systems that are an essential part of every modern bond tester. As an added benefit, these camera systems can also be programmed to automatically take high-resolution images of the failure modes while the automatic test is carried out. There are routines within the software that account for the offset between the camera and the test tool, so all the teaching and fiducial recognition can be carried out by just using the camera system. In addition, in the case of wire pull applications, the software provides routines that handle possible hook eccentricity variations.

As shown in **Figure 3**, the camera system has locked at a feature of a ball grid array (BGA) type device that will be used as a fiducial. Usually a set of three fiducials is utilized that encloses the area of the testing. Advanced image recognition algorithms are employed by the bond tester software to compensate automatically for transitional and rotational misalignment. To achieve a

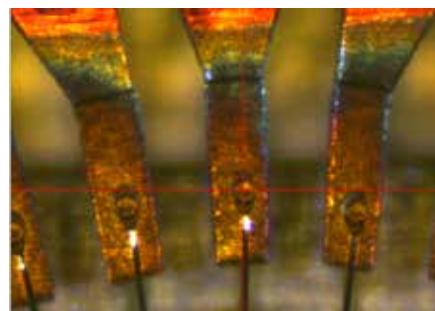


**Figure 3:** Fiducial recognition routine within the auto-teaching procedure. The fiducial is locked within the red square.

repeatable system operation, the fiducial mark needs to be easily recognizable by the optical system and be of unique nature within the camera's field of view. The capability of multiple fiducial levels assures that complex samples that exhibit die placement variations can also be programmed. Fiducials can also be machined within the sample holder for the cases of multiple discrete devices or if appropriate fiducials are not available in the case of PCB/wafer samples. It is very important to emphasize that, based on our experiments, the introduction of optical fiducials and image recognition algorithms brings the accuracy and the repeatability of automatic bond testing to a new, much higher level that cannot be achieved using only mechanical means.

After the fiducial alignment is programmed successfully, the next step is teaching the locations for the test. As mentioned before, these could be bond wires, BGA solder balls, Cu pillars, micro-bumps, or individual dies within a wafer. The main types of tests being automated include wire pull and various types of shear. For bond wire auto testing, there is the option to select the two ends of the wire and a testing point, or to select the two ends of the wire and specify the test position along the wire as a fraction or percentage of the wire length.

As shown in **Figure 4**, the operator is using the crosshair displayed in the camera window to teach the essential location for the wire pull test. Using the camera streamlines the programming process and results in very high accuracy that is not achievable by simply using the test tool as a teaching device.

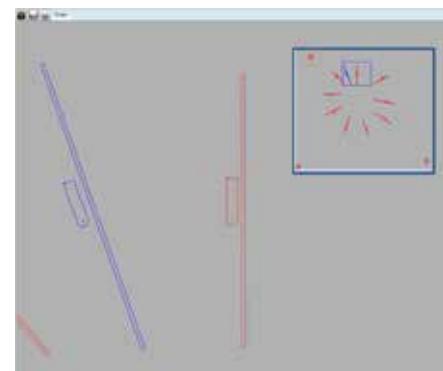


**Figure 4:** Teaching bond wires within the automation routine using camera-assist functionality.

In addition, as shown in **Figure 5**, the graphical user interface (GUI) incorporates areas that graphically display the test surface, giving the

opportunity to the operator to fine tune the program by using CAD tools and slightly modifying or even drawing test locations manually.

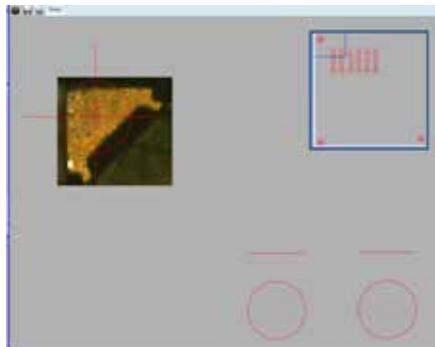
For the particular example in **Figure 5**, the inset shows a computer-aided design (CAD) drawing of the test area within the fiducials. The operator has just slightly modified the test position of the hook as marked in blue. The bond wire dimensions and hook size are input in the software, thus permitting worry-free programming. For the case of shear tests of bumps and BGA balls, the operator inputs the ball diameter and the offset corresponding to the desired shear tool placement.



**Figure 5:** A CAD drawing that was automatically generated through the programming process. Interactive tools permit slight modifications of tool position. Copy/paste functionality is very useful for repeating patterns.

Copy/paste functionality is also available to the programmer. This programming capability is very useful for BGA balls/bumps/multiple die shear applications as well as wire pull applications of multiple discrete devices.

**Figure 6** shows an example of CAD output automatically generated by the software. The inset shows the whole test area within the three fiducial marks. The operator has programmed the first row and used the copy/paste functionality to populate the test positions for the next two rows. Ball diameter and tool offset have been input by the operator. The software automatically displays the CAD drawing, including fiducial image, and test locations for BGA balls and tool positioning. The area in the blue square within the inset corresponds to the enlarged view that includes the optical image of one of the fiducials. The operator can move the little blue square



**Figure 6:** CAD drawing of the testing surface within a BGA device. The inset shows the whole area within the fiducials. The large image is an enlarged view of the blue square within the inset showing BGA ball positions, tool positions and an optical image of one of the fiducials.

and display different areas of the testing surface.

### Summary

The addition of high-resolution camera systems has resulted in a streamlining of the modern bond tester automation capabilities for a wide variety of applications exhibiting much improved testing repeatability. This includes high-accuracy/high-speed automatic testing of MEMS devices as discussed in the above paper. The camera-assist automation capability is also vital in many other bond testing applications including wafer-level bond and die shear, Cu pillar/flip-chip micro-bumps, ultra-fine pitch interconnect, wire pull, and shear/pull of hybrid devices.

### Acknowledgements

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# 3D stacked ICs: from vision to volume

By Gretchen Patti [\[Tezzaron\]](#)

**B**ack in 1999, 3D stacked integrated circuits were just an exciting futuristic idea. The vision was to stack finished wafers, remove the extra silicon from the back side of each wafer, pierce the stack with copper vias, and then dice it into 3D integrated devices. On paper, the benefits looked fantastic: a 3D device would have a smaller footprint and much shorter wires. The shorter wires would provide better performance; they would also exhibit less capacitance thereby allowing the device to run at lower power. The device's "circle of control" would become a sphere, encompassing many more circuit elements. Input and output signals would not be limited to the sides of the chip, but could emerge from its face, creating a fabulously wide I/O bus. Various layers of the device could be built in different processes, different geometries, or even different materials. It looked like a revolution whose time had come, if only the technology could be put in place. That was when Tezzaron decided to enter the field.

## Wafer stacking

Our first attempts at wafer stacking used aluminum. We quickly discovered that aluminum was far too reactive. The surfaces oxidized before we could even get the wafers into the bonder. The process team turned its attention to copper bonding – at the time, a highly experimental practice. It proved to form a tenacious, uniform bond. The same copper layer also served as interconnect and as a very efficient heat spreader.

At about the same time, Ziptronix was developing its DBI® covalent oxide bonding. This process creates a useful bond at room temperature. The bond becomes permanent when annealed. Before annealing, the bond can be checked for alignment and adjusted as necessary. This "do-over" ability is a tremendous asset and the annealing temps, as low as 150°C, are kinder than copper's 380°C.

When production-ready, the two processes proved nicely complementary. Tezzaron licensed Ziptronix's DBI and now offers both bond types. The copper process is still the cheapest and best for many applications, especially high-volume runs with homogeneous wafers. DBI is better for small runs and for heterogeneous stacks where thermal properties don't match well – for example, bonding CMOS wafers to indium phosphide.

Both processes start with finished wafers. The wafers' front sides are coated with an insulating glass layer and then patterned with copper in a single- or dual-damascene process. Then the two processes diverge as described below:

**The copper thermal diffusion process.** The copper serves as both bonding material and electrical interconnect. First, the surrounding glass is recessed slightly so that the copper spots, or "bondpoints," protrude above the surrounding oxide. Two wafers are aligned with their front sides facing one another and then treated with a thermal diffusion process at 380°C to produce a metal-to-metal bond.

**The DBI® covalent oxide process.** The oxide serves as the bonding material and the copper serves as electrical interconnect. First, chemical-mechanical polishing (CMP) forms a highly planarized surface. The oxide is then activated. Two wafers are aligned with their front sides facing one another and brought into contact at room temperature. The oxide forms a spontaneous bond. The bond may be examined for alignment; if necessary, the wafers are separated and re-bonded. The wafer pair is then annealed at low temperature to form a permanent bond.

Both processes produce a bond that

is hermetically sealed; it is actually stronger than the silicon itself and cannot be separated without destroying the wafers. This adds a level of security to the circuitry and effectively thwarts reverse engineering.

After bonding, the structural base (back side) of one wafer is thinned to less than 10µm by using a combination of conventional wafer grinding, spin-etching, and CMP. This thinning reveals the tips of the vertical interconnect built into each wafer – in fact, the interconnect serves as a thinning control. [Figure 1](#) illustrates this process.

For multi-layer stacks, the back side of the thinned wafer is processed and bonded to the front side of a third wafer, with the exposed interconnect tips acting as alignment markers. Thinning, processing, and bonding may be repeated as desired. When the wafer stacking process is complete, one side of the stack is thinned and padded out for I/O; the other side is backlapped to remove excess silicon.

Our wafer stacking process completely bypasses the much-discussed problem of thin wafer handling. A permanent bond is formed before the top wafer is thinned, so it is never handled separately as a thin wafer. The bottom wafer maintains its full thickness throughout the process, providing support for the upper thinned layer(s). This allows the wafers to be ground extremely thin; each wafer adds only 13µm to the stack. This means that a 16-layer 3D-IC could fit easily into standard packaging.

There are ways to make 3D-ICs without stacking – monolithic manufacturing, for example, and printed interlayer transistors – but it's still early days for these methods and we have not yet seen applications that require them.



**Figure 1:** Two wafers being stacked and thinned (using either process).

## Vertical interconnect

Our original copper vias worked, but we discovered an issue with thermal effects because copper's coefficient of thermal expansion is so much greater than that of silicon. With temperature cycling, the copper vias flexed enough to pop loose from their surface connections. There are ways to mitigate this "copper pumping" problem: treat the copper to produce a larger grain size, maintain an adequate "keep-out" zone around the vias, see that the vias in multi-layer applications do not align vertically, etc. Another solution is to use tungsten instead of copper to fill the vias. Tungsten is a reliable and well-known material. It is already a common element in semiconductor process lines; it conducts well, it doesn't migrate, and it matches the thermal qualities of silicon. The one great difficulty with tungsten is that it cannot effectively fill holes wider than about 2 $\mu\text{m}$ , nor aspect ratios greater than 10:1.

Our solution is to offer both copper and tungsten. Where large, deep vias are necessary we use copper, observing a set of careful design rules and process steps. More often, though, we implement a forest of fine, short tungsten "wires" that are more like contacts than like vias. We call them SuperContacts™. Rather than penetrating an entire wafer, a SuperContact reaches only from the back of the silicon to the bottom layer of wiring. Because we thin the wafers so aggressively, the tungsten plugs need be only about 6 $\mu\text{m}$  deep. **Figure 2** shows a cross section of a finished wafer, before thinning, with five layers of metal and a tungsten SuperContact.

Copper through-silicon vias (TSVs) are used mainly for 2.5D applications, where the TSV must pierce the interposer itself, and for post-production insertion of TSVs into finished dies from other fabs. For our own 3D designs, we use SuperContacts exclusively. **Table 1** compares the properties of these two types of vertical interconnect.

## Stacking wafers, dies, and interposers

Semiconductor 3D research continues to produce interesting strategies for implementation. Several different stacking methods have already proven to be practical and manufacturable:

**Wafer-to-wafer.** Wafer-to-wafer (W2W) stacking was our first strategy

and, for many applications, it's still the best. However, it does place demands on the design of the stacked devices: the layers may vary in process, substrate, and geometry, but all layers of the design must have exactly the same length and width. Also, there is the question of yield. There is no way to choose which dies to stack when an entire wafer is stacked. Multi-layer designs must implement some kind of redundancy and repair scheme to keep the yield acceptably high. Assuming proper design constraints and robust repair mechanisms, W2W is the ideal 3D strategy.

Our memory devices are built in W2W. With numerous layers of identical cells and a profusion of SuperContacts, we can implement repair and redundancy at a very fine-grained level. Similar schemes could be used for FPGAs, sensors, or other devices that contain a plethora of repeating circuitry.

**Die-on-wafer.** For other applications, die-on-wafer stacking is a better solution. Die-on-wafer is more time-consuming and labor intensive than wafer-on-wafer, but it offers distinct advantages. Dies of different sizes can be vertically integrated and dies can be tested before

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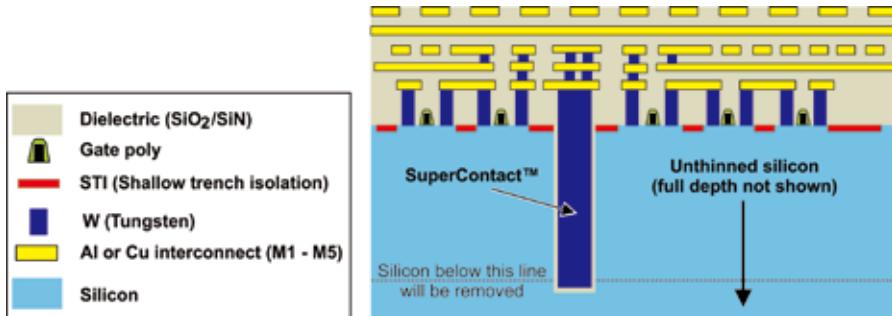


Figure 2: Diagram of SuperContact™ implementation (before thinning).

	Material	Diameter	Depth	Pitch	Usage
Copper TSV	copper	10µm	up to 100µm	30µm	Insertion into finished dies or interposers
SuperContact™	tungsten	0.6 - 1.2µm	2 - 8µm	1.2 - 2.4µm	Built into designs for die or wafer stacking

Table 1: Interconnect properties.

stacking in order to implement a known-good-die (KGD) strategy. The bottom dies stay in wafer form until the process is completed. As in W2W stacking, this bottom layer provides support and stability for the stack as it is formed. Multiple dies may be added to a stack, thinning after each addition, much as in a

wafer stack. We developed a temporary stencil structure to aid in die-on-wafer alignment as shown in Figure 3. The stencil also protects the edges of the dies during thinning.

**Stacks of stacks.** The two types of stacking may be combined in interesting ways. For example, in the die-on-wafer

scenario described above, the bottom wafer might actually be a stack of wafers. The singulated die might also be a 3D stack diced from a stack of wafers. Such a “stack of stacks” device is illustrated in Figure 4.

**Interposers.** The latest twist on 3D stacking is the use of interposers. Chips are attached to an interposer that acts as a substrate and interconnect medium, rather like a next-generation circuit card. Unlike a circuit card, the interposer accepts bare dies and the whole assembly is enclosed in a package. The architecture is quite versatile. Dies can be flip-chipped onto the interposer or bonded like a 3D part; dies can be KGD or even off-the-shelf parts. An interposer needs significantly less electrostatic discharge (ESD) protection than a circuit card and no signal termination. The wires between chips are much shorter than on a circuit card, but not as short as in a 3D part. In all, an interposer assembly delivers better performance and lower power requirements than traditional 2D – some of the same advantages as 3D, but to a lesser extent. For this reason, interposer-based devices are often referred to as “2.5D.” There is a power and performance trade-off compared to 3D, but the reduced time-to-market is very attractive. Interposers come in three materials: glass, organic, and silicon. At present, we work exclusively with silicon interposers, which support a finer pitch than organic and match the coefficient of expansion of the mounted dies. Current silicon interposers are passive components, supplying only structure and interconnect. In the future, we expect to see active silicon interposers that contain power supplies, active interface circuitry, silicon photonics, etc.

## No one best solution

To sum up, there are many different ways to implement stacking. There is no one “best” solution; flexibility is key. The optimal stacking solution is the one that best suits the specific application. Copper thermal diffusion or covalent oxide? Copper vias or tungsten contacts? Wafer

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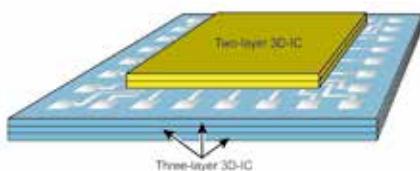
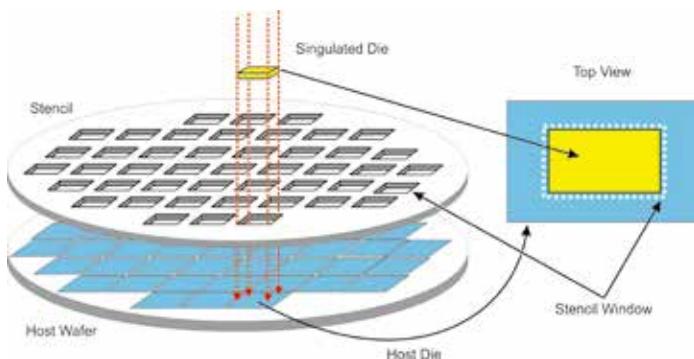


Figure 4: 3D stack of stacks.



**Figure 3:** Die-on-wafer placed in stencil before thinning.

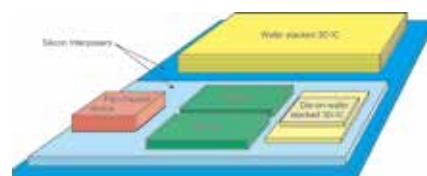
stacking, die-on-wafer, or interposers? A wide spectrum of solutions is essential, providing an intriguing range of permutations. A hypothetical example is shown in **Figure 5**.

### Summary

After fifteen years of work, we are still discovering ways to extend and refine the technology. When we designed our first working prototype 3D-ICs in 2004 it was an arduous process. Design tools were not 3D-aware, so the vertical dimension had to be verified by hand. Countless man-hours were spent writing scripts, extensions, rule decks, etc. Finally, functional devices emerged – and they did indeed exhibit power and speed advantages as predicted.

3D-ICs are now fully manufacturable. The tools have improved and matured – especially verification tools. The process flow is firmly in place. Building the separate layers with different optimization has proven immensely beneficial. We can successfully mix wafer types and/or process nodes. Better tools keep emerging and manufacturing is ramping up.

Although we haven't seen a revolution yet, the semiconductor industry has made long strides toward high-volume 3D. The biggest applications right now are memory, FPGAs, sensors, and multi-core processors. As clever 3D designs proliferate, more new ideas are sparked.



**Figure 5:** Diagram of a mixed-stacking interposer solution.

The exciting thing is that the true “killer app” probably hasn’t even been invented yet! Someday soon a brainy inventor will connect a set of dots that was never connected before, and the revolution will happen. We can’t wait.

### Biography

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# Thermal management using phase change materials

By Hong Min Huang, Chris Lee, Hyo Xi, Yaqun Liu, Liang Zeng, Linda Shen [Honeywell Electronic Materials]

**W**hile a variety of thermal management solutions are available in the marketplace, phase change material (PCM) technology is growing in popularity because of its ability to take thermal management to the next level in terms of device performance, long-term reliability and processing efficiency.

The use of PCM technology is critical because heat generation is a growing concern as more power and speed is packed into smaller devices across applications – from mobile smart phones and tablets to CPUs, gaming consoles, video graphics array (VGA) display cards, telecom products and servers. This trend is requiring integrated circuits (ICs) to perform at significantly higher power densities under extremely tight real estate and package constraints.

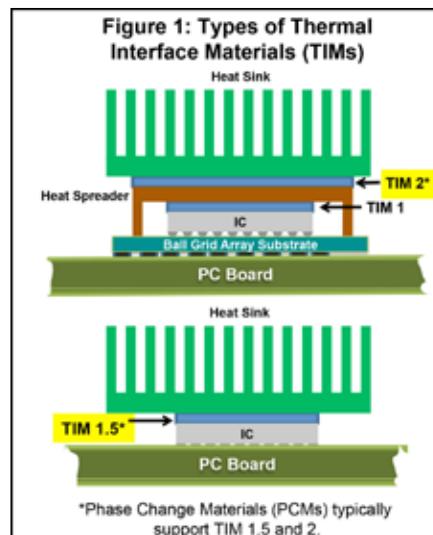
As power increases, so does heat, which is why thermal management is becoming an increasingly vital step in the design process. Because building larger heat sinks isn't possible given shrinking architectures, manufacturers are applying more resources toward the study and selection of thermal interface materials (TIMs) that manage excess heat, reduce operating temperatures (and thereby improve speed) and ensure long-term reliability.

Various classes of TIMs provide their own set of benefits and trade-offs. Greases, for example, may offer excellent thermal performance, but ongoing reliability is a challenge in high heat situations because of degradation issues. Advances in PCM technology are overcoming such trade-offs, making it an attractive and proven thermal management solution in challenging applications.

## TIM types

In a typical high-powered IC application, the thermal material applied at the interfaces between chip, heat spreader and heat sink is critical to long-

term device performance. The TIM needs to reliably fill air gaps and surface irregularities, increasing heat transfer to the heat sink so the device can run cooler. As shown in **Figure 1**, types of TIMs



**Figure 1:** Types of thermal interface materials (TIMs).

include: 1) TIM-1 – which is applied between the IC and heat spreader; 2) TIM-2 – which is applied between the heat spreader and heat sink; and 3) TIM 1.5 – which is becoming more common. In this design, there is no heat spreader and the TIM 1.5 is applied between the IC and heat sink.

## TIM properties

Key properties critical to evaluating the performance of TIMs include:

**Low thermal impedance.** The true test of performance is thermal impedance (TI), which measures resistance in units of  $^{\circ}\text{C}\cdot\text{cm}^2/\text{W}$ . This measure shows how a material performs in the actual application, accounting not only for its bulk thermal conductivity, but also for its performance at the interfaces where thermal contact resistance occurs (e.g., heat spreader and heat sink). While high bulk conductivity is important, it is not

exclusive. While materials with a lower TI should be the focus as they provide the best heat transfer, testing in-system will determine TIM performance. TI is affected by the properties described in the following formula:

$$\text{TI}_T = \text{BLT}/K + R_C$$

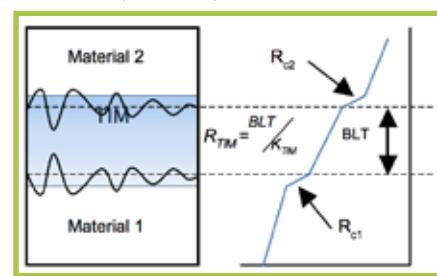
where:

$\text{TI}_T$  = Total thermal impedance

BLT = Bond line thickness of the TIM

K = Bulk thermal conductivity of the TIM

$R_C$  = Thermal contact resistance at the interfaces (see inset)



inset

**High bulk thermal conductivity.** A higher bulk thermal conductivity indicates a better heat transfer rate through the material itself. Measured in  $\text{W}/\text{m}\cdot\text{K}$ , it is an intrinsic property that indicates the "potential" for heat transfer through the bond line of the TIM. While commonly listed in data sheets, it alone does not truly reflect the TIM's actual performance relative to surface interfaces and contact resistance.

**High surface wetting and low thermal contact resistance.** Achieving full surface wetting and contact at the interface is critical to minimizing contact resistance and maximizing heat transfer. The flexibility to penetrate varying degrees of surface roughness is critical. Lower viscosity is associated with higher wetting properties and can be measured by contact angle. A lower contact angle is an indication of excellent wetting.

**Low bond line thickness.** Bond lines well below 0.1mm are necessary

for today's high-powered applications. Achieving thin bond lines while maintaining a stable polymer matrix (even under clamping pressures) reduces the thermal resistance path, improves reliability, and meets the needs for confined spaces. TIMs with a lower viscosity have the higher flowability needed for thinner bond lines.

**High thermal stability (reliability) over time.** Thermal stability is an important indicator of the long-term performance of a material. It is measured by assessing the performance of a TIM after accelerated life tests (ALTs). Such tests include temperature cycling, high-temperature bake, and highly accelerated stress tests (HASTs). TIMs that can withstand this abuse have a reduced risk of failure and can help define product life and end-use warranties.

### Classes of TIMs

Several classes of TIMs are available in the marketplace, including thermal greases, PCMs, thermal adhesives and thermal gap pads. While this article focuses primarily on PCM performance, below is a high-level comparison of the benefits and limitations of each class:

**Thermal greases.** Typically silicone-based, greases are non-curing, conformable and reworkable. While they provide low thermal resistance, they can degrade, pump-out or dry out after repeated thermal (on/off) cycles, causing failure and potential contamination of adjacent components. They also can be messy and difficult to apply because of its paste form factor, requiring high-precision dispensing equipment. Furthermore, mechanical clamping is required.

**PCMs.** PCMs combine the advantages of a thermal gap pad along with the thermal performance of a grease. This material transforms from a solid state to a liquid or gel state as the temperature reaches its phase change or melt temperature. Like greases, PCMs provide low thermal resistance and are non-curing and conformable, but do not have bleeding, dry-out and other degradation issues. PCMs, which are typically available in a film form factor but also in a paste format, are easy to apply. They can be coated directly onto release liners and cut into pads at various thicknesses to better meet design and heat requirements. Mechanical clamping is required, and they are reworkable.

**Thermal adhesives.** These are one- or two-part cross-linkable materials based on epoxies or silicones. They provide low thermal resistance and are known for their structural support. While this can eliminate the need for mechanical clamps, cure time is required and they are not reworkable.

**Thermal gap pads.** Pre-cured thermal pads are typically thicker (>1mm) than other TIMs, and are designed to have good compression properties. When pressure is applied, the material conforms to the surface, filling gaps and irregularities. Gap

pads are reworkable, and may require a carrier film such as silicone or fiberglass to maintain their thickness. They usually cannot deliver the same level of thermal performance as the TIMs described above. Mechanical clamping or screws are typically required.

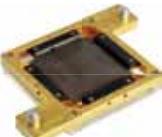
As noted, each class of TIM has limitations. While PCMs, for example, require mechanical clamping, this is significantly outweighed by their advantages in long-term performance and reliability.



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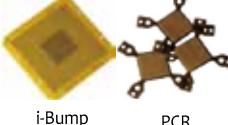
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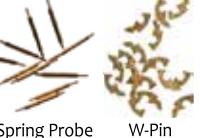
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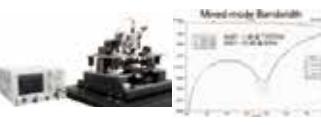
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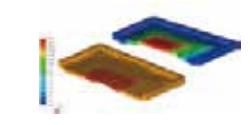
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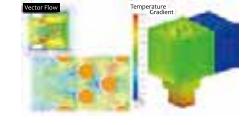
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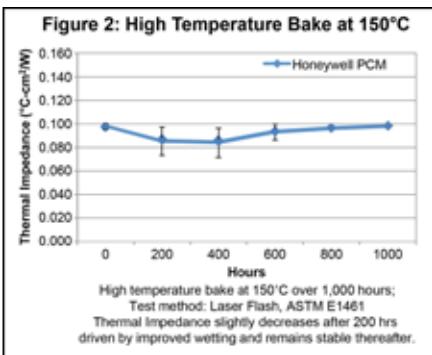
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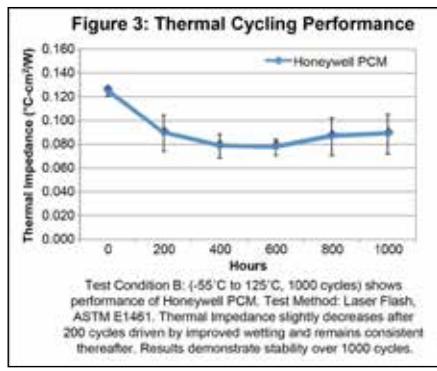
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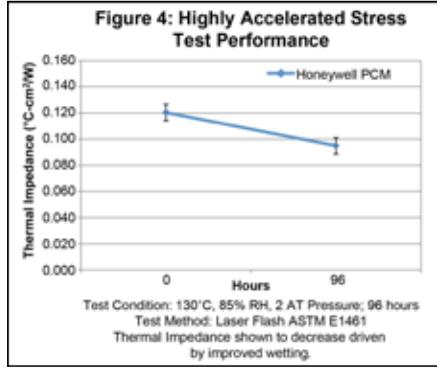




**Figure 2:** High-temperature bake performance of PCMs.



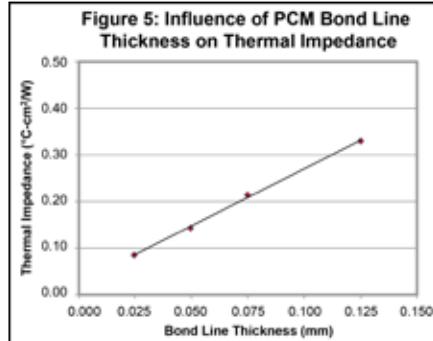
**Figure 3:** Thermal cycling performance of PCMs.



**Figure 4:** PCM performance in highly accelerated stress tests.

## PCM performance

As shown in **Figures 2-4**, PCMs typically deliver a low thermal impedance (TI) ( $<0.1^{\circ}\text{C}\cdot\text{cm}^2/\text{W}$ ) and high thermal stability over time, demonstrating excellent long-term wetting and reliability. This is true despite repeated thermal cycles, elevated temperatures and extended harsh test conditions. Specifically: 1) **Figure 2** shows the outstanding performance of a PCM in a high-temperature bake test over 1,000 hours; 2) **Figure 3** demonstrates the excellent stability of a PCM over 1,000 thermal cycles with no degradation; **Figure 4** reveals the ability of a PCM to perform under HASTs with no loss



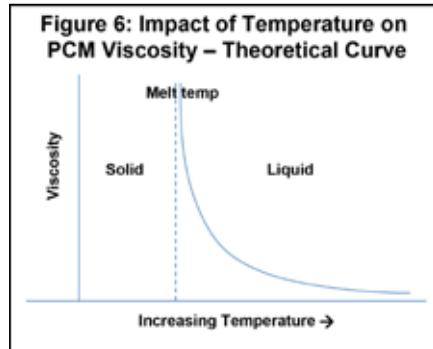
**Figure 5:** Influence of PCM bond line thickness on thermal impedance.

in performance. In addition, **Figure 5** shows the ability of a PCM to achieve a bond line thickness of  $<0.03\text{mm}$ , further reducing TI.

## Impact of polymer structure

PCMs meet all of the critical TIM properties stated above: low thermal impedance, excellent wetting, low contact resistance, low BLTs and high thermal stability. This is largely because of their unique polymer structure and phase-change capability.

Most PCMs contain wax-based polymers, transforming from solid state to a liquid or gel state as the temperature increases during device operation. The melting process, which is reversible, occurs when temperatures exceed the melt temperature – typically in the  $45^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  range. **Figure 6** shows the transition



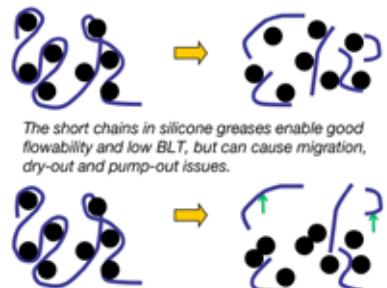
**Figure 6:** Impact of temperature on PCM viscosity.

from a solid to liquid state and the impact of temperature on viscosity. Increasing temperatures result in low viscosity, which not only delivers high wetting at the interfaces but also excellent flowability for ease of application.

Polymer structure and molecular chains play an important role in performance, as illustrated in **Figure 7**. PCMs are

## Figure 7: Molecular Structure of PCMs versus Greases

The long chains in PCMs enable stable and consistent filler dispersion and polymer matrix in all states, minimizing migration and other issues.



**Figure 7:** Molecular structure of PCMs vs. greases.

higher molecular weight polymers in the 5,000-7,000mw range, comprised of longer polymer chains than those found in greases. Long chains enable a stable and consistent filler dispersion and polymer matrix, improving thermal conductivity and minimizing migration. In addition, as the temperature decreases, the PCM solidifies, maintaining the polymer matrix integrity and thereby, long-term reliability.

In comparison, silicone greases are comprised of non-curable silicone with short-chains in the matrix. This ensures good flowability and low BLT, which is a key contributor to their thermal performance. However, as mentioned, the easy migration of silicone may cause bleeding, pump-out and dry-out issues over time.

As with most TIMs, PCMs include a filler material responsible for conducting heat. Filler loading (type and particle size) affect viscosity and flowability, and are chosen to provide the best balance. Common PCM fillers include metal particles, such as silver and aluminum, and ceramic powders, such as alumina and zinc oxide.

An additional important property inherent to PCMs is latent heat of fusion – the storage and release of energy as they change states. This enables thermal absorption and provides a valuable temperature buffer, regulating the device temperature particularly during sudden bursts of power and temperature spikes.

## PCM growth and versatility

PCM growth in electronics is largely driven by the material's ability to meet

demand for higher thermal performance, long-term reliability and cost-effectiveness, including productivity improvements. For example, PCMs: 1) Can be dropped into the current production environment without new equipment investments; 2) Are easy to apply, improving yields while reducing rejects and waste; 3) Can help reduce product failures and returns; and 4) Are easy to rework, reducing assembly failure.

In addition, PCMs have the versatility to support the different priorities of multiple applications. Examples include: servers, telecom equipment, notebooks, tablets, smart phones, video graphics arrays (VGAs), high-brightness light emitting diodes (HBLEDs), as well as compact video recording devices.

## Summary

Thermal management is a growing concern as more power and speed are packed into smaller devices across applications. As heat increases, so does the need to dissipate it. PCMs are gaining widespread acceptance as a TIM that can take the heat. They can deliver similar, if not better, thermal performance than traditional TIMs but with greater long-term reliability, improved application ease, and minimal risk of migration and pump-out. These and other benefits can also help manufacturers improve productivity – a welcome bonus.

PCMs are expected to play a pivotal role in the future of electronics and are already proving their value in a variety of demanding applications. Manufacturers will see continued innovations as these materials not only respond to, but also enable, advances in the electronics industry.

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# Consideration of high-vacuum WLP for a MEMS optical sensor

By Katsunori Mae [GLOVA JAPAN R&D]

Optical sensors that detect infrared and/or ultraviolet rays have been adopted for a variety of applications, for which the sensing device is shrunk through the use of microelectromechanical systems (MEMS) technology. Larger metal can packages (Figure 1), however, are still mainly used for the packaging of optical sensors.

Optical sensors comprise a sensing device and a conditioning IC in tandem with optical components, such as filters, to accept only the desired wavelengths, along with a condenser and an aperture—all placed with high-dimensional accuracy within a highly air-tight or high-vacuum sealed environment. Such a structure makes downsizing difficult. Even some wafers incorporating both a sensor and a conditioning IC fail to transition to wafer-level packaging (WLP). In particular, problems are common in high-vacuum WLP, which is highly influenced by the materials and processes adopted. This makes the transition to high-vacuum WLP for the purpose of reduction in cost and size prone to failure. As there are many issues that cannot be resolved by transitioning from a conventional package for cost-cutting purposes, it is important to evaluate the design for each die.

Here, we will consider the points to be evaluated for WLP, taking as an example an infrared sensor. An infrared ray is a type of electromagnetic wave. The wavelength of visible light (light that a person can see) ranges from  $0.36\mu\text{m}$  to  $0.83\mu\text{m}$  (Figure 2), while an infrared ray is a type of light with a wavelength longer than  $0.83\mu\text{m}$ .

## Infrared sensor considerations

Infrared rays increase the temperature of certain objects through absorption when the rays make contact. Of the rays not absorbed, some reflect and some pass through. Meanwhile, the object absorbs and emits infrared rays at the same time.

Infrared rays are classified as near-infrared rays ( $0.83\text{--}3\mu\text{m}$ ), middle-infrared ( $3\text{--}6\mu\text{m}$ ) and far-infrared ( $6\text{--}1,000\mu\text{m}$ ).



Figure 1: T08 can package.

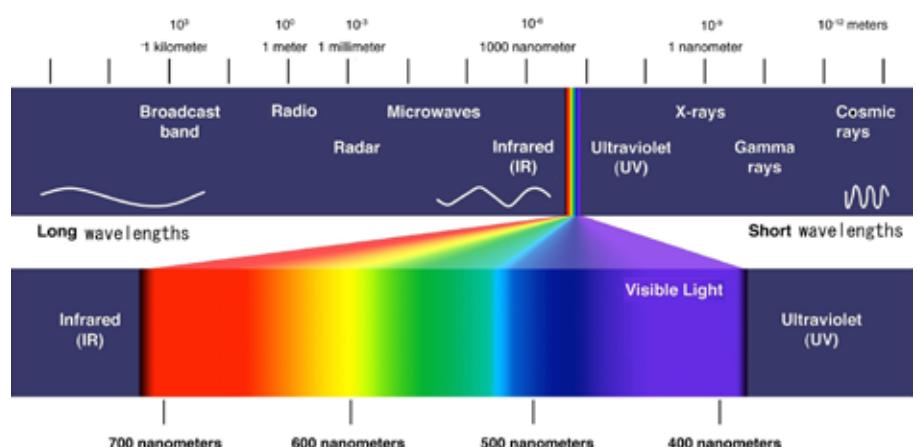


Figure 2: Visible spectrum wavelengths.

The range of a wavelength, referred to as the “atmospheric window” (Figure 3), is used for sensing, in which the transmittance of all gas molecules in the air is high. Among the many methods used for infrared sensing, we take the common thermo pile method as an example. Thermo piles employ the Seebeck effect—thermoelectric force generated in proportion to the temperature differential between two metal joints. In a MEMS sensor, two

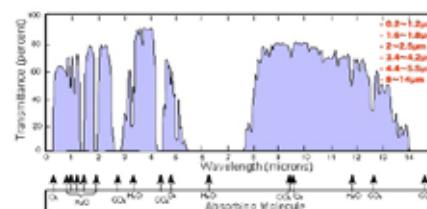
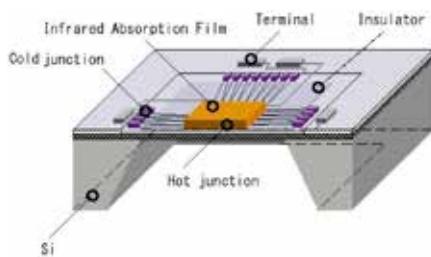


Figure 3: Atmospheric window.

thermocouples made from p-type and n-type polysilicon are connected in series, and a metal joint (hot junction) on the thin film and the other joint (cold junction) on the silicon frame are formed (Figure 4). The hot junction, accepting infrared light, contains a membrane film that absorbs the infrared rays produced from the metallic thin film or nitride film.

As many MEMS infrared sensors are not only uncooled but also contain a small device, only minute inputs are available. The necessity of high sensitivity for higher detection precision requires large temperature changes in the device in the MEMS sensor. Assuming temperature increase  $\Delta T$  at the time of the generation of thermal power  $W$ , with temperature of the MEMS sensor device  $T$ , the thermal



**Figure 4:** Infrared sensor structure pattern diagram.

equation is expressed by the following formula [1]:

$$C(d\Delta T/dt) + G\Delta T = W$$

where  $C$  = Heat capacity of the heat-generating part, and  $G$  = Heat conductance of the heat emitted from the heat-generating part.

Replacing  $W$  with  $W_0 \exp(j\omega t)$ , one obtains:

$$\Delta T = 2W_0/G(1+\tau^2\omega^2)^{1/2}$$

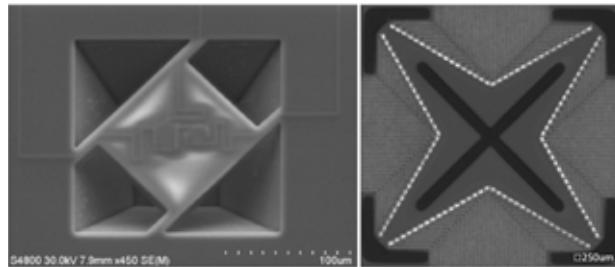
where the thermal time constant  $\tau = C/G$ .

$W$  denotes the absorbed infrared rays emitted from the subject. Increasing  $\Delta T$  against  $W$  and reducing thermal time constant  $\tau$  for faster responses is important for the performance of the infrared sensor. To minimize  $\tau$ , all you need to do is decrease heat capacity,  $C$  of the heat-generating part, and increase the heat conductance,  $G$ .

For the MEMS sensor, the size of the device needs to be downsized to decrease heat capacity  $C$ , while the infrared sensor for which the acceptance surface cannot be downsized needs to implement a floating thin film. In addition, the infrared sensor package needs to be associated with a high-vacuum seal to prevent the heat generated from the thermo pile from radiating out to the air (**Figure 5**).

### Vacuum considerations

A “vacuum” is a generic name given for a state where the density of substances (gas) is lower than that of open air. Gas molecules exist in a vacuum (**Table 1**). As the density of a gas molecule is proportional to pressure, the degree of vacuum is expressed by the term “pressure.” While an absolute vacuum is the state where there are no molecules existing in a space, the number of gas molecules in a space of  $1\text{cm}^3$  under a pressure of  $100\text{kPa}$  is  $2.69 \times 10^{19}$  at a temperature of  $0^\circ\text{C}$ . An artificially produced vacuum is  $10^{-11}\text{Pa}$



**Figure 5:** MEMS thermo pile hot junction.

at best. Even under this pressure, there are thousands of gas molecules in a space of  $1\text{cm}^3$ . It is extremely difficult to produce an even lower pressure, mainly because of the gas emitted from the substances.

Many gas molecules can be absorbed on the

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Title	Range
Low-vacuum	more than $10^2\text{Pa}$
Medium-vacuum	$10^2\text{Pa} \sim 10^{-1}\text{Pa}$
High-vacuum	$10^{-1}\text{Pa} \sim 10^{-5}\text{Pa}$
Ultra high-vacuum	less than $10^{-5}\text{Pa}$
Extreme high-vacuum	less than $10^{-9}\text{Pa}$

Table 1: Vacuum range.

surface of a solid including metal, and these are emitted over time under high vacuum, contaminating the vacuum. In order to minimize such gas emission, the structures are not only cleaned in the process, but also undergo ashing, and a bake out process, which is a degassing process at a high temperature of hundreds of degrees Celsius.

While the infrared sensor requires high vacuum, the minute emission of gas has significant impact in the small cavity of a WLP, greatly degrading the quality of a high-vacuum package. The issue for a MEMS sensor, necessitating a high degree of vacuum while containing a variety of materials, is how to reduce gas emission.

A high-vacuum WLP can consist of either a two-layer system constructed from a sensor wafer utilizing feedthroughs to form terminals for implementation and

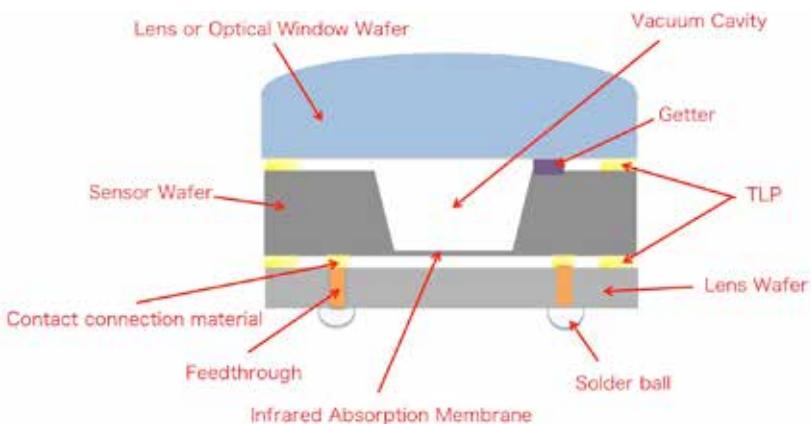


Figure 6: WLP cross section view.

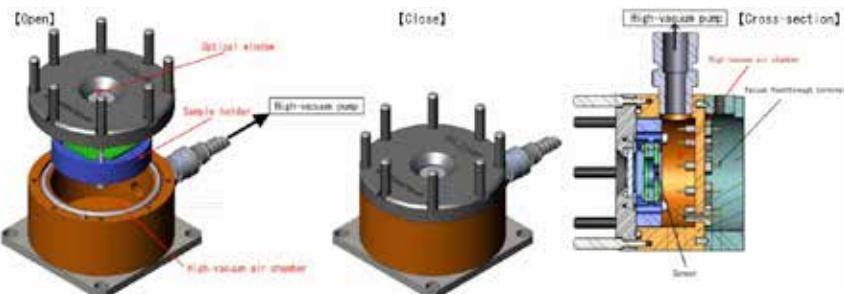


Figure 7: High-vacuum socket.

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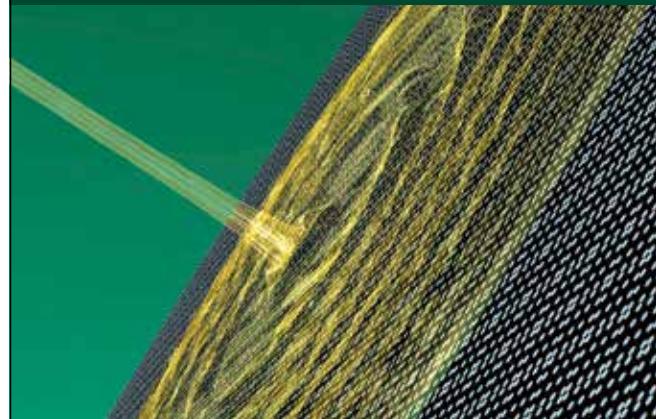
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**Table 2:** Comparison of different wafer bonding techniques.

an optical window wafer, or a three-layer system constructed of a sensor wafer, an optical window wafer, and a feedthrough wafer [2].

Methods for wafer bonding include anode bonding, glass frit bonding, transient liquid phase solder bonding (TLP), side braze (SB) bonding, and Si-Si bonding (**Table 2**). The layer structure and the bonding method are chosen in consideration of the required degree of vacuum, heat resistance, gas emission prevention at high temperatures, and cost [3]. A structure involving three layers with TLP (Au-Sn) bonding is used as an example (**Figure 6**) [3].

An optical window wafer is made of Si with a high transmittance of infrared rays and an anti-reflective film is formed on the wafer. A metal undercoating film for TLP solder is required on the bonding surface with the sensor wafer. The electric bonding between sensor terminals and the feedthrough wafer terminals are made of Au and also require a metal undercoating film. Organic materials, causing the degradation of a vacuum, are excluded as much as possible. The remaining oxygen, carbon monoxide, water vapor, carbon dioxide, nitrogen, and hydrogen are eliminated through a bake out process and by getters to retard degradation.

## Manufacturing considerations

The manufacturing of semiconductors and MEMS devices entails the use of various materials. Gas molecules absorbed by these materials reduce the degree of vacuum when they are emitted within a package. For example, getters are unable to capture fluoride that can adhere to structures during the process of deep etching used in the formation of MEMS structures and residual noble gases, such as argon, in the sputtering process of metal undercoating for TLP bonding. With a small cavity, a large sensor surface, and wide bonding surfaces for higher joint strength, it is sometimes impossible to ignore these emitted gases. Additionally, there is the risk of gas emission, sensor drift, or the destruction

of the conditioning circuit upon exposure to the getter activation temperature, bonding temperature, or the high temperature of TLP.

Achieving these characteristics through prototyping requires a significant number of tasks. In designing a sensor, it is necessary to determine the materials and processes in consideration of the WLP. When using a high-vacuum package, the package takes priority regarding the consideration of said materials and processes. In addition, it is difficult to achieve a package that maintains a high degree of vacuum for a long time; the package degrades at a certain leak rate. It is therefore impossible to completely eliminate the gases emitted from materials.

The getter material must be effective with respect to the dominant gas in the vacuum space, and it is necessary to consider the temperature and procedure of getter activation in the design of both the device and the process.

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to the WLP of the metal can packaged sensors during either prototyping or volume production, it is required that you evaluate the sensor elements and verify the degassing for the die. Conventional evaluation, using a large vacuum chamber, exhibits the problem of the inability to adjust optical axes and to evaluate the angle of view. GLOVA's high-vacuum socket (**Figure 7**) is an ultra-compact vacuum chamber. Its small oil-sealed vacuum pump is able to maintain a high vacuum of  $10^{-5}$ Pa. Also, the cover accommodates an optical window in accordance with the sensor and wavelength, and the sample holder fixes the sample with the optical axis and the back focus of the lens and sensor adjusted. Power and signals can be supplied through the vacuum feedthrough terminal to check for the sensitivity of a device.

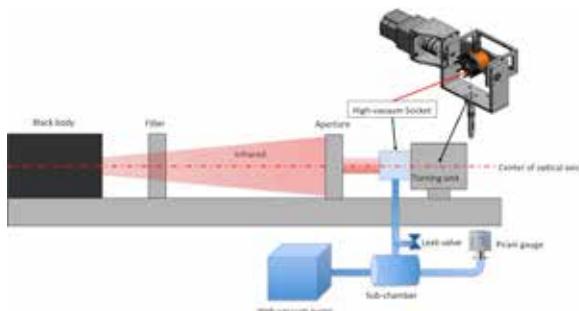
The sensor element is accommodated in the socket, with its power supply, signal lines, and lens properly embedded at the sample holder. The socket is then connected to the high-vacuum pump via the sub-chamber. Then, so as to enable rotating movement, a flexible hose for the vacuum is used to connect with the high-

vacuum pump. The sub-chamber enables reduction in electric noise from the pump and the avoidance of impact from vibration. It is also important to prepare power supplies for the measurement device separate from those for the high-vacuum pump and the rotating stage.

Vacuum range and sensitivity are evaluated using a high-vacuum socket. A gas in the socket is released such that the sensitivity of the infrared sensor is at a maximum. While in that maximum range, the sensitivity measurements take place as the vacuum is gradually degraded using a leak valve. When taking these sensitivity measurements, an oil diffusion pump, which has a wide range, is preferred over a high-vacuum pump such as a turbomolecular pump.

By using a calibrated black body as a light source, one can allow infrared light to pass through wavelength filters and an aperture. One can then adjust the optical axis from the source to the sensor's surface of incidence to increase the accuracy of the sensitivity evaluation. By using a calibrated black body as a light source, one can allow infrared light to pass through wavelength filters and an aperture. One can then adjust the optical axis from the source to the sensor's surface of incidence to increase the accuracy of the sensitivity evaluation.

The socket (**Figure 7**) enables you to measure the sensitivity of a single sensing device, evaluate the condensing magnification of a lens, and verify the sensitivity degradation by changing



**Figure 8:** Evaluation system configuration.

the degree of vacuum (**Figure 8**). Fixing the socket onto the rotating stage enables the evaluation of the angle of view.

The socket (**Figure 7**) enables you to determine the materials to be used and to optimize the process conditions flexibly through the evaluation of major elements without packaging. It is important to evaluate vacuum degradation and to predict the lifetime through such detailed evaluations. During the prototyping stage of the optical sensor, an evaluation environment is required for the easy and accurate evaluation of high vacuum.

## Summary

For the types of sensors requiring high-vacuum packaging, it is important to reduce the time required for prototyping as well as to identify and optimize various elements that are difficult to analyze in the event of failure after the process of packaging. A simplistic change of packaging to WLP without such steps can lead to a vicious cycle of failure analysis and prototyping, possibly forcing you to go back to where you started the development phase.

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# 3D heterogeneous system integration

By Peter Ramm [Fraunhofer Research Institution for Solid State Technologies EMFT] Peter Schneider [Fraunhofer Institute for Integrated Circuits, Design Automation Division IIS-EAS], and Renzo Dal Molin [SORIN Group]

**T**here are certainly different understandings in the microelectronics community with respect to the definition of 3D heterogeneous integration. A very general definition is as follows: 3D integration of different *devices* such as a CMOS processor and a memory, for example. According to a more limiting specification, there would be, as well, the integration of different substrate materials as a necessary condition (e.g., GaAs/silicon). This article will provide a reasonable definition of heterogeneity in between: 3D integration of components with *significantly different device technologies* such as CMOS and MEMS.

Fraunhofer has been working on 3D integration for almost 3 decades. Already in the mid-90s the Munich institute IFT (now EMFT) focused on 3D technologies for the use of known good dies by chip-to-wafer stacking (against at the time's mainstream concepts of wafer-to-wafer stacking). Understanding the necessity for combining research on both 3D technology and design at an early stage, we established a fruitful cooperation between the two Fraunhofer Institutes in Munich and IIS-EAS Dresden. 3D integration is now considered to be a new paradigm for the semiconductor industry. There are various ways to vertically interconnect devices, where the most advanced technology is based on through-silicon vias (TSV) [1]. Within wafer-level packaging, the platforms using TSVs are 3D IC integration and interposers ("2.5D"). Silicon interposer technologies are already mature and used in several production lines. Concerning "true" 3D ICs, the situation is different: the first companies are just beginning to take the step to production of 3D integrated products. This also provides a motivation to investigate the 3D IC patent situation. The large companies IBM, Samsung, Micron, TSMC, Hynix, and STATS ChipPAC are the leading players concerning the number of

patents, as expected. On the other hand, relevant patents on 3D integration are also found among different academic institutions with ITRI being the top institute, followed by CEA (France) and Fraunhofer-Gesellschaft München (Germany). Apparently, Europe is strong in intellectual properties for 3D ICs too. Worldwide, memory-enhanced applications are seen as the main driver for 3D integration. According to revenue forecast surveys by Yole, heterogeneous MEMS/IC systems could become the driving markets for 3D-TSV integration with a predicted demand for MEMS with 3D-TSV of several hundred thousand wafers a year by 2015 [2]. With the maturity of heterogeneous 3D integration technologies and corresponding low-cost fabrication, a diversity of 3D integrated CMOS-MEMS products will be developed, leading to a further key application track (Figure 1).

## Making 3D heterogeneous system integration possible

3D ICs are certainly the key enabler for 3D heterogeneous systems. Moreover, specific requirements are highly-reliable

and robust processes for stacking, vertical interconnections for fully-processed devices by wafer-level 3D integration of known good dies (KGD), and being able to accomplish very small form factor and fine-pitch vertical interconnects. In particular, 3D-TSV technologies with freely selectable TSV positions have a strong demand for 3D system design methods to enable high performance of extremely miniaturized heterogeneous systems. The technology developments will have to deal with the following three basic conditions for heterogeneous integration: The components to be integrated will in general: 1) Be fully-processed devices (e.g., ICs with different complex back-end-of-line layers, sophisticated MEMS/NEMS or antennae devices); 2) Exhibit different chip areas; and 3) Not necessarily be fabricated with very high wafer yield.

As a consequence, robust and reliable 3D technologies based on chip-to-wafer stacking of KGDs are needed. To supply solutions for these requirements the European e-BRAINS consortium established the 3D Heterogeneous Integration Platform where technologies

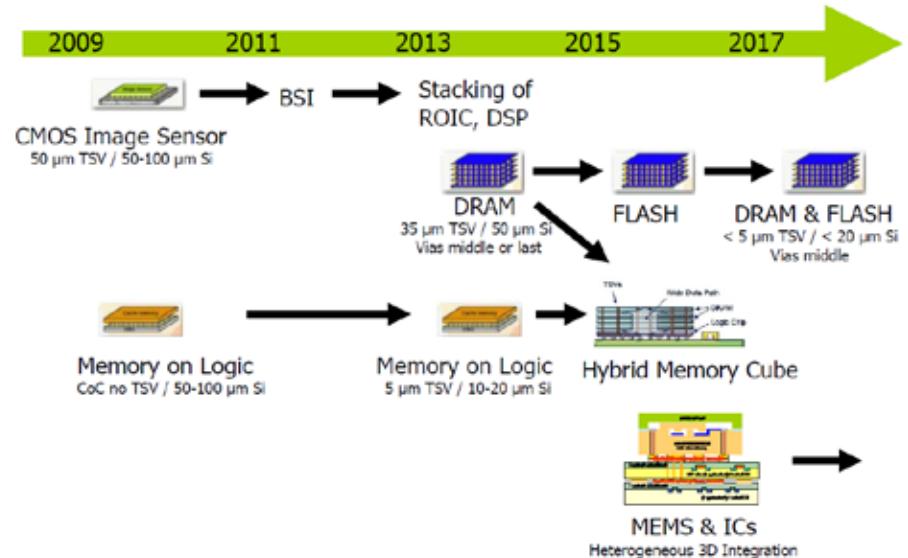


Figure 1: Application development for 3D integrated products [2].

of the following relevant main categories (with definitions according to ref. #1) of 3D integration are provided to enable future applications of smart sensor systems [3]: 1) 3D system-on-chip integration – 3D-SoC: TSV technology for stacking of thinned devices or large IC blocks (global level); 2) 3D wafer-level-packaging – 3D-WLP: embedding technology with through-polymer vias (TPV) for stacking of thinned ICs on wafer-level (no TSV); and 3) 3D System-in-package – 3D-SiP: 3D stacking of packaged devices or substrates.

Regarding TSV performance, the applications do not need ultra-high vertical interconnect densities as for 3D stacked integrated circuits – 3D-SIC (definition per ref. #1). Nevertheless, the lateral sizes of the TSVs are preferably minimized to allow for place and route for small “open” IC areas. Smaller TSVs are also preferred in order to reduce thermomechanical stress. e-BRAINS’ focus is on how heterogeneous integration and sensor device technologies can be combined to bring new performance levels to targeted applications with high market potentials. The consortium, under coordination of Infineon and technical management by Fraunhofer EMFT, comprises major European system manufacturers (Infineon, Siemens, SensoNor, 3D Plus, Vermon and IQE), SMEs (DMCE, Magna Diagnostics, SORIN and eesy-ID), the large research institutions CEA Grenoble, Fraunhofer (EMFT Munich & IIS-EAS Dresden), imec, SINTEF, Tyndall and ITE Warsaw, and universities (EPFL Lausanne, TU Chemnitz and TU Graz). Target applications include automotive, ambient living and medical devices, with a specific focus on wireless sensor systems. Concerning the enabling 3D Heterogeneous Integration Platform, the e-BRAINS partners are working close together, where Infineon, Fraunhofer EMFT, imec and SINTEF are focusing mainly on 3D-SoC and 3D-WLP, while the French system manufacturer 3D Plus and Tyndall are focusing on 3D-WLP and 3D-SiP technologies.

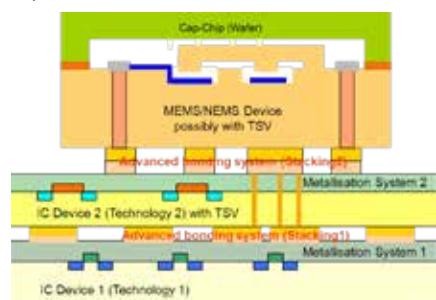
In future sensor systems components, especially those used for the internet-of-things (IoT) applications, application-specific ICs (ASICs) and sensors will be integrated using dedicated 3D heterogeneous integration schemes. A 3D architecture of a wireless sensor system,

for example, typically contains at least two IC devices: a sensor read-out and a communication ASIC (**Figure 2a**). In **Figure 2b**, an IoT-relevant application example is shown that implements additional security features to essentially hinder manipulation and misuse of secret/private data and counterfeiting of components (Fraunhofer EMFT trademark e-S<sup>3</sup>ense and patent pending); the robust face-to-face metallization is realized by intermetallic compound (IMC) bonding of the two ASICs. The sensor is connected by tungsten-filled TSVs through the ASIC 1. IMC bonding by solid-liquid-interdiffusion (SLID) [4] is used to mechanically and electrically interconnect the MEMS and IC devices in a robust and reliable way, as well as ensure sealing of the complete MEMS/IC stack.

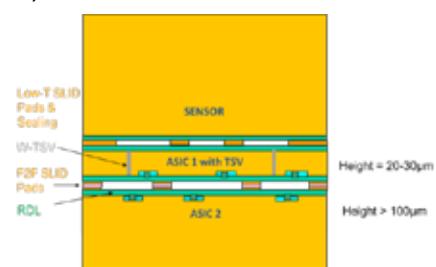
Fraunhofer EMFT’s 3D-SoC technology “TSV-SLID” can be applied to completely fabricated devices and fulfills the requirements for heterogeneous products described above. In this technology, TSVs are processed through all exposed layers of the IC (Si and dielectrics). The complexity of corresponding processing for vertical interconnects can be seen in a cross section of an ASIC with 7-level metallization and tungsten-filled TSVs prepared for device stacking (**Figure 3**). Ultra fine-pitch W-TSVs (lateral dimension 1-2µm) are used for the 3D-SoC process, because of reduced built-in stress, full CMOS compatibility, and particularly the established production capability. Obviously, until today, only 3D IC integration based on W-TSV has been used for production (e.g., at Tezzaron and IBM).

Substantial progress beyond the state-of-the-art in 3D integration is especially needed for sensor applications and has been achieved within the e-BRAINS project. One of the key issues for heterogeneous systems’ production

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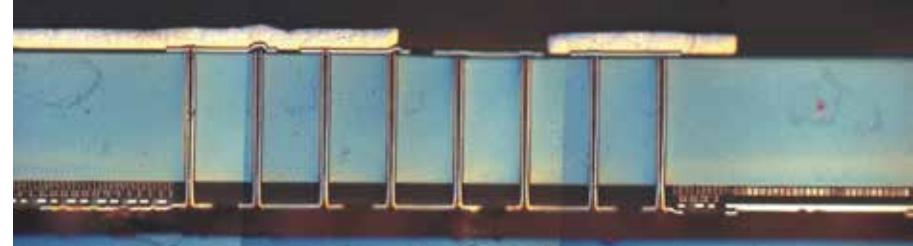


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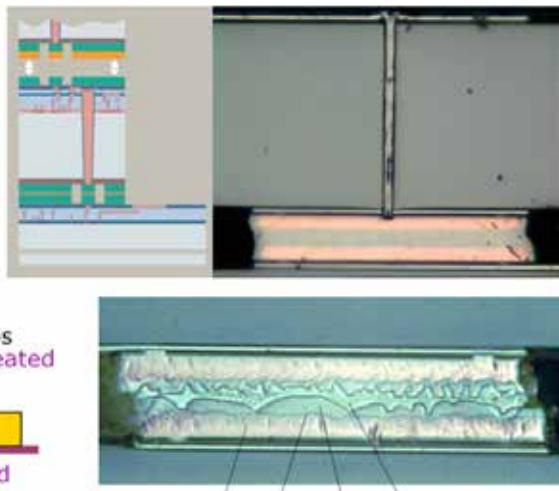
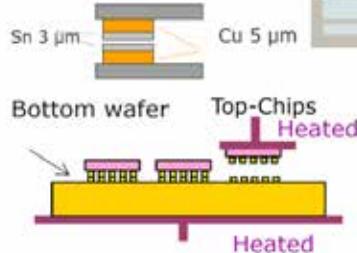
**Figure 2:** a) Typical sensor/IC integration schemes based on 3D-SoC technology with a back-to-face IC stack, and b) face-to-face IC stack by TSV-SLID technology. Source: Fraunhofer EMFT

is the impact of 3D processes on the reliability of the product, i.e., the high built-in stresses caused by, as an example, the coefficient of thermal expansion (CTE) mismatch of complex layer structures (thin Si, inter-metal dielectrics, metals, etc.) in combination with elevated bonding temperatures. In simplified terms, the lower the process temperatures, the lower the stress issues. As a consequence, Fraunhofer EMFT focuses on the development of highly reliable low-temperature bonding for 3D heterogeneous integration. A new IMC bonding technology was developed using ultrasonic agitation in a Panasonic FCB3 Bonder to reduce the assembly temperature below the melting point of tin (see **Figure 4**). Robust die-to-wafer bonding at 150°C has been demonstrated based on a Cu/Sn metal system, with shear forces



**Figure 3:** ASIC with 7-level metallization and W-TSV prepared for stacking by SLID bonding. Source: Fraunhofer EMFT

Reference:  
SLID Bond of Fraunhofer  
EMFT's TSV-SLID test  
structures by EVG at 280°C



Low temperature (150°C) Cu-Sn SLID Bond by Panasonic FCB3 with US-head

**Figure 4:** Low-temperature IMC bonding technology using ultrasonic agitation (Fraunhofer EMFT).

of 17MPa and an alignment accuracy of 3μm [5].

### System design requirements

With heterogeneous 3D integration, specific challenges for system design

come up. Partitioning is not only given by functional building blocks, but also by specific technologies for sensor elements, ASICs, microcontrollers, or communication circuits. To summarize, the design task for the 3D integrated

system is to find an integration scheme considering the following: 1) The number and location of connection points of the components, 2) Available capabilities for redistribution layers/interconnects, 3) Operational constraints, (e.g., accessibility of sensors, orientation of antennas), and 4) Requirements regarding the process sequence (e.g., maximal processing temperature, materials involved).

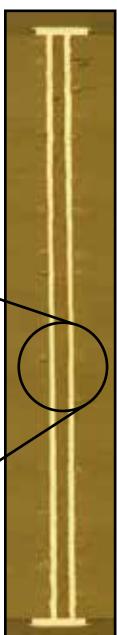
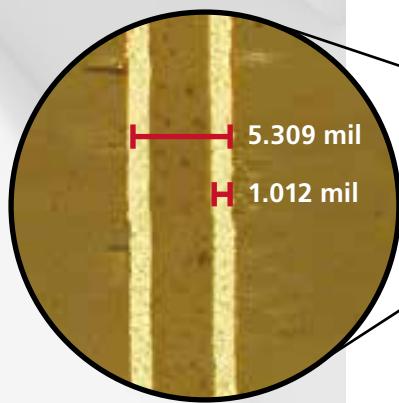
This integration scheme has to meet the given requirements concerning performance, reliability and cost. Because some of the above mentioned conditions are usually not fixed at the beginning of the system design, a huge design space opens up. The only way to handle this complexity is to find a model representation of the system that can be used for design space exploration and that must be refined and adapted later on during the design process.

Component design for a heterogeneous integrated sensor system is usually carried out in parallel using different design approaches and flows. Analyses of system variants in early design phases provide

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important input for component design. However, a raw estimation of a stack layout and TSV positions may change within the design process. Therefore, it is necessary to interlink the parallel component design flows to enable a continuous optimization of the integration scheme. For that reason, within e-BRAINS, a design flow framework for heterogeneous integration has been defined. In **Figure 5**, an overview of the framework is shown.

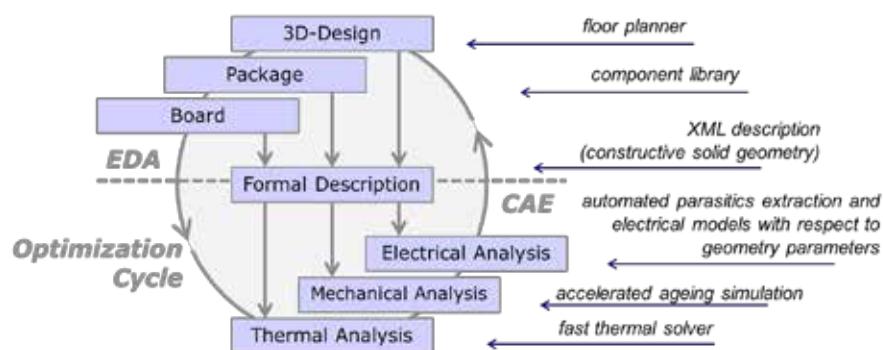
An XML-based approach for a unified representation has been developed to describe geometry data of stack components such as electrical interconnects, dies or packages. A library of basic elements, for example, that are characterized regarding electrical or thermal behavior is provided. This allows one to build up comprehensive system models and enables a high degree of reuse.

Furthermore, a hierarchical modeling

approach is necessary for multi-physics-simulations in different design phases and incorporating different sub-components. The term "hierarchical model" in this approach refers to a set of multi-level models applied for the detailed description of system behavior implemented on various levels of abstraction. Basically, it consists of a principal model structure that is "loaded" with models suitable for a specific analysis. That means, for example, for early design phases a raw estimation of interconnect delays is completely sufficient; while later on, parasitic extraction and a detailed characterization of the timing of critical interconnect paths are crucial. The models for this spectrum of analysis have to be consistent on all levels of abstraction. Of course, these models are also correlated with the manufacturing technology and must be validated by measurements.

## Range of applications

In general, all fields of ambient assisted living, smart buildings (e.g., wireless gas sensors for air quality systems), safety and security (e.g., IR imagers), biosensors



**Figure 5:** Outline of the e-BRAINS design flow framework.

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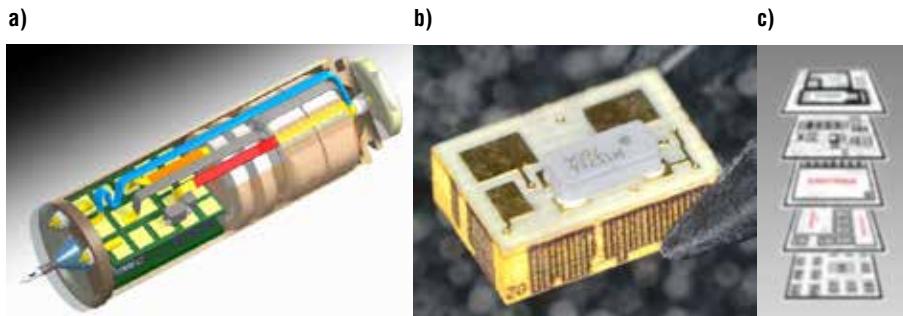
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**Figure 6:** a) Leadless pacemaker prototype; b) 3D heterogeneous integration; and c) stacked IC layers.

and smart medical systems (e.g., active medical implants) are all foreseen applications.

More than 1 million pacemakers and more than 0.2 million defibrillators are implanted around the world each year. These numbers are increasing every year due to the increasing aging population and to the increase in implantation rates in emergent countries. Infusion pumps for diabetes or back pain represent more than 0.2 million devices implanted per year. Neurostimulators implanted for pain management, epilepsy, Parkinson's disease, obesity, or depression, are growing rapidly and currently more than 0.2 million devices are implanted each year. In 2010, 219,000 people worldwide had cochlear devices implanted. In the U.S alone some 900,000 people are believed to be deaf or near deaf. In India, there are an estimated 1 million profoundly deaf children, while only about 5,000 have cochlear implants. The main indication for pacemaker implantation is the atrioventricular block, which induces bradycardia or very slow, or no heart rate at all. In 2012, 4.89 million people were estimated to have this pathology worldwide. The global market revenue for pacemakers in 2012 was \$4.3bn.

Leadless pacemakers are expected to be revolutionary to the cardiac rhythm management industry by eliminating the need for lead replacement, which can generate an infection in 4% of the cases. In case of infection, the removal of the lead attached to the heart tissue is performed. This intervention might be critical and necessitates the patient hospitalization for several days in specialized care units. The state-of-the-art for the volume of a subcutaneous pacemaker is  $8\text{cm}^3$ . The state-of-the-art for the leadless pacemaker volume is  $1.5\text{cm}^3$ . The first subcutaneous pacemaker was implanted in 1958. The first leadless pacemaker was implanted in

a human in 2013. Leadless pacemakers need extremely miniaturized system integration to reduce the size. The use of 3D heterogeneous integration is one technique that satisfies this constraint.

### Leadless pacemaker (SORIN)

**Figure 6a** shows a leadless pacemaker. The diameter of the device is 6.5mm and the length is 27mm. All the electronics of the pacemaker are located in a 3D stacked heterogeneous module, built with 3D PLUS wireless-die-on-die (WDoD) technology, as represented in **Figure 6b**. The size of the 3D heterogeneous module is  $2.3 \times 5.2 \times 7.3\text{mm}^3$ . **Figure 6c** shows the different layers stacked to get the module represented in **Figure 6b**.

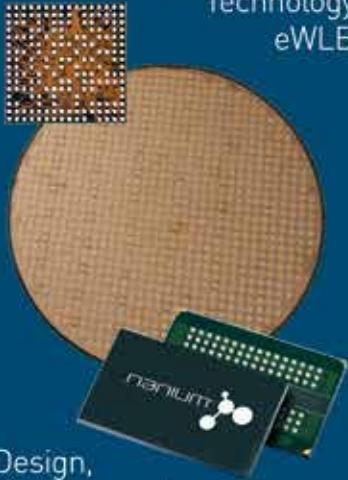
Two redistributed layers based on the embedded wafer-level ball grid array (eWLB) process were used. These layers have a thickness of  $300\mu\text{m}$  and are populated with multiple back lapped chips having the same height. The other layers are PCB-based having surface mount devices (SMDs) of different heights. Manufacturing of 3D heterogeneous integrated modules for all the electronics of a leadless pacemaker has been proven effective. It can be concluded that 3D heterogeneous integration allows a reduction of the size of the electronics, which is necessary to fit inside the small volume allocated in a leadless pacemaker.

The next-generation pacemakers will deal with heterogeneous integration of energy harvesters and other passive components as super-capacitors. Corresponding low-temperature 3D integration processes have to be implemented in order to fulfill the challenging process temperature specifications for such components. For developing suitable technology solutions, i.e., for integration of durable energy harvesters to heterogeneous systems, SORIN, 3D PLUS, and Fraunhofer



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EMFT are continuing their cooperation in a new large European project called "MANpower" [6].

The main driver of 3D heterogeneous integration is certainly sensor integration. The system integration of sensors with ICs and passive components, such as energy harvesters, actuators and batteries, is becoming more and more important, especially for the high growth

market area of distributed wireless sensor systems, which will constitute the key connected hardware infrastructure of the Internet of Things.

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## Biographies

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**Upcoming Trade Shows (2015):**

**European 3D/TSV Summit**  
 Grenoble, France ; January 19-21, Booth: 9

**iMAPS Int. Device Packaging Exhibition 2015**  
 Fountain Hills, AZ, USA; March 17-18, Booth: 6

# INDUSTRY NEWS

(continued from page 15)

## IMAPS 2014 explores the future of packaging

By Chip Scale Review staff



The 47th annual IMAPS 2014 International Symposium on Microelectronics convened at the Town and Country Resort and Convention Center in San Diego, CA on October 13-16, 2014 (Figure 1). The theme of the event this year was "Future of Packaging." Dr. Subramanian S. Iyer, IBM Fellow and IMAPS 2014 Technical Chair, commented, "With classical silicon scaling saturating, and the cost per

medical, and communications applications that continue to drive the electronics industry.

The technical program featured 104 excellent presentations organized in six parallel tracks: 1) Future of Packaging, 2) Advanced Packaging Interconnect & Assembly, 3) Materials & Processes, 4) Modeling, Design & Test, 5) Interposers & 3D Packaging, and 6) 3D Embedding & Reliability. As anticipated, the most popular track appeared to be the one focused on interposers and 3D packaging. Outside of this track, several presentations drew large crowds.

For example, it was standing room only for the "Wafer Dicing Using Dry Etching on Standard Tapes and Frames"

presentation by Thierry Lazerand of Plasma-Therm (Figure 4).



Figure 4: Thierry Lazerand, Plasma-Therm.

The exhibition hall was sold out this year with 120 companies promoting their products and services, including Premier sponsors Natel, Heraeus, and Metalor. The majority of exhibitors surveyed indicated that it had been a good show for them with most of the booth traffic coming on the first day (Figures 5-9). Total attendance was up over last year's 2013 event.

In addition, there were 15 Professional Development Courses offered on 1) Chip Packaging Processes and Materials, 2) Fundamentals of Microelectronics Packaging, 3) IC Fabrication and Electronic Packaging, 4) Interposers - Silicon, Organic

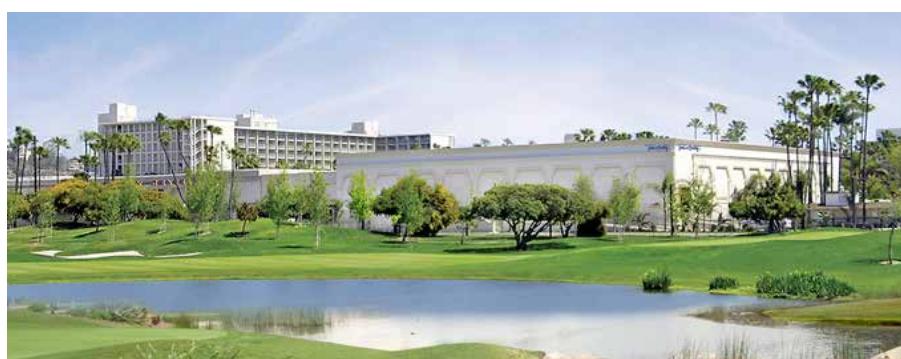


Figure 1: Town and Country Resort & Convention Center.

transistor, in some estimates potentially increasing, keeping the expectations of Moore's 'law' going for another decade or two will depend on how we successfully scale packages and boards."

This year's event was highlighted by five keynote presentations by distinguished business leaders: Dr. Steve Bezuk of Qualcomm (Figures 2,3), Dr. Kamal Sikka of IBM, Dr. Franck Murray of IPDIA, Dr. Ilyas Mohammed of Jawbone, and Kunal Parekh of Micron. They were joined by Dr. Rao Tummala of Georgia Tech and Dr. Bharath Rangarajan of Advanced Nanotechnology Solutions for a stimulating panel discussion on the "Future of Packaging." The talks and discussions echoed a common theme that 2.5D and 3D packaging is the key to higher performance, smaller size, and lower costs needed to manufacture future portable, wearable, and mobile products developed for computing,



Figure 2: Keynote, Dr. Steve Bezuk of Qualcomm.



Figure 3: Keynote - standing room only.



Figure 5: Exhibitor Unisem, Angela Lee & Rino De Leon.



Figure 6: Exhibitor EPP GmbH, Dayton Bishop & Heinrich Stenger.



**Figure 7:** Exhibitor Azimuth Electronics: Melissa L. Johnsen, RoJean Hall, Kenneth C. Johnsen, Priscila Agbayani.



**Figure 8:** Exhibitor, AMICRA: Johann Weinandler.



**Figure 9:** Special demonstration by Carlsbad High School, FTC Robotics Team 6226 in exhibit hall.

and Glass, 5) Packaging and Testing of Implanted Medical Devices, and 6) Understanding the Common Failure Modes from a Physics of Failure Perspective.

IMAPS Executive Director, Michael O'Donoghue, observed, "We were extremely pleased to see a substantial increase over last year's event. One of the primary strategic goals of the Society is to always work to strengthen the technical content of the Symposium (Figure 10).

#### Statistics from IMAPS 2014:

- 1136 total registrations in our IMAPS 2014 database this year.
- Total attendance increase of 25.8% over 2013 (Orlando).
- Total attendance increase of 12.5% over 2012 (San Diego).
- Total attendance increase of ~5% over both 2011 (Long Beach) & 2010 (Raleigh).
- IMAPS first sold out symposium exhibition in more than 10 years!



**Figure 10:** IMAPS Executive Director, Michael O'Donoghue.


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- A 19% increase in full conference registrations (those in sessions) over 2013.
- An increase in IMAPS member participation and a 49% increase in non-member registrations over 2013!
- A 79% increase in "exhibits only" participants visiting the exhibit floor!
- Across the board in registrations, PDC/ short course sign-ups, exhibits and more – we had more people participating this year.
- Attendees came from 22 countries around the globe: Germany, UK, Japan, Taiwan, France, Austria, Singapore, and Turkey, to name a few.
- More than 500 people attended from the host state of California.
- More than 147 "Chief Executives" (C-Level, Presidents, VP, etc.) were in attendance.
- 132 exhibit booths were on display at IMAPS 2014, including five "Research Lab" Corridor booths.

## European 3D TSV Summit 2015: keynote speakers announced

By Chip Scale Review staff



SEMI announced keynote speakers for the third edition of the European 3D TSV Summit event that will take place on January 19-21, 2015 in Grenoble, France. As an increasing number of companies, such as IBM, Xilinx, Samsung and Bosch, are



taking 3D through-silicon via (TSV) technology to the commercialization phase, the necessity for understanding the business and technological context surrounding these devices has become more important than ever. In this context, SEMI invited experts on the forefront of the technology to share their perspectives on the industry.

Joining the conference as a keynote speaker, Bryan Black, senior fellow at AMD, will inform participants that

die stacking is finally happening in mainstream computing and explain the impacts of this technology on the industry. Timo Henttonen, senior manager packaging at Microsoft, will discuss his vision of the future of 3D TSV for smartphones and connected devices. Additionally, Bill Chen, fellow and senior technical advisor at ASE Group, will deliver a talk about the integration of 3D TSVs into the DNA of packaging.



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In addition to these three keynote speakers, over 20 invited speakers and panel discussion participants will share their views during the 3D TSV conference, including industry experts from Qualcomm, IBM, HP, ams AG, imec, CEA-Leti, Fraunhofer-IKTS, Broadpak, SPTS, SUSS Microtec, EV Group, BESI, KLA-Tencor, Rudolph Technologies, Asahi Glass, Corning, Oerlikon, STMicroelectronics, Amkor and more.

New this year, the Summit will include a Pre-Summit Market Briefing dealing specifically with the 3D TSV market outlook and hosting several talks by financial analysts and industry consultants, including Yole Développement, TechSearch International, AlixPartners and ATREG.

Over 30 companies will join the event as exhibitors. In addition to the exhibit and conference, attendees will have the opportunity to set up one-on-one business meetings and visit the CEA-Leti 300mm TSV-capable clean room.

For more information, please visit [www.semi.org/european3DTSVSummit](http://www.semi.org/european3DTSVSummit) or contact Yann Guillou, SEMI Europe Grenoble Office ([yguillou@semi.org](mailto:yguillou@semi.org)).



## **WinWay Technology acquires Wentworth Laboratories' Saber® Probe-based vertical probe card products**

WinWay Technology Co., Ltd., has acquired the Saber® Probe-based vertical probe card assets and related intellectual property of Wentworth Laboratories, Inc., which is headquartered in Brookfield, CT, USA. Wentworth is a global supplier of probe cards and wafer probing products for the semiconductor test industry. The acquisition of

Wentworth Saber® Probe-based vertical probe card products immediately and substantially increases WinWay Technology's total available market, and is expected to assist in the penetration of vertical probe card markets while providing additional scope and performance advantages for existing product lines.

The acquisition includes all patents and trademarks associated with Wentworth Verimax™, Accumax, and Micromax® vertical probe card products. At the core of Wentworth's vertical probe card technology and central to this acquisition is the proprietary Saber® Probe, a photo mask-defined, chemically-etched probe that enables its vertical probe cards to deliver robust overall electrical performance with longevity.

WinWay Technology and Wentworth customers are poised to benefit from both company's well established global service and support and continuing commitment to quality SaberProbe-based vertical probe card manufacture. Mark Wang, WinWay Technology Founder and Chief Executive Officer commented, "SaberProbe-based vertical probe card technology complements WinWay Technology's socket products as well, and this is only one area where we anticipate cost, efficiency and performance advantages to be realized as a result."

"Wentworth's patented SaberProbe-based vertical technology has been production proven in many extreme test environments", said Stephen Evans, Wentworth Laboratories Chief Executive Officer. "There is exceptional synergy between Wentworth Verimax products in particular and the strategic vision and capabilities of WinWay. This transaction benefits all stakeholders of Wentworth Laboratories and WinWay Technology, including our dedicated employees and our valued customers."

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## Ultratech introduces Superfast 4G low-cost in-line inspection system for patterned wafers

Ultratech, Inc. (Nasdaq: UTEK) has introduced the Superfast 4G high-volume, in-line, 3D topography inspection system. Ultratech's new 4G system builds on the field-tested capability of the Superfast 3G. The new system's patented coherent gradient sensing (CGS) technology provides a high degree of flexibility that enables end users to utilize a single type of wafer inspection tool to measure the front side of patterned wafers across the entire fab line at the lowest cost. Ultratech plans to begin shipping the Superfast 4G systems in the first quarter of 2015.

Ultratech Vice President, Marketing Inspection System & Technology Transfer, Shrinivas Shetty, commented, "By working with leading-edge memory and logic customers using Ultratech's 3G systems, we were able to successfully implement the industry's requirements for 3D topography with in-line inspection tools." He further noted that the company invested heavily in the algorithm and factory automation capabilities, expanded manufacturing capacity in Singapore, and developed regional senior applications managers to help ensure a smooth ramp to volume production. The company also made significant improvements to the Superfast 4G inspection system, resulting in increases of 2.5x in performance and 65% in throughput, as well as a 30% reduction in edge exclusion, compared to the 3G system.

The two inspection systems have identical process modules – retaining all critical optical components ensuring a smooth transition from the 3G to the 4G system for high-volume production.



## SPTS Technologies named MEMS/Sensors Supplier of the Year at the 2014 MEMS Executive Congress U.S.

SPTS Technologies, an Orbotech company, was named MEMS/Sensors Supplier of the Year at the MEMS Executive Congress U.S. 2014, held in Scottsdale, Arizona. In addition, Kevin Crofton, President, SPTS Technologies



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### Ellsworth Adhesives expands in Mexico with new Dow Corning agreement

Ellsworth Adhesives announced a new agreement with Dow Corning as authorized distributor for the Industrial Assembly and Maintenance Market in Mexico. Ellsworth Adhesives offers a comprehensive line of Dow Corning® branded adhesives and sealants, elastomers, foams and fluids, as well as a full line of Molykote® branded lubricants from Dow Corning, which include compounds, dispersions, oils, greases, pastes, and anti-friction coatings for use in industrial assembly and maintenance applications.

“Our current industry and market knowledge will allow us to aggressively develop business throughout the region with Dow Corning,” said Roger Lee, Vice President and General Manager of Ellsworth Adhesives North America. “We are anxious to begin leveraging our local expertise immediately to maximize our mutual growth in this area.”

Ellsworth Adhesives has been a Dow Corning authorized distributor for over 35 years, and remains as one of Dow Corning’s largest North American and Global Distributors.

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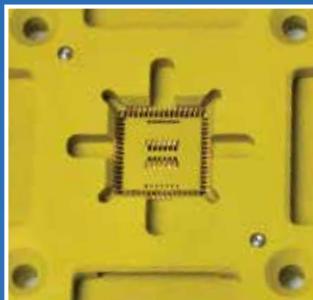
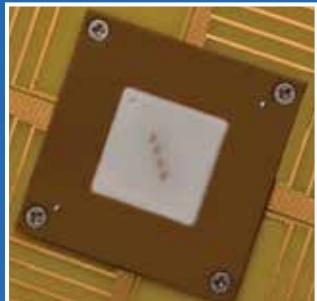
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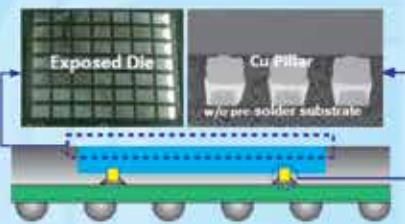
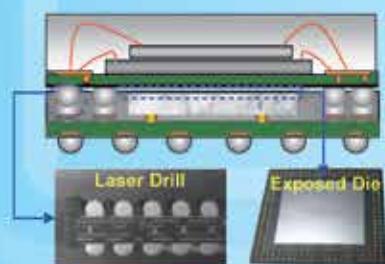
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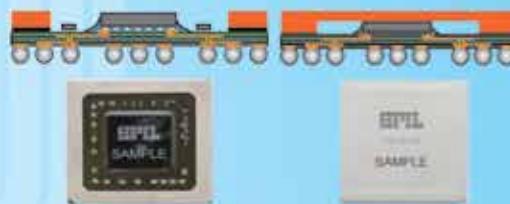
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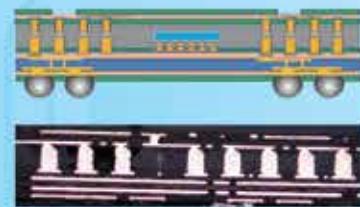
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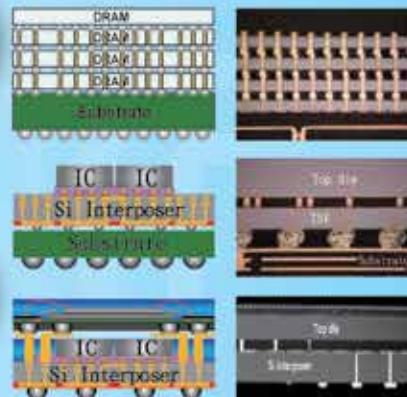
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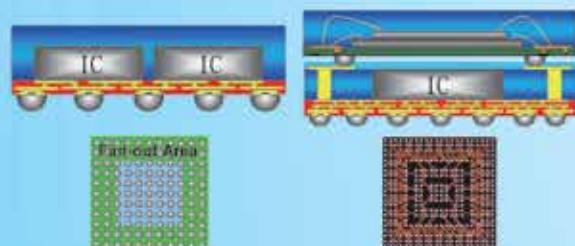
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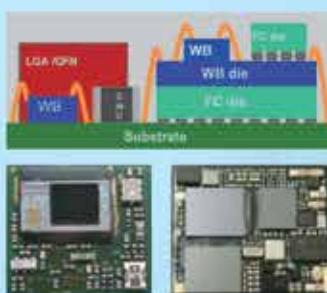
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