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The Future of Semiconductor Packaging

Volume 23, Number 4

July • August 2019

The New 3D Architecture

- MRAM testing for HVM
- 2.5D packaging design flow
- Reliability physics analysis (RPA)
- Semiconductor-on-Polymer CSP
- Battlefields of fan-out packaging
- Advanced packaging carriers for FOWLP
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Data centers (*i.e.*, AI, machine learning, deep learning, computation run-off data center hardware) are driving next-generation semiconductor packaging, especially 2.5D and 3D integrations. In particular, data centers are the primary target market for 3D DRAM, 3D NAND for SSDs, and 2.5D CPU/GPU/FPGA/SoCs, etc. These devices are the focus of all the large semiconductor companies for not only their current high-end product lines, but also those of the future.

Cover art courtesy: XPERI Corporation

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The International Magazine for Device and Wafer-level Test,
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High-density Interconnection of Microelectronic IC's including
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STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Lawrence Michaels Managing Director/Editor

lmichaels@chipscalereview.com

Debra Vogler Senior Technical Editor

dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Steffen Kröhnert - Advanced Packaging

steffen.kroehnert@esp-consulting.com

John L. Lau, Ph.D - Advanced Packaging

john_lau@unimicron.com

Ephraim Suhir, Ph.D - Reliability

suhire@aol.com

Rao R. Tummala, Ph.D - Advanced Packaging

rao.tummala@ece.gatech.edu

EDITORIAL ADVISORS

Andy Mackie, Ph.D (Chair) Indium Corporation

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Leon Lin Tingyu, Ph.D National Center for Advanced

Packaging (NCAP China)

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Lawrence Michaels

lmichaels@chipscalereview.com

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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. In the U.S. subscriptions by first class mail are \$125 per year. Subscriptions outside of the United States are \$225 per year to other countries.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January–February, March–April, May–June, July–August, September–October and November–December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine
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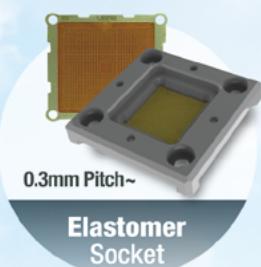
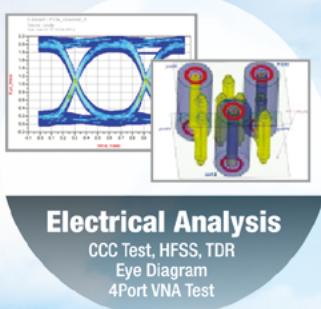
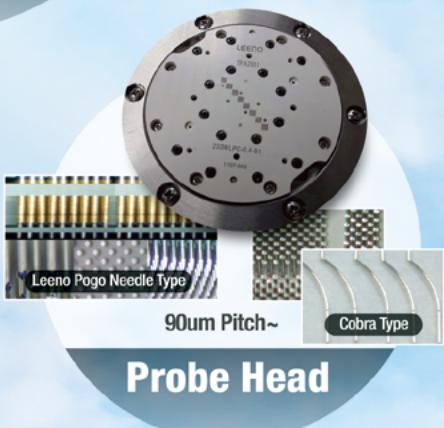
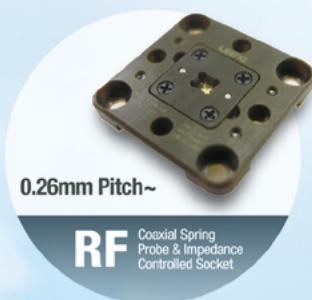
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Semiconductor-on-Polymer™ chip-scale packaging (SoP CSP)

By Douglas Hackler, Dale Wilson [[American Semiconductor](#)]
and Edward Prack [[MASIP LLC](#)]

Semiconductor-on-Polymer™ (SoP) chip-scale packaging (CSP) is a new advanced packaging approach for ultra-thin integrated circuits (ICs). The technology results in the thinnest CMOS ICs theoretically possible and is currently being used to produce the industry's thinnest system-on-chip (SoC) devices. The thin technology based on full polyimide die encapsulation resolves many challenges in homogeneous integration and is especially applicable to the emerging field of flexible hybrid electronics (FHE).

SoP CSP is a wafer-level packaging (WLP) process that integrates die into a package such that the end result can be thinner than what is possible with bare die (**Figure 1**). When bare

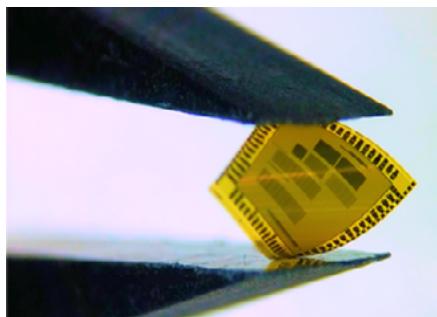


Figure 1: A FleX IC produced using the SoP CSP process is shown. Silicon thickness is less than 2µm with a total package thickness less than 35µm.

die are less than 50µm in thickness, they become prohibitive to process on account of cracking and chipping during assembly and are prone to all types of environment-related failures typical of unprotected die. At <15µm, bare die become mechanically unstable for handling. SoP CSP commonly includes die at <15µm and restores mechanical robustness by replacing the underlying silicon that typically supports the active device with

polyimide. The SoP CSP process can fully encapsulate the top surface, backside and die edges without the use of any die reconstitution, and is truly a wafer-level capability. The polyimide encapsulation restores many of the benefits of package die protection that are lost in a number of applications.

American Semiconductor Inc. (ASI) recognized early that the growth of the emerging printed electronics industry was severely limited by a lack of IC performance. The printed industry's reliance on printed transistors could not produce the performance and capability necessary to field thin, flexible technology systems with the computational, memory or communications capabilities necessary for modern electronic products. The ASI engineering team's response was to develop a hybrid approach that combined the performance of conventional ICs with printed large-area, flexible circuit boards (FCB) and printed devices.

Surface mounting conventional rigid high-performance ICs on flexible printed substrates was available commercially from companies such as Soligie, now a part of Molex, and the idea that flexible chips might be feasibly fabricated and applied to create hybrid "systems in foil" was suggested as early as 2009 (**Figure 2**) [1]. However, a feasible solution for producing ultra-thin, and possibly flexible chips, was not available.

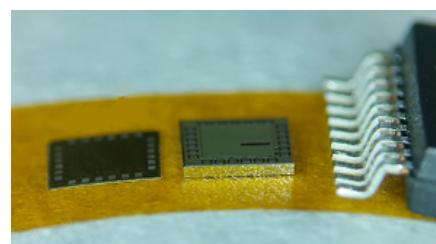


Figure 2: This image, a comparison of thickness is easily observed for an SoP CSP device in comparison to a bare die and a standard SOIC packaged device.

ASI addressed this lack of capability with the introduction of Semiconductor-on-Polymer (SoP) technology as a solution to enable a concept described as flexible hybrid systems, which later evolved into what is known today as FHE.

In 2011, SoP was presented as a wafer conversion process demonstrated using silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) wafers. Initial results proving feasibility were reported using high-performance CMOS ring oscillators in a 130nm process with silicon thickness as thin as 2000Å supported with polyimide [2]. Proof of feasibility for hybrid system assembly was demonstrated using SoP die and reported in 2013 using fully-flexible epoxy attach and interconnects on printed FCBs to produce ultra-thin flexible high-performance electronics systems [3]. Progress accelerated following the innovations in SoP wafer-level processing and FHE assembly.

In 2015, the FleX-ADC™, an 8-bit analog-to-digital converter (ADC) IC was introduced as the industry's first SoP packaged IC. The ADC was available in the FleXform™ ADC Kit, which included a FleX-ADC assembled on a PET FCB for the industry's first fully-flexible FHE commercial product. In 2017, ultra-thin wireless capability was demonstrated with the SoP version of the EM Microelectronic 4325. Also, the first ultra-thin and flexible SoC, a Cypress CY8C20, was produced, which included the first ever demonstration of a physically-flexible MCU and Flash memory capability based on a bulk CMOS technology. In 2018, SoP CSP was applied to NXP's NHS3100 to produce the industry's first ultra-thin near-field communication (NFC) SoC and demonstrated a physically-flexible ARM processor core. This year, SoP CSP utilization is further expanding with the release of the AS_NRF51822P, an ultra-thin and flexible Nordic 2.4GHz Bluetooth® Low Energy (BLE) IC.

Process details

SoP CSP is a wafer-level CSP capability (WLCSP) that can produce chips fully encapsulated in polyimide without the need for any reconstitution prior to encapsulation. Initially, SoP was released with only front and back polyimide coatings without encapsulation of the die sidewalls. This version of the process provided a solution for applications that required direct chip attach (DCA). SoP CSP resolved the cracking and chipping issues that are common when thin bare die are used. Most significantly, the front and backside packaging FleX-C SoP process, informally referred to as the “oreo” version, eliminated edge chipping for ultra-thin die and enabled singulation using industry standard dicing saws. The robust nature of the ultra-thin CMOS once sandwiched in the polyimide was evaluated for reliability under an Air Force Research Laboratory (AFRL) project to develop advanced reliability test procedures for thin devices. SoP packaged ICs achieved dynamic radius of curvature (RoC) and torsional testing in excess of 100,000 cycles. Programmable SoCs packaged in this style of SoP demonstrated full functional capability at RoC = 1mm. FleX-TM, the version of the SoP package with edge encapsulation is scheduled for release in 2019.

SoP CSP is moving beyond just overcoming the challenges of integrating high-performance devices on printed electronic substrates. Today, SoP ultra-thin package technology has gained broader interest and is considered anytime that an ultra-thin IC solution is desired. Automated assembly techniques originally developed for FHE have been applied to integration of SoP CSP ICs on conventional flex FCB (**Figure 3**). Flex FCB capabilities provide much smaller features and pitch than what is available for FHE. SoP CSP is a natural extension of z-height reduction for advanced packaging IC roadmaps. SoP has the potential to affect IC package thickness in the following 3 areas: 1) mold cap thickness, 2) elimination of encapsulation of FC packages, and 3) in embedded packaging. For conventional molded packages, the mold cap above the die can be reduced based on the very thin (10-45 μ m) SoP packaged die. This applies directly to flip-chip and wire-bonded molded packages.

In addition, SoP has the potential of eliminating encapsulation to protect the die in FC-BGA packages because the SoP package provides protection for the whole die. In this case, SoP can be used to produce thinner packages, simplify conventional package approaches, and lower the overall IC packaging cost by eliminating the encapsulation process after die attach and underfill. Integration of SoP CSP can result in thinner devices in embedded packaging, which could result in thinner final packages and improved yield/reliability the die protection afforded by the SoP process.

Summary

In conclusion, integration of ultra-thin die on printed materials, embedded applications and during reconstitution, places new demands on IC reliability. SoP packaging technology provides an opportunity to create high-reliability thin assemblies and can mitigate processing yield loss caused by surface damage, cracking and chipping of thin ICs in heterogeneous processing.

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Biographies

Douglas Hackler is President & CEO of American Semiconductor and the co-inventor of Semiconductor-on-Polymer technology. He has more than 30 years of experience in wafer fabrication, process development, manufacturing and commercialization at American Semiconductor, M/A-Com, Zilog, Intel, NorTel and General Instrument. Doug holds engineering degrees from the U. of Idaho (MSEE), Boise State U. (BSEE) and in management from Texas Tech U. (BBA). Email doughackler@americansemi.com

Ed Prack received his PhD from Texas A&M U. in Analytical Chemistry. He worked for Celanese Research Company for 5 years doing research in organic and inorganic fibers and resins. He worked for Motorola for 15 years including managing a package prototype line and a content expert in interfacial optimization and material/process selection for electronics from the fab through final products (e.g., cell phones, automotive modules). He worked for Intel for 12 years in IC packaging development. Dr. Prack subsequently founded MASIP (material analysis surface interface process).

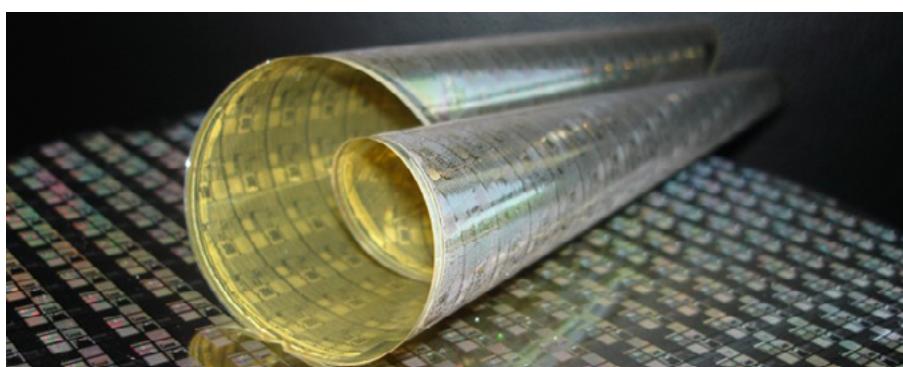


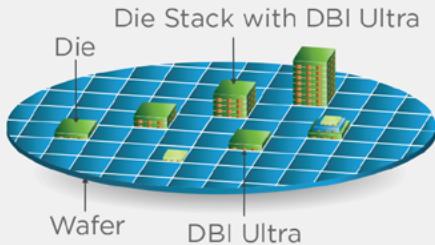
Figure 3: A 130nm CMOS triple-layer metal wafer processed using SoP WLCSP is shown. Wafers are not generally released from carriers prior to dicing, but the release has been done here to demonstrate the ultra-thin and flexible nature of the SoP wafer-level process.



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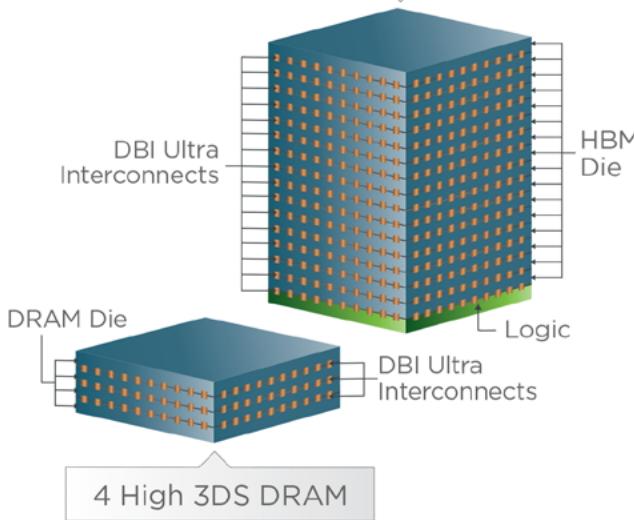
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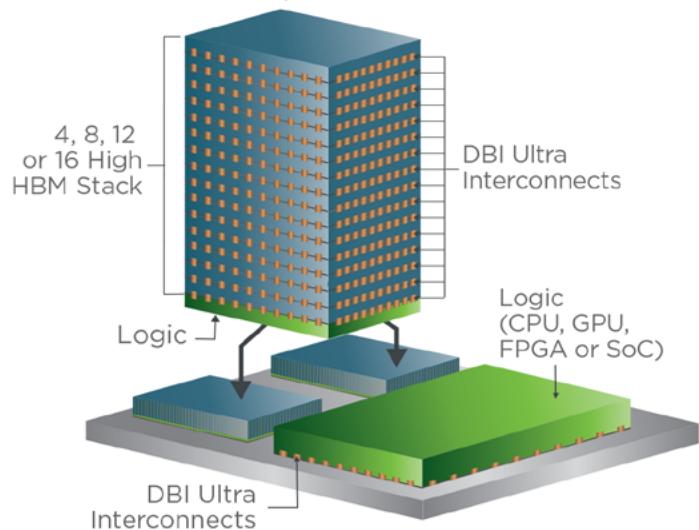
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Improving 2.5D packaging design flow: a brief history

By Tony Mastroianni *[eSilicon Corporation]*

The increasing demands of 2.5D packaging technology are driving the need for a more advanced and integrated design solution that includes digital prototyping capabilities for verification, validation and sign-off. We recently addressed the task of improving our package design flow to meet these increasingly complex requirements. Until late 2016, a spreadsheet, known as PLOC (short for pad location), had met our needs. When it became apparent that the PLOC methodology had reached its limits, we got to work on a full-featured tool set as described below.

Historical methods: a custom in-house solution

As a fabless semiconductor company, we provide a variety of services, including semiconductor intellectual property (IP) and custom application-specific integrated circuit (ASIC) design. Historically, we had done the complete package design for 90% of our ASIC customers. Originally, these were simple wire bond designs that were easily handled with the in-house PLOC spreadsheet solution.

As packaging technologies evolved, we expanded PLOC spreadsheet capabilities by adding new features and additional utilities. We used the PLOC spreadsheet to define the I/O centric information in the design database; the spreadsheet essentially defined the I/O ring design intent. The spreadsheet also included the ball-out and placement information.

Migrating to flip-chip packaging created an entirely new set of challenges for dealing with bumps and redistribution layers (RDL). We added additional utilities to the PLOC tool to help with rudimentary design planning. The expanded tool was capable of providing visual feedback of the placement. We wrote macros to highlight different design elements. Even with these enhancements, design planning with PLOC was still largely a manual exercise. We added

software engineers to the team specifically to develop new algorithms to continue growing the PLOC tool's capabilities.

The PLOC spreadsheet reaches its limits

We had been developing 2.5D test vehicles since 2011, but it was not until late 2016 that we started our first production 2.5D design. It quickly became apparent that the PLOC spreadsheet had reached its limits. We completed this first 2.5D production design using PLOC, but realized the approach had limitations. These limitations included the manual entry of data and the inability to do full end-to-end connectivity checks. Something radically different was required to address the complexity of 2.5D and, eventually, 3D designs. In mid-2017, we chartered a cross-functional team to solve the problem. The team consisted of designers familiar with the use and limitations of PLOC. We were highly dependent on using PLOC for defining the I/O ring, which we used to drive our layout vs. schematic (LVS) flow.

Our design team assessed what it would take to develop a full-featured tool that would meet all of the current and anticipated future needs. At that time, we also began looking into commercial solutions. One requirement was a solution that was not tied to any specific vendor's physical design tools. An open solution that would integrate seamlessly with the existing design flow and layout tools was the goal. The team also prepared a plan to develop an entirely new custom tool from scratch if it had to do so. That would be a very aggressive approach and would have been a significant effort in both time and manpower. Ultimately, we determined the available internal resources were insufficient to complete such a large effort within the desired timeframe. In lieu of a full-blown internal development program, the next step was to revisit available commercial solutions.

Selecting a commercial package planning solution

Selection of a commercial package planning solution was driven by several key needs:

- Replacing the spreadsheet solution with a package planning tool capable of handling complex 2.5D and 3D package designs;
- Finding an open solution not tied to any specific vendor's physical layout tools; and
- Making sure we could extend the tool's capacities through user-defined properties and a robust API.

Evaluation process

One of the solutions we evaluated was Xpedition Substrate Integrator (xSI) from Mentor, a Siemens Business. It appeared to have all the capabilities we were looking for in a prototyping/package planning tool. After our initial internal evaluation, we began working closely with Mentor to integrate xSI into our existing design flow. This combined effort also addressed design planning. Our physical design flow had previously depended on our PLOC spreadsheet. Because this new flow would obviate the use of PLOC, the I/O-centric database would be replaced with xSI. PLOC-type spreadsheets can still be used for importing and exporting intermediate formats, but the "golden" database – a single database that includes the entire design intent – resides within xSI. The xSI database would be used for floor planning of all designs.

In addition to design planning, xSI has replaced all the additional functions that used to be performed in PLOC and added several new capabilities. The xSI LVS flow and Calibre 3DSTACK capability were the perfect fit for us. xSI provides a much more robust design flow by adding a real database to manage and track connectivity. We have fully integrated the xSI Calibre 3DSTACK flow into our new design process.

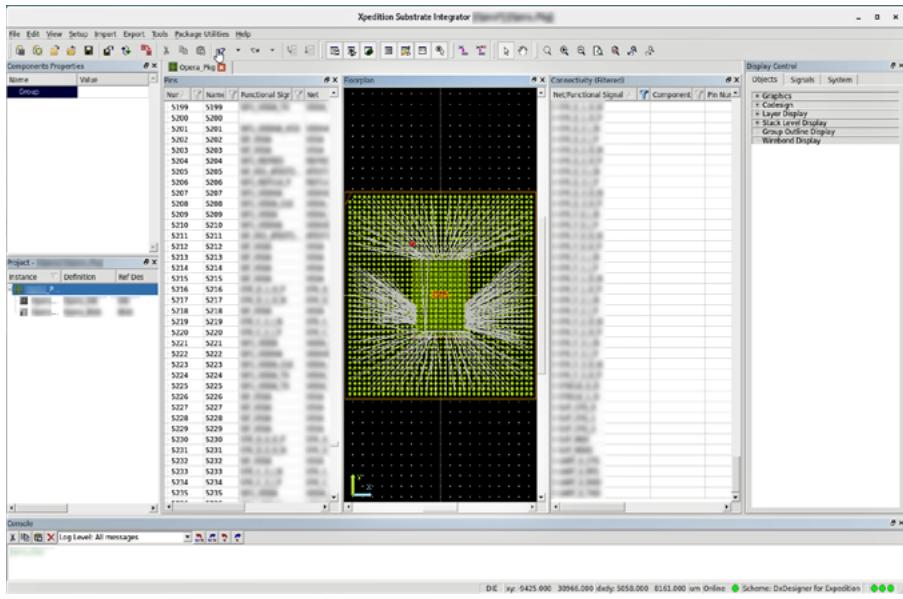


Figure 1: Multiple LVS violations that went undetected during layout were successfully identified using a package integration tool with full 3D connectivity checking.

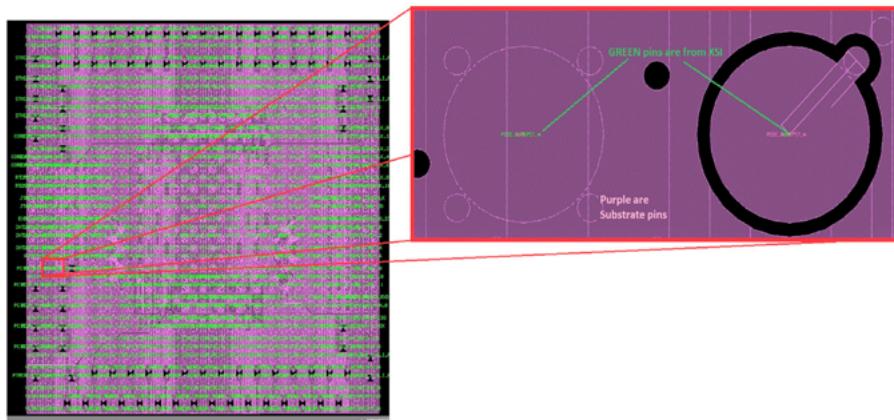


Figure 2: A short identified using 3D connectivity checking.

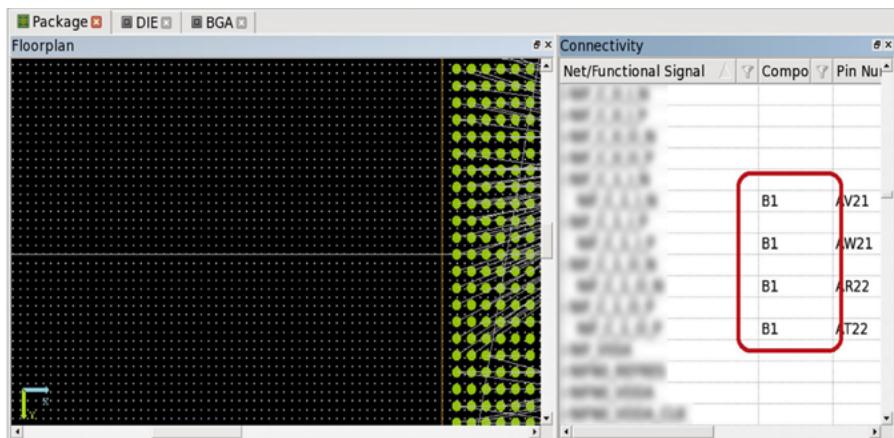


Figure 3: An open identified using 3D connectivity checking.

One of the first designs completed using this new process was a simple flip-chip package that illustrated the advantage of using a package integration tool with full 3D connectivity checking. For this project, we started the design in PLOC, and the PLOC data was imported into the planning tool mid-project. With the planning tool containing the entire package assembly's connectivity, it was possible to compare the intended connectivity with the actual implemented connectivity of the layout tool. As a result, we identified several open connections and short circuits that, if undetected and not corrected, would have resulted in chip failures (Figures 1-3). The impact of not catching these issues would have been costly in terms of both direct cost and delay to market. Typical debug time is two to three weeks to find the root cause of a package problem. Once the root cause has been identified, the design needs to be updated and new samples fabricated. In addition to the direct cost of manufacturing new samples, the total delay would have been in the 10–12 week range of real calendar time.

For our team, risk mitigation and improved productivity are two of the main benefits of using a dedicated package planning tool. To further ensure the design intent has been captured correctly, we exported the netlist from the planning tool, we then ran simulation, and verified the results. This is a much more robust methodology for complex 2.5D and eventually, 3D designs.

Summary

As the needs of our customers have evolved, we have grown our capabilities to meet more complex design requirements. By choosing the xSI solution, we can better serve the ever more complex demands of our growing customer base. In the one year since eSilicon began working with the xSI team at Mentor, we have already reaped the benefits of a more robust packaging solution. These benefits will continue to grow and be passed on to our customers.

Biography

Tony Mastroianni is Senior Director, Packaging Design at eSilicon Corporation, Allentown, PA. He joined eSilicon in October, 2001 and has managed over 30 ASIC designs from kickoff to tape-out. He has a Bachelor's Degree in Electrical Engineering from Lehigh U., and a Master's Degree in Electrical Engineering from Rutgers U. – New Brunswick. Email: amastroianni@esilicon.com

Enabling the new 3D architecture

By Javier DeLaCruz, *[XPERI Corporation]*

T

he challenges of sustaining Moore's Law and the shift to a "more than Moore" approach in the industry have been discussed in considerable detail [1,2]. We have seen numerous technologies to address both trajectories, with the introduction of new materials, processes and structures, including various integration and 3D-stacking approaches. Leading-edge CMOS image sensors (CIS) manufacturers, for example, have utilized wafer-to-wafer (W2W) Direct Bond Interconnect (DBI[®]) bonding technology, also known as hybrid bonding, in high volume for several years now because of its various advantages [3]. For other applications, such as high-bandwidth memory (HBM) and 3D-stacked dynamic

bonding to such applications would provide many benefits including lower cost, improved reliability, lower power consumption, and higher thermal and electrical performance [4]. Historically, however, DBI has been only available in a W2W configuration. Shifting such a bonding technology platform to a D2W configuration, however, has implications such as a need to address increased particulates generated as a result of pre-bond wafer dicing and thin die handling.

Given the numerous advantages of W2W DBI, we have spent significant engineering effort to develop DBI[®] Ultra, a D2W hybrid bonding process that allows known good die (KGD) to be stacked. With the elimination of both the underfill layers and the accompanying die standoff,

this latest bonding process provides a pathway for increasing the number of die stacked from 4 and 8 high, to 12, and even 16 high, while meeting the stringent height requirements for various electronic applications. In addition, the availability of a dense interconnect solution in a high-yielding, D2W process opens up architectural possibilities in heterogeneous integration for 2.5D and 3D assemblies.

Development of D2W processing

DBI and DBI Ultra are bonding platforms that allow for interconnect densities down to 1μm in a W2W and D2W format, respectively. In the DBI Ultra process, as seen in **Figure 1**, the host and die wafers are chemically-

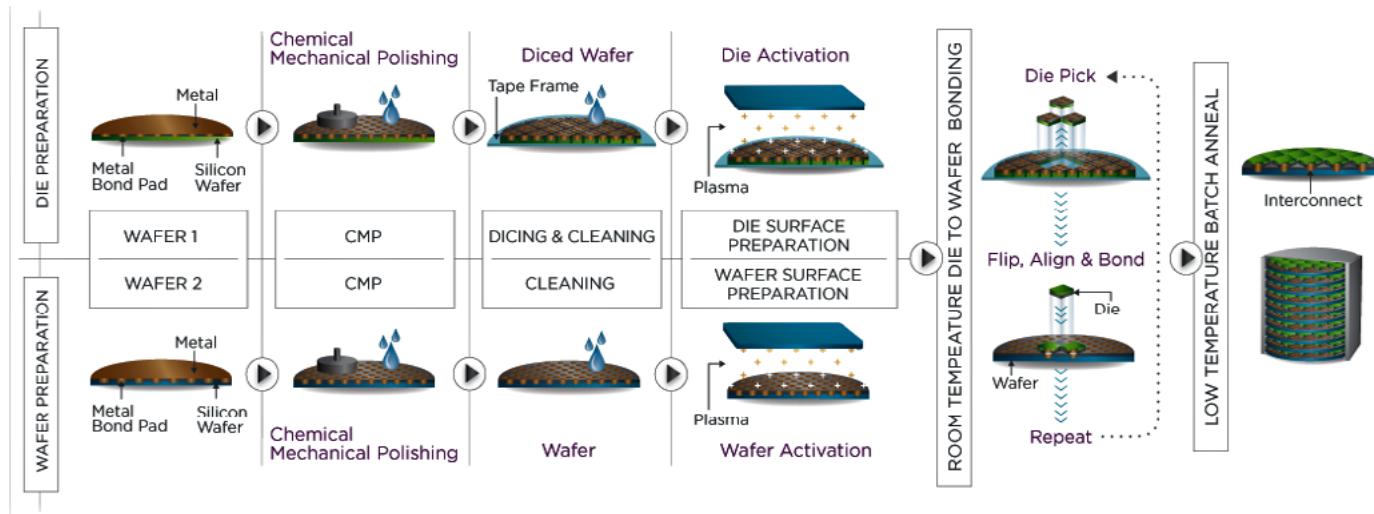


Figure 1: DBI Ultra process flow.

random access memory (3DS DRAM), manufacturers have been reluctant to adopt a W2W approach on account of the required changes in design, test and self-repair. Instead, manufacturers have focused on die to wafer (D2W) approaches, such as microbumps and thermocompression bonding (TCB). Such techniques have inherent limitations and require expensive and time-consuming underfill between die. Applying hybrid

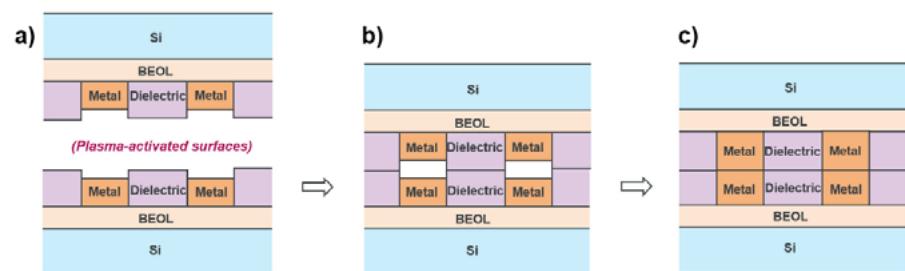


Figure 2: a) Bringing activated surfaces together; b) Instantaneous dielectric bonding upon contact; c) Metal joining during the anneal process.



mechanical polished (CMP), cleaned, and then activated. Wafers are then singulated and the resulting die are flipped and placed upon a host wafer. This flipping and placement is repeated until the host wafer is fully populated. Upon contact and at room temperature, the dielectrics bond as seen in **Figure 2**. A subsequent anneal process strengthens the dielectric bond and allows the interconnects to join.

DBI (Direct Bond Interconnect) was introduced by Ziptronix, an RTI spinoff, in the early 2000s. Starting with nickel as the interconnect metal in the mid 2000s, Ziptronix demonstrated the first copper-based hybrid bonded interconnects with 10 μm pitch in 2009. The company developed the technology for wafer-to-wafer applications and subsequently licensed it to Sony [5] in 2015 for the production of CIS in high volumes. Ziptronix was later acquired by Tessera Technologies, now XPERI and the technology has been licensed to many semiconductor manufacturers and suppliers around the world. Early efforts to produce a D2W hybrid bonding process were hampered by low yield due to a process sensitivity to particles and the propensity for singulated devices to have many particles.

A mere three years or so ago, the potential for die-to-wafer applications in 2.5D and 3D was understood, but the challenge of yield, testability and die handling remained a barrier. Since 2015, we have devoted significant resources to die-to-wafer process development and optimization and has since developed a high-throughput production-worthy process leveraging standard production tools and industry infrastructure. The main features of the current production-ready process are shown in **Figure 1**. With a cycle time approaching the “dry” pick and place time of a die bonder, this process is able to bond dies at a rate of thousands per hour, per layer, whereas TCB takes considerably longer on account of the temperature, pressure and dwell times needed.

Addressing stacking requirements of HBM

A prime candidate for DBI Ultra is HBM (high-bandwidth memory). Currently available in 4 and 8 high stacks [6], the industry trajectory is

to stack 12 [7] and even 16 high HBM stacks. A test vehicle for this approach is seen in **Figure 3**.

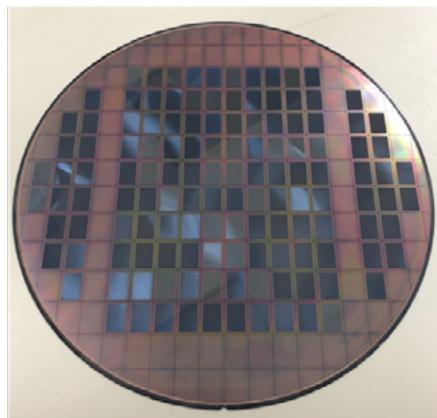


Figure 3: HBM test vehicle.

An additional benefit to the hybrid bonding approach in HBM structures is thermal performance, where the stack of die thermally behave as a single die [8]. **Figure 4** shows that with the conventional approach, the DRAM die in the center of a stack are less capable of dissipating heat as the die on the top and bottom. This effect is created by the thermal-insulating effect of several layers of underfill material. On the other

hand, if we compare this to a similar stack using hybrid bonding technology, as seen in **Figure 5**, greater thermal uniformity is observed. These analyses both assume thermal paths through an interposer and a heatsink with 2W of power per layer. With this DBI Ultra example, there is one-third the maximum-temperature rise compared with the conventional approach. More importantly, the die in the hybrid bonding approach are similar in temperature with each other, which helps to realize similar timing performance between

the die. The die in the stack are generally frequency throttled to accommodate the slowest (likely the hottest) die in the stack. In this case, hybrid bonding would allow for an increase in the operating frequency of the stack.

With the development of a production-worthy D2W process, taller stacks of HBM die are possible because the height of the microbumps is eliminated. With this approach, ultra-low-profile stacking of 16 die is now possible, as seen in **Figure 6**. Alternatively, with the existing thermocompression approach, the height of the copper pillars and underfill would not only increase the height of the stack, but also negatively impact its thermal uniformity. In the same manner that CMOS image sensors paved the way for DBI W2W bonding, HBM stacks are poised to pave the way for DBI Ultra D2W approaches and the resultant architectures.

Moving to true 3D design

While image sensors, RF, and memory applications are able to benefit from the DBI process in W2W and early D2W, there is significant applicability of D2W DBI in the system-on-chip (SoC) space. Depending upon the application, there are several ways that disaggregating

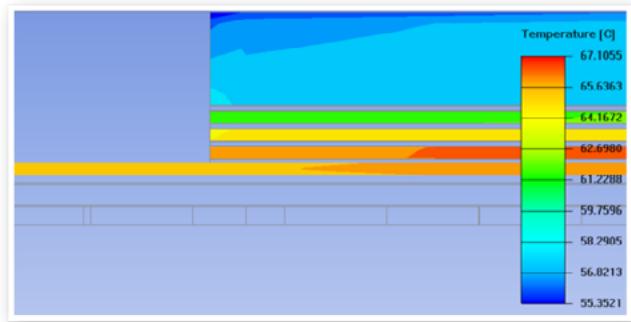


Figure 4: Thermal analysis of conventional 4-high HBM.

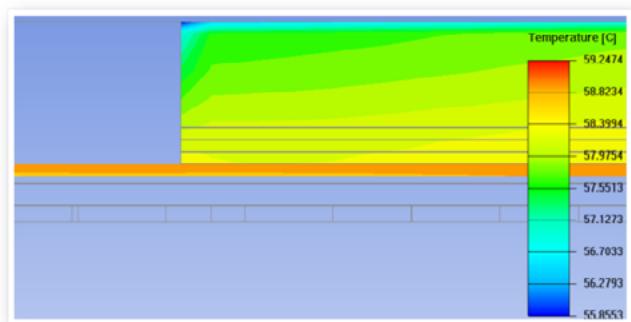
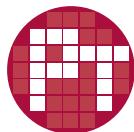


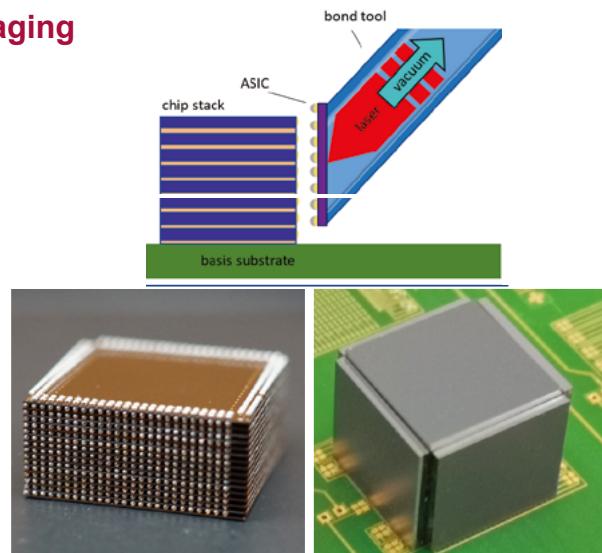
Figure 5: Thermal analysis of DBI Ultra 4-high HBM.



New Advanced Bonding Technologies

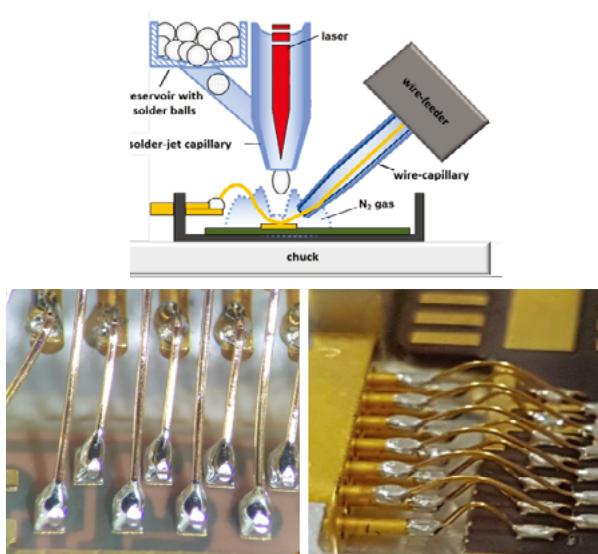
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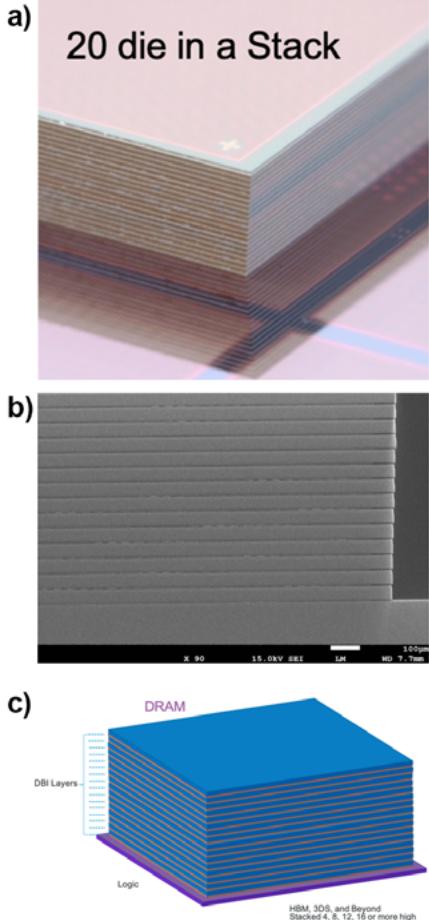


Figure 6: a) 20-high die stack; b) Cross section of a die stack; and c) DBI Ultra HBM representation.

an SoC with a D2W approach would not only increase memory bandwidth, but also improve performance. For example, having a SoC bonded with high-density DBI pads to a memory device would allow for more memory bandwidth than utilizing a HBM. This is achieved by having the potential for orders-of-magnitude more interconnects between the die. In addition, assuming that this was done without the need for a standardized memory interface, such as HBMx, low-power double-data rate (LPDDRx), double-data rate (DDRx), etc., there would then be a savings of area, power and latency by eliminating the need to have this interface serialize data, consume power and area.

Now, with DBI® Ultra availability, the need to match the size of the memory die and the SoC is no longer a constraint. Assuming the interconnect pitch between die can be made sufficiently fine-pitch, such as a 1-3 μ m pitch, these interconnects should be considered no different than interconnects

within a die. For example, if a SoC device is interfacing with a memory die, the interface between the die would be the same type of bus one would use if it were connecting two blocks on the same die.

If we consider a SoC with various blocks on the die as shown in **Figure 7**, where each block is 1mm by 1mm in size, we can see that the block in the center would be able to use all four edges to communicate with neighboring blocks. If we also assume

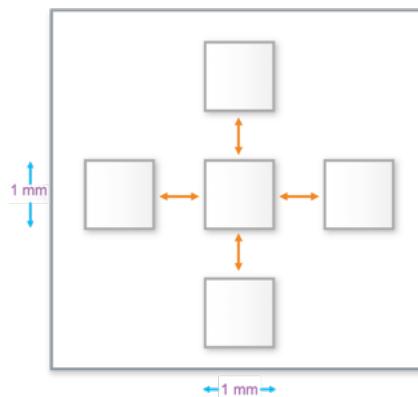


Figure 7: Block-to-block communication within a SoC.

that this die is in 10nm process technology with 4 signal routing layers (middle layers in the metal stack) of which two are north-south oriented routes, and two are east-west oriented routes, then we can approximately route 100,000 signal nets along this block's edges. Alternatively, if we were to consider a 3D approach with a 1 μ m pitch, then 1,000,000 interconnects would be achievable in this same area. Based upon this, we can conclude that more interconnects are possible across a dense D2D interface than would be between blocks within the same SoC. Furthermore, by not having to push the nets within these blocks to the periphery of the block, routing is reduced.

This may simplify timing closure at the block level. Less routing not only means lower latency, but also lower power dissipated in routes. With shorter routes, there are fewer repeaters needed as well, which drives down power and area further. The connection between the die should just be considered a trace, no different than a connection within a die, but shorter.

Having the potential for lower latency, less area, heterogenous process mix, lower power and higher performance simultaneously comes with one significant requirement. The design must be a true 3D design. Much of what is currently called 3D is just a stack of 2D designs. Just having through-silicon vias (TSVs) does not make for a 3D design. Instead, having signals that can cross a D2D boundary with a similar electrical load as would be seen in just moving between blocks within a die is key to a true 3D design. Many of the benefits of this 3D architecture are lost when an interface is inserted between these die that serializes the signals, like an LPDDR. Planning a design that spans more than one die, potentially more than one technology process and process design kit (PDK), and designing it concurrently allows for a sizable benefit that will exceed the area and performance savings of moving to a new node, at a considerably lower investment as well. A 15-20% performance benefit is often expected by advancing to the next node [9], but at staggering costs. There are also growing limitations on wiring because the wires do not scale with the nodes, thereby affecting the area benefits of moving to a new node. With a true 3D design, the wiring burden is reduced as signals do not need as much lateral movement, especially if the critical high-density connections are aligned well vertically. Furthermore, the lateral routing capacity is extended as there are routing layers available on both sides of the DBI or DBI Ultra interface.

If we consider a typical application processor architecture as shown in **Figure 8**, we see that there is a need

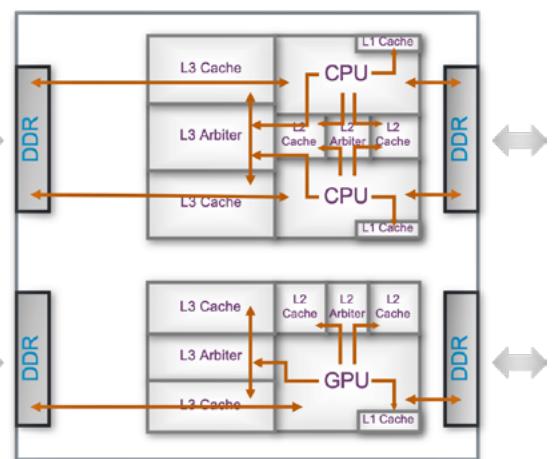


Figure 8: Cache hierarchy in a SoC.

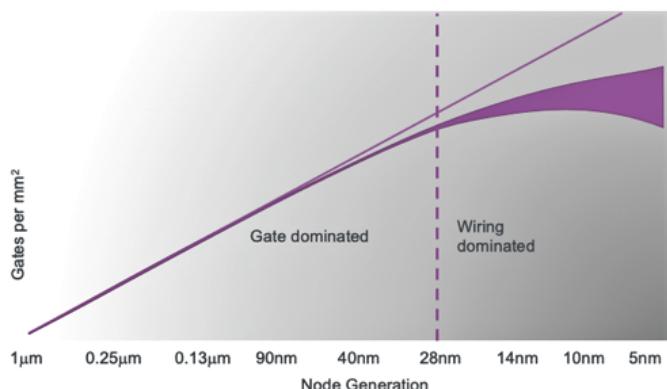


Figure 9: Gates per mm^2 with evolving nodes.

for multiple levels of cache in a die. The L1 cache is generally the smallest and integrated into a given processing unit. Once there is a need to move data from a processor to cache, a price in power is paid. This is especially true when there is a need to add a network on chip (NoC) or an arbiter to connect to many memories and/or processors. Instead, consider treating the memory in the adjacent die as if it were bonded or located on top of the same die, yet the routes will travel a shorter distance in the 3D case, given that they can route just a few microns between die, but would have to travel millimeters within the same die in a 2D situation. Using this mindset, a design can be envisioned with L1 cache completely over the processor, and L2 elsewhere. There is little need for L3 or external memory unless it is needed for storage capacity instead of low-latency bandwidth.

Historically, scaling transistor density predictably improved device transistor density with each new process node. For the last few nodes, starting around the 28nm node, however, this scaling factor was no longer linear. This was because a given high-performance design became routing-limited instead of transistor-limited. As seen in **Figure 9**, designs have not increased density in recent nodes because of this phenomenon. Instead, consider that in a dense DBI implementation, there is the opportunity to have far more routing layers because the routing can be shared between the face-to-face bonded die. This could pull the density scaling back to the original linear proportion and reduce area in designs using emerging nodes.

Test considerations

One question that often comes up is regarding test and KGD. In a W2W bonding scenario, there is little use for wafer probe prior to bonding as there is no simple way to eliminate bad sites, as the whole wafer will still be bonded. Some approaches

to alleviate this in a W2W environment, but none have been implemented effectively. Now, with the advent of DBI Ultra, there is the opportunity to assemble tested chiplets onto a tested host wafer utilizing only the good sites.

The fine pitch ($\sim 1\mu\text{m}$) interconnect used for these truly 3D designs would not accommodate probing. In addition, the probe mark left behind may make these pads unbondable. That said, there are two main approaches that can be used to get around this issue as discussed below.

Test a subset of pads. Leveraging test compression for built-in self-test (BIST), a significant portion of the device can be tested. These would not test the external interfaces unless there is a pre-drive loopback or something similar. The circuits that require the multiple layers of die to be bonded in order to complete the circuit would also not be available. The balance of tests performed at wafer probe through a BIST engine would be available through this reduced pad count. These extra pads can be accommodated in the DBI® Ultra process without an impact to the bonded interface.

Known good die. If the devices bonded together have a composite area less than the equivalent monolithically designed part, then the yield should be expected to be similar. In other words, assuming that defects are randomly scattered on the wafer surface, half the area will capture half the defects. As long as only the area and performance benefits are observed, and no more

is added to the 3D design than what was in the 2D equivalent, the yield should be similar, and testing prior to 3D bonding may not be necessary.

On the other hand, if the die are much larger, approaching the size of a reticle, then the composite yield of both die may be poor. Probing prior to bonding, leveraging DBI Ultra with KGD by testing a subset of pads, may make more sense.

Still, a better approach may be to leverage architectural improvements that take advantage of the closer proximity of compute elements enabled by DBI and DBI Ultra. Memory self-repair is widely used currently, but logical self-repair is not as broadly used on account of the timing requirements in an SoC. Blocks, such as processors, are large due to the efficiency of computing in a 2D layout [10]. This adds to the timing difficulty in large SoCs. In 3D, instead, the x-y area can be a fraction of that depending upon the number of die layers used, making them more densely packed and more suitable for having spare blocks for repair. Considering an array of compute elements arranged over an array of complementary elements, where microarchitectures are more densely packed, a repair would have a shorter reach and be more likely to fit within the necessary timing window for a usable repair. This can be seen in **Figure 10** where an array of processors (PRC) and memories (MEM) can be mapped such that a memory over a faulty processor can be remapped to a neighboring processor, and vice-versa. This is only effective if the mapping can be made within the same number of cycles, which is enabled by the close proximity of this logical repair.

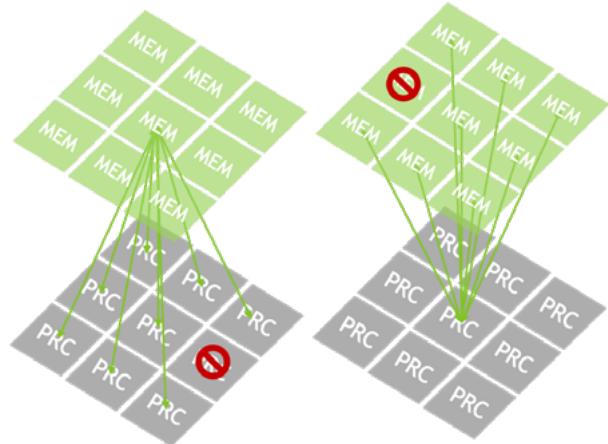


Figure 10: Self-healing methodology for co-designed arrays.



Summary

A new architecture that takes advantage of interconnect densities that rival the density within a die can have benefits in performance, area, yield and thermal efficiency. The hurdle to overcome is designing in 3D instead of stacking 2D designs. Elimination of the inefficient interfaces between die, and instead treating these connections as if they were connections within the same die, is what opens the door for these benefits. Furthermore, the ability to use DBI Ultra allows for dissimilar die sizes and testability makes this approach more accessible to applications in SoC devices.

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Biography

Javier DeLaCruz is VP of Engineering at XPERI Corporation, San Jose, CA, where he leads the architecture, design, and simulation team to develop and enable successful introduction of new technologies. He has over 20 years in the field, including work at eSilicon, STATS and MACOM. He also authored over 20 patents and holds a MS degree from Boston U., and an MBA from Babson College. Email: javi.delacruz@xperi.com

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The battlefields of fan-out packaging

By Favier Shoo, Santosh Kumar [Yole Développement]

In 2019, all the key outsourced semiconductor assembly and test suppliers (OSATS), foundries, and integrated device manufacturers (IDMs) have fan-out (FO) packaging solutions in the market. In a mega-trends-driven era, fan-out platforms are viewed increasingly as one of the top options among leading package technologies. Inevitably, key players with different business models are penetrating and competing in the same market space with different FO technologies and strategies. This has resulted not only in an increasingly divided market from high-end to low-end applications of FO packaging, but also an unavoidable battle of cost vs. performance trade-off between panel-level vs. wafer-level processing.

Market perspective on fan-out packaging

Fan-out packaging market value is expected to grow at a 19% compound annual growth rate (CAGR) from 2019-2024 (Figure 1), reaching a market size of \$3.8B. Core FO market confirmed its stability with substantial new entrants joining via fan-out panel-level packaging (FOPLP). Although existing FOWLP players have a long history of established qualifications, mid-end devices may be too costly for FOWLP players [1].

Amkor Portugal (NANIUM, S. A.) and JCET Group (STATS ChipPAC) used to have almost 80% of the market prior to 2016, thanks to their strong start with embedded wafer-level ball grid array (eWLB) FOWLP. Furthermore, with a strong track record of FOWLP production maturity and time-to-market, FOWLP technology has proven its quality and gained trust from customers. The situation changed drastically with the entrance of TSMC with integrated fan-out (InFO), which attained more than 50% of the market in 2017, thanks to Apple A10, A11 and A12 packaging. These products have become the high-end benchmark of FOWLP technology.

Fan-out success and growth are well-confirmed in the “core” standard FO market and made possible in the high-density FO (HDFo) market as well. Consequently, numerous other FO providers are trying to enter the game and the competitive landscape is changing (Figure 2).

For core FO, the current FOWLP installed base is enough to sustain existing demand. There was no significant expansion for existing end-products in 2018, while fabless continued to push packaging houses for mid-end to high-end applications at a lowered cost. In core FO, existing players are expected to go

on a cost competition between wafer level vs. panel level. Especially within OSATS, the player who can capture the market share of mid-end applications for mobile and automotive will lead the way and set new standards. Panel players have a great chance to secure mid-end device business at the lowest cost possible. SEMCO has proven FOPLP device qualification with ePLP package-on-package (PoP) [2]. At the same time, Powertech Technology Inc. (PTI) has a big ambition to expand new FOPLP fabs to capture existing or new business in the market. ASE/Deca are in preparation for Qualcomm's

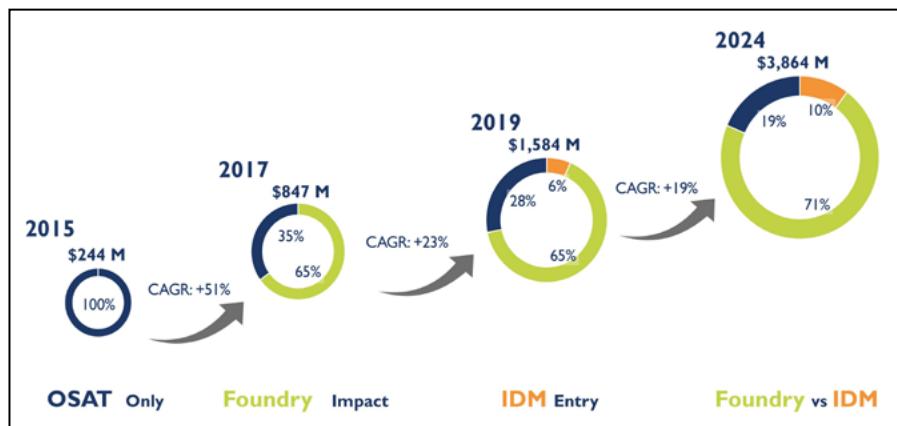


Figure 1: Fan-out market: business model evolution. SOURCE: [1]

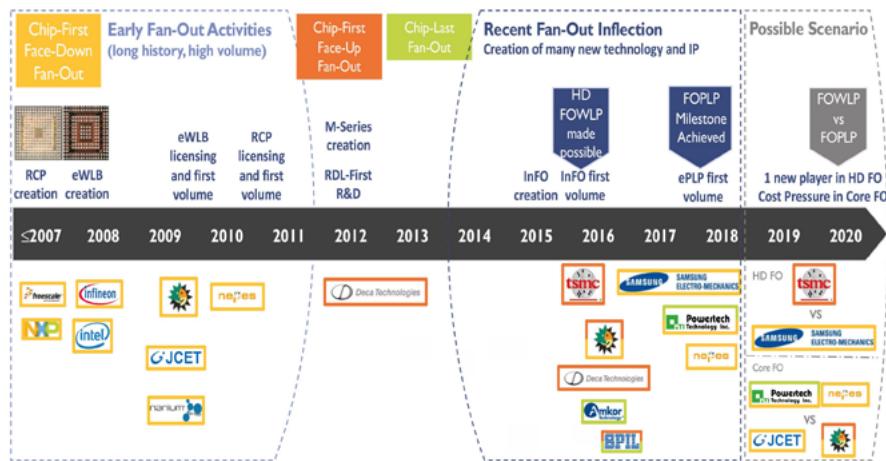


Figure 2: Fan-out packaging progression. SOURCE: [1]

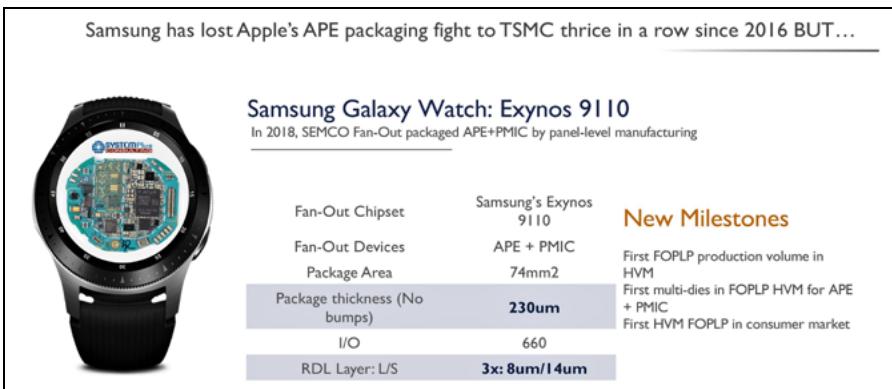


Figure 3: What about Samsung's fan-out solution? SOURCE: [1]

business. STATS ChipPAC and Amkor Portugal remain strongholds in eWLB. The core FO market, therefore, will move progressively forward in all likelihood.

In 2016, TSMC penetrated FO packaging with high-end applications in mobile application processor engines (APEs) and high-performance computers (HPCs) in networking. This has created a new market, the HDFO market, where TSMC is still the only dominant player. Significant growth is expected with InFO technology for advanced mobile and high-end computing demands in this mega-trend driven era. TSMC is therefore expected to ramp-up InFO further and potentially double the current capacity. Consequently, HDFO is dominated by APE sales and volume, with a small portion of low-volume manufacturing (LVM) qualification for HPCs mainly supplied by TSMC. There was still no other contender in HDFO in 2018. This market is riskier because some considerations and leverages go beyond packaging, and in fact, involve both front-end choice and complicated politics between key players, etc. With such new market growth, FO packaging is set to gain a significant share of the market from either advanced substrate (by InFO) or interposers (by InFO-memory on substrate) [3].

Fan-out technology evolution

Fan-out packaging technology is not only a bridge to chip-package interaction (CPI) mismatch in pitch size, but is also a viable solution for heterogeneous integration of functionalities in a desired package dimension and design, potentially for mmWave 5G and Cloud data server applications.

Chip-first fan-out solutions are still well established in the market. Since 2009,

eWLB has been the most famous FO technology in the core market. Its long history and device-proven qualification have provided customers with confidence and is continually being adopted. It is considered a mature process for single-die packaging and potentially a good solution for system-in-package (SiP), with products that embed several active dies and numerous passives already available.

As there are several licensees, multi-sourcing is possible. This is key for supplying end-customers, especially for those with high-volume needs such as the handset market. Redistributed chip packaging (RCP) technology has better performance in terms of die shift, and consequently easier photolithography steps, as well as better resolution. However, it has suffered from a lack of licensees and cost competitiveness as compared to eWLB. Although it had some success thanks to the NXP portfolio, it is progressively disappearing.

TSMC maintained technology leadership in HDFO and extended it even further with high-volume manufacturing (HVM) InFO package-on-package (InFO-PoP) for Apple's latest APEs. In addition, TSMC is rolling out InFO on substrate (InFO-oS) for high-performance devices in HPC applications. Fan-out antenna-in-package (FO-AiP) has gained the interest of FO players because FO has well-known capabilities in core radar. Also, with FO, the embedded RF chip will suffer less interference. In this manner, a new performance value can be generated for FO-AiP. Also, FO packaging adopting memory on substrate is possible with TSMC and potentially PTI. This will become an alternative to 2.5D interposers.

The key technical benefit of FOWLP is the ability to integrate dies together flexibly, while remaining thin. It can displace 2.5D interposers with fine

L/S FO packaging on substrate and can also displace flip chip and advanced substrate. As an example, in the case of the APE market, TSMC's InFO-APE has replaced advanced IC substrate in all the latest iPhones, which is significant. Fan-out (InFO) has taken more than 13% of the mobile APE market from advanced substrates in just 3 years—such is the potential of this technology. FOWLP continues to cannibalize from, and jeopardize, advanced substrate makers, pushing them out of business. FOWLP on substrate is another special case. In this case, the fan-out package is flipped over onto a substrate and therefore a substrate manufacturer is added to the supply chain. In such a situation, the FO packaging cost is comparable to flip chip, but the competing platform is 2.5D, not flip chip. The savings come from the removal of the Si interposer.

Nepes, SEMCO and PTI have successfully invested in and developed FOPLP for production in 2018. New panel-level fan-out (PLFO) production is still immature. Nepes is entering LVM with analog/mixed integrated circuit (IC) and fingerprint sensor packaging. There is HVM production by SEMCO for Samsung's Galaxy smartwatch (**Figure 3**), and LVM production by PTI for MediaTek's automotive applications. Moving forward, the next challenge is expected to process good development yield for HD FOPLP production.

Technical consortia also see opportunities, such as the new materials, tools, and processes involved in scaling from wafer to panel size. Material and equipment suppliers want to join consortia with research institutes like Fraunhofer IZM and A*STAR IME to prepare themselves for the challenges in case FOPLP takes off.

Clearly, PLP must create a new production infrastructure, as front-end equipment cannot be reused for this purpose. PLP can leverage WLP knowledge and infrastructure and use it on printed circuit board/flat-panel display (FPD)/photovoltaic industry equipment. This is not simple, as it needs some reengineering, but it is happening.

Supply chain

For commercialization of FOWLP packages, the established OSATS are ASE, Amkor Portugal (NANIUM S.A.), JCET (STATS ChipPAC and JCAP), Deca and nepes. OSATS that are pursuing FO packaging capabilities are Amkor Korea, ASE/Deca, Huatian, and SPIL. More OSATS are becoming involved in

FOWLP; they are the main contributors for core FO and are all targeting volume production though still with different developmental status [1].

The FOWLP supply chain is simpler and controlled by experienced players in the semiconductor industry, but it requires collaboration at the design level, in contrast to flip-chip ball grid array (FCBGA). FOWLP involves simplification and consolidation of the packaging, assembly and testing in a “middle-end” type of infrastructure, where the cost of production is essentially at the wafer fab. For example, FCBGA needs substrate supplier, wafer fab RDL, wafer bump, and assembly and testing, while FOWLP only needs assembly, wafer fab RDL, wafer bump and testing. There is a shift in the value chain created by FOWLP.

TSMC has been the sole contributor of HDOF since 2016 and has adopted a unique strategy. It is not only an advanced foundry for the front end (FE), but also a high-end packaging house for the back end (BE). This business model will continue to lead the way to create new value and breakthroughs. With TSMC’s InFO being able to package high-end APE for Apple’s iPhone, a new market, HDOF, was generated. InFO-oS technology is now being utilized for HPC in LVM, InFO-MS (memory on substrate) has been developed for servers and InFO-AiP for 5G.

Many package technologies can be considered as PLP, but it is FOPLP that is attracting the most attention because of the success and awareness of FOWLP. This attracts players with many different business models, including OSATS, integrated device manufacturers (IDMs), foundries, substrate manufacturers and flat-panel display (FPD) players.

They sense an opportunity to enter the advanced packaging business via fan-out technology. These players include those who missed the early FOWLP wave with eWLB technology. For example, PTI, ASE, SEMCO and Unimicron were affected by losses in the substrate business of more than \$100M each year. Therefore, they want a new business model that utilizes their experience in substrate manufacturing. Other potential entrants include companies that already have experience in panel processes, for example, liquid crystal display (LCD) packaging, and believe they can leverage this for PLP, like nepes, or those that want to develop high-density, low-cost packaging to support their front-end chip business, like Samsung Electronics and Intel.

SEMCO is the next biggest FO contender, being part of Samsung Electronics (IDM). Samsung has been instrumental in design, memory, logic, packaging, chipset assembly and end-product and can, therefore, drive breakthroughs internally. SEMCO, being part of the Samsung group, is pressured to develop differentiated yet cost-effective technology. In 2018, SEMCO achieved a new milestone by rolling out AP+PMIC devices with FO embedded panel-level packaging (ePLP) PoP technology for the Samsung Galaxy Watch. SEMCO will continue to innovate for a cost-effective HDOF market space in order to compete with TSMC for Apple’s packaging and FE business again. In years to come, SEMCO’s HDOF is expected to be utilized first in Samsung’s smartphones. Besides, a reorganization between SEMCO and Samsung Electronics could be beneficial for Samsung’s position as a full turnkey provider for a FE+BE bundle.

This will be a direct battle against TSMC fighting to be the supplier for Apple’s APE die and packaging business.

Currently, PTI has successfully secured MediaTek’s business in automotive radar applications. Qualcomm and MediaTek will continue to request mid-end to high-end devices at lower price from OSATS. With new mega-trend applications requesting more functionalities and shorter routings, a larger package with multi-dies like processor+memory is ideal. PTI is a good choice for fabless/IDMs/foundries because PTI is already a specialist in memory packaging and a driver in FOPLP. PTI is investing \$1.6B in a new FOPLP fab and we can expect PTI to emerge as a cost-effective leader in FOPLP technology for core FO in the years to come.

Summary

It can be concluded that opinions are still divided, and strategies are different in this new age digital era. Clearly, fan-out packaging is growing strongly in a landscape that is more fragmented than ever. Consequently, different levels of battles are unfolding in both the core FO market and the HDOF market.

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Biographies

Favier Shoo is a Technology and Market Analyst in the Semiconductor & Software division at Yole Développement (Yole), member of Yole Group of Companies. Based in Singapore, he is engaged in the development of reports as well as the production of custom consulting projects. With prior experience at Applied Materials and REC Solar, he developed a deep understanding of the supply chain and core business values. Being knowledgeable in this field, Favier has conducted professional training for industry players and obtained two patents. He was also the co-founder of a startup company. He holds a Bachelor’s degree in Materials Engineering (Hons) and a minor in Entrepreneurship from Nanyang Technological U. (NTU), Singapore. Email: shoo@yole.fr

Santosh Kumar is a Principal Analyst and Director Packaging, Assembly & Substrates, Yole Korea, a member company of Yole Développement (Yole). Based in Seoul, Santosh is deeply involved in the market, technology and strategic analyses of the microelectronic assembly and packaging technologies and presents his vision of the industry in numerous conferences, as well as through papers and patent publications. His main interest areas are advanced IC packaging technology including equipment and materials. He is the author of several reports on fan-out/fan-in WLP, flip-chip, and 3D/2.5D packaging. Santosh Kumar received Bachelor’s and Master’s degrees in Engineering from the Indian Institute of Technology (IIT), Roorkee, and U. of Seoul, respectively.



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Advanced packaging carriers for WLFO applications

By Jay Zhang, Yu Xiao, Andy Teng, Indrajit Dutta, Varun Singh [Precision Glass Solutions, Corning Incorporated] and Lei Yang, Ming Li [ASMPT]

Fan-out wafer-level packaging (FOWLP) has been around for many years with embedded wafer-level ball grid array (eWLB) being the most well-known solution in the industry. Applications of FOWLP reached a new phase in 2016 when TSMC's integrated fan-out (InFO) platform was commercialized to address application processor (AP) uses in a mobile phone. For such higher-end applications, a glass carrier becomes the preferred choice during the FOWLP process for the following reasons:

- Glass can deliver a wide range of precise coefficients of thermal expansion (CTEs) in fine granularity to match different fan-out (FO) ratio and epoxy molding compound (EMC) properties.
- Glass enables stress-free laser debonding;
- Glass wafers can deliver very low total thickness variation (TTV);
- In some cases, glass offers a very smooth surface to deposit fine redistribution layer (RDL) features; and
- Glass can often be reused multiple times.

As the industry matures, more sophisticated packaging structures are being considered, and the FO process is also becoming more complex. In many high-end applications, yield is key to product and business success, and a high-yield process often demands new and improved materials to deliver superior performances. Warp control is key in any FO applications, and a glass carrier plays a critical role in managing warp throughout the FO process.

Why is warp so important in a typical FO process? Warp impacts how a wafer behaves with various process tools. For example, spin coating

and EMC backgrinding both rely on vacuum chucking for proper operation. Vacuum chucking depends on the wafer being sufficiently flat. Another example is physical vapor deposition (PVD), such as metal adhesion layer and Cu seed layer deposition using sputtering. In these cases, wafer flatness ensures proper heat sinking, and thereby film thickness and property uniformity. Some lithography steps also require that the top surface is flat within the depth of focus of the lithography system, and bad warp could lead to improper feature definition and development. A rule of thumb is that throughout the FO process, being able to control warp to be <1mm is a good practice [1].

Levers to control warp

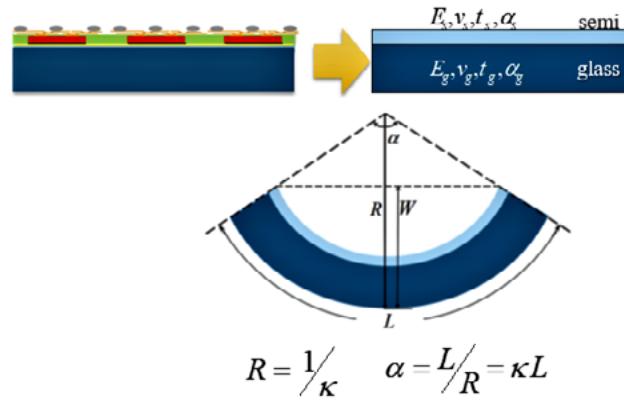
We begin by first developing the fundamental understanding of how FO processes generate warp. To model warp, we consider a typical FO structure as a bi-layer in which the bottom is the glass carrier, typically 0.5-1.2mm in thickness. The top of the structure is a combination of materials that are added as the FO process progresses. For example, in a typical chip-first scenario, dies are placed on an adhesive film, followed by EMC molding, EMC backgrinding, RDLs, and finally, bumping. At any process step, we can picture the added composite layer as a single layer with an average property of the constituting materials. As shown in **Figure 1**, let us

call that a semiconductor layer and use subscript *s* to designate the material properties of this layer, E_s for Young's modulus, t_s for the layer thickness, ν_s for Poisson's ratio, and α_s for thermal expansion coefficient. For the carrier glass, we use subscript *g* for the same parameters accordingly.

Assuming the bi-layer is fabricated with no stress at process temperature of T and then returns to room temperature, and we further assume that CTE mismatch is the dominant stress-producing mechanism, the resulting warp in the simplest form is expressed as:

$$\text{Eq. 1} \quad W = R \left(1 - \cos\left(\frac{\theta}{2}\right) \right) = \frac{1}{\kappa} \left(1 - \cos\left(\frac{\kappa L}{2}\right) \right) \\ \approx \frac{3L^2(\alpha_s - \alpha_g)(T_{\text{process}} - T_{\text{room}})(t_g + t_s)t_g t_s}{4 \left[\frac{E_g(1-\nu_g)}{E_s(1-\nu_s)} t_g^2 + \frac{E_s(1-\nu_s)}{E_g(1-\nu_g)} t_s^2 + 2t_g t_s (2t_g^2 + 3t_g t_s + 2t_s^2) \right]}$$

It is clear that ΔCTE and ΔT are both linear in contributing to warp. If CTE can be perfectly matched, or the fabrication process is at room temperature, we should expect no warp. In reality, the FO process adds



$$R = \frac{1}{\kappa} \quad \alpha = \frac{L}{R} = \kappa L$$

E: Young's modulus; *v*: Poisson's ratio; *t*: Glass thickness;
α: Coefficient of thermal expansion; *T*: Temperature.
g: glass; s: semiconductor layers (MC + redistribution layers + die)

Figure 1: Model of warpage in a typical fan-out structure.

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materials and develops patterns in some layers, and the average CTE of the semiconductor layer is a constantly evolving parameter. Many of the FO processes also happen at elevated temperatures: polyimide (PI) curing, EMC molding, EMC curing, etc. Given the evolving nature of average CTE, there is no perfect match for a carrier, and a carrier CTE needs to be chosen to control the warp throughout the FO process to be smaller than a certain threshold.

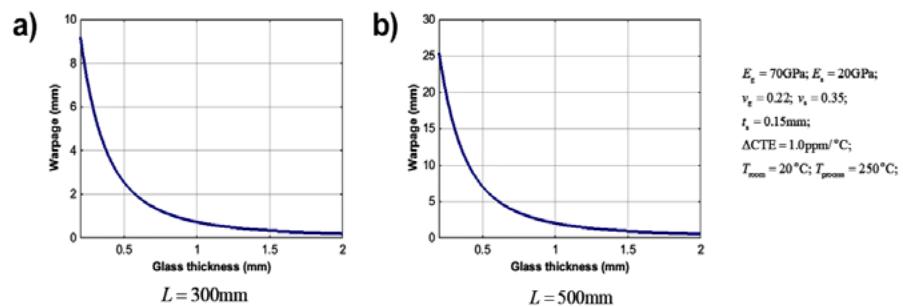
How the other carrier characteristics impact warp is embedded in the formula (Eq. 1). To more clearly see the relationship, we can make some further simplifications. If we assume the semiconductor layer is significantly thinner than the carrier, the second and third terms in the denominator of the warp formula can be ignored in comparison to the first term, and the warp expression becomes:

$$\text{Eq. 2} \quad \approx 0.75L^2\Delta\alpha\Delta T \frac{E_g(1-v_g)t_s}{E_g(1-v_s)t_g^2}$$

Here we can see the additional trends clearly. Under the conditions stated above, the warp is inversely proportional to the carrier's Young's modulus (YM). The warp is also inversely proportional to the square of the carrier thickness. Indeed, when we use the typical conditions encountered in FO and plotted out the warp as a function of carrier YM and carrier thickness, we see this trend in Figures 2-4.

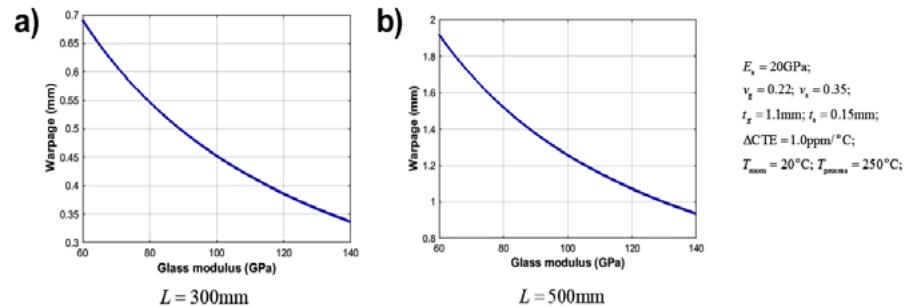
Figure 5a combines the effect of ΔCTE and YM in a 3D plot. It clearly shows the linear relation to ΔCTE; and for any ΔCTE, it also shows that a higher Young's modulus can reduce warp effectively.

Figure 5b shows iso-warp lines on a ΔCTE vs. warp plot. The purple triangle is meant to illustrate how YM can impact ΔCTE tolerance. When maximum allowable warp is 250μm in this example, a glass carrier with 60GPa YM can only tolerate a ΔCTE of ~0.35ppm/°C. If one were to engineer a glass carrier with 140GPa YM, tolerable ΔCTE would increase to ~0.8ppm/°C. Such scenarios could be needed as future FO packages involve more layers and a broader materials set, and glass has the potential to meet such high YM values.



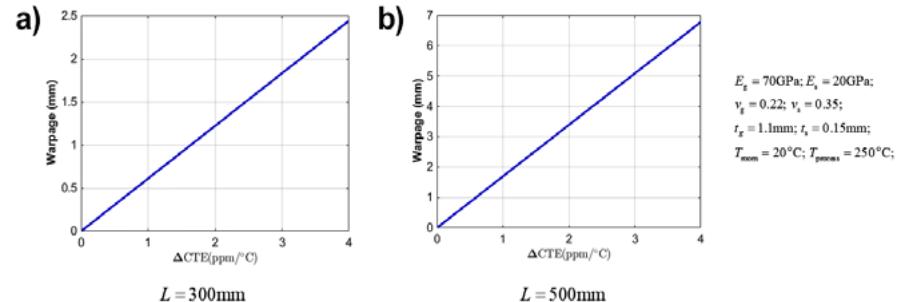
Warp is inversely proportional to carrier thickness squared, but returns diminish beyond 1mm

Figure 2: Warpage as a function of glass thickness for: a) L=300mm, and b) L=500mm.



Warp is inversely proportional to the Young's modulus of the carrier

Figure 3: Warpage as a function of the glass Young's modulus for: a) L=300mm, and b) L=500mm.



Perfect CTE match is desirable, but often not possible due to different CTE materials added

Figure 4: Warpage as a function of ΔCTE(ppm/°C) for: a) L=300mm, and b) L=500mm.

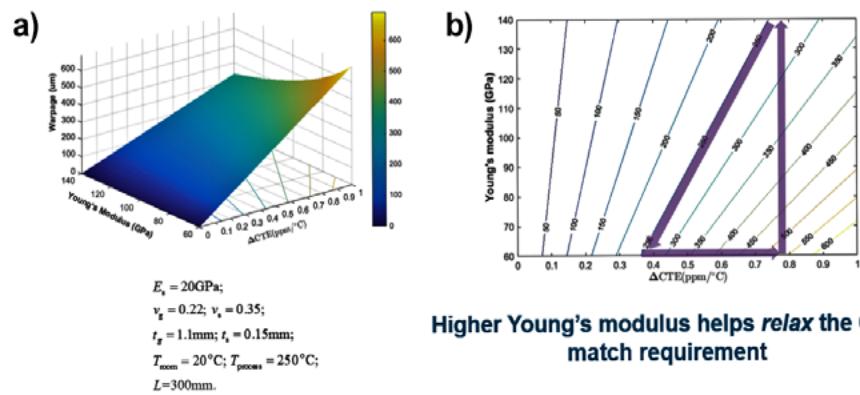


Figure 5: a) Effect of ΔCTE and Young's modulus on warpage for L=300mm; b) The purple triangle illustrates how Young's modulus helps relax the CTE match requirement

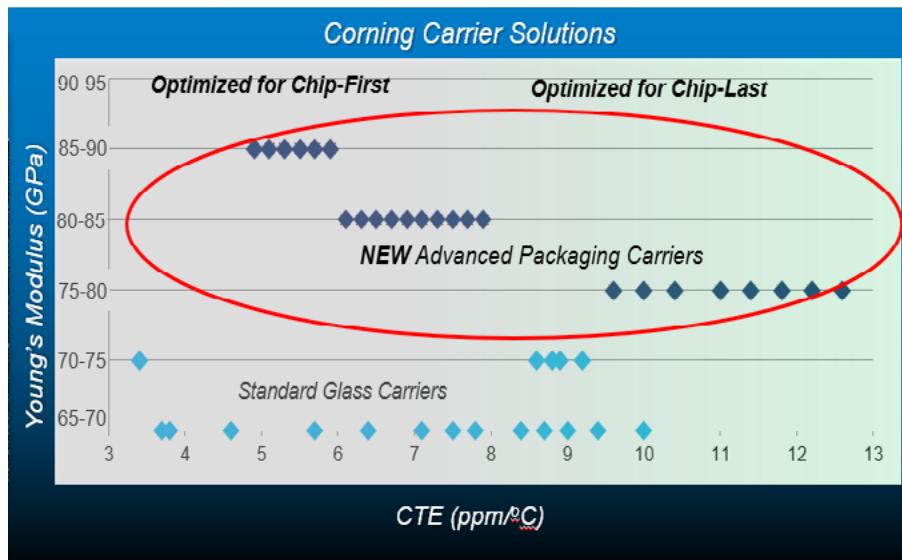


Figure 6: APC's CTE and Young's modulus coverage with existing carrier products.

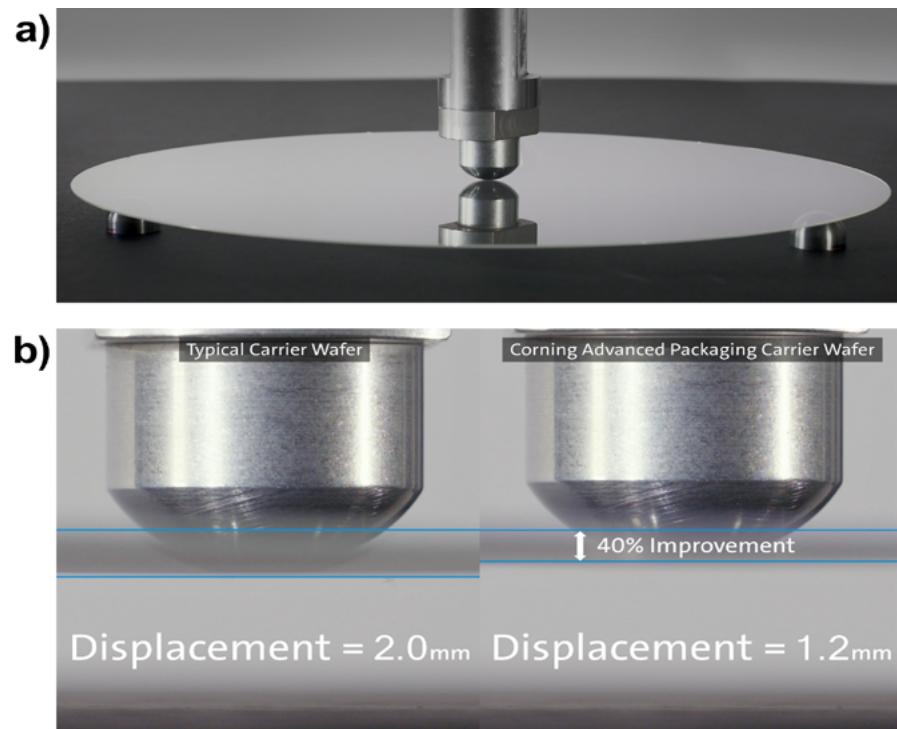


Figure 7: a) (top): Load vs. deflection setup: the glass wafer is supported by three steel balls near the wafer periphery; and b) Deflection of the high Young's modulus wafer is ~40% lower when the glass' Young's modulus is ~40% higher.

Glass considerations

The discussions above focused on three levers for a glass carrier to help manage warp. We discuss specific requirements and constraints for each of the three below.

CTE is the most important attribute. A typical EMC has a CTE of 7-10 ppm/°C, and Si has a CTE of ~3 ppm/°C. A different FO

ratio in the molding stage requires a carrier to have a CTE in the range of ~5-10 ppm/°C in order to manage warp during this important step of the FO process. Although the carrier CTE is often chosen to manage warp in the whole FO process, rather than one particular step, the optimal choice often requires accuracy down to +/- 0.1 ppm/°C. An ideal carrier

wafer supplier needs to offer carriers covering the entire CTE range with granularity down to ~0.2 ppm/°C. While glass scientists have shown technical feasibility of having CTE values in the negative to >14 ppm/°C, to have so many stock keeping units (SKUs) could be a business challenge.

Young's modulus is an effective lever to control warp. When a perfect CTE match is not possible because the evolving nature of the FO stack-up, YM is an effective lever to control warp. While popular glass compositions typically show YM in the 65-75 GPa range, highly technical glass can exhibit a YM as high as 140 GPa. Whether one should go to that extreme is another question. There are definitely risks associated with a YM being too high. This is especially true when the FO industry is still in its infancy, and using glass is still a challenge to many users in this community. One risk that is being studied is thermal stress. When a carrier wafer encounters a thermal gradient, be it through thickness or across the wafer, ΔT leads to thermal strain, and thermal strain leads to thermal stress with YM being the multiplier. If YM is too high, the same ΔT could generate too high a thermal stress, causing wafer breakage. This is particularly risky when a high CTE is involved.

Carrier thickness is another lever available to the FO developer. The thickness squared relationship makes it highly effective in controlling warp, especially in the 0.5-1 mm range. The constraint with respect to thickness is total available Z-height in the equipment set through which a FO package goes. While equipment modification is an option, we find most customers prefer to use an existing tool set and limit the carrier thickness to allow room for the package itself. A popular carrier thickness range is 0.5-1.2 mm in Corning's experience.

Other considerations

We discussed previously the need to cover a wide CTE range with fine granularity. While this may suit the need of an R&D group, the manufacturing group will further demand that during mass production,



Figure 8: Demonstration of warp impact on vacuum chuck performance.

the same CTE glass carrier will show stable and consistent material properties. A nightmare scenario would be for R&D to receive samples from a glass supplier that makes such samples using an R&D tool, and the manufacturing side would receive very different materials after spending precious resources qualifying the experimental material.

Another common complaint from the FO R&D side is long lead times for samples. If a request for a new CTE takes a few months to be filled, impact on the product development cycle could mean the loss of new business to a competitor. If a glass carrier wafer supplier can deliver small quantities of various CTE samples within weeks of time rather than months, it brings significant value to its customers.

Results

Corning Advanced Packaging Carriers (APC). As a result of understanding the warp drivers and in response to market demand, Corning has introduced a new product line – Corning Advanced Packaging Carriers (APC). This new product line covers CTEs from 4.9 to 12.6 ppm/ $^{\circ}$ C with 0.2-0.3 ppm/ $^{\circ}$ C granularity and enhanced YM values. The chosen YM values reflect an ~20% improvement over what is on the market and deliver warp performance without increasing customer risks in thermal stress-induced breakage. **Figure 6** shows APC's CTE and YM coverage with the existing carrier products listed for comparison. When higher YM benefit is combined with that from fine granularity, a customer might achieve up to 40% improvement in warp.

Demonstration of value of high stiffness. A high YM results in high stiffness in the carrier resisting bending under typical FO process conditions. We show two demonstrations below.

In the first demo, we use two wafers of identical thickness but vastly different YM values. We support the wafers using three steel balls near the wafer periphery. A push-down hemisphere deflects the wafer at the wafer center while both the down-force and wafer deflection are recorded. **Figure 7** shows that deflection of the high YM wafer is ~40% lower when the glass YM is ~40% higher, in agreement with theory.

In the second demo, we laminate a high-modulus polymer film to a glass carrier wafer to introduce a predictable amount of bow. When the same film is laminated to a high-YM wafer and a low-YM wafer, we reach warp value of ~0.8mm in the former case, and >1mm in the latter case. When the low-warp wafer is placed on a vacuum chuck, shown in **Figure 8**, the wafer is properly chucked under vacuum and it does not spin on the vacuum chuck. The high-warp wafer exhibits a completely different behavior: it does not chuck properly, and one can easily spin the wafer even when the vacuum chuck is turned “on.” This demonstration confirms the industry’s rule of thumb: keeping warp below 1mm is a good practice. Further, the demo clarifies an instinct-based misconception that the YM effect cancels out during vacuum chucking – the lower warp sample is harder to chuck on account of the higher YM. The truth is: warp <1mm allows proper chucking for a wide range of YM values. High warp would lead to improper chucking even when the YM is

near the low end of the typical range for glass, or ~60GPa.

Warp shape and bifurcation. Multiple publications, e.g., [2], have shown warp results that are somewhat counterintuitive. In many FO configurations, even though the chip shape and layout are both symmetric in nature, the warp appears to be elliptical or cylindrical in shape. It turns out this is a well understood phenomenon in plate theory [3]. When stress applied to a plate exceeds a certain threshold, the shape of the resultant warp will undergo bifurcation: the spherically symmetric warp at low applied stress with a single curvature splits into two stable curvatures, and the shape becomes elliptical above this threshold stress level. Further increase in stress will eventually cause the shape to be cylindrical with one single curvature. This phenomenon is illustrated in **Figure 9**.

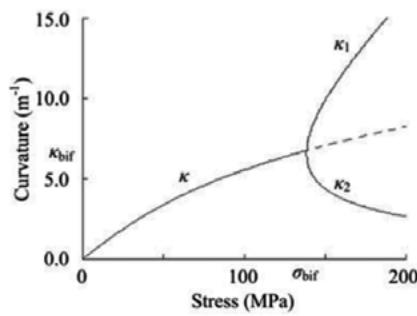


Figure 9: Effect of stress on curvature.

Because one of the curvatures is now greater than if the shape were to follow the original spherical shape, maximum observed warp tends to increase, causing potential issues in the FO process. For this reason, we must understand how carrier material properties and carrier geometry impact the bifurcation threshold. Because of the complexity involved, this paper will not discuss details of the fundamental understanding. What is clear is that the threshold condition for bifurcation is a function of carrier size and thickness: the larger the size and the thinner the wafer, the more prone to bifurcation the carrier becomes. Bifurcation is also impacted by the carrier’s YM: the lower the YM, the lower the bifurcation threshold.

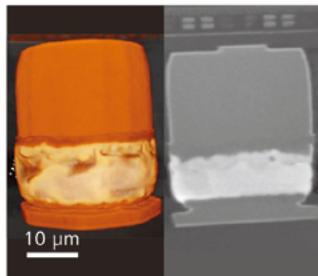
To demonstrate the bifurcation phenomenon, we use a configuration where relatively thick Si chips and EMC layers are used on a glass carrier. The

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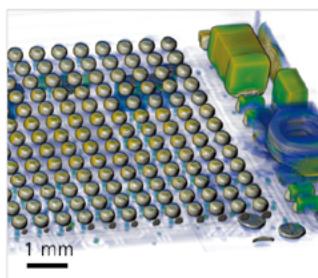
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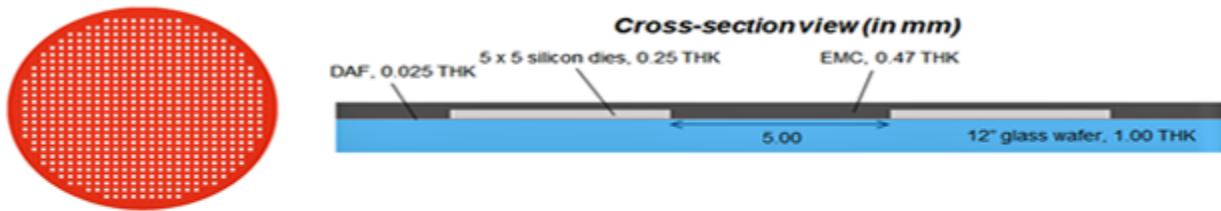
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a) Top view showing die arrangement



	Silicon	EMC	DAF	Typical glass wafer	Corning APC wafer
Young's modulus (GPa)	Orthotropic	19.0	2.3	73.2	92.6
Poisson ratio	Orthotropic	0.25	0.40	0.23	0.26
CTE (ppm/ $^{\circ}$ C)	2.56	10.00	120.00	8.30	8.32
Density (g/cm ³)	2.33	1.00	1.00	2.40	2.42

b)

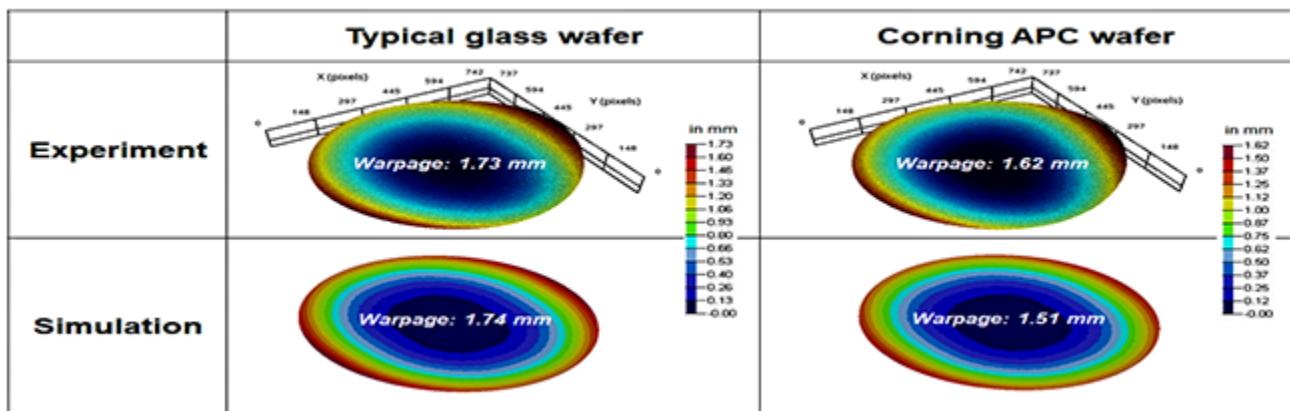


Figure 10: a) (top, including the table) Si chip configuration and material properties; b) (bottom) Experimental and simulation results demonstrating warp bifurcation.

detailed material and configurational parameters are indicated in **Figure 10**. It can be seen that the warp is in an elliptical shape even though the chip layout is more or less symmetric. Experimental data support the theoretical prediction even though the warp magnitude is not in complete agreement.

Summary

In summary, FO is a fast-growing field with high-end implementations requiring high-performance glass carriers. We discussed both technical and business requirements based on fundamental understanding and experience in the field. In response to market demand, Corning's APC offering not only covers

the desirable CTE range, but also does so with 0.2-0.3 ppm/ $^{\circ}$ C granularity. All the APC products offer a high Young's modulus without introducing risk in thermally-induced breakage.

Acknowledgements

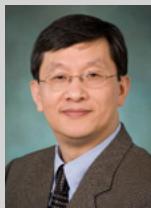
Corning's Drs. Lisa Lamberson and Bob Morena contributed to the realization of high Young's modulus glasses covering a wide CTE range in fine granularity. We thank Kaitlin Cutler of Corning in providing editorial support to this article.

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Biography

Jay Zhang is Business Development Director at Precision Glass Solutions, Corning Incorporated, in Corning, New York. He earned a PhD in applied physics from Yale U. and an MBA from Cornell U. He has been working at Corning for 18 years and holds five U.S. granted patents with Corning. Email: zhangjj@corning.com

Lei Yang received BSc, MSc and PhD degrees in Materials Science and Engineering from Harbin Institute of Technology, Harbin, China. He is a Senior Process Engineer with ASM Pacific Technology Ltd., Hong Kong. His current research interests include fan-out wafer level packaging technology, TCB technology, and modeling for microelectronics packaging assembly.

Reliability physics analysis (RPA) of semiconductor packaging

By Gil Sharon, Nathan Blattau, Maxim Serebreni, Greg Caswell [\[ANSYS\]](#)

The use of simulation tools to model the performance of semiconductor packaging is a well-known practice. However, because of resource limitations and prior experience, these activities are typically highly limited to key product lines and generic environments. With the explosion in package geometries to meet the unique demands of electrification, autonomous, and internet of things (IoT) market drivers, semiconductor manufacturers are being challenged to quantitatively understand these variations and how reliability may change in a customer-specific application. This paper will discuss how reliability physics analysis (RPA) is increasingly being used by the semiconductor industry and its customers to understand package-level and board-level reliability (BLR) and to clearly communicate performance expectations during material selection and product design. RPA is a technique that leverages the philosophy of physics of failure and simulation to predict mechanism-specific reliability performance. Identifying opportunities for model simplification based on industry standard geometries and implementing closed-form equations to replace time-stepping analyses, RPA allows for more agile evaluation of design and material options and provides insight into system-level effects on package-level reliability. Two key case studies that demonstrate the capability of RPA to improve the design and qualification process of semiconductor packaging, solder fatigue and low-k cracking, are reviewed.

Introduction

The silicon-based transistor gate is the fundamental enabling technology that drives innovation. The transistors on the silicon needs to be connected to the rest of the world through the package. The size and scale of the connection between the silicon die and the package makes it difficult to directly measure the stresses in the package. There have been many advancements in simulation capabilities

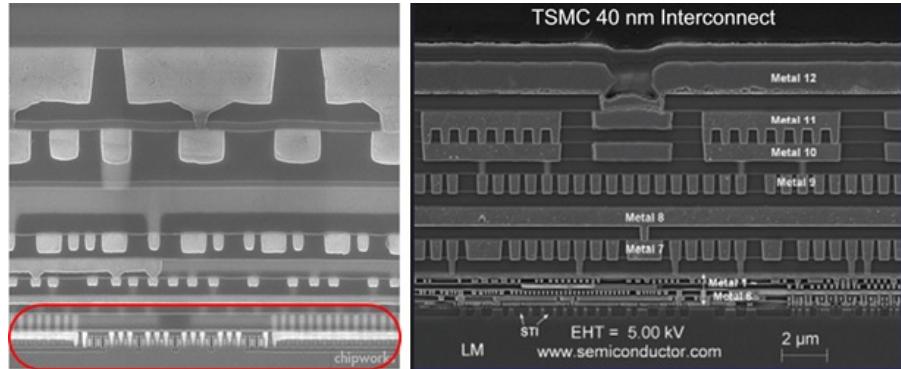


Figure 1: Cross section examples of the FEOL and BEOL structures on a silicon die. The FEOL structure is highlighted in red [1].



Figure 2: Example of a wafer warpage caused by CTE mismatch between the active layers and the silicon wafer [2].

regarding package design. This paper discusses how RPA is increasingly being used by the semiconductor industry and its customers to understand package-level reliability and to clearly communicate performance expectations during material selection and product design.

The fundamental properties of silicon

The silicon die processing and manufacturing process begins with wafers. Wafers are round discs of single crystal silicon that is ready for deposition of materials that will make the individual gates and interconnects of the individual “chips.” Each silicon wafer is processed as one unit. A single wafer may contain as many die as will fit on it. The active layers are the smallest material structures that create the gates. These layers, commonly called the front end of line (FEOL), are highlighted in red in **Figure 1**. It is common for dies

to have several metal interconnect layers between gates. The last interconnect layers also include the I/O aluminum pads. These layers are commonly called the back end of line (BEOL) as shown in **Figure 1**.

Many of the problems that are tackled in semiconductor packaging arise from the fundamental material properties of silicon. The coefficient of thermal expansion (CTE) of silicon is 2.6 ppm/ $^{\circ}$ C and the elastic modulus is 130 GPa. The active layers are made from materials that have a different CTE than silicon.

As shown in [2] **Figure 2**, the CTE mismatch between the active layers and the silicon material can cause the wafer to warp. The die warpage can be predicted with finite element modeling (FEM) techniques. The stress in the die can influence chip-package-interaction if the stress in the die and active layers is high enough. The stresses will remain even after the individual die are singulated. Die warpage is an indicator

of residual stresses and those stresses are present at the time of the attach process of the chip.

The properties and flavors of package substrates

There are many kinds of packaging. This paper concentrates on the types of packages that employ a flip-chip die connected to a substrate. The modeling methodology used in this paper can be modified to fit other package types. Multi-chip module (MCM) and system-in-package (SiP) designs can have several die and other components attached to a substrate. The substrate serves as a thermal, electrical and mechanical connection for the die and most importantly, the active layers. Flip-chip packages, as shown in **Figure 3**, use a tin-silver (SnAg) solder “bump” as the interconnect. The silicon die has the active layers facing the substrate. The substrate is made from multiple layers of copper traces and vias.

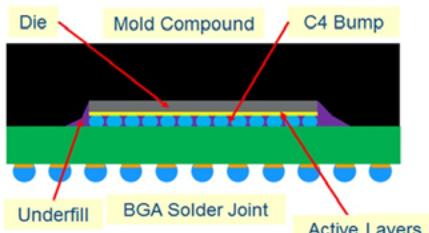


Figure 3: Example of a ball grid array (BGA) package with a flip-chip interconnected die.

The chip-to-package interconnect

Any reliability physics analysis that includes details of the first-level interconnects needs to capture the various geometries and materials between the die and the substrate. The resulting geometry of the entire bump will include the solder, the under bump metallurgy (UBM) and the copper pad on the substrate side. The C4 bump is made of SnAg solder and the copper pillar is made of copper.

Copper pillars are being used for applications that need a smaller pitch between interconnects. The copper pillar is made in a similar way as the solder bump UBM. **Figure 4** shows examples of copper pillars that can be connected to surface mount devices (SMD) and non-solder mask defined (NSMD) substrate pads.

The C4 bumps will tend to be round due to the nature of the solder melting during reflow, but copper pillars have more variety in geometry. The usual copper pillar is

round but elliptical, and even rectangular pillars have been designed. Copper pillars can also be attached to traces on the substrate instead of pads.

It is difficult to make a reliability physics analysis that will fit all scenarios and failure modes. The interconnect model is usually the most critical part of modeling chip-package interactions. The main modeling challenge is trying to capture small details in a large package model. However, it is getting easier to add more details to the model as finite element solvers get better and computer capabilities increase.

The chip attach process

Flip-chip dies can be attached to the substrate with a reflow process. The cool down from solder solidification temperature (230°C) is when the stresses begin building on the interconnect. The softest material in the interconnect is the solder, but it takes time to deform and undergo stress relaxation. The shear load on the solder creates a moment load on the aluminum pad and result in a tensile stress on the extreme low-k (ELK) dielectric layer. A higher first principal stress (S1) will result in a higher probability of fracture in the low-k layers. The fractures in the low-k layer are sometimes called “white bumps” because they appear as white circles in confocal scanning acoustic microscopy (CSAM) images. **Figure 5** shows the moment created on the solder joint and the resulting tensile stress in the low-k layer.

The corner bump has the highest stress in dies that have a continuous bump pattern. It is possible to see high stresses in other regions of the die if there is a sudden bump pitch change or large areas of depopulation. The ELK dielectric failure mode is more prevalent in copper pillar structures than solder bumps. Large dies are more susceptible to ELK dielectric cracks due to the larger distance to neutral point. Different passivation thicknesses and materials can be used to mitigate these failures. It is also possible to change the bump passivation opening diameter, but there is a tradeoff between the risk of ELK dielectric overstress cracking and the delamination between the copper pillar and aluminum pad.

Flip-chip solder fatigue due to temperature cycling

The SnAg solder used in packaging electronics has many desirable properties, but it is susceptible to fatigue failure. The CTE mismatch between the die and the substrate causes a shear load on the solder joint. The solder is the material that incurs most of the damage because it is relatively soft compared to the copper in the UBM and the substrate pads. The shear load on the solder will undergo stress relaxation due to a creep mechanism at every temperature cycle. Accordingly, the damage in the solder accumulates because the shear load is reversed and stress-relaxes in every temperature cycle.

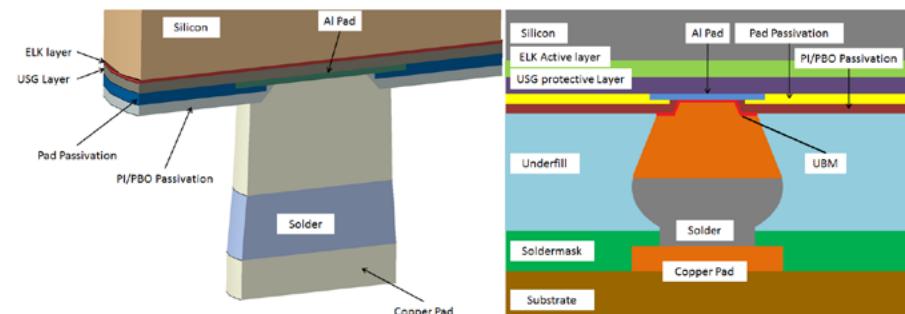


Figure 4: Copper pillar detailed models: a) (left) an example of an NSMD substrate, and b) (right) an SMD substrate.

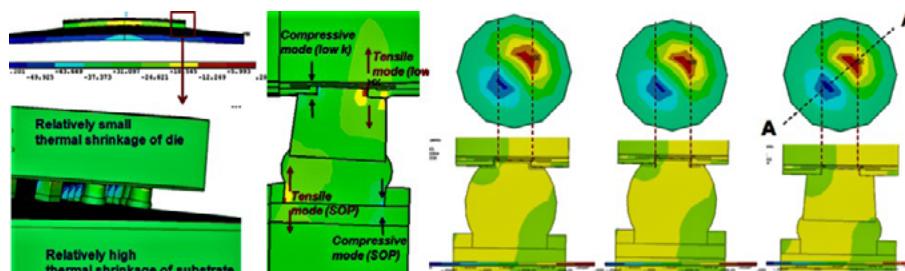


Figure 5: Explanation of the ELK stress model results. NOTE: Adapted from [3].

The strain energy density (SED) accumulated in each cycle is the damage indicator for damage in the solder. There are several experimentally driven equations to calculate the number of cycles to failure from the SED. The first temperature cycle starts at a stress-free state and the SED in one cycle is directly calculated in the finite element solver. **Figure 6** shows a comparison between two hysteresis loops of the stress-strain plot of a solder joint with two different underfills.

The hysteresis loop area is the SED of the solder. A larger area inside the loop indicates more damage in the solder. **Figure 6** shows three loops representing three temperature cycles, but the difference between the second and third cycles is extremely small. Because temperature cycling tests are performed on finished packages, the solder fatigue model should include all the features of the finished package. Each type of package will have a different behavior depending on how it is finished. Overmolded packages are different from bare die and those with stiffener rings or lids.

The damage in the solder accumulates because the shear load is reversed and undergoes stress relaxation in every temperature cycle. The CTE mismatch between the die and the substrate causes a shear load on the solder joint.

The SnAg solder used in packaging electronics has many desirable properties but it is susceptible to fatigue failure. The reliability physics analysis for the solder fatigue failure mechanism can be used to predict the package performance.

Summary

As the utilization of semiconductor packages continues to diversify and expand with the increased implementation of electronics, there has been a growing need to better understand the environment and interaction of the components within electronic packages. The powerful capabilities of advanced simulation that rely on reliability physics analysis provides designers a more accurate interpretation of the system-level effects of these packages. This leads to the production of predictable and reliable products.

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Biographies

Gil Sharon is a Senior Application Engineer at ANSYS, Beltsville, MD. Dr. Sharon is a diverse industry expert with research specialties including mechanical reliability of electronic systems and characterization; embedded components failure analysis and particle beam accelerator mechanical fatigue; multidisciplinary reliability of complex electromechanical systems; characterization and modeling of material behavior; mechanical performance of flip-chip packages; and Physics of Failure of electromechanical and MEMS systems. In addition to his responsibilities at ANSYS, he serves as an adjunct faculty member at the U. of Maryland; email gil.sharon@ansys.com

Nathan Blattau is an R&D Fellow at ANSYS, Beltsville, MD. Dr. Blattau has been involved in the packaging and reliability of electronic equipment for over twenty years. His primary research interests are in the areas of development of Physics of Failure models and algorithms, design-for-reliability in electronic packaging, nonlinear finite element analysis, solder joint reliability, and fatigue mechanics of materials. Through extensive testing, analysis, and simulation, he has developed a thorough understanding of the defects and degradation mechanisms that can induce failures in electronics. He also holds two patents pending in software-based simulation and accelerated life testing. He received a PhD in Mechanical Engineering from the U. of Maryland.

Maxim Serebreni is an R&D Engineer at ANSYS, Beltsville, MD. He has a background in experimental mechanics, material characterization and numerical modeling. His current research involves integration of Pb-free solder alloys in harsh use environments. He has consulted in the fields of electronics reliability, electronic packaging design, and solder alloy metallurgy. He is currently completing his PhD in Mechanical Engineering at the U. of Maryland, College Park under the supervision of Dr. Patrick McCluskey.

Greg Caswell is a Lead Consulting Engineer at ANSYS, Beltsville, MD. He has over 50 years of experience in microelectronics. Previously, he was the VP-Engineering for Reactive NanoTechnologies and VP Business Development for Newport Enterprises. His experience encompasses SMT manufacturing, circuit board fabrication, advanced packaging, IC fabrication processes and materials, solder reflow, and RoHS. A past president of IMAPS NA, he is currently the Editor in Chief for Advancing Microelectronics magazine and recently received the Lifetime Achievement Award from the Society. He received his BSEE from Rutgers U. and has a Bachelor's degree in Management from St. Edwards U. in Austin.

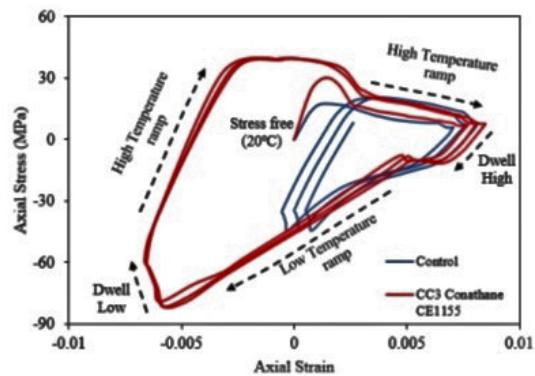
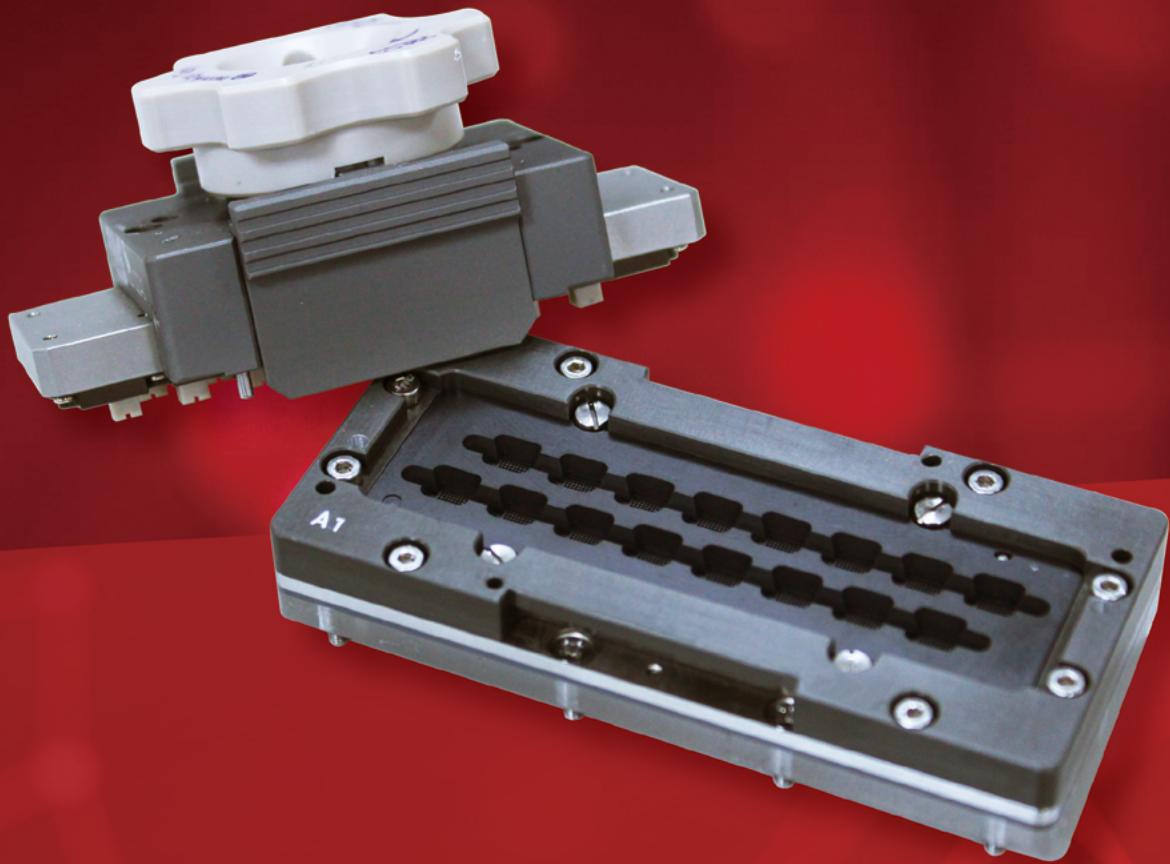


Figure 6: Example of stress-strain curves for a temperature cycle analysis [4].



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MRAM testing for high-volume manufacturing

By Siamak Salimy [\[Hprobe\]](#)

Industry interest in perpendicular spin transfer torque magnetic random access memory (STT-MRAM) technology as a new nonvolatile memory (NVM) has been confirmed by the production schedules of major foundries announced last year. Today, the technology is considered as one of the most promising emerging NVM devices for embedded applications. Thanks to its fast writing speed, lower power consumption, and the ultra-low latency of STT-MRAM, several applications are targeted such as static random access memory (SRAM) replacement in last-level cache (LLC), dynamic random access memory (DRAM) replacement in data centers, and memory control units (MCU) for artificial intelligence (AI) and neuromorphic calculation.

MRAM technology scalability down to low single-digit technological nodes has been an important driver for big industrial players implementing their Moore's law journey. Shrinking of the unit memory cell (i.e., the magnetic tunnel junction) below 10nm was demonstrated last year by research groups from Spintec [1] and Tohoku University [2]. Performance and size shrinking drivers resulted in consequential efforts with large investments to transfer STT-MRAM technology to the back end of line (BEOL) of the 300mm manufacturing process for embedded memory applications. Samsung and GLOBALFOUNDRIES will offer STT-MRAM embedded in the fully-depleted silicon on insulator (FD-SOI) process at 28nm and 22nm, respectively. Taiwan Semiconductor Manufacturing Company (TSMC) will start producing in 28nm, as well as United Microelectronics Company (UMC). Lastly, Intel announced the manufacturing of MRAM memory chips in its 22nm FinFET process.

STT-MRAM

STT-MRAM is based on a perpendicular magnetic tunnel junction (pMTJ) build with a stack of thin-film layers including a minimum of two magnetic films, fixed and free layers, with a thin insulator between them. Each magnetic layer has its intrinsic electronic spin oriented in the up or down

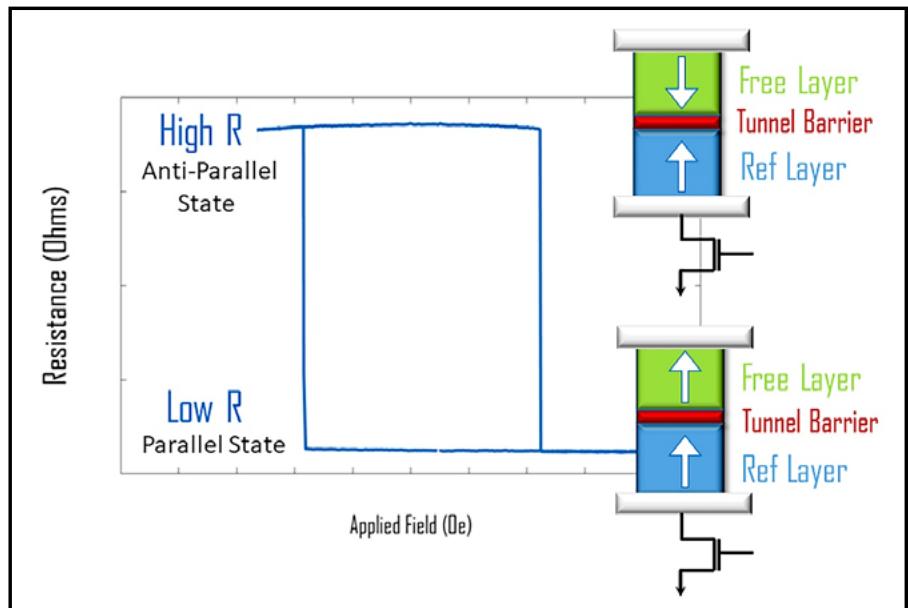


Figure 1: Illustration of a perpendicular magnetic tunnel junction and its resistance vs. perpendicular hysteresis cycles.

direction as illustrated in **Figure 1**. If the two magnetic orientations are parallel, the MTJ is in the lower resistance state (bit '0'). If the two orientations are in the opposite direction, the resistance is in high state (bit '1'). Applying an external field perpendicular to the device surface can switch it from one state of resistance to another as shown in the hysteresis cycle (**Figure 1**). Switching can also be done by STT using an electronic current passing through the MTJ. One MTJ associated with one transistor builds a single bit memory cell that when duplicated "n" times in a matrix array creates the number of bytes required by the application. The MRAM manufacturing process has most steps in common with a traditional BEOL CMOS process with the exception of the MTJ formation step, where the device is placed in between the M(i) and M(i+1) metallization layers.

Challenges in MRAM testing

The specificity of STT-MRAM in being a magnetic memory based on a perpendicular magnetic tunnel junction requires that the MRAM wafers be tested using an external perpendicular magnetic field while doing

electrical probing. In addition, the probing is done with high-frequency hardware that provides the ultra-narrow time domain voltage/current pulses used to write and read the devices. The use of a varying external magnetic field above the wafer while probing brings some difficulties, which includes having a fast sweeping capability for time domain pulsing. Both of these requirements are difficult to integrate into a 300mm wafer probing system. Furthermore, electrically probing wafers with STT-MRAM under a magnetic field with testing time performances compatible with volume manufacturing requirements is challenging.

Test requirements for STT-MRAM. The test requirements for STT-MRAM, the wafer-level testing is done by:

1. Applying a variable magnetic field in the perpendicular direction above the device for extraction of the hysteresis curve as illustrated in **Figure 1**. This is done to evaluate the ability of the unit cell to switch from one state to another and to extract physical parameters giving insight on the ability of the memory cell to retain the stored

information. The perpendicular field above 5000 Oersted is needed to switch both the free and fixed layers.

2. Applying a pulsed signal with an ultra-narrow pulse width (down to 1ns and up to 5V amplitude) to the device to validate its writing/reading operation, as well as its breakdown voltages/currents.

One baseline test program for MTJ characterization and testing comprises three protocols as shown in [Figure 2](#).

The switching process in STT-MRAM is stochastic. To validate reliable operation for the memory point, both wafer and device statistics need to be extracted. It is therefore preferred that perpendicular magnetic field sweeping be done a number of times as there is a distribution on the switching fields on account of the stochastic nature of the spin switching process in the MTJ. The faster the field amplitude can sweep up and down, the lower the testing time that will be achieved. For wafer testing in mass manufacturing, magnetic-controlled heating and probe stability on the wafer while varying the magnetic field must be guaranteed at both ambient and high temperature. In addition, on the same probing system, the bit writing process in the MTJ is tested using a pulsed signal that has a pulse width down to 1ns where rising/falling times are accurately controlled up to an amplitude of 5V. Accordingly, the pulse test is performed using a high-frequency probing system with a Gigahertz bandwidth range to ensure that pulse signal integrity is not degraded.

Testing time is the key performance indicator in production and a strong added value to reduce development time. Being the next generation of NVM for embedded application in the lower technological nodes means potentially having a large number of MRAM wafers coming out of the fab every year. It is known that the testing time per chip, or per wafer, in production is critical. Indeed, as the testing cost is linear with time, it may represent a consequential percentage of the chip's final cost if it is not optimized.

Throughput performances are usually considered as not being too critical in technology development, and sometimes not even during qualification phases. However, the metric in production is to get a testing time per chip as close to zero as possible. In the case of MRAM, this means that throughput for performance of the hysteresis cycles R(H) and R(V) should be in the shortest time possible. Nevertheless, sweeping a fast magnetic field at high amplitude is not

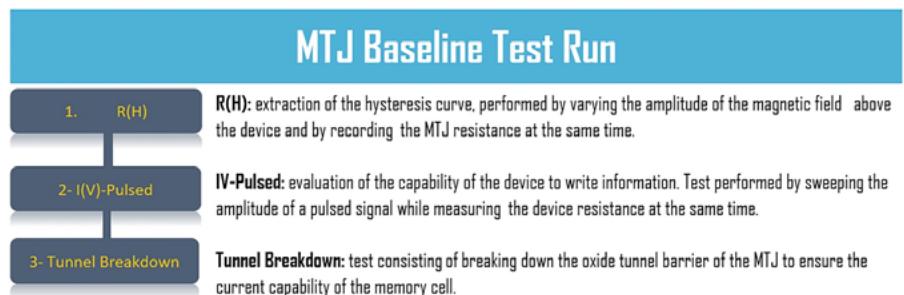


Figure 2: Baseline test program for an STT-MRAM magnetic tunnel junction.

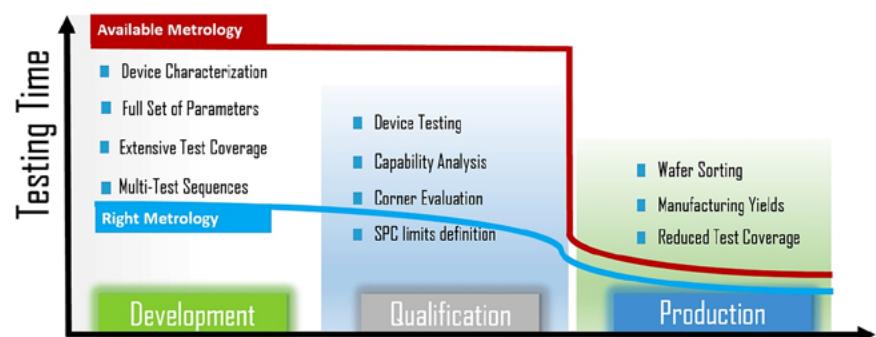


Figure 3: Wafer test metrology in all phases of technology development for volume manufacturing.

straightforward. Superconducting magnets can achieve high amplitude fields, but do so with poor field sweep speed performances and are subject to mechanical vibration, which is problematic to achieving a stable probing system. Classic electromagnets and copper coils enable attainment of a very fast field sweep, but suffer from low field amplitude for a given volume of copper turns. Furthermore, using the classic solution it is very difficult to achieve a perpendicular field above 5,000 Oe.

In addition to specific technical challenges of testing STT-MRAM, reducing the overall time of development to release an emerging technology into volume production is critical in today's competitive global semiconductor market. With the goal in mind of not impacting the production schedule, we often see the cost optimization of wafer monitoring process steps (i.e., throughput performances) happening during the ramp-up phase and after technology release. Nevertheless, being able to develop and qualify the technology with the same metrology tools during all phases of development is a strong value add. Using the same metrology tools helps to reduce the development and qualification time while providing a strong baseline for production wafer testing. For example, monitoring wafer flow, and the test conditions for it, could all be optimized at the same time as the technology is being developed.

Testing STT MRAM wafers under a magnetic field and with various pulsed signals is mandatory for all phases of development, qualification and production of MRAM devices, even if the objectives are different. As illustrated in [Figure 3](#), in development, engineers are willing to use the largest set of parameters to evaluate, with multiple test conditions and with extensive test coverage, including design variations and with process splits, which could result in a very large number of chips to test. In qualification, the objective is to evaluate the capability and stability of the manufacturing process with specific test vehicles and corner test conditions. In production, it is all about cost performance and yield management.

As an example of the above discussion, consider STT-MRAM wafers, which include 500 MTJ test structures per wafer to be tested. This results in a lot of 25 wafers having a total number of about $500 \times 25 = 12,500$ devices under test (DUT). Running under a test with a minimum of 10-100s per DUT, this is a testing time that can be considered as a state of the art standard. The resulting test time for this example is above 34 to 340 hours of testing for the full lot, which is a consequential amount of time. One can therefore see that a non-optimized testing time in a development or qualification phase results in extending the time to release of the technology. The non-

optimized test time slows down the loop learning of the technologist by reducing the statistical evaluation that in turn lowers the slope of the learning curve. As a result, the cost of test will dramatically increase in production. In each of these phases, testing time is definitely very important, but for different reasons.

The amount of investment to develop a new technology is largely dominated by process tools (e.g., deposition and etching). However, using the available metrology (red curve in [Figure 3](#)) for wafer testing always seems attractive. Nevertheless, when it's time to bring the technology into production, the gap to achieve a competitive cost of test could be very high should process control metrology tools be changed along with any associated changes in test protocols and test conditions.

Building the optimal wafer test equipment dedicated to STT-MRAM technology with good testing time performances in the development phase (illustrated by the blue curve in [Figure 3](#)) brings strong value add when reducing the overall time to release the technology during the ramp-up to high-volume manufacturing (HVM). Using this method, an excellent baseline for cost optimization of test time and yield management can be achieved during the ramp-up to production. The challenge is to have MRAM wafer testing equipment able to fulfill the need for flexibility with sufficient performance to support engineers on their long road to the full release of process technology, and then, to control and monitor the production at a competitive cost.

Dedicated magnetic wafer-level test equipment for STT-MRAM

We have developed a turnkey system for users to test STT-MRAM MTJ devices as shown in [Figure 4](#) (called IBEX300-2C). With this test equipment, the wafer sorting process is performed through parametric testing under a magnetic field and by using pulses with duration on the order of nanoseconds or sub-nanoseconds. This magnetic ATE resolves the bottleneck in MRAM wafer control and monitoring during the production process, as well as giving a flexible tool for development and qualification phases.

The system uses a type of 3D magnetic generator® with ultra-fast field sweeping capability. The magnet technology has been spun off at Hprobe by the Centre National de la Recherche Scientifique (CNRS) in France to solve the challenges of testing MRAM under a magnetic field. Indeed, with the 3D magnetic generator, a field sweeping rate

above 10ksamples/second can be achieved to record the hysteresis cycle of STT-MRAM devices. This solution enables the implementation of testing requirements for MRAM mass production. Furthermore, the 3D generator is an air cooled design without requiring any liquid cooling system to get reliable continuous operation. This type of design facilitates its implementation in the wafer fab (no water and no helium cabling system required along with the associated maintenance).

The test bench we developed is illustrated in [Figure 5](#) where the magnetic generator is placed on the top plate of the wafer prober and is associated with a set of instruments for double-channel testing of the MTJ (i.e., two independent devices tested at the same time). The baseline test program for MTJ testing illustrated in [Figure 2](#) runs in less than a single second on the two channels, thereby resulting in the best equivalent testing time per device that is shorter than 500ms. Thanks to the ultra-fast magnetic



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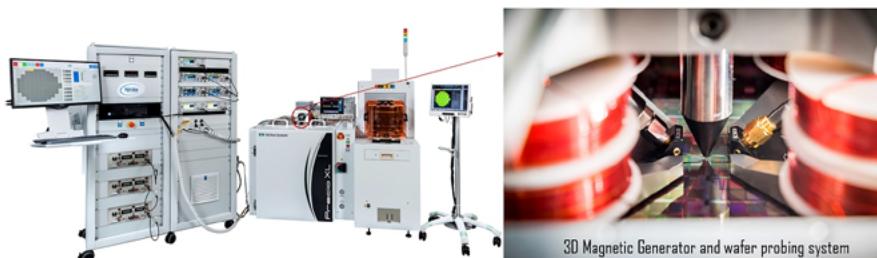


Figure 4: Test equipment developed by Hprobe for STT-MRAM testing.

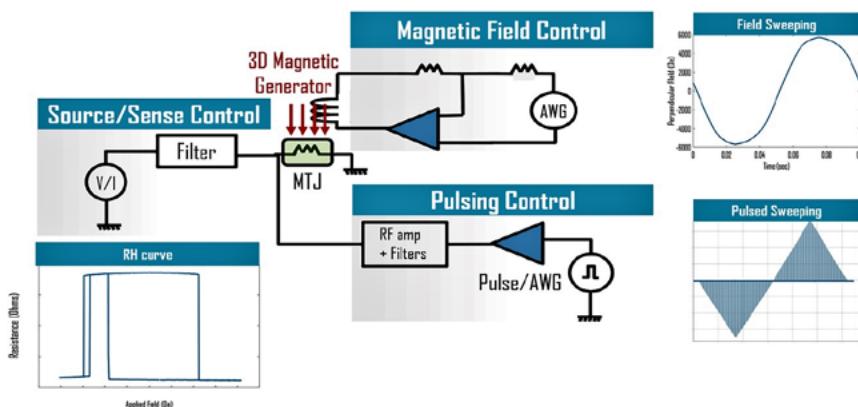


Figure 5: The tool is using a 3D magnetic generator for field sweeping and an ultra-fast AWG system for pulsing signals generation.

field sweeping capability of the 3D magnetic generator, the R(H) hysteresis curve itself can be extracted in less than 100ms. Although the fast magnetic field generation capability of the system has been important in the throughput performances achieved, other factors have been optimized to build a fast testing solution. Indeed, the communication and interaction between instruments have all been optimized. Full synchronization of signals is performed at the low-level hardware to ensure fast operation. In terms of pulsed signal capability, the system is operating with more than a 6GHz bandwidth in the signal path down to the probes. Any pulsed signal pattern can be created with an amplitude up to 5V with a high impedance load and a minimum pulse width of 200ps. The pulse rising/falling time is controllable from 85ps. The pulsing system has a capability of two pulsing channels operating up to 12Gsamples/s with sub-nanosecond pulse width and accurate pulse edge control. The biasing and sensing of the

resistance is synchronized with the magnetic field sweep and pulsed signals.

Associated with the tester and wafer probe hardware, a full suite of software interface has been developed and is called Hmap®. This suite can be used by test engineers and technology developers to easily establish their own MRAM test program by using available pre-defined test modules such as R(H), I(V)-DC, I(V)-Pulsed, tunnel breakdown, bit error rate (BER) and endurance tests. Both tester hardware and wafer probe are controlled by the software, which also includes automation features related to an advanced 300mm automated wafer fab environment.

To run the testing on a MTJ bit memory cell, the test modules are sequenced by user input to build the test program. Each test module has its own dedicated extraction parameters algorithms for automated extraction of key parameters, such as field switching probability, anisotropic field, data retention factor, switching voltage

distribution, BER, etc.

To bring flexibility and enable the use of the tester in all phases of technology development, as well as in volume production, test engineers can also program their own test protocols in the Hmap® environment using LabVIEW® language. The Hmap® software controls the tester, the wafer prober at ambient or high/low temperature, the probing process, and it also drives an embedded magnetic field calibration system used to control and monitor the magnetic field at the exact position of the MTJ under test.

Summary

The magnetic ATE described above handles up to 10-100 times more wafers per hour than current state of the art solutions for the testing of MRAM under a magnetic field and with current pulses. It is compatible with all phases of technology development, as well as for mass production, with unique throughput performances in MRAM testing and sorting. Presented here for STT-MRAM development, ramp up and mass manufacturing purposes, the hardware gives MRAM engineers the possibility of also testing spin orbit torque MRAM (SOT-MRAM) and voltage-controlled MRAM (VC-MRAM). Indeed, the 3D generator has a multi-axis magnetic field feature with independent XYZ axis control. The tool is certified per SEMI S2 and already shipped to major MRAM industrial players for development and manufacturing of STT-MRAM.

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Biography

Siamak Salimy is the founder and CTO of Hprobe, Grenoble, France. Before Hprobe, he led test development and transfer to production of an RF MEMS breakthrough technology for 4G/5G mobile applications at Delfmems. He also was a scientist at Teledyne Dalsa Semiconductor in charge of the CMOS/DMOS process and MEMS sensor test development and he developed advanced passive device technology at Atmel Semiconductor. He founded China Consultants International, providing services to bring products from samples to volume manufacturing. He holds a PhD from the U. of Nantes, France, and is an engineer from the Polytech' School of Engineering. Email siamak.salimy@hprobe.com

MEMS packaging trends: from LGA to 3D integration

By Stéphane Elisabeth, Audrey Lahrach [*System Plus Consulting*]

In the last few years, microelectromechanical systems (MEMS) have been widely used in different segments: consumer, automotive, industrial, etc. With products such as inertial, microphones, pressure sensors, etc., innovation with MEMS has long been a hallmark in process manufacturing. With the introduction of heterogeneous systems, the use of MEMS packaging is expected to expand significantly in the next few years. Wafer-level packaging (WLP), 3D through-silicon or through-glass vias (TSVs or TGVs), and wafer bonding are key enablers for heterogeneous integration in every segment where devices require small form factor, high-speed operation and low power consumption. Cost efficiency is also, of course, critical.

Packaging solutions for MEMS devices have been well settled over the past few years. With simple packaging like quad-flat no-leads (QFN), or land grid array (LGA), MEMS cost breakdown distribution gives a low value for this aspect. But with increasing demands to reduce both footprint and power consumption, along with an increase in performance, packaging is now at a turning point in order to satisfy the industry.

Three stages or levels of packaging can be defined. The first level corresponds to the wafer. Here, several challenges can be overcome using technologies like capping or wafer bonding. At this level, several innovations have been seen over the last few years that move toward monolithic or heterogeneous structures. The second level has helped to achieve these two structures and it corresponds to the interconnect. At this level, TSVs, wire bonds, bumps, and conductive glue have been developed. The last stage is the final package where traditional packaging still dominates the market. As shown in **Figure 1**, in 2018 the packaging market for MEMS was estimated to be above \$3B, and it is expected to double to \$6B in 2022.

The growth will be mainly driven by the radio-frequency (RF) device market with the introduction of 5G and mmWave

technologies, mostly for consumer applications. The “core” market is expected to maintain the use of traditional packaging, such as LGA and QFN. But some innovations are currently in development in fields like automotive and consumer, which will open the market to advanced packaging. Indeed, in the next few years, embedded die in laminate or fan-out wafer-level packaging (FOWLP) are expected to grow.

Packaging technologies: from standard to WLP

In the field of MEMS, the most common packaging types are LGA, QFN and dual-flat no-leads (DFN), as we confirmed in [2]. LGA packages use a printed circuit board (PCB), unlike QFN and DFN packages that use a lead frame in the structure. The cost driver of these packaging types is different. However, these common types of packages are evolving toward wafer-level chip-scale packaging (WLCSP). In some categories, the package tends to remain at the same level. In other categories, however, we observe some manufacturers who

are constantly trying to improve their products with disruptive changes, such as with bonding or via technologies. This shows the potential of WLCSP packaging leading to 3D integration.

Based on the large number of components analyzed, the market seems to be dominated by LGA packaging, at 60% [2]. The other 40% is shared between QFN/DFN, small outline integrated circuit (SOIC) and WLP. At the field level, this split is not the same. For automotive applications, where harsh environmental requirements could apply, LGA is no longer the main driver and SOIC packaging dominates the field. In consumer applications, however, LGA is the leading type with its simplicity of integration. Finally, WLP use is mainly driven today by MEMS. Magnetometers, with their similarity to an integrated circuit, have been widely introduced with WLCSP packaging. Another field is RF applications where small devices like filters require the smallest interconnection with the mainboard in order to reduce losses. This has brought WLP to a next level with TSV and CuFlip™.

Total MEMS packaging market revenues Breakdown by family of devices

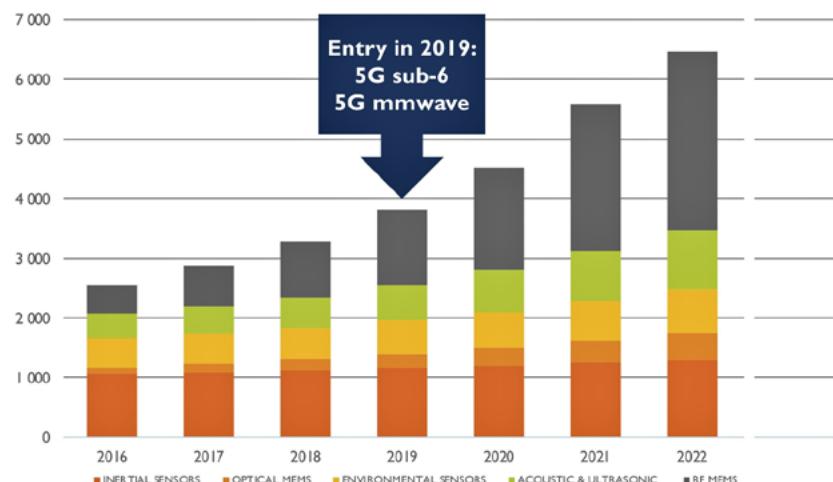
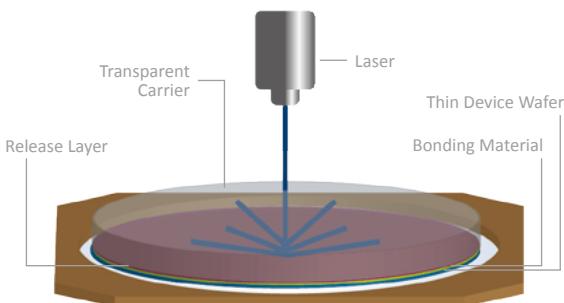


Figure 1: MEMS packaging activity market forecast [1].

Creating Safe Environments

Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with: 308 nm 343 nm 355 nm

QFN, LGA, etc.: What's driving the cost?

This year we observed several MEMS devices showing the potential of standard packaging in high-performance components. Companies like Honeywell, Analog Devices and Bosch Sensortec are still using LGA, QFN and ceramic leadless chip carrier (CLCC).

Even in high-performance applications, different specifications could lead to different packaging approaches. In tactical grade applications, Honeywell supplies an inertial measurement unit (IMU) using CLCC packaging, supposedly for performance reasons, such as an accelerometer in automotive applications or a microbolometer in industrial applications.

The CLCC packaging used for the high-performance IMU is realized in-house by Honeywell. Besides the performance, cost reduction could also come from the fact that Honeywell has the capability to do this type of package. The cost breakdown of a MEMS IMU packaged with CLCC technology is shown in **Figure 2**. Because of the extreme specification required for the tactical grade, the final test, calibration and burn-in steps comprise almost 40% of the cost. But when we only consider the remaining three components (see **Figure 2**), the packaging took one-third of the remaining cost, while 80% is due to the ceramic substrate.

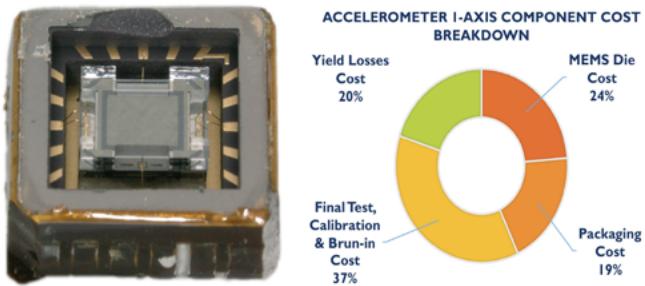


Figure 2: a) (left) Honeywell 75001513 [3]; and b) (right) Component cost breakdown [3].

When the expectation of the device is lower, simple LGA packaging could be preferred as the cost is relatively low and the performance quite acceptable. This type of packaging could be used for components like environmental sensors, inertial sensors, microphones, RF MEMS, etc. For inertial sensors, Bosch Sensortec has always preferred LGA packaging for its consumer devices. The company offers several devices all based on a similar structure.

The internal structure of several Bosch components is shown in **Figure 3**. Besides the single magnetometer that is packaged using WLCSP like a standard IC, all the inertial and combo sensors are integrated into LGA structures. This shows the potential flexibility of the LGA package. All 7 sensors rely on only 6 different dies. It's only the combination that gives the different components from the 3-axis to the sensor hub. And all of these have a low packaging cost, which is mainly driven by the equipment cost and not the substrate [4].

In other cases, such as high-frequency applications, less complicated and less expensive packaging could be used for the components. For example, Analog Devices offers in its portfolio a SP4T MEMS RF switch in a QFN package. The MEMS sensor is integrated into the package based on a lead frame using wafer-level capping, glass frit bonding, and gold wire bonds along with a dedicated application-specific integrated circuit (ASIC). In the cost breakdown, the packaging took 34% of the cost mainly due to the consumables like wire bonding or EMC [5]. But the larger

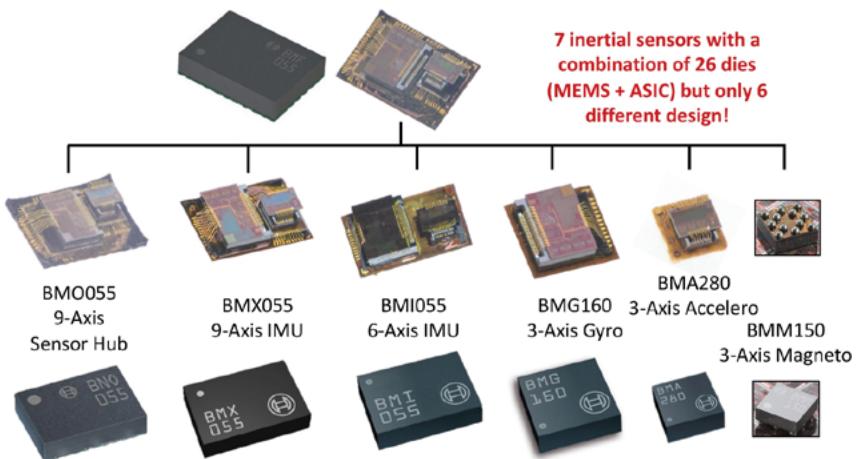


Figure 3: Bosch Sensortec portfolio extract and component detail [2].

part of the cost is for the MEMS itself at the wafer-level packaging stage. Specifically, as the MEMS devices require an inert environment to work without any interference, the mechanical part has to be protected from the outside. An EMC is not enough to realize the full potential of the MEMS. As a result, at the wafer level, there is a capping filled with an inert gas using a second silicon substrate. This corresponds to the first level of WLP.

Introduction to WLP

Several levels of WLP can be defined. All the devices that are discussed in the following paragraph utilize a final package like LGA or QFN, different from WLCSP, which is moving toward 3D integration. At the first level, the WLP begins with a simple capping. After that, at the second level of integration, we will define a level where the mechanical part is manufactured using WLP. Finally, at the third level, we

will consider a structure called "MEMS over CMOS." These three structures are presented in **Figure 4**.

In the three examples noted above, different types of wafer bonding are used to assemble the different parts at the wafer level. The simplest technology is glass frit bonding. Using a wafer with several cavities created while using dry etching, bonding with a glass paste is used to seal the mechanical part in vacuum. When the form factor of the component is a critical specification, fusion bonding could be used. In the case of the high-performance 1-axis accelerometer from Colibrys (now part of Safran Group), the sensing part is bonded to two other substrates creating the cap and supporting the device. In this case, several advantages linked to the bonding technology are realized: miniaturization, strength, and electrical connection between the substrates. The drawback is that ultra-smooth wafers are

required. Today, the tendency is to move to eutectic bonding. In looking for more integration, the industry has developed a new method called "MEMS over CMOS." In this architecture, the MEMS is on top of the CMOS structure and connections could be made at the side or the top of the MEMS, or at the rear of the CMOS wafer. In this way, the seal width could be reduced by 75%, but first the need for post-bond alignment must be reduced. InvenSense was the first company to introduce this technology for inertial sensors. The process is called Nasiri-Fabrication™. In this process, the CMOS and the MEMS processes are realized separately. In the MEMS process, the metal layer (germanium) for bonding is deposited on the standoff part. These parts are used to bond the wafers, as well as to create a space allowing the movement of the mechanical parts. In the CMOS process, some aluminum pads are dedicated to the bonding. Also, as in glass frit bonding, the bonding temperature must go up to 400°C in order to create Al-Ge metal bonding. In terms of cost, glass frit has a low cost of ~\$7 per 8-inch wafer. Fusion bonding and eutectic bonding are more expensive, respectively, almost 2 times and 7 times higher [8]. Even if it is costly, the latter is fully CMOS-compatible, which makes it a successful candidate for 3D-integration.

Packaging technologies: toward 3D integration

Packaging technology is an important part of MEMS development. Indeed, as devices move to 3D integration with smaller form factor and more functionality in one component, the MEMS design must be upgraded in order to provide the smallest form factor along with the best performance. "MEMS over CMOS" was a first step. At the wafer level, it allows the combination of the ASIC driver with the MEMS actuator directly onto the same chip. However, it required additional standard packaging to be on the main board. Today, monolithic integration is the path taken by a few manufacturers. They look at solutions able to integrate the ASIC driver and the MEMS actuator in one bloc on a main board or in a system-in-package (SiP). In this configuration, the redistribution of the electrical connections is the more difficult process. Several technologies have been considered and are in production now: TSVs, TGVs, etc.



Figure 4: Example of MEMS using wafer-level packaging. From left to right: ADI ADGM1304 [5], Safran-Colibrys V1000 [6], and InvenSense ICM-20789 [7].

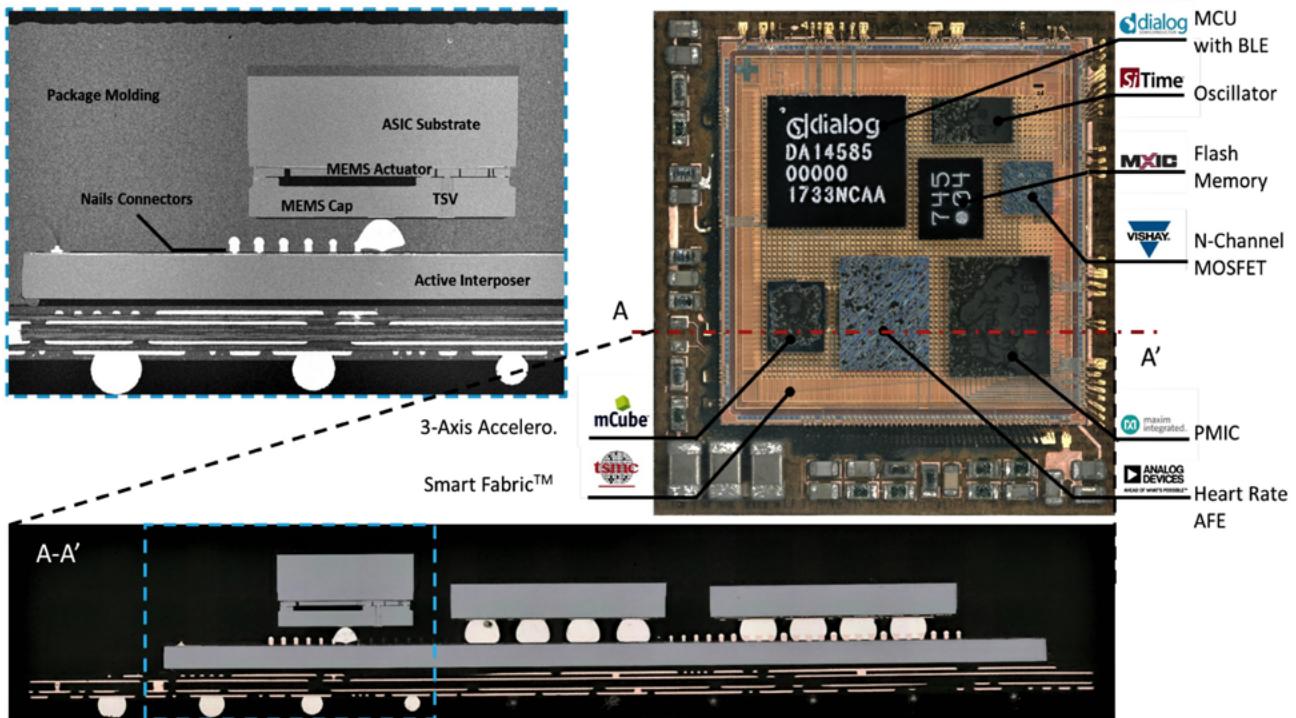


Figure 5: zGlue zOrigin chip: detail and cross section.

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Monolithic approach

There are only a few companies that have the technology to supply the demands of monolithic integration. The first was mCube in 2016, which offered a WLCSP 3-axis accelerometer. mCube started to use the technology “MEMS over CMOS” for its MEMS process with eutectic bonding. But for the MC3672, it additionally combined the process with TSV through the “MEMS cap” to create a WLCSP accelerometer. By doing so, the company managed to do away with wire bonds, the printed circuit board (PCB) substrate, EMC, and to reduce the silicon consumption giving a cost reduction.

In the third mCube generation, two packaging types have been considered: LGA and WLCSP. Both MEMS designs have the same footprint. In the case of LGA packaging, the die cost is 65% of the component cost, whereas the packaging and final test is 35%. In the case of WLCSP with via-middle TSV manufacturing, the relative die cost is higher at 75%, with 25% for the redistribution layer (RDL), the top resin, the solder ball dropping and the final test. At the end of the process, the WLCSP is 10% cheaper than the LGA packaging with a footprint reduction of 44% [9].

Bosch Sensortec is a second company that is working on the transition to WLCSP for accelerometers. Initially, it implemented a WLP accelerometer into LGA packaging. The structure is similar to the mCube structure. It has the MEMS cap as a structure support with the MEMS actuator in the middle and the ASIC with the TSV at the top. Finally, the connect to the PCB is with wire bonding. As Bosch Sensortec has proved its capability to integrate a monolithic structure, we can expect that they are near to progressing onto WLCSP.

WLCSP structures could also be applied in other MEMS fields. In RF, Menlo Microsystems, together with Corning, has developed a MEMS package based on TGV. Indeed, the MEMS substrate and the capping use glass substrate and the TGV goes through the glass cap to the solder balls. By using this technology,

the company can offer a very powerful device in a small form factor. Moreover, the structure could be coupled with an ASIC in LGA packaging, but the benefit of the MEMS in WLCSP gives a footprint reduction of 20% compared to a competitor like Analog Devices.

First sight of heterogeneous structure

In all the structures described above, that of mCube is the most mature WLCSP technology on the market. This gives them a head-start in 2.5D integration. Indeed, with its very small form factor it is the more suitable device for heterogeneous structures. A startup company, zGlue, has proposed a solution based on the mCube device in a 2.5D integration (**Figure 5**). zGlue has developed a programmable interposer that could combine several chiplets together to form a SiP. In the first version, an entire fitness tracking system was offered featuring an MCU, a flash memory, an accelerometer (mCube MC3672), a heart rate front-end, and oscillator and a power management integrated circuit (PMIC) all in an 80mm² component.

The programmable interposer is a CMOS die featuring several switches made with transistors between the bridges. These transistors formed the routing between the chiplets regardless of the technology. In a standard system, the routing will use blind vias in a multilayered PCB between the different components. Moreover, if the system requires passive components, the routing could go through the wire bonding to the PCB and return to the interposer via another wire bonding. To connect the different chiplets to the interposer, several copper pillars are created on top of the interposer in face-up configuration. These copper pillars, called “nail connectors,” support the solder balls from the WLCSP components. In this configuration, several nails could be connected to one solder ball depending on the ball size. The density (100 nails per mm²) is large enough to provide good support for the chiplets and good electrical connection with the interposer.

Summary

Starting with standard packaging technology, the MEMS packaging industry has evolved a lot in the past few years. As we have seen, WLP has become the new standard, even if most of the time it's followed by an integration on a metal lead or a PCB substrate. With the arrival of 2.5D assembly technology, however, like embedded multi-die interconnect bridge, or chip on wafer on substrate (CoWoS), WLCSP is starting to be developed by several companies and will be implemented in the future in heterogeneous structures. This year, it will start with 2.5D integration, but the goal is to reach 3D integration in the future. This future may not be far off, as it will start to be revealed by Intel this year with the new Foveros structure dedicated to everything “from mobile devices to Data Center.”

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Biographies

Stéphane Elisabeth, PhD, joined the System Plus Consulting team in 2016. He is an expert cost analyst in RF, Sensors and Advanced Packaging, who has a deep knowledge of materials characterizations and electronics systems. He holds an Engineering Degree in Electronics and Numerical Technology, and a PhD in Materials for Microelectronics.

Contact author: Audrey Lahach is in charge of costing analyses for IC, LCD & OLED Displays and Sensor Devices. She holds a Master’s degree in Microelectronics from the U. of Nantes. Email: alahrach@systemplus.fr

Surfaces matter for semiconductors

By Edward Hughes, Don Cunningham [[Aculon, Inc.](#)]

The demand for innovation across the semiconductor industry is accelerating. As the demand grows, system original equipment manufacturers (OEMs) are fueling the drive toward ever higher performance features, higher speed data transmission, higher definition video, effortless data access, and power storage in smaller, smarter, faster, thinner electronic devices. The race for miniaturization and the development of chips with transistor and function densities previously unimaginable requires immediate access to new materials that can be easily applied and manipulated. Chip designers and manufacturers are responding with new packaging concepts with mandates to squeeze as much as possible from existing packaging design rules. The new semiconductor product design elements are the instigators of diverse new package form factors/outlines; new production formats driven by production cost reductions; and the slowing of Moore's Law. The new product concepts, structures, and formats are challenging and exceeding the limits of industry-standard materials.

Nanoscale surface treatments

Newly developed nanoscale surface treatments and previously developed surface treatments re-purposed for semiconductor package surfaces with properties that enhance and extend the functionality and performance of existing base materials are meeting those challenges. Just as alloying metals achieves elevated performance with base elements, new surface treatments can make base elements, such as copper and silver, perform new or more expanded functions. They protect tiny surfaces, provide more structure for design rule freedom, narrow process variation of other materials, reduce production costs, extend the useful life of existing materials, enable use of lower cost materials, and increase the wear-life of high-volume equipment components.

Die attach in the package assembly environment is a particularly delicate

step in the manufacturing process. Continuously escalating performance requirements only add to the challenge. Bonding a super thin, large area flip-chip onto a laminate substrate or a tiny chip on a wire bond metal lead frame stretches the processes that use epoxy, soft solder, eutectic and flip chip. Each combination presents unique challenges in both the process and the execution. Integrating surface treatments into the processes mitigates several of these challenges while enhancing performance.

Among the new approaches noted above are technologies available today that generate highly ordered nano-scale films called self-assembled monolayers (SAMs), which feature an unprecedented mechanism for adhering to a wide variety of metals including precious metals that are normally unconsidered unreactive such as gold and silver, and creating a high-performance repellent surface to control the location of high adhesion materials. These SAMs are nano-scale self-leveling materials, which allow great freedom with low-cost application methods such as selective spraying, dipping, or wiping. Thicknesses of different versions of SAM's range from 2nm to 20nm are shown in [Figure 1](#). The

self-assembling nature allows a small variation in thickness for each version for significant performance predictability. Because of their nanoscopic scale, SAM-enabled treatments have no impact on electrical or thermal resistance, thereby imparting valuable functionality without negatively impacting performance. In addition to repellency, SAMs can be tuned chemically to impart adhesion promotion.

The semiconductor industry is continually searching for die bonding materials that take up less package area outside of the die-to-epoxy-to-substrate interface while exhibiting high adhesion to prevent delamination. An ideal material would also do the following: 1) offer excellent thermal conductivity to dissipate the heat generated from the die; 2) develop perfect contact between the chip and substrate without any voids; 3) be low stress to maintain silicon integrity; and 4) be able to withstand extreme temperatures without degradation. SAM-based nanocoating surface treatments, sometimes one-to-four nanometers thick, meet these criteria. They enable superior control of epoxy and solder location in semiconductor packaging, particularly in flip-chip, lead frame, and stacked-die packages. Die attach epoxy, epoxy mold

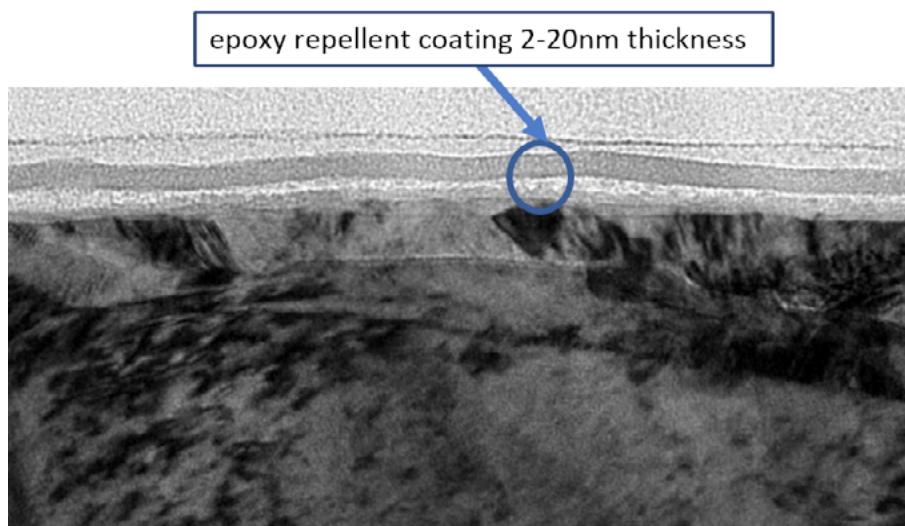


Figure 1: Epoxy repellent coating 2-20nm thickness.

Trial Lot	Surface Treatments	Die Attach - Supplier	Bleed Measurement (mm)
1	control	A-1	0.30
2	SAM #5	A-1	0.42
3	SAM #5 + anti-bleed01	A-1	0.12
4	SAM #5 + anti-bleed02	A-1	0.01
5	SAM #6	A-1	1.94
6	SAM #7	A-1	0.70
7	control	B-2	0.12
8	SAM #5 + anti-bleed 01	B-2	0.10
9	Sam #5 + anti-bleed 02	B-2	0.07

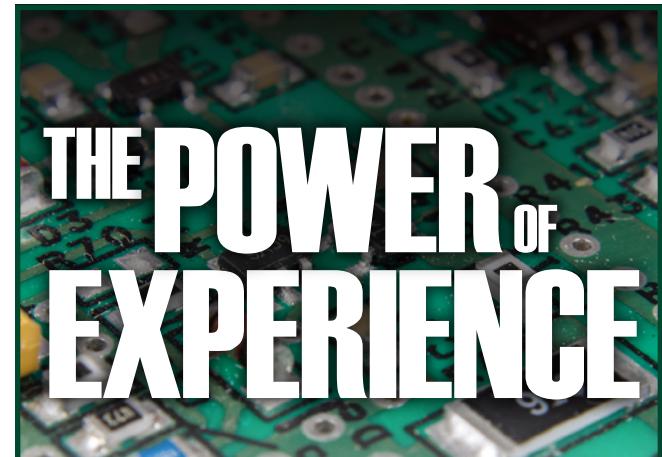
Table 1: Epoxy bleed measurements for various trial lots.

compound, solder die attach, flip-chip underfills, and motherboard underfills can have more precise design rules, taking up less substrate area, and saving motherboard space. Tests demonstrated an astounding 97% reduction of epoxy bleed when using a specific blend of SAMs compared to the standard material set (**Table 1**). Epoxy bleed is virtually stopped and assembly yield is increased with less epoxy location variability, which reduces wire bond fails and solderability interference. For complex flip-chip modules combined with surface mount technology (SMT) components, keep-out zones are greatly reduced and in some cases, epoxy molding is more reliable with less complicated epoxy overlaps.

The increasing use of delicate silicon interposers for 2.5D and 3D applications can cause complex challenges for the use of epoxy intended for bonding to forgiving laminate substrates. In addition to most metal surfaces, SAM nanocoating can also be applied to silicon, glass, or ceramic substrates. Hydrophobic coatings that have been highly developed for selective dispensing and jet printing can be used as a high-aspect ratio dam for high-volume epoxy flow control on printed circuit boards, flex circuits, and semiconductor modules.

In general, SAM surface treatments can extend the life of production equipment, expensive production consumables, glass displays, and tools by repelling epoxy, solder, flux, oils, grease, solvents, acids, and many other contaminating materials used in the production process. Existing surface treatments used in the oil and gas industry are being repurposed to protect expensive equipment components being relied on to shield, support, and protect. Because of this, components that were previously surrendered can now be reused.

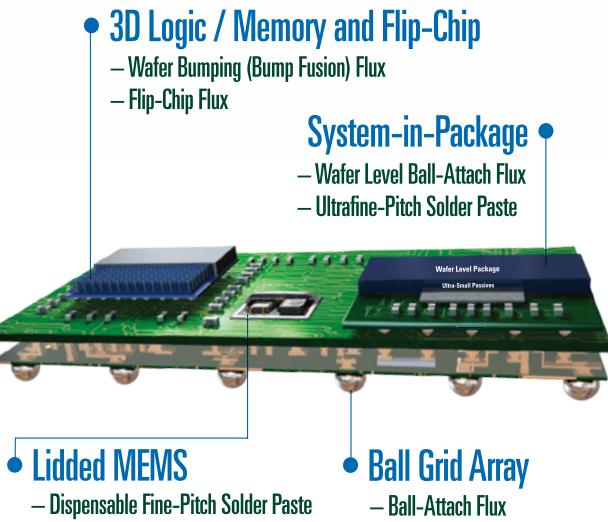
The use of SAM repellency characteristics can also address the ever-shrinking dispensing geometries for solder pastes and epoxies used in semiconductor packaging and board assembly that are being pushed to meet the next-generation materials requirements. Smaller dispense application tool diameters such as tubes, needles, and syringes, driven by smaller solder connections and tiny die attach areas, need better performing surfaces inside such narrow passages. Many epoxies and solder pastes contain more advanced and complex loaded and mixed ingredients that clog and drag inside small diameters. Originally developed for very small diameter glass tubing for jewelry, a super low viscosity family of SAM nanocoatings can be easily applied inside metal, glass, ceramic, and plastic needles, tubes, and syringes to increase material flow and reduce machine downtime.



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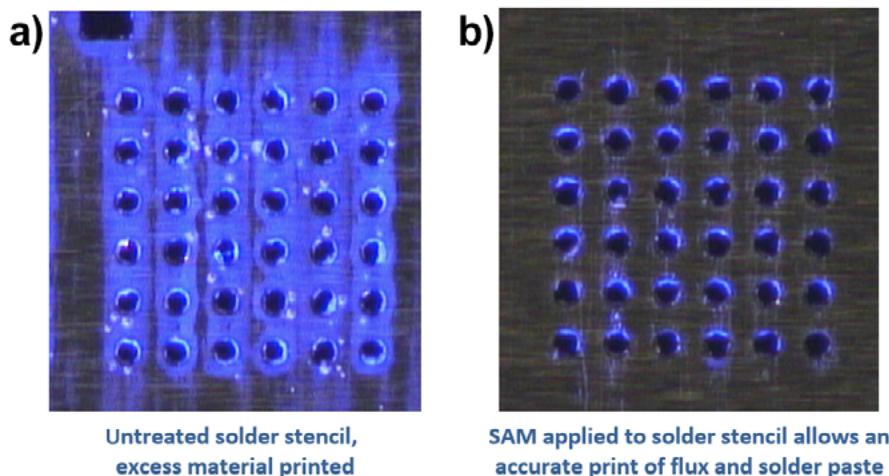


Figure 2: a) An untreated solder stencil showing excess material printed; and b) A solder stencil with SAM applied, which allows for an accurate printing of the flux and solder paste.

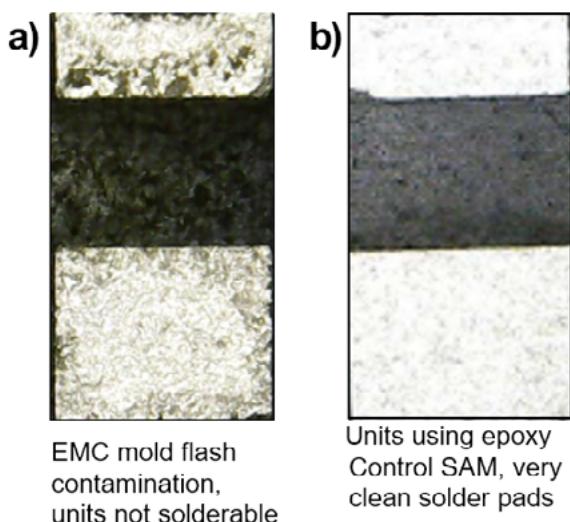


Figure 3: Elimination of EMC mold flash contamination: a) (left) Solder pads not solderable; and b) (right) Units using epoxy control SAM, very clean solder pads.

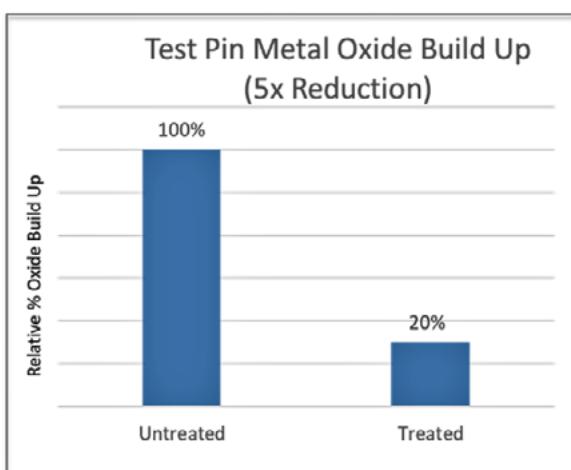


Figure 4: Reduce ATE test pin metal oxide build-up (5x reduction).

The solder printing stencil itself becomes increasingly critical as the size of components decreases and the density of placements increases. Fine-pitch solder balls with shrinking ball diameters on many solder ball array package types, fine-pitch small area solder pads on quad flat no-leads (QFN) packages, and closer placement of shrinking SMT passive components has manufacturers alert to the basic metal solder stencil. A high-performance solder stencil nanocoating – a surface treatment that was developed seven years ago using a similar underlying SAM technology – facilitates better solder print accuracy through solder printing stencils (**Figure 2**). It supports higher density interconnect packages and reduced motherboard area. Any high-end expensive metal solder stencil can be made to perform better with less solder bridging

by incorporating the use of an applied SAM. SAM surface treatments make expensive fine-grain stainless steel stencils drilled with high-precision lasers perform with even better solder printing accuracy at a low cost and with no stencil design changes. Tests show SAMs have the highest water contact angle and the highest oil contact angle in the solder stencil coating industry. In using a specific version of that SAM surface treatment, it may be possible to combine super-high water/oil contact angle SAM with other stencil coatings for a big step-up in performance.

Even the epoxy transfer molding encapsulation process, the standard for the majority of semiconductor packages, is being pushed by large format no-lead package lead frame strips causing excessive mold flash on QFN solder pads and resulting in yield loss. Not only can SAM nanocoatings be used at the lead frame strip level to prevent mold flash contamination of the ever-shrinking QFN solder pads, it can also be selectively and easily removed so as to not interfere with epoxy mold compound (EMC) adhesion to the EMC-lead frame mating surfaces (**Figure 3**). The resulting 3D multi-plane coating elevates lead frame manufacturing capabilities and design options are further improved. Independent tests revealed SAM use combined with this process eliminates yield loss on account of EMC mold flash preventing solderability.

Finer pitch solder balls and bumps and environmentally friendly harder surface solder balls are also instigating the prospect of using nanocoatings to prevent metal oxide build-up on final test automatic test equipment (ATE) and probe pogo pins. Nanocoatings provide higher test accuracy, faster throughput, and less frequent pin replacement – all of which creates higher performance at a lower cost. Because they are only 2-4nm in thickness, there is no electrical resistance increase and oxide build-up is reduced by five times (**Figure 4**). Nanocoatings are also being expanded to semiconductor probe cards, burn-in sockets and boards to extend the useful life of the metal contacts.

Hydrophobic coatings originally developed for motherboard waterproofing are making their way into semiconductor packaging. When applied as a moisture barrier for semiconductor components, corrosion and electromigration of metals such as silver or copper are prevented. In some cases, companies are pushing very low-cost packaging to achieve high-performance automotive conditions. Low-cost epoxy packages that failed full immersion, for example, pass with no failures when combining the standard epoxy layered with motherboard waterproofing polymers. Semiconductor packaging materials demonstrate improved moisture sensitivity ratings and, in some cases, a lower cost/higher electrical

performance material set, which is an added bonus. Additionally, high electrical conductivity silver can be a welcome performance boost for some parasitic sensitive devices and circuits.

The layers of materials that make up microelectronic packages and assemblies are comprised of dissimilar properties. They are challenged to maintain bond layer integrity on account of the differences in coefficient of thermal expansion (CTE) properties that cause stress between layers during temperature changes. Lead frame substrate materials have to be strong enough to withstand handling, yet compliant enough to bend, and have high enough thermal conductivity to dissipate heat generated by the IC. They also need appropriate electrical properties so electrical performance is not compromised.

In addition to simply coating the surface of a material on a 2D plane to enhance that material's performance, it is now possible to pattern nanoscale surface treatments to impart regional performance enhancements and new characteristics selectively on the same surface. Because of multiple cost-effective methods for applying surface treatments and selectively removing them, surfaces can be enhanced in 3D with a single step without the use of expensive tape. This has positive implications for complex package structures, chip stacks, and multi-tier soldering and underfill. For example, by allowing epoxy to adhere to one plane and then not adhere to the plane below, or preventing epoxy wicking, or solder adhering to a pad but not wicking to another plane, very complex tight geometry designs can become much easier to produce in high-volume production. Complex multi-plane lead frame packages used for flip-chip and multi-component hybrid modules can more easily have

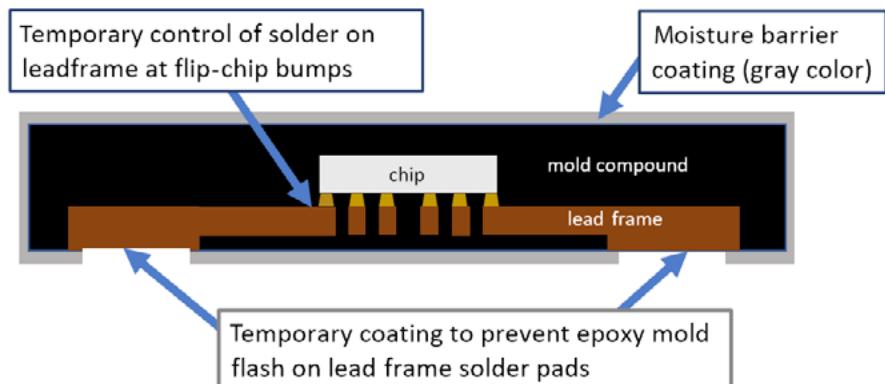


Figure 5: Coating locations for epoxy and solder location control and added moisture barrier.

different component attach methods with selected enhanced adhesion and repellency as needed (**Figure 5**). Wafer-level fan-out packages with dissimilar regions of epoxy outer regions and silicon-controlled inner regions can benefit by improving conductor trace adhesion and repelling solder from possible bridging. The use of conductive epoxies in general would become easier and more precise.

Surface treatments enhance adhesion of epoxy die attach and mold compounds to a variety of semiconductor package surface metals, such as gold and palladium. Epoxy adhesion enhancement treatment results in improved moisture sensitivity and better component moisture sensitivity level (MSL) ratings in semiconductor lead frame packages that do not have a MSL rating of one. Printed conductive inks and epoxies can potentially be printed thicker and with more precision by using a combination of SAMs that promote adhesion, as well as control dimensional accuracy.

The one constant in the semiconductor industry is change. In the last few months, there has been a huge increase

in inquiries for applying nanoscale SAM and waterproofing surface treatments to handle the accelerated change in semiconductor and system designs. Fueling the industry's future growth is artificial intelligence (AI), 5G, Internet of Things (IoT), advanced driver-assist systems (ADAS), augmented and virtual reality, and other new applications. Even high-volume production equipment benefits from increased performance accuracy, longer wear-life, less frequent replacement of consumables such as those used in ATE test, epoxy and solder paste dispensing, and solder printing. Advanced IC packages with various functions will be key enablers for moving toward application-specific and system-level solutions. Recently developed low-cost nanoscale materials are ready to meet the challenges of new OEM system demands, new package production formats, and new package designs. Surface treatments, when applied appropriately, will increase electrical performance, enhance reliability, reduce production costs, extend the useful life of existing materials, and enable lower cost material sets.

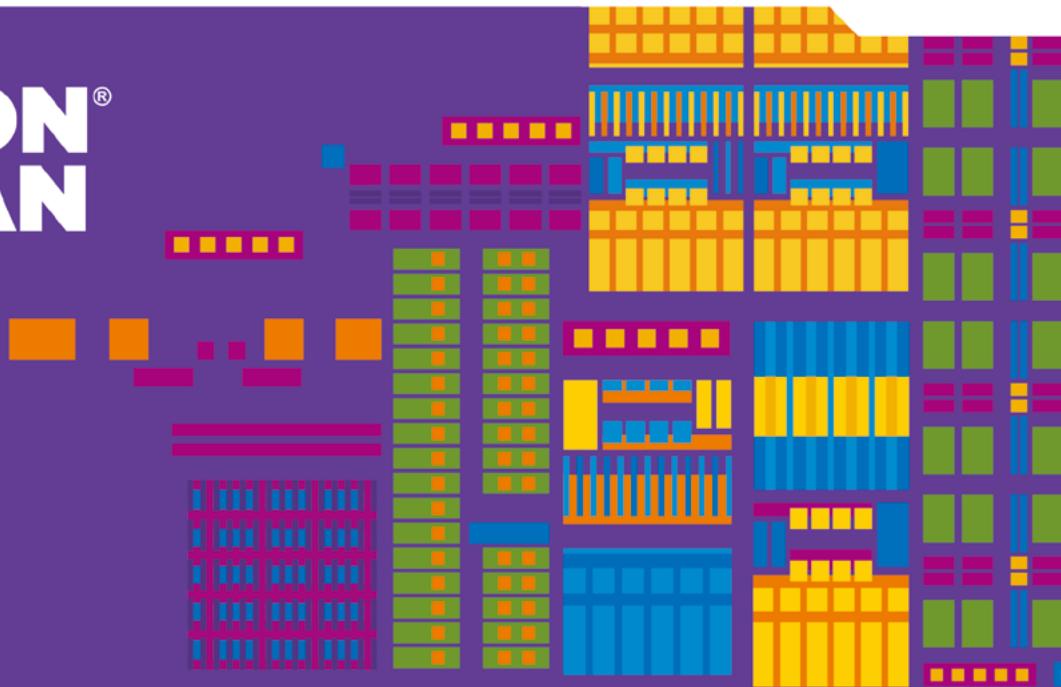


Biographies

Edward Hughes is Chairman & CEO of Aculon, Inc., San Diego, CA. In his 25-year career, he has led, built, turned around and sold technology and consumer product companies (Aculon, PowerMetal Technologies, TaylorMade-adidas Golf, Maxfli Golf, Dunlop Slazenger). In addition to sitting on several nonprofit boards, he is President of the Harvard Business School Club of San Diego, and teaches new venture management at the MBA program at U. of California, Irvine. He earned his Master's Degree from U. of Cambridge in England and his MBA from the Harvard Business School, where he graduated with High Distinction and was a George F. Baker Scholar.

Contact author: Don Cunningham is VP of Sales at Aculon, Inc, San Diego, CA. A pioneer in the electronics industry holding executive and management positions at Amkor Technology, General Electric Research, and Texas Instruments, he has developed and marketed multiple new semiconductor packaging technologies resulting in nine semiconductor and cell phone patents. His forte is navigating from product concept to production, introducing new technologies to high-value markets, commercializing and licensing technology and IP, and implementing original sales strategies for large revenue streams. He has a BS Industrial Management degree from the U. of Cincinnati. Email: cunningham@aculon.com

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INDUSTRY NEWS



Report from the 69th ECTC

By Mark D. Poliks, 69th ECTC General Chair [Binghamton University]

The IEEE Electronics Components and Technology Conference (ECTC) continues to break records in attendance living up to its reputation as the premier global event of the microelectronics packaging industry. The 2019 ECTC was held at The Cosmopolitan of Las Vegas, May 28 to May 31, 2019. The results, listed below, demonstrate that IC packaging is continuing to gain the attention of the semiconductor and electronics systems industry and that this event is the place to be to learn about the latest developments. Highlights from this year's ECTC include:

- 1563 attendees, the second highest attendance at an ECTC in its 69-year history;
- Attendees came from 25 different countries;
- 358 technical papers, presented in 36 oral and five interactive presentation sessions, including a student interactive presentation session (**Figure 1**);
- 18 professional development courses attended by 509 participants—a new record;
- 44 corporate sponsors with a record level of industry support, including two Platinum, 21 Gold, and 4 Silver sponsors; and
- 102 Technology Corner exhibit booths.

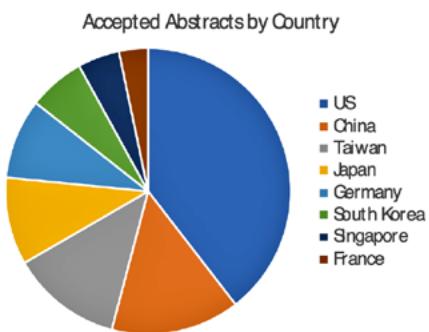


Figure 1: Accepted abstracts by country.

The success of the 69th ECTC is due to the many authors and invited speakers who publish and present their cutting-edge work on semiconductor packaging technologies, the more than 200 program subcommittee members who work for nearly a year to create the technical sessions, the exhibitors at the Technology Corner and the exceptional financial support from our conference sponsors. As General Chair of the 69th ECTC, I thank all of these individuals for their role in making this happen.

Fan-out packaging topics again the most attended sessions

Technical sessions on fan-out wafer/panel-level packaging (FOWLP/FOPLP) were again the most popular sessions for a fifth year in a row with as many as 400 attendees. Papers from key players in that industry segment, such as TSMC, NEPES Corporation, and Advanced Semiconductor Engineering, Inc., generated a lot of interest. This year, other well-attended sessions throughout the week included: Materials and Process Trends in FOWLP and PLP, Fine-Pitch Solderless Bonding, Fan-Out and Heterogeneous Integration, Power and Panel Assembly, and Bonding Manufacturing Technologies. Sessions on other packaging topics such as 2.5D/3D integration, flip chip, and opto-electronics, were also well attended.

Special sessions

In addition to the regular daytime sessions and courses, seven other well-attended special sessions and panel discussions were held on various days of the conference:

- ECTC Panel Session
 - Co-chaired by IEEE EPS President Avi Bar-Cohen of Raytheon and Karlheinz Bock of TU Dresden on “Future (Visions) of Electronic Packaging,”

- ECTC Plenary Session
 - Chaired by Tanja Braun, Fraunhofer Institute for Reliability and Microintegration (IZM) on “Sensors and Packaging for Autonomous Driving,”
- IEEE EPS Seminar
 - Co-chaired by Yasumitsu Orii of Nagase, Japan and Sheigenori Aoki of Lintec, Japan, on the “Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements,”
- Photonics Special Session
 - Co-chaired by Rena Huang of Rensselaer Polytechnic and Soon Jang of ficonTEC (USA) Corporation on “Photonics on the Cutting-Edge of Technology Evolution,”
- ECTC Special Session
 - Chaired by W. Hong Yeo of Georgia Tech and Mikel Miller of EMD Performance Materials on “Transient Electronics: A Green Revolution for Packaging?”
- ECTC/ITHERM Women’s Panel
 - Co-chaired by Kristina Young-Fisher of GLOBALFOUNDRIES, and Cristina Amon of University of Toronto on “Unleashing the Power of Diversity in our Workforce,” and
- ECTC/ITHERM Young Professionals Panel
 - Chaired by Yan Liu of Medtronic, Inc. on career development for young professionals with panelists from the EPS Board of Governors.

ECTC luncheon keynote address

Prof. John A. Rogers, Director of Center for Bio-Integrated Electronics at Northwestern University was the ECTC luncheon keynote speaker. In his talk, “Soft Electronic and Microfluidic Systems for the Skin,” Prof. Rogers described that recent advances in materials, mechanics and manufacturing have established the

foundations for high-performance classes of electronics and other microsystems technologies that have physical properties precisely matched to those of the human epidermis. The resulting devices can be integrated with the skin in a physically imperceptible fashion, to provide continuous, clinical-quality information on physiological status. His talk summarized the key ideas and presented specific examples in wireless monitoring for neonatal intensive care, and in capture, storage and biomarker analysis of sweat.

IEEE Electronics Packaging Society (EPS)

The sponsoring organization of the ECTC, the IEEE Electronics Packaging Society (EPS) hosted the Thursday luncheon. Avram Bar-Cohen, IEEE EPS President, presided over this event and said that technology areas critical for our future included advancing packaging for heterogeneous integration and for 5G and IoT networks that will support greater utilization of artificial intelligence, constantly growing data transfer rates, use of quantum devices for network security and ultimately, high-performance computing. David B. Durocher, the 2019-2020 Division II Director represented IEEE at the lunch. The following industry pioneers and innovators were also honored with 2019 IEEE EPS awards:



Figure 2: Ephraim Suhir (center) with David B. Durocher, the 2019-2020 IEEE Division II Director (left), and Avram Bar-Cohen, IEEE EPS President (right).



Figure 3: The 69th ECTC Executive Committee.

- Ephraim Suhir, the 2019 IEEE EPS Field Award for seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems (**Figure 2**).
- Jie Xue, the 2019 IEEE EPS Electronics Manufacturing Technology Award for over twenty years of technical contributions to the microelectronic packaging industry.
- S. W. Ricky Lee, the 2019 IEEE EPS Outstanding Sustained Technical Contribution Award for two decades of continuous contributions and professional leadership in multiple technical fields encompassed by EPS, including solder joint reliability, lead-free transition, 3D IC integration, and LED packaging.
- Chuan Seng Tan, the 2019 IEEE EPS Exceptional Technical Achievement Award for technical contributions and leadership in 3D packaging and integration, particularly on solder-less Cu-Cu bonding and innovations in TSV technology.
- Andrew Tay, the 2019 IEEE EPS David Feldman Outstanding Contribution Award for outstanding contributions in leadership in EPS conferences, chapter and Board of Governors over 28 years, notably the development of the EPS flagship Electronics Packaging Technology Conference in Region 10.

Joint events with ITHERM

The 2019 ECTC featured two joint events with its sister conference, ITHERM, that was also co-located at the same venue. The Wednesday evening Women's Panel and Reception, “Unleashing the Power of Diversity in our Workforce,” was co-chaired by Kristina Young-Fisher from

GLOBALFOUNDRIES, and Cristina Amon from the University of Toronto.

Another joint event — ECTC/ITHERM Young Professionals Panel and Reception — on Tuesday evening was chaired by Yan Liu from Medtronic, Inc. It consisted of panelists from the EPS Board of Governors (BOG), including EPS President, Avi Bar-Cohen. Participants were paired with BOG members for a series of engaging activities.

The ECTC tradition continues

The ECTC continues to enjoy record attendance and a filled-to capacity Technology Corner exhibit. Popular technical sessions on wafer-level fan-out technology, such as session #1, were filled beyond the allowed capacity of the meeting room. Ushers were needed to help seat attendees in available seats and additional chairs were added during the session break. Despite the challenges, the 69th ECTC was a resounding success and the attendees responded to the customer satisfaction survey with a high level of approval. The ECTC Executive Committee (**Figure 3**) is looking into various options for future meeting locations that could sustain, or even accommodate any anticipated growth in industry participation.

Mark your calendar for the 70th ECTC. Planning is already underway for the event, which will be held May 26 – 29, 2020, at the Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida, USA. The first call-for-papers has been issued; abstracts must be received by October 6, 2019. For more information, visit www.ectc.net.

INDUSTRY NEWS



International Wafer-Level Packaging Conference (IWLPC) Program Announced and Registration Now Open

"Advanced Packaging in the New Connected World"

Chip Scale Review and The Surface Mount Technology Association (SMTA) are pleased to announce the program for the 16th annual International Wafer-Level Packaging Conference. The IWLPC will be held October 22-24, 2019 at the DoubleTree by Hilton Hotel in San Jose, California.

The technical sessions on Tuesday and Wednesday are organized into the three tracks: Wafer-Level Packaging, 3D Packaging, and Advanced Manufacturing and Test. The Wafer-Level Packaging (WLP) track features sessions on materials, reliability, metrology, processing, and new technology like Fan-Out WLP. The 3D Packaging track features sessions on design, test, characterization, wafer bonding, chip stacking, and processing for fan-out. The Advanced Manufacturing and Test track features sessions on process materials, equipment, inspection, and more.

Packaging technology experts John Lau, Ph.D., Unimicron Technology; John Hunt, ASE (US) Inc.; Gilad Sharon, Ph.D., ANSYS and Jeff Gotro, Ph.D., InnoCentrix, LLC, are scheduled to lead half-day workshops on Thursday, October 24, 2019.

Registration for IWLPC is now available online. Discounted rates are available for conference registration made on or before September 27, 2019. Visit www.iwlpc.com for more information.

Contact Jaclyn Sarandrea at +1-952-920-7682 or jaclyn@smta.org with questions.



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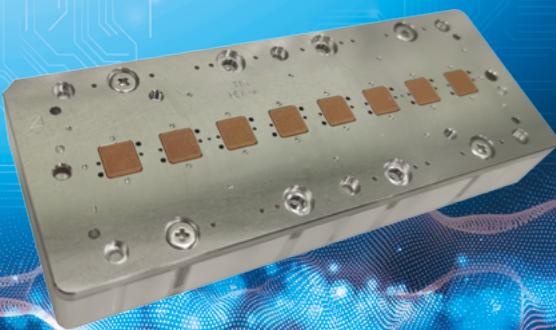


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