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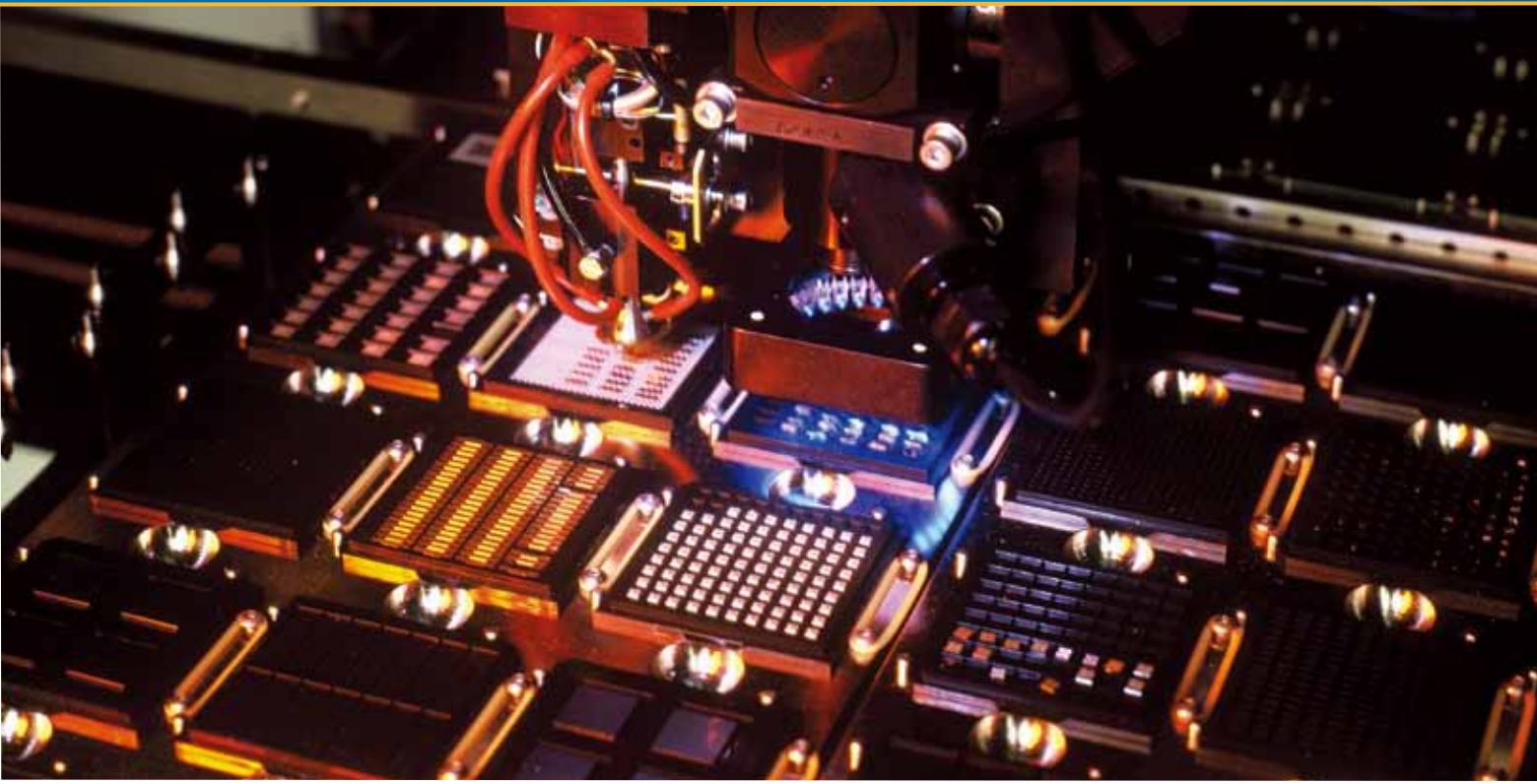
*The International Magazine for the Semiconductor Packaging Industry*

Volume 16, Number 3

May - June 2012

- Copper Pillar Bumping
- Update on PoP Test Sockets
- Detecting 3D Die-Attach Failures
- 3D Integration & the Supply Chain Shift
- Glass Interposers: Superior Material at Lower Cost
- **International Directory of Die & Flip Chip Bonders**





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May June 2012  
Volume 16, Number 3



The front cover complements our feature article on copper pillar bumping technology.

The 300mm wafer contains roughly 20 million copper pillar micro-bumps. The distinctive die footprint hosts a full matrix bump array of 51K bumps at  $\leq 45\mu\text{m}$  pitch.

Photo courtesy of Amkor Technology and Xilinx, Inc. with special thanks to the Amkor Technology Korea R&D and Packaging Engineering team.

**Chip Scale**  
REVIEW

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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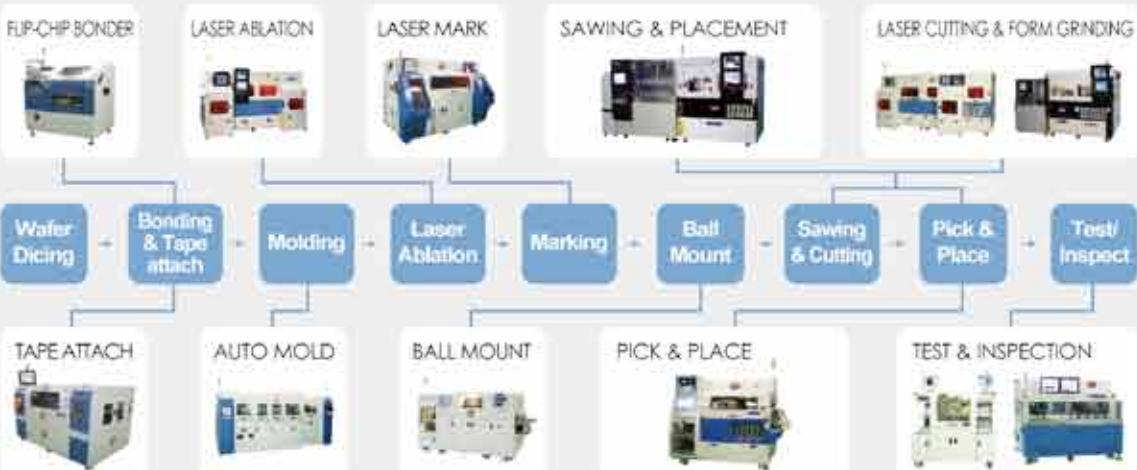




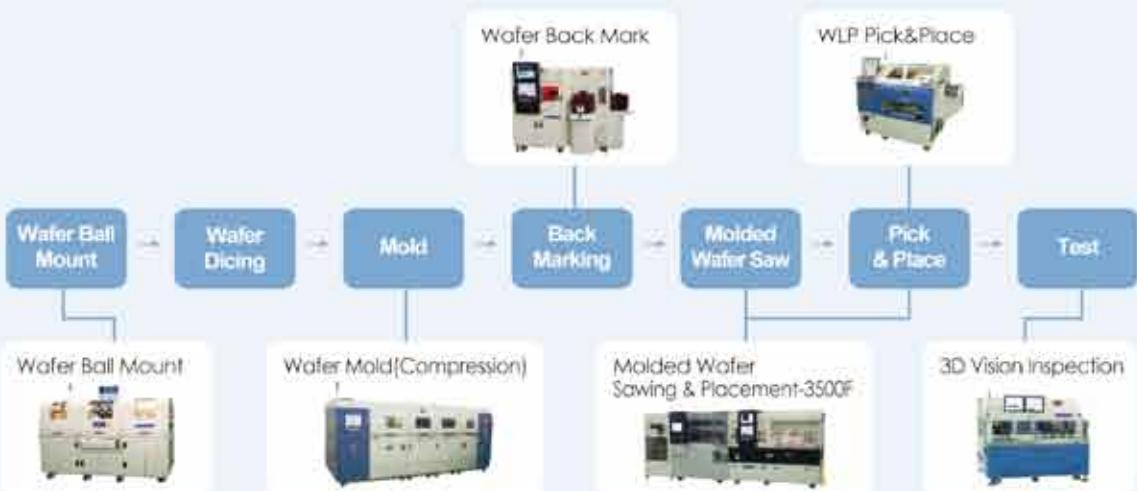
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# FROM THE PUBLISHER



## Let's Have a Really Big Show

*Edward Vincent "Ed" Sullivan (September 28, 1901 – October 13, 1974)*

**T**

he industry is abuzz this time of year with events such as the SEMI Arizona Forum addressing the 450mm Wafer Transition, the 10th Annual MEMS Technology presented by Meptec, the Semico IMPACT Conference Series: The IP Ecosystem and the 62nd Electronic Components & Technology Conference (ECTC).

If you missed the details of these events in Chip Scale Review's May monthly e-newsletter **CSR Tech Monthly** you can catch up on them by visiting Chip Scale Review's website [www.chipscalereview.com](http://www.chipscalereview.com)

If you have not booked your plans for this year's ECTC being held at the Sheraton San Diego Hotel & Marina May 29 - June 1st, it is not too late. Read about this year's event in the Industry News section further in this issue. Over 300 technical papers in 36 sessions are presented covering emerging and contemporary topics, such as MEMS, 3D/TSV, and RF packaging in addition to the array of standard topics in advanced packaging technologies, interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, electronic components, and simulation.

"Typically 25 states and 20 countries submit abstracts," said Dr. Senol Pekin, the 62nd ECTC Program Chair. There will be a special appearance by Arizona's Secretary of State Ken Bennett who will preside over an informal press conference on Tues May 29th to discuss doing business in Arizona. Pekin further comments, "Arizona typically ranks fourth in terms of papers presented at the conference". CSR is once again the Official Media Sponsor for ECTC. Pick up a copy while you are attending the conference. You will not want to miss the exhibits on May 30-31st. Exhibits Chair Bill Moody comments "There are a total of 79 exhibitors in 81 booths plus 2 tabletops for a total of 81 exhibitors. This is the most exhibitors we have had at ECTC. 26 are first time exhibitors. Many of the first time exhibitors are involved in 3D/TSV technology and were attracted by ECTC's emphasis in this area."

The technical committee for the **2012 IWLPC** - the International Wafer-Level Packaging Conference is well underway putting the technical program together. Contact any one of the technical committee members in their track if you wish to submit an abstract but don't wait there only a few openings left.

Exhibits is officially open and limited to 50 spaces for IWLPC. Contact your CSR sales rep or visit the IWLPC website [www.iwlpc.com](http://www.iwlpc.com) for further details. Be sure to mark your calendar for IWLPC Nov 5-8, 2012 being held at the Doubletree Hotel in San Jose, California. The Platinum, Gold and Flash Drive Sponsorships are sold out. The Silver Level Sponsorships, Wi-Fi, Reception, Lunch and Refreshment are still available and are on a first come, first serve basis.

**Enjoy the show(s)!**

*Kim Newman*

Publisher

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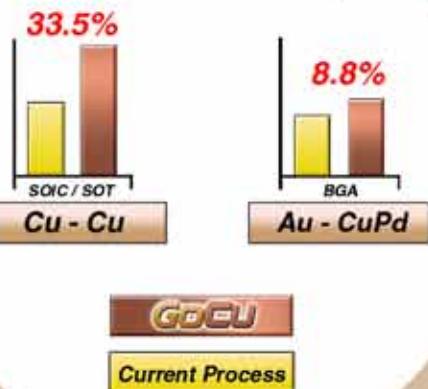
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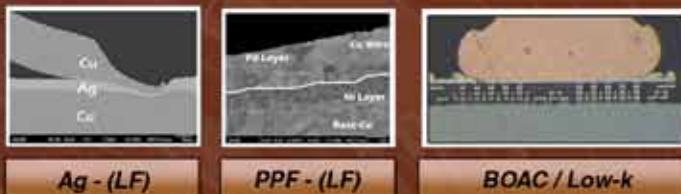
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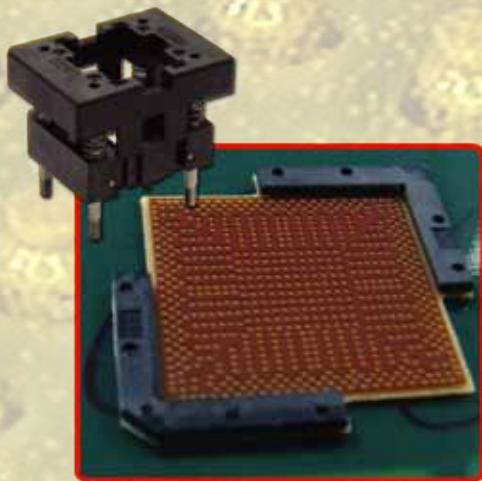
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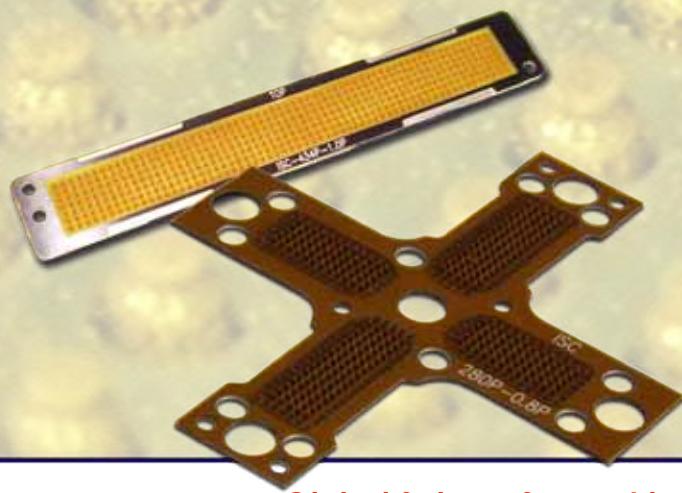
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# GUEST EDITORIAL



## What's New with Interposers?

By Phil Marcoux [PPM Associates]

**I**nterposers are emerging as a new element inside an IC package. In time they may be as important as underfill epoxy is to flip chips mounted on BGA substrates and PCBs.

One of the early uses of an interposer was to enable interconnection of very fine pitch ( $<350\mu\text{m}$ ) flip chips onto a BGA substrate without having to fabricate the high density interconnect (HDI) with its layers of tiny vias and small traces and spaces on the BGA substrate. This approach promised to be less expensive even though it required an additional assembly element.

As interest in stacking multiple die within a package is growing, it has occurred to many that the leap from 2D, single chip assembly into 3D stacked assembly is too much, too soon. Therefore, the term 2.5D was coined to express the use of an interposer as a “stepping stone” from 2D to 3D.

2.5D advocates explain that silicon is the ideal interposer material. As a substrate, it provides a versatile and reasonable approach to replacing wirebonds and large solder balls since silicon is fairly stable and can be fabricated to form small diameter through silicon vias (TSVs) and use  $<100\mu\text{m}$  microbumps, such as copper pillars as electrical interconnects. Other substrate materials such as glass and even HDI PCBs may be just as ideal.

There are many performance benefits with this approach including improved signal integrity due to lower electrical parasitics, lower power due to shorter traces between die, and improved reliability due to better match of thermal and better thermal cooling.

As interposers and stacked die use increases, new discoveries are being made as to the benefits of both. One possible interposer benefit is the ability to put circuit elements closer to where they are needed, such as ESD protection and filter capacitors. Currently, most die have ESD protection, usually diodes or transistors, fabricated on the chip. Often the ESD protection devices are placed directly under the bond pads as a space saver. When multiple die are stacked, the combination of ESD circuits connected in parallel add a large signal delaying capacitance on the signal lines. Fabricating ESD protection as part of the interposer reduces the capacitance and puts the protection closer to where it's more effective. Similarly, the capacitors needed to filter power and ground noise and jitter can be made smaller and more effective if they are fabricated on the interposer and closer to the ICs.

Another silicon interposer benefit is to exploit silicon's versatility. One example is the ability to etch trenches into the interposers along with the pits for the TSVs. The vias are filled with metal for electrical conduction and the trenches can be used to contain and accurately align fiber optics in the product, providing electro-to-opto interfaces.

It's an incorrect assumption that the coefficient of thermal expansion (CTE) of a silicon interposer is the same as the silicon IC. Adding copper-filled TSVs to silicon actually increases the CTE. Plain silicon has a CTE of 2.7 ppm/ $^{\circ}\text{C}$ . Mounting a large plain silicon die on a BGA substrate (CTE of approximately 17 to 22 ppm/ $^{\circ}\text{C}$ ) may incur a significant

reliability risk even if an underfill epoxy is injected between the die and the BGA substrate. This is due to the large CTE mismatch and the increasing lack of tolerance for stress in ICs that are fabricated from smaller lithography nodes in order to increase their density. Placing a TSV-loaded interposer in between the IC die and the BGA substrate reduces the reliability risk by reducing the magnitude of the mismatch between the assembly elements. The CTE of a silicon interposer laden with copper-filled TSVs can range from 5 to 8 ppm/ $^{\circ}\text{C}$ . This may be enough to mitigate the large CTE mismatch. New underfill formulations are being developed to accommodate the smaller gaps and needs of this stack.

Glass continues to be pursued as a silicon alternative. Advocates promote the ability to fabricate glass interposers in large area panels as more economical than silicon. There are a number of issues holding glass back but these are being addressed. Issues include the ability to etch small vias, handling, and flatness.

There are several interposer applications where the thermal conduction properties of silicon and even glass will hinder performance. In these applications the thermal insulating properties of an epoxy or aramid fiber substrate offer advantages.

It's my opinion that interposers are far from being a stepping stone for stacked multichip package assembly and are an essential foundation for a new exciting area of IC packaging. 

*Phil Marcoux, consultant, PPM Associates, may be contacted at oneppm@ymail.com*

# MARKET TRENDS



## Strategies of the Top Ten OSATS

By Sandra Winkler [New Venture Research]

Outsourced semiconductor assembly and test (OSAT) companies package bare integrated circuits (ICs), otherwise known as die, thus converting these die into chips. These companies contract with semiconductor or fabless companies, who either do not have packaging capability or do not have sufficient capacity to meet all their own packaging needs. Thus OSAT companies are also referred to as contractors.

### What Does The package Do?

The package surrounding the die provides mechanical protection, fans the electrical connections to something that can be routed to a PCB, and can have thermal enhancements such as heat sinks, heat slugs, and thermal interface materials (TIMs). All these chips are tested prior to placement on the PCB, and testing is a service many of the OSAT companies offer.

Having the OSAT company develop leading-edge packages makes sense. The research and development cost associated with a given package can be spread over many companies, and thus be more cost effective for the OEMs.

There are approximately 60 OSATs around the world competing for the outsourced package assembly dollars. The top ten comprise 60% of this OSAT market, as seen in **Figure 1**. Strategies vary, with some companies specializing in assembling multitudes of smaller packages, as is Carsem's strategy, and others clamoring for the higher value-added advanced packages, such as 3D solutions, FBGAs, BGAs, and the like. Amkor, ASE, SPIL, and STATS ChipPAC

fall into this latter category.

The top ten OSAT companies are, in order of IC package assembly revenue:

- ASE, Inc.
- Amkor Technology
- Siliconware Precision Industries Co., Ltd. (SPIL)
- STATS ChipPAC, Ltd.
- PowerTech Technology Inc.
- Signetics High Technology, Inc.
- United Test and Assembly Center, Ltd. (UTAC)
- Carsem
- Orient Semiconductor Electronics (OSE)
- Unisem

### ASE, Inc.

ASE is the top revenue OSAT company, with \$3,649.5M in package assembly revenue in 2011. Package assembly is 55% of their net sales, thus total revenue for assembly, test, and other services is \$6.308M. The company offers a broad spectrum of packages to fit a variety of needs, offering a one-stop shop with their services. While they assemble lower-end packages, their main focus and support is with the top dollar value-added packages that bring more to the bottom line. Being vertically oriented to include package substrates in their product

portfolio gives them a competitive edge in the array package business.

### Amkor Technology

Founded in 1968, Amkor pioneered the outsourcing of IC assembly and test and is now a strategic manufacturing partner for more than 200 of the world's leading semiconductor companies and electronics OEMs. The company reported \$2,493M in package assembly revenue in 2011. A key Amkor strategy is to provide customers with innovative microelectronics assembly and test solutions to their challenging advanced packaging problems.

Customers enjoy time-to-market benefits when they work with Amkor in an alpha customer engagement for the development of the new package solution to meet their device's product requirements.

Amkor has built relationships with a number of system design companies to better understand long-term interconnect and packaging performance requirements and in many cases, such as package-on-package (PoP), had active co-development projects with system design companies that enabled developing solutions that address system and device integration requirements.

Top 10 % of Total OSAT Market	2009	2010	2011	2012	2013	2014
Percent of revenue of the top ten of the total OSAT market OSAT % of Total IC Market	63.2%	64.6%	60.0%	61.8%	61.9%	61.6%
Percent of the total OSAT companies of the total IC market	21.7%	20.6%	22.2%	23.4%	23.6%	24.1%
Top Ten OSAT % of Total IC Mkt Percent of the top ten OSAT companies of the total IC market	13.7%	13.3%	13.3%	14.5%	14.6%	14.9%

**Figure 1.** Top 10% of the total OSAT Market. (Source: *The Worldwide IC Packaging Market*, New Venture Research.)

## Siliconware Precision Industries Co., Ltd. (SPIL)

SPIL offers a variety of packages within their portfolio, but focuses mainly on those with high growth rates for handheld electronics—QFN and MCP solutions—which include stacked packages and systems-in-package (SiPs). SPIL ramped up their package and service options approximately seven years ago, putting them on a fast pace towards higher revenue earnings. Wafer bumping, final test, and drop shipment became part of their service portfolio. With \$1,821M in package assembly revenue, SPIL is in third place in the package assembly line-up.

## STATS ChipPac, Ltd.

STATS ChipPAC is a merger of STATS, which had a focus on final test, and ChipPAC, a package assembly company. This marriage, which occurred approximately five years ago, propelled them forward, providing complete back-end service. They added wafer bumping as a service two or three years ago, thus completing their flip chip line. They are in fourth place with \$1,365M in assembly revenue only, not including test. They offer a host of QFN, FBGA, and MCP solutions (stacked packages, SiPs), which cater to the handheld communications market. Communications constitute 67% of their package assembly revenue.

## Powertech Technology, Inc.

PowerTech is a more recent entrant into the package assembly business, entering in 1997. The company assembles a large number of MCPs, and focuses on packaging memory devices. Package assembly is all performed in China. As with STATS ChipPAC, final test is a large part of their business. Package assembly is \$685M of their revenue.

## Signetics

Signetics offers a number of array packages, in both wire bond and flip chip formats. The company also offers SO, QFN, QFN, and MCP solutions to round

out its offerings. Its portfolio is not as broad as the top leaders, and focuses more on the top competing packages, rather than a complete mix of all packages, which would include DIPs, TSOPs, CCs, DFNs, and WLPs. The company aims its products toward cell phones and consumer markets

to flip chip products for networking and graphics applications.

## United Test and Assembly Center, Ltd. (UTAC)

UTAC offers a wide mix of package  
*(continued on Page 48)*

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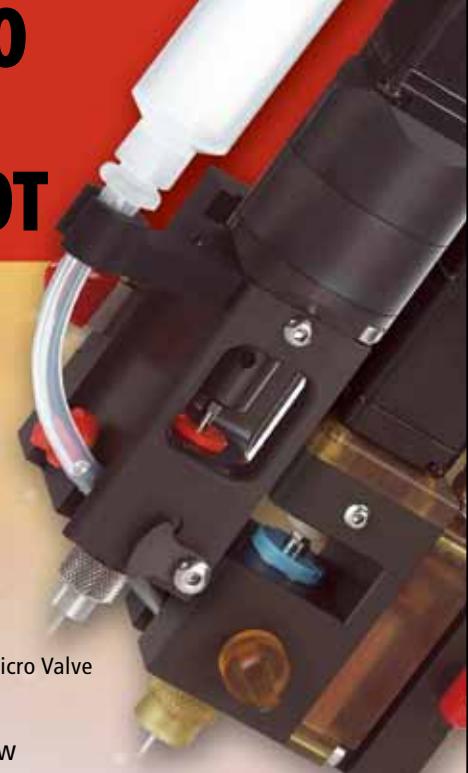
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# INDUSTRY NEWS



## IWLPC Announces 2012 Event Sponsors

**S**MTA and Chip Scale Review are pleased to announce that plans for the 9th Annual International Wafer-Level Packaging Conference (IWLPC) and Tabletop Exhibition, scheduled to take place November 5-8 2012, in San Jose CA, are well underway. This premier industry event explores leading-edge design, material, and process technologies being applied to wafer-level packaging applications. There will be special emphasis on the numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand WLP solutions for integration, cost, and performance requirements. In addition to professional development courses, the conference includes three tracks with two days of technical paper

presentations covering: Wafer Level Packaging; 3-D (Stacked) Packaging; and MEMS Packaging. The IWLPC Technical Committee invites all those interested to submit an abstract for this program. Contact a technical committee member or visit the website and submit your abstract at [www.iwlpc.com](http://www.iwlpc.com). **The Call for Papers has been extended to May 14, 2012.**

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Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
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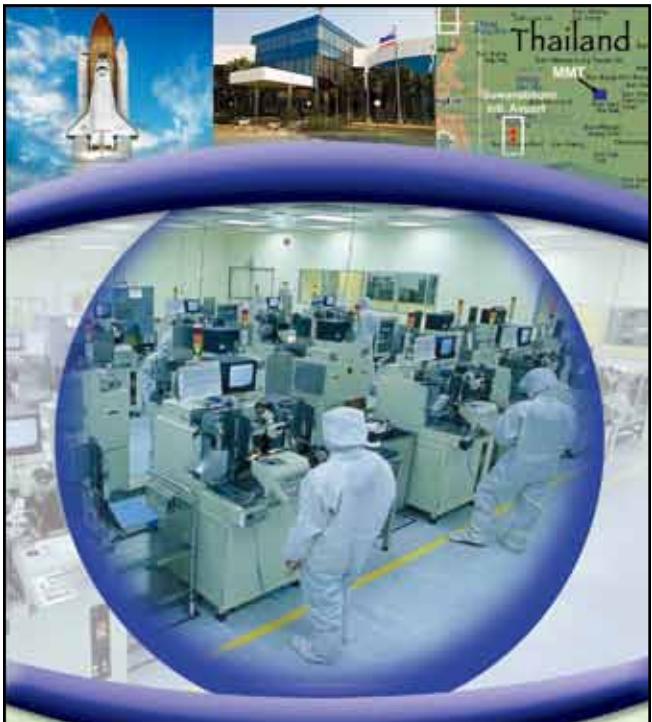
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## Arizona Secretary of State to visit the 62nd ECTC



Recognizing the impact of microelectronics in the Grand Canyon State, Arizona's Secretary of State Ken Bennett will

attend the 62nd Electronic Components and Technology (ECTC) conference on May 29, 2012 in San Diego. Arizona is home to more than 60 microelectronics companies, world-class engineering degree programs and a burgeoning workforce.

ECTC, which is sponsored by the IEEE Components Packaging and Manufacturing Technology Society (CPMT), is the premier event in the industry where over 300 technical papers in 36 sessions are presented covering emerging and contemporary topics, such as MEMS, 3D/TSV, and RF-packaging, in addition to standard topics in advanced packaging technologies, interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, electronic components, and simulation.

"Typically 25 states and 20 countries submit abstracts," said Dr. Senol Pekin, the 62nd ECTC Program Chair. "Arizona typically ranks fourth in terms of papers presented at the conference. In fact, some have labeled the region as "Silicon Desert". Industry leaders recognize that Arizona's business climate is as friendly as its actual climate. We're excited to have Secretary Bennett attend the conference and talk about the benefits of doing business in Arizona."

"This will be an excellent opportunity for me

to interact with experts and leaders from the microelectronics industry," said Secretary Bennett. "These high-tech industries fuel education, employment and business opportunities in an environmentally friendly manner. The role of microelectronics in Arizona's economy and around the globe cannot be understated. Arizona is open for business and we are aggressively pursuing cutting-edge businesses like these. It's my goal to bring a couple of these companies home with me!"

## Assembléon Announces New Management Team

One year after its privatization from Royal Philips, Assembléon's management has been transferred to a new CEO and management team, comprising individuals with experience

(continued on Page 46)

An advertisement for the Plasma Etch PE-50 plasma etching system. The ad features a green background with white text and a large image of the equipment. The top section reads "PLASMA ETCH" and "PROGRESS THROUGH INNOVATION". Below that, it says "AFFORDABLE PLASMA ETCHING SYSTEM". The middle section highlights "THE PLASMA ETCH, INC. PE-50 IS OUR LOWEST PRICED PLASMA SYSTEM." and "SURFACE ENERGY MODIFICATION WITH PLASMA TREATMENT YIELDS IMPROVED MARKABILITY, ADHESION AND EASE OF ASSEMBLY WITH A LOW ENVIRONMENTAL IMPACT.". The bottom section mentions "REMOVES ORGANICS AND IMPROVES BONDS.". On the right side, the model "PE-50" is shown with the price "STARTING AT \$ 10.950". At the bottom, it says "TO LEARN MORE VISIT OUR WEBSITE OR CALL US TODAY!" and provides the website "WWW.PLASMAETCH.COM" and phone number "775.883.1336".

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# Fast and Easy Method for Detecting 3D Die-Attach Failures

By John Parry, Ph.D. [Mentor Graphics Corporation]

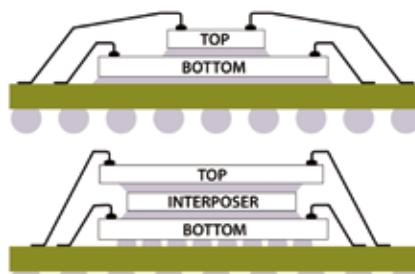
Three dimensional (3D) stacked die packages are common today in hand-held devices, especially in cell phones and digital cameras. For these system-in-package (SiP) designs to be possible, the chips in the die stack are thinned down to some tens of microns to reduce the overall package height. The thinned chips are attached to each other and to the substrate by thermally conducting die-attach material or die-attach film layers.<sup>1</sup> However, the die-attach material is not as a good a thermal conductor as the die themselves.

Thermal problems in stacked die packages multiply. Heat dissipation in the top die of a stacked dice package results in much higher junction temperatures than if the circuit was in a single-die package. Consequently, 3D stacked die packages are limited to low-power electronics, mostly memory circuits.

In typical 3D stacked die packages, wire bonding is used for the interconnection to the substrate.<sup>2</sup> The structure is usually pyramidal (**Figure 1**, top), or it contains a spacer or interposer (**Figure 1**, bottom) to facilitate wire bonding and help spread the heat. With the most advanced chip-on-flex technology, as many as 50 stacked chips have been reported in a single package.<sup>3</sup>

Delamination or a void in any of the die-attach layers is a major risk and will result in locally increased thermal resistance, which can cause overheating that will quickly ruin the device. For this reason, quality control of the die-attach material and die-attach process used in stacked die packages is very important.

The structure-function-based methodology is recommended as the fastest and least expensive technique for the qualification of die-attach problems in 3D stacked die packages.<sup>4</sup> It allows us to



**Figure 1:** Typical structure of stacked die packages.

find the severity and location of possible die-attach problems with a single thermal transient measurement and the subsequent direct mathematical transformations within a few minutes. The obtained thermal transient curves are usually easy to evaluate; and, for a large number of samples, the evaluation may be automated.

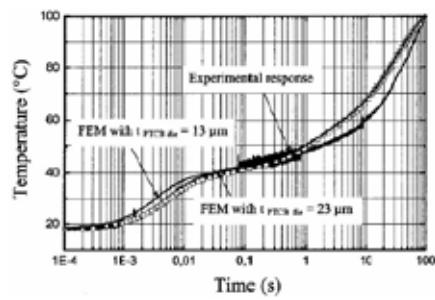
During the development phase, the thermal response of a detailed thermal model gives a baseline response for a package with perfect die-attach between all die. During pre-production prototyping, the thermal response of samples are measured and compared with the simulation model. If the die-attach quality is as designed, the measured and simulated curves will closely overlap. However comparing the simulated and measured transient temperature vs. time responses gives no clue as to the cause of any differences (**Figure 2**). For this, we need to use structure functions.

Structure functions provide a map of the cumulative thermal capacitances of the heat flow path with respect to the thermal resistances measured from the location of the heat source on the die surface to the ambient. They are obtained by direct mathematical transformation of the measured and simulated thermal transient curves.<sup>5</sup>

Where the two curves depart from

one another identifies which die-attach layer is affected, and the difference in the thermal resistance shows how bad the actual die-attach is. This provides a unique way to identify and hence correct die-attach processing issues ahead of full production, and it allows the simulation model to be calibrated for other unknowns, such as thermal conductivity of the mold compound, so that differences in the die-attach resistance are clearly resolved.

This approach is useful during the accelerated testing that is required before a product can go into volume production. Accelerated aging at elevated temperature and humidity (HAST) is undertaken to ensure the lifetime of the product in the field. This is a time-consuming process that takes weeks and in many cases months to complete. Consequently, it is imperative to harvest as much information about the reliability of the package during this exercise. Structure functions can be derived from the thermal response of



**Figure 2:** Data results for finding the die-attach thermal resistance.

packages while they are still mounted on the test board at intermediate stages during the HAST process so that the thermal degradation of the die-attach layers can be profiled against the number of thermal cycles.

Once in production, again using the structure function methodology, packages with die-attach problems can be quickly

and easily detected. The steps involved in using the method are as follows:

1. Create the structure function of a good physical sample as a reference (done during development).
2. Similarly create the structure function from the measured thermal transient response of a package from the batch of parts to be evaluated.
3. Compare the structure function of the known good (reference) device to the structure function of the device from the batch under test. The shift in the appropriate points in the structure functions gives the increased thermal resistance of the layer(s) in question.

Unlike scanning acoustic microscopy, which is expensive, time-consuming, and sometimes results in blurred images of the voids, the structure function approach directly measures the thermal significance of the voids. If a die-attach layer is not directly in the heat flow path, voids in the layer will have little influence on the die

temperature and so may not adversely affect the lifetime of the part. Structure functions show the effect of process window variation on die-attach thermal quality, giving manufacturers confidence to release batches of parts into the market.

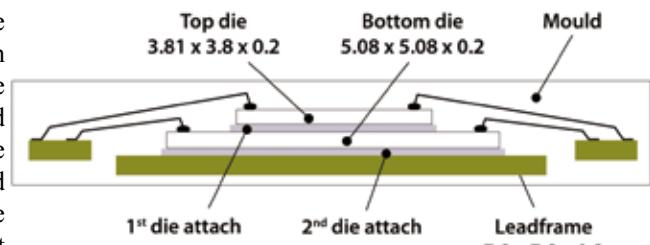
### Examples

In one example,<sup>6</sup> the measured samples contained stacked thermal test dies<sup>7</sup> in a pyramidal structure, packaged in LQFP144 packages. **Figure 3** shows a cross-section of the measured packages. The top die was used as a heater and temperature sensor, however different die in the stack could also be used as a heater/sensor, providing further information and helping pinpoint the location of any die-attach problems, for example during an accelerated testing program. The bottom was connected to a cold plate to ensure one-dimensional heat flow from the top die

toward the cold plate. The T3Ster thermal transient tester<sup>7</sup> was used to obtain thermal transient measurements on the top die.

The structure function constructed from the measured heating curve is shown in **Figure 4**. The horizontal axis represents the thermal resistance values measured from the heated top die toward the ambient. The corresponding thermal capacitance values are represented on the vertical axis in logarithmic scale. The first vertical step of the function refers to the thermal capacity of the top die itself.

The next element of the structure is the die-attach under the top die; this appears with its high thermal resistance value, as an almost horizontal section in the



**Figure 3:** Cross-section of the measured packages.

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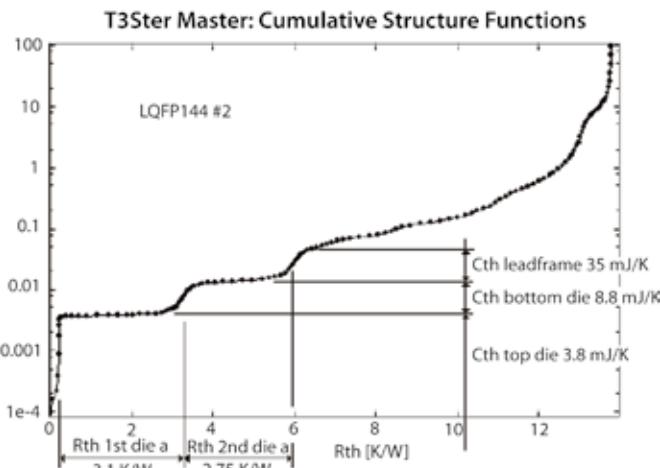
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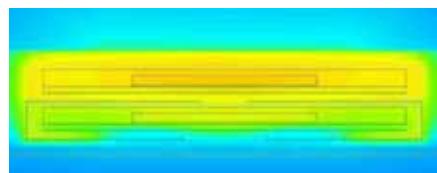
**Figure 4:** The obtained structure function of a good sample of the package of the baseline design.

structure function. The next very steep section of the curve refers to the bottom die; both the thermal resistance and the thermal capacitance values of this die can be read from the function.

This methodology also works well in the case of functional dies stacked in the package.<sup>8,9</sup> The main advantages are the speed and simplicity of the method. All the failure analysis can be done within the time of the thermal transients in the package because the computer time needed for the calculation of the structure functions is negligible, and the calculation is a built-in function of the tester.

In another example, a leading supplier of high-density memory stacking solutions used thermal simulation software\* to ensure that new products met thermal management requirements. Thermal performance is critical to the designs, which double, triple, or quadruple memory in the same physical footprint as the underlying packaged component. One of the company's most important design challenges is to ensure that the stacked packages have superior thermal performance (**Figure 5**).

The company's engineers modeled the new design in the simulation software to obtain the junction temperatures of the



**Figure 5:** Thermal simulation software models stacked memory in a JEDEC still-air environment.

devices in the stack. They evaluated several ideas to thermally improve the performance of the low profile stack using the simulation software tool's model. By making minor modifications to the stack, they found that they could equal the thermal performance of the low-profile stack with

2. Charles W.C. Lin, Sam C.L. Chiang, T.K. Andrew Yang, "3D Stacked Packages With Bumpless Interconnect Technology," 2003 IEEE/CPMT/SEMI International Electronics Manufacturing Technology Symposium.
3. R. Fillion, R. Wojnarowski, C. Kapusta, R. Saia, K. Kwiatkowski, J. Lyke, "Advanced 3-D Stacked Technology," 2003 Electronics Packaging Technology Conference.
4. JESD51-14 "Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow through a Single Path," November 2010, [http://www.jedec.org/sites/default/files/docs/JESD51-14\\_1.pdf](http://www.jedec.org/sites/default/files/docs/JESD51-14_1.pdf). Structure functions are described in details in Annex A of the JEDEC JESD51-14 Standard.
5. M. Rencz, V. Székely, B. Courtois, L. Zhang, N. Howard, L. Nguyen, "Die Attach Quality Control of 3D Stacked Dies," Proceedings of the IEMT Symposium of SEMICON West, 2004, pp. 78–84.
6. <http://www.delphi.com/pdf/techpapers/2004-01-1681.pdf>
7. <http://www.mentor.com/products/mechanical/products/t3ster/>
8. M. Rencz, V. Székely, A. Poppe, B. Courtois, L. Zhang, N. Howard, L. Nguyen, "Testing the Die Attach Quality of 3D Stacked Dies," Proceedings of IMECE2004 ASME International Mechanical Engineering Congress, 2004.
9. O. Steffens, P. Szabo, M. Lenz, G. Farkas, "Junction to Case Characterization Methodology for Single and Multiple Chip Structures Based on Thermal Transient Measurements," Proceedings of the 21st IEEE SEMI-THERM Symposium, 2005.

## References

1. Stephane Pinel, et al., "Thermal Modeling and Management in Ultrathin Chip Stack Technology," IEEE Transactions on Components and Packaging Technologies, Vol. 25, No. 2, 2002.

John Parry, Ph.D., Electronics Industry Manager; Mechanical Analysis Division, Mentor Graphics Corporation, may be contacted at [john\\_parry@mentor.com](mailto:john_parry@mentor.com)



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# 2.5/3D Packaging Enablement through Copper Pillar Technology

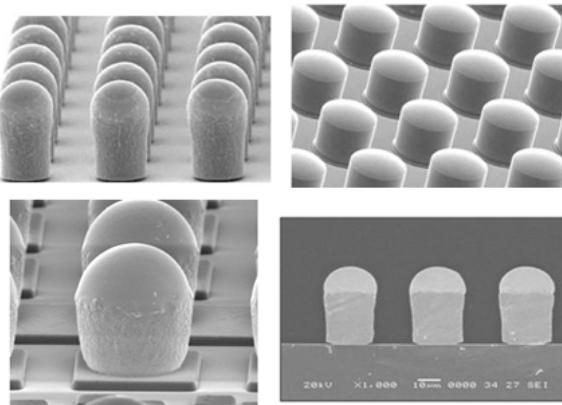
By Deborah S. Patterson [Amkor Technology]

Copper pillar bumping, now in high volume production for mobile electronics<sup>1</sup>, is also a transformative technology for next-generation 2.5/3D packaging and IC design. Ultra-fine-pitch copper pillar flip chip, together with the high reliability assembly of silicon interposers, opens up a world of possibilities for the IC and system designer.

Fine-pitch copper pillar bumps have replaced conventional flip chip solder bumps when the need for extremely low profile, high connectivity interconnect is required. Devices such as high-end processors, graphics, FPGAs, power amplifiers, MEMS, and HB-LEDs have incorporated fine-pitch copper pillar bumps and demonstrate the range of the technology. Copper pillar bumps can be found in handheld consumer electronics and are being introduced in high-reliability server, network and computing applications. Their widespread adoption<sup>2</sup> continues with the enablement of next-generation 2.5D packaging architecture which, in turn, is being driven by a mutual convergence of semiconductor material and design limitations coupled with interconnect and assembly advancements.

**Figure 1** shows four SEMs of 40µm pitch copper pillar bumps capped with SnAg solder. The SnAg solder reflows to join the die to the silicon interposer. Sub-40µm pitch has also been demonstrated.

**Figure 2** illustrates three packaging examples moving toward a more efficient system-in-package (SiP) approach. Vertical stacking or the close side-by-side



**Figure 1:** Examples of 40µm pitch copper pillar bumps capped with SnAg solder.

placement of individual die – perhaps through the decoupling of functions once found together on a monolithic IC – can produce significant performance and cost improvements.

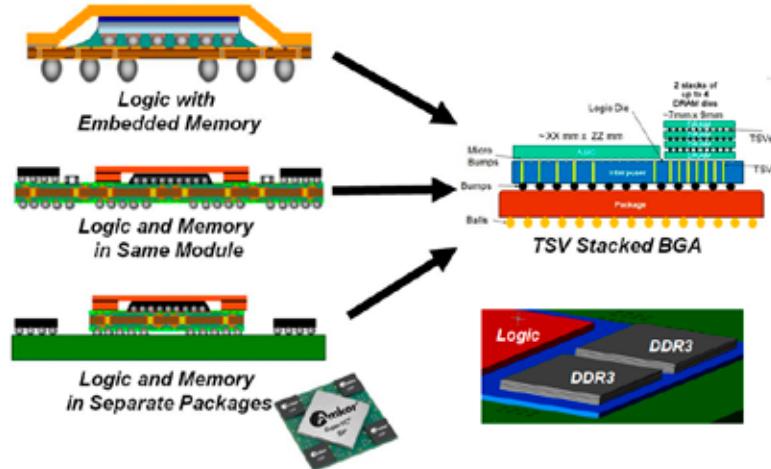
## Interconnect Enablers for 2.5/3D Packaging

To support high speed data transfer

and preserve signal integrity between die, a very fine-geometry circuit board and enabling interconnect solution is required. Silicon interposers and fine-pitch copper pillar micro-bumps represent the two technologies that have come to define a 2.5D packaging approach.

To create the silicon interposer, foundries use well characterized and high yielding 65nm-130nm fab processes to produce a multi-layer circuit board with through silicon vias (TSV). This passive interposer (no transistors) bridges the feature gap between the IC and package substrate. The high wiring density found within these silicon circuit boards create opportunities for improved system performance and simplified chip architectures.

Copper pillar micro-bumps are already in high volume production driven by strong demand in smartphones and tablets.<sup>3</sup> They provide the short, low inductance, efficient interconnections (a) between ICs in vertical stacks as well as (b) between an IC and the silicon interposer. Together,



**Figure 2:** The reconfiguration of three packaging approaches toward a heterogeneous BGA SiP that integrates various die. TSVs, shown within the interposer, provide a key performance enhancement. Copper pillar micro-bumps enable the very fine-pitch interconnect required to make this concept functional.

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the micro-bumps and silicon interposer provide a high-speed and high-bandwidth communication highway for side-by-side die (and stack) placement. The interposer bottom fans out to wider pitches that employ conventional solder bumps for connection onto the BGA substrate.

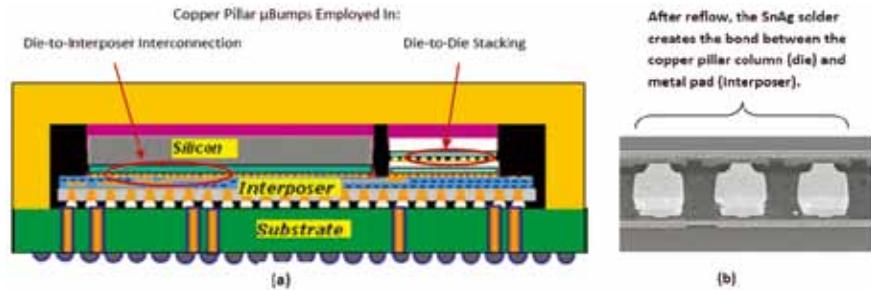
The BGA cross-section illustrated in **Figure 3** shows both side-by-side and vertically stacked ICs. Interposer inclusion defines the 2.5D approach. It will route thousands of interconnections between the devices. Coupled with true 3D stacked die (enabled by TSVs), the high routing density and short chip-to-chip interconnect ensures the highest possible performance while packing as much functionality as possible into the smallest footprint.

Functional blocks may include a microprocessor or special purpose logic IC (GPU, applications processor, ASIC, FPGA, etc.) connected through high-speed circuitry to other logic devices or memory (DRAM, SRAM, Flash) and supported by analog components (power management, RF), as well as other passive and/or specialized devices.

### Advantages of New Architecture Approaches for Next Generation Die

IC size and complexity have continued to grow in tandem with the foundry's ability to generate high yields through stringent front-end process controls and state-of-the-art equipment as successively larger wafer sizes and smaller process nodes are introduced. However, as device sizes grow, they threaten manufacturing yields to a point where time-to-market or unit cost targets are excessively compromised. New device development will, by definition, incur a high failure rate until the process matures and the designs are validated. The failure of one large die loses a considerable amount of silicon real estate. When ramping next generation process nodes with large size die such as an FPGA, the defect density is higher at the transistor and wiring levels and presents more of an impact on yield. Aside from the cost of the lost silicon, there is also the lost opportunity cost of not having access to the silicon to produce smaller good die.

In the case of memory, bandwidth can



**Figure 3:** (a) Illustration of a lidded 2.5D BGA package. A logic die on the left and a 3D die stack (e.g., memory) on the right are connected through copper pillar µbumps to a silicon interposer which is assembled to a BGA substrate with coarser pitch flip chip solder bumps. (b) Photo of assembled 40µm pitch copper pillar µbumps.

be severely constrained within a highly integrated chip due to the shortage of I/O capacity to support the complex networks of wires within the IC. At the die level, "I/O resources do not scale with interconnect logic resources with each new process node...the transistors comprising device I/O structures must be much larger to deliver the currents and withstand the voltages required for chip-to-chip I/O standards."<sup>4</sup> The silicon interposer can support Wide I/O standards to considerably improve bandwidth without compromising communication speeds or increasing power. By supporting thousands of

interconnections, overall system capacity is greatly improved.

The main hurdle in offloading functional blocks has been the inability of traditional semiconductor packaging to support the capacity (number of I/Os), speed, bandwidth or power reduction of the partitioned circuit. However, with its high wiring density, the passive silicon interposer becomes the final wiring layer connecting die that can now be designed to optimum process nodes and floor plan. The 2.5D process enables a forward-looking, planned foundation upon which to architect the functional circuit blocks

2.5D Considerations	Time-to-Market	Yield	Performance	Cost	Comments
IC design less complex	X	X	X	X	Faster ramp to production, Reduced wafer start costs, Reduced layer count, mask & lithography complexity
Improved IP block management	X	X	X	X	Design respins reduced, Faster feedback on new IP, Logic code reuse (interposer could split out proven functional blocks and piggyback new IP to prove or add functions)
Process node / Functional block optimization	X	X	X	X	Eliminates fab overdesign
Multiple sourcing / Mixing of die	X	X	X	X	Competitive pricing, feature sets, Eliminates process node overkill
IC Size Reduction	X	X	X	X	Yield increase; Large die failure devalues silicon - lost opportunity cost
Wide I/O Standard supported (silicon interposer)			X		Increased bandwidth/decrease latency
High wiring density / High density interconnects			X		Increased capacity and speed, Reduced power consumption
Electromigration resistance			X		Longer term reliability
Higher electrical conductivity			X		Copper pillar interconnect offers roughly 25% lower resistance than SnPb
Thermo-migration improvement			X		Longer term reliability
Stress mitigation for ELK, ILD		X			Silicon interposer, underfill, etc. act as a CTE buffer between thin fragile die and the BGA substrate
Test intersection point flexibility with functional		X		X	Assembly yield mitigation
Passives integration			X	X	Passives closer to die or removed from PCB, Simplification of PCB designs
Bridging gap to 3D				X	Lower cost than full 3D integration for certain products

**Table 1.** The benefits of re-architecting the IC.

# Semiconductor Assembly

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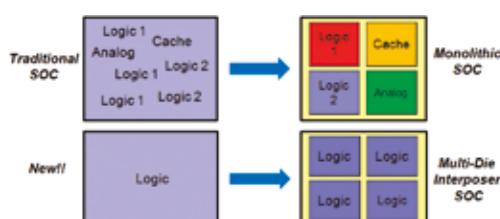
to optimize chip performance, reuse, fab technology, etc. Thus, a reassessment of the IC architecture is required to determine the best approach.

For example, a repartitioned IC that offloads power management (analog) and cache memory to older, mature fab processes provides benefits in overall costs and time-to-market. Components can be mixed and procured based upon multiple sourcing of the most competitive price and performance offered. Alternatively, if interconnect densities and communication speeds are not compromised, the logic itself may be partitioned into its smaller constituents, with the end result achieving an increase in overall yields and performance. **Figure 4** shows a conceptual view of two types of logic partitioning.

**Table 1** identifies several benefits of re-architecting the IC, either during the next new design phase or to support downstream iteration. Reduced wafer start costs due to reductions in layer count and subsequent mask and lithography complexity, along with the ability to outsource functional blocks to secure the best pricing and feature set from dedicated suppliers are compelling cost factors. There is no reason to dedicate the newest process nodes to functions that receive no cost/performance benefit from them.

If the logic IC is sufficiently partitioned with the silicon, then various downstream interconnect opportunities can be leveraged through the silicon interposer, depending upon die-to-die I/O requirements. This requires advanced planning and design for downstream flexibility. For example, one suggestion is to segment proven functional blocks from new IP to more easily validate a new design or to confirm additional functions as they are added.

For leading-edge systems designers, 2.5D packaging bridges a



**Figure 4:** Die are being partitioned to offload functions that can be accessed without compromising speed. The chosen process node is driven by function, reducing total cost-of-ownership, improving wafer yields, and addressing design bottlenecks.

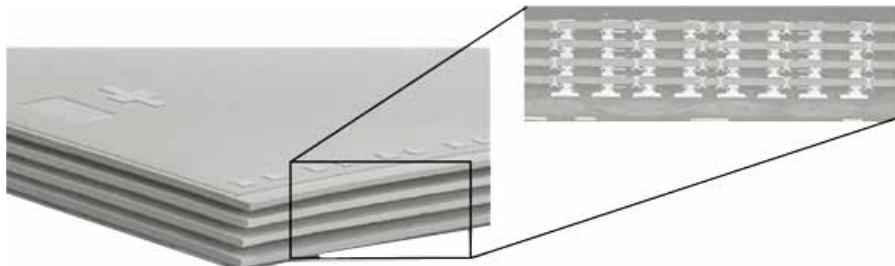
gap to allow not only system design flexibility, but also large potential gains in performance and yield as well as significant cost and time-to-market reductions.

## 3D Case Study: Memory

Memory has been stacked within packages for years, driving wafer thinning technology, wire bonding and flip chip advancements. TSVs and fine-pitch flip chip interconnect produce true 3D memory stacks to increase the amount of memory offered while maintaining reasonable die size. **Figure 5** shows a memory stack enabled through TSVs and copper pillar flip chip bumps.<sup>5</sup>

## 2.5D Case Study: FPGA<sup>6</sup>

Manufacturers of large scale FPGAs are challenged to provide high-capacity, high-bandwidth devices early in the product life cycle while they are still ramping a new process node to



**Figure 5:** A four die DDR memory stack with TSVs and fine-pitch copper pillar bumps. This type of construction represents a true 3D silicon packaging solution.

production. Initial defect densities are high and yields decline dramatically with large die size. Although yields eventually rise as the foundry process matures, there is a substantial time delay between product introduction and high-volume production availability.

Past examination of segmenting the monolithic FPGA into two or more adjacent devices identified several challenges such as insufficient I/O to connect the multiple FPGAs to each other and within the package, and relatively low signal bandwidth passing between the die (high signal latency between the packages and through the PCB), which would limit performance and increase power consumption.

Using 2.5D packaging, Xilinx successfully partitioned their next-generation FPGA into four 28nm devices that could be mounted onto a silicon interposer through a copper pillar flip chip bump array. The resulting structure enabled twice the bandwidth and capacity offered by the largest monolithic devices available at the time (**Figure 6**). It achieved this performance because of the enormous number of high speed data connections available through the 4-layer interposer. The assembly also provided much lower latency since the signals never traveled out of the BGA. In addition, the approach reduced power consumption by 50% over previous generation FPGAs.

The silicon interposer and copper pillar bumps facilitated the integration of massive quantities of interconnect logic and on-chip resources within a single package, allowing the resulting SiP to deliver exceptionally high improvement in performance. Aside from exceeding their performance objectives by partitioning the die into four smaller slices, Xilinx also

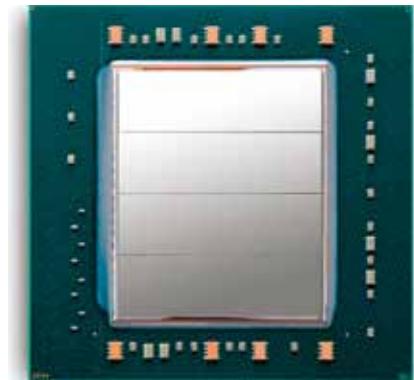
expects to achieve a faster yield ramp at the foundry.<sup>7</sup>

An impressive 50,000 bumps were designed into the 8mm x 24mm die area. Four of these die were assembled onto each interposer for a total of 200,000 operational bump connections. After the devices were successfully assembled onto the interposer, an additional 20,000 flip chip bumps were reflowed to connect the large 31mm x 25mm interposer to the BGA substrate. The BGA measured 45mm x 45mm and contained 2,000 balls for final board level assembly. **Figure 7** shows the copper pillar array and a cross section of the assembled package.

The engineering knowledge required to successfully implement and assemble this package is considerable. It validates the 2.5D approach and allows the silicon interposer to be recognized as a viable interconnect platform, opening up new packaging options for a wide variety of products. The silicon interposer is a scalable platform that can be used to integrate mixed functions (logic, PLD, memory, dedicated I/O blocks) and mixed processes (analog, processor, memory).<sup>10</sup>

### Assembly Considerations

Successful assembly of the 2.5D structure requires a substantial amount of

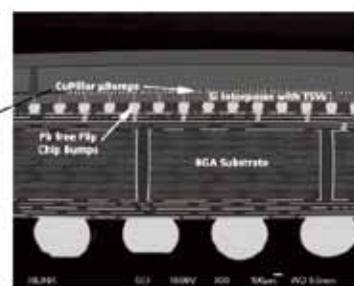
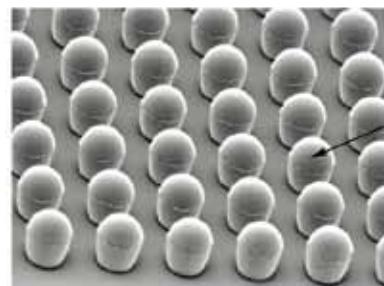


**Figure 6:** Top view of the 2.5D Virtex®-7 2000T FPGA. (Image courtesy of Xilinx)

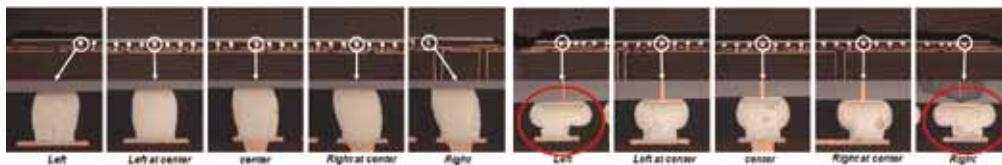
packaging experience and infrastructure. Thermo-compression bonding has been identified as a viable process for fine-pitch copper pillar flip chip assembly. One of the most pressing challenges is controlling warpage within the structure (die to interposer, interposer to substrate).

One possible flow has the interposer assembled to the BGA substrate where flip chip solder bumps are reflowed and underfill is dispensed and cured. The top die are then aligned and assembled to the interposer. Because copper has a higher elastic modulus than solder, it is more susceptible to stress during the attach process. Thermo-compression bonding of copper pillar micro-bumps, along with underfill application, minimizes stress on both copper pillars and die, allowing the substrate to maintain planarity. In addition, temperature profiles, pre-heating and materials selection ensure that flatness is controlled and full connectivity achieved.

**Figure 8** identifies flatness as measured at the underfilled gap between the interposer and the BGA substrate.<sup>11</sup> In this example, thermo-compression bonding produces little variation in the gap, whereas the mass reflow process shows an



**Figure 7:** Four FPGA tiles are mounted onto a silicon interposer through 200,000 copper pillar bumps (left). A cross-section of the assembled part is shown in the SEM (right). (Images courtesy of Xilinx)<sup>8,9</sup>



**Figure 8a:** Cross-sections of solder bumps assembled with thermo-compression (TC) bonding (left) and mass reflow bonding (right) processes. Edge bumps show more collapse during the MR Process.

increase in gap size as measurements are taken from die center to die edge. A series of SEM cross-sections taken through the die edge and die center are shown. The two sets of photos present cross-sections of bumps that were assembled using both thermo-compression bonding and mass reflow processes. The variation in uniformity between the two processes is readily observed. **Figures 8a and 8b** show consistent bump height uniformity across the die with thermo-compression bonding as compared with varying degrees of bump height variation seen on the mass reflow assembly example in the right-hand series of photos.

**Figure 9a** shows a SEM of the top of a silicon interposer with four landing pads. The long striations on the surface of the interposer are circuit traces. **Figure 9b** shows a cross section of a memory die with five TSVs and the landing pads on top. On the bottom side of the memory die, a connection is made to the silicon through a copper pillar bump. **Figure 9c** shows a cross section of copper pillar bumps joined to a BGA substrate and presents a good view of the SnAg solder after reflow.

### Test Considerations

**Copper Pillar Micro-bumps** - Copper pillar/SnAg capped bumps designed at conventional solder bump pitches are suitable for vertical probing. The probe makes contact with the SnAg solder cap. Bump height variation and the ratio of pillar height to diameter must be taken into consideration. However, in-line pitches of 50 $\mu\text{m}$  and staggered bump array pitches of 40 $\mu\text{m}$ /80 $\mu\text{m}$  that represent today's fine-pitch copper pillar footprints present significant challenges including limited capability and the availability of probe cards that service ultra-fine-pitch. With thousands to tens of thousands of bumps on a single die, the contact force increases tremendously.

Therefore, electrical test should be

completed prior to fine-pitch copper pillar bumping. However, this assembly and test flow is only feasible if the bumping process is proven to be robust enough

to accommodate probe mark damage to the bond pad. Otherwise landing areas designed in to the die to accommodate vertical probe should be considered. Logistics and test costs also support a probe before bump flow as optimal. Wafer thinning (<100 $\mu\text{m}$ ) as well as the wafer material (low- $k$  dielectrics, final metal pad) and its structural sensitivities also

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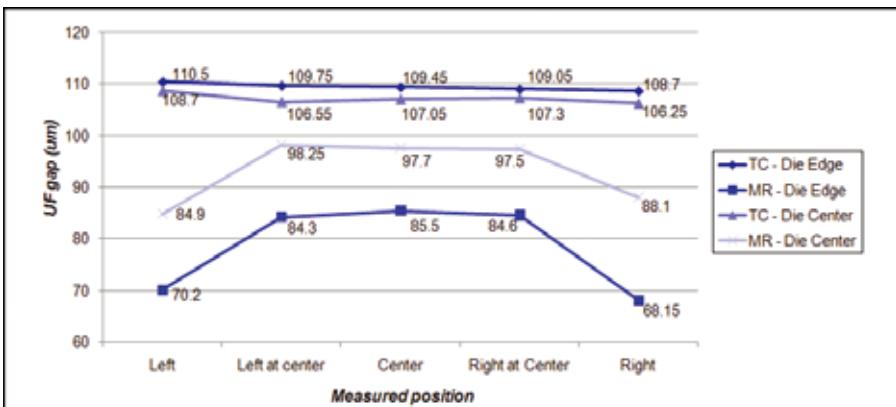
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**Figure 8b:** Measurement of the flatness of the interposer-substrate gap when comparing thermo-compression (TC) versus mass reflow (MR) bonding. TC bonding maintains a more consistent gap across the device.

influence wafer probe choices.

**2.5D SiP Packages** - Complexity is introduced with stacked die and integrated 2.5D packaging since a primary concern is the mitigation of downstream bill-of-material (BOM) loss. It is here that test becomes the differentiator. The number of test insertion points varies for high BOM products. Testing is often done after the logic die is assembled to ensure 100% connectivity prior to committing expensive memory to the package. Most OSATs should have a proven track record of high-yield die-to-BGA substrate placement. Although a natural test insertion point occurs after the logic die is assembled to the interposer, OSATs are being asked to investigate the feasibility of test at different assembly points. The insertion points will be determined by the assembly steps – both before and after test – to justify its value within the assembly flow. Challenges also include testing or socketing of the BGA side of a substrate prior to ball-attach and not damaging the exposed die due to high contact force.

## Summary

The demand for fine-pitch copper pillar

flip chip is considerable. It is found in high-volume mobile electronics and will continue to be fed by emerging markets employing 2.5D and 3D interconnect structures. 2.5D SiP will bridge the 3D TSV gap, enabling substantial performance and cost improvements while 3D IC development continues. The expansion of infrastructure – including foundries, OSATs, materials, equipment, test and software providers – coupled with close collaboration between the package, IC and system engineers will speed technology adoption. 2.5D and 3D TSV packaging will continue to build momentum and change the semiconductor and packaging landscape. Fine-pitch copper pillar flip chip and complex package assembly will bridge the gap between today's SoC constraints and successful SiP execution.

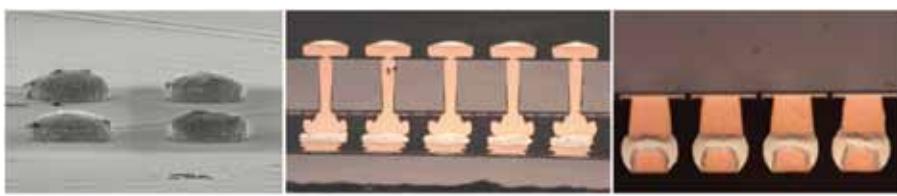
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## References:

- “Amkor Technology and Texas Instruments Deliver Industry’s First Fine Pitch Copper Pillar Flip Chip Packages to Market,” Press Release, July 7, 2010.
- “2010 Flip Chip and WLP: Market Projections and New Developments,” TechSearch International, December 2010, Figure 2.7 Copper Pillar Demand, page 72.
- “Amkor Technology Reports Financial Results for the Fourth Quarter and Full Year 2011,” Q4 and 2011 Amkor Technology, Inc. Earnings Conference Call, February 9, 2012.
- Kirk Saban, “Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency,” WP 380 (v1.1), October 21, 2011.
- Ministry of Knowledge Economy of Korea, “3D Package Technology Development Using Deep Via Project,” November 2006 – October 2009.
- Saban, Op. cit.
- Vincent Tong, “3D in the Deep Submicron Era,” SEMICON West 2011.
- Saban, Op. cit.
- Xilinx Xcell Journal, “Stacked & Loaded: Xilinx SSI, 28-Gbps I/O Yield Amazing FPGAs,” Issue 74, First Quarter 2011.
- Saban, Op. cit
- Ron Huemoeller, “Through Silicon Via (TSV) Platform Development,” Amkor Technology Customer Symposium, February 9, 2012.12. Randy Abrams, Kevin Chen, Credit Suisse, “Asia Semiconductors Sector,” January 10, 2012.



**Figure 9:** (a) SEM of four landing pads on the topside of a silicon interposer, (b) cross-section of a memory die with TSVs that is mounted onto a silicon interpose. It shows topside landing pads and bottom side copper pillar bumps, and (c) cross-sections of copper pillar pbumps joined to a BGA substrate through reflowed SnAg solder.

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# Glass as an Ideal Material for Next-Gen Interposers and Packages

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New packages are needed for three reasons. Current organic packages are expected to reach limits below about 50 $\mu\text{m}$  area array interconnections. The second reason is the need to package 3D ICs with I/O pitch of 20 $\mu\text{m}$  or less. The third is to provide a lower cost alternative to 3D ICs, going beyond 2.5D interposers reported by Xilinx.<sup>1</sup>

Si interposers solve some of these problems, but at high cost. Glass is proposed to solve all of these; not only at lower cost but at higher performance.<sup>2</sup> The high performance of glass comes from its low dielectric constant, high resistivity, and low electrical loss. Its low cost comes from both availability of glass in ultra-thin and ultra large sizes and also its processability to form metalized electronic structures. In addition, it's coefficient of thermal expansion (CTE) can be tailored from as low as 3ppm/ $^{\circ}\text{C}$  to as high as 9ppm/ $^{\circ}\text{C}$ , making SMT interconnections much more reliable than with Si.

However, glass has two problems. So far, it has not been used with high-density through vias in electronics. This remains the biggest barrier to the use of glass as an electronic interposer or package. The other is its low thermal conductivity, even though higher than organics but low compared to silicon. This article summarizes the pioneering efforts by a large Georgia Tech global industry consortia team, with particular focus on through vias.

## Barriers to Glass Interposers and Packages

Glass as an interposer substrate material has been previously described as providing several benefits compared to

silicon interposers and organic substrates including excellent dimensional stability, smooth and flat surface for fine line lithography, high electrical resistivity, excellent chemical inertness, low to medium coefficient of thermal expansion (CTE) matched or tailored to silicon die and PWB, and availability of ultra-thin glass (30 $\mu\text{m}$  thin glass) in ultra-large panel formats.<sup>3</sup> However, lack of fine-pitch through package vias (TPV) processes prevented glass from being adopted as an electronic substrate. The key technical challenges that need to be addressed to demonstrate glass as an ideal electronic substrate are: handling of ultra-thin and ultra-large glass substrates, high throughput TPV formation, reliability of TPVs, and low cost re-distribution layers (RDL).

## Conquering The Barriers

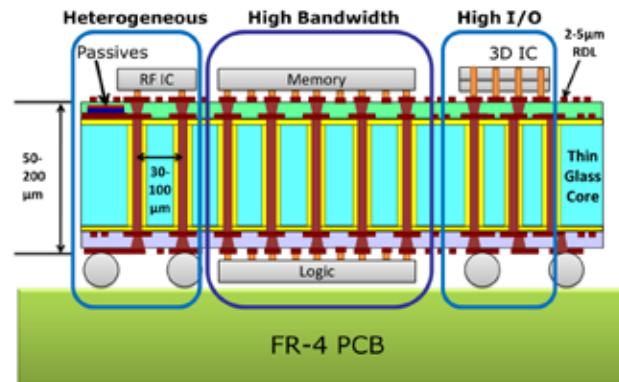
In partnership with an industry consortium of more than 30 semiconductor, package and supply-chain companies from the US, Europe and Asia, Georgia Tech's PRC has been pioneering ultra-thin, low-cost, wafer- and panel-based glass interposers, targeting 10x higher I/Os than today's organic packages at 2-10x lower cost per mm<sup>2</sup> than wafer BEOL Si interposers.

**Figure 1** illustrates Georgia Tech's pioneering 3D package concept. It involves ultra-thin glass with through-vias, having TSV-like dimensions to enable high bandwidth interconnections between logic and memory both in 2.5D and 3D interposer configurations.

Phase 1 of the Silicon and Glass Interposer (SiGI) consortium demonstrated groundbreaking technologies to handle ultra-thin glass wafers and panels, form small through-package vias (TPV) at fine-pitch with high throughput and high reliability and 5 $\mu\text{m}$ , double-sided RDL on both sides of ultra-thin glass panels with 10-50x lower signal loss than oxide-lined TSV interposers. In addition, Cu-bump chip-to-interposer interconnections have been demonstrated at 50 $\mu\text{m}$  I/O pitch, comparable to traditional Si interposers. Reliable SMT interconnection to FR-4 PWB is an important focus area and early reliability data on 7-10mm body size has been positive. The SiGI R&D at GT PRC covers electrical and mechanical designs to materials to processes to reliability and application demonstrators. The following sections describe early innovations in thin glass with TPVs.

## Ultra-Thin Glass Handling

Thinner glass not only enables the formation of ultra-small TPVs having TSV-like dimensions (<10 $\mu\text{m}$  via diameter) while maintaining reasonable aspect ratios for low process costs, but



**Figure 1:** Concept of Ultra-Thin Glass Substrate for 2.5D and 3D interposers, and a highly integrated SMT BGA Package.

also significantly improves via formation throughput since the etch rate of glass is typically slower than that of polymers. Thin glass also reduces interconnect length, hence shorter signal path, leading to smaller latency. Glass, however, is inherently brittle, and handling of ultra-thin glass during processing is, therefore, a key challenge. Rather than the complex and expensive carrier wafer bonding and de-bonding techniques common in Si TSVs, the PRC glass team has developed a handling method for double-side processing using polymer lamination of glass with a low modulus and low electrical loss ( $\tan \delta$ ) polymer. Polymer lamination not only facilitates thin glass handling (Figure 2), but also reduces laser impact on the glass surface during laser via formation and avoids direct metallization on glass surfaces. The first generation process of record (POR) is based on 180 $\mu\text{m}$  thin borosilicate glass, with 30-100 $\mu\text{m}$  glass being explored for the second generation process.

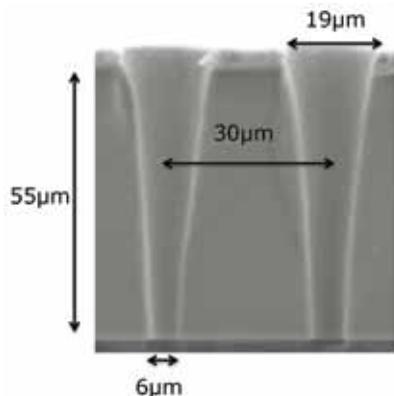


**Figure 2:** Crack-free handling of 50 $\mu\text{m}$ ; 6" x 6" thin glass panel, laminated with polymer on both sides

### TPV Formation

There is a clear need for high throughput, fine-pitch via formation processes and tools in glass, comparable to the DRIE infrastructure developed for TSV in silicon. The Georgia Tech program has already made significant advances in addressing this need, in partnership with leading global glass and tool companies. Via formation in glass using different laser types and mechanical drilling processes have been explored.<sup>4</sup> In partnership with Asahi Glass Co, Japan, we have demonstrated laser ablation using lower UV wavelength excimer laser (193nm) in achieving via diameters less than

35 $\mu\text{m}$  in 180 $\mu\text{m}$  thin glass. Thinner glass (55 $\mu\text{m}$ ) helped achieve smaller via diameters of less than 20 $\mu\text{m}$  at 30 $\mu\text{m}$  via pitch (Figure 3). Laser ablation using a mask projection technique enabled the formation of via arrays with thousands of vias simultaneously, thereby increasing the throughput and thus providing a path to low cost via formation.<sup>5</sup>



**Figure 3:** Fine pitch vias in Ultra-Thin Glass by Excimer Laser Ablation

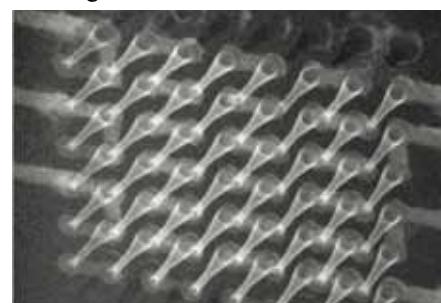
### TPV and Double Side RDL Metallization

A double side plating process has been applied to simultaneously metallize the TPVs and fine line wiring on both sides of the glass core. A low-cost, package-substrate-compatible, semi-additive-plating (SAP) process was used, starting with electroless Cu seed plating, followed by dry film photoresist lithography and high speed electroplating. The final thickness of copper traces are in the range of 8-12 $\mu\text{m}$ , resulting in much lower signal transmission loss per mm compared to thin BEOL wires on Si interposers, and lends itself well to power and ground plane integration in the glass package. Wet chemistry for metallization (as opposed to wafer-based sputtering), enables large panel processing. TPV diameters of 60 $\mu\text{m}$  at 120 $\mu\text{m}$  pitch and fine lines down to 5 $\mu\text{m}$  line and space have been demonstrated, and 15-30 $\mu\text{m}$  TPVs and 2-5 $\mu\text{m}$  lines and spaces are targeted for the second generation process.

### TPV and Glass Substrate Reliability

Microcrack formation during via ablation in glass has been a major

concern for metallized TPV reliability. Stresses are also induced in, and at the interface of, TPVs due to the CTE mismatch between glass and metallized copper. These stresses may induce mechanical damage, eventually leading to electrical failures of the metallized vias or cracks in glass. The thermo-mechanical behavior of glass TPVs was studied through reliability characterization in accordance with JEDEC standards. A daisy chain pattern was designed using TPVs (60 $\mu\text{m}$  via at 120 $\mu\text{m}$  pitch) arrays (8x8 or 16x16), and the metallized samples were subjected to MSL3 pre-conditioning, 3x reflow at 260°C, followed by thermal cycling (TCT) between -55°C and 125°C. A stable DC resistance was measured even after 1500 cycles, showing reliability of TPVs. Figure 4 shows a 3D X-ray image of a TPV array after 1500 thermal cycles. No macro-cracks in the metal via were observed. To the best of our knowledge, this is the first, albeit preliminary, demonstration of reliable fine-pitch TPVs in thin glass.



**Figure 4:** 3D X-ray image of 60 $\mu\text{m}$  diameter, 120 $\mu\text{m}$  pitch TPV array after TCT (1500 cycles at -55°C to 125°C)

### Demonstration of Ultra-thin Glass Interposer

A full integration process of TPV and RDL was first applied to 180 $\mu\text{m}$  thick borosilicate glass, and recently to 75 $\mu\text{m}$  thin borosilicate glass to demonstrate feasibility of fabricating glass packages. Such ultra-thin glass sheets are readily available in large-panel format (> 400mm x 400mm), unlike silicon wafers which need backgrinding and chemical mechanical polishing (CMP) to achieve 50-200 $\mu\text{m}$  thickness desirable for interposer applications. The ultra-thin glass (75 $\mu\text{m}$ ) is more flexible and easy to

handle post polymer lamination. Through vias of 30 $\mu\text{m}$  diameter in the 180 $\mu\text{m}$  thin glass using excimer laser ablation and 35-45 $\mu\text{m}$  diameter in the 75 $\mu\text{m}$  thin glass by 355nm UV laser ablation has been demonstrated. The plated copper thickness was around 10 $\mu\text{m}$  which resulted in conformal metallization of the through vias. **Figure 5** shows a snapshot of the two-metal layer, 150mm x 150mm, 180 $\mu\text{m}$  and 75 $\mu\text{m}$  thin glass test vehicles. No cracks or defects were observed after fabrication.

### Electrical Superiority of Glass over Silicon

Vector network analyzer (VNA) measurements were carried out on the fabricated sample to characterize the electrical loss of the glass interposer interconnections (transmission lines and TPVs). The high electrical resistivity and low dissipation factor of glass resulted in very low insertion loss (<1dB) until 10GHz for co-planar waveguide (CPW) lines and TPVs through the glass substrate (**Figure 6**), validating the high quality of the processes and structures. Glass packages with fine-pitch TPVs and fine line RDL are ideal for system integration of high I/O digital and high frequency RF/wireless devices.

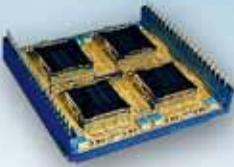
### Reliable SMT Interconnection to FR-4 PWB

Reliable SMT interconnection of glass substrates to FR-4 PWBs are critical to eliminate the need for an additional organic package common to current silicon interposer technologies. A systematic engineering approach combining compliant dielectric layers and flexible interconnections is being pursued to address the fundamental SMT interconnection reliability issues caused by huge TCE mismatch between silicon or glass interposers and organic PWBS. The ability to tailor the TCE of the glass package is an important benefit over the fixed TCE of silicon, especially for large body size packages. Finite element modeling was used to analyze the effectiveness of the compliant dielectrics. Parametric

studies were performed to analyze the influence of multiple variables, such as material properties and geometry parameters, on the reliability of the SMT interconnections, to optimize the buffering effect. Test vehicles of size 7.2mm x 7.2mm were fabricated with unique 25 $\mu\text{m}$  thick polymer, laminated on both sides of glass and silicon interposers. The test vehicles were assembled on FR-4 system boards, using

ball grid array (BGA) interconnections, and JEDEC standard thermal cycling test was performed to investigate the reliability of solder ball joints. The combination of intermediate TCE thin glass core and compliant dielectric material has shown promising reliability performance of BGA interconnections without underfill at a body size of 7.2mm. Further testing at 10-20mm body sizes is in progress.

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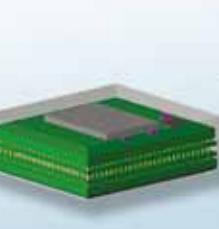
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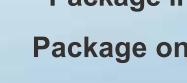
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**Hybrid Assembly**



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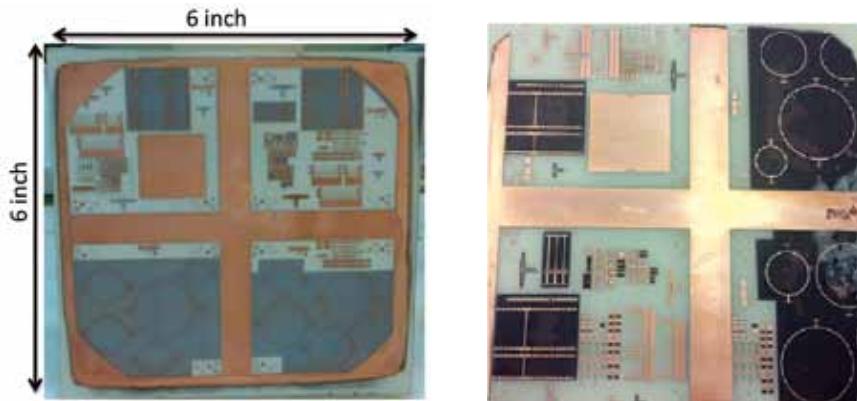
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**Figure 5:** Ultra-thin glass interposer Test Vehicles (150mm x 150mm), at 180µm (left) and 75µm (right) thickness

## 2.5D and 3D Glass Interposer and Package Applications

The baseline process defined for thin glass interposers is now being applied to several functional demonstrators to assess the benefits of package integration on glass. Side-by-side chip attach with high I/O and high bandwidth interconnection on multi-RDL glass interposer is a compelling first application. For form factors comparable to 3D-IC stacking for smart phone and high performance applications, Georgia Tech PRC has proposed so-called 3D Interposers with TPV to achieve wide I/O logic-memory stacking without requiring complex TSVs in logic IC.<sup>6</sup> In this scenario, TPVs are fabricated in the ultra-thin glass interposers of 50–100µm thickness at the same density or pitch of I/Os as the TSVs. The 3D glass interposer approach is scalable, allowing stacking of multiple ICs but on both sides of the interposer in both

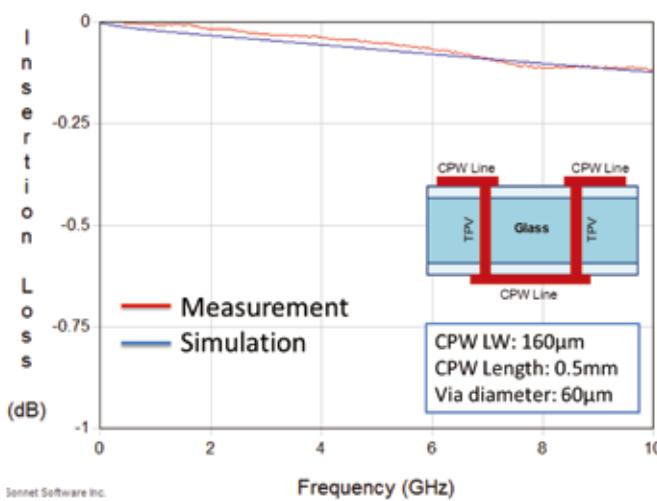
vertical and horizontal directions, with the same I/O pitch as TSVs. The 3D interposer approach enables improved thermal management, and testability, compared to 3D ICs with TSV. The ease of thermal management comes from separating logic and memory on opposite sides of ultra-thin interposers, thereby allowing access to the back side of the logic die, very similar to the current flipchip assembly. Additionally, the 3D interposer approach addresses the testability of the interposer itself, then with the memory stack, and finally with logic die. Modeling and electrical characterization results from TPV and RDL in thin glass indicate that the 3D glass interposer approach can achieve equivalent bandwidth to direct memory on logic 3D-IC stacking.

## Low-cost Manufacturing of Glass Interposers & Packages

Glass can be processed in wafer form and in panel form.

### Glass Wafer

**with BEOL:** Thin glass wafers can be processed using standard wafer processing with carrier wafers to integrate through vias and BEOL re-distribution layers (RDL). The advantages at this level are mostly related to electrical superiority of glass over silicon, and the



**Figure 6:** Ultra-low Insertion loss of CPW lines and TPV in thin glass interposer

cost benefits of glass are minimal.

**Glass wafers with advanced low cost processing:** Low cost process methods and package materials such as dry film polymers and wet metallization can be integrated into wafer based interposers for fine feature capability of wafer-level process tooling. Since 3D interposers connect active and passive components to each other on both sides, and to organic packages or motherboards on the bottom side with TPVs and RDL wiring, double-side processing approach applied to wafers can result in approximately 2x cost reduction by significantly reducing unit process steps.

### Glass panels for ultimate low cost:

The dominant cost factor is clearly the size of the wafer or panel used to fabricate interposers. As an example, for a 25mm x 25mm interposer size, and assuming a 80µm kerf width and 5mm edge clearance, the number of interposers from a 300mm wafer is around 89; whereas this number increases to 729 on a 700mm x 700mm panel. This is about 8X cost reduction but assumes the same yield in both small wafer and large panels. The Georgia Tech program with glass builds upon glass compositions and draw technologies for LCD manufacturing, thus guaranteeing the availability of large and thin glass panel sizes and future innovation in starting materials. Key manufacturing solutions such as novel handling methods for thin glass are being evaluated at supply chain partner sites for feasibility assessment.

## Future Work

Glass is clearly an ideal solution to address miniaturization, performance and cost needs of future packaging of electronic and bio-electronic systems. The Georgia Tech SiGI program has demonstrated proof-of-concept feasibility overcoming some of the biggest concerns with glass, namely, high throughput TPV formation and its reliability in glass interposers. The two-year Phase 2 of the SiGI program is planned for launch in June 2012, building upon and expanding Phase 1

advances, with focus on:

- Thinner glass (30-100 $\mu$ m) with finer pitch TPVs (15-50 $\mu$ m pitch) and reliability
- Multi-level RDL with 2-5 $\mu$ m lines and spaces and 5-10 $\mu$ m RDL vias
- Cu-to-Cu chip-to-interposer interconnections at 15-50 $\mu$ m pitch
- Reliable SMT interconnection to PWB with large package sizes of 20-40mm
- Enhanced thermal dissipation of glass interposers comparable to that of Si interposers
- High performance and thin film Passives as IPDs or thin embedded layers
- Electrical, thermal, mechanical and thermo-mechanical modeling and characterization
- Additional application demonstrators in Power, Analog, Digital, RF, mm-wave, MEMS and LED Packaging

## References

1. Patrick Dorsey, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency", White Paper, www.xilinx.com.
2. V. Sukumaran, Q. Chen, F. Liu, N. Kumbhat, T. Bandyopadhyay, H. Chan, S. Min, C. Nopper, V. Sundaram, and R. Tummala, "Through-package-via Formation and Metallization of Glass Interposers," in Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th, 2010, pp. 557-563
3. V. Sukumaran, T. Bandyopadhyay, Q. Chen, N. Kumbhat, F. Liu, R. Pucha, Y. Sato, M. Watanabe, K. Kitaoka, M. Ono, Y. Suzuki, C. Karoui, C. Nopper, M. Swaminathan, V. Sundaram, and R. Tummala, "Design, Fabrication and
4. R. Tummala, V. Sundaram, V. Sukumaran, and G. Kumar, "3D Glass and Silicon Interposers with TPV vs. 3D ICs with TSV," to be published in Pan Pacific Symposium Proceedings, 2012
5. V. Sukumaran, Q. Chen, F. Liu, N. Kumbhat, T. Bandyopadhyay, H. Chan, S. Min, C. Nopper, V. Sundaram, and R. Tummala Op. cit.
6. R. Tummala, V. Sundaram, V. Sukumaran, and G. Kumar, Op. cit.

*Characterization of Low-cost Glass Interposers with Fine-pitch Through-package-vias," in Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st, 2011, pp. 583-588*

*Venky Sundaram, Director of Industry Programs, 3D Systems Packaging Research Center, GIT, may be contacted at vs24@mail.gatech.edu.*

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# PoP Test Socket – Challenges and Approaches

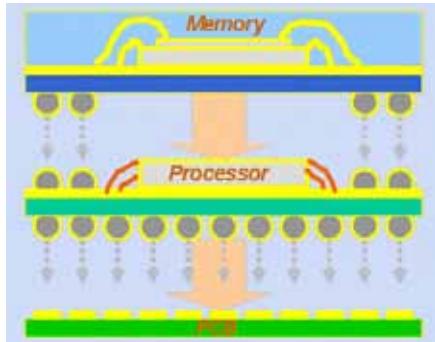
By Jiachun Zhou (Frank), PhD and Siang Soh [IDI]

**D**uring the last couple of years, package on package (PoP) and 3D assembly for IC devices has moved from development to high-volume production. It is well accepted that 3D or PoP is the way to achieve better IC performance, smaller scale, and a lower assembly cost for semiconductor devices, as shown in **Figure 1**. As PoP is gaining more popularity, the test socket industry faces more challenges since the conventional socket structure works only for conventional packages with pads or balls on one side of the substrate.

There are several different test setups in PoP device testing:

1. The known good memory device is placed above the processor device to test performance of the processor device. This is mostly used in manual test during the device development stage.
2. The processor device (or bottom device) is tested individually without the top device. This is commonly used in both high-volume and manual qualification testing.

Most test socket requests from customers are for case 2, and development work on PoP also focuses on the processor device testing socket.



**Figure 1:** Typical structure of PoP

## Basic Structure of PoP socket

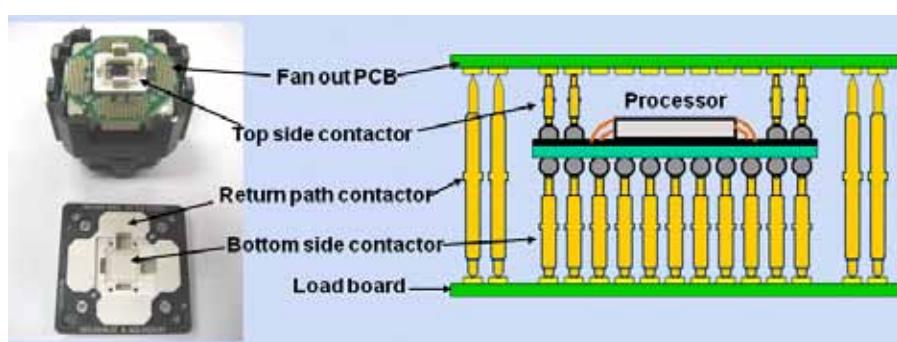
The PoP processor (bottom) package has pads or solder balls on the top sides of the substrate, which is a major difference from traditional packages. Usually there are two columns of pads or solder balls along outside edges on the substrate's top side. The pads may be above or recessed in the substrate's mask surface. The topside pads or balls will affect contactor selection, mainly at the contactor tip structure. In package testing, the topside pads must be connected to a load board in order to test the performance of the whole device. **Figure 2** shows the basic PoP socket structure. The bottom side pads (balls) are connected to the load board through conventional contactors, such as spring probes. The topside pads (balls) are connected through a path of topside contactors, topside fan-out PCB, and return path contactors. Generally, the bottom side contactors and return path contactors are installed in one bottom socket. The bottom side socket looks similar to the conventional socket with device pocket and alignment features. The device pocket in the socket is below the return path contactors socket surface. The return path contactor section is arranged in 4 wings of the device pocket. The alignment feature varies based on the customer nest structure.

The PoP socket can be used in manual

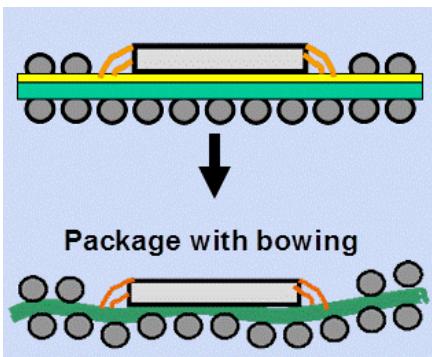
testing with a lid or in HVM in a pick-and-place handler. The topside fan-out PCB and topside contactor socket are installed on the manual lid or on the nest of handler. At the customer's request, the topside fan-out PCB and contactor socket can be designed for both manual testing and HVM handler testing. Due to its complex structure, PoP socket design has more technical challenges.

## Package Flatness

It is well known that the interconnector function is to provide reliable connection with enough travel (or deflection) to cover the flatness tolerances of the package and other features in the socket system. It can be simplified as "Z-stack" tolerances. Usually, PoP packages have larger flatness tolerance (or bowing) than conventional one sided packages, shown in **Figure 3**. To determine the proper contactor travel in a PoP socket, the contactors should be designed separately based on their functions. The bottom side contactor has the same function as a conventional one-sided package socket. Due to larger PoP package bowing, the working travel of the bottom side contactor should be larger (~ 15%) than a conventional contactor. Topside contactors connect topside pads of the PoP package and fan-out PCB. Due to mechanical limitations, a topside contactor is usually much shorter than the bottom



**Figure 2:** PoP socket basic structure



**Figure 3:** PoP package bowing

contactor with less travel. An optimal topside contactor travel must be able to cover all Z-stack tolerances in the package, PCB, and other structures, while allowing for small contactor length. The return path contactor connects the fan-out PCB and load board, and is much longer than both the bottom and top side contactors. Its working travel is much larger than conventional bottom contactors. A shorter contactor is always preferred to reduce the electric path for better signal integrity performance of the whole connection

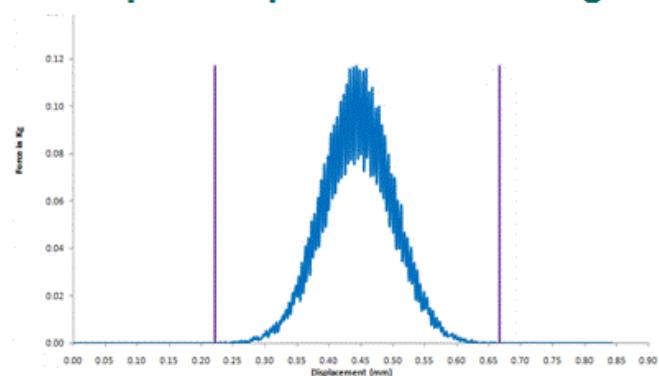
path. Thus, the optimal design of the contactors for a PoP socket is more critical than a conventional socket. One approach to achieve optimal design is to perform a Z-stack analysis, as shown in **Figure 4**, which summarizes all mechanical feature tolerances relating to the contactor, and should be performed separately for contactors of the bottom side, topside, and return path. It allows for better understanding of the vertical tolerance impact to provide optimal contact travels in the system. A statistics method can be applied to have more reliable tolerance distribution. For example, the curve on **Figure 4** indicates a tolerance range of ~0.4mm that should be the minimum contactor

travel. Generally, the contactor length for a PoP socket is ~ 2.5mm for the topside contactor, ~ 3.5mm for the bottom side contactor, and ~ 6mm for return path contactor.

### Force Balance and Finite Element Analysis

Both sides of a PoP package substrate are

### Z-stack Analysis Example: Requested pin deflection range



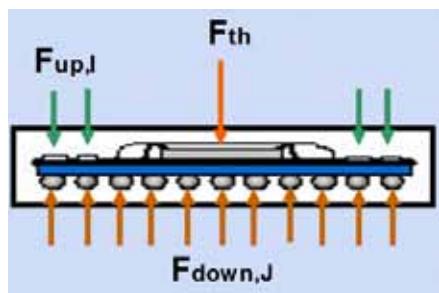
**Figure 4:** Z-stack analysis

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compressed by contactor forces in the PoP socket. Usually, little compression force is allowed on die. The forces of all contactors are applied only on the substrates. Generally, a PoP package has many more bottom side pads (> 400 pads) than topside (~100 pads). Since the topside contactor is shorter than the bottom side contactor, it has a lower compression force than the bottom side. Due to such great force that is unbalanced on the substrate, the package may be deformed or even damaged during the compression process, which is another major technical challenge in PoP socket design. To design a mechanically reliable PoP socket, force balance and substrate Finite Element Analysis (FEA) on stress/deformation will be requested. Force balance includes static and dynamic. Static force analysis on a substrate, shown in **Figure 5**, uses the formula below:



**Figure 5:** Force balance analysis

$F_{\text{down},j} * M = F_{\text{up},i} * N + F_{\text{th}} + F_{\text{up},\text{house}}$   
**Where,**  $F_{\text{down},j}$  – bottom side contactor compression force;  $M$  - quantity of bottom side contactor;  $F_{\text{up},i}$  – top side contactor compression force;  $N$  – quantity of top side contactor;  $F_{\text{th}}$  – force applied on die;  $F_{\text{up},\text{house}}$  – Reaction force from top socket housing (applicable once housing comes in contact with top side of substrate)

When the substrate is strong enough with less bowing, forces at both sides of the substrate can be balanced by contacting the surfaces of the socket pocket and substrate. Currently, a thinner substrate is another trend in package technology. To avoid substrate damage by external forces, the force balance calculation becomes more important in the selection of contactor forces and even in socket

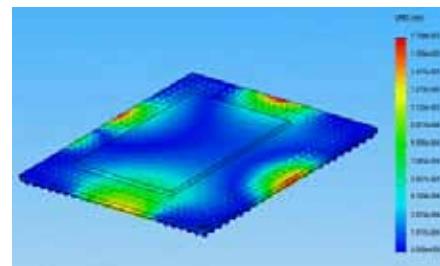
structure design.

Static force balance is considered only at the compressed still status of the package. What is also needed is the transient force balance analysis for the period when the chuck moves down with contactor compression forces on both sides. This transient force balance analysis provides maximum force on the device substrate identified from a curve of force vs. moving distance. Based on the maximum force and substrate material strength, the stresses and deformation in the device substrate can be predicted by FEA, which also provides the possibility of substrate damage under all contactor forces.

**Figure 6** presents the force distribution on the substrate. Due to specific features of this PoP socket, the mid sections along four substrate sides have the highest stress. Compared with material strength, substrate damage possibility can be determined. Substrates usually consist of a variety of different materials that may be known only to the customer, so the FEA should apply conservative material characters to ensure the reliability of a PoP socket.

### Tolerance Analysis

A PoP socket is more complex than a conventional socket due to more components, which increases accumulated tolerances of all components and potential missing contacts. Tolerance analysis at the X-Y direction is an approach in socket design stage that predicts the possibility of contactor

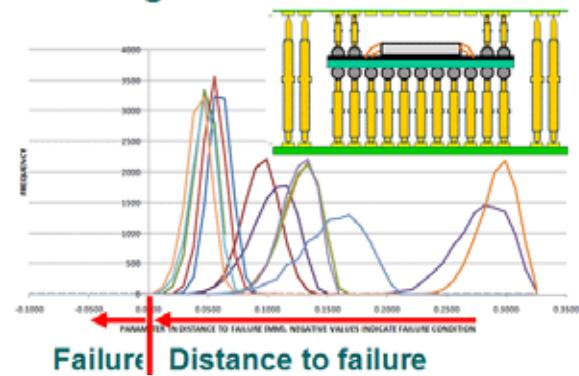


**Figure 6:** Stress analysis

misalignment with package pads. Among the three contact structures in a PoP socket, the top side contactors have the highest potential for misalignment because:

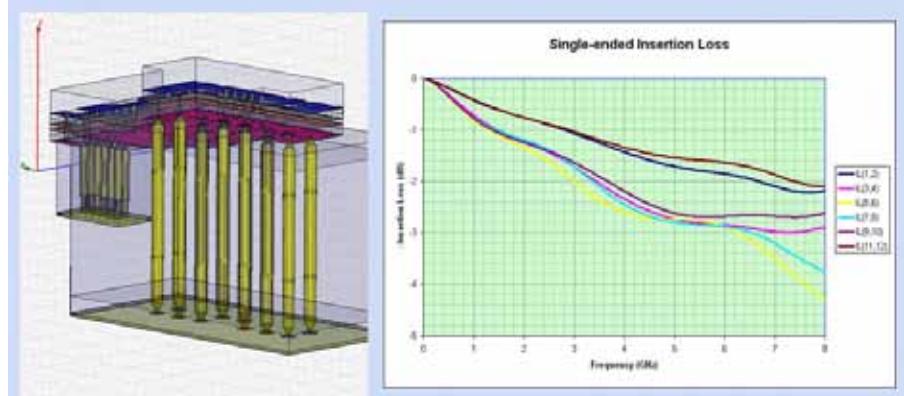
- The PoP device sits inside the bottom socket pocket and the position of the device may move in the X-Y direction by both tolerances of device and socket pocket. With the increase of a smaller pitch application, device body size tolerances and topside array true-position tolerances have became more critical factors to misalignment.

### Output: Failure Possibility @ Each Contact Point



**Failure Distance to failure**

**Figure 7:** Example of tolerance analysis curves



**Figure 8:** Signal integrity analysis model and results (example).

- The topside contactor is mounted on the topside lid or handle nest. The reliable alignment of topside lid and handler nest to the bottom side socket becomes another key factor that affects alignment of the topside contactor to device. **Figure 7** is an example of tolerance analysis curves. The tolerance analysis is a time-consuming analysis, but it allows us to understand the alignment challenges, fine-tune the systems, and achieve better results.

### Signal Integrity Analysis

Poor signal integrity (SI) performance of a PoP socket is one of the major concerns in PoP socket development. The topside pads must be connected through contactors of topside and return path, and also the fan-out PCB. The total electrical path may be over 12mm, which is much longer than a conventional bottom side contactor. To minimize the impact of this structure on signal integrity, a coaxial structure on the return path socket section is usually applied. However, the remaining electrical length of the connection is still over 8mm.

SI simulation on a PoP socket is another approach in socket design to predict the SI performance of the design. Based on simulation results, the socket design and contactor selection can be optimized. **Figure 8** gives an example of signal integrity simulation model and results. For this complex SI simulation, HFSS software is preferred. A 3D model must be built based on the actual socket design. Assumptions and experiences in SI simulation, such as port structure selection, are critical for the reliability of SI simulation results. Ideally, using a network analyzer with a SI test set up to characterize SI performance of the socket structure and compare measurement results to simulation results is more valuable. However, building up this type of SI measurement system is still a technical challenge with high cost. Thus, SI simulation in PoP socket design process becomes a major step.

### Summary

The PoP socket has been another business growth point in the test socket industry due to continuous increases in 3D packaging. A more advanced socket mechanical structure is the basis for the success of a PoP socket. At the same time, a series of analyses and simulations must be performed to ensure reliability of this socket design. The items include:

- Tolerance analysis (Z stack and X-Y direction)
- Force balance analysis (static and dynamic)
- Stress and deformation FEA (package and socket)
- SI simulation (whole top side connection path to load board)

All these analyses and simulations as well as the socket design must be considered in a whole interface solution, including socket and lid, change kit, and load board, to ensure success of a PoP socket contactor. 

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Esec AG Subsidiary of BE Semiconductor Industries N.V. Hinterbergstrasse 32 Cham 6330, Switzerland Tel: +41-41-749-5111 www.esec.com	FA A, S	WD: up to 300 mm DS: 0.25 - 25.4 mm XY: ± 15 - 80 μm θ: CM CT: 0.17 - 0.60 sec	FA CM	WD: up to 300 mm DS: 0.5 - 25 mm XY: ± 12 μm θ: ± 0.1 - 1.0° CT: 0.4 sec
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Mühlbauer Inc. Josef-Mühlbauer-Platz 1 Roding 93426, Germany Tel: +49-9461-952-1653 www.muhlbauer.com	FA A	WD: up to 200 mm DS: CM XY: $\pm 30 \mu\text{m}$ $\theta$ : CM CT: 0.36 sec	FA CM	WD: CM DS: CM XY: $\pm 20 \mu\text{m}$ $\theta$ : CM CT: 0.36 sec
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Semiconductor Equipment Corporation 5154 Goldman Avenue Moorpark, CA 93021 Tel: +1-805-529-2293 www.semcorp.com	SA A, E	WD: CM DS: 0.15 - 25.4 mm XY: $\pm 5 - 25.4 \mu\text{m}$ $\theta$ : CM CT: 18 sec Min.	SA A, S, U	WD: CM DS: 0.15 - 25.4 mm XY: $\pm 5 - 25.4 \mu\text{m}$ $\theta$ : CM CT: 18 sec Min.
Shibaura Mechatronics Corporation 2-5-1, Kasama, Sakae-ku, Yokohama Kanagawa Prefecture 247-8610, Japan Tel: +81-45-897-2421 www.shibaura.co.jp	FA A	WD: up to 300 mm DS: CM XY: CM $\theta$ : CM CT: 0.2 sec	FA A, S, U	WD: up to 300 mm DS: 2 - 6 mm XY: $\pm 2.5 - 15 \mu\text{m}$ $\theta$ : CM CT: 1.0 - 2.5 sec

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Shibuya Kogyo Co. Ltd. Mameda-Hommachi, Kanazawa Kanazawa 920-8681, Japan Tel: +81-76-262-1200 www.shibuya.co.jp	FA A	WD: up to 300 mm DS: 2 - 6 mm XY: ± 2.5 µm θ: CM CT: 3.0 sec	FA A, S, U	WD: up to 300 mm DS: 0.25 - 20 mm XY: ± 1.0 - 15 µm θ: CM CT: 1.6 - 60 sec
Shinkawa Ltd. 2-51-1 Inadaira, Musashimurayama-shi Tokyo 208-8585, Japan Tel: +81-42-560-1231 www.shinkawa.com	FA A, E	WD: up to 300 mm DS: 0.18 - 25 mm XY: ± 20 - 30 µm θ: ± 0.5 - 3° CT: 0.15 - 0.35 sec	FA U, O	WD: up to 200 mm DS: 0.3 - 25 mm XY: ± 2 - 5 µm θ: CM CT: 0.8 - 1.4 sec
Smart Equipment Technology SAS 131, Impasse Barteudet, BP 24 Saint Jorioz 74490, France Tel: +33-450-358392 www.set-sas.fr	FA A	WD: up to 300 mm DS: 0.2 - 100 mm XY: ± 0.5 - 3.0 µm θ: CM CT: CM	FA, SA A, S, U, O	WD: up to 300 mm DS: 0.2 - 100 mm XY: ± 0.5 - 3.0 µm θ: CM CT: CM
TDK Electronics Europe GmbH Wanheimer Strasse 57 Dusseldorf D-40472, Germany Tel: +49-211-90770 www.tdk-components.de			FA A, S, U	WD: up to 200 mm DS: 0.3 - 30 mm XY: ± 3 - 8 µm θ: CM CT: 0.8 - 5.3 sec
Toray Engineering Co. Ltd. Nihonbashi Muromachi Building 3-16, Nihonbashi-Hongokucho 3-chome, Chuo-ku Tokyo 103-0021, Japan Tel: +81-3-3241-1543 www.toray-eng.com			FA, SA A, S, U, O	WD: up to 300 mm DS: 0.2 - 20 mm XY: ± 0.5 - 5 µm θ: ± 0.2° CT: 1.7 - 30 sec
Tresky AG Boehnirainstrasse 13 Thalwil CH-8800, Switzerland Tel: +41-44-772-1941 www.tresky.com	FA, SA A, E, G, O	WD: up to 300 mm DS: 0.07 - 50.0 mm XY: ± 1 - 5 µm θ: CM CT: CM	FA, SA A, S, U, O	WD: up to 200 mm DS: 0.07 - 50.0 mm XY: ± 1 - 5 µm θ: CM CT: CM
Ultron Systems, Inc.t 5105 Maureen Lane Moorpark, CA 93021 Tel: +1-805-529-1485 www.ultronsystems.com	SA A, E	WD: CM DS: CM XY: ± 25.4 µm θ: CM CT: CM		
Unovis-Solutions 147 Industrial Park Drive Binghamton, NY 13904 Tel: +1-607-779-3800 www.unovis-solutions.com			FA S	WD: CM DS: CM XY: CM θ: CM CT: CM
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# GUEST EDITORIAL



## 3D Integration and the Supply Chain Shift

By Francoise von Trapp, *[3D InCites]*

**M**arket adoption and production of 3D ICs is closer to reality than it's ever been. In the past year, processes have reached the point where issues have been ironed out and efforts are underway to make sure they are optimized for high volume manufacturing (HVM). In fact, at this year's Electronic Design Process Symposium, April 5-6, 2012, in Monterey, CA, Qualcomm's Riko Radojcic said that there are "no intrinsic technology show stoppers for memory on logic. All the things we worried about a year or two ago are in good shape (in terms of technology processes)," and cited such examples as high aspect ratio (HAR) vias, backside processes such as thinning, microbumping and joining, integration and stacking. "What we need now is volume so yield issues can be addressed," he said.

The ecosystem has mobilized, and we're now hearing from the foundries and OSATS who are ready to broadcast their plans for HVM of 3D ICs. The jump start came when the industry latched on to 2.5D with TSVs in a passive interposer as a starter 3D solution. It's believed that 2.5D will exist alongside true 3D, as well as being used in conjunction with 3D ICs to create 3D heterogeneous systems.

### The 3D Roadmap

According to Jim Feldhan, president of Semico Research, 2012 will see pilot production for 3D DRAM with HVM coming in 2013. The hybrid memory cube (HMC) of DRAM on logic will be in pilot production in 2013, with HVM in 2014. 3D NAND will also be in pilot production in 2013 and HVM in 2014.

From an applications perspective, the first to adopt 3D will likely be data centers and base stations, where the 10x performance at lower power consumption benefits offsets the cost of implementation. By 2015, Feldhan says he expects market penetration for 3D devices in servers will be over 60% (**Figure 1**). Market penetration for 3D devices for tablets and smartphones is expected to reach just over 10% by 2015. Ultimately, Feldhan says the bottom line as seen by Semico Research is this: applications need performance that can be provided by 3D. Adoption is starting, but the eco system still needs development and maturity.

### The Supply Chain Shift

With 2D packaging, the supply chain was clearly defined. The fab handled front-end processes. The outsourced semiconductor assembly and test (OSAT) providers handled the back-end. There was no such thing as the middle end. But with 3D ICs using through silicon vias (TSVs) as the method of interconnect, we're

playing a whole new ballgame. Middle-end processes have emerged as a distinct manufacturing area, and include such backside processes as redistribution layer (RDL), TSV formation (etch, barrier, seed, and fill), temporary bond and debond, microbumping, stacking, and thinning.

### Where's the Hand-Off

Much of the debate over the supply chain for the past few years was around handling the wafer, where the hand-off point from the fab to the OSAT should be, and who was responsible for potential damage to a wafer stack. As a result, three different possible scenarios have emerged to address this (**Figure 2**). Two are collaborative models involving both the foundry and OSAT, and the third is what TSMC's Douglas Chen-Hua Yu calls a "single integration model". In the first foundry/OSAT model, the front-end-of-line (FEOL) and middle-end-of-line (MEOL) processes take place at the foundry, with the hand-off product being a thinned wafer mounted on a temporary carrier, ready

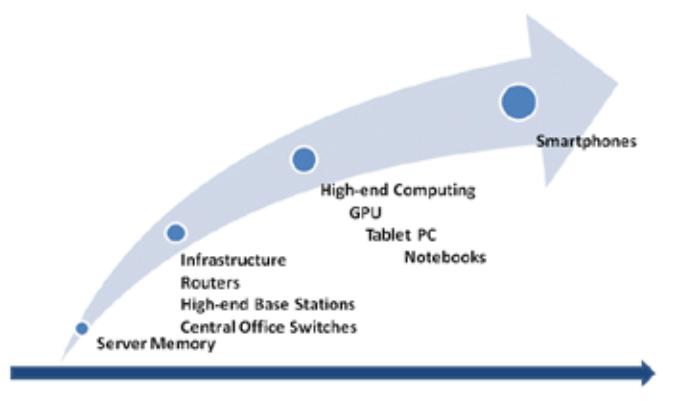


Figure 1: Interposer & 3D TSV IC Application Roadmap, (courtesy of Semico Research)

for back-end-of-line (BEOL) final assembly (stacking) and test at the OSAT. The second foundry/OSAT model puts the FEOL processes at the foundry and the MEOL and BEOL processes at the OSAT. The hand-off product in this scenario

is a via-mid TSV wafer, still in thick form for easier handling. Alternatively, in the single integration model all end-to-end manufacturing takes place at one location: foundry, IDM or OSAT, thereby eliminating the issue of liability ownership in the event of damage to the wafer stack. Over the past few months, many of the pure-play foundries, OSATs and IDMS have stepped forward to draw their lines in the sand.

### Who's Doing What

TSMC has made its plans quite clear, publicly declaring it is ready, willing, able and intends to take on production of 3D ICs end-to-end. The company has invested heavily in adding capacity for 3D ICs and announced it will be production ready by the beginning of 2013. The company is working feverishly to put physical design kits and EDA support in place so that customers can begin designing with what TSMC calls its "chip on wafer on substrate" (COWOS) technology platform.

Two of the other major foundries, GlobalFoundries and UMC, have come forth supporting collaborative approaches with end-use customers and major OSATS. During the 3D panel discussion at the 2012 IMAPS Device Packaging Conference, Jon Greenwood, of GlobalFoundries said the company will rely on collaborative relationships with major OSATS and key material suppliers to provide a flexible supply chain for its customers. GlobalFoundries launching its program just 18 months ago. Remy Yu of UMC said the foundry is also driving an open ecosystem, and in addition to the partnership with Elpida and Powertech, he said there are other projects in which UMC is involved.

Rich Rice, of ASE reports that the company is poised to support backside and middle processing. "We love to do assembly; we do test really well and work with customers to develop test strategies and deliver product," he noted. "I think OSATS are going to play a critical role. It's going to evolve into an ecosystem that supports a much bigger pie than we need

to worry about. ASE is pumped about what this has to offer."

At the 2011 Architectures for Systems Integration and Packaging Symposium (ASIP) in Burlingame, CA, STATS ChipPAC's Raj Pendse said the company has the capability for mid-end through back-end assembly, and is ready to

process thick wafers that are easier to handle in transport. "By changing the way packaging is done, it impacts our knowhow and business model," he said. "We're managing this quite well."

Amkor is also firmly behind a customer-driven collaborative approach. According to Ron Huemoeller, who leads 3D product



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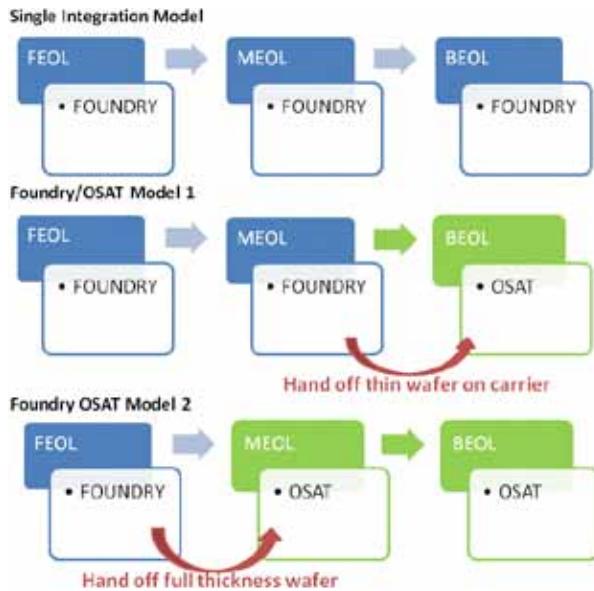
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**Figure 2:** Three supply chain models that have emerged, based on the wafer hand-off.

development for the company, Amkor doesn't invest in a platform until they

a continuous feedback loop, which helps to drive down costs and improve yields.

know it's going to stick. The company began by investing in 2.5D, and Huemoeller says that by starting off there, it allows the kinks to be ironed out for true 3D. The company has a complete set of 300mm (& 200mm) tooling in place to support TSV product development/growth, and there are customers with programs in place for both 3D IC and 2.5D.

According to IBM's Dan Berger, who presented on behalf of the company at ASIP 2011, the company is also suited to handle end-to-end manufacturing. He said its approach requires

That isn't as likely to happen when the hand-off is between different outsourced companies. IBM has experience and understanding of all these elements. "From that perspective," he noted, "it's good to be an IDM."

### Conclusion

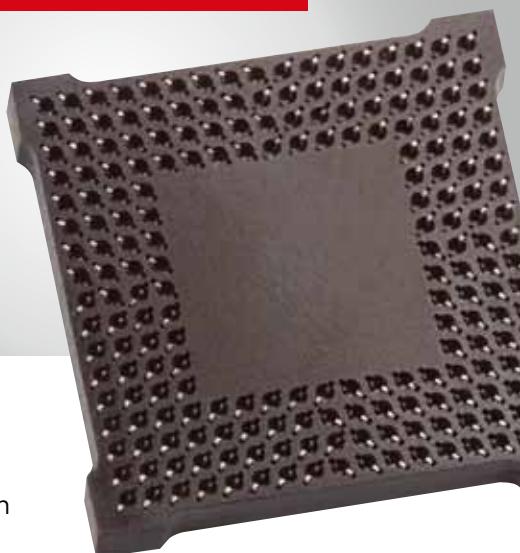
What has become increasingly clear is that there will be more than one supply chain model, dependent on the customer requirements. One big question mark with TSMC's end-to-end approach is who will provide the memory, as TSMC is not a memory manufacturer. When it comes to fabless customers who want to combine chips from various sources, a foundry/OSAT model might be the more viable solution. 

*Françoise von Trapp, Editorial Director of 3D InCites, may be contacted at francoise@3dincites.com*

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# Thin-Gate Acoustic Imaging of Flip Chips

By Tom Adams, [Sonoscan, Inc.]

“**W**hite bumps” are a frequent and important defect found when examining flip chips with an acoustic microscope. A bump that appears white in the acoustic image is not fully bonded to its bond pad on the face of the chip. It is the gap between the pad and the bump that creates the near-100% reflection of ultrasound that makes the bumps appear bright in the acoustic image.

Vertically, the location of white bumps is typically near the top of the offset between the chip and the substrate. But the entire vertical dimension of the underfill region from the die face to the substrate is of interest because it is where several types of defects and anomalies occur that can slowly or rapidly degrade the electrical reliability of the flip chip. These include bump de-bonds, cracks, and voids at any depth within a bump, de-bonds of the bump from the substrate, and voids in the cured underfill, especially voids that are in contact with one or more bumps. There are other less frequent anomalies, including uneven distribution of filler particles.

Until recently, it has been difficult to assign these anomalies to a specific depth. A reflection-mode acoustic microscope operates by pulsing ultra-high frequency ultrasound into the back side of the silicon chip and receiving the return echoes for analysis and imaging. Echoes come back from solid-to-air interfaces in gaps (highest amplitude), from solid-to-solid interfaces (a range of medium amplitudes), but not from homogeneous materials, since they contain no material interfaces.

The time, measured in nanoseconds, for a given echo to arrive at the transducer for collection and analysis depends on the depth from which it

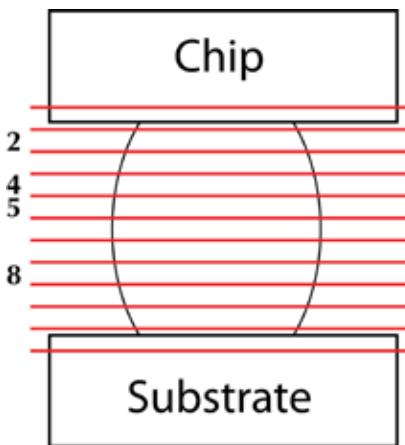
has been reflected. Ultrasound pulsed into the flip chip by the scanning transducer travels first through the homogeneous bulk silicon of the chip, which has no internal interfaces and is virtually transparent to ultrasound. The first strong echoes of interest come from the interface between the die and the substrate (including the surface circuitry and the passivation layer). Other echoes of interest come from the remainder of the underfill depth and the substrate. The entire vertical extent of this region may be 75µm or less, but diagnosis of a problem can be made easier by knowing at what depth within this region a particular acoustically imaged feature lies.

Reflection-mode acoustic images are typically gated, meaning that only those echoes falling within a given time gate are used to make the image. When imaging a flip chip, the first image may be gated rather broadly on the interface between the die and the solder bumps. If white bumps appear in this image, they probably represent gaps (non-bonds) at the tops of the bumps. But they could, and occasionally do, represent gaps between the passivation layer and the chip, or cracks within the bump. And it is often tricky to assign a particular depth to acoustic features that lie deeper than the chip-to-bump interface.

One manufacturer of acoustic imaging equipment\* has approached this problem by developing a module that creates a desired number of gates within a defined depth. In effect, the depth of interest is sliced into several or many layers. A separate acoustic image is made for each layer during the same transducer scan. In a flip chip, the region from the die face to the substrate is typically divided into several gates. In other thicker materials, where the depth

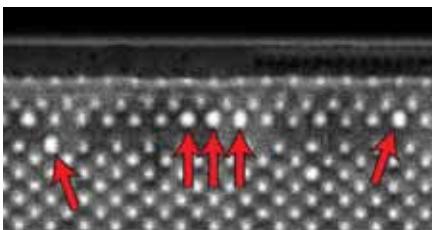
of interest is considerably thicker than in a flip chip, the number of gates can be as many as 200. There are limitations, of course; each individual gate needs to be thick enough to send back enough echoes to create an acoustic image, since there will be one image per gate.

The gates are set by observing the A-scan waveform, which is made by sending multiple pulses into a single x-y location and using the echoes from all depths to assemble the waveform. In flip chips, the chip face-to-substrate region is easily identified in the waveform, and markers are placed to define the vertical extent to be covered by the gates. In the flip chip shown here, a total of 11 gates of equal thickness were set to cover the depth from the chip face to the substrate as shown in **Figure 1**. Each gate uses only echoes from within its specified depth to make the acoustic image; echoes from other depths are ignored. The gates whose acoustic images are shown are numbered in **Figure 1**.



**Figure 1:** The underfill depth was imaged using 11 time gates, each producing a separate acoustic image.

**Figure 2** is part of the Gate 2 image from this sequence. Gate 1 intentionally impinged slightly on the die face, but

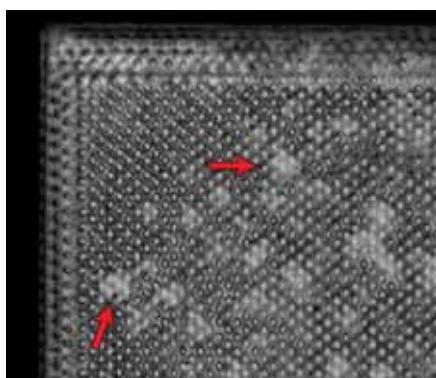


**Figure 2:** Gate 2 revealed debonds at the tops of some solder bumps.

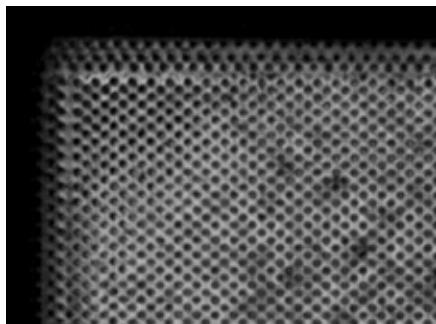
displayed no interesting features at that depth, although in some flip chips delamination of the passivation layer or cracks within the low-*k* dielectric are imaged. In **Figure 2**, the small round bright features marked by arrows in the Gate 1 image are de-bonds between the bumps and their bond pads — the classic “white bump” signature that identifies the solid-to-air interface that is present in the broken connections at this depth. The interface in any gap reflects >99.99% of the ultrasound even if the gap is <0.1µm thick. Several of the white bumps in **Figure 2** are marked by arrows. The remaining bumps' gray amplitude color was created by the bond between two different solid materials.

Gate 4 (**Figure 3**) was initially somewhat puzzling. It contains numerous white features that are rather vague in outline but all of similar size. Since this is the fourth of eleven gates, they appear to lie roughly one-third of the way down into the underfill. A few of them were faintly visible in Gate 3.

The image in Gate 5 (**Figure 4**) gives



**Figure 3:** Gate 4 showed vaguely defined bright features.

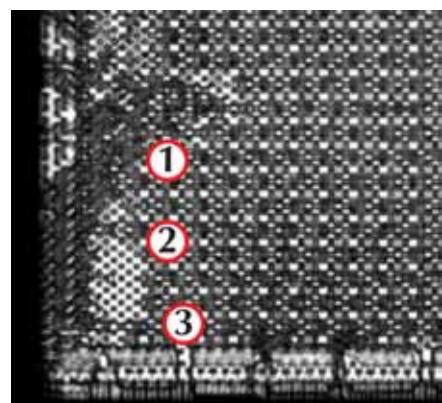


**Figure 4:** Gate 5 displayed the bright features (particle clumps, probably) as shadows, precisely defining their depth.

significant additional information: these features now appear as dark acoustic shadows; a change that means the features do not lie in Gate 5. The echoes being reflected from Gate 5, when traveling back toward the transducer, are being partly blocked by these features, indicating that the features lie above Gate 5 and in the lower part of Gate 3. Vertically, they are confined to Gates 3 and 4. Close

inspection of their structure suggests that the features represent changes in particle density around some groups of solder bumps. They are probably regions where there are more particles (=higher reflectivity) than in other regions.

Gate 8 (**Figure 5**) presented multiple anomalous structures. Item #1 is a dark region that



**Figure 5:** A variety of anomalous features appeared in Gate 8.

appears to continue to the extreme left as a bright (de-bonded) feature. In lower gates, and in an X-ray image of the chip, it can be seen that this is the location of a wire on the substrate. The dark region in item 1, however, extends horizontally and irregularly beyond the area of the wire. The larger feature size and the bright area at left suggest that this is a defect or an anomalous structure.

Item #2 is a bright gap that is imaged in Gates 8, 9 and 10, but not above those gates. It is probably a void or de-bond that borders the substrate.

Item #3 sits just above a small bright area indicating a de-bond. Two similar structures to the right are dark, meaning that they are well bonded, but another at far right is probably de-bonded.

## Conclusion

The ability to make individual acoustic images at well-defined vertical gates within the critical underfill/bump zone of a flip chip can locate anomalies that might otherwise not easily be assigned to a specific depth. The irregular clumps of filler particles, for example, appear to be confined to Gates 3 and 4; the next step is to ask what may be causing clumping at this depth. The anomalies seen in other gates in this flip chip may give information that leads to corrective modifications of process steps. ☺

\*Sonoscan

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at Assembléon, its customers and technology.

Assembléon became an independent company in April 2011. Since then the company has become profitable, mostly due to the introduction of its pick & place platform, iFlex, and its expansion into the back-end, embedded and module market.

The new management team is led by Jeroen de Groot, formerly responsible for Marketing and Innovation of Assembléon. Jeroen has worked for Assembléon for 15 years, in Asia as well as in Veldhoven. He has a Masters degree in Technology Management from the University of Eindhoven, the Netherlands. Additionally, the management board includes:

- Jeroen de Groot: CEO, responsible for Marketing, Innovation and global HRM
- Thierry Girardot: CFO, responsible for Global Finance, Admin and IT
- Burkhardt Frick: CCO, responsible for Global Sales and Service
- Miel Ramselaar: COO, responsible for Global Production, Supply chain and Logistics
- Tonn van de Laar: non executive chairman of the board

The new management team says it's fully committed to further pursue the present strategy, with continued focus in the back-end, embedded and module market, in addition to capitalizing on its established strengths of its A-Series platform in the most challenging SMT applications (e.g. high end smart phone production), rolling out iFlex and further improving Assembléon's cost structure.

## **SEMI Arizona Forum Addresses the 450mm Wafer Transition**

On Tuesday, April 24, the Arizona Chapter of SEMI Americas organized a Breakfast Forum that was hosted and sponsored by Intel Corporation and co-sponsored by ASML. Over 120 industry professionals attended the event to hear an overview of the transition to 450mm wafers.

Abbie Gregg, President of Abbie Gregg, Inc., gave an excellent overview of Arizona technology challenges and opportunities. Jim Feldhan, President of Semico Research, described the semiconductor market outlook and 450mm opportunities. He's forecasting a 9% increase in semiconductor revenue for 2012. Kirk Hasserjian, Corporate VP Strategic Programs at Applied Materials, identified and discussed five key factors for a successful industry transition to 450mm wafers. Ron Rinfret, Director of Technology Manufacturing Engineering, Strategic Programs for Intel Corporation, closed with the history of Intel in Arizona and a status update on the industry-wide collaboration program known as G450C.

Lee Smith, former Sr. Director of Business Development, at Amkor Technology raised the most questions from the audience. He noted, "The event on the 450mm wafer fab transition had a great line-up of speakers, yet all of them neglected the challenges to develop 450mm infrastructure in the backend. Probe, bump, WLP, TSV mid, thin/reveal, bond/de-bond and die-attach processes all need substantial expenditure to develop, qualify and deploy in high-volume manufacturing. Where will the investment come from when the back end suppliers are at a critical crossroad with the changing competitive and technical landscape?" Ron Rinfret acknowledged that the 450mm backend issues have yet to be addressed.

Karen Savala, President of SEMI Americas, commented, "The SEMI Arizona Steering Committee, re-formed in December of last year, is absolutely delighted by the member support shown at the event. Intel was a gracious host and the speakers held the attention of the attendees until the very last moment. The agenda of the Steering Committee members goes beyond just holding periodic events. They

care deeply about Arizona's future high-tech workforce and about gaining visibility and recognition for SEMI member company contributions to jobs in Arizona."



## **IDC Expects Worldwide Semiconductor Market 6-7% Revenue Growth in 2012**

According to the International Data Corporation's (IDC) semiconductor applications forecaster, worldwide semiconductor revenues increased more than 3.7% year over year to \$301 billion in 2011. Looking forward, the organization expects the current semiconductor cycle to bottom out in the second quarter of 2012, with fab utilization rates accelerating in the second half of this year. According to Mali Venkatesan Research Manager, overall semiconductor revenue growth is expected to be in the 6-7% range for 2012.

IDC's SAF tracks more than 100 semiconductor companies. Over 40 of these companies experienced year-over-year revenue growth greater than 5%, while about the same number of companies saw their revenue decline by more than 5%.

Intel, with total semiconductor revenues of \$51.8B in 2011, once again was the overall market leader. Samsung was the number two vendor overall with semiconductor revenues of \$29B. Rounding out the top 5 chip suppliers were Texas Instruments, Toshiba, and Renesas Electronics. The next five suppliers were Qualcomm, Hynix, STMicro, Micron, and Broadcom. Together, the top 10 vendors represented 53% of total worldwide semiconductor revenues, an increase of 3% over 2010. The top 25 vendors captured 72% of

overall semiconductor revenues for the year.

Within the semiconductor device types, microprocessors registered strong growth due to high demand and increased ASPs for Intel's chips. Similarly NAND revenues also increased. However, DRAM saw revenue decline more than 25% due to supply glut and falling ASPs. Pure play DRAM vendor Elpida Memory saw revenue declines of 40% in 2011, ultimately leading to its bankruptcy earlier this year.

Both Asia/Pacific and Americas showed growth above the industry average, while Japan and Europe showed negative growth. Among the market segments, semiconductor revenues for the computing segment declined year over year due to the DRAM price collapse. The consumer segment was essentially flat, while wireless communication and automotive

segments registered over 10% year-over-year semiconductor revenue growth.

### Kelvin Contactor for High Power Applications



Semiconductor test equipment manufacturer, Multitest announces the debut of its latest Kelvin contactor, the ecoAmp™, a solution for high-power applications of 500+ Amperes.

This Kelvin contactor was developed specifically to respond to the challenging

requirements of high voltage/high current test. To achieve equal current symmetry over I/Os within the contactor, the contacting resistance needs to be held low and stable. Resistance stability is influenced by the contact spring itself and the condition of the device pin.

Additionally, the contactor must be able to stand the high thermal stress and support temperature stability during test. Thermal energy dissipation requires thermal management within the contactor.

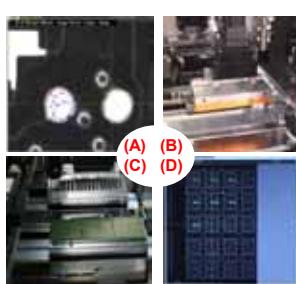
The ecoAmp™ is designed for an electrical performance of 500+ Amperes with a maximum inductance of 4.5 nH for 0.5 mm pitch. It is applicable for the complete temperature range from -60° to 175°C. Based on volume production-proven Multitest Cantilever technology, the contactor reportedly features excellent mechanical performance with a lifespan of 1 Mio. insertions. 

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solutions, covering nearly all major package categories. The company offers semiconductor assembly and testing services for a broad range of integrated circuits, including mixed signal, analog, and memory, areas for which units are manufactured in high volume.

### Carsem

Carsem's specialty is meeting the tight tolerances of very small packages, and offers numerous SOs within their package portfolio. They also package MEMS chips, which are coupled with ICs, and have more complicated packaging issues. The company produces a huge volume of assembly output, plus a full range of turnkey test services for RF, mixed signal, analog, digital, and power devices. They cater to the automotive, telecom, computer, and consumer electronics industries.

### OSE

OSE offers testing services and electronics manufacturing services (EMS/CEM) in addition to IC packaging

services. The company assembles a range of IC packages, without indulging in the higher tech packages such as stacked packages and SiPs.

### Unisem

Unisem also offers a broad mix of package solutions. The company's turnkey services include design, assembly, test, failure analysis, as well as electrical and thermal characterization. Wafer bumping is also offered for their flip chip packages. The company also packages some MEMS devices.

### So What Makes a Successful OSAT?

The success formula lies in a complete package portfolio, rather than just a narrow range of a few package solutions. This broad spectrum grabs the higher revenue packages, SiPs, stacked packages, FBGAs, BGAs, etc., as well as the multitudes of smaller packages such as QFN, SO, and the like. The smaller, lower I/O packages are in high volume demand in any economy, used to package the multitude of

analog and simple logic chips.

Currently, handheld electronic gadgets are all the rage; so ensuring a portfolio of packages that are aimed at these consumer electronics makes a lot of sense. These include stacked packages and SiPs. Flip chip and through silicon vias (TSVs) offer advanced performance at a reduced size, which also yield increased profits for the OSAT. These are included in the portfolio of the higher performing OSATs. The leading OSATs push the leading edge, and consider package development critical. They are aggressive at pursuing the top customers for volume production of higher revenue packages.

Test and turnkey services are also part of the services offered by the leading OSATs. The more complete a service is to meet customer's needs, the more successful the company. One stop shopping helps the customer, and the OSAT bottom line. 

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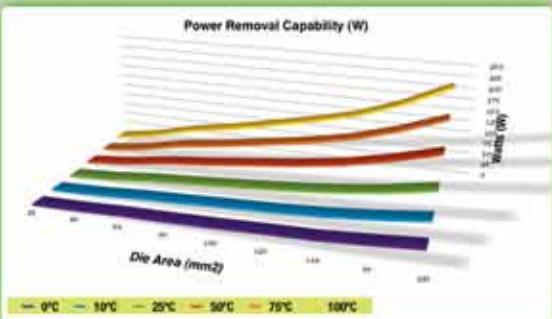
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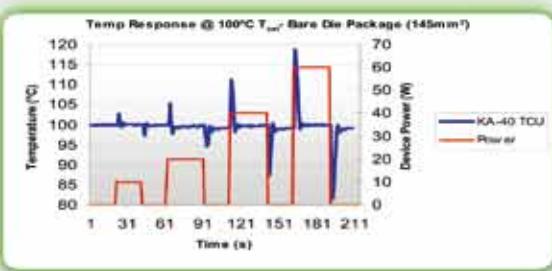
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