

ChipScale

www.ChipScaleReview.com

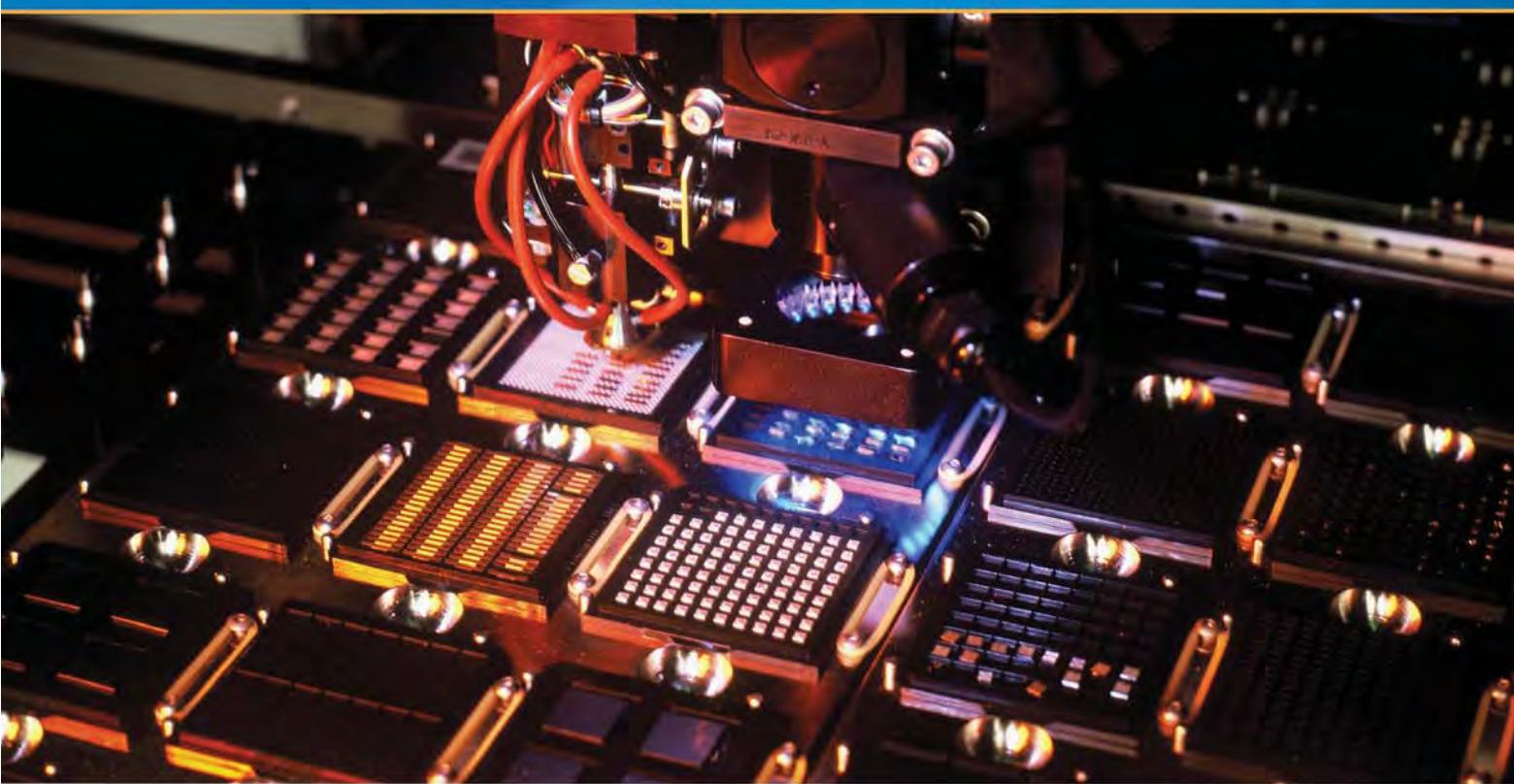
REVIEW®

The International Magazine for the Semiconductor Packaging Industry

Volume 15, Number 4

July - August 2011

- Cost-effective Collaboration
- The Many Flavors of TSVs
- Next-Gen Test Handlers
- Designing for Performance
- 3D Metrology and Defect Inspection
- International Directory of Automated Encapsulation Systems



MRSI-M5

Typical Applications

- Microwave / RF Modules
- MEMS
- Advanced Semiconductor Packages
- Multi-chip Modules
- Hybrid Devices
- Photonic Packages

MRSI-M5™ Setting the Standard for 5 Micron Die Bonding

Accurate, stable, fast and reliable, Newport's MRSI-M5 provides advanced assembly solutions for complex epoxy die attach, eutectic and flip chip bonding. It's the next generation assembly work cell you've been waiting for – from the company that has set the industry standard for 20 years.

The MRSI-M5 achieves 5-micron placement accuracy with a highly stable machine platform and the market's most advanced lighting and machine vision. It has a large work area for flexible, high volume production and "feather touch" force control to handle delicate devices.

With Newport you can rest assured that you are working with an industry leader who delivers global support, process experience and manufacturing expertise. Visit newport.com/bond1 for more information. Or call **978-667-9449**.

 **Newport**
Experience Solutions

CONTENTS

July-August 2011

Volume 15, Number 4



In addition to being chock full of technology features, this annual SEMICON West issue features a SEMICON West product showcase, and a SEMI authored column providing a status update on the 3D standards effort. ECTC 2011 was a huge success and you'll find the review and photos to prove it. There's also a featured interview with STATS ChipPAC, giving an inside look at one of the top 4 OSATs in the world.

Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

FEATURE ARTICLES

Impact of 3D ICs with TSV is Profound but Complex and Costly - Is There 16 A Better Way?

Rao R. Tummala and Venky Sundaram, *Georgia Institute of Technology PRC*

Collaborating for Cost Effective Semiconductor R&D 20

Simon Deleonibus, *CEA-Leti*

The Many Flavors of TSVs and Its Uses 26

Phil Marcoux, *PPM Associates*

New Test Handler Generations for New Challenges: Finding the Best Platform Strategy 30

Barbara Loferer, *Multitest*

THE BEST BURN-IN SOLUTION

- Individual temperature control for each device under test up to 150 Watts
- Individual pattern zone per burn-in board slot
- Up to 24 temperature channels per burn-in board
- Tests devices at a maximum temperature of 150°C
- System capacity of 384 devices under test with individual temperature control per device
- 128 digital I/O channels per burn-in board
- 16 programmable voltage regulators with 1080 amps of DUT power per burn-in board 8 high-current supplies (0 to 4 volts at up to 125 amps each) 8 low-current supplies (0 to 6 volts at up to 10 amps each)

**MICRO
CONTROL
COMPANY**

7956 Main Street NE
Minneapolis, MN 55432
USA
Phone: 763-786-8750
800-328-9923
www.microcontrol.com

**The Choice is Clear...
the HPB-5A/5B for
High-Power Burn-In
Requirements!**



NOW AT THESE WORLDWIDE TEST HOUSES:

EAG Labs/USA • ISE Labs, Inc./USA
LSI Logic Corporation/USA • STS/USA
ASET/Taiwan • Avi-Tech/Singapore
KES/Singapore • Stats ChipPac/South Korea

The technology in which the sun never sets **HANMI Semiconductor!**



**Technology Trusted by
over 220 companies in 20 countries around the world**

HANMI Semiconductor has the number one market share at semiconductor manufacturers with expertise that more than 220 companies rely on. We are also leading development of PCB, semiconductor, photovoltaic, and LED equipment technology.

HANMI Semiconductor
Since 1980

#532-2, Gajwa-Dong, Seo-Gu, Incheon, 404-250, Korea
TEL +82-32-571-9100 FAX +82-32-571-9101 www.hanmisemi.com

SAWING & PLACEMENT (MODEL : SAWING & PLACEMENT - 20000D)



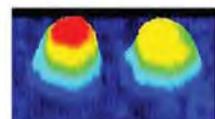
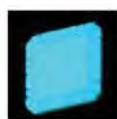
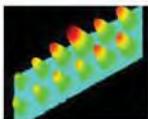
DUAL CHUCK SAWING CUT PROCESS
& MULTIPLE UNIT HANDLING



Highest productivity through
the individual operation
dual chuck sawing process

3D VISION INSPECTION SYSTEM (MODEL : 3D VISION INSPECTION)

TRUE 3D VISION INSPECTION
IN PMP TECHNOLOGY



FLIPCHIP BONDER (MODEL : FLIP CHIP BOND - A100)



HIGH SPEED & HIGH ACCURACY
BONDING SYSTEM FOR FLIPCHIP



LASER ABLATION (MODEL : LASER ABLATION - 3000)

FIELD PROVEN EXCELLENT
LASER ABLATION QUALITY



KYZEN

All around the world Kyzen cleaning experts work with our customers to find the best possible solution to their cleaning challenges.

With Kyzen You Can Expect:

- ✓ Increased Product Reliability
- ✓ Residue Removal From Fine Pitch and Low Standoff Packages
- ✓ The Latest Cleaning Technology and Process Design
- ✓ Experienced Process Engineers
- ✓ Environmentally Friendly Solutions
- ✓ Proven Results

 **KYZEN**

Nashville, USA ♦ Manchester, USA ♦ Maldegem, BE
Penang, MY ♦ Shenzhen, CH ♦ Shanghai, CH ♦ Guadalajara, MX

FEATURE ARTICLES

Metrology and Defect Inspection Critical for Bonded Wafer Yield Greg G. Baker, <i>Olympus Integrated Technologies America, Inc.</i>	35
Step-and-Repeat UV Imprint Lithography for Wafer-level Camera Manufacturing G. Kreindl, T. Glinsnera, M. Kasta, D. Treiblmayra, and R. Miller, <i>EV Group</i>	42
Predictive Modeling to Prevent Thermal Stress Failures in Electronics and Photonics Ephraim Suhir, <i>UC Santa Cruz</i>	48
Package Design: A Performance Killer or a Savior Madhavan Swaminathan and Bill Martin, <i>E-System Design</i>	52

DEPARTMENTS

From the Publisher Kim Newman, <i>Chip Scale Review</i>	6
Test Patterns Is Traditional ATE Done For? Paul Sakamoto, <i>DFT Microsystems</i>	8
Guest Editorial 3D IC Standardization is Underway James Amano, <i>SEMI</i>	10
Industry News <i>Chip Scale Review Staff</i>	13
International Directory of Automated Encapsulation Systems Ron Molnar, <i>Az Tech Direct LLC</i>	33
Interview STATS ChipPAC's Secret Sauce <i>Chip Scale Review Staff</i>	39
SEMICON West Product Preview <i>Chip Scale Review Staff</i>	58
What's New!	60
Advertiser Index, Advertising Sales	64

OPEN-molded Plastic Package™



Quik-Pak's NEW Open-molded Plastic Package

- Superior bondability
- Standard and Custom body sizes and lead counts
- Ready when you need them
- Full assembly services available

Quik-Pak™
Microelectronic Packaging & Assembly Solutions
www.icproto.com

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Ron Edgar Technical Editor

redgar@chipscalereview.com

Françoise von Trapp Senior Technical Editor

fvontrapp@chipscalereview.com

Ron Molnar Contributing Editor

rmlnar@aztechdirect.com

Sandra Winkler Contributing Editor

slwinkler@newventureresearch.com

Dr. Tom Di Stefano Contributing Editor

tom@centipedesystems.com

Paul M. Sakamoto Contributing Editor Test

paul.sakamoto@comcast.net

Jason Mirabito Contributing Legal Editor

mirabito@mintz.com

Carol Peters Contributing Legal Editor

cpeters@mintz.com

SUBSCRIPTION INQUIRIES

Chip Scale Review

T 408-429-8585

F 408-429-8605

Carrie Stalker

cstalker@chipscalereview.com

Advertising Production Inquiries:

Kim Newman

knewman@chipscalereview.com

EDITORIAL ADVISORS

Dr. Thomas Di Stefano Centipede Systems

Dr. Andy Mackie Indium Corp. of America

Dr. Thorsten Teutsch Pac Tech USA

Charles Harper Technology Seminars

Dr. Guna Selvaduray San Jose State University

Prof. C.P. Wong Georgia Tech

Dr. Ephraim Suhir ERS Company

Nick Leonardi Premier Semiconductor Services

Copyright © 2011 by Gene Selven & Associates Inc.

Chip Scale Review (ISSN 1526-1344) is a registered trademark of Gene Selven & Associates Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$85 per year to Canada or \$95 per year to other countries. In the U.S. subscriptions by first class mail are \$75 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER



Much More than More than Moore

A

nother trip around the sun, and here we are once again at SEMICON West. This annual event always inspires me to stop and take the industry's collective temperature. I'm happy to report that things are looking brighter than ever, and as consumer electronics continue to be all the rage, with the explosion of smart phones, tablets, and cloud computing, optimism and enthusiasm for things to come once again reign as the overall sentiment across the semiconductor device packaging ecosystem.

I recently returned from the 61st Electronic Components Technology Conference (ECTC), held this year at the Swan and Dolphin Resort at Disney World, in Lake Buena Vista, Florida where *Chip Scale Review* was the official media sponsor for this event. Organizers of this event (IEEE and CPMT) report some impressive statistics including increased attendance (over 1,000 attendees from 32 countries); 342 high caliber technical presentations; over 60 papers/posters presented on 3D/TSV (a hot topic for sure); 16 professional development courses attended by a record 386 participants; and 61 Technical Corner exhibitors. Further into this issue is a review of ECTC with photos of some familiar faces and more indepth coverage on this important industry event.

Over lunch the first day, I had the opportunity to hear Nasser Grayeli, VP Manufacturing Group and Director of Corporate Quality Network at Intel, who set the stage for the week with his keynote address, Challenges and Opportunities Ahead... Are we ready for the future digital world? I would have titled his talk "Much More than More than Moore". A mouthful, I know, but it really describes the near-future world he talked about, where "more people will be doing more things with more types of devices." He offered astounding numbers to support this prediction. By 2015, Grayeli predicts that there will be 1 billion more internet users, 10 billion more connected devices, 8 times the internet traffic of today, and 16 times more storage needed. He says that new approaches and capabilities are a "must have" to survive in this rapidly progressing world, where technologies and form factors change at warp speed and are increasingly more complex. Maintaining quality and reliability is critical to success, and involves collaboration across the entire ecosystem and supply chain.

Here at *Chip Scale Review*, we couldn't agree more! We believe that it's our job to be that conduit of information, continuously bringing quality technology features from all over the world and across the wafer level packaging supply chain to keep our readers informed about the latest and greatest new processes, materials, technologies, architectures and more. In this edition, get an inside look at collaboration for R&D from Simon Deleonibus of Leti. Rao Tummala of Georgia Tech shakes up the 3D world with a report on PRC's progress with 3D silicon interposers. Additionally, Phil Marcoux provides a thorough primer on TSVs. EVG contributed a piece on nanoimprint lithography for wafer level cameras. Wondering about signal integrity solutions for package design? We've got that too, thanks to Madhavan Swaminathan and Bill Martin, of E-System Design.

Kim Newman

Publisher

40+ years of perfect pitch.



And now, the perfect name

QinexTM

Introducing Qinex, the new brand name for superior interconnection solutions from Sensata Technologies. Qinex, the new word in perfect pitch.



Sensata
Technologies

QUALITY. High-value interconnection solutions since 1970.

- 24/7 global engineering
- 24/7 global support teams
- Local engineering and sales
- Six Sigma quality management
- Proven, reliable high-volume manufacturing
- Expert molding, design, and customization

INNOVATION. More I/O choices, smaller form factors, superior performance in less time.

- Latest 3D design tools
- On-site model shops
- Rapid prototyping
- Advanced thermal analysis
- Design on demand
- Broad range of innovative contact designs

PARTNERSHIP. In a fierce global market, only Qinex reliably supports the innovation, reputation and competitiveness of your business. We'll work with you to get it right, the first time.

**40+ years of perfect pitch.
And now, the perfect name.**

WEB www.qinex.com

EMAIL qinex@sensata.com

CALL 1-508-236-1306

Is Traditional ATE Done For?

"It's the end of the world, as we know it..."

- R.E.M

By Paul Sakamoto, Contributing Editor [[DFT Microsystems](#)]



Paul Sakamoto came to Silicon Valley from Oregon State University in 1977. His first job was in product and test engineering at Intel. He has worked at Megatest, MCT, Credence, Inovys and is currently CEO of DFT Microsystems. He is a long time author of this column in Chip Scale Review and can be reached at paul.sakamoto@comcast.net.

It was but ten years ago that worldwide ATE revenues had grown to almost \$7B a year. It had been a long haul up from less than \$1B a year in the early 1980s. The semiconductor industry had hit right around \$200B at the turn of the century, and most pundits were forecasting \$300B on the near horizon with \$1T (Trillion) annual revenue just beyond that. The ATE space was supposed to grow proportionally and bless its seven or eight viable participants with ever-growing revenues and profits. The future seemed rosy. The biggest problems facing the leaders of the ATE companies seemed to be what companies to buy, where to get enough people and how to secure adequate supplies. I can personally remember urgent discussions regarding the entertainment for our company's SEMICON West party.

Not only was that as good as it ever got for ATE, but I'm predicting that this was as good as it will ever get. There are more

than a few who believe this already, but in this column we'll briefly discuss why.

The reasons behind the decline of the ATE industry can be debated to no end. I am sure that there will be more than a few discussions about this topic during SEMICON West 2011, which should be occurring as you read this. My favorites are:

1. The relentless focus of the semiconductor customer companies, and their subcontractors, on reduction in the absolute dollar amount (versus the percentage of their revenue) spent on test. This drive insured that the R&D money spent by the ATE suppliers would never result in a "fair share" of the gains provided.

2. Intel. Schlumberger was forced to create the partial DFT (design for test) system called "DEFT" specifically for Intel's requirements. It's unclear how much money the supplier made in this deal, but it did not leave them a strong company since the platform worked only for Intel processors. Later, Intel got Advantest to bid the Open Architecture systems for the "Semiconductor Test Consortium" or STC. Advantest sold a lot of systems, but it is once again unclear how much money they made. It is a matter of record that during much of the shipment run of the Intel system Advantest was not making much money - in fact they had a lot of losses. The vast majority of the STC systems went to Intel, and Advantest was left with no choice but to buy Verigy in order to enlarge their presence in the SoC test market with a high-end offering. Other ATE companies also spent a lot of time, money and effort

in trying to gain Intel's favor. In the end, Intel is making most of its own testers this next generation. All the effort put into the last two Intel centric commercial ATE platforms helped them learn how to do it. So, the largest non-memory ATE customer is essentially gone forever from the test industry's revenue picture.

3. The vast amount of consolidation in the ATE customer base. It's hard to argue against the efficiencies gained, but it has been a huge factor in reducing ATE purchases.

4. The changing of the quality bar. There are no official numbers published on this that I know of, but then why would there be? Semiconductor suppliers would have to, in many cases, admit that they don't test all that much. I've personally witnessed orders go away because customers decided that they didn't receive a lot more returns if they tested versus not testing. This is especially true in high volume consumer applications such as mp3 players, phones, toys, games, Bluetooth accessories, etc. Nobody will admit this, but it is absolutely true that not every wafer is probed before it is packaged and not every package is tested before it is mounted. It is true that the consumer ends up doing a lot of testing. If you've ended up receiving defective electronics in the last few years, this is likely why. Test quality and associated expense is a purely economic decision in most companies today and there is seemingly no technical veto in many cases.

What this all means is ten years from now there will be no "ATE Industry." Given current market trends, we can expect total revenues to shrink to well below \$2B/yr. If the surviving ATE companies spent 15% of their revenue on R&D, a very aggressive amount, it would be a pitiful \$300M. What relevance does this have to a \$500B semiconductor industry, which will likely be composed of a mere handful of super players?

Not much!

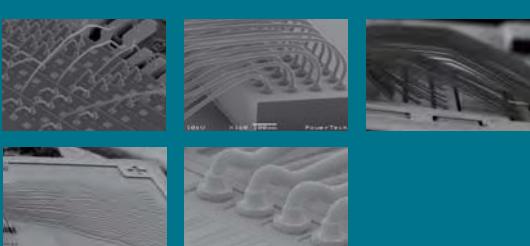
PTI Powers Integration Technology Revolution



wafer thin to 20um



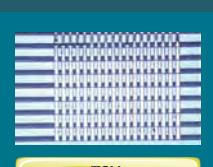
High density chip stacking



Advanced wire bonding



Cu pillar bump



TSV

As the largest merchant memory IC package and test design and manufacturing service provider in the world, PTI has enabled its customers products to deliver leading edge performance in advanced computing, wireless, consumer, and industrial applications around the world.

Advanced core process technologies for wafer thinning, die stacking, ultra low loop wire bonding, copper pillar flip chip assembly, and surface mount enable PTI's seven highly efficient global manufacturing facilities to deliver a wide range of high performance and cost effective package and test solutions.

Headquartered in Hsinchu, Taiwan, PTI's unique vertically integrated network of alliances provides customers with a robust suite of design, development, and manufacturing services for wafer sort, highly integrated packaging such as MCP/SCSP (Multichip Package/Stacked Chip Scale Package), PoP (Package on Package), SiP (System in Package), final test and both upstream and downstream supply chain management services.

With a focus on delivering the next generation of IC integration solutions, PTI will leverage these core strengths to bring advanced 3D IC solutions incorporating TSV (through silicon via) technology to market.

PTI Group - PTI : www.pti.com.tw

MTI : www.mti-hsip.com.tw

Contact window : info@powertech-usa.com

GUEST EDITORIAL

3D IC Standardization is Underway

By James Amano, [SEMI]



James Amano has led the SEMI International Standards Program since 2008. Prior to joining SEMI in 2000, he worked as the Silicon Valley sales engineer for Matsusada Precision, and as a trade specialist for the Japan External Trade Organization (JETRO). He holds degrees in Economics and Environmental Conservation from the University of Colorado at Boulder.

Given their potential for increased performance, smaller footprints, and reduced cost and power consumption, 3D IC technologies are now on the leading edge of innovation, with the industry poised to jump from concept to commercialization. However, multiple manufacturing challenges must first be solved, as 3D ICs' increased design and mechanical complexity can lead to increased manufacturing defects, as well as thermal management issues and signal interference. While 3D integration using through silicon vias (TSVs) promise a fundamental shift for current multi-chip integration and packaging approaches, cost-effective, high-volume manufacturing(HVM) will be difficult to achieve without standardized equipment, materials, and processes.

The needs and opportunities for 3D IC manufacturing standards were first

explored at SEMICON West in 2010, and the first 3DS-IC SEMI Standards Committee was formed in North America late last year. After a kick-off meeting in January, the 3DS-IC committee met again during the recent NA Spring 2011 meetings and made further progress in targeting the Committee's initial priorities. At the conclusion of the meetings, activities had been organized into three Task Forces (TFs): Thin Wafer Handling, Bonded Wafer Stacks, and Inspection and Metrology (**Figure 1**).

Thin Wafer Handling

The Thin Wafer Handling TF aims to develop standards for reliable handling and shipping of thin wafers and dies (e.g., micro-pillar grid arrays, or MPGA) used in HVM. As part of this effort, the TF will define thin-wafer handling requirements

including physical interfaces used in 3DS-IC manufacturing, shipping requirements, packaging, reliability, and other relevant criteria for both thin wafers and MPGAs.

The TF's first effort is a guide for multi-wafer transport and storage containers for thin wafers. Current standards for shipping boxes, FOUPs, and FOSBs are not well suited

for the reliable storage and transportation of thin wafers and dice on tape frames used in 3DS-IC manufacturing. Wafer thicknesses of 30-200 μm will need significant changes to the current design criteria of current wafer transport and storage containers. This document will include specifications for tape frames, thin wafers on tape frames, container capacity requirements, and transportation/vibration and mechanical shock requirements.

Future topics for the Thin Wafer Handling TF could include shipping carriers for thin wafer (wafer cassette, box or frame), shipping carriers for dies (MPGA), and reliability test methods.

Inspection and Metrology

The Inspection and Metrology TF is working on standards to be used in measuring the properties of TSVs, bonded wafer stacks, and dies used in 3D IC manufacturing. Specific areas that have been identified to be in need of inspection and metrology standards include TSV physical properties (depth, top, bottom critical dimensions, side wall, etc.) and bonded wafer stack properties (overlay, bond inspection).

The TF will initially focus on the physical parameters of TSVs. Multiple different technologies exist for measuring various physical parameters of a single TSV or arrays of TSVs, such as pitch, top critical dimensions, top area, depth, and taper. However, currently it is difficult to compare measurements from the various technologies, as in some cases parameters are called by similar names but are different aspects of the same measurement. This standard will group the various technologies and allow for valid correlations and comparisons.

Additional candidates for standardization include whole wafer damage inspection (crack, break, etc.) at the macro level as well as inspection at the micro level (microbump, pad, etc.). The TF is working on a process

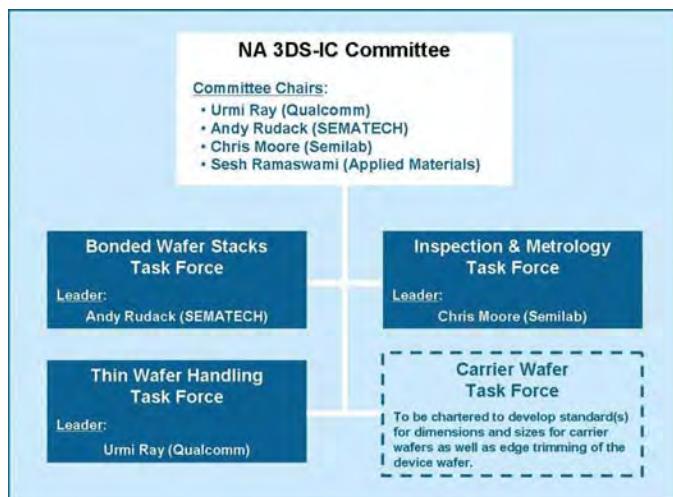
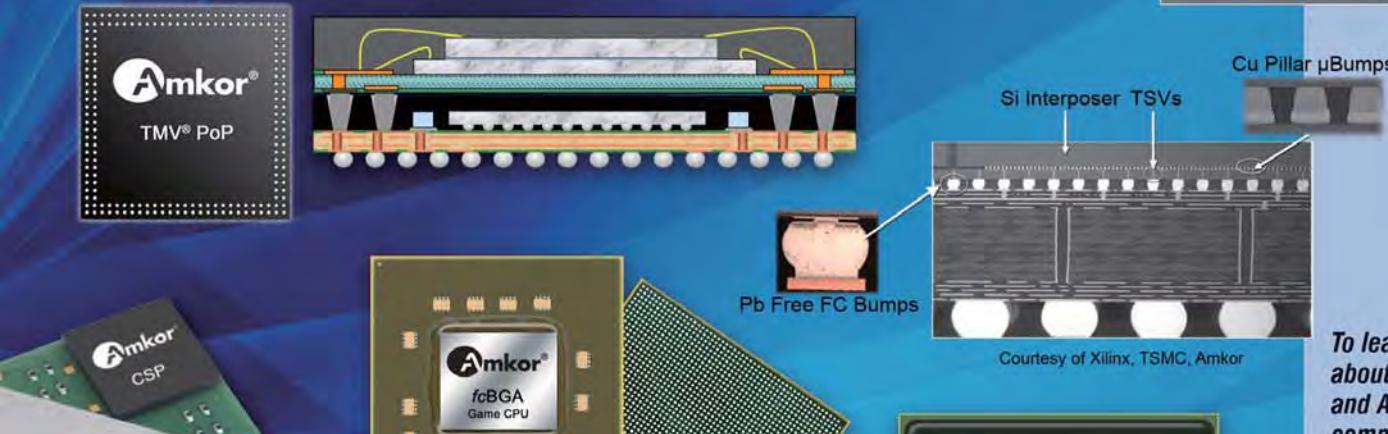


Figure 1. Organizational Chart of the North American 3DS-IC Committee

Amkor Technology

Semiconductor Packaging & Test Innovator and Technology Leader

- Advancing microelectronic technologies for over four decades
- Over a decade of leadership in 3D packaging; industry leader in PoP
- Broad turnkey services in FC and MEMS packaging
- Now aggressively expanding copper pillar from fine pitch flip chip to 20nm and TSV based applications



Courtesy of Xilinx, TSMC, Amkor

To learn more about our products and Amkor's complete portfolio, visit our booth at the following shows:

Semicon West 2011
July 12-14, 2011
Moscone North Hall
ATM TechZONE
Kiosk 6571A
San Francisco, CA

GLOBALFOUNDRIES GTC 2011
Aug. 30, 2011
Santa Clara, CA
Convention Center

IWLPC
Oct. 5-6, 2011
Marriott Hotel
San Jose, CA

VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND
TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

ENABLING A MICROELECTRONIC WORLD®
www.amkor.com

Amkor
Technology®

flow map that identifies known, as well as potential, areas for metrology, and all members are encouraged to identify areas where they can contribute.

Bonded Wafer Stacks

The Bonded Wafer Stacks TF has two activities underway. The first is a specification for parameters, as existing wafer standards

Polished Single Crystal Silicon Wafers do not adequately address the needs of wafers used in bonded wafer stacks. Wafer thickness, edge bevel, notch, mass, bow, warp and diameters are changed when wafer stacks are bonded together, or when wafer stacks are bonded and thinned. These deviations from wafer parameters specified in SEMI M1 have

hardware standards that reference SEMI M1, and are the motivation for a new standard to reflect wafer parameters associated with bonded and bonded/thinned wafer stacks. This activity will include both silicon and glass carrier wafers.

Similarly, the wafer identification and marking needs of bonded wafer stacks are not covered by current standards. Locations currently used for ID marking (such as backside near notch in SEMI T7: Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol) will be removed during backside thinning operations or edge-trim operations, or buried under an opaque layer of silicon and rendered unreadable by optical readers when bonded. Multiple wafer stacks will combine wafers with multiple process history, including tracking of temporary carrier wafers, and a standard needs to be developed to combine and track bonded wafer stacks with multiple wafer histories.

Lastly, an additional new task force is being formed to work on standards for dimensions and sizes of carrier wafers as well as edge trimming of device wafers. The output of this task force will be used in the development of the bonded wafer stacks specification by the Bonded Wafer Stacks TF.

These activities are just the beginning of what promises to be a global, industry-wide effort. Over 125 technologists from industry, research institutes, and academia around the world have already joined the SEMI 3DS-IC Standards Committee and are at work on these critical standards. The committee and task force will next be meeting at SEMICON West 2011 in July, and the Standards Program will also present a 3DS-IC Workshop to introduce the development and commercialization status of key aspects of TSV manufacturing and TSV integration. If you aren't involved, now's the perfect time - see you at SEMICON West!

TEMPORARY WAFER BONDING ULTRA-THIN WAFER PROCESSING

Solutions for 3D Integration and TSV

- ▶ Field-proven, ultra-thin wafer handling solution – up to 300 mm
- ▶ Integrity-assured bonding and de-bonding of high-topography wafers
- ▶ Flexible options – glass or silicon carriers, immediate carrier re-use
- ▶ Adhesive stability at high temperatures and defect-free removal – no additional cleaning tool required

www.EVGroup.com



www.emc3d.org



The key to your success

Join the Effort

Participation in the SEMI Standards Program is free, but requires registration. If you are not yet a member, please register at www.semi.org/standardsmembership.

INDUSTRY NEWS

Nordson Corp. Opens Chinese Demo Center for Advanced Technology Systems Customers

In an effort to meet the needs of customers in its Advanced Technology Systems operating segment, Nordson Corporation has opened a demo center in Dongguan, China. The new center will initially be focused on products and solutions provided by the company's Advanced Technology brands including Nordson ASYMTEK, manufacturer of dispense and coating systems; Nordson DAGE, manufacturer of high resolution X-ray inspection and bond testers; and Nordson YESTECH; manufacturer of automated optical inspection and X-ray systems. The facility is expected to provide greater access to equipment demonstrations, application engineering support, training, sales, and service for customers in South China's expanding high tech manufacturing industry.



Figure 1. Nordson leaders celebrate the opening of the company's newest facility in China. From left to right: Leyu Louis, Sales & Business Development Manager (Bondtester Division) Nordson DAGE; Greg Wood, Vice President, Nordson Advanced Technology Group, Asia; and Frank Wang, General Manager, Greater China Nordson ASYMTEK

According to Greg Wood, VP, Nordson Advanced Technology Group Asia, the Dongguan facility will complement existing facilities in Beijing, Shanghai, Guangzhou and Suzhou, adding to the current support. "Our business serving customers in electronics and related technology end markets in South China continues to grow. The Dongguan center allows us to be closer to these customers and offer solutions to meet their dispensing, coating and testing needs more rapidly," he explained.

Imec and Cadence Deliver Automated Solution for Testing 3D Stacked ICs

Imec and Cadence Design Systems, Inc. have introduced an automated test solution technology for design teams deploying 3D stacked ICs (3D-ICs). The technology addresses the test challenges involved as electronics companies turn to 3D-ICs as a way to increase circuit density and achieve better performance at lower power dissipation for mobile and other applications where space is at a premium. This collaboration is said to provide the design-for-test (DFT) and automatic test pattern generation (ATPG) technology that will make it easier to test 3D-ICs with through silicon vias (TSV) and help ensure that the stacked system will work as intended. Based on the concept of die-level test wrappers, the solution is expected to enable chip testing with TSVs and micro-bumps before, during, and after stacking, as well as after packaging. The design flow automation for adding 3D-enhanced IEEE 1500-based die wrappers to existing chip designs was created by enhancing the existing IEEE 1500 wrapper insertion support in the Cadence Encounter? RTL Compiler synthesis product. Initial results on customer designs reportedly showed that the 3D DFT structures can be implemented with negligible area costs—about 0.2%, which is far less than what some in the electronics industry have been speculating.

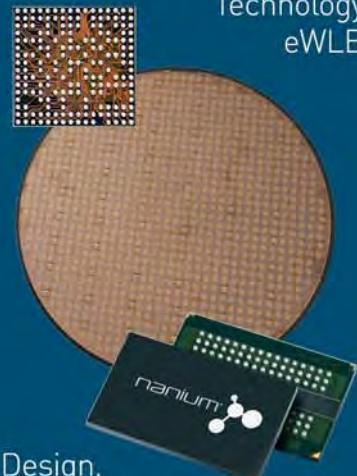
According to Brion Kellor, senior architect at Cadence, the DFT is the latest in a series of tools targeting 3D-IC TSV and silicon interposer capabilities. Three months ago, Cadence introduced the first wide I/O memory controller IP solution with a robust 3D-IC integration environment. "Collaboration is an essential element of effective Silicon Realization and the EDA360 vision we adhere to, and this initiative with imec demonstrates why," he noted.

"Using 3D-IC and TSV technology, electronics companies look forward to creating a new generation of super chips,"



Semiconductor Packaging, Assembly and Test

Leading Edge Fan-out WLP Technology eWLB



Design,
Development,
Engineering and
Manufacturing Services



www.nanium.com

said Erik Jan Marinissen, principal scientist at imec. “The imec-Cadence offering inserts DFT structures with minimal area overhead, and the ATPG method helps drive towards zero manufacturing defects on the TSVs. This unique offering reduces risk and promotes cost-effective fabrication of these chips.”

EV Group Teams with ITRI on Advanced MEMS Research and Development

EV Group (EVG), and Industrial Technology Research Institute (ITRI) have announced a collaboration to in the development of advanced manufacturing processes for next-generation MEMS devices. As part of the collaboration, ITRI has purchased two tools; a semi-automated wafer bonding system and an automated mask alignment systems that will be installed at ITRI’s Microsystems Technology Center. EVG will work closely with ITRI to develop, optimize and customize ITRI’s wafer-level bonding processes for its partners and customers. The bonder will reportedly play a key role in supporting ITRI’s transition to 200-mm MEMS wafer processing.

“At ITRI’s Micro Systems Technology Center, our mission is to create innovative applications and develop interdisciplinary technologies that will drive continued growth in the MEMS industry,” stated Tzong-Che Ho, Center Director of ITRI’s Micro Systems Technology Center, adding that ITRI is pleased to be working with EV Group to develop new processes that will enhance the competitive edge of partners and customers.

“ITRI has played a pivotal role in maintaining Taiwan’s position as a center of innovation and excellence in the field of microelectronics,” stated Dr. Viorel Dragoi, chief scientist at EV Group. “We look forward to continuing our long-standing relationship with ITRI, and leveraging our industry-leading technology and process expertise to support their MEMS process development and pilot production services.”

Alchimer Technology Breakthrough Targets Silicon Interposer Applications

Alchimer’s latest technology breakthrough is an interesting twist on the way semiconductor solutions generally presents themselves. Generally, technologies scale from bigger to smaller. This latest generation of wet deposition processes scales up to meet application needs. While the company’s flagship AquiVia line works on the vertical to molecularly grow nanoscale films, the latest addition, AquiVantage, works on the horizontal to grow microscale films. “We’re talking 1-5 μ m as opposed to 50-200nm thick,” notes Steve Lerner, CEO, Alchimer, “using the same processes, same tools, and materials; it’s just a different application.” AquiVantage is suited to via last backside metallization processes, such as isolation, redistribution layer (RDL), and under bump metallization (UBM). The most interesting application opportunity for both the AquiVia and AquiVantage processes to be used together is in silicon interposers. “With interposer we can simultaneously grow the TSV stack and the horizontal metallization,” notes Lerner. “Provided that you can balance the thickness, isolation can be grown in the via as well as on top.

Lerner says Alchimer has always seen itself as being very applicable to interposer processes because it’s one of those areas that will be extremely cost competitive, it’s far less critical than handling expensive wafers, and offers a huge value to the OSATs. “I personally believe that interposer is going to be not only our catalyst, but that of the industry as a whole,” predicts Lerner. “While everyone is waiting for (TSV) standards, some innovative people are going to come in and do interposer to capture certain products like Xilinx/TSMC did. We’re all super excited about this.”

ASE COO to Present Keynote at SEMICON West

ASE Group’s COO Dr. Tien Wu will deliver the opening keynote at SEMICON West 2011, with a presentation entitled,



“The New Dynamics of Semiconductor Business.” During his talk, Dr. Wu will explore long term trends and the current characteristics of slower industry growth, as well as the effect of increasing capital expenditure and R&D investment. He will discuss ongoing industry consolidation, and seek to identify the new dynamics, which are creating opportunities across the broad spectrum of innovative companies within the semiconductor business community. Dr. Wu will appear on the Keynote Stage, Esplanade Hall on Tuesday, July 12 , 9:00am-9:45am.

Silicon 360 to Productize Enhanced Bridge Products with Integrated Device Technology

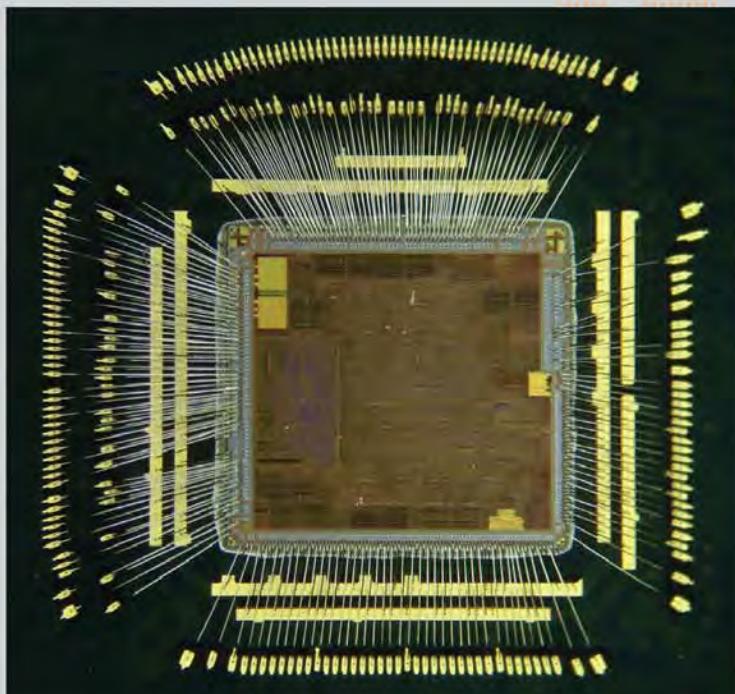
Silicon 360, LLC (Si360[®]), enablement provider of end-to-end semiconductor products and services, have entered into an exclusive agreement with Integrated Device Technology, provider of mixed-signal semiconductor solutions, that enables Si360 to manufacture and sell Universe II PCI-to-VMEbus Bridge products in various high-reliability and ruggedized versions to the military and aerospace industries

This definitive agreement establishes Si360 as the sole supplier for these high performance, ceramic and enhanced plastic package versions of this family of bridge products, IDT will continue to sell their standard CA91C142D products to their existing customers.

“This agreement further strengthens the synergistic partnership and extends the product portfolio between IDT and Si360,” said Don Pecko, Business Manager of Si360. “Designers of military and aerospace systems will now be able to utilize these industry-leading PCI-to-VMEbus bridge products in their newest applications such as VME Single Board Computers and I/O peripheral boards.”



Copper Wire



Copper Wire is a lower cost alternative to the traditional gold wire used in semiconductor packaging. Offering clear advantages, copper wire bonding is gaining popularity for products at 25 microns and below, where the majority of wire bond applications lie. ASE's copper wire bonding initiative is geared towards this group of applications. Bonding pad composition and wafer structure are major factors for copper wire evaluation, and ASE is customizing products based in specific customer needs.

Impact of 3D ICs with TSV is Profound But Complex and Costly - Is There A Better Way?

By Rao R. Tummala and Venky Sundaram [Georgia Institute of Technology PRC]

At Georgia Tech PRC, we think so; we call it 3D interposer. Unlike 2.5 interposer, the 3D interposer does not require through silicon vias (TSVs) in the logic chip. It is based on ultra-thin interposers that are the same thickness as the individual chips in the 3D IC stack; about 30 μ m. It has through vias that are the same diameter and same pitch as TSVs in the 3D ICs — about 5-10 μ m diameter on 15-30 μ m pitch. Unlike 3D ICs with TSV, however, the Georgia Tech (GT) approach is scalable, testable, and presents less thermal problems than the 3D IC stacks. It is also cheaper.

3D ICs with TSV are being widely developed around the world for two reasons. First of all, heterogeneous integration of logic, memory, graphics, power and sensor ICs requires it since these functionalities cannot be integrated into a single chip. Secondly, 3D ICs with TSVs offer improved electrical performance due to the short interconnect and ultra-high number of TSV interconnections between stacked ICs to address the perceived engineering limits in leakage and electrical performance of CMOS ICs beyond 11-16nm. But these benefits come at very high cost and with significant disruption in wafer fabs. Additionally, the 3D stack presents major technical and manufacturing challenges that include testability and yield, scalability, along with thermal and standardized IC interface challenges. The electrical performance improvement with 3D ICs is temporary. Intel has already announced that it will develop FinFET to overcome the shortcomings of traditional CMOS, to continue Moore's Law beyond 11-16nm. Improved performance alone is no longer a good argument for 3D ICs or heterogeneous ICs.

Georgia Tech PRC proposes and demonstrates an entirely different concept; one that addresses many of the

above challenges and allows packaging of ICs without disruption to wafer fabs. **Figure 1a** illustrates the current approach to 3D IC stacking with TSVs on an interposer such as silicon. In contrast, **Figure 1b** shows GT PRC's approach, which is based on an ultra-thin, double-side 3D interposer, made of either low-cost ultra-thin polycrystalline silicon or low-cost ultra-thin glass, not in 200-300mm wafer form but in large, 450-700mm panel form. Since the interposer is identical to one of the 3D ICs in the 3D stack with regards to through-via interconnection length and interconnect density, it behaves like a 3D IC stack with TSV. Such an approach does not require TSV in the logic chip yet it achieves the same bandwidth as 3D ICs with TSVs by virtue of logic on one side and memory stack on the other side interconnected and separated by the 30 μ m thick interposer. **Figure 2** shows the superiority of GT approach over the 3D ICs with TSV in signal delay between logic and memory as well as over wafer-based silicon interposers with thin oxide liner.

In addition, the 3D interposer approach allows for testability first of the interposer

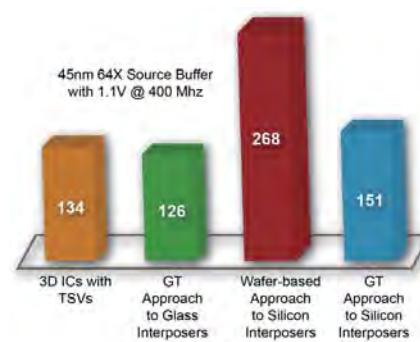


Figure 2. Superiority of GT 3D interposer approach over traditional silicon interposers and 3D ICs in signal delay (PS) between logic and memory¹

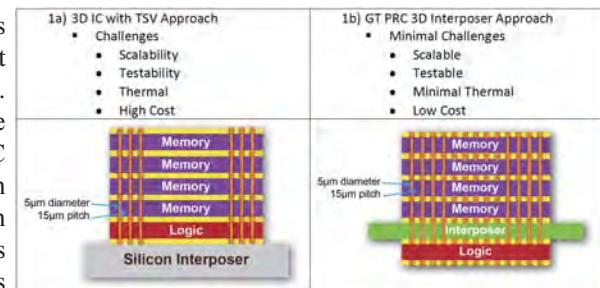


Figure 1a. 3D IC with TSV approach

Figure 1b. GT PRC 3D interposer approach for bandwidth¹

itself, followed by testing with memory stack and then with logic chip or vice versa. The 3D interposer approach is scalable by simply attaching chips side by side on both sides interconnected by ultra high I/O redistribution layers (RDL) made of 0.5 to 5 μ m wiring. The thermal management problems are simplified as well by virtue of separating the logic IC from the memory stack. The single most important benefit of this approach is a cost reduction by a factor of 5-10X over silicon interposers fabricated out of wafer fabs, as illustrated in **Figure 3**. Contributing reasons are many and include large panel, low cost through-via processes, and low cost RDLs.

3D Glass Interposer Technology

Glass has many advantages as an interposer material over silicon; namely ultra-high resistivity and availability in thin and large sizes. It is used as a thin and large panel in LCD displays, and thin-film metallization onto glass panels is well known in plasma displays. It has excellent resistivity on par with SiO₂ and is available in a variety of compositions with TCE ranging from 3ppm, matching silicon IC, to 9ppm, in between silicon IC and organic board. The main technical barriers of glass interposers are how to form large and ultra-thin glass panels, through-package-via (TPV) holes at high throughput, and how to handle ultra-thin glass panel substrates. For some

From One Engineer To Another®

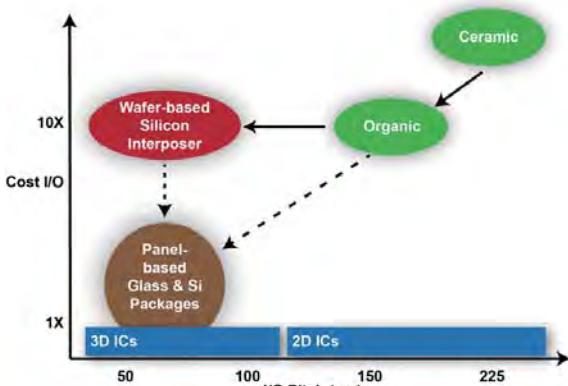


Figure 3. GT PRC panel-based strategy for low cost of 3D silicon and glass Interposer vs. wafer-based silicon interposer (courtesy of Tummala)

applications, low thermal conductivity, although higher than current organic polymer interposers, may be another barrier.

Recently, numerous glass companies have developed new and innovative processes for forming large and thin glasses in a variety of compositions. Laser ablation and photosensitive glasses for the formation of via holes are two of the most promising processes. Laser ablation provides small vias in glass but has conventionally been a serial process. GT PRC, in collaboration with one of its industry partners, demonstrated, for the first time, a parallel via formation method. This method enabled formation of more than a thousand vias simultaneously within few seconds. The result was a 33x33 (1089) through-via array of 19µm on 30µm pitch, drilled simultaneously in 55µm thin borosilicate glass.²

3D Silicon Interposer Technology

Table 1 compares and contrasts the GT PRC approach to the traditional wafer-based industry approach for silicon interposers. In general, the GT PRC approach to 3D silicon interposers has the potential to achieve equivalent interconnect density at significantly lower cost by a factor of 5-10X, by using the following:

- 1) Large panel-based substrate up to 450-700mm in size
- 2) Cheaper polycrystalline silicon
- 3) Low-cost TPV process without DRIE
- 4) Low-cost thick polymer liner
- 5) Low-cost, double-side RDL process.

The high I/O routing capacity combined with the low cost of GT PRC's approach to glass and silicon interposers presents a

Substrate	Single crystalline silicon wafer	Polycrystalline silicon panel
Size	300mm	450~700mm
Thickness	50µm with chem-mech polish	50-200µm without chem-mech polish
Hole Formation	DRIE	Laser
Liner Formation	SiO ₂ by CVD + Barrier layer by PVD	Polymer filling and laser via
Seed Layer	PVD	Electroless plating
RDL	BEOL	Dry film and plating

Table 1 .Wafer approach to silicon interposer vs GT approach to silicon interposer for lower cost and higher Performance.³



Andy Mackie PhD, MSc
amackie@indium.com

"Excessive warpage in my package-on-package process means I need a PoP solder paste, not a PoP flux. How do I know what kind of PoP solder paste to choose?"

Find out: indium.us/E107

- answers
- blogs
- tech papers
- one-on-one
- support
- live chat



scan code with
mobile device



INDIUM
CORPORATION®

ASIA • CHINA • EUROPE • USA

indium.com

©2011 Indium Corporation

number of application opportunities, both in mobile and high performance systems. Applications include mixed function digital logic-memory, RF, analog and MEMS in mobile applications. Additionally, glass and

silicon interposers can be applied for high performance applications requiring more than 10,000 I/Os between multiple logic ICs placed side by side in the same large package, as big as 50-70mm in size.

Industry Consortium at Georgia Tech PRC

3D interposer R&D is being performed at GT PRC under an industry consortium that includes the following companies to date: Asahi Glass, Atotech, Corning Glass, Dupont, EVG, Henkel, Life BioScience, Maxim, Namics, Qualcomm, Rogers, Schott Glass, Shinko, STMicro, and Zeon Corp. These companies fall into a complete supply chain for glass or silicon material, via hole formation tools, via metallization processes, RDL materials and processes, metalized substrates, package integrators or end users.

Summary

The 3D interposer presented here makes a compelling case for the 3D interposer over both 3D IC stacks with TSV as well as over traditional wafer-based silicon interposers. It doesn't require a new business model of having multiple ICs from different vendors to be integrated into one standardized 3D IC stack. It is scalable, testable and offers thermal solutions in a traditional way. There is no disruption to wafer fabs or loss of real estate within the CMOS chip to accommodate TSVs. While the initial concepts have been demonstrated at Georgia Tech, it requires additional R&D, and additional industry partnerships with both manufacturing and end user companies. 

References

- [1] G. Kumar, et al., "Ultra-High I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 217-223.
- [2] V. Sukumaran, et al., "Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package-Vias," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 583-588.
- [3] Q. Chen, et al., "Design and Demonstration of Low Cost, Panel-Based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs)," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 855-860.

THERE ARE NO SHORTCUTS TO A 5-MIL DOT

Small, repeatable volumes are a challenge. But not impossible if you have been creating them as long as we have. However, to do it well, you need three things:

Dispensing Expertise

in a variety of applications: micro-attach, precision fill, highly-repeatable patterns;

Feasibility Testing

and process verification based on years of product engineering, material flow testing, and software control;

Product Development

 for patented valves, dispensing cartridges, needles, and accessories.

For Micro Dispensing, there is one product line that is proven and trusted by manufacturers in semiconductor packaging, electronics assembly, medical device, and electro-mechanical assembly the world over.



DispenseLink® for Micro Volume Dispensing

www.dltechnology.com

DL Technology is a registered trademark of DL Technology LLC. DispenseLink is a registered trademark of DL Technology LLC.
HY-FLO is a trademark of DL Technology LLC.

Full Range Fluid Dispense

True Volumetric Dispensing

It's not an Auger, it's Total Fluid Control

From water to pastes, TRUE volumetric dispense of any fluid without drip or drool



Rotor/Stator in PCD Series Pump

GPD Global® PCD True Volumetric Dispensing technology improves all dispense processes as it is unaffected by syringe material level and viscosity changes due to pot life or temperature changes. With **volumes down to 1 µl and ±1% repeatability**, PCD technology can fit into any process.

PCD Technology is easily integrated into any robotic system for immediate process improvement or used on a benchtop for manual volumetric applications. And, of course, the PCD is available on all GPD Global® MAX, DS, and TMax Series dispense systems for the ultimate dispense solution.

Your Process, Our Pump

- Lubrication
- Underfill
- Pastes
- Greases
- Silicones
- Encapsulation

FREE sample - contact GPD

For improved material flow & repeatability,
GPD Global® recommends S Type Taper Tips



GPD Global®
Precision Dispensing Systems

Collaborating for Cost Effective Semiconductor R&D

By Simon Deleonibus, [CEA-Leti]

The increased cost of Semiconductor Research and Development (R&D) investment has lead integrated devices manufacturers (IDMs), equipment suppliers (ES) and research centers to cooperate and share their efforts. Today, the minimal R&D investment for developing nanoelectronics has surpassed the billion dollar range. Cooperation between institutes, universities, and companies—as well as between companies in complementary ways—has grown at various levels of the value chain. One example is the MINATEC Campus with CEA-Leti as a Core partner, in which the whole value chain is integrated from basic research to early stage development. Technology platforms capable of integrating “More Moore-”, “More than Moore-” and “Beyond CMOS”-types of devices exchange wafer know-how and technology steps with partners’ research and industrial platforms on a daily basis and worldwide.

The MINATEC Campus also hosts start-up small-to-medium size enterprises (SMEs) and common laboratories with main players and SMEs to value the whole innovation generation process. This model serves as an example to future heterogeneous co-integration of key enabling technologies by adding new campuses to the same site.

Since the early 1990's, collaborative research has been shared worldwide by different models in the framework of joint development programs (JDPs) between IDMs, ES, academia, and research institutes. SEMATECH and Semiconductor Leading Edge Technologies (SELETE) were set up as a safeguard from national industry. These consortia brought in IDMs and ES to evaluate future-generation equipment (SEMATECH) or to develop the process modules of the core process of future technology nodes (SELETE). In an open model, IDMs, fabless companies and ES collaborate in



Figure 1. The MINATEC Campus groups several platforms in the same location, bridging basic research and education to advanced development. These platforms use different wafers sizes and exchange wafers with other industry and research campuses worldwide day-by-day

affiliate program structures in a host institute or welcoming infrastructure such as IMEC or the IBM Alliance.

The French Way

The MINATEC Campus (Figure 1) is famous for dedicated joint efforts of the French national and local authorities in addressing overall competitiveness of national, European research institutes, universities, and enterprises based in the Grenoble area in the field of micro and nanotechnologies. It is a good example of concentrated effort on a specific thematic subject area—in this case micro and nanotechnologies and their applications—which is conducted in one of the French Competitiveness Clusters. In 2005, the French government selected 71 Competitiveness Clusters based on their excellence at the national level, which has international or national impact. Approximately 1B Euros have been dedicated supporting these clusters via a complex funding system involving national agencies, local authorities, or tax refunds for companies. Each of these Clusters dedicates effort to a specific domain. Main examples of Competitiveness Clusters with international impact are:

- The Grenoble MINALOGIC Pole, dedicated to Information and Communication MicroNanotechnologies.
- The Paris SYSTEM@TIC Pole,

dealing with complex systems for monitoring, supervision, regulation, and control.

- The Toulouse and Bordeaux Aerospace Valley, which specializes in aeronautics, space technologies and embedded systems.
- The Lyon AXELERA is dedicated to chemistry and environment, or Lyonbiopole, dedicated to vaccination and diagnosis

The French government declared that the responsibilities and funding come from a joint effort at the national and local level (regional and town communities), involving national funding agencies as well as local authorities and tax refunds or loans. A total investment of 1.5B Euros comes mostly from tax refunds to companies, co-funding from various agencies (ANR, Oseo, CDP), and local authorities.

The whole framework was structured by a 2006 Act defined by the French government for funding research from the basic level to industrial development, and through the intermediate stage of applied technology research (Figure 2), which strongly bridges the basic research to the development phase. The “Institut Carnot” label has been attributed to the research institutes or laboratories that contribute to intellectual property (IP) generation followed by its transfer to the industry.

This model is also practiced in the 96 German Kompetenznetze supported by the regional authorities (“Lander” governments) connected to the Fraunhofer Institutes, which operate under similar funding schemes. The six Italian “Technological Districts” have also been defined nationwide. In all cases, the general idea is to mobilize energies and efforts in an eco-system based on excellence to maintain and develop the competitiveness of the network by applying a mixed private and public type of co-funding. A strong local geographic asset is necessary to be efficient and pertinent: local enterprises, national laboratories, research institutes and academia are involved in the frame of focused projects. The goal is to give the local networks the highest visibility as possible beyond the local, national scales at the international level to enhance their competitiveness in a globalized economy.

The MINATEC model: Think globally and act locally.

The local Thematic Networks, based on excellence, are the “central nervous system” of the organization. The whole effort is to leverage and incite collaboration between local universities, national institutes, and local companies. The local networks envision a strong local asset and a wide distribution of their IP and more on material productions at the national, European, or international levels. This recognition is targeted at the fundamental and applied research, as well as advanced development stages. This will also be a pre-requisite to remain alive in a global competitive world.

The MINATEC Campus

The MINATEC Campus is an example of the complete value chain integration from fundamental research to industrialization. It hosts different institutes of CEA; such as Leti at the center of the system, as a micro, nanoelectronics, photonics, biotechnologies and systems R&D institute; INAC as the Fundamental Research Institute; Grenoble - Institut National Polytechnique; and local Grenoble and Metropolitan communities in the same geographic location. Inside this set up, one of the largest nanocharacterization centers worldwide supports the activities and develops characterization techniques as well. Academia, CEA and private companies — whether established or start ups — are co-inhabitants of the MINATEC campus. This campus is unique worldwide, where fundamental researchers, integrators, equipment suppliers, designers, and end users can meet face-to-face, and day-by-day.

The MINATEC Campus integrates (**Figure 1**) a set of buildings hosting CEA-LETI, the INP Grenoble Engineering School Phelma (Physics, Electronics and Materials) and an incubation area for new activities or companies; among which starting SMEs have a central position. In this area, the CEA-Leti technology platforms, operating 24/7, play a central role. They receive the support of the CEA Nanocharacterization Platform settled on the same campus. As a matter of fact, besides the undergraduate education dedicated platform hosted by Phelma, the CEA-Leti platforms host several clean rooms dedicated to collaborative research and development achieved on Si wafers of different sizes ranging from pieces of substrates to 300mm, in addition to 100mm and 200mm diameters sizes.

RTI...
**Where Innovative Solutions
Meet Improved Performance
and Reliability...**



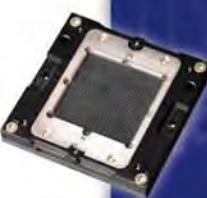
Machined Semi-Custom Burn-In Socket Solutions

Fast-Turn, High-Performance and Reusable Lids for Long Term Value



Lower “Cost-Per-Site” Test Socket Architecture

Innovative design, biased or joined signals help lower cost of test.



High Performance, High Pin Count Universal BGA

Test Multiple packages of the same pitch in a single test socket body



Positive “Scrub-Action” on Pads and Leads

Eliminates Solder Transfer Issues!



Positive Solder-Ball Contact

Secure Contact with minimal wear



Patented Flat-Pin High-Performance Contacts

Up to 40GHz Bandwidth @ 0.50nH



Robson Technologies, Inc.
www.testfixtures.com
(408) 779-8008

The MINATEC Campus platforms exchange wafers with other state-of-the-art clean rooms located worldwide, whether on research platforms or in factories (Albany Nanotech, IBM East Fishkill, ST-Crolles, Rousset and Agrate, SOITEC, etc.) as well as equipment suppliers facilities. A strict contamination control protocol is approved, qualified, and followed to allow such an exchange within the partners.

CEA-Leti promotes several types of collaborations with start-ups, its spin-offs, or already established companies. This has been a long tradition since EFCIS, the French ancestor of ST Microelectronics, started in 1971 on the Leti premises. Another example is SOITEC, founded in 1991 in the Leti clean rooms. The common laboratory model is often adopted on a specific focus or multi-year partnership. In the incubation area, several start-ups and common labs set up their office and facilities in a state-of-the-art environment. Examples include Microoled, which makes OLED based displays; Replisaurus, which is developing a new interconnect scheme with high aspect ratio (HAR) conductors; ARNANO, which is achieving highly secured mass storage and imaging by etching on sapphire; CYTOO, PX Theurapeutics, Fluoptics, and SERMA, all servicing in the field of physical characterization and reverse engineering; and Movea, dedicated to position detection by using MEMS devices in portable systems. 3000 researchers and company affiliates work on the MINATEC Campus.

A global policy and ecosystem involving local actors, linked to the national framework

The MINATEC Campus operates its activities in strong connection with the Grenoble Nanotechnologies Competitiveness Excellence Cluster MINALOGIC (**Figure 2**), dedicated to information and communication micro and nanotechnologies. To achieve this goal, incentives had to be given to define a good method and provide funding at the right level, whether public or private. Such programs would not be efficient without leveraging outputs of R&D results. The partners set

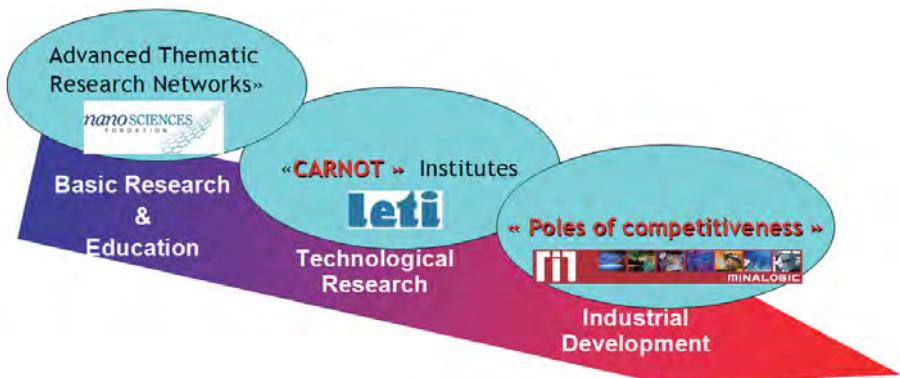


Figure 2. Featuring a view for R&D funding Global value chain at the French National Level and its declination at the Grenoble level through Basic Research and Education, Technological Research and Industrial Development

up project proposals and compete for funding in the frame of MINALOGIC calls. Projects in the More Moore and More than Moore fields are eligible. Part of the funding is supported by local, regional, and central government tax money, defining thus a “virtuous circle” in which funding comes back to the tax payers for the benefit of knowledge, wealth, new business, and employment creation. The MINALOGIC Pole represents 189 members 142 companies (81 % are SMEs), 15 research centers or universities, 15 local administrations, 14 funding agencies, and 3 venture capital companies. 155 projects have been identified, with an overall R&D budget of 1.7B Euros over 5 years, and with 535M Euros from local and national agencies.

Among the projects receiving the support from MINALOGIC is NANOSMART, which involves mainly CEA LETI and SOITEC, and allows for development of advanced ultrathin SOI substrates (200 men. years over 5 years). In the field of new circuit design architectures, the ATHOLE project has transferred a flexible and programmable architecture, thanks to a low power, high performance network-on-chip(NOC) technology. The ATHOLE project associates STMicroelectronics, Thales Communication, Coupling Wave Solutions (CWS), CEA Leti and Verimac (280 men. years over 4 years). Other realizations have been possible in the frame of the NANOPROJ project aiming at developing an ultra-small (ca. 1cm³ volume) embedded projector for nomadic, domotic and automotive

applications. The project involves STMicro, FagorBrandt, Optinvent, H2I Technologies and CEA-Leti (Total effort: 100 men.years).

Fundamental research cooperation

To leverage private initiative contributions to fundamental research funding, the French Ministry of Education launched a national program setting up 13 thematic local networks (Réseaux Thématiques en Recherche Avancée - RTRA) neighbouring their Competitiveness Clusters. These local networks involve the local university as well as the national laboratories and institutes that collaborate in the frame of Scientific Cooperation Foundations managing the funding (**Figure 2**). The middle and long term objective is to let private initiatives support visiting professors or young scientist positions based on the excellence and fame of the researchers. Private corporations are invited to support the chairs of excellence financially. In Grenoble, the Nanosciences Foundation operates “at the limit of nanoelectronics”: 1000 researchers cooperate in the frame of projects supporting the visiting professors and young scientist positions on various subjects such as quantum nanoelectronics, nanophotonics, nanospintronics, nanomaterials and nanofabrication, biotechnology and nanoelectronics interface, education, and fundamental research technology platforms. The actions of the Nanosciences Foundation are thus well matched to the MINALOGIC Competitiveness Pole, and the major part of its activities is associated with the MINATEC Campus. These foundations still

have to prove that they can fly by themselves in a context of economic crisis that does not incite private initiatives to support research, in a French context without any significant culture in that field. This effort represents an initial budget of 200M Euros over 5 years nationwide and 25M Euros at the Grenoble level over the same period.

One step further to define structuring investments to support a continuum between Fundamental Research and Advanced Development—the GIANT Grenoble University Campus.

The Grenoble Initiative on Advanced New Technologies (GIANT) (**Figures 3 a and b**) will be a unique West Campus located geographically between the rivers Isere and Drac (**Figure 3b**) which is a pre-figuration of a future Grenoble University. Three major themes are put forward in connection with their basic research (**Figure 3b**): micro-nanotechnologies, biotechnologies, and new energy technologies. In the near future, GIANT will involve six different campuses located one beside the other: MINATEC, dedicated to micro-nanotechnologies in the field of information and communication; GreEn (Grenoble Energies), in charge of new technologies for energy; NanoBio, working on biotechnologies; the basic research campus; the European Photon and Neutron(EPN) Campus, allowing access to synchrotron X-rays and neutron sources; and a technology management campus. This location is well placed near the historical sites of ST Microelectronics and Schneider Electric. The investment represents a 1B Euros investment and a manpower effort of 10000 researchers.

This initiative, started from a bottom-up approach, is well in line with the policy developed in wider frameworks such as the French National Grand Emprunt (Great Loan) and the European Key Enabling Technologies. These frameworks would certainly strengthen France and Europe in reshaping their high-tech global value chain from basic research to industrialization.

Other existing models

SELETE and SEMATECH are two examples of national collaborations built

on slightly different types of models. United efforts between national IDMs and equipments suppliers were put together to support R&D on the core CMOS part of nanoelectronics process at the beginning of 1990's for SEMATECH and in 1995 for SELETE.

The original idea of SEMATECH was to sustain US industry in the evaluation of new equipment types for next-generation ICs, and reduce the cost of

development. This initiative was mainly based on a reaction by the US companies to Japan's domination of the semiconductor business in the 1980's. SEMATECH was the first consortium to launch a 300mm initiative (I300I), which would reintroduce US domination in the business. However, this model failed for several reasons, due to its bottom-up based approach. First, the IDMs were not ready to share their own knowhow or give

New Horizons in Bond Testing

The Nordson DAGE 4000Plus is the most advanced bondtester on the market, representing the industry standard in bond testing.

Data Integrity

Developed by the world leader in bond testing technology, the 4000Plus offers unsurpassed accuracy and repeatability of data providing complete confidence in results.



See the 4000Plus bondtester in action at Semicon West Booth No. 5971

Featured Application

Hot Bump/Pin Pull on the 4000Plus

A unique patent protected technique for attaching a probe to solder bumps or paste and performing a pull test in accordance with the IPC standard IPC9708 pad cratering testing for surface mount and printed board assemblies.

The 4000Plus HBP application is achieved by simply selecting a specialized load cartridge which can be programmed to apply a temperature-time reflow profile to individual bumps/bonds using a probe. Pre-heating, soak, rate of rise, liquidus and cooling are all integrated into the 4000Plus Paragon® software for easy on screen profiling and control. A selection of standard probe sizes are available with custom tips available on request.





www.nordsondage.com | csglobalsales@nordsondage.com

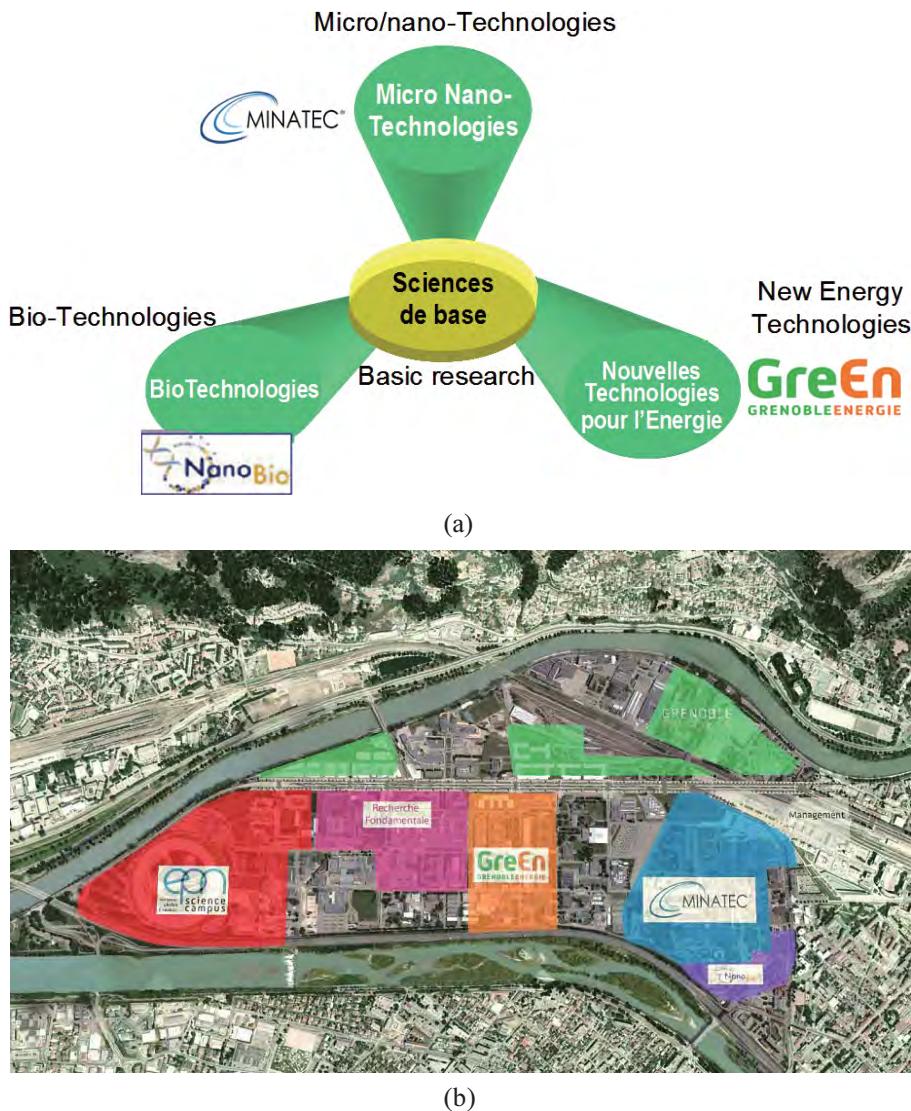


Figure 3. The GIANT (Grenoble Initiative on Advanced New Technologies) place where Heterogeneous Technologies meet: (a) thematic declination through Micro Nanotechnologies, Bio Technologies, New Energy Technologies and their campus linked to their Basic Research; (b) geographic location West of Grenoble where the GIANT will also include the European Photon and Neutron (EPN) and the Technology Management(not shown) Campuses

feedback from their knowledge acquired in the frame of SEMATECH; the assignees at SEMATECH were competing with their own colleagues, which made no sense as it increased the cost of R&D. Secondly, SEMATECH did not get the state-of-the-art tools (lithography for example) that the vendors preferred to place at the IDMs factory or development sites. Finally, many of the SEMATECH members have gone fabless, focused their efforts on internal development, made alliances with Asian founders, joined other consortia with state-of-the-art tools, or disappeared. In that context national solidarity was forgotten as a motto.

Today, SEMATECH is seeking for a new identity as a company and trying to get closer to the IBM Alliance and other initiatives such as Globalfoundries' in the New York State, while opening their alliance to partners outside America. Now, SEMATECH is concentrating on manufacturing effectiveness.

SELETE was the first example of a consortium organized around a defined objective to build the next-generation core CMOS with state-of-the-art tools. It was established as a reaction by Japanese IDMs (Fujitsu Semiconductor Limited, Panasonic Corp., Renesas Electronics Corp., ROHM Co., Ltd., SANYO Semiconductor Co., Ltd., Seiko Epson

Corp., Sharp Corp., Sony Corp., Toshiba Corp.) to the increasing influence of SEMATECH on the industry and 300mm development initiatives. It gained influence because the equipment suppliers, joining as share holders, made an effort to place state-of-the-art equipment with high-risk/high-gain challenge. Moreover, it started the 300mm initiative well before the industry would be ready to take over. Recently, however, many of the IDMs decided to concentrate their high-volume manufacturing efforts at foundries sites (TSMC, UMC, and Chartered). Today SELETE has evolved towards common governance with MIRAI in the framework of the Advanced Industrial Science and Technology (AIST). The organization works on selected topics agreed by the consortium, in which SELETE takes part nearest to application (EUV, Nanoscale Integration) and MIRAI focuses on Ballistic transistors on Si or III-Vs. Strong links for Basic Research are established in the frame of the AIST and Japanese Universities.

Sharing efforts in an open structure: IMEC and IBM

These platforms are open worldwide to assignees who share an affiliation program proposed at the R&D site by the means of an adhesion fee, reducing development costs by sharing efforts. The program can be upgraded by bilateral cooperation with a given assignee on the basis of a different fee. In both cases, support from public authorities (Flanders government in the case of IMEC, and New York State in the case of IBM) is essential to support this model. As it is open worldwide, this model brings in a multicultural dimension that is less present in SELETE or SEMATECH; recently partially open to new partners. A link with a nearby manufacturing site is missing in the case of IMEC, even though TSMC is affiliated. In the case of IBM, Chartered/GLOBALFOUNDRIES joined their Alliance, based at East Fishkill and Albany, and is now building a production site in the New York State with the help of public authorities and private investors.

One must keep in mind that major foundries located in Asian countries have made a strong commitment to education and bet on industrial investment, while

encouraging long-term investment supported by regional or national governments. In the IMEC and IBM models, lack of strong connection to manufacturing might turn out to be detrimental to the pertinence of research.

IMEC affiliate programs are shared by TSMC, Samsung, Intel, Infineon, Panasonic, NXP, and others. IBM Alliance hosts Chartered/GLOBALFOUNDRIES, Infineon Technologies, NEC Electronics, Samsung Electronics, Co., Ltd., STMicroelectronics, and Toshiba. CEA-LETI collaborates on the most advanced part with IBM at the University of Albany. In both IMEC and IBM models, collaboration with local universities and institutes cover the basic research side.

The Grenoble model and necessary cooperation in Europe: Heterogeneous Key Technologies co-integration.

The originality of the Grenoble model relies on a strong link between research institutes with the local, national, and European industries that have a view and connections at the international level. The day-by-day wafer exchange with other high tech platforms worldwide is another strong asset of the model as compared to the other existing models. Heterogeneous co-integration of key enabling technologies, necessary to ensure Europe's future, are under development in the frame of the Grenoble Research and Technology Platforms, where a continuum is practiced between basic research, technological research and industrial development. It is critical for Europe to recognize key enabling technologies by defining key investments needed in the future.

With almost 500M inhabitants, Europe is the wealthiest, most peaceful federation with the highest political stability worldwide. Nanoelectronics and "More-than-Moore" types of devices will particularly rely on key strategic enabling technologies that big nations or federations will need to survive in the future. These activities will generate, directly or indirectly, 15 to 20% of world's wealth in the 2020s. If South Korea, a country of almost 50M inhabitants, is capable of defining a long-term policy for high tech, giving birth to the 2nd IDM worldwide (Samsung), why can't the European federation afford to do so for the co-

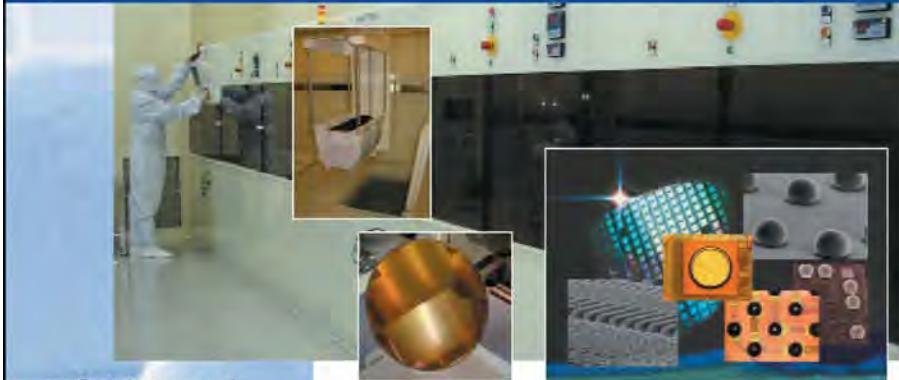
integration of key enabling technologies? Important challenges ahead must be faced to hit future milestones of co-integrating classical "More Moore" and "More-than-Moore" domains in a heterogeneous way, bringing up new applications by serving society beyond its information and communication needs, for healthcare, environment and various societal needs.

This is certainly a great asset that the Grenoble community was the first to put forward and that could become reality for future developments in the frame of GIANT.

Simon Deleonibus is a chief scientist and scientific director at CEA-Leti, MINATEC Campus, Grenoble, France. He can be reached at simon.deleonibus@cea.fr.

Global Low-Cost Wafer Bumping Services

• Europe – USA – Asia •



- Quick-turn and mass-production
- Highly competitive, low-cost bumping technology
- Exceptional quality through high-level expertise

PAC TECH PACKAGING TECHNOLOGIES

Pac Tech GmbH
Tel: +49 (0)3321/4495-100
sales@pactech.de
www.pactech.de

Pac Tech USA
Tel: 408-588-1925, ext. 202
sales@pactech-usa.com
www.pactech-usa.com

Pac Tech Asia Sdn. Bhd.
Tel: +60 (4) 6430 628
sales@pactech-asia.com
www.pactech-asia.com

NAGASE & CO., LTD.
Tel: +81-3-5640-2282
takahiro.okumura@nagase.co.jp
www.nagase.co.jp

Available Processes

- Electroless Ni/Au under-bump metallization
- Ni/Au bump for ACF or NCP assembly
- Solder paste stencil printing
- Solder ball drop for wafer-level CSP
- Solder jet for micro-ball placement
- BGA and CSP reballing
- Wafer backside thinning and wafer dicing

Special Features/Technologies

- Over 10 years experience
- U.S. Government Certified
- 4- to 12-inch wafer capability
- Wafer pad metallization: Al and Cu
- Solder alloys: eutectic SnPb37, lead-free, low-alpha, and AuSn
- Fluxless and contactless bumping for MEMS and optoelectronics
- Ni/Au interface for wire-bond applications

Please visit us at SemiconWest
North Hall, Booth 5577

The leader in low-cost electroless wafer bumping.

The Many Flavors of TSVs and Its Uses

By Phil Marcoux [PPM Associates]

Phil Marcoux is a semiconductor packaging consultant specializing in business and IP development. He is the past CEO and co-founder of ChipScale, Inc., one of the first WLP companies, and AWI the first US-based SMT company. Phil's website is www.oneppm3d.com

There is a belief that there are only two types of through silicon vias (TSVs), when in fact, there are more. They range in many sizes and cost variations similar to the variety of vias used to construct printed circuit boards (PCBs). For that matter, the earliest mass volume uses of TSVs are in devices called silicon interposers, which are little more than very dense printed circuit boards using silicon as the substrate material.

Options for Fabrication TSVs

The most discussed TSVs are called via-first and via-last TSVs. Both of these via structures are used as interconnections in

active devices. Via-first vias are formed on the front side of the wafer, where the active devices reside. Via-last vias are introduced into the wafer from the back side after all of the front-end processing on the wafer is completed. In current practice, last vias make contact to the underside of the bond pad region. First vias are commonly filled with metal such as copper, and last vias have a thin plate of metal conforming the walls of the via. First vias may or may not be formed in the bond pad area depending on via diameter.

There are several variations in the via-first and -last mix. When vias for interposers are added, the variations list grows a little longer. The various TSV options are driven by cost and size. Performance, while a consideration, does seem to take a backseat in most decisions.

PCB via options

To describe the TSV options it helps to review via options used with PCBs (**Figure 1**). PCB vias have evolved over the years to meet the need for greater circuit density. The least dense PCB via is the simple punched hole via. It generally has no plated metal inside, and is primarily used for very low cost consumer products. The most

common vias are formed using mechanical drills and metal is plated in the barrels. Costs for mechanically drilled vias are reduced by stacking and drilling several boards simultaneously. However, as the need for smaller via diameters arises, the number of boards in the stack reduces and costs increase.

The smallest PCB via, called a microvia, is formed using a laser. These are formed in single, not stacked boards. Since the lasers create a significantly rough barrel wall surface, microvias are generally full plated with copper metal.

TSV Variations

Silicon's crystal properties make it a very compatible material for machining using etching processes. There are two etching processes common to silicon—wet and dry. Potassium Hydroxide (KOH) is a popular chemical used for anisotropic wet etching. Silicon reacts very quickly to KOH and the etching pattern tends to follow crystal orientation (anisotropic) resulting in large area vias on the side of the via exposed to the etch. As shown in **Figure 2**, the vias have slanted walls.

Dry etching is accomplished by ionizing a gas chemical that reacts with silicon. One such chemical is sulfur hexafluoride (SF₆). When SF₆ is ionized using high temperature or RF energy, the fluorine ions readily react with any exposed silicon to remove the silicon from the wafer.

Deep vias with vertical walls can be formed by using a variation on the plasma etch, a method called the Bosch process (also known as deep reactive ion etching (DRIE)). This method, invented by Robert Bosch, adds another chemistry which acts to deposit a polymer on the walls after a short etch cycle. This polymer acts to protect the walls from further horizontal etching allowing only the exposed vertical surfaces of the via to continue to react with the plasma.

Currently aspect ratios (via depth to via diameter) of 3 or 5 to 1 are economically reasonable. Higher aspect ratios (HAR) become very costly due to the extra chemistry

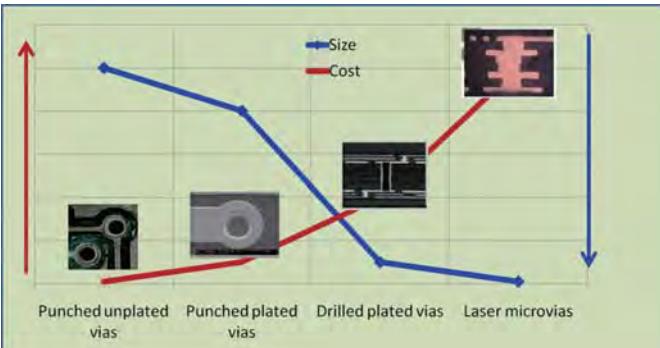


Figure 1. Graph of relative cost and via diameter size of common printed circuit vias. Source: PPM Associates

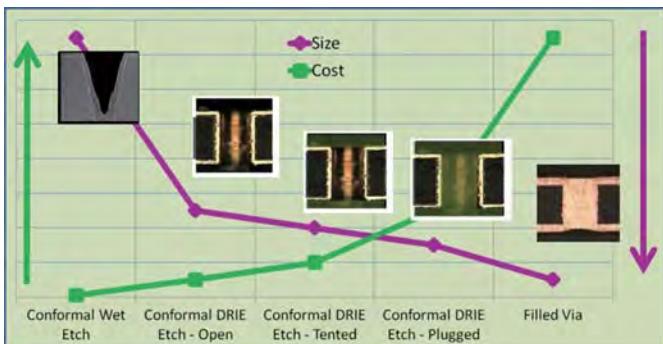


Figure 2. Graph of relative cost and via diameter size of some of the various through silicon vias. Source: PPM Associates

costs and longer equipment usage. Some users try to achieve HAR by reducing the wafer thickness. However, once silicon wafers are thinned below approximately 250µm, they become very flexible and fragile. The thin wafers may be bonded to a thicker handle wafer, but this adds to the cost and handling complexity.

Once etched, the via walls need to be insulated before adding metal. The choice of insulation material is determined as much by the via size and allowable cost as it is by the required performance. Thermal oxide is one of the less expensive insulation materials. However, it needs to be relatively thick to provide adequate protection from voltage breakdown and current leakage between the via metal and the silicon substrate. Unlike the non-conductive property of the fiberglass epoxy in PCBs, silicon is conductive. A polymer insulator, such as polyimide, provides better electrical performance but at higher cost.

To Fill or Not to Fill

Filling the vias with plated conductive metal is possibly the most expensive process for TSVs. Completely plating the vias full can take hours and days. Highly controlled processing with expensive equipment is required to avoid voids and seams in the metal.

Once a via is fully plated it may still need additional processing, such as chemical mechanical polishing (CMP) and thermal annealing. The CMP step flattens the front and back of the via. The anneal is used to change the crystal structure of the plated copper to prevent it from “pumping” or swelling in the via.

Several TSV adaptations are using other methods to avoid the plating. One adaptation uses unfilled vias, which results in an inexpensive via but it can present manufacturing challenges if the wafer needs to be held by any vacuum fixtures. As a twist on this the unfilled vias may be tented with a polymer, such

or chemistry in the barrel of the via a polymer may be injected before tenting.

Can there be too many vias?

The cost to form vias in silicon, unlike conventional PCBs, is not a function of the number of vias. The etching, insulating, and plating of the vias are mass wafer level processes. Therefore it costs as much to introduce one via as it does to form thousands. However, a high number, and in particular if they are arranged in tight proximity to each other, can cause severe yield limits when handling and singulating the die from the wafer.

Significant Cost Advantages of TSVs

A select grouping of products realizes significant advantages from the use of TSVs in 2.5D (die mounted on interposers) and 3D (die stacked on die) technologies. Given the early stage of these new approaches, this is to be expected. Stacking memory die in a 3D assembly and heterogeneous die mounted

Learn More at www.ser.co.jp

GHz Signal Probing Socket

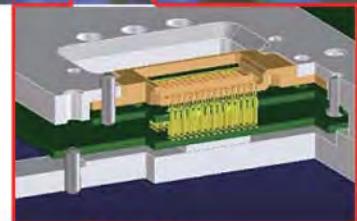
- DDR Signal Wave Analysis at 1.8Gbps or over.
- Best for wave analysis and evaluation on production board.
- For Logic analysis and PoP intermediate signal observation.
- Solder-less mount featured.

BEST SOLUTION

ELECTRONICS PARTS

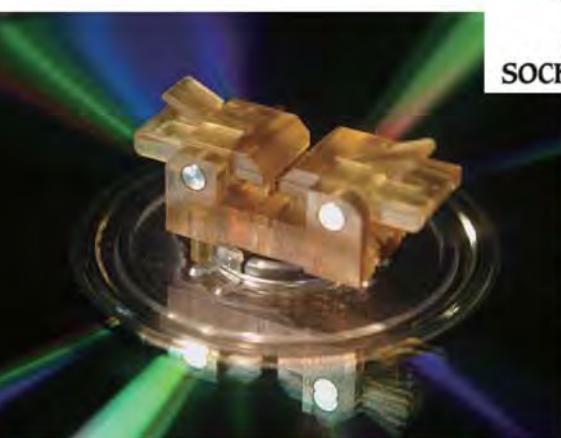


CUSTOMIZED
SOCKETS & CONNECTORS



Crystal Device Socket

- Manual and automatic test operations.
- GHz frequency performance.
- All package size variation.
- Wide operating temperature range
- GPS, SAW, TCXO, VCXO, OSC and etc.



For more information, Contact Us at +81-3-5796-0331 or ser@ser.co.jp

on 2.5D interposers offer the size, speed, and cost advantages needed to fuel the acceptance of these new approaches.

Applications for Interposers with TSVs

The advantages of using a 2.5D approach for heterogeneous products can be explained by examining a product, such as, the recently announced Virtex 7 by Xilinx. This product consists of 2M logic cells, 85Mbits of internal memory, 6.7 Tera-MACS DSP throughputs, and 2.8 Tb/s of serial bandwidth. Typically a producer of this type of product would rely on the most leading-edge semiconductor fabrication technology and create a single die incorporating each of the functions, albeit many being dissimilar and therefore difficult to make in a single die. The development costs and time-to-market from this development path have reached the point where this may no longer be the wisest choice.

According to Javier De la Cruz, Director of Manufacturing Technology at eSilicon, "The graph (**Figure 3**) shows

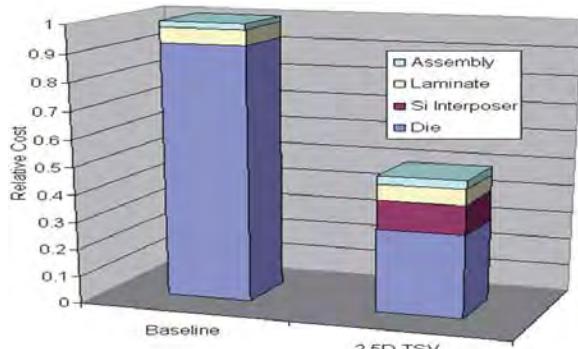


Figure 3. Estimated cost comparison of a large single die FPGA (the Baseline) vs. the same function using a 2.5D stacked die on silicon interposer assembly. Source: eSilicon

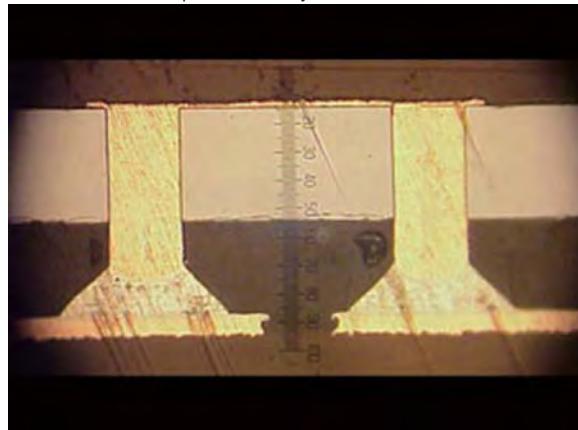


Figure 4. A copper filled pair of DRIE formed TSVs soldered onto a substrate. Source: ALLVIA, Inc.

the costs of various options considering tested and yielded silicon, the package laminate, and assembly. It shows the benefit of having taken a large piece of silicon and partitioning it into four smaller die. In the baseline (single chip) option, the silicon cost grossly dominates the cost of the device, followed by the cost of the package substrate and the assembly cost. The 2.5D option shows the incremental cost of the silicon interposer and a much lower cost of the four smaller, currently manufactured die. This is a strong case for the negative yield impact of using such a large die. It's estimated that the yielded cost of the 2.5D assembly is about half that of the current monolithic solution." Additionally, modeling of this device predicts a dramatic improvement in signal quality due to the reduced inductances using TSVs rather than long wire bonds.

Silicon PCBs - the big enabler

A significant development that enables the move to vertical assembly is silicon PCBs, aka interposers using TSVs. Forming multiple layers of wiring on silicon is a well understood technology. The TSVs provide the means of connecting the topside wires to the bottom wires without wire bonds. This addition opens up new uses of silicon as a very dense equivalent to the PCB. As stated earlier, TSVs are analogous to the plated through vias in PCBs, but the supporting substrate is silicon rather than reinforced fiberglass. Therefore, a silicon interposer is nothing more than a silicon PCB.

In current practice, TSV vias range from the "large" ($>100\mu\text{m}$) diameter backside wet etched and conformal plated vias to the very small

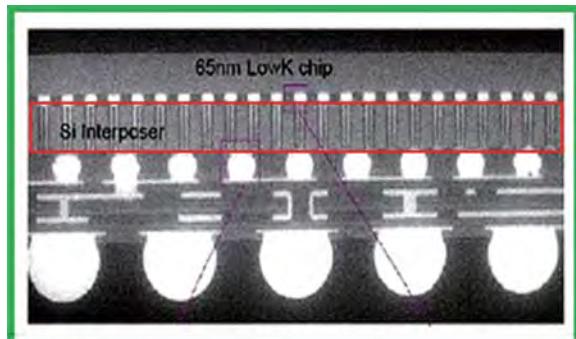


Figure 5. A 65nm IC die mounted on an interposer. The backside pads of the interposer are on a larger pitch. Source: Nokia

($<20\mu\text{m}$) diameter DRIE, fully plated vias. Cross sectional views of these are shown in **Figure 4**. The most common is a 50-70 μm diameter in a 250 to 300 μm thick wafer.

Interposers provide many benefits

The fundamental purpose of a silicon interposer has been as an enabler to connect small and finely-placed IC pads on larger and wider pitched package substrate pads. One example is the transposing of 35 μm^2 IC pads on a 60 μm pitch to the minimum capable pads of a package substrate, namely 120 μm^2 pads on a 250 μm pitch. This is illustrated in **Figure 5**.

An interposer is expected to become as essential as underfill epoxy for the reliable assembly of large, very stress-sensitive die. Underfill epoxy became a standard assembly element when it was recognized for its ability to constrain the CTE of the package substrate to something approaching the very low CTE of silicon. In a similar vein, an interposer coupled with underfill will provide stress relief between the package substrate and the increasingly sensitive lower lithography node ICs ($< 60\text{nm}$ nodes).

Summary

Silicon interposers with TSVs are the gateway to the many benefits of 3D product assembly. For a growing variety of products, the multi-die assembly approach provides significant cost, performance and size improvements over the single large die approach. 

Acknowledgements

The author would like to thank Dr. Sergey Savastiouk, CEO ALLVIA and Javier DelaCruz, Packaging Director, eSilicon, for contributing to this article.

PLASTRONICS

The H-Pin® Family is About to Get Bigger

Smaller

The H-Pin® gives you all the mechanical and electrical performance of a spring probe, but at a fraction of the cost.

The H-Pin® is made using a fully automated, high volume manufacturing process which eliminates the delivery headache you face with other pins.

Call us to today to learn more about the newest H-Pin®.



H-Pin®

www.H-Pins.com

1-800-582-5822

New Test Handler Generations for New Challenges: Finding the Best Platform Strategy

By Barbara Loferer [Multitest]

Barbara Loferer (MBA), Marketing Manager at Multitest, is responsible for all Multitest product lines including test handlers, test contactors, test interface boards and burn-in boards. After her degree at the European University, Munich, she worked in the finance industry, and the paper commodity industry before she joined Multitest in 2000.

Historically, test handlers have been categorized by their method of internal device transportation, e.g., gravity force or pick-and-place mechanisms. The transportation method was closely related to the media in which the packages were delivered, such as tubes or metal magazines for gravity, and trays for pick-and-place. With the requirement for higher parallelism, testing ICs in arrays (e.g., strip test, test-in-tray) also may be considered a separate category in contrast with traditional singulated test.

Gravity test handlers offered a list of advantages that were unachievable with pick-and-place handlers. For a long time, pick-and-place handlers were chosen only for packages that were unmanageable with a gravity handler, such as QFPs. Gravity handlers were considered to be less complex, cheaper, and faster. However, with the new requirements (e.g., for multi-site capabilities), in addition to an innovative generation of pick-and-place handlers, strip test handlers, and the new concept of test-in-trays or test-in-carriers, this situation needs to be reviewed.

What is the best platform strategy for volume production, given today's test handler alternatives? Aspects that must be considered include capital investment, package range, cost and time for package style conversion, speed, maximum throughput, reliability, ease of operation, external package transportation media, and overall cost of test.

Complexity and Initial Investment

Over the past few years, the requirements for multi-site (parallel) test have increased. The crucial issue is how much the complexity of the handler

configurations and the general equipment requirements have grown to be ready for new technologies.

Years ago, the complexity for gravity single-site configurations was low and so was capital investment. Pick-and-place was more complex and, therefore, more expensive. Strip tests forced the change to the back-end process and the abandonment of final test as the last process step because singulation has to be done after the strip test. The new concept of test-in-trays overcomes this, but requires additional equipment loading and unloading into/from the trays (Figure 1).

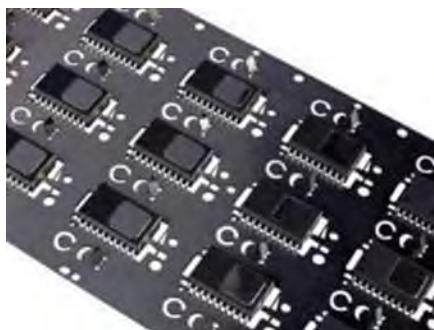


Figure 1. Test in carrier allows for parallel test after singulation

Process Requirements and Opportunities

Strip tests require a change in the traditional back-end process flow. Packages stay in their lead frames while being tested. Sawing and singulation are performed after final test. For quality-sensitive applications such as automotive, this is an issue. The test-in-tray concept overcomes this. Additional advantages can be leveraged by using the loaded trays not only for final test, but also for burn-in or by using the loaded trays for all three test cycles at tri-temp test.

Test Floor Situation and Lots

Although gravity handlers require less space on the test floor, lot sizes and the

number of package style changes still must be taken into account. Large lots (i.e., for mass products) absorb the cost of conversion kits better and avoid test cell downtimes due to package style conversions. The change kits for gravity handlers are substantially more expensive (if package style conversion is even possible) and the test cell downtime is in the range of hours, whereas pick-and-place handlers offer simple conversion kits and conversions times of only several minutes. This new test-in-tray concept supports the idea of a "kit-less" handler (i.e., the carriers/trays are standardized and will not change with the package dimensions). The drawback is that the additional capital investment for package-to-carrier loading/unloading will pay off only for real mass production.

Speed: Maximum Throughput

The task for test handlers is to bring as many devices to the contact site as the tester can process to avoid tester idle time. From the tester's perspective, it is either testing or waiting for new devices. From the handler's viewpoint, there are several parallel processes. While one set of packages keeps the contact site busy, the next set of untested packages must be received from the loading station and brought to test temperature. The tested packages from the previous set then need to be sorted and transported from the contact site to the respective unloading station. Here, strip test and test-in-trays cannot be beaten for all applications with limited electrical test complexity, such as MEMS test.

For singulated test handling, depending on the application and its typical test time, either the index time for the device under test (DUT) exchange or the time for the transportation and sorting processes becomes more critical.

Applications with long test times

In the case of long test times, there is enough time for the handler's internal

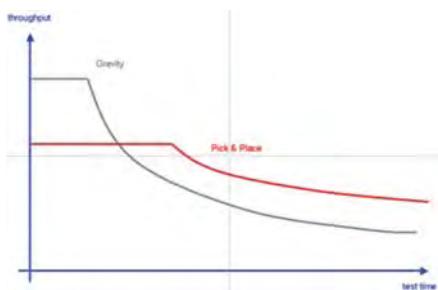


Figure 2. Comparison of test times between gravity and pick-and-place handler

infrastructure to transport the packages. The most critical issue is the time needed to replace the tested devices with new, untested ones at the contact site. Here, pick-and-place has an advantage, especially for multi-site testing; the packages at all contact sites can be replaced simultaneously. Gravity has clear limitations that lead to significantly longer index times (**Figure 2**). Using gravity force only, the speed for the DUT exchange is given and cannot get faster. Additionally, because of the design, multi-site gravity handlers often are unable to completely exchange all DUTs simultaneously, but need two (or



Figure 3. Gravity feed handlers like this offer advantages over pick-and-place for ICs requiring short test times

more) iterations.

Applications with short test times

For ICs that require short test times, the handler's internal transportation speed is the pivotal feature. Even compared to the latest pick-and-place generation,



Figure 4. Pick-and-place handlers like this one support easy conversion to other packages

gravity handlers have clear advantages (**Figure 3**). Today's state-of-the-art pick-and-place mechanisms that are based on the actual handling of each single package cannot beat the gravity handling of multiple packages in tubes and tracks (**Figure 4**).

Reliability — Jam Rates

Of course, no package jam is possible if the ICs are handled in their lead frame or in a carrier. Here, both handling methods are unprecedented. Comparing

Life test of
ultra high power
dissipative devices

STS Launches ITC360™

A Revolutionary Technology that breaks through the barriers of conventional burn-in testing for SIPs, SOCs, LEDs, processors and other high power dissipative systems.

Silicon Turnkey Solutions (STS), a solutions enabling company introduces ITC360™, an innovative product designed to overcome temperature regulation of high power dissipative devices. This unique product addresses the current industry bottleneck experienced during burn-in of microprocessors, SOCs, SIPs and high power LEDs thus enabling precision, accuracy and flexibility.

ITC360™ Features:

- Ultra Precision Thermal Regulation
- High Reliability Thermal Management to 250 watts/DUT
- Accuracy
- Flexibility of Exercise, Diagnostics and Test
- Intelligence of Exercise, Device or System Level
- Intelligence of Data Collection
- Value Solution
- Chamberless
- Socketless: Option Available



For detailed information, please contact:
T: (408) 432 1790 | F: (408) 432 7350
www.sts-usa.com | sales@sts-usa.com

STS
Silicon Turnkey Solutions

the two concepts of motion induced by gravity or forced mechanism, jams at gravity transportation are caused by unforeseen random events, e.g., because two ICs got hooked-up. On the other hand, jams at pick-and-place transportation result from malfunctions or bad performance of the pick-and-place mechanisms. Here, optimization of the modules or even reducing their number offers the chance for substantial performance improvements

even for higher parallel testing.

Package Types

For many years, pick-and-place handlers were deployed only for QFPs and BGAs. Currently, this categorization is blurring. Now, pick-and-place handlers are used for QFNs, DFNs and even SOs. Today's pick-and-place handlers can handle almost every package style. In other words, the package type is of minor



Figure 5. Strip handlers offer a robust handling process for even the smallest devices

importance for handler type selection and will lose priority to the decision criteria previously described. One of the major criterion for selecting strip handling is the robust handling process for even the smallest devices (e.g. WLCSPs (Figure 5)). Test-in-carrier expands this to previously singulated packages, and therefore allows robust test handling of the smallest highly quality-sensitive devices.

Conclusion

What is the best test handling decision? One issue is clear: For very short test times, gravity test handlers remain the optimum solution. For all other applications, however, it depends on the test floor situation. Besides the number of required package style conversions and lot sizes, the external transportation media of the ICs often determines the choice of the test handler. Whether the additional cost of changing to or converting into trays will be offset by the advantages of pick-and-place is a straightforward calculation. The same is true for a process change from traditional singulated test handling to strip test or test-in-carriers. Today's test application landscape is diverse and requires innovative solutions for either method of test handling. Often, these solutions will overlap with only some differentiation, but this is the base for an optimized test handler platform decision.

Acknowledgments

The author would like to thank the following individuals for contributing to this article: Guenther Jeserer, Business Unit Manager Gravity and Pick-and-Place; Andreas Nagy, Business Unit Manager Engineering Driven Business; and Bernhard Lorenz, VP Engineering Group.

Az TECH DIRECT, LLC

Electronics Resource Network

ELECTRONICS INDUSTRY CONSULTING

WIRELESS

LED OPTO

MEDICAL

CONSUMER

MIL AERO

SOLAR

AzTD

www.AzTechDirect.com

Contact: Sales@AzTechDirect.com or (480) 215-2654



INTERNATIONAL DIRECTORY OF AUTOMATED ENCAPSULATION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	NEEDLE DISPENSING	JET DISPENSING	THERMOSET MOLDING
Company Street Address City, State, Country Telephone Website Note: CM = Contact Manufacturer	Equipment Type Batch, Inline Valve / Pump Type AP - Auger Pump PD - Positive Displace TP - Time and Pressure Materials A - Adhesive, C - Coating D - Dam, E - Encapsulant F - Flux, P - Potting SP - Solder Paste U - Underfill	Equipment Type Batch, Inline Materials A - Adhesive, C - Coating E - Encapsulant, F - Flux S - Solder, U - Underfill Specifications DD - Dot Diameter SV - Shot Volume	Equipment Type Automatic, Manual Technology C - Compression F - Film Assist T - Transfer, V - Vacuum Applications LED - Light Emitting Diodes LP - Leadframe Packages RR - Reel to Reel SP - Substrate Packages WLP - Wafer Level Packages
Advanced Systems Automation Ltd. Block 25 Kallang Ave #02-01 Kallang Basin Industrial Estate Singapore 339416 Tel: +65-6309-5500 www.asa.com.sg			Automatic T, V LP, SP
Apic Yamada Corporation 90 Kamitokuma, Chikuma-shi Nagano-ken 389-0898, Japan Tel: +81-26-275-2111 www.apicyamada.co.jp			Automatic, Manual C, F, T, V LED, LP, SP, WLP
ASM Pacific Technology Ltd. 2 Yishun Avenue 7 Singapore 768924 Tel: +65-6752-6311 www.asmpacific.com	Batch, Inline AP, PD, TP A, C, D, E, F, P, SP, U	Batch, Inline Materials: F, U Specs: CM	Automatic, Manual C, F, T, V LED, LP, RR, SP, WLP
Asymtek (Division of Nordson) 2747 Loker Avenue West Carlsbad, CA 92010 Tel: +1-760-431-1919 www.asymtek.com	Batch, Inline AP, PD, TP, Other A, C, D, E, F, P, SP, U	Inline A, C, E, F, U DD > 200 um; SV > 1.0 nl	
Boschman Technologies B.V. Stenograaf 3 6921 EX DUIVEN, The Netherlands Tel: +31-26-319-4900 www.boschman.nl			Automatic, Manual F, T, V LED, LP, RR, SP, WLP
Creative Automation Company 11641 Pendleton Street Sun Valley, CA 91352 Tel: +1-818-767-6220 www.creativedispensing.com	Batch, Inline PD A, C, D, E, F, P, SP, U		
DIAS Automation (HK) Ltd. Unit A7-A8, 3/F, Merit Industrial Bldg., 94 Tokwawan Rd. Kowloon, Hong Kong Tel: +852-2333-6298 www.diasautomation.com	Batch AP, TP, Other C, D, E, P, U	Batch C, E, U Specs: CM	
Epoxy & Equipment Technology Pte Ltd No. 20 Bukit Batok Crescent, #03-16 Enterprise Centre Singapore 658080 Tel: +65-6899-3839 www.eet.com.sg	Batch, Inline AP, PD, TP, Other A, C, D, E, P, SP, U	Batch, Inline A, E, F, U DD - CM; SV > 2.0 nl	
Fico B.V. (Division of BE Semiconductor Industries B.V.) Ratio 6 6921 RW Duiven, The Netherlands Tel: +31-26-319-6100 www.fico.nl			Automatic, Manual F, T, V LED, LP, RR, SP

INTERNATIONAL DIRECTORY OF AUTOMATED ENCAPSULATION SYSTEMS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	NEEDLE DISPENSING	JET DISPENSING	THERMOSET MOLDING
Company Street Address City, State, Country Telephone Website Note: CM = Contact Manufacturer	Equipment Type Batch, Inline Valve / Pump Type AP - Auger Pump PD - Positive Displace TP - Time and Pressure Materials A - Adhesive, C - Coating D - Dam, E - Encapsulant F - Flux, P - Potting SP - Solder Paste U - Underfill	Equipment Type Batch, Inline Materials A - Adhesive, C - Coating E - Encapsulant, F - Flux S - Solder, U - Underfill Specifications DD - Dot Diameter SV - Shot Volume	Equipment Type Automatic, Manual Technology C - Compression F - Film Assist T - Transfer, V - Vacuum Applications LED - Light Emitting Diodes LP - Leadframe Packages RR - Reel to Reel SP - Substrate Packages WLP - Wafer Level Packages
GPD Global Precision Dispensing Systems GPD Global 611 Hollingsworth Street Grand Junction, CO 81505 Tel: +1-970-245-0408 www.gpd-global.com	Batch, Inline AP, PD, TP, Other A, C, D, E, F, P, SP, U		
HANMI Semiconductor Hanmi Semiconductor Co., Ltd. 532-2 Gajwa-Dong, Seo-Gu Incheon, South Korea Tel: +82-32-571-9100 www.hanmisemi.com			Automatic, Manual T LED, LP, RR, SP
Musashi Engineering, Inc. 8-7-4, Shimorenjaku, Mitaka-shi Tokyo 181-0013, Japan Tel: +81-422-76-7111 www.musashi-engineering.co.jp	Batch TP, CM A, C, D, E, F, P, SP, U	Batch, Inline A, C, E, F, U Specs: CM	
Newport Experience Solutions Newport Corp. (Advanced Packaging Solutions) 101 Billerica Avenue North Billerica, MA 01862 Tel: +1-978-667-9449 www.newport.com	Batch, Inline PD, Other A, C, D, E, F, P, SP, U		
Panasonic Factory Solutions Company of America 5201 Tollview Drive, Panazip 13 Rolling Meadows, IL 60008 Tel: +1-847-637-9600 www.panasonicfa.com	Batch, Inline AP A		
Speedline Technologies Inc. 16 Forge Park Franklin, MA 02038 Tel: +1-508-520-0083 www.speedlinetech.com	Batch, Inline AP, PD, Streaming A, C, D, E, F, P, SP, U	Batch C, E, U Specs: CM	
TOWA Corporation 5 Kamichoshi-cho, Kamitoba, Minami-ku Kyoto 601-8105, Japan Tel: +81-75-692-0250 www.towajapan.co.jp		Batch, Inline A, E, F, U DD - CM; SV > 2.0 nl	Automatic, Manual C, F, T, V LED, LP, SP, WLP

Metrology and Defect Inspection Critical for Bonded Wafer Yield

By Greg G. Baker [Olympus Integrated Technologies America, Inc.]

Three dimensional stacked integrated circuits (3DS-ICs) will provide many technological advantages in faster performance, lower power consumption, and smaller form factors. As continued shrinks in two dimensional chips become more difficult and expensive, vertically stacking the 2D chips allows more capability in the same or smaller form factor.

3DS-IC manufacturing processes utilize through silicon via (TSV) technology for 3D interconnect in wafer-to-wafer (W2W) bonding. Making a high-yield W2W bond has many prerequisites: exactly matched die patterns on both wafers (die-step and pattern offset from the center of the wafer), flat bonding surfaces, contamination-free bonding surfaces, and highly accurate W2W alignment prior to bonding. Contamination can cause voids, delamination, and other issues. Pattern offsets or overlay misalignment during bonding can cause failed or compromised electrical connections.

The 3DS-IC processes require monitoring, measuring, and controlling as many of these factors as possible before, during, and after the bonding process. Prior to bonding there are a number of metrology solutions available for single wafers, but post-bonding metrology presents a problem because device interfaces are buried inside the bonded wafer pair, and silicon is non-transparent to most metrology methods. A non-destructive, through-silicon metrology technique is required for monitoring a variety of post-bond parameters including:

- post-bond overlay alignment measurement
- bonding interface thickness variation
- bonding interface quality including pre- and post- bond defect inspection

There are several possible technologies available for through-silicon metrology including scanning electron microscopy (SEM), scanning acoustic microscopy (SAM), X-ray inspection, and infrared (IR) microscopy. However there are some

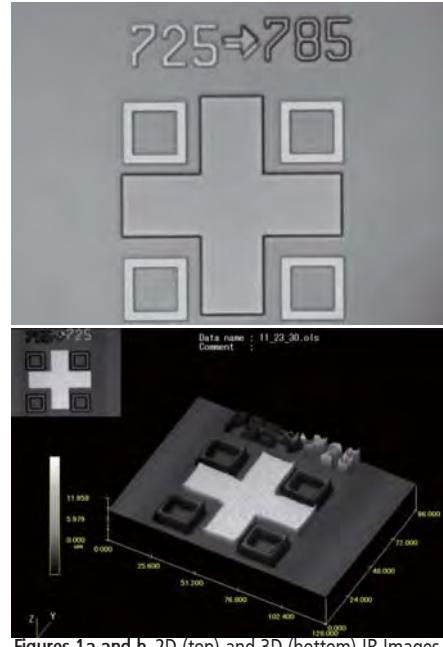
limitations. SEM cannot image below the wafer surface and therefore is limited to samples that can be cleaved for cross sectioning or delayed to expose the structures of interest. This is a very time consuming process. SAM, though non-destructive, uses sound waves and requires immersion in water for transmission of the high-frequency acoustic energy to and from the wafer. Immersion in water introduces the possibility of contamination, even with post-immersion cleaning. Additional processing to seal the wafer at the edge to prevent water incursion between the wafers adds steps and cost to the process. X-ray radiation will offer high transmissivity through silicon, but has additional costs and security measures associated with the additional shielding required for safety.

IR Microscopy for Metrology

Microscopy has long been used for inspection and metrology, but conventional visible light methods fail as silicon is non-transparent to visible light. Near infrared wavelengths do transmit through silicon and IR microscopy also offers a non-destructive solution for through-silicon metrology of the bonded interface. Confocal IR laser scanning microscopy offers the additional benefit of constructing 3D images, allowing measurement of feature heights and layer thicknesses of the bonded interface between wafers (Figure 1).

Overlay Metrology using IR Microscopy

During the bonding process, wafers are aligned to each other using fiducial marks on the top and bottom wafers. In Figure 1, the 2D image shows top and bottom wafer fiducial marks on a SEMATECH bonded wafer pair.* The bottom wafer (725 and boxes) and the top wafer (785 and cross) are aligned relative to each other prior to bonding. A perfect



Figures 1a and b. 2D (top) and 3D (bottom) IR Images of Bonded Wafer Alignment Fiducials



Figures 2. Post-bond overlay measurement using IR microscopy shows an alignment offset of 0.5053 μ m in X and 2.7300 μ m in Y

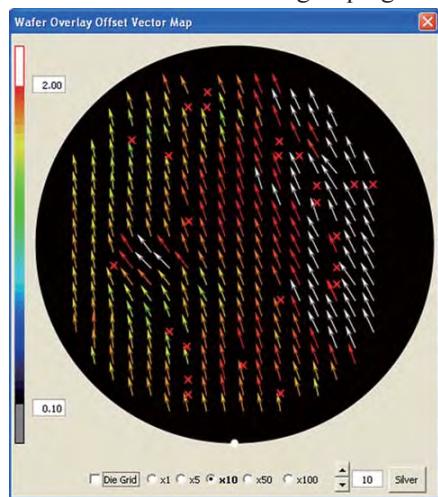
alignment would center the cross in between all four boxes.

Accurate alignment is required for good electrical yield of bonded wafers, but a number of factors during the bonding process can influence the results of the wafer bond alignment (wafer slippage, heat, and pressure effects). Monitoring the immediate post-bond overlay alignment result is critical to manufacturing; if the wafers are not aligning well the yield will be impacted. Alignment issues must be detected early and resolved quickly or it will be very costly. The post-bond overlay

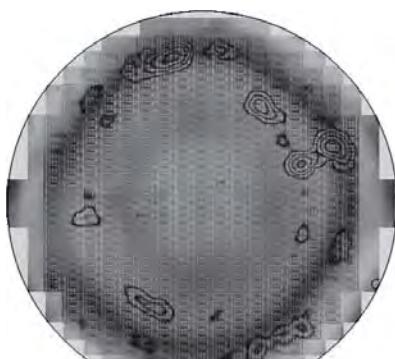
alignment results can be measured using IR microscopy. **Figure 2** shows a post-bond overlay alignment measurement using IR microscopy.

Post-bond overlay results will vary across each wafer. Automated overlay measurement of a broad sampling or all alignment points on a wafer can quickly characterize the overlay results as well as provide indications of bond quality problems. A recipe was set up to measure alignment points at each die of the SEMATECH bonded wafer pair. The data was tabulated in a spreadsheet for further review and analysis, and the overlay offset for each measurement point was plotted as a vector on a wafer map as shown in **Figure 3**, giving a quick indication of the wafer bonding result. Each vector gives the overlay offset direction and magnitude for each overlay measurement. A color scale is applied (left side) as an additional indicator of offset size: dark blue indicates an offset in the $0.2\mu\text{m}$ range, red indicates a $2\mu\text{m}$ offset and white indicates an offset $>2\mu\text{m}$. Results for this bonded wafer pair shows that virtually all of the overlay offsets are $>1\mu\text{m}$, with many $>2\mu\text{m}$. If these wafers were using $1\mu\text{m}$ via structures, this bonded pair would likely have low yield due to electrical opens. By correlating electrical yield with overlay offset, IR microscopy can be used as an early indicator of electrical yield in bonded wafers.¹

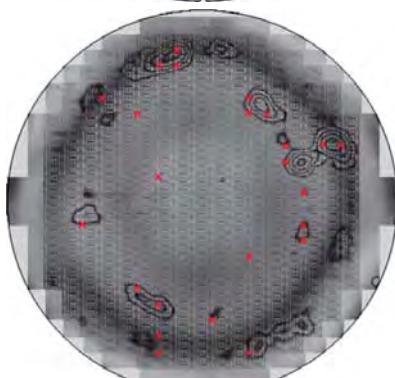
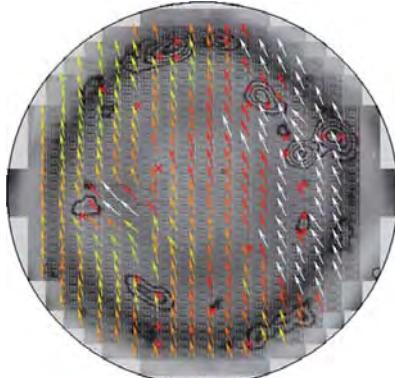
Note that the vector map contains some missing alignment points; these are failed measurements and are indicated in **Figure 3** with a red 'x'. These failed measurements show some grouping and



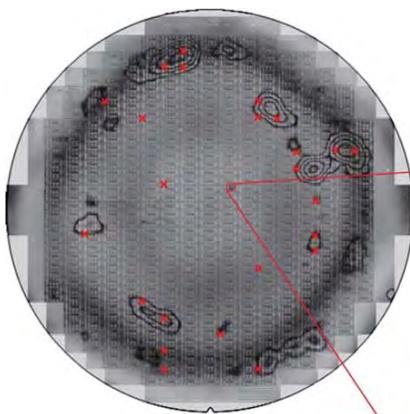
Figures 3. Post-bond overlay offset result as vector map



Figures 4. IR scanned and stitched image of the bonded wafer pair interface



Figures 5a and b. Overlay offset vector map superimposed on IR wafer scan



Figures 6. Stitched image zoom function shows higher resolution detail

may be indicative of some sort of anomaly in the bonded interface.

Bonded Interface Analysis

Using the IR microscope imaging capability, a recipe can be set up to automatically scan the wafer at low magnification. Software will analyze and stitch the images together into a single wafer image as shown in **Figure 4**. The IR wafer image shows some voids centered on defects and many of the characteristic topographical features that can be associated with bonding interface defects.

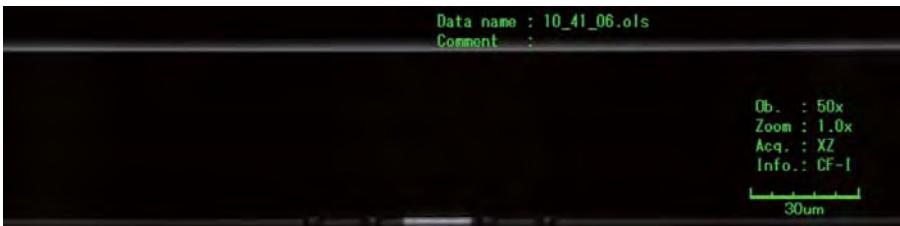
Superimposing the overlay vector map on the scanned wafer image (**Figure 5**), reveals the correlation of many failed overlay measurement points to bonded interface anomalies.

The stitched image is stored and available for further review and analysis. Because the wafer scan was done using an IR microscope, the stitched image can be viewed and zoomed for more detail. For example, the circled smaller void in the scanned wafer image shows a contamination induced void defect (**Figure 6**). In addition, any site can be revisited and the image reviewed or rescanned and imaged using the IR microscope with objective magnifications up to 90X and $0.14\mu\text{m}$ pixel resolution.

Thickness Metrology

Thickness metrology is more challenging and usually requires a technique such as SEM or focused ion beam (FIB) cross sectioning to obtain data. These methods come with high precision, but they are destructive and time consuming as the sample is usually sent to a lab for processing.

A microscope with confocal capability allows thin optical sectioning in the Z-direction, and is therefore very useful in constructing 3D images. An IR microscope with confocal capability can provide 3D



Figures 7. XZ profile of top wafer and overlaid fiducial marks at bonded pair interface



Figures 8. Successful (left) and unsuccessful (right) overlay measurement points

images of the bonded wafer interface and structures as was shown in **Figure 1**. The 3D reconstructions can be used to create sections in the XZ plane to provide a measurable profile of an imaged structure or feature. **Figure 7** shows an XZ section of the fiducial marks at the bonded interface of the SEMATECH wafer pair at 50x magnification. The range of measurement in the Z plane was set to a large enough distance to cover the entire top wafer and bonded interface, and the step size between measurements was set appropriately to realize the desired resolution.

The IR microscope confocal functionality can be utilized to further investigate some of the anomalies indicated by the failed measurement sites on the wafer overlay vector map. These failed measurements could indicate voids or thickness variations at the bonded interface. Two adjacent measurement sites were chosen for an XZ profile. **Figure 8** (stitched image IR wafer scan) shows the two alignment sites: the left site is the

successful measurement site; the right site is the failed measurement site. **Figure 9** shows the results of the XZ profile image of each fiducial mark and there is a clear difference between the two; the failed measurement site shows that the top wafer fiducial mark is raised above the bottom wafer. In other words, the bond interface is thicker at this point by 2.7μm; the fiducials have some additional separation. This difference in height between the fiducial marks is indicated not only by the failed measurement, but by the dark rings on the IR scanned image, created by the interference of diffracted light at the wafer interface.

Variations in height between sections of the bonded wafers, as can be seen between the top and bottom wafer fiducial marks, cause an improper autofocus and subsequently a measurement failure. There are software solutions to allow for overlay alignment measurement of fiducials on two different Z planes. In these cases, the overlay measurement will

be successful and the difference in focal plane height can be recorded as indicators of different bond interface thicknesses.

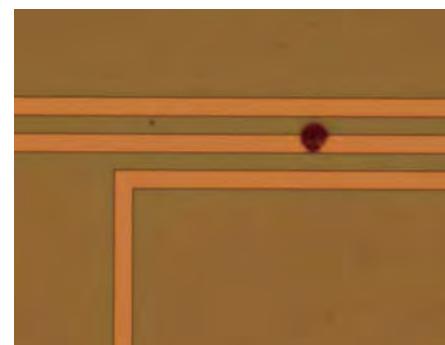
Using the confocal capability of the microscope to take XZ measurements at various points on the wafer will provide information on the bond interface thickness uniformity.

Defect Metrology

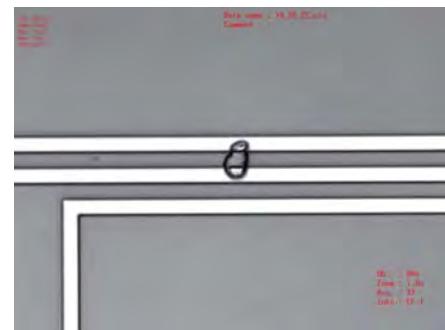
Contamination and other pre-bond defects can cause issues with the bonding process. IR microscopy allows review of pre-bond surface defects at the bonded interface after bonding. However, there are limitations as IR cannot transmit through some pattern materials. If the defect falls below a non-transparent pattern feature after bonding, it will not be visible to IR defect review.

Two examples of pre-bond defects causing a potential problem after bonding are shown in the contamination induced void (**Figure 6**) and the post-bonding short of two lines in **Figure 10**. **Figure 10** shows a pre-bond particle defect before bonding in visible light, sitting on one line but not causing a short. The post-bond IR image on the right shows the same defect after bonding — the bonding process has compressed and enlarged the defect to short two lines.

In order to review known pre-bond defects after bonding, it's necessary to be



Figures 9a. XZ profile of fiducials at a successful overlay measurement site



Figures 9b. XZ profile of an unsuccessful overlay measurement site, showing separation of top and bottom wafer fiducials

Figures 10. XZ profile of an unsuccessful overlay measurement site, showing separation of top and bottom wafer fiducials

able to read pre-bonded wafer defect files of both the top and bottom wafers. The top wafer defect file coordinate system must be flipped and combined with the bottom wafer defect file (**Figure 11**); then it's possible to navigate to pre-bond defect sites from either wafer and analyze the effects of the bonding process on the defects. Any new defects found can be imaged using IR microscopy at various magnifications and the new defect location and image information can be added to the combined defect file. Larger defects, such as voids, could optionally be rescanned at various magnifications using the stitching algorithms.

Conclusion

Technology has come a long way to accommodate Moore's law and the continued demand for miniaturization. 3DS-ICs using TSV technology are destined to help continue this trend not by shrinking, but by stacking vertically. Through-silicon metrology and defect inspection / review methodologies are

required to help move 3DS-IC processes toward high volume manufacturing.

Presently, there are three areas of metrology methods that can aid in ensuring that the wafers are bonded correctly with vias properly aligned and connected. These methods are

- post-bond overlay alignment measurement
- pre- and post-bond defect inspection (voids, delamination, contamination, etc.)
- bonding interface feature heights, interface and substrate thickness variations

Traditionally these types of metrologies have been done on separate tools: IR metrology tools, SAM, SEM, X-ray. The costs associated with moving wafers through multiple pieces of equipment in terms of extra processing, time consumption, and added handling risks may outweigh the cost of the equipment itself. The metrology tasks discussed herein can all be achieved in a single SECS/GEM-compliant tool

using confocal IR laser scanning microscopy. ☺

References

1. Andrew C. Rudack, Pratibha Singh, J. Christopher Taylor, Vadim Mashevsky, "IR Microscopy as an Early Yield Indicator in Bonded Wafer Pairs used for 3D Integration", Proc. SPIE Advanced Lithography Conference, Jan 2010, San Jose, CA, paper #7638-39

Acknowledgements

* The author would like to thank SEMATECH for the bonded wafer pairs used in this article; all wafer images are from the SEMATECH 403AZ bonded test wafers. The author would also like to recognize and thank the following individuals for their assistance in working with the bonded wafer pairs to acquire images and data in the preparation for this paper:

- Vadim Mashevsky, Olympus Integrated Technologies America, Inc.
- Afroz Khan, Wipro Technologies

INTRODUCING

A New Material Solution for Key Microprocessor Test Socket Applications

Piper Plastics' Kyron EPM-2204 Ceramic PEEK™ polymer, offers excellent dimensional stability and tolerance control across a broad range of temperature and humidity conditions, making it ideal for high performance test socket components. Competitive advantages include:

- Significantly lower moisture absorption
- Very tight tolerance machining
- Impact strength, stiffness and minimum creep levels
- Half the weight of ceramics
- Greater impact resistance and toughness compared to ceramics
- Excellent processability and wear performance
- Good dielectric properties for insulative applications
- Clean white or grey color

For more information on Piper Plastics'
Kyron EPM-2204 ceramic filled PEEK™ polymer
for microprocessor test sockets, please visit Piper Plastics
at SEMICON West 2011



For more information contact
Ryan Close at
rclose@piperplastics.com

(800) 526-2960
www.piperplastics.com
MACHINING • FABRICATION • DISTRIBUTION
PLASTICS & METALS

STATS ChipPAC's Secret Sauce

Chip Scale Review Staff



It's been a productive year so far for STATS ChipPAC. The company continues to roll out announcements about its progress in advanced packaging technologies including fine-pitch copper wire bonding, flip chip production, plant expansions, and progress on the next generation of embedded Wafer-Level BGA (eWLB). Year after year, this outsource semiconductor assembly and test service provider (OSAT) has been among the industry front runners. Chip Scale Review talked to Hal Lasky, Executive VP, Chief Sales Officer and President, STATS ChipPAC US, to learn more about the company's strategy to remain competitive.

CSR: STATS ChipPAC has consistently maintained a position as one of the top 4 OSATS. What do you think is the primary reason for that?

Lasky: Since our merger in 2004, we have transformed our company into an industry leader by focusing on the right technology, manufacturing capabilities, and customers. We have made some very important, strategic investments in advanced technology such as wafer level packaging (WLP), eWLB, flip chip, TSV and 3D packaging, which has allowed us to differentiate our company and our solutions. We embraced and implemented Lean Six Sigma throughout our company as our operational mindset, which has lead to the achievement of significant milestones year over year that reduce costs and increase efficiencies using breakthrough methodologies and process improvements. We've focused on penetrating growing market segments driven by the convergence seen in the communication, computing, and consumer markets and delivering value solutions

and differentiation to our customers. We have aligned ourselves with customers who are leaders in the industry and we have a number of key development activities going on with both our customers and leading foundries that support our customers.

CSR: In your opinion, what differentiates STATS ChipPAC from the other top 4 OSATS?

Lasky: As a company, STATS ChipPAC (**Figure 1**) does not try to be all things to all companies. Instead, we have chosen to take a more focused approach. We have developed key technologies such as WLP, flip chip and TSV that enable us to provide differentiating solutions with cost and performance benefits for our customers. STATS ChipPAC has made significant investments in research and development and is aggressively expanding our Intellectual Properties (IP) portfolio. Over the last six years, STATS ChipPAC's patent portfolio grew from 67 to 473 patents as of Q1 2011, which is a compound annual growth rate (CAGR) of 37%. Since 2005, 58% of our IP is in advanced technologies such as fan-out wafer-level package (FO-WLP), TSV, 2D/3D wafer level packaging, wafer bumping, IPD and SiP. This patent focus translates into our ability to provide solutions addressing increasingly challenging form factor, cost and performance requirements.

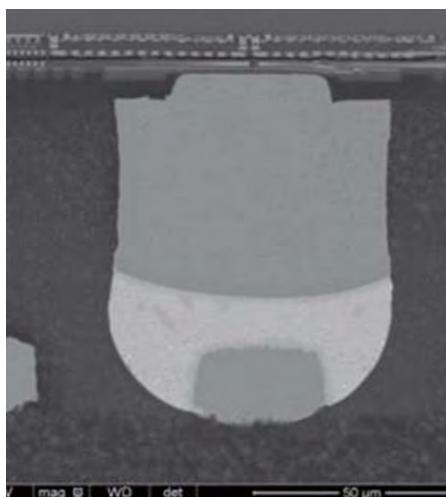
CSR: In 2011, there have been several significant announcements by STATS ChipPAC including expansions for WLP, fine pitch copper wire bonding, flip chip advancements, and mid-end processes for TSVs. What is the strategy around this approach?

Lasky: As the industry moves to finer and finer geometries, packaging technology is going through a significant change and becoming an important differentiator. STATS ChipPAC is driving integration through advanced technology such as FOWLP, TSV and flip chip technology; and we are combining advanced technologies into 3D and hybrid solutions that raise the bar on functional integration and increased performance for our

customers. The cost reduction roadmap is also a critical factor to customers and we are aggressively driving a cost paradigm shift in WLP, flip chip and copper wirebond interconnect to bring the performance and cost advantages to our customers. While growing our IP portfolio, we have introduced innovative packaging solutions



Figures 1. STATS ChipPAC Singapore factory



Figures 2. fcCuBE Copper Column



8th Annual

International Wafer-Level Packaging Conference & Tabletop Exhibition

October 3-6, 2011 Marriott Hotel, Santa Clara, CA

IWLPC Conference: October 3-6 IWLPC Exhibit: October 5-6

IWLPC EVENT SCHEDULE

- Oct. 3-4 Professional Tutorials
Oct. 5 Keynote Dinner
Oct. 5-6 Tabletop Exhibits, Panel Discussion,
Technical Presentations (three tracks),
Poster Sessions

CUTTING EDGE TOPICS INCLUDE

- WLCSP
- 3D WLP
- Flip-Chip Bumping
- Through-Silicon Vias
- Stacking Processes
- MOEMS Integration
- SIP/SOP vs. SOC
- MEMS Processes and Materials
- Quality, Reliability, and COO

"I started attending IWLPC a few years ago and found it to be a very valuable conference. Whether your focus is on MEMS, Advanced Packaging, or 3D Integration, IWLPC offers pertinent presentations and a qualified user community which will surely generate some lively discussions on current topics in these fields. Furthermore, the exhibit area always provides a venue for more detailed discussions or just catching up on some of your best contacts in the field. For these reasons and others, IWLPC will always be high on our list of trade shows to attend." — KEITH A. COOPER OF SET NORTH AMERICA



and Chip Scale

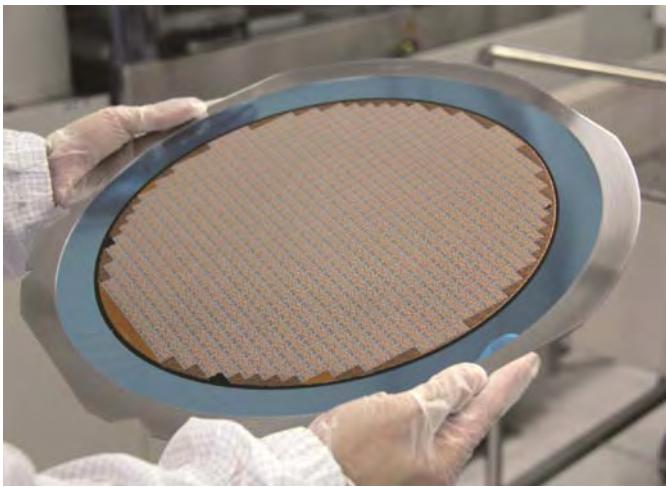
REVIEW
are proud to present
the event of the year for
buyers, specifiers and producers
of chip-scale and wafer-level
packaging equipment,
materials and services.

PLATINUM SPONSORS



GOLD SPONSORS



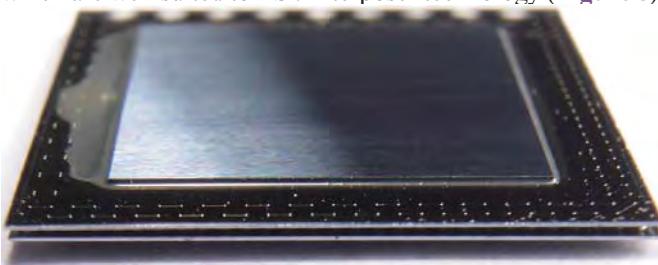


Figures 3. 300mm eWLB wafer manufactured in the Singapore facility

such as fcCuBE and eWLB (**Figures 2** and **3**) that provide solutions to our customers who are looking for increasing density and thin profile, all at a reduced cost over time.

CSR: *Many experts are calling silicon interposers the first step towards full 3D. Do you agree?*

Lasky: Yes, silicon interposers are an immediate and practical approach to die-level integration. TSV interposers provide flexibility for the integration of die from different technology nodes and deliver advantages in miniaturization, thermal performance and fine line/width spacing in a semiconductor package. Increasing bandwidth and finer lithography geometries drive a higher level of integration including more integrated passive device (IPD) (**Figure 4**) integration and cost optimization, which are well suited to TSV interposer technology (**Figure 5**).



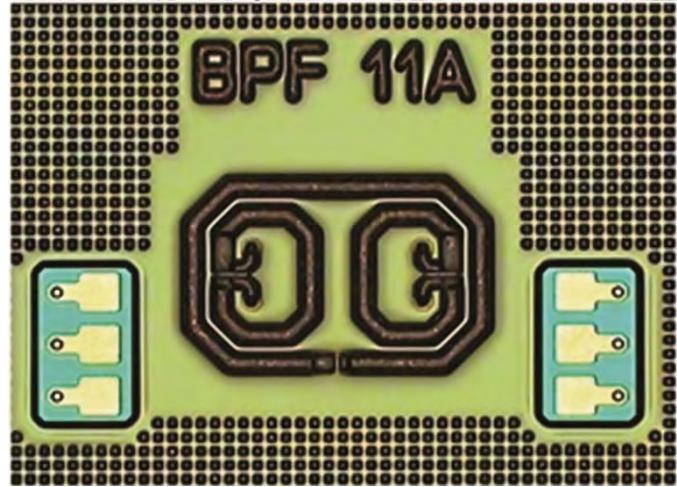
Figures 5. Super thin TSV PoP interposer

CSR: *With the approaching adoption of 3D ICs, a supply chain shift is expected. What is STATS ChipPAC's position in addressing this?*

Lasky: As the industry shifts to 3D IC integration, there are a number of different avenues and choices that companies can make and OSAT companies are working closer than ever with customers to drive technology integration. STATS ChipPAC has been investing in R&D, equipment and resources to establish a strong platform of 2.5D and 3D solutions. We have had the capability to fabricate, assemble and test TSV interposers for four years and are now implementing mid-end TSV processes which occur between the wafer fabrication and back-end assembly process.

CSR: *What collaborative efforts is STATS ChipPAC involved in?*

Lasky: STATS ChipPAC is involved in a number of collaborative efforts



Figures 4. Integrated passive device with TSV

with both our customers and leading foundries that will enable us to develop integrated packaging solutions for smaller, faster, more complex devices with optimum performance and manufacturability. One of our most notable collaborative efforts is with Intel IMC (formerly Infineon) and STMicroelectronics where we have developed a range of new design configurations for next-generation eWLB. A critical element of our long term success is alignment to foundry solutions that our customers are intent upon delivering to the market. To ensure our customers are well positioned with their solutions, we have technology collaborations with the leading semiconductor foundries that have enabled the early prove out of packaging solutions for silicon and provided STATS ChipPAC with technology leadership in the industry.

CSR: *With the explosion of the smart phone and tablet market, what are the biggest challenges the industry faces?*

Lasky: The ever increasing performance demands and continually shrinking form factor are what excite consumers, yet pose a difficult, ongoing challenge for the semiconductor and OSAT industry as we strive to hit the aggressive cost requirements. As die sizes and lithography nodes continue to shrink, the challenge is to find the most efficient way to integrate more functionality and performance into a final solution. STATS ChipPAC is combining technologies such as eWLB, TSV and IPD to achieve design flexibility and increased performance in a smaller form factor. Leveraging the combination of these advanced technologies into cost effective 3D structures will also be key to achieving challenging performance and power management requirements.



Figures 6. STATS TSV Interposer

Step-and-Repeat UV Imprint Lithography for Wafer-Level Camera Manufacturing

By G. Kreindl, T. Glinsnera, M. Kasta, D. Treiblmayra, and R. Miller [EV Group]

The ever-increasing adoption and consumption of CMOS image sensors (CIS) is driven by dramatic improvements in the cost/performance ratios of the entire systems into which the CIS is inserted. The drivers behind this are advancements such as improved signal-to-noise ratio and wafer-level processing technology related to 3D packaging. The primary improvement examined in this article is related to lens molding — especially the fabrication of wafer-level master stamps. The massive introduction of digital cameras in cell phones and smart phones has led the industry to produce increasingly higher quantities of lenses for camera objectives.

Wafer-level cameras (WLCs) enable the design and manufacture of miniaturized optics at wafer scale up to 300mm. The camera modules can be produced cost effectively with reduced form factor by applying micro molding processes. The production technology is scalable from a single-element for VGAs up to multi-element megapixel modules, where the lens wafers are precision aligned, bonded together and diced to form multi-element lens stacks.

The technical challenges in fabricating WLCs include: manufacturing the master stamp; replicating the lens on the wafer level; combining these full-wafer, micro-molded lens wafers with other essential parts like apertures or filters; and finally, aligning and assembling these modules in a manner that yields an integrated optical component. High-end megapixel WLC modules require tighter alignment and profile tolerances for the entire process — from the mastering to final stacking and dicing.

A high-precision and cost-effective mastering process for WLC image sensor applications has been developed. A single lens pin is used in a UV-nanoimprint lithography (UV-NIL) step-and-repeat approach to fabricate a high-precision, full-wafer master stamp for single step, large-area soft UV-NIL. This technique enables

the fabrication of next-generation, multi-element, mega-pixel modules where increased device performance is critical. The described approach offers a process flow, which covers all essential process steps for the fabrication of master stamps featuring unmatched lens position accuracies of <200nm and high lens shape repeatability, which is key for the fabrication of high-end WLC modules.

Wafer Scale Master Stamp Manufacturing Challenges

UV-NIL replication processes find various applications, such as micro-lens arrays, optical elements, and nano-imprint lithography. It can be classified into single step and step-and-repeat nano imprinting with soft polymeric or hard transparent templates.¹ Generally, the WLC application leverages step-and-repeat for master manufacturing and single-step, large-area soft UV-NIL for the replication process. The master stamp for WLC is a wafer-size template up to 300mm fully populated with lenses, with each lens to be stacked layer-on-layer first duplicated many times on a wafer in a step-and-repeat approach. Conventional master stamp fabrication processes like diamond or micro milling,^{2,3} UV proximity printing⁴, resist reflow^{5,6} or gray scale lithography⁷ can not address all critical parameters like lens axes tilt control, lens-to-lens lateral positioning, and profile accuracy. Step-and-repeat UV-NIL mastering meets all requirements for low-end camera modules such as VGAs, and also high-end multi-element megapixel cameras. Consider, for example, a low-end VGA camera module consisting of one lens element with two refractive optical elements on front and back side; there is the need for two lens master stamps with the desired optical design.

The top and bottom master stamps must match each other accurately in lateral distance and position without lens-to-lens de-centering. Figuring that conventionally available wafer scale master stamp fabrication techniques like diamond or

micro milling can achieve $\pm 1.5\mu\text{m}$ absolute lateral position accuracy with lens-to-lens profile accuracies down to <100nm, the lens apex de-centering can end up at 3 μm without considering the misalignment in the wafer scale replication process. Thus, for high-end megapixel modules, where up to four lens elements or more are stacked together, the lateral placement accuracy is inadequate to achieve the required optical properties of the camera module. Furthermore, these techniques have their limitations in regards to lens axis tilt control. Mastering techniques with good lateral placement accuracies and tilt control like resist reflow have their deficiencies in final lens form error. A lens-to-lens form error leads to yield loss because of image quality deterioration.

A single metal lens pin was used for single lens soft stamp replication. The liquid polymer pre-cursor is dispensed onto the master pin and squeezed between the master and a stepper-specific template. The stiffness of the fabricated working stamps can be adjusted by changing the mixture ratio of the base liquid and the curing agent, or also by changing the molecule end group in case of UV curable polymer. The created soft template usually



Figure 1. Photograph of the EVG 770 Gen II Semi-automated NIL Stepper

Lens-to-lens Positioning Measurement			
Nr.	Position [mm]	Measured Position [mm]	Lens-to-lens positioning deviation [nm]
0	14.422	14.4222	0
1	34.422	34.42191	-290
2	54.422	54.42177	-140
3	74.422	74.42184	70
4	94.422	94.42165	-190
Average lens-to-lens deviation [nm]			-138

Table 1. High precision profilometric measurement of a 20-mm by 20-mm lens grid array

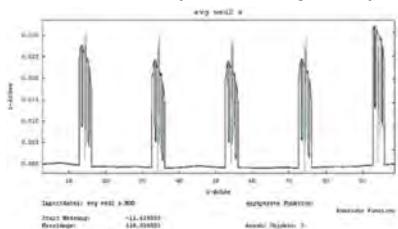


Figure 2. Profilometric measurement of a 20 mm by 20 mm lens grid array

resembles a negative counterpart from the used master. There is also the possibility for tuning the stamp polymer to actually replicate positive and negative counterparts from one master design. Soft working stamps have a relatively low surface energy, which ensures easier separation from the substrate after UV-NIL without additional anti-sticking layer treatment. In addition, because of the inherent properties of the soft materials (elastomers), the risk of master mechanical damage is

largely reduced. Therefore, template as well as processing costs of soft UV-NIL are significantly lower than other nanoimprint techniques. UV light through the glass and the transparent soft stamp polymer initiates the radical polymerization of the mastering material. As UV curable polymer* was used for the mastering process. The UV energy was set to 100mW/cm² for material polymerization. The system consists of a high precision moving stage to align the lens template, a polymer dispenser, a UV broadband exposure unit and an optical microscope. (Figure 1)

For accurate imprint control, there are three load cells implemented in the imprint head, to measure and control the imprinting and de-embossing force. This capability improves lens-to-lens as well as wafer-to-wafer resist thickness and residual layer uniformity, which are key features for the optical performance of the final device.

Position Metrology

Lateral placement

The lateral distance in x and y direction between each lens is defined by the optical module. A low-end VGA master stamp with a lens diameter of 1.66mm and an image sensor die size of 1.76mm in diagonal requires maximum ~ 4500 lenses on one master stamp, whereas a high-end mega pixel camera master stamp with a lens diameter of 4.25mm and an image sensor die size of 4.55mm consists of only ~770 lenses per substrate with increased lateral placement specifications. Herein a VGAtype master stamp was used to fabricate a 20mm by 20mm lens array over an 8" wafer area. The lens-to-lens positioning was measured using a profiler with a high-precision laser interferometer stage. The average measured deviation from the nominal lens position was ± 137nm in average (Table 1 and Figure 2).

Global Positioning

Low-end optical modules for WLC, such as VGAs, require at least a stack of two lenses with different shapes. State-of-the-art replication processes use standard mask aligner technology, where two global alignment keys on the substrate are used for the aligned top and bottom replication process. To meet state-of-the-art-fabrication processes, the step-and-repeat replicated lens array has to match these two global alignment keys. Herein, a convex and concave wafer-level lens master

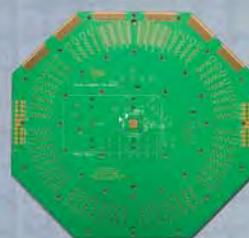
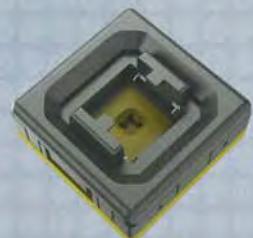


631 Montague Avenue
San Leandro, CA 94577
(510) 357-7900
Fax (510) 357-7600
www.contechsolutions.com

When it comes to test sockets and semi custom sockets, we provide an easy turn key solution to all your applications regardless of package type, lead count, or performance level.



Sockets for all types of packages



DUT Boards



Socket Receptacles

From engineering test to ATE test to RF test, our socket performance combined with our customer service and pricing will convince you that we should be your vendor of choice.

Get in contact with ConTech Solutions.

SEMI EXPOSITIONS

- SEMICONDUCTOR
- PHOTOVOLTAIC
- LED
- MEMS
- PRINTED/FLEXIBLE ELECTRONICS
- EMERGING MARKETS

THE PREMIER INTERNATIONAL EVENTS FOR MICRO – AND NANO – SCALE MANUFACTURING



UPCOMING EVENTS

SEMICON WEST 2011

JULY 12-14
Moscone Center
San Francisco, California
www.semiconwest.org

- North America's largest microelectronics manufacturing event
- More than 100 hours of technical conferences, sessions, and presentations covering the microelectronics supply chain from design/EDA to advanced packaging and test
- New—TechZONE exhibit pavilions covering high-brightness LEDs, MEMS, printed/flexible electronics, design, manufacturing services, materials, and secondary equipment and services

SEMICON TAIWAN 2011

SEPTEMBER 7-9
Taipei World Trade Center
Taipei, Taiwan
www.semicontaiwan.org

- Special pavilions: 3D IC & Advanced Packaging/Testing; Advanced Materials; Compound Semiconductor; Green Management; LED; MEMS; OEM Equipment/Parts; Cross Strait
- More than 60 programs, including FREE technical presentations at the Innovation Technology Center on the show floor
- The SEMICON Taiwan Golf Tournament attracts 200 participants from the semiconductor, FPD and PV industries

SEMICON EUROPA 2011

OCTOBER 11-13
Messe Dresden
Dresden, Germany
www.semiconeuropa.org

- SEMICON Europa is in the heart of the largest semiconductor cluster in Europe
- Segments in: Semiconductor Front-End; Test; Advanced Packaging; MEMS/MST; TSV; Secondary Equipment; Services and Technology
- In conjunction with PE2011 Conference and Exhibition—where plastic, organic and printed technology meets manufacturing

For the complete schedule of 2011 SEMI Expositions, visit
www.semi.org/events



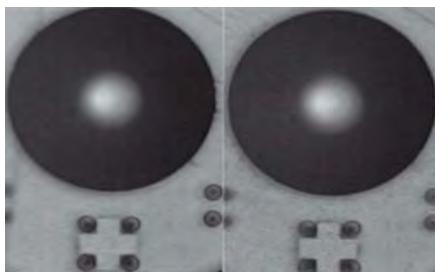


Figure 5. Left and right optical image of top and bottom aligned lens wafer

Top to bottom measurement				
Substrate Nr.	x left [μm]	y left [μm]	x right [μm]	y right [μm]
1	1,6	1,6	-0,7	-1,2
2	1,5	-1,2	-0,3	1,2
3	-0,2	-0,7	-1,6	0,7
Maximum Deviation	1,6	1,6	-1,6	-1,2

Table 2. Top to bottom measurement

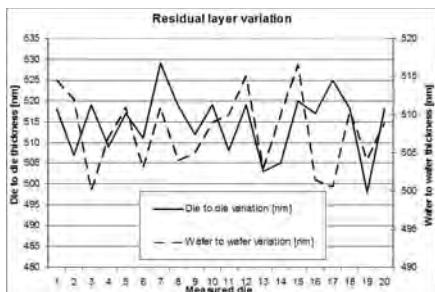


Figure 6. Graph of die-to-die and wafer-to-wafer resist uniformity

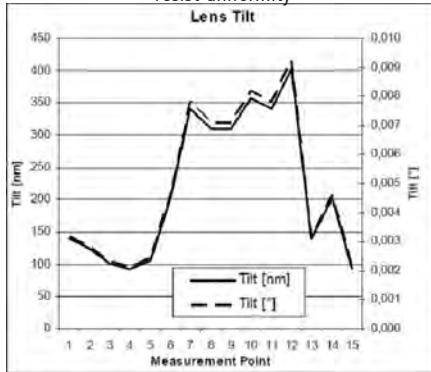


Figure 7. Graph of the optic axes tilt on a 2.5mm lens

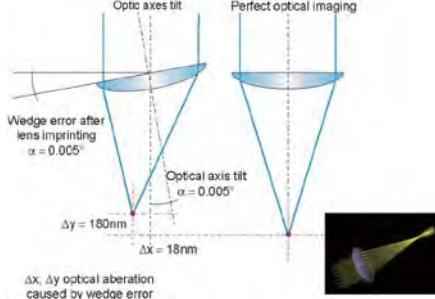


Figure 8. Optical simulation of optic axis tilt

was fabricated for double-side replication (Figure 3).

The fabricated double-side replicated lens stack was measured using state-of-

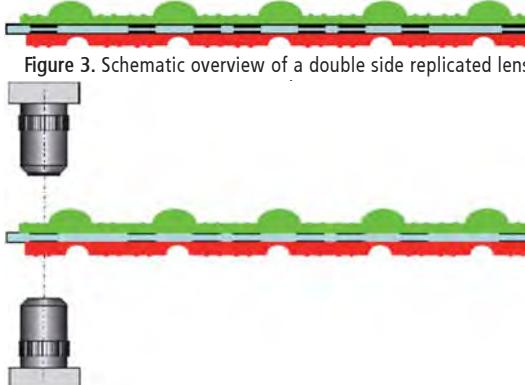


Figure 3. Schematic overview of a double side replicated lens

the-art, front-to-back side measurement equipment (Figures 4 and 5). The resulting lens apex de-centering measured on 3 wafers was less than ± 1.5 μm (Table 2), which reflects state-of-the-art replication processes using standard mastering processes such as diamond turning.

Master stamp lens-to-lens resist layer irregularity leads to yield loss caused by focal length differences, unwanted light path deviations, as well as intensity changes. The lens-to-lens uniformity of <3% and wafer to wafer uniformity <2% on a 515nm-adjusted resist layer thickness at 9N imprint force was measured on an atomic force microscope (AFM)** (Figure 6).

Resist Metrology

Lens-to-lens / Wafer-to-Wafer Residual Layer Deviation

Optic axes tilt results in focal length and focal point variation. An array of 15 lenses with a diameter of 2.5mm was replicated on a 200mm wafer. The optic axis tilt measured using a profiler*** was ~220nm or ~0,005° (Figure 7). Calculating the optic axes tilt in a simulation tool, the resulting focal point variation is about ~20nm in x and < 200nm in z direction.

Optic axes tilt

Optic axes tilt causes optical aberration. The diagram shows a lens with a wedge error after lens imprinting ($\alpha = 0.005^\circ$). The resulting optical axis tilt is $\alpha = 0.005^\circ$. The optical aberration is $\Delta y = 180\text{nm}$ and $\Delta x = 18\text{nm}$. The diagram also shows a perfect optical imaging without tilt.

Conclusions

We have introduced a master stamp fabrication technique for WLC application using step-and-repeat nanoimprint lithography. A metal master pin is replicated into a soft stamp, which is used for the fabrication of large area masters in a step-and-repeat UV-nanoimprinting process. These large area master stamps are well-suited for double-side, single-step imprinting for optical modules for WLC. The fabricated master stamps outperform state-of-the-art mastering techniques in regards to lateral placement, optic axis tilt, and resist layer uniformity.

*ORMOCOMP from Micro Resist Technology.

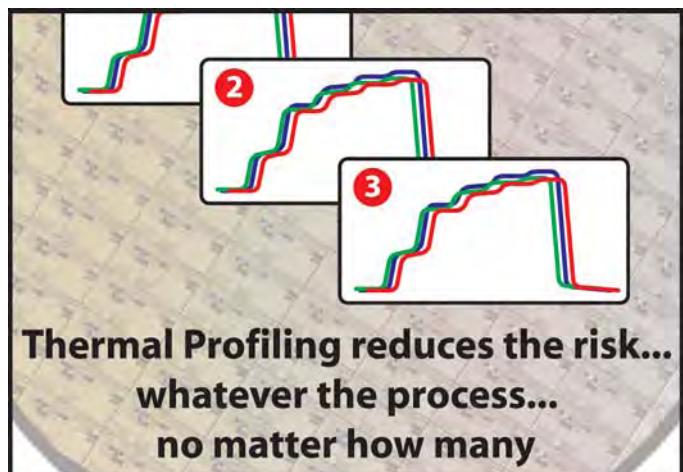
** D 3100 Veeco Instruments

***Tencor Profiler

References

- [1] S.Chou, et. al, Nanoimprint Lithography, J.Vac. Sci. Technol. B 14 (6), 1996
- [2] Badrawy, S.: "Micro Milling - An Alternative Solution for Diamond Turning of Lens Arrays". Proc. Optonet - Ultra Precision Workshop, Jena, Germany (2008)
- [3] Scheiding, S. et al.: "Lens array manufacturing using a driven diamond tool on an ultra precision lathe". Proc. 9th int. EUSPEN Conference, San Sebastian, Spain, Vol II, p. 423-426 (2009)

For a full list of references, please contact the author.



Thermal Profiling reduces the risk...
whatever the process...
no matter how many



www.ECD.com • sales@ecd.com
+1 503 659 6100 or +1 800 323 4548

Home of the M.O.L.E.® Thermal Profiler

ECTC and the Future of Engineering

By Sandra Winkler [New Venture Research]



At the first SVEC (Silicon Valley Engineering Council) banquet I attended, I was quite impressed with the speeches given by the inductees into the Engineering Hall of Fame. Stanley Myers, President and CEO of Semiconductor Equipment and Materials International (SEMI®), spoke of inspiring change, of wanting to encourage young people to create the future. He spoke of the importance of



engineering here in Silicon Valley and its effect on the rest of the world. So many of the

innovations now in use across the globe were rooted here, in Silicon Valley, and, he added, "What happens here goes around the world in a blink of an eye." He alluded to the need for more education in engineering, and a political landscape in which companies can come to Silicon Valley and build on the legacy created by the engineers who turned this valley into what it is today.

What is also needed is a chance for engineers to showcase their research so that technology can be built upon it. Much of this occurs at the annual ECTC (Electronic Components Technology Conference) event, the premier engineering conference.

The 61st ECTC was held in Lake Buena Vista, Florida, from May 31st through June 3rd, 2011 and featured six tracks of papers presented simultaneously each day. This year's paper topics included:

- Advanced IC packaging
- Interconnection
- Optoelectronics
- Materials and processing
- Electronic components and RF
- Modeling and simulation

- Emerging technologies
- Applied reliability
- Assembly and manufacturing technology



Senol Pekin, of Intel, Dr. Nasser Grayeli Director Intel Quality Network, David Mc Cann Amkor Technology and Rajen Dias, Intel gather after Grayeli's luncheon keynote

Geographically, presenters represented 32 countries and 25 states, with the top five locations being the U.S., South Korea, Taiwan, Japan, and Germany. Some conference statistics include:



Bill Chen, ASE, and Rolf Aschenbrenner, Fraunhofer IZM, present Rao Tummala, founder, Georgia Tech. PRC, with the IEEE Components and Packaging Technology Award for "Pioneering and innovative contributions to package integration research, cross disciplinary education, and globalization of electronic packaging."

- Over 1,000 attendees
- 342 technical papers presented in 36 oral and five poster sessions including a student poster session
- Over 60 papers/posters presented on 3D/TSV
- 16 professional development courses attended by a record 386 participants
- 61 Technical Corner exhibitors

Attendance was up slightly over last year, with conference attendees numbering 861, professional development course attendees at 386 and a slight drop in exhibitors to 60 from 65.

Most notable was that eight of these technical sessions focused on 3D Packaging



Attendees enjoy the perks of the conference: great food and friendship

and TSV(Through-Silicon-Via) to address exciting new developments and applications in this quickly expanding field.



The conference kicked off Tuesday with a full day of professional development courses, followed by a student reception and an evening plenary session titled, "Spotlight On China". Speakers representing industry, R&D, and academia provided a broad overview of semiconductor activities in China. According to C.E. (Ed) Pausa, PwC, China has become the dominating consumer of semiconductors. In fact, consumption growth has outrun the rest of the world, with 29% CAGR vs 4% CAGR worldwide. Part of this is because China was less impacted by the global economic recession. Pausa added



Karen May and Rao Tummala of Ga Tech with Patricia MacLeod and John Hunt of ASE



Ron Molnar of Az Tech Direct, Debra Walker and Jim Walker of Dataquest / Gartner Group

that China's consumption is concentrated in communication computing and less in automotive and military. There is some concern with the IC consumption vs. production gap. In 2010 there was an \$85.5B difference between the value of semiconductors consumed vs. produced in China. There is motivation for the Chinese government to increase indigenous production, which in turn can mean both opportunity and challenges for established multinational companies.

The Wednesday plenary session was titled "Power Efficiency Challenges and Solutions: From Outer Space to Inside the Human Body", which I found to be the most interesting. Raj Master of Microsoft gave some scary examples of the harm that can come to humans if electronic devices they are holding and operating overheat. Whereas miniaturization, flexibility, and portability are desired traits in consumer electronics, these features also cause overheating, which can lead to product failure and human catastrophes. 3-D packaging doubles the heat density, which degrades product performance by 30%. Power and noise both increase, which is why it is important for thermal and noise management to be part of the initial product design.

Sayfe Kiaei of Arizona State University presented a number of forward-looking medical electronics products designed to improve the lives of the disabled. A wireless, swallowable capsule can be used to record data that can then be transmitted to the patient's doctor. An implantable RF transceiver can be used to treat heart conditions and manage pain, and as an implantable



ECTC Finance Chair, Patrick Thompson, and Rolf Aschenbrenner, Fraunhofer IZM, present John Lau, ITRI, the 2011 IEEE CPMT Outstanding Sustained Technical Contribution Award



Rao Tummala celebrates a successful event with 2011 ECTC Program Chair, Wolfgang Sauter, IBM Corp

wireless neural, act as a sensor and control. The sensor can be used to control prosthetic limbs, powered by RF from outside the body. The RF power could be stored in a transceiver, which gives information to a receiver at the end of the prosthetic or in a pocket. A cochlear implant (in the ear) can be used as a sensor for a prosthetic arm or hand. An integrated hearing aid can have a microphone array to focus which sound to pay attention to; a MEMS device can be used for this with its small size. An adapted microphone can cancel background noise.

A number of annual awards were presented at the Thursday luncheon. Rao R. Tummala, Endowed Chair Professor at Georgia Institute of Technology, received the prestigious 2011 IEEE CPMT Award for pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging. Five more IEEE members were honored for their distinguished service and contributions to the industry.

Rao R. Tummala
2011 IEEE Components, Packaging and Manufacturing Technology Award

John Lau
2011 Outstanding Sustained Technical Contribution Award

Xuejun Fan
2011 Exceptional Technical Achievement Award

Mark Brillhart
2011 Electronics Manufacturing Technology Award

Muhannad Bakir
2011 Outstanding Young Engineer Award

Paul Wesling
2011 Regional Contributions Award

In addition, three 2010 IEEE Transactions Best Paper awards were announced and ten individuals were named as 2011 IEEE CPMT Fellows. Congratulations to all of the recipients.

There were many interesting exhibits this year. ITRI's John Lau was showing off some interesting new 3-D technology, which starts with a $5\mu m$ thin wafer. This is thin enough that one could see through it when holding it up toward the ceiling facing the light!



Sandra Winkler of New Venture Research and John Lau of ITRI hold a $5\mu m$ thin wafer

Next year's ECTC event will be held in San Diego, California, May 29 through June 1st, 2012 at the Sheraton San Diego Hotel & Marina. Submit your 750 word abstracts to www.ectc.net by October 10, 2011.

Predictive Modeling to Prevent Thermal Stress Failures in Electronics and Photonics

By Ephraim Suhir [UC Santa Cruz]

Thermal stress caused by the thermal expansion/contraction mismatch of dissimilar materials and/or by temperature gradients is typical in electronic systems used in information, telecommunication, high power and other “high” technologies. It is also the major reliability concern and the main reason of the finite service life of assemblies, packages, devices, and systems. Ductile rupture, brittle fracture, thermal fatigue, creep, excessive elastic or inelastic deformations, thermal shock, and stress corrosion are examples of structural thermal stress failures that can also lead to functional (electrical, optical, thermal) failures.

Predictive modeling is a powerful and cost-effective means to understand the physics and prevent thermal stress failures. Analytical (“mathematical”) modeling

occupies a special place in the modeling effort. Although powerful and flexible computer programs enable one to obtain, within a reasonable time, a solution to almost any stress-strain-related problem, the broad application of computers does not make analytical solutions unnecessary or even less important. Simple analytical relationships offer clarity and “compactness” of the obtained information and clear indication on the role of various factors affecting the given phenomenon or the behavior of the given system.

Bimetal thermostats and biomaterial assembles are the simplest and the most typical structural elements in electronic systems. 1) A typical electronic thermostat assembly is highly rigid, and its appreciable bowing, if any, is viewed as a shortcoming, and not as a merit, of the assembly

**Stresses in Adhesively Bonded Joints:
Effect of Joint Size**

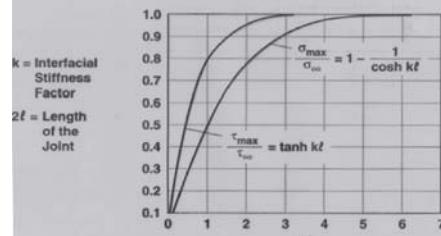


Figure 1. Effect of the material-length parameter kl of the interfacial shearing stress on thermal stress level performance. 2) Thermostat materials (metals) are quite different from the materials used in typical electronic and photonic structures, and so is their propensity to failure. 3) The thermal stress related response of concern in thermostat strips are significant bending stresses acting in its cross-sections; the main concern in electronics assemblies are both the stresses acting in the assembly

Need a one-stop supplier?



www.multitest.com

components (primarily in the chip) and the interfacial shearing and peeling stresses that can lead to adhesive or to cohesive failure of the bonding material, and/or to brittle cracks at the chip corners.

Die substrate assembly is the heart and brain of an electronic or a photonic device. Die failure and/or cohesive or adhesive failure of the bonding material are typical failure modes observed. A crack on the die's upper ("free") surface should be attributed to the excessive normal bending stress at low temperature conditions. If such a crack is observed, it means that the tensile stress caused by the convex bending of the assembly exceeds the compressive stress due to the thermal contraction mismatch of the high expansion substrate and the low expansion die. The crack at the die's corner, at its interface with the substrate, is caused by the elevated interfacial stresses. Measures that could be taken to reduce the induced stresses depend on the type/category of the stress responsible for the particular failure mode. In the case of a crack in the die in its mid-portion, it is the improved thermal

match between the die and the substrate materials and/or the reduced assembly bow that might improve the situation.

Ceramic substrates, although more expensive, are preferable not only because they are inorganic, and, hence, more robust, but because their low CTE makes them a better match with Si. Lower bow can be achieved also by using a thick substrate (with a high flexural rigidity), or by going in the opposite direction and using a thin-and-flexible substrate. Cracks at the die corner can be prevented by using thicker bonding layers and/or by using low modulus adhesives. The stresses in small-size assemblies (5-7mm die size), increase as the assembly size increase and with the decrease in the compliance of the attachment. The stresses in sufficiently large assemblies ($> 8-10\text{mm}$) do not increase with a further increase in the assembly size (**Figure 1**). The product kl , of the parameter k of the interfacial shearing stress and half-the-assembly-size l can be used as a suitable criterion of the effect of the assembly size and the interfacial compliance on the thermal stress level.

The models⁴⁻⁷ were applied by numerous investigators to many problems in electronics and semiconductor crystal growth and other areas of engineering. By using the analogy between the thermally induced and lattice-misfit induced strains, a new approach to the high quality (dislocation free) epitaxial growth of lattice-mismatched materials was suggested.⁸

Low-yield-stress bonding layer results in a situation, when peripheral zones of the bonding assembly exhibit inelastic strains.⁹ This problem is important in connection with using Indium-based alloys as highly compliant bonding materials to attach laser chips to metal sub-mounts in the quantum wells of GaAs lasers. The actual stress condition can be found between two extreme situations: ideal elasticity and ideal plasticity. The developed model enables one to determine the lengths of the peripheral plastic zones. This information can be used in the development of figures-of-merit for solder-joint attachments in electronic and photonic packages.

Tri-material assemblies¹⁰ should be considered if the bonding material is high-

Visit us in Santa Clara, CA

OPEN HOUSE WEEK
2011

- > live demos
- > fab tours
- > expert discussions

www.multitest.com/open-house



modulus and/or is thick, so that all the materials in the assembly become “equal partners”. If a compliant bonding layer is used at one or at both interfaces, it can be accounted for in the same fashion as it has been done in a bi-material assembly, i.e., by adding the interfacial compliance of the bond to the interfacial compliances of the bonded materials themselves.

Global and local mismatch stresses occur and interact when the bonding layer is inhomogeneous, as, e.g., in solder joint interconnection systems; when the assembly components are bonded to each other at the assembly ends only; or when low modulus adhesives are used for lower interfacial stresses at the assembly ends. “Local” mismatch loading is due to the thermal expansion mismatch of dissimilar materials within the bonded region, while the “global” loading is caused by the mismatch of bonded materials in the unbonded region. “Global” mismatch stresses can be modeled as structural response to an equivalent external “mechanical” loading.

Assemblies bonded at the ends are also of interest in some electronic assemblies. In many flip-chip designs the solder joint stand-off is so small that it is next-to-impossible to bring in the underfill material underneath the entire chip, especially in the case of large chips. On the other hand, there might be no need for doing that, since the underfill works only with its peripheral portions. Modeling is crucial in order to establish the adequate width of the bonding layer.¹²

Numerous, experimental and/or FEA based models were developed for the evaluation of thermal stresses in, and the lifetime of, solder joint interconnections. The majority of today’s studies address thermal fatigue of lead-free ball-grid-array (BGA) and land-grid-array (LGA) systems due to the accumulated cyclic inelastic strain (“lost elastic energy”) in the material. There are some specific requirements for the photonics solders: ability to achieve high alignment, to withstand creep, etc. “Hard” (high modulus) solders (e.g. gold-tin eutectics) have better creep characteristics than “soft” (silver-tin) solders. “Hard” solders can result, however, in a higher thermal stress than “soft” solders. For this reason their ability to withstand creep might be

not as good as expected, not to mention the short-term reliability of the material.

Assemblies with low modulus adhesive at the ends are used to minimize the interfacial stresses.¹⁶ There is no need to employ a low modulus material throughout the interface: it is sufficient to use it only at the assembly ends where the interfacial stresses are the highest.

Thermally matched assemblies could be viewed as a desirable extreme case of a bi-material assembly. Examples are Si-on-Si flip-chip (FC) technology,¹⁹ ceramic Cerdip/Cerquad package design,²⁰ and low-cost holographic memory storage assemblies,²¹ in which a thick and low modulus photosensitive adhesive is used. A solder joint in a Si-on-Si flip-chip design can be modeled as a short circular cylinder subjected to the axisymmetric shear loadings applied to its plane ends.¹⁹ Such loadings reflect the “local” mismatch situation during temperature cycling or reflow soldering conditions.

The case of identical ceramic adherends²⁰ was considered in connection with choosing an adequate CTE for a solder (seal) glass in a ceramic package design. The numerous failures in the initial AT&T design of the ceramic/seal-glass package assembly were due to the higher CTE of the bonding glass than that of the ceramics. This led to the tensile stress in the glass layer at low temperature conditions and to its brittle fracture. The situation had been improved dramatically when the seal glass with a CTE lower than in the ceramics was selected. The package manufactured in accordance with the developed recommendations exhibited no failures.

It was determined that the best result could be achieved by using a probabilistic modeling approach, in which the CTE of the solder glass and the ceramic materials were treated as random variables. The design of the improved structure was based on the requirement that the probability that the normal stress in the seal glass is always negative (compressive) and that this compression is low enough, so that the interfacial stress at the glass-ceramic interface does not exceed the allowable level, is close to unity. It is always advisable to carry out sensitivity analyses of the thermal stress in order to establish, when one could get away with a deterministic approach and when a

probabilistic analysis and a probabilistic design for reliability (PDFR)^{22,23} is advisable.

A Probabilistic approach is a must in situations where the “fluctuations” from the mean values are significant and when the variability, change and uncertainty play a vital role,^{24,25} so that the structure will most likely fail if the uncertainties are ignored. Wide and consistent use of probabilistic models not only enables one to establish the scope and the limits of the application of deterministic approaches, but can provide a solid basis for a well-substantiated and goal-oriented accumulation, analysis and effective utilization of empirical data.

Thin films are widely used in electronics. Typical thermal stress failures in thin films are interfacial delaminations (including delamination buckling), film cracking and blistering. Stress in the given film layer of a multilayer film structure is due to its CTE mismatch with the substrate, and not with the adjacent layers. Edge stresses in the film are affected by the edge configuration. Circular assemblies are somewhat “stiffer” than the rectangular ones and result in higher stresses that concentrate at a more narrow peripheral portion (ring) of the assembly. Stress in a thin film, which does not experience bending stresses, is not affected by the assembly bow, while the assembly bow and the stresses in the substrate are strongly affected by the stresses in the film. The application of the well-known Stoney’s formula will be misleading, if used for the design purposes.^{26,27}

Thermal stress-induced bow can be as detrimental to the performance of an assembly²⁸⁻³¹ as the stress is. Significant bow can prevent further processing of BGA and LGA packages, or of thin plastic IC packages, and lead to cracking of ceramic substrates in thin over-molded packages, or have another adverse effect on the design and processing of plastic packages of IC devices. Ceramic substrate cracking in over-molded plastic packages can be prevented by decreasing the thermal stress induced bow.^{30,31} This can be achieved by applying a thin surrogate layer of a high-expansion, high-modulus and high-strength layer of a polymeric material fabricated at the free side of the ceramic substrate³⁰ or by applying a thin surrogate layer of a negative-expansion ceramics on the polymer side of the package.³¹

Bow-free assemblies are particularly

important in photonic systems³²⁻³³. To be bow-free, a multi-material assembly should be made statically indeterminate and should contain, therefore, at least three dissimilar materials with large enough flexural rigidities, so that the resulting bending moment, caused by the induced forces in all the three materials, is zero. Computations based on the developed analytical models have indicated that the “thick” bonding layer in a bow free assembly can still be made thin enough (not thicker than about 4 mils or so) to do the job, provided that the material and/or the thickness of at least one of the adherends is adequately chosen.

Conclusion

Thermal stress is the major reliability concern in electronic systems used in information and telecommunication technologies, and other areas of “high-tech” engineering. Predictive modeling is an effective and low-cost means for the prediction and prevention of thermal stress failures in these systems. Analytical modeling should be used, whenever possible, in addition to FEA modeling in any effort aimed at the analysis and rational design of a viable, reliable and cost-effective product. ■

References

- W.T. Chen and C.W.Nelson, “Thermal Stresses in Bonded Joints”, IBM Journal, Research and Development, vol.23, No.2, 1979.
- E. Suhir, “Stresses in Bi-Metal Thermostats”, ASME Journal of Applied Mechanics, vol. 53, No. 3, Sept. 1986.
- E. Suhir, “Die Attachment Design and Its Influence on the Thermally Induced Stresses in the Die and the Attachment”, Proc. of the 37th Elect. Comp. Conf., IEEE, Boston, Mass., May 1987.
- E. Suhir, “Interfacial Stresses in Bi-Metal Thermostats”, ASME Journal of Applied Mechanics, vol. 56, No. 3, September 1989.
- E. Suhir, “Analytical Thermal Stress Modeling in Electronic and Photonic Systems”, ASME Applied Mechanics Reviews, invited paper, vol.62, No.4, 2009.
- S. Luryi and E. Suhir, “A New Approach to the High-Quality Epitaxial Growth of Lattice - Mismatched Materials”, Applied Physics Letters, vol. 49, No. 3, July 1986.
- E. Suhir, “Interfacial Thermal Stresses in a Bi-Material Assembly with a Low-Yield-Stress Bonding Layer”, Modeling and Simulation in Materials Science and Engineering, vol. 14, 2006
- E. Suhir, “Analysis of Interfacial Thermal Stresses in a Tri-Material Assembly”, Journal of Applied Physics, vol.89, No.7, 2001
- E. Suhir, “Predicted Thermal Mismatch Stresses in a Cylindrical Bi-Material Assembly Adhesively Bonded at the Ends”, ASME Journal of Applied Mechanics, vol.64, No. 1, 1997.
- E. Suhir, “Thermal Stress in a Bi-Material Assembly Adhesively Bonded at the Ends”, Journal of Applied Physics, vol. 89, No.1, 2001.
- J. Lau (ed.), “Ball Grid Array Technology”, McGraw-Hill, 1995.
- J.S.Hwang, “Modern Solder Technology for Competitive Electronics Manufacturing”, McGraw-Hill, New York, 1996
- E. Suhir, “Thermally Induced Stresses in an Optical Glass Fiber Soldered into a Ferrule”, IEEE/OSA Journal of Lightwave Technology, vol. 12, No. 10, 1994.
- E. Suhir, “Thermal Stress in an Adhesively Bonded Joint with a Low Modulus Adhesive Layer at the Ends”, Applied Physics Journal, April 2003.
- E. Suhir, “Thermal Stress in a Polymer Coated Optical Glass Fiber with a Low Modulus Coating at the Ends”, Journal of Materials Research, vol. 16, No. 10, 2001
- E. Suhir, “Electronic Assembly Having Improved Resistance to Delamination”, U.S. Patent #6,028,772, 2000
- E. Suhir, “Axisymmetric Elastic Deformations of a Finite Circular Cylinder with Application to Low Temperature Strains and Stresses in Solder Joints”, ASME Journal of Applied Mechanics, vol. 56, No. 2, 1989.
- E. Suhir and B. Poborets, “Solder Glass Attachment in Cerdip/Cerquad Packages: Thermally Induced Stresses and Mechanical Reliability”, ASME Journal of Electronic Packaging, vol. 112, No. 2, 1990
- E. Suhir, “Adhesively Bonded Assemblies with Identical Nondeformable Adherends and “Piecewise Continuous” Adhesive Layer: Predicted Thermal Stresses and Displacements in the

(continued on Page 57)

ZIP® Flat is the Future of Test

2012: 0.10mm
2011: 0.20mm
2010: 0.30mm
2008: 0.40mm
2006: 0.50mm
2004: 0.80mm

A Cost-Effective Single Architecture for Your Lab, Final, Burn-In, and Wafer-Level Test

High Performance



Kelvin



Scrub S



Scrub W



Super Short



Long Travel



Everett Charles Technologies
A DOVER COMPANY

www.ectinfo.com/zip

909-625-9390

Patents 7,862,391, 6,462,567 and 6,396,293 and other Patents Pending

Package Design: A Performance Killer or a Savior

By Madhavan Swaminathan and Bill Martin [E-System Design]

The frequencies common in today's products are magnitudes higher than a decade ago. The downside of these new realities is that packages are no longer perfect transfer components. Instead they act as low pass filters where the cut-off frequency is dictated by how well the signal lines are routed. In today's technology, assuming an IC package is a perfect conductor of signals can be a huge mistake. Packages can no longer be considered 'simple', cheap conductor of signals that are perfect transfer mechanisms between the IC and printed circuit board (PCB). With the advancements in package materials and manufacturing, densities and layers once dreamed about are becoming a reality. What's more, with the trend towards 3D integration, wiring densities will increase in the package, thereby making the design of the package more complex to manage the noise budgets.

Packaging: no longer passive but a "killer" for signal integrity

Years ago, operating frequencies were below 1GHz and signal integrity was limited to a few designs pushing high frequency limits. In the 'good old days', packages were 'ideal' transfer mechanisms to transfer signals from integrated circuits (ICs) to printed circuit boards (PCBs). With recent technology advancements and consumer demand for transferring large files (audio, video, etc) in short time periods, products must operate at much higher frequencies. These higher frequencies cause materials to exhibit properties that were once hidden. Often times differential signaling has been used to mitigate the anomalies associated with poor routing in the package.

In today's environment, extensive signal and power integrity (SI and PI) analysis on the package must be completed to ensure the quality of both the signals and power distribution in the package. Given the size difference between packages and PCBs, most of the

SI/PI budgets are often times allocated to PCBs with little for the package. Unfortunately, a poorly designed package can swallow most of this budget. This effect is amplified due to Return Path Discontinuities (RPD), which have

a larger effect in the package than the PCB. To illustrate the effect of RPDs, a simple example is described in Figure 1a and 1b consisting of 2 pairs of differential signals with via transitions where the microstrip signal lines transition from the top layer to the bottom layer and back to the top layer. The effect of the vias due to return currents on the planes causes degradation in the signal performance. A general misconception is that differential signaling will mitigate this effect. Hence, the lines in Figure 1 are routed as differential pairs.

The differential lines were designed with line width $w=5\text{mils}$, line spacing $s=5\text{mils}$, differential pair spacing $S1=20\text{mils}$, line thickness $T=0.7\text{ mils}$ and dielectric thickness $D=3.3\text{mils}$ for a 100ohm differential impedance. The signal lines are 2" long with a plane size of 2" x 2" inches. The vias in Figure 1a have a pitch of 100mils. The resulting differential insertion loss frequency response for Diff Pair 1 (Figure 1) is shown in Figure 2. The result is compared with a differential microstrip line (called ideal here) of same length without any via transitions and with 100ohm differential impedance. As can be seen, the ideal microstrip line has a maximum insertion loss of -2.5dB @ 10GHz and -5dB @ 20GHz. However, the differential lines with via transitions begin to deviate from the ideal microstrip line around 4GHz, and have

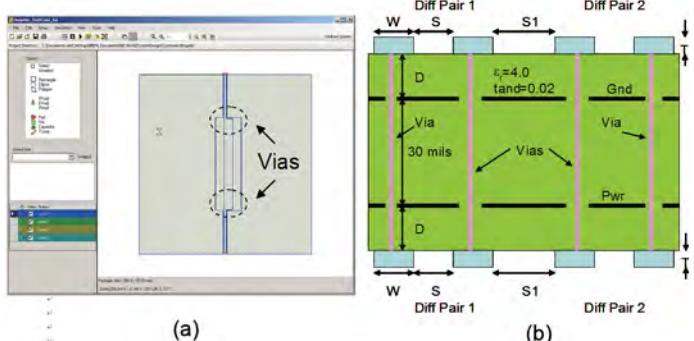


Figure 1. Differential Lines (a) Layout and (b) Cross section

insertion loss in the range -7dB to -32dB in the 10 — 20GHz range. Since a large insertion loss represents a loss of transmitted power, this is a major problem. Unlike differential lines illustrated here, single-ended lines will incur much higher insertion loss. Therefore, modern packages MUST be thoroughly analyzed for their effect on signal integrity. The degradation in the signal frequency response due to RPD occurs due to the interaction of signal lines and power distribution and hence the need for signal and power co-simulation for obtaining design signoff for packages supporting high frequencies. Many board designs consider a link budget insertion loss that includes the package and PCB from transmitter to receiver of -10dB. Package insertion loss larger than -5dB reduces the insertion loss budget allowed for PCB. Since signal lines in the PCB are much longer than in the package, this can pose a huge problem. (Detailed

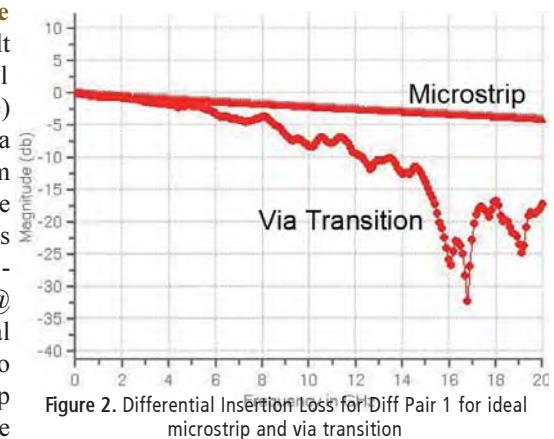


Figure 2. Differential Insertion Loss for Diff Pair 1 for ideal microstrip and via transition

discussions on RPDs are described in References 2 and 3.)

What analysis is required for good signal integrity analysis?

RPDs occur due to interruption in the return currents on the power and ground planes of the package. So, what kind of analysis is required to ensure that these effects can be caught early in the design cycle? Typical guidelines for a high frequency design operating upwards of 1GHz are provided here:

- Insertion loss (IL) measures the signal strength from top (C4) to bottom (BGA) of the package. Any signal that has larger than -5dB insertion loss (assuming a maximum package size of 4cm x 4cm) across the frequency range provides little budget for the PCB level interconnects and hence can cause performance or functionality issues in the design. The closer to ideal (0dB), the more margin is provided for other design components (i.e. printed circuit board or other packages). IL needs to be measured for each signal and any signals with poor IL need to be addressed.
- Near-end cross talk (FEXT) and far-end cross talk (NEXT) measures the interaction between nearby signal lines (closest neighbors) and occur due to the electromagnetic fields in the vicinity of the structure. Once the cross talk levels are above -15 to -20dB, they will begin to affect the performance of these signals.
- Substrate noise measures the interaction between signals that are far away from each other through the power and ground planes in the package. This is an effect that can only be captured by analyzing the entire package that includes the signal lines and the power distribution structure and is the most difficult to mitigate. A target of -25 to -30dB is preferred between individual lines due to the need to support many drivers switching simultaneously.

Each design will have criteria for passing or failing signal integrity, depending on the operating environment

for the design. Products used in critical, life-threatening environments will have tougher signal integrity criteria than other products. An example is tighter insertion loss of -3dB or cross talk or substrate noise set at -30dB and -40dB, respectively. These environments may alter guidelines provided above. Since RPDs occur due to the interaction between the signal and power distribution, it is imperative that signal lines are analyzed in the presence of its power distribution network.

Two designs in different stages of development: a comparison

When packages are designed, signal routing in the presence of power and ground planes has a large impact on signal integrity. This effect is illustrated in two designs. The first design provided by IBM is a 32mm x 32mm, 8 layer, flip chip, multi-layered BGA package. The package was measured using high frequency TDR measurements and correlated with Sphinx, a signal and power integrity co-simulator.^{4*} The other is a 7 layer package that is in development and from a different vendor. This design will be denoted as PID. Each package has chosen different manufacturing processes and therefore the stack-up's electrical/physical parameters and layout rules differ. Why these different processes are chosen is a combination of cost, requirements, performance, and

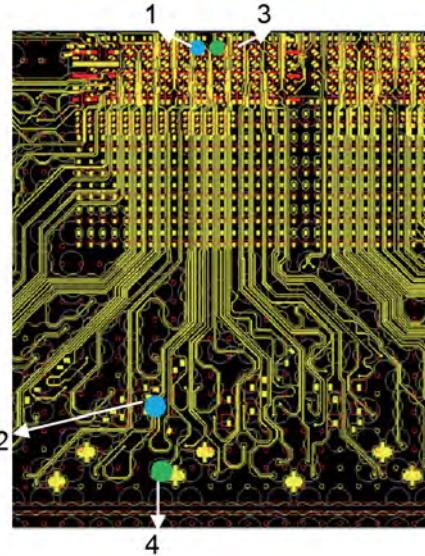


Figure 3. IBM package showing the input and output ends of adjacent signal lines (shown as blue and green dots)

ZIP SCRUB[®]

Eliminate Your Solder Transfer Issues!



Positive “Scrub-Action” on Pads and Leads



Positive Solder-Ball Contact



**Everett Charles
Technologies**
A DOVER COMPANY

www.ectinfo.com/zip
909-625-9390

Patents 7,862,391, 6,462,567 and 6,396,293 and other Patents Pending

manufacturing process accessibility and is not of importance here. However, the frequency response of the signal lines is the focus of the comparison.

Only two transmission lines from the center ‘cage’ area on the top surface to the ball grid layer at the bottom were analyzed. This allows insertion loss, cross talk and substrate noise to be simulated. On each design, the two transmission lines that were chosen have similar functionality, are physical neighbors in the ‘C4 cage’ area, and traverse from top to the bottom layer. The screen shot in **Figure 3** shows the layout for a section of the IBM design. The blue and green dots represent transmission line ends that were ported, to compute the IL and other parameters. Similar analysis was performed on the PID. Ports represent the excitation and measurement points and are defined as numbers (1, 2, 3, and 4) in **Figure 3**.

The measurement from the IBM package was used to calibrate the accuracy of Sphinx, a signal and power integrity co-simulator that was used for the analysis.³ Since, measurements were conducted in the time domain using TDR equipment; frequency response obtained from the simulator was converted into a spice netlist to reconstruct the measurement set-up. The simulated results were compared to measurements⁴ for signal transmission, NEXT and FEXT, with only the FEXT correlation shown in **Figure 4**. As can be seen the correlation is excellent, providing high confidence in the accuracy of the frequency domain response obtained from Sphinx. In **Figure 4**, both the FEXT and reflected cross talk waveform are correlated well with measurements. Though calibration of any simulator is required, laboratory measurements are

often times the most expensive and require large amounts of time to obtain. On the other hand, frequency and time domain analyses are much faster and less expensive than laboratory measurements. Though digital applications require package analysis in the time domain, it is often times simpler to analyze the signal waveforms in the frequency domain to identify RPD effects. Frequency domain analysis is generally computationally inexpensive compared to time domain analysis, and often allows a designer to identify RPD effects at specific frequencies that can then be mitigated by modifying the layout geometry. Therefore, frequency domain analysis provides a signal and power integrity analysis methodology that can accelerate release of design to manufacturing.

Shifting now to PID; are the results from the two packages similar? This can be assessed by reviewing two transmission line neighbors that traverse from the C4 cage to BGA, similar to **Figure 3**. This comparison can therefore serve as an excellent indicator as to how close each design is to meeting release criteria. The PID was analyzed using 200 frequency points over a frequency range of 1MHz up to 20GHz using Sphinx. This analysis was completed in 49 minutes (~15 seconds per frequency point). **Figure 5** compares insertion loss (IL) for IBM and PID packages (zoomed to 0 to 10GHz). Any higher frequencies show much worse IL for PID. From these responses, it can be seen that the IBM package is fairly consistent up to 10GHz, IL is -

4.11dB. For the PID, it is obvious that beyond 4GHz, one of the signals has an IL worse than -5dB. Both of these packages will be mounted on a printed circuit board, which will only worsen the overall IL for these signal lines. If the PID required operating frequency is higher than 4GHz, clearly a re-design effort is required. Re-designs require an iterative design process where repeated simulations are required. Hence, faster simulation time is a critical aspect for achieving reduced design cycle time.

This is possible by reducing the frequency points used in the simulation. As an example, use of only 20 frequency points to cover a frequency range of 10GHz requires only 5 minutes (~16 seconds per frequency point) to run simulations using Sphinx. This short simulation time allows multiple ‘what if’ scenarios to be run and evaluated; providing designers with a methodology to quickly hone improvements to meet signal integrity budgets. In addition, designers could run alternative manufacturing stack-up parameters to determine manufacturing cost versus

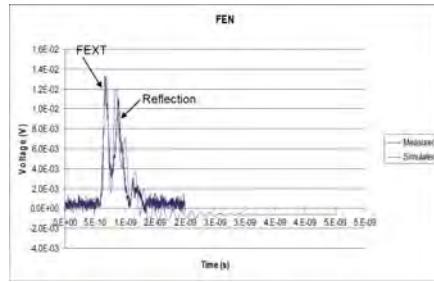


Figure 4. FEXT model to hardware correlation for IBM package

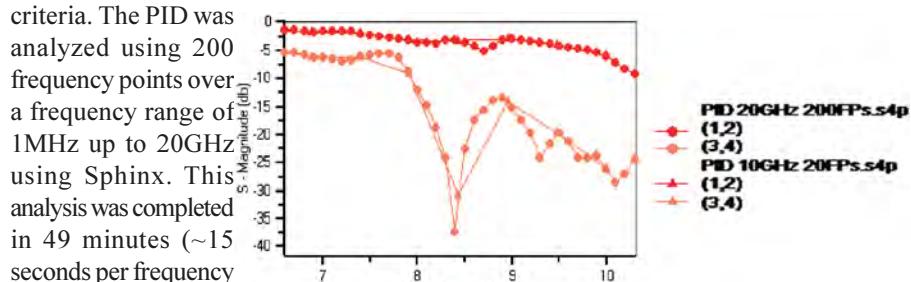


Figure 6. Reduced frequency points provides similar conclusions

performance trade-offs. The frequency response in **Figure 6** shows the PID design between 7GHz and 10GHz comparing 200 frequency points vs. only 20 frequency points over a frequency range of 10GHz. Lower than 7GHz shows

no differences and the results from 7 to 10GHz show similar results with many frequency points, which are sufficient to draw the same conclusions as described earlier.

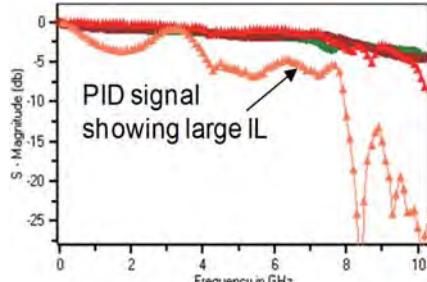


Figure 5. Insertion Loss (IL) for two signal lines for IBM package and PID

Two other key signal integrity parameters to examine are NEXT and FEXT. **Figure 7a** compares both packages for NEXT. NEXT measures the near

ZIP

High Performance Contacts

- Up to 40GHz Bandwidth

- 0.50nH Inductance

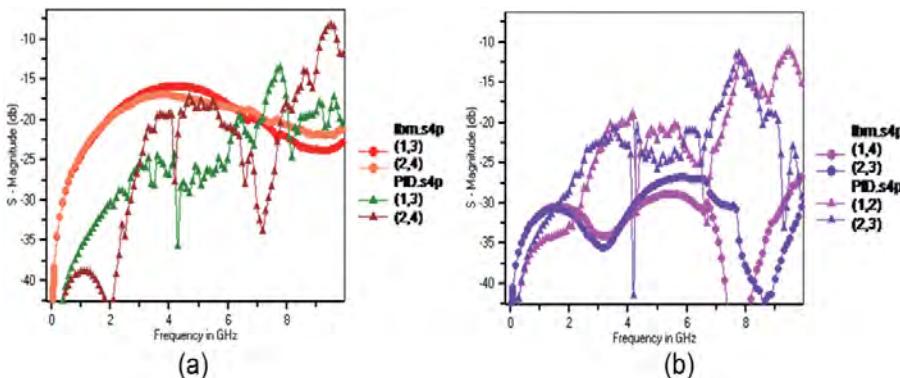


Figure 7. Comparison of IBM package and PID (a) NEXT and (b) FEXT

end cross talk and looks at coupling between the signal lines at the input and output ends (between ports 1 & 3; ports 2 & 4). As with IL, the IBM package is more consistent up to 10 GHz. Although the PID looks good up to 7 GHz, above 7GHz the cross talk exceeds that of the IBM package and reaches levels that begin to affect nearby signals, which can cause functional or performance problems. FEXT represents the coupling between the input (C4) and output (BGA) end of signal lines (between ports 1 & 4 and 2 & 3). **Figure 7b** shows the cross talk to be much higher for PID as compared to the IBM package. As with NEXT, the IBM package is more consistent up to 10GHz and at 10GHz provides -26dB of isolation. Similar to the IL and NEXT results, the PID has poor isolation above 3GHz. This once again increases the power transfer from one signal line to the other causing unwanted effects such as jitter and signal loss.

All of the PID results for IL, NEXT and FEXT were all simulated in under 5 minutes using frequency domain analysis with Sphinx. To accurately view RPD effects on signals, IL, NEXT and FEXT must all be evaluated simultaneously. As was seen with the PID design, poor signal integrity was observed at different frequencies. IL showed major problems above 4 GHz, NEXT showed issues above 7 GHz and FEXT had problems above 3 GHz. Without simulation and the assessment of signal integrity metrics for PID, a poor design could have been released into manufacturing.

Conclusion

Advancements in technologies to meet consumer's appetite for digital content

have placed a large burden on package developers. Packages and their operating frequencies create signal integrity phenomena that must account for return path discontinuities (RPDs). Designers trying to apply 'old rules' in today's demanding package environments can result in disaster. In addition, analyzing small sections of a package for IL, NEXT and FEXT can provide a false sense of security concerning the integrity of your design. Fortunately, new methods and tools have been developed to help identify RPDs and reduce BOTH the risk and time required to validate package designs for signoff. Frequency domain analysis may not be the standard method for many design teams focused on digital applications; but it is a method that requires little information and preparation which can yield big returns in a very short time period; allowing package design and verification long before silicon is available.

**A nine page white paper titled Evaluating Accuracy can be requested from E-System Design on this topic.⁵ Please send email to info@e-systemdesign.com with subject: Evaluating Accuracy. The white paper provides details on simulation method used, frequency response of the signal lines in the package, correlation to time domain measurements and IBM's laboratory measurement technique.⁶*

About Author

Madhavan Swaminathan, CTO E-System Design

He is also the Joseph M. Pettit Professor in Electronics in the School of Electrical and Computer Engineering and



Everett Charles
Technologies

A DOVER COMPANY

www.ectinfo.com/zip

909-625-9390

Patents 7,862,391, 6,462,567 and 6,396,293
and other Patents Pending

What are return path discontinuities (RPDs)?

Currents always flow in loops and follow the path of least impedance. A signal line being charged or discharged causes return currents on the planes closest to it. RPDs are physical topologies that cause return current to deviate from an optimal return path and hence worsen the signal integrity of transmission lines. These discontinuities manifest themselves as changes in impedance as a signal line traverses through a package structure. Common structures such as vias, voids, split planes and cut-outs used in all package designs cause RPDs. Typical situations such as via transitions, signal lines over apertures, or crossing split planes can cause significant signal integrity issues. RPDs are easily discovered by analyzing insertion loss or crosstalk in the frequency domain and ‘what if’ analysis can quickly determine the cause of RPDs which can be mitigated by modifying the layout. Examples of two RPDs arising in packages are shown in **Figure 1**.

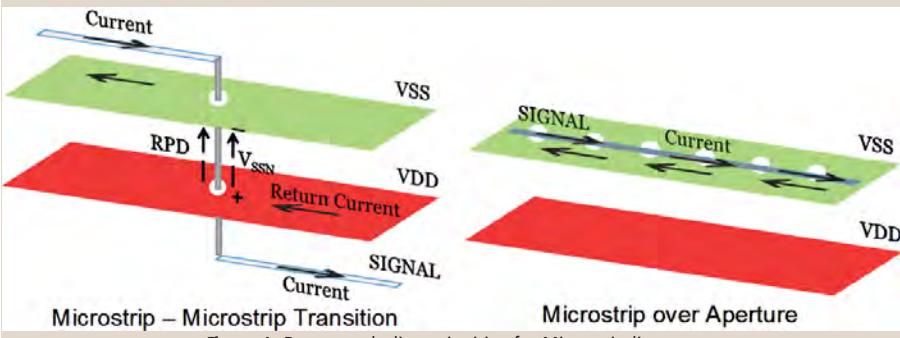


Figure 1. Return path discontinuities for Microstrip lines

Why frequency domain rather than time domain analysis?

This is not an either/or situation. Users need to perform both during their development and verification process. Frequency domain analysis allows much faster analysis, ‘what if’ scenarios, and resolution to many common SI/PI related issues. Time domain analysis requires various IBIS and Spice models, as well as simulation patterns to be created in a simulation environment. Unlike time domain, frequency domain analysis only requires the physical structure (topology and stack up parameters) and the operating frequency range; information easily obtained. The only preparation required is to place ports to excite and observe responses; a simple and fast process. Once ports have been placed, frequency domain analysis can be completed in 1-2 minutes per frequency point and this fast turnaround time enables users to quickly modify the design’s topology or stack up parameters to view the affect on SI/PI responses. Users can quickly determine if they are working on an unachievable design. Once the fast iterations result in acceptable responses, then the more complex and slower turnaround time domain analysis can be completed. This enables a significant reduction in redesigns and results in faster release to manufacturing.

Director of the Interconnect and Packaging Center, an SRC Center of Excellence @ Georgia Tech. He was the Deputy Director of the Microsystems Packaging Research Center, Georgia Tech from 2004 - 2008. He is the co-founder of Jacket Micro Devices, a leader in integrated RF modules and substrates for wireless applications and founder of E-System Design. Prior to joining Georgia Tech, he

was with IBM working on the packaging for supercomputers. He is the author of more than 300 journal and conference publications, holds 17 patents, and is the author of two books entitled “Power Integrity Modeling and Design for Semiconductors and Systems”, ISBN 0_13_615206_6. Prentice Hall, Nov 2007 and “Introduction to System on Package”, ISBN 978-0-07-145906-8, McGraw Hill,

Mar. 2008. He is an IEEE Fellow and has been recognized for his research through several awards including the 2007 Technical Excellence Award from the Semiconductor and Global Research Corporation (SRC/GRC). He received his M.S and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

Bill Martin, VP E-System Design

Bill has over 29 years of experience in consulting, product design and project management with Semiconductor and EDA companies. Prior to joining E-System Design, Bill worked at Mentor Graphics as the GM of their silicon IP Division and earlier as VP of their Mentor Consulting Division. Prior to Mentor, Bill worked at Synopsys as Director of Corporate Application Engineering releasing new products to the market. The most recognized product was PrimeTime, the de facto static timing tool for SoC/ASIC designers. Earlier in his career, Bill worked in the semiconductor industry at VLSI Technology and Mostek. While at VLSI, Bill’s last position was Director of Corporate Planning, where he coordinated all technical disciplines required by their ASIC customers. Earlier in his VLSI tenure, Bill held various field technical and management positions. Bill started his career at Mostek where he held various positions including Product Engineer and Product Engineering Manager. Bill earned an MBA from the University of Texas at Dallas, and a BS in Computer Engineering from the University of Illinois, Urbana. He has been granted 5 patents.

References

- [1] Example provided by Dr. Eric Bogatin, Bogatin Bootcamp on Differential Pairs, October 4, 2010, CA.
- [2] M. Swaminathan and E. Engin, “Power Integrity Modeling and Design for Semiconductors and Systems”, Prentice Hall ISBN-13: 978-0-13-615206-4, 2007.
- [3] Madhavan Swaminathan, Daehyun Chung, Stefano Grivet-Talocia, Krishna Bharath, Vishal Laddha, and Jianyong Xie, “Designing and Modeling for

Power Integrity”, Invited Paper, IEEE Transactions on Electromagnetic Compatibility, pp. 288 - 310, Vol. 52, No. 2, May 2010.

[4] Sphinx for Signoff, Signal and Power

(continued from Page 51)

Adhesive”, Int. Journal of Solids and Structures, vol.37, 2000

20. E.Suhir, “Probabilistic Design for Reliability”, ChipScale Reviews, vol.14, No.6, 2010

21. E.Suhir, R.Mahajan, “Are Current Qual Practices Adequate?”, Circuit Assembly, April 2011

22. E.Suhir, “Applied Probability for Engineers and Scientists”, McGraw-Hill, 1997.

23. E. Suhir, “Thermal Stress Modeling in Microelectronics and Photonics Packaging, and the Application of the Probabilistic Approach: Review and Extension”, IMAPS International Journal of Microcircuits and Electronic Packaging, vol.23, No.2, 2000

24. E. Suhir, “An Approximate Analysis of Stresses in Multilayer Elastic Thin

Films”, ASME Journal of Applied Mechanics, vol. 55, No. 3, 1988.

[5] Madhavan Swaminathan, “Evaluating Accuracy”, Application note, E-System Design, 2010.

[6] Alina Deutsch, Jason Morsey and

Christopher Surovic, “Problem Description”, provided by IBM, 2010.

[7] B. Martin, “Ports, ports, ports”, Application note, E-System Design, 2010.

29. E. Suhir, “Arrangement for Reducing Bending Stress in an Electronics Package”, U.S. Patent #6,180,241, 2001

30. E. Suhir, “Device and Method of Controlling the Bowing of a Soldered or Adhesively Bonded Assembly,” US Patent #6,239,382, 2001.

31. E. Suhir, “Bow Free Adhesively Bonded Assemblies: Predicted Stresses”, Electrotechnik & Informationstechnik, 120 (6), June 2003.

32. E. Suhir, “Optical Fiber Interconnects: Design for Reliability”, Society of Optical Engineers (SPIE), Proc. of SPIE, Vol. 7607 760717-8, 2010

33. E. Suhir, “Effect of Initial Curvature on Low Temperature Microbending in Optical Fibers”, IEEE/OSA Journal of Lightwave Technology, vol. 6, No. 8, 1988.

Be Part of the Solution...



October 16-20, 2011
Fort Worth Convention Center
Fort Worth, Texas

Where Leaders Solve 2012's Technical Challenges Today

Technical Conference

October 16-20, 2011

Solve Your Technical Challenges With
Help From the SMTA Brain Trust™

Electronics Exhibition

October 18-19, 2011

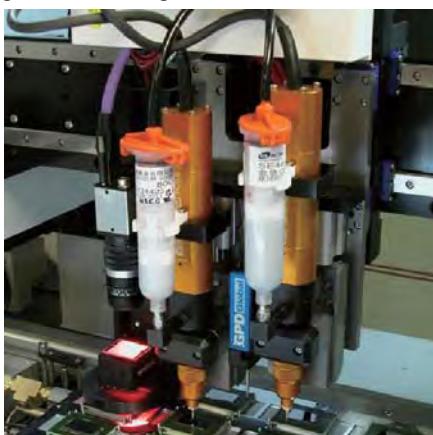
Discover the latest products and
services from leading suppliers

952.920.7682 | www.smta.org/smtai

SEMICON WEST PRODUCT PREVIEW

Positive Cavity Displacement Dispensing

GPD Global will showcase Positive Cavity Displacement (PCD), a next-generation volumetric dispensing process that delivers viscous fluids to the substrate via luer nozzles and using GPD Global 'S' Taper tips. The metering technique is not affected by variations in temperature or reservoir pressure, thereby improving day-to-day and start-to-finish process results. GPD's enhanced flow rate luer dispense tips offer higher flow rates than standard luer nozzles with a much lower pressure build-up.



PCD is compatible with materials used in electronics assembly such as epoxies, thermal greases, underfills, oils, silicones and UV encapsulants, as well as materials outside of the electronics industry. Designed for GPD Global platforms, it may be used with other robots or tabletop operations with an easy-to-use tabletop controller.

GPD will display the PCD Technology on its MAX Series platform, which offer high accuracy, precision dispensing over a wide range of applications. The MAX Series platforms are ideal for die attach, underfill, MEMS, micro-volume conductive adhesive and paste applications. North Hall, Booth #6186 [www.gpd-global.com]

Flat Technology Pogo Pins

Everett Charles Technologies' (ECT) Contact Products Group (CPG) will showcase the latest additions to its ZIP® family of flat technology Pogo® pins at SEMICON West. The ZIP® patented 2-D design features planar contact surfaces fabricated by a unique manufacturing process, delivering performance and cost advantages. It is designed to meet today's



demanding test requirements and economics. All pin products are available in ZIP® Steel, a stainless steel alloy base material to increase probe tip life. ECT personnel on hand to demonstrate the company's latest technologies and answer customer inquiries related to its new range of products. ZIP® Long-Travel Z3, developed for contacting large devices and strip tests where planarity and compliance are an issue. It is being released in .40, .50 and .80 mm version and can be supplied in different overall lengths. ZIP® SCRUB™ features a positive scrub-action pad and ball contact on lead-free plated array, and peripheral devices where solder transfer causes frequent cleaning and maintenance cycles. North Hall Booth #5670. [www.ectinfo.com]

Aqueous Cleaner for Flip Chips

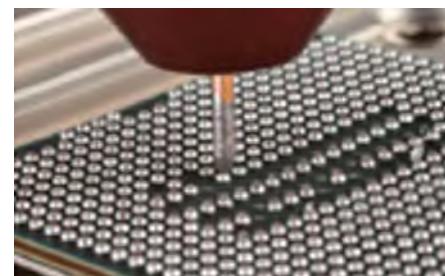
AQUANOX 4520 from Kyzen is a highly tested aqueous cleaner for flip chips and advanced packaging that is reportedly effective on all lead-free, no-clean, and eutectic materials when run at low temperatures and low concentrations. It features a long bath life, is RoHS compliant, contains no CFCs or HAPs, and is a biodegradable aqueous solution. The cleaning chemistry can clean numerous soils including lead-free flux, tacky flux, reflowed paste, no-clean flux, RMA flux, OA paste, oils, fingerprints, light oxides and polymerized soils. Easy to use, it does not require use of sump-side additives and provides brilliant joints. A4520 is suited for use in military



applications or anywhere a robust cleaner is needed for the harder to clean fluxes. North Hall, Booth #6180 [www.kyzen.com]

Bond Tester

Nordson DAGE 4000Plus features a patented hot bump/ pin pull technique for attaching a probe to solder bumps or paste and performing a pull test in accordance with the IPC standard IPC9708 pad cratering testing for surface mount and printed board assemblies. The 4000Plus HBP application is achieved by simply selecting a specialized load cartridge which can be programmed to apply a temperature-time reflow profile to individual bumps/bonds using a probe. Pre-heating, soak, rate of rise, liquidus and cooling are all integrated into the 4000Plus Paragon™ software for easy on screen profiling and control. A selection of standard probe sizes is available with custom tips



available on request. North Hall Booth # 5971 [www.nordsondage.com]

Tabletop Coating System

The ExactaCoat Tabletop Coating System from SonoTek is a fully enclosed programmable XYZ motion system for depositing uniform thin-film coatings for electronics and solar applications including photoresist deposition and various thin-film solar cell coatings. A full coating solution for R&D and low-volume production applications, the system is ideal for coating photoresist onto wafers and MEMS, or applying buffer layers for thin-film solar cells (CdS), active layers such as (CIGS, CdTe), phosphoric doping for inline diffusion, organic solar cell coatings, and fluxing of solder bus lines. The ExactaCoat can be tailored with a number of customizable options including nozzle tilt, dual nozzle, camera, laser pointer, low oxygen atmosphere, and rod coating

Exacta-Coat



attachment. Additionally, the ExactaCoat can be configured with any of Sono-Tek's precision ultrasonic atomizing nozzles to reportedly reproduce highly uniform targeted thin-film coatings with very little overspray and exceptional non-clogging repeatable performance with significant savings in spray materials, maintenance and cleanup costs. North Hall Booth #2631 [www.sono-tek.com]

Copper-Pillar Flip-Chip Flux

Copper-Pillar Flip-Chip Flux WS-641 from Indium Corp. is a water-soluble



semiconductor-grade dipping flux designed for micro-bump copper pillar attach. It is suited for 2.5D chip-on interposer, as well as chip-on-chip, or chip-on-wafer flip-chip applications. WS-641's rheology and chemistry is capable of dipping down to 40µm pitch. It has an activator system reportedly powerful enough to promote solder wetting even on mildly oxidized copper. Its cleanability in deionized water and NIA (no-intentionally-added) halogen-free nature makes it environmentally-friendly as well. Designed for standard Sn and Sn/Ag microbumps, additional benefits include uniform dipping volumes over long periods and high yields in copper pillar flip chip. North Hall Booth

6265 [www.indium.com]

Open-molded Plastic Package

OmPP from Quik-Pak includes pre-molded QFN (Quad Flat No-Lead) and



SOIC package configurations designed to provide quality, quick, and cost-effective solution for IC packaging and assembly needs. They can be used in production beyond prototype builds. Ni/Au plated QFN's come in a broad assortment of body sizes from 3x3mm to 12x12mm with pitches including 0.40mm, 0.50mm and 0.80mm. Custom designs are available. [www.delphon.com]

ARIES® test sockets: with more of what you want... and less of what you don't!



More Performance... Aries ultra high frequency sockets have a mere 1 dB signal loss at up to 40 GHz!!! Center probe and Microstrip sockets deliver more than a half million insertions with no loss of electrical performance.

More Choices... Aries offers a full range of sockets for handler-use, manual test and burn-in...for virtually every device type, including the highest density BGA and CSP packages. Choice of molded or machined sockets for center probe and Kapton interposer models, too!

Less Cost... in addition to extremely competitive initial cost, Aries replacement parts and repair costs beat the competition, assuring you of lowest total cost of ownership.

Less Wait... Aries can deliver the exact sockets you need in four weeks or less!

So why settle? Aries makes it easy to get the world's best test sockets. Call or visit our web site to find out how!

NOW AVAILABLE
for ICs Down
to 0.3mm Pitch!



ARIES®
ELECTRONICS, INC.

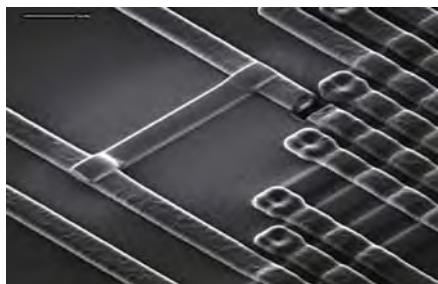
Bristol, PA 19007-6810
(215) 781-9956 fax: (215) 781-9845
e-mail: info@arieselec.com
www.arieselec.com

Sensible Solutions... Fast!

WHAT'S NEW!

Vion Plasma Focused Ion Beam

FEI's plasma focused ion beam (FIB) is industry first, offering improved speed and performance over FIBs based on gallium liquid metal ion sources (Ga-LMIS). Plasma FIB is reportedly 20 x faster than current FIBs



FIBs are used for "real work" to remove and add material in addition to forming images. It sputters away material from one area, and the ion beam will deposit on the wafer surface in a predefined location. New applications have emerged where FIB benefits are well appreciated and desired, but the Ga-LMIS based FIB is "too slow" due to larger material volumes in technologies like IC packaging intergration, 3D IC development and commercialization, through silicon vias (TSVs), bumps, wire bonds, and stacked die.

Vion™ plasma focused ion beam (PFIB) system reportedly removes material > 20 x faster than existing FIB technologies. Based on inductively coupled plasma (ICP) source technology using xenon ion beam, the maximum beam current extends to >1 μ A compared to tens of nA for Ga-LMIS. Additionally, it maintains performance at lower currents used for high-precision final cuts and high-resolution (sub-30nm) imaging. It enables the kind of structural analysis customers are used to on devices to the package level, provides faster development feedback and failure analysis; and has potential applications in material sciences and natural resources as well.

Silicon Realization Flow for ICs in Lead Frame Packages

CAD Design Software, Inc., and Cadence Design Systems have converged CAD Design's Electronics Packaging Designer (EPD) and the Cadence Design Systems Allegro IC Package design and

analysis environment to enable a silicon realization flow for ICs that reside in lead frame packages. Freescale Semiconductor is an early adopter of the converged solution and helped refine the flow.

Lead frame designs with high I/O counts require silicon realization tools that enable chip-package-board co-design, complex wirebonding with 3D design rule checks, and characterization and modeling tools. CAD Design Software integrates mechanical design packages, where a typical lead frame package is initially designed, with the Cadence Allegro IC Packaging tools where constraint-driven organic and ceramic substrate packages have typically been designed.

According to Neil Tracht, Freescale Design Manager, this collaboration makes designing complex Lead Frame packages less complex and has significantly reduced cycle time. This integration has significantly reduced our design cycle time."

Mario Rocha, CAD Design Software's Sr. Product Manager says, "CDS has worked closely with Freescale and Cadence to architect a converged solution that enhances the value of the individual tools, reduces time to market, and enhances design reliability, through the entire design flow, from intent through abstraction to convergence."

Brad Griffin, Product Management Director for the Cadence Allegro IC Packaging solutions, says, "More efficient Silicon Realization is now enabled for chips targeted for low-cost packages through this collaboration with CAD Design Software. Lead Frame packages can now be realized more efficiently using the convergence chip-package-board co-design capabilities that include sophisticated 3D visualization and wirebond rule checking."

40 GHz Bandwidth Socket

The SM-BGA-9000 socket from Ironwood Electronics is a high performance BGA socket uses a unique elastomer capable of high speed, low inductance, high endurance and wide temperature applications. It is designed for 23x23mm package size and operates at bandwidths up to 40 GHz with less than 1dB of insertion loss. The socket dissipates 4.5 watts with a



heat-sink compression screw and can be customized up to 100 watts with modified fin design and adding axial flow fan. The contact resistance is typically 15 milliohms per pin. All pins are connected with 40 GHz bandwidth on all connections. The socket is mounted on the target PCB with no soldering, and uses industry's smallest footprint (only 2.5mm more on each side). It is constructed with shoulder screw and swivel lid which incorporates a quick insertion method for rapid IC change-out. [\[ironwoodelectronics.com\]](http://ironwoodelectronics.com)

Automated Macro Inspection System

The NSX®320 Automated Macro Inspection System from Rudolph Technologies, Inc. is designed specifically for advanced packaging processes that use through silicon vias (TSV) to connect multiple die in a single package. The system also provides critical inspection capabilities for edge trimming metrology, wafer alignment during bonding processes, sawn wafers on film frames and other TSV related processes.

According to Rajiv Roy, VP business development and director of back-end marketing, the system addresses requirements defined by customers in foundries, IDMs, fabless, and equipment manufacturers. In addition to advanced speed and sensitivity, the NSX 320 System incorporates Rudolph's proprietary XSoft™ system software capabilities including high-speed staging, on-the-fly image capture and a wide range of sensor and objective options. New features engineered into the NSX 320 include the ability to perform critical dimension measurement; the addition of 3D sensors for TSV depth or bump metrology; and the ability to flip wafers to allow inspection of both front and back surfaces. Macro defects of 0.5 μ m and larger can be



created during wafer manufacturing, probing, bumping, dicing, or by general handling, and can have a major impact on the quality of a microelectronic device and the yield manufacturing process. The NSX quickly and accurately detects yield-inhibiting defects, providing quality

assurance and valuable process information. [www.rudolphtech.com]

Johnstech Opens Singapore Sales & Service Center

Johnstech International Corp. test contactor solutions provider has opened a Singapore Sales and Service Center to house field service engineering, application engineering and customer service support in Asia.

According to Dave Ruelle, director of sales and service, Singapore is significant to Johnstech and its customers for a number of reasons. "Singapore is a free trade zone, making it easy to import and export materials for our operations," he explains. "It is a central point in S.E. Asia where a large number of our customers are located. It also is a good location for tapping into an experienced workforce. This last point clearly shows in the quality of staff we were able to hire for this new office."

"As test and design markets continue to shift to Asia, we continue to adjust our

service and support to best meet our partner and customer need. Our partners include not only our distributors, but OEMs, integrators, and other value-add suppliers that work with us and our customers to provide the industry's best test solutions," says Johnstech's Founder and CEO, David Johnson.

The new Johnstech Singapore Sales & Service Center will house field service engineering, applications engineering, and customer service in support of Asia. "The new Asia Sales & Service Center in Singapore allows us to be closer to our Asian-based customers," says Gary Teh, Asia regional channel manager. "We can now respond to channel partner demands for real-time business and technical support." An open house event was held in May to honor partners and customers. The festivities included a ribbon cutting ceremony followed by a traditional Chinese Lion Dance to create an environment of luck and prosperity.

Best-in-Class Sockets

The eZ-Test™ System from Protos

**Superior Thermal Control
Sustainable High Yields
Low Insertion Cost**



Test/PoP/Burn-in Sockets • Performance Boards • Complete Interface Solutions

office (408) 492-9228 • fax (408) 330-0093 • info@protoelectronics.com
1040 Di Giulio Avenue • Suite 100 • Santa Clara, CA 95050

Protos
ELECTRONICS

INDUSTRY NEWS

SEMI High Tech U Inspires Kids to Study High Tech

Since 2001, the SEMI Foundation has been putting its money where its mouth is, heeding the cry for stimulating interest in high tech careers among the youth in the United States and abroad. They established SEMI High Tech U for the purpose of inspiring teenagers ages 14-16 to pursue their interests in science, technology, engineering and math. In 2010, 15 student programs in 5 states and 4 countries reached over 500 students. Overall, 3100 students have graduated from SEMI High Tech U's program.

In early June 2011, ON Semiconductor, ASML, Fab Owners Association, and EV Group co-sponsored the foundation's 120th program to date, which was held in Phoenix and Tempe AZ locations, exposing 43 local youth to various fields of high tech including microelectronics, engineering, nanotechnology and more. Xaxiri Yamane, project coordinator, Maricopa Advanced Technology Education Center organizes the program for Arizona on behalf of the SEMI Foundation. She explained that local high-school age youth (mostly sophomores and juniors) interested in science, technology, engineering and math (STEM) but don't quite know what they want to do are invited to participate in 3-day sessions to exposed them to what technology is all about. "We target 14-16 year olds, because it gives us the chance to influence classes they want to take." she said, adding that the only criteria is an interest in technology - there are no grade requirements. Candidates complete a two page application answering two



Figure 1. Students participate in the Human Calculator Team Challenge



Figure 2. Students conduct nanotechnology experiment



Figure 3. EVG staff explains binary addition to one student

basic questions: 1. Describe your extracurricular activities, and 2. describe your interest in high tech and reasons for applying to the program. Selections are made based on the students responses. There were 80 applicants from which the final 43 selections were made, said Yamane.

The agenda for the week was divided into 3 days; one day at ON Semiconductor was devoted to hands-on activities such as the Hacky Sack Catapult, used to demonstrate how medieval technology relates to modern day chip making in a math and statistics exercise called "Statapult". Day two was a mixture of hands-on activities and a tour of EV Group's clean room facility (**Figure 1**). Day three took the group back to ON Semiconductor for Career Day, which gave students the opportunity to learn about different career paths and college opportunities, and practice interviews.

There is no cost for attending SEMI High Tech U. Each program, which costs \$30,000 to produce, is funded entirely by the industry through corporate sponsorship.

In addition to financial support, sponsors provide volunteer instructors, class room space, and venue tours. LaVitta Cooks, Human Resources director at ON Semiconductor, said the company's motivation for sponsoring is to plan for the future of the high technology industry, to prepare our youth for the field and give them the opportunity to learn. "There's a need for this. Unless we reach out to the local community, there's going to be a shortage of local talent to draw from," she explained.



Figure 4. Students partner to perform IC experiments



Figure 5. Semi Hi Tech U Electronics lab

Steven Dwyer, Vice President and General Manager, EV Group North America concurs "SEMI's High Tech U program offers a unique opportunity for young people, who represent our future, to not only get excited about math and science, but to experience real-world applications in the high-tech industry so that they truly understand the 'why' behind learning. EV Group is thrilled to be a part of this program. We hope our participation will help to instill in students the same passion we have for technology that is critical to keep innovation in our industry moving forward."

IWLPC 2011 Program Update and Keynote Speaker Announced

The 2011 International Wafer Level Packaging Conference (IWLPC), will



take place October 3-6, 2011 in Santa Clara, CA. Final touches have been put on the program.

In addition to

a three full technology tracks and an exhibit hall, highlights include Wednesday's morning keynote delivered by Matt Nowack, of Qualcomm, who will address High Density TSV Chip Stacking: Fabless Infrastructure Status. On Thursday, John H. Lau, PhD,



Matt Nowack,
Qualcomm

Director of the Electronics and Optoelectronics Research Laboratory Industrial Technology Research Institute (ITRI), will talk about "Evolution,



John Lau, ITRI

Challenges, and Outlook of 3D Si/IC Integration".

Wednesday evening will feature an attendee reception, followed by the Keynote

Dinner Speaker Raj Master, General Manager, Microsoft Hardware Silicon, Packaging, Quality and Reliability. The title of his talk will be Thermal and Power Considerations in Electronics Packaging.

Wednesday's technology panel, *3D Infrastructure Issues for Technology Adoption*, which will discuss and evaluate the existing industry infrastructure and the technological momentum driving/regulating adoption, as well as the role of infrastructure in determining technological progress. Panelists include experts in the packaging industry, including: Jim Walker, vice president of research, Gartner Technology; Ron Leckie, Invensas, Rozalia Beica, Applied Materials, Peter Ramm, Fraunhofer Institutue, Andre Rouzaud CEA-Leti along with Jan Vardaman, president and founder, TechSearch International. The panel will



Raj Master,
Microsoft

be moderated by Simon McElrea, president, Invensas Corporation.

Thursday's panel, *Will 2.5D and 3D*

Compete or Coexist?

will look at various scenarios that could unfold in the next few years. Confirmed 3D panelists include Ron Huemoller Sr. VP of Adv 3DIC, Amkor Technology, Scott Jewler, Chief Engineering, Sales and Marketing Officer at Powertech Technology; Phil Marcoux, of PPM Associates, consultant for TSV technologies, and Rao Tummala, director, 3D Packaging Center, Georgia Tech.

Exhibitor opportunities are still available. Attendee registration will open soon. For more information, visit the IWLPC website at www.iwlpc.com.



Francoise von Trapp,
3DInCites

Elastomer High Speed Sockets

- bandwidth options to 40 GHz
- pitch down to 0.30mm
- very short current paths of 0.30mm, 0.50mm & 1.00mm
- cost effective locking systems (FastLock, QuickLock, - TwistLock, ClamShell, etc)
- interchangeable elastomer
- adaptable to existing PCB layout dimensions

Contact E-tec for more information. Special custom requirements, such as clearances in socket body, mounting configurations, stiffeners, heatsinks, etc. are welcome. Interchangeable elastomer & probe pin sockets are also available.

E-tec Interconnect Ltd
Tel: +41-21-781 08 10
Fax: +41-21-781 08 11
e-mail: info@e-tec.com
website: www.e-tec.com

USA /Canada contact:
Mr. Bud Kundich
P.O.B. 4078
Mountain View CA 94040
Tel: 408-746-2800
Fax: 408-519-6611
e-mail: info-us@e-tec.com

SRO – Solder Reflow Ovens

- Perfect reflow soldering
- Rapid thermal annealing under controlled atmosphere, vacuum and pressure
- Perfect solder joints, no voids

Also available PEO – Semiconductor Process Furnaces

U.S. and Canada Representative:
Please contact atv@pactech-usa.com or call 408-588-1925

PAC TECH USA
PACKAGING TECHNOLOGIES

www.atv-tech.de

MEPTEC & SMTA PRESENT

2011 Medical Electronics Symposium

Vital Technologies for Health

September 27 & 28 • Arizona State University • Tempe, AZ

REGISTER ONLINE TODAY AT WWW.MEPTEC.ORG

In Association With



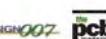
Corporate Sponsors



Association Sponsors



Media Sponsors



ADVERTISER INDEX

Amkor Technology	www.amkor.com	11
Aries Electronics	www.arieselec.com	59
ASE	www.aseglobal.com	15
Az Tech Direct	www.aztechdirect.com	32
Contech Solutions	www.contechsolutions.com	43
DL Technology	www.dltechnology.com	18
ECD	www.ecd.com	45
Essai	www.essai.com	OBC
E-tec Interconnect	www.e-tec.com	63
Everett Charles Technologies	www.ectinfo.com/zip	51,53,55
EV Group	www.evgroup.com	12
GPD Global	www.gpd-global.com	19
Hanmi Semiconductor	www.hanmisemi.com	2-3
Indium Corp	www.indium.us/E107	17
IWLPC	www.iwlpc.com	40
Kyzen	www.kyzen.com	4
Meptec	www.meptec.org	64
Micro Control Company	www.microcontrol.com	1
Multitest	www.multitest.com	48,49
Nanium S.A.	www.nanium.com	13
Newport	www.newport.com/bond1	IFC
Nordson Dage	www.nordsondage.com	23
Pac Tech USA	www.pactech-usa.com	25,63
Piper Plastics	www.piperplastics.com	38
Plastronics	www.H-Pins.com	29
Powertech Technology	www.pti.com.tw	9
Protos Electronics	www.protoelectronics.com	61
Quik-Pak	www.icproto.com	5
RTI	www.testfixtures.com	21
SEMI	www.semi.org/events	44
Sensata	www.qinex.com	7
SER Corp	www.ser.co.jp	27
SMTA	www.smta.org/smtai	57
STS	www.sts-usa.com	31

ADVERTISING SALES

Western USA, Europe

Kim Newman *Chip Scale Review*
[knewman@chipscalereview.com]

P.O. Box 9522 San Jose, CA 95157-0522

T: 408.429.8585 F: 408.429.8605

Mountain and Central USA, Europe

Ron Molnar *AZ Tech Direct*
[rmolnar@chipscalereview.com]

13801 S. 32nd Place Phoenix, AZ 85044

T: 480.215.2654 F: 480.496.9451

Eastern USA

Ron Friedman [rfriedman@chipscalereview.com]
P.O. Box 370183, W. Hartford, CT 06137

T: 860.523.1105 F: 860.232.8337



IDI WORLD CLASS TESTING SOLUTIONS

SYNERGETIX + ANTARES : PUT THE IDI CONNECTION TO THE TEST

When two of the most innovative test socket product lines were connected by Interconnect Devices, Inc., the world's most comprehensive package test offering emerged – providing you solutions for virtually any lab, system level or ATE requirement. And a global network of Manufacturing, Design Engineering, Application Engineering and Sales support throughout the U.S., Europe and Asia now guarantees that we can help you around the clock – and around the world. Put IDI to the test today.

1.913.342.5544 : www.idinet.com

smiths

bringing technology to life

IDI is a Smiths company. To learn more visit www.smithsinterconnect.com

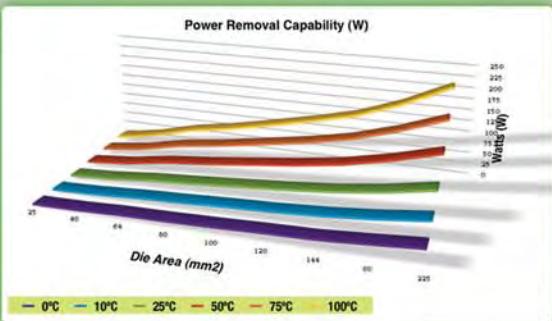
introducing

Advanced Thermal Management

...it's elemental



Essai's New Generation Thermal Management Systems Offer Performance & Versatility for I.C. Temperature Testing



Highly efficient thermal response with Thermo-Electric Cooler, Liquid & Heater assist based technologies

Distributed force loading between the Die & Substrate that prevents silicon cracking while maintaining proper thermal contact

Smaller footprint that can fit in various applications – manual or automated System Level & Final Test handlers

Integrated vacuum pickup designed for handler applications

Cold test capable with efficient condensation abatement features

Available for **wide range of packages**: Bare Die, Lidded, Thin Core, and Ultra Small Form Factor devices

essai
www.essai.com