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Volume 22, Number 3

The Future of Semiconductor Packaging

May • June 2018

Creating 1µm RDL structures for FOWLP

Page 7

- Sequential-3D integration
- Sub-micron die placement
- Thermal cycling of IC devices
- 8 ways to make RDLs for FOW/PLP
- Biodegradable and recyclable materials
- Challenges of flip-chip MEMS microphones

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Advanced packaging techniques like FOWLP demand mature lithography solutions for the challenging processes required to manufacture high-performance devices. The Veeco-Ulitech AP3000®, which was used for the research in the featured article, has a variable numerical aperture lens that can be optimized to maximize depth of focus while maintaining higher resolution performance. It can process wafers with up to 7mm of warpage and is configurable with an optical system that provides a full wafer topography map to help optimize the focus position for each exposure.

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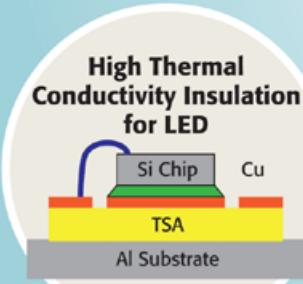
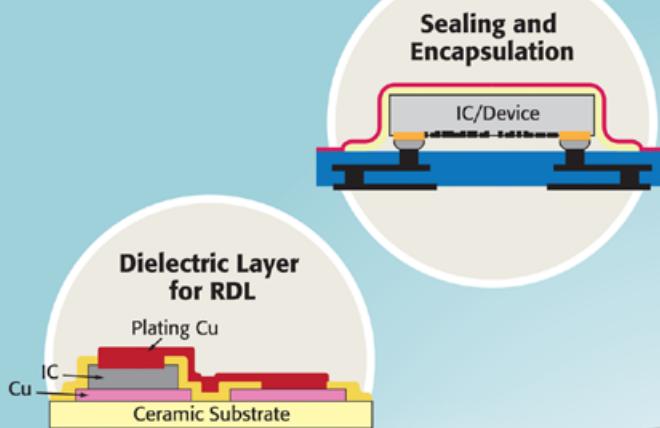
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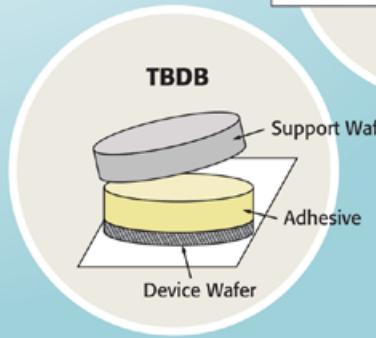
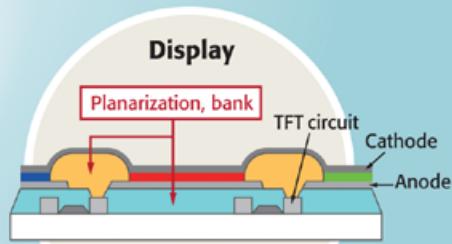
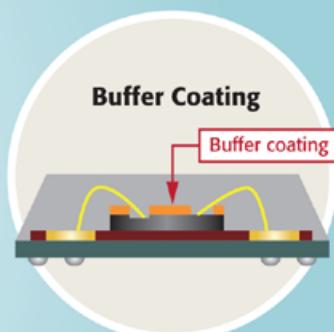
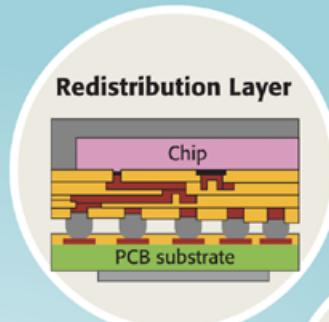
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Creating 1µm RDL structures for fan-out wafer-level packaging

By Warren W. Flack [Veeco Instruments Inc.] and John Slabbekoorn [imec]

Consumer demand for mobile electronic products with superior performance, enhanced features and thinner profiles is driving growth in the semiconductor industry. Advanced packaging plays a critical role in delivering the required form factor and electrical, thermal, and power consumption improvements essential for next-generation semiconductor devices.

In particular, fan-out wafer-level package (FOWLP) technology has seen rapid adoption due to its inherent advantages compared to 3D packaging techniques. Originally developed for small- to mid-size packages [1], FOWLP has also been adapted to meet increasingly stringent packaging requirements for larger semiconductor chips, such as applications processors [2].

Redistribution layers (RDLs) are used to route the very high-density connections on the chip to the much lower density connections of the substrate. High-density FOWLP requires multiple RDL levels to match the line density of the chip, which raises the cost of the total package. Decreasing the metal linewidth supports reducing the number of RDL levels, and thereby lowers the overall packaging cost.

Reducing RDL critical dimension (CD) and pitch is also necessary to enable design flexibility while improving electrical performance [2]. These developments create challenges for a number of processes including lithography, electroplating and seed layer etch [3].

This article investigates methods to image and maintain the integrity of 1.0µm RDL structures using a through-resist electroplating process. Electrical performance of the 1.0µm RDL process was validated using meandercomb-based electrical test structures. (A meandercomb is a

long resistor line interlaced between two lines that are not connected to the resistor.) The results indicated excellent electrical yield for 1.0µm line/space (L/S) test structures.

Lithography characterization

The lithography system used for this study is an Ultratech (a division of Veeco) 300E 1X stepper that supports broad exposure with g-, h- and i-lines of mercury (Hg) arc lamp and a variable numerical aperture (NA) lens from 0.16 to 0.22. For this experiment, the exposure was narrowed to i-line (Hg), and the lens NA was set at 0.20 to enable 1.0µm-resolution L/S imaging. The tool was also equipped with both a wafer edge exposure (WEE) unit, enabling precise removal of photoresist on the edge of the wafer where electrical contact is required during electroplating, and a wafer edge protection (WEP) unit. The WEP blocks exposure and is used to retain photoresist inside the WEE ring, preventing plating solution leakage during the electroplating step.

For lithography process set up, a resolution test reticle was used to facilitate testing across a range of CDs for L/S and contact patterns. The L/S and contacts were arranged to support cross-sectional analysis. Photoresist coating was on 300mm copper (Cu) seed layer wafers; the chemically amplified positive photoresist used for this study was 3µm thick and required a post-exposure bake. Development was performed in standard tetramethylammonium hydroxide (TMAH).

A focus/exposure matrix (FEM) was performed to determine the nominal exposure dose and focus using

the reticle. In the FEM wafer layout, a 13-column by 17-row array of fields was exposed, with focus varying in the horizontal axis and exposure varying in the vertical axis. This allowed a wide range of lithography conditions to be evaluated on a single wafer.

The scanning electron microscope (SEM) data from the FEM wafers for a 1.0µm L/S feature is presented in the Bossung curve format shown in **Figure 1** [4]. This format allows quick visual appreciation of the data and enables further processing with curve fitting and process window analysis. The photoresist's isofocal bias of about +0.15µm for the space width CD is advantageous in compensating for the subsequent Cu seed etch process. With this bias, the depth of focus (DOF) was 7.5µm at a dose of 150mJ/cm². At the nominal exposure dose of 150mJ/cm², the CD uniformity was 4% across the 7.5µm DOF.

Test lot fabrication

For process development of multilayer RDL, a mask set was designed to study feature sizes ranging from 1.0µm to

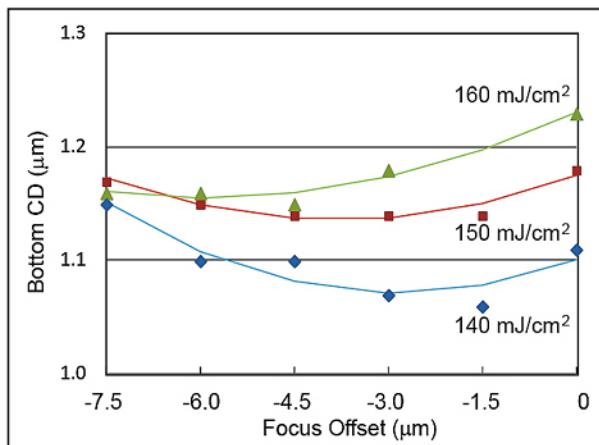


Figure 1: Bossung plot for 1.0µm L/S in 3.0µm thick positive chemically amplified photoresist on Cu seed. The measured space CD is plotted against the focus offset (µm), with data points having the same exposure energy (mJ/cm²) plotted on one curve.

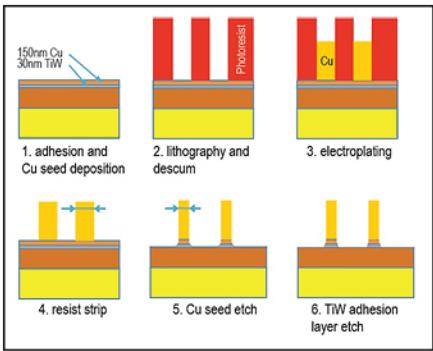


Figure 2: Fabrication steps for the semi-additive process flow. The resulting meandercomb structures are tested for electrical shorts and resistance.

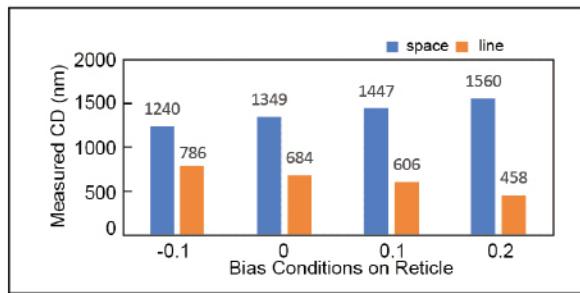


Figure 3: Comparison of the measured CD for $1.0\mu\text{m}$ L/S after lithography as a function of the bias applied to the reticle. The photoresist space bias increases from left to right. Standard deviation is about 50nm.

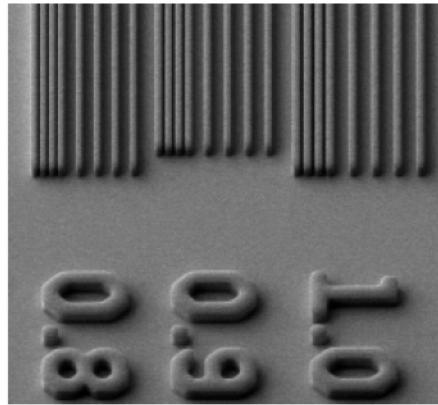


Figure 4: Dense line and space CD resolution structures after electroplating and photoresist strip.

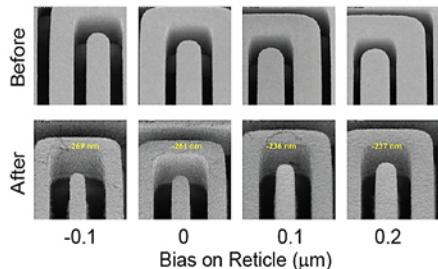


Figure 5: Comparison of the before and after Cu seed etch for $2.4\mu\text{m}$ thick electroplated $1.0\mu\text{m}$ L/S meandercomb test structures. The photoresist space bias increases from left to right.

$5.0\mu\text{m}$, containing a variety of structures useful for studying different properties. Examples include meandercomb structures for investigating line fidelity, daisy chain for via fidelity, coplanar waveguides and microstrip for RF properties, and line and planar capacitance structures for reliability. A complete set of L/S structures ranging from $0.8\mu\text{m}$ to $5.0\mu\text{m}$ were also included to monitor lithographic performance.

This experiment focused on performance of a single metal layer with a $1.0\mu\text{m}$ CD. In leakage current mode, voltage was applied to one of the meandercomb resistor line ends, while both leakage test fingers were connected to ground, so that any leakage between the resistor line and the fingers would result in a measured current. In resistor mode, a voltage was applied over the resistor, with the resulting current indicating the thickness and effective width of the resistor line.

Figure 2 shows the fabrication process sequence as a semi-additive flow. The process of record (POR) designed for $2.0\mu\text{m}$ and larger features provided the starting point for process optimization. All experiments were performed on 300mm wafers deposited with 30nm titanium tungsten (TiW) and 150nm Cu as seed for electrochemical deposition.

The Cu seed wafers were exposed at 150mJ/cm^2 , i-line wavelength, and $-3.5\mu\text{m}$ focus offset. Cross-sectional SEM measurements for both vertical and horizontal $1\mu\text{m}$ L/S were measured at multiple locations across the wafer to verify CD uniformity. The sidewall profile is near vertical throughout the DOF. The average space width was $1.145\mu\text{m}$ with σ of $0.017\mu\text{m}$. The resulting photoresist trenches were partially filled by electrochemical deposition (ECD) of Cu. Finally, a wet process sequence consisting of resist strip, Cu seed removal and TiW removal was performed and the resulting meandercomb structures were tested for shorts and resistance.

To investigate the effect of lithography and plating on the seed-etch, variation in CD was introduced by duplicating the meandercomb structure with different nominal sizes and bias on the reticle. Selected CDs were 1.0, 1.6, 2.0, 3.0, 4.0

and $5.0\mu\text{m}$. Applied bias was -0.1 , 0 , $+0.1$ and $+0.2\mu\text{m}$, affecting the space width in positive resist. Experimental splits included two nominal plating thicknesses: $1.2\mu\text{m}$ and $2.4\mu\text{m}$. Based on initial testing, seed-etch times were varied to optimize the process yield.

Results and assessment

After lithography, the CDs for $1.0\mu\text{m}$ L/S at 23 locations on the wafer were measured. The results are summarized in **Figure 3**. The biasing increment of 100nm is clearly seen in the CD data trend. (Note that the space width in resist will become the Cu line width after electroplating.) The photoresist displays excellent resolution, while resist lines as small as 400nm are retained with good definition.

After electroplating and photoresist strip, the dense CD line and space resolution structures were evaluated. Structures with CD down to $0.8\mu\text{m}$ are well defined in $2.4\mu\text{m}$ thick electroplated Cu (see **Figure 4**). The Cu seed etch also etches the plated Cu and therefore has a significant effect on Cu linewidth. **Figure 5** shows SEM photos of the $1.0\mu\text{m}$ L/S meandercomb structures before and after Cu seed etch with different reticle biases. For the POR etch time, the CD loss is on the order of 250nm. For the images shown in the figure, no residues remain between the Cu lines of the meandercomb structures. However, on other wafer locations there are some residues that will lead to electrical-test shorts.

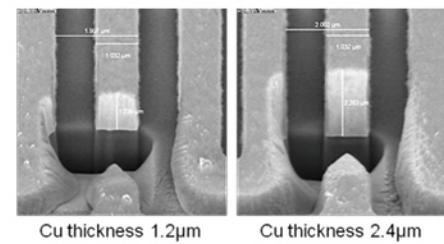


Figure 6: Focused ion beam (FIB) cross-sections of $1.0\mu\text{m}$ L/S meandercomb test structure after Cu seed etch for two electroplating thicknesses.

Figure 6 shows typical focused ion beam (FIB) cross-sections of $1.0\mu\text{m}$ L/S pattern after seed etch for the two electroplating thicknesses. The CD after seed etch is close to nominal, and the images show fine straight profiles without undercut. The observed thicknesses are close to the predicted values.

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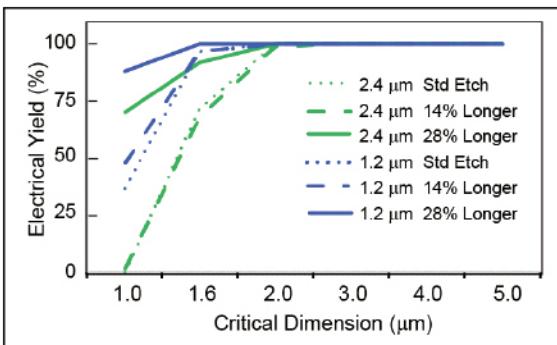


Figure 7: Electrical yield versus the meandercomb CD. The yield data is highest for the 1.2μm thick Cu electroplating and the longest over-etch.

Figure 7 summarizes electrical yield data for all CDs and process conditions. For both Cu thicknesses and using the POR etch time, 100% yield was obtained for all structures of 2μm and larger. The yield drops for 1.6μm and is then dependent on Cu thickness and Cu etch time. The effectiveness of the Cu etch chemistry is reduced by the narrow and relatively deep trenches in which it has to remove the Cu seed. To a certain extent, this can be overcome

by extending the Cu etch times. There is a limit, however, to the amount of Cu etching that can be performed because extra etching will result in smaller Cu lines. Below a certain width, the line fidelity will be affected by lifting Cu lines and broken connections.

For the 1.0μm L/S meandercomb structure, 100% yield can be achieved for 1.2μm Cu thickness, smaller biases and a 28% longer seed etch. However, this result comes at a relatively large loss in CD of approximately 530nm at a 28% longer etch. To maximize the robustness of the Cu line, the remaining CD after seed etch must be as large as possible. For this condition, 100% yield is obtained at a maximum CD of 800nm. Taking into account the 530nm CD loss for Cu seed etch, this means that the post-lithography linewidth must be approximately 1350nm.

Summary

Future high-performance devices will require RDL linewidths of 2μm or below. To image these smaller linewidths, the lithography process window must have a large depth of focus in order to accommodate the chip height variation after chip placement on the reconstituted wafer. The challenge is that depth of focus decreases when the NA of the exposure tool is increased to image the smaller line sizes.

To investigate the viability and advantages of reducing RDL CD and pitch in FOWLP technology, 1.0μm L/S Cu lines for fine-pitch RDL integration schemes were fabricated and tested electrically. Lithography gave excellent CD uniformity and reproducible results. For 1.0μm L/S features, a depth of focus of 7.5μm was measured; with the space bias adjustable in the mask to accommodate etch process requirements. Resist lines of 500nm and smaller could be defined in a 2.0μm pitch, indicating that the lithography process has room for further scaling.

Another important finding is that 100% yield of 1.0μm L/S meandercomb structures can be obtained with reduced Cu thickness of 1.2μm and a 28% longer seed etch, compared to the POR etch used for 2.0μm and larger features. To maintain the maximum DOF of 7.5μm in the current lithography process, a mask bias of 0 to 100nm would optimize the structure for Cu etch.

Acknowledgment

Elements of this article appeared in the paper, “One Micron Redistribution for Fan-Out Wafer Level Packaging,” originally distributed at the Electronics Packaging Technology Conference in Singapore, December 6-9, 2017.

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Biographies

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8 ways to make RDLs for FOW/PLP

By John H. Lau [ASM Pacific Technology Ltd.]

Redistribution layers (RDLs) [1-2] are the most integral part of wafer-level packaging (WLP). In this study, various methods for the fabrication of RDLs for fan-out wafer/panel-level packaging (FOW/PLP) are presented. Emphasis is placed on four different methods in making the RDLs for FOWLP, and the other four for FOPLP. Some recommendations are also provided. Finally, the critical issues of panel-level technology are presented.

FOWLP RDL methods

As noted in the introduction, there are four methods for making RDLs used in FOWLP. This section discusses them.

FOWLP RDLs by polymer and ECD Cu + etching. This is the oldest method to make RDLs for fan-in WLP—for examples, see [3,4]. The RDL consists of two layers, the dielectric layer and the Cu conducting layer. The dielectric layer is made of a polymer, e.g., polyimide (PI), benzocyclobutene (BCB), or polybenzobisoxazole (PBO) and the conductor layer is made by electrochemical deposition (ECD) of Cu and etching. The key process steps are described as follows: 1) First, spin coat a polymer on the whole wafer; 2) That step is followed by spin coating a photoresist; 3) Then the photoresist is opened with a mask aligner or stepper. 4) The polymer is then etched, and the resist is stripped off; 5) Next, the adhesive/seed layer (Ti/Cu) is sputtered using physical vapor deposition (PVD); 6) The photoresist is then spin coated, and then the photoresist is opened with a mask aligner or stepper; and 7) Next comes electroplating the Cu. After the resist is stripped off and the TiCu is etched off, we have the first RDL. If one repeats the processes, you get the other RDLs. For example, Figure 1 shows the schematic of the chip and the RDL, the PCB assembly, and the cross section of the fan-in WLP [3]. Today, most outsourced semiconductor assembly and test suppliers (OSATS) use this method to make RDLs for FOWLP with chip-first and chip-last processing.

FOWLP RDLs by photosensitive polymer and ECD Cu + etching. A

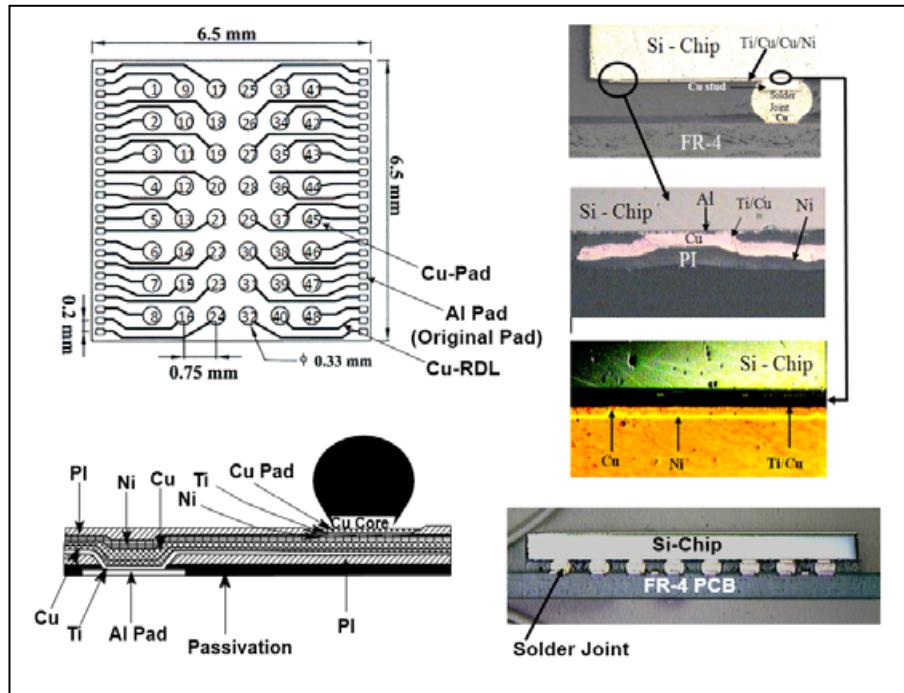


Figure 1: Fan-in WLP.

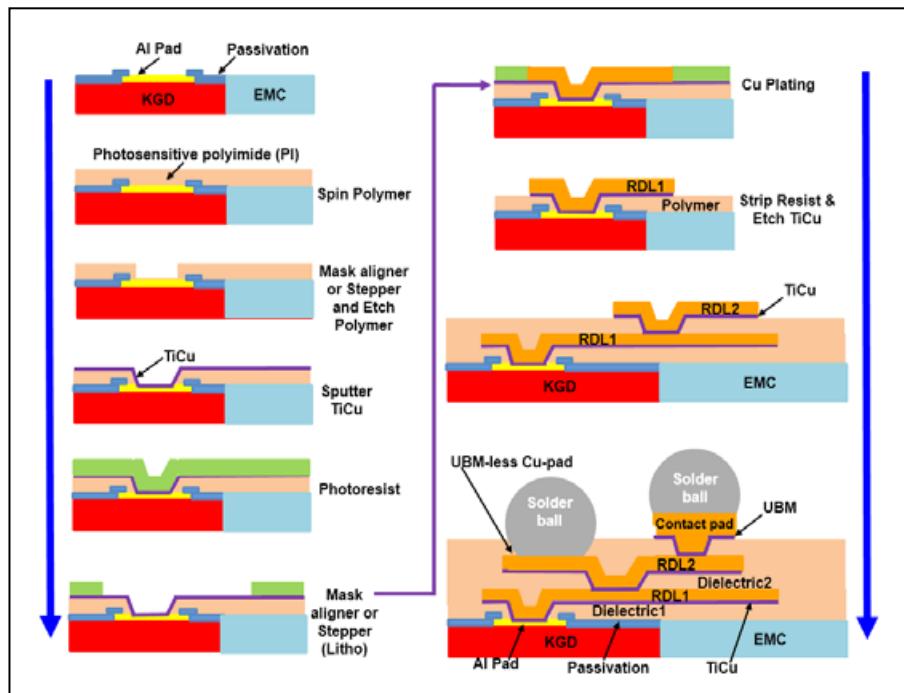


Figure 2: FOWLP RDLs process flow using photosensitive polymer and ECD Cu + etching.

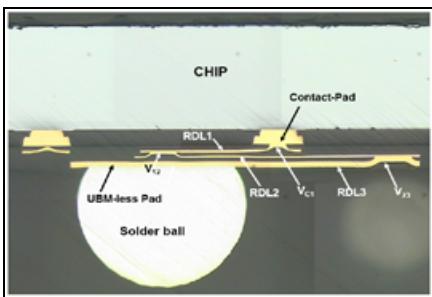


Figure 3: Cross section of FOWLP RDLs using photosensitive polymer and ECD Cu + etching.

better and simpler process is shown in **Figure 2** [5]. It can be seen that for the PI (polyimide) development, the whole reconstituted wafer is spin-coated with a photosensitive PI. It is followed by applying a stepper and then using photolithography techniques to align, expose, and develop the vias of the PI. Finally, the PI is cured at 200°C for one hour—this will form a 5μm-thick PI layer. It is followed by sputtering Ti and Cu by PVD at 175°C over the entire reconstituted wafer. Then, apply a photoresist and a stepper and use photolithography techniques to open the redistribution trace's locations. Next, electroplate the Cu by ECD at room temperature on the Ti/Cu in the photoresist openings. These steps are followed by stripping off the photoresist and etching off the Ti/Cu; RDL1 is thereby obtained. Finally, repeat all the above steps to obtain other RDLs. **Figure 3** shows the cross section of a FOWLP with 2 RDLs. This can be used for FOWLP with chip-first and chip-last processing. The RDLs made by the polymer (either photosensitive or not) and ECD Cu + etching are called organic RDLs.

FOWLP RDLs by PECVD and Cu-Damascene + CMP. This is the oldest back-end semiconductor process. This process uses SiO₂ or SiN for the dielectric layer and ECD to deposit the Cu on the whole wafer. That is followed by using CMP to remove the overburden Cu and seed layer to make the Cu conductor layer of the RDLs. The key process steps are shown in **Figure 4**. First, use PECVD to form a thin layer of SiO₂ (or SiN) on a full thickness bare silicon wafer and then use a spin coater to laminate the photoresist. These steps are followed by using a stepper to open the resist and a reactive ion etch (RIE) to remove the SiO₂. Then, a stepper is used

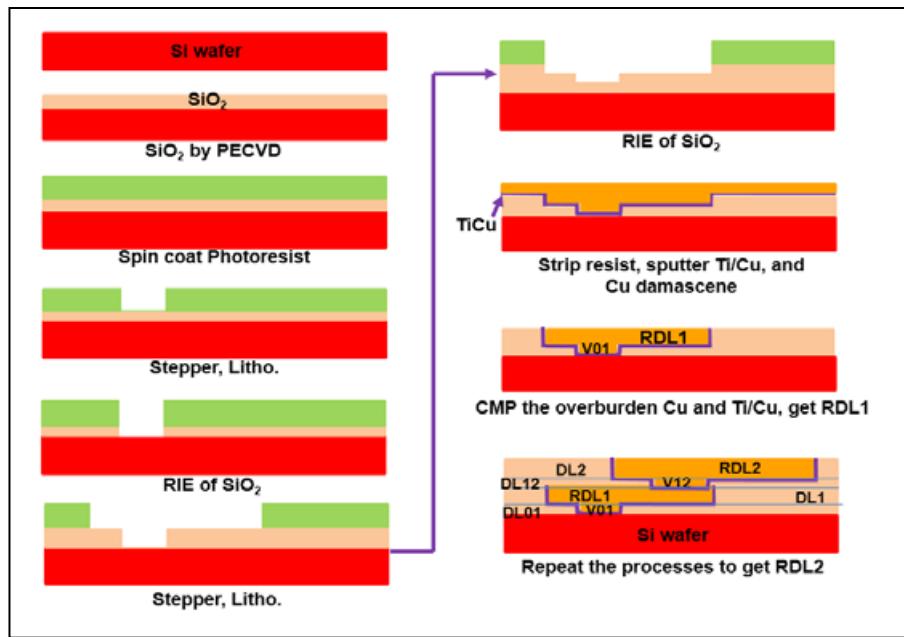


Figure 4: FOWLP RDLs process flow using PECVD and Cu-damascene + CMP.

to open the resist wider and RIE to etch more of the SiO₂. Next, strip off the resist, sputter the TiCu, and ECD the Cu on the whole wafer. These steps are followed by CMP to remove the overburden Cu and the TiCu, and then we have the first RDL1 and V01 (the via connecting the Si and RDL1) as shown in **Figure 5** [2]. This is called the dual Cu-damascene method [2]. Finally, repeat all the processes to get the other RDLs. This method can be

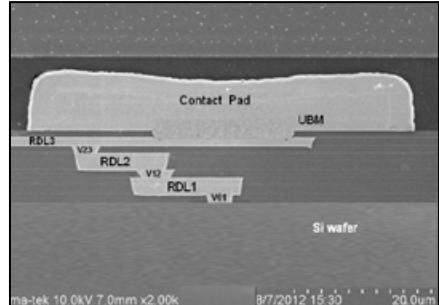


Figure 5: Cross section of RDLs using PECVD and Cu-damascene + CMP.

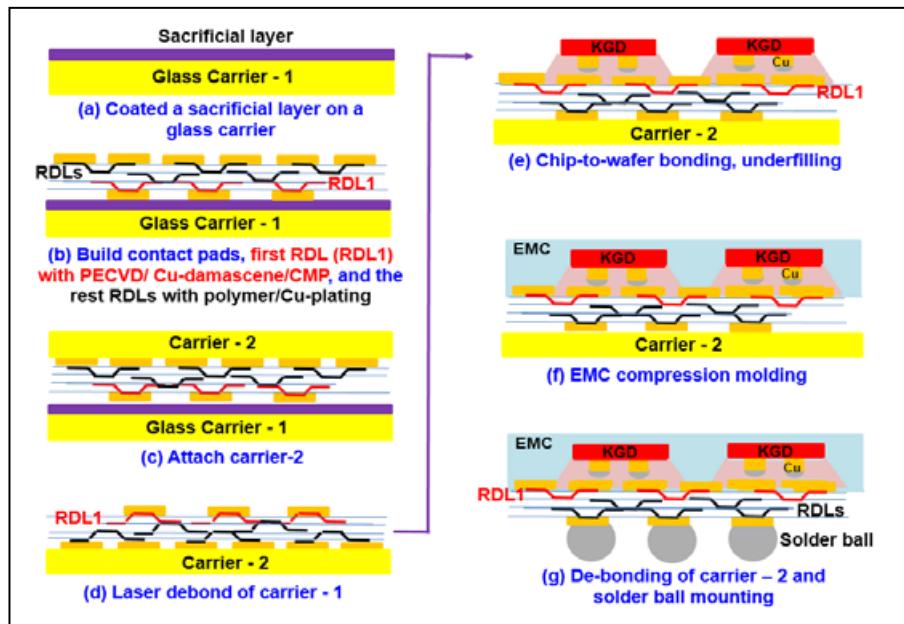


Figure 6: FOWLP RDLs process flow for hybrid-RDLs.

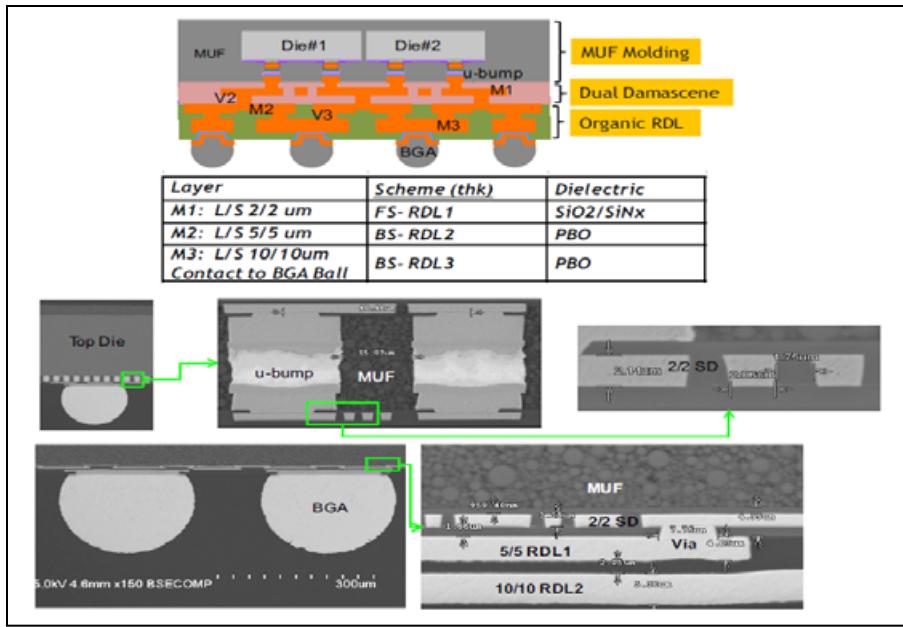


Figure 7: SPIL's cross sections of hybrid RDLs.

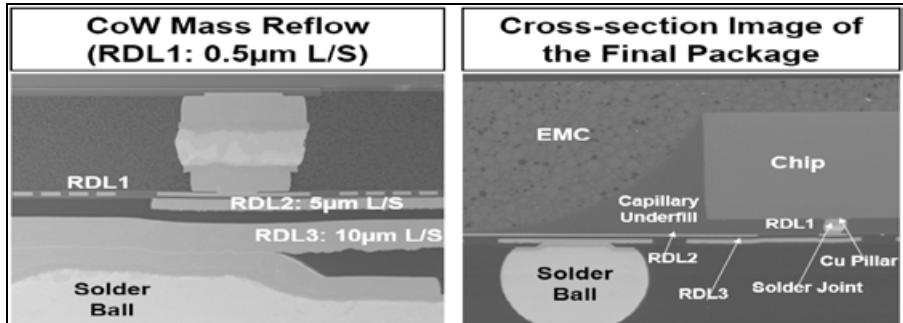


Figure 8: Amkor's cross sections of hybrid RDLs.

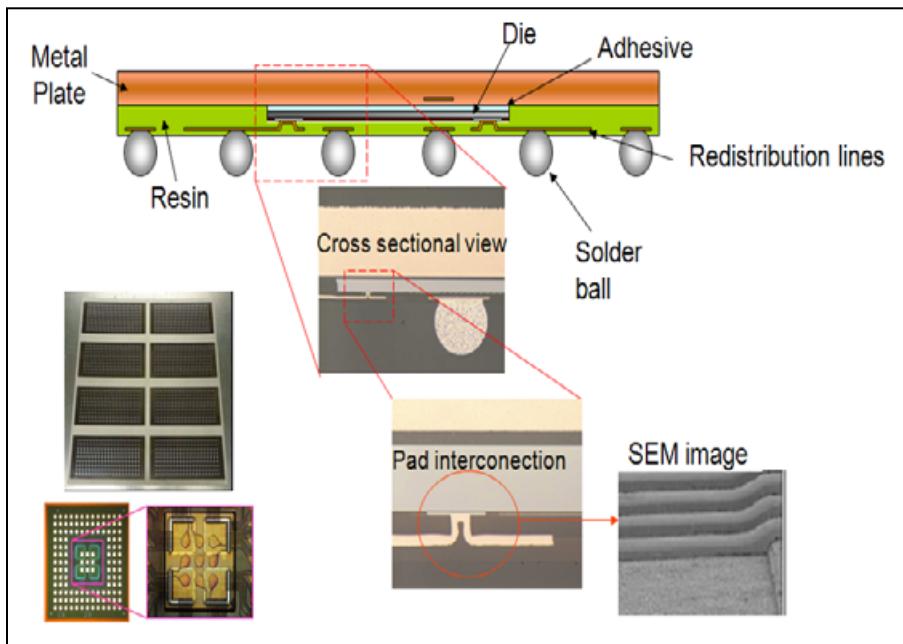


Figure 9: J-Devices' WFOP.

applied to FOWLP with chip-first and chip-last processing. The RDLs made by PECVD and Cu-damascene + CMP are called inorganic RDLs.

FOWLP RDLs by hybrid-RDL. As of today, this hybrid-RDL method only applies to chip-last or RDL-first, i.e., wafer bumping and chip-to-wafer bonding are necessary. The key process steps for chip-last by hybrid RDLs are shown in **Figure 6**. It can be seen that a glass carrier-1 is coated with a sacrificial layer (**Figure 6a**). The contact pad and the first RDL (RDL1) are then fabricated by the PECVD for the SiO₂ dielectric layer and dual Cu-damascene + CMP for the conductor layer (**Figure 6b**). The remaining RDLs are fabricated by the ordinary polymer (or photosensitive polymer) and Cu-plating + etching method. Another carrier-2 is then attached to the other side of the reconstituted wafer (**Figure 6c**). That step is followed by debonding of the carrier-1 as shown in **Figure 6d**. That, in turn, is followed by fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing as shown in **Figure 6e**. Then, the reconstituted wafer is molded with EMC (epoxy molding compound) by the compression method (**Figure 6f**). Next comes debonding of the carrier-2 and solder ball mounting as shown in **Figure 6g**. **Figure 7** shows the cross section of a FOWLP with hybrid RDLs published by SPIL in ECTC2016 [6]. **Figure 8** shows the cross section of a FOWLP with hybrid RDLs published by Amkor in ECTC2017 [7,8]. The two cross sections are very similar.

FOPLP RDL methods

There are also four methods for fabricating RDLs used in FOPLP; they are discussed below.

FOPLP RDLs by PCB + SAP. The structure of J-Devices' WFOP™ is shown in **Figure 9**. It can be seen that there is not an EMC. However, there is a metal plate to support the whole package. The RDLs are fabricated by a printed circuit board (PCB) technology using a semi-additive process (SAP) [9-11]. First, the KGD is placed face-up with adhesive on a metal panel carrier (320mm x 320mm) (**Figure 10**). Then, photosensitive resin is coated (as the dielectric layer of the RDL) on top of the KGDs on the whole panel. This is followed by

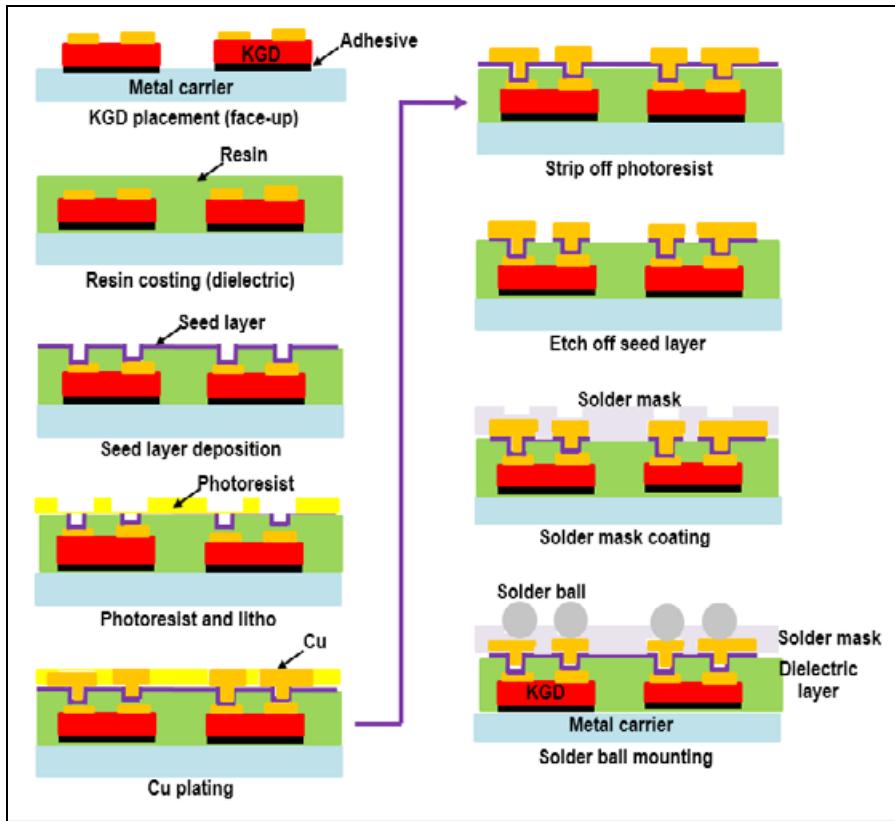


Figure 10: J-Devices' WFOP process flow.

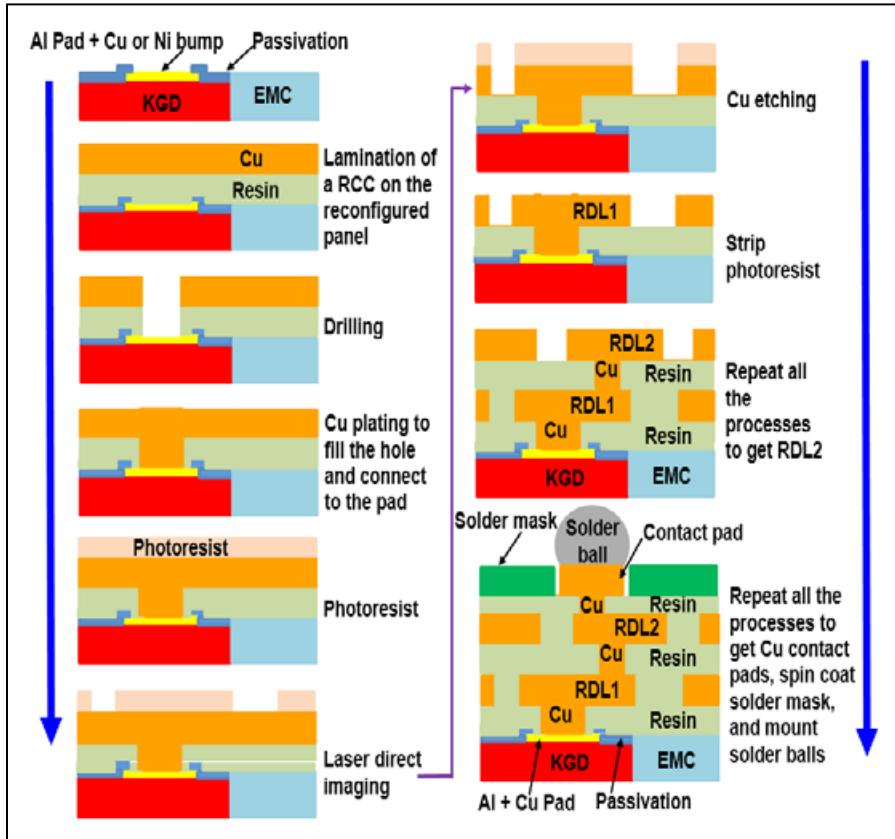


Figure 11: Fraunhofer's FOLP process flow.

exposing and developing the opens of the KGD's window and direct current (DC) sputtering a seed layer for Cu plating. Next comes the application (coat) of a photoresist and then pattern the redistributed interconnections by photolithography techniques. Then, Cu-plating, photoresist stripping, and seed layer etching are done. Those steps are followed by solder mask coating, contact pad patterning, surface finishing, and solder ball mounting. Then, the panel and resin (dielectric) layer are diced into individual units (packages) (Figure 9). Basically, J-Devices' (20 μ m linewidth and spacing) RDLs are fabricated by a PCB technology and SAP [9-11].

FOLP RDLs by PCB + LDI. Fraunhofer's FOLP key process steps are very similar to the embedded wafer-level ball grid array (eWLB) technology proposed by Infineon. However, Fraunhofer's RDL key process steps are different [12-14]. The Fraunhofer process begins with laminating a resin coated copper (RCC) on the reconstituted panel (610mm x 457mm) (Figure 11). Then, a mechanical or laser drill is used to make holes in the RCC. That process is followed by PCB Cu plating to fill the holes and connect to the Al or Cu pads. Next, a dry-film photoresist is laminated, and then an LDI is used to remove the resist. Next comes accomplishing Cu etching and stripping off the resist. Fraunhofer then has the first RDL1 and can repeat all the processes to get the other RDLs. The final RDL can be used as a contact pad. The next processes include lamination, photolithography, and curing of the solder mask (in either a solder mask defined or a non-solder mask defined format) before mounting the solder balls. Figure 12a shows the 610mm x 457mm panel and Figure 12b shows the x-ray image of the 8mm x 8mm package, which is housing two chips with dimensions of 2mm x 3mm. Basically, Fraunhofer's RDLs are fabricated by a PCB and LDI technology [12-14].

FOLP RDLs by PCB + TFT-LCD. Based on a PCB technology, TFT-LCD (thin-film transistor liquid-crystal display) 2.5G (generation) technology (panel dimensions = 370mm x 470mm), and backend technology, SPIL developed its P-FO technology [15,16]. The chip is

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embedded in a dry film and currently, there is only one layer of RDL. The key process steps in making the P-FO package are as follows. First, an adhesive on top of a glass panel carrier-1 is applied (**Figure 13a**). The next step is to pick and place the known good dies (KGDs) face-down on the glass carrier-1 (**Figure 13b**). PCB technology is then used to laminate a dry film on top of the whole panel as shown in **Figure 13c**. It is followed by attaching another carrier-2 on the other side of the reconstituted panel and debonding the glass carrier-1 as shown in **Figure 13d**. Then, TFT-LCD 2.5G processing technology is used to fabricate the RDL on top of the Al or Cu contact pads and dry film (**Figure 13e**). It is followed by solder ball mounting (**Figure 13f**) and dicing of the reconstituted panel as shown in **Figure 13g**. A test package (9mm x 9mm) that has an embedded chip (6mm x 6mm) with only one-RDL has been demonstrated and is shown in **Figure 14**.

FOPLP RDLs by PCB/ABF/SAP + LDI. The dielectric and conductor layers of the RDLs fabricated by the Fraunhofer RCC method are too thick. **Figure 15** shows a new process flow for fabricating the RDLs on a 340mm x 340mm panel published in [17]. It starts off by laminating an Ajinomoto build-up film (ABF) on the reconstituted EMC molded panel. It is followed by laser drilling and electroless Cu seed layer plating as shown in **Figure 15**. Then, follow those steps with dry-film lamination, LDI lithography, dry film developing, and PCB Cu plating for RDL1. Follow those steps with stripping off the dry film and etching off the seed layer. These steps are then repeated to get the other RDLs. The final RDL can be used as a contact pad. The next steps are laminating, photolithography, and curing the solder mask (in either a solder mask defined, or a non-solder mask defined format) before mounting the solder balls. In this case, the dielectric layer thickness can be as little as 10 μ m and the conductor layer thickness can be as little as 5 μ m. **Figure 16** shows the panel (340mm x 340mm) and the package (10mm x 10mm) with four chips, and the cross section of the PCB assembly of a package made by the presented method, where RDL1 and RDL2 are shown.

Summary

Eight methods for fabricating RDLs for FOW/PLP have been presented. Some important results and recommendations are summarized as follows:

- For the four methods, namely a) polymer and ECD Cu + etching, b) photosensitive polymer and ECD Cu + etching, c) PECVD and Cu-damascene + CMP, and d) hybrid RDL, in fabricating the RDLs for FOWLP, the photosensitive polymer and ECD Cu + etching is recommended.
- By viewing the change of the line width and spacing (from 5 μ m to 10 μ m) of the RDLs of the application processor chipsets (from A10 of iPhone 7 to A11 of iPhone 8), the chance of using PECVD and Cu-

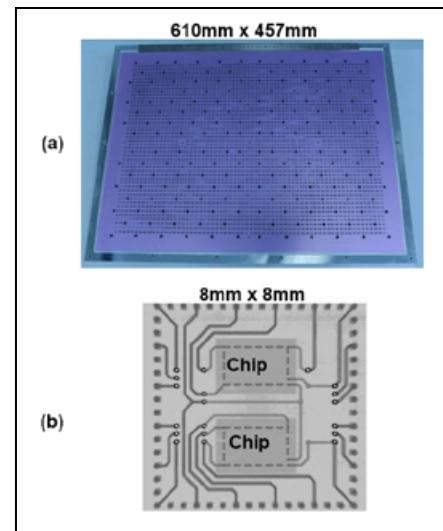


Figure 12: Fraunhofer's panel and package.

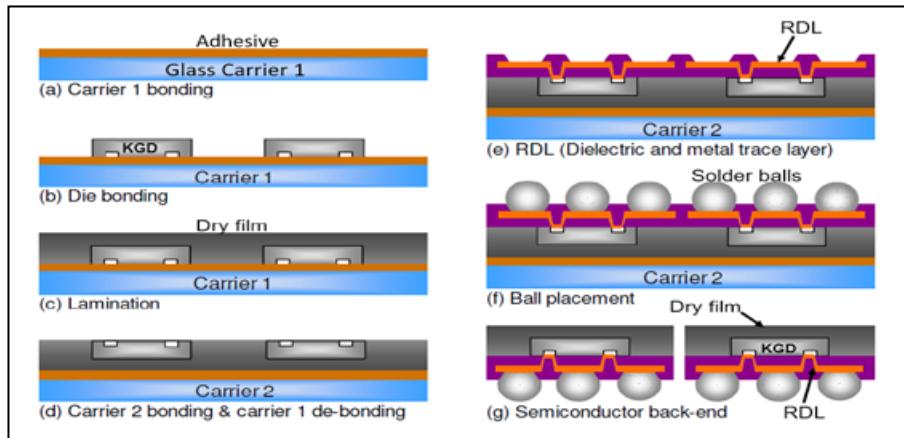


Figure 13: SPIL's P-FO process flow.

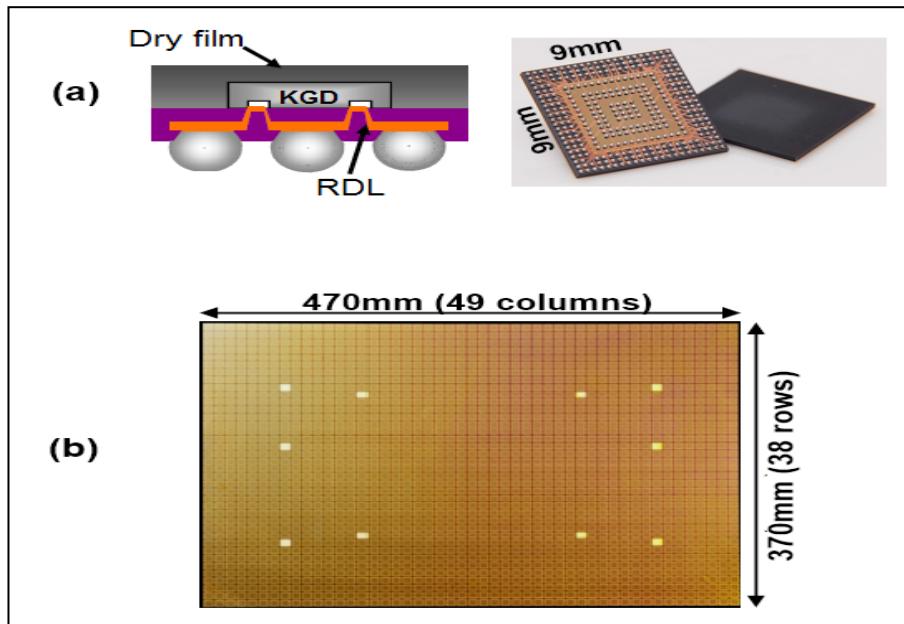
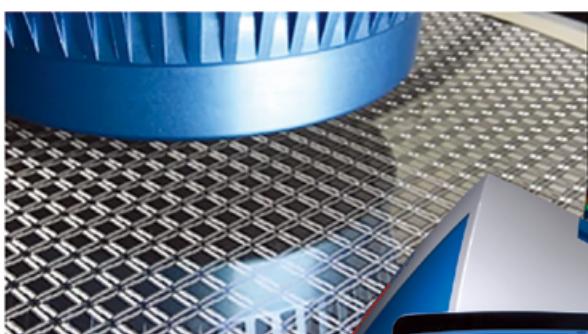


Figure 14: SPIL's panel and package.

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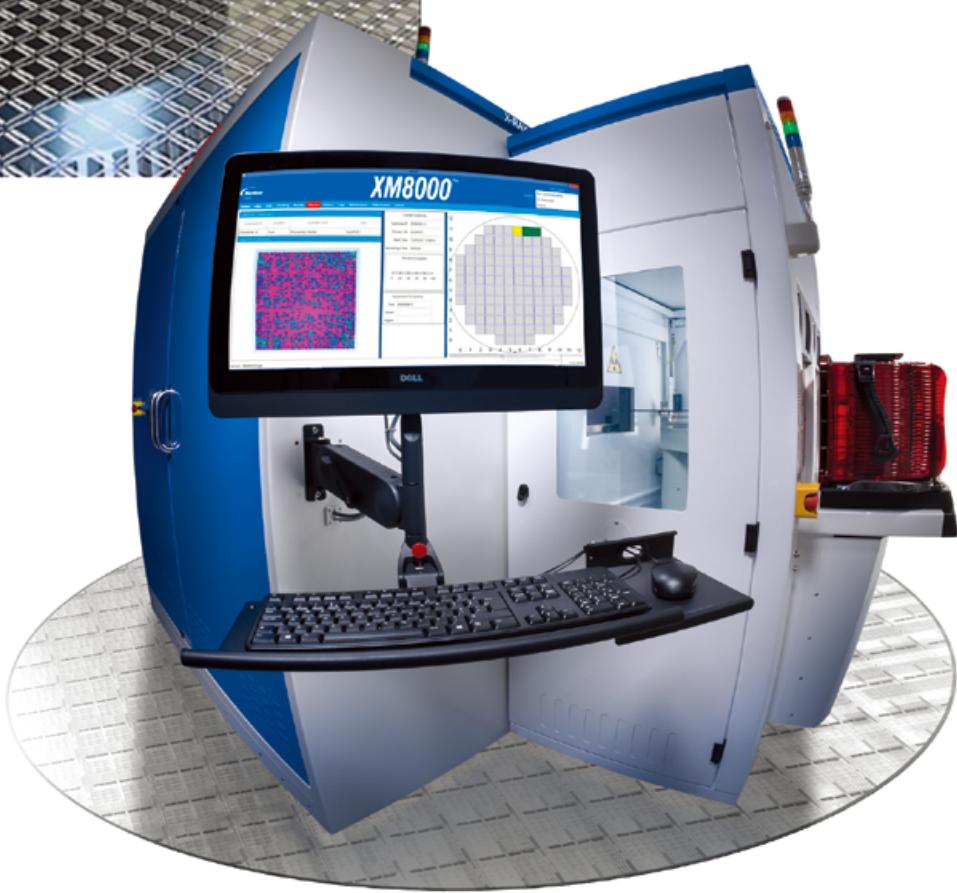
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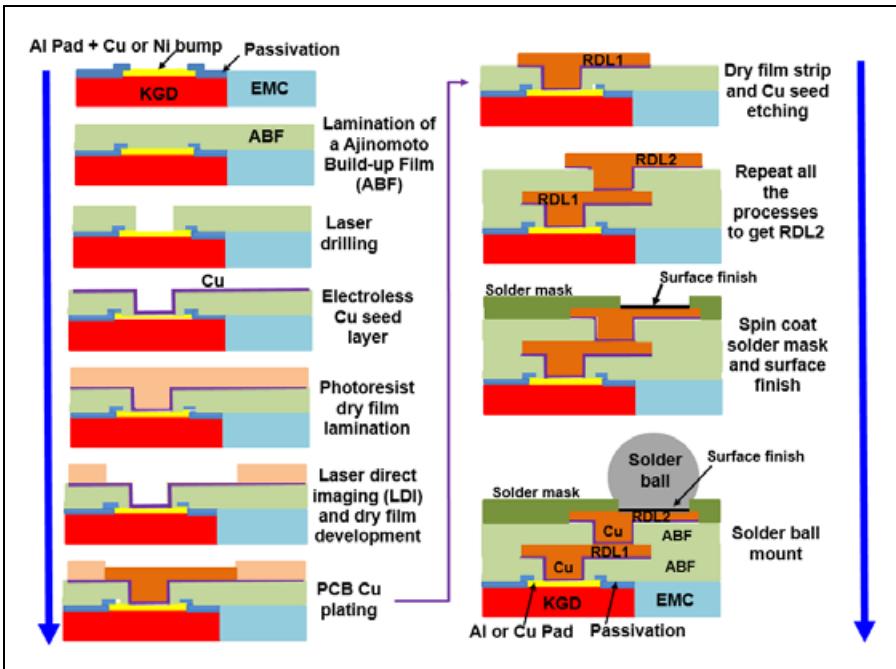


Figure 15: FOPLP process flow by PCB/ABF/SAP + LDI.

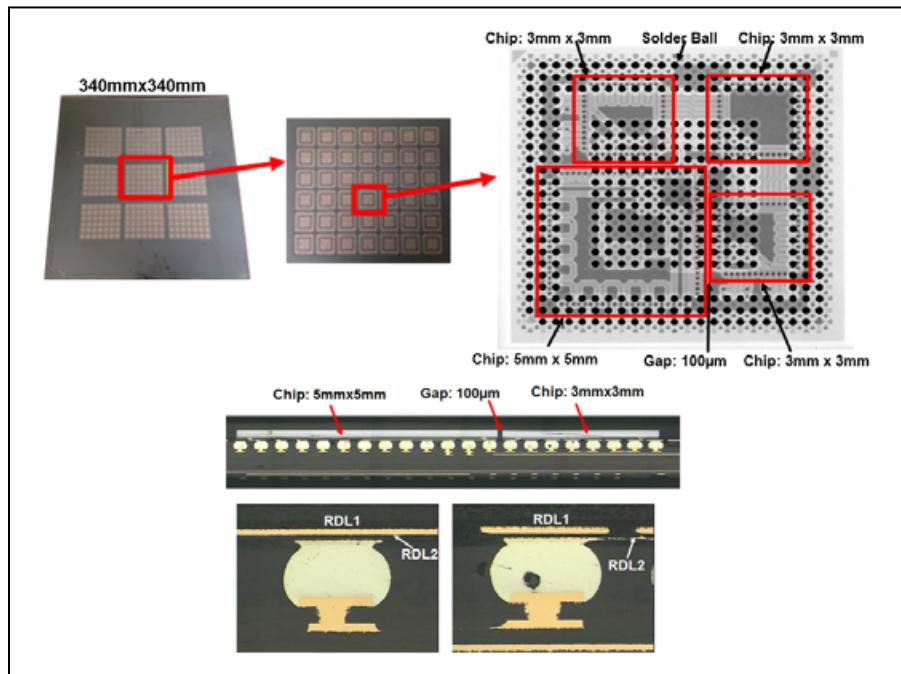


Figure 16: Panel size, individual package, and PCB assembly of the FOPLP PCB/ABF/SAP + LDI.

damascene + CMP in fabricating the RDLs for FOWLP is very slim (may be only for niche applications). Also, it is very expensive and can only be afforded by very-high density and performance applications. On the other hand, for high-density and high-performance applications, why insist on the FOWLP technology because there are many packaging alternatives?

- For the four methods, namely a) PCB + SAP, b) PCB + LDI, c) PCB + TFT-LCD, and d) PCB/ABF/SAP + LDI used in fabricating RDLs for FOPLP, the PCB/ABF/SAP + LDI is recommended.
- Theoretically speaking, FOPLP will potentially increase throughput and reduce cost. However, in order to achieve these goals, the following issues [18,19] for FOPLP need to be noted and/or resolved:

- Most OSATS and foundries already have the necessary equipment for FOWLP. For FOPLP, new capital will have to be expended on newly developed equipment.
- Inspection of wafers is a well-known process. FOPLP inspection must be developed.
- The yield of FOWLP is higher than that of FOPLP (assuming the size of the panel is larger than that of the wafer).
- The cost advantages of panel over wafer need to be carefully determined. (Yes, the throughput is higher, but the pick & place and EMC dispensing times are longer, and the yield is lower.)
- A fully loaded high-yield wafer line might be cheaper than a partially loaded low-yield panel line.
- The panel equipment takes longer to clean than wafer equipment.
- Unlike FOWLP, FOPLP is for medium chip size and linewidth and spacing.
- If indeed, the panel processing is developed and is high yield for fine linewidth and spacing, there is a chance to produce a major oversupply of capacity.
- IP, materials background, equipment automation, and management of the dimensional stability and yield of the panel in a large format are needed.
- The lack of a panel standard for FOPLP means equipment suppliers cannot make the equipment.

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Biography

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A closer look into sub-micron die placement: Cpk and Cmk

By David R. Halk [ASM AMICRA Microtechnologies GmbH]

Placement accuracy is one of the most critical process parameters to obtain and to maintain in the photonics assembly industry. For a well-informed buyer and user of die bonding equipment, it is important to be familiar with the terms Cpk and Cmk and their significance, especially when selecting an automated tool for a bonding process that requires sub-micron placement accuracy.

Die bonding, or die attach, is an essential part of the assembly process, where electronic components, in their rawest form (semiconductor die), are picked and placed onto a substrate medium held temporarily in place by a semi-liquid material (epoxy or solder). In other words, die bonding plays a major role in the “level one” assembly process. The die must be positioned accurately in a repeatable position to establish interconnect with the package substrate.

As interconnect dimensions are getting smaller and smaller, die bonders’ placement accuracy and repeatability are forced to obey ever tighter limits, pushing placement requirements to sub-micron levels. In some cases, the die attach machine must bond the die held in place during the heating process.

The engine of a photonic integrated circuit (PIC) is based on light generated by a laser. Here the die attach machine is required to bond the laser, typically using an in situ AuSn eutectic bonding process. The goal is to direct the emitted light into the PIC’s waveguide, which is a very small opening etched into the silicon sub-mount or substrate.

Definition and significance of Cmk and Cpk

The objective of this article is to show how Cmk data is used in selecting a die bonder that requires sub-micron placement accuracy, with the following considerations:

- How is Cpk/Cmk calculated and what are the constituents of Cpk?
- How does Cpk apply to first-pass yield and PPM?
- How can the photonics assembler apply Cpk to critical processes?

Cmk, or machine capability index, is an effective measure to quantify a die bonder’s

placement capabilities. To understand the importance of Cmk, we will first cover the more popular process capability indices, Cp and Cpk, which serve as useful tools in gaining insight on how to improve first-pass yield throughout the assembly line.

Cpk, or process capability, compares the upper and lower specification limits (USL, LSL) to the output deviation of a process. This comparison is made by forming the ratio of the required process specification or limits to the measured process values, as indicated by standard deviation, or sigma [1].

Cpk, therefore, is a capability index that assesses how close the measured process mean (average) is to the specification limits (USL, LSL). If the process is under control and the distribution of the measured data is well within the specification limits, the difference between USL and mean (or the difference between LSL and mean) should be >3 sigma, or 3 standard deviations. If Cpk is >1 , the process mean is sufficiently far from the specification limit [1].

Calculation of Cp and Cpk [2]

$$Cpk \text{ (upper)} = \frac{USL - Xmean}{3 * \text{Sigma}}$$

$$Cpk \text{ (lower)} = \frac{Xmean - LSL}{3 * \text{Sigma}}$$

where:

$$Cpk = \min(Cpk \text{ upper}, Cpk \text{ lower})$$

USL = upper specification limit

LSL = lower specification limit

X = mean (average)

σ (sigma) = standard deviation (Std)

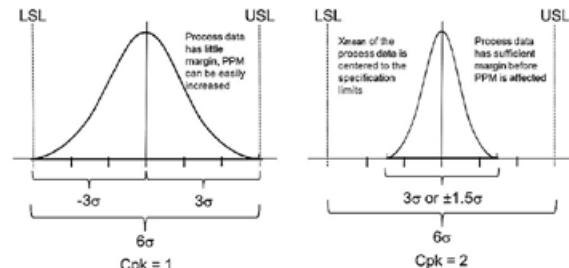


Figure 1: Cpk diagrams where a) Cpk = 1; and b) Cpk = 2.

The theoretically achievable repeatability of a die bonder is difficult to measure or estimate. There are several factors that must be considered, such as: the sub-pixel grey-level vision system, the vision alignment algorithm, linear encoder quadrature, optical resolution, etc. Figures 1a and 1b show these values and their interrelations as a Cpk diagram.

Popular example of managing Cpk

To get an idea how Cpk influences a specific industrial process such as photonics placement, let’s take a look at a familiar daily routine such as navigating a car though a narrow garage door as shown in Figure 2.

The garage opening illustrates, or defines, the specification limits of a process and the position of the parked car represents the output of the process. If the width of the car is just a bit narrower than the opening, you better park it right in the middle (which is the center of the specification) if you want to get all of the car into the garage. If the car is wider than the opening, it does not matter if you have it centered, it won’t fit anyway. If the car is 2X narrower than the opening (six sigma process), it doesn’t matter if you park it exactly centered. It will fit and you have plenty of room on either side.

What the above discussion illustrates is that if you operate a process that is in full control and shows little variation, you should be able to meet customer requirements (i.e., to park the car easily within the garage). Cpk indicates the relationship between the size of the car, the

size of the garage opening and how far away from the center line the car was parked.

Consider another analogy: playing a game of darts, also shown in **Figure 2**. The rings of the dart board define how far the landed darts are from the bulls-eye. A good player consistently achieves a tightly placed group of landed darts as shown in **Figure 2b**. With a small offset adjustment, this player can zero in on the bulls-eye – this situation is shown in **Figure 2a** – as compared to an inexperienced player (**Figure 2d**). Clearly visible is that the inexperienced player has no distinct pattern, with a few darts even thrown outside the boundaries. What this illustrates is that the inexperienced player needs to work on the repeatability or standard deviation (Std) of the process. Once he or she gains an acceptable repeatability, one can work on moving the pattern centered on another target. In other words, one needs to adjust the overall offset or improve the accuracy.

The discussion points above also hold true for a die bonder. Fundamentally, the goal of a traditional epoxy die bonder is to establish a repeatable placement process around the initially taught die position. Next, the bonding process needs to be optimized by bonding a few dies to the substrate. In terms of Cpk, repeatability of the die placement process translates to a smaller standard deviation.

There are several parameters, process adjustments and external factors of influence that affect the placement outcome: epoxy consistency, bond force, parallelism between bonding tool and bond pedestal, substrate flatness, quality of the alignment features, etc. This is why a Cpk >1 is required for a process to be sustainable over time, as shown in **Figure 1b**. Once the placement process is stable, the operator can adjust the overall die position (placement offset) to get a best fit of all the wire bond pads. This is usually done by centering the die to the bond pad of the substrate, which translates to the accuracy or system resolution of the die bonder, increasing the Cpk value as shown in **Figure 1a**.

Another definition of Cpk

Another definition of process capability, or Cpk, is derived from a method or tool to measure the confidence level of a process. With most assembly processes there are many variables that can affect the outcome. To help ensure that the process results stay within the specification limits, it is best to provide a sufficient margin between the process results and the specification limits. It is therefore imperative to be aware of all key process variables that can affect the

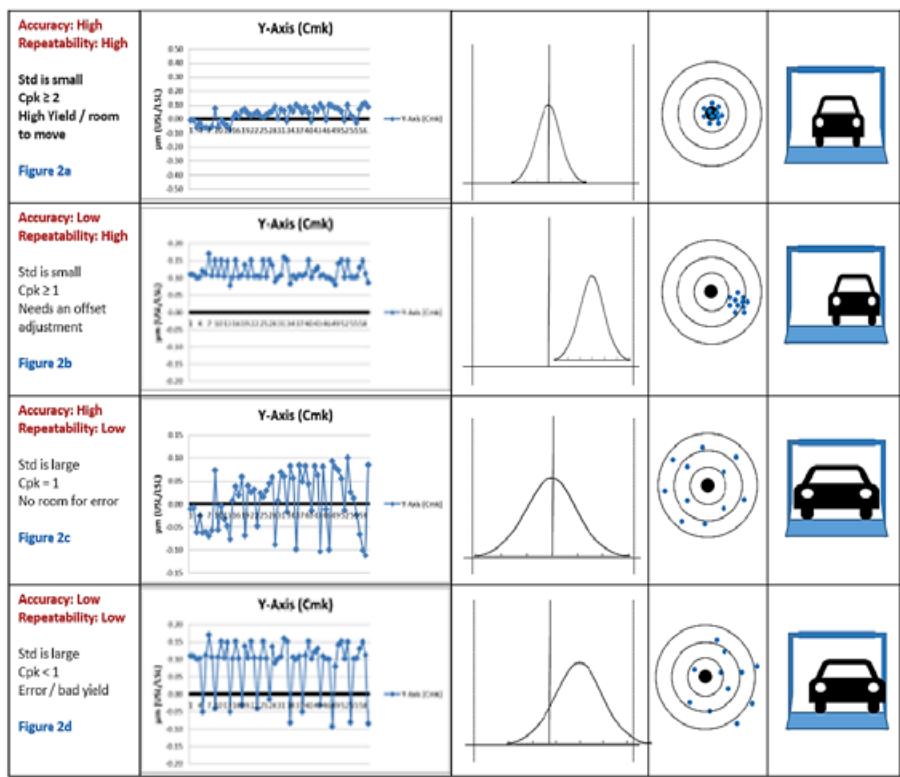


Figure 2: Popular examples of Cpk variations.

| PPM / SIGMA / Cpk Conversion Table | | | |
|--|-------------------------------|---------------------------------|------|
| RECALL: PPM may or may not = DPMO. Only if each part has one defect type will they be the same value. If one PART has >1 defect opportunity then these values can be drastically different. | | | |
| *Converting to Cpk from a sigma level is an estimation since Cpk uses the USL or LSL, whichever is closest to the process mean. The opposite side that is not accounted for may have a tail that is unaccounted for. | | | |
| SIGMA LIMITS (long-term) | % POPULATION WITHIN LIMITS | PPM DEFECTIVE OUTSIDE LIMITS | Cpk* |
| +/- .6745 Sigma | 50.00% | 500,000 | |
| +/- 1.00 Sigma | 68.27% | 317,300 | 0.33 |
| +/- 2.00 Sigma | 95.45% | 45,500 | 0.67 |
| +/- 2.36 Sigma | 98.00% | 20,000 | 0.79 |
| +/- 3.00 Sigma | 99.73% | 2,700 | 1.00 |
| +/- 3.12 Sigma | 99.82% | 1,800 | 1.04 |
| +/- 3.19 Sigma | 99.86% | 1,400 | 1.06 |
| +/- 3.23 Sigma | 99.88% | 1,200 | 1.08 |
| +/- 3.29 Sigma | 99.90% | 1,000 | 1.10 |
| +/- 3.35 Sigma | 99.92% | 800 | 1.12 |
| +/- 3.54 Sigma | 99.96% | 400 | 1.18 |
| +/- 3.71 Sigma | 99.98% | 200 | 1.24 |
| +/- 3.89 Sigma | 99.99% | 100 | 1.30 |
| +/- 4.00 Sigma | 99.9937% | 63 | 1.33 |
| +/- 4.26 Sigma | 99.9980% | 20 | 1.42 |
| +/- 4.42 Sigma | 99.9990% | 10 | 1.47 |
| +/- 4.50 Sigma | 99.99966% | 3.4 | 1.50 |
| +/- 4.75 Sigma | 99.9998% | 2 | 1.58 |
| +/- 4.89 Sigma | 99.9999% | 1 | 1.63 |
| +/- 5.00 Sigma | 99.99994% | 0.6 | 1.67 |
| +/- 5.20 Sigma | 99.99998% | 0.2 | 1.73 |
| +/- 5.32 Sigma | 99.99999% | 0.1 | 1.77 |
| +/- 5.61 Sigma | 99.999998% | 0.02 | 1.87 |
| +/- 5.73 Sigma | 99.999999% | 0.01 | 1.91 |
| +/- 6.00 Sigma | 99.9999998% | 0.002 | 2.00 |

Reference: <http://www.six-sigma-material.com>

Table 1: PPM/sigma/Cpk conversion table [3].

result or outcome, such as: 1) Material, 2) Method/process, 3) Operator, 4) Machine/tool, 5) Management, 6) Environment, and 7) Measurement. To manage these variables well, it will be helpful to maintain a Cpk value >1 .

What is Motorola Six Sigma?

Motorola Six Sigma ($Cpk = 2$) denotes an in-depth management strategy based on a continuous improvement process, this continuous improvement process is beyond the scope of this article. Simply put, Motorola Six Sigma is allotting ± 1.5 sigma to the process data while adding another margin of ± 1.5 sigma to allow for process variables that will inevitably affect the process and/or increase the standard deviation. This additional ± 1.5 sigma will help ensure a minimum parts-per-million (PPM) loss in an ever changing production environment (Figure 1a and 1b).

Table 1 shows the relationship between sigma, yield loss (PPM) and Cpk. As the standard deviation of the placement population decreases, the number of placements falling outside of the USL, and the LSL is reduced. Assuming that

placement data is centered around zero, the Cpk value will increase, which results in a more confident process even when materials might change, or a different operator is assigned. In reference to **Figure 1a**, assuming that the USL and LSL are set to $\pm 0.5\mu m$, this graph represents a process with a $Cpk = 1$. Therefore, if something changes and causes the bond placement to fall slightly outside of one of the specification limits, thereby reducing the Cpk to <1 , there will be an increase in the PPM value, 3 sigma, as shown in **Table 1**.

If a die bonder placement specification states $\pm 0.5\mu m$ @ 3 sigma and no Cpk value is noted, this assumes Cpk = 1, which means this die bonder supports a 3

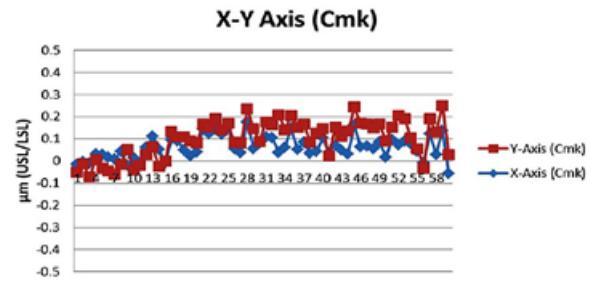


Figure 3: Cmk results for the Nano die bonder.

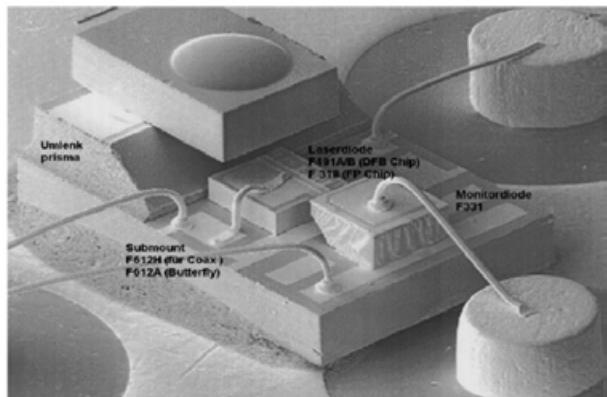


Figure 4: A photonic package.



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sigma process. If, however, the die bonder states $\pm 0.5\mu\text{m}$ @ 3 sigma, Cpk equals 1.33, this translates into a 4 sigma process allowing 1 sigma for unforeseen influences while decreasing the PPM value. Likewise, for the same example the placement requirement is $\pm 0.5\mu\text{m}$ @ 3 sigma, Cpk = 2 translates into a 6 sigma process as shown in **Figure 1b** and in **Table 1** with no PPM loss.

Working with adjusted Cpk values

How would an application engineering manager consider the installation of a sub-micron die bonder be best advised on how to determine its repeatability? And how should he or she compare it to a competitive equipment solution in light of the many variables that affect placement accuracy and repeatability?

One strategy is to differentiate or separate the bonding process from the die bonder's core capability by eliminating the many bond process variables that can influence the outcome, such as bonding epoxy or adhesive, substrate, actual die, bonding materials, temperature, etc. Eliminating these process variables will expose the true placement capability of the die bonder and quantitatively determine the absolute bonding repeatability of the machine. Essentially, this is the best placement repeatability the die bonder is capable of producing. This, then, is the machine capability, or Cmk.

Calculating Cmk

Cmk is calculated the same way as Cpk. With this Cmk data gathered, you can make a first-order comparison with a competitive die bonder. This is especially important at the sub-micron level of placement capability. To ensure the bonder will deliver a repeatable process, die attach equipment manufacturers typically conduct a basic glass-board test.

A Cmk glass die test is a useful method to prove a die bonder's placement capability. However, this test does not guarantee whether the actual bond process is feasible. It does, however, provide insight into the bonder's collective resolution. Knowing the machine's placement capability will help determine what Cpk value is reasonable. The Cmk glass die test, therefore, is an effective method to separate the bond process from the bonder.

To be clear, Cmk does not replace Cpk. Cmk is a tool to measure the fundamental placement repeatability of the bonder. This is important under more controlled conditions for determining whether the bonder achieves the basic system resolution

to meet the required specification limits of the bonding process.

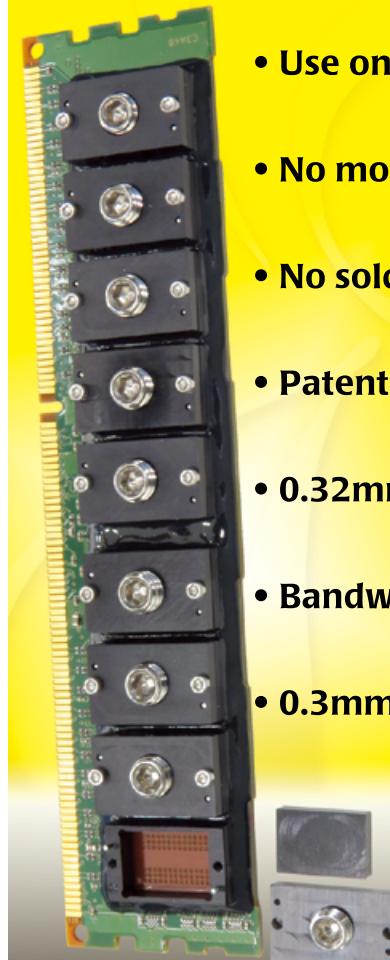
If the required bonding specification limits USL and LSL are $\pm 1.0\mu\text{m}$ @ 3 sigma with a Cpk > 1 , you might want to see a result for Cmk > 1.33 , or even 1.67, just to be sure the bonder has the basic capability or system resolution to meet the given bonding specification in a production environment. More

| Parameters | X-Axis | Y-Axis |
|-----------------|---------|---------|
| Average | 0.0621 | 0.0383 |
| ST DEV | 0.0506 | 0.0568 |
| ST DEV*3 | 0.1519 | 0.1704 |
| Cmk (USL=0.5μm) | 2.8833 | 2.7098 |
| Cmk (LSL=0.5μm) | 3.7016 | 3.1595 |
| Cmk (USL=0.3μm) | 1.5663 | 1.5360 |
| Cmk (LSL=0.3μm) | 2.3846 | 1.9856 |
| Mean (X) | 0.0621 | 0.0383 |
| Min | -0.0558 | -0.0775 |
| Max | 0.1773 | 0.1696 |

Table 2: Calculated Cmk results for the Nano die bonder.

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conservative users might want even higher Cmk values for the same specification limits.

The AuSn eutectic bonding process is even more challenging, especially when the placement accuracy or USL, LSL is $\pm 0.5\mu\text{m}$ @3 sigma when a Cpk >1 is required. This is the case when bonding a laser diode to a silicon photonics package (see **Figure 4**). For such a placement condition, you might need a Cmk >1.67, as well as also conducting a machine capability test.

Cmk test results

The data listed in **Table 2** and **Figure 3** is an actual example of Cmk data performed on Amicra's latest die bonder, the Nano. Keep in mind that the Cmk test eliminates the influence of the actual bonding process by repeatedly picking and placing a glass die on a glass substrate held by vacuum and measuring the placement results. Clearly visible is that the Cmk results will increase or

decrease depending on the USL/LSL chosen, with USL/LSL depending on the required assembly process.

Summary

Knowing the basic Cpk concepts and Motorola's six sigma perspective plays a key role in the decision making process when selecting a die bonder for photonic-level placement. For die attach and for sub-micron placement accuracy you need to ask for the Cmk values. This will give you a good starting point on the most critical specification, thereby stripping away outside influences or excuses why the bonder is not meeting the placement specification. Again, it is important to strip away the influences that can skew the results.

Understanding Cpk and Cmk is critical especially when selecting an automated tool for a bonding process that requires sub-micron placement accuracy. The glass die test is one useful method to quantify a die bonder's placement capability. This is a more "apples to apples" comparison for a complex piece of assembly equipment.

The Cmk glass die test does not guarantee that the actual bond process is possible, but it does provide insight into the die bonder's collective resolution and capability. Knowing the machine's placement capability (Cmk) will help determine what Cpk value is reasonably possible. Simply put, the Cmk results must be better than the required Cpk target. Therefore, the Cmk glass die test is an effective method to remove the bond process and other outside influences from the bonder with the intention to expose and quantify its true placement capability.

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2. D. Montgomery, *Process and Measurement System Capability Analysis, Statistical Quality Control*, 7th Edition, Ch. 8, June 2012.
3. www.six-sigma-material.com

Biography

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Thermal cycling of IC devices

By Ila Pal [Ironwood Electronics]

Various market reports suggest that automotive semiconductors are the major driving force for the growth of the semiconductor sector as a whole. Different types of semiconductor ICs are used in a number of automotive products like navigation control, infotainment systems, collision detection systems, local network systems, advanced driver assistance systems, and fully autonomous systems. Requirements for the semiconductor devices used in automotive applications are very stringent, such as: an operating temperature range of -40°C to 155°C, an operating lifespan of 15+ years, withstanding 0% to 100% relative humidity and most importantly, maintaining a field failure rate of 0%. Various tests need to be performed in order to validate the function of automotive ICs due to the exposure of extreme temperatures over time in addition to various other environmental factors. Example tests include highly accelerated stress test (HAST), biased HAST, thermal cycling (TC), power TC, high-temperature storage life (HTSL), and high-temperature operating life (HTOL), etc.

One of the tests that is a must for automotive IC qualification is thermal cycling at extreme temperatures. Increasing temperature requirements are driven by rising temperatures under the hood, rising power dissipation of microcontrollers, rising control unit loads and higher component integration into smaller packages. Materials expand and contract with temperature change. The objective of thermal cycling is to determine the ability of ICs to resist extremely low and extremely high temperatures, as well as their ability to endure cyclical exposure to

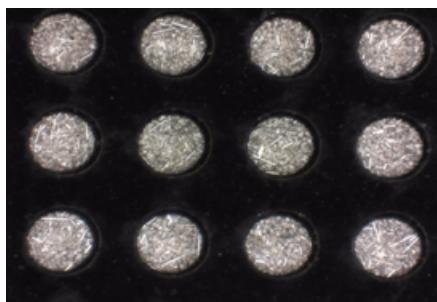


Figure 1: Silver particle filled elastomer interconnect for testing semiconductor devices.

temperature extremes. In order to qualify an IC, it has to be placed in a socket and its functionality verified over the temperature range. Automotive ICs require high-speed performance due to the nature of their applications in radar, quick response collision detection, etc. Socket needs driven by this high-speed performance requirement are 70+GHz. Because sockets are the test platform used in qualifying ICs, two criteria have to be met: 1) the socket has to withstand the thermal cycling and the aging process and, 2) it should be capable of performing high-speed signal testing.

High performance elastomer

Ironwood Electronics high-performance elastomer sockets use an interconnect technology that delivers low signal loss (-1dB at 75GHz) and supports ball grid array (BGA) packages with pitches down to 0.2mm. The contacts consist of silver particles held in conductive columns (buttons) that are embedded in a nonconductive polymer substrate that provides high compliance for BGA packages, which may have co-planarity issues and can be applied in extreme temperature ranges. A magnified photograph revealing the silver button elastomer contact is shown in **Figure 1**. The picture shows a top view of a 4x3 array of contacts. A guide on top of the contacts has an opening for each ball that precisely guides the device's balls onto the elastomer buttons. The sockets are designed such that force is evenly distributed on the top of the IC pushing the solder balls into very high-bandwidth elastomer buttons with silver particles. Socket design is very critical as it has to keep constant pressure on the device, bringing it in contact with the printed circuit board (PCB) via elastomer contacts while the temperature fluctuates. When the socket is exposed to thermal cycling, various components expand and contract at different rates due to variations in the coefficient of thermal expansion (CTE). A first set of experiments were focused on what happens to elastomer when it becomes cold or hot. The socket is then designed to accommodate the CTE mismatch. A final set of experiments was focused on full thermal cycling.

Cold temperature test

Silver button elastomer contacts were placed between a daisy-chained test PCB and a counter daisy-chained device emulator. A recommended force was applied using a simple fixture consisting of two flat plates that sandwich the entire elastomer PCB device assembly. Total chain resistance was measured and the resistance per contact was calculated and logged at room temperature (25°C). The entire test set-up was placed inside a Thermotron S-1.2C benchtop environmental chamber capable of testing -73°C to +180°C. Time, temperature and resistance data were collected as the temperature dropped to -55°C and plotted as shown in **Figure 2**. Total contact resistance of the interconnect for a 609-ball device was measured by connecting a complete daisy chain from the test PCB to the elastomer to the emulated device to the elastomer and back to the test PCB. Contact resistance per ball was calculated and is shown in the primary Y-axis. Time is shown on the X-axis. Temperature is shown on the secondary Y-axis. Results from the graph show that as the temperature drops, contact resistance decreases in a directly proportional relation. Once -55°C is reached, contact resistance stabilizes as well. This stabilization can be surmised from the flat line portion of the graph. Silver button elastomer connects the device balls to PCB pads via compressed silver particles that contact each other. As the temperature decreases, contraction enables more compression between each of the silver particles, which in turn causes reduction in resistance.

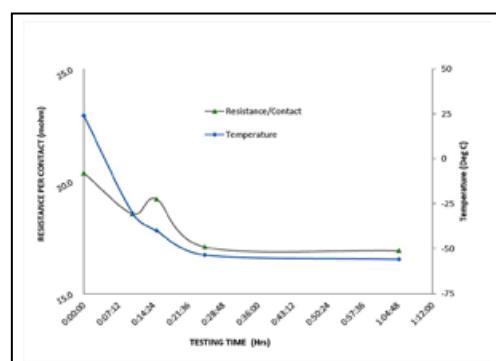


Figure 2: Contact resistance change over time as the temperature decreases to -55°C.

Elevated temperature test

Similar to the cold test setup, silver button elastomer, sandwiched between the test PCB and device, was measured at room temperature and placed inside a hot chamber. Time, temperature and resistance data were collected as the temperature increased to +160°C and plotted in **Figure 3**. Again, total contact resistance of the interconnect for a 609-ball device was measured by connecting a complete daisy chain from the test PCB to the elastomer to the emulated device, and back to the test PCB. Contact resistance per ball was calculated and is shown in the

next to it. The silver button elastomer socket is designed for a 35x35mm package size and operates at bandwidths up to 75GHz with less than 1dB of insertion loss. The socket is designed to dissipate a few watts using a compression screw and can be customized to accommodate a few hundred watts with a modified fin design on top of the screw and the addition of an axial flow fan (not shown in the picture). The socket is mounted on the daisy-chained PCB with no soldering, and its small footprint allows capacitors/resistors to be placed nearby. Other passive components can be placed on the back side of the PCB by creating custom cutouts in a stiffener plate. The socket is constructed with a clamshell lid that employs a quick insertion/extraction method so that ICs can be changed out quickly. The clamshell lid has an integrated compression plate that has a properly selected and fully enclosed spring. To use this structure, place the daisy-chained device emulator inside the socket, close the lid by latching and apply downward pressure by turning the compression screw, which in turn will compress the springs. The springs are pre-loaded to accommodate temperature

this assumption may not be the only factor to consider. It is highly possible that colder temperature stresses may actually have a more adverse effect on life than elevated temperatures. Therefore, thermal cycling needs to be represented in another manner. The three basic variables to be defined for thermal cycling are amplitude, cycle time and frequency. Amplitude is the difference between the high and low temperatures. Cycle time is the time it takes to complete one cycle from room temperature to the elevated temperature to the cold temperature and back to room temperature. Frequency is the number of temperature cycles executed.

Our focus was to verify if the socket platform was capable of identifying faults in an IC when performing a thermal cycle experiment. In our experiment, we cycled between -55°C and 160°C. The amplitude in our case was 215°C. The room-hot-cold-room temperature cycle was 2 hours. The

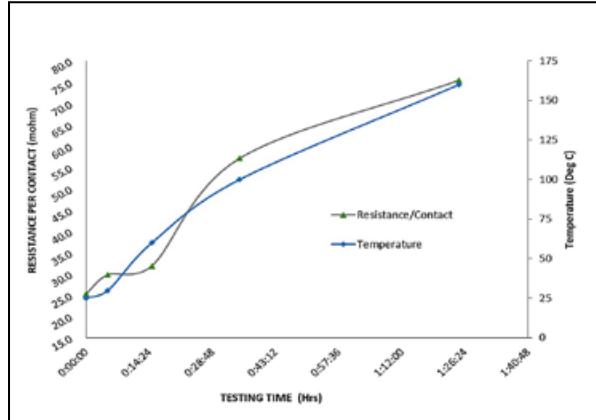


Figure 3: Contact resistance change over time as the temperature increases to +160°C.

graph. Results from the graph show that, as the temperature rises, contact resistance increases in a directly proportional relation. An increase in temperature causes expansion of materials and results in less contact between silver particles. Less contacted silver particles show an increase in contact resistance. Because a proper compression force was not selected, it can be seen from the graph that the contact resistance is 3x higher when compared to the original value at room temperature.

Socket design

The above cold/hot temperature testing uses simple fixtures to show that socket components expand and contract at different rates than the silver button elastomer and that the contact force plays a significant role in optimum connection. In order to keep compression at equilibrium, spring-loaded compression mechanisms are utilized. Spring rate is selected such that its rate accommodates CTE mismatch between the metal compression plate and elastomeric silver button contact. **Figure 4** shows a spring-loaded clamshell lid socket for a 1152-pin BGA device mounted on a daisy chained PCB with the emulated device on the side

variations. Spring material is selected to minimize spring rate fluctuations within the temperature range, number of cycles and frequency planned for thermal cycling testing.

Thermal cycling

There are multiple ways a change in temperature can cause damage to an IC or the system. If the rate of change is too fast (thermal shock), some ICs cannot accommodate the temperature imbalance between the cold and hot sides and can result in fracture of the package. Sometimes, the accumulating effect of small changes leads to a failure. Thermal cycling is a time-dependent phenomenon. All these issues need to be factored into the design of a thermal cycle experiment. In general, less stress implies a longer life, but when considering extreme temperatures,

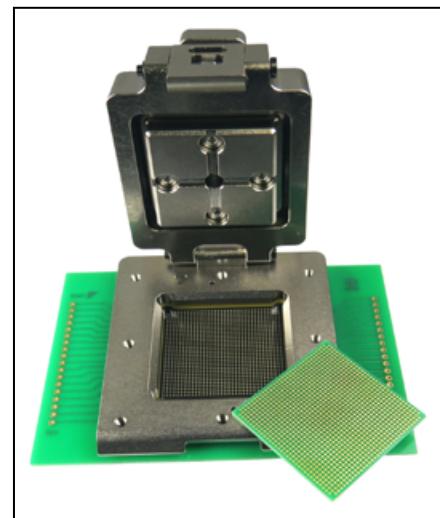


Figure 4: Spring loaded clamshell lid socket with silver particle filled elastomer buttons mounted on a printed circuit board with an emulated device shown next to it.

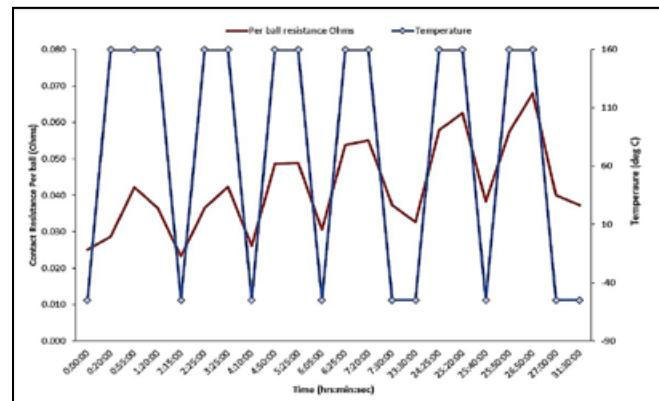


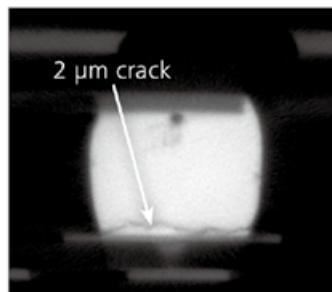
Figure 5: Contact resistance change and temperature change over time — thermal cycling data.

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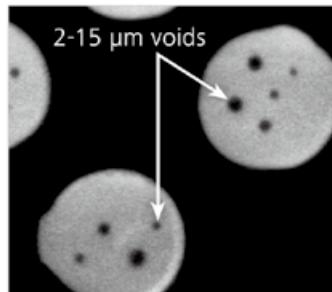
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frequency was 6. The Thermotron chamber was programmed to carry out the above mentioned thermal cycle set up. The output of our experiment was the contact resistance between device balls to PCB pads via the elastomer contact. These variables can be changed and performed until failure to determine the life of a product. Results are shown in **Figure 5**. Total contact resistance of the 1152-ball device interconnect was measured by connecting the complete daisy chain from the PCB to the elastomer to the

device to the elastomer, and back to the PCB. Contact resistance per ball was calculated and is shown in the graph. It can be seen from the graph that the contact resistance fluctuated around 30 milliohms per contact as the temperature cycled from cold to hot and vice versa. Contact resistance is seen to trend upwards as the frequency increases. This is due to the reduced cycle time (temperature changed at a faster rate). An increased cycle time indicates a slower frequency, which means that the temperature is changing at a

much slower rate. Therefore, the rate of change in temperature is commensurate with the shock to the component. As the frequency increases, the stress that the component sees actually increases, resulting in the upward trend observation in the contact resistance.

Summary

The above experiments provide a very brief introduction to thermal cycling and how elastomer sockets can be used in thermal cycling. Cold temperature allows for better connections between a device and a PCB via an elastomer contact. Elevated temperatures diminish the connection between the device and the PCB via the elastomer contact. A socket design has to accommodate these variations and keep the connection within a range where electrical testing of semiconductor devices is not affected.

Thermal cycling is an aging process. While we use sockets in thermal cycling to accelerate IC device aging and determine their failure point, the life of the socket itself is accelerated as well. There are various ways in which IC devices become damaged. This implies that the specific failure mechanisms have to be understood thoroughly before designing the thermal cycling based life test. The thermal cycling profile has to replicate the same path to failure as seen in normal use. If you accelerate the life testing by cycling more often than it occurs in normal use, you may inadvertently accelerate different mechanisms than desired. For example, most modern vehicles incorporate a pushbutton start-stop system that involves high-power switching ICs. Expectations are >50,000 start-stop events during its lifetime. These events happen on hot summer days where the car's control system temperature reaches 80°C+ and on cold days where the temperature can fall below -20°C. Thermal cycling-based life tests for semiconductor ICs have to be carefully designed based on the actual events, to drive failure mode, by considering the number of cycles with the extreme temperatures and the time between events.

Acknowledgement

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Biography

Ila Pal is Chief Operating Officer at Ironwood Electronics and can be reached at ila@ironwoodelectronics.com

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| Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 USA Tel: +1-401-823-5200 www.advanced.com | D, P, T | BA, LA, SM | CP > 0.5mm (>0.5 CM) CL > 200,000x OT = -CM FQ < 3.5GHz @ -0.9dB CF < 18g CR < 2.8A |
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| Aries Electronics, Inc. 2609 Bartram Road Bristol, PA 19007 USA Tel: +1-215-781-9956 www.arieselec.com | B, D, P, T | BA, LA, SM, TH | CP > (0.3-0.5)mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1-80)GHz @ -1dB CF < (15-110)g CR < (1.0-3.0) A |
| Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 USA Tel: +1-949-492-6481 www.azimuth-electronics.com | D, T, B, P | BA, LA, SM, TH | CP > 0.5mm OT to -55°C to +250°C CL, FQ, CF & CR = CM |
| BeCe Pte Ltd Blk 5000, #03-09 Ang Mo Kio Ave 5. Singapore 569870 Tel : +(65) 6853 1065 www.bece.com.sg | T | BA, LA | CP = CM CL = CM OT = CM FQ = CM CF = CM CR = CM |
| C2WIDE Co., Ltd. RM705, Ace High-End Tower 8,354-4 GasanDong Geum Choen-Gu Seoul, Korea Tel: +82-2-364-1878 www.c2wide.com | B, D, P, T | BA, LA | CP = 0.4/0.5/0.65/0.8/1.0mm CL = 300,000 OT = -55° to 130°C FQ > -0.63dB @ 20GHz CF = 25~35g CR = 3A Continous |
| C.C.P. Contact Probes. 5F, No. 8, Lane 24, Ho Ping Rd., Panchiao District, New Taipei City 220, Taiwan R.O.C. Tel +886-2-29612525 www.pccp.com.tw | B, D, P, T | Refer to company website for additional information | CP = >0.2mm CL = >500k OT = -40~170 FQ = >10GHz CF = 15~45 grams CR = >3A |
| Centipede Systems Inc. 2906 Scott Boulevard Santa Clara, CA 95054 USA Tel: +1-408-321-8201 www.centipedesystems.com | T | BA, LA, SM | CP > 0.3mm CL > 500,000x OT < +160°C FQ = CM CF = CM CR < 2.0A @ 150°C |

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| Chip Shine Inc. 2070 Business Center Drive, Suite 140 Irvine, CA 92612 USA Tel: +1 949-536-5268 www.chipshine.com | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Cohu, Inc 12367 Crosthwaite Circle Poway, CA 92064-6817 USA Tel: +1-858-848-8000 www.cohu.com | D, P, T | BE, BD, LA, SM | CP > 0.20mm CL = up to 3 Million OT = -60°C to 175°C FQ = < 81GHz CF = 5 – 50 gram CR = < 5A |
| Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 USA Tel: +1-510-357-7900 www.contechsolutions.com | B, D, T | BA, LA, SM | CP > (0.2-0.5)mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19-39)g CR < (1.5-4.0) A |
| Custom Interconnects, LLC 7790 E. Arapahoe Rd, Suite 250 Centennial, CO 80112 USA Tel: +1- 303-934-6600 www.custominterconnects.com | D, T | BA, LA, TH | CP > 0.5mm CL > 500,000x OT = -60°C to +150°C FQ < 40GHz CF = CM CR < 5.0A |
| Enplas Tech Solutions Inc. 3211 Scott Blvd, Suite103 Santa Clara, CA 95054 USA Tel: +1 669-243-3600 www.enplas.com | B, D, T | BA, LA, SM | CP > 0.4mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14-35)g CR < (0.5 -1.0) A |
| Essai, Inc. 45850 Kato Road Fremont, CA 94538 USA Tel: +1-510-580-1700 www.essai.com | T | BA, LA, SM, TH | CP > 0.3mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30GHz @ -1dB CF < (15-40)g CR < (0.5-1.0) A |
| E-tec Interconnect AG Friedhofstrasse 1 2543 Lengnau Switzerland Tel: +41 32 654 15 50 www.e-tec.com | D, P | BA, LA, SM | CP > (0.4-0.5)mm CL > (100 - 10,000)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40g CR < (0.5-3.0) A |
| Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 USA Tel: +1-800-392-8766 www.exatron.com | D, T | LA, SM | CP > 0.4mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40GHz @ CM CF < (10-12)g CR = CM |
| FineOhms 11-2, Wonnam-ri, Eumbong-myun, Ahsan-si, Chungcheongnam-do South Korea Tel. +82 41 538 9012 www.fineohms.com/en | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Gold Technologies Inc. 1648-A Mabury Road San Jose, CA 95133 USA Tel: +1 408-321-9568 www.goldtec.com | B, D, T | CM | CP > (0.4-0.5)mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6-16.0)GHz @ -1dB CF & CR = CM |

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| High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 USA Tel: +1-408-743-9700 www.hcdcorp.com | B, D, P, T | BA, LA | CP > .35mm CL > (50k - 250k)x FQ < (4.4 - 40GHz) -50-150 CF < (10-50g) CR = 8 amps/pin |
| High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 USA Tel: +1-510-445-1182 www.hptestusa.com | B, D, T | BA, LA, SM | CP > 0.5mm CL > (100K - 300K)x OT = -50°C to +150°C FQ < 3.0GHz @ CM CF = CM CR < 5.0A |
| HiCon Co., Ltd. 9th floor, Star Tower, 37, Sagimakgol-ro 62 beon-gil, Jungwon-gu, Seongnam-si, Gyeonggi-do Republic of Korea 13211 Tel: +82-31-698-2741 www.hi-con.kr | D, P, T | BA, BD, LA, SM | CP = ≥0.3mm CL = Product Dependant OT = -55° to 155°C FQ > 15-40Ghz @ -1dB CF = Product Dependant CR = 2-4A |
| Inno Global Inc. 123 Cheomdan, Gwagiro Bukgu, Gwangju Republic of Korea Tel: +82-10-5236-2581 www.inno50.com | D, T | BA, LA, SM | CP = > 0.2mm CL = (10K - 200K) x OT = (-40 ~ 150) degree C FQ = > 20GHz @ -1db CF = (4 ~ 40g) CR = (1.0 ~ 7.0) A |
| Incavo Otax, Inc. 4407 Bee Cave Road, Suite 512 Austin, TX 78746-6496 USA Tel: +1-512-328-2220 www.incavo.com | B, D, P, T, CM | BA, BD, LA, SM, TH | CP > 0.01mm CL = 300K to 1000K OT = -55°C to 155°C FQ = 3.0~40GHz@-1dB CF = 6g to 50g CR < 6.0A |
| Ironwood Electronics 1335 Eagandale Ct Eagan, MN 55121 USA Tel: +1-800-404-0204 www.ironwoodelectronics.com | B, D, P, T, CM | BA, BD, LA, SM, TH | CP > 0.2mm CL > 2K - 500K OT = -70C to +200C FQ < 75 GHz @ -1dB CF < 15 - 50g CR < (2.0 - 8.0) A |
| ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr | B, D, T | BA, LA, SM | CP > (0.3-0.4)mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A |
| JC Electronics Corporation 1-33-14, Todoroki, Setagaya-ku, Tokyo 158-0082 Japan Tel: +81-3-5706-4360 Website: www.jcel.com | B, D, P, T, CM | BA, BD, LA, SM, TH | CP = 0.3mm CL = 10K - 500K OP = -55C to +300C FQ = < 75GHz CF = 10 - 40 gm CR = 2 - 8A |
| JF Microtechnology Sdn. Bhd. Lot 6, Jalan Teknologi 3/6 Taman Sains Selangor 1 Kota Damansara 47810 Petaling Jaya Selangor, Malaysia Tel: +603-61408668 www.jf-technology.com | D, P, T, CM | BD, LA, SM, TH | CP = ≥ 0.3mm CL > 300K to 2KK OT = -60°C to +180° FQ = 40GHz@ -1dB CF = 20g to 120g/Pin * CR = >3A to >100A * *depend on test pin design |
| Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 USA Tel: +1-612-378-2020 www.johnstech.com | D, P, T | BA, BD, LA, SM | CP > 0.3 mm CL > (300K - 1,000K)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A |

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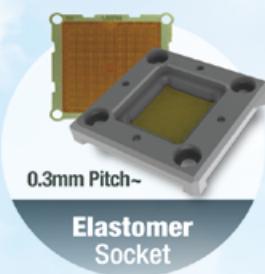
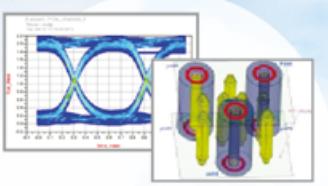
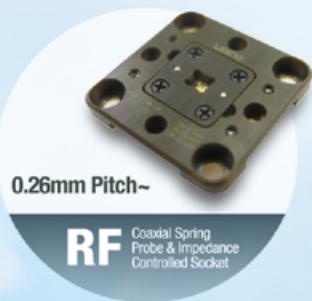
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| Kyosei Co. Ltd. Chiyoda Building 2-37 Ichigaya Tamachi Shinjuku-ku Tokyo Japan 162-0843 Tel: +081 (03) 3260-5326 www.kyoseiltd.co.jp | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Leeno Industrial Inc. (46748) 10, Mieumsandan-ro 105beon-gil Gangseo-gu, Busan, Korea Tel: +82-(0)51-831-3232 www.leeno.com | B, D, P, T, CM | BA, BD, LA, SF, TH | CP > 0.1mm CL = >200K OT=-55C~150C FQ = 6ghz ->50ghz@ -1db CF = 6g-50g CR = <3.0A @0.4p |
| Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 USA Tel: +1-408-727-4234 www.loranger.com | B, D, T | BA, LA, SM, TH | CP > (0.25-0.4)mm CL = CM OT = CM FQ = CM CF = CM CR = CM |
| M Specialties LLC 1815 W 1st Ave, ST 112 Mesa, AZ 85202 USA Tel: +1-800-892-8760 www.mspeciallc.com | D, T | BA, LA, SM | CP > 0.3mm CL > 500,000x FQ < 25GHz @ -1dB OT, CF & CR = CM |
| MCS Co., LTD 15-21, Oh song 2gil, Seonggeo-Eup, Seobuk-Gu Cheon-An, Chung-Nam 331-831, South Korea Tel: +82-041-621-4331 www.mcsgroup.co.kr | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Microfriend Inc. 10F Seoul Techno Park #232 Gongneung-ro, Nowon-gu Seoul, South Korea Tel : +02-944-6400 www.microfriend.co.kr | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjc.co.jp | B, D, T | BA, SM | CP > 0.2mm FQ < 40GHz @ -1dB CL, OT, CF & CR = CM |
| Mikuro Spring 22 - 6 Kowata-minami, Suwa, Nagano 392-0023 Japan Tel: +81 0 266 52 3550 www.mikuro-spring.com | Refer to company website for additional information | Refer to company website for additional information | Refer to company website for additional information |
| Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 USA Tel: +1-516-922-6000 www.mill-max.com | P | SM, TH | CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25-50)g CR < (1.0-3.0) A |
| Modus Test LLC 651 North Plano Road, Suite 419 Richardson, TX, 75081 USA Tel: +1-972-914-7866 www.modustest.com | D, T | BA, LA, SM, TH | CP > 0.3mm CL > 1,000,000x OT = +200°C Max. FQ < 20GHz @ CM CF < 35g CR < 5.0A |

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| OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong, Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 www.okins.co.kr | B, D, T | BA, LA, SM | CP > (0.4-0.5)mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0-12.4)GHz @ -1dB CF < (7-15)g CR < (0.5-1.0) A |
| Paricon Technologies Corporation 500 Myles Standish Blvd. Unit 103 Taunton, MA 02780 USA Tel: +1-508-676-6888 www.paricon-tech.com | B, D, P, T | BA, LA | CP > (0.1-0.4)mm CL > 1,000,000x OT < 150°C FQ < 40GHz @ -1dB CF & CR = CM |
| Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 USA Tel: +1-602-518-5799 www.phxtest.com | D, P, T | BA, BD, LA, SM | CP > 0.3mm DL > 1,000,000 OT = -55°C to +155°C FQ > 40GHz @ -1dB CF = 20-45g CR = 3.5-8.5A |
| Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 USA Tel: +1-972-258-1906 www.plastronics.com | B | BA, LA, SM | CP > (0.4-0.5)mm CL > (5k-20k)x OT = -65°C to +150°C FQ < 15GHz @ -1dB CF < (7-50)g CR < (0.4-1.2) A |
| Precision Contacts Inc. 990 Suncast Lane El Dorado Hills, CA 95762 USA Tel: 1+ 916-939-4147 www.precisioncontacts.com | D, P, T, CM | BA, LA, SM, TH | Refer to company website for additional information |
| Qualmax, Inc. 3003 North First St. Suite 340 San Jose, CA 95134 USA Tel: +1-408-519-5748 www.qualmax.com | D, T | BA, LA, SM | CP < (0.4-0.5)mm CL < (200k - 500k)x OT = CM FQ < (9-25)GHz @ -1dB CF < (18.5-40)g CR < (1.0-4.0) A |
| R&D Altanova 3601 So. Clinton Avenue South Plainfield, NJ 07080 USA Tel: +1-732-549-4554 www.rdaltnova.com | D, P, T | BA, BD, LA, SM | CP < 0.3mm CL = 150,000x OT = -40° to 150°C FQ > 38GHz @ -1dB CF = 15g CR = 4A |
| Rika Denshi Co., Ltd. 13F Mita International Building 1-4-28 Mita, Minato-ku Tokyo 1080073 Japan Tel: +81 3 6635 0620 www.rikadensi.com | D, T | BA, LA, SM | CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36GHz @ -1dB CF < (15-30)g CP & CR = CM |
| Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 USA Tel: +1-408-779-8008 www.testfixtures.com | B, D, P, T | BA, LA, SM | CP > (0.3-0.4)mm CL > 25,000x OT = -50°C to +150°C FQ < 30GHz @ -1dB CF = CM CR < 3.0A |
| RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 USA Tel: +1-623-879-6690 www.rstechinc.com | B, D, T | BA, LA, SM, TH | CP > 0.35mm OT = -55°C to +150°C FQ < (9-10)GHz @ CM CR < (1.0-15.0)A CL & CF = CM |

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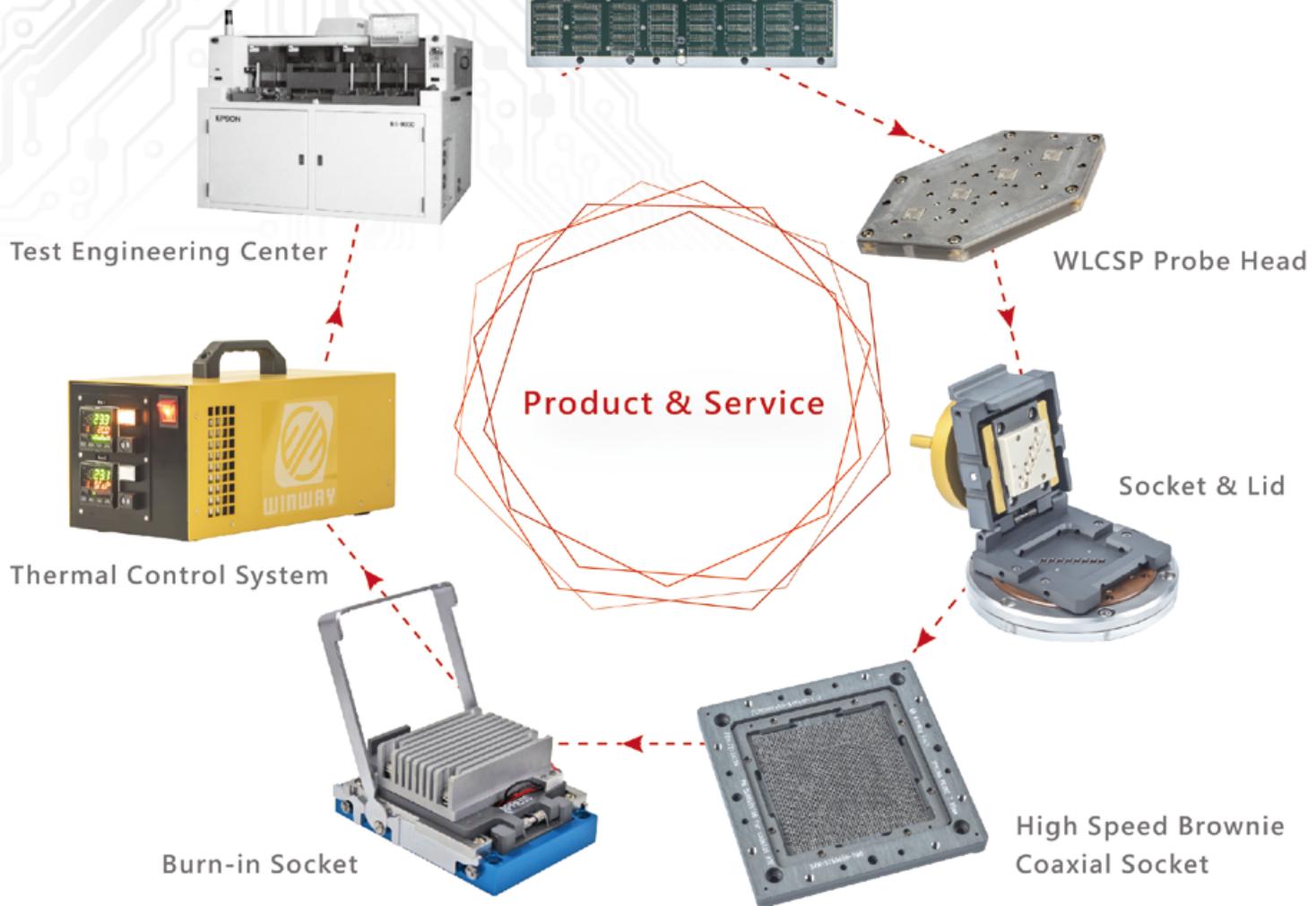
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| Sanyu Electric, Inc. 6475 Camden Ave., Suite103 San Jose, CA 95120 USA Tel: +1-408-269-2800 www.sanyu-usa.com | CM | CM | CP > 0.2mm CL = CM OT = -40°C to +150°C FQ < 40GHz @ -1dB CF < (15-25)g CR < (4.0-5.0) A |
| Sensata Technologies 529 Pleasant Street Attleboro, MA 02703 USA Tel: +1-508-236-3800 www.sensata.com | B | BA, LA, SM | CP > (0.4-0.5)mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10-25)g CR < 1.0A |
| S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp | B, D, T | BA, LA, SM, TH | CP > (0.3-0.4)mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5-20)GHz @ CM CF & CR = CM |
| Smiths Interconnect 860 Hillview Court; Suite 240 Milpitas, CA 95035 USA Tel: +1-408-957-9607 x-1125 www.smithsinterconnect.com | D, P, T | BA, BD, LA, SM, TH | CP > 0.2mm CL > 250k-1M OT - 40° to 150°C FQ < 25GHz @ -1db CF 8-85 grams CR 1.5 to 5Amps |
| Test Tooling Solutions Group Singapore Tel: +65 6779 6866 www.tts-grp.com | D, T, P | BA, BD, LA, SM, TH | CP 0.15mm CL > 300k OT = -40°C to +180°C FQ < 81GHz @ 1dB CF = 8 to 45g CR < 6.0A |
| 3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 USA Tel: +1-512-984-1800 www.3mconnector.com | B, D, P | BA, LA, SM, TH | CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5-80)g CR < (0.5-1.0) A |
| TSE Co. Ltd. 78, 4sandan 5-gil, jiksan-eup Cheonan-si, Chumgnam 31040, South Korea Tel: +82 10 8822 5630 www.tse21.com | B, D, P, T | BA, BD, LA, SM | CP ≥ 0.2 CL = (100–500K) OT = -55° to +150° FQ = (20-67)GHz @ -1dB CF = (10-35)g CR =(1- 4) A |
| TwinSolution Technology Co. Ltd. Guoshoujing Road Zhangjiang Hi-tech Park Shanghai, PRC Tel: +86-512-67069861 www.twinsolution.com | B, D, P, T | BA, BD, LA, SM | CP > 0.08mm CL > 250K~1M OT = -55°C~200°C FQ < 40GHz@-1dB CF = (0.5~150)gf CR = (1.5~10)A |
| Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com | B, T | SM | CP > 0.4mm OT = -40°C to +150°C FQ < (6-8)GHz @ CM CL, CF & CR = CM |

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| WinWay Technology Co. Ltd. No. 68, Chuangyi S. Road, Second District of Nanzih Export Processing Zone, Nanzih Dist Kaohsiung City 81156, Taiwan Tel: +886-7-361-0999 www.winwayglobal.com | B, D, P, T | BA, BD, LA, SM | CP > 0.12mm CL > (50k-1000k)x OT = -55°C to +180°C FQ = 60Ghz/112Gbps @ -1dB CF = (6~60)g CR = (0.5~7)A |
| Xcerra Corporation 825 University Avenue Norwood, MA 02062 USA Tel. +1-781-461-1000 www.xcerra.com | D, T | BA, LA, SM | CP > (0.25-0.5)mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5-40)GHz @ CM CF < (26-55)g CR < (1.8-4.6) A |
| Yamaichi Electronics Co., Ltd. 11F Technoport Mitsui Seimei Bldg. 2-16-2 Minamikamata, Ota-ku, Tokyo 144-8581 Japan Tel: +81-3-3734-0110 www.yamaichi.co.jp | B, D, P, T | BA, BD, LA, SM, TH | CP > 0.4mm CL = CM OT = -65°C to +150°C FQ < (2.7-6.9)GHz @ -1dB CF < (13-30)g CR < (0.5-1.0) A |
| Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com | B, D, T | BA, LA, SM | CP > 0.3mm OT = -55°C to +150°C FQ < 16GHz @ -1dB CL, CF & CR = CM |

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Sequential-3D integration for advanced semiconductor scaling

By Anne Vandooren, Jacopo Franco, Arindam Mallik, Liesbeth Witters, Nadine Collaert [imec]

Technology innovations are expected to allow traditional Moore's Law scaling to continue for at least five to ten years. At the same time, researchers worldwide are exploring alternative options to overcome a number of challenges – physical, technological and economical – associated with further scaling of CMOS transistor dimensions. One of these alternatives is sequential-3D integration (S3D), a relatively new technology that promises to alleviate problems in classical 2D CMOS (Figure 1). This integration technique involves the vertical integration of sequentially processed device layers, and comes in three different flavors – depending on where the partitioning and stacking takes place. First, in transistor-

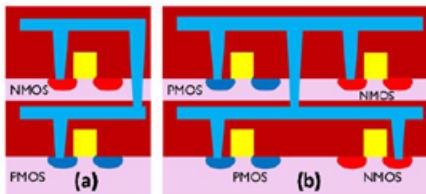


Figure 1: A sequential-3D a) at transistor level, and b) at cell level.

level S3D, the CMOS gate is split into tiers of pMOS and nMOS. Second, in CMOS-level S3D, conventional 2D standard cells are placed in different tiers. And finally, the partitioning can be done at the IP block level to separate, for example, the analog and I/O functionality from the logic and memory part. This is referred to as hybrid S3D (or heterogeneous S3D) (Figure 2) where besides CMOS devices, different flavors of technologies can be combined.

S3D comes with its own set of technology challenges, which are further discussed in this article. When these challenges can be overcome, the technique is expected to further enhance device density per chip area, reduce the length of the interconnection lines, and facilitate the co-integration of heterogeneous device

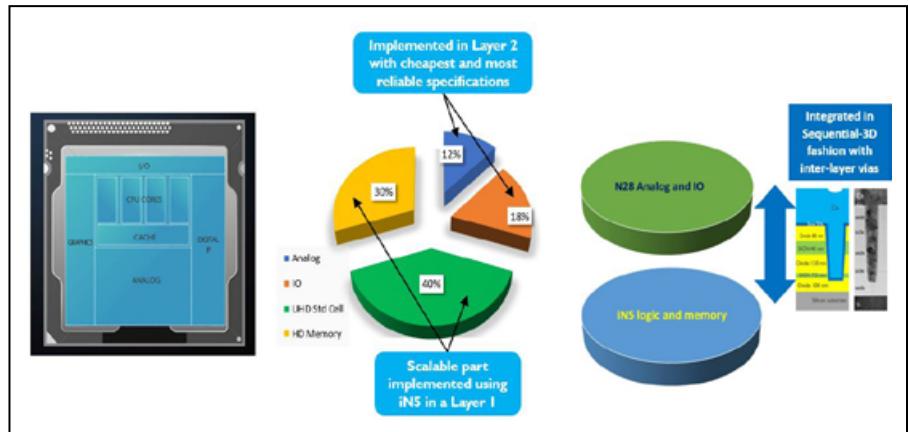


Figure 2: Illustration of the hybrid S3D technology. In this example, the logic and memory part is scaled to the 3nm (or iN5) node in the bottom tier, and the remaining part (analog and I/O) is manufactured at the 28nm technology node in the top tier. In this particular case, the non-scalable analog and I/O part takes up to 30% of the overall circuit area.

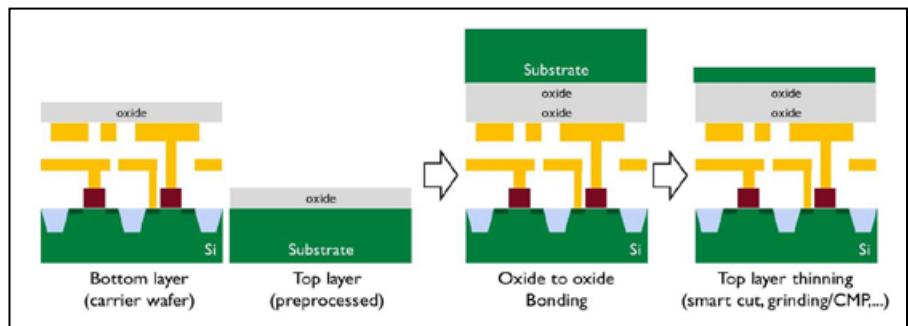


Figure 3: Schematic of an envisioned 3D sequential integration flow. After thinning the top Si layer, top-tier devices can be fabricated in a low thermal budget flow.

technologies. However, to quantify the real benefits in terms of power, performance, area and cost, a systematic investigation is required for each of the S3D flavors. In this article, the benefits of the integration technology are evaluated using advanced technology nodes, i.e., 5nm and beyond.

Thermal budget: a key technology challenge

In general, the processing of S3D integrated circuits consists of three different blocks (Figure 3). The first block involves standard bottom tier device processing, up to a certain level

of interconnects. In a second block, a blanket semiconductor layer needs to be created on top of the processed device and interconnect layers. At imec, this is done by layer transfer based on a dielectric-to-dielectric wafer bonding technique and a donor silicon-on-insulator (SOI) wafer. The third block is the top device processing, during which the first patterned layer is aligned to the last processed (interconnect) layer at the bottom tier level.

During standard MOS device processing, various thermal steps are applied, some of them exceeding 1000°C, and this presents some major technological

challenges. On the one hand, to avoid degradation of the bottom tier devices, the thermal budget for the top-tier processing needs to be limited, and this may induce a mismatch in performance between the two tiers. On the other hand, the materials used in some critical process steps for the bottom tier device (such as the interconnect metals, device contacts and gate stacks) need to be sufficiently thermally stable as to withstand the (limited) thermal budget required for top tier fabrication. Furthermore, the thermal processes may impact the dielectric that is used for the wafer bonding (**Figure 4**). At high temperatures, for example, voids can be created at the bonding interface. The dielectric therefore needs to be sufficiently outgassed prior to bonding, at a temperature equivalent to the total thermal budget required for the top device processing.

A thermally stable metal for the back-end-of-line

In view of thermal limitations, the imec team has investigated metal alternatives to

copper (Cu) for routing at the bottom layer. These interconnect metals must have both a good thermal stability to withstand top device processing, and a low resistance to maintain a low RC delay. Cu, for example, has a low thermal stability (450–500°C). At higher temperatures, Cu atoms can easily diffuse into the dielectrics and contaminate the front-end-of-line devices. Tungsten (W), on the other hand, has a higher thermal stability than Cu (up to 600°C), but is less suited due to its higher resistivity. The team therefore proposes cobalt (Co) as a bottom back-end-of-line metal. Co provides a 2 to 3 times lower resistance than W, and a thermal stability as good as W.

Gate stack and contact optimization

Gate stack challenges are also confronted with thermal limitations, and therefore, an alternative approach to gate stack engineering is proposed. A first challenge relates to the gate stack of the bottom device. In contemporary technologies, industry uses a replacement metal gate flow. As part of this flow, a dummy gate is deposited to implement a self-aligned

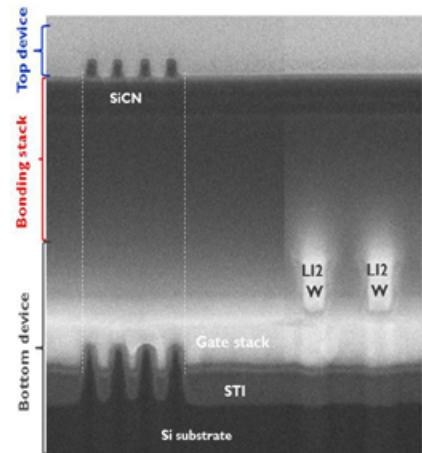


Figure 4: FinFET on FinFET device stacking enabled on 300mm wafers, featuring wafer-to-wafer bonding and 14nm FinFET technology.

device fabrication; the dummy gate remains in place during all the high-temperature process steps (e.g., junction activation), and only at the end of the process flow is it removed and replaced by the real gate stack. This allows larger flexibility in the choice of work function metals, without this

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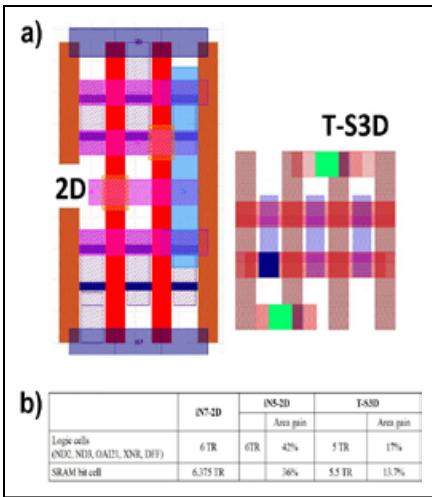


Figure 5: a) Logic cell layout (ND2 cell) in (left) traditional 2D and (right) transistor-level S3D implementation. The figures demonstrate a representative graphic database system (GDS) in accordance to 5nm design rules. The top and bottom tiers are connected to each other through three types of inter-tier vias. b) Comparison of the area gain in 2D and transistor-level S3D implementations. iN7-2D and iN5-2D are 5nm and 3nm 2D implementations, respectively; T-S3D, C-S3D and H-S3D are sequential-3D implementations at the transistor, cell and IP block level, respectively.

choice being limited by thermal stability concerns. In a S3D flow, however, the bottom tier device processing is followed by the top tier device processing, which can further affect the stability of the bottom gate stack. To address this issue, imec has investigated the thermal stability of various work function metal stacks, and optimized them for improved stability.

A second challenge relates to the gate stack of the top tier device. In industry, rapid high-temperature annealing steps (“reliability anneals”) are commonly applied after gate stack deposition to cure defects in the dielectric SiO₂/HfO₂ layers. These defects can trap charge carriers and deteriorate the device reliability, inducing, as an example, severe bias temperature instability (BTI). These high-temperature “reliability anneals” cannot however, be used when fabricating the top device layer to preserve the integrity of the bottom tier interconnects. Therefore, the team looked into alternative oxide stacks, which could offer improved reliability without requiring a thermal treatment. By careful engineering, the energy level of the traps with respect to the Fermi level in the semiconductor channel, the interaction of carriers with the traps can be minimized. This engineering can be realized, e.g., by inserting a thin LaSiO_x interlayer in between SiO₂ and HfO₂. With this novel

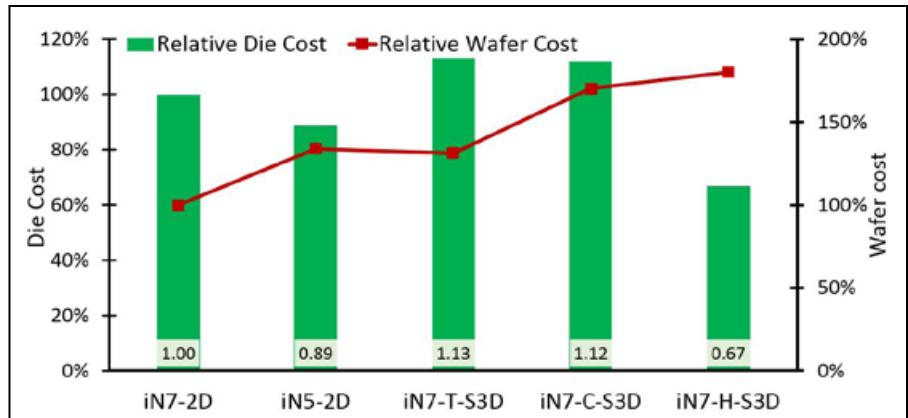


Figure 6: Die cost for different S3D variations. iN7-2D and iN5-2D are 5nm and 3nm 2D implementations, respectively; T-S3D, C-S3D and H-S3D are sequential-3D implementations at the transistor, cell and IP block level, respectively.

oxide stack, the team demonstrated sufficient BTI reliability without resorting to high-temperature “reliability anneals.”

Contacting the transistor’s source, drain and gate is traditionally done by using silicides such as nickel (Ni) silicide. These silicides, however, typically show a limited thermal stability of the contact resistivity. The imec team, therefore, looked into direct contacting to a metal contact (such as titanium (Ti)/Ti-nitride), a technique that is increasingly used within advanced FinFET technologies. With direct contacting, a higher thermal stability is obtained, giving additional relief on the thermal budget limitations.

Potential benefits of sequential-3D integration

Compared to a 2D implementation, the sequential processing of device layers promises an enhanced device density per chip area, and a reduced length of the interconnection lines. But is it really that beneficial? Can we, for example, expect a 50% area reduction by stacking devices in two tiers? What is the impact on the RC delay? And does it follow the economics of scaling? To answer these questions, imec has analyzed and quantified the benefits in terms of power-performance-area-cost at 5nm and 3nm technology nodes, for the three different S3D variations.

Transistor-level and CMOS-level S3D: limited gains in cost and area scaling. The acceptance of a technology innovation by the semiconductor industry is heavily dependent on the manufacturing cost. Imec used its cost modeling framework to quantify the cost – at wafer level and at die level – for transistor-level and cell-level S3D. As a main conclusion, almost

no cost reduction is obtained compared to the traditional 2D 5nm and 3nm implementations. This is mainly due to extra process steps, such as additional steps in the layer transfer, that significantly add to the manufacturing cost. Also, depending on the implementation, some of the modules (such as gate patterning) would have to be performed twice, and this considerably adds to the processing cost of the dies.

Moreover, the gain in terms of area reduction is found to be less favorable for a S3D implementation compared to a 2D scaling scenario (**Figure 5**). In traditional scaling, the primary target is a 50% area shrink for both logic and SRAM bit cells. Typically, to achieve a 50% gain, a number of scaling boosters are applied, such as a reduction of the number of tracks (i.e., the number of middle layers within the standard cell). For example, to transition from the 5nm node to the 3nm node, the number of tracks is reduced from 6 tracks to 5 or 4 tracks. In order to have a comparable 50% area benefit with S3D for the 5nm node, only a very limited number of tracks (2 – 2.5) would be suitable. There is, however, a fundamental limit to the minimum number of tracks required for cell fabrication: at least 3 to 4 tracks are needed in order to interconnect the transistors (drain/source and gate/gate), and deliver power to the transistors. Consequently, due to the required track resource, an area gain of 50% is not feasible for the transistor- and cell-level S3D.

The imec team also investigated the benefits in terms of RC delay. When scaling continues, the resistance-capacitance product (RC) of the interconnect system strongly increases on account of the reduced cross section of the wires. It can be

expected that stacking transistors or cells brings some benefits, as the cross section of the wires can be relaxed to some extent. The cell-level S3D case indeed turns out beneficial in terms of RC delay, but the results very much depend on the process assumptions. For example, when the top tier is as performant as the bottom tier, and the metallization between the two tiers is in Cu, a 25% reduction in RC delay is expected for the S3D case compared with

a 2D implementation. When, however, the top tier performs less than the bottom tier due to process restrictions, and W, which is more resistive, is used between the two tiers, the reduction in RC delay is smaller. For example, a 15% reduction in RC delay is obtained when the top tier has about 20% lower drive compared to the bottom tier.

The results of the analysis very much depend on the process assumptions and the

technology nodes considered in the study. For example, in this study, the technology is assumed to be mainly front-end-of-line dominated, i.e., its performance is still heavily dependent on the parasitics in the device front end. However, with further scaling, technology might become more back-end-of-line dominated, with increasingly larger RC delay limiting the overall performance. In this case, because of gains in RC delay, S3D integration at the transistor level and cell level might turn out to be more beneficial.

Hybrid S3D: true benefits. True benefits are found for a hybrid S3D case, where the logic and memory part is scaled to the 3nm node in the bottom tier, and the remaining part (analog and I/O) is assumed to be manufactured in the 28nm technology node in the top tier (Figure 6). In this particular case, the non-scalable analog and I/O part takes up to 30% of the overall circuit area (see also Figure 2).

Despite a considerable increase in wafer cost, a 33% reduction in die cost compared to a 5nm 2D system-on-chip (SoC) implementation (with 125mm² die size) has been estimated. This can be understood as follows. In a traditional 2D implementation, all devices of the circuit need to be fabricated and optimized in the same advanced technology (e.g., 5nm FinFET technology). With hybrid S3D, the analog and I/O part can now be moved to a separate tier and fabricated with older technologies (28nm, in this case). This clearly makes the processing less complex and costly. The same holds for the interconnect schemes. The wiring that interconnects the transistors of the scalable parts can be optimized separately from the interconnects within the other tier, and the connection between them can be realized through a regular, dense interconnect scheme.

It should be noted that the resulting gains largely depend on the relative amount of the scalable vs. the non-scalable part. For example, the effective area reduction depends on the area of the largest component. In general, the smaller the non-scalable part, the smaller the overall benefit of the hybrid S3D implementation.

Through-Si-via-like processes: a brief comparison

Sequential-3D integration and through-Si-via (TSV)-like processes involve different technologies. TSV-like processes are used, for example, in 3D stacked ICs. As an example, these are realized through



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die-to-wafer stacking, and dies are interconnected using TSVs and microbumps. S3D, on the other hand, relies on sequential processes and layer transfer processes. In S3D, the alignment of transistors or cells is not defined by wafer alignment, but by lithography. As a consequence, S3D allows achieving smaller contact pitches (a few 100nm) as compared to TSV-like processing – where the diameter of the TSVs cannot be scaled below a certain limit. Therefore, S3D will provide the most benefit when a large number of interconnections between two subsystems is required. Overall, the final decision will very much depend on the circuit and the envisaged application. A typical application of a S3D implementation can be stacked SRAM cells, where transistors of neighboring cells are stacked on top of each other. The hybrid S3D approach will benefit the implementation of next-generation application hardware such as 5G and machine learning.

Summary

Sequential-3D integration (S3D) is perceived as a promising alternative to continue the benefits offered by semiconductor scaling. This integration technique involves the vertical integration of sequentially processed device layers, and comes in three different flavors – depending on where the partitioning and stacking takes place. In this article we have reviewed some of the solutions proposed by imec to tackle the technology integration challenges. Also, the benefits of the technology have been quantified through a power-performance-area-cost analysis. As a main conclusion, the largest benefit is found for a heterogenous S3D case, where the logic and memory part is using a scaled technology, and the remaining non-scalable part (analog in combination with I/O) is manufactured in a more relaxed 28nm technology in the top tier. S3D is found to be less straightforward for dimensional scaling (i.e., S3D at transistor or cell level). The relative benefits are largely dependent on the technology assumptions and on the component distribution.

Acknowledgement

These results have been presented at the 2017 IEDM conference, within the paper, “The impact of sequential-3D integration on the semiconductor scaling roadmap,” by A. Mallik, et al.

Biographies

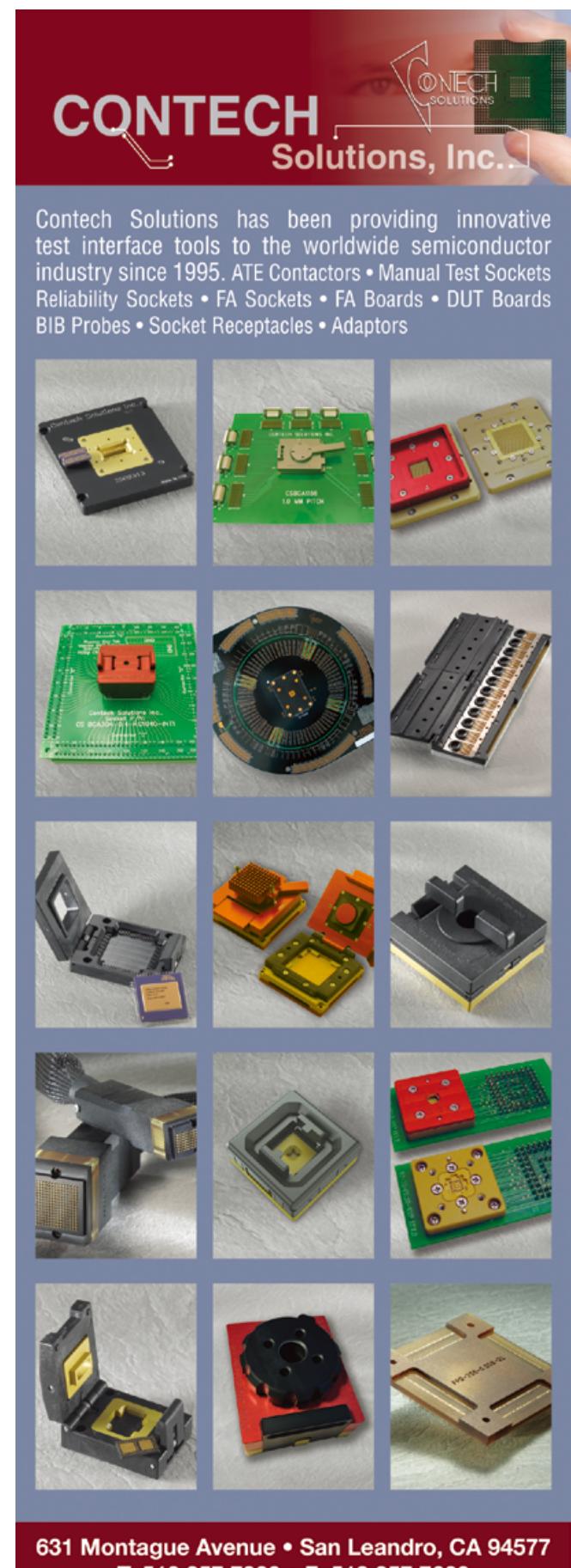
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Biodegradable and recyclable materials in semiconductor packaging

By Randy H.Y. Lo, Andrea S. Chen /Siliconware USA, Inc.]

Environmental consciousness has pushed reusability of materials in all aspects of society, whether it be recycling aluminum beverage cans and plastic water bottles, or re-purposing vehicle tires. To date, the impulse to go “green” in semiconductor packaging has been reflected by eliminating the use of lead (Pb)-based solders and by eliminating halogens like bromine and antimony as molding compound flame retardants. There has been minimal discussion, however, in the literature and trade press about recycling or taking apart said packages in a more environmentally-friendly manner. One logical reason is due to the compound nature of an IC package—with so many component elements and the use of many disparate materials, both organic and inorganic in nature.

Given the situation, there could be plenty of opportunities to utilize novel materials in order to make a semiconductor package into less hazardous waste. Areas of research include substituting the epoxies in molding compounds and die attach adhesives with biodegradable versions, or finding substitutes for silver flakes in conductive die attach, or perhaps using cellulose (paper)-based materials instead of fiberglass for substrates. As for conductive wiring, researchers might look to iron, which is considered non-toxic and more environmentally-friendly than gold, silver or copper. Or better still, one might look to an electrically-conductive polymer to create an all-organic materials package system.

This paper looks at some ideas and concepts that might be used to develop more environmentally-friendly engineered materials for semiconductor packages. The intent here is to consider various thought experiments on what might be possible in reducing waste in the area of electronics packaging.

Introduction

While societies in advanced economies have made moves towards recycling, reusing and being environmentally conscious in general, some things have proven more difficult than others in those efforts. For instance, materials used in semiconductor packaging tend not to fit any of the green categories, though there were successful steps to restrict the use of Pb and other hazardous materials through the implementation of the European Commission’s Restriction of Hazardous Substances (RoHS) Directive back in the early 2000s [1]. Admittedly, compliance to the RoHS directive took several years to implement, which continues to the present day as standards undergo continuous updates [2] (see the sidebar).

Given the implementation precedence noted above, it has been generally difficult to substitute more biodegradable and recyclable materials in a semiconductor package, both due to the stringent reliability requirements and the heterogeneous structures inherent in said packages, as illustrated in **Table 1** and **Figure 1**, respectively. Which is not to say that it should not be attempted. The intent of this paper is to look at the possibilities to improve the materials used in semiconductor packaging from an environmentally-friendly perspective.

Research into biodegradable and recyclable electronic materials

The literature and news reports show that there is considerable interest and research into the topic of environmentally-friendly electronic materials [5,6], but much of the existing work is looking into novel uses rather than replacing existing materials in established packaging bills of materials. Examples include soft and flexible disposable sensors that can be worn on the skin’s surface, perhaps to collect and store certain health data for a patient, or even implantable health sensors. In these cases, the materials would need to be biocompatible as well as biodegradable. The

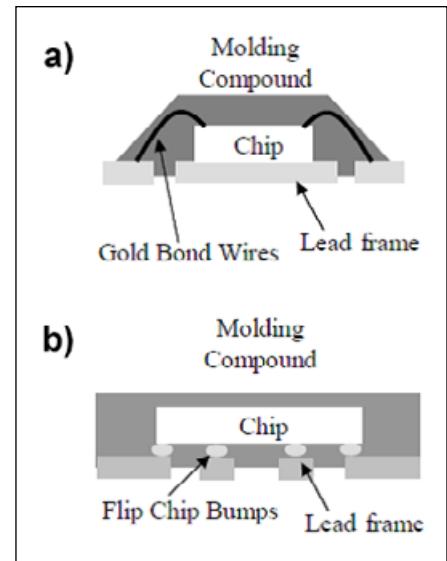


Figure 1: a) Generic cross-section illustration of a wire bonded quad-flat no leads (QFN) package; and b) of a flip-chip QFN [4].

end result is the ability to decompose the electronics into inert materials that are safe for the environment. One of the examples cited used a weak acid, like vinegar, to dissolve the conductive polymer into non-toxic components and using iron for the conductive circuitry because iron oxide (rust) is considered relatively non-toxic.

Also, it has been shown that carrier trays and tape for semiconductor packages can be made from biodegradable plastics without sacrificing functionality [7]. **Table 2** shows the attributes comparison for different types of biodegradable plastics. However, it may prove difficult to substitute biodegradable organic materials into the existing bill of materials used for semiconductor packaging, though perhaps not be impossible to find suitable substitutes for the epoxies used in molding compound, die attach adhesives or chip underfills. As mentioned previously, however, the performance requirements could prove daunting, whether technologically or economically, not to mention the additional complexity



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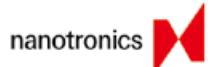
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| Test | Abbreviation | Goal | Test Conditions |
|--|--------------|--|--|
| Preconditioning | Precon | Mimics solder reflow board attachment for surface mount plastic packages. Done prior to other reliability tests. | Varies with anticipated floor life conditions. |
| High Temperature Storage | HTS | Induce bond pad metallization failures through heat and halides. | 1000 hours at 150°C or 175°C |
| Temperature Cycling | TC | Thermal stressing of the physical construction of the chip and package. | -65°C to 150°C for 1000 cycles in air |
| Thermal Shock | TS | Thermal stressing of the physical construction of the chip and package. | -65°C to 150°C for 100 to 1000 cycles in liquid |
| Temperature-Humidity-Bias | THB | Passivation Integrity against ionics under moisture and electrical bias conditions. | 1000 hours at 85°C/85%RH |
| Autoclave | ACLV | Passivation integrity against ionics under moisture conditions. | 168 hours or more at 121°C and between 15 to 30 psig. |
| Highly Accelerated Temperature and Humidity Stress Testing | HAST | An accelerated version of the THB test. | 110°C or 130°C under 85%RH and under vapor pressure for at least 96 or more hours. |

Note: RH = relative humidity

Table 1: Partial list of reliability tests for semiconductor packages [3].

| Type of Biodegradable Plastic | Aliphatic Polyesters | | | Starch-based |
|-------------------------------|-----------------------------|--------------------|-----------|---|
| | PHBV | PLA | PBS | PVA + Starch |
| Raw Materials | Biomass (microorganisms) | Biomass (plants) | Petroleum | Blend of petroleum and biomass (plants) |
| | Synthesis by microorganisms | Chemical synthesis | | |
| Mechanical Strength | Poor | Good | Good | Poor |
| Moisture Resistance | Good | Good | Good | Poor |
| Biodegradability | Excellent | Good | Good | PVA: Poor |

Notes: PHBV – Copolymer polyhydroxybutyrate-polyhydroxyvalerate

PLA – Polyactic acid

PBS – Poly butylene succinate

PVA – Polyvinyl alcohol

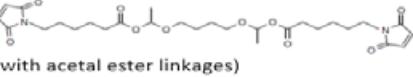
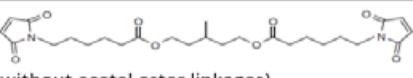
Table 2: Features of biodegradable plastics [7].

of finding substitutes for components like conductive silver flakes in die attach adhesives. Again, finding a comparable green material with similar electrical and mechanical properties that interacts well with the organic matrix compounds is the issue, so to speak.

Recyclable epoxy or thermoset materials

As already hinted, the organic constituent in most plastic packaging materials—molding compound, die attach adhesive, chip underfill—is an epoxy thermoset material. For example, the current types of epoxy materials used in commercial plastic packaging materials cannot be recycled or reused easily and ends up being disposed of as industrial waste, whether in landfills or in a chemical incinerator [8,9]. There has been recent research in this area in pursuit of recyclable, biodegradable thermosetting materials [10]. Some of the thermosetting materials discussed tended to degrade starting around 200°C, which might prove problematic during high-temperature solder reflow processes. **Table 3** compares two reworkable thermosetting underfill materials, specifically, adhesives based on maleimides and with/without acetal ester linkages, subject to die shear testing after curing, both at room temperature and after heating for rework [10]. Thermosetting materials utilizing maleimides have found uses in electronic packaging applications, partly due to their rapid cure and an ability to be reworked. The first cured material in **Table 3**, with the acetal ester linkages, shows the potential to be reworked after exposure to heat. On the other hand, the second material retains much higher adhesive strength even after heat exposure, suggesting poor reworkability.

More broadly, there has been work done towards commercialization of a recyclable epoxy system for industrial and consumer products, like surfboards and snowboards [11, 12]. For example, the RECYCLAMINE proprietary epoxy hardener, which allows for thermoset composites to be recycled without pyrolysis (breaking down plastics with elevated temperatures and typically in the absence of oxygen to prevent combustion [13]). In the case of RECYCLAMINE, the epoxy can be converted into a thermoplastic material that can be reused after a prolonged soak in a heated weak acid (vinegar) bath. Whether something similar can be found that can meet a semiconductor package's performance and reliability requirements is not yet known but appears worth investigating.

| Thermosetting Material | 25°C Adhesion (kg) | 150°C Adhesion (after exposure to 250°C for 2-min.) |
|--|--------------------|---|
|  (with acetal ester linkages) | 35.2 | 2.3 |
|  (without acetal ester linkages) | 44.9 | 18.6 |

Note: The second material's higher adhesive strength at 150°C also caused substrate damage during the die shear test.

Table 3: Die shear strength readings for re-workable thermosetting underfill materials [10].

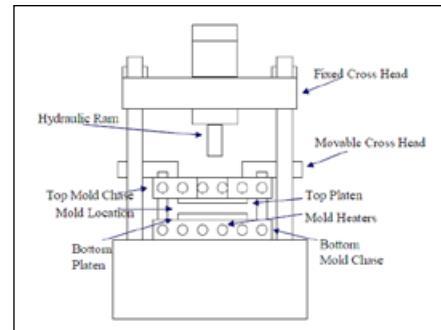


Figure 2: Transfer mold press [15].

Commercialization challenges

There are many issues that would need to be addressed before any potential material could be used commercially in a semiconductor package. Due to the heterogeneous nature of IC package technology, changes in one component may result in unintended effects or consequences to the entire system. Many of these issues have been alluded to earlier in this paper, but described next is an example with epoxy molding compounds. Epoxy molding compounds are generally an epoxy thermoset resin filled mostly with fused silica and some additives like catalysts and hardeners. In the past, small amounts of bromine (Br) and antimony (Sb) were added to the mixture as flame retardants but RoHS declared those elements as harmful to the environment and, therefore, needed to be eliminated.

The unintended consequences discussed above resulted from the alterations to molding compound formulations to make the end package RoHS-compliant. Those changes also made the molding compound “stickier” during the molding process, and thereby harder to remove the excess material from the mold surfaces and subsequently increased wear on metal mold platens and plungers (see **Figure 2** for an illustration of a transfer mold press) during production. This means that more time must be devoted to cleaning the mold press to prevent defective packages. Additionally, the working life of the mold surfaces in contact with the molding compound are all reduced, which in turn reduces manufacturing efficiency and increases operation costs [14].

Therefore, perhaps the lesson here is that the path to a more environmentally-friendly end product may be filled with unanticipated costs and issues. That should not preclude pursuing research and development to find such materials to be used in semiconductor packaging, but researchers should be aware of the risks and issues that can come from altering a stable system. Reducing e-waste and harm to the environment are all admirable goals, but they do not come without risks or a price.

Materials used in semiconductor packaging [21]

This section lists different types of materials used in semiconductor packaging.

| | |
|-------------------------------|---|
| Bonding wires | Provide the electrical pathway from the IC to the package leads. Copper and gold are commonly used for wire materials. |
| (Metallized) bumps | Creates an electrical and physical connection between IC and a lead frame or substrate in lieu of wire bonding. Used for flip-chip (FC) packaging or wafer-level chip-scale packaging (WLCSP). Metallization can include solder—tin-silver (Sn-Ag) for example—or copper pillars with a thin layer of solder plated on top. |
| Die attach adhesive | Material used to affix the IC to a lead frame or substrate. Organic-based adhesives full of a thermally and electrically conductive filler, like silver flakes, are commonly used. |
| Heat spreaders/sinks/slugs | Piece of metal added to a package to dissipate more heat away from the IC than the standard packaging BOM can do so alone. |
| Lead frame | Provides a metal framework and electrical connections from the IC to the PCB. Often also provides a conduit for heat transfer from the IC. Copper and Alloy-42 (iron-nickel or Fe-Ni) are commonly used metals for lead frames. |
| Molding compound | Epoxy resins typically full of silica filler and small amounts of other additives such as carbon black for color. The silica acts to lower the CTE to better match that of the lead frame or substrate. |
| Substrate | In this context, the substrate is an epoxy-impregnated glass fabric sandwiched with conductive layers (often copper) etched out with lines and circuitry—much like a PCB except for one or more bare ICs. One of the epoxy resins used is bisphenol A triazine (BT). Serves the same purpose as a lead frame but with a higher density of electrical and thermal connections. |
| (Chip) underfill | Can be used in flip-chip and wafer-level packaging applications instead of molding compound. Material fills the gap created by bump connections between the IC and substrate. Much like molding compounds, underfills are typically epoxy-based and filled with fused silica. |
| Peripheral Item Carrier trays | Plastic trays to safely store the finished individual packages for shipping as well as handling on the manufacturing floor. |

Table S-1: Materials used in semiconductor packaging [21].

Molding compounds, die attach adhesives and underfills

A molding compound's properties are a balance between ease of use in a high-volume manufacturing environment and its relationship to the overall package's performance and reliability. **Table S-2** shows how much effect each ingredient in a molding compound has on its manufacturing performance and reliability.

Die attach adhesives are similar to molding compounds, usually consisting of a liquid epoxy resin, a filler material, reactive epoxy diluent or solvent, catalyst, and hardener.

Finally, chip underfill materials are similar to both die attach adhesives and molding compounds, typically being a liquid epoxy resin filled with fused silica and additives such as catalysts, hardeners, and coloring agents.

| Property | Filler (>70%) | Epoxy (~10%) and Hardner (~7%) | Elastomer (<5%) | Catalysts | Flame Retardants and Scavengers | Waxes and Oils |
|--|---------------|--------------------------------|-----------------|-----------|---------------------------------|----------------|
| Viscosity (rheology) | --- | +++ | | --- | | |
| Cure Rate (Productivity) | | +++ | | +++ | | |
| Mold Cleanliness | | | 0 | | | 00 |
| Mold Release | --- | -- | | | +++ | |
| Stress in Device | + | | +++ | | | |
| Glass Transition Temperature (T_g) | | 0 | | | | |
| Strength | ++ | 0 | - | | | |
| Moisture Absorption | +++ | --- | - | 0 | | 0 |
| Thermal Conductivity | +++ | | | | +++ | |
| Combustibility | +++ | * | | | | |
| Electrical Reliability | + | 0 | - | - | 0 | 0 |

Table S-2: Influence of molding compound ingredients on physical properties [22].

Summary

The area of recyclable and biodegradable materials for use in semiconductor packaging is relatively unexplored to date. There have been some novel concepts explored in recent literature, but less so in regards to supplanting some, if not all of the typical bill of materials used. Granted, the performance and reliability requirements for most standard forms of chip packages may render incorporating green materials more difficult. And, green materials are not without their own issues and may result in unintended consequences at some process step or interactions with another package component. But with the number of electronic devices being created and sold growing yearly, the issue of dealing with these products when no longer needed or useful will need to be addressed sooner or later.

Using the example of China, the government came out with its “National IC Industry Development Guidelines” in 2014 and its “Made in China 2025” industrial policy in 2015 [16]. Both initiatives contain the goal of increasing

the percentage of domestically-produced semiconductors and making China a global force in ICs through the use of the \$150 billion National IC Industry Investment Fund—also known as “Big (investment) Fund”—to help local companies compete with foreign rivals, as well as boosting internal manufacturing capabilities [17]. Currently, China consumes nearly 45% of the world’s semiconductor output – currently valued at nearly \$340B – but domestic IC production is a small fraction of that, perhaps only 15-20% [18]. The balance must be imported, which has made ICs the leading import category into China, topping even crude oil or iron ore [19]. Given these statistics, China’s internal semiconductor manufacturing still accounts for tens of millions of packaged IC units produced per year. If China were to fulfill even part of its Made in China 2025 goals, that could mean hundreds of millions of chips undergoing the packaging process domestically, which will then ultimately need to be disposed or recycled when the electronic end products are broken or obsolete. And this does not take into

account all the waste materials generated in the initial manufacturing steps. Therefore, innovations in materials used in semiconductor packaging could prove to be some of the important and necessary steps in becoming a more environmentally-friendly process all around.

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Biographies

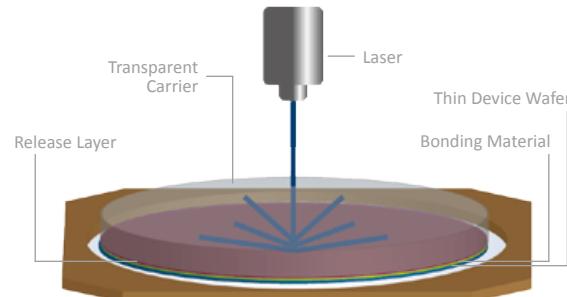
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Challenges of flip-chip MEMS microphones: from state-of-the-art to small housing sizes

By Sebastian Walser, Anton Leidl, Wolfgang Pahl [EPCOS, a TDK Group Company]

Today, microelectromechanical systems (MEMS) are commonly used as sensors in numerous electronic consumer products. The main reason for this is an accurately controlled silicon micromachining technology in combination with low cost at mass production. Currently, in mass production, tight sensitivity distributions down to $\pm 1\text{dB}$ or beyond can be reached [1]. Especially for high-volume consumer applications (e.g., mobile phone communication), capacitive silicon MEMS microphones have become state-of-the-art and reach high signal-to-noise ratios (SNR) of approximately 65dB(A) with sensitivities of -38dBV/Pa and component sizes of approximately $3.5 \times 2.6 \times 1.0\text{mm}^3$ [2,3]. With the increasing requirements of smartphone technology, a demand of the MEMS microphone market is a continuous reduction in size with the current acoustic performances. It will be a challenge for the next few years to minimize the MEMS microphone package size without downgrading the electroacoustic microphone characteristics.

Classification of MEMS microphones

Today the most popular commercial MEMS microphone principle is the capacitive transducer. Such microphones consist of two chips: a sensor chip and an application-specific integrated circuit (ASIC) chip. Both chips are integrated in a surface-mount device (SMD) package. In general, the sensor chip has a movable membrane and a rigid perforated back-plate electrode. Within this structure, an incoming sound wave results in a capacitive change and will be converted by an ASIC into an electrical audio signal.

During the last few years, different package variants established themselves in the commercial market. A classification of these MEMS microphones can be done on the basis of the sound port (**Figure 1**). If the sound pressure gets through a hole in the metal lid to the sensor, the microphone is called top-port (**Figure 1a**). Otherwise, if the sound pressure gets through a hole in the substrate, the

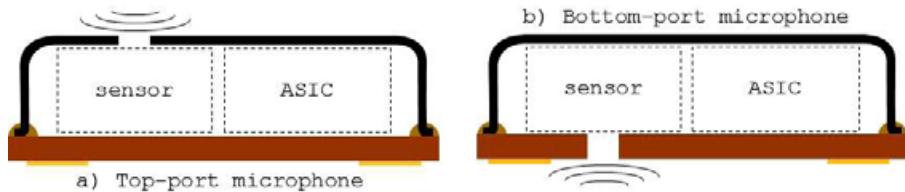


Figure 1: Classification of MEMS microphones on the basis of sound port: a) top-port, and b) bottom-port (by using image source [6]).

microphone is called bottom-port (**Figure 1b**). In general, both classifications reach a similar electroacoustic performance parameter with similar package sizes.

In the case of bottom-port MEMS microphones, there are two different packaging technology approaches on the market. Depending on the internal connection, the MEMS microphone can be built up by wire bond or flip-chip (**Figure 2**). Both cross sections show a carrier substrate with electric contact pads and a sound hole. In each case, a sensor chip and ASIC chip are mounted on the carrier substrate. For flip-chip assembly, the mechanical and electrical connection of both chips is done by soldering (**Figure 2a**). An example of a flip-chip MEMS microphone is presented by G. Feiertag, et. al in [4]. In a wire bond assembly (**Figure 2b**) the mechanical connection of both chips to the carrier substrate is done by adhesive. Due to the electrical contact pads on the sensor and ASIC, both chips are mounted reversed to the flip-chip assembly, and the electrical connection is done by wire bonding. An example of a wire-bond MEMS microphone is presented by A. Dehe, et. al in [5].

The main advantage of a flip-chip MEMS microphone package is the space-saving design [4]. In comparison to the flip-chip package, the wire bond assembly needs additional spaces on the carrier substrate for the wire bonds (see **Figure 2**). Assuming a package size of $3.35 \times 2.5 \times 1.0\text{mm}^3$, a sensor chip size of $1.45 \times 1.45 \times 0.45\text{mm}^3$ and an ASIC chip size of $1.00 \times 1.45 \times 0.30\text{mm}^3$, a flip-chip MEMS microphone has a front volume of around 0.2mm^3 and a back volume of around 3.4mm^3 . The front volume includes everything from the sound hole to the membrane. The back volume includes everything behind the membrane. In comparison to a wire bond assembly, the sensor cavity increases the back volume of around 0.5mm^3 . Assuming the same sensor, ASIC and package size — and without taking the polymer foil thickness into account — the back volume of a wire bond package can be calculated as follows: $3.4\text{mm}^3 - 0.5\text{mm}^3 + 0.2\text{mm}^3 = 3.1\text{mm}^3$. This corresponds to a decrease in the back volume of around 8.8%. A smaller back volume leads to a larger restoring force to the membrane. This results in a smaller deflection of the

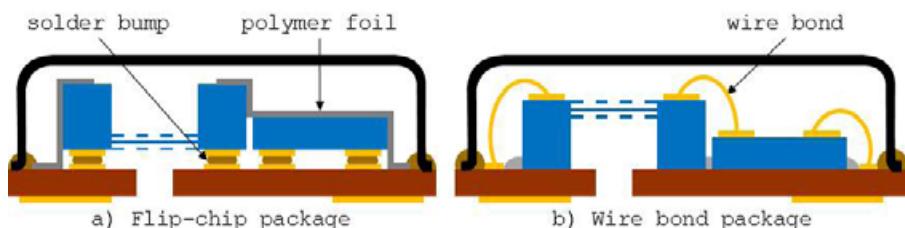


Figure 2: Classification of bottom-port MEMS microphones on the basis of packaging technology: a) flip-chip package, and b) wire bond package (by using image sources [3] and [6]).

membrane, which is equivalent to a lower sensitivity. Since the back volume has small influences to the noise properties, a large back volume increases the SNR leveraging the sensitivity [3,6].

One main aspect in terms of MEMS microphone functionality is the acoustical separation of front and back volume. Without a separation of the two volumes, the sound pressure applies to both sides of the membrane and leads to lower membrane displacement. A static pressure exchange between front and back volume is given by small holes in the membrane. These vent holes are also responsible for the low-pass filtering of the sound pressure. In view of a wire bond MEMS microphone design, the acoustical separation of front and back volume is done by enclosing adhesive between the sensor chip and the substrate. Due to the solder bumps in a flip-chip process, there is a gap between sensor chip and carrier substrate. As a consequence, the incoming sound pressure reaches both sides of the membrane. In view of a flip-chip MEMS microphone design,

the acoustical separation of front and back volume is one of the key challenges [3].

Flip-chip MEMS microphone

To avoid the conjunction of the front and back volume in a flip-chip MEMS microphone design, the separation can be done by a polymer foil, as described in [4]. The drawback of covering the sensor by a polymer foil is to limit the back volume in relation to the sensor chip height. A solution to eliminate this limit is to open the sensor chip on the covered side and close the complete microphone by a metal lid (**Figure 2a**). This allows for defining the back volume size by the metal lid. A detailed production process of such a flip-chip MEMS microphone is shown in **Figure 3**. The process is based on a MEMS microphone that is presented earlier in [3]. All subsequent production process steps are performed on a panel. For simplification, the steps are shown on single devices [3].

The MEMS microphone is built on a high-temperature, co-fired ceramic (HTCC) carrier

substrate (**Figure 3a**). The ceramic comprises the sound holes, the contact pads and the conducting paths. In contrast to the ASIC chip, the stencil printing process does not allow the addition of the solder balls directly to the sensor chip without contaminating the membrane. For this reason the lead-free solder balls for the sensor chip are applied on the ceramic substrate. In the next step, the sensor chips are positioned by a pick-and-place process onto the ceramic (**Figure 3b**). Afterwards, the panel passes through a reflow process to solder the chips onto the ceramic substrate. The mounting of the ASIC chips occurs similarly to the sensor chips. The ASIC chips with solder balls are positioned by a pick-and-place process onto the ceramic (**Figure 3c**). Afterwards, the panel passes through a second reflow process to solder the chips onto the ceramic substrate [3].

When using a polymer foil to separate front and back volume, the sensor back cavity has to be closed in preparation. Otherwise, the polymer foil sags into the sensor chip back cavity during the vacuum lamination process. To avoid this, the sensor back cavity is closed by a rigid lift-off foil and therefore, the rigid foil is laminated onto the panel only to the taller sensor chips, as shown in **Figure 3d**. To remove the not required lift-off foil parts, a circular laser cut onto the sensor chip is made (**Figure 3e**). Afterwards, the redundant parts of the lift-off foil are peeled off, and the microphone panel with closed sensor chips still remains, as shown in **Figure 3f** [3].

To separate front and back volume, a soft polymer foil is laminated over the sensor and ASIC chip (**Figure 3g**). This process separates front and back volume by sealing between polymer foil and ceramic. The front volume is defined by the solder bump height and the surface area beneath the two chips. For the dicing and capping process, the foil has to be removed by a laser ablation process in the dicing streets and on the cap assembly region (**Figure 3h**). For increasing the microphone back volume, the sensor cover has to be removed. Thereafter, a second circular laser cut onto the sensor chip is made (**Figure 3i**). Then the two foils on the top of the sensor chip can be removed (**Figure 3j**) [3].

The microphone is closed by a metal lid. The metal lid defines the back volume, protects from external influences, and shields from electromagnetic interferences. An electric conductive adhesive is then dispensed gapless around the two chips onto the provided electrical contact surface (**Figure 3k**). Afterwards, the metal lid is assembled, as shown in **Figure 3l**, and within a thermal

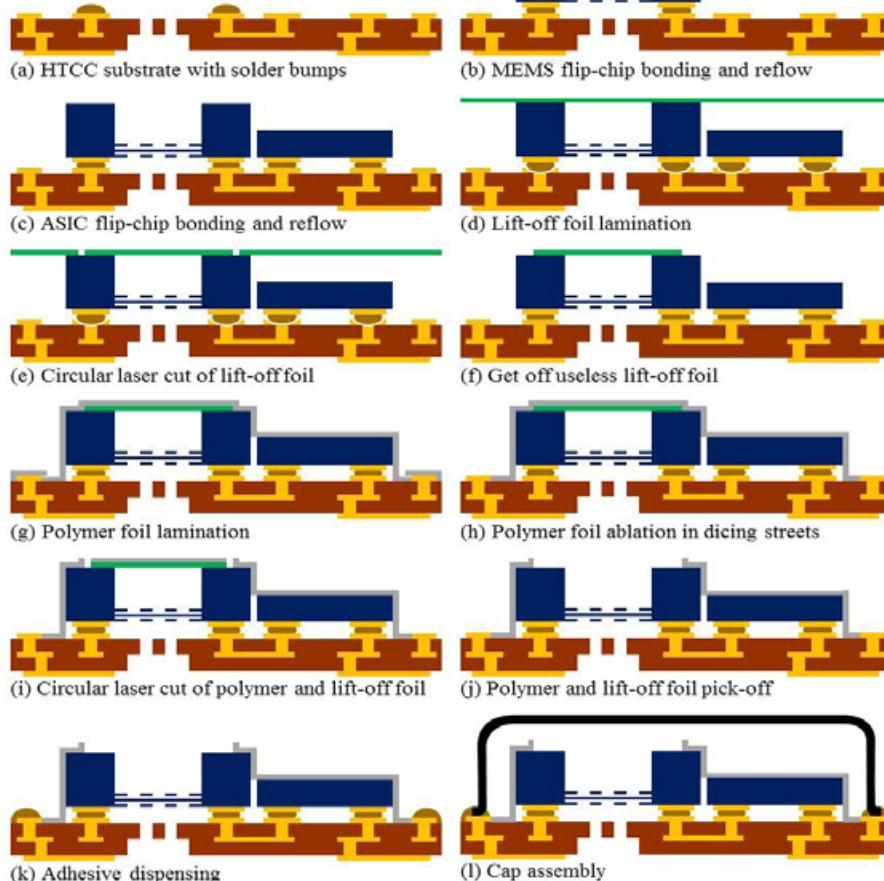


Figure 3: Backend production process steps of a flip-chip bottom-port MEMS microphone (by using image sources [3] and [6]).

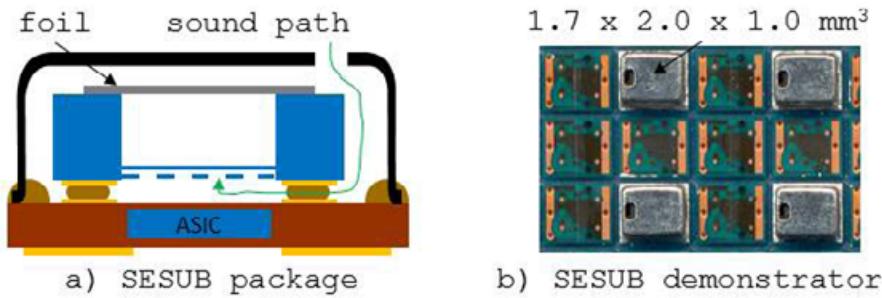


Figure 4: SESUB top-port MEMS microphone package: a) cross section sketch of a SESUB package, and b) the first SESUB demonstrator.

| Name | Dimensions | 1kHz Sensitivity | SNR in dB(A) |
|----------------------|-----------------------------|------------------|--------------|
| Device A | 3.10 mm x 2.50 mm x 1.00 mm | -42 dBV/Pa | 59 dB(A) |
| Device B | 3.20 mm x 2.20 mm x 0.90 mm | -42 dBV/Pa | 59 dB(A) |
| Device C | 3.50 mm x 2.65 mm x 1.00 mm | -38 dBV/Pa | 65 dB(A) |
| Device D | 3.76 mm x 2.24 mm x 1.10 mm | -42 dBV/Pa | 59 dB(A) |
| Device E | 3.76 mm x 2.95 mm x 1.10 mm | -42 dBV/Pa | 59 dB(A) |
| "SESUB demonstrator" | 2.00 mm x 1.70 mm x 1.00 mm | -38 dBV/Pa | 59 dB(A) |

Table 1: Listing of bottom-port analog MEMS microphones available on the market at present compared to the first SESUB demonstrator.

process, the adhesive is cured. The separation of the microphones on a panel is done by a dicing process [3].

The challenge of small housing sizes

A particular further challenge is to reduce the MEMS microphone package size without downgrading the SNR significantly. This concerns both MEMS microphone classifications: the bottom-port as well as the top-port. An interesting approach for reducing the microphone package size is to integrate the ASIC into the substrate (**Figure 4a**). This can be achieved by using the semiconductor embedding substrate (SESUB) technology by TDK. In this process, the sound pressure enters via the metal cap and reaches the membrane beneath the flip-chip-mounted sensor. The sensor cavity is closed by a foil and constitutes the microphone back volume. Using this process, a first top-port MEMS microphone demonstrator was built up with a small housing size of $1.7 \times 2.0 \times 1.0\text{mm}^3$ (see **Figure 4b**). The SESUB MEMS microphone demonstrator fulfills a SNR specification of 59dB(A) with a sensitivity of -38dBV/Pa.

Currently available analog top-port MEMS microphones have component sizes of around $3.0 \times 2.5 \times 1.0\text{mm}^3$. **Table 1** shows a comparison table in relation to dimensions, sensitivity and SNR. For a specified 1kHz sensitivity of -42dBV/Pa, these microphones reach an SNR of 59dB(A).

High SNR microphones up to 67dB(A), with a specified 1kHz sensitivity of -38dBV/Pa, have package sizes of $3.3 \times 2.65 \times 0.98\text{mm}^3$. However, with the first SESUB MEMS microphone demonstrator, the package volume can be reduced from 7.75mm^3 to 3.4mm^3 when compared to the smallest available package size. This corresponds to a reduction in package area of around 40% compared to the currently available analog top-port MEMS microphones.

Summary

As described above, the sensor and the ASIC chips are integrated by a flip-chip process into an SMD package. After the flip-chip bonding, the acoustic front and back volume are separated by a polymer foil. A large back volume can be reached by exposing the sensor back cavity and covering the back volume by a metal lid. Compared to a wire bond design, the presented flip-chip MEMS microphone increases the back volume by approximately the sensor cavity size. This allows the sensor to reach an SNR of around 65dB(A) with a specified sensitivity of -38dBV/Pa in a package size of $3.35 \times 2.5 \times 1.0\text{mm}^3$ [3].

By using the SESUB technology, it is possible to shrink current packages without downgrading the back volume significantly. A first SESUB MEMS microphone demonstrator allows reducing the package area to 3.4mm^3 . Compared to the smallest

currently available analog top-port MEMS microphone, this corresponds to a reduction in package area of 40%. With the increasing requirements of smartphone technology, a demand of the MEMS microphone market will be to achieve a continuous reduction in size. Therefore, the SESUB approach can help to minimize the microphone package size without downgrading the electroacoustic microphone characteristics significantly.

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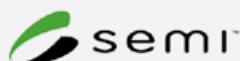
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INDUSTRY NEWS



ASE Industrial Holding, Co., Ltd. completes equity exchange on the Taiwan (TWSE) and New York (NYSE) Stock Exchanges

ASE Industrial Holding Co., Ltd. is jointly established by the combination of Advanced Semiconductor Engineering, Inc. and Siliconware Precision Industries Co., Ltd (SPIL). ASE Industrial Holding will enhance research and development capability, expand global market footprint, contribute advanced technical support for next-generation applications, and provide miniaturized, high-quality, highly integrated, and fast time-to-market services to all customers.

ASE Industrial Holding is the leading provider of semiconductor manufacturing services in assembly and test. The company develops and offers complete turnkey solutions covering front-end engineering test, wafer probing and final test, as well as IC packaging, materials and electronic manufacturing services through USI. By integrating the resources of each business entity, the new holding company remains committed to long term partnerships for a sustainable future.

ASE Industrial Holding's global manufacturing facilities are strategically located in Taiwan, China, South Korea, Japan, Singapore, and Malaysia, Mexico as well as the Americas and Europe, with 90,000 employees.

Milestones

- In June, 2016, ASE and SPIL entered into the Joint Share Exchange Agreement, pursuant to which, the board of directors from ASE and SPIL approved the formation of ASE Industrial Holding Co., Ltd.
- On February 12, 2018, ASE and SPIL respectively held Extraordinary General Meetings and each approved the proposed Joint Share Exchange plan, pursuant to which, the to-be-established ASE Industrial Holding will acquire 100% of shares of both ASE and SPIL.
- On April 30, 2018, ASE Industrial Holding listed on the Taiwan Stock Exchange (TWSE code: 3711) and

New York Stock Exchange (NYSE code: ASX) through the issue of ADR.

Members of ASE Industrial Holding Co., Ltd.

Advanced Semiconductor Engineering Inc. & Siliconware Precision Industries Co. Ltd., the leading companies of semiconductor assembly and test services. USI Inc., a leading electronic manufacturing service provider.



Cohu to acquire Xcerra

Cohu, Inc. (NASDAQ:COHU) and Xcerra Corporation (NASDAQ:XCRRA) announced they have entered into a definitive merger agreement pursuant to which Cohu will acquire Xcerra for a combination of cash and stock. The acquisition is expected to make Cohu a global leader in semiconductor test, with combined sales for Cohu and Xcerra in excess of \$800 million for the last twelve months.

Upon the closing of the transaction, Xcerra shareholders will be entitled to receive \$9.00 in cash and 0.2109 of a share of Cohu common stock, subject to the terms of the definitive agreement. Based on the closing price of Cohu common stock as of May 7, 2018, the transaction values Xcerra at \$13.92 per share, or approximately \$796 million in equity value, with a total enterprise value of approximately \$627 million, after excluding Xcerra's cash and marketable securities net of the debt on its balance sheet as of January 31, 2018. The transaction value represents a premium of 8.4% to Xcerra's closing price on May 7, 2018, and a premium of 15.4% to Xcerra's 30-day average closing price.

"This proposed acquisition is a powerful combination of two complementary companies that will accelerate our strategy to diversify our product offerings and strengthen Cohu's position as a global leader in back-end semiconductor equipment. The depth and breadth of the combined product portfolios, engineering and product development resources, as well as the global customer support platforms will enable us to deliver comprehensive semiconductor back-end solutions that better meet the future needs of our customers," commented Luis Müller, Cohu's President and CEO. "The acquisition

of Xcerra increases our addressable market to approximately \$5 billion across handlers, contactors, test and inspection, further strengthening our ability to fully capitalize on the secular growth opportunities in the automotive, IoT, industrial and mobility markets. We are excited to welcome the Xcerra team to Cohu and look forward to an efficient completion of the transaction, with a focus on delivering long-term value to our customers, employees and shareholders."

The transaction is expected to be immediately accretive to non-GAAP earnings per share and generate over \$20 million of annual run-rate cost synergies within 2 years of closing, excluding stock-based compensation and other charges. Cohu intends to fund the cash payable to Xcerra shareholders with a combination of cash on hand from the combined companies' balance sheets, and approximately \$350 million in debt financing. The transaction is expected to close in the second half of calendar year 2018, subject to approval by both companies' respective shareholders, antitrust regulatory approvals and other customary closing conditions. Xcerra shareholders are expected to own approximately 30% of the combined company upon the closing of the transaction. The transaction has been unanimously approved by the Boards of Directors of both companies. Luis Müller will remain President and Chief Executive Officer and lead the combined company, and Jeff Jones will continue to serve as vice president of finance and chief financial officer. Two members of Xcerra's board of directors will join Cohu's board upon the closing of the transaction.



EV Group begins construction of new manufacturing III building to expand production capacity

EV Group (EVG) announced that it has started construction work for the next expansion phase of its corporate headquarters. The new, state-of-the-art building will house EVG's "Manufacturing III" facility, which will more than double the floor space for the final assembly of EVG's systems.

"With our innovative manufacturing solutions for the high-tech industry as well

as new biomedical applications, we operate in very dynamic markets with great future prospects," stated Dr. Werner Thallner, Executive Operations and Financial Director at EV Group. "In light of the high-capacity utilization in all areas of our existing facilities, as well as the positive market outlook, we decided to implement our plans for building our Manufacturing III facility this year. This will support our long-term growth targets at our corporate headquarters in St. Florian am Inn."



From left to right: Paul Lindner, Hermann Waltl, Erich Thallner, Aya Maria Thallner, Dr. Werner Thallner / EV Group Executive Board

The new Manufacturing III building, adjacent to the new test room site that was opened just a few months ago, will be built next to the river Inn. The building will provide about 4,800 square meters of additional space in total, which will benefit not only manufacturing, but other departments as well. In addition to an expansion of warehouse space, a new delivery area with a dedicated packaging site designed for cleanroom equipment will be created, along with an airfreight security zone and new truck loading docks for the shipment of the completed systems to EVG's worldwide customers. The construction of the new Manufacturing III building is set to be completed in early 2019.

ASM  **Pacific Technology**

ASM Pacific Technology Ltd. completes acquisition of AMICRA Microtechnologies GmbH

ASM Pacific Technology Ltd. ("ASMPT") announced that it has completed its acquisition of 100% of the shares of AMICRA Microtechnologies GmbH ("Amicra"). Amicra is a leading supplier of high-precision die bonders for the photonics and advanced packaging markets. The transaction, which

completed on April 4, 2018 will bring about a strengthened business, well-placed to serve not only the fast growing silicon photonics assembly equipment market, but also the wider high-precision flip-chip and die bonding markets.

Headquartered in Singapore and listed in the Hong Kong Stock Exchange, ASMPT is

the world's largest back-end semiconductor equipment supplier and SMT solutions provider. ASMPT will rename Amicra to ASM AMICRA Microtechnologies GmbH as it integrates Amicra into ASMPT's back-end equipment segment.

"We are excited about this strategic investment," said Mr. Lee Wai Kwong, CEO



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of ASM Pacific Technology. "Amicra's sub-micron high-accuracy die bonder is complementary to the Group's existing product portfolio. Amicra has a leading position in the photonics market, which the Group believes is of high-growth potential. I am confident that this combination will further strengthen our future growth opportunities and help to deliver even higher value-add to our customers."

"Following our increasing penetration of markets for high precision die attach, especially in the rapidly growing area of silicon photonics manufacturing, it makes a lot of sense to merge with a strong strategic partner to better support our growing international customers' base," noted Rudolf Kaiser, Managing Director of Amicra. "With their scale and established international supply chain, sales channel and customer support capability, the merger with ASMPT will allow us to take next steps in the further development of our business. I am happy for Amicra and our customers and I am excited about the opportunity to work with ASMPT."

ASM Pacific Technology

ASM Pacific Technology Ltd. signs agreement to acquire TEL NEXX, Inc.

ASM Pacific Technology Ltd. (ASMPT) announced that it has signed a definitive agreement with Tokyo Electron Limited (TEL) to acquire TEL NEXX, Inc. (NEXX). The deal is expected to close when approvals from the authorities have been received. The acquisition is another major step by the Group in pursuing its growth strategy of tapping into new high-growth markets and expanding their product offerings to the semiconductor advanced packaging market.

Established in 2001, NEXX is an industry leader in the advanced packaging market and has strong technological capabilities in the highly specialized electrochemical deposition (ECD) and physical vapor deposition (PVD) technologies. This new business acquisition will be subsumed under the back-end equipment segment of ASMPT.

"This strategic acquisition complements our current offerings in advanced packaging

applications and establishes ASMPT as a premier interconnect technology company, while supporting our commitment in driving innovation and delivering the highest value and innovative solutions to our customers," said Lee Wai Kwong, CEO of ASMPT. "By combining NEXX's highly specialized ECD and PVD technologies, we see tremendous opportunity to grow our business in the advanced packaging market, which is being driven by the dawn of the data-centric era."

"ASMPT offers an exciting opportunity for NEXX to boost and expand its product offerings in advanced wafer-level packaging, ECD and PVD," said Toshiki Kawai, President and CEO of TEL. "TEL believes that NEXX will benefit from greater synergies with ASMPT's outsourced assembly and test customers."

"With the demand for semiconductor devices at a historical high, we are looking forward to an increased global customer footprint with ASMPT, as well as expanded sales and service capabilities for our customers," noted Tom Walsh, President of NEXX.

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