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REVIEW®

January-February 2010



- Wafer-Level Packaging Reliability
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January-February 2010

Volume 14, Number 1



Tessera Wafer-Level Camera (WLC) technologies, including wafer-level optics and image sensor packaging, enable manufacturers to significantly advance the integration of miniaturized cameras in cell phones, personal computers, security cameras and other portable devices. Cover Artwork courtesy of Design 2 Market. [www.design2marketinc.com](http://www.design2marketinc.com)

## Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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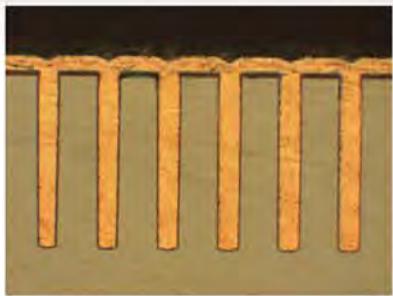


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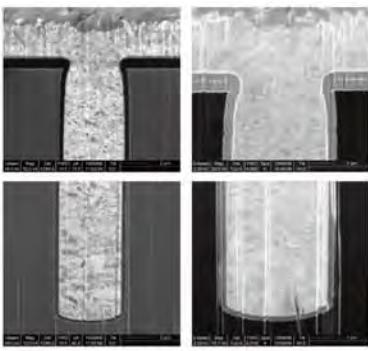
Hitting the home run in TSVs

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# FROM THE PUBLISHER



## New Year's Resolutions

By Kim Newman

The first issue of a new year is always exciting because it gives us at *CSR* a chance to share our New Year's thoughts and resolutions with you. As you join us for 2010, we are cautiously optimistic that it will be a year that sees positive growth as companies pursue the industry's hallmark R&D, introduce innovative products, and create additional applications for legacy lines.

We at *Chip Scale Review* resolve to continue to grow, expanding our coverage to keep pace with all the developments in the industry that relate to chip scale technology. As you probably noticed, this issue's cover (photo courtesy of Tessera) depicts Wafer-Level Camera (WLC) technologies, including wafer-level optics and image sensor packaging, which enable manufacturers to significantly advance the integration of miniaturized cameras in cell phones, personal computers, security cameras and other portable devices. You can read more about the technology for these mobile devices in our article entitled *Development of Wafer Level Packages of Normal and High Pin Count Devices for Mobile Applications* in this issue.

We also resolve to continue to introduce ourselves to new readers, whether they are new engineers learning the industry, veterans who have shaped it, or those who are now bringing their knowledge of another segment of electronics to the exciting field of chip scale packaging.

And we resolve to engage them with articles and columns that cover new, existing, or changing technologies, such as this month's article on WLP-TSV Interconnects. You'll also find a feature that looks at 3D Technology Trends, titled *3D - Talking About a Revolution*.

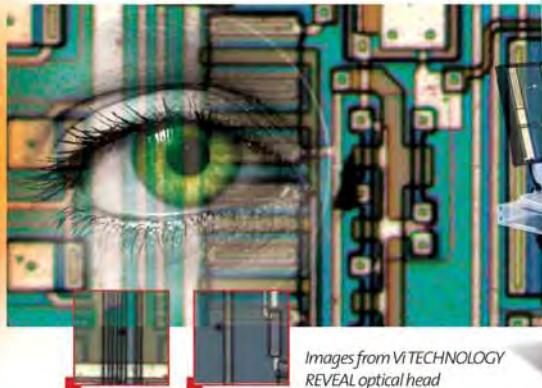
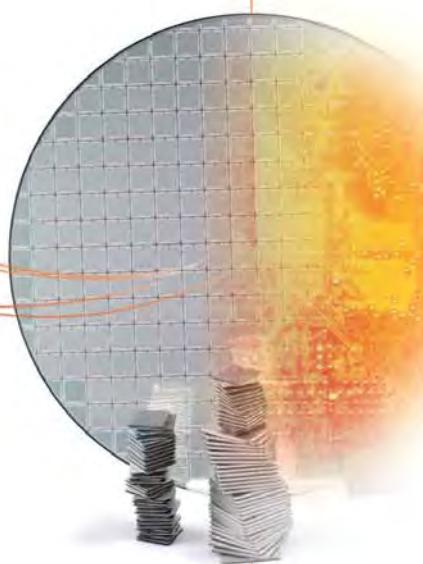
Of course you need good device testing, 3D or otherwise, so in this issue we are publishing the International Burn-in and Test Socket Directory, making it an issue you will definitely want to save. By the way, *Chip Scale Review* is proud to be one of the sponsors for this year's BiTS Workshop in Mesa, AZ which runs from March 7<sup>th</sup> through 10<sup>th</sup>. Stop by and say hello.

And, with budgets still tight, just in case you wonder about when to buy or how to select used versus new equipment, we have an article on that too. So whether you're an industry veteran or a new engineer wanting to learn the ropes, welcome to *Chip Scale Review* for 2010. Glad to have you aboard! 

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# EDITOR'S OUTLOOK



## Is It Alchemy?

By Ron Edgar [redgar@chipscalereview.com](mailto:redgar@chipscalereview.com)

**I**t always amazes me when I gaze at that innocent-looking IC package that so much function could live in such a small space. My youth was in the final, halcyon days of the vacuum tube, the transistor radio was all the rage, and my college computer heated the physics building. Within that space we are outgrowing the abilities of the X and Y axes and, like Manhattan, are developing the Z axis. And that IC package is growing ever smaller and more complex.

How far we have come in the 60 or so years since the transistor was developed at Bell Labs. The whole field of solid-state physics has shrunk functionality into the micro-devices we know today and new developments zoom from college lab to Main Street in the blink of an eye.

But how did this happen? The late 40s and early 50s saw Shockley and many others at Bell Labs hard at work developing transistor technology. Then, in a series of pivotal events in late 1951 and 1952, Bell released the technology to the world. Companies from the US and abroad came to Bell and learned how to make transistors. It cost each company a licensing fee of \$25,000. Large companies like IBM to (then) small companies like TI paid the price of admission, then went off and made their own, improving on the original ideas and adding their own. TI was among the first to make transistors for radios that appeared in the mid-50s.

The next paradigm shift got rid of most of the components that needed to surround transistors and is credited to two independent developments in the late 50s, one by Jack Kilby of TI and the other

by Robert Noyce of Fairchild. In somewhat different ways, they invented the Integrated Circuit. In a single stroke they got rid of many resistors, capacitors, and wires thus enabling even more miniaturization. And chip packaging as we know it was created.

In 1968, Intel was born. From the original model 4004 with about 2,500 transistors to the latest multi-core microprocessors exceeding 2 billion, Moore's law has held good. The microprocessor led the charge into mainstream computing and, with the development of the PC, into the home. With the implosion of size and cost of electronics came the explosion of applications. There is little we do from washing our clothes, driving our car, or talking with grandma that does not involve ICs. And while we marvel at the ability of these devices we tend to forget the unsung heroes, the chip packagers. Like the fabulous Fabergé eggs from Russia of old, each containing their treasure, chip scale and wafer level packages are the exotic containers of their treasures. To ensure the connectivity, reliability, and manufacturability is truly a work of art.

When we look at the complexity of the modern package, the underlying technology is stunning. In medieval times, the alchemists searched for the Philosopher's Stone, the ultimate turning of lead into gold. Their formulae were complex and not well understood. They substituted guessing and blind faith for measured science. Of course, none succeeded. Today's packaging designers are like the alchemists in that they search for the ultimate package. But unlike the alchemists, theirs is a methodical

approach. Like the development of the IC itself, packaging engineers relentlessly test and try and test again. Genius truly is 1% inspiration and 99% perspiration.

The lead feature of this edition is one such work, a thorough and studious report on the *Development of Wafer-Level Packaging of Normal and High Pin Count Devices for Mobile Applications*. In-Soo Kang and his team who authored this paper were voted 2009 Best of Conference after review by members of the 2009 IWLPC Technical Committee. We are proud to present an edited but nonetheless complete version of their paper. Also of great practical value, the article by Steven Golovato and his team about an inexpensive approach to making high aspect ratio TSVs makes interesting reading. Our business article this edition is by Gary Alexander and looks at buying refurbished equipment in these troubled times, an option I am sure many of you are looking at with fear and trepidation. George Riley's look at *Pressure Control in Flip Chip Assembly* completes our set of major features.

Of special interest this month is a guest editorial by Françoise von Trapp on 3D integration. She is *Talking about a Revolution*. Gail Flower, in her guest editorial, wonders if the burn-in socket engineer at BiTS might get inspiration from looking at other branches of technology: printed electronics, perhaps? Looking into her crystal ball is Sandra Winkler who, in our *Emerging Trends* section, maps the future of the photo-voltaic business.

If you got this far down the page, thank you for being a thorough reader. Don't forget, however, that I am just an old time alchemist; the real stuff is on the succeeding pages! ☺



## 7<sup>th</sup> Annual International Wafer-Level Packaging Conference

October 11-14, 2010, Marriott Hotel, Santa Clara, CA

SMTA and Chip Scale Review magazine are pleased to announce plans for the 7<sup>th</sup> Annual International Wafer-Level Packaging Conference and tabletop exhibition. This premier industry event explores leading-edge design, material, and process technologies being applied to **Wafer-Level Packaging** applications. There will be special emphasis on the numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand wafer level packaging solutions for integration, cost, and performance requirements.

The IW LPC Technical Chair, Lee Smith of Amkor Technology, Phoenix, AZ, and the IW LPC Technical Committee would like to invite you to submit an abstract for this program. **Deadline for submittal is April 23, 2010.**

The conference includes three tracks with two days of papers covering: Wafer Level Packaging; 3D Stacked Packaging; and MEMS Packaging.

### Wafer Level Packaging:

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- Fan-Out and Redistribution
- Markets and Trends
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- MEMS Processes and Materials
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- Nano-MEMS and Bio-MEMS
- MOEMS Integration
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### 3-D Integration:

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- Substrates and Interposers
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# GUEST EDITORIAL



## 3D Integration: Talking about a Revolution...

By Francoise von Trapp, Contributing Editor [*3D InCites*]

**T**here's no question: everyone in the industry agrees that future growth relies on the success of 3D integration, and that through-silicon vias (TSVs) are the only way to achieve the required functional density at desired cost. In a word, scaling is out, 3D is in. But even though there is agreement in concept, there seem to be two camps emerging as to how all of this will progress; will it be evolution or revolution?

The traditionalists who compare each turn in the 3D road with historical trends for how other technologies have progressed to production insist that this transition will be an evolutionary process. Then there are others who declare this to be a revolution; 3D changes everything and it's time to let go of the 2D way and adopt a new set of processes suited to exploiting the Z-direction.

The 3D Architectures for Semiconductor Integration and Packaging conference, held December 9-11, 2009 in Burlingame, CA, and organized by RTI international, assembled representatives of both camps from across the globe, sharing the latest technology breakthroughs, and depending on who was speaking, advocating one or the other approach. I sat, always an observer of these proceedings on the outside looking in, listening to and watching all these industry experts duke it out, and I wondered, if the ultimate goal is the same for all who are here, why does it seem like there are still sceptics in the room? And then it hit me; they're not debating the Why 3D, they're arguing over the How 3D.

Clearly, there are points to be made for both evolution and revolution. In his pre-conference symposium presentation, Phil

Garrou, Ph.D., of Microelectronics Consultants of North Carolina described 3D integration as an evolutionary process that began with face-to-face wafer bonding, no TSVs; followed by TSV technologies; now working on 3D stacking, because "It's always easier to institute one new process in your foundry at a time than introduce several." Clearly a logical approach.

Also in favor of evolution is ALLVIA founder, Sergey Savastiouk (credited with coining the term "through-silicon via"), who told me, "Before people learn to run, they have to learn to walk." He thinks the fastest way to benefit from TSV technologies is through interposer technology, rather than making the leap directly to die stacks with TSVs.

However, with the imminent end of CMOS scaling only 10 years away, according to Ho-Ming Tong, chief R&D officer and general manager of group R&D, ASE Group, a revolution just might be in order. What makes it time? Atoms don't scale, explained Tong, and adds jokingly, "unless you use a particle accelerator." Tong said that we have a choice about 3D integration; we can be a believer or a non believer. For the believers, it is clear that as the future unfolds, 3D IC innovations create a new market place.

Also speaking out in favor of revolution was Claudio Truzzi, CTO, Alchimer, who, in describing advantages of high aspect ratio (HAR) TSVs, said, "I believe 3D IC is a revolution, and cannot be achieved using evolutionary processes, as has been the trend." In other words, the industry is getting bogged down trying to apply existing processes to a technology that may have outpaced legacy process capabilities.

If there are proven processes available that overcome manufacturing limitations and open the process window, why not implement them?

Yann Guillou, who heads up strategic technology activities for ST-Ericsson, the wireless arm of ST Microelectronics, says that for the wireless market, the emerging More than Moore makes more sense. Differentiation will not come from scaling, but from package and integration innovation. In fact, cell phones have 3D packaging in the form of package-on-package (PoP), embedded die, and fan-out wafer-level packaging. A packaging revolution is needed for increased performance, and TSV will be part of that.

Speaking from a chip design perspective, Eby Friedman, professor at the University of Rochester, says designing for 3D requires a different approach than the one taken for design for 2D architectures. "I think heterogeneity is going to be the dominate issue," he noted, "because it involves inter-die process variations, disparate technologies, and different materials." In redefining problems for the 3D world, a two-step solution to floor planning will be required because placement routing now happens across planes.

Similarly, Paul Franzon, Ph.D., professor of electrical and computer engineering at North Carolina State University urged the conference attendees to "admit their addiction" to electronics as they are built today, and "kick the 2D habit." Franzon's 10 step program outlines a holistic approach to creating 3D-specific systems.

(continued on Page 17)



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# Development of Wafer Level Package of Normal and High Pin Count Devices for Mobile Applications

## Test vehicles have been developed to evaluate package and board level reliability

By In-Soo Kang, Jun-Kyu Lee, Gi-Jo Jung, Yun-Mook Park, Byeung-Gee Kim [Nepes Corporation]

In order to evaluate Wafer Level Package (WLP) technology for devices from low to high pin count, various types of WLPs have been developed and evaluated in terms of package size, structure, and materials. The reliability of a range of WLPs from 6 x 6 ball array (36 balls) in 0.5mm pitch to 14 x 14 ball array (196 balls) in 0.4mm pitch has been tested. Also, a Wafer Level System-in-Package (WLSiP) which has two chips inside one WLP has been developed and tested.

### Introduction

Recently, semiconductor devices for mobile products, such as cellular phones and portable media players (PMPs), have been changing. Due to the trends in mobile convergence and the expansion of the market for mobile products, the need for smaller size components and electronic packages has been increasing. Packages like WLP and WLSiP are emerging as real chip-size packages for various LSIs from small to high pin count devices.<sup>1</sup>

WLP has so far been applied to lower pin counts and smaller die size devices for the consumer product because of reliability issues at the outermost solder joints of larger size and higher pin count devices on boards. However, the requirement from mobile product makers for WLPs of larger size and higher pin count has continuously increased and the development has progressed. To achieve this, it is important to ensure solder joint reliability for the application of WLP to high pin count devices.<sup>2</sup>

In the case where WLP is applied to higher pin count devices, because of large die size and fine solder ball pitch, various environmental reliability issues are expected such as thermal, moisture and drop impact. Bigger die size results in a

relatively smaller contact area and more fragile solder joints, especially at the outermost ones. To apply WLP to various devices from small pin count to high pin count, various types have been developed and evaluated in terms of die size, Under Bump Metallurgy (UBM), solder composition, and substrate types, especially including drop shock loading as well as thermal fatigue performance.<sup>3</sup>

Recently, WLSiP technologies have been emerging to put both small pin and high pin count devices inside one WLP to expand the technology into System-in-Package (SiP) applications. A WLSiP which has two chips inside one WLP has been developed. To optimize the structure and materials for WLSiP, various reliability tests have been performed in terms of die size and material type.

### Experiments

Various WLP samples with the daisy chain design were prepared for evaluation of the reliability of both small die size and high pin count packages.

For small die applications, firstly a WLP with 6 x 6 ball array (36 balls, 3mm x 3mm) was prepared in 0.5mm pitch with solder ball, composition Sn3.0Ag0.5Cu, on electroplated Cu/Ni/Au UBM. The package level reliability tests were preconditioning, Temperature Cycling (TC), and High Temperature Storage (HTS). The procedure for preconditioning was to start with a bake of 24hrs at 125°C for the inspected samples. This was followed by a soak lasting 24hrs with the chamber at 85°C and 65% RH. Finally, 3 cycles of reflow with peak temperature of 260°C was performed. The samples were then inspected visually and confirmed by ball shear testing. After the precondition test, the WLPs were subjected to the reliability tests of HTS and TC. The

temperature for HTS was 150°C and the target was 1000hrs. The temperature range for TC was from -55°C to 150°C and the target was 2000 cycles. All of the reliability test samples were confirmed by ball shear test and optical microscope.

Secondly, a WLP with 9 x 9 ball array (65 ball depopulated array, 4mm x 4mm) having 0.4mm pitch using Sn3.0Ag0.5Cu solder balls on electroplated Ni UBM and Electroless Nickel Immersion Gold (ENIG) finished substrate was used for both package and board level reliability tests. Figure 1 shows pictures of the WLP and the test board. Package level reliability tests were done for preconditioning (MSL2), multi-reflow, and PCT. The quality was confirmed by microscope inspection, ball shear and ball pull testing. WLP samples were flip-chip bonded onto the reliability test board and evaluated for TC, Temperature Humidity Test (THT), 4-point bending, and drop test. The test items and conditions are summarized in Table 1. All the samples of the reliability tests were judged based on JEDEC standards and cross-sectioned to analyze failure mode.<sup>4-6</sup>



Figure 1. 9x9 ball array WLP and test board

Items	Condition	Target	Sample size
Drop Test	1500G, 0.5mscc	500 times	2 board(56WLP)
4-Point Bending Test	2000με, 1.0mm, 1Hz	30,000 cycles	1 board(4WLP)
TC	-40/125°C, 1 cycle/hr	500 cycles	2 board(56WLP)
THT	85°C, 85%RH,no bias	240hrs	1 board(28WLP)

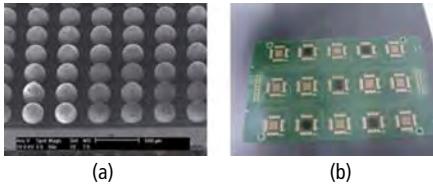
Table 1. Reliability test items of 9x9 ball array WLP

WLPs of 5.6mm x 5.6mm and 6.0mm x 6.0mm were fabricated on Si<sub>3</sub>N<sub>4</sub> wafers for testing high pin count devices. The WLPs consisted of 4-layer structures:

reconfiguration, redistribution, passivation, and solder ball with UBM. Polyimide and electroplated Cu were applied as materials of dielectric and RDL respectively. Solder ball arrays were 12 x 12 (144 balls) and 14 x 14 (196 balls) and ball pitch was 0.4mm. Solder balls were 250 $\mu$ m in diameter with three kinds of solder composition: Sn3.0Ag0.5Cu, Sn1.2Ag0.5Cu, and Sn1.0Ag0.5Cu. Two kinds of UBM structures, electroplated Cu and electroplated Cu/Ni, were used. **Table 2** shows the specification of the WLP test vehicles in detail. The test board was fabricated based on JEDEC standard JESD22-B111, with FR4 material and size 132mm x 77mm x 1mm, 8-layer. Both Via-in-Pad (ViP) and Non-Via-in-Pad (NViP) with NSMD for the pad structures were formed on each side with the pad finished with two types of material: Cu OSP, and ENIG. **Figure 2** shows images of the WLP test vehicle and a test board with five flip-bonded WLPs.

Items	Features
Chip size	5.6mm x 5.6mm (14x14 ball array) /6.0mm x 6.0mm (12x12 ball array)
Chip thickness	0.3mm
Ball pitch	0.4mm pitch
RDL layer	Electro-plated Cu, Land size $\phi$ 250um, 5.5~7.5um THK
PSV layer	Polyimide, Open $\phi$ 210um, 10um THK
UBM	Electro-plated Cu and CuNi bi-layer, $\phi$ 230um size, 10um THK
Solder ball	SAC305 & 125 & 105, Ball size $\phi$ 250um

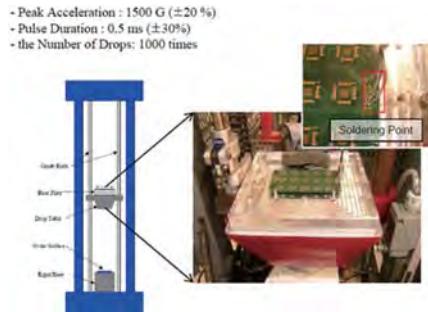
**Table 2.** Specification of high pin count WLPs



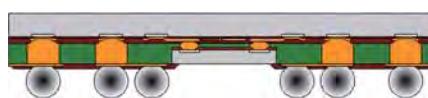
**Figure 2.** Test Vehicles (a) High pin count WLP, (b) Test board after SMT of 5 WLP samples

For the reliability testing of high pin count WLPs, package level test items of TC, HTS, PCT, and multi-reflow, and board level tests of TC and drop shock were conducted. Board level TC was carried out up to 800 cycles with the temperature range of -40°C to 125°C, 2 cycles per hour. The resistance of each unit was measured every 100 cycles and the failure criteria set to 200% increase of initial resistance. As shown in **Figure 3**, drop shock tests were conducted up to 1000 drops at 1500G and pulse duration of 0.5ms.

A WLSiP with two chips inside one WLP was developed. **Figure 4** shows a cross-



**Figure 3.** Equipment and mounting board of drop shock tests



**Figure 4.** Cross-section scheme of Wafer Level embedded System-in-Package

section of the WLSiP structure which has a daughter chip flip-chip mounted on a mother chip. Then molding, polishing the surface and conventional wafer level packaging (redistribution, passivation, and ball mounting) follow. WLSiP footprint size is the same as that of the mother chip.

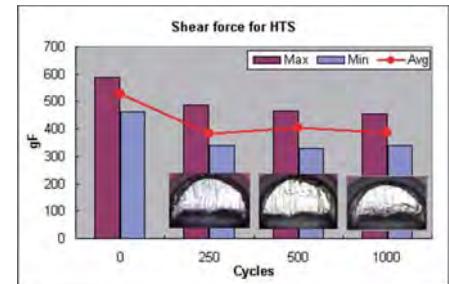
To optimize the structure and materials of the WLSiP, reliability tests MSL2, PCT (121°C/100%RH/2atm), TC (-40/125°C) and HTS (150°C) were performed with the test vehicles using 2 die sizes, 3 types of dielectric materials, and 3 types of molding compound materials.

### Reliability of WLP with 6 x 6 (36 balls) ball array

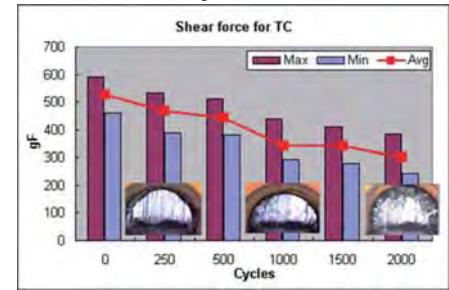
The reliability tests for the 6 x 6 ball array WLP (36 balls, 3mm x 3mm) were performed at the package level. After preconditioning, the result of the shear test showed that a fracture had occurred at the bulk solder and the average shear value was 526.7gF. **Figure 5** shows the cross-section and ball shear test images. IMC of (Cu,Ni)6Sn5 and IMC spalling have been observed at the interface between Ni and Sn3.0Ag0.5Cu solder. **Figure 6** shows the changes of shear strength and fracture modes after HTS and TC. According to the



**Figure 5.** (a) Cross-section image of UBM structure, (b) top view of fracture mode after ball shear



**Figure 6 (a)**



**Figure 6 (b)**

**Figure 6.** Shear strength variations and fracture modes after (a) HTS at 150°C, (b) TC at -55°C / 150°C

HTS result, shear strength decreased with time, but all shear fractures occurred at the bulk solder even after 1000hrs. In the case of TC, similarly, shear strength decreased with passing cycles, but fractures occurred at the bulk solder even after 2000 cycles.

### Reliability of WLP with 9 x 9 (65 balls) ball array

Package and board level reliability tests for the 9 x 9 ball array WLP (65 ball depopulated array, 4mm x 4mm) were performed to verify the application of medium die size. Concerning package level testing, all WLP samples passed precondition level 2 and PCT of 168hrs. As shown in **Figure 7**, the results of ball shear after testing showed cohesive failure mode in which fractures occurred inside the bulk solder, that is, ductile failure mode. **Figure 8** shows shear strength and fracture mode as results of the reflow cycles. There were no big changes of shear strength or ductile fracture mode even with higher numbers of reflow cycles.

After board assembly, board level reliability tests of drop, 4-point bending, TC, and THB were performed. For the board drop test, a board with 28 WLPs was built. There were no failures of the board level drop test. Judgment was based on the JEDEC standard by the first event of

(continued on Page 30)

# Pressure Control in Flip Chip Assembly

## Pressure-indicating sensor film provides a convenient, accurate, repeatable, and lower cost control for both bonding and coplanarity.

By George A. Riley, PhD [FlipChips Dot Com]

Flip chip assembly electrically connects a face-down chip to a circuit board or substrate by microscopic conducting bumps of solder or pure metals. Accurate control of chip placement pressure and chip-to-substrate coplanarity is essential. Undetected pressure variations are a hidden cause of poor connections and non-coplanarity, reducing bonding yields and device performance. These pressure variations can be revealed and remedied by using pressure-indicating sensor film.

Bonders usually depend upon a force preset in a machine which is not capable of measuring pressure variations across the die. Some top-of-the line bonders provide laser measurements or optical auto-collimator measurements of coplanarity as expensive options. Pressure-indicating sensor film offers a viable solution for flip chip bonders to measure the pressure, or the uniformity of that pressure, across the die or bonding tool. A recent conference paper showed the advantages of a pressure-indicating film in wafer-to-wafer bonding.<sup>1</sup> Film may have similar advantages for several applications in flip chip assembly.

Placing pressure-indicating sensor film between two surfaces causes it to change color in direct proportion to the local pressure applied, giving an irreversible “pressure footprint” of the surface. Pressures over a wide range may be revealed with one vendor claiming 2-43,200 PSI (0.14-3,000 kg/cm<sup>2</sup>). The pressure magnitude at any point may easily be determined by comparing the color to a calibrated color correlation chart, analogous to using litmus paper to determine acidity. Figure 1 shows a color map of a wafer and its pressure interpretation. Visual comparison gives  $\pm 10\%$  accuracy in determining pressure. An optical measurement system increases accuracy to  $\pm 2\%$ .

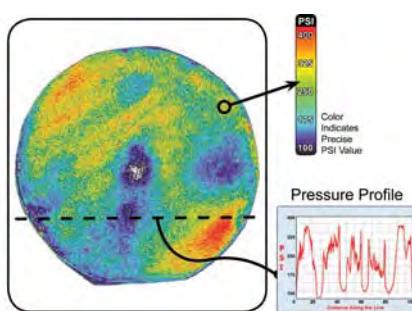


Figure 1. Wafer pressure footprint and interpretation (courtesy Sensor Products Inc.)

The success of pressure-indicating sensor film in wafer bonding suggests similar applications in flip chip assembly, where pressure magnitude and spatial uniformity may be critical. This is particularly likely with large die, which are becoming more common. Die larger than 20mm<sup>2</sup>, with more than 25,000 bumps per die, are already in routine production.<sup>2</sup> Potential pressure sensing applications include die-to-substrate coplanarity, bump coining for uniform bump heights, and several pressure-sensitive bonding methods.

### Coplanarity

Successful flip chip assembly of large die with many bumps for applications such as image sensors depends upon the substrate, and the die that is being placed upon it, having parallel, coplanar surfaces when they are brought into contact. Any deviation from coplanarity can cause open or poor electrical connections. Extreme cases may misalign the die by imparting a sideways sliding motion during placement pressure, or may even crack the die. Figure 2 and Figure 3 show some potential effects of non-coplanar bonding.

Conventional approaches for establishing and verifying coplanarity depend upon optical or laser equipment. However, most flip chip bonders do not have either of these expensive add-ons. Without them, establishing coplanarity often requires repeated trial-and-

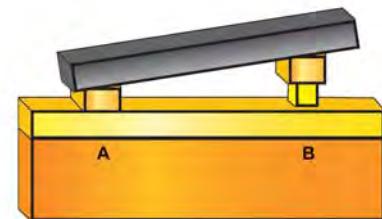


Figure 2. Misalignment may create acceptable bonds on side A but open circuits from failure to bond on side B

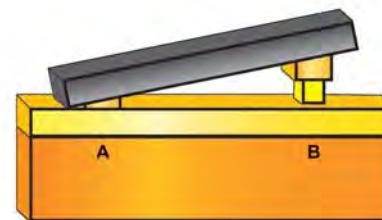


Figure 3. Misalignment may create short circuits on side A due to overpressure, and acceptable bonds on side B

error planarity adjustments using sample assemblies and microscopic inspection.

### Coining

Gold stud bump flip chip assembly places gold bumps on the die using a modified wire bonder. As deposited, those bumps have wire tails of varying length, as well as variations in bump height. Figure 4 shows a bump as deposited.

“Coining” by pressing the bumped die against a flat surface is a common method to reduce height variations and create larger contact areas. Figure 5 is a cross-section

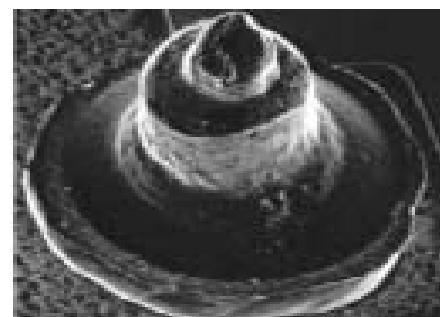


Figure 4. Gold stud bump showing wire stub at top



Figure 5. Cross section of a coined gold stud bump connection

of a coined bump. When this is done, inadequate or non-uniform pressure across the die surface may cause some bumps to have varying heights, causing some open or poor contacts. Pressure-sensing film would verify uniform bump height.

### Bonding

Many common methods of flip chip bonding require controlled, uniform pressure to avoid opens, poor contacts, and die cracking:

- Thermosonic bonding experiments found an optimum pressure for best bond adhesion. Higher or lower pressures gave poorer bond shear results.
- Thermocompression bonding requires higher bonding pressures than thermosonic, raising the consequences of inadequate pressure control. Copper/Copper thermocompression bonding of copper "nails" on a die to copper bond pads on a wafer has been demonstrated for high density 3D assemblies.
- Copper/Tin interdiffusion bonding of chips to wafers in 3D heterogeneous assemblies depends upon proper pressure at 300°C to form a stable copper-tin intermetallic, with copper upper and lower bonding surfaces.
- Gold/Tin wafer bonding tests show that too much pressure causes squeeze-out of solder, potentially leading to open or short circuits. Non-uniform pressure may squeeze solder out in some areas, but not in others.<sup>1</sup> The same problem could occur with large die in chip-to-substrate or chip-to-wafer Gold/Tin bonding.

### Common Assembly Problems

There are many common assembly problems associated with variations in pressure. Here are some common examples:

- Thermocompression bonding is used in both ordinary chip mounting and in 3-D die-on-wafer assembly. Thermocompression flip chip

bonding requires high temperatures and pressures up to 475°C with 200 Newtons/mm<sup>2</sup> of contact surface. In each case, the coplanarity of die and substrate and the uniform distribution of pressure are essential to thermocompression yield and performance.

- Non-conductive adhesive bonding pre-dispenses an adhesive on the substrate, and then applies pressure to squeeze out the

adhesive from between the conducting bumps and the substrate bond pads to form metal-to-metal connections. The connection is maintained by curing the adhesive that fills the remaining space. Too little squeeze-out pressure on the die risks poor connections. Too much pressure

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# What's New With Used Equipment?

## If you are up to the challenges, there's a lot of opportunity

By Gary Alexander [AMC Intl., LLC.]

**9**-1-1 is the emergency telephone number that was adopted by the United States in 1968. In most situations, a caller anywhere in the United States can immediately access police, fire, and ambulance services by calling this three digit number. And while the system works pretty well, there continue to be those instances where individuals call 9-1-1 looking for other than emergency information because they do not know where else to turn.

In researching this article, I could not find a documented instance where someone called 9-1-1 to inquire about used electronics manufacturing equipment but that does not mean it is not a possibility. Why? Because over the past couple of years, the secondary market for electronics manufacturing equipment has been turned upside down. To better understand what this means, one needs to recall the situation prior to 2008.

### A Bit of History

The early secondary equipment market can be best typified as a business where wheeling and dealing flourished and the guiding rule was "let the buyer beware." The first real organized effort to develop standards and establish structure for the semiconductor secondary equipment market began in the late 1980s with the establishment of the SEMATECH Surplus Equipment Council (SSEC). This was followed in 1998 with the founding of the Surplus Equipment Consortium / Network (SEC/N). SEC/N was very active in the semiconductor industry in promoting standards, ethics, and objective information primarily through conferences, seminars, and trade shows around the world. Semiconductor Equipment and Materials International (SEMI) was supportive of SEC/N almost from the beginning and ultimately

acquired SEC/N in October 2008. While there were a few secondhand equipment dealers in the printed circuit board and electronics assembly industries who became members of SEC/N, the IPC never formally recognized SEC/N.

### Recessionary Impact

The original equipment manufacturers (OEMs) were the first equipment sellers to be impacted as the economy slipped into recession during 2008.

Based on lessons learned in previous industry cycles, most end users reacted rapidly to the recessionary signals. Inventory builds, technology enhancements, and expansion plans were frozen almost immediately. Capital for purchasing manufacturing equipment virtually dried up. To understand what happened next, one needs to understand how the secondhand equipment market typically reacts to industry recessions.

As capital for the purchase of manufacturing equipment evaporates, end users still find it necessary to replace equipment. One way to stretch limited capital is to purchase refurbished, used equipment that generally sells for much less than new equipment. The secondhand equipment market is also negatively impacted by recessions, but there is still some limited sourcing activity for which used equipment dealers clamor. And then, when the recession starts to ease off, end users look to secondhand equipment as a way to maximize the limited amount of capital that starts to become available.

As a rule of thumb, reduced demand for used equipment lags new equipment going into a recession, never really dries up during a recession, and leads the purchasing of new equipment coming out of a recession.

### What Went Upside Down?

The answer is "virtually everything!"

End users cut back across the board. Management had to make serious resource decisions when production was scaled down and/or whole manufacturing lines ceased production. The immediate question was, "Would those manufacturing lines ever be needed again and if not, what to do about the equipment?" As a result, surplus manufacturing equipment, especially 200mm, started flooding the market from all parts of the world. Not only did the value of the equipment plummet, a significant amount of secondary market knowledge and experience was lost due to layoffs. Many companies found themselves at the mercy of having to outsource the sale of their surplus equipment with little clue to the real value of that equipment.

The OEM's new equipment business virtually disappeared. Some astute OEMs had previously established internal equipment refurbishment operations while still others had outsourced the business to third party refurbishers. However, as the recession dragged on and it came to defending their core competencies, internal refurbishment operations were some of the first to be eliminated. Those OEMs who had outsourced refurbishment operations were often left with much smaller, struggling independents, many of whom had already closed their doors or were looking into merge opportunities. What the OEMs were left with was a limited ability to respond to decreasing demands at selling prices that were sometimes far below what they had paid for their core units already in inventory.

As for the independent brokers, dealers, and refurbishers, survival meant being able to cover their overhead while trying to land one of the few refurbished equipment orders available, often from half way around the world. Several did not make it and some were faced with

merging or being acquired by the few independents still able to survive. To further complicate the situation, many independents were also caught with large inventories of core systems previously acquired for various "strategic" reasons.

And let's not forget the large leasing companies who ended up being stuck with equipment coming off lease with high residual values, no interest in a buyout and virtually no market for resale.

### Where Are We Today?

*Caller: "9-1-1 Used Equipment?"*

*Operator: "Yes. What is your emergency?"*

*Caller: "Our offshore foundry urgently needs to locate some refurbished electronics manufacturing equipment and I don't know where to turn. The broker and refurbisher that we had previously used have gone out of business, the OEMs are no longer supporting the refurbishment of their legacy products, I don't have a clue about the reputation and quality of the refurbisher names that I have been given, and the trade association we belong to is not actively supporting the market for secondhand equipment?"*

OK, maybe a little dramatic but nevertheless, if you are an electronics device manufacturer trying to make sense of what has happened to the global secondary equipment market, it can be very frustrating.

Speaking of the global secondary market, the electronics market for used manufacturing equipment has virtually become a one-way street. The buyers of used equipment are overwhelmingly located in Latin America and Asia, with the manufacturers in China being the biggest customers. Globally locating reputable sources of refurbished equipment from new and previously unknown dealers can certainly be a challenge, especially for companies in Asia.

Throw in some convoluted international recycling rules, an increased push for sustainability, the globally fluctuating value of currency, plus an escalating emphasis on being environmentally friendly and green and it is not hard to get the feeling that things have turned upside down!

We have become a throw-away society complete with short-term thinking and rationalized ethics. If nothing else, the current recession has shown us that many things need to change.

Everyone, from children to adults, wants what is new. This includes toys, clothes, appliances, cell phones, computers, electronic games, and cars.

Manufacturing managers and engineers are no different. Given the choice of new versus used equipment, of course they would prefer a new tool over one that is refurbished.

Companies are rapidly recognizing that they must place more emphasis on closely managing their resources to enhance their financial positions. This often translates

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into sourcing refurbished instead of new equipment and liquidating surplus equipment for as low as ten cents on the dollar if necessary to maintain cash flow.

The world has become impatient for short-term results. This includes stockholders, corporate managers, government officials, and everyone else right down to our own communications devices for texting and twittering. Performance reviews measure results in terms of days, weeks and months; not years. Management proudly expounds on their long-term planning practices while in actuality reacting to short-term needs. Here are a couple of examples to help illustrate the point:

1) Most managers understand the principle of supply and demand. It is well known by knowledgeable secondary participants that when there is a surplus of used equipment available, the price per unit goes down. One might think that a truly visionary and recession experienced company would create a capital reserve during good times for the purpose of buying critically needed and normally hard to come by equipment during recessionary periods. I don't know of a company that does that. Do you?

2) "Total cost" has evolved into being a fundamental principle touted by management worldwide. And an iceberg is a beautiful sight as it glides along with its shimmering crystal, sunlit peak silhouetted against the cold blue sky. Total cost is much like an iceberg where the vast majority of the liability is hidden beneath the surface. With all of the surplus electronics equipment now floating around the industry, the temptation to shortcut one's homework and snatch up a really good deal often causes even total cost advocates to get burnt.

Ethics is another one of these flag-waving principles that companies need to strategically and publicly salute. Since the early years of the business, the ethics associated with secondhand equipment has improved significantly. However, when business slows down, things get tough, and survival is in question, ethical considerations are not

above being rationalized. Buyers would do well to beware.

### Industry Metrics

Caller: "9-1-1 Used Equipment?"

Operator: "Yes. What is your emergency?"

Caller: "My management needs information on the size of the global used equipment market and what percentage of the price of refurbished versus new equipment that we should use for budgeting. I cannot find any good answers. Could you point me in the right direction?"

Unfortunately, there is no universally recognized source for this information. Why? Because given the infinite number of possible used equipment sellers, tiers of potential parties involved in any one transaction, and the daily dynamics of equipment supply, there is no way to objectively calculate secondary market sales metrics. However, there are always projections out there and research companies willing to provide snapshot reports on specific equipment.

At the risk of being passed off as a projectionist or forecaster, there are some things that can be extrapolated from what we do know.

Virtually all of the industry research and forecasting organizations concur that it appears things have started to turn around for the semiconductor electronics industry. The SIA is reporting that November 2009 was the ninth consecutive month of increased chip sales in all geographic regions.<sup>1</sup> SEMI is reporting the semiconductor manufacturing equipment Book-to-Bill ratio to have been over 1.0 since July 2009.<sup>2</sup> And the IPC website (Current Industry Trends) states that the Book-to-Bill ratio for PCBs has been over 1.0 since May 2009.

While there is a wide discrepancy as to just what this all means for new equipment sales in 2010 (estimates +10% to +22%),<sup>3</sup> a corresponding increase in refurbished equipment activity has been informally reported for the past nine months, thus once again reinforcing used equipment as being a leading edge indicator.

There are however some things that can be forecast with confidence:

- 1) The secondhand equipment business will play a significant role as the industry recovers.

- 2) The exact size of the secondhand equipment market will not be known.
- 3) The "early bird gets the worm."
- 4) After the good stuff has been cherry picked, the rest will be off to the auction house or the scrap pile.

### Getting Right Side Up

The first thing that would be of tremendous value to the industry would be for the third party associations and publications to quit cowering under fear that the OEMs will drop their association memberships or cease to advertise in publications that openly address the secondary equipment market. Chip Scale Review is to be applauded for their courage and leadership. Associations must recognize the importance of the secondary market to their members and customers providing objective information through their internal programs and public seminars at international trade shows.

It would also help if government agencies would come together on international secondhand equipment commerce but some things are just too much to hope for.

OEMs need to openly publish position papers on the refurbishment of their own equipment including the legacy equipment that they no longer support. They also need to clearly define their replacement parts and component programs as well as standardizing on realistic software licensing fees. Intellectual property rights are to be respected but restraint of trade actions are unethical as well as being illegal.

There has been, and will continue to be, a consolidation and reduction in surplus equipment dealers and refurbishers. Less than honorable characters will often surface under new names and some of the more reputable ones will seemingly disappear. Respect for intellectual property, regardless of country, needs to continue to be everyone's goal. International alliances between remaining companies, and yes, even OEMs, will be imperative as the global market migrates amongst geographic locations.

As for the chip and device manufacturers, their emphasis needs to be on strategic preparation and planning as opposed to reactionary buying and a lack of knowledge. The following should be considered as a minimum before venturing out to buy:

- Understand your company and their real commitment to buying refurbished equipment.

1) Which technologies require refurbished equipment? For example, the chances of finding 400mm related used equipment is slim but there is a glut of 200mm equipment and a significant amount of 300mm equipment available.

2) What is management's real level of commitment to used equipment? Will they spend the time and effort to evaluate "total cost versus lowest cost" alternatives? Will they support the time and effort that is required?

3) Who makes the decisions? Does manufacturing define the need, purchasing source the alternatives, and management make the final decision? Or in reality, does manufacturing source the equipment and purchasing just places the order?

4) Is there internal experience in globally sourcing secondhand equipment available that is knowledgeable and networked? Or will the responsibility be dumped on someone as an additional duty?

5) What role does finance and accounting play? Are there immediately accessible funds available to move on prime opportunities when they occur or does the acquisition trigger a tiered process of delayed capital approvals?

- Understand the global secondary market.

1) How do the key players (OEMs, refurbishers, dealers, brokers, and service providers) participate as members of the secondary market? How do they interface? Where are the conflicts?

2) How have other companies been successful participating in the global secondary market? What advantages and disadvantages do large companies have over smaller companies?

3) What is the best way to network with the various segments of the secondary market?

4) What are the geographic and cultural differences of the secondary market that

need to be comprehended and understood?

5) Where is the best place to go for current and objective secondary market information when it is needed?

### In Conclusion

Albert Einstein once said, "In the middle of every difficulty lies opportunity."

"What's new with used equipment?" The answer is "a whole lot of opportunity, if you are prepared and up to the challenges!"

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2. "Chip tool demand slows, but still rebounding"- Solid State Technology (12/21/2009)
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*(continued from Page 8)*

These revolutionaries have a point. Think about it, did Leonardo DaVinci use the same set of tools to paint the Mona Lisa as he did to cast his famous bronze horse statue, Gran Cavallo? When Einstein invented the incandescent light bulb, he said, "It was not my intention to improve on the candle." As Truzzi pointed out that it's not about who's right and who's wrong. It's about making determinations based on certain assumptions. Truzzi urges the industry shift its frame of reference and consider a different set of assumptions based on design advantages rather than manufacturing limitations.

Obviously, it goes without saying that there is still much work to be done before 3D TSVs are fully commercialized. But that's not the point. The point is that the best way to overcome the remaining limitations (design, test, thermal management) is to take a forward-thinking approach. It's time to take off the 2D blinders and don the 3D glasses instead. I have a pair, if anyone needs to borrow them.

# Three Ways to Get Control Over Your Burn-In and Test Costs:

# Collimated Physical Vapor Deposition for Through-Silicon Via Barrier-Seed Deposition

**Using inexpensive collimators and scanning deposition, production-worthy throughput is achieved**

By Stephen Golovato, George Seryogin, and Daniel Goodman [[NEXX Systems, Inc.](#)]

**B**arrier-seed deposition by Physical Vapor Deposition (PVD) for Through-Silicon Via (TSV) is limited to lower aspect ratio (AR) unless more advanced and expensive equipment such as ionized PVD is used. By using the so-called long throw approach, conventional PVD is typically used up to AR=5. Another approach equivalent to long throw is to use a collimator between the sputter target and the substrate. This approach has long been used in the front end, for example, for Ti deposition in contact vias. A collimator is demonstrated to provide barrier-seed coverage for AR=5 and above. Collimators are inexpensive and easily adjustable to control overburden and avoid pinch off at the top of the via. By applying barrier and seed in the same chamber, the film adhesion to the collimator is improved, extending the collimator lifetime.

## Introduction

3D die stacking to improve IC performance has driven the need to interconnect the stacked die using TSVs. These vias may be used to transport signals, power, or heat. A key challenge is filling the TSVs with conductor. The TSVs are significantly larger than front-end Damascene vias, being on a micron to tens of micron scale in diameter with ARs on a roadmap from 5 to >10.<sup>1</sup> The vias are generally etched using a process that leaves a rough scalloped vertical sidewall. An insulating liner must be provided which can serve to smooth out the sidewall structure. Sputter deposition, also known as PVD, is used to provide a layer of adhesion-barrier metal and a seed metal for electroplating. Electroplating fills the via with metal. The PVD process involves the sputtering of a given metal from a target usually situated directly above the wafer. The sputtered metal

flux rains down onto the wafers and coats it. There are many integration challenges for the processes that form and fill the TSVs. We are concerned here with the challenges to the PVD process. To provide a seed metal for electroplating, a two-metal layer PVD deposition is used. The first layer provides adhesion to the via liner and the bottom metal surface. It also has to provide a barrier to intermetallic diffusion. Typical adhesion-barrier layers are titanium, titanium nitride, tantalum, or titanium-tungsten. The vias are usually filled with copper so a copper seed layer is deposited over the barrier layer. Standard PVD alone is usually applied to AR<3. By using filtering techniques such as long-throw or collimation, standard PVD can be extended to AR=5 or more.<sup>2</sup> AR=5 is not an intrinsic limitation of the process; one can always deposit longer and provide adequate seed coverage above AR=5. However, the cost effectiveness of using these filtered PVD techniques relative to more expensive techniques such as ionized PVD or CVD becomes less clear above AR=5.

## Collimated PVD

When PVD is used to provide seed deposition in via, longer deposition times are required as the AR increases. Deposition at shallow angles does not penetrate deep into the via and eventually begins to close off the top, preventing deep deposition. The shallow angle deposition also produces a thick top layer (overburden) that must eventually be etched away. A technique to avoid this is to filter out, or scrape off, the shallow angle metal flux so only the more vertical metal flux reaches the wafer.<sup>2</sup> Two approaches are typically used to do this. One, known as long throw, extends the distance between the target and the wafer so that shallow angle flux goes to the walls of the

chamber, missing the wafer. Collimated PVD uses the same approach as long throw, mechanically eliminating all but the most vertical metal flux. In this case, rather than extending the target-wafer distance, a grid is placed between the target and the wafer. The grid is a metal plate with holes in it that allow some of the metal through to the wafer. For example, by making the diameter of the holes equal to the grid thickness, metal flux at angles greater than 45 degrees pass through to the wafer. This would be a collimator with AR=1. Collimators generally have an AR of 1-2. Collimators are usually designed as a hexagonal grid with thin walls (Figure 1) so that as little vertical flux as possible is intercepted.

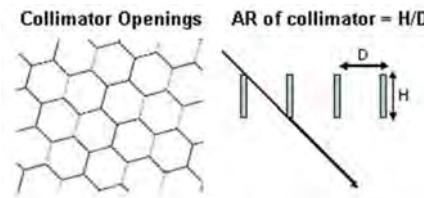


Figure 1. Collimator Design

As with long throw, 70-80% of the metal flux does not reach the wafer. While inefficient in the use of sputtered metal, these processes can provide seed coverage in vias when used in conjunction with RF biasing of the wafer. By applying RF, usually at 13.56 MHz, to the wafer, a glow discharge is produced in the argon background gas above the wafer. The RF also produces a DC self-bias on the wafer which attracts argon ions from the glow discharge to the wafer surface, resulting in sputtering of the deposited metal on the wafer. In the via opening, the sputtering produced by the RF bias technique reduces pinch-off and allows the metal flux into the via. It will also sputter metal off the via

bottom and onto the via sides near the bottom. It is the bottom corner of a via with vertical sidewalls that is most difficult to cover since only a limited range of angles allows metal to reach this area. This process is known as resputtering and may be applied during metal deposition or as a resputter-only process step.

Comparing long throw and collimated PVD, long throw has the disadvantage that the long distance between the target and wafer allows more scattering of metal atoms off of the background argon gas atoms, spreading the angular distribution of the metal so there is less vertical flux. Typical target wafer distance is 25cm to 30cm, which is on the order of the scattering mean free path for typical sputtering pressures of around 1mTorr argon pressure. Avoiding this effect completely forces operation at lower than normal sputtering pressures.<sup>2</sup> Another disadvantage of long throw when applied to single wafer chambers is that there is a wafer edge effect where the sidewall coverage is not symmetric around the via wall.<sup>2</sup> A disadvantage of the collimator is that it is situated directly above the wafer so any flaking of metal from the collimator may land on the wafer.<sup>2</sup> Therefore, good metal adhesion to the collimator is critical. Since the target-wafer distance can remain lower with the collimator, scattering is less of an issue. It is also easy to control overburden since the collimator is a simple inexpensive part that can be made in a variety of aspect ratios depending on the application. Both collimated PVD and long throw are used successfully in production. These techniques have limitations as the via AR increases because the amount of deposition required to achieve continuous coverage in the via increases faster than linear with AR. Figure 2 shows a calculation of via bottom coverage and lower sidewall coverage versus aspect

ratio. This calculation does not include gas scattering but does model resputtering from the bottom.

### Challenges to Via Coverage at Higher AR

As the AR increases, details of the via formation can limit the ability to produce continuous seed coverage in the via. If the via is highly scalloped or has an overhang at the top, shadowing of the metal flux on the underside of these features may result. Figure 3a shows a SEM image of an AR=5 via which has had seed deposition using collimated PVD.

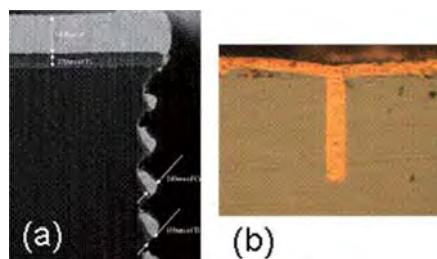


Figure 3. Successful seed deposition for highly scalloped AR=5 via using collimated PVD

Thick build-up of metal can be seen on the top side of each scallop with thinning underneath, making continuous coverage a challenge. This build-up sticks out farther than the scallops on the sidewall, causing further shadowing. Using RF bias to resputter from the top of the scallop onto the sidewall can reduce the shadowing but longer deposition time is also necessary when scallops are deep. The optical image in Figure 3b shows a plated sample of this via, demonstrating that a continuous seed was produced using a collimator for this AR=5 via with highly scalloped sidewalls. Figure 4 shows a via with an oxide liner that smoothes out the scalloped sidewall,

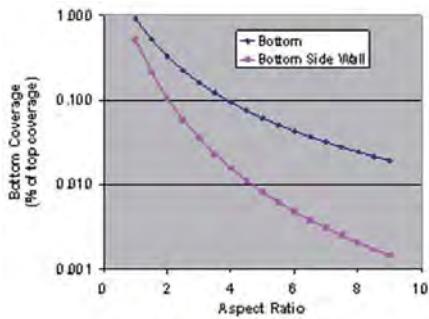


Figure 2. Model calculation of via coverage vs. aspect ratio

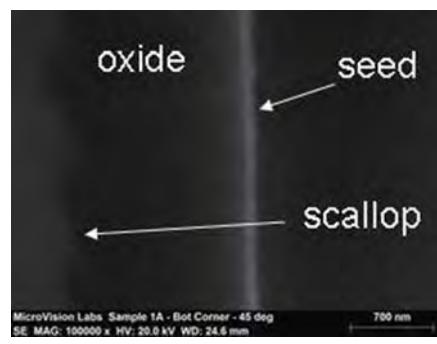


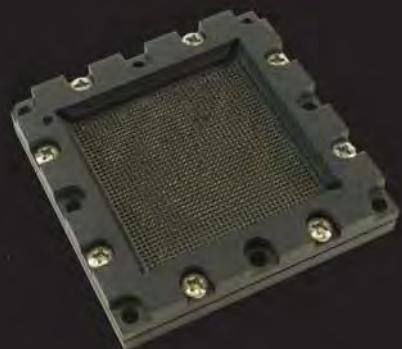
Figure 4. Oxide liner smoothes scalloped sidewall

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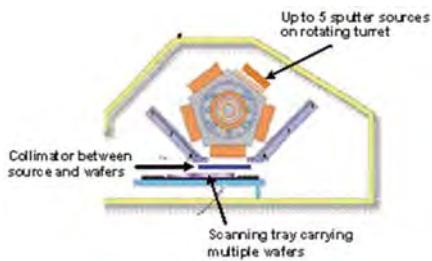


Figure 5. Collimator implementation in multi-wafer, multi-target chamber configuration

providing an easier surface for continuous seed deposition.

The quality of seed deposition is directly related to the via sidewall quality so there are important integration issues for seed deposition in high AR vias.

#### **Collimator in a Multi-target Chamber**

In many cases, long throw is easy to implement. For example, in a single wafer chamber, an insert can be installed between the sputtering source and the wafer to increase the distance between them. For some PVD equipment that run simultaneous

deposition on multiple wafers and use scanning techniques to achieve good uniformity, a collimator may be the easier implementation. A collimator has been implemented in a multi-wafer, multi-target chamber configuration. In this configuration, both adhesion-barrier and seed metal are deposited in the same chamber. Rectangular magnetrons are used (Figure 5) with the wafers scanned under the magnetrons to produce good uniformity.

The configuration also includes RF bias for resputtering. RF bias is important to get continuous seed coverage at AR>3. Figure 6 shows two cases with the same seed deposition with and without RF bias. To illustrate that the seed coverage is continuous, electroplated Cu is applied to thicken the deposition on the sidewalls and bottom so it can be seen clearly in cross-section.

In Figure 6a, without RF bias, there is no plated Cu at the bottom of this AR=4 via, indicating that seed metal is missing in the bottom corners. Figure 6b shows the same via structure plated after seed

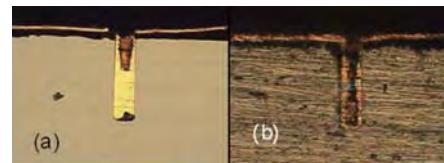


Figure 6. Improved seed coverage using collimator and RF bias for resputter. Plated vias with (a) no RF bias (b) RF bias

deposition with RF bias. Continuous coverage of the plated metal demonstrates that the seed is also continuous.

Another key issue is throughput using collimated PVD. Since most of the metal flux is deposited on the collimator, longer depositions are required to get continuous coverage in high AR vias. To maximize throughput, deposition time should be kept to a minimum for a given via structure. Figure 7 shows this effect. Figure 7a shows an AR=5 via after plating, illustrating that the seed coverage was continuous. Figure 7b shows an AR=6 structure on the same wafer did not plate all the way to the bottom, indicating that the seed was not continuous.

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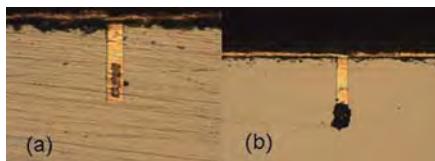
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**Figure 7.** Aspect ratio limit for a given recipe and a given via structure. Via (a) AR=5 has full seed coverage and plates to the bottom, via (b) AR=6 does not

This is the limitation of the particular recipe. By depositing longer and adding resputter steps, a continuous seed for AR=6 can be achieved. **Figure 8** shows an FIB image of an AR=6 via plated all the way to the bottom. These techniques can be extended to even higher ARs at the expense of throughput.

A disadvantage of collimated PVD is the potential for metal flaking from the

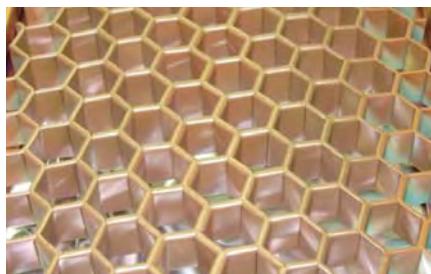
Electroplated to highlight seed



**23 X 140 um via**

**Figure 8.** AR=6 via plated to the bottom using longer deposition and additional resputter steps

collimator onto the wafer. To avoid this may require frequent collimator changes. By depositing both the adhesion-barrier and the seed in the same chamber, the collimator is coated with interleaved layers of two metals. This enhances adhesion to the collimator and balances the film stress. In this way the collimator cleaning cycle is extended. This technique, known as “pasting” is sometimes used for standard PVD in chambers that deposit only one metal. Separate pasting steps are done periodically to reduce flaking and extend the preventive maintenance cycle of the chamber at the expense of throughput. In the case that barrier and seed metals are deposited on the same collimator, pasting occurs with every deposition with no cost to throughput. As deposition builds up on the collimator, the opening will begin to close off. For the AR~1 collimator that produced the results shown in this paper, >100kW-hours of deposition reduced the openings <10% and showed no evidence of flaking or peeling. **Figure 9** shows this collimator after >100kW-hours of deposition. A slight rounding on the top edge of the collimator



**Figure 9.** Collimator after >100kW-hours of deposition shows little reduction in opening area and no evidence of particulation

can be seen but there is no evidence of particulation. This was a stringent test since the chamber was vented many times during the testing. Exposure to atmosphere oxidizes the metal surfaces and can degrade adhesion.

### Conclusions

The results presented in this paper show that the collimator approach to PVD deposition can be used to provide the seed required for electroplating to fill through-silicon vias in the same manner as other PVD techniques. It is particularly well suited for PVD system designs that use multiple target chambers, multiple wafer processing, and wafer scanning for uniformity. These systems have high throughput, low cost of ownership, and small footprints that make them well suited for the packaging market. As the roadmap for TSV pushes aspect ratios well above 5, all PVD techniques suffer from loss of throughput and therefore are more costly. Many new technologies are being pursued that will compete with PVD in this market, including CVD, particularly for the adhesion-barrier layer, and electroplated wet seeds for Cu. This approach is known as “direct on barrier.” It is possible that PVD will eventually be circumvented by these other technologies. In the interim, there are many applications at AR=5 and <10 where PVD can still play an important role. The key will be to have the most reliable, cost-effective solution.<sup>8</sup>

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2. S M Rossnagel, Sputter deposition for semiconductor manufacturing, IBM Journal of Research and Development; Jan-Mar 1999; 43, p. 163.

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# Emerging Trends

By Sandra Winkler, Contributing Editor  
[slwinkler@newventureresearch.com](mailto:slwinkler@newventureresearch.com)

**W**orld economies appear to be on the upswing; the fear of a "W" (or double dip) recovery is less likely. A single down-swing "U" or "V" recovery seems to be what we are experiencing, thanks to worldwide economic stimulus packages. The semiconductor industry began rebounding mid - 2009, and most major OSAT companies' earnings are reflecting that. While revenue for these companies is still down when compared with 2008 figures, revenue is heading in the right direction, positive. Forecast for ICs are expected to continue going up for the foreseeable future. Both units and revenue of IC packaging are expecting to have an approximate 7% CAGR from 2009 through 2013, which is pretty darn good (Source - The Worldwide IC Packaging Market, 2009 Edition from Electronic Trend Publications).

What else is going up? The demand for green technologies, such as solar power, will experience tremendous growth. According to keynote speaker Steve Paak, PhD, of Applied Materials at the Nanotechnology Council chapter of the IEEE ([www.ieee.org/nano](http://www.ieee.org/nano)) at a half day symposium on nanotech-enabled energy generation and management, growth could be as high as 40%, which is quite impressive.

The sun is a massive ball of fire. Only 0.001% of the sun's enormous energy is required for solar power to operate. Harvesting solar energy can be done in many ways, but two are with crystalline silicon and thin film. Crystalline silicon is used to harness solar power for the residential market, while thin film is used in utility scale projects.

The cost per watt is expected to drop for both over the next few years, from

\$1.65 today to \$1.20 in 2012 for crystalline silicon, and for thin film, from \$1.20 today to \$0.70 in 2012. Crystalline silicon is made on silicon wafers, while thin film is made on panels or squares. The declining price will boost demand for this technology, as it will become more affordable.

How can the prices drop like that? Price reductions can be obtained through automation and efficiencies in manufacturing. Increasing the number of ingots of silicon produced at a single time should produce thousands of wafers in a single shot. Creating a thinner wafer will result in the price per wafer to go down. The weight will go down from 9.7 grams to 5.7 grams. The size of the wafers will go up from 6" to 8" and 12". Automation will also bring costs down; currently manual labor is heavily used in making solar panels. Screen printing can be used to metalize solar panels.

Research into making solar power economical is on-going. Currently there is 20% degradation to solar cells made of crystalline silicon over a 10 year span. Research to reduce the amount of degradation in future generations of solar cells will continue.

Working with nanomaterials should help with all this. Semiconductor nanoparticles known as quantum dots can help reduce losses and increase overall efficiency. Sintering must take place for any of the energy to be harvested, according to Campbell Scott, PhD, of IBM Almaden Research Center.

The outlook for solar power looks good, as long as the sun keeps shining. Nanomaterials will help in increasing the efficiency of the panels, and making power more affordable for you and me. ☺

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# WHAT'S NEW!

## Small Footprint Socket Made for 10x10mm Packages

A new high performance QFN socket for 0.4mm pitch QFN 84-pin ICs has recently been introduced by Ironwood Electronics. The CG-QFN-7003 socket is designed for 10X10mm package size and operates at



bandwidths up to 10 GHz with less than 1dB of insertion loss. The sockets are designed to dissipate up to several watts without extra heat sinking and can handle up to 100 watts with custom heat sink. The contact resistance is typically 20 milliohms

per pin. The socket is mounted using supplied hardware on the target PCB with no soldering and claims the smallest footprint in the industry. The CG-QFN-7003 sockets have a temperature range of -35°C to +100°C and current capacity of 2 amps per pin.

[<http://www.ironwoodelectronics.com/>]

## Stencil Provides Dimensional Stability and Long Life

Offering a "valuable alternative to precision screen technologies," DEK has released a new double-layer platinum stencil. Incorporating tensioning technology, the mesh layer of the two-layer structure serves to hold the stencil intact while accurately controlling the flow of paste to the second layer. The circuit layer determines the thickness and shape of the print deposits to deliver high tolerance, fine dimension printing. For their new platinum VectorGuard stencil, DEK claims



dimensional accuracy better than 0.1µm/mm and a screen alternative that generates a tenfold increase in product lifetime. In addition, Michael Zahn, Product Manager for Stencils at DEK explains that the new systems offer "major advantages for semiconductor packaging and component manufacturing" and are suitable for accuracy-critical applications such as solar cell or LTCC manufacture. [[www.dek.com](http://www.dek.com)]

## Stress Buffer Protects Delicate Features

A methodology for creating a stress buffer to protect delicate features of

(continued on Page 32)

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# GUEST EDITORIAL



## Sockets for Emerging Packaging – Get Ready for a Changing World

By Gail Flower, Editor of *Industrial + Specialty Printing* magazine and *Screen Printing* magazine at ST Media Group International. Contributing editor, *Chip Scale Review*

**S**ockets for emerging packaging will present huge problems in the future so where will the typical burn-in socket engineer attending BiTS turn for inspiration? Sometimes you have to look beyond your own backyard. This article provides a review of one direction that electronics is seeking to produce lower cost, more flexible, smarter products and that direction is printed electronics.

### What is printed electronics?

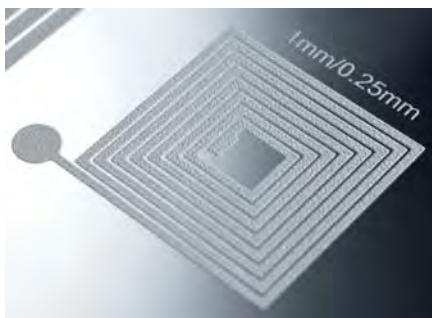
Printed electronics is a set of printing methods—screen printing, digital printing, micro dispensing, stamping, jetting, offset lithography, flexography and more—used to create electrically functional devices. The substrate materials can vary as well including glass, paper, plastic, textiles, and more.

One type of printed electronics is called organic printed electronics or polymer electronics technology. Organic printed electronics uses conductive polymers and can be printed at room temperature, rather than diffused into pure silicon at approximately 1000°C, which is typical of semiconductors.

Printed electronics have spread across the consumer market already. For example, you press printed buttons to dial your phone or Blackberry device on printed membranes to make electrical connections. The back-lighting with the device involves printed electronics as well. For tracking new clothing and most of the high-ticket items purchased, all have a radio frequency

identification (RFID) tracking device. In the 3D movie Avatar, all military personnel used electroluminescent displays. In the real world today, air baggage, freight, and ticketing commonly use RFID tags for tracking baggage and passengers.

Solar cells are popping up everywhere. Screen printing has long been the leading and most established process for creating metallization on photovoltaic cells. Why? It remains the most reliable, lowest cost method in an industry where demand is soaring. One critical factor determining its continued growth is the ability to lower PV system costs continually to the point of parity with grid electricity.



Is it able to replace the printed circuit board? In July 2009, Robert Tarzwell, DMR Ltd. (PCB Design 007) revealed that he has been testing printed electronic technologies for three years, intending to replace the typical non-green PCB. In the beginning, he used inkjet and other printing methods to lay conductive trace at least 15µm thick over a layer of dielectric. After 4-6 layers, the trace surfaces were too bumpy for attaching SMT components. Line definition and edge quality was not good enough either. Eventually, he began working with a series of printed electronics circuit (PEC) inks, such as the nano-silver, low resistance, low temperature fusing inks with better results. He learned that it's difficult to keep nanomaterials from clumping. But after various test results he was able to use a multiple screen application and

create a 2 mil thick dielectric with a straight side wall and higher resolution. The results were promising.

Can it replace integrated circuits? Today's organic semiconductor materials are not direct substitutes for highly integrated semiconductors. New inks and nanomaterials can help with performance development and lower functionality replacements will grow where ever applicable.

### Test methods

All this is interesting, but how does it affect the typical burn-in test socket engineer attending BiTS? Until industrial printed electronics becomes more mainstream in the logic and memory market, it won't affect BiTS attendees that much but changes are surely in our future. In 2007, iNEMI added organic and printed electronics to their microelectronics roadmap. IEEE now has standards developed specifically for printed electronics. Other groups, including the military for wearable displays, have been working on resolution, registration, thickness, orientation, dimension, processing, ink development, in-process electrical testing, and final product testing for a much longer time. All devices need test and burn-in sockets. Those who know what is coming will have the knowledge base to work with each new trend.

### Conclusion

Electronics assembly and test is at a crossroads. The road to low - cost manufacturing and testing of printed industrial electronics may take any number of paths.

How will this affect burn-in test sockets? The more you know about testing of all types of devices, the better prepared you are to face any challenge, whether that is chip scale or printed electronics. 

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AQL Manufacturing Services 25599-D SW 95 <sup>th</sup> Ave. Wilsonville, OR 97070 1.503.682.3193	<b>A</b>	<b>CM</b> <b>OT</b> = -50 to +150 °C <b>CP</b> = 0.4mm to 2mm	aqlmfg.com  Doug Kocher, President doug@aqlmfg.com
Ardent Concepts Inc. 4 Merrill Industrial Dr. Hampton Beach, NH 03842 603.929.2517	<b>A</b>	ATE Socket for chip-scale RF devices <b>OT</b> = -40 to +155 °C <b>CP</b> = down to 0.4mm	ardentconcepts.com Steve Cleveland, VP Business Dev. scleveland@ardentconcepts.com
<b>Aries Electronics Inc.</b> 2609 SE Bartram Rd. Bristol, PA 19007 1.215.781.9956	<b>A</b>	CSP/MicroBGA Test and Burn-in Sockets <b>T</b> = Spring Pin <b>OT</b> = -55 to 150°C <b>CP</b> = 0.3mm to no maximum <b>U</b> =Spring pin with optional adjustable pressure pad enabling 0.010 inch (0.254 mm) displacement per screw revolution.	arieselec.com  Frank Folmsbee, Sales Manager frankf@arieselec.com
BeCe Pte. Ltd. 1, Yishun Street 23 Unit 01-03, YS-01 Singapore	<b>A</b>	BeCe Socket <b>T</b> = Braided Electrical Contact Element <b>OT</b> = -55to 150 °C <b>CP</b> = 0.25mm and above <b>U</b> = fine pitch, high frequency, low inductance and low force contact	bece.com.sg  sales@bece.com.sg
<b>Cascade Microtech Inc.</b> 7115 Northland Terrace, Suite 400 Brooklyn Park, MN 55428 1.763.509.0066	<b>A</b>	BGA40 Test Socket <b>T</b> = spring pin, stamped and/or formed contacts <b>OT</b> = -40 to 150 °C <b>CP</b> = 0.4mm to 0.5mm <b>U</b> = Miniature stamped and formed contacts provide superior electrical & mechanical performance	cascademicrotech.com/gryphics  Mark Murzda, Sales Manager sockets@cmicro.com  Dan MacCoux, Product Application Manager dmaccoux@cmicro.com

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Centipede Systems Inc. 2110 Ringwood Ave. San Jose, CA 95131 1.408.321.8201	<b>B,T</b>	Centurion <b>T</b> = High performance contractor <b>OT</b> = -65 to +160 °C <b>CP</b> = 0.3 to 1.5 mm	centipedesystems.com Thomas Di Stefano, President tom@centipedesystems.com
Contech Solutions. 631 Montague Ave. San Leandro, CA 94577 1.510.357.7900 1995	<b>B,T</b>	Semi custom socket with RCS contacts <b>T</b> = Semi custom test sockets with barrel-less spring probes <b>OT</b> = -40 to 160 °C <b>CP</b> = 0.4 to 1.27 mm	contechsolutions.com Afshin Nouri, Sales Director afshin@contechsolutions.com
Custom Interconnects 2055 S. Raritan Street Suite A Denver, CO 80223 1.303.934.6600	<b>P,T</b>	Ultra HF100 <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	custominterconnects.com Edward Petsuch, General Manager epetsuch@custominterconnects.com
E-tec Interconnect Ltd. Industrial Zone C Forel (Lavaux) - CH-1072 Switzerland +41.21.781.08.10	<b>A</b>	FastLock Series <b>T</b> = Spring pin & elastomer & interposer <b>OT</b> = -55 °C to +200°C <b>CP</b> = 0.30 to 2.00mm, also mixed pitch <b>U</b> = High speed to 40 GHz & custom footprints	e-tec.com E-tec USA Bud Kundich P.O.B. 4078, Mountain View, CA 94040 1.408.746.2800 info-us@e-tec.com
Emulation Technology (Interconnect Systems Inc.) 759 Flynn Rd, Camarillo, CA 93012 805.383.8480	<b>A</b>	Hilo Flexible Interconnect System <b>CM</b>	emulation.com Perry Munroe perry@emulation.com
Enplas - Tesco 765 North Mary Ave. Sunnyvale, CA 94080 1.408.749.8124	<b>B,T</b>	Type S BGA <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	enplas-ets.com info@enplas-ets.com
Essai 45850 Kato Road Fremont, CA 94536 510.580.1700	<b>A</b>	<b>T</b> = Distributed force loading <b>OT</b> = -55 to 150°C <b>CP</b> = Including bare die, ultra small form factor <b>T</b> = Thermo-electric cooler and the Liquid & Heater Assist Cold test capability with condensation abatement features	essai.com info@essai.com
Exatron 2842 Aiello Dr. San Jose, CA 95111 1.408.629.7600	<b>P,T</b>	Duo Particle Interconnect Sockets <b>T</b> = CM <b>OT</b> = -150 to 250 °C <b>CP</b> = 0.2mm	exatron.com Bob Garcia bgarcia@exatron.com
Gold Technologies Inc. 752 Charcot Ave. San Jose, CA 95131 1.408.321.9568	<b>CM</b>	CM <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	goldtec.com contactus@goldtec.com
High Connection Density Inc. 820A Kifer Rd. Sunnyvale, CA 94086 1.408.743.9700	<b>A</b>	SuperButton, SuperSpring <b>T</b> = CM <b>OT</b> = -40 to 125°C <b>CP</b> = 0.5 to 1.27 mm <b>U</b> = Custom footprints, No NRE	hcdcorp.com Charlie Stevenson, COO charlie.stevenson@hcdcorp.com
High Performance Test 48531 Warm Spring Blvd. Fremont, CA 94539 1.510.445.1182	<b>T</b>	CM <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	hptestusa.com Mark Malfatti, Sales Manager mmalfatti@hptestusa.com

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Interconnect Devices, Inc. 5101 Richard Ave Kansas City, KS 66106 1.913.342.5544	T	Dyno Socket for Lead Free QFN Devices <b>T</b> = spring probe and formed metal <b>OT</b> = - 55 to 150 °C <b>CP</b> = 0.4 to 1.27 mm <b>U</b> = test sockets, lead free test sockets, wafer level sockets	idinet.com/synergetix Jeff Tamasi, Director of North American Sales jefft@idinet.com
InTEST Silicon Valley (Division of InTEST Corp.) 101 Nicholson Lane San Jose, CA 95134 1.408.678.9123	P	V-Touch <b>T</b> = Spring pin <b>OT</b> = -40 °C to 155 °C <b>CP</b> = 0.2 to 1.27 mm <b>U</b> = standard and Kelvin probes in Vespelbody	intest.com info@intest.com
Ironwood Electronics 11351 Rupp Dr. Burnsville, MN 55337 1.952.229.8200 1.800.404.0204	B, T	SG-BGA-7116 <b>T</b> = elastomer <b>OT</b> = - 40 to 100 °C <b>CP</b> = 0.2 to 1.27 mm <b>U</b> = Stacked Socket for testing Processor with socketed top-mounted POP memory	ironwoodelectronics.com Jason Cramer, Applications Director Jason@ironwoodelectronics.com
Johnstech International Corp. 1210 New Brighton Blvd. Minneapolis, MN 55413-1641 1.612.378.202	T, P	Leaded ROL 400 Series <b>OT</b> = - 40 to 155 °C <b>CP</b> = 0.40 to 1.27 mm <b>U</b> = Consistent Contact Resistance, Increased MTBA & Prolonged Load Board Pad Life	johnstech.com Heidi Theede hmtheede@johnstech.com Regional/Field Service Office 2450 Scott Blvd., Suite 305 Santa Clara, CA 95050 1.408.448.2020
LorangerInternational 303 Brokaw Rd. Santa Clara, CA 95050 1.408.727.4234	B, T	CSP & QFN <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = 0.30mm Pitch	loranger.com Debbi Stanley, Sales Administrator debbis@loranger.com
M&M Specialties 1145 W. Fairmont Dr. Tempe, AZ 85282 1.480.858.0393	P, T	Fine pitch BGA 10+ GHz BGA <b>T</b> = Spring Pin <b>OT</b> = - 20 to 120 °C <b>CP</b> = 0.4 to 1.27mm	mmspec.com Chad Rosser, Sales Manager crosser@mmspec.com
MJC Electronics Corp., division of Micronics Japan Co.,Ltd. 11004 Metric Blvd. Austin, TX 78758 1.512.276.8951	P, T	PB Free NF Series <b>T</b> = J-Contact <b>OT</b> = 40 to 125 °C <b>CP</b> = >0.3mm	mjc.co.jp John Jordan, US Sales Manager johnj@mjcelectronics.com Fred Megna, Technical Director MEC, fredm@mjcelectronics.com Minoru "Gucci" Takiguchi Package Probe Business Development Mgr MinoruT@mjcelectronics.com
Multitest Aeussere Oberaustr. 4 83026 Rosenheim, Germany +49.0.8031.406.0	T	ECON <b>T</b> = Cantilever, singel piece concept <b>OT</b> = -60 to 200 °C <b>CP</b> = 0.25mm <b>U</b> = Best CoT, compatible to existing sockets, current capability, interfacev options	multitest.com/sockets Gerhard Gschwendtberger Business Unit Manager Contactors g.gschwendtberger@multitest.com  Bob Chartrand bob.chartrand@multitest.com
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technoplia 196-5, Ojeon-dong Uiwang-si, Gyeonggi-do, 437-821 Korea 82.31.460.3530	A	Quick Custom Socket Series <b>T</b> = Stamped/spring pin buckle beam, pinch/tweezer <b>OT</b> = -40 to 150°C <b>CP</b> = 0.25mm and above <b>U</b> = Shortest spring pin for High speed test sockets	Okins Electronics USA Portland, OR Jay Kim, Director Jay.kim@okins.co.kr 503.810.6439  Victor Pyo, Technical Staff ehpyo@okins.co.kr

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Paricon Technologies Corporation 421 Currant Rd. Fall River, MA 02720 1.508.676.6888	<b>A</b>	PariProbe® <b>T</b> = Elastomer <b>OT</b> = -50 to 150°C <b>CP</b> = 0.1 to 1.27mm <b>U</b> = Less than 0.3 dB loss at 40 GHz	paricon-tech.com  Roger Weiss, President rweiss@paricon-tech.com
Phoenix Test Arrays 3105 S. Potter Dr. Tempe, AZ 85282 1.602.518.5799	<b>T</b>	FIREBIRD C300, 0.6mm structure with robust contacts for extremely high performance in both manual and automated test <b>OT</b> = -55 to +155 °C <b>CP</b> = down to 0.4 mm	phxtest.com Kat Smith, Operations Director kat@phxtest.com  Frank Bumb, CTO, frank@phxtest.com
Plastronics Socket Co. 2601 Texas Dr. Irving, TX 75062 1.972.258.2580 1.800.582.5822	<b>A</b>	H-Pin <b>T</b> = Stamped Spring probe <b>OT</b> = up to 200 °C <b>CP</b> = down to 0.5 mm	plastronicsusa.com  salesinfo@locknest.com  Steve Durrett, Sales Manager
Precision Contacts Inc. 990 Suncast Lane El Dorado Hills, CA 95762 1.916.939.4147	<b>P,T</b>	QFN Molded RF <b>T</b> = cantilever beam <b>OT</b> = -55 to 155 °C <b>CP</b> = down to 0.3 mm	precisioncontacts.com  Ken Bottin, Sales kbottin@precisioncontacts.com
ProFab Technology Inc. 40983 Encyclopedia Circle Fremont, CA 94538 1.925-600-0770	<b>T</b>	Kelvin Contact Socket <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	profabtechnology.com  Ravi Shankar sales@profabtechnology.com
Protos Electronics 1040 Di Giulio Ave., Suite 100 Santa Clara, CA 95050 1.408.492.9228	<b>B,T</b>	High-Performance PTS Line <b>T</b> = Pogo pin <b>OT</b> = -55 to 135 °C <b>CP</b> = 0.4 to 1.27 mm <b>U</b> = unique features	protoelectronics.com  Adam Hopper, Sales Account Manager a.hopper@protoelectronics.com
R&D Circuits 3601 South Clinton Ave. South Plainfield, NJ 07080 1.732.549.4554	<b>A</b>	Fine Pitch and Pitch Transformation Technologies <b>T</b> = ConnectFlex Interconnect <b>OT</b> = -40 to 150 °C <b>CP</b> = 0.3 mm and above <b>U</b> = Fine Pitch, Electrically Transparent connections	rdcircuits.com  Tom Bresnan, Sales Manager tbresnan@rdcircuits.com
Rika Densi America, Inc. 112 Frank Mossberg Drive Attleboro, MA 02703 1.508.226.2080	<b>CM</b>	BGA <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	testprobe.com  Larre Nelson larrenelson@testprobe.com
Robson Technologies Inc. 135 E. Main St. Morgan Hill, CA 95037 1.408.779.8008	<b>A</b>	Universal Multi-Site Optical Production Sockets <b>OT</b> = 0 to 85 °C <b>CP</b> = 0.5 mm	testfixtures.com  David Dick, Applications Director davidd@testfixtures.com
RS Tech Inc. 222 W. Parkside Lane, Suite 117 Phoenix, AZ 85027 1.623.879.6690	<b>A</b>	Flex Burn-In <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	rstechinc.com  Richard Elliott, National Sales Manager richardelliott@rstechinc.com
Sensata Technologies 529 Pleasant Street Attleboro, MA 02703 1.508.236.3800	<b>A</b>	0.4 mm POP socket <b>T</b> = dual pitch, dual buckling beam <b>OT</b> = -40 to 150 °C <b>CP</b> = 0.3 to 1.27 mm <b>U</b> = ZIF, High Density Sockets, Thermal solutions, Chip scale solutions	sensata.com  Tom Sutton tsutton@sensata.com

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SER Electronics (SER Corp.) Tokyo Japan 81.3.5796-0120	<b>A</b>	Coaxial test socket for high-speed requirements <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	ser.co.jp serusa.com
3M Electronic Solutions Div. 6801 River Place Blvd. Austin, TX 78726 1.800.328.1368	<b>B, T</b>	0.65 mm, OT BGA, Type 3 (963X Series) <b>T</b> = Open Top type sockets with micro-wipiong,double bea contacts that deliver a balanced force with minimal shear stress to the solder balls. <b>OT</b> = -55° to 150 °C <b>CP</b> = 1.27, 1.0, 0.8, 0.65 and 0.50 mm <b>U</b> = Inductance up to 6 nH with typically acceptalbe signal loss up to 2 GHz	3m.com/interconnects Micheal Giesler 512.984.5326 msgiesler@mmm.com
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9, 2-Choume Shibaura Minato-ku Tokyo 108-0023, Japan +81.3.5476.5661	<b>A</b>	<b>T</b> = MU Series <b>OT</b> = -50 to 150 °C <b>CP</b> = 0.5 to 1.0 mm <b>U</b> = Repleaceable tip lower maintenance cost and high GHz testing	unitechno.com Cupertino, CA 1.408.255.3550 Masa Fuchigami, President info@unitechno.com
Wells-CTI 2102 West Quail Ave, Suite 2 Phoenix, AZ 85027 1.800.348.2505 1.480.682.6100	<b>B</b>	772 Series <b>T</b> = Open Top CSP <b>OT</b> = to 150°C <b>CP</b> = to 0.4 mm <b>U</b> = Open Top Socket for Large Array	wellscti.com John Hartstein, VP Sales John.hartstein@wellscti.com
WinWay Technology Co. Ltd. 2F, No. 315, Minghua Rd. Gushan Dist., Kaohsiung, Taiwan, 804 +886.7.5524599	<b>CM</b>	CM <b>T/T</b> = CM <b>OT</b> = -CM <b>CP</b> = CM	winway.com.tw Monica_Huang monica_huang@winway.com.tw
Yamaichi Electronics USA 475 Holger Way. San Jose, CA 95134 1.408.715.9100	<b>A</b>	NP506 QFN Open-Top Production Sockets <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	yeu.com Nick Langston Jr. nickl@yeu.com
Yokowo Co., Ltd. (Ciruit Testing Connector) Tokyo 114-8515, Japan +81.3.3916.3111	<b>P, T</b>	Hi-Giga Socket for Final Test and Wafer Level <b>T</b> = CM <b>OT</b> = CM <b>CP</b> = CM	yokowo.com Yokowo America Corp. Sunnyvale, CA 94085 1.408.522.0326 Alvy Padiyil, Sales Engr. alvy@yokowo.com

(continued from Page 11)



Figure 7. Fracture images of ball shear test after (a) precondition test (MSL2) and (b) PCT of 168hrs

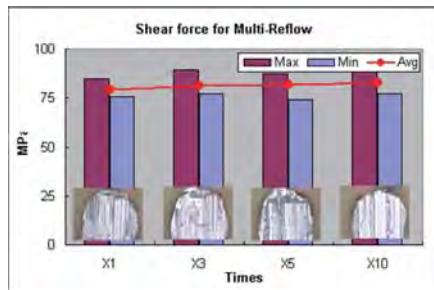


Figure 8. Shear strength and failure mode of multi-reflow test

intermittent discontinuity followed by three additional such events during five subsequent drops.<sup>2</sup> To check solder joints after the drop test, cross-section analysis was performed. Some resin cracks were found on the board side underneath the pad of the outermost solder joint array as shown in Figure 9.

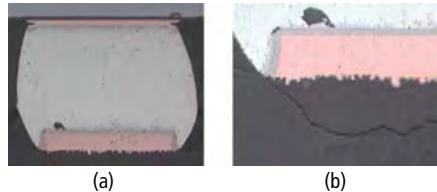


Figure 9. Cross-section images (a) solder joint between WLP and board, (b) resin crack on board side after 500 drops

For the 4-point cyclic bending test, 2 boards were tested and each board had 4 WLP samples, as shown in Figure 10. Using the JEDEC standard, failure was judged by the first event of intermittent discontinuity with resistance peak greater than the threshold value followed by at least nine additional confirmation events within 10% of the cycles from the first event.<sup>3</sup> Threshold value was 1000 ohm. During the bending test of 30,000 cycles, there was no electrical discontinuity and both boards passed. Figure 11 shows a crack between the IMC and the solder on the board side and was observed through cross-section analysis. The crack has stopped inside the solder joint even after 30,000 cycles of bending.

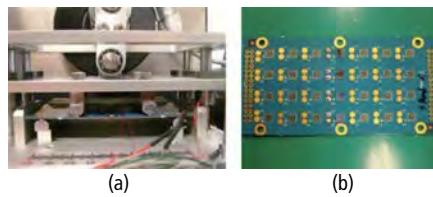


Figure 10. Pictures of (a) 4-point cyclic bending test machine, (b) bending test board which has 4 WLPs

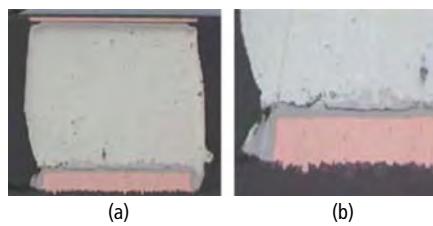


Figure 11. Cross-section images of (a) the outermost solder joint of 1st row, (b) crack on board side after bending test of 30,000 cycles

Temperature/humidity test passed and the maximum resistance variation observed was 2.9%, less than 10%, as shown in Figure 12(a). The temperature cycle test passed with two boards, one of which had been underfilled and the other had not. Both of them passed. Resistance variations after the temperature cycle test are shown for samples with underfill (Figure 12(b)) and without underfill (Figure 12(c)). All of the 28 samples with underfill passed board level TC, but one of the 28 samples without underfill showed high resistance. It was S20 and the high resistance occurred at the 334<sup>th</sup> cycle.

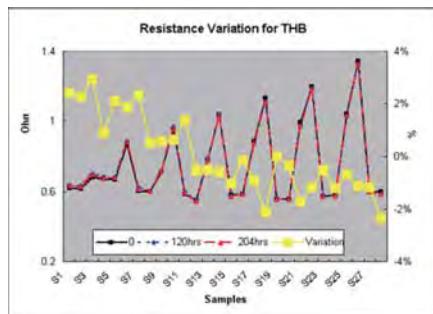


Figure 12 (a)

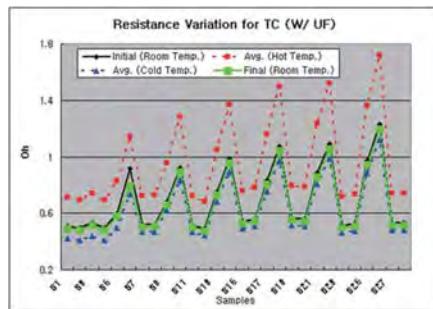


Figure 12 (b)

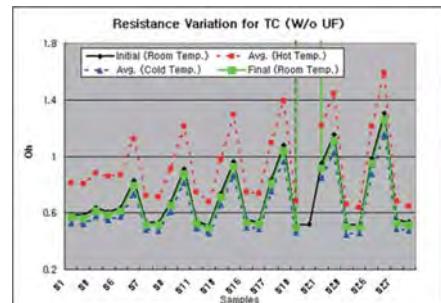


Figure 12 (c)

Figure 12. Resistance variation of (a) temperature/humidity test, (b) temperature cycle test of samples with underfill, (c) temperature cycle test of samples without underfill

For failure analysis of S20, a cross-section was performed and a poor solder joint and a crack on the board side were observed (Figure 13). Based on this, it is believed that the high resistance issue has been caused by a poor solder joint compared to the others, which might come from defects of the flip-chip bonding process.



Figure 13. Cross-section image of S20 solder joint on board without underfill after TC 500 cycles

## Reliability of WLP with 12 x 12 (144 balls) ball array

Package and board level reliability was evaluated for the 144 I/O (12 x 12) ball array using SAC305 and SAC125 composition which had a distinguished characteristic on the Cu-only UBM.

Table 3 shows the condition and results for package level reliability. After visual inspection and shear testing for all reliability items of HTS, TC, PCT, and multi-reflow, the tests were shown to pass. Figure 14 shows the variation of shear strength for the solder balls during the HTS and TC tests. From the results, SAC305 was more robust than SAC125 before the tests. As time goes by, decrease of the

Items	Condition	SS	Duration	Result
TC	-40~125°C	35ea	1000cycles	Pass
HTS	150°C	35ea	1000hrs	Pass
PCT	121°C/100%RH/2atm	35ea	168hrs	Pass
Multi-Reflow	Peak T=260°C	30ea	10 times	Pass

Table 3. Results of package level reliability tests



due to the small amount of Ni acting as a barrier layer to reduce the IMC growth rate as previously reported in papers.

## Wafer Level System-in-Package

To optimize the structure and materials used for WLSiPs, package level reliability tests MSL2, PCT (121°C/100%RH/2atm), Temperature Cycle (-40/125°C), and High Temperature Storage (150°C) were performed for the test vehicles with 2 die sizes, 3 types of dielectric material, and 3 types of molding compound material. **Table 8** shows the summary of reliability test results for each test vehicle. All test vehicles passed MSL2 and PCT of 168hrs. Test vehicles with MC3 passed TC of 2000 cycles except the 4mm x 4mm test vehicle on which D1 dielectric material was used. Concerning HTS, only one test vehicle with 4mm x 4mm die and D2 dielectric material passed HTS of 1000hrs.

Items	Molding Compound	Dielectric Materials	Die size (mm)	Result
TC	MC3	D1	4x4	1000cyc.Fail
		D1	6x6	2000cyc.Pass
		D2	4x4	2000cyc.Pass
		D2	6x6	2000cyc.Pass
		D3	4x4	2000cyc.Pass
		D3	6x6	2000cyc.Pass
PCT	MC3	D1	4x4	168hrs Pass
		D1	6x6	168hrs Pass
		D2	4x4	168hrs Pass
		D2	6x6	168hrs Pass
		D3	4x4	168hrs Pass
		D3	6x6	168hrs Pass
HTS	MC3	D2	4x4	1000hrs Pass
			6x6	1000hrs Fail

**Table 8.** Summary of reliability results for various types of test vehicles in terms of material and die size

As a result of the tests above, a WLSiP of size 4mm x 4mm, D2 dielectric, and M3 mold material has been designed in daisy chain and manufactured. The sizes of the mother and daughter chips are 4mm x 4mm and 2.95mm x 2.31mm respectively. The daughter chip is 70µm thick. **Figure 20(a)** shows images after the whole wafer level SiP assembly process and **Figure 20(b)**

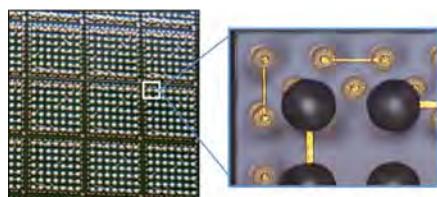


Figure 20 (a)



Figure 20 (b)

**Figure 20.** Images of (a) top view of wafer level SiP, (b) its cross-section image

shows a cross-section; there are no mold cracks, voids, or delamination.

For the fabricated WLSiP, package level reliability tests MSL2a, PCT (121°C/100%RH/2atm) of 168hrs, TC (-40/125°C) of 500 cycles, and HTS (150°C) of 1000hrs were performed and passed. TC (-40/125°C) and drop test (1500G/0.5ms) are under evaluation. More details about board level reliability will be discussed in a future paper.

## Conclusions

In this work, to verify wafer level packaging as it applies to various devices from small pin count to high pin count, various types of WLP have been evaluated in terms of I/O count, UBM type, solder material, and substrate type, and proven to be desirable for various applications of wafer level package.

First, WLPs with small pin counts of 6 x 6 I/O (36 balls) in 0.5mm pitch and 9 x 9 ball array (65 ball depopulated array) in 0.4mm pitch, have passed package & board level reliability tests.

Second, WLPs with larger pin counts of 12 x 12 I/O (144 balls) in 0.4mm pitch have passed package and board level reliability tests and verified as applicable to various devices.

Third, a WLP with a ball array of 14 x 14 (196 balls) in 0.4mm pitch has been fabricated and board level temperature cycle testing is complete. Other tests are under evaluation. Based on testing up to this point, design of WLPs with a ball array of 14 x 14 (196 balls) will need to proceed more cautiously in relation to structure and material of both package and substrate as compared to other ball array WLPs. More detail will be discussed in a future paper.

Finally, for one package with both small and high pin devices, a WLSiP with two chips inside one WLP has been optimized in terms of structure and materials. A WLSiP test vehicle was designed and fabricated to evaluate package level and board level reliability. Up to now, WLSiP has been proven to pass package level reliability and is under evaluation for board level reliability.

## Acknowledgements

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semiconductor devices has been developed by Unisem Advanced Technologies (UAT), a provider of wafer bumping technology. This customizable stress buffer structure includes a polymer layer formed by one or more coatings and a metal stack overlaying the polymer. The structure serves as a bunker to protect sensitive devices within its coverage from external stress. Its use may extend beyond stress mitigation, including shielding of sensitive devices from light, moisture, and electromagnetic interference. "Conventional semiconductor packages offer little or no additional protection to sensitive device features," said S.C. Lau, General Manager of UAT. "We are excited about the unique solution we have created to help our customers protect these features in a way that is highly effective and cost efficient."

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# Through-Silicon Via (TSV) Technology Implementation

## TSVs enable smaller, reliable devices across many market segments

By Nagesh Vodrahalli [ALLVIA, Inc., Sunnyvale, CA]

Miniaturization and higher performance needs of the electronics industry continue to drive technology innovations to achieve increased levels of integration. 3D stacking of silicon dies provides a very attractive way of improving functional density of electronics in addition to potentially providing increased electrical performance. Through-silicon via (TSV) technology along with flip chip technology significantly augment these improvements over the traditional wire bonded die-stack technologies.

TSV technology provides different

advantages to different market segments. For optical applications, TSVs provide electrical and optical connections from different sides of the silicon and improve sensor performance. Electrical via feed through is important for MEMS Cap applications. In the memory market, the ability to stack very thin dies and short electrical distances are important for integrating both memory and logic. Reducing the size and thus getting lower electrical parasitics provides benefits to both electrical and battery-life performance for some applications. Miniaturization is useful for all markets.

Via First (for MEMS) and Via Last (for semiconductors)



The image shows a promotional flyer for the ECTC 2010 conference. The top half features a night view of the Las Vegas strip. Text on the left says "Don't miss out on the industry's premier event!" and "The only event that encompasses the diverse world of integrated systems packaging!". The center features the logo "ECTC 2010" with "The 60th Electronic Components and Technology Conference". Below it is a "Highlights" section listing various sessions and exhibits. At the bottom, it says "June 1-4, 2010 Paris Las Vegas Las Vegas Nevada USA" and includes logos for EIA, PMI, IEEE, and EIA.

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mechanical and plasma processes. The vias thus formed are hermetic and are suitable for hermetic MEMS Cap applications.

The second TSV technology is backside TSV, more applicable for finished semiconductor wafers with active and/or passive devices. TSV technology is integrated with redistribution layer(s) that can be processed either on the front side or backside of the wafer. Backside via TSV involves wafer front side protection, backside thinning, lithography, via formation, and metallization. Via dimensions of 50 $\mu$ m to 100 $\mu$ m diameter and depths from 90 $\mu$ m to 350 $\mu$ m have been achieved with promising results at 500 $\mu$ m depths.

TSV interposers for advanced packaging of logic devices and for System-in-Package (SiP) applications have been developed. The silicon interposer technology developed also integrates embedded passives technology that provides high value capacitors for decoupling purposes. Silicon interposer technology can provide 5 $\mu$ m lines and spaces or better with integrated capacitors better than 600nF/cm<sup>2</sup>.

Preliminary reliability data gathered on reasonable sample sizes show excellent results for both Via First and Via Last technologies. Thin Si TSV interposers have been assembled on organic substrates using flip chip technology and the reliability results on such assemblies through thermal cycle testing are excellent. Technology developed has been applied to many different applications including medical electronics, communication ICs, and X-ray and gamma ray imaging.

# INDUSTRY NEWS

## Use SAC305 More Efficiently

Following a two-year study on the effect of impurity limits on the performance of lead-free solder, the IPC Solder Products Value Council (SPVC) has announced the publication of a white paper, Take Action Limits (TAL) for SAC305 Lead-Free Soldering Processes Utilizing Solder Baths/Pots. The paper provides electronics manufacturers with better-defined limits to guide them on a more efficient use of solder and, as a result, improve yields. The report is based on testing of eight common SAC alloys that were subjected to strenuous tests including wetting and electron microscope examination. "The report is another example of how the industry can come together and work together to create a coherent set of technical requirements that the industry can use to increase efficiencies and eliminate unnecessary waste," added Karl Seelig, AIM Inc. and chairman of the IPC SPVC.

[[www.ipc.org/SPVC-TAL-download](http://www.ipc.org/SPVC-TAL-download)][[www.ipc.org/SPVC-TAL-purchase](http://www.ipc.org/SPVC-TAL-purchase)]

## NBS Bucks the Trend – Growth Doubles

"In stark contrast to the slowdown in our industry in 2009, NBS enjoyed more than a doubling in revenue growth," reports NBS' President and CEO Michael Maslana. Continued growth in demand for the company's end-to-end solutions fueled the need for what is now their fifth fully automated line. The new SMT line features Juki's sixth generation KE 2070/2080 modular high speed placement system with on-the-fly laser centering and 16,000 CPH placement rate. This additional line further expands NBS' capacity to accommodate volume assembly and all up-to-date package styles including 01005, 0201, 0402, QFP, QFN, BGA, microBGA, and chip scale packages. Chris Alessio, VP Sales and Marketing, adds, "Our latest addition is not simply about capacity expansion but an extension of a facility capitalization that is second to none in the Tier II space." [[www.nbscorp.com](http://www.nbscorp.com)]

## Fredrik Arp joins Qioptiq as Chairman and CEO

After ten years as its CEO, Benoît Bazire has left Qioptiq to pursue other opportunities. Mr Bazire will be replaced by Fredrik Arp who joins the company as Chairman and CEO. Mr Arp has held senior executive positions in large global companies for the last 20 years, most recently as CEO and President of the Volvo Car Corporation. He holds a Bachelor of Science in Business and Economics, as well as being a Doctor in Economics from the University of Lund in Sweden. Qioptiq, with locations throughout Europe, Asia, and North America, is a provider of advanced optical systems, equipment, modules and components for a diverse range of civilian and defense applications. [[www.qioptiq.com](http://www.qioptiq.com)]

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squeezes adhesive out the sides and may cause die cracking.

- Indium bonding is used in flip chip assembly of large image sensor die that have thousands or tens of thousands of indium bumps connecting them to processor chips. Indium bumps self-weld on contact, so there are no second chances with a die that may cost thousands of dollars. Non-coplanarity on contact or non-uniform planar pressure can misalign the die or cause open or poor contacts, compromising the imaging performance of the sensor.
- Gold stud bumps for flip chip assembly are made with a modified wire bonder, which breaks the gold wire after attaching it to the chip leaving a small gold "stud." Pressing a flat surface against the bumps gives uniform stud heights by compressing the random-height wire stub left when the bond wire is broken. The uniformity of pressure ensures a higher probability of making all bump connections to the substrate, which saves time and money.

## Conclusion

Flip chips minimize assembly size and improve electrical performance, making possible hand-held consumer products such as cell phones, cameras, calculators and iPods. More than 20 million wafers, each with thousands of chips, are forecast for flip chip bonding in 2010. The performance of pressure-indicating sensor film in wafer bonding and the importance of quality control in all of the above assembly examples suggest that film pressure sensing could significantly improve flip chip assembly yield, costs, and set-up time. ●

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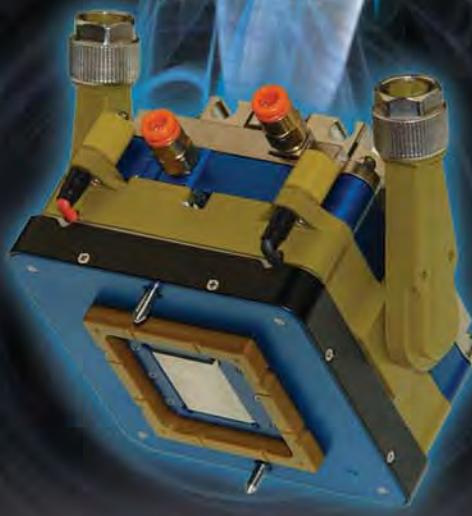


  
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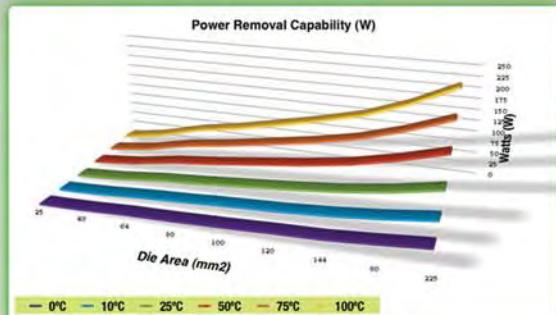
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