

# Chip Scale Review®

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*The Future of Semiconductor Packaging*

Volume 23, Number 3

May • June 2019

- **Automotive packaging**
  - SoCs
  - OSAT market challenges
  - Driving reliability in automotive electronics
- **Avoiding wire bond failures**
- **Flexible hybrid electronics**
- **Inspection and metrology challenges**
- **Exposed die FOWLP by transfer molding**

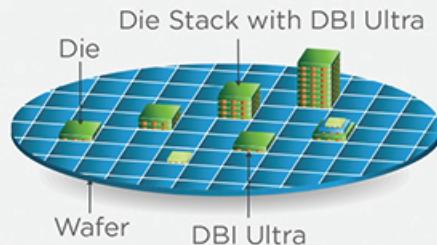




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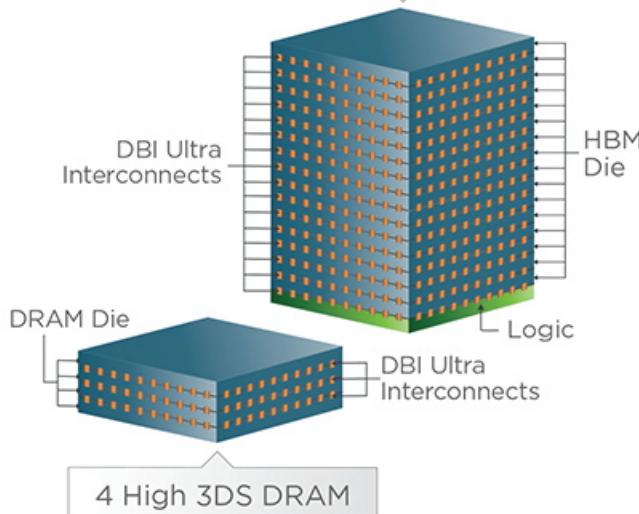
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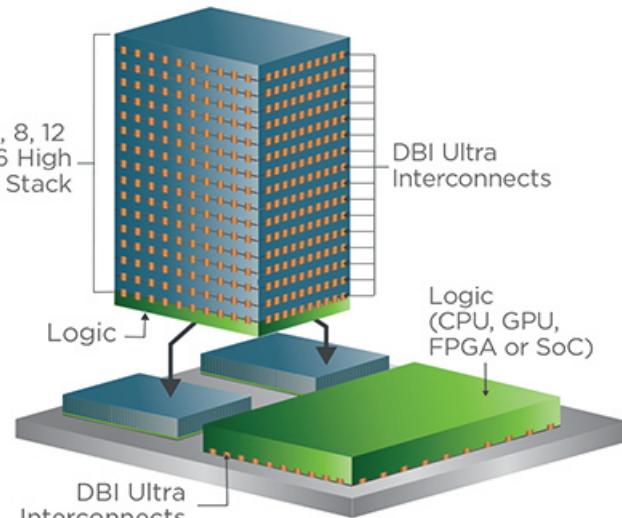
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*Automotive applications are driving a number of packaging technologies, such as reliability of packaging materials and screening of SoCs. But flexible hybrid electronics (e.g., for biosensors and personal wearable body monitors) and "More than Moore" nontraditional scaling are also pushing the packaging market segment forward. This issue covers the above topics in detail across a broad swath of the packaging industry.*

*Photo courtesy of Brewer Science, Inc.*

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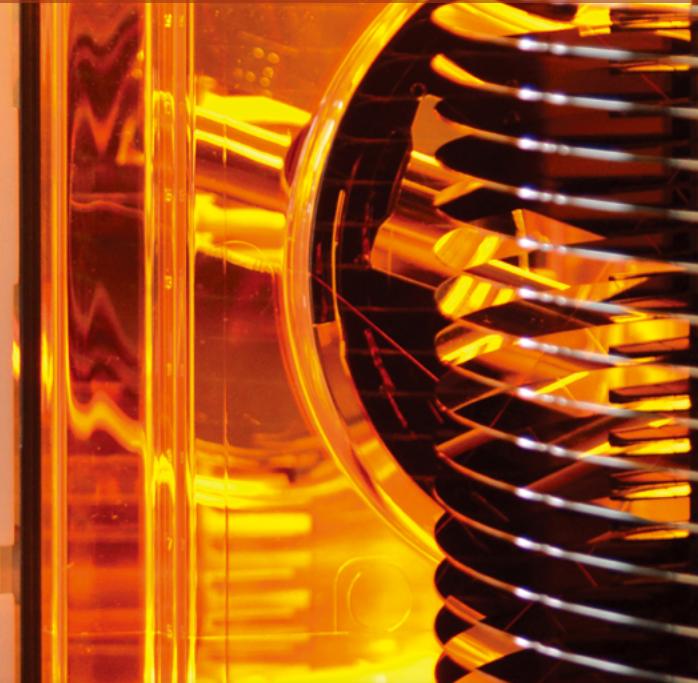
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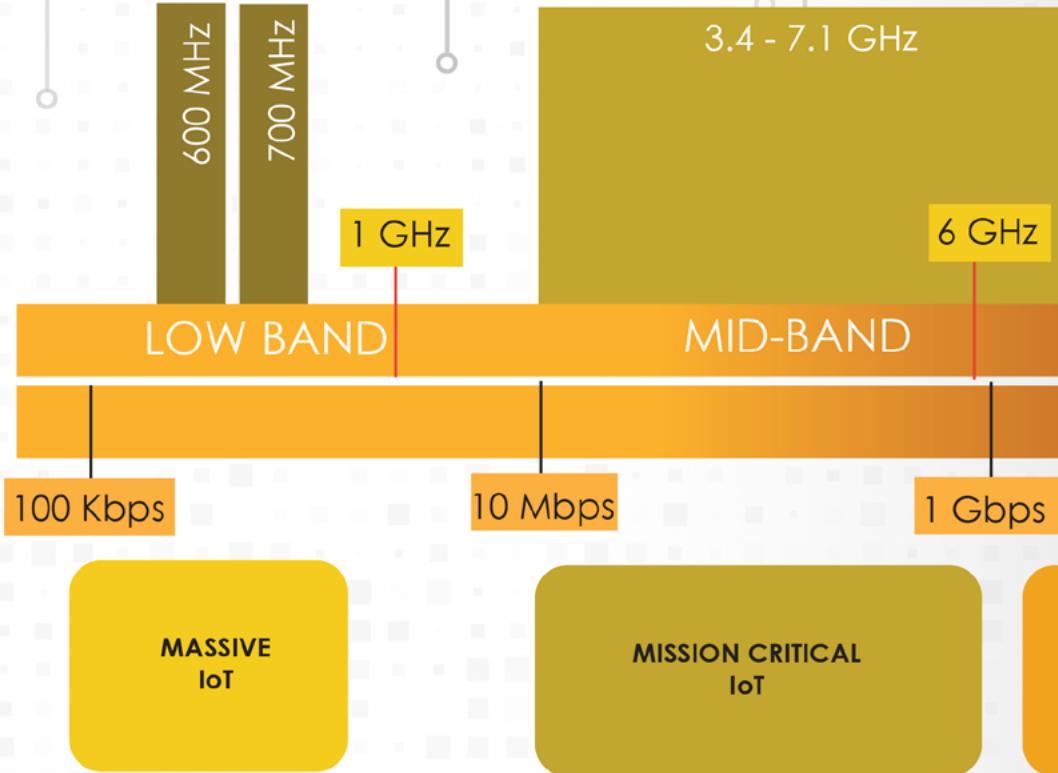
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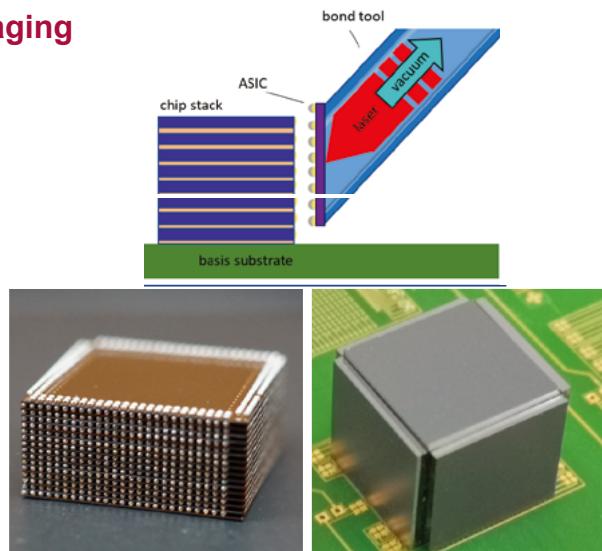
Automotive Network

FRASTRUCTURE

# New Advanced Bonding Technologies

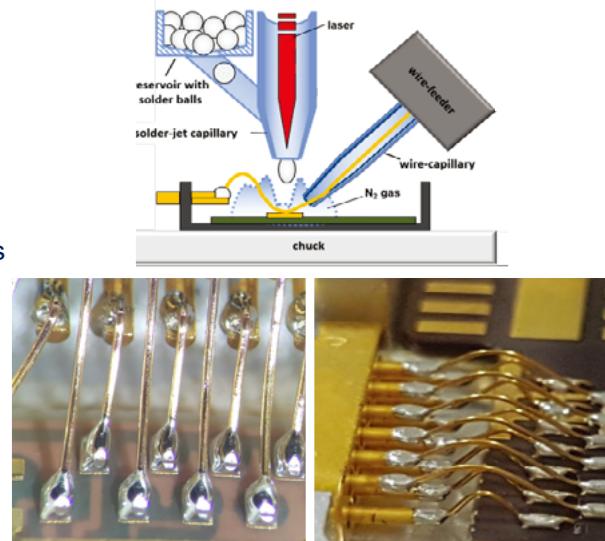
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## Stretchable flexible hybrid electronics

By Marius Ivan [Pricos Technologies Inc.]

The technological advances witnessed by the semiconductors and electronics industries are happening at an incredible pace, and with it, truly remarkable technologies are unleashed, such as machine learning, artificial intelligence (AI), Internet of Things (IoT), body monitor networks, independent robots, and the list keeps growing by the year.

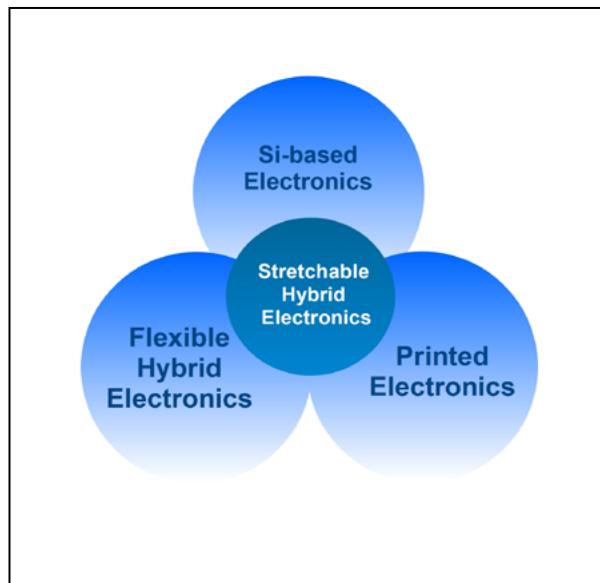
Towards the end of the '90s and early 2000s, large-area flexible electronics took off, promising some amazing features and new products that did not exist before. The new direction was enabled by the free form factor, the large area of the plastic substrates on which transistors were built, the low cost, and the enthusiasm of those who were part of the new technology wave.

The first processes to fabricate transistors on flexible substrates were borrowed from the semiconductor industry, when i-line and g-line optical lithography on plastic substrates temporarily attached to a Si wafer were used to fabricate transistors [1]. Optical lithography is still the patterning technology of choice for higher end flexible electronics that require high-performance/high-density of conductive tracks.

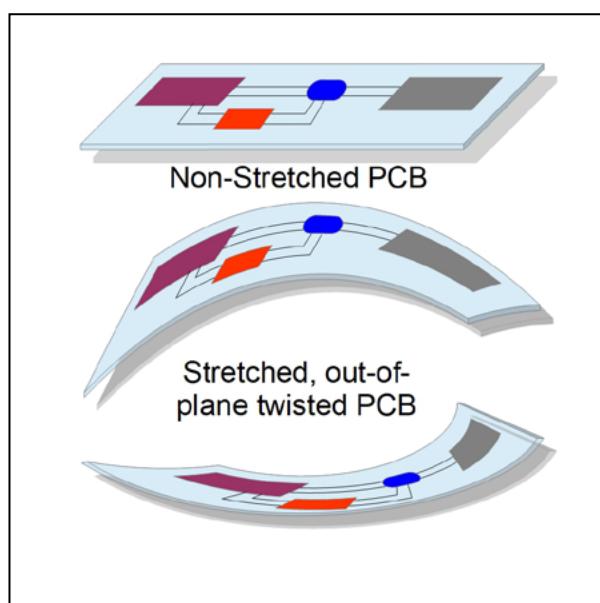
However, if flexible electronics were to make inroads, new patterning technologies had to be developed, enabling truly large-area and low-cost electronics. Printed electronics came along, together with development of printers and materials, and the introduction of roll-to-roll (R2R) fabrication. Vacuum deposition, photoresists, and etchants have been replaced by metallic, semiconductor and dielectric inks, and Si wafers are replaced by plastic foils, such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide [2]. The fundamental concept in flexible electronics is building from the bottom-up, making use of additive technologies as opposed to subtractive processes, which are used in optical lithography. The feature sizes in printed/flexible electronics are on the order of microns to tens of microns, so 2-3 orders of magnitude larger than state-of-the-art feature sizes in CMOS technologies.

The concept of fabricating low-cost large-area electronics like printing newspapers in R2R lines has been largely adopted by the flexible printed electronics industry. Technologies that were familiar to the printing industry, such as ink-jet printing, aerosol jetting, screen printing, R2R printing, and gravure, are now used to fabricate transistors, sensors, flexible displays, organic light-emitting diodes (OLEDs), solar cells, antennas, and memories.

The paradigm shift in the last few years has made room for a new concept, namely flexible hybrid electronics (FHE), which brings out the best of both worlds: Si-based microelectronics and flexible electronics. Silicon-based devices and components are highly performing and reliable. Embedding high-performance electronic components in a flexible printed circuit board (PCB) makes sense for some applications. The new island-bridge approach embraced largely by the FHE industry is more familiar to the traditional electronics industry, where the electronic components (islands) are



**Figure 1:** Illustration of the emerging stretchable hybrid electronics that builds on technologies, materials, processes, and components from Si-based electronics, hybrid flexible electronics, and printed electronics, while also demanding new materials and specific processes to be developed.



**Figure 2:** Graphical representation of stretchable, bendable, and twistable PCBs with embedded components linked by stretchable, electrically-conductive interconnects.

attached and soldered to an integrated circuit board.

The next generation of FHEs is built on substrates that are not only flexible, but also stretchable, bendable, twistable, and rollable down to a zero bending radius. A graphical representation of the synergy of the industries upon which stretchable hybrid electronics is built is displayed in **Figure 1**. The stretchable flexible hybrid electronics enable new applications, such as wearable (bio)sensors for monitoring human body functions, embedded electronics in textiles and clothing, and soft robot skin to name just a few. The “stretchable” term used to describe the property of the substrate and of the overall device encompasses other in-plane and out-of-plane deformations such as twisting, bending, and rolling as represented in **Figure 2**.

Stretchable FHEs bring up a new set of challenges that stem from the properties of the substrate, which is usually an elastomeric polymer such as the commonly used polydimethyl siloxane (PDMS). The use of polymer substrates and polymeric inks imposes limitations on the processing temperature, typically below 150–200°C, and on the use of organic solvents. The polymer substrates are prone to deformation during processing due to factors such as heat-induced deformations, and mechanical deformations. For substrates processed in R2R lines, the pulling induces stretching, which needs to be taken into account when patterning interconnects, and sometimes the substrates are pre-stretched on purpose for the patterning of interconnects.

The most obvious challenge is the development of materials and patterning of electrically conductive tracks that maintain their conductivity while stretched. The electrical resistance grows exponentially with the elongation, a feature not desired for certain applications that rely on resistance monitoring. Various routes have been adopted for the fabrication of stretchable interconnects, most of which fall under the following categories:

1. Patterning intrinsically conductive materials, such as:
  - composite materials of conductive particles with elastomeric polymers;

- electrically conductive polymers; and
- liquid metals.

2. Patterning engineered tracks with special structural design:
  - 2D serpentines;
  - 3D coils;
  - Nanomeshes; and
  - Origami, kirigami-shaped metal tracks.

Each solution mentioned above is suitable for certain applications and comes with its own pros and cons. Conductive composites are obtained by blending electrically conductive particles (e.g., metal particles such as Ag nanowires), multi-wall carbon nanotubes (MWCNTs), graphene, etc., with the polymer matrix. Such conductive composites rely on percolation of charges, and there is a minimum concentration of filler particles required to induce the electrical conductivity. The size and shape of the particles also influence the percolation threshold, as do their dispersion in the polymer matrix and properties of the matrix itself. Among the liquid metals, some Ga alloys are promising, and Hg, although used in the past, is highly toxic and its use has been banned [3]. While highly conductive, stretchable and adaptable to the shape of the substrate, liquid metals have their own limitations such as incompressibility, and need to be contained in micro-channels, environmental impact, leakage, etc.

Thanks to organic electronics, many electrically conductive polymers have been developed, i.e. polyaniline, polyacetylene, PEDOT-PSS, poly(3-hexylthiophene), etc. [4]. All-stretchable thin-film transistors (TFTs) printed on stretchable substrates have been previously reported [4].

In the island-bridge approach, as seen in **Figure 2**, the device is stretchable overall, however, its rigid electrical components (i.e., processor, antenna, battery, memory, etc.) are not, and that creates new challenges at the interface with the stretchable electrical interconnects. The contact between the stretchable interconnects and the rigid components will undergo additional mechanical strain during deformations.

Using the structural design, metal interconnects patterned as

2D serpentines, 3D coils, origami or kirigami, allow elongation of the conductive tracks. The design of each of these lithography- or laser-patterned shapes has a tremendous influence on the strain that the metal tracks may absorb, and several reviews have covered this topic in recent years [3]. Metal tracks are impacted by the mechanical strain and the different coefficients of thermal expansion (CTEs) of the metals and the elastomer, which ultimately leads to cracks, buckling or delamination of the tracks.

For the higher end applications, where processors and memory chips are embedded in the stretchable device, the challenge is to print stretchable interconnects with a high density. Soldering would need to be replaced by conductive adhesives. Packaging and encapsulation will need to be adapted to the new stretchable substrates. A processor packaged for a rigid PCB will most likely not work in a stretchable multi-layered device. Alternative routes would need to be investigated, with newly designed packaging, or even thinned bare dies that would be encapsulated in the stacked, multi-layered device. Wearable electronics patches that are attached to the skin and monitor various body functions such as blood pressure, pulse, oxygen levels or detect various analytes and disease-specific biomarkers in sweat are some of the first and most obvious applications of stretchable electronics. With capabilities such as sensing, data storage, processing, and Bluetooth transmission, these devices must be encapsulated with biocompatible materials.

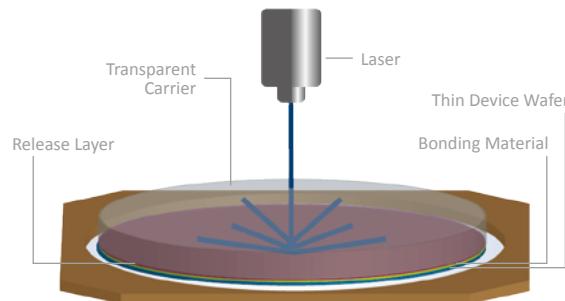
Heat management and heat dissipation need to be addressed, particularly in multi-layered stretchable devices built with elastomers, adhesives, and organic dielectrics, materials that typically have low heat transfer properties. Conduction, convection, and radiation are the mechanisms for spreading and releasing the heat to the environment. In the case of wearable patches, anisotropic heat transfer towards the environment and away from the skin would be ideal. Heat management solutions such as bulky and rigid heat sinks or mechanical cooling are not suitable for stretchable electronics, leaving the industry in need to develop novel and compatible heat management solutions. Such solutions need to be easily



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embedded, without significantly increasing the overall thickness or affecting the stretchability of devices.

Given the above considerations, a combination of multifunctional materials and device architecture would be needed to deal with the stringent requirements. The mismatch of the CTE of the various materials used to manufacture the FHEs adds to the complexity [2]. Although the nm-thick metal tracks (Au, Ag, Cu) deposited on top of an elastomer are flexible, they crack when subjected to elongations of the substrate. Due to differences in CTEs, metal layers deposited on stretchable substrates could delaminate or buckle. The use of various designs to induce stretchability in the metal interconnects (2D serpentines, origami, nano-/micro-meshes) allows fabrication of truly stretchable and soft electronics [5]. The use of design features, however, increases the area (footprint) on which these tracks are patterned, which may be incompatible with the dense interconnects needed to contact memory or processor chips. Therefore, there is a need to develop new materials for patterning interconnects that are intrinsically both highly conductive and stretchable.

## Summary

While seemingly two separate worlds, flexible electronics and microelectronics industries share many common challenges, and the enormous volume of knowledge and experience built over decades in the microelectronics industry could offer solutions to the challenges encountered by the flexible electronics industry.

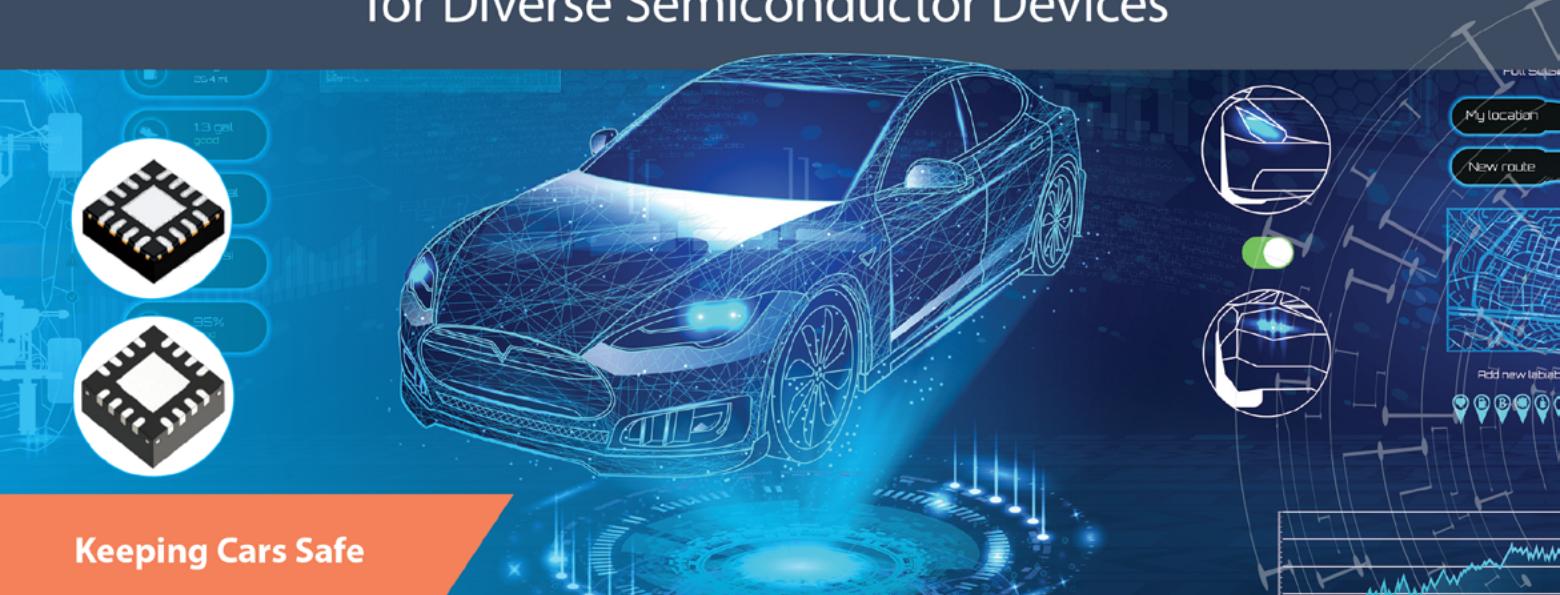
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## Biography

Marius Ivan is a Scientist/Owner at Pricos Technologies Inc., Ottawa, ON, Canada. He received his PhD in Chemistry from the U. of Ottawa in 2007 for his research on the photochemistry of chemically amplified resists. He then went on to work on flexible and printed electronics at Holst Centre in Eindhoven, Netherlands, followed by research on the development of quantum dots-based photonic materials, and devices at Philips Research. He continued his work on flexible electronics, specifically UV-curable polymer dielectrics and all-printed self-aligned transistors, at the National Research Council in Ottawa, Canada. At Pricos Technologies he works on the development of novel stretchable interconnects for flexible electronics. email [marius.ivan@pricostechnologies.com](mailto:marius.ivan@pricostechnologies.com)

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# Structural plastics for flexible hybrid electronics fabrication

By Tony D. Flaim and Jennifer See [Brewer Science, Inc.]

**A** surprisingly small range of polymeric materials have served the structural plastic needs of the microelectronics world for many years. The usual cast of characters has included epoxies (filled and unfilled), polyimides, silicones, benzocyclobutene thermoset (BCB), and bismaleimide-triazine (BT) resins. In large part, these polymer chemistries have been selected to match the rigidity and low thermal expansion characteristics of silicon and the generally high processing temperatures utilized in traditional package fabrication. However, the advent of flexible hybrid electronics, which are fabricated primarily by low-temperature, additive processing techniques, has created a need for plastic packaging materials with greater flexibility and elongation and that do not require long curing cycles at temperatures above 200°C or, more preferably, above 150°C.

## Basic types of plastics

Polymeric materials can be divided into two main classes — thermoplastics and curable plastics — which have very different molecular architectures. Thermoplastic polymer materials consist primarily of long, unbranched molecular chains that are coiled and physically intertwined, but that do not have permanent chemical linkages, i.e., crosslinks, between the chains. As a result, thermoplastics can be softened reversibly by heating them to a temperature where there is sufficient segment motion within the chains to allow them to flow under a shearing force. This behavior is the basis for convenient thermo-forming processes such as melt extrusion and injection molding. The crosslink-free architecture and typically high polymer molecular weight of thermoplastics give rise to many desirable properties such as good mechanical strength, ductility, elongation, and toughness. On the

other hand, the viscous polymer chains may not conform easily to a contacting surface, leading to poor adhesion when the thermoplastic is coated on or bonded to another material. At the same time, the absence of crosslinking can leave the plastic susceptible to attack by organic processing solvents, for example, when solution coating another layer onto a thermoplastic substrate. Likewise, the reversible softening of thermoplastics can be detrimental in process flows where elevated temperatures are encountered.

The second main class of polymeric materials are the curable plastics, which have been the dominant form used for semiconductor packaging. These materials are typically applied and processed as low-molecular-weight resins, which react to form highly branched, ultrahigh-molecular-weight networks when cured by heating at  $\geq 200^{\circ}\text{C}$ . The densely crosslinked architecture leads to high stiffness and rigidity along with robust thermal stability. Curable plastics are also known for their outstanding adhesion to other materials, with epoxies being the cogent example. However, as one might expect, most curable plastics exhibit very low elongation and can be brittle and subject to cracking under repeated thermal cycling, which makes them less than ideally suited for flexible electronics applications.

## A new polymeric material: photocurable thermoplastic

We have envisioned a new type of polymeric material that combines the desirable features of thermoplastics and curable plastics to better enable the production of flexible hybrid circuitry. In our concept, the polymer material performs like a thermoplastic in providing high strength, elongation, and toughness, and like a curable plastic in providing high chemical resistance and resistance to thermal flow. More specifically, we have developed photocurable thermoplastics

(PCTs) that can be crosslinked by ultraviolet (UV) exposure after coating and forming. Our overarching design objectives for the new PCT materials have included the following:

- High polymer molecular weight with moderate post-cure crosslinking density to maintain good mechanical strength, flexibility, and toughness;
- Intrinsic photosensitivity without the need for additives such as photo-acid generators, photo-initiators, synergists, crosslinking agents, etc.;
- Use fab-friendly solvent compositions for coating and film casting;
- Strong adhesion to semiconductor materials and other plastics;
- Ability to thermo-form (mold, emboss, extrude, etc.) below 200°C prior to photocuring;
- Thermal stability in excess of 300°C; and
- High-pulsed UV laser sensitivity to facilitate fast and clean laser drilling.

The ability to photocure the thermoplastic materials after application and final forming allows the user to take advantage of their reversible softening behavior prior to curing and then to convert the materials to a flow-resistant state by curing. The ability to use photocuring, as opposed to thermal curing, avoids the narrow processing latitude that can result from a competition between simultaneous thermally-induced softening and crosslinking.

## PCT materials & properties

Several examples of the new photocurable thermoplastic compositions can serve to demonstrate their unique combination of chemical, mechanical, thermal, and processing properties. Two of the new polymer compositions are designated here as PCT 1 and PCT 2. Their glass transition temperatures ( $T_g$ ) and molecular weight (MW)

Composition	Weight-Average MW	Number-Average MW	Polydispersity	T <sub>g</sub> (°C)
PCT 1	50,010	12,938	3.87	74
PCT 2	34,559	12,466	2.77	84

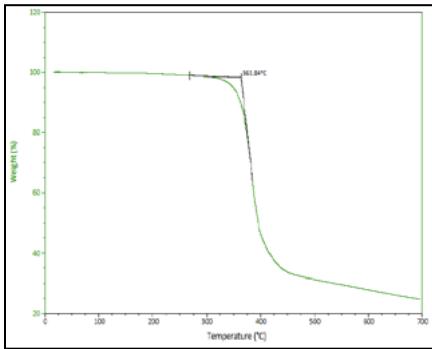
**Table 1:** Molecular weight characteristics and glass transition temperatures of new PCT polymers.

Composition	Film Thickness (μm)	Tensile Modulus (GPa)	Tensile Stress at Yield Point (MPa)	CTE (ppm/°C)
PCT 1	70	1.25	35	68
PCT 2	50	1.85	44	69

**Table 2:** Room-temperature mechanical properties of as-cast PCT films (no photocuring).

characteristics appear in **Table 1**. The T<sub>g</sub> values were determined by differential scanning calorimetry analysis of solid polymer samples, while the molecular weight properties were determined by gel permeation chromatography (versus polystyrene standards) for solutions of the as-prepared polymers. The following sections discuss properties associated with PCT materials.

**Thermal stability of PCT materials.** The ramp thermogravimetric analysis (TGA) scan image for composition PCT 1 is presented in **Figure 1**. The material showed excellent stability with no weight loss occurring until beyond 360°C. Composition PCT 2 behaved similarly, showing an instantaneous decomposition temperature of 348°C.

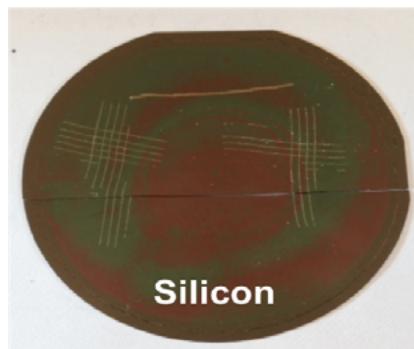


**Figure 1:** Ramp TGA scan image for composition PCT 1 under nitrogen at 10°C/min.

**Mechanical properties of PCT materials before and after photocuring.** PCT polymers in the pre-cured state are true thermoplastics and possess good flexibility and strength. The mechanical property data presented in **Table 2** for films of compositions PCT 1 and PCT 2 indicates that they are glassy and moderately stiff materials at room temperature. However, they are pliable and can be flexed repeatedly without fracturing. (Note that the tensile stress values are

reported at the yield point rather than the breaking point. Presumably, the tensile stress, i.e., the tensile strength, would be higher at the breaking point.) The mechanical properties and coefficients of thermal expansion (CTE) were determined by dynamic mechanical analysis (DMA) and thermo-mechanical analysis (TMA), respectively.

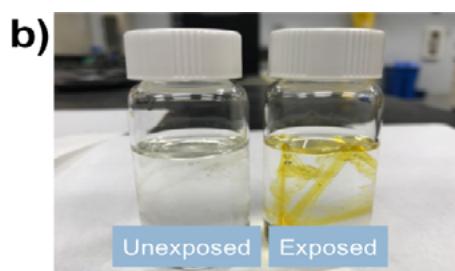
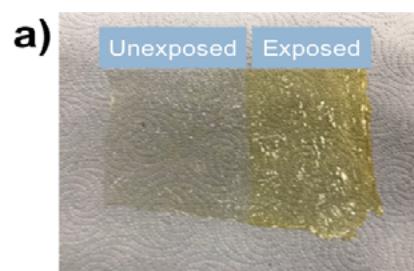
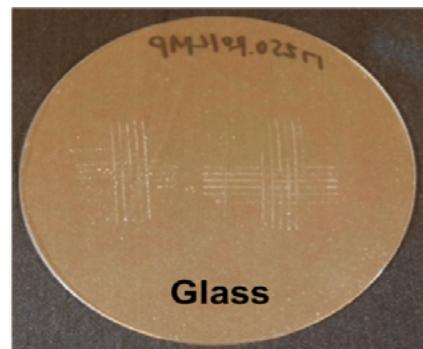
The introduction of chemical crosslinking into a PCT film by photocuring is beneficial for improving chemical resistance and reducing thermal flow (see later section). However, it does not cause embrittlement, but improves toughness and resistance to cracking when sharply bent. A film of composition PCT 1 remained very flexible and could be creased and folded after photocuring for five minutes under a 650W laboratory UV lamp.



**Figure 2:** Results of tape pull testing of cross-hatched films of composition PCT 1 coated on silicon and glass substrates.

**Adhesion properties of PCT materials.** PCT polymers show tenacious adhesion to many materials, including other polymers. As an example, silicon and glass wafers were spin-coated with a solution of composition PCT 1 and then baked at 120°C for 10min on a hot plate and subsequently at 130°C for 30min in an oven to remove solvents and leave a dry film. A standard cross-hatched tape pull test was then performed on the scored films using the highest adhesion strength 3M® test tape. Images of the test substrates appear in **Figure 2**. None of the pixelated features were removed from either substrate, indicating that the PCT material had excellent adhesion to silicon and glass.

**Effects of photocuring on solvent solubility and flow properties of PCT materials.** Exposure to mid-UV light changes the solubility and melt flow properties of the new PCT materials quite dramatically as a result of photo-induced crosslinking within the polymer structure. In **Figure 3a**, the image of a film sample of composition PCT 2 before and after a 5min exposure with a 650W laboratory UV lamp is presented. UV exposure caused an obvious color change in the film. At the same time, however, it became completely impervious to attack by dimethyl sulfoxide (DMSO), a powerful polymer solvent, whereas a sample of the uncured (unexposed) film dissolved within less than



**Figure 3:** a) (left) Appearance of film of composition PCT 2 before and after exposure; and b) (right) Exposed and unexposed film materials after immersion for 20min in DMSO.

a minute when placed in the same solvent. The radical change in solubility can be discerned clearly in the image of the two vial samples in **Figure 3b**. Later studies showed that a similar solubility shift was observable with as little as a 30s exposure to the UV lamp.

Photocuring also changes the thermal softening properties of PCT materials quite dramatically. The image in **Figure 4** reveals how exposed and unexposed film strips of a third composition, PCT 3, behaved in response to heating at 100°C for 30min. Composition PCT 3 has a  $T_g$  near room temperature and possesses very high elasticity and elongation, i.e., it is a soft material. When a strip of the film was exposed for several minutes to our laboratory UV lamp and then folded over so that the ends of the strip made contact with the center portion of the strip and subsequently heated, the areas in contact did not flow and bond together because they were crosslinked by the exposure process. On the other hand, the areas of the unexposed film strip that were in contact easily flowed and bonded together, essentially becoming a solid mass.

**Embossing of PCT materials.** To demonstrate that PCT materials can be thermo-formed below 200°C, an uncured, 5.8 $\mu\text{m}$  thick film of composition PCT 2 that had been spin coated onto a 200mm wafer was embossed by pressing it against a polysiloxane stamp formed on a second silicon wafer. The pressing step was conducted in a standard wafer bonding tool (EVGroup Model 510) with the wafers heated to 170°C under a force of 4000N for five minutes (pressure = ~18.5psi). The assembly was then cooled to room temperature and the stamp was mechanically peeled away from the embossed film. Microscopic images of the embossed features in the PCT film appear in **Figure 5**.

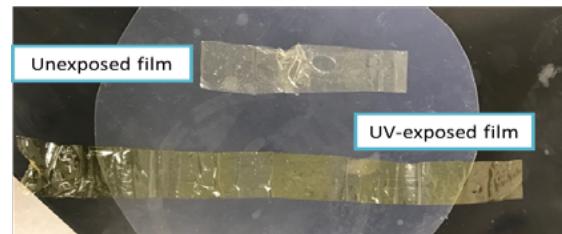
We assumed that photocuring of the embossed patterns would stabilize them against reflow when heated to high temperature. One of the embossed wafer substrates was masked in half and one side was exposed to the laboratory UV lamp for five minutes while the other side was left unexposed. When the wafer was heated to 180°C for five minutes, the features on the photocured side were well preserved, while the features on the uncured side flowed and became non-distinct as the comparative microphotographs in **Figure 6** reveal.

#### Optical properties of PCT materials.

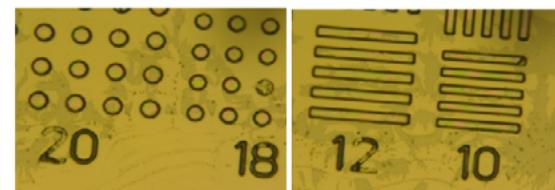
The new PCT materials have been designed with intrinsic photosensitivity to mid-UV radiation. That is, photocuring involves the direct reaction of functional moieties within the polymer structure and does not require any kind of added photo-initiators or synergists such as free radical-cured acrylic resins or cationically-cured epoxy coatings require. These same functional moieties possess very strong ultraviolet absorption as evidenced, for example, by the large optical extinction coefficients ( $k$ ) at mid-UV wavelengths for a structural relative of composition PCT 1 listed in **Table 3**. (A material with a  $k$  value of 0.1 is normally considered to be strongly absorbing.) The refractive index and extinction coefficient values in **Table 2** were determined by variable-angle scanning ellipsometry of a thin polymer film coated onto a silicon wafer.

**Laser etching of PCT materials.** The strong optical absorbance of PCT materials in the mid-UV portion of the spectrum makes them very sensitive to pulsed laser etching systems that typically operate at 308-355nm wavelengths for a structural relative of composition. Silicon wafers coated with a 10-15 $\mu\text{m}$  thick layer of a close variant of PCT 1 were patterned with pad (200 x 200 $\mu\text{m}$ ) and via (100 $\mu\text{m}$  diameter) features by Laser Light Technologies (Herman, MO) using a custom picosecond pulsed laser system operating at 355nm. The other relevant laser operating parameters were as follows:

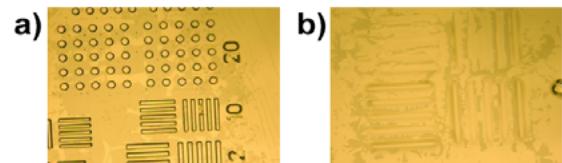
- Laser pulse energy - 0.33 $\mu\text{J}/\text{pulse}$
- Average laser power - 0.825mW
- Peak laser power - 22kW
- Pulse length - <15ps
- Laser repetition rate - 2500Hz



**Figure 4:** Appearance of UV-exposed and unexposed film strips of composition PCT 3 after heating at 100°C for 30min.



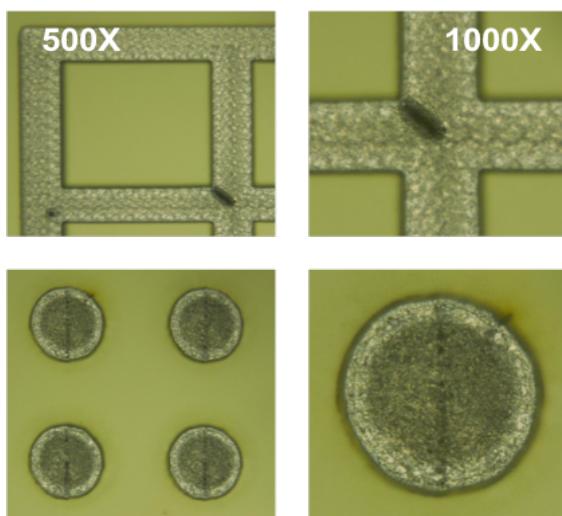
**Figure 5:** Microscopic images of circle and line features embossed in a film composition PCT 2 at 170°C. The numbers in the microphotographs refer to the feature sizes in microns.



**Figure 6:** a) (left) Microphotograph of embossed features after photocuring and then heating to 180°C; and b) (right) The same embossed features but not photocured before heating.

Wavelength (nm)	Index of Refraction ( $n$ )	Extinction Coefficient ( $k$ )
308	1.4477	0.179
343	1.4997	0.300
355	1.5578	0.372
365	1.6846	0.415

**Table 3:** Refractive index and optical extinction coefficient values for a structural relative of PCT 1.



**Figure 7:** Microscopic images of pad and via features patterned in a closely related structural variant of PCT 1 by a picosecond laser etching system.



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Figure 7 displays microscopic images of the pad and via features after the specimens were cleaned by sonication for a few minutes in deionized water. (The PCT material is yellow-green in color while the exposed silicon, which was slightly etched by the laser, has a roughened, metallic appearance.) As can be seen, the etching process produced little carbonaceous residue and the feature edges were sharp and crisp. It is notable that the etching was performed at  $<1\text{mW}$  average laser power. Higher power settings caused the PCT material to char because it absorbed the laser light so effectively.

### Summary

Photocurable thermoplastic polymers represent a new design paradigm in structural plastics. They combine the desirable mechanical properties of high molecular weight thermoplastics with the thermal and chemical resistance of curable plastics. Moreover, one can take advantage of both the thermoplastic and curable characteristics of the materials in a conventional processing flow because curing of the starting thermoplastic form relies on UV irradiation, rather than heating to high temperatures as curable plastics usually require.

We foresee that the robust physical properties and unique processing possibilities with PCT materials can be valuable in a variety of flexible hybrid circuit applications. Obviously, their good flexibility and elongation combined with good stiffness to well above room temperature suggests their use as a base substrate material. Perhaps more intriguingly, one can imagine a substrate in which there are more rigid regions created by patterned photocuring and more flexible regions that are left in the thermoplastic (uncured) state. It is not difficult to imagine other uses for these new materials and we challenge readers to consider how PCT materials might be used in their microelectronic applications.



### Biographies

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# Challenges in automotive packaging technologies

By Emilie Jolivet [Yole Développement] and Prasad Dhond [Amkor Technology, Inc.]

**F**our main trends are driving innovation in the automotive industry: electrification, autonomous driving, connectivity and comfort. Due to environmental considerations, governments want to decrease carbon dioxide ( $\text{CO}_2$ ) emission levels by promoting electric cars and developing clean energy consumption. While safety has always been a major factor in modern vehicles, with the expansion of autonomous vehicles, a lot of investment has been made to develop even safer cars. With advanced driver assistance systems (ADAS) in cars and robotic vehicles, passengers' comfort and entertainment are also becoming a nice "must have" for in-cabin options.

Today, the automotive industry is looking more and more to the semiconductor industry and expectations for the coming years are getting higher. The car industry represents US\$2.3 trillion with a compound annual growth rate (CAGR) of +2.7% over the next five years. Automotive electronics accounts for US\$142 billion with a CAGR of +7% (Figure 1) [1]. The amount of electronics in a car has increased by 2.5 times since the 90s. Driven by the adoption of more electronics components in end-products, the semiconductor industry is growing strongly.

Although the automotive market has a greater inertia to change compared to the consumer market, advanced packaging technology will become more and more overriding (see Sidebar). As a result, the packaging market is projected to grow from US\$3.7 billion in 2017 to almost US\$7 billion in 2023 [1]. Also, regulations and qualification needs are getting more specific for this industry. To respond to the demand and reduce production costs, original equipment manufacturers (OEMs) and Tier 1 suppliers have started subcontracting more from outsourced semiconductor assembly and test (OSATS) companies.

On one hand, packages need to be simple, reliable and affordable. On the other hand, some modules are including more chips with a higher level of

## Electronic megatrends: 2021 market values

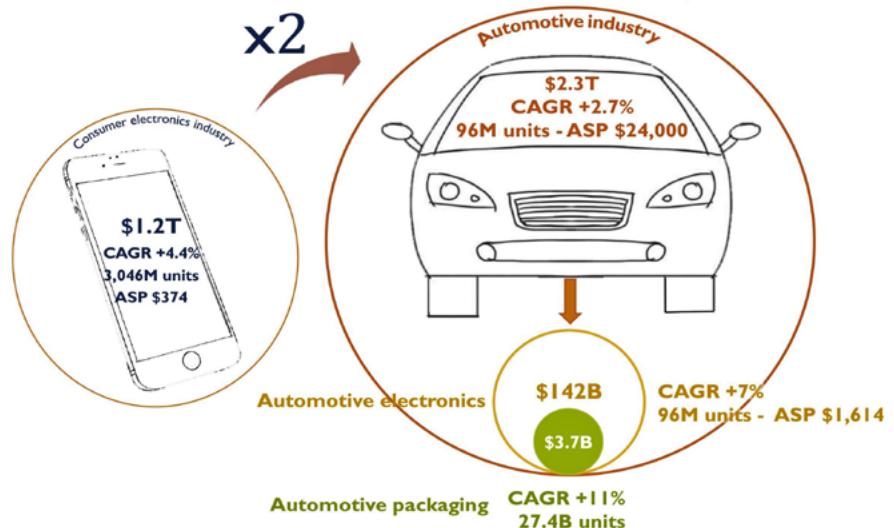


Figure 1: The automotive industry's need for advanced technologies continues to drive increasing electronics content. SOURCE [1]

## 2017-2023 Packaging revenue breakdown by the 4 market drivers for the automotive industry

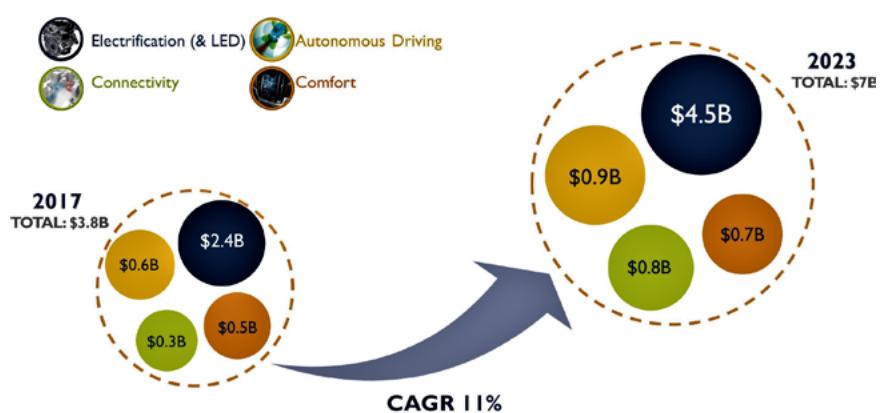


Figure 2: 2017-2023 Packaging revenue breakdown by the four market drivers for the automotive industry. SOURCE [1]

integration and a higher added value. With these varied requirements, OSATS are being given the opportunity to address these needs. This has been made possible because OSATS' manufacturing

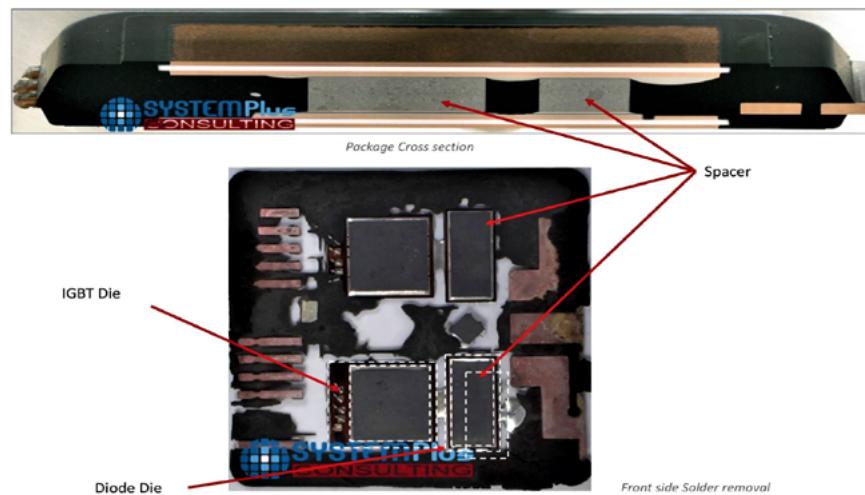
technologies are getting more sophisticated, thereby enabling them to handle higher levels of complexity. In the span of a few years, OSATS' market share in automotive packaging has grown

and reached 38% in 2017. As safety and comfort have to be increasingly implemented in ADAS cars and robotic vehicles, the number of sensors is increasing by 21% CAGR from 2017 to 2023 (**Figure 2**). By 2025, camera, light detection and ranging (LIDAR) and radar sensors will equip all of the high-end vehicles and a large portion of the middle range cars. With the augmentation of sensitive sensors for safety applications, chip performance needs to be optimum. To meet those stringent requirements, chip packages need to evolve. For example, for CMOS image sensors (CIS), there are two types of setups, some are packaged with organic materials and others with ceramic materials. Both types of packages will grow due to a significant increase in the number of camera sensors per car. Radar sensors were originally packaged in wire bond packages. Now, they are slowly moving to fan-out (FO) designs with more chips integrated per package thanks to flip-chip technology. With larger systems, such as multi-dies and wafer-level chip-scale packaging (WLCSP), the objective is to cut costs.

To enter the automotive market, components have to pass qualification tests depending on the grade associated with their application. Each grade level from the Automotive Electronics Council (AEC) merely provides a reference of what the device or system has to withstand at its operating conditions. Some packages are already qualified for automotive standards, but for the most aggressive grades, some improvements are expected. Reliability and high-temperature resistance are key. To qualify a new package, quality checks are longer and more demanding than for other industries.

Investing in new types of packages for sensors in the automotive industry is a way to add value. Thanks to flourishing integration of infotainment and entertainment applications in cars, technologies from the consumer market are being adapted to the automotive market. In fact, the car is becoming an extension of the driver's smart phone or smart home. By adapting consumer products to the automotive world, their packages are getting automotive qualified for use in vehicles, helping OSATS and integrated device manufacturers (IDMs) to reduce development time—if minimal or no modifications are required.

## Package opening - From front side



**Figure 3:** Infineon FF400R07A01E3 Double Side Cooled 700V 400A IGBT Module – multiple cross sections.  
SOURCE [2]

Driven by in-cabin safety, more and more equipment is implemented in the cockpit that could also be used for infotainment and entertainment. Gesture and speech recognition are the next way to interact with the central cluster and the on-board system. Cameras could be used for driver monitoring, but also for gesture recognition and man-machine interaction. Those systems will use artificial intelligence (AI) and will require powerful processing hardware. Those new applications will take advantage of the ADAS computing platform built in for autonomous driving computing. Packaging these new systems is also a challenge. Today, there is no automotive standard for these advanced chips, so most of the OEMs use expensive and powerful chips from Nvidia, Renesas or Kalray. Those platforms use graphics processing units (GPUs) that are currently packaged on an interposer with stacked memory, and still not yet optimized for the automotive market.

Following the trend towards more electrification, power conversion applications are the strongest driver for automotive packaging innovation with 18% CAGR. While talking about power conversion, one of the main issues is thermal management. To provide better cooling solutions without expanding the footprint, improved packaging techniques must be implemented. With double-side cooled, card-like modules, copper clips

and side-to-side chips in quad flat no-lead (QFN) packages, the degree of integration gets higher, requiring better thermal power dissipation (**Figure 3**). To achieve better thermal management, new types of heat dissipation materials must be used. As a result, the industry is searching for ceramic-less substrate solutions as an alternative to organic substrate materials. This year, it has been made public that Tesla was the first high-class car manufacturer to integrate a full silicon carbide (SiC) power module. This new module is made by STMicroelectronics and multiple modules are integrated in the new Tesla Model 3. Each module contains two SiC MOSFETs with an innovative die attach solution and connected directly onto the terminals with copper clips, and thermally dissipated by copper baseplates.

## Acknowledgments

This article has been written in collaboration with Mario Ibrahim, Technology & Market Analyst, Advanced Packaging and Jérôme Azémar, Project Development Director at Yole Développement.

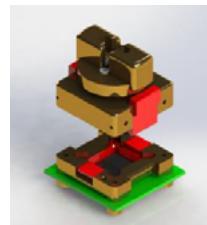
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1. “Trends in Automotive Packaging 2018” report, Yole Développement, 2018.
2. “Infineon FF400R07A01E3 Double Side Cooled IGBT Module” report, System Plus Consulting, 2018.

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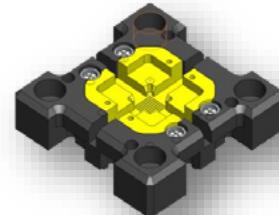
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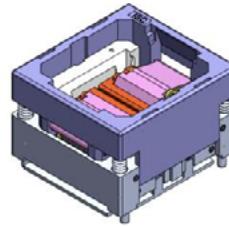
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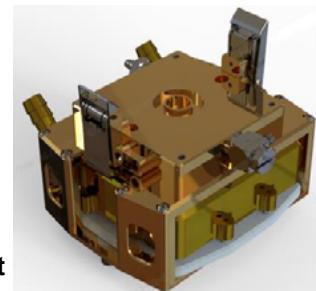
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# Automotive OSAT challenges

By Prasad Dhond [Ankor Technology, Inc.]

**A**utomotive is one of the fastest growing segments in the semiconductor industry. Due to their long lifecycle, automotive applications provide a stable volume base and higher returns on investment (**Figure S1**). However, the automotive business is also tough and has high barriers to entry. Suppliers must support long lifecycle products to ensure business continuity. Automotive customers are looking for suppliers that have the highest levels of experience, technical capability and quality.

## The shift towards advanced packaging in automotive

Although 80% of automotive packaging still uses wire bond technology, the trend is towards advanced packaging. Flip-chip ball grid array (FCBGA) is the most popular advanced package for processors used in advanced driver-assistance systems (ADAS). The high I/O count, thermal and electrical performance requirements of these processors are best supported using FCBGAs (**Figure S2**).

Low-density fan-out (LDOF) technology is used for packaging mmWave radar transceivers to achieve superior electrical performance. Flip-chip chip-scale packaging (fcCSP) is also used for radar transceivers and high-performance microcontrollers (MCUs) that were previously packaged in wire bond BGAs.

Infotainment applications use processors in system-in-package (SiP) form factors. These SiPs combine the

processor, memory and other support components together in a standard form factor such as FCBGA. A modular SiP approach speeds up time to market and provides flexibility to car original equipment manufacturers (OEMs) to upgrade processors without making changes to the surrounding circuitry.

## Wire bond packages in automotive

A majority of analog integrated circuits (ICs) and MCUs that are sprinkled all over the car still use wire bond packages. Wire bond packages have a long history in automotive electronics, and will continue to play a crucial

part in powertrain, body, and chassis applications. The focus for automotive wire bond packages has been to improve reliability performance using enhanced material sets. Almost all new automotive wire bond products now use copper wire. To achieve higher automotive reliability, there are many variations of copper wire being tested. Lead frame packages use lead frames that undergo treatments such as roughening for better adhesion with interfaces to prevent delamination. For some packages, epoxy molding compounds (EMCs) with lower sulfur content are used to enhance the reliability with copper wire in automotive applications.

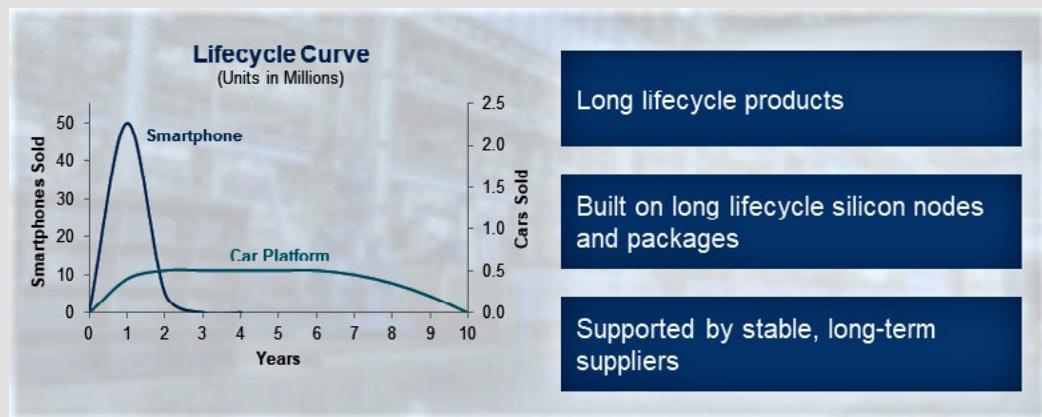


Figure S1: Automotive product requirements provide a challenge to any supplier.

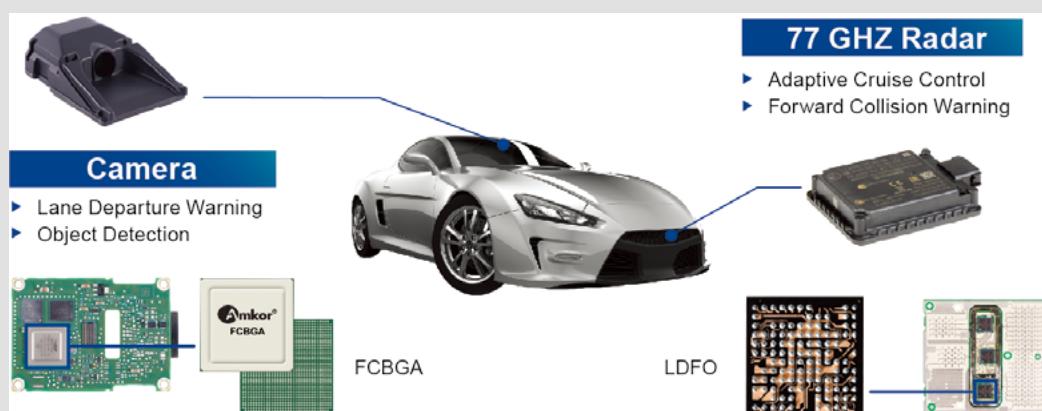
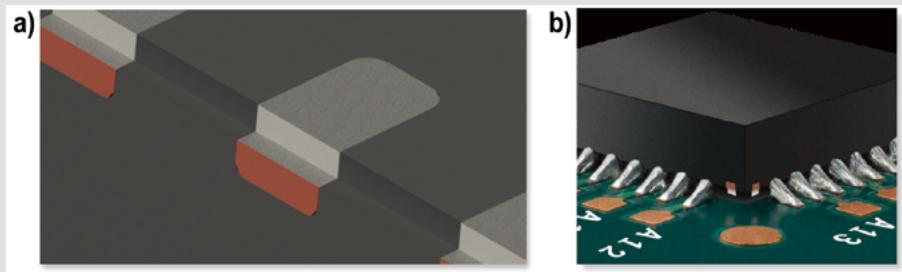


Figure S2: Emerging applications in cars require different types of advanced packages: SOURCE: IHS Markit Teardown

Quad flat no-lead (QFN) packages with plated-end-lead (PEL) designs are popular in automotive applications. Automotive customers require solder joint inspection of IC packages mounted on printed circuit boards (PCBs). However, solder joints of leadless QFN packages are not visible and require the use of expensive X-ray inspection. The PEL option for QFN packages forms visible solder fillets that can be inspected using standard automated optical inspection (AOI) equipment (**Figure S3**).



**Figure S3:** Plated-end-lead QFN packages provide a visible solder fillet when mounted on a PCB: a) (left) Saw-singulated QFN bottom view, b) (right) Mounted on board.

<b>Operating Hours per Day</b>	1.5 hours	8 hours	22.5 hours
<b>Operating Hours over Lifetime</b>	8,000 hours	40,000 hours	123,000 hours
<b>HTSL</b>	1,000 hours	4,000 hours	10,000 hours

**Figure S4:** Automotive lifetime requirements dictate rigorous qualifications tests.

The use of electric vehicles is growing and power semiconductor suppliers, including OSATS need to provide reliable, efficient and cost-effective solutions. Sub-systems such as traction inverters, DC-DC converters and on-board chargers for xEV vehicles use power semiconductors in different form factors such as:

1. Discrete packages: Standard power packages such as TO263, TO247 and their derivatives are popular in automotive applications.
2. Modules: Modules house multiple components used as switches for power stages. For example, Si insulated-gate bipolar transistors (IGBTs) with free-wheeling diodes; or SiC metal-oxide semiconductor field-effect transistors (MOSFETs) with Schottky barrier diodes. In

addition, the modules provide cooling mechanisms such as double-sided cooling (**Figure 3**, main article).

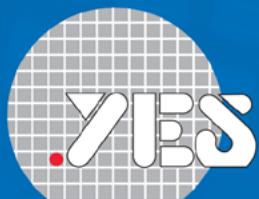
### New challenges for automotive packaging

There are several automotive trends that impact the semiconductor and packaging industry:

1. Leading-edge technology nodes are being used in ADAS processors. For example, Intel's Mobileye EyeQ5 is planned to be developed on a 7nm FinFET process [SR1]. There is limited field experience with advanced nodes that require different techniques to assess reliability of the silicon and packaging.
2. The mission profiles of cars are changing. For example,

components in electric cars have longer operating hours on account of the additional charging time. This translates into higher requirements for reliability tests such as high-temperature storage life (HTSL) (**Figure S4**). The requirements specified in documents such as the Automotive Electronics Council's (AECs) AEC-Q100 standard are often extended or modified to closely match the actual mission profiles of specific applications.

The “multiplier effect” is the main challenge in automotive semiconductor reliability. Even a 1 part per million (ppm) failure at the component level will multiply to a 1% defect rate in the vehicle. For the highest reliability, the goal is zero defects. This challenge is even more pronounced with the



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rising electronic content in cars. In spite of this, quality expectations have never been higher, and customers now measure defects in “number of quality incidents” instead of ppm.

## Certifications and standards

Suppliers to the automotive industry must have International Automotive Task Force IATF16949:2016 Quality Management System (QMS) certification. The suppliers must also be compliant with or support other Automotive Industry Action Group (AIAG) standards/requirements such as advanced product quality planning (APQP), failure modes and effects analysis (FMEA), Production Part Approval Process (PPAP), statistical process control (SPC) and measurement systems analysis (MSA). Process audits must be conducted using VDA 6.3 checklists.

Qualification and reliability testing are conducted using AEC standards. The standard varies by the type of component, such as AEC-Q100 for integrated circuits, AEC-Q101 for discrete components, and AEC-Q104 for multi-chip modules.

## Beyond certifications and standards

Achieving certifications and standards compliance is a good start, but only the minimum requirements for a successful automotive supplier. There are other controls and best practices that must be implemented for automotive products, such as:

- Automotive products should be manufactured using designated equipment that is operated by automotive trained operators.
- Automotive material sets and process flows must be developed to achieve higher reliability. Automotive control plans must be established for enhanced monitoring and tighter SPC control.
- Design rules must be established to improve reliability and manufacturability of automotive packaging construction.
- A reliable and high-quality supply chain must be established and maintained. This supply chain must be managed with enhanced practices such as using VDA 6.3 checklists for audits and establishing more stringent material inspection criteria.
- A higher level of automation must be used in automotive factories to eliminate human error and minimize variations in production.
- Automotive suppliers must use best known 5S (a Japanese method to sort, set in order, shine, standardize and sustain) practices to maintain a cleaner manufacturing environment for automotive products.
- A safe launch process must be used to ramp automotive products successfully to high-volume production.

Suppliers must be financially sound to support long life-cycle applications. They should have a strategic focus on the automotive market that is backed up by investments in automotive quality initiatives. Automotive OEMs and Tier 1 suppliers are looking for stable partners that can support them in the long-term. An increasing number of automotive applications are moving to advanced packages that require packaging partners with technology expertise.

Quality remains the most important factor in automotive applications. Automotive suppliers must go beyond basic certifications and standards. They must provide intelligent package design, automotive materials and processes, tighter controls and automotive-certified personnel that help manufacture consistently high-quality products. This creates an automotive culture and mindset at the supplier that is necessary to achieve the zero defects goal.

## Sidebar reference

SR1. The Evolution of EyeQ, Mobileye's website, <https://www.mobileye.com/our-technology/evolution-eyeq-chip/>



## Biographies

Emilie Jolivet is Director of the Semiconductor & Software Division at Yole Développement, part of the Yole Group of Companies, where her specific interests cover package and assembly, semiconductor manufacturing, memory and software and computing fields. Based on her valuable experience in the semiconductor industry, Emilie manages the expansion of the technical and market expertise of the Semiconductor and Software Team. She holds a Master’s degree in Applied Physics specializing in Microelectronics from INSA (Toulouse, France). After an internship in failure analysis at Freescale (France), she was an R&D engineer for seven years in the photovoltaic business where she co-authored several scientific articles. Enriched by this experience, she graduated with an MBA from IAE Lyon and then joined EV Group (Austria) as a Business Development Manager in 3D & Advanced Packaging before joining Yole Développement in 2016. Email: [jolivet@yole.fr](mailto:jolivet@yole.fr)



Prasad Dhond joined Amkor Technology in 2014 and is VP of Amkor’s Automotive Market Segment. He previously managed the Quad and Dual Leadframe product lines. Prior to joining Amkor, he worked at Texas Instruments for 12 years where he held roles in product definition and marketing in the Analog product group. He holds a BSEE degree from the U. of Texas at Austin, and an MBA from Southern Methodist U.

# OSAT perspective: automotive semiconductor market & manufacturing challenges

By Asif R. Chowdhury [UTAC Group]

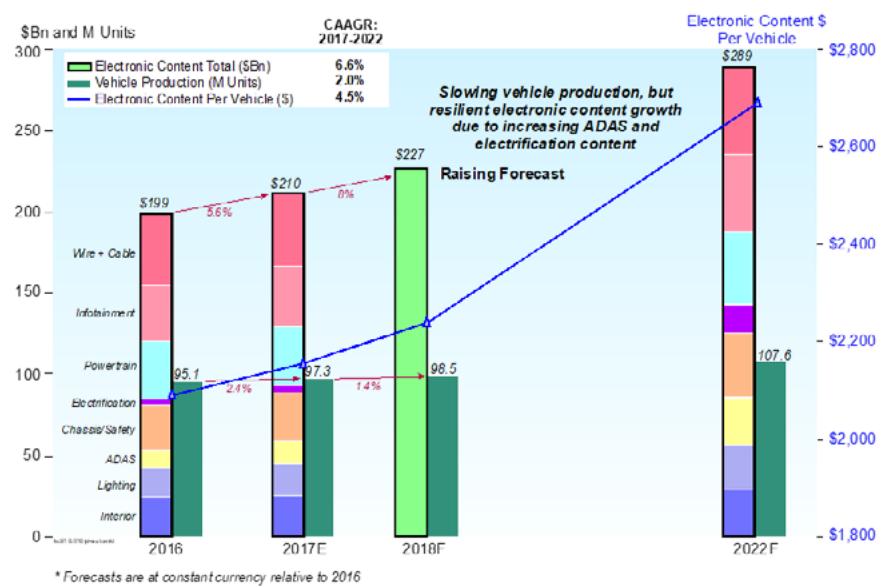
The automotive semiconductor segment has consistently grown during the last ten years showing no sign of slowing down. Primarily driven by adoption of electronics in almost all aspects of vehicle management, the growth has become even more secured by acceleration of safety standards and the growth of semi-to-full autonomous electric vehicles. **Figure 1** shows that the automotive electronic content is forecasted to rise from \$199B in 2016 to \$289B in 2022 — an increase of 45% — despite a 13% growth in vehicle production during the same period. **Figure 1** also shows that hockey-stick style growth of electronic content dollar per vehicle — from a little over \$2,000/vehicle in 2016, to an estimated \$2,700/vehicle in 2022.

**Figure 2** shows the estimated growth of the number of radars, camera (CMOS image sensor [CIS]) and light detection and ranging (LIDAR) sensor modules per the level of vehicle automation. Most of the high-end vehicles today are at Level 2, whereas Level 5 is a fully autonomous vehicle. As the figure shows, the number of each of these sensor modules is predicted to grow significantly at Levels 4/5 [1].

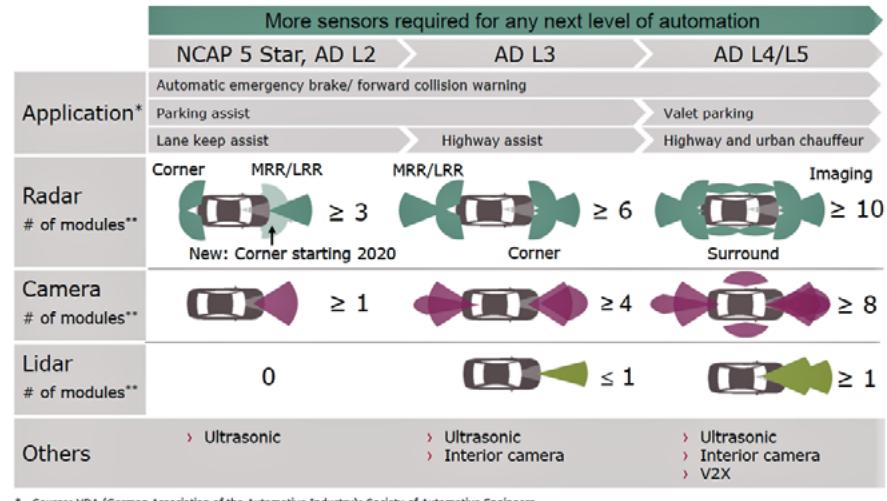
All the electronic content growths areas noted above are utilizing various kinds of semiconductor products. **Table 1** shows the semiconductor revenue growth by end application from 2013 through 2018, as well as the forecast from 2019 through 2023. In the last five years (2013–2018), the automotive market had grown by 7.3% compound annual growth rate (CAGR) and in the next five years, from 2019 through 2023, it is predicted to grow by another 6.3% CAGR, the highest semiconductor market segment growth.

## The automotive supply chain and key players

**Table 2** summarizes the automotive semiconductor supply chain and the top players within each of these supply chain



**Figure 1:** Automotive electronic market 2016-2022. SOURCE: Prismark Oct'18



**Figure 2:** Number of radar, camera and LIDAR modules per vehicle per level of automation. SOURCE: © Infineon Technologies AG.

industries. Unlike most other markets and industries, the semiconductor integrated device manufacturers (IDMs) typically do not supply their products directly to the automotive original equipment

manufacturers (OEMs). Instead, they supply their products to a different group of companies known as “Tier 1” suppliers, such as Bosch and Continental in Europe, Denso and Aisin in Japan, or Mobis in

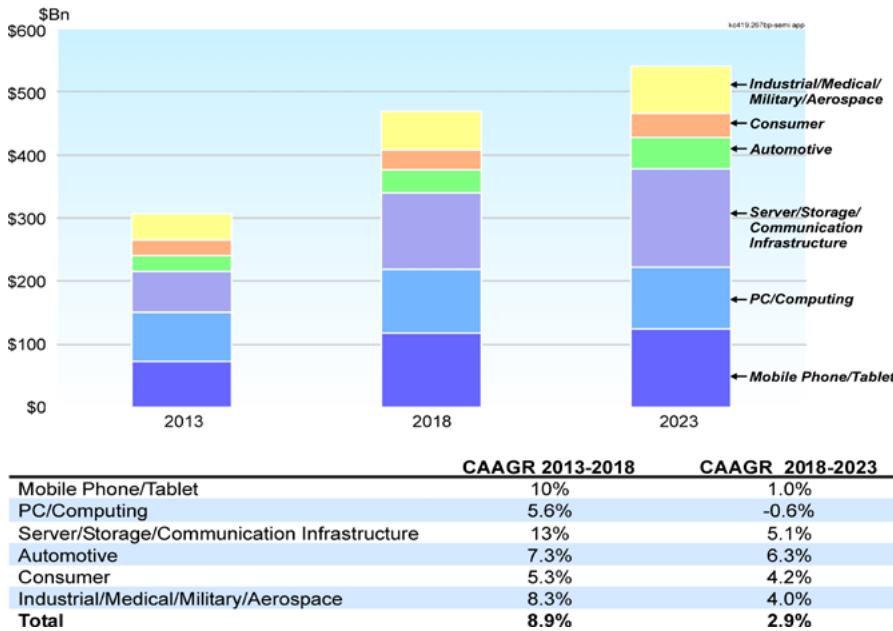


Table 1: Semiconductor revenue by end application 2013-2022F. SOURCE: Prismark

Korea. These Tier 1 suppliers produce various electronic and sensor modules and components for the automotive OEMs. For example, the Tier 1 suppliers produce brake or transmission modules, oil pressure or level sensor modules, and air bag sensor modules. Semiconductor components are an integral part of these modules manufactured by Tier 1 suppliers. Most of these top semiconductor IDMs such as NXP, Renesas or Analog Devices, have their own internal wafer fabs, assembly and test facilities. However, the outsourcing trend has been on the rise with outsourcing of assembly leading the path. The IDMs typically prefer not to outsource the wafer fabrication, nor the wafer probe and test

operations in order to have better control over these manufacturing processes. This is primarily because of the stringent quality requirements for automotive applications. Perhaps for the same reason, there are only a handful of outsourced semiconductor and test suppliers (OSATS) participating in the automotive assembly and test market. The top three OSATS providing automotive assembly and test services are Amkor, ASE and UTAC with a combined market share of 95% [2]. The challenges of automotive assembly, as outlined in the later sections, are not trivial and the barrier to entry is relatively high – it requires specially trained manufacturing personnel with a “continuous improvement leading towards a zero defect” type of mindset. Additionally, it may take up to four years to realize any meaningful revenue from a lot of hard work and effort by a lot of valuable resources. It must be mentioned that some fabless design houses (such as Qualcomm)

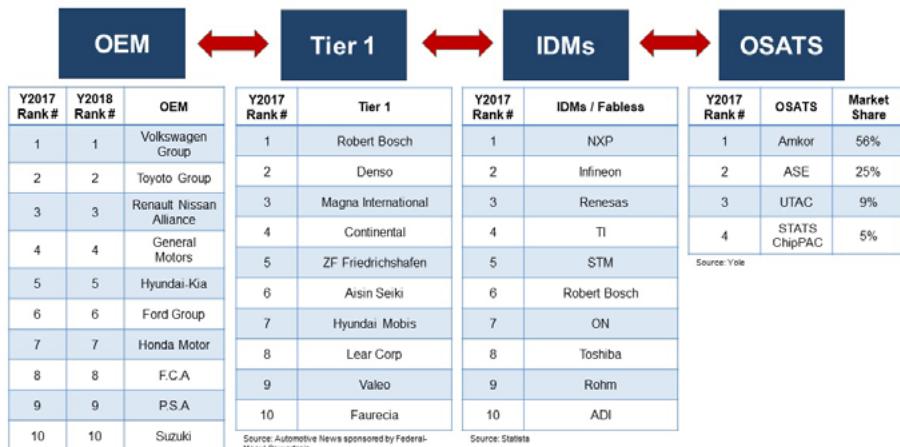


Table 2: The automotive semiconductor supply chain and the top players.

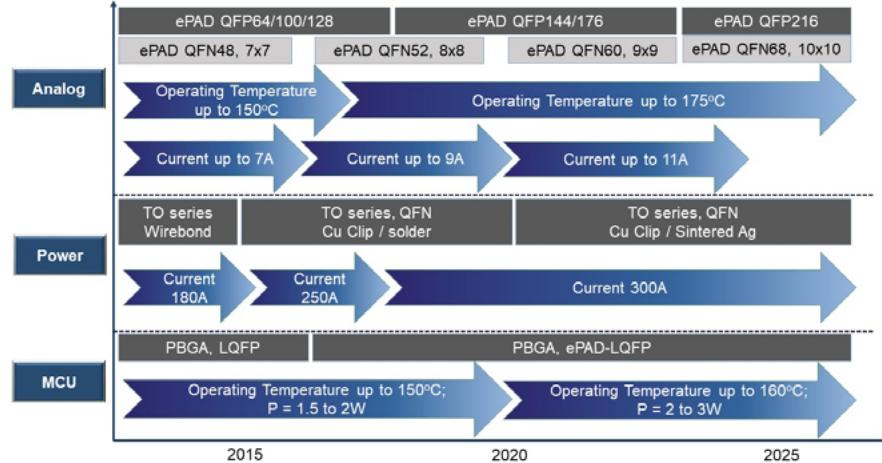


Figure 3: Automotive packaging technology roadmap based on technical requirement for MCU, power and analog products [3].

also provide semiconductor components to the Tier 1 automotive suppliers. Of course, they outsource all their manufacturing to foundries and OSATS.

### Package technology in automotive applications

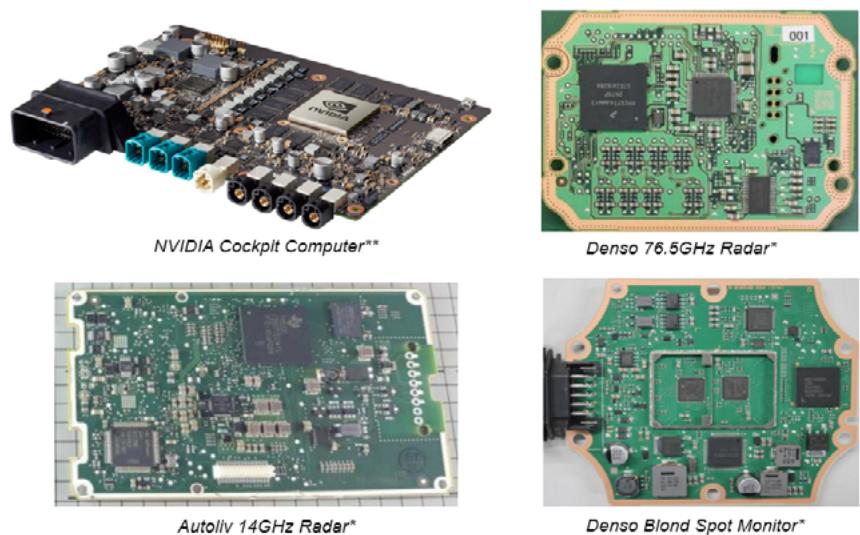
With respect to package types, automotive Tier 1s and OEMs are now using advanced packaging solutions along with the traditional lead frame-based packages. The trend is driven by technology requirements, package size, and cost reduction. For example, 8-bit automotive microcontrollers used to be in thin shrink small outline package (TSSOP) and quad flat package (QFP)-

type packages and have mostly migrated to quad flat package no-leads (QFNs), which have smaller form factor and lower cost. However, going to 16-bit and to 32-bit microcontrollers, flip-chip ball grid array (FCBGA) package solution is utilized due to higher I/O density. **Figure 3** shows a high-level roadmap for automotive microcontroller units (MCUs), analog, and power products based on operating temperature and current/power requirements [3].

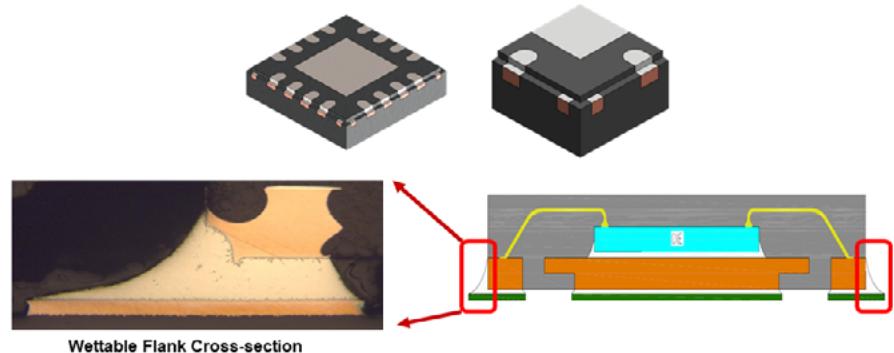
The roadmap shows the significant use of lead frame based packages through 2025. However, with high-power and current or high-temperature applications, advanced lead frame packaging solutions such as exposed pad, Cu-clip interconnect technology, and Ag-sintering process are utilized. **Figure 4** shows modules from various Tier 1 suppliers showing the heavy use of lead frame-based packages. Within the lead frame family, driven by the need for size and cost reduction, the use of QFNs in cars has significantly increased. The automotive industry, however, requires a special version of the QFN, which has side-solderable flanks. Automotive component manufacturers require inspectable solder joints that can't be done with standard QFNs. **Figure 5** shows details of side-solderable QFNs. Both UTAC and Amkor Technology have patents for side-solderable QFN solutions.

Traditionally, automotive players used to stick to standard lead frame packages with proven reliability. Due to the proliferation of semiconductor applications in vehicles, there has been an increase in the use of advanced packaging solutions. **Figure 6** shows a general automotive package roadmap. While standard packages will continue to be used for years to come, advanced packages are now being used and are increasingly showing up in the automotive package roadmap. The advanced packaging solutions are being used in products such as radars (wafer-level chip-scale packages [WLCSPs] and system-in-package [SiP]), high-performance CPUs (high-pin count FCBGA and SiP), and multi-function modules (SIP and embedded solutions).

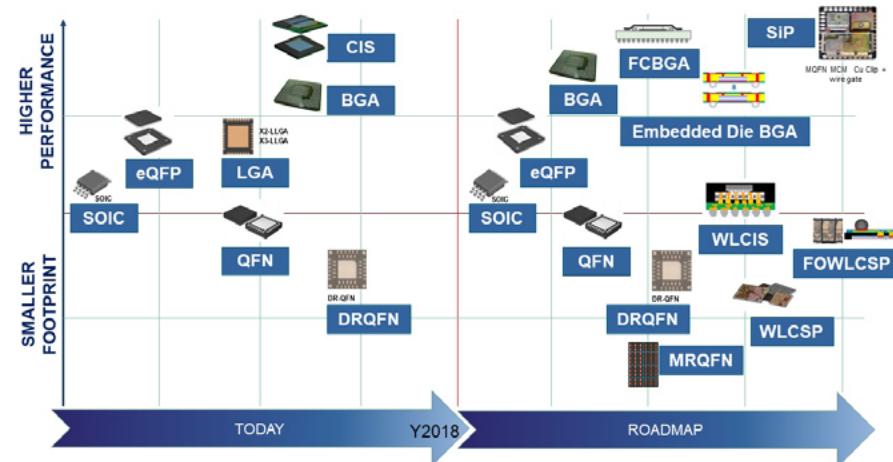
The use of sensors in cars has proliferated significantly—it is estimated that there are more than fifty sensors in a standard automobile today. Whereas microelectromechanical systems (MEMS) sensors, such as accelerometers and gyros, are using more standard laminate-



**Figure 4:** Examples of various automotive application modules showing high usage of lead frame packages.  
SOURCE: \*TechSearch International; \*\*NVIDIA



**Figure 5:** The automotive industry requires side-solderable QFNs allowing inspection of the board-level solder joint.

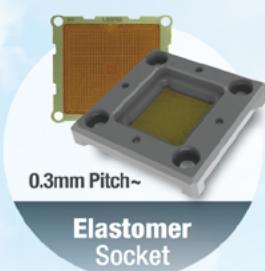
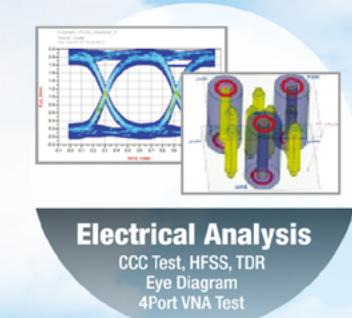
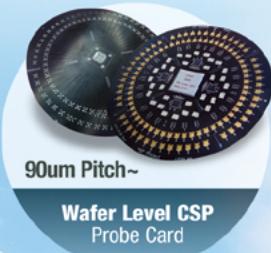
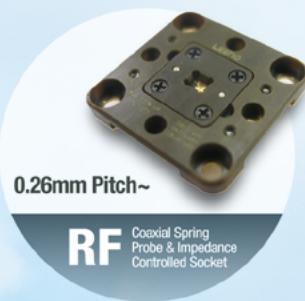


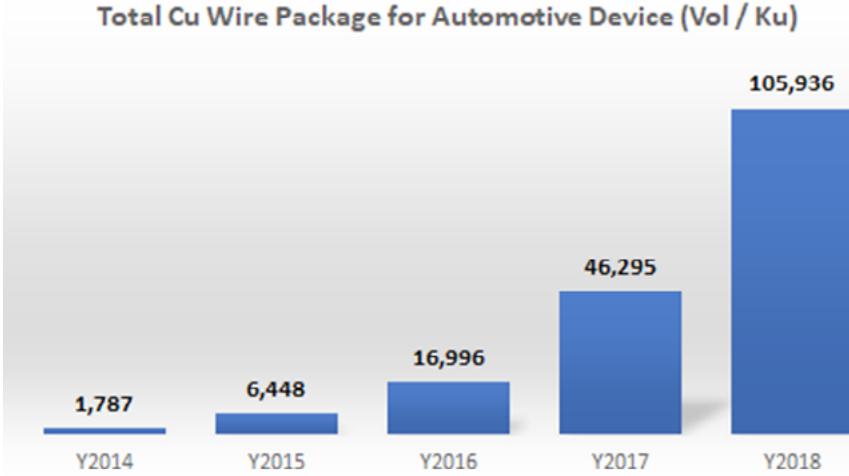
**Figure 6:** High-level automotive packaging roadmap showing increasing usage of advanced packaging technology.

ceramic-based packages, many of the other sensors, such as oil pressure or oil level sensors, require unique packaging solutions. The increased use of cameras in automotive applications is driving ceramic or unique

laminate-based CIS solutions, as well as wafer-level packaging (for infotainment). LIDARs are deemed essential for full autonomous vehicles. Many IDMs, as well as design houses, are working on solid-

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**Figure 7:** UTAC's historical shipment of package types with Cu wire interconnect technology for automotive application.

state LIDAR technology that requires a full-custom packaging solution utilizing advanced technology and materials.

Automotive packaging requirements also drive the development of higher performance materials, such as mold compound and die attach material for higher operating temperature under-the-hood and high-power applications. Cu-Clip is increasingly used as an interconnect technology for high-power and high-current applications as shown in **Figure 3** for power products. Cu wires have been widely adopted in standard automotive packages to reduce cost. **Figure 7** shows the growth of Cu wire in automotive applications for UTAC. The Cu wire shipment started in 2015 and since then, we have shipped over 163 billion units of QFN with Cu wire with no quality issues.

### Semiconductors in automotive warranty claims

According to a TechSearch International report on automotive

semiconductor packaging, about 4% of annual warranty cost for a car today is related to semiconductor products [3]. This is not surprising with the proliferation of semiconductor products in today's automobiles. Of that 4% of semiconductor-related failures, over 50% of the failures are related to assembly and final test. **Figure 8** shows the breakdown of the semiconductor failures. So, the pressure to continuously improve quality towards "zero defects" is acute everywhere in the automotive supply chain including OSATS.

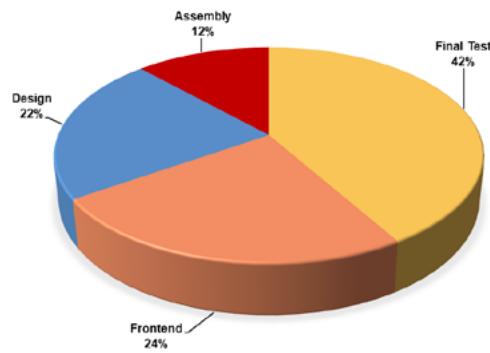
### OSAT assembly and test challenges

**Table 3** compares the differences between some of the key high-level requirements between automotive and consumer products. Some of the key differences that can have significant impact on business are long qualification times resulting in ~24-48 months to

start production. Automotive companies may require 15~20 years of supply guarantee with a similar time frame for all production-related data retention. Changes are typically not allowed with a long drawn out product change notification (PCN) approval process that can take up to 30 months. Then there is the drive towards "zero defects," which requires a certain higher quality standard and continuous improvement mindset by all levels within the OSAT organization.

The OSAT challenges for automotive assembly and test can perhaps be bucketed in five separate areas: a) Qualification and reliability, b) Release to manufacturing, c) High-volume manufacturing/operations, d) Logistics & resources, and e) Cost management.

**Qualification and reliability.** Packaging is an integral part of the quality of automotive semiconductor products. The best product development process requires IDMs to engage with OSATS early in the development phase to ensure the correct device-package interaction. This will require OSATS to run several sets of reliability tests as the IDMs tweak their device design or



**Figure 8:** Breakdown of warranty defects for semiconductor devices by manufacturing process [3].

fab process. Additionally, and especially for sensor devices, OSATS may have to run several sets of package design and material design of experiments (DOE) trials to fine-tune package-device interactions. This is especially true for MEMS sensors, for example. For new package and process development, advanced product quality planning (APQP) will need to be followed, which is essentially a phase-gate development methodology designed to adequately catch and address any issues as (or if)

**Table 3:** Key high-level differences between automotive and consumer semiconductor assembly and test businesses.

they develop during the development cycle. Additionally, design and process failure modes and effects analyses (FMEAs) are required to be established, addressed and updated throughout the development process.

AEC-Q100 specifications are used for automotive package qualification, which are more stringent than the standard qualification process for consumer products. **Table 4** summarizes some of the fundamental differences between typical consumer and automotive product qualification requirements. AEC-Q100 classifies automotive grade classification from zero to four in line with exposure to the operating temperature range. Grade Zero is considered the highest grade and requires the most stringent reliability testing. Every reliability test, as well as sample size and CpK for automotive products, requires higher standards. Two key reliability tests, temperature cycling (TC) and high-temperature storage (HTS) conditions for various automotive grade reliability testing are summarized in **Table 5**. Again, note that these tests show stringent automotive requirements. **Figure 9** shows examples of automotive grade product requirements depending on application and usage of the product. For example, powertrain modules operating under harsher conditions require either Grade 1 or 0, whereas components going into the dashboard inside the car require Grade 3.

**Release to production.** Once the automotive product is fully qualified, extensive documentation related to all aspects of the design and qualification of the product is required before starting mass production. The Automotive Industry Action Group (AIAG) has created this documentation process called production part approval process, or PPAP. PPAP is used to ensure that manufacturers and suppliers communicate and approve production designs and processes before and during volume manufacturing. The PPAP documentation is typically not required to be submitted by

Topic	Automotive	Consumer
Stress Condition / Operating Temperature Range	Grade 0: -40°C to 150°C Grade 1: -40°C to 125°C Grade 2: -40°C to 105°C Grade 3: -40°C to 85°C Grade 4: 0°C to 70°C	-40°C to 85°C
Test Hours / Cycle Time	>1000 hours/cycle → Test to failure	500 ~ 1000 hours/cycle
Electrical Test	Room, hot and cold temperature	Room temperature
Cpk	≥1.67	Meet datasheet spec
Unique Stress Tests to Automotive Qualification	1. Power Temperature Cycle 2. Bond Pull after Temperature Cycle 3. Early Life Failure Rate	None
Composition of Qualification Lots	3 non-consecutive wafer lots and 3 non-consecutive assembly lots for all qualification lots; 77 units / lot	Wafer fab technology qualification = 3 wafer lots and package qualification = 3 assembly lots; 30 units / lot

**Table 4:** Difference between automotive and consumer product qualification methods.  
SOURCE: TechSearch International



**Figure 9:** Examples of different grades of automotive semiconductor products based on application.  
SOURCE: TechSearch International

Package STRESS	ABV	TEST METHOD			Duration			
		Standard	Condition	Unit	Grade 3	Grade 2	Grade 1	Grade 0
Temperature Cycling	TC	AEC-Q100, JESD22-A104	-50 ~ +175C -50 ~ +150C	cycles	500	500	1000	2000
High Temperature Storage Life	HTSL	AEC-Q100, JESD22-A103	+175C +150C	hours	500	500	1000	2000

**Table 5:** Temperature cycle and high-temperature storage life reliability test conditions for automotive qualification. SOURCE: TechSearch International

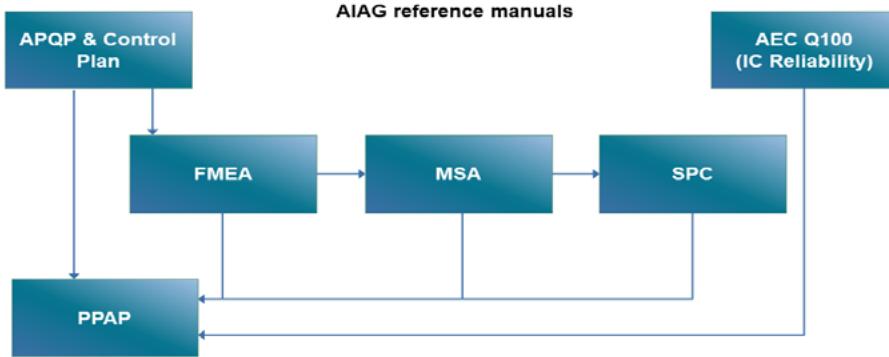
the OSATS, but is required by the IDMs to provide to the Tier 1 suppliers. Increasingly, however, the automotive players are requiring assembly and test data from OSATS. The data set can be extensive, so it is good to have a brief fundamental understanding of the PPAP process. The documentation requires the following and recording of certain

data throughout the package development and qualification process.

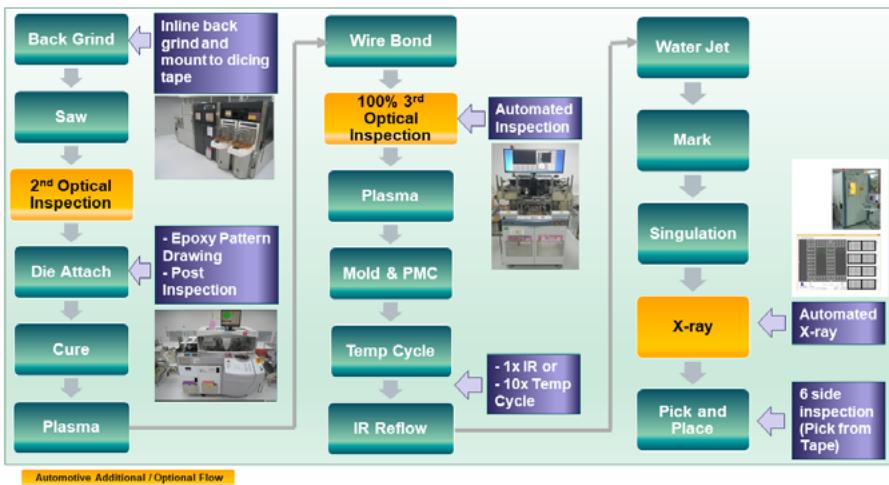
The complete automotive PPAP checklist is summarized in **Table 6** [4]. There are five different levels of PPAP documentation and data that need to be submitted during the various stages of the qualification and release processes. The key is to ensure that all items are documented, especially any changes in design or process. As mentioned in an earlier section, design and process FMEAs are required, which is not necessarily standard practice for OSATS

- Design records
- Engineering change document
- Design FMEA
- Process flow diagrams
- Process FMEA
- Control plan
- MSA
- Dimensional analysis
- Material performance reviews
- Initial process studies
- Qualified laboratory documentation
- ARR Master sample
- Checking aids
- Records of compliance
- PSW
- Sample product

**Table 6:** AIAG check-list for automotive PPAP process [4].



**Figure 10:** The link of all key aspects of automotive product development required by the PPAP process [4].



**Figure 11:** Comparison of automotive and standard (non-automotive) assembly process flows.

running non-automotive products. All these practices are geared towards developing a six-sigma process that targets higher quality products. The relevant documentation from these development processes becomes part of the PPAP documentation. **Figure 10** demonstrates the link among all the key aspects of automotive product development that is required for PPAP. Most OSATS today are not very familiar with the PPAP process as it relates to automotive assembly and test development. The key for OSATS is to work closely with the IDM to ensure a clear understanding of what is required from them for PPAP from the project get-go. Otherwise, OSATS can find themselves in a PPAP “nightmare” if the required documentation has not been prepared before going into mass production.

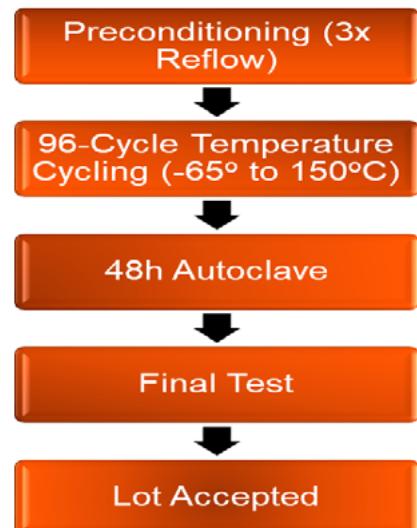
**High-volume manufacturing.** The assembly and test manufacturing flow is quite different between automotive and standard products as shown in **Figure 11**. Automotive flow requires additional process steps such as plasma cleaning, additional inspection steps, as well as tri-temperature testing. Once

in production, the operations team needs to stay vigilant to ensure quality throughout the lifetime of the assembly process. Operations will need to ensure that ALL process parameters finalized during the assembly and test qualification are locked and cannot be changed without permission. This will mean digitally locking out the possibility of accidentally changing any process parameters in each piece of manufacturing equipment. Beyond that, automotive customers ask for continuous improvement to drive the defect level down to zero. This typically requires a higher level of skill sets by the operators who run the automotive products. For example, we use specially certified operators to handle the automotive assembly and test process. Many automotive products also require going through a reliability monitoring program (RMP) to ensure that quality targets are met on a continuing basis. **Figure 12** shows a typical RMP flow. The RMP allows monitoring of the reliability of key wafer fab and assembly processes under accelerated conditions. Any failures are verified and analyzed, and failure analysis results are used to establish corrective

actions to eliminate the failure mechanism of future production lots.

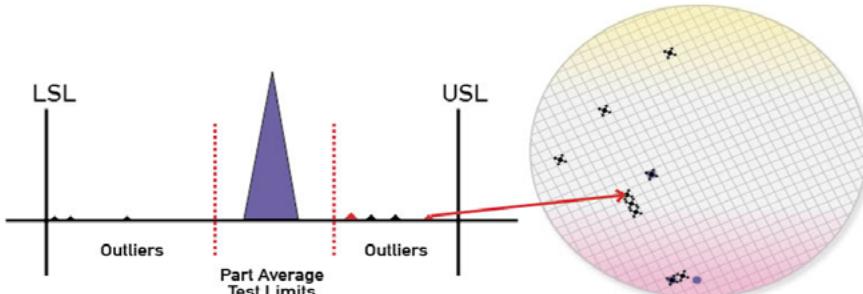
Wafer sort and final test for most automotive products require testing in three temperature conditions, room, cold (typically -40°C) and hot (typically 150°C). This requires special handlers that can drive capital expenditure. Additionally, many IDMs require part average testing (PAT) for wafer sort test to drive towards zero defects. The objective of PAT is to detect outliers within a wafer. PAT can capture every die in the wafer that falls outside the tighter sigma limit. **Figure 13** shows an example of the statistical bin limits of PAT testing for a wafer. Additionally, some automotive customers require burn-in testing (to eliminate early failures) service as well. The challenge here is incurring capital expenditures for burn-in infrastructure (ovens and boards). However, with the typical long-life span of automotive products, return on investment is typically a non-issue.

**Logistics and resources.** As already discussed and outlined in **Table 4**, automotive customers’ requirements are very different from traditional applications with which most OSATS are familiar. Because automotive lines require each equipment set to be qualified, it makes the planning process less flexible. OSATS are increasingly using a “designated” line approach as opposed to “dedicated” lines for running automotive products. The “designated” line approach qualifies multiple equipment sets for each process step to ensure loading flexibility for automotive products. OSATS need to ensure continuous quality vigilance through the “sort, set, shine, standardize, sustain (5S)” approach, agree to a long PCN approval



**Figure 12:** Lot acceptance reliability test for automotive products during high-volume manufacturing.

**Static PAT limits = $\mu \pm 6\sigma$**   
**LSL = Lower Spec Limit, USL = Upper Spec Limit**



**Figure 13:** The diagram shows how part average testing (PAT) detects outliers within a wafer.

process, and guarantee over ten years of continuous service and data retention. Additionally, any quality excursions require a diligent problem-solving approach such as the “8 disciplines” (8D), as well as disciplined failure-analysis methods such as fault tree analysis (FTA). Automotive customers require fast response times to any quality excursions. To ensure the level of support required for automotive product development and manufacturing, OSATS will need automotive trained resources in all key functions such as R&D, operations, supply chain, and of course, the quality group.

Finally, top automotive customers frequently demand more stringent warranty clauses in their service agreements. OSATS will need to carefully weigh the potential impact of such warranty claims if such situations arise.

**Cost management.** Finally, managing cost reduction in line with IDM and Tier 1 expectations poses a serious challenge. Some Tier 1s are expecting a 5% price reduction quarter-over-quarter, while a 5% year-over-year reduction is becoming quite common. The biggest challenge in cost reducing automotive products is that the customer does not allow any changes without a PCN, which can take anywhere between 18 to 30 months after qualifying the change (process or bill of materials [BOM]). For consumer and even industrial assembly and test applications, major cost reduction is achieved through process

simplification or consolidation, and/or using lower cost BOM while keeping the same quality. However, this is not possible for automotive products without the long qualification and PCN cycle. On the flip side, there are many instances where automotive customers want OSATS to introduce new process control steps (other than those originally agreed upon), which introduces additional costs. Yet, most of the IDMs and Tier 1s are unwilling to adjust the pricing accordingly. This makes the annual cost reduction even more difficult. Automation of some of the key process steps, such as visual inspections and x-ray, not only reduces cost, but also improves quality through the reduction of manual handling.

While it may sound like a cliché, the successful OSAT will need to ensure upfront due diligence on selection of the final process flow, BOM and detailed analysis of the financial models of each individual automotive request for quotations (RFQs). It can work to both parties’ advantage to agree on price reduction roadmaps and paths to achieve such cost reductions from the beginning of the RFQ process. Reviewing various “what if” scenarios for potential process flow and BOM changes during the qualification process, while understanding the price reduction roadmap and running the cost models accordingly, will provide insight and intelligence into the possible business outcome.

## Summary

Getting a slice of the automotive assembly and test business is not easy and comes with its share of challenges. It’s certainly challenging for OSATS with a different set of stringent requirements than standard assembly and test services they typically provide, which generates most of their revenue. The long qualification cycle and significantly longer time-to-revenue of automotive semiconductor products sometimes works as a deterrent for many OSATS to get into this market. The ones that are trying to penetrate today may find themselves years behind the competitors who have established themselves as an automotive grade supplier over many years. A lot of valuable engineering time and resources go into designing, qualifying and launching an automotive package. It may take up to four years to realize any material revenue from years of such hard work and effort. However, once qualified and designed into an automotive socket, the reward is a continuous steady stream of revenue that can last well over ten years. It certainly provides a nice cushion in an otherwise volatile industry.

## Acknowledgements

The author would like to thank Brandon Prior from Prismark, Jan Vardaman from TechSearch International, Carol Chiang from UTAC Singapore, Lee Smith from UTAC USA, and Somchai Nondhasitthichai from UTAC Thailand, for their contributions regarding certain data, tables and figures.

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## Biography

Asif Chowdhury is the SVP of Marketing and Corporate Business Development at UTAC Group, Singapore. He has over 25 years of experience in the semiconductor industry in various aspects of the semiconductor assembly and test business including package design and development, product/business line management, R&D and business development. Before joining UTAC, he held senior positions at Amkor Technology, Chandler, AZ, and Analog Devices, Wilmington, MA. He holds a BS in Mechanical Engineering from U. of Texas at Arlington, an MS in Mechanical Engineering from Southern Methodist U., and an MS in Finance and an MBA from Northeastern U. email [asif\\_chowdhury@utacgroup.com](mailto:asif_chowdhury@utacgroup.com)



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# Driving reliability in automotive electronics assembly materials

By Andy C. Mackie, Andreas Karch, Kay Parker, Erron Pender, Ricky McDonough [Indium Corporation]

The automotive electronics industry is advancing at a rate never seen before. The standard mass-produced passenger car has evolved over the past 100 years from a purely mechanical form of transportation to the “world’s most complex edge device” (Figure 1) [1]. It has been noted that a 2018 luxury car used over 100 million lines of code to run its operations [2]. Ensuring potential 24/7 functionality and long-term reliability has never been more challenging.

From a technology standpoint, electric-powered vehicles (EV) are already making significant inroads into the global market as we slowly move away from the standard internal combustion engine (ICE). Over the next 15 years, major cities could see individual car ownership giving way to mobility as a service (MaaS), potentially enabled by autonomous driving (AD) driverless cars using 5G wireless infrastructure. Advances toward true AD (so-called “level 5” cars) are already bearing fruit as level 2-4 advanced driver-assistance systems (ADAS), which enable the safer operation of standard human-operated vehicles, whether EV or ICE-powered.

Newer EV manufacturers are blurring the lines between a Tier I (traditional electronic subassembly supplier) and a semiconductor supplier, such as in the area of EV engine control technology [3]. This is a trend we can expect to continue as the need for increased functionality in smaller packages that drives heterogeneous integration ineluctably moves from digital into analog and power packaging, driven by the need for increased power density.

This technology evolution towards EV will also impact infrastructure, such as charging stations and the power grid. Since the beginning of 2018, European original equipment manufacturers (OEMs) have been pushing for mostly battery electric vehicles (BEV) in the

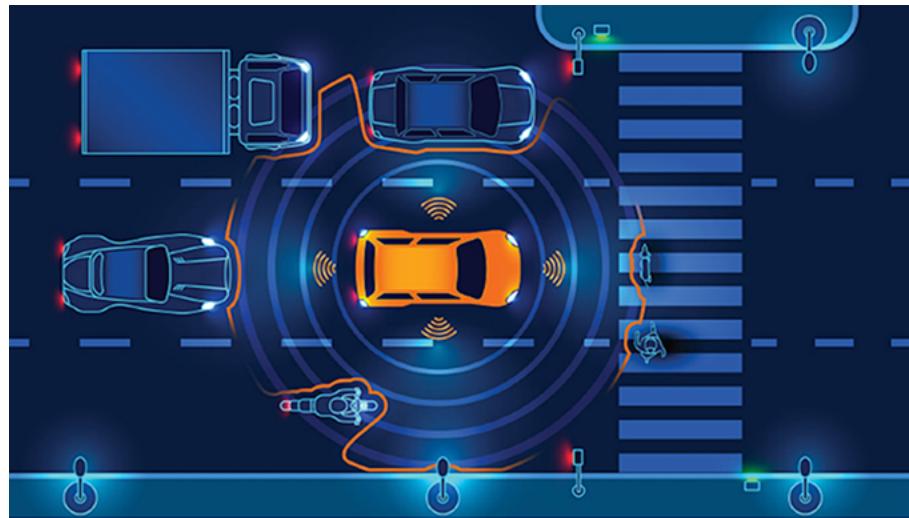


Figure 1: Car as edge device.

European market by 2025; however, it has been estimated that an overnight conversion of all passenger vehicles in the USA to electric power would require a 35% increase [4] in the total electric grid capacity to supply power for charging those vehicles. An estimated 350-500kW or more would be needed for the fastest charging stations; probably at 1,000V, with the last 10-20% of battery charging always proving the slowest [5].

## Evolution of mission profile

One of the key elements in defining the reliability of a vehicle, and of its systems and components, is its “mission profile.” This is the series of environments—such as temperature, humidity, vibration, dust, and salt-spray—and usage scenarios that a vehicle will be exposed to in a set period of time. A “100,000-mile/10-year” warranty is typical for a modern ICE vehicle. Mission profiles have a central role in reliability assessment as they take into account the key factors that affect systems both in the operating or non-operating modes.

One recent example for a future EV usage mission profile was given by Audi [6]:

- Driving (8,000 hours);
- Charging (30,000 hours); and
- Off-grid parking (92,000 hours).

This mission profile results in a total of 15 years of required working life for the car, and a 50% increase in lifetime warranties.

## Reliability by location in vehicle

The mission profile describes the automotive overall environment challenges, but each location in the car will see a different use case. The long-established Automotive Electronics Council (AEC) standard Q100 for integrated circuits covers several grades of device usage, from 0 (higher temperature exposure) down to grade 3 — equivalent to the mild temperature exposure of mobile devices. “In-cabin” electronics may be considered to be in a fairly benign environment (grade 3 or 2), except where the electronics are dashboard mounted, and hence, in an ICE car, exposed to more heat (grade 2 or 1). “Under the hood” for an ICE car obviously means being in a compartment with burning fuel, and

grade 0 is standard, with future grade 00 and 000 for higher temperatures on the horizon [7].

As gasoline usage declines, conditions can be expected to be more benign in the EV, but with notable exceptions. High local junction ( $T_j$ ) and ambient ( $T_a$ ) temperatures will be experienced on account of the flow of kiloAmps of current: most specifically, in the on-board battery charging system, and in the power control systems for the electric machines.

## Automotive batteries

The automotive battery for standard passenger vehicles is seeing a major change: from 12V to 48V, enabling higher power capacity for electronic start-stop systems without increasing current drain. There is also much discussion among OEMs of higher voltage batteries: 500V or even 1000V, but these will need special management due to safety issues.

The ultimate goal of speed-charging is to be able to charge the battery in as

much time as it takes to pump a tank of gasoline, and a large part of charging design is balancing power demand versus charging time. While fast charging is desirable, battery thermal management using highly conductive thermal interface materials (TIMs) and active fluid cooling is now commonplace.

## Reliability organizations and standards

The Joint Electron Device Engineering Council (JEDEC) remains the main source of standards and test methods for electronic systems for a variety of markets. The US-based Automotive Electronics Council (AEC) is an internationally-recognized organization that sets globally-applicable standards for semiconductor and device-packaging reliability in vehicles, and frequently references JEDEC test methods.

The AEC, as a standard-setting organization, has now been tasked by European OEMs and the Society of Automotive Engineers (SAE) to expand beyond its current remit of purely semiconductor and package reliability and move into board-level reliability (BLR), especially in light of expanding mission profiles. For example, the current IPC surface insulation (SIR) test [8] only calls for a minimum 76 hours of testing. Compare this with the expected working life of a vehicle and you can begin to see the perceived gulf between mission profile and materials testing for suitability.

## What does this mean for packaging and device assembly?

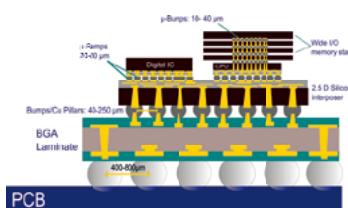
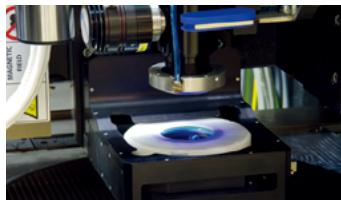
Moving from ICE to EV means that heat is no longer generated from burning gasoline; however, a high junction temperature ( $T_j$ ) in power die is induced by passage of high currents through a power control device. Ambient temperatures ( $T_a$ ) immediately adjacent to electric machine control components and the electric machines themselves will likely rise well above the current 150°C maximum used for grade 0 thermal cycle classification.

There is increasing adoption of components and assembly types from consumer applications into automotive. For example, most 77GHz radar packages are produced in the form of wafer-level packages [9]. OEMs and Tier 1s are now having to work out how to take the increasingly compact and complex packaging technologies designed for



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consumer applications, and make them suitable for reliable automotive usage.

Consider “Moore, more, more;” while Moore’s law is reaching its limit and packaging is enabling “more than Moore,” EV and ADAS/AD simply need more components. Two stark examples include:

- There are over 5x more capacitors used in EV than in ICE vehicles; and
- Adoption of a 100% reliability model for all automotive systems, based on the automotive safety standard ISO-26262, will mean increased software and system level redundancy, therefore, more identical components will be needed.

## Automotive technology and materials

New technologies are initially rolled out as value-added features in luxury cars where price is less of a concern and novelty is at a premium. Once any initial issues in higher volume manufacturing are addressed, and the costs of assembly have been understood and reduced, and any functionality or reliability issues have been addressed, then variations of these lower cost devices finally make their way into larger market and lower-cost vehicles. The proliferation of novel automotive electronics technology really begins at that point.

While change is continuous, there is also an innate engineering desire to maintain as many things as possible exactly the same. This presents a two-fold challenge to materials suppliers:

1. Ensure that “known good materials” remain useful for as many applications as possible. This can be accomplished by, for example, adapting to sizing (such as finer-pitch solder pastes), surface cleanliness (for printed wiring boards [PWB]), and higher purity (assembly materials), as well as meeting the higher SIR and zero electrochemical migration (ECM) needs of finer pitch devices.
2. Demonstrate that any new materials and associated assembly processes will result in packages and assemblies that are very likely to meet the reliability needs of the design vehicle.

## Examples of assembly materials usage in automotive electronics

The following sections present examples of assembly materials used in automotive electronics and challenges associated with their use.

### Current and developmental materials.

In this section, we discuss how we have been working to eliminate major issues in automotive packaging, device assembly, and board-level (PWB/surface mount technology [SMT]) assembly.

**Logic and memory: Flip-chip.** For larger, finer-pitch flip-chip die at around 60-80 microns and less, the cleaning process after assembly becomes much more problematic. Using the example of flip-chip ball grid array (BGA), not only does the cleaning process become more difficult as the die pitch shrinks, but die-substrate clearances are also decreasing. Warpage can be caused by either water jet impingement on the increasingly thin substrate and die, or induced by water absorption and desorption during wash/dry and reflow. Stress damage can be caused either to the die inner layer dielectric, to the under bump metallization (UBM), or even the flip-chip solder joint itself [10]. Increasingly, whether the flip-chip assembly process uses standard mass reflow, thermocompression bonding, or the emerging laser-assisted bonding flip-chip processes, assembly engineers are moving toward the usage of low and ultralow residue no-clean fluxes. These new flux types provide near-equivalent solderability and wetting in comparison with water-soluble fluxes, yet do not require cleaning as they do not block the flow of underfills. This is true even in copper pillar flip-chips down to 60 microns pitch or less. These fluxes also must have a strong bond to the underfill, even in the case of molded underfills, which are very sensitive to surface contamination.

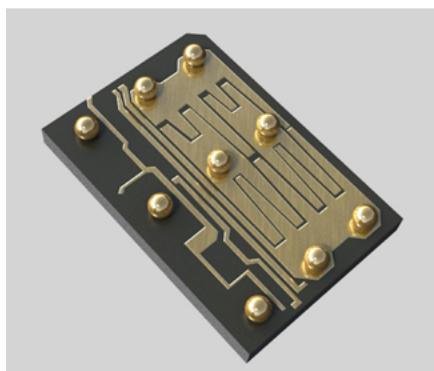


Figure 2: Package monolithic FCOL device.

Monolithic flip-chip on lead frame (FCOL) devices (Figure 2) are beginning to replace separate small modules, such as MOSFET/driver used as low voltage DC/DC inverters. In the FCOL assembly process, the lead frame itself is very thin and delicate, and in these package types, water-soluble fluxes are simply too difficult to use. The only solution is a low or ultralow (<10% by weight) residue no-clean flux.

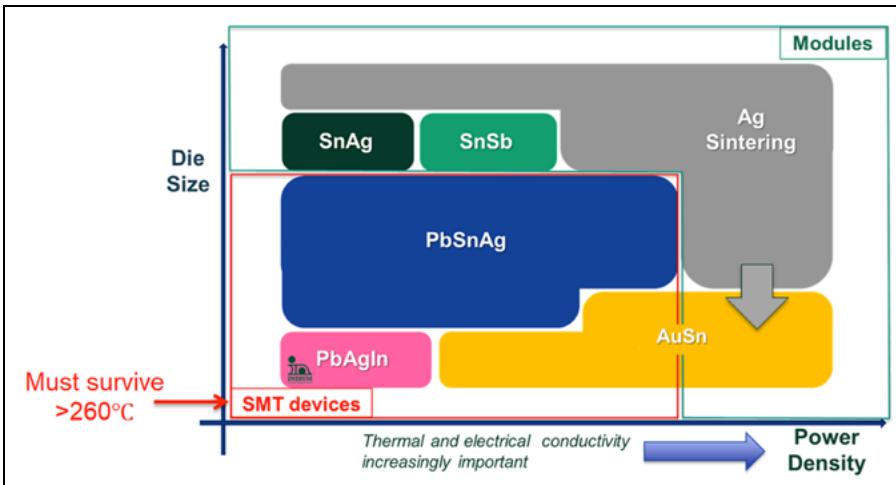
**Power devices: Die attach.** Die attach is significantly different from flip-chip attach. In the former, large amounts of current flow through the die in the z-axis, rather than from point to point on the die surface. Discrete analog/power devices fall under the Q101 standard. Those devices that are mounted to a circuit board using wave soldering can use a die attach material with a melting point between 230-260°C, so they are not directly heated in reflow, a die attach solder such as one of the SnSb family is often used. Figure 3 shows how materials are positioned for usage in the different power device types.

Devices designed to be SMT mounted, on the other hand, must survive reflow temperatures up to 260 or 265°C (discussed in IPC/JEDEC J-STD-020). Mostly Pb-(lead-) based solders are used in these die-mount applications on account of their known track record of reliability, especially on smaller, lead frame-based devices.

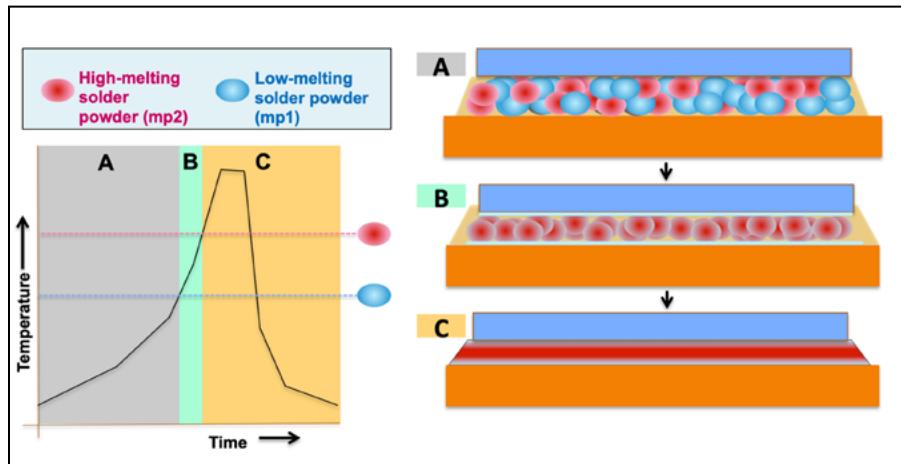
Clips are slowly replacing wire bonds as a means of forming a reliable, low RDS(on), connection to the die top (drain and sometimes gate) of the die. This has led to the increasing use of solder to finalize all the electrical interconnects. While flux residue contamination can cause wire bond failure at the ball bond/wire bond pad interface, an all-solder system allows for the possibility of a no-clean solder paste to be used inside lower- to medium-power voltage devices, with a molding-compound-compatible ultralow residue flux system such as SMQ®75 being used in high volume for these applications.

Although the European DA5 consortium is constantly working to eliminate lead from all analog/power packages, there is currently no easy replacement for these types of solder inside SMT-mounted packages. The now industry-standard and patented BiAgX® technology uses a mixed alloy system to create a final solder joint that melts at a temperature over the IPC/JEDEC J-STD-020 limit (Figure 4).

For large high-power density modules, compressed sintered silver preforms



**Figure 3:** 2019 state of play for die attach materials.



**Figure 4:** BiAgX® reflow mechanism.

are being used as die attach materials; however, coplanarity of both die/direct bonded copper (DBC) and DBC/heat spreader are major concerns. This, along with concerns about potential damage to thinned die caused by the use of high compression forces during fast pressurized sintering processes, means that damage can be caused by uneven application of pressure (a tooling process issue), small planarity variations in the sinter preform, or roughness in the pad metallization.

Because of the issues mentioned above, pressureless sintering is therefore much preferred, and sintering pastes are the only means of doing this. Indium Corporation's QuickSinter™ silver sinter pastes are capable of rapid print and dispense, and fast sinter without pressure. This material allows a near drop-in material to be used for smaller die and lead frame applications.

Our InFORMS® technology combines the known joint strength of solder with a

self-leveling matrix inside the preform, resulting in a highly coplanar joint, with the rigidity of a composite joint and the stability and strength of a solder joint. The InFORM has been used widely in baseplate-attach applications, but now is available in a form thin enough for use in direct die attach.

**Power modules and lidded die: TIMs.** In contrast with cheap thermal greases, solid compressible TIMs offer long lifetime, and reliable heat pathways. Compressible polymeric materials typically have a thermal conductivity of  $<10\text{W/mK}$ , while similar metallic TIMs, such as the HeatSpring®, can provide a conductivity  $>50\text{W/mK}$ . However, these materials do require pressure (typically  $>30\text{psi}$ ) to maintain good thermal contact between the backside of the heat spreader or lid with the heat sink.

**LED/optoelectronics: AuSn.** The recent release of Q102 provided a standard for optoelectronics, including light-emitting

diodes (LEDs). Smaller, lower-powered laser die and LED assemblies typically use a cascade of solder alloys with high-melting, good thermal conductivity AuSn being used for the initial die attach. While not suited to large die applications on account of its cost and high tensile strength, AuSn as either a eutectic (Au80Sn20) or off-eutectic solder (to allow for tin in the solderable surfaces) has found a niche in LED die attach.

While silver sintering may seem like a useful alternative, the usage of silver in automotive LEDs has been discouraged due to issues with both silver electrochemical migration and sulfur reactivity.

**MEMS: SMT-BiAgX®:** Materials used for structural lid attach in microelectromechanical systems (MEMS) devices have typically been dispensing solder pastes using SnSb alloys with melting (solidus) points just slightly higher than those of SAC solders. The recent publication of Q104 for MEMS and similar electromechanical devices now appears to necessitate that the melting point of lid-attach solder must be higher than 260°C, which is a design target for Indium Corporation's SMT-BiAgX®, designed to be reflowed at below 290°C (to minimize board-level reliability [BLR] issues), with a final joint that melts at over 260°C.

**PWB assembly.** Both electrical and thermomechanical reliability are highly important for so-called BLR, which covers surface mount and wave-soldered assemblies. Older style packages such as gull-wing, J-leaded, or BGA type include a large margin of compliance in the interconnect structure, so BLR has not been a major concern until fairly recently with the introduction of tiny passive devices such as 0201m capacitors, and finer-pitch camera modules and quad flat no-leads (QFN) and no-lead grid array (NGA) packages. These latter packages provide a "perfect storm" of reliability concerns:

- **Thermal:** The die inside shrinking packages usually have a much higher current density (amps/unit area). The ability to remove heat from the die (usually through a package-bottom thermal escape pad) is important. Any voiding here can lead to build up of heat within the package, and early device failure. Low voiding means high, consistent thermal conductivity across the die bottom and in both the die attach and board-level attach, is therefore

increasingly critical. In the case of solder paste-based board-level attach, this is exacerbated by the low BLT (**Figure 5**).

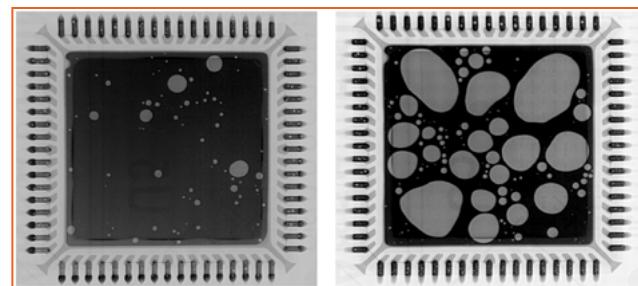
- **Electrical:** As no-clean solder pastes become increasingly important, current leakage between adjacent conductors must be kept very low, even with these large, fine-pitch low clearance QFNs. The entrapment of residue under large devices provides an opportunity for solvent from the solder paste flux to be trapped as it will volatilize much more slowly (**Figure 6**). A flux vehicle that can provide high SIR and prevent electrochemical migration (ECM), even when trapped under a flat surface such as in a glass slide on FR4 ECM test, can be highly effective (**Figure 7**).
- **Signal frequency:** Higher frequency devices will also necessitate minimal packaging signal losses, and hence, straighter signal pathways, such as is seen in wafer-level packaging for radar devices. It will also increase the need for ultralow residue fluxes and solder pastes to minimize dielectric losses.
- **Mechanical:** The small coefficient of thermal expansion (CTE) mismatch between the PWB substrate and the QFN means that thermal cycling stresses are small; however, because the QFN effectively has a bond line thickness (reflowed SMT solder height) of only 10-20 microns, shear stresses from both thermal and shock are significantly exacerbated. High-strength antimony-containing alloys are seeing increasing usage for higher temperature (grade 0 and beyond) SMT applications.
- **Warpage:** As we have seen in previous discussions, low-temperature solders using either bismuth- or indium-based solder alloys are being used in assembly applications where either the finished package includes materials or components that cannot survive high-temperature thermal excursions, or where heat-induced warpage of large components, such as logic FCBGA devices gives rise to head-in-pillow (HIP) defects.

## Summary

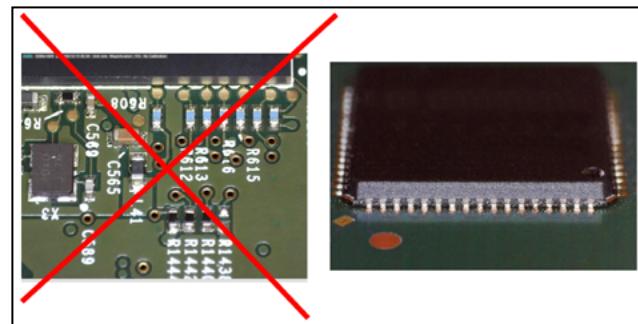
As the very nature of personal transportation, car ownership, automotive functionality, and reliability change simultaneously, OEMs and their Tier I and II suppliers are putting increasing demands on component and materials suppliers to show zero defects and 100% reliability. This trend is driven by the demands of increased vehicle life, zero defects, and perfect safety. Indium Corporation's materials development strategy, our long-term membership in the AEC, and our solder paste manufacturing site IATF 16949:2016 certifications are an indication of our strong commitment to partnering with our automotive customers for the supply of innovative and reliable semiconductor and board assembly products now, and into the future.

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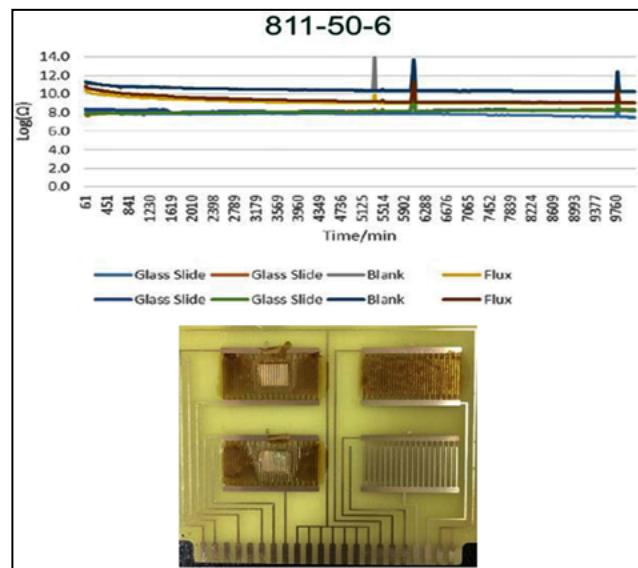
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**Figure 5:** Good and bad voiding under a QFN package.



**Figure 6:** High SIR no-clean fluxes are increasingly needed.



**Figure 7:** Large QFN components need high resistance between I/Os.



## Biographies

Andy C. Mackie is a Senior Product Manager, Semiconductor and Advanced Assembly Materials at Indium Corporation, Clinton, NY. He is an electronics industry expert in physical chemistry, surface chemistry, rheology, and semiconductor assembly materials and processes. He has more than 20 years of experience in new product and process development, and materials marketing in all areas of electronics manufacturing, from wafer fabrication to semiconductor packaging and electronics assembly. He has a Doctorate in Physical Chemistry from the U. of Nottingham, U.K., and a Master's degree in Colloid and Interface Science from the U. of Bristol, U.K. He is also formally trained in Six Sigma – Design of Experiments; email amackie@indium.com

Andreas Karch is a Regional Technical Manager for Germany, Austria, and Switzerland at Indium Corporation, Germany. He has more than 20 years of automotive industry experience, including the advanced development of customized electronics. Karch is an ECQA-certified integrated design engineer, has a Six Sigma Yellow Belt, and was selected by the Austrian Patent Office as one of the 2014 recipients of the Top 10 Inventum Awards for an automotive LED assembly.

Kay Parker is a Technical Support Engineer at Indium Corporation, Clinton, NY. She earned a Bachelor's degree in Applied Mathematics with a minor in Engineering Science. Her past accomplishments include managing the details of a National Science Foundation grant, forming and leading an award-winning competitive student robotics club, developing industrial manufacturing process technologies, and modeling the flow of blood in the human eye using mathematical equations and computer programs.

Erron Pender is a Technical Support Technician at Indium Corporation, Clinton, NY. He has experience in light manufacturing; assembly, testing and quality control of infrared thermal imaging systems for military and civilian applications; and customer design and fabrication of dental implant components using various dental alloys, including titanium, chromium, palladium, and gold.

Ricky McDonough is a Product Specialist at Indium Corporation, Clinton, NY. He earned his Bachelor's degree in Chemistry from West Virginia U., where he completed his thesis on Effective Methods of Hydrogen Storage in Hydrogen Fuel Cells. Ricky also earned a Master's degree in Physical Chemistry from Syracuse U. where he studied microorganisms using analytical techniques.

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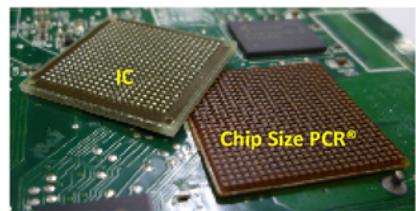
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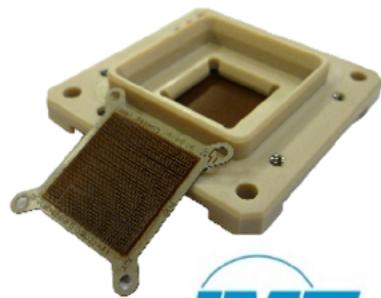
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# Effective screening of automotive SoCs by combining burn-in and system-level test

By P. Bernardi, D. Calabrese, M. Restifo, F. Almeida, M. Sonza Reorda [*Politecnico di Torino*] and D. Appello, G. Pollaccia, V. Tancorre, R. Uglioli, G. Zoppi [*STMicroelectronics Srl*]

This paper describes the benefits and the money savings by combining the system-level test (SLT) and burn-in (BI) steps for automotive system-on-chip (SoC) devices. Moreover, the paper suggests the requirements to merge SLT and BI. In this way, SLT can detect faults that can be excited only functionally, for example in the logic of power-on self-test. Moreover, BI brings the device under test (DUT) in the worst possible condition by means of the climatic chamber. This allows one to check the correctness of the DUT's behavior (using the SLT) under the worst condition compared to the application condition (by means of BI). In addition, the SLT equipment can control the design for testability (DfT) structure of the DUT. In this perspective, the goal is to reduce the tests performed by the final test (FT) automatic test equipment (ATE), thereby reducing test time and cost. The proposed approach is affordable only with the BI time reduction with high-voltage, which is described in [1].

## Background

This section provides the reader with the required information about system-level test and burn-in flow.

**System-level test.** SLT often complements the other steps of a test flow, which include wafer sort, BI, and FT, using functional test. The functional test complements the structural test because it covers some defects that structural testing does not detect. For example, the functional test works at the system operational speed, while some DfT techniques do not. Moreover, SLT exercises the system exactly in the same conditions as the operational phase [2].

SLT is sometimes used as an effective method to lower the defectivity, often measured in terms of defective parts per million (DPPM). SLT increases the quality of the shipped products, which is crucial for safety-critical applications. SLT addresses

both defects and marginalities [3]. In our view, a possible defect (physical) is always present, and test conditions may only change the set of visible symptoms. Conversely, a marginality (behavioral) may not be present in a subset of possible test conditions, and may impact the functionality under specific process, voltage, and temperature (PVT) condition(s), only. A marginality might also be active only after a specific functional sequence (including software) is applied. Detection of marginalities have always been delegated to bench-top validation, under the assumption that a reduced number of corner cases are enough to view the symptoms of all marginalities.

Moreover, the inherent limits of optical lithography and process variation control in deep-nanometer manufacturing are creating more subtle defect types that cause failures only under certain system operating (voltage, temperature) conditions and workloads [4]. Production test running on ATE is unlikely to cover all failing conditions to expose such so-called marginal defects. Even though area scaling continues, the end of Dennard voltage scaling has brought power and thermal reductions to the forefront as the key design challenges in the era of mobile computing. Complex power management schemes orchestrated by energy-aware scheduling software are now the norm in multi-core system-on-chip (SoC) devices. With shrinking voltage margins, supply grid noise and activity-dependent local aging can push weak devices below safe operating thresholds and trigger failures [5].

In the following, we report a list of cases (from the literature) that are addressed by functional test and not by the structural test:

1. Complex clock and power domain interactions controlled by embedded software [6].
2. Functional interactions as the operating system boots [6].
3. Under certain application scenarios where memory is accessed at a high

rate, read/write soft data errors can occur, on account of local workload-dependent aging or activity-induced supply droop and cross-talk [7].

4. Complex protocols are increasingly being implemented in hardware. These protocols cannot be tested in isolation by structural test [8], e.g., a bus at its maximum bandwidth.
5. Hardware resource management, such as dynamic system re-configuration [8].
6. Exercising central processing units (CPUs) with extreme work loads, stress architectural specific operations such as multithread, floating-point units, maximum concurrent operations on multiple threads and cores, TLB hit/miss, caches and its tag-RAM, pipeline exerciser [8].

Some further defects are targeted by the SLT solution, which are specific to new automotive devices, e.g., to consider the environment in which they are expected to work [9].

**Burn-in flow.** The main purpose of BI is activating those latent defects not observable during wafer sort and package test activities at time zero. During BI, we increase temperature to reach a possibly stable and high value with respect to the maximum allowed junction temperature of the device. Supply voltage is elevated to complete the stress concept. In previous works [10-13] we discussed advances regarding BI. We aimed to maximize the quality of stress and reduce the cost for optimizing this stage by interleaving the stress phases with the test.

Because of its relatively long test duration, system-level test represents a cost challenge if purely considered as an additive stage to existing test flows. BI or test during burn-in (TDBI) stages permit a relatively cost efficient solution to manage very long test times. However, there are several technical obstacles that complicate the merging of these two methods. The rest of the paper analyzes these obstacles and proposes some

solutions, as well as presents a cost analysis of alternative configurations.

Considering the case of a SoC, it is assumed that a DUT is composed of at least a CPU, random access memory (RAM), embedded nonvolatile memory (eNVM), and some peripherals. **Figure 1** shows the common phases of the BI process of an automotive SoC. The typical phases that constitute the BI process of a SoC are the following [11-12]:

- Data Flash modules cycling, which is oriented to perform a predetermined number of eNVM erases.
- Dynamic burn-in, which aims at maximizing the stress of the device and is divided into sub-phases:
  - ATPG generated patterns, applied through scan chains.
  - Functional tests: often derived from functional patterns devised for verification and test, these programs trigger a high activity with an execution of loop statements [13].
  - Logic and memory BISTS.
  - Write/read cycles of the memory using appropriate patterns, such as checkerboard.
- Other IP-specific stresses and tests.

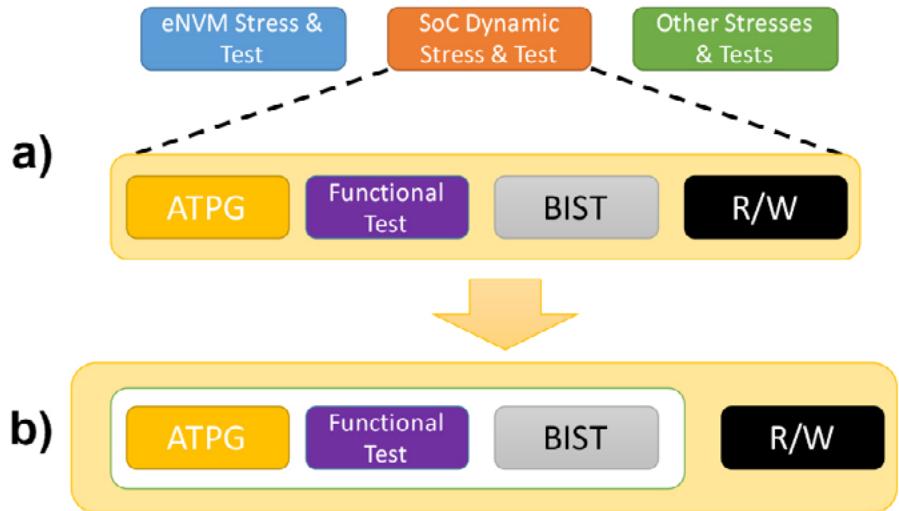
## Proposed approach

The approach proposed in this paper aims at providing a solution to rearrange the test flow merging BI and SLT in a single step. In addition, in the proposed approach we can access the DfT structures using the JTAG interface.

The main goal of the combination of BI and SLT in a single step is the reduction of test cost. The test cost reduction is driven by:

- Merging BI and SLT allows avoidance of the load and unload phases, which are done semi-manually. These semi-manual phases require extra time, which drastically impacts the test cost.
- The test cost in the time unit of the proposed method is lower than the sum of the two costs in the time unit.
- The possibility to use a high-voltage technique introduced by [1] reducing drastically the required burn-in time to guarantee a defect part per million.

The next sections describe how to insert an instance of SLT inside the BI,



**Figure 1:** a) Common burn-in test flow for automotive MCUs; b) System-level test insertion inside the burn-in test process.

the hardware required inside the BIBs to enable the SLT, and two protocols to activate the functional test of SLT and to perform an ATPG phase of the dynamic BI.

**Merging system-level test inside burn-in.** The main purpose of this sub-section is to describe how to run an instance of SLT inside the BI step. SLT inside the BI step can run any kind of functional program—both functional programs aiming at increasing the stress under BI and functional programs aiming at testing the correct system-level behavior of the DUT.

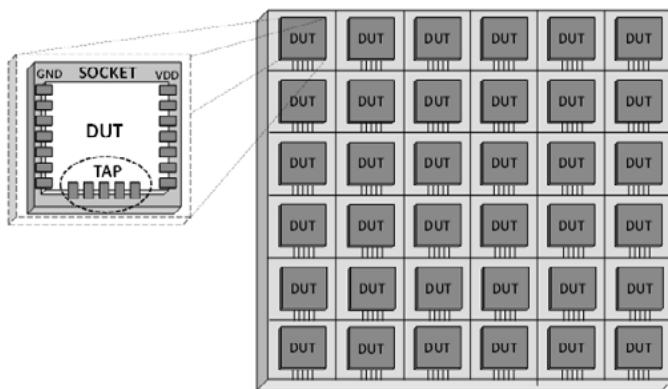
The additional SLT step inside the BI can command the test access port (TAP) by means of the JTAG interface. The access to the TAP controller gives the possibility to access possible built-in self-test (BIST) structures inside the DUT.

**Figure 1b** shows how to merge the SLT within the BI inside the dynamic burn-in from the BI flow point of view. The insertion of an SLT step is possible inside the dynamic burn-in phase. Its insertion allows the triggering of the following sub-phases of the dynamic burn-in:

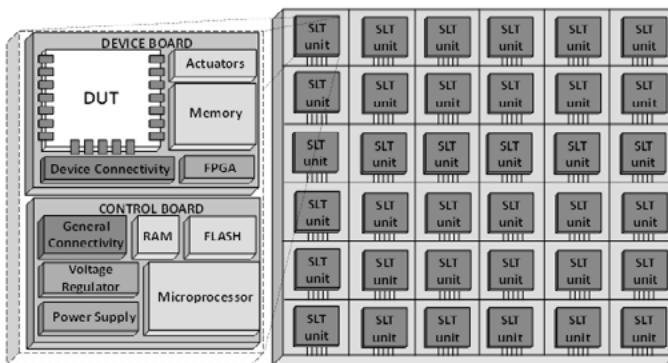
1. The application of stimuli based on automatic test pattern generation (ATPG), which configures all the scan chains of the DUT into a single scan chain. This configuration is called the “burn-in scan chain” configuration. The tester accesses the resulting burn-in scan chain and performs a toggling activity. This phase uniformly stresses the DUT.
2. During the functional test run, when the tester loads the functional test program into the eNVM memory of the SoC, it triggers the execution of the program and downloads the results of the functional test program. The program can correspond to a procedure for stressing the DUT, like the common functional test phase of the dynamic burn-in, or a procedure for testing the device at the system level performed by the SLT.
3. During the BIST phase, the tester accesses the instruction register of the TAP controller via the JTAG interface, activates the protocol for launching the logic/memory BISTS, and downloads the results of the BIST.

**Augmented burn-in board.** The insertion of the SLT inside the BI flow requires changing the structure of the BI boards, because SLT needs additional logic for enabling and testing the system features.

**Figure 2** shows the structure of a common BIB. A BIB has two main characteristics. The first is a high number of sockets, which allows a high parallelism inside the climatic chamber. The second is the routing of the power signals and JTAG signals, which permits the tester to interact with all the DUTs at the same time using the TAP controller. A BI tester can execute all the steps of BI using the described BIB architecture. However, the tester must have a bandwidth large enough to command all DUTs and sample the DUT



**Figure 2:** Structure of a common burn-in board.



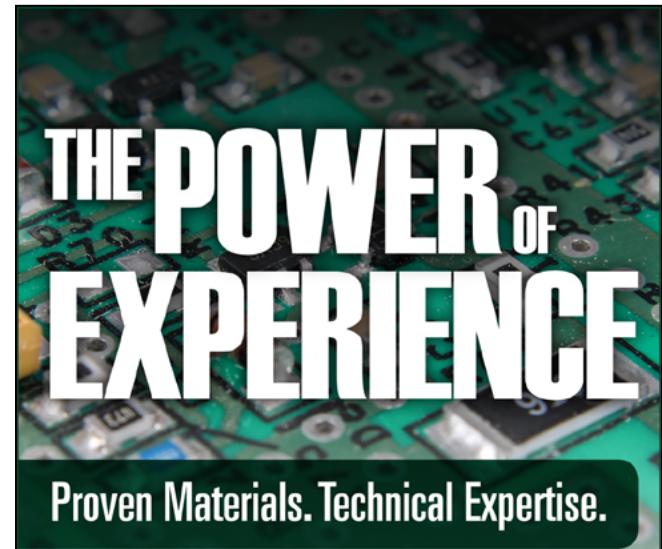
**Figure 3:** Structure of a new burn-in board to enable SLT.

responses at the same time. Common BIBs have a limited number of resources, so it is necessary to change the architecture of the BIB to enable SLT.

The proposed test flow moves the total control from a central ATE to a workstation (as a simple host PC), which orchestrates the smart and improved BIBs. **Figure 3** depicts the new architecture of the BIB, which maintains the same parallelism of the common SLT. In this case, the parallelism is no more on the DUTs, but it is on SLT units.

A SLT unit is composed of two different boards:

1. A controller board, which interacts with the BI tester and transforms the high-level commands into low-level instructions and values to be applied to the DUT. The controller board is also in charge of receiving the output values produced by the DUT, analyzing them and conveying the results of the test to the BI tester. The control board is equipped with a variety of components. A microprocessor manages all the SLT steps, and an eNVM and RAM module support the microprocessor. The general connectivity module implements all the possible communication interfaces such as I2C, serial peripheral interface (SPI), Ethernet, controller area network (CAN), etc. Moreover, the voltage regulator and the power supply enable a telemetry feature allowing a fine-grain tune of the supply voltage to the DUT.
2. A device board, which includes the socket where the DUT is loaded and all the other IPs required for an efficient and exhaustive SLT. The device board directly hosts and interacts with the DUT using additional interfaces. Hence, the device board is equipped with the required number of interfaces



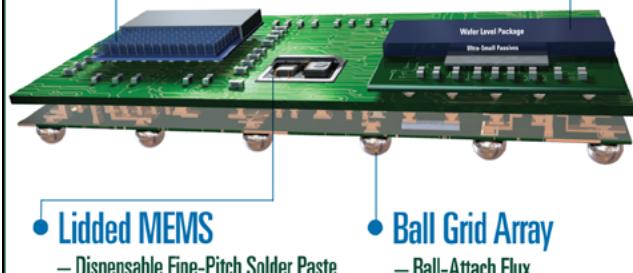
## Soldering Materials to Enable Heterogeneous Integration

### 3D Logic / Memory and Flip-Chip

- Wafer Bumping (Bump Fusion) Flux
- Flip-Chip Flux

### System-in-Package

- Wafer Level Ball-Attach Flux
- Ultrafine-Pitch Solder Paste



### Lidded MEMS

- Dispensable Fine-Pitch Solder Paste

### Ball Grid Array

- Ball-Attach Flux

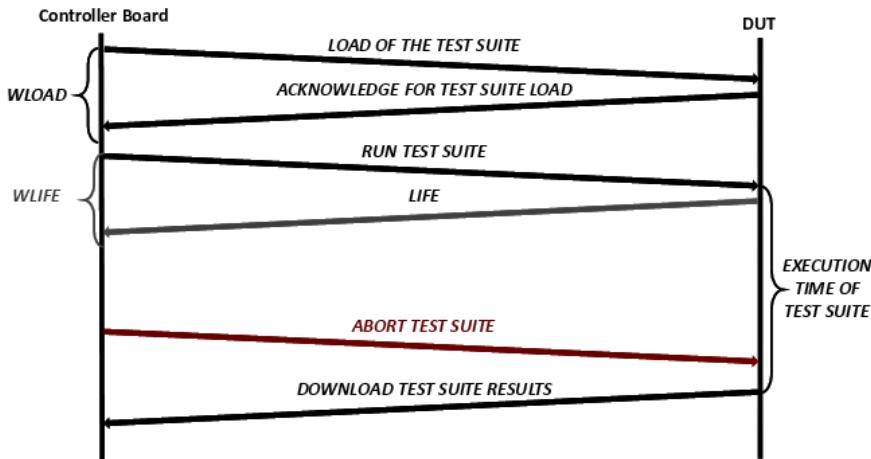
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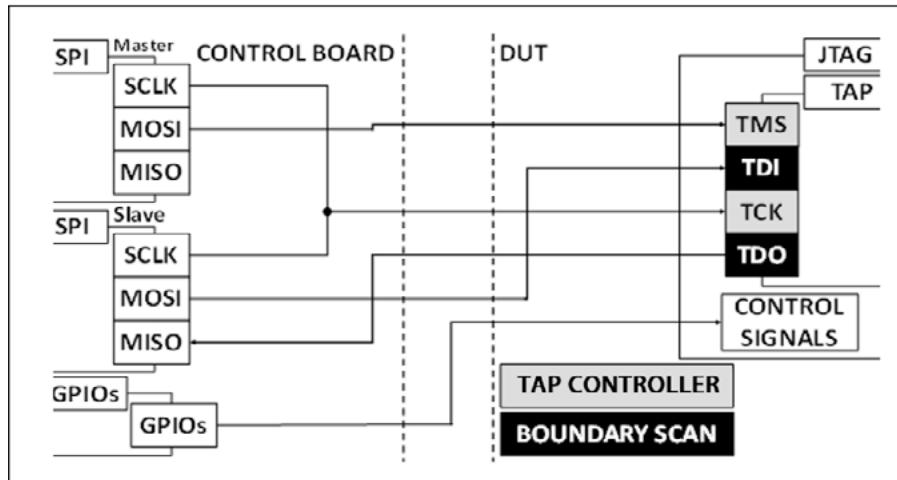
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**Figure 4:** Protocol for enabling a functional test suite in an SLT environment.



**Figure 5:** Protocol for enabling a structural test inside an SLT environment.

that are necessary for testing the device connectivity. Moreover, the device board is equipped with internet protocols (IPs), which are necessary to functionally use the system to be tested. Some memory may be required to store the low-level stimuli to be applied to the DUT, and the values to be compared with those it produces and to support the DUT boot. Finally, a field-programmable gate array (FPGA) device may sometimes be present to act as a programmable switch-matrix interfacing the DUT data channels with those of the controller board.

The device board is specific to the DUT product that is currently being tested, while the controller board is designed to be highly versatile so as to be compliant with a broader range of products. The device board

is mounted on top of the control board. The control board is fixed for all the DUTs and reusable, while the device board changes when testing a different DUT family. Typically, the device board and control board are stacked one over the other.

**Protocol for enabling functional tests.** The BIB architecture requires a special purpose protocol for triggering a functional test suite and the access to the TAP controller. The proposed protocols enable the ATPG, the functional test, the BIST phase used in the common dynamic BI, and the functional test used for SLT.

**Figure 4** shows the test protocol implemented for running a functional test suite in the SLT environment. First, the controller board loads the test suite inside the memory of the DUT. Then, the controller board initializes a watchdog timer “WLOAD” for monitoring the correct load of the test suite. If the DUT replies

to the control board with an acknowledge message, the loading process ends with success. If the watchdog timer WLOAD expires, the control board turns off the power supply of the DUT, thereby moving the system to a safe state.

After the test suite loading, the control board triggers the execution of the test suite. Then, the control boards initialize a watchdog timer “WLIFE” for checking if the device is still alive. If the device replies with a life message, the watchdog timer restarts. If the watchdog timer WLIFE expires, it means that the DUT is not behaving correctly, the control board aborts the test suite and restarts the test suite. If the DUT continues not to behave as expected after the reset, the control board turns off the power supply moving the system to a safe state. Finally, if the DUT executes the test suite correctly, the control boards download the test suite results.

The interface for implementing the protocols can be implemented with a software command interface, which is built upon UART. This interface is usually present on all SoCs and allows attainment of the necessary speed for the actual desired purpose. It is also possible to transfer data in parallel with the CPU activity. An additional feature, a real-time kernel operating system, provides independent threads useful for real-time applications and, therefore, it is necessary to test their responses.

#### Protocol for enabling structural tests.

The proposed BIB also allows running a structural test using the JTAG interface of the DUT. This section describes a protocol that enables the TAP interface by means of interfaces equipping the control board.

The control board uses at least two SPI interfaces (a master SPI, which controls a slave SPI, plus the JTAG) and some general purpose input/output (GPIOs) inside its general connectivity module for establishing a communication with the TAP interface through the JTAG connector. **Figure 5** shows details about the connection between the control board and the DUT.

Managing a TAP controller requires commanding at least the TMS and TCK signals (TRST is optional). The TMS signal is connected to the MOSI signal of the first SPI, while TCK is in short circuit with the SCLK signals of both SPIs. This configuration permits the evolution of the state inside the finite state machine (FSM) implemented by the TAP controller. Managing a boundary scan

needs to also control TDI and TDO. TDI is connected to the MOSI of the second SPI, while TDO is connected to the MISO of the first SPI. The JTAG interface can require an additional signal, for example an asynchronous reset, which is called JCOM. These kinds of signals can be controlled using common GPIOs.

This is the minimal protocol for accessing a standard TAP. The protocol controls the state inside the TAP controller, loads instructions inside the TAP register, downloads results of TAP instructions and uses the DUT scan chain. If the structural test requires additional signals, the protocol can be enhanced with further SPI interfaces.

### Experimental results

The proposed approach has been used for testing a SoC, which is based on a 40nm CMOS technology microcontroller by STMicroelectronics, which serves automotive applications. The DUT is safety-compliant with the ISO-26262 [14] up to ASIL-D applications. Inside the DUT there is a microcontroller with embedded non-volatile memory (i.e., a MCU).

This product undergoes severe test requirements to reach very low DPPM figures. Especially beginning with the 40nm node, these devices reached a relatively high complexity. The complexity depends on a combination of factors, including the relatively large number of integrated IPs and the possibility of IP reconfiguration offered by the non-volatile memory. The widest possible verification of configurations is a main goal for the applicative test. To implement this objective, we defined an applicative setup with the minimum possible set of components, for the obvious objective of minimizing the board space occupation. Space occupation is a key parameter determinant in the cost of test because it directly influences the test parallelism for a given board space.

The additional key factors driving test costs are typically the test duration, the number of stages (e.g., a stage requires the DUT to be handled and put in a socket for the test), the parallelism, the throughput ratio, and the cost of the equipment. In our analysis we did not consider other factors, which are independent from our project scope, such as the efficiency and the electrical yield.

**Table 1** gives some figures used to compute the test costs per device without the proposed methodology, i.e., with a solution where BI and SLT are applied independently (BI+SLT).

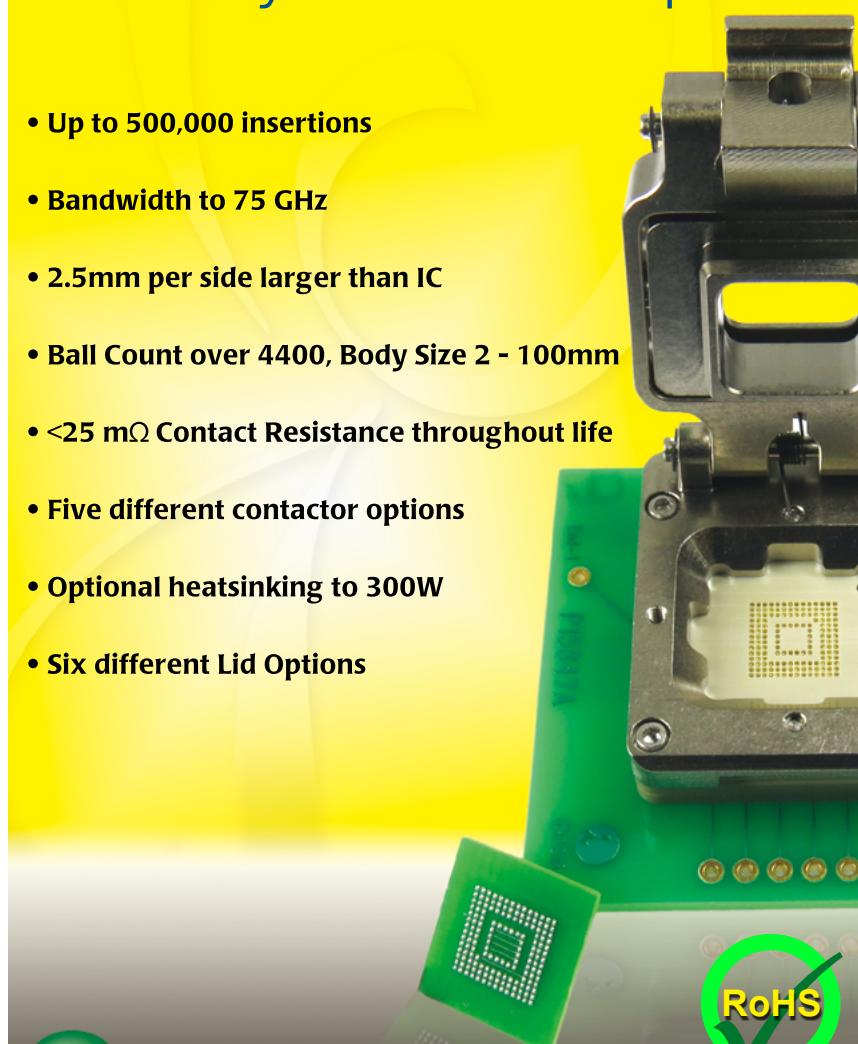
Traditional burn-in operations, usually characterized by off-line automation, give better cost efficiency with relatively longer durations. In this case, to load devices to the sockets on the board, an equipment is shared between multiple burn-in testers,

named automated loader/unloader (ALU). The board movement from the ALU to the BI tester may happen either manually or by robots depending on the level of the automation. These off-line operations add an overhead time to the electrical burn-in time and an extra cost.

**Table 2** presents the test costs per device per minute with the proposed approach. This methodology will be referenced as BI&SLT. Our analysis does

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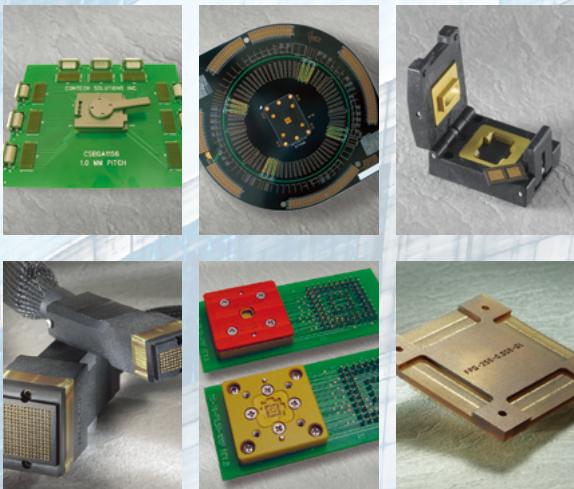
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# of stages	2	
Stage	Burn-In	SLT
Equipment cost [arbitrary unit]	500,000	500,000
Board Parallelism	100	64
Batch Size <sup>a</sup>	4,800	1,280
Additional costs	120 min of Load/Unload devices	None
Equipment depreciation period (EDP)	6 Years	6 Years
Test Cost per device per min [arbitrary unit/minutes]	0.0000330	0.0001239

<sup>a</sup> A batch is the number of DUTs which are simultaneously tested by the equipment

**Table 1:** Test costs per device without the proposed methodology.

# of stages	1
Stage	Burn-In & SLT
Equipment cost [arbitrary unit]	100,0000
Board Parallelism	64
batch Size <sup>a</sup>	1,280
Additional costs	None
Equipment depreciation period	6 Years
Test Cost per device [arbitrary unit/minutes]	0.0002477

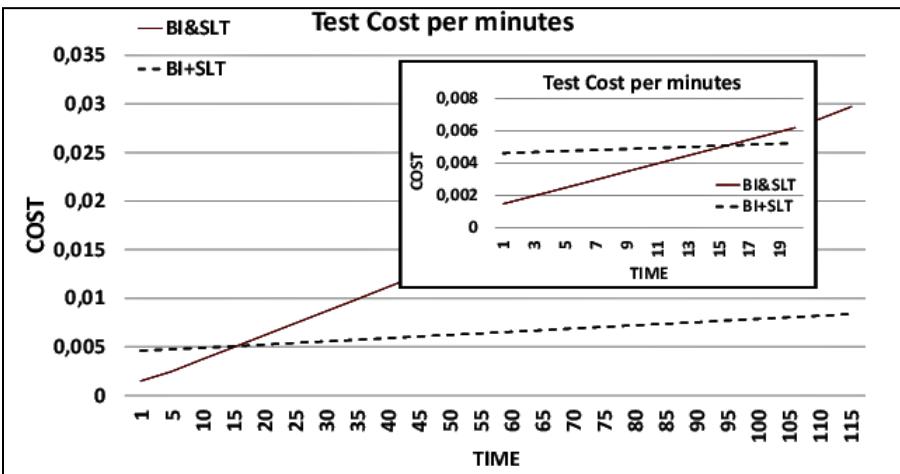
**Table 2:** Test costs per device with the proposed methodology. For footnote a, refer to Table 1.

not account for the utilization efficiency, which we considered the same for each equipment. Our work aims at enabling the technical conditions to maintain the best possible cost effectiveness of the test flow during its entire lifecycle. In the early phases, with relatively high defectivity and consequent long time for the screening of early-life fails, the adoption of a flow with both BI&SLT is economically affordable. In these phases, you should also expect relatively low manufacturing volumes. **Figure 6** shows that a cost tradeoff exists between the BI&SLT and BI+SLT approaches depending on the BI time. It is possible to combine BI and SLT duration such that the possibility of combining them together becomes economically convenient.

In **Figure 6** the time axis represents the effective burn-in time without the additional time for load/unload operations. Conversely, the time for the BI+SLT approach accounts also for the extra time for the load/unload operations, because it is required intrinsically by the approach, while the time for the BI&SLT methodology is only the BI time.

The proposed strategy becomes even more convenient when exploiting the high-voltage stress for exponentially reducing the BI time, as described in [1]. Using high voltages in BI reduces dramatically the DPPM even with a short BI time duration.

The proposed flow has its maximum saving when the BI time is lower than 10-12min. In addition, it is also important to remark on the existence of mechanical effects at each stage. Each time parts are handled, there is the probability of a mechanical damage to leads/balls and/or to the package body. The reduction in the number of stages,



**Figure 6:** Trade-off between BI&SLT and BI+SLT approaches.

therefore, benefits the final mechanical yield, which in our experience, may account for a fraction of a percent. This apparent small number is instead very relevant with the economy of scale and a function of the device bill of material (BOM) cost.

## Summary

This paper introduces and illustrates a new approach for combining the BI and SLT steps, which are today commonly used when dealing with ICs used in safety-critical applications. Possible scenarios for a stress parallelization are analyzed and investigated. The approach guarantees complete parallelization of the two test steps exploiting a new architecture that mixes the benefits of both BI and SLT, thereby implementing a better screening while reducing the whole cost.

The solution is oriented to devices with a low-power consumption like the MCU test case which is controlled in temperature by passive systems. There is also the possibility for reducing the cost of the following final test tasks to the

adoption of the proposed approach. This topic will be investigated in future works.

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## Biographies

Paolo Bernardi (MS'02 and PhD'06 in Computer Science) is an Associate Professor of the Politecnico di Torino U., where he works in the Electronic CAD and Reliability research group. His current interests include system-on-chip test and reliability, especially in the area of high-quality automotive devices. Prof. Bernardi is a member of the IEEE and currently acting as the General Chair of the Test Technology Educational Program (TTEP) and the Program Chair of the Automotive Reliability and Test (ART) Workshop. He was recently acting as Topic Chair for several IEEE conferences and he published more than 120 scientific papers.

Davide Appello is Director of Product Engineering at the Automotive Digital Products division of STMicroelectronics Srl, Agrate Brianza, Italy. He is in charge of managing all industrialization activities (probe and package) for all ranges of digital products for automotive including MCUs with embedded non-volatile memories, devices for infotainment, and ADAS. He earned a degree in Electronic Engineering from the “Alma Ticinensis Universitas” of Pavia in Italy. He is also active with IEEE-TTTC and is vice-chair of the automotive and reliability test workshop (ART) and on the program committee of several conferences including ETS and DATE. He has published more than 80 papers for various conferences and magazines.

# Exposed die fan-out wafer-level packaging by transfer molding

By Sebastiaan H.M. Kersjes, Jurrian L.J. Zijl, Niels de Jong, Henk Wensink [Besi Netherlands B.V., The Netherlands]

**W**ith continuous development in packaging technology, fan-out wafer-level packaging (FOWLP) has become an established approach to reach higher integration levels and geometric efficiency. Up to now, the FOWLP market has been mainly focused on compression molding using relatively thick mold caps, basically as an outcome from the embedded wafer-level ball grid array (eWLB) development started by Infineon. With the wider adoption of FOWLP, new encapsulation processes and equipment have also been introduced into the market. One such technology is wafer-level transfer molding. This technology evolved from the current FOWLP capabilities, and achieves the thinnest mold cap possible via a process called exposed die molding, which can only be accomplished using transfer molding.

This paper discusses two of the key factors that are crucial for a successful transfer molding process of thin 12" exposed wafer-level packages. First, the influence of epoxy mold compound (EMC) on warpage is discussed. Contrary to compression molding, transfer molding uses materials that so far tend to induce more warpage. This paper introduces the basics behind warpage and how this can be used to select a proper EMC. Completing this section is an indicative warpage calculation using an analytical approach. Second, the topic of dynamic clamping in correlation to exposed die molding is discussed. A key part of exposed die molding is the critical balance between the clamping force and the fluid pressure of the injected EMC. The control strategies used to maintain this balance will be discussed in this second section. Finally, an exposed die 12" wafer-level molded demonstrator is presented.

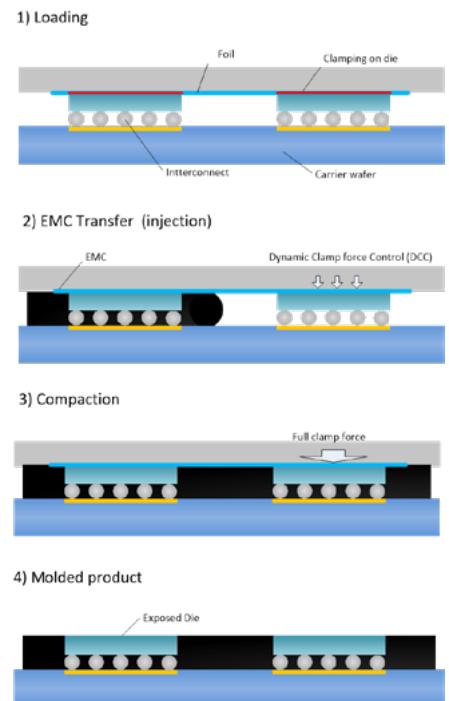
## Introduction

Performing transfer molding on 12" wafers is something many have thought to be impossible. The EMC has to flow through a narrow slit over such a long

distance that it becomes very challenging for the EMC as well as for the equipment. Traditional EMC will inhibit a high viscosity, which leads to a very high flow resistance. Also, gel times are often too short to allow enough time for completely filling of the 12" mold cap. Hence, this process development started by characterizing the flow behavior of EMCs, which resulted in the discovery of varieties that could do the task. This encouraged the development of actual equipment, and the pursuit to realize a repeatable basic wafer-level transfer molding process. Because there are many types of applications in wafer-level packaging, the research continues to have the best combination of process settings and material properties. One particularly challenging application is exposed die molded underfill (E-MUF) at the wafer level, for which the schematic process flow is shown in **Figure 1**.

In the first phase shown in **Figure 1** – "Loading" – a carrier wafer (further called simply "wafer") containing flip-chip devices can be seen where the mold tool is closed and is gently pressing against the top surface of the flip chips (die). In the second phase, the EMC is transferred through the gap between the top mold tool and the wafer, thereby encapsulating the flip chips on five sides. The pressure on the flip-chip device should be high enough to prevent EMC from flowing over the flip chips, but low enough to prevent damage to the interconnect. In the third and final phase, the EMC is compacted to eliminate potential voids and improve adhesion. This leads to a high EMC fluid pressure, and the full clamp force has to be applied on the package, while keeping the resultant force on the die surface unchanged. This dynamic clamping behavior needs to be accurately tailored to the application.

The reason to pursue this path of wafer transfer molding is to bring something extra to the 12" wafer package. In general, the EMC material is available at



**Figure 1:** Schematic process flow of the E-MUF FOWLP process.

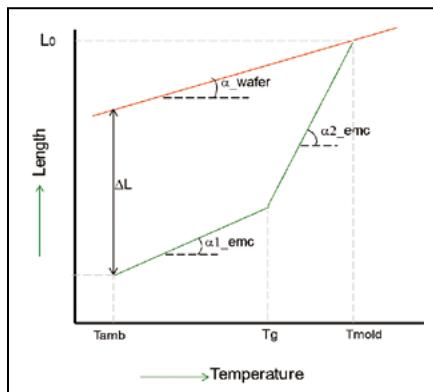
a lower cost and has a shorter cure time, which can boost the throughput. When performing molded under fill (MUF), the process of capillary underfill (CUF) can further be omitted yielding another cost reduction. Also, because the mold tool is closed before the injection of the EMC, parts on the wafer or die can be kept clean and exposed without an extra backgrinding step, which gives new possibilities in packaging strategies like 3D stacking. Furthermore, by clamping on the die, the die position is secured and "die swim" is prevented. Of the many challenges that were faced during the development of this process, two are highlighted in this paper. One refers to the material side and selection of the EMC that has the least warpage. The other challenge refers to the force balance on the mold tool and how this is maintained in the equipment.

## Wafer warpage

The following sections discuss predicting warpage and model validation.

**Prediction of warpage.** In the search for a suitable EMC that causes minimal warpage, close collaboration between the equipment supplier and the EMC supplier is needed. The EMC supplier can manufacture several small batches of test EMCs with a low coefficient of thermal expansion (CTE), a low viscosity, and a good particle distribution. The feedback from the equipment supplier to the EMC supplier after doing the molding tests is crucial for the development of the best EMC for wafer-level transfer molding. Even with a close collaboration, soon there are many types of EMCs that should be tested. Finite element method (FEM) analysis in combination with a trial and error testing method works well [1], however a faster selection method is possible by doing some simple calculus in advance and predicting which EMC will have the best warpage behavior.

Traditionally one uses the material properties of the wafer and EMC for the prediction of warpage. For the wafer, the CTE ( $\alpha_{\text{wafer}}$ ) is the only parameter that is used. For the EMC, one uses the material properties  $\alpha_{1\text{-emc}}$ ,  $\alpha_{2\text{-emc}}$  and  $T_g$ , where  $\alpha_{1\text{-emc}}$  and  $\alpha_{2\text{-emc}}$  are the CTEs below and above the glass transition temperature  $T_g$ , respectively. In order to predict the warpage, one calculates the difference in effective length change  $\Delta L$  of the EMC when the EMC cools down from mold temperature to ambient temperature relative to the wafer. The smaller the effective length change  $\Delta L$  between wafer and EMC, the better the warpage will be. Graphically this can be seen in **Figure 2**. At mold temperature  $T_{\text{mold}}$ , both the wafer and EMC have the same length  $L_0$ . When they cool down to ambient temperature,  $T_{\text{amb}}$ , the diameter of the wafer



**Figure 2:** The shrinkage of the wafer and EMC during the cool down process. The distance  $\Delta L$  is generally assumed to be a measure for the warpage.

decreases equal to a slope of  $\alpha_{\text{wafer}}$ , while the EMC length decreases first with a slope of  $\alpha_{1\text{-emc}}$ , and below  $T_g$  with a slope  $\alpha_{2\text{-emc}}$ . At  $T_{\text{amb}}$ , a difference in length will remain, which will cause warpage. Using this graphical method in practice does not always work well, because important parameters like the thickness and Young's modulus of the wafer and mold cap have been neglected, which have a significant influence on the warpage.

A more accurate method to predict the warpage, whereby the thickness and Young's modulus of the materials is taken into account, is Timoshenko's formula of the bimetallic strip [2]. The bimetallic strip consists of two layers of materials with different properties as can be seen in **Figure 3**. With this formula, one can calculate the radius of curvature,  $\kappa$ , as a function of the material and geometric properties of a bimetallic rectangular strip:

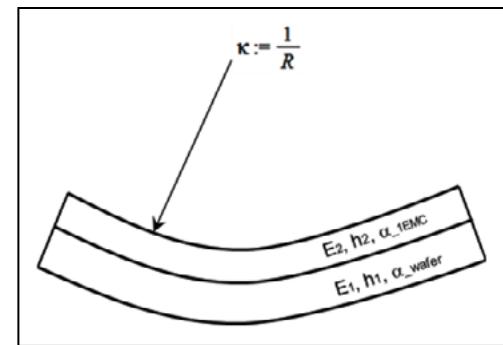
$$\kappa = \frac{6E_1 E_2 (h_1 + h_2) h_1 h_2 \epsilon}{E_1^2 h_1^4 + 4E_1 E_2 h_1^3 h_2 + 6E_1 E_2 h_1^2 h_2^2 + 4E_1 E_2 h_2^3 h_1 + E_2^2 h_2^4}$$

Where  $E_1$  and  $h_1$  are the Young's modulus and thickness of material one (wafer material); and  $E_2$  and  $h_2$  are the Young's modulus and thickness of material two (EMC material) as can be seen in **Figure 3**.  $\epsilon$  is equal to the misfit strain and can be calculated by:

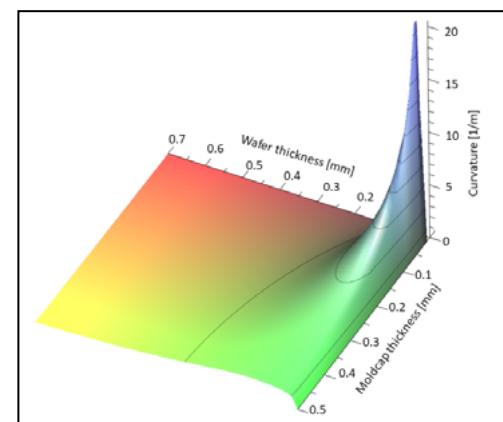
$$\epsilon = (\alpha_{1\text{-emc}} - \alpha_{\text{wafer}}) * \Delta T$$

Here,  $\alpha_{1\text{-emc}}$  is equal to the CTE of the EMC below its glass transition temperature, and  $\alpha_{\text{wafer}}$  is equal to the CTE of the wafer.  $\Delta T$  is equal to the current temperature minus the glass transition temperature,  $T_g$ .  $T_g$  is used under the assumption that above  $T_g$ , no significant stresses will be built up that contribute to the warpage due to the much lower Young's modulus. In this formula, the curvature ( $\kappa$ ) shows a dependency of the thickness of the mold cap ( $h_2$ ) and wafer ( $h_1$ ). This makes it very useful to see if the ratio between mold cap thickness and wafer thickness has been balanced to reduce warpage. In **Figure 4** one can see a three-dimensional plot of Timoshenko's formula for a silicon wafer with an EMC mold cap. When the value of the curvature becomes high, a highly warped wafer can be expected. This is the case when a thin wafer of for instance, 50  $\mu\text{m}$ , is used in combination with a 100  $\mu\text{m}$  EMC layer.

**Validation.** Although the Timoshenko formula has been derived for a rectangular strip, it will give a qualitative estimation of the warpage of a circular wafer with a mold cap. Therefore, it is suitable to make a comparison among the different EMC types, without giving the exact value of the warpage. In order to prove this comparison method, an experiment is done where several EMC types are molded on a 12" silicon wafer using several cap heights ( $h_2$ ) and EMCs (**Table 1**). Based on the calculations with Timoshenko's formula, the four most promising EMCs have been selected, which give a variety in the calculated  $\kappa$  values. After molding, the warpage of the wafers were measured, which can be seen in the last row of **Table 1**. Clearly, a strong correlation can be observed between the calculated curvature and the amount of



**Figure 3:** A bimetallic strip. With Timoshenko's formula, one can calculate the curvature  $\kappa$ .



**Figure 4:** A three-dimensional plot of Timoshenko's formula. The curvature as a function of the layer thickness of the wafer and mold cap is shown in this plot.

warpage. With this very simple calculation method it is easy to get a qualitative indication of the warpage in advance of complicated simulations, which makes the selection of promising EMC types and package dimensions much faster.

## Dynamic clamping

The following sections discuss clamping dynamics, and the setup and control strategy.

**Clamping dynamics.** Transfer molding starts by closing the mold tool before the molten EMC is applied to the device. This makes it possible to clamp gently on the die and protect it from the EMC, thereby keeping the top die surface exposed (see [Figure 1](#)). Clamp force at this stage is still relatively low to protect the (carrier) wafer, dies and interconnect from damage. Next, the molten EMC is injected into the mold tool and the clamping force has to be increased gradually together with the rise of the EMC pressure, to prevent the mold tool from opening. Finally, the complete wafer is covered with the EMC, and in the compaction phase, the final transfer pressure is increased to eliminate potential voids and ensure full adhesion. Forces can now rise up to 1000KN for a 12" FOWLP package.

To visualize the balance that needs to be maintained during this sequence, [Figure 5](#) displays a simplified force model of the process. In this model, the clamping and fluidic pressure are modeled as a force  $F_1$  and  $F_2$ , respectively.  $Z_1$ ,  $\Theta_1$ ,  $Z_2$ ,  $Z_3$  represent the movement and tilt of respectively, the mold tool, the die, and the interconnect.  $K_1$  is the stiffness of the foil,  $K_2$  the stiffness of the die, and  $K_3$  the stiffness of the die attach film (DAF) or interconnect in case of E-MUF.  $A_1$ ,  $A_2$  and  $A_3$  represent the contact areas, respectively, between the mold tool to wafer, the foil to the die, and that of the die to the interconnect. The clamp pressures are represented by  $P_1$ - $P_3$ , where  $P_1$  and  $P_2$  are the sealing pressures on the wafer edge and die, and  $P_3$  is the pressure in the interconnect. The challenge is to keep the forces and surface pressures in balance. In other words, for a given fluidic pressure  $F_2$ ,  $F_1$  should be adjusted such that there is no movement in  $Z_1$ ,  $\Theta_1$ ,  $Z_2$  or  $Z_3$ .

As the clamping area  $A_1$  is typically less than 2% of the full area of the mold, the clamping pressure  $P_1$  to seal the mold cavity to the

EMC	A	B	C	D	
Wafer thick. [ $\mu\text{m}$ ]	$h_1$	775	722	722	775
E mod. [GPa]	$E_1$	130	130	130	130
Cap thick. [ $\mu\text{m}$ ]	$h_2$	140	532	366	200
E mod. [GPa]	$E_2$	8.1	11	21	8
CTE diff. [ppm]	$\Delta\alpha$	11.8	20.8	4.8	7.8
Temp. dif. [K]	$\Delta T$	147	100	134	145
Curvature [1/m]	$\kappa$	0.171	1.349	0.467	0.163
Warpage [mm]	-	0.406	10.41	1.412	0.324

**Table 1:** EMC D gives the lowest calculated value of the curvature, which is in line with the warpage measurements displayed in the last row.

wafer is relatively low. A larger contribution comes from the surface of the dies where the clamping pressure  $P_2$  should be above a certain minimum to keep the die free from EMC. At the same instance, the clamping pressure  $P_3$  has a maximum, which depends very much on the design of the product. For exposed D2W products, the die and DAF can generally accommodate a range of force. For more advanced products such as E-MUF, or when a soft DAF is used, pressure on the die must be maintained relatively constant in order to prevent damage to the interconnect, or sinking of the die into the DAF. Hence, there is a more narrow balance window in

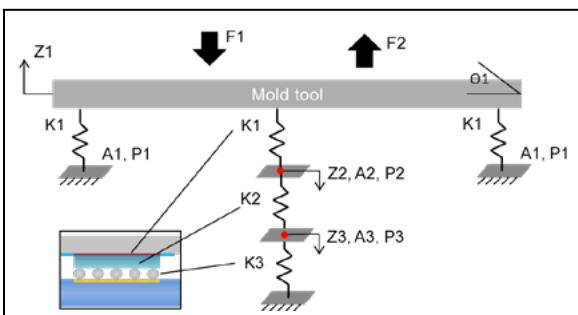
which the forces need to be arranged. The balance between the clamping pressures  $P_1$  and  $P_2$  is defined mechanically by the mold tool by using differences in height, which can be adjusted if needed.

Because flow length is long (300mm) and relative to that, the mold cap is thin (down to 150 $\mu\text{m}$ ), a large pressure gradient is formed over the wafer going from a high pressure at the EMC injection point to a zero pressure at the EMC flow front. In the model, this pressure is annotated with  $F_2$ , and can be substantial depending on the injection speed and flow properties of the EMC. This gradient changes the force balance and to maintain sufficient pressure on the die this unbalance needs to be controlled. In addition, the position of  $F_2$  starts at the injection point and moves during the transfer towards the middle of the wafer. Therefore,  $F_1$  needs to be adapted constantly in magnitude, as well as in position, to prevent planar opening or tilt of the mold tool. The next section will discuss how this is achieved.

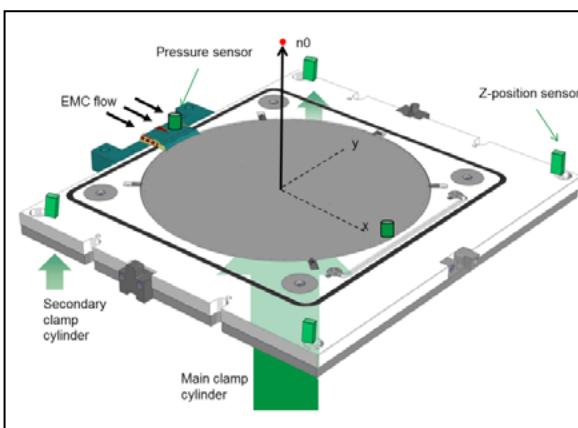
**Setup and control strategy.** To control the clamping balance during the injection state, a setup is created as displayed in [Figure 6](#). Visible are a bottom mold tool onto which a 12" wafer can be centered.

Injection of the molten EMC occurs from the left-hand side via a separate construction that is attached on top of the wafer edge, and that is part of the clamping edge of the mold tool. For clamping, the bottom mold tool is moved upward against a stationary top mold. The clamping forces thereby come from below created by a main clamp cylinder acting on the center of the mold tool. Two secondary clamp cylinders are placed at the injection side (left side) of the mold tool. These secondary cylinders can deliver up to 15% of the full clamp force, and are only intended to steer the mold tool during the injection phase.

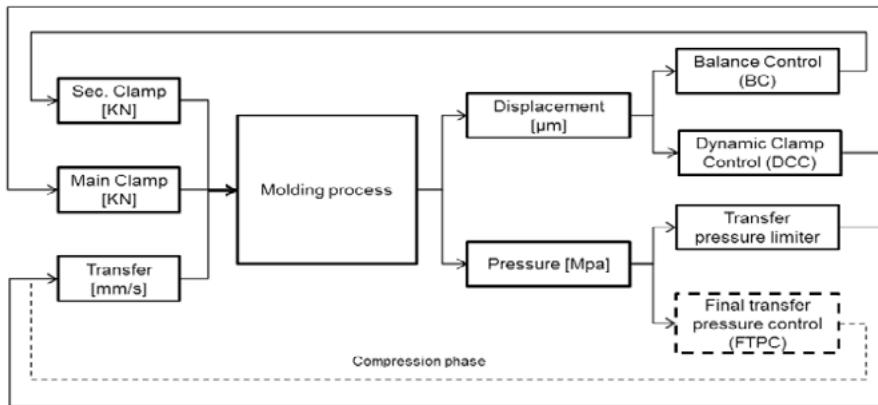
To monitor the motion of the mold tool, four Z-position sensors are attached to the bottom mold. By registering the displacement of all four corners of the mold tool, the motion vector  $n_0$  can be calculated and used for control purposes. [3]. To monitor the fluidic pressure in the mold tool, two pressure sensors are included. They are placed in the top mold and are shielded from the EMC flow by a release foil. The first pressure sensor measures the EMC pressure at the injection point (left side) just before it



**Figure 5:** An illustration of the force model of the transfer molding process, including the stiffness, that needed to be considered.



**Figure 6:** Mechanical setup created to control the mold balance during transfer molding.



**Figure 7:** Interaction diagram of the applied control strategies.

enters the mold cavity. The second pressure sensor is located at the venting side of the cavity where the flow of the EMC stops at the end of the filling process. With the sensors located at these positions, the injection pressure can be monitored, as well as when the EMC flow completely fills the mold cavity. Secondly, the pressure sensors can be used to determine the pressure gradient over the mold tool [4].

Using the setup described above, several control strategies were applied over the injection and compaction phase as mentioned in the introduction. **Figure 7** shows a schematic overview of how the control strategy implementations interact with the molding process. The left-hand side represents the inputs for the molding process consisting of the secondary clamp force, the main clamp force, and the transfer speed at which the EMC is injected. Coming from the molding process are the sensor outputs, displacement and pressure, which are fed into the control strategies. Based on the sensor outputs, these control strategies adjust the input parameters. The strategies individually control the inputs, which simplifies the control strategies. However, as they merge at the molding process, they are prone to influencing each other. By defining proper control parameters it can be ensured that a stable and workable process is maintained.

Going from top to bottom in **Figure 7**, the first control strategy that is applied is the balance control (BC) of the mold tool. As discussed before, the fluidic pressure in the first phase of the injection causes a pressure gradient in the mold tool. As a relative low clamping force is applied in the beginning of the molding process, this gradient can open the mold tool at the injection side, which needs to be prevented. By using the data from the distance sensors, the tilt ( $\Theta$ ) in the x and y directions is calculated and accordingly,

the force applied by the secondary clamp cylinders is adapted. Using this strategy, the tilt of the mold tool can be minimized while the total clamp force is not increased.

The second strategy is called dynamic clamping control (DCC) and controls the vertical opening of the mold tool. By once again using the input of the distance sensors, the opening of the mold tool can be monitored. This opening typically occurs when pressures inside the mold tool are already high. The DCC thereby acts on the main clamping force. To prevent the DCC from affecting the BC, or acting earlier than intended, a threshold value for the mold opening is included before the DCC increases the clamp force.

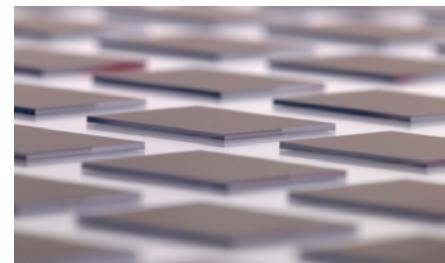
The third strategy is the transfer pressure limiter, which ensures that the fluidic pressure stays within a defined window. Without this limiter, the pressures can increase infinitely, and there is the risk that the BC or DCC act too aggressively, or even reach their operational limit. For very low viscous EMCs this pressure limit is typically set to 1MPa or less, but for high viscous EMCs, the limit can go up to 99% of the final packing pressure. The transfer pressure limit is part of the injection (transfer) profile, and is defined per amount of transferred EMC.

The last strategy is the final transfer pressure control (FTPC). This control acts when the mold cavity is completely filled and replaces the transfer pressure limiter. At this point the molding process enters the compaction phase. Using a predefined time in the molding recipe, gradients are calculated for the needed increase in clamping force and packing pressure to reach the programmed final values. When increasing the clamping force however, the EMC pressure can also increase by compression of the mold tool. During the compaction phase the FTPC measures the EMC pressure, and adjusts the

transfer motion to ensure the final packing pressure is maintained. The latter also holds that in the event of large compaction, the transfer motion can become negative to prevent packing pressures from getting too high. After the final clamping force is reached, the FTPC controls the packing pressure for another defined period of time (FTPC final adjustment) so complete stability is achieved before the final curing stage starts.

## Results

Combining the technology described above, a demonstrator was made of the exposed die wafer-level packaging process via transfer molding. For the purpose of demonstration, a simple D2W sample was molded. The sample consisted of a 12" 800 $\mu$ m-thick glass carrier, and blank Si dies (**Figure 8**).



**Figure 8:** Die setup of the molded demonstrator; 300 $\mu$ m thick dies are bonded on a 12" glass carrier using DAF.

For bonding, a soft die attach film is laminated to the glass carrier on which the dies are then placed using a standard die attach machine. In total, 284 dies are placed in the samples, which are 8.2 x 10.7mm wide, and 300 $\mu$ m thick. As it will be an exposed molded product, the latter will also be the thickness of the EMC mold cap.

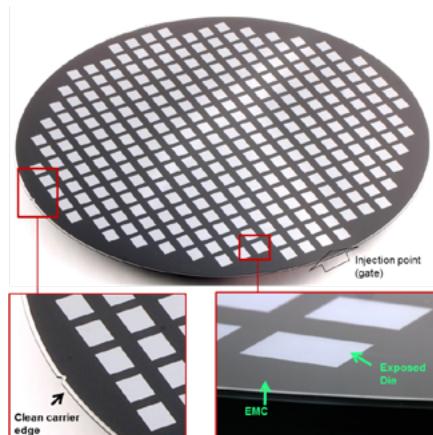
As this is a demonstrator, no sample preparations are done prior to molding. Actual samples will, however, be prepared using, for instance, pre-baking to remove moisture and plasma cleaning to activate surfaces at and underneath the die in the case of E-MUF. The EMC chosen for this demonstration is a low viscous type of 1.5Pa.s, a filler cut of 20 $\mu$ m, and a gel time of more than 45 seconds. The latter properties typically allow a good molded underfill, but also challenge the bleed prevention on top of the die. The release foil is a standard PET foil with a soft adhesive. Standard transfer molding parameters are used for the molding process (**Table 2**). **Table 2** also includes the control parameters mentioned in the previous paragraph.

Parameter	Value
EMC	48 gr (8x6gr pellets)
Temperature	165 °C
Cure time	240 sec
Pre-clamping	950 kN
Final clamping	1100 kN
Pressure limiter	4 MPa
Final packing pressure	6 MPa
Compaction time	4 sec
Opening threshold (DCC)	10 µm
FTPC final adjustment	15 sec

**Table 2:** Molding parameters used for the demonstrator sample.

After the EMC pellets are loaded, they are melted and injected into the cavity with a pressure limit of 4MPa. During this operation, the sample is clamped at 950kN, which increases to 1100kN if the mold opening exceeds a threshold of 10µm, or when the compaction phase is activated. This high pre-clamping force, or relatively low increase in clamp force of 16%, is possible due to the simple layout of the demonstrator sample. As explained earlier, the die population and interconnect density determines the maximum amount of clamping that can be applied. Although this simple demonstrator product has a die population of only 35%, the pressure that can be applied on the die is high as the die is directly supported by the bond layer and carrier (P3 and K3 in **Figure 5**). Therefore, a high pre-clamping force can be used, which is beneficial for the process.

The final result of the molded demonstrator is shown in **Figure 9**. The injection point is located at the lower right side, and the EMC flows from the lower right to the upper left. The notch for rotational alignment is on the left side. Further, one can see the clamp edge of the mold to the glass carrier, (P1 in **Figure 5**) and an overview of the exposed dies. Clearly,



**Figure 9:** A molded D2W demonstrator sample. Using wafer-level transfer molding, an exposed die 12" FOWLP on a glass carrier was achieved.

the die surfaces are kept exposed. All dies are visible, but more important, however, is that no discoloration is visible, and therefore, no signs of flash. This indicates a good uniformity of how the mold tool clamps onto the die, and thereby the achievement of a stable clamping process, for which the dynamic clamping was setup. Secondly, it is visible in the lower left picture that the mold cap and die are on the same height level, which is beneficial for further processing, but also shows that the loading on the die was not too high, as the die would then sink into the release foil leaving an imprint in the mold cap. So this operation again shows the purpose of applying dynamic clamping. Finally, it is important to notice that, although clamping of the mold tool occurred directly onto the glass carrier, this surface is clean and shows no damage.

### Summary

- This paper explains that both EMC properties and clamp force control

are dominant topics in the field of 12" wafer-level transfer molding.

- A basic method to estimate the effect of EMC choice on the resulting wafer-level warpage after molding is demonstrated.
- The impact of clamping dynamics during exposed die transfer molding were discussed and accompanying control strategies were introduced.
- Finally, the process of exposed die wafer-level packaging is demonstrated on a 12" exposed D2W sample.
- With both warpage control and the exposed dies capabilities, transfer molding at the wafer level is shown to be a serious alternative to compression molding

### Acknowledgments

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Niels de Jong is Product Manager Molding at Besi Singapore, Taiwan branch. After a brief start as a physics teacher, he made the jump to production machine building and has been doing that ever since. He has been working for Besi for 8 years now, mostly in the Asian region, where he is currently also stationed.

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# Improving Si and SiC wafer dicing yields with thermal laser separation

By Dirk Lewke, Christian Belgardt, Hans-Ulrich Zühlke, Mandy Gebhardt [3D-Micromac AG]

**I**ncreasing semiconductor content in mobile, high-performance computing, automotive and Internet of Things (IoT) applications is driving continued growth in demand for materials such as silicon and silicon carbide (SiC). Silicon wafer shipments are expected to continue to reach record levels through 2021 [1], while the SiC power device market is expected to grow from \$302 million in 2017 to \$1.5 billion in 2023 [2].

For both silicon and SiC-based devices, die singulation – dicing the product wafers into individual dies that are subsequently packaged – is an essential process that is critical to product yields. At this stage, there is no possibility for rework, and maintaining the integrity and performance characteristics of the devices is paramount to fab profitability. Mechanical blade dicing is the predominant dicing technology in the semiconductor industry today for both silicon and SiC die singulation. However, with the migration to larger-sized substrates and thinner wafers, such as for 3D-IC packaging or for reducing “on” resistance in vertical power transistors, mechanical blade dicing is increasingly challenged by cost of ownership, throughput and yield factors.

In a previous article [3], we investigated the yield benefits of applying a laser dicing approach, known as TLS-Dicing™ (thermal laser separation), to SiC wafers, and demonstrated improved process performance by reducing or eliminating micro cracks, chipping and delamination that lead to yield loss. In this article, we will study the impact of thermal laser separation on the electrical performance of singulated SiC devices, which is a particularly critical metric for power devices. In addition, we will also investigate the effects of thermal laser separation on wafer bending strength for both SiC and silicon wafers, a crucial parameter for wafer thinning applications.

## Thermal laser separation (TLS)

TLS is a kerf-free laser-based dicing technology [4]. By performing TLS, a crack is guided by controlled thermally-induced mechanical stress using a continuous-wave laser to locally heat up the material to be cut along the dicing street. Directly after the laser-heated zone, a water aerosol quickly cools down the material (Figure 1). This temperature gradient introduces a tensile stress capable of running one controlled crack independent of the lattice plane through the material. This cleaving process results in high edge quality without scratches, micro cracks or chipping, and runs with up to 400mm/s feed rate. The complete wafer material is fully separated by one laser pass.

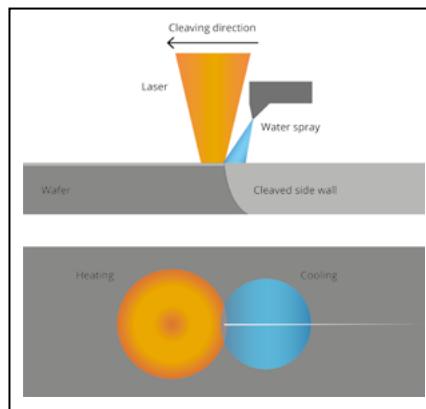


Figure 1: Principle of TLS-Dicing™.

This cleaving is the main principle of TLS. Nevertheless, TLS is always a two-step process. The introduced stress field is capable of guiding a crack, but not introducing a crack. Therefore, a crack must be introduced before the cleaving process. This is done by a scribing process where an initial crack is introduced in the material to be cut. This initial scribe involves a very short (less than 300µm long) ablative laser scribe that is introduced at the beginning of the crack. TLS with initial scribe is used in the photovoltaic industry to cut solar cells into two half cells for half-cell modules. In order to increase the straightness of the TLS cleaving line,

a continuous scribe can be used. With this technology, a scribe is performed all along the line to be cut in order to define the cleaving position at each point along the cleaving line.

For surface scribes on wafer substrates, two technologies are used. For SiC wafers, a continuous surface scribe together with a technology to remove particles in situ, called Clean Scribe, can be used. For silicon wafers, there are higher requirements regarding particles and breaking strength. Therefore, a different continuous scribe is needed for silicon, which is performed beneath the surface in order to not affect edges of the dice to be cut. This technology is called Deep Scribe. Following, these two different approaches for SiC and Si are explained in detail and results are shown.

## TLS with clean scribe for SiC wafers

SiC is mainly used for power electronic devices. Main drivers for SiC wafer dicing are the dicing costs and the throughput. While mechanical blade dicing is sufficient for standard power electronic devices on silicon-based devices, this technology suffers from high process costs and low throughput with SiC dicing. These drawbacks are due to the very high hardness and brittleness of SiC. However, these material properties make SiC an optimal candidate for TLS technology. For example, the TLS feed rates of up to 400mm/s are up to 40 times faster compared to mechanical blade dicing.

To improve straightness during TLS processing, a continuous surface scribe is used for TLS. Additionally, this surface scribe opens structures (e.g., product control monitoring structures) inside the dicing street or metal pads at the wafer edge region. Nevertheless, with a continuous surface scribe, particles are generated, which can subsequently migrate to the active chip regions and lead to yield loss during packaging. To minimize the number of particles without the need for expensive protective coatings, the clean scribe technology (patent pending) was developed. During clean scribe, a water aerosol (similar

to the water aerosol used during cleaving) is applied to the laser influence zone. This water aerosol cools and removes the particles during their formation. In **Figure 2**, two examples of a dicing street after scribing and cleaving are shown: one without, and one with, clean scribe technology. As shown in **Figure 2**, clean scribe removed virtually all particles from the dicing street.

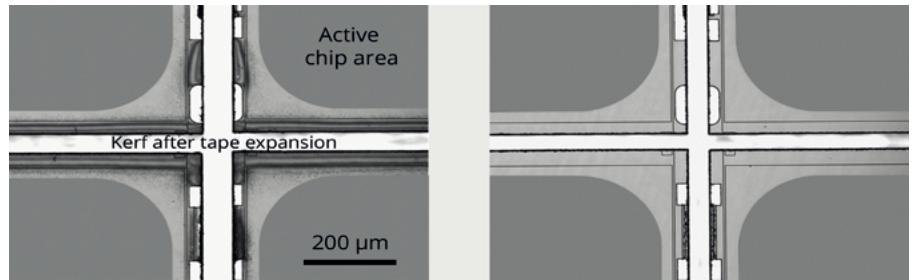
As demonstrated, TLS with the clean scribe technology is ideal to cut SiC wafers with thicknesses from 100 $\mu\text{m}$  to 550 $\mu\text{m}$  with one scribing path and one cleaving path with higher feed rates and higher edge quality compared to other dicing technologies [5]. In order to test the compatibility of the TLS process with the standard assembly workflow, fully-processed SiC wafers were diced using TLS. After dicing, the wafers were inspected and assembled at a standard production line in an assembly fab.

These assembled devices were electrically analyzed for forward blocking characteristics as well as electrically/thermally stressed using a high-temperature reverse bias (HTRB) test (**Figure 3**). All electrical test results met specifications, proving good electrical performance of the TLS-diced chips. In addition to the electrical measurements, cross section analyses of the die attach were performed in order to prove the correct die attach on the lead frame [6].

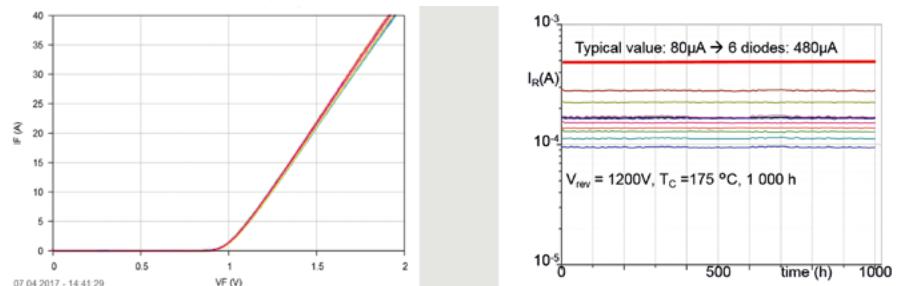
These results demonstrate that the electrical properties of the SiC diodes are not affected by the TLS process and it is possible to handle the zero kerf devices on the wafers for shipping and packaging in a high-volume backend facility.

### TLS with deep scribe for silicon devices

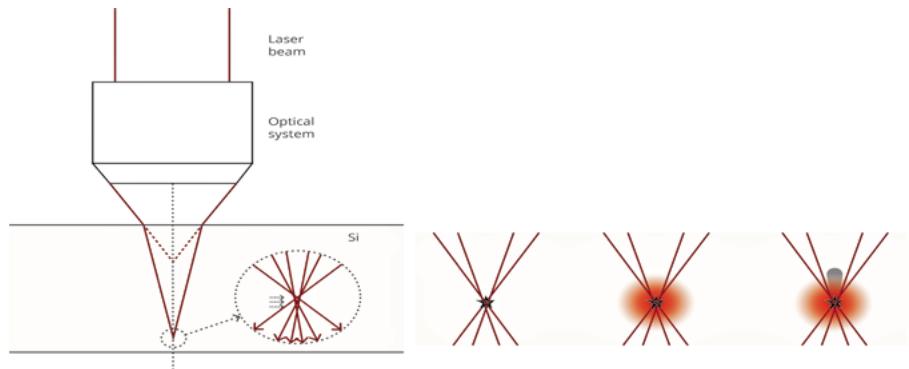
In order to improve the straightness and the bending strength of separated chips from silicon wafers, deep scribe technology was used. Deep scribe is a laser-induced subsurface material modification. A pulsed laser beam of near-infrared wavelength is focused with an objective into the silicon, which is partly transparent at 1064nm. Due to the refractive index, an extension of focal length and spherical aberrations will occur. Therefore, an optical system with a high numerical aperture and a capability to correct these spherical aberrations is used. The incident rays propagate through the silicon until the absorption increases abruptly when reaching the threshold fluence near the focal point. This increase in absorption results from the presence of free charge carriers and causes an increase in the temperature, which



**Figure 2:** Difference between a) (left) standard surface scribe and b) (right) clean scribe. Structures inside the dicing street are test structures. The tape was expanded after TLS dicing in order to visualize the kerf. The scribing depth for both scribes is approx. 20 $\mu\text{m}$ .



**Figure 3:** Electrical characteristics of TLS diced and fully assembled SiC devices: a) (left) Forward I-V characteristics of 25 random samples of SiC diodes; and b) (right) Reverse current IR during HTRB test (56 TLS-diced SiC diodes and 4 mechanical diced SiC diodes) [6].



**Figure 4:** Principle of deep scribe.

also causes lattice absorption to take place. Due to the heat conduction, a club-shaped material modification along the caustic of the laser beam will be created (**Figure 4**).

Compared to processes like stealth dicing, using the deep scribe technique modifies the material in only a very limited region. By adjusting parameters such as focus position, duration of laser pulse and laser power, an adjustment of the position and size of the modified area can be achieved. In combination with cleave, one single deep scribe layer is sufficient to separate a wafer up to 775 $\mu\text{m}$  in thickness. Nevertheless, a stacking of two or more deep scribe layers is also possible in order to provide higher perpendicularity at the edges of the separated chips (**Figure 5**).

If maximum bending strength is required, placing the deep scribe layer in the middle of the chip side wall will minimize the introduction of tensile stress to the modification layer during the bending test. To determine the bending strength of the separated dies, 200 $\mu\text{m}$  thick wafers were cut with deep scribe TLS with layers on different layer positions. For comparison, similar wafers were cut with current state-of-the-art mechanical blade dicing. The chip size for this experiment was 3.6 x 3.6mm<sup>2</sup>.

Breaking strength measurements were performed with a three-point bending test of 100 chips per side (front and back) for the different dicing technologies. The evaluation was done by Weibull analysis distribution, whereby the values for the

probability of breakage of 63.21% of all chips are determined. As expected, the breaking forces are maximized by moving the deep scribe layer into the neutral fiber (middle of the wafer), where the forces of front and back sides are nearly identical. With this approach, it is possible to achieve a more than three times higher stability of the separated chips than in the sawing process (Figure 6).

## Summary

Wafer dicing is an essential semiconductor fabrication process that is critical to die yields. As substrate sizes for SiC wafers scale upward, and new applications such as 3D/stacked die packages impact silicon wafer thickness, mainstream wafer dicing methods, such as mechanical saw dicing, become increasingly limited in their practical use. Thermal Laser Separation is a wafer dicing method that provides important cost-of-ownership, throughput and yield benefits for SiC and silicon wafers. As demonstrated in this article, the two-step TLS-Dicing™ method eliminates the need for protective coatings to mitigate particle generation during the dicing process, provides dramatically improved breaking strength of processed wafers, and does not affect the electrical properties of processed die.

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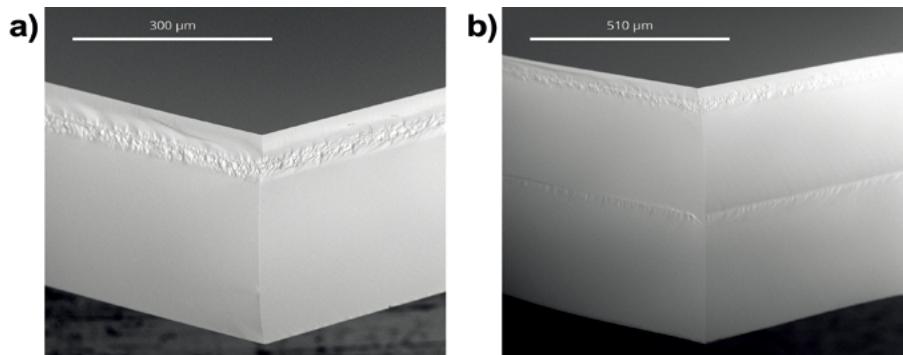
## Biographies

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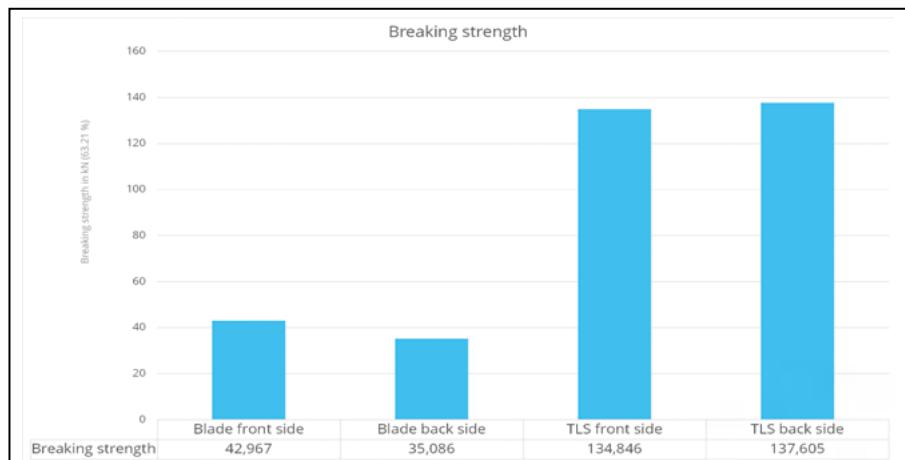
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Mandy Gebhardt is Manager Marketing/PR at 3D-Micromac AG, Chemnitz, Germany. She has an MBA in Economic Computer Science from the U. of Cooperative Education Glauchau. Since 2000, she has worked in marketing for different high-tech companies.



**Figure 5:** SEM images of Si chips cut with deep scribe TLS: a) (left) 380µm thick wafer with one deep scribe layer; and b) (right) 750µm thick wafer with two deep scribe layers.



**Figure 6:** Breaking strength evaluation of 200µm thick Si wafers with 3.6 x 3.6mm<sup>2</sup> chip size.

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<b>3D-Micromac AG</b> Technologie-Campus 8 D-09126 Chemnitz, Germany Tel: +49 371 40043-222 www.3d-micromac.com	Method: Laser Automation: LU, WA, CD WD: 300 mm FR: Models: 6 CM		Method: Laser (TLS) Automation: LU, WA, CD WD: 300 mm FR: Models: 5 CM
<b>Advanced Dicing Technologies Ltd.</b> 5 HaMada St., P.O. Box 87 Hi-Tech Park (South) Yokneam 2069202, Israel Tel: + 972-4-8545222 www.adt-co.com		Method: Saw Automation: LU, WA, CD WD: 300 mm FR: 700 mm/s Models (3)	
<b>American Precision Dicing, Inc.</b> 642 Giguere Court, San Jose, CA, 95133 USA Tel: +1-408-214-3723 www.wafer-dicing.com		Method: Saw Automation: CM WD: 300 mm FR: CM Models (CM)	
<b>ASM Laser Separation International (ALSI) BV</b> Platinawerf 20g 6641 TL Beuningen Netherlands Tel +31 24 678 2888 www.alsi.asmp.com			Method: Laser Automation: LU, WA, CD WD: 300 mm FR: 500 mm/s Models (3)
<b>Coherent Inc.</b> 5100 Patrick Henry Drive Santa Clara, CA 95054 USA Tel: +1-408-764-4983 www.coherent.com			Method: Laser Automation: CM WD: CM FR: CM Models (CM)
<b>Control Micro Systems (CMS Laser)</b> 4420-A Metric Drive Winter Park, FL 32792 USA Tel: +1-407-679-9716 www.cmslaser.com			Method: Laser Automation: CM WD: CM FR: CM Models (CM)
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<b>EO Technics Co., Ltd.</b> 91 Dongpyeonro Anyang Korea (13930) Tel : +82 31-422-2501 www.eotechnics.com			Method: Laser Automation: WA, CM WD: 300 mm FR: 500 mm/s Models (1)
<b>Hanmi Semiconductor Co., Ltd.</b> 532-2 Gajwa-Dong, Seo-Gu Incheon, South Korea Tel: +82-32-571-9100 www.hannimsemi.com			Method: Laser Automation: CM WD: 300 mm FR: CM Models (1)

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Hylax Technology Pte Ltd 11 Yishun Industrial Street 1 #02-100 Northspring Bizhub Singapore 768089 Tel: +65 6465 9902 www.hylax.com	<p>Method: Laser</p> <p>Automation: CM</p> <p>WD: CM</p> <p>FR: CM</p> <p>Models (CM)</p>		<p>Method: Laser</p> <p>Automation: CM</p> <p>WD: CM</p> <p>FR: CM</p> <p>Models (CM)</p>
IPG Photonics Corporation 50 Old Webster Road Oxford, MA 01540, USA Tel: +1-508-373-1100 www.ipgphotonics.com	<p>Method: Laser</p> <p>Automation: WA, CM</p> <p>WD: CM</p> <p>FR: CM</p> <p>Models (1)</p>		<p>Method: Laser</p> <p>Automation: LU, WA, CM</p> <p>WD: 300 mm</p> <p>FR: CM</p> <p>Models (2)</p>
Loadpoint Ltd. Chelworth Industrial Estate Cricklade Swindon, Wilts. SN6 6HE, England Tel: +44-1793-75116 www.loadpoint.co.uk		<p>Method: Saw</p> <p>Automation: WA, CM</p> <p>WD: 300 mm</p> <p>FR: 500 mm/s</p> <p>Models (3)</p>	
Loomis Industries, Inc. 1204 Church Street St. Helena, CA 94574 USA Tel: +1-707-963-4111 www.loomisinc.com	<p>Method: Mechanical</p> <p>Automation: WA</p> <p>WD: 150 mm</p> <p>FR: CM</p> <p>Models (1)</p>		
NPOS Technologies Inc 155 N. Lake Ave, Ste 800 Pasadena, CA 91101 USA Tel: +1-626-398-0327 www.npos-usa.com	<p>Method: Mechanical</p> <p>Automation: CM</p> <p>WD: 200 mm</p> <p>FR: 100 mm/s</p> <p>Models (3)</p>		
Opto System Co Ltd. 100 Nogami, Miyamaki Kyotanabe City Kyoto 610-0313 Tel: +81-774-68-4441 www.opto-system.co.jp	<p>Method: Laser, Mechanical</p> <p>Automation: LU, WA</p> <p>WD: 100 mm</p> <p>FR: 50 mm/s</p> <p>Models (1 each)</p>		
Panasonic Factory Solutions Co., Ltd. 2-7, Matsuba-cho, Kadoma Osaka 571-8502, Japan Tel: +81-6-6905-5535 www.panasonic.com/jp/company/pfsc	<p>Method: Plasma</p> <p>Automation: CM</p> <p>WD: 300 mm</p> <p>FR: CM</p> <p>Models (1)</p>		
Planar Corporation 2 Partizansky Ave. Minsk 220033 Republic of Belarus Tel: +375-17-223-7211 www.planar.by	<p>Method: Laser</p> <p>Automation: CM</p> <p>WD: 150 mm</p> <p>FR: 600 mm/s</p> <p>Models (3)</p>	<p>Method: Saw</p> <p>Automation: LU, WA, CD</p> <p>WD: 300 mm</p> <p>FR: 600 mm/s</p> <p>Models (3)</p>	
Plasma-Therm 10050 16th St. North Saint Petersburg, FL 33716 USA Tel: +1-800-246-2592 www.plasma-therm.com		<p>Method: Plasma</p> <p>Automation: CM</p> <p>WD: 300 mm</p> <p>FR: 3,000</p> <p>Models (2)</p>	
Shibuya Kogyo Co., Ltd. Ko-58 Mameda-Honmachi, Kanazawa Ishikawa 920-8681, Japan Tel: +81-76-262-1200 www.shibuya.co.jp			<p>Method: Laser/Water</p> <p>Automation: CM</p> <p>WD: CM</p> <p>FR: CM</p> <p>Models (1)</p>
SPTS Technologies Ltd. Ringland Way Newport, NP18 2TA United Kingdom Tel: +44 1633 414000 www.orbotech.com/spts			<p>Method: Plasma</p> <p>Automation: CM</p> <p>WD: 300 mm</p> <p>FR: CM</p> <p>Models (3)</p>

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Synova S.A. Route de Genolier 13 CH-1266 Duillier (Nyon) Switzerland Tel: +41 21 55 22 600 www.synova.ch		<p>Method: Saw + Laser/Water Automation: LU, WA, CD WD: 300 mm FR: 600 mm/s Models (1)</p>	<p>Method: Laser/Water Automation: LU, WA, CD WD: 300 mm FR: 1,000 mm/s Models (4)</p>
Thermocarbon Inc. 391 Melody Lane Casselberry, FL 32707 USA Tel: +1-407-834-7800 www.dicing.com		<p>Method: Saw Automation: CM WD: CM FR: CM Models (1)</p>	
Tokyo Seimitsu Co., Ltd. (Accretech) 2968-2 Ishikawa-machi, Hachioji-shi Tokyo 192-8515, Japan Tel: +81-42-642-1701 www.accretech.jp		<p>Method: Saw (M), Laser (L) and Plasma (P) Automation: CD, CM WD: 300mm FR: CM Models (11)</p>	<p>Method: Plasma (P) and Laser (L) Automation: CD, CM WD: 300mm FR: CM Models (4)</p>

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*The Evolution of Interconnect Innovation*

# Packaging high-performance memory devices

By Damon Tsai [Rudolph Technologies, Inc.]

**W**hile wire bonding remains the dominant technology for chip-to-package connections, advanced packaging processes are gaining a growing share of the market. The transition away from wire bonding is especially notable in high-performance memory applications, where shorter signal paths, higher speed, smaller form factor and lower power are most valuable. Significant growth is forecast for both flip-chip dynamic random access memory (DRAM) and high-bandwidth memory (HBM) across a broad range of applications, with a commensurate decrease in wire bonding. Flip-chip, wafer-level packaging (WLP), fan-out wafer-level packaging (FOWLP), and fan-out panel-level packaging (FOPLP) are now seeing increasing adoption. These advanced packaging methodologies present unique inspection and metrology challenges and opportunities, including through-silicon vias (TSVs), fine-pitch redistribution layers (RDLs), copper pillar bumps, micro-bumps and die-level cracks.

## Market drivers

Demand for more functionality in a smaller footprint has driven the microelectronics industry since it began. In the context of memory, functionality refers to dramatic increases in the amount of data to be stored and the read/write speeds. In applications such as network servers, artificial intelligence and machine learning, the need for speed and the massive volume of data are driving reductions in size because shorter signal paths are inherently faster. Graphics applications require fast, wide connections between the graphics processing unit (GPU) and integrated high-bandwidth memory (stacked DRAM). For autonomous driving applications, the need for speed and capacity is coupled with increased reliability requirements. In mobile and wearable applications, small size is itself a virtue, but the coming of 5G will multiply demands for memory capacity and speed. In all cases,

increasing speed and volume requirements are also driving increases in the number and density of I/O connections.

Packaging technologies play a critical role in determining a device's ability to meet performance and size requirements, which include:

- Wire bonding, where fine wires connect pads on the die to pads on a substrate or to other die within the package, remains the dominant interconnect technology. As design rules shrink, however, wire bonding struggles to achieve the speed, small size and I/O density needed for advanced applications.
- Flip-chip packaging is a mature technology that reduces package size, increases I/O density, and increases speed by depositing solder on pads on the top surface of the chip and then flipping the chip over to connect to pads on a substrate.
- Advanced 2D and 2.5/3D packaging processes use front-end-like processes to form external connections on the chip and come in many varieties. Wafer-level processes form the connections on the wafer before it is cut into individual die. Fan-out wafer-level processes separate the die but then reconstitute them on a wafer-like substrate, adding space between die to allow room to redistribute the connections on the die using a thin organic substrate. Fan-out panel-level processes are similar, but the reconstituted panel is not constrained to be wafer-like and is both larger and rectangular.

Though wire bonding is likely to retain its dominance for many mainstream applications, its growth rate is limited while the share of packages using flip-chip and advanced packaging processes is increasing at a faster pace as a percentage of overall package growth. Growth in flip-chip packaging

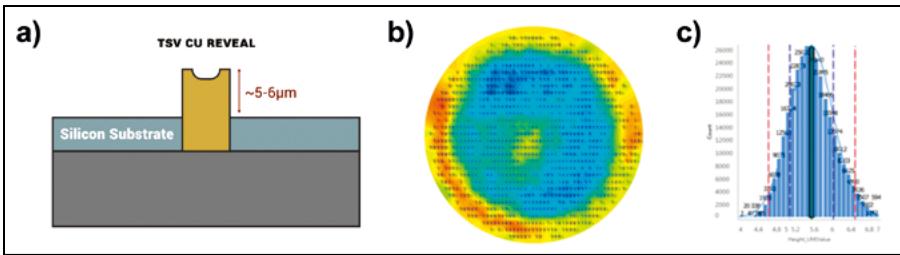
is driven primarily by the transition of DRAM from wire bond to flip chip. This is especially true for mobile DRAM where 5G will make it increasingly difficult for manufacturers to meet performance and cost targets with wire bond technology. Flip-chip DRAM is already used in application processors from major providers, including Qualcomm, HiSilicon, and MediaTek, and the transition is expected to expand, with flip chip dominating DRAM by 2023. One study [1] projects a compound annual growth rate (CAGR) of 7.8% for flip-chip packages from 2017 to 2022.

Demand from smartphones, tablets and laptops is driving growth in WLP as well, with CMOS image sensors, wearables and automotive devices also contributing. The same study [1] predicts a CAGR for WLP at 12% from 2017 to 2022, and projects WLP to surpass flip chip in total number of packages in 2019. Many new applications, including base-band processors, application processors, RF transceivers, switches, power management integrated circuits (PMIC), Internet of Things (IoT), automotive, sensors, and logic/memory combinations, are using fan-out packages, and the study also predicts an aggressive transition from wafer- to panel-based fan-out processes.

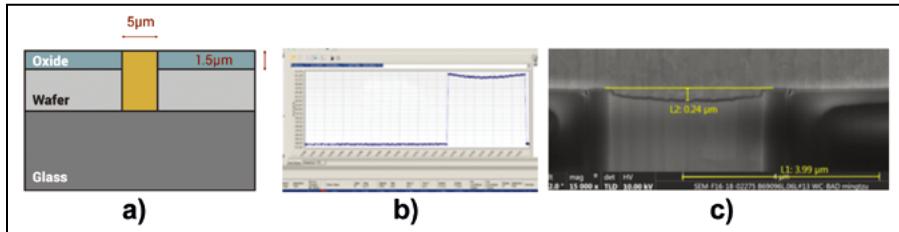
## Inspection and metrology for advanced packaging processes

Although advanced packaging technologies generally use more front-end-like processes, they include many structures not used in most front-end applications, including TSVs, RDLs, pillars, micro-bumps, and solder bumps. These are inherently three dimensional and all bring inspection and measurement requirements that are unique to advanced packaging processes.

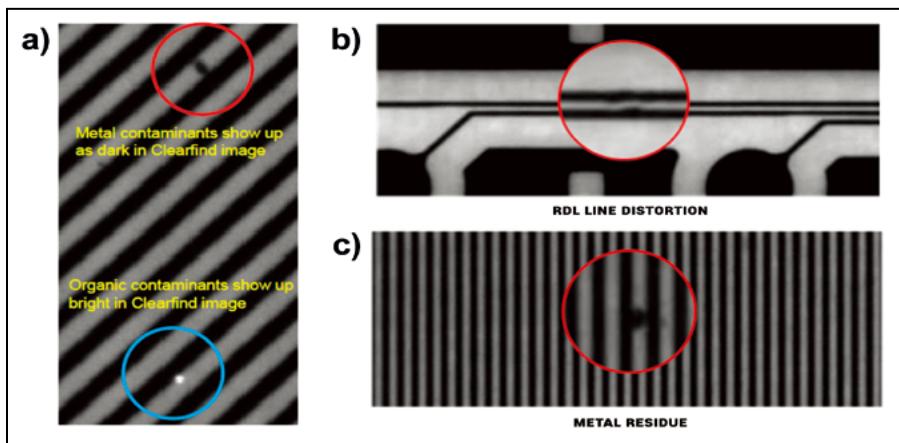
Metrology and inspection systems for advanced packaging processes have often adapted technologies used in traditional front-end or back-end applications, but some



**Figure 1:** TSV Cu reveal step: a) (left) TSV reveal height, b) (middle) full wafer plot of reveal height, and c) (right) histogram of individual measurements.



**Figure 2:** After TSV process step and data: a) (left) TSV oxide CMP, b) (middle) VTSS measurement of TSV recess, and c) (right) cross-sectional electron microscope image of the TSV recess.



**Figure 3:** a) (left) CF image of organic (bright) and metallic (dark) contaminants; b) (right upper) CF image RDL line distortion; and c) (right lower) CF image of metal residue.

critical applications have required the development of new sensors and techniques, including: high-speed laser triangulation for whole-wafer bump height metrology and advanced white light and infrared interferometry for measurements of film thickness, optical profiling, substrate metrology, and via and carrier trench depth metrology. Additionally, there are new non-visual defects that traditional inspection technologies have not been able to detect. These defects may be invisible cracks or residues that may not be caught during electrical test but cause reliability issues downstream. In this case, the development of laser-based contrast inspection has provided much needed defect detection capability.

### Through-silicon vias

TSVs are used to make connection between vertically-stacked die by creating a hole through the silicon substrate and filling it with metal. There are several types of TSVs, and many different process sequences used to form them, such as:

- TSV reveal height: The TSV reveal step is an etch process that removes the last bit of silicon after the bulk is removed by backside grinding. It “reveals” the TSV, leaving the metal fill protruding slightly above the surrounding silicon surface. The height of the protrusion is critical.
- A visual thickness and shape sensor (VTSS) provides accurate measurements of reveal height needed to control the process. **Figure 1**

Illustrates the TSV reveal step. The full wafer plot shows height variations across the wafer and the histogram shows the frequency distribution of individual measurements.

- Recess: After reveal, the wafer surface and protruding TSVs are covered with an oxide layer and the oxide is planarized with chemical mechanical polishing (CMP), leaving a flat surface with exposed TSVs. It is important to avoid excessive dishing of the TSVs, which erode faster than the surrounding oxide during CMP. The VTSS sensor can accurately measure the depth of the recess and the thickness of the oxide layer. **Figure 2** illustrates the process step and compares a VTSS measurement to a cross-section image acquired with an electron microscope showing close correlation.
- Other TSV inspections and measurements include bright-field scans for surface defects (scratches, metal residues, and particles), dark-field scans for TSV defects, and VTSS measurements of pad height and tetraethyl orthosilicate (TEOS) thickness.

### Redistribution layers

RDLs allow signals from a location on the die surface to be routed to a different location in WLP and FOWLP packages. They are typically formed by plating copper through a patterned photoresist mask, then isolated by an organic polymer (polyimide [PI] or benzocyclobutane [BCB]). Organic contaminants on metal pads can cause reliability problems that are often not apparent until a device fails in the field due to a partial connection or repeated cycling. These defects are difficult to detect with conventional optical inspection systems because they “disappear” in the noise generated by the background material. To uncover these defects, Rudolph developed Clearfind (CF) technology. CF technology is a combination of illumination, optics and image processing capabilities specifically designed to enhance contrast differences between metal and organic materials. When using CF technology, imaged metals are dark and organics are bright, eliminating the background noise.

- Shorts/opens/distortions: As shown in **Figure 3**, the enhanced contrast provided by CF images facilitates

- the detection of shorts, opens, and distortions in redistribution lines.
- (PI)/(PR)/Metal residue: Metal grains generate a random “grainy” texture in conventional optical images that complicates the detection of low contrast organic defects. CF images suppress this graininess. This suppression, combined with the bright signal generated by organic materials in CF images, makes organic residues on critical metal surfaces easy to detect (**Figure 4**).

## Solder bumps

Solder bumps deposited on contact pads provide the last layer in the connection chain for flip-chip packages or package-on-package (POP) applications. The height and coplanarity of the bumps are critical to ensuring reliable electrical connections. High-speed laser triangulation (LT) can measure height and coplanarity for every bump on the wafer, as follows:

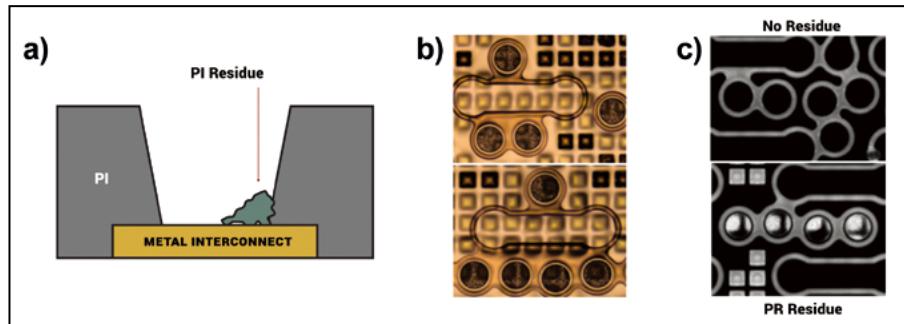
- Advanced bumping processes use a PI layer to add mechanical strength to the solder connection. This reduces the number of process steps by eliminating the under-bump metal but complicates the measurement of bump height. The PI layer is added after the bump is formed. PI is semitransparent and varies in thickness across the wafer, so it interferes with conventional bump height measurements. Combining VTSS measurements of PI thickness with LT measurements of bump height yields the true height of the bump above the surface on which it was deposited (**Figure 5**).
- Bump residue: Similar to the problems described for RDL, organic residues on bumps can degrade connection reliability, and the graininess of metal bumps in conventional optical images makes those residues hard to detect. The bright signal of organics and the suppression of metal graininess makes them easy to see in CF images (**Figure 6**).

## Copper pillar bumps

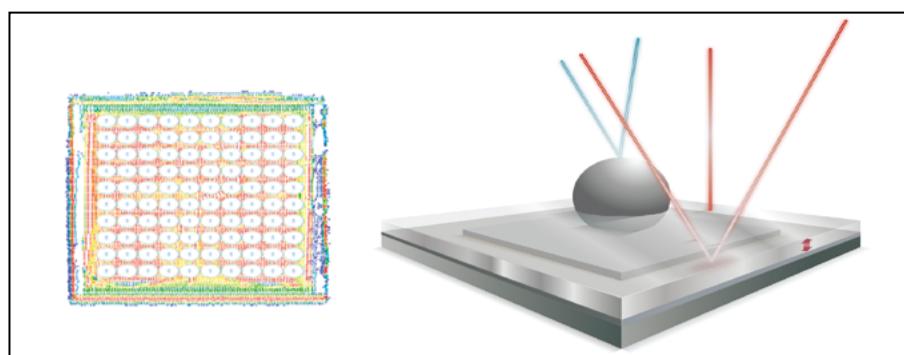
Copper pillar bumps consist of a cylindrical copper pillar topped by a solder bump. They allow manufacturers to increase bump density (by decreasing diameter and pitch) while preserving

enough height to underfill with insulating adhesives. Copper pillar bumps have additional inspection and metrology requirements, such as top and bottom critical dimension (CD). With the pitch and density of pillar interconnects increasing to

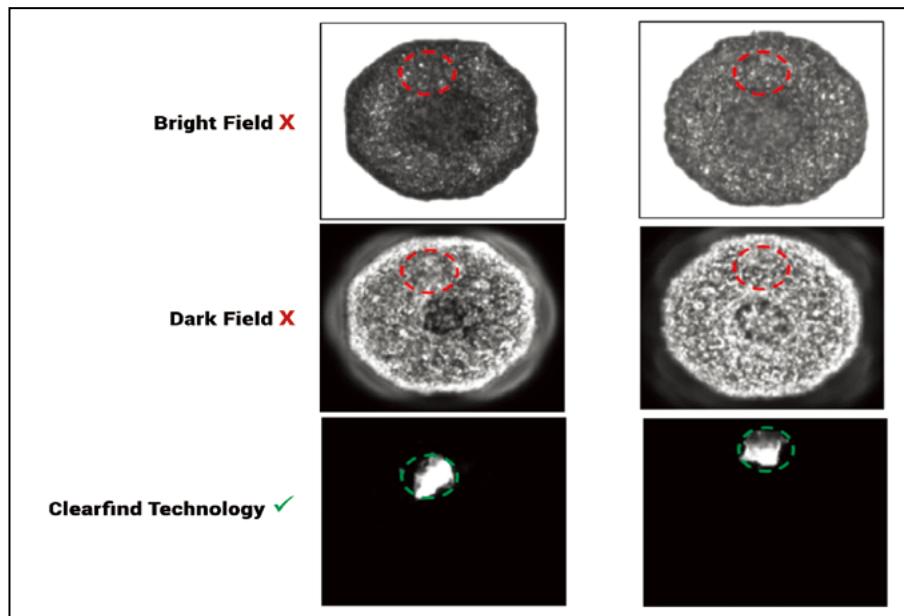
address scaling and latency, a single wafer may have more than 50 million bumps with heights down to 5 microns or less. The ability to measure CD and capture, process, and analyze the associated data are critical to process monitoring.



**Figure 4:** a) (left) Illustration of organic residue on metal contact; b) (middle) Conventional optical images of clear (upper) and contaminated (lower) metal contacts; and c) (right) CF images of clear (upper) and contaminated (lower) metal contacts.



**Figure 5:** (left) Laser triangulation measurements of bump top and between bump data points; and (right) Bump height measurement through the PI layer.



**Figure 6:** (top to bottom) Bright field, dark field, and CF images of solder bumps with organic residue.

**Figure 7** illustrates a copper pillar bump and shows full wafer plots of coplanarity, diameter, and height measurements.

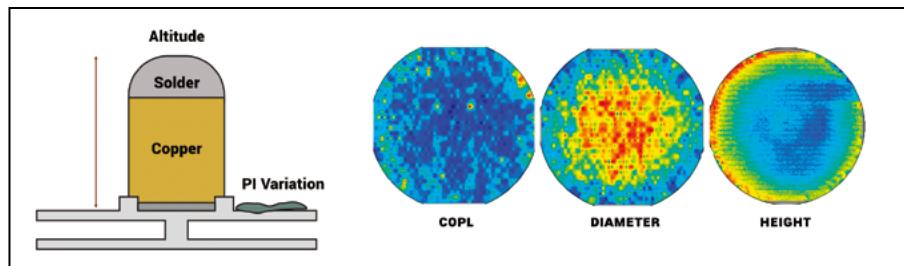
## Cracks

With the introduction of low-k dielectrics and material property mismatches, the edges of a die are prone to chipping and cracking during the saw process. Cracks then propagate into the active area of the die causing immediate impact to yield or device reliability issues downstream, as discussed below:

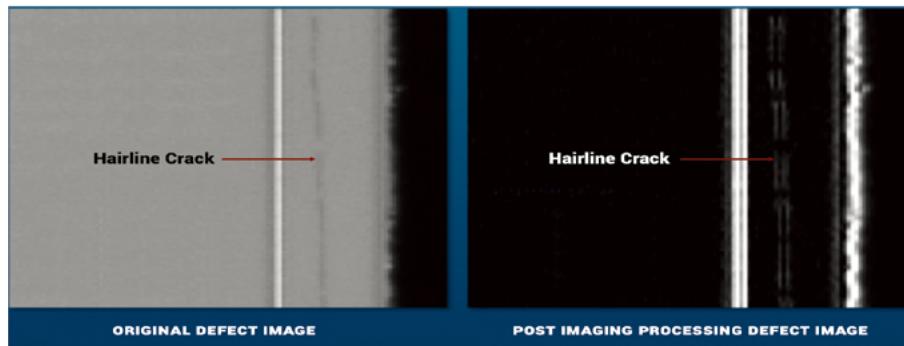
- Hairline cracks or fine surface cracks generally run across the surface of the active area of a die. Their small size and low contrast make them difficult to detect. Existing detection methods also generate unacceptably large numbers of false defects, sometimes as many as 20X the number of real defects. Die crack detection (DCD) software uses sophisticated post-image processing techniques to enhance the detectability of hairline cracks by increasing their apparent size and contrast (**Figure 8**). In an experiment, DCD software detected all cracks found by conventional techniques in addition to a number of crack defects that went undetected, while showing a significant reduction in false positive nuisance defects.
- Sidewall cracks are seen post saw and protrude past the die seal ring into the active area of the die. They are difficult to see because they are typically below the surface and are obscured by device patterning. By combining DCD with die seal ring (DSR) inspection, these defects can be detected and classified. In addition, infrared imaging can provide valuable corroborating evidence that the “disappearing” sidewall cracks are real and not nuisance defects (**Figure 9**).

## Summary

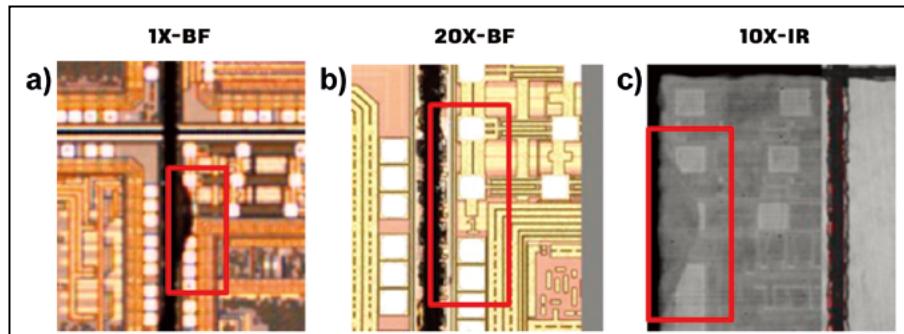
Many new products are replacing wire bonding for high-performance memory technologies that require fast communication with other chips and external connections to transport and store large volumes of data. Flip-chip and advanced packaging processes provide shorter, denser, more numerous



**Figure 7:** (left to right) Copper pillar bump; and full wafer measurements of the bump: coplanarity, diameter and height.



**Figure 8:** (left) Original image of a hairline crack; and (right) DCD enhanced image of the hairline crack.



**Figure 9:** (left) a) 1X bright-field image of sidewall crack, b) (middle) 20X bright-field image of sidewall crack; and c) (right) 10X IR image of sidewall crack.

signal pathways and smaller package sizes. The transition is expected to continue and accelerate. Although these packaging technologies use many front-end-like processes, the unique structures they create present new challenges for inspection and metrology. Many of these challenges are best addressed by sensors and systems specifically developed for

the application. Rudolph has developed a flexible suite of inspection and metrology sensors to address these challenges.

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1. VLSI Research - private communication, Feb. 2018.



## Biography

Damon Tsai received his Master of Science degree in Laser and Optical Engineering from National Tsing Hua U. and is Director of Inspection Product Management at Rudolph Technologies; email [damon.tsai@rudolphtech.com](mailto:damon.tsai@rudolphtech.com)



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# Avoiding the downfalls of bond wires with printed interconnects

By Bryan Germann [Optomec Inc.]

**C**onsider the most expensive wire bond failure in history. In 1997, NASA experienced a failure in the solid-state data recorder aboard the Hubble Space Telescope, which at the time was roughly 350 miles above the Earth's surface (**Figure 1**). The data recorder contained multi-chip stacked dynamic random access memory (DRAM) modules that were connected to circuit boards with 25 $\mu$ m gold bond wires. Apparently, several of these bonds fractured from a combination of poor initial quality and fatigue from subsequent vibration in service.

## Wire bonds to the moon and back

Each year, the electronics industry creates over ten trillion semiconductor interconnects – more than 1000 interconnects for every human on Earth. At ~3mm length apiece, that would amount to 30 million km of wire – enough to go to the Hubble Telescope and back over 27,000 times. For the last 50 years, the vast majority of these connections were made with wire or ribbon bonds, so one might conclude that, by now, the process is in a state of near perfect reliability. Unfortunately, wire bonding still suffers failures during processing, as well as failures in the field during use. Direct printing of semiconductor interconnects with finely-sprayed inks containing conductive nanoparticles is a promising alternative to wire bonding in many cases.

Non-contact micro direct printing technology has proven to be a more gentle method of producing interconnects, which is of particular interest for those packaging fragile parts such as gallium arsenide (GaAs). Furthermore, this direct printing process is not limited to planar arrangements. ICs can be stacked or arranged on curved surfaces to save space or improve signal integrity.

## How wire bonds fail

Wire bonds can fail in a number of ways (**Figure 2**). The U.S. Department of Defense, in MIL-STD-883F Method 2011 [1], lists eight common failure modes for wire bond interconnects:

1. Wire break at neckdown point (reduction of cross section due to bonding process).
2. Wire break at point other than neckdown.
3. Failure in bond (interface between wire and metallization) at die.
4. Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.
5. Lifted metallization from die.
6. Lifted metallization from substrate or package post.
7. Fracture of die.
8. Fracture of substrate.

Many of the failure modes listed above are exacerbated by the wire bonder's injection of contact energy — either thermal or mechanical — into the bond pads of the die or the substrate. The die or substrate can crack and the pads can delaminate from the intense ultrasonic or thermosonic zap from the bonding equipment.

Even when the pads, the die and substrate are not damaged from the bonding process, there is a chance for wire fracture at the neckdown point from the residual bending stresses in the wire loop. Higher wire loop heights reduce the stresses in locations 1 and 3; however, this increases the required

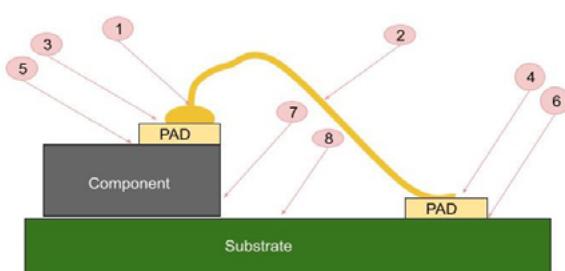
package height and can degrade the signal acuity and coupling efficiency. Furthermore, the higher loop heights can result in lower mechanical resonant frequencies in the wire itself. In fact, in the case of the Hubble Telescope failure, the resonant frequency of the failed bond wires was below 1kHz—within the operating range of the electronics' expected environment.

## Low-impact, printed interconnects

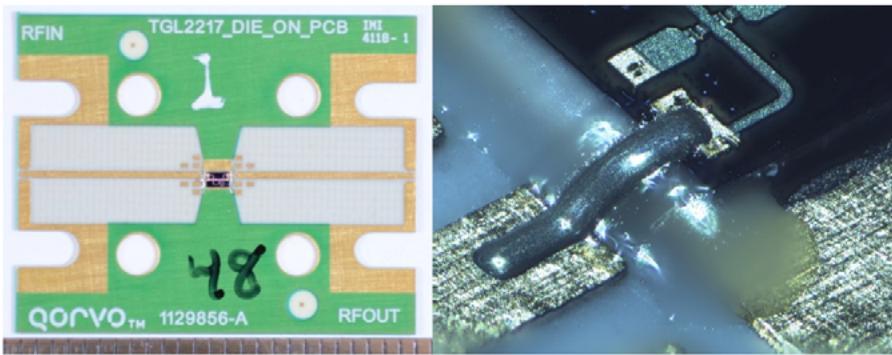
For many applications, getting rid of the wire bond entirely with a printed interconnect is worthy of consideration. A printed interconnect does not require a static or oscillating force to be applied to fragile components, pads or substrates. It is essentially a non-contact process. In fact, some non-contact printing processes can print the conductor from



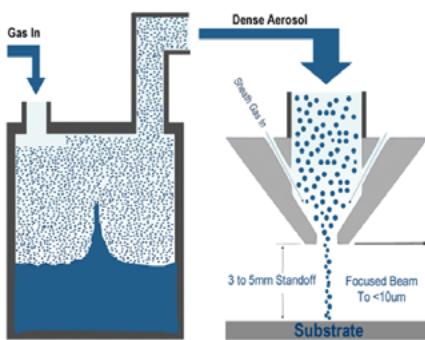
**Figure 1:** A bond wire failure in your home PC is one thing, but in the case of the Hubble Telescope at its current altitude, the service call had a price tag of around \$1 billion. SOURCE: NASA Hubble Space Telescope (Courtesy NASA/JPL-Caltech [[www.jpl.nasa.gov/imagepolicy](http://www.jpl.nasa.gov/imagepolicy)])



**Figure 2:** How wire bonds fail.



**Figure 3:** Photo of an RF interconnect printed from a ceramic substrate onto an IC. The 140 $\mu\text{m}$  printed bond wires were made with Optomec's Aerosol Jet connecting a RF power limiter PIN diode to a microstrip line.



**Figure 4:** Non-contact direct printing process diagram.

up to 5mm away from the parts, and can easily accommodate changes in the Z-height. The parts do not need to be on the same plane and can have relatively loose tolerances in the Z-dimension.

There are, however, limitations to implementing printed interconnects. Obviously, the process needs something on which to print. Unlike bond wires, printed interconnects cannot “jump” over gaps between components. They require a relatively smooth transition. In **Figure 3**, for example, an RF interconnect has been printed from a ceramic substrate up and onto an IC. To provide a stable and smooth ramp on which to print, a glass-filled epoxy fillet was dispensed. As shown in the figure, the resulting interconnect has practically no height, is physically shorter than a wire bond, and was produced without touching the components. This low profile enables minimization of overall package height, as well as reduction in overall interconnect inductance, which is preferential for high-frequency RF interconnects.

### Interconnect dimensions

Application requirements drive the wire bond dimensions needed for that particular application: high-I/O memory

die require tightly spaced bond pads and minimal wire dimensions. In contrast, high-power RF applications, such as limiter PIN diodes for power transmission lines, require multi-millimeter wide bond ribbons or multiple larger diameter bond wires to produce the target wire impedance and resistance the application requires. In most cases, different machines, or even bonding techniques, may be needed to meet all of those individual requirements. Furthermore, in some cases, the substrate fragility or minimum bond pad spacing may limit which types of bond wire or bond wire dimensions can be used.

Printed wire interconnects deposited with Optomec's Aerosol Jet (see **Sidebar**), for example, have a range of dimensional flexibility, meaning that interconnects as narrow as 20 $\mu\text{m}$  to as wide as 2.5mm with thicknesses as low as 10 $\mu\text{m}$  have been demonstrated. This makes the process of scaling the printed conductor to the dimensional requirements of packaging application as simple as changing a process recipe

— all done without any increased force applied to the substrate or sacrificing of bond pad spacing due to direct contact with the die substrate. However, because the interconnect is directly printed onto differing materials, interconnect dimensions may be limited by the physical properties of both the interconnect and the underlying substrates. For example larger, thicker interconnects printed onto substrates with wildly differing coefficients of thermal expansion may result in cracking of the interconnects.

### The non-contact direct printing process

Non-contact direct printing (**Figure 4**) begins with the atomization of an ink, usually consisting of conductive particles ideally less than 500nm, suspended in a liquid solvent forming a colloidal suspension <500cP in viscosity. The suspension is then atomized into a dense aerosol via different atomization methods, producing a dense aerosol of droplets with diameters in the 2-5 $\mu\text{m}$  range.

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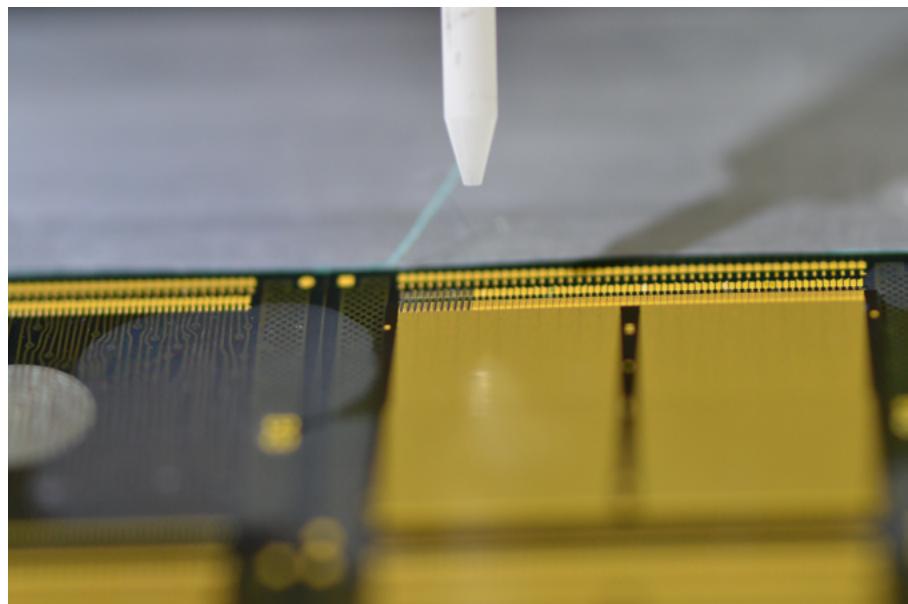


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The dense aerosol is transported by a conditioned gas to the print head where a focusing sheath gas is introduced to collimate and accelerate the aerosol down onto the substrate. This collimation process takes place by forcing the aerosol and sheath gas through a converging nozzle that compresses the aerosol stream. The jet of droplets exits the print head at high velocity ( $>50\text{m/s}$ ) and impinges upon the substrate, adhering to its surface and producing a fine line of conductive ink. The high velocity of the print stream enables an amazingly high stand-off distance of up to 5mm, greatly relaxing the fixturing requirements in the Z-dimension. This feature also allows for conformal printing on non-planar surfaces, such as stacked ICs or chip-on-board interconnects. There is a shutter mechanism built into the print head to pause printing as directed by the controller unit.

Continuing with the discussion above, electrical interconnects or other circuit patterns are then printed onto the substrate by means of precision multi-axis motion controllers and drive equipment in up to five axes of motion, depending on the application requirements. Any arbitrary



**Figure 5:** Optomec Aerosol Jet printing on a stacked die with  $60\mu\text{m}$  bond pads. The figure shows  $35\mu\text{m}$  printed wires deposited via Aerosol Jet from 3+ mm off the substrate.

digitized form can be printed on planar or non-planar surfaces with print resolutions as fine as  $10\mu\text{m}$ . The printing takes place in normal production atmospheres—no special heating or pressurization of the printing volume is required.

Finally, a post-printing process is applied to sinter, dry or cure the ink to the desired electrical and mechanical properties. This usually consists of applying heat, UV light or laser light, depending on the ink and substrate materials.

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## Capabilities needed

The non-contact direct printing process needs to be capable of printing very fine features with lines as small as  $10\mu\text{m}$  at  $20\mu\text{m}$  pitch. Wider features, up to 2.5mm, should also be able to be printed. Also, the process must be able to be applied to many types of substrates including FR4, ceramics, ceramic/PTFE composites, metals, glass, plastics, Si and GaAs (Figure 5). The post-printing process is dependent upon the ink and substrate material, but can take place at room temperature using in situ UV or laser light, or may require heating.

## Summary

Wire bonds will not suddenly be replaced by printed interconnects. However, given the limitations of wire bonds in terms of both space requirements and inherent reliability, it is not surprising to see more production customers looking to printed solutions. While this article focused on space requirements and reliability concerns, the other critically important issue that needs to be addressed is the issue of electrical performance. There have been a number of studies comparing the RF performance of printed interconnects to that of wire bonding. The results show no reduction in performance in signals up through the microwave spectrum.

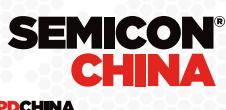
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## Background

In the late 1990s, the Defense Advanced Research Program Agency (DARPA) initiated a project to develop a new tool specifically designed for the printing of electronics. The goal of the project, named Mesoscale Integrated Conformal Electronics (MICE), was to: “Develop a single tool capable of rapid production of electronics directly from CAD [computer-aided design] models. This tool must support processing of a wide variety of materials to produce robust, customized electronic components in a conformal manner on virtually any substrate, including low-temperature (<200°C).” The new tool developed under this DARPA program was named Aerosol Jet and has been applied in hundreds of leading-edge applications across many industry segments.

There are many conventional and emerging methods available for manufacturing electronics. For the most part, these methods represent either adaptations of graphic printing methods, or new technology specifically designed for printing electronics. For many of today’s more advanced applications, new 3D manufacturing methods, such as non-contact direct printing, will be required.



## Biography

Bryan Germann is the Aerosol Jet Product Manager at Optomec Inc., St. Paul, MN. He is responsible for product management of the Aerosol Jet Platforms and print engine products, as well as strategic customer projects centered around volume production implementations of Aerosol Jet technology. He joined Optomec in mid-2017, and previously worked for GE Power where he successfully integrated several Optomec Aerosol Jet print engines for a production application involving printing high-temperature ceramic sensors on heavy-duty gas turbine blades. His background as a mechanical engineer brings a unique perspective to the Optomec marketing team as do his insights as an Optomec customer working with high-volume, precision production applications for Aerosol Jet. He currently holds 13 published patents, and BS and MS degrees in Mechanical Engineering from the U. of South Carolina (USC).

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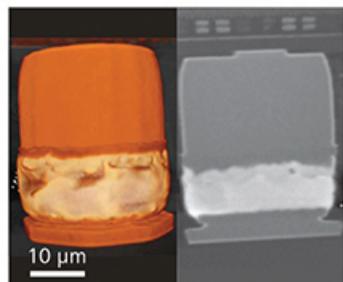
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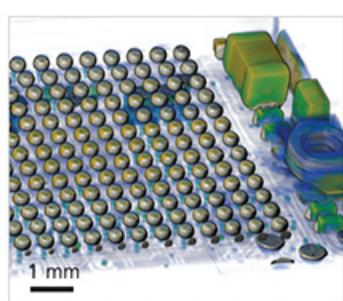
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