

ChipScale® REVIEW

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The International Magazine for the Semiconductor Packaging Industry

Volume 17, Number 4

July- August 2013

Real-Time Dispatching for Semiconductor Package Assembly P. 31

- Thin-Wafer Handling
- Integrating Diamond
- Alpha Radiation Dynamics
- Cu-Cu Direct Bonding for CTC Interconnect
- 2.5D Interposers; Organics vs. Silicon vs. Glass
- Packaging Solutions for Power Electronics
- Wafer-Level Packaging for 3D Heterogeneous Integration



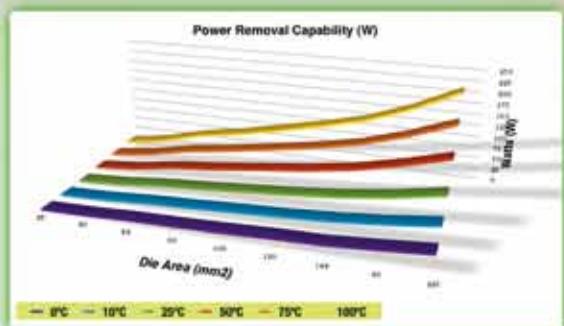
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CONTENTS

July August 2013
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This photo demonstrates the wire bonding operation in the chip assembly manufacturing process. The machine attaches lead wires to the chip. It is commonly a constraining step in the assembly manufacturing process. Technologies such as Applied Materials' dispatching software determine what chips are best to process next in real time. This has proven to increase throughput at manufacturing bottleneck steps like wire bonding. Photo courtesy of Applied Materials.

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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

FEATURE ARTICLES

2.5D Interposers; Organics vs. Silicon vs. Glass

Prof. Rao R. Tummala, *3D Systems Packaging Research Center, Georgia Institute of Technology* **18**

Cu-Cu Direct Bonding for Ultra-high Density Chip-to-Chip Interconnects

Eric Bersch, Chris Kim, Klaus Hummler, Brian Sapp, *SEMATECH* **20**

Integrating Diamond to Maximize Chip Reliability and Performance

Richard S. Balmer, Bruce Bolliger, *Element Six* **26**

Real-Time Dispatching for Semiconductor Package Assembly

Shekar Krishnaswamy, David Hannay, *Applied Materials* **31**

Alpha Radiation Dynamics in Electronics Packaging Structures

Brett M. Clark, Derek Grove, Tora Unuvar, *Honeywell Electronic Materials* **34**

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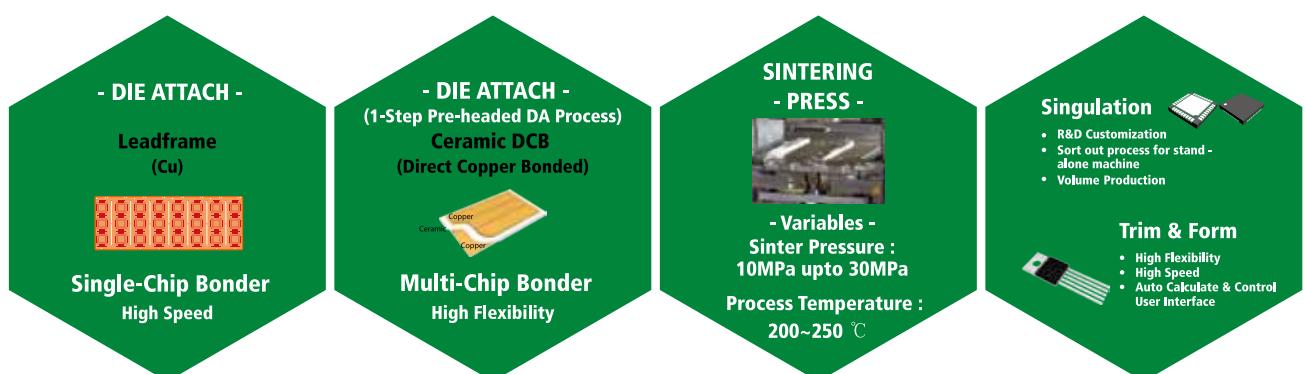
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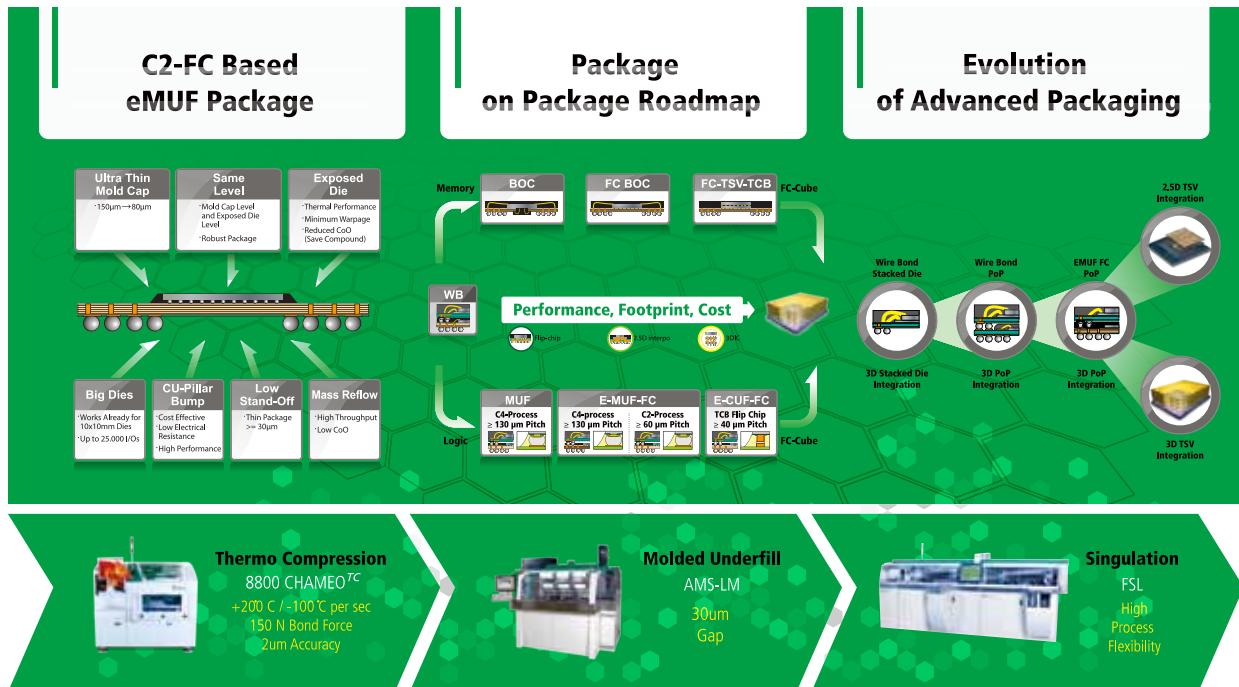
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Highlights

Thermal Compression Meets Productivity

Thermal Compression Bonding is the breaking through technology for flip chip packaging of silicon based on < 28nm nodes. It is also the enabling technology for TSV(through silicon via) for 2.5D and 3D integration.



ASEKH Announces ASE Group 2012 Best Supplier Award

BE Semiconductor Industries N.V. - Besi - is honored to be awarded the prestigious ASE Group 2012 BestSupplier Award for its Fico equipment brand.

The coveted award was presented by Mr Tien WU, COO of ASEKH Taiwan to Mr Ab CLASSEN (Director, CPM) of Besi Netherlands B.V. on March 15 2013 on the merit of Performance in the order of :-

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- Service on site support to improve machine up time.
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This award holds great significance as it bears the mark of Besi's decade-long pursuit of excellence with ASE Group - it also serves as a testament that Besi is committed to remain as the unsurpassed leader in the supplyof backend semiconductor equipment.



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FEATURE ARTICLES

Advanced Wafer-Level Packaging Technology for 3D Heterogeneous Integration	38
Seung Wook Yoon, Patrick Tang, Steve Anderson, Raj Pendse, <i>STATS ChipPAC, Inc.</i>	
Adapting an OmPP™ QFN for GaN Power Devices	43
Bill Lawrence, Steve Swendrowski, <i>Quik-Pak</i> , Greg Klowak, <i>GaN Systems</i> , Andy Longford, <i>Panda Europe</i>	
Taking Copper Wire into High-Volume Manufacturing	46
Usman Chaudhry, Willmar Subido, <i>Texas Instruments</i>	
Cost & Performance for Packaging at 28nm & Beyond	50
Bob Chylak, Ivy Qin, Patrick Desjardins, Horst Clauberg, <i>Kulicke and Soffa Ind., Inc.</i>	
Latest Insights in Thin Wafer Handling Technologies	54
Margarete Zoberbier, Stefan Lutter, <i>SUSS MicroTec</i>	

DEPARTMENTS

From the Publisher Planning for Success!	6
Kim Newman, <i>Chip Scale Review</i>	
From the Boardroom Editorial Advisory Board Update	8
Dr. Andy Mackie	
3D Market Trends Interconnectology: A System-Level Approach to Semiconductor Device Manufacturing	10
Françoise von Trapp, <i>3D InCites</i>	
MEMS Market Trends: Automotive MEMS Packaging Enables Sensor Fusion	13
Russell Shumway, Adrian Arcedera, <i>Amkor Technology</i>	
Patents: First Inventor To File: The Race Is On!	16
Jason Mirabito, <i>Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C.</i>	
Industry News	58
<i>Chip Scale Review Staff</i>	
Product News	68
<i>Chip Scale Review Staff</i>	
Advertiser Index, Advertising Sales	72

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FROM THE PUBLISHER



Planning for Success!

There comes a point in time when proper planning begins to pay off with forward momentum, which seems to push you to the next level of success. Over the course of several years, as publisher of *Chip Scale Review*, I have been involved in the planning of every stage of the business; from page layout to printing and web site development, from staffing to advisory boards, from technical editorial content to corporate advertising, and from industry events to organizational relationships.

Annual planning is typical for most companies. The CSR Editorial Calendar is revised annually and defines the upcoming editorial features scheduled for the publication. Take a moment to review the Editorial Calendar posted on our website to determine which topics are most important to your business. Identifying key topics for 2014 is already well underway. In this issue, our Editorial Advisory Board chairperson, Dr. Andy Mackie of Indium Corporation, describes the charter of the Board and some of the challenges of reporting the technologies that support the proliferation of new IC packages to meet the needs of both readers and advertisers.

Contributed editorial from Element Six on incorporating CVD diamond in IC packages for better thermal management and improved chip reliability, Honeywell on alpha-particle radiation concerns driven by shrinking device and package geometries, SUSS MicroTec on handling of thin wafers for wafer-to-wafer bonding, and Applied Materials on a software solution for real-time dispatching in IC package assembly, cover a broad range of interesting topics. Specifically related to "3D" and "copper" are contributions from STATS ChipPAC on wafer-level packaging for 3D integration, Georgia Tech on 2.5D interposer material choices, both K&S and Texas Instruments on the adoption of copper wire bonding, and SEMATECH on copper-to-copper direct bonding without solder.

When planning your advertising, pay attention to the show schedule column on our Editorial Calendar. CSR distributes the publication to the attendees of a number of worldwide events throughout the year reaching readers beyond our subscriber list. For example, *Chip Scale Review* was again pleased to be the Official Media Sponsor for ECTC 2013, the premier IEEE/CPMT technical conference and exhibition on component-level packaging and assembly. Ron Molnar of AZ Tech Direct, and CSR staff member, captures the highlights from this year's event in this issue.

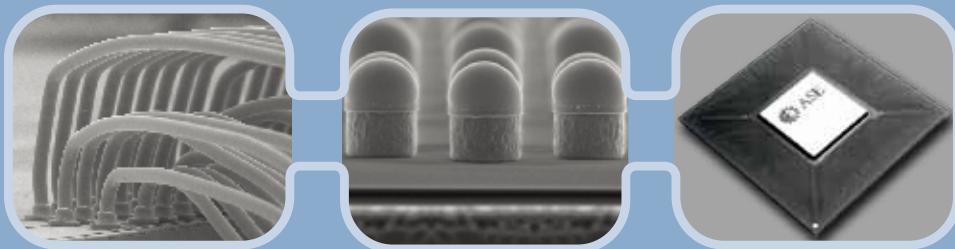
Take the opportunity to contact a member of the CSR Staff or our Editorial Advisory Board during one of the industry events, such as SEMICON West in July, or IWLPC in November, to share your industry perspectives and recommendations for our publication. I encourage our global industry colleagues and devoted readers to take full advantage of the planning efforts by our CSR Staff and Advisory Board members to promote your companies through regular editorial contributions and advertising as you plan for success!

Kim Newman
Publisher



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FROM THE BOARDROOM



Editorial Advisory Board Update

By Dr. Andy Mackie

Welcome to the SEMICON West edition of *Chip Scale Review*! As chairperson of the Editorial Advisory Board, I have been asked by publisher, Kim Newman, to write a few words about the board: who we are, what we do, and why we do it.

The “why” part is probably easiest to explain; each board member is a technical or market expert in one or more fields related to post-FEOL semiconductor processes, and each of us has a passion to share our knowledge and experience with others.

The board is tasked with guiding, and sometimes creating, the magazine’s content. Our main goal is to keep the magazine relevant and interesting to a growing global audience of engineers, materials scientists, and technical decision makers in the field of “semiconductor packaging.” It is no surprise that in reality, this term covers a broad and expanding spectrum of activities. The board is made up of consultants, market experts, and technology luminaries around the world.

For those of you who are new to semiconductor packaging (aka semiconductor assembly) - in its broadest sense, it is all about protecting a semiconductor device (the ubiquitous “chip”) and allowing it to reliably communicate to the outside world for a well-characterized period of time. Twenty-five years ago, electronics packaging referred to just die-attach. This was done mostly with wire bonding and a little flip-chip, followed by final encapsulation in a metal lid or

a polymeric material of some kind. It also included the testing and reliability that go with ensuring device utility and longevity.

The essence of these processes still remains, but the evolution of the field of semiconductors as a whole has meant that CSR magazine now has to reach an audience involved in the manufacture and testing of a huge array of device and package forms, from the tiniest transient voltage suppressor (TVS) or surface-mount zener diode (many of which will fit on the head of a match), through discrete power devices and clip-bonded die in QFN format and insulated gate bipolar transistor (IGBT) modules the size of a shoebox and operating at 1700V. Although I left electrical and thermal considerations out of this description, a thorough understanding of the materials and processes used in semiconductor packaging is increasingly important, even to those engineers involved in device modeling.

The board meets bimonthly via conference call, and we will have at least one major face-to-face meeting this year at SEMICON West. We

directly contribute written material to *Chip Scale Review*, and we also seek out and encourage others to write full-length feature articles or columns for publication. These articles may appear in either hard copy or online at www.chipscalereview.com.

Although we try to avoid any bias towards one process, company, or topic, you can help us balance our content by contacting one of the board members, or Debra Vogler (Senior Technical Editor), to contribute articles. We encourage authors to discuss topics at the cutting edge of chip-scale technology and packaging, such as implantable medical devices and the seemingly-inevitable interfacing of machine and man, while remaining firmly rooted in the question of “how are scientists and engineers going to make this work?”

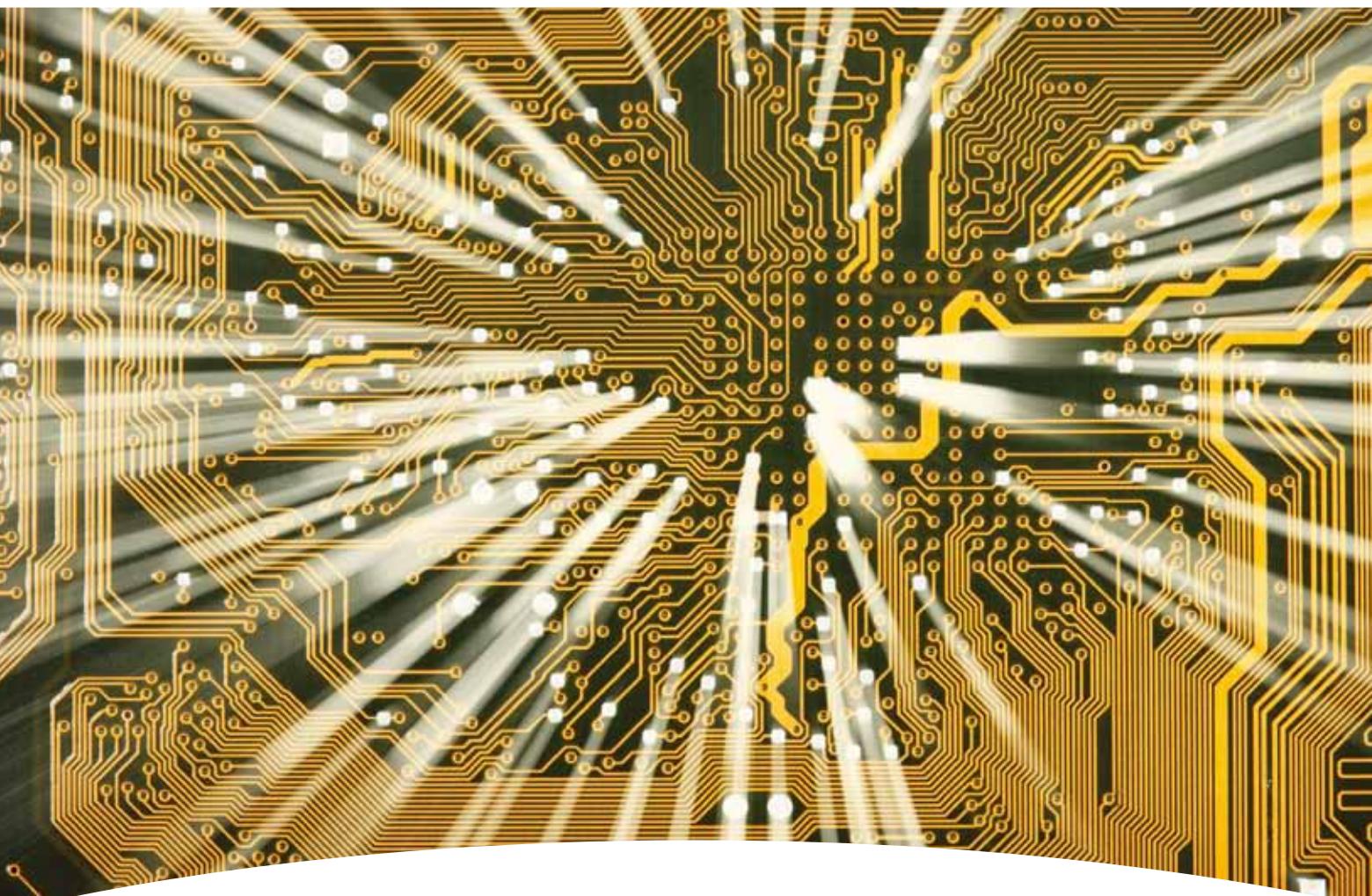
Starting with this issue, each board member will be asked to contribute an editorial (as chairperson, I get first dibs on this), and we hope that you will continue to find the magazine worthy of your time to read and for which to write. Cheers!

Andy

And the Winner Is...

I would like to take this opportunity to congratulate members of the CSR Editorial Advisory Board for recognition by the IEEE - Components, Packaging and Manufacturing Technology Society (CPMT). Among the recipients are John Lau received the 2013 IEEE "Field Award" Components, Packaging and Manufacturing Technology Award and Rolf Aschenbrenner received the "David Feldman Outstanding Contribution Award." Both were recognized and presented with these awards at the CPMT Society luncheon by the Executive Committee at the 63rd ECTC.

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3D MARKET TRENDS



Interconnectology: A System-Level Approach to Semiconductor Device Manufacturing

By Françoise von Trapp *[3D InCites]*

Introducing a new term to an industry lexicon is a task that should not be entered into lightly, particularly in an industry already overrun with made-up words and acronyms. However, as the semiconductor industry is going through a major ecosystem overhaul, elegant, novel terminology can help define that transition. A grassroots effort is now underway to introduce the terms, "interconnectology" and "interconnectologist", not to replace advanced packaging entirely, but to carve out a space for advanced interconnect as a system-level value-add, and the holistic approach needed to realize next-generation devices.

Interconnectology Defined

Interconnectology has been defined as system-level approach to the design and development of next-generation interconnect devices that adds value to the entire system architecture by positively impacting performance, form factor and power consumption. An interconnectologist understands the science of integrating expertise from chip to package to board (the value chain) in order to overcome technology barriers, optimize device performance, and accelerate the path to high value manufacturing while reducing system-level cost.

Scott Jewler, VP of Advanced Nanotechnology Solutions, Inc., is credited with coining the term "interconnectologist" as a way to describe his own particular skill set that, after years in the OSAT industry,

has evolved into an understanding that extends beyond that of merely "packaging engineer." The current problem with the terminology is that the way the industry looks at things hasn't changed, notes Jewler. As such, he applauds this effort of creating an environment where the terminology brings to mind what's actually going on in the industry.

Interconnectology and the Ecosystem

In the past, the industry took what has become known as the "over the wall" approach to design and development, where the foundry handled the local and sometimes first-level interconnects, and then handed it off to the packaging engineers to figure out the next steps. These were in the early days of wire bond and even flip-chip technologies when design margins didn't matter much. Then, explained Jewler, 130nm low-k copper dielectrics were introduced, and suddenly, wafers coming in from the foundry didn't pass reliability. "It shut down the industry. We finally hit a wall. Products got delayed," Jewler recalls. But it was a lesson clearly learned, as now all major OSATS now have upstream relationships with

the fabs, and fabless companies run fab and process engineering under the same roof.

Through-silicon via (TSV) technology has created more respect for the packaging side, notes Sitaram Arkalgud, VP of 3D Technologies at Invensas Corp. "It's much more complicated now," he notes. "We have to understand the whole science of interconnects, from the device level all the way up to the board level. You have to take into account all the factors that give you reliability, cost savings, performance benefits, and functionality. Bringing it all together is interconnectology to me."

Market Drivers

According to Ira Feldman, principal consultant, Feldman Engineering, the market drivers to support the concept of interconnectology have to do with who's driving the end products. When



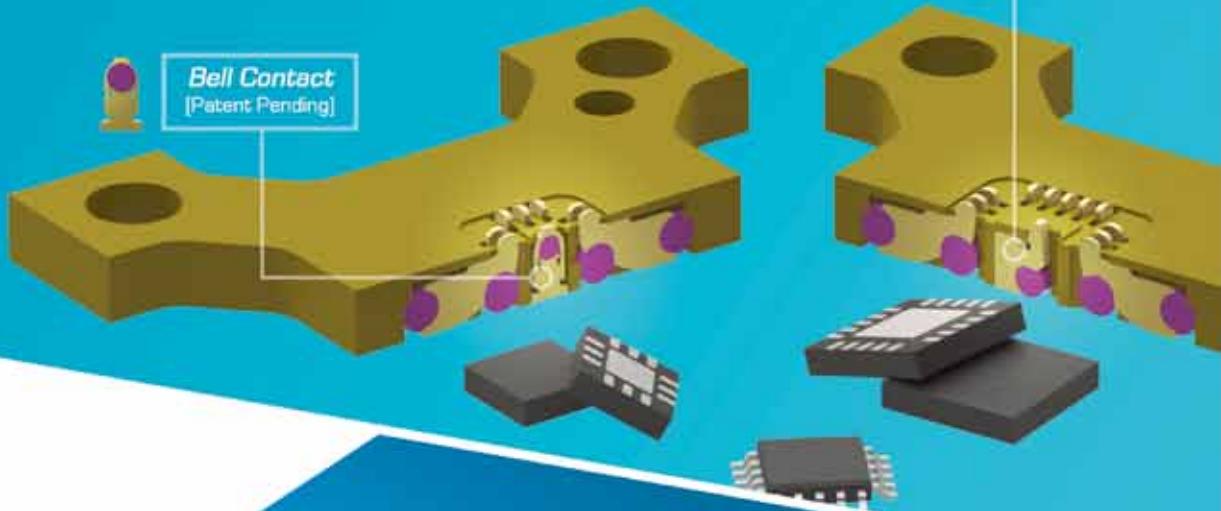
Françoise von Trapp interviewed industry experts about how they define interconnectology during a panel discussion at Bits 2013. Pictured left to right, Scott Jewler, Advanced Nanotechnology Solutions, Inc.; Sitaram Arkalgud, Invensas; and Chris Scanlon, Deca Technologies. Not pictured is Ira Feldman of Feldman Engineering Corp.



We Bring Possibilities

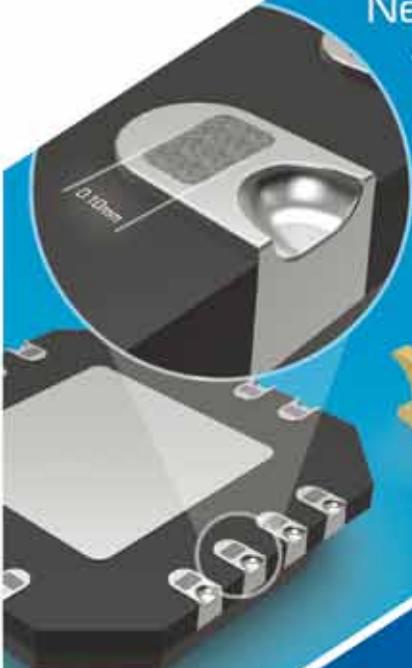
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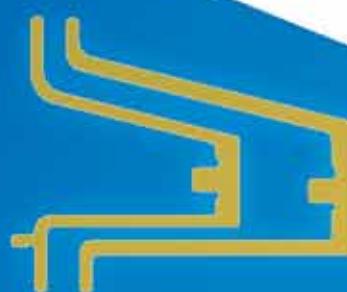
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IBM first developed the PC architecture, it controlled the form factor for circuitry and devices, explains Feldman. "Now that we're in a post-PC era, where people are differentiating processes, we need different ICs and different interconnects to be part of the solution to hit their value proposition," he said.

The real shift, notes Feldman, comes down to who is making the technology decisions. Designers no longer have to settle for what package is available. Interconnectology involves thinking across the whole product, and the product designer will define such requirements, for example, putting six die of a certain size that consume a given amount of power. An interconnectologist has the skill set to put this all together.

Does Interconnectology Replace Packaging?

"Traditional packaging steps still remain," says Jewler, "but there's a new area emerging that is the value-add and involves finer geometries that are integral to the functionality of the device." He says it really goes beyond nomenclature, and will greatly impact the next five to ten years in the semiconductor industry. Interconnectology creates opportunity for companies to integrate multiple IP and multiple process technologies to create more competitive products.

Because packaging is fragmented, it's the right space for grabbing differentiation, notes Arkalgud, but it can't be done just by developing the next clever package. "It has to be a holistic approach that says 'here's what I'm offering from an interconnect perspective, and here's how it interacts up and down the value chain. Then you have a shot at clearing a space for yourself,'" he says.

All This, From One New Word?

"Interconnectology is a powerful term," says Chris Scanlan, VP of Product Development, Deca

Technologies. "Interconnectologists have to understand the electrical, thermal, and thermo-mechanical issues—essentially all the constraints that go into designing a product involving electronic interconnect. Its more powerful than 'advanced packaging' technologist."

But beyond the nomenclature, it's the opportunity that comes with the concept. Coining a new term or terms helps to define what's happening in the industry. "You can't just do thermal or test engineering," notes Feldman. "It all needs to be interconnected across all the disciplines and areas. We have to figure out how to put pieces from multiple places in the supply chain together in ways that deliver against product requirements and the value that's needed."

Jewler says he's concerned that few young engineers are entering the packaging space. "As an integral part of More than Moore, interconnect and interconnectology needs smart young creative people to drive these solutions," he says. "Improving the name makes recruiting new college graduates more successful."

Another area in which interconnectology can prove to be useful is in driving roadmaps on what this needs to be, says Arkalgud, which allows us to be more efficient and deliver cost-saving solutions fast.

According to Larry Furman, of Plastronics, the most successful relationship his company, which manufactures test sockets for the advanced packaging sector, has had is when there's a strong co-relation with the packaging engineers. He says that until advanced packaging engineers communicate with back-end test in advance to give them time to develop the infrastructure, products will get held up. "When we're looking at the back-end infrastructure up front, that's when we can cut lead-times and deliverables to end-users." He further noted that implementing interconnectology across the supply chain provides this system-

level approach to the ecosystem that everyone is calling for, but don't know what to call it.

The Poster Child for Interconnectology

2.5D and 3D ICs represent the poster child for implementing interconnectology. Simon McElrea, CEO, Invensas, says manufacturing 2.5D and 3D devices requires more knowledge than putting vias into silicon and plating them. While the core competency to do this comes from the wafer processing industry, that's only a piece of it. It doesn't mean you'll end up with a working product. There needs to be an understanding of how to put it all together, considering reliability and thermal issues at the same time. "The job for interconnectologists begins with the TSV right up to the physical connector/module level," says McElrea. "It's more than just packaging. It requires sufficient wafer-level skills overlapping with packaging skills."

Summary

In reality, it's the lessons learned in this march toward 3D IC integration that has brought the most awareness to a system-level approach across the ecosystem. Just think how much further we might be along in commercialization of 3D ICs if interconnectology had been implemented from the beginning? Perhaps adopting it as a manufacturing approach for the next-generation of technologies – silicon photonics, for example – we can help to improve time-to-market and implement cost savings much earlier in the game. 

Biography

Françoise von Trapp, Queen of 3D, writes about emerging 3D integration technologies on 3D InCites, the online content source for 3D IC integration and 3D packaging technologies. von Trapp also contributes content and communications strategy development for Impress Labs clients in the Semiconductor Lab. She serves on the editorial advisory board for *Chip Scale Review*.

MEMS MARKET TRENDS



Automotive MEMS Packaging Enables Sensor Fusion

By Russell Shumway, Adrian Arcedera *[Amkor Technology]*

MEMS sensors were initially adopted into the commercial market by way of automobiles. Mandated fuel efficiency laws first introduced manifold and barometric pressure sensors. This was followed by driver safety measures adding accelerometers for crash detection, and gyro sensors were later added for electronic stability control and roll over detection. Applications have continued to evolve through further implementations or combinations of these key sensor types. Newly added sensors also address fuel efficiencies, driver and occupant safety, and more recently, driver assistance in passive and active sensor systems.

Automotive pressure sensor packages have always had the unique requirements of protecting the internal device and interconnect within a cavity, while also allowing external pressure to be measured through port holes into the package. Protection of the internal components can be difficult in harsh automotive mounting environments where heat, moisture, and corrosive chemicals are present and can enter through the ports. The evolution of the dedicated pressure packages has taken on many forms, from through-hole lead frame dual inline packages (DIPs) to gull-wing leads on small outline ICs (SOICs) that are surface-mount soldered, welded within modules, or act as connector push fit pins. True package standardization for this particular type of sensor in the automotive space has remained a challenge.

The earliest examples of automotive accelerometer sensors required

package-level hermetic sealing in ceramic cavities to provide a low stress environment, control of transducer damping rate often under vacuum, and protection from foreign particle contamination that could physically hinder mechanical function of the exposed transducer elements. The earliest packaging solutions of automotive inertial sensors were high grade and more costly solutions than used for common ICs. This was due in part to a developmental origin in aerospace, military or government, as well as the unique attributes and requirements inherent to inertial MEMS.

The advancement of cavity wafer bonding technology over MEMS transducers was a major step forward that later allowed transducer protection at the wafer level. This removed the sealing requirement from the package design and allowed more common over-molded surface mountable packaging, such as SOICs, to quickly become a compatible and popular platform. The sensors could then share in the high-volume manufacturing efficiencies and maturity of standard IC packages. The gyrometer sensors that entered automotive applications following this innovation benefitted by being capped and having compatibility with standard, but often lower stress, over-mold package options.

The compatibility of MEMS with standard IC packages was also made possible by intelligent design advancements of the transducer elements themselves. Many MEMS die designs have become more tolerable to direct surface exposure of nonlinear

thermo-mechanical stress coupling present in over molded IC packages. Devices with high accuracy needs, or particular sensitivities to molding compounds, have generally benefitted from low stress cavity options of a given package type formed in the common platforms described above.

Sensor Fusion in Today's Automobiles

Sensor fusion is a combination of multiple sensors working together to provide greater performance or benefit than the sum of the individual sensor devices. It is a system approach that includes both hardware and software partitioning. A key benefit is the opportunity for error cancellation and output correction by analyzing multiple sensor outputs of the same measured event. There is also decreased software complexity and reduced power consumption for computational data processing [1]. One example of automotive sensor fusion being promoted is the advanced driver assistance system (ADAS). The ADAS system shown in [Figure 1](#) enhances automobile intelligence through a combination of ultrasonic and radar sensors. The system provides awareness of objects small or large around the entire perimeter of a vehicle and increases safety through passive or active collision avoidance software functions linked to the sensory detection. The actual driver assistance functions and partitions will vary among OEM manufacturers and vehicle models.

There are examples in the market of applying optical CCD camera, IR, or inertial-based fusion systems that

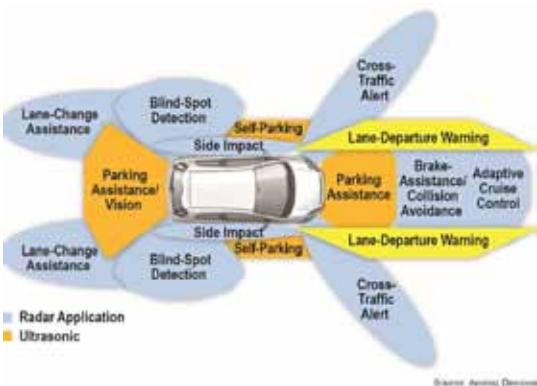


Figure 1: Advanced driver assistance system (ADAS) based on radar and ultrasonic Sensor Fusion. SOURCE: Analog Devices

similarly combine individual sensors with hardware and software selections to provide greater vehicle intelligence and safety. The microelectronic packages that are housing these sensor devices have evolved as the market volume and diversity of applications has increased. There has been a long trend of sensor integration, which occurred mainly in the past decade, such as moving from single-axis to multi-axis inertial devices, as well as the combination of similar sensor types. The fusion packaging trend should now see more heterogeneous integration of mixed sensor types.

Packaging Challenges

There are challenges to expand the flexibility of automotive packages to address the needs of these system combinations. The needs of sensor packages within a modern fusion system can either be addressed per a single sensor application or by providing combo sensor packages that allow full flexibility to mix, match and partition sensor network elements more freely. **Figure 2**

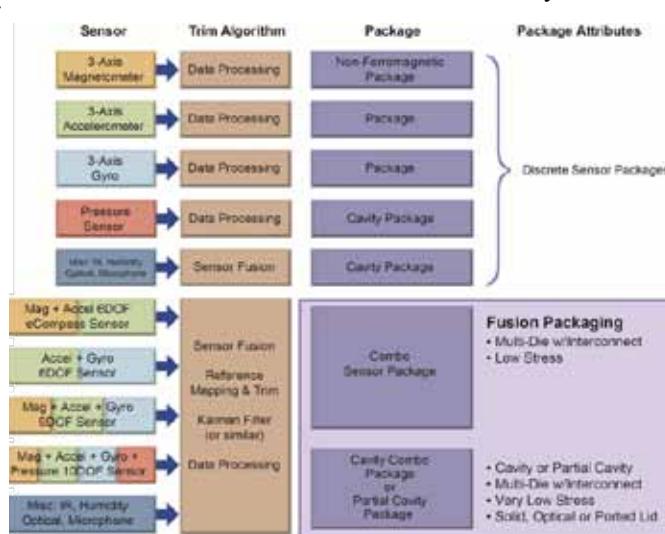


Figure 2: Amkor packaging for Sensor Fusion.

indicates how package type and attribute requirements may be categorized within the framework of combinations found in a fusion system.

Combo sensor packages will have to manage the placement and interconnect of several different die types and may include passive devices. At least a portion of the package may require a cavity with a lens or port hole cover lid allowing for acoustic, pressure, humidity or optical stimulus input to be received.

The automotive reliability expectations in terms of quality and reliability will remain unchanged. Consequently, proven platforms today should remain a popular basis for adding the integration needs. There are automotive package platforms already proven such as ChipArray® BGA, MicroLeadFrame® (MLF®), and dual lead frame (Dual LF) with SOIC or shrink small-outline package (SSOP) type packages.

Laminate-based ChipArray BGA provides a highly scalable platform basis to expand with combo sensor and cavity derivatives for less harsh mounting conditions and in cases where flexibility of routable high density interconnects are necessary. Amkor's

lead frame MLF with plated end lead option allows for visible solder joints in automated surface mount technology (SMT) inspections and enhanced board level reliability that meets automotive requirements. Consequently, the MLF platform is also a very viable platform for adding derivative forms that apply to the needs of sensor fusion packaging.

The gull wing formed leads of Dual LF provide physical standoff of the package body from the PCB board, which reduces thermo-mechanical stresses and improves stability of sensor output readings. Cavity options in this platform provide additional stress reduction to improve sensor stability and accuracy over a more broad application temperature range. Although the Dual LF is the most mature of the platforms mentioned, it is expected to remain popular because of its lower stress options and proven reliability.

Microelectronic MEMS packages have always played a critical role in the total sensor device performance by managing stress effects and allowing environmental input stimulus. With the recent advancements in semiconductor packaging, combo-packages will now take an even greater role in the partitioning of advanced multi-sensor systems.⁸

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Biographies

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First Inventor To File: The Race Is On!

By Jason Mirabito [Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C.]

In my last article in the November/December 2012 issue of *Chip Scale Review*, I focused on largely post-grant procedures available since the passage of the “America Invents Act,” known as the AIA. However, another set of changes became effective recently (March 16, 2013) and made dramatic changes for the U.S. Patent System even though, in actuality, the rest of the world had been operating on this system for many years. This change is a movement from a first to invent (FTI) to a first inventor to file (FTF) system and affects all original patent applications filed after March 16, 2013, and thus any original application filed by the time readers peruse this article.

Under the prior law, a second applicant for patent who filed an application for the same invention after a first applicant filed might be entitled to the patent if the second applicant could prove that he or she was the first inventor through the process of a somewhat complex, expensive proceeding known as an interference. In such a proceeding, the respective applicant would be required to prove first person to conceive with additional probing of reduction to practice of the invention as well as so-called due diligence from the time of invention to the time of filing or a reduction to practice. These interference proceedings were battles fought within the U.S. Patent Office and have largely been eliminated with the new law, except as described below.

Now, that is, for original applications filed after March 16, 2013, the U.S. has moved to an FTF system. Under this system, there’s no need to prove the date of invention. The interference procedure

is replaced, in part, with a so-called derivation procedure. The sole question now is who was the earliest filer at the U.S. Patent and Trademark Office. Certainly, this is a simpler system but there were, during the pendency of the legislation that became the AIA, some groups that were against adopting an FTF system, arguing that, among other things, the FTI system was “more fair” and that smaller companies would be disadvantaged. Ultimately, the U.S. Congress determined that harmonization with the rest of world would prevail and FTF became part of the AIA.

An exception to the first to file system occurs if the earlier-filed applicant can be demonstrated to have “derived” the invention from the later-filed applicant. It will be interesting to see how these derivation procedures progress and whether they become complex and expensive, but the limited scope of the derivation procedure will likely temper the expenses of this procedure.

The “old” law also had a one year “grace period” to allow the inventor to delay filing after, for example, publishing the invention in an article or making the invention public (at a trade show, for example). However, even under the old law, public disclosure or publication did and could cause problems with filing outside the United States where, for the most part, there is no such grace period. This potential disability to file overseas remains under the new law as well since it does not and cannot obviously affect foreign countries’ so-called absolute novelty statutes.

Under the AIA, a limited form of the grace period is retained for the inventor’s disclosure for a period of one year. This is not as broad as a prior

art but, again, one must be cautioned that even though one’s U.S. application may be saved, the inventor may still be prohibited from filing outside the United States. Also under the AIA, the scope of what is considered to be prior art that is applicable to an application for patent has dramatically changed and is of such importance that the next article in this series will be dedicated to the explanation of the revised prior art system.

So what are the strategies that companies might consider following in dealing with these changes? Here are several:

1) Be the first to file: this seems simple, but since you cannot rely on being the first to invent (and you really don’t know anyway) file as the old joke goes by “voting early and often.”

2) With the likelihood that you may be filing more often, consider filing provisional applications as soon as possible. There has been a lot of controversy considering the benefits and deficits of provisional applications and the simple fact that provisional applications do not get on the queue at the U.S. Patent and Trademark Office. However, given the circumstances of the new FTF provisions, it may be wise to file provisional applications and then supplement those provisional applications as time goes on and as the inventions develop and results of experimentation involved with the invention become solidified.

3) Review corporate guidelines: while in the past, the process from conception of the invention to filing potentially took many months involving: conceiving the invention, recording and describing the invention in an inventor’s notebook (more on this below),

contacting corporate resources, then contracting client's patent counsel to draft the application, drafting the application, making revisions and finally filing. Often this can take up to six months. However, at the time these were done, the inventor could rely on the belief that he or she was the first to invent and could prove, by notebooks and by counsel work, that from the date of conception to the date of filing there was so-called due diligence in getting the application on file. That procedure, as mentioned, is now gone. So it's important to find and choose counsel who can react quickly rather than putting your application, "on the pile" for eventual drafting and filing. Set short time limits for filing and stick to it and if your counsel cannot make those dates, change counsel.

4) Continue to use inventor notebooks: while some might think that it is no longer important to maintain inventors' notebooks given the first to file system and the lack of necessity to show who was the first inventor, that is not entirely true considering the existence of the new derivation proceedings. Notebook entries may be important in demonstrating that the first to file inventor derived the invention from a disclosure he or she received from the real, second filed inventor, through a notebook entry recording the disclosure to the first to file inventor. Also, the notebook entry can act as an "initiator" of the patent process as to whether to file an application quickly.

From the foregoing, and my earlier article, it is clear that the AIA has brought many changes in the basic U.S. patent law, and like it or not, these changes are now with us. In some cases, such as the first to file system, some fundamental changes need to occur in the way inventions are filed at the U.S. Patent Office. While some protested the transition to a first to file system, it is clear that the rest of the world has somehow been able to cope fairly well with it without causing the collapse of their economies. Let us hope that the

same occurs here.

Please look for upcoming articles on the AIA in subsequent issues of *Chip Scale Review*. SM

Biography

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2.5D Interposers; Organics vs. Silicon vs. Glass

By Prof. Rao R. Tummala *[3D Systems Packaging Research Center, Georgia Institute of Technology]*

Smart mobile systems are driving unparalleled packaging paradigms in system miniaturization, functionality, and cost. Unlike in the past, with a singular focus on transistor scaling and minimal advances in packaging of devices and systems, the new focus needs to be on total system scaling, system integration and system cost. But the system scaling technologies that need to be explored, developed, integrated, interconnected and tested are many. These technologies include new electrical, mechanical and thermal designs, new system substrate materials and processes, the integration of ultra-thin actives and ultra-thin passives, miniaturized and innovative thermal structures, thin-film power storages, and interconnections between all of these. These technologies need to perform a variety of circuits and system functions that range from digital, analog, RF, LED, power, bio, MEMS and network sensing. A new packaging platform is necessary—one that is driving lithographic ground rules to 1 μm and pitch to 50 μm in the short term, and 25-10 μm in the long term, at single and multi-chip levels in 2D, 2.5D and 3D. The packaging materials can be

organic, ceramic, metal, single crystal silicon, polysilicon or glass. **Figure 1** compares these materials against ideal properties and processing costs at the package level at a 25 μm bump pitch.

Organic Packages

Organic packages currently in use have four main limitations: 1) lithographic ground rules leading to low I/O pitch because of poor dimensional stability, 2) poor thermal performance because of low thermal conductivity, 3) low reliability due to a large mismatch in TCE and moisture absorption and, most importantly, 4) warpage due to low elastic modulus during substrate fabrication, chip and board-level assembly. These thermal processes lead to via misregistration from layer to layer, thus requiring large capture pads, and thereby leading to low I/O pitch. **Figure 2** shows the advances in area array pitch from a 225 μm pitch in 1987 to a 120 μm pitch now in use. To overcome these challenges, there are unprecedented global activities leading to the development of a new class of low TCE and high T_g laminate materials by changing the resin, as well as by increasing the glass content by both fiber and particle loadings. The key

question is whether this new class of low TCE and high T_g organic packages can extend to provide I/O pitch to 25 μm and below, as required for 2.5D and 3D, as well as for system scaling.

Silicon Packages

Glass and silicon packages address all of the fundamental problems mentioned above. These inorganics can be combined appropriately and selectively with ultra-thin and special polymer thin films as dielectrics, liners and stress-relief members. Silicon is the best known material in the electronics industry, primarily because of its semiconducting properties and the CMOS devices that enabled the historic billion-transistor chip. Can silicon also be an ideal material for packaging applications? Silicon has excellent properties such as surface finish, flatness, TCE and thermal conductivity. But, it has two major short comings: its electrical loss is too high for packaging applications, and it is available only up to 300mm in wafer size currently, making it costly for packaging applications. Polysilicon is available in large panel form at low cost and its electrical loss can be addressed by lining with a thick and low cost polymer liner.

Glass

Glass is the most well-known material in the display industry. It is available, for the first time, in ultra-thin, roll-to-roll sizes without having to grind and polish. This, combined with its superb electrical properties, such as its low dielectric constant and its ultra-low loss, make it an ideal candidate for packaging. Glass' low thermal conductivity can be handled selectively by utilizing a large number of low cost copper-vias, where needed. Through-via drilling was perceived to be the main problem with glass, which has been

Characteristic	Materials						
	Ideal Properties	Glass	SC Si	Poly Si	Organic	Metal	Ceramic
Electrical	▪ High resistivity ▪ Low loss	Good	Poor	Poor	Good	Poor	Good
Physical	▪ Smooth surface finish ▪ Large area availability ▪ Ultra thin	Fair	Fair	Good	Fair	Fair	Fair
Thermal	▪ High Conductivity ▪ CTE matched to Si	Fair	Good	Good	Poor	Good	Fair
Mechanical	▪ High strength ▪ High modulus	Fair	Fair	Fair	Poor	Good	Fair
Chemical	▪ Resistance to process chemicals	Good	Fair	Fair	Poor	Poor	Fair
Through Vias	▪ Low cost Via formation and metallization	Fair	Poor	Fair	Poor	Poor	Poor
Cost/mm ²	▪ Low cost per I/O at 25 μm pitch	Good	Poor	Fair	Poor	Poor	Poor

Figure 1: Comparison of package materials for bump pitch performance and cost.

largely overcome recently, by Georgia Tech and its industry partners, by at least two processes - laser and electrical

discharge - each drilling more than 1000 holes in a few seconds. Compared to FR-4, which is viewed as being the

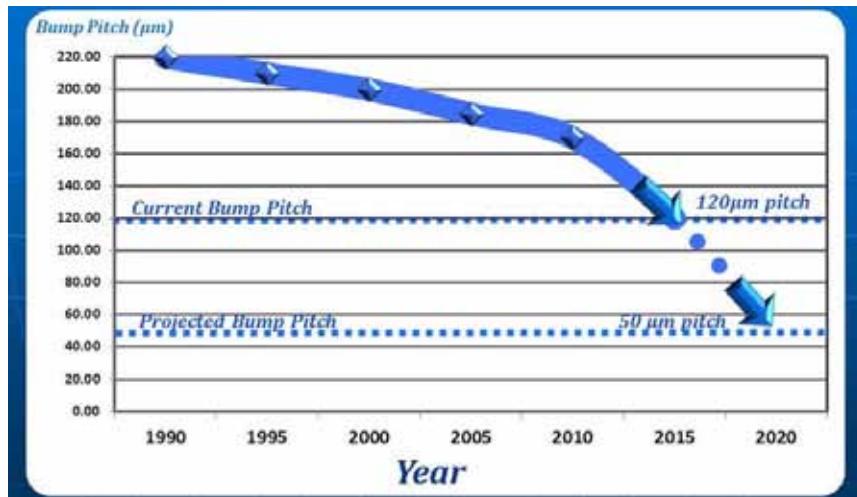


Figure 2: Potential extendibility of low TCE and high T_g organic packages.

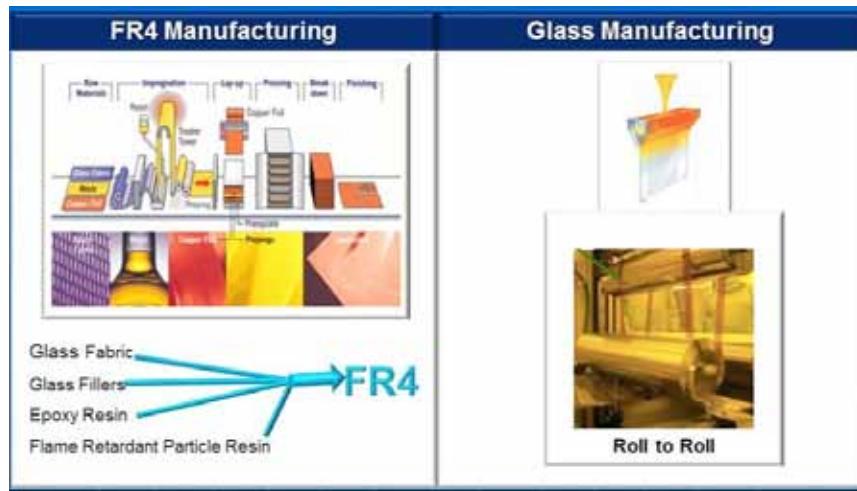


Figure 3: Simplicity and low-cost nature of glass manufacture.

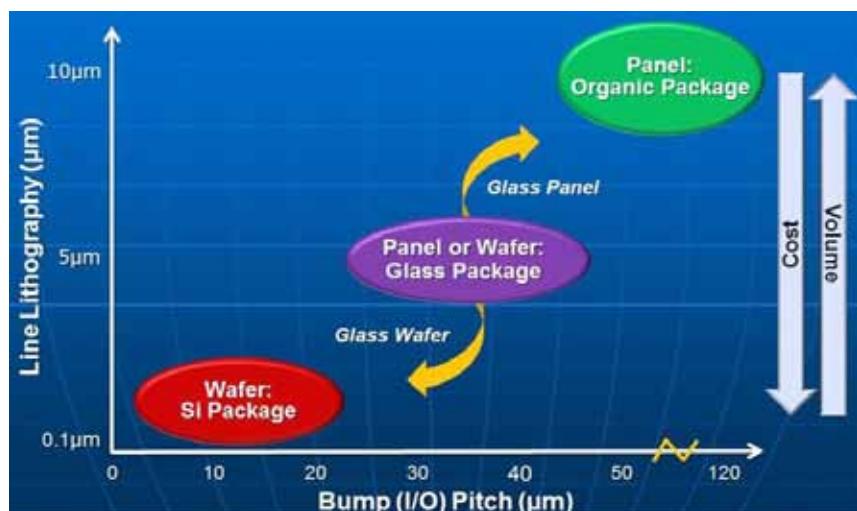


Figure 4: Three interposer options and regimes in bump pitch.

cheapest package material, glass can actually be cheaper, as can be inferred from **Figure 3**. FR-4 requires four different materials and four different processes to form one pre-preg, two of them being high temperature glassy materials, and the other two are resin and flame retardants. Glass requires only one material and one process, as drawn by the latest fusion techniques by Corning, and by similar processes by Asahi Glass and others. Glass, unlike FR-4, is isotropic which makes via formation uniform across the entire panel.

Summary

Figure 4 compares silicon, organic and glass packages for lithographic ground rules, bump I/O pitch and relative cost. The Figure shows that Si provides the smallest bump I/O pitch using wafer-based sub-micron BEOL processes, but at the highest cost. Additionally, it shows that organics provide the lowest cost at the highest bump I/O pitch using panel processes. It appears that the limits in bump pitch with organic packages can readily and quickly be extended by increasing the glass content in low TCE organics from 80% with fibers and fillers, to pure and ultra thin glass at 100%. Glass is poised, therefore, to fill the gap between sub-micron wafer-based Si lithography and 10μm panel-based organic packages. Glass can eventually be applied to both 300 and 450mm wafers in fabs thereby taking advantage of its electrical superiority over Si, and in large panel form in package foundries providing both cost and performance benefits. 

Biography

Rao R. Tummala received his PhD in Materials Science and Engineering at the U. of Illinois, and is the Joseph M. Pettit Endowed Chair in Electrical and Computer Engineering and in Materials Science and Engineering. He is also the Director of the Packaging Research Center (PRC) at the Georgia Institute of Technology. Prior to Georgia Tech, he was an IBM Fellow at IBM Corp; email rao.tummala@ece.gatech.edu

Cu-Cu Direct Bonding for Ultra-high Density Chip-to-Chip Interconnects

By Eric Bersch, Chris Kim, Klaus Hummler, Brian Sapp [SEMATECH]

In recent years, a trend to integrate more and more chips within one electronic package has emerged. This system-in-package (SiP) integration is motivated by limitation in board-level integration with respect to power, performance, cost, and space. The drivers to integrate multiple chips within one package have always been present and had previously resulted in a push towards multi-chip modules (MCMs). MCMs have been only mildly successful for higher-end systems due to cost and complexity issues. Lately, advances in packaging technology have accelerated the SiP trend by offering many innovative ways of integrating multiple chips in closer vicinity and at lower cost (flip-chip, package-on-package, wire-bonded chip stacks, embedded die packages, 2.5D and 3D chip stacking, etc.). Any successful SiP integration must solve the challenges in interconnect bandwidth, power, form factor, and cost.

Among all advances in packaging, through-silicon vias or through-substrate vias (TSVs) have by far the highest potential for improved bandwidth, reduced latency, power and size. By creating a local connection directly through the substrate, TSVs provide an inter-chip signal and power path with unbeatably short lengths and low parasitics. Leading-edge TSVs can be manufactured at very tight pitches ($10\mu\text{m}$ and below) and can therefore provide off-chip interconnects of superior parallelism. To take full advantage of the power, form factor and performance benefits of 3D chip stacking, the chip-to-chip interconnect (CCI) method of choice has to be able to keep pace with the interconnect density provided by the TSVs. Fan-out and fan-

in at the CCI interface would waste space, increase cost and compromise performance. Ultra-high density CCI (UHD-CCI) at $10\mu\text{m}$ pitch or less will be needed for full area array CCI or for locally dense interconnect buses. The 2012 update to the ITRS Interconnect roadmap (www.itrs.net) predicts CCI pitches as low as $2-3\mu\text{m}$ for the 2015-2018 timeframe. In addition, the CCI approach must support the thermal and mechanical requirements of the chip-to-chip interface.

While scaling progress is being made to finer pitches of solder-based CCI, it remains questionable if solder-based CCI will scale below $10\mu\text{m}$ pitch. Alignment issues, extrusion of solder material, thermal properties of the required underfill, and reliability issues related to the presence of inter-metallic compounds will ultimately limit the scaling of solder-based CCI.

Figure 1 shows CCI sizes and pitches published at major packaging

conferences in 2011 and 2012. Keep in mind that these are mostly research and development results, and not CCI dimensions qualified in high-volume manufacturing (HVM). The transition from solder reflow, to thermocompression (TC) bonding with solder, to Cu direct bonding without solder is evident. In the research realm, the transition to solder-less bonding currently takes place at about $10\mu\text{m}$ pitch. The timeline and pitch limit for the actual transition in HVM from solder-based interconnects to solder-less interconnects is hard to predict, because it depends on many factors such as infrastructure, cost, reliability, application drivers, etc.

Copper-Copper Direct Thermocompression Bonding

One approach to replacing solder-based CCI at pitches of $10\mu\text{m}$ or less is direct Cu-Cu thermocompression bonding (CuDB) [1,2]. In this approach,

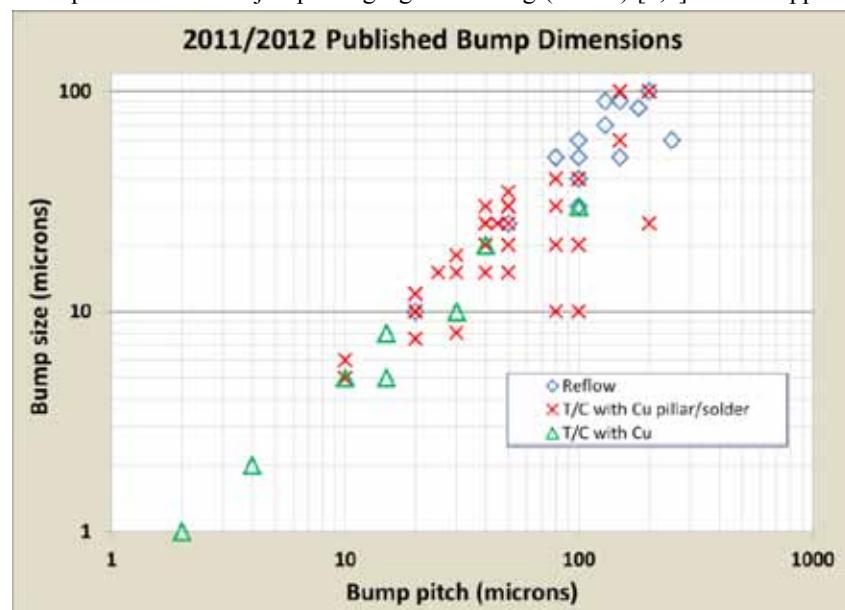


Figure 1: CCI bump sizes and pitches published at major packaging conferences in 2011 and 2012.

copper bumps or pads from one chip are connected directly to matching Cu interconnects on another chip by thermocompression bonding. Other materials may be involved to facilitate or strengthen the bond mechanically (hybrid bonding), but electrically, a copper-only connection is formed without any intermetallic compounds. Achieving the bond at low temperatures (i.e., below 200°C) is imperative for good alignment, low warpage, high throughput and compatibility with other materials like solder or underfill already present in the 3D chip stack at the time Cu-Cu direct bonding is performed. Once a good bond is achieved, its mechanical and electrical properties are virtually indistinguishable from bulk Cu properties.

Successful CuDB bonding is primarily a function of surface preparation, activation and cleaning. Methods resulting in sufficiently flat surfaces are mostly wafer processing-based. Therefore, CuDB has been practiced primarily within wafer-to-wafer or die-to-wafer assembly flows. For a truly manufacturable process flow, additional steps like passivation and depassivation have to be considered to accommodate queue or shipping times and exposure to ambient between surface preparation and bonding. Alternatively, in situ surface preparation within the bond tool can be considered. Publications about CuDB have typically focused on one or two of these necessary steps. Chemical mechanical polishing (CMP) [3, 4] and cutting using a diamond bit [5, 6] have been reported as surface preparation methods. Benzotriazole (BTA), which is typically part of any CMP process, and self-assembled monolayers [7] have been used as surface passivation methods. Depassivation, cleaning and surface activation have been performed in inert atmosphere, wet chemistry, forming gas and plasma chambers [8-11]. Ultimately, the target of these surface preparation methods is to enable a short, low-temperature initial bonding step that fixes the two die surfaces in place and results in a mechanically strong, void-free Cu-Cu bond interface.

The initial bonding step is often followed by longer batch anneals to strengthen the bond and facilitate vacancy diffusion away from the interface and Cu grain growth. Reported bond temperatures, pressures and times for the initial bond step vary widely. Most bonds were performed at temperatures between 250°C and 400°C. Due to concerns with alignment, warpage, throughput and

compatibility with solder and underfill, bond temperatures below 200°C should be targeted. To achieve high-volume manufacturing readiness, wafer-to-wafer bond times of a couple of minutes are acceptable, but for die-based assembly flows, times cannot exceed a few seconds. Acceptable bond pressures depend on the mechanical stability of the joined devices and must be kept as low as possible, especially when ultra-low-k



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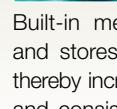
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(ULK) dielectrics are involved. If we use ULK-compatible CMP downforces as a guide, bonding downforces on the order of ~1kN for a 300mm wafer would have to be achieved.

CuDB bonding methods generally fall between two extremes of underlying fundamental mechanisms. Even poorly prepared Cu surfaces with significant roughness and some degree of oxidation or contamination can be joined at high temperatures, high pressures and long bond times. The underlying mechanisms are plastic deformation and material transport by Cu and impurity diffusion. On the other end of the spectrum are methods that result in an atomically flat surface, without any contamination or surface passivation. Once brought into contact, we can expect such a pair of surfaces to bond spontaneously at room temperature and with negligible pressure, simply due to the overlap of electron orbitals. Pursuing the latter mechanism is more likely to achieve the low temperatures, pressures and short times required for HVM CuDB. In this article, we report what role specific surface preparation methods, impurities, depassivation steps, and cleans play toward achieving a close to ideal bond scenario. For fast screening of processes, we performed most bonding studies using blanket copper 300mm wafers, and evaluated results using CSAM and 4-point bend measurements.

Experimental Details

On top of the 300mm wafers, stacks of Cu/Ta/TaN/SiO₂ (from surface to substrate) were deposited in the cleanroom at the College of Nanoscale Science and Engineering in Albany. After electrochemical deposition of the Cu films, wafers were annealed before being subjected to CMP. Then one of several cleaning procedures was applied before bonding. Most wafers were exposed to a forming gas anneal (FGA) for 6 cycles of a reference time (6 x ref). Another clean was a nitrogen anneal (NA), which was identical to the FGA but in a 100% N₂ environment. A third cleaning method was a wet chemical (WC) clean, where the wafers

were immersed in a proprietary cleaning solution and then given a spin dry before bonding. The fourth and final cleaning method was to expose the wafers to formic acid vapor for a time of 6 x ref before bonding.

Surface Contamination (XPS, CSAM)

To study the conditions of the surfaces of the wafers after cleaning, we performed X-ray photoelectron spectroscopy (XPS) on blanket Cu films that were cleaned by a forming gas anneal (FGA), a nitrogen anneal (NA), immersion in the plating chemistry (WC), or left in the CMP-last condition. The wafers that received the FGA and NA were cleaved into pieces and placed in the XPS vacuum chamber 30 minutes after cleaning. Cu 2p 3/2 spectra from a sample cleaned by a FGA, a sample cleaned by a nitrogen anneal (NA) and a CMP-last sample are shown in Figure 2a. The spectra have been normalized with respect to each other. The main peak of these spectra, centered at ~932.6eV, is primarily due to metallic Cu. Peaks due to Cu₂O and CuO are also a part of this main peak, as their binding energies are not far from those of metallic Cu (932.6eV and 933.6eV, respectively) [12], and thus they are difficult to resolve. It can be observed in Figure 2 that there is a broad feature on the high binding energy side of the spectrum from the CMP-last sample that is not present in the spectra from the samples that received the FGA and NA. This peak is due to Cu(OH)₂ and/or CuCO₃ (accepted values for these peaks are 934.6eV and 935.1eV, respectively) [12]. Thus, the FGA and NA removed the Cu(OH)₂ and/or CuCO₃ from the Cu surfaces.

Figure 2b shows the O 1s spectra from the FGA, NA, and CMP-last

samples, where the spectra are plotted in counts per second (c/s). In these spectra, the main peaks for the spectra from the FGA and NA samples occur at a binding energy of ~530.2eV. This peak is primarily due to O in Cu₂O and CuO, which have accepted binding energies of 530.4eV and 529.6eV, respectively [12]. In the spectrum from the CMP-last sample, the main peak is centered at ~531.2eV. This peak has contributions from O in Cu₂O and CuO, as well as from O in Cu(OH)₂ and CuCO₃, which have accepted binding energies of 531.5eV [12].

An important difference between the O 1s spectra from the FGA and NA samples is that the peak intensity from the NA sample is greater. This can be interpreted to show that the FGA treatment was more effective at removing the Cu₂O and CuO from the Cu surface than the NA treatment.

Figure 2c shows the N 1s spectra from the FGA, NA and CMP-last and WC samples, where the spectra are plotted in c/s. The N 1s peak on these samples is an indication of benzotriazole (BTA) on the surface. The BTA (5 methyl-1H-benzotriazole: C₇H₇N₃) was a constituent of the slurry used to polish the wafers after Cu deposition and was thus deposited on the Cu surface as a result of the CMP. As the WC sample was measured two weeks after the WC process, the Cu 2p 3/2 and O 1s spectra were not suitable for the time dependent comparisons shown in Figures 2a and 2b, but it was included in the comparison of N 1s spectra, which is time independent. It can be observed that the N 1s peaks from the FGA, NA and CMP-last samples are very similar in magnitude, showing, to a first approximation, that the FGA and NA anneals did not strongly remove BTA

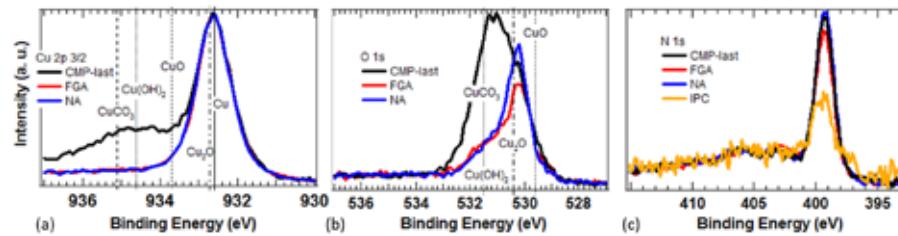


Figure 2: a) Cu 2p3/2, b) O 1s, and c) N 1s spectra from FGA, NA and CMP-last samples.

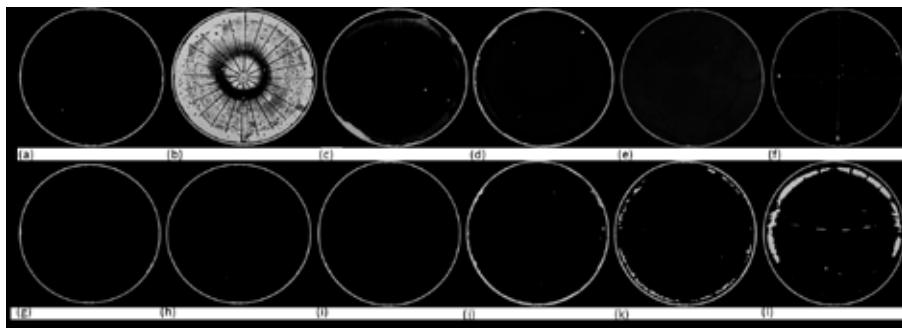


Figure 3: CSAM images from a) FGA-, b) NA- and c) WC-cleaned bonded wafers. CSAM images from Cu films grown by tool/chemistry d) 1, e) 2 and f) 3. CSAM images of wafers annealed to g) 150°C and h) 350°C. CSAM images from wafers a) cleaned with an FGA of 4X the reference value, b) bonded for 2 minutes with a downforce of 10kN, c) bonded at 180°C, and d) cleaned with a formic acid vapor treatment.

from the surface.

A closer look at these peaks shows that the area under the curve of the peak from the NA sample is 6% greater than that from the CMP-last sample. This can be explained by the hypothesis that the NA does nothing to remove the BTA on the surface, and that there is a thicker atmospheric contamination layer on the CMP-last sample than the NA sample, thus attenuating the N 1s signal from the CMP-last sample more strongly. In contrast, the area under the curve from the FGA sample is 12% less than that from the CMP-last sample. This suggests that the FGA removed a portion of the BTA. The area under the peak from the WC sample was 60% less than that from the CMP sample, showing that the WC was more effective than the FGA for BTA removal.

Figure 3 shows C-mode scanning acoustic microscope (CSAM) images from the FGA, NA and WC samples, where black within-the-wafer circumference indicates good bonding and grey indicates voiding. It is clear that the wafers cleaned by the NA did not bond well, but that those cleaned by the FGA did. It should be noted that there is a small, pin-hole void in the CSAM image for the FGA-cleaned wafers, but bonds with a small number of these voids are still considered to be successful. As the FGA treatment was shown to be more effective in removing the Cu₂O and CuO, we attribute less Cu₂O and CuO on the FGA-cleaned wafers to the better bonding of these wafers than the NA-cleaned wafers. We also note that good bonding can

be achieved with only a slight (12%) decrease in the amount of BTA on the surface, as was the case with the FGA wafers. Relatively good bonding was also achieved with the wafers given the WC clean, though there is some slight voiding near the edge. This good bonding for the WC cleaned is likely an indication that this treatment was effective at removing Cu₂O and CuO from the Cu surface. Since the WC process takes less time than the FGA process, it is a promising method for higher throughput Cu-Cu direct bonding.

Impurity Concentration (TOF-SIMS, CSAM)

Two other factors that may play a role in Cu-Cu direct bonding are the impurity concentrations at the surface and in the bulk of the Cu films. We used time of flight secondary ion mass spectrometry (TOF-SIMS) to measure depth profiles for S and Cl for Cu films grown by three different tool/chemistry combinations. Representative S and Cl depth profiles from Cu films grown by each of these tool/chemistry combinations are shown in **Figure 4**, where concentration is plotted on a log scale. In these depth profiles, it can be observed that the S and Cl concentrations decreased sharply over the top ~10nm of these films, and then were relatively constant throughout the bulks of the films. To obtain bulk values for the S and Cl concentrations, we averaged the S and Cl concentrations over depths between 50–350nm. The S and Cl surface concentrations ranged from S surface reference and Cl surface reference

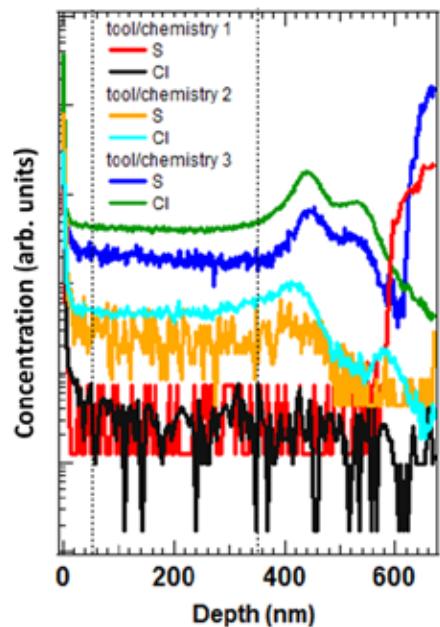
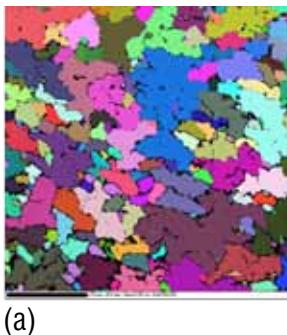


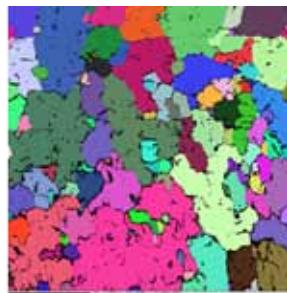
Figure 4: TOF-SIMS depth profile of tool/chemistry 1, 2 and 3.

4.4 x S surface reference and 9.4 x Cl surface reference, respectively, and the S and Cl bulk concentrations ranged from S bulk reference and Cl bulk reference to 72 x S bulk reference and 134 x Cl bulk reference, respectively. Despite these ranges of S and Cl surface and bulk concentrations, good bonds were obtained for Cu films deposited by all three tool/chemistry combinations, as can be seen in the CSAM images shown in **Figures 3d, 3e and 3f**.

Grain Size (EBSD, CSAM). In the diffusion-based model of Cu-Cu direct bonding, Cu diffusion takes place along grain boundaries [13]. By this model, a Cu film with smaller grains, which has a higher density of grain boundaries than a Cu film with larger grains, would bond more effectively. To investigate this effect, we prepared a Cu film with smaller grains and one with larger grains by annealing them at 150°C and 350°C, respectively. We performed electron backscattered diffraction (EBSD) to map the grains in the Cu films. EBSD grain maps from the 150°C and 350°C annealed Cu films are shown in **Figure 5**, which had average grain sizes of 1.9μm and 2.6μm, respectively. Despite these differences in average grain sizes, wafers that were annealed to 150°C and wafers that were annealed at 350°C were both observed to bond well.



(a)



(b)

Figure 5: EBSD images from Cu films annealed at 150°C and 350°C before CMP. The average grain sizes for these films were 1.9 μ m and 2.6 μ m, respectively.

CSAM images for wafers pairs annealed to 150°C and 350°C before CMP are shown in **Figure 3g** and **3h**.

TEM/Four-Point Bend. In addition to CSAM imaging, we used transmission electron microscopy (TEM) and four-point bend testing to evaluate the quality of the Cu-Cu bonds. TEM images from wafers bonded at 195°C and 400°C are shown in **Figures 6a** and **6b**, respectively. In both of these images, the Cu-Cu interface appears to be free from voids and is primarily a straight line. A more jagged Cu-Cu interface or one that has disappeared entirely due to grain growth is indicative of good bond strength [13], but our four-point bend results demonstrate that it is not a necessary requirement for a strong Cu-Cu bond.

We performed four-point bend tests on wafers where the CSAM images indicated defect-free bonding. A representative force vs. displacement curve from a wafer pair bonded at 195°C is shown in **Figure 6c**. The critical release energy extracted from this curve was 8J/m², which is comparable to other

critical release energies from Cu-Cu bonds reported in the literature [14]. In addition, we observed that the failure during this four-point bend and nearly all others that we performed did not occur at the Cu-Cu interface, but rather at one of the other interfaces. This was determined by performing energy dispersive spectroscopy (EDS) on the delaminated surfaces and observing that Cu was only present on one of the surfaces. This suggests that a clean, void-free, straight line Cu-Cu interface after the initial bond can provide sufficient strength and stability for 3D interconnect structures.

Varying Cleaning and Bonding Conditions. As the time involved in the typical FGA we performed is not conducive to high throughput, we tried reducing this time and observed that an FGA of 4X the reference value could also produce a void-free bond, as shown in the CSAM image in **Figure 3i**. Due to the desirability of reducing the bonding time, temperature and downforce, we investigated how far these parameters could be minimized while still achieving a successful bond. We observed that a void-free bond could be achieved with a bonding time of 2 minutes and a downforce of 10kN, as shown in **Figure 3j**. When we reduced the bonding temperature to 180°C, however, we observed edge voiding in the CSAM, as shown in **Figure 3k**. Finally, as an alternative to the FGA, we

cleaned wafers with formic acid vapor, as described above. The CSAM for wafers cleaned with formic acid before bonding, shown in **Figure 3l** indicates that this clean was not successful in producing a void-free bond.

Summary

This work shows that, with the right surface preparation, high-quality Cu-Cu bonding of 300mm wafers can be achieved at a temperature of 195°C, downforce of 10kN, and bond time of 2 minutes. These bonding conditions are close to targets compatible with high-volume manufacturing. The choice of surface cleaning and depassivation methods is a major factor, with FGA and WC cleans shown to be most effective in removing copper oxides and BTA. Larger Cu grain sizes (fewer grain boundaries) and S or Cl impurities don't seem to inhibit successful bonding. TEM and four-point bend analyses confirm that grain growth across the bond interface is not a necessary condition for a strong bond. All these findings indicate that the fundamentals of our bonding method are close to a regime of a spontaneous bond formation by overlapping atomic states rather than relying on Cu plastic deformation and Cu transport by diffusion. This suggests that it should be possible to further extend bonding conditions to even lower temperatures, pressures and durations, resulting in a highly manufacturable process. 

Acknowledgements

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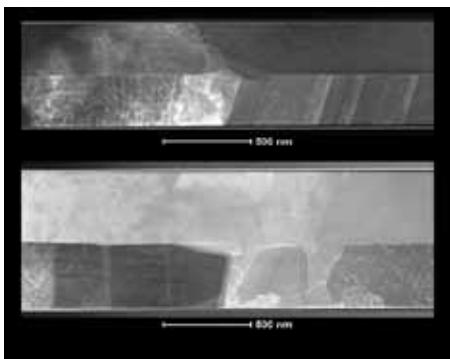
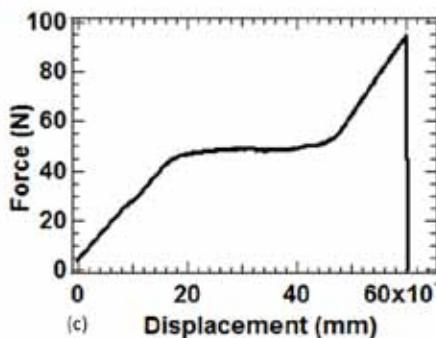


Figure 6: TEM images of Cu-Cu bonded films bonded at a) 195°C and b) 400°C; b) Four-point bend test force vs. displacement curve.



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Biography

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Integrating Diamond to Maximize Chip Reliability and Performance

By Richard S. Balmer, Bruce Bolliger [[Element Six](#)]

As semiconductors continue to follow Moore's Law, with technology nodes in mass production below 20nm, device power densities are on a trajectory to be well above 100W/cm² at 14nm (ITRS Roadmap). When combined with the need for higher power solid-state switching devices for power converters and high frequency components for cellular and satellite communications, the need to manage higher power densities and associated heat is an issue spanning all major segments of the industry.

Such power densities, using incumbent thermal interface and heat sink materials, will result in heat sinks scaling inversely to channel length as device densities increase. Naturally, this will impact the ability of device manufacturers to reduce device size, or enable higher degrees of integration and it may force designers to compromise on performance, or reduce their design thermal margins, impacting product reliability.

When determining the reliability of a packaged chip, most failure processes follow a temperature-dependent behavior. Like all Arrhenius processes, reaction rates increase with temperature. The same holds true for chip lifetime, hence every 10°C increase in junction temperature represents a 2x decrease in device lifetime. In fact, more than half of failures in today's electronic systems are due to temperature (**Figure 1**).

The quest for improved heat extraction includes higher conductivity materials compared to incumbent materials such as copper. Synthetic diamond is an interesting material for thermal management including semiconductor packaging, especially

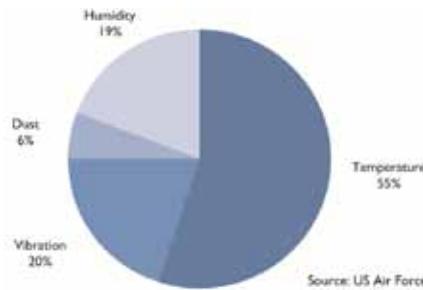


Figure 1: Failure modes in electronic systems.

for today's advanced electronic systems driving towards higher and higher power density, as it combines exceptionally high thermal conductivity with electrical isolation. In addition, for mobile and aerospace applications, diamond has the advantage of low density (3.52g/cm³) combined with its high thermal conductivity, which enables small heat spreader dimensions and makes diamond a very low-weight thermal management solution. For rugged applications, the high Young's modulus of diamond (1000 to 1100GPa) helps increase the reliability of the entire package or module. However, to maximize the effectiveness of synthetic diamond's exceptionally high thermal conductivity for thermal management of packaged chips, careful design of its integration into the package is required, particularly at the bonding interfaces.

Why CVD Diamond

For over 50 years, synthetic diamond manufactured using high pressure and high temperature techniques (HPHT) has been used for abrasive applications, exploiting its extreme hardness and wear resistance. Over the last 20 years, new methods of growth based on chemical

vapor deposition (CVD) have been commercialized to allow for the cost-effective growth of single crystal and polycrystalline diamond. The highest purity synthetic diamond is manufactured by microwave assisted CVD.

Material purity is important in synthetic diamond where heat is transmitted via phonon (vibrations in the crystal lattice) transport. In contrast, metals like copper transmit heat via free electrons that are also responsible for its electrical conductivity. In diamond, impurities act as scattering centers that hinder the transport of phonons and reduce the thermal conductivity of the material. An added benefit of microwave assisted CVD is that it is a scalable technology that deposits diamond over large areas (10–30cm in diameter) (**Figure 2a**, inset), at a cost similar to semi-insulating SiC wafers. The thermal conductivity of CVD diamond can be tailored to the application requirements (and budget), and with a room temperature conductivity that can exceed 2,000W/mK (**Figure 2a**), is 5x greater than copper (400W/mK).

Many segments of the semiconductor market, for example power converters and solid-state RF power amplifiers, are driving towards higher power densities, increasing the burden on local thermal management. CVD diamond, which combines extreme properties such as high thermal conductivity, robustness, low mass and electrical isolation, is uniquely positioned to address this need. Application examples where synthetic diamond is integrated into chip packages (**Figure 2b**) as part of a thermal management solution include:
1) An RF package consisting of discrete



THERMAL CONDUCTIVITY

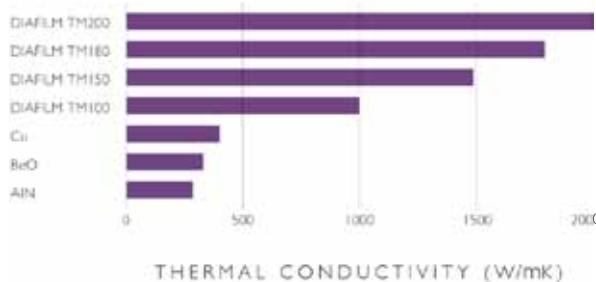


Figure 2a: Thermal conductivity of commercially available thermal grades (TM) of CVD diamond compared with alternative materials. Inset is a photograph of a 140mm CVD diamond wafer.

RF devices attached to a diamond heat spreader mounted on a CuW flange, where the diamond replaced a 1mm thick beryllium oxide (~200W/mK) heat spreader resulting in a 30% decrease in thermal resistance; 2) A laser diode array with an emitted output power of 100W from a 200W input power, where 100W is dumped as heat into the diamond heat spreader upon which the laser diode array is mounted; 3) An embedded CPU board with a processor flip-chip generating 45W of power, with the diamond mounted between the top of the flip-chip and the heat frame; and 4) A photonic integrated circuit as a heat spreader that also uses its insulator characteristics to enable two chips

within the package to be close together for better performance.

The effectiveness of CVD diamond as a heat spreader in electronic packages depends very much on how it is integrated into the package. CVD diamond can be integrated in the following two different ways: 1) Free-standing, individual CVD diamond units bonded using conventional metallization and soldering techniques; and 2) Prefabricated wafers to hold multiple devices allowing wafer-scale processing at device manufacturers (including metallization and mounting), followed by singulation of wafers to produce individual subcomponents.

uniformly distributed across the device (such as in a IGBT), or are there local hot-spots (as in the case of a GaN RF HEMT)? The mounting and interconnect technology (i.e., via holes, wire bonding, ribbon connectors, etc.); 3) The heat spreader characteristics including thermal conductivity, electrical conductivity or isolation, coefficient of thermal expansion, density (weight is important for mobile, airborne and space applications), and flatness; and 4) The average bulk thermal conductivity (of the heat spreader and thermal interface materials) and the thermal barrier resistance, which contributes to the overall thermal resistance in the heat path. These characteristics are key to integration of CVD diamond into a sub-mount package.

Thermal Expansion of CVD Diamond

When calculating the actual length change of a material from one temperature to another, it is most convenient to use the average expansion coefficient from a reference temperature to the final temperature. In other words, the linear expansion coefficient is the gradient of the change in length at a specific temperature, while the average expansion is the gradient of a straight line from the reference temperature. **Figure 3** shows a comparison of average expansion coefficient for type IIa natural diamond and silicon [1] with Element Six measurements of 32.5mm long bars of polycrystalline CVD diamond over the temperature range 25 to 1300°C.

The thermal expansion must be considered for a number of crucial reasons. While the use of CVD diamond as a heat spreader is fundamentally to lower the operating temperature of electronic and opto-electronic devices, it can also enable a higher operating output power for the same junction temperature. In either case, changes in temperature result in changes in length of materials bonded in a stack, which results in thermo-mechanical stress in the device. The magnitude of these stresses depends on the size/geometry of the device and the change in

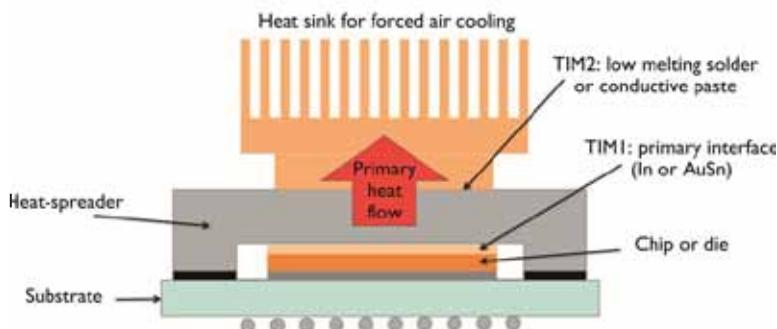
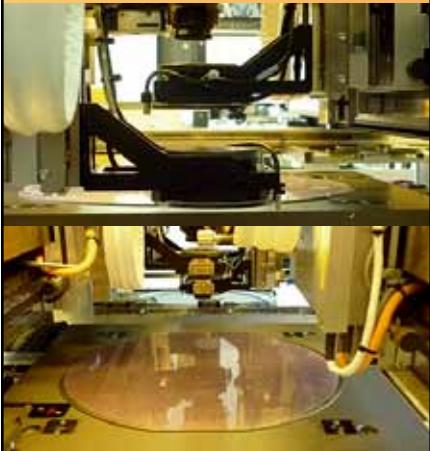


Figure 2b: Schematic diagram showing a typical sub-mount architecture incorporation of a chip (or die) and a heat spreader.

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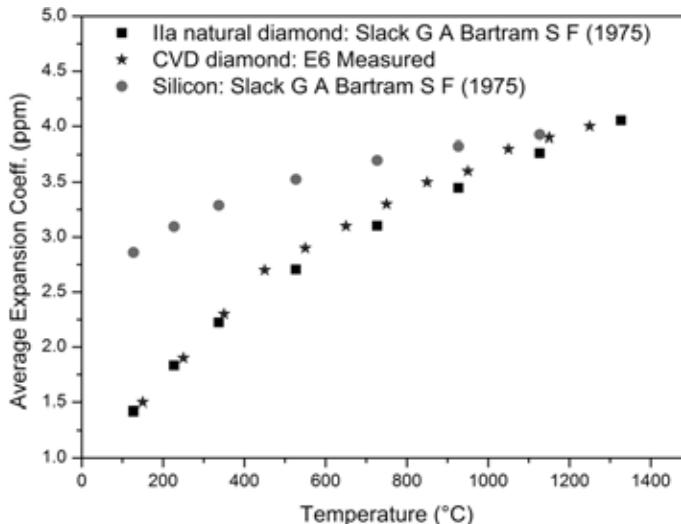


Figure 3: The average expansion coefficient of diamond and silicon calculated from the published linear expansions values and the measured values by Element Six. The reference temperature is 300K.

temperature during attachment and during operation. Unless properly managed, these stresses can alter the output of the devices (for example the output wavelength of a laser diode) or significantly impact the lifetime of the device. This latter issue is compounded if the device undergoes thermal cycling. Approaches to managing these stresses include pre-cracking the compound semiconductor [2], using a diamond sandwich, where the upper layer acts to balance stresses, or using compliant layers such as pure indium or indium compounds to attach the CVD diamond heat spreader and the device, with careful control of the thickness of such a layer to avoid increasing the overall thermal resistance.

Thermal Barrier Resistance and Average Bulk Thermal Conductivity

Two additional figures of merit for electronic packaging thermal management solutions are the thermal barrier resistance and the average bulk thermal conductivity. The thermal barrier resistance should be minimized, while the average bulk thermal conductivity is maximized. In any geometry where CVD diamond is used in thermal management, these properties come into play. In a metallized bonded approach, for example, the thickness of the metal, its thermal conductivity and interfacial thermal properties all

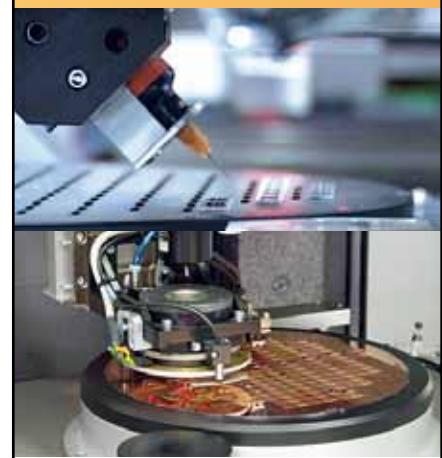
contribute to an overall thermal barrier resistance, while the average thermal conductivity then determines the heat spreading capacity, once the heat has travelled through the interface.

To minimize thermal barrier resistance, it is important to match the acoustic velocities between materials, so the best match for CVD diamond is CVD diamond. However, for a number of practical and integration reasons, compromises have to be made with the bonding material, it is therefore desirable that all other factors that contribute to thermal barrier resistance be as low as possible.

In CVD diamond, factors that contribute to the thermal barrier resistance are those that lead to scattering of phonons; intrinsic (phonon-phonon related), point defects (e.g., impurities, vacancies and sp^2 bonds) and extended defects (e.g., stacking faults, dislocations and grain boundaries). These factors and their contribution to thermal barrier resistance for various physical reasons will show a strong dependence on temperature.

Additional factors that contribute to the overall thermal barrier resistance are the thickness and conductivity of bonding metals, and the flatness of the interface. The flatness is important when bonding two materials to prevent or minimize any voids that dramatically affect the thermal resistance and the

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adhesion. Any deviation of the surfaces must be accommodated by the bonding material. If the surfaces are not flat, a greater thickness of bonding material is necessary, thus increasing the thermal resistance. CVD diamond is processed using a combination of lapidary and polishing techniques to planarize, control thickness, and apply a surface finish to the material. The average surface roughness can be controlled to $R_a < 20\text{nm}$. The flatness specification that is available is dependent on the wafer diameter and thickness. For a 100mm diameter wafer 500 μm thick, the flatness can be controlled to $< 40\mu\text{m}$. For a 10mm diameter wafer, 500 μm thick, the flatness can be controlled to $< 1\mu\text{m}$.

Metalization and Joining

CVD diamond is a chemically inert material, therefore common metals such as Au do not adhere well. To metallize CVD diamond, carbide forming materials are commonly used such as titanium, tungsten, silicon and silicides. A commonly used metallization scheme is Ti/Pt/Au. The Ti layer is key to adhesion by the formation of a carbide layer at the interface with the diamond. The thickness of the Au layer depends on the use case; for example whether it is a base layer for soldering or wire-bonding. The Pt layer serves as a barrier to Au diffusion that can result in the formation of unwanted intermetallics. The best results are achieved with sputtered coatings, where the sputtering energy can be controlled to ensure carbide formation at the Ti/diamond interface. This can be achieved also with evaporated films, by inclusion of a post-deposition anneal under the appropriate conditions.

When joining a device and CVD diamond, the joining method should be selected depending on the device material (thermal budget) and the application operating environment; for example, whether the sub-mount will be subject to significant vibration or g-forces if mounted on a vehicle, such as a car or aircraft engine, or whether it will be exposed to dust or a humid environment when deployed in the

field. A room-temperature bond can be achieved using a simple epoxy glue, however, the thermal conductivity of such materials is generally fairly low (typically 1–10W/mK), which can seriously impact the thermal barrier resistance. A metallic bond is therefore preferable, such as solder (joining temperature 100–300°C), or a thermal compression joint or diffusion bond ((joining temperature typically >450°C), or a braze (joining temperature 300–800°C). In many mechanical applications of CVD diamond, a braze such as TiCuSil or AuTa is used, because this joint has very high shear strength. However, most electronic devices would not survive the high joining temperatures associated with this type of braze technology. A common joint for mounting electronic devices for example is $\text{Au}_{0.8}\text{Sn}_{0.2}$ eutectic solder, which has a liquidus temperature of 278°C.

RF Power Amplifier Use-Case

The case for thermal management in the latest generation of GaN-based solid-state RF power amplifiers (SSPA) is compelling. The need for higher thermal conductivity substrates was identified in 2000 to minimize self-heating effects that significantly reduce peak output power [3]. While many of the reliability issues that have been a barrier to adoption for GaN-based HEMTs (high electron mobility transistor) in SSPAs have been solved, the RF performance (output power and power-added efficiency) is most often thermally limited. For emerging GaN-on-SiC devices, practical operation in a realistic PA architecture with moderate bias, the output power density is limited to around 7W/mm [4], compared to the record GaN power density value of 40W/mm measured at high bias [5]. It has recently been reported that within an individual HEMT conductive channel, the localized heat fluxes can exceed 1MW/cm² over a 150 μm wide by 0.5 μm gate, and an MMIC with 50 μm gate-to-gate spacing could experience average heat fluxes of 10kW/cm² over the transistor footprint [6, 7].

MORE THAN PRECISION

GaN-on-diamond as an integrated thermal solution has been developed in the US by Group4 Labs [8], in Japan by researchers at NTT [9] and in Europe under the European Framework 7 MORGaN program [10]. This field continues to advance under US government-funded programs. A further development under the MORGaN program was the demonstration of a 160W power amplifier with optimized thermal management incorporating CVD diamond [11]. This report describes the fabrication of a microwave power amplifier that operates at 2GHz using InAlN/GaN/SiC HEMT technology. With a gate periphery of 36mm, the power chip reached an output power of 160W in pulsed mode, and 105W in continuous wave (CW) mode, due to the optimized thermal management. Two architectures were compared, the case with the HEMT on a 400 μ m SiC substrate, and the case with the SiC thinned to 100 μ m and soldered to a 250 μ m thick CVD diamond heat spreader. During CW operation, the power chip dissipates 140W, which in the first case results in a maximum junction temperature of around 260°C. With the combination of thinner SiC, and the CVD diamond heat spreader in the second case, maximum junction temperature is only 200°C, as shown in **Figure 4**.

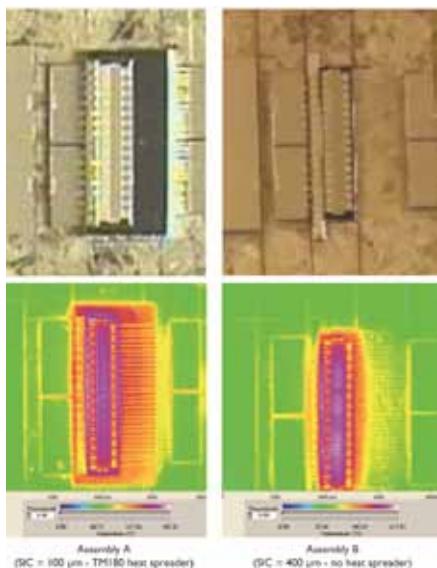


Figure 4: Optical and thermal image of InAlN/GaN/SiC power chip with a) 100 μ m SiC and TM180 CVD diamond heat spreader, and b) 400 μ m SiC.

Summary

With power densities increasing toward 100W/cm², the need for thermal management is accelerating across much of the semiconductor industry. High power RF chips and laser diodes are good examples of applications requiring careful thermal management. CVD diamond, with its very high thermal conductivity, 5x that of copper, combined with its insulating property, low density, and high stiffness characteristics, is an attractive thermal management solution in many of these very high power density applications. However, careful design of the CVD diamond heat spreader's integration into the semiconductor package is required to optimize its thermal management effectiveness. With appropriate attention to differences in thermal expansion, design of the bonding interfaces, and metallization and joining processes, CVD diamond can significantly lower junction temperatures, thereby enabling much longer chip lifetime and/or higher performance. 

Acknowledgment

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Real-Time Dispatching for Semiconductor Package Assembly

By Shekar Krishnaswamy, David Hanny [[Applied Materials](#)]

In semiconductor package assembly, the wire-bond operation is a significant step. Any medium to large-size factory includes hundreds to thousands of wire bond machines. Because of the increasing complexity of packages with increasing lead and wire counts, a product lot spends more processing time in wire bond than other assembly operations. This typically drives wire bonding equipment to be an assembly manufacturing bottleneck [1].

The continuous evolution of products and the migration from integrated device manufacturers (IDMs) to outsourced assembly and test services (OSATs) requires that numerous packaging technologies co-exist in the same factory. This requirement creates additional operational complexities that impact equipment and factory productivity. More importantly, it often adversely impacts customer delivery performance. In the past, the product, technology, equipment, and customer matrix was simple enough for human decision making to manage and operate the wire bond process. These challenges, coupled with the growing need to provide and use suitable data, dictate timely, accurate, consistent, and scalable operational decision-making to ensure high customer delivery performance.

Additional Package Assembly Challenges

As assembly factories have undergone major advancements, the evolution of semiconductor products has led to an explosive number of product and part types. This evolution has spawned numerous challenges associated with

capability imbalances, setups, and data management.

Managing Imbalances in Capability. First, with more factories being consolidated into larger factories, the diversity of equipment models, particularly in wire bond, has increased considerably. This diversity is in areas such as: 1) Degree of automation (manual, semi-automated, and automated); 2) Product type capability; 3) Wire/pad pitch capability; and 4) Wire type and size capability.

Even among machines with a similar capability for these characteristics, disparities exist in reliability, processing speed, and quality. If not comprehended accurately, this inherent imbalance in capability causes problems in tactical planning.

The next challenge is the execution of the plan at the shop floor level. A major IDM has reported a drop in wire bond tool utilization by about 13% (68% actual utilization vs. 81% planned utilization) [2].

Managing Setups. A second challenge is managing setups or product changeovers. The wire bond setup operation is complex, tedious, and iterative. Although the objective of factories is to achieve a successful first pass setup, success often follows only after a few iterations. This constraint causes long setup durations (typically in hours) that require a significant amount of technician time. The result is lost product because time and units are consumed during the setup operation.

Typically, the planning process assumes a certain number of setups per machine per week. What is commonly missed during the planning process

is that certain setups are sequence-dependent and will positively or negatively impact the productive time on the machine. As a result, the planned number of setups or the planned setup time is often exceeded. Product priority changes, quality problems, unscheduled equipment downtime, improper product routing, and so forth can cause more setups to the machines than the plan recommends. Such changes require two-way communication—manufacturing knowing the setup quota from planning and planning obtaining feedback when this quota has been exceeded so that future plans can be adjusted accordingly.

Managing Data. The third challenge relates with data complexity. Typically, data sources in manufacturing are diverse and include factory systems such as: 1) Manufacturing execution systems (MES); 2) Engineering systems for product specifications and equipment capabilities; 3) Industrial engineering systems for processing times and equipment setup times; and 4) Enterprise resource planning (ERP) systems for product demand and supply volumes.

With this diversity, it is becoming more challenging to quickly gather all needed data for timely decisions. Shortcuts include using stale data or examining data on processing equipment less frequently and using highly aggregated data. Such shortcuts impact the ability to deliver the right quantity of product on time to end users.

Managing Changes in Assumptions. Finally, the influence of factory dynamics cannot be understated. Even if good plans are developed, good execution mechanisms are in place, and data is aggregated from multiple

sources, the process breaks when changes in assumptions are not understood and operational adjustments are not properly executed. Example scenarios include product holds, equipment downs, product priority changes, non-availability of peripheral resources like paddles/clamps, and so forth.

Dispatching Requirements for Package Assembly

The complexities of package assembly have increased significantly over the years; achieving high end user satisfaction with on-time delivery and cost competitive products is a primary objective. Manufacturing scheduling and dispatching are proven systems that contribute towards meeting these objectives. However, current methodologies of manual planning and execution will not achieve these goals. The effects of factory and customer dynamics are so large that manual methods characterized by data latency, human latency, human variability,

and errors cannot compete for long. Moreover, such manual methods do not scale in a cost efficient manner with changes in product mix, volume, technology, and factory sizes.

Solutions are therefore needed that enable factories to be nimble with fast decision making. Solutions must not only be accurate, but must execute quickly and seamlessly. Obtaining real-time data aggregated from manufacturing, engineering, and planning systems is a necessity. In addition, solutions must easily capture business rules and provide useful information to all manufacturing stakeholders. Mission critical requirements include:

Reporting and Business Rules Representation. A successful planning and scheduling solution must provide data management and data transformation functions so that planners can create weekly, daily, or even per shift plans. The data management functions must have access to real-time

data so that operational changes can be made as needed.

Dispatching and Scheduling Execution.

After a good plan is created, a mechanism to execute to plan must be provided. The solution's execution mechanism must be systematic and not prone to variability in human latency. This means that it must be integrated with factory MES transactions. The results of material processing decisions must align with the plan where the same business logic used to generate the plan are used in the dispatching and scheduling function. In addition, shop floor and equipment specific considerations must be incorporated so that overall factory objectives are balanced with practical operating constraints.

Real-time Data Access and Representation.

Because the factory floor is dynamic, real-time data must be used in the decision-making. The lack of real-time data renders decisions ineffective and makes the planning and scheduling functions less credible. This promotes circumventing system logic by humans leading to higher manufacturing variability. In addition, real-time feedback is necessary to the ERP and planning functions for better planning.

Change Management. A successful planning and scheduling solution must be implemented with minimal impact on business processes and shop floor end users. Many good systems fail because they are implemented as add-on functions to existing business processes. Other important aspects are managing changes in business logic and the availability of data sources. Such changes must be implemented with minimal reliance on complex coding and the expertise of additional IT personnel.

Compliance monitoring. A system is effective only to its degree of use. A planning and scheduling solution must therefore enable usage to be monitored for effectiveness. This supports consistent system execution and reduction in variability. If operators don't follow dispatch decisions, it may indicate inherent flaws in business logic. Such measurement of operator

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Clearly, meeting all these disparate requirements for the semiconductor assembly, test, and package industry is a tall order. These requirements, however, have been addressed by the Applied APF RTD and Reporter. This solution can be deployed in factories quickly to provide real-time reporting and dispatch capability to enhance factory operations. Tight integration capability is provided to key factory data sources with standard offerings for well-known leading edge MES, as well as custom capability for integrating to in-house MES and database systems. Among the capabilities provided are: 1) Rules-based dispatching; 2) Real-time reporting; 3) Data integration and storage; and 4) Analysis and animation using temporal data.

Production planners using APF RTD can optimize dispatch decisions and improve asset utilization, which drive greater returns on investment and profitability. Factory performance increases, reported publicly by customers using APF RTD, are listed in **Table 1**.

Summary

Real-time data access, rules-based dispatching, real-time reporting, and scheduling for reacting to changes as they occur are important to semiconductor assembly, test, and packaging end users. Developed and deployed at over 200 factories worldwide, the APF RTD solution has incorporated these requirements and successfully demonstrated bottleneck

capacity and cycle time improvements. Production planners using this solution have optimized dispatch decisions and improved asset utilization, driving greater returns on investment and profitability. ³

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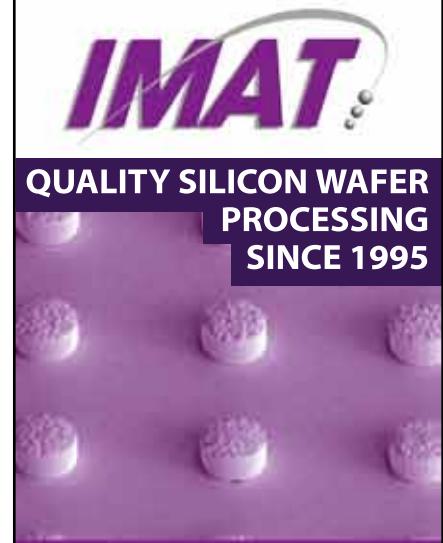
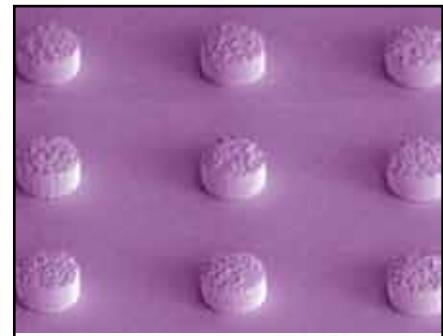
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Biography

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Fab Type	Results
High volume OSAT	<ul style="list-style-type: none"> Increased wire bond OEE by nearly 30%. Significantly reduced setups. Reduced the need for high capability operators through automated decision making. Reduced the training and assimilation of new operators.
High volume IDM	<ul style="list-style-type: none"> Increased customer delivery performance through the availability of real-time data and with reduced data latency and better business rules representation in APF RTD.³

Table 1: Results of factories using APF RTD and Reporter.



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Alpha Radiation Dynamics in Electronics Packaging Structures

By Brett M. Clark, Derek Grove, Tora Unuvar *[Honeywell Electronic Materials]*

Alpha radiation emissions from IC packaging materials have become a greater concern as device geometries continue to decrease, design complexity increases, and critical charge Q_c thresholds become lower. The trend towards flip-chip and 3D-IC architecture, in particular, has increased the need for packaging materials with alpha radiation levels several orders of magnitude below ambient. Packaging structures, including wafer-level solder bumps and copper pillar solder caps, are being placed in closer proximity relative to device transistors. This, coupled with continuously increasing transistor densities, potentially increases device vulnerability to alpha emissions from these features and can lead to increased soft error upset (SEU) rates.

The transition to Pb-free, Sn-based interconnect solder materials for many applications has not eliminated the possibility of significant levels of alpha emission from tin. Recent literature reports substantial alpha emission from high purity Sn solder bumps, indicating that high purity lead-free materials do not necessarily meet demanding alpha emission specifications [1]. Additional research at Honeywell confirmed the observation of alpha emission from some high purity tin significantly above the current industry specification of $2 \text{ } \alpha \cdot \text{hr}^{-1} \cdot \text{cm}^{-2}$ [2]. The cause of the emission was identified as the trace contaminant ^{210}Pb , which is present in concentrations less than 10^{-18} g/g . ^{210}Pb beta decays to form ^{210}Po , which decays by the emission of a 5.3 MeV alpha with a half life of 138 days. Removing impurities at this level represents a significant challenge, in part due to the difficulty of measuring the species of

interest. Contaminates in this attogram/gram concentration regime are beyond analytical instrument capabilities, and can only be measured by specialized low background radiation counters.

Recently, diffusion of ^{210}Po through high purity tin was documented for the first time. Experiments measured the increase of surface ^{210}Po alpha emission as a function of time and temperature, and demonstrated that diffusion at 200°C was a factor of ~240 greater than at room temperature. The mobility of this element and the possibility to accumulate at interfaces presents an entirely new list of questions regarding the true radiation dose to which sensitive nodes are exposed and the change of that dose with respect to temperature and time. These data challenge assumptions regarding the static nature of radiation sources and suggest that further investigation into potential impacts on SEU is warranted. In this article, we propose potential changes in alpha radiation exposure experienced by ICs due to these mechanisms.

Packaging Overview and Applications

Electronics packaging strategies have evolved with the IC technology trends to support increasingly demanding interconnect challenges. Those challenges include increasing interconnect count while decreasing geometry, and changing from lead-containing solders to lead-free solders. Future demands include increasing trends toward flip chip configurations and implementation of 2.5 and 3D packaging required by device miniaturization.

These trends, coupled with the inexorable march of Moore's Law pushing transistor density higher, have a

potential dual impact on reliability. First, the increasing number of transistors per unit area (and the associated decrease in Q_c) increases the number of targets for emitted alpha particles to strike. Second, the proximity of the sensitive nodes with respect to the sources of alpha emitters in general decreases with each technology iteration. The dual effect of increasing the number of targets and decreasing the range between the source and targets increases the probability of alpha-induced SEU events.

Microsegregation Effects on Alpha Distribution

Recent research reported evidence of non uniform distribution of trace alpha emitters in tin [2]. This observation is consistent with the phenomenon of microsegregation. Microsegregation occurs in solid/liquid systems where trace element solutes partition between liquid and solid phases according to the partition coefficient K. As solidification occurs, trace elements, for which $K < 1$, increase in concentration in the liquid phase. The result is an elemental gradient between the first solidification volume (i.e., surfaces) and the final volume (approximate center of mass), with the magnitude of the gradient directly proportional to solute concentration. Microsegregation is commonly observed in alloy systems and can lead to gradients on the order of 10x [2].

Microsegregation is present in all solid/liquid systems, and the extent to which it is present is proportional to solidification time. Therefore, cool down cycles longer than a minute in reflow processes will most likely result in microsegregation within the bumps. Processes utilizing solid/liquid phase transitions, including solder forming

and reflow processes, will be subject to microsegregation. The result is that trace alpha emitting species will be concentrated on the interior of a volume. The alpha particle will not escape with sufficient energy to cause a soft error if the position of the emitters inside a structure is deeper than the alpha particle range (16 μ m in tin for a 5.3MeV alpha particle). The converse of this statement is that the alpha particles will not be initially detected in the material, and any direct measurements will underestimate the true concentration of alpha emitting species in the material. This would be an acceptable risk, and even be advantageous, if the emitter position was static, and thus was shielded inside the structure.

If a concentration gradient is present, however, polonium will diffuse to minimize the gradient. This diffusion in tin has been documented to occur at a rate estimated to be 2×10^{-25} mol \cdot m $^{-2}\cdot$ s $^{-1}$ at 293K, and 4.5×10^{-23} mol \cdot m $^{-2}\cdot$ s $^{-1}$ at 473K [2]. The result will be a uniform concentration across the volume, but will also effectively increase the alpha emission from the volume by transporting emitters previously shielded to a depth less than 16 μ m from which they can escape. The actual emission from the structure will depend on the specific geometry as well as the concentration and degree of microsegregation in the material.

Figure 1 displays this theoretical distribution pictorially. Initially, the lead and polonium distribution is concentrated on the interior volume by microsegregation. The initial alpha emission will be relatively small due to self-shielding effects. The ^{210}Pb parent concentration will be 160x the ^{210}Po content. In addition, Pb does not exhibit the same mobility as Po, and maintains its initial distribution while polonium begins to diffuse. The result is a Pb reservoir inside a structure that will continuously generate Po, which will proceed to diffuse uniformly across the structure. This will result in an increase in the number of alpha emitters within the escape volume at steady state, and a corresponding increase in alpha

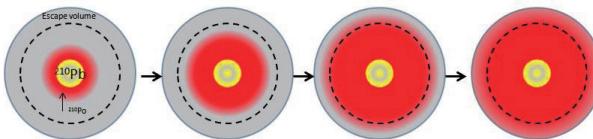


Figure 1: Microsegregation and diffusion effects on Pb and Po distribution in a solder sphere.

particles escaping from the solder.

Since diffusion is a function of temperature, device temperature will impact the diffusion rate. For devices

at ambient temperature, application of power to the device/chip will result in a temperature increase, which will in turn increase the diffusion rate of Po sequestered inside a

structure to a volume. In this scenario, there is a possible linkage between the alpha emission and SEU rate with changes in operating temperature.

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Research has demonstrated that diffusion at 473K reaches a maximum within two hours in tin 0.8mm thick. Therefore, any increase in alpha emission from a typical solder structure as a function of temperature would be within a short time frame.

Hypothetical Case: Solder Bump Radiation Dynamics

The theoretical alpha emission from a tin solder bump with 1000 polonium atoms per gram is calculated from:

$$\alpha(\text{counts } \text{x} \text{hr}^{-1} \text{cm}^{-2}) = \frac{1000 V_{\text{eff}} \rho_{\text{Sn}} \lambda_{\text{Po}}}{\eta}$$

Eq. 1

where λ_{Po} is the polonium decay rate, V_{eff} is the effective emission volume, ρ_{Sn} is the density of tin, and η is a geometric factor to account for isotropic emission. V_{eff} is calculated from:

$$V_{\text{eff}} = \frac{4}{3}\pi(r_{\text{sphere}} - 16\mu\text{m})^3$$

Eq. 2

The effective emission volume represents that fraction of the volume that is within the escape depth of the surface. For bumps less than $16\mu\text{m}$ in diameter, essentially any alpha particle emitted at any angle will escape from the volume. For bumps larger than $16\mu\text{m}$ diameter, the effective volume is less than the total volume.

Consider the case of a $30\mu\text{m}$ solder bump manufactured from tin that contains 1000 polonium atoms per gram. The difference in concentration between the surface and the concentration at a depth of $100\mu\text{m}$ was reported to approach an order of magnitude with the distribution linear along the solidification axis [2]. In the case of microsegregation in a spherical geometry, the trace contaminants (including ^{210}Pb and ^{210}Po) will be concentrated in the center of mass, with the resultant radial distribution displayed in **Figure 2**. The alpha emission from the sphere will be from the escape depth. Given the initial distribution, the Po concentration (and

hence alpha emission) in this region is significantly smaller than the rest of the volume. When diffusion drives the distribution to a uniform state as shown in **Figure 2**, the polonium concentration in the escape volume increases as represented by δ . For this example, the alpha emissivity increases by a factor of 2.

The alpha emissivity versus sphere diameter is displayed in **Figure 3**, and was calculated, again, assuming 1000 polonium atoms per gram. The emissivity scales with sphere surface area as expected, increasing as $3/r$ with the sphere diameter. If alpha emission from spheres is a concern, this indicates that, to the extent possible, there are advantages to minimizing sphere diameter. Applying this principle more generally, the smaller the solder

volumes used in packaging, the lower the expected alpha emission.

Mitigation Strategies for Dynamic Alpha Emission

The specific alpha emission dynamics will vary depending on the specific system/device geometry and operational parameters, but some possible guidance for mitigating these effects is suggested. First, deposition processes lacking solid/liquid transitions (ECD, PVD, CVD) do not experience microsegregation. Material deposited by these processes is initially gradient free, and therefore not subject to diffusion induced alpha radiation increase. However, these processes do not, by themselves, guarantee low alpha emissivity from the deposited material.

The quality of the deposited material is also a critical factor. In addition, many packaging processes utilize elevated temperatures after deposition steps. The potential to induce microsegregation effects may be considered when selecting processing temperatures. The most direct solution to the problem is to utilize solder materials sufficiently low in alpha emissivity that any diffusion effects are insignificant.

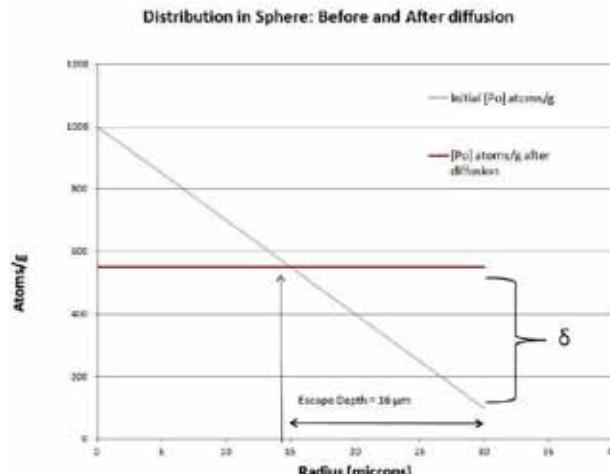


Figure 2: Distribution of polonium and lead in sphere before and after diffusion.

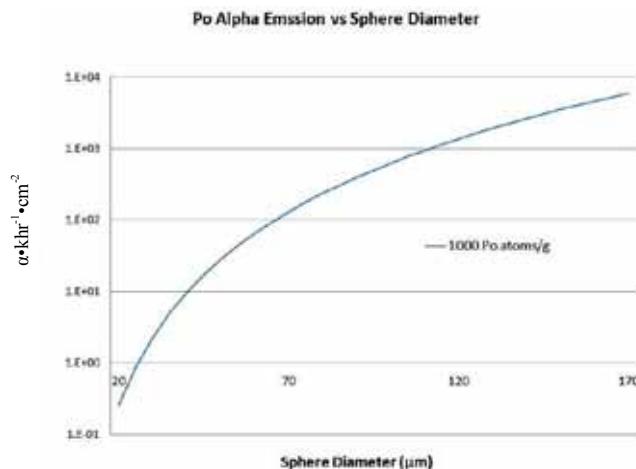


Figure 3: Alpha emissivity from sphere as a function of sphere diameter.

Summary

With the confirmation of microsegregation of contaminants in the ultra trace concentration range, potential impacts should be explored. Microsegregation impacts distribution of alpha emitters on a micron scale in packaging materials, and in some cases may cause delayed

alpha emissions from solder structures that exceed the initial emissivity by an order of magnitude. Polonium has been shown to be agile within tin solder materials, and further research is being directed to ascertain dynamics in more complex systems. The most direct solution is to utilize consistently low alpha solder materials to remove the root cause. Given the risk posed by microsegregation to disguising the true activity of the solder material, care is recommended in performing alpha measurements and evaluating resultant data.

Theoretical situations proposed could result in increased alpha-induced single-event transients, particularly with larger geometry packages. In addition, a mechanism for the temperature-induced increase in alpha emissivity has been proposed. While the impacts on specific architectures are expected to vary widely, this discussion is directed to stimulate thought on potential additional factors relating to SEU causes.

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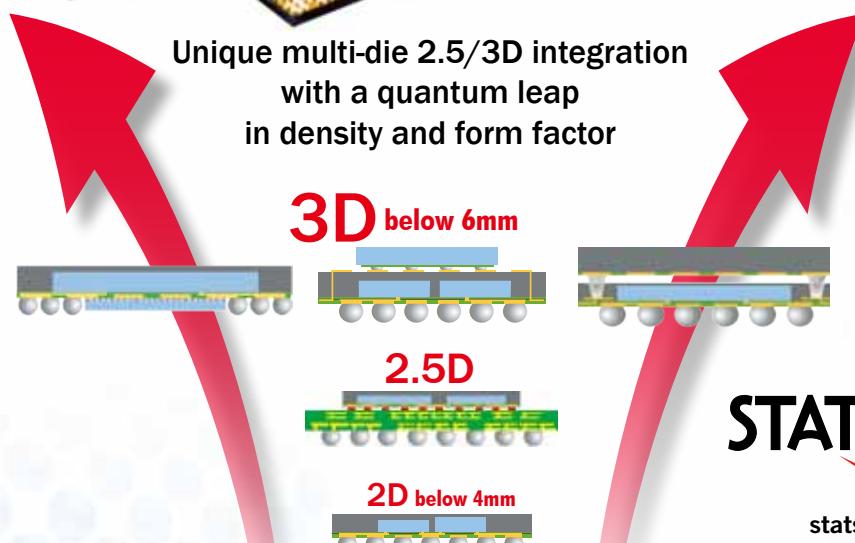
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eWLB A new path for 3D integration



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Advanced Wafer-Level Packaging Technology for 3D Heterogeneous Integration

By Seung Wook Yoon, Patrick Tang, Steve Anderson, Raj Pendse [[STATS ChipPAC, Inc.](#)]

Three-dimensional (3D) integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together into a single device. This approach is expected to effect an industry paradigm shift because of its tremendous benefits. 3D applications will soon begin to appear in portable memory devices and high-performance computers, and will quickly extend to a variety of electronic markets such as information technology, nanotechnology and biotech and medical applications, which will benefit from the high-density, multifunctional heterogeneous integration that 3D technology can offer. The market for portable and mobile data access devices connected to a virtual cloud will continue to drive increased functional convergence, as well as increased packaging complexity and sophistication. Depending on the approach, the potential benefits of 3D integration can vary, including multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs.

This article will discuss the role of advanced wafer-level technology related to fan-in/fan-out (FI/FO) wafer-level packaging (WLP), copper column, integrated passive devices (IPD) and 2.5D/3D through-silicon via (TSV) technology in the development of integrated 3D packaging solutions. Advanced wafer-level technology is rapidly developing into a versatile platform for the semiconductor industry's evolution from 2D package

designs to 2.5D interposers and 3D IC integration, and is moving to a larger scale panel manufacturing approach to further maximize yield, throughput and cost-effectiveness. This article will also highlight recent advancements in design and characterization of highly integrated wafer-level solutions, such as extended die/flip-chip embedded wafer-level ball grid array (eWLB) and 3D FO-WLP.

2.5D and 3D Packaging Evolution

Increasing demand for more advanced, smaller and lighter mobile products with superior functionality and lower overall cost has driven the development of innovative and sophisticated packaging technologies. One of the exciting electronic market trends is the growing availability of mobile devices, such as smartphones, tablets and Ultrabooks, that fully realize the dream of computing and communication convergence, with adequate bandwidth and speed to provide a rich user experience. It is particularly important that the next generation of WLP meets the increasing demand for higher bandwidth, improved thermal dissipation and enhanced reliability in cost-effective, scalable solutions to satisfy the growing mobile market.

The need for higher levels of integration, improved electrical performance/reduction of timing delays and shorter vertical interconnects is driving a shift from 2D to 2.5D and 3D package designs. 3D integration is proceeding on three fronts: moving from package level (die and package stacking) to wafer level (especially FO-WLP), and, more recently, to the silicon (Si) level with TSV and interposers. Today's new lightweight mobile computers are innovative devices providing true convergence with powerful computing

functions, high-speed communications and visual, sensing, and imaging technologies. This convergence is pushing traditional packaging well beyond its typical limits in the areas of form factor, reliability and performance.

Choosing the Right Solution

While the need to combine more mobile functions in an efficient and low profile solution is fueling the shift towards 3D packaging, challenges still remain in the areas of design, test, mass production, cost, and materials compatibility. Given that system-in-package (SiP), package-on-package (PoP), and 2.5D interposer technologies have become more mature and widespread, the further deployment of FO-WLP and TSV will continue to enable the migration to advanced fab technology.

Driving forces behind wafer-level and silicon-based technologies include smaller footprint, increased functional integration, increased I/O density, improved electrical and thermal performance, and lower cost due to batch processing. Examples of wafer-level solutions that address these key requirements are: 1) FI-WLP with tighter pitches for shorter signal lengths; 2) FO-WLP solutions with integration; 3) High speed memory and processor applications with high bandwidth interconnect using 2.5D TSV interposer technology; and 4) Full implementation of TSV 3D packaging technology for mobile products.

Fan-out Flip-Chip eWLB Driving 2.5D Systems

The growth of low-power mobile device applications, today's highest growth segments for advanced

packaging, is driven by the need for increased bandwidth and speed. This drive to put a level of computing performance and networking capability into consumer and lower cost business systems that were once considered high-end is driving a more aggressive push towards advanced WLP solutions and 3D packaging, given the limited form factors and space required for portability.

Wafer-level technologies such as eWLB are leading the way to the next level of thin packaging capability. eWLB provides a robust packaging platform that can support very dense interconnection and routing of multiple die in extremely reliable, low-warpage 2.5D and 3D solutions.

The use of these embedded FO-WLP packages in a side-by-side configuration to replace a stacked package configuration or to serve as the base for a 3D TSV configuration is critical in enabling a more cost effective mobile market capability (**Figure 1**). eWLB has the capability to support structures containing multiple die, multiple redistribution layers (RDL) as well as line-width/line-space (LW/LS) ratios of less than 10 μ m/10 μ m. In addition, technical advancements have enabled eWLB integration of different components such as Si devices, integrated passive devices (IPDs), discrete, MEMS or glass-based devices in a single package.

Flip-chip eWLB provides a fan-out area that features a larger pad pitch and RDL [1, 2]. The I/O reconfiguration minimizes substrate layer numbers, while optimizing electrical performance such as combined power and ground. Flip-chip eWLB has the option to integrate a decoupling capacitor and place it closer to the device for better electrical performance. With eWLB's superior electrical performance, it is possible to reduce the number of layers in the organic substrate. As shown in **Figure 1**, a 10-layer flip-chip substrate could be replaced by a 6-layer substrate using flip-chip eWLB technology.

There are many variables in a flip-chip substrate design, including copper trace line width/spacing, substrate

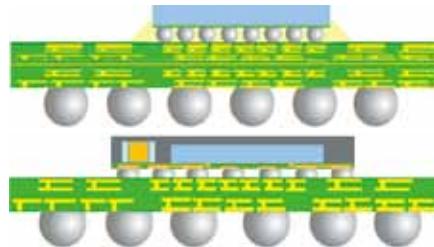


Figure 1: Extended die/fan-out flip-chip packaging approach with fewer layers of organic substrate [1, 2].

thickness, via pad and via hole size, as well as flip-chip/solder ball pitch. Designs that are converted to eWLB should be approached utilizing more actual data to meet electrical performance and signal integrity. eWLB RDL designs provide optimized and efficient signal integrity in interconnection routing that has a coarse bumping pitch (**Figure 2**). Employing a flip-chip eWLB approach in a design with a coarse bump pitch should require a lower cost organic substrate with large pad pitch and reduced number of metal layers. In addition, 3D FO-WLP enables unique applications for mobile devices, such as the 3D eWLB, eWLB-PoP [3-5] and 3D FO-WLP face-to-face (F-t-F) [6].

As shown in **Figure 3c**, 3D FO-WLP F-t-F methodology is the result of direct chip attach using eWLB as an interposer between logic and memory components for high-speed data transfer, low signal path and improved signal integrity. This can be combined with other 3D packages (**Figure 3a, b**) for a highly integrated packaging solution.

TSV Technology

Portability and data-on-demand is forcing increased packaging density and

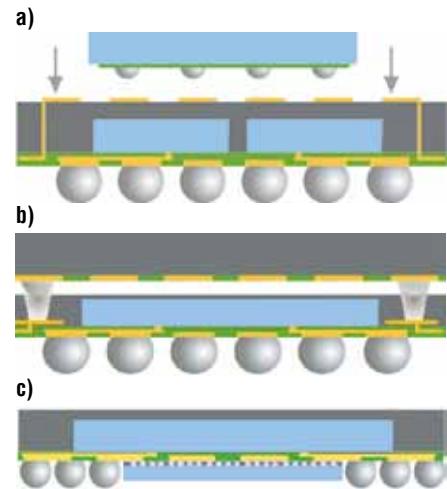


Figure 3: 3D FO-WLP solutions: a) 3D eWLB, b) eWLB-PoP [3-5], and c) 3D FO-WLP F-t-F [6].

more cost-effective 3D solutions. While current PoP technologies are effective for integrating functions in a small package, they lack the high bandwidth and low profile increasingly needed by the new generation of thin tablets and more powerful mobile processors.

Technical and manufacturing issues are the key challenges for 3D stacks. These include issues of testability and yield, scalability, thermal performance, and standardized IC interfaces. 3D TSV packages are being developed to provide heterogeneous integration of memory, logic, graphics, and power functions that cannot be integrated into single die, and to offer improved electrical performance below 28nm from very short and high-density interconnects between the stacked ICs.

TSV technology is being propelled by the need for much faster processing speeds and memory width in order to manage all of the advanced functions

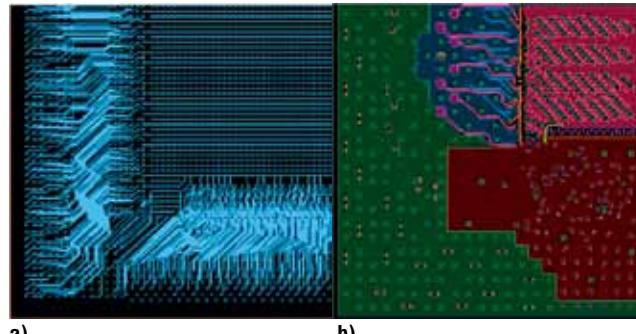


Figure 2: Extended die/flip-chip eWLB packaging technology design optimization of a) 2-layer RDL in eWLB and b) 6-layer organic substrate for a 10-layer flip-chip substrate.

required in high-performance products. For successful market penetration, the TSV ecosystem comprised of IDMs, OEMs, OSATs, foundries, design houses, and PCB suppliers must be properly enabled. The advantages of the TSV packaging approach over system-on-chip

(SoC) are many, including higher bandwidth due to shorter interconnects, power reduction, lower cost, greater miniaturization and greater modularity and flexibility.

Mid-end-of-Line (MEOL). The mid-end TSV process flow occurs between the wafer fabrication and back-end assembly process, and supports the advanced manufacturing

requirements of 2.5D and 3D packaging, including wafer-level, flip-chip and embedded die technologies. MEOL assembly includes micro-bumping (a bumping technology that offers bump pitches of less than 50 μm), temporary bonding/debonding, wafer thinning and planarization, backside via reveal, isolation, and metallization (**Figure 4**).

Back-end-of-Line (BEOL). BEOL assembly includes chip-to-chip (C2C) and chip-to-wafer (C2W) assembly, high-density micro-bump capabilities in both solder and copper column, ultra-fine pitch micro-bump bonding, thin die handling, wafer-level underfill, thin wafer dicing, and micro-bumps for flip-chip interconnection. Micro-bump bonding technology is critical to the delivery of fine-pitch, low-profile solutions for high-performance devices, as illustrated in **Figure 5**. **Figure 6** shows a 3D stacked 3D TSV IC package.

3D Heterogeneous Integration

Increasing interconnect density is driving smaller bond pad pitches, stacked die, mixed interconnect such as flip-chip and wire bond in the same package, as well as advanced interconnect technologies such as interposers and TSV. For mobile and handheld applications, portability is a critical factor for product selection. A thinner package can provide better board-level reliability as well as a lighter

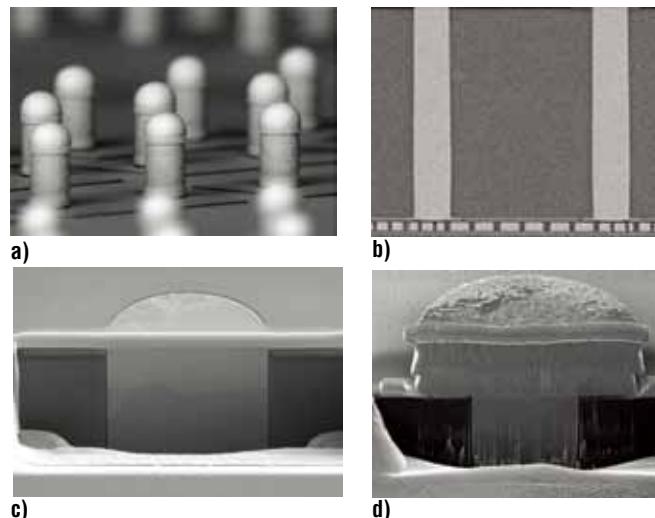


Figure 4: Micrographs of the TSV MEOL process: a) Cu column micro-bump, b) and c) backside via revealed TSV, and d) bump landing pad on TSV.

and thinner profile at the system level. This trend is transforming customer ball patterns to manage the escape routing and costs for system boards.

Overall package performance is heavily influenced by electrical and thermal performance. The modeling and management of these functions

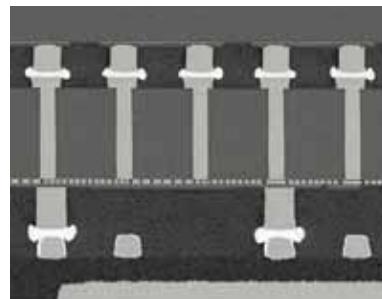


Figure 5: SEM micrograph showing cross-section of a 3D TSV IC stacked package.

is becoming even more critical as expanded functionality is absorbed in fewer packages in these heterogeneous 3D packaging structures. This also means that system performance can be increased and improved if the proper 3D packaging elements can be successfully implemented.

Increasingly recognized as the next industry thrust, 3D WLP SiP (**Figure 7**) addresses a potentially large need in the market, including heterogeneous functional integration, miniaturization, system performance, system flexibility (die/component sourcing, integration), and testability.

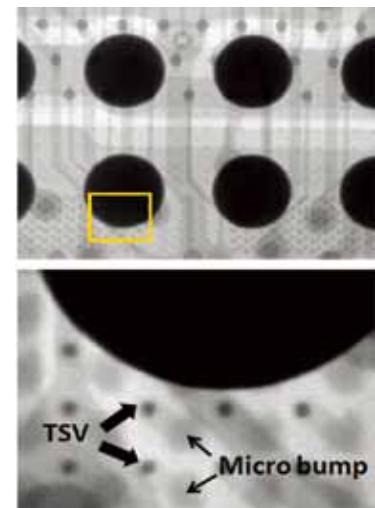


Figure 6: X-ray images of a 3D TSV assembled package.

3D FO-WLP (eWLB) F-t-F

A F-t-F configuration [6] is achieved through direct chip attach on the BGA side of a standard single sided eWLB package using direct vertical interconnects between an application processor die and a memory die through the eWLB layers to enable a high bandwidth memory interface with near-zero parasitics. This FO-WLP approach is shown in **Figure 8** [6]. Such interconnection is uniquely enabled by eWLB technology by virtue of the very fine via pitch (sub-50 μm range) for vertical interconnects made possible by the thin-film structure of the eWLB package, which is not feasible using traditional build-up substrate technology.

There is a need for miniaturization at the IC, module (or sub-system), and system levels. At the IC level, scaling continues as it has over the last four decades according to Moore's Law. Additionally, 3D chip stacking technology utilizing TSVs has garnered much attention recently

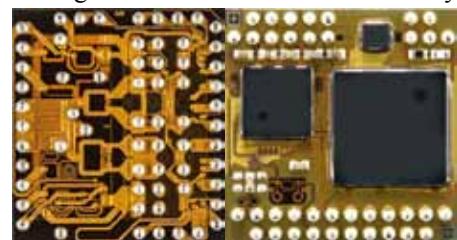


Figure 7: 3D SiP wafer-level integration with embedded passives, IPD and discrete components.

Semiconductor-Grade Fluxes for 2.5D and 3D

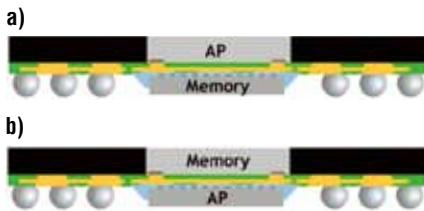


Figure 8: Fan-out package with F-t-F configuration showing: a) Application processor stacked on top of a memory chip, using eWLB as an interposer; b) A memory chip stacked on top of an application processor chip, using eWLB as an interposer.

due to its potential in improving the performance, form factor, cost, and reliability at the subsystem or module level. There is still a great deal of research and development required to bring this heterointegration technology to cost-effective implementation while meeting reliability and performance requirements. In addition to the module level, we must also focus on the performance, form factor, cost, and reliability of the entire system.

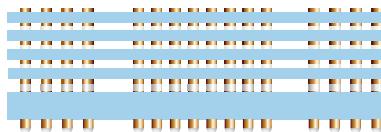
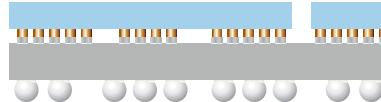
Although active and stacked ICs are a highly functional and important element of the overall system, they are only one set of components. Many other components including other actives, passives, power systems, wiring, and connectors must be considered in a complete system. As a result, there is a need to think at both the module and system levels. This need is largely being met by the current technology domain in the areas of TSV, 3D stacking, and wafer-level packaging. There should be further study on integration, focusing on TSVs, 3D stacking and 2.5D/3D eWLB with better electrical and thermal performance, greater system reliability, and reduced form factor and overall cost. Eventually, technology will go far beyond this, however, to realize truly seamless wafer-level integrated 3D packaging that will incorporate aspects of 3D stacking, silicon packages with embedded passives and actives in a FO-WLP configuration, TSV and micro-bump, as well as 3D WLPs.

Summary

Building 3D packaging infrastructure requires a good system to manage the IC, packaging, and board design, while trying to establish common standards for at least the memory interfaces. An ecosystem consisting of the IP suppliers, foundries, OSATs, IDMs, OEMs, and design houses, is being developed with co-design and standards collaboration. Cost effectiveness depends on the proper co-design of the chip, package, and board.

As the demand for mobile and portable electronics grows, the demand for smaller, lighter, and higher bandwidth packaging will increase, further evolving from today's PoP configurations or SiP to more complex embedded WLP and vertical 3D TSV technology. Differentiation, and even product success, is being driven by ever-expanding feature sets, functionality, convergence and adoption of more computing-rich gesturing and graphic applications. The increase in cloud computing access points requiring improved packaging for the mobile networking market will only further the adoption of variation in 2.5D and 3D packaging. Advanced wafer-level packaging technologies such as TSV, and FO-

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WLP platforms - such as eWLB, are enabling these advances, leading to further exciting developments in the 3D evolution. 

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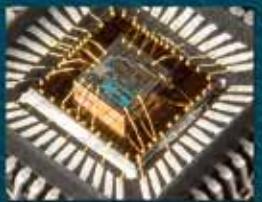
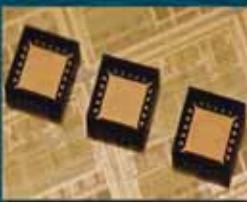
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Adapting an OmPP™ QFN for GaN Power Devices

By Bill Lawrence, Steve Swendrowski [*Quik-Pak*], Greg Klowak [*GaN Systems*], Andy Longford [*PandA Europe*]

Packaging for the wide-band gap power semiconductors, such as gallium nitride (GaN), has been lagging the technology advances of these new devices. Typically, the packaging being used is a legacy option based on thermal requirements. There has been little accommodation made for the performance requirements of the device. GaN has emerged as the technology of choice for power semiconductor applications due to its intrinsic ability to operate at higher voltages, higher switching frequency, handle higher power density, and have better power efficiency than pure silicon devices.

A GaN transistor will typically provide switching times under 10ns and more than 15Amps switching capability. Any significant inductance in the driver circuit will result in unwanted transients that can exceed the threshold voltage of the device. To minimize this, the interconnection has to be as short as possible. But putting the CMOS driver and GaN transistor in close proximity could create thermal issues. This configuration will often produce peak power surges of 40W that the package will need to dissipate to keep the T_j below 125°C when $T_a = 25^\circ\text{C}$.

To fully utilize the benefits of GaN, the package must have low inductance, minimal thermal resistance and handle localized thermal excursions caused by transient peak switching power. Additionally, there are three important parameters to consider when designing power semiconductor packages: thermal dissipation, current, and voltage. A standard package that had enough pins for the driver I/O requirements and could minimize interconnect impedance capable of operation at higher voltage and handle the thermal requirements did not exist. For the GaN device, the

package required a special lead frame, custom molding, and thermal dissipation on the top and bottom of the package.

The Packaging Challenge

To meet the performance criteria, plus time and fiscal constraints, an integrated approach to this packaging challenge was taken. The package developed was an adaptation of a standard power quad flat no-lead (PQFN) package. **Figure 1** is a cross sectional view of the package. The technologies utilized to make this package included custom split pad (die flag) pre-molded open cavity plastic QFN, flip-chip attach, 2D stacked die assembly, and 2-D thermal management. To best utilize each of these packaging technologies, accommodations were also made in the GaN die and control die final fabrication.



Figure 1: Cross section view of GaN and controller chip in package.

The solution started with a transfer molded open-cavity semiconductor package. These packages have unique challenges compared to typical semiconductor transfer molded packages. The package requires the mold compound to be pushed through thinner and longer half-etched lead frame gaps than are normally the case. In addition, features must be added to prevent the unsupported copper die paddle from flexing, causing separation with the mold compound. (**Figure 2** shows examples of transfer molded open-cavity packages.)

The custom PQFN package required control pins, a die attach/ground pad, and a thermal attach pad. In addition, there was a 2.7mm minimum gap required to isolate the 650V output from the lower voltage and ground pins.

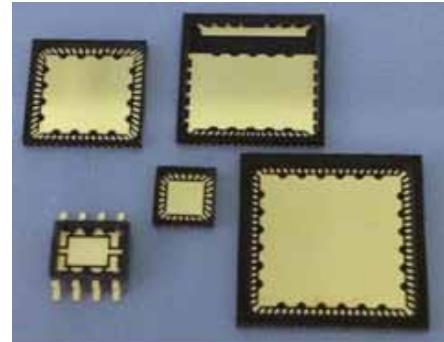


Figure 2: Examples of transfer molding open-cavity semiconductor packages.

All of these features created a package that was very asymmetric that posed a high level of complexity. The lead frame for the package was created to match the mechanical and device specifications plus meet the design rules for etching copper lead frames. Once the lead frame was modeled, flow analysis was performed to validate the package and ensure that the mold design and rheology of the selected molding compound would enable the mold to be fully filled without voiding and air entrapment. Moldex3D™ and Moldflow™ software programs were used for the analysis. Once engineering proved the design viable, the mold was manufactured, tested, and then put into production.

The interconnection scheme chosen for the GaN die to CMOS controller was copper pillars. The use of copper pillars reduced the interconnection inductance by a factor of 10 when compared to a wire bond interconnect. Copper posts also created a transient thermal barrier impedance so that the higher power GaN device would not be directly coupled thermally to the CMOS during the typical short switching cycles seen in power converter circuits.

The manufacturing approach taken for the assembly performed the die-to-die flip-chip attach first. The GaN die was fabricated with tin/silver/copper

(SAC) solder tipped copper pillars that are nominally 115 μm +/-5% tall. The CMOS controller die had solder mask defined attach pads that enable attachment without bridging. The copper pillars and the ability to place interconnects on a grid across the total face of the die create a multiplicity of parallel connections that provide a very low impedance interconnection scheme. The flip-chip attach conditions used in the manufacturing process were standard settings for an SAC solder reflow with nominal placement accuracy.

The die stack was then underfilled and the flip-chip die-to-die was attached to the custom pre-molded open cavity plastic package (OmPPTM). The CMOS driver die was attached to the package die flag using either a conductive silver-filled epoxy or SAC solder attach. Gold thermosonic ball bonding of the CMOS die was the next step required to connect the control pins and improve the ground connection from the die to the die attach pad. For ease of assembly, a 1.0 mil gold wire was used, but ribbon bonding could have been used for the ground connections.

Once the bonding was completed, the assembly was partially molded to stabilize and protect the wire bonds prior to attachment of the thermal heat spreader. The copper heat spreader was pre-formed into the desired shape and attached with solder or super conductive epoxy-filled paste. The final step was molding the part to the final package dimensions. So the fabrication process flow for the package consisted of selecting the package, attaching the die stack, curing, wire bonding, clip attach, reflow, fill, cure, and marking. **Figure 1** shows a cross sectional view of the custom PQFN that was designed and fabricated; **Figure 3** is the unfilled PQFN, while **Figure 4** is a diagram of the finished product. This completed part has a 10mm x 10mm footprint and complies with the JEDEC MO-220 specification.

The packaged device closely matched the simulated and calculated figure of merit (FOM) numbers shown in the graph in **Figure 5**. This was accomplished by keeping the package

impedances at a minimum in two ways. First, the source contact has 3 groups of 28 wire bonds connected to the 200 μm -thick lead frame to reduce unwanted

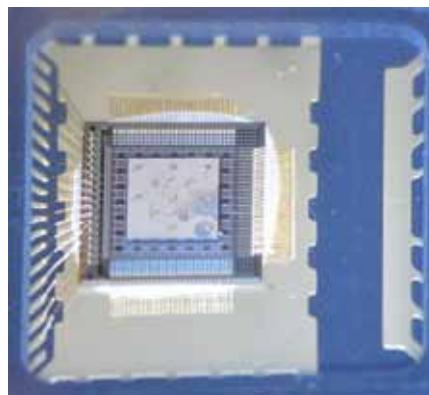


Figure 3: Unfilled PQFN.

source inductance and resistance, which could de-bias a high speed GaN transistor. Second, was the low impedance copper pillar interconnect that directly attaches to the integrated driver on the CMOS side of the device.

To manage the thermal requirements of the package, double-sided cooling was used to allow the CMOS device on the bottom to be cooled by thermal vias in the PCB and the GaN transistor to be cooled via a heat sink attached to the top side of the package. It was determined that with 25 thermal vias under the packaged device with 1oz copper layers in a standard double-sided FR4 PCB, the CMOS device could dissipate enough heat under all typical operating conditions.

The thermal decoupling that the copper posts between the GaN and the CMOS devices created and the top heat spreader clip enabled a 2-D cooling scheme. There are two thermal paths and thus two thermal case-to-junction resistance parameters. Both paths have a thermal resistance less than 1°C/W and allow for dual cooling paths for the drive components and power transistor. To ensure good thermal transfer, the die and clip attach adhesive used had thermal conductivity of 60W/m K and good electrical properties.

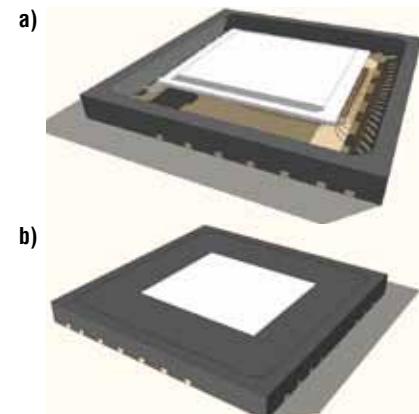


Figure 4: package a) before, and b) after, final molding.

Summary

This customized GaN package offers the significant advantage of a form factor half the size of typical power transistor devices allowing for a decrease of the associated printed circuit board real estate. The electrical and thermal performance, as indicated on the FOM graph, demonstrates the importance of the package design and construction on overall performance. The resulting custom PQFN with segmented lead frame and 2-D thermal dissipation proved to be an excellent package option for these power semiconductors. 

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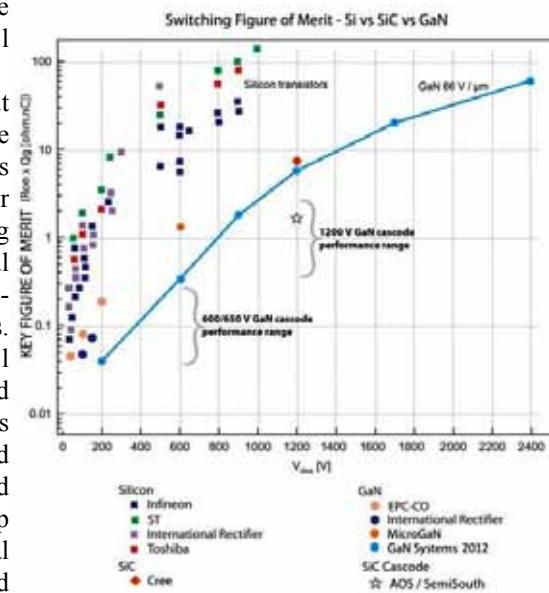


Figure 5: Figure of merit (FOM).



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Taking Copper Wire into High-Volume Manufacturing

By Usman Chaudhry, Willmar Subido *[Texas Instruments]*

The use of copper wire bonding in semiconductor packages has seen a steady evolution in recent years. This technology offers better performance, is more economical than traditional gold wire bonding, delivers proven performance, reliability, quality and cost advantages across analog and embedded processing products, and is gaining broader acceptance in the semiconductor industry.

Developing a robust manufacturable copper wire bonding process requires joint collaboration with wire suppliers, wire bond equipment manufacturers, and tool suppliers. Copper wire has a narrower process window and challenges associated with that can be overcome by developing portable wire bonding parameters across the wire bonder fleet and should result in equivalent productivity and yields to gold wire.

Copper Versus Gold

Copper has normally been the metal of choice for the wires used for power and communications because it provides excellent conductivity, durability and ductility at an economic cost. Copper has also been used in recent years for the interconnections between the transistors on integrated circuits. However, for the ultra-fine pitch, thin wiring that connects an integrated circuit's die pads with its package leads, chip makers have traditionally used gold because it is easy to work with in manufacturing. Gold is relatively soft, non-reactive (except with aluminum), and offers sufficient electrical conductivity for many applications, though less than copper.

However, high electrical performance depends on excellent conductivity or, in other words, low resistance. Since copper has less electrical resistance

than gold, its conductivity is up to 40% higher, which translates into important performance benefits. As a result, copper can provide significant advantages in high-performance communications, computing, industrial equipment and other areas.

Copper's improved thermal conductivity pulls heat away from the die better than gold, leading to better performance at elevated temperatures and with greater reliability. This performance advantage is particularly evident when copper wire is bonded on die pads plated with thick copper and nickel palladium finish in analog and power products where support for high currents is essential. In this case, the metal joint formed is a solid-solution weld that is extremely stable at high temperatures. In addition, the metal's hardness means that bonds stay more stable mechanically in stressed operating environments. Overall, copper wire bonding is technically more challenging than gold, but once achieved, the wiring is more resilient and performs better, especially in high-current analog products.

Copper Wire Bonding Challenges

Despite the cost, performance, quality and reliability benefits, there are technical challenges in developing copper as the choice interconnect material for chip-to-package thin wiring. One formidable challenge of using copper is its reactivity with oxygen in the surrounding air. Wire bonders equipped with specially designed copper conversion kits provide an inert atmospheric envelope by a forming gas that surrounds the wire tip, thus preventing oxidation throughout the bonding process and enabling

stronger bonds (**Figure 1**). Oxidation build-up on the wire during the free air ball formation process can result in a poor and unreliable bond and cause wire bonder errors. Forming gas flow rate is controlled within specifications

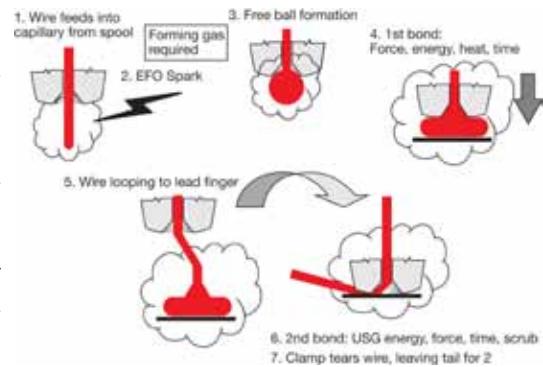


Figure 1: An overview of a copper wire bonding process that uses forming gas.

and free air ball formation parameters are optimized to eliminate this risk. Forming gas is also used over the entire bonding area to allow continuous wire bonding and prevent any oxidation during the bonding steps.

Another important technical issue has to do with copper's hardness and brittleness relative to gold. This impacts both first and second bond quality and productivity. Semiconductor manufacturers have worked closely with wire material suppliers to drive development of new, softer copper wire material compositions to enable a highly reliable process across entire silicon and package portfolios. Specifications have been put in place around manufacturing floor life and shelf life for the wire to maintain the highest levels of quality.

It is necessary to handle copper wires very carefully in order to eliminate the risk of damaging bond pads and underlying circuitry during first bond and to form robust stitches during second bond without impacting throughput. New generation wire

bonders are designed to bond copper wires more precisely on circuit pads and lead frames/substrates, with more finely tuned force, heat, and ultrasonic energy applied to create the bond.

Modifications to the bonding wire capillary design are critical to reducing stress on the silicon. Changes to capillary surface finish are needed to improve second bond quality. Because gold wire is much softer than copper wire, the same capillary cannot be used. For copper wire bonding, a capillary with a granulated rough tip is needed for better gripping between wire and capillary and for better formation of stitch bond and significant reduction in machine stoppages.

The new bonding techniques for copper require careful development and thorough testing, with characterization under a variety of different manufacturing and environmental conditions, including those designed to be worse than anticipated in actual production. In production, maintaining

yield and quality levels equivalent or better than gold wire is always a major concern. Manufacturers must overcome this challenge by running extensive design of experiments (DOEs) early in the product development cycle to establish wide process windows for a high-volume production process. Keeping package type, bonding wire diameter, silicon technology, factory and assembly/test sites in mind, generating detailed risk assessments and running several DOEs to establish and qualify robust first and second bond process windows are required. Next, one must verify the developed process windows across multiple bonders to address any bonder to bonder variation and achieve a process that is portable over the entire bonder fleet.

Once a process has been developed and verified, it is necessary to conduct extensive reliability testing at both low and high ends of the process window to simulate any process drift in production and ensure there will be no

impact on product reliability through extended life cycles. Novel quick testing techniques should be used to assess reliability impact of any process changes very early without having to run full qualification. These techniques, combined with regular equipment maintenance, calibration and tooling modifications such as improved lead frame clamping and heater-block design specifically for copper wire allow achievement of desired productivity levels in high-volume production.

Moving from gold to copper wire bonding requires a slow and careful adaptation of the technology in order to gain significant benefits. Because of the metals' different characteristics, the transition is not a simple switch of materials, but a carefully monitored re-engineering effort that involves improvements in packaging materials, silicon chip design rules, manufacturing equipment, environment, and maintenance in order to provide the necessary quality and reliability in the

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shipped product. Like every stage in IC manufacturing, the processes of selecting, forming and bonding chip-to-package wires have to be extremely precise.

Packaging materials will need to be modified for copper wire compatibility. This includes qualifying halogen-free mold compounds with reduced chlorine content to eliminate any corrosion risk of intermetallics formed after copper wire bonding. Also to be considered is improving compatibility and increasing product performance with copper wire through enhanced silicon design rules and fan-out across multiple silicon technologies. It is necessary to characterize silicon stack-ups and underlying structures in detail through wire bonding and reliability testing and put in place design rules to promote the most manufacturable and reliable production process without any impact on device requirements. To prevent reliability concerns, it is important to achieve the highest standards of quality and design, and maintain specific manufacturing equipment and toolings for copper wire, while improving the manufacturing environment and quality controls.

Prepping the copper wire bonding process requires detailed preliminary studies and experiments and extensive testing and process qualification so that customers can have confidence in the performance and reliability advantages of copper wire bonds. As the process moves from development into manufacturing, success with different types of products can drive the learning curve for assembly.

Analog power ICs, where copper wires are bonded to thick copper nickel palladium plated pads (Figure 2) on the chip require a stable operation with high currents in order to provide a safe electrical environment for the device and the rest of the system. On the other hand, embedded processing devices demand the assembly and operational specifications that are characteristic of high-volume digital products, including precise, secure bonding of copper wires to aluminum pads. Additionally, these product areas make use of various types

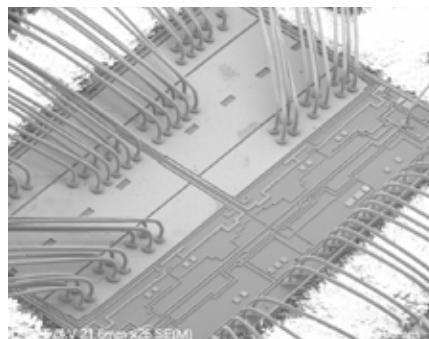


Figure 2: Copper wire on thick Cu/Ni/Pd bond pads. of leaded packages and ball grid arrays, requiring accommodation of wiring techniques to different physical layouts. Mastering the challenges involved in copper wire bonding across this wide range of products have resulted in new devices now being designed from the beginning with copper wire (Figure 3).

The Future of Copper Wire

Copper wire bonding is here to stay and the semiconductor industry is making tremendous innovative advancements in overcoming the remaining technical challenges in areas where copper wire could not be used. This includes areas such as automotive and high-reliability applications, die-to-die bonding at high productivity and yield levels, multi-tier low loop wire bonding, and bonding of unique silicon stack-ups.

Improvements in quality across the entire supply chain and manufacturing environment, methodical development of bonding processes, reliability testing across process windows, and

detailed upfront characterization has allowed devices in automotive and high-reliability applications to start production with copper wire.

Historically, the die-to-die bonding process that uses the stand-off stitch bond (SSB) wire bonding technique avoids the use of copper wire due to impact on productivity and yield (Figure 4). Die-to-die interconnect is necessary to enable multi-chip semiconductor packages. Wire bonding challenges can be addressed by running detailed DOEs and characterization and optimizing the wire bond process parameters and tools.

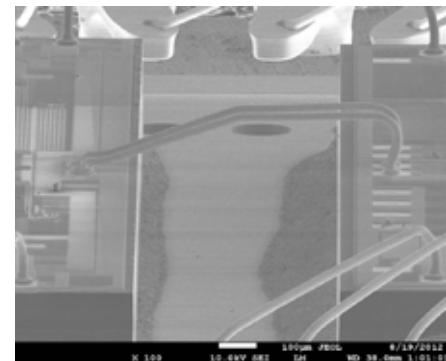


Figure 4: Copper wire bonds in a multi-chip package using SSB bonding.

As copper wire is harder compared to gold wire, multi-tier low loop wire bonding (Figure 5) has been a challenge. This type of bonding is needed for stacked-die and thin packages to provide the maximum performance advantage with the smallest possible form factor. Unique wire bonding techniques, bonding parameters, and capillary designs can help overcome this

TI's history with Copper Wire Bonding

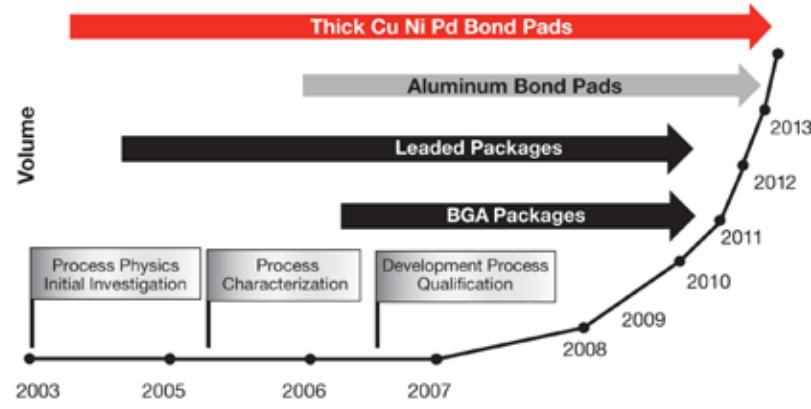


Figure 3: Example of TI's timeline of copper wire bonding research, development, qualification and production ramp.

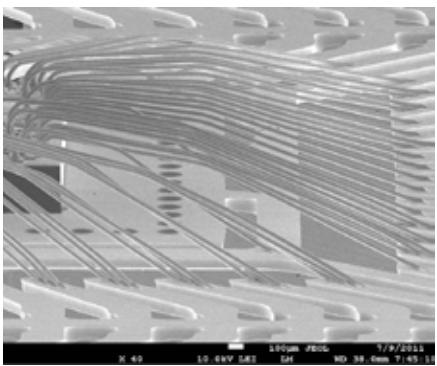


Figure 5: Multi-tier low-loop bonding using copper wires. challenge and allow such devices to be produced in high volume with quality, productivity and yields equivalent to, or better, than gold wire.

Summary

Copper wire has different characteristics as compared to gold wire, which requires any new silicon technology to have copper wire specific characterization done for package assembly readiness to address any challenges such as silicon damage due

to wire bonding. These challenges may be overcome using bonding parameter optimization, capillary design changes and wire bonder setups. However, it is recommended that silicon design rules should be developed specifically for copper wire through early wire bond process characterization on any new silicon technology.

Copper wire bonding brings greater reliability, quality and performance in the semiconductor devices that are designed into a growing range of applications. In manufacturing operations, using copper for wiring provides a hedge on rising prices that can affect the supply of gold available for industrial uses. Thus, copper helps ensure a steady supply of components that can support business growth. As the materials, equipment and tools continue to mature, the semiconductor industry will realize major benefits with the move to copper wire.

Companies must continue to innovate. In the past decade, copper wire bonding

has become one of the most significant innovations in semiconductor packaging and an important competitive advantage. In an industry where packaging is seen as an integral part of the design process and a strategic product differentiator, a transition to copper wire bonding represents an important step in the evolution of packaging technology that benefits customers today and in the future.

Biographies

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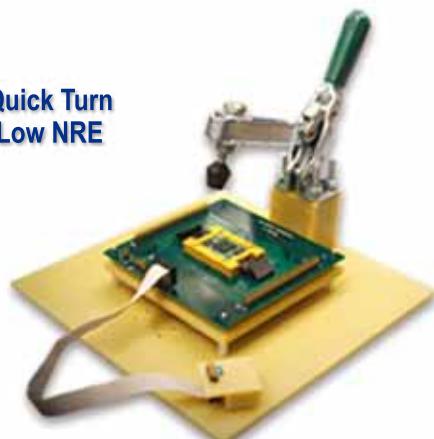
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Cost & Performance for Packaging at 28nm & Beyond

By Bob Chylak, Ivy Qin, Patrick Desjardins, Horst Clauberg [Kulicke and Soffa Ind., Inc.]

Advancements in electronic packaging performance and cost have historically been driven by higher integration primarily provided by wafer fab node shrinks that have followed the well-known Moore's law. However, the tremendously increasing cost of building new fabs will soon cause the performance/cost improvements achieved by moving to smaller technology nodes to become negative [1]. This has initiated the idea of More-than-Moore and vigorous R&D for greater performance through packaging. Substantial performance improvements have been realized through wire bonded stacked die and stacked package-on-package technologies. On the cost side, the recent revolution in the use of copper wire bonding to replace gold has significantly reduced packaging costs. Now new highly integrated heterogeneous 2.5D packages with interposers and 3D packages containing through-silicon vias have been developed, coupling memory and logic more closely. This enables bandwidth gains at reduced power by reducing package impedance. While these configurations greatly improve performance at lower power, the cost has not yet been addressed adequately. Cost control will be essential for successful mass adoption.

Controlling Cost

We as consumers have an insatiable appetite for features that require performance at low power, but only if they come at a low cost. Performance drives increased chip complexity, which leads to rising design costs, few new market entrants and industry consolidation. The need for innovative

solutions and the complexity of the solutions results in rising cost for R&D. Increasingly R&D partnerships and collaborations are formed to spread these costs. Greater package complexity also results in increased manufacturing costs, which lead to continued progression of manufacturing outsourcing. This is all in the context of the volatile global economy that suggests careful inventory management to control cost.

Copper wire bonding will continue to be the lowest cost packaging option. Major subcontractors such as ASE have copper wire bond roadmaps that extend to the 20nm node [2]. Cu wire bonding will always be less costly than existing alternative interconnect technologies for advanced packages – for example flip-chip, or TSV. This is due to the extra process steps, materials costs, and poor assembly throughputs for 2.5 and 3D packages. Today, many of the fundamental technical hurdles of creating these advanced packages have been solved; next, cost reduction, productivity and yield improvements are coming into focus.

Advances in Cu Wire Bonding

Cu wire is about one-tenth the cost of Au wire. In a cost comparison of the three leading interconnect technologies Au wire bonding, Cu wire bonding and flip-chip, Au wire bonding becomes more expensive than flip-chip for devices with 1024 I/Os and more. If Cu wire is used, the cost is lower with wire bonding than flip-chip for packages up to 2000 I/O count [3]. For a 48 lead QFN, a 25% reduction in assembly cost was achieved [4] when switching from Au to Cu wire bonding. Other benefits

of Cu wire include better electrical conductivity and mechanical strength.

The enormous cost advantage of Cu wire bonding makes it a very attractive solution. However, there are several major challenges with Cu wire bonding. First is the requirement of a cover gas delivery system to prevent Cu oxidation during free air ball formation. The most advanced flow system designs, guided by computational fluid dynamics simulations and flow visualization, enable lower levels of oxygen with reduced amounts of inert gas flow [5]. **Figure 1** shows the flow simulation for one of the latest gas delivery systems.

The second challenge has to do with the increased energy required to form good bonds between a Cu ball and a

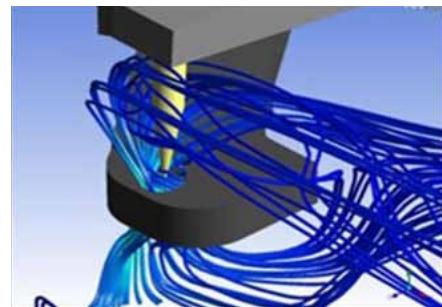


Figure 1: CFD model of IConn ProCu gas delivery system.

pad. Cu balls are about 40% harder than Au balls and also work-harden more. These factors increase the risk of dielectric layer crack and Al splash compared to Au wire and result in a smaller first bond process window. Process window is defined as a range of parameter settings that can meet the target specifications. In a study done in [6], the Cu first bond ultrasonic current window is only half that of a similar Au process. A narrower process window also exists for the second bond due to

the increased hardness of the material and lower bondability of the wire. While a single level of force and ultrasonic current are often used for Au processes, a good Cu process often requires multiple levels of force and ultrasonic current and sometimes also table scrub in different stages. Process optimization becomes a very challenging task.

New ProCu™ processes enable faster, better process recipe optimization and achieve wider process windows [5]. Additionally, these processes are model driven processes, in which default bonding parameters such as ultrasonic current and bonding force are calculated based on desired bonded ball diameter, which is a user input – K&S refers to this as “response-based parameter” input. A set of adjustments are available to account for material variations. This approach enables faster, better process recipe optimization and can achieve a process with a wider process window [5]. These new processes have been widely implemented in production for the most challenging devices today.

The third major challenge is passing humidity-related reliability tests such as the highly accelerated stress test (HAST), because Cu/Al intermetallic compounds are more easily corroded than Au/Al intermetallic compounds [7]. Passing HAST reliability testing was enabled by the development of molding compounds formulated for Cu wire [7]. Pd-coated Cu wire has better corrosion resistance and can pass HAST tests more easily [8]. Optimized wire bonding processes with good IMC coverage also help to ensure reliability [9].

There are two main types of Cu wire – Pd-coated Cu wire (PCC) and bare Cu wire. The main advantages for PCC wire are its better reliability performances and better second bond capability. Because of these advantages, PCC wire is more popular than bare Cu wire in fine pitch production (<1mil wire diameter) today. The main disadvantage of PCC wire is that it is about twice the cost of bare Cu wire.

Other cost reduction in wire bonding interconnect comes from new developments in substrates and lead

frames. New technology such as pre-plated frames (PPF) and uPPF for QFP and QFN reduce the plating material cost. PPF reduces cost by eliminating the wet processing steps in assembly, including deflash and tin plating. One of the issues with some of these new packages is second bond bondability. Due to the thin plating, second bondability is often reduced resulting in a narrow process window. Reduced

capillary life is also seen with these types of packages. One advancement in capillary technology was the development of roughened surfaces. **Figure 2** shows a “granular surface” capillary that can provide an increased grip to the wire and can provide more effective bonding. A wider process window and longer capillary life is often found in this type of capillary.

Over the past decade, the industry's



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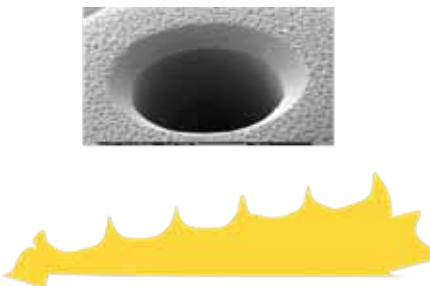


Figure 2: A “granular surface” capillary helps second bond strength and process window.

Fundamental R&D in copper wire bonding has resulted in improved knowledge of Cu wire bonding and many improvements in bonding equipment, processes and materials. The improved technology and production control enabled the successful Cu wire bonding transition to high-volume manufacturing. 0.7 mil and 0.8 mil wire are widely used in production and 0.6mil wire bonding has been demonstrated in production environment on advanced nodes such as the 28nm technology node [2]. Today, Cu wire bonding makes up over 30% of total wire bonding [2]. Due to its low cost, flexibility, demonstrated capability at advanced nodes, and large installed base, wire bonding is here to stay and grow. Future advancements will come from the further proliferation of Cu wire bonding, increased share of bare Cu wire, low cost packages such as QFN, PPF, and uPPF, as well as fine-pitch bonding to advanced nodes.

Controlling Costs in Thermocompression Bonding

While wire bonding remains the most cost-effective interconnect technology and will remain so for some time to come, advanced packaging is emerging as the highest performance packaging technology. However, any widespread adoption in consumer electronics will require a dramatic decrease in manufacturing cost. Improvements in equipment cost-of-ownership (CoO) will be the main pathway toward reducing overall costs for this technology. Throughput as a function of cost for the bonder is one component of this equation. But as has recently been pointed out in detail [10],

controlling yield in multi-chip packages is equally important for controlling cost. Next-generation thermocompression bonders will play a vital role in both improved throughput-per-cost and yield improvement. We believe that the best cost-performance in a high-volume manufacturing environment can only be achieved by highly function-specific, rather than highly versatile multi-use, assembly equipment.

Productivity and Control

K&S is developing the next-generation thermocompression bonder to provide a much improved cost and performance solution. Our emphasis is on higher throughput and yields by bringing greater control over the process and providing integrated process quality control features. The greater control is rendered by better force accuracy, sub-micron position control and thermal stability and thermal uniformity at the tool during ultra-rapid heating and cooling. Many current bonders fall short in these capabilities and have to trade off speed for process robustness.

Better control with higher speed is achieved through state-of-the-art motion control, motor designs, thermally stable designs with advanced materials, and sensors that reflect true position and true temperature at the die being placed. The commonly used method of measuring accuracy using glass scales instead of a real bonding process neglects potential shifts from the temperature ramps and flexing under high pressure. Improved metrics for measuring accuracy are needed. Many current bonders do not have sophisticated servo-controlled linear motors and do not control temperature at the die and Z-position adequately. **Figure 3a** shows an example of a good joint made with our precise temperature and motion controls. In contrast, **Figure 3b** shows joints with over squashed solders made by a current bonder, which could lead to potential yield losses.

One effective way to develop better dynamic motion and temperature control is through computer modeling. **Figure 4** compares the finite element model

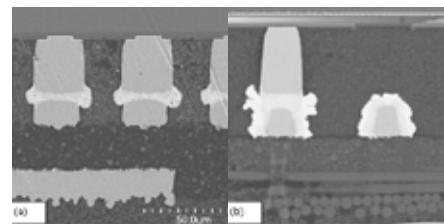


Figure 3: Thermocompression bond made by K&S with 50µm pitch Cu pillar test device on Cu-OSP traces showing good solder flow; b) Cross section of a commercial device produced on a current bonder.

of the temperature distribution of the bonding tool during a rapid temperature ramp typical of a thermocompression bonding process to that measured with a thermal camera. The close correlation of the two images confirms the accuracy of the model, and the model provides much more fundamental insight into the behavior of the system and how it might be improved.

To achieve cost effective bonding processes, equipment and materials need to be designed hand-in-hand collaboratively, not independently. This is analogous to our cooperation with molding compound manufacturers that was essential in getting Cu wire bonding into high-volume manufacturing. To achieve the fastest processes, the properties of non-conductive paste (NCP) underfill as a function of time and temperature need to be understood in great detail. This can only be achieved through collaboration between equipment, materials suppliers, and end users.

Yield Enhancement

Next-generation bonders will need better on-bonder inspection capabilities to improve yields. One of the assembly yield issues is ultra-thin die crack (with TSVs) during dicing or die picking.

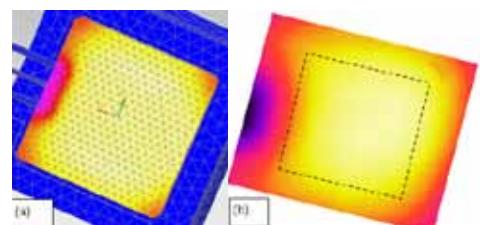


Figure 4: a) Thermal FEA model, and b) actual thermal image of a place tool during a fast temperature ramp. The dotted rectangle in b) shows the approximate location for a 15 x 15mm die.

We are improving die picking and also adding the ability to detect cracked die before they are assembled and expensive packages are lost. At a cost of more than \$1/cm² for an interposer, and more than \$7 for a typical 10 x 10mm die [10], placing a cracked die onto a good package can be very expensive. Other yield enhancement we are developing include new sensors for better control of the dispense process and accuracy inspection capability for 40µm pitch pillars.

Summary

Semiconductor packaging is responding aggressively to provide lower cost and higher performance solutions in the face of a slowdown in front-end (Moore's Law) advances. Tried-and-true wire bonding has responded by enabling much lower cost copper wire to replace gold wire, and new advanced interconnect technologies are entering the market. Optimization of the assembly equipment, materials and processes for

advanced packaging is still needed to make it a true commercial success. ¹⁰

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Latest Insights in Thin Wafer Handling Technologies

By Margarete Zoberbier, Stefan Lutter [[SUS MicroTec](#)]

The demand for further improvement of semiconductor device performance, such as processing speed, lower power consumption, and smaller form factor, has made 3D integration technology employing through-silicon via technology (TSV) increasingly more attractive. Thin-wafer handling (or temporary bonding/debonding) and permanent wafer bonding are the key enabling technologies for 3D integration. After attaching the device wafer to a solid carrier, it can be thinned to expose TSV nails, handled through the backside redistribution layer (RDL) steps and micro-bumping. Eventually, thin die can be stacked using permanent bonding methods. For reliable thin-wafer processing, the selection of a suitable temporary bonding adhesive is crucial. Distinct adhesive properties, such as thermal stability, chemical resistance, and mechanical strength are required for the actual production processes.

To meet the tight requirements for recent new applications, room-temperature mechanical debonding methods have been improved over the last few years and tailored for specific applications. Mechanical debonding at room temperature induces little or no mechanical or thermal stress on the device wafer, and therefore overcomes the major drawbacks that have been described with other debonding methods.

This article highlights the latest insights in thin-wafer handling, or temporary bonding and debonding, especially room temperature mechanical release methods and laser-assisted room-temperature debonding, which have both gone through significant technical evolution.

Temporary Bonding and Debonding Requirements

Forecasts for the demise of Moore's

Law are fairly common. There is a limit to making smaller features where cost and complexity issues become prohibitive. The semiconductor industry has established, rather quickly, a new path forward focused around 3D stacking of integrated circuits. Adding a third dimension to an integrated circuit packs more transistors into the same small footprint without the need to shrink the features of the circuit. The layers are stacked like floors in a skyscraper, effectively allowing Moore's law to continue, albeit, down a slightly different path. 3D integration, or vertically stacked chips or wafers, requires new technology and new equipment, specifically new adhesives and 300mm wafer bonders, as the newest technology is focused on the larger more efficient 300mm wafer size. Just as chemical mechanical polishing (CMP) became the enabling technology for the industry years ago, temporary wafer bonding has been identified as its next enabling technology. Temporary wafer bonding and debonding have emerged as challenging processes necessary for most 3D integration schemes. The selection of a suitable temporary adhesive is the key to success. TSV processing places significantly higher technical demands on the adhesive system compared to MEMS or GaAs processing on smaller wafers. The adhesive must be able to withstand

temperatures of up to 300°C or more, while at the same time be easily removed at room temperature. It must be resistant to a wide range of semiconductor chemicals that it will contact, from solvents and acids, to plating solutions and cleaning agents. Finally, it must have a very gentle debond process imparting the least amount of stress on a fragile wafer thinner than a strand of human hair.

Thin wafers - those for which the final device wafer thickness is typically 30–100µm - need to be processed and also need to be mechanically stiffened by temporary carriers, which can be released easily after the processing is finished. There are a lot of requirements that temporary carrier solutions need to fulfill based on the variety of different conditions in process type, wafer type and the final device application. [Figure 1](#) shows the general process flow for temporary bonding and mechanical debonding.

Today's requirements for temporary wafer bonding adhesives and processing equipment are characterized by the follow-on processes, like bump reflow, plasma-enhanced chemical vapor deposition (PECVD), lithography processes, chemical mechanical polishing (CMP), etc. Therefore, no outgassing, e.g., for PECVD processes, is desired, which means, in general, vacuum process compatibility. Temperature stability is also one of the key requirements. Thermal stability of 250°C to 350°C is required, for example, in bump reflow steps. Due to lithography, CMP, and recess processes,

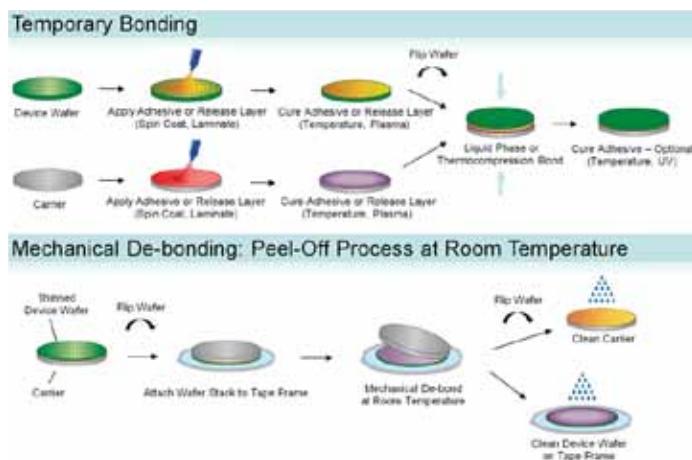


Figure 1: General process flow for temporary bonding and mechanical debonding.

the chemical compatibility is of key importance as well. The system needs to be easy to debond, as thermal or mechanical stress can reduce the yield. It needs to be easy to clean (no chemical stress). The adhesives used for temporary bonding need to have a wide range of thicknesses because of the different applications (see **Table 1**). The ranges of the required TTVs vary between 2 and 5 μm and are dependent on the type of topography that is embedded in the adhesive. Finally, the possibility to reuse or recycle the carriers is an important aspect.

Application	Type of Topography Embedded in Adhesive	Adhesive Thickness	Today's Si TTV Requirements
Thinning / TSV exposure	Pad / RDL	20 μm	<2 μm
Chip stacking / Interposer	Co-Heel / Micro Bump (10 - 40 μm)	20 - 70 μm	≤5 μm
Interposer	Co-bump (10-40 μm)	≥100 μm	≤5 μm

Table 1: Overview about TTV requirements depending on the application/topography type.

2.5D/3D-IC Process Compatibility and Debond Methods

The different debond methods

are solvent or laser release, thermal slide, and mechanical debonding at room temperature. These debonding technologies need to meet a number of different requirements, which are: high throughput capability, low cost carrier material (standard silicon or glass), and in some applications, silicon carriers are preferred, and finally, it is required that there be no mechanical, thermal or laser-induced stress on the device wafer during debonding. Having a closer look at these requirements shows clearly that not all the available methods are suitable for 2.5D/3D-IC applications. Solvent release is a time-consuming process, while thermal slide debonding induces mechanical and thermal stress. Only mechanical debonding at room temperature meets the conditions mentioned above. Nevertheless, excimer laser-assisted release methods are promising candidates too, as these methods fulfill all requirements except the need for compatibility with a silicon carrier.

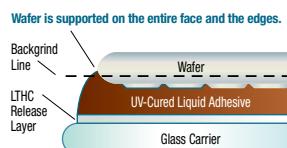
Laser-Assisted Room-Temperature Debonding

Another alternative besides mechanical debonding is a laser-assisted room temperature process, which uses glass carriers with sufficient transmission at the wavelength used for debonding. The laser release is achieved through irradiation using a 248nm or 308nm excimer laser. In contrast to a solid-state laser, which leaves a thermal footprint, the excimer laser breaks the chemical bonds in the adhesive close to the glass carrier interface. While achieving very high throughput, excimer laser debonding does not produce any thermal or mechanical stress on the device wafer. **Figure 2** shows a principle workflow of laser-assisted debonding. What makes it so interesting is the advantage over the other methods in process time. For selected adhesives, a 200mm temporary wafer stack can be debonded in 30s with an appropriately sized laser system as shown in the described test run below.

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Figure 2: Principle workflow of laser-assisted debonding.

Debonding of the glass carrier wafer can be obtained by irradiation of the adhesive bond layer through the glass wafer using a 248nm excimer laser. In the following discussion of the test run, some results with DuPont HD3007 adhesive are described. The absorption spectrum of the adhesive layer shows that wavelengths <248nm are fully absorbed within a 200nm thick film of the adhesive layer. Therefore, above a certain value of energy fluence, the material is decomposed within this zone so that the bond layer is opened. Because of that, the debonding zone is always located 200nm behind the glass wafer surface.

Results show no adverse effects of the excimer laser debond process. The debonding mechanism itself is not dependent on the thickness or thickness deviation of the adhesive bond layer. **Figure 3** shows the principle workflow of the excimer laser-induced debonding approach. The debonding tests were performed with 200mm wafers on a SUSS ELP300 high speed excimer laser system featuring an x-y moving stage and on-the-fly laser processing as shown in

Figure 4. The compound wafers were either mounted onto a film frame carrier or directly chucked with the glass side up onto the stage that was used to raster scan the wafer under the laser beam (**Figure 4**).

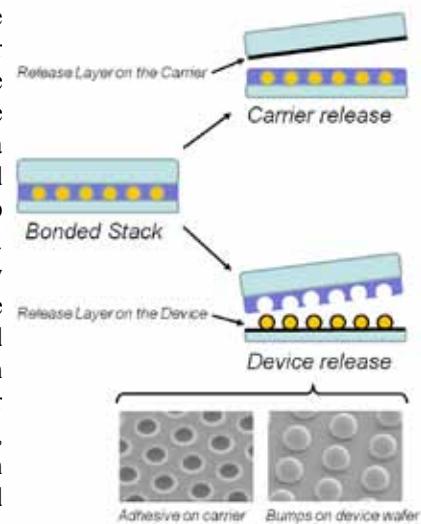


Figure 3: Debonding method: carrier vs. device release.



Figure 4: Setup of laser debonding with a 248nm UV excimer laser and x-y moving stage.

After the laser irradiation, the glass wafer can be easily removed from the silicon wafer by using vacuum tweezers or the robot end-effector. After removing the glass carrier, both the device and carrier wafer need to be cleaned to remove the residual adhesive, which is roughly 200nm thick at the glass side. The major part of the adhesive is left on the device wafer. By immersion of the wafer into a 60°C warm remover bath, a 4-5µm thick adhesive layer could be removed within less than 30s. Even the 200nm thin layers on the glass wafers could be removed by this method.

Carrier vs. Device Release

Besides the different debonding methods there is another aspect that is important for the production process and depends on the desired requirements. As shown in **Figure 3**, there are two alternatives where the bond interface can be separated. The release layer can be deposited on the silicon, glass carrier or on the device wafer. In case of having the release layer on the carrier side, the adhesive remains on the device wafer after debonding (**Figure 3**, carrier release). Solvent cleaning or ashing processes can be used to clean release layer residues from the carrier. The adhesive layer on the device wafer needs to be cleaned by a solvent, which typically leads to a longer cleaning process compared to the second alternative that is described below.

In the case where the release layer is on the device wafer (**Figure 3**, device release), the adhesive layer will stick to the carrier after debonding from where it needs to be solvent cleaned or ashed. Device wafer cleaning is typically a very short process as the release layer residue is very thin compared to the adhesive that is left on the carrier.

Summary

Temporary wafer bonding has an important role in 3D-IC applications. Wafer bonding and debonding are essential requirements and the only viable means to achieve cost effective chips. The selection of temporary bonding materials is governed by a comprehensive review of the thinned wafer processing steps. The physical and chemical requirements of these processes are well known and involve standard CMOS fabrication methods. The temporary carrier in essence is the facilitator that allows for the thin wafer to continue in standardized equipment steps. Bonding temporary adhesives is straight forward and uses bonding equipment that is very similar to what has been widely used in other industries, the MEMS industry for example, for nearly twenty years.

Debonding methods can be tailored to the application with respect to device wafer compatibility. Thermal, solvent, mechanical and laser release can be chosen, depending on the nature of the process flows. More importantly, the variety of materials and carrier combinations enable end users to balance all considerations and arrive at volume manufacturing cost targets that are in line with market expectations. ☀

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Biographies

Maggie Zoberbier received her degree in Mechatronics/Precision Engineering from the Georg Simon Ohm U. of Applied Sciences in Nuremberg and is a Business Development Manager at SUSS MicroTec Lithography GmbH; email margarete.zoberbier@suss.com

Stefan Lutter received a degree in Microsystems Engineering from the U. of Applied Sciences in Regensburg, Germany, as well as a Master of Business and Engineering (MBE®) degree from Steinbeis U. in Berlin. He is the International Product Manager for temporary bonding systems at SUSS MicroTec Lithography GmbH.

The advertisement features a blue-themed background with a white rectangular area containing the company's logo and text. The logo consists of a stylized hand icon above the word "brewer science". Below this, a photograph shows a person's hands holding a thin, reflective silicon wafer. To the right of the photo, the text "ZoneBOND® Technology" is displayed. Further down, the text "The Versatile Solution for Thin Wafer Handling" is written in a serif font. The bottom half of the ad is a dark blue section with three white, bold, stacked words: "MATERIALS", "PROCESSES", and "EQUIPMENT". At the very bottom, there is contact information: "Visit us at SEMICON Taiwan Booth 539" next to a QR code, and the website "www.brewerscience.com".

INDUSTRY NEWS



IWLPC Keynote Announced The Origins of Silicon Valley: Why and How It Happened Here



Paul Wesling, CPMT Society Distinguished Lecturer, a CPMT Society Distinguished Lecturer, will give an exciting and colorful history of device technology development and innovation that began in San Francisco and Palo Alto, moved down the Peninsula (seeking lower costs and better housing), and ended up in the Santa Clara Valley during and following World War II. You'll meet some of the colorful characters – Lee DeForest, Bill Eitel, Charles Litton, Fred Terman, David Packard, Bill Hewlett and others – who came to define the worldwide electronics industries through their inventions and process development.

The 10th Annual International Wafer-Level Packaging Conference brings together the semiconductor industry's most respected authorities addressing all aspects of wafer-level, 3D, TSV, and MEMS device packaging. This year the conference and tabletop exhibition will be held November 5-7, 2013 at the DoubleTree by Hilton Hotel in San Jose, California.

Conference sessions will explore leading-edge design, material, and process technologies focused on wafer-level packaging (WLP) applications. Special emphasis will be placed on the numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that

demand WLP solutions for integration, cost, and performance requirements.

Exhibit space is limited but there are still tabletop spaces available. Please contact Emmy Garner, emmy@smta.org at SMTA or CSR sales representative Ron Molnar at rmolnar@chipscalereview.com with questions or for more information about the exhibition.

Sponsors Update

ACM Research has accepted the



Gold Sponsorship.

Based in Shanghai, ACM Research manufactures innovative tools and novel processes for advanced copper interconnect technologies including electroplating, TSV cleaning and stress-free polishing. ACM has an IP portfolio of over 100 patents filed internationally, of which over 60 have been granted. ACM is committed to providing their customers with advanced and affordable solutions, world-class quality products, and excellent service.

Applied Materials is the 10th



Anniversary Reception Sponsor. Applied Materials, Inc. (Nasdaq:AMAT) is the global leader in providing innovative equipment, services and software to enable the manufacture of advanced semiconductor, flat panel display and solar photovoltaic products. Applied Materials technologies help make innovations like smartphones, flat screen TVs and solar panels more affordable and accessible to consumers and businesses around the world.

Brewer Science has taken the Hotel Keycard sponsorship.

Brewer Science is a global leader in the development and



manufacturing of specialty materials, integrated processes, and laboratory-scale wafer processing equipment for reliable fabrication of semiconductors, compound semiconductors, advanced microelectronic packaging and 3-D ICs, MEMS, sensors, displays, LEDs, and printed electronics.

Watch for the full program to be announced soon! Contact Patti Hvidhyd at 952-920-7682 or patti@smta.org regarding the conference. www.iwlpc.com



Advantest Ranks as Top Semiconductor Test Equipment Supplier For 25 Years

Semiconductor test equipment supplier Advantest Corporation has earned a place on the VLSIresearch list of the 10 Best Suppliers for 2013. For the 25th consecutive year, ratings from the world's leading IDMs, OSATs and fabless companies have secured Advantest a position on the time-honored survey conducted by the industry-analyst firm, VLSIresearch Inc. of Santa Clara, CA.

The annual customer satisfaction survey collects feedback from more than 98% of the worldwide chip market. Participants are asked to rate equipment suppliers among fifteen categories based on three key factors: supplier performance, customer service, and product performance. In total, over 70,000 responses were tallied into the results. The annual VLSIresearch Customer Satisfaction Survey on Chip

Making Equipment is the only publicly available opportunity since 1988 for chip manufacturers to provide feedback on their suppliers.

Advantest reports that the specific areas in which their customers expressed the greatest degree of satisfaction with the company's performance included trust in supplier, product performance, quality of results, partnering, and technical leadership. Reportedly Advantest won the highest rating in the industry in the categories of trust, partnering, field engineering support, commitment, and support after sales.

"Advantest takes pride in the high standards it sets for its products and services and we are gratified that our commitment to excellence is so highly recognized by the world's leading semiconductor manufacturers," stated Haruo Matsuno, president and CEO

of Advantest Corporation. "We are grateful to our customers for the trust and confidence they place in our capabilities and we remain steadfastly focused on their success and to delivering the industry's highest performing test solutions."

Mouser and Advanced Thermal Solutions, Inc. (ATS) Sign Global Distribution Agreement

Advanced Thermal Solutions, Inc. (ATS) announced a new global agreement with Mouser Electronics, Inc. to distribute heat sinks and cooling solutions.

Mouser Electronics maintains a worldwide distributorship for design engineers and buyers, with 19 global support locations, reportedly featuring the latest semiconductors and electronic components.

The agreement with ATS gives Mouser Electronics customers access to

a wide range of heat sinks available in thousands of shapes and sizes. "We look forward to providing thermal solutions to Mouser's customers around the world," said Sharon Koss, VP of Operations and Business Development of ATS.

ATS heat sinks are designed for use in many applications including telecom, datacom, LED, automotive, medical, and aerospace. Their maxiFLOW™ heat sinks feature a low profile spread fin array and are available with thermal tape, push pin or its patented maxiGRIP™ attachment methodology, which permits attachment to BGAs, flip chips and other hot components on a PCB without needing to drill holes in the board. Both the spring and frame clip in the assembly can be removed, allowing the heat sink to be detached and reattached without damaging the device, surrounding components or PCB.

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Aledia Welcomes New Board Member

Aledia, developer of microwire-based 3D LED technology, announced that solid-state lighting (SSL) industry veteran Bernhard Stapp, Ph.D has joined its board of directors.

Stapp brings more than a dozen years of executive experience in LED lighting technologies to Aledia, most recently in senior management positions at OSRAM, a global leader in SSL manufacturing and marketing, where he was responsible for the company's professional LED and OLED business and oversaw launch of the world's first OLED lighting products.

"Aledia's technology is, quite simply, a breakthrough for the entire LED sector," said Stapp. "It can meet

the industry's critical requirement for cost-reduction, while using far simpler production processes and much less material than conventional approaches. I am very excited about the opportunity to join this team."

"Bernhard has been a key player at the heart of the global LED industry since its inception, and also has an outstanding technical background," said Giorgio Anania, co-founder, president and CEO of Aledia. "His unique perspective on this industry's future will be invaluable as Aledia moves into the next stage of its evolution."

SV Probe Establishes Repair Center in Italy

SV Probe ("SV") announced that it has signed a contract with K314 srl, an electronics service company in Vimercate, Italy, to perform probe card repair

work. Probe cards are essential tools for electrical testing of semiconductor wafers before they are diced, packaged, and assembled in electronic products such as tablets, smart phones, computers and digital media players.

According to the two companies, this collaboration will not only provide European customers with efficient and timely repair solutions, but bolster SV's global expansion of support facilities.

"The establishment of this repair center demonstrates SV's commitment to our customers in the European region," explained Karen Lynch, Senior VP of sales and marketing, SV Probe. "At the same time, it further strengthens SV's worldwide infrastructure offering our customers faster and more cost-effective probe card services."

"The K314 team is very pleased to join SV Probe in supporting their European clientele," added Cristiana Molina, CEO, K314. "Combining K314's electronic assembly and design strengths with SV's innovative test solutions will provide our European customers with turnkey solutions to meet their time-to-market needs."

imec and GLOBALFOUNDRIES Announce Collaboration

imec and GLOBALFOUNDRIES have expanded joint development efforts to advance spin-transfer torque magnetoresistive random access memory technology (STT-MRAM)—a promising high-density alternative to existing memory technologies, like SRAM and DRAM.

"Innovation in next-generation memory is required to give chip designers new options to continue to deliver leading-edge products with higher performance, lower power-consumption, and better bandwidth" explained Gregg Bartlett, CTO, GLOBALFOUNDRIES.

The first IC manufacturer to join imc's R&D program on emerging memory technologies, GLOBALFOUNDRIES

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completes the value chain of imec's research platform, which fuels industry collaboration from technology up to the system level.

"Our unique research environment harnesses the collective expertise and knowledge of the entire value chain, bringing together foundries, IDMs, fabless and fablite companies, packaging and assembly companies, and equipment and material suppliers to drive innovation and the development of new, competitive products," said Luc Van den hove, president and CEO, imec, of the collaboration.

GLOBALFOUNDRIES is joining a team that includes Qualcomm and several worldwide equipment suppliers to provide the complete infrastructure necessary for R&D on STT-MRAM. Together, imec and the program members aim to explore the potential of STT-MRAM, including performance below 1ns and scalability beyond 10nm for embedded and standalone applications.

"We are elated to intensify our collaboration with GLOBALFOUNDRIES and the other program members on advanced memory technologies," Van den hove continued.

Bartlett added, "This new partnership with imec will enable close collaboration with customers, partners, and the supplier community to help reduce the risk in bringing this new memory technology to market."

Mentor Graphics and Tezzaron Collaborate on 3D ICs

Mentor Graphics Corp and Tezzaron Semiconductor Corp are teaming up to integrate Mentor's Calibre® 3DSTACK product into Tezzaron's 3D-IC offerings.

Tezzaron works with industry academia and government to create advanced 3D-ICs. It offers both wafer and die stacking technology with TSVs, built in self-test and repair (Bi-STAR®) circuitry for continuous error detection and recovery, and memory devices for both standalone and stacked applications.

"Tezzaron specializes in 3D wafer stacking and TSV processes," explained Robert Patti, CTO and VP of design engineering at Tezzaron Semiconductor. "We work with dozens of customers to create custom 3D-ICs for prototyping and commercialization, including recent 3D-ICs in 40 nm and 65 nm; the first at these small nodes."

Mentor Graphics' contribution to the collaboration is its Calibre 3DSTACK signoff solution, which reportedly provides DRC, LVS, and parasitic extraction (PEX) capabilities. It verifies physical offset, rotation, and scaling at the die interfaces and enables connectivity tracing and extraction of interface parasitic elements needed for multi-die performance simulation. Additionally, it supports dies based on different technologies or process nodes.

By integrating these capabilities, the companies expect to provide fast, automated verification of die-to-die interactions in 2.5D and 3D stacked die configurations by verifying individual

dies in the usual manner, while verifying die-to-die interfaces in a separate procedure with specialized automation features. The two companies plan to extend their collaboration to include development of solutions for the silicon photonics market.

"Over the last two years, the relationship between Mentor Graphics and Tezzaron has really blossomed as we work together to bring volume 3D-IC applications to the IC industry mainstream," said Michael Buehler-Garcia, senior director of marketing for Calibre Design Solutions at Mentor Graphics. "Combining flexibility, ease-of-use, and interoperability provides the highest value for our mutual customers, and will help make the adoption of 3D-IC design techniques successful."

"By collaborating with Mentor Graphics, we can offer our mutual customers a comprehensive design verification solution. It creates the highest value for them with the least disruption to their existing flows," added Robert Patti.

XILINX Achieves PCI Express Compliance Across 28nm Programmable Device Family

Xilinx announced that its All Programmable 7 series FPGAs and Zynq®-7000 All Programmable SoCs are now in full compliance with PCI Express® and were added to the PCI-SIG integrator's list. All of Xilinx's 28nm devices passed rigorous electrical, protocol and interoperability tests at the latest PCI-SIG event held on April 15, 2013. This marked PCI-SIG's first official PCI Express Gen3 compliance and interoperability testing since the introduction of the specification.

According to the company, this achievement is significant because it will allow designers to meet high system bandwidth and programmable systems integration requirements needed in a variety of markets, including communications, storage, and server applications. The device families

are said to enable design productivity in industrial and automotive applications.

HELIOS Program a Success: Good News for Europe

As a result of the success of the recently completed HELIOS program, CEA-Leti reports that Europe is positioned to design and manufacture volume silicon photonics device design.

Launched by the European commission in 2008, HELIOS focused on developing essential building blocks like efficient optical sources (silicon-based and heterogeneous integration of III-V on silicon), integrated lasers, high-speed modulators, and photo-detectors. The €8.5M, 20-member project combined and packaged these building blocks to demonstrate complex functions that address a variety of industry needs. It developed a complete design and fabrication supply chain for integrating a photonic layer with a CMOS circuit using microelectronics fabrication processes. Most recently, Leti's HELIOS program reportedly demonstrated a complete design flow, integrating both silicon photonics device design and electronic/photonics system design in an EDA-compatible framework.

"It is strategically important for Europe to maintain photonic chip-design and chip-integrating functions to compete with other countries and to encourage innovation by European microelectronics companies," said Laurent Malier, CEO, Leti. "HELIOS' success in creating the essential building blocks for integrating photonics with CMOS circuits and making the process available to a variety of users underscores the key role that broad European technological cooperation plays in a very competitive global business environment."

Thomans Skordas, head of the EC's photonics unit, said HELIOS shows a variety of potential

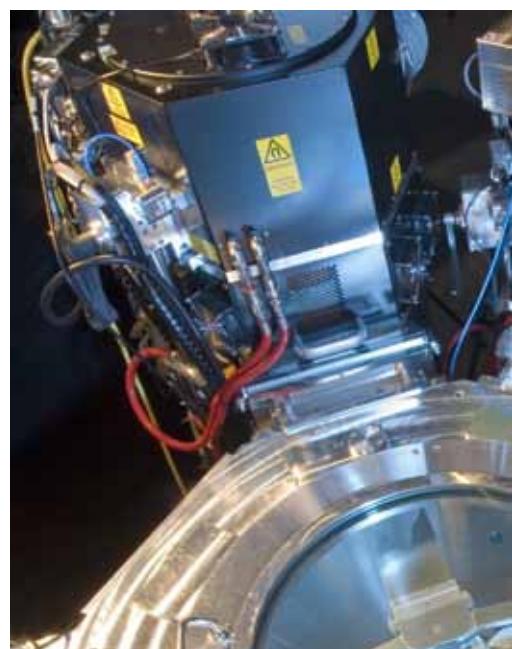
applications for silicon photonics, such as applications in data communications.

"The technology roadmap of silicon photonics becomes clearer now. Europe will have to move fast to become competitive in this new field," said Skordas. "Strategies for the industrialization of silicon photonics are currently being discussed in the context of Horizon 2020—the EU's new framework program for research and innovation for 2014-2020."

According to Leti, due to the cost advantages of integrating photonic and electronic functions on the same chip, silicon photonics is key to developing optical telecommunications or for optical interconnects in microelectronic circuits. The company also reports that CMOS photonics may lead to low-cost solutions for a range of applications such as optical communications, optical interconnections between semiconductor chips and circuit boards, optical signal processing, optical sensing, and biological applications.

SPTS Ships 1000TH DRIE Module

Semiconductor equipment and



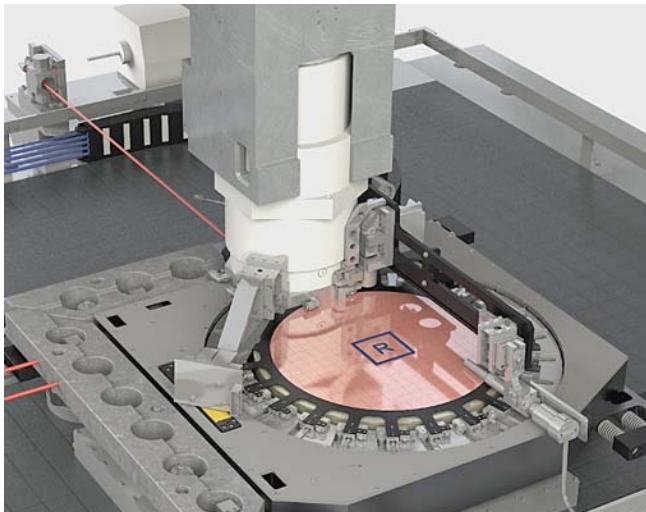
solutions provider, SPTS Technologies, reached a major milestone with the shipment of its 1000th deep reactive ion etch (DRIE) module. The company announced the news at the 2013 SEMICON Singapore MEMS Forum.

"This 1000th shipment is a proud moment for everyone at SPTS," noted. Dave Thomas, Ph.D. marketing director for etch products at SPTS. "MEMS feature in every automobile, smartphone, tablet and gaming console on sale today. Our lives are hugely enriched by these microscopic sensors, and in the near future our healthcare will become reliant on them. For nearly 20 years, our engineers have contributed to this widespread adoption by producing reliable, cost effective DRIE systems with the precision and control that is required for ever more sensitive and functional devices. We continue to develop our DRIE technology for future generations of MEMS and related chip-sets."

SPTS was the original licensee of the Bosch process, a patented process fundamental to the DRIE, and shipped its first commercial system in 1995. Since that time, DRIE process capability has continuously improved to the point where etch rates in production exceed 30 μ m/min, aspect ratios can exceed 90:1 and device features of <50nm are achievable. Recently, DRIE is also being applied to through-silicon via (TSV) technology for 3D integration.

Rudolph Technologies Installs First JetStep System

Rudolph Technologies, Inc. a provider of process characterization, photolithography equipment and



software for the semiconductor, FPD, LED and solar industries, announced the first sale and installation of its JetStep™ Photolithographic tool to a provider of advanced semiconductor packaging and test services. The company reports that the system, which was shipped to Asia in Q4 2012 for wafer-level packaging processes, was put in production during the first quarter of 2013.

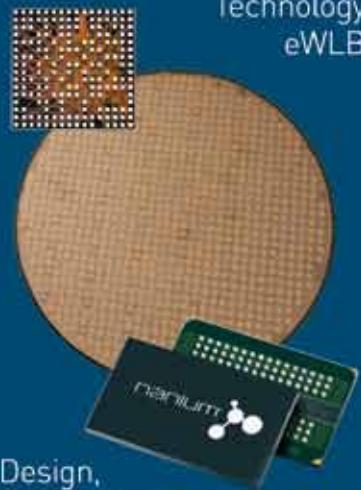
"Adoption of Rudolph's revolutionary 2X reduction system confirms our belief that the unique capabilities of the JetStep System are the best available solution for the highly demanding lithography needs specific to advanced packaging processes. These needs, such as the ability to accommodate warped-wafer substrates, are markedly different from front-end lithography," explained Mayson Brooks, senior V.P. and general manager of Rudolph's Advanced Packaging Lithography Business Unit.

Elvino da Silveira, CTO of the Lithography Systems Group, explained that as technological specifications change, more companies are moving from aligners to steppers to meet new requirements in advanced packaging processes. He said the JetStep System is a 2X reduction stepper with a large field of view (52mm x 66mm) that can handle a wide spectrum of substrate sizes and warped wafers, which may



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What does this mean for Rudolph Technologies? Paul F. McLaughlin, chairman and chief executive officer of the company noted that this is good news, calling it a "milestone." He also discussed how the sale of the JetStep system is "validating the commercialization of our innovative 2X stepper total lithography."

"Advanced packaging is in the early stages of dynamic growth and is a critical driver of mobile connectivity and, therefore, a critical driver for Rudolph. Consumer device demand is driving the need for new packaging technologies for 2.5D and 3D multi-die integration. These and other advanced wafer-level packages now in

development at leading IDMs, foundries and OSATs require a more sophisticated stepper lithography solution," noted McLaughlin, "The Rudolph JetStep 2X Solution is positioned not only for today's leading edge packages, but also for future advanced packaging technology needs."

Tonka Bay Acquires Corwil Technology Corp.

Tonka Bay Equity Partners LLC announced the acquisition of Corwil Technology Corporation, which was founded in 1990 as a provider of assembly and test services for integrated circuits (ICs). The company subsequently grew to become a strategic manufacturing partner in high-cost-of-failure and high-reliability market segments, including medical devices, and military and aerospace industries.

In a recapitalization transaction, Tonka Bay partnered with Corwil's current management, including cofounders Rob Corrao and Finn Wilhelmsen. The acquisition is Tonka Bay's fifth investment in its third fund, which had \$150M in capital under management.

"Corwil is poised for significant growth," said Matt Bergeron, president and board member. "We have an unparalleled assembly and test offering and our customers truly see us as manufacturing partners."

Stephen Soderling, Principal of Tonka Bay and Corwil Board member, explained that the company holds a defendable niche in on-shore assembly and test marketplace, thanks to unique capabilities and deep customer relationships.



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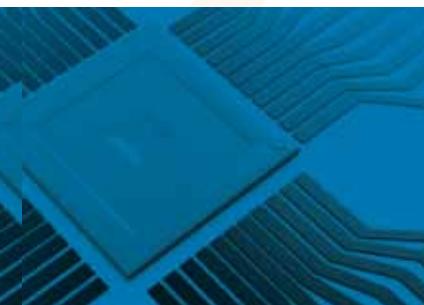
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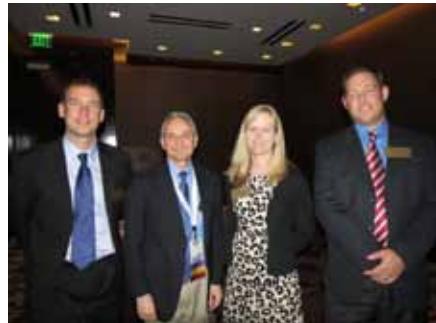
ECTC 2013 Confirms Traction Gains in 2.5D and 3D Integration

The 63rd annual Electronic Components and Technology Conference (ECTC) convened at the Cosmopolitan Hotel and Casino on May 28 – June 1, 2013. By all measures, the event, considered by many to be the premier international conference on IC packaging, components, and microelectronic systems technology, was an outstanding success and lived up to its stellar reputation.

It's clear that 2.5D and 3D research took center stage at the conference and is gaining traction. Perhaps Dave McCann, 63rd ECTC Sponsorship Chair, summed it up best when he said, "At the conference, we saw the discussion turning from the promise and inevitability of 2.5D and 3D, to solving the challenges of implementing 2.5D and 3D, including low cost interposer technologies, memory supply, and the need for bare die stack probe, microbump reliability, power distribution through TSVs, and driving cost down and yield up to enable implementation."

Although highly acclaimed for the quality of its 377 original technical presentations (up from 347 in 2012), the event has steadily increased the size of its exhibition area as well. The Technology Corner exhibition area was "sold out" again this year as it grew to 95 exhibitors from 81 last year (a 17% increase)! Both figures are new ECTC records.

As a strong sign that the semiconductor market segment has fully recovered from the 2009 economic downturn, the conference has grown from 550 attendees in 2009, to more than 1,300 attendees in 2013, representing 31 states and 26 countries. This year's attendance also set a new record – surpassing the 50th anniversary ECTC held in 2000.



ECTC Technical Team: Wolfgang Sauter, IBM, 63rd ECTC General Chair, David McCann, GLOBALFOUNDRIES, Jr. Past General Chair, Beth Keser, Qualcomm Technologies, Program Chair, Alan Huffman, RTI International, Assistant Program Chair

Comments from Wolfgang Sauter, 63rd ECTC General Chair

This year's conference was a huge success. From abstract submissions, conference attendance, industry support and exhibit interest - ECTC 2013 set new records in just about every metric we know how to measure. Semiconductor packaging continues to receive more and more recognition as the solution to solving tomorrow's bandwidth, cost and yield problems. We have successfully transitioned from concepts with process-by-process capability, to being a critical factor in the IC architecture and design with fully integrated capabilities and solutions.

Comments from Beth Keser, 63rd ECTC Program Chair

2013 was an outstanding year for the technical program of ECTC. In addition to the 36 technical sessions and five poster sessions, there were five Tuesday and evening sessions that were very well received. On Tuesday, over 200 people attended the Special Session on "The Role of Wafer Foundries in Next Generation Packaging," hosted by Sam Karikalan of Broadcom Corporation. Presentations by TSMC, SMIC, GLOBALFOUNDRIES, IBM, and UMC kicked-off ECTC's technical program. The message was collaboration between wafer foundries, OSATs, and the materials and tooling suppliers is key to the success of next-

generation packages. On Wednesday evening, the 2013 ECTC Plenary Session on "Packaging Challenges Across the Wireless Market" was also well-received with over 200 attendees. Lou Nicholls of Amkor Technology brought together panelists from Nokia, Qualcomm, RFMD, Amkor, and SEMCO, and all agreed we need to overcome the thermal challenges in the handheld market. The Cosmopolitan of Las Vegas was a new venue for ECTC that turned out to be an excellent fit and we look forward to returning in 2016."

Highlights of the Conference

Over 330 registrants attended 16 Professional Development Courses (PDCs) to kick off the conference. The PDC program included four new courses plus two significantly updated offerings this year. The five themes were Reliability, Modeling, TSV & 3D, Polymers, and Electrical. The most popular PDC was "TSV and Other Enabling Technologies for 3D IC Integration," led by John Lau of Industrial Technology Research Institute.

At least 25% of the 36 technical sessions dealt with various aspects of 3D packaging technology. The most popular technical session was Session 7 titled "Interposers," followed closely by Session 1 entitled "3D Assembly and Reliability."

The annual ECTC Luncheon on Wednesday featured a stimulating keynote speech by Dr. Chris Welty, Research Scientist at IBM T.J. Watson



Dr. Chris Welty, Research Scientist at the IBM T.J. Watson Research Center, gave the keynote to over 1000 attendees on the development of Watson, the IBM computer that defeated the best players on the American game show Jeopardy.

Research Center, on “Engineering Challenges in Building Watson.” He described the analysis factors developed for “cognitive computing” software and the challenges of hypothesis scoring of text-based knowledge as was used for the IBM computer, named Watson, that defeated the best players of the American game show, Jeopardy.

Five poster sessions held in the Technology Corner exhibit area, including one student poster session, covered 121 different interactive presentations (up from 95 last year).

Five special sessions addressed 1)



Interactive presentations

the role of wafer foundries in next-generation packaging, 2) LED for solid-state lighting, 3) packaging challenges across the wireless market supply chain, 4) advanced low-loss dielectric materials for high frequency and high bandwidth applications, and 5) modeling and simulation challenges in 3D systems.

A number of ECTC and CPMT awards were announced for the best 2012 session, poster, and student



Prof. John H. Lau of ITRI, Taiwan (at center) was the recipient of 2013 IEEE CPMT Award, also in the picture (second from the right) is Prof. Ricky Lee, President of IEEE CPMT society.

papers. In addition, a number of individuals were honored by the IEEE CPMT Society for their service to the industry. Receiving the highest honor, the 2013 Field Award, was John H. Lau for contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging.



At the Gala Reception, Prof CP Wong, Lawrence Michaels, Prof James J.Q. Lu

Technology Corner Exhibits

From the Technology Corner exhibition area.



NTK Technologies Inc. Hirohito (Hugh) Hashimoto, Mariel Stoops, Bill Moody, Kim Newman, Ron Molnar



CORWIL Technology Corp. Brian Riley, Matt Hansen



Teledyne Microelectronic Technologies, Harry Kellzi, Sharon Fletcher



STATS ChipPAC, Patrick Tang, Heather Garonzik



IMAT, Michael Danylchuk, Yoshi Ono

Mark your Calendar for the 64th ECTC

Planning is already underway for the 64th ECTC, which will be held May 27 – 30, 2014 at the Walt Disney World Swan and Dolphin Hotel in Lake Buena Vista, FL. The first Call-for-Papers has been issued and abstracts must be received by October 14, 2013.

Product News

EV Group Rolls Out Next-Generation Automated Resist Processing System



EVG®120 Automated Resist Processing System

Semiconductor equipment supplier EV Group (EVG) introduced the latest version of its EVG®120 automated resist processing system at SEMICON Singapore 2013. This next-generation tool features enhancements that were originally developed for 300mm equipment platforms such as newer robots and handling systems for faster throughput. The result is a 200mm tool targeted for the intricacies of handling microelectromechanical system (MEMS) wafers in high-volume manufacturing (HVM).

Dr. Thomas Glinsner, head of product management for EV Group, credits 15 years of experience in the process for these tool enhancements. "In independent surveys, our customers consistently attribute the highest scores to EVG's lithography equipment, and we've listened to their feedback to create a more optimized system," he said.

In addition to MEMS, the EVG120 system reportedly supports coating and developing applications for advanced packaging and compound semiconductors. The tool can be configured with combined spin and spray coating modules—a unique feature

that is said to maximize productivity and optimizes cost of ownership (CoO).

The automated resist processing system features a new robot with dual arms for fast wafer swapping and additional processing chambers. It runs the same EVG CIM Framework software as the company's high-end XT Frame systems and offers full software integration with SECS/GEM standards. Two customizable wet processing bowls are complemented by 10 stacked modules for vapor prime, soft and hard bake, and chill processes. Like its predecessor, the EVG 120 system can accommodate wafers up to 200 mm in diameter.

Coventor's SEMulator3D 2013 Addresses 3D Fab Era Requirements

Expanding the value of virtual fabrication to the semiconductor Ecosystem by reducing learning cycles and subsequently cost, Coventor®, Inc. announced that its SEMulator3D® 2013 software platform is now available. Targeting semiconductor device and MEMS design, this platform reportedly brings physical accuracy and predictive modeling capabilities to process development and integration.

This simulation software platform comes at time when semiconductor companies are grappling with the complexities of integrated 3D front-end-of-line (FEOL) manufacturing processes such as Tri-Gate and High-k/Metal Gate logic, as well as advanced 3D memory technologies. Fabless design teams also face challenges migrating their intellectual property (IP) into these new technologies. SEMulator3D 2013 reportedly responds to such evolving requirements with a virtual fabrication platform that makes it possible for

foundry and fabless development teams to effectively collaborate at the physical process level.

According to the company, the core of this platform is a physics-driven modeling paradigm for addressing physical process behavior that makes virtual fabrication more predictive and provides new opportunities for replacing actual silicon learning cycles with faster, less costly virtual cycles. In addition, virtual metrology innovations and the automation of virtual experiments enable process developers to perform virtual fabrication operations in hours or days instead of the months required for actual silicon learning cycles.

"With new silicon architectures ramping quickly, IBM is introducing new manufacturing technologies that will keep us on the cutting edge of chip-making for server microprocessors, systems-on-chips and specialty silicon for consumer applications," said Gary Patton, Vice President, IBM Semiconductor Research & Development Center. He credits tools such as Coventor's virtual fabrication platform with speeding up end-to-end technology development in 22nm and beyond, enabling a faster time to market for customers.

Hesse Mechatronics Offers New Service for Bondjet BJ939

Hesse Mechatronics, Inc. introduces application development, prototyping and pre-production services on a newly installed BONDJET BJ939 Fully Automatic Heavy Wire Bonder in addition to demonstrations. They are offering these services at the company's west coast demonstration and applications lab, located at long-time company manufacturer's representative Chalman Technologies in Anaheim, California. Additionally, at its demonstration labs in Tempe, AZ and Clinton, MA, the company will offer expanded services for heavy wire and ribbon along with thin wire applications.



10th Annual International Wafer-Level Packaging Conference Exhibitor Opportunities

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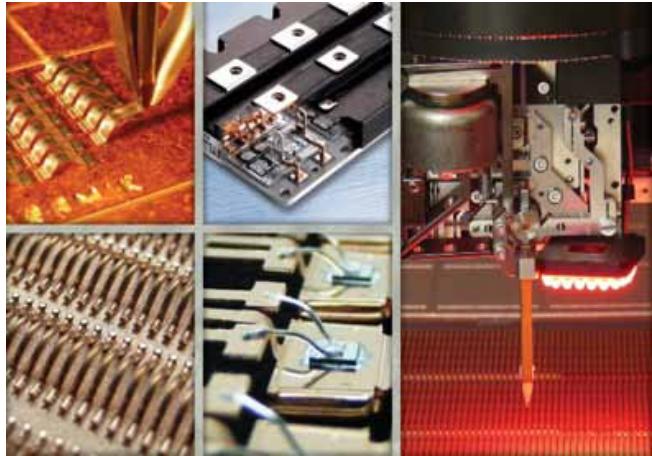
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Hesse Mechatronics -BONDJET BJ939 Heavy Wire Bonder

According to Hesse Mechatronics, the BONDJET BJ939 heavy wire bonder is used for power electronics and automotive device applications. The tool can now work with heavy wire and ribbon on a single platform. The new application bonds both aluminum, gold, silver, or ribbon wire. It can work with 3 mil to 20 milwire and .075mm by .075 mm to .3mm by 2 mm on the same machine. Hesse also reports the bonder can place up to 3 wires a second, can complete and integrated pull test, and comes with a large travel table. Additionally, the bonder features E-Box™ optical tool adjustment. Process-integrated Quality Control (PiQC™) is said to measures true bond quality in real time and the in-air cut feature eliminates marking on die. [www.hesse-mechatronics.com]

Essemtec Debuts High Speed Jetter at SEMICON West

For the first time in North America, Essemtec, a Swiss manufacturer of production systems for electronic assembly and packaging, will unveil its Scorpion high-speed jettter at SEMICON



Essemtec - Scorpion High Speed Jetter

West this July.

The Scorpion is a fully automatic jetting system in dispensing technology that is said to improve overall equipment efficiency. Absolute throughput is maximized with piezo jetting valves that enable the jetting of fluids over a wide range of viscosity with speeds of up to 800 Hz. Material use is reduced due to

a fluid box with capacity less than 50 nanoliters, thereby reducing waste. The fluid box is connected to the jet valve without tubing, which helps to minimize messy cleaning and maintenance operations are minimized. eDIS software provides context sensitive help. Point and touch features are intuitive to learn, and programming of dots, lines or various shapes is supported along with CAD import.

The Scorpion can be equipped with up to four valves or pumps, including jet valves, Archimedian screw valves,

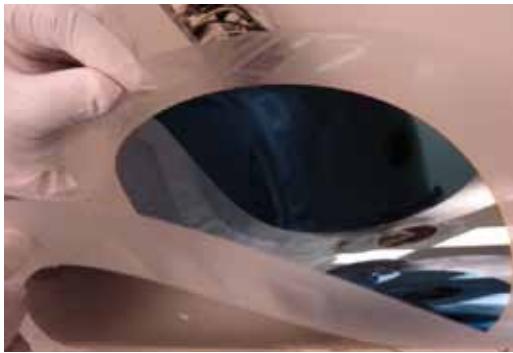
time pressure valves and slider valves to accommodate applications such as encapsulation, dam-and-fill, underfill, LED cavity, conductive adhesive, solder paste, phosphor silicon cavity fill and more.

Dow Corning and SÜSS MicroTec Report New Temporary Bonding Solution for 2.5D and 3D IC Packaging

The semiconductor industry's march toward broader 3D IC integration marked an important milestone with the report of an advanced new temporary bonding solution for 3D Through Silicon Via (TSV) semiconductor packaging. The breakthrough was unveiled during ECTC 2013, in a paper co-authored by Dow Corning and SÜSS MicroTec, a leading supplier of semiconductor processing equipment, and presented by Ranjith John, materials development & integration engineer at Dow Corning.

The paper, titled *Low Cost, Room Temperature Debondable Spin on Temporary Bonding Solution: A Key Enabler for 2.5D/3D IC Packaging*, details the development of a bi-layer spin-on temporary bonding solution that eliminates the need for specialized equipment for wafer pretreatment to enable bonding or wafer post-treatment for debonding. The solution is said to improve the throughput of the temporary bonding/debonding process to help lower the total cost of ownership (CoO).

"This advance underscores why Dow Corning values collaborative innovation. Combining our advanced silicone expertise with SÜSS MicroTec's knowledgeable leadership in processing equipment, we were able to develop a temporary bonding solution that met all critical performance criteria for TSV fabrication processes. Importantly, the spin coat-bond-debond process we detailed in our co-authored paper takes less than 15 minutes, with room for further improvement," said John. "Based on these results, we are confident that



Dow Corning and SÜSS MicroTec - Temporary Bonding Solution for 2.5D and 3D IC Packaging

this technology contributes an important step toward high-volume manufacturing of 2.5D and 3D IC stacking."

Cost-effective temporary bonding solutions are a key enabler for 2.5 and 3D IC technology. However, in order to be competitive, candidate temporary bonding solutions must

deliver a uniformly thick adhesive coat, and be able to withstand the mechanical, thermal and chemical processes of TSV fabrication. In addition, they must subsequently debond the active and carrier wafers without damaging the high-value fabricated devices.

Through their collaboration, Dow Corning and SÜSS MicroTec were able to develop a temporary bonding solution that met all of these application requirements. Comprising an adhesive and release layer, Dow Corning's silicon-based material is optimized for simple processing with a bi-layer spin coating and bonding process. Combined with SÜSS MicroTec equipment, the total solution offers the benefits of simple bonding using standard

manufacturing methods. In their co-published paper, the collaborators report a solution exhibiting a total thickness variation of less than 2 µm for spin-coated films on either 200 or 300mm wafers. The bonding material exhibited strong chemical stability when exposed to phosphoric acid, nitric acid, organic solvents and other chemicals familiar to TSV fabrication. In addition, the bonding solution and paired wafers showed good thermal stability when exposed to the 300°C temperatures common to the TSV process.

Assembléon to present its Hybrid Solution at SEMICON West

For many the existence of PCB assembly machines in the backend market is still unknown or considered strange. Rapid technology changes and miniaturization have caused an equally

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BESI	www.besi.com	2&3
Brewer Science	www.brewerscience.com	57
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DL Technology	www.dltechnology.com	35
Emulation Technology	www.emulation.com	49
Essai	www.essai.com	IFC
E-tec Interconnect	www.e-tec.com	60
EV Group	www.evgroup.com	51
HCD Corp	www.hcdcorp.com	56
Honeywell	www.honeywell-radio.com	9
IMAT Inc.	www.imatinc.com	33
Indium Corporation	www.indium.us/E033	41
Ironwood Electronics	www.ironwoodelectronics.com	17
IWLPC	www.iwlpc.com	69
JF Microtechnology	www.jftech.com.my	11
KYEC	www.kyec.com	32
Kyzen Corp	www.kyzen.com	4
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Plastronics	www.h-pins.com	45
Quartet Mechanics	www.quartetmechanics.com	53
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Rudolph Technologies	www.rudolphtech.com	OBC
SEMI	www.semiexpos.org	65
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Sierra Electronics	www.tapessplice.com	25
SMTA International	www.smta.org/smtai/vip	71
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Assembléon - Hybrid Solution

rapid shift of specialized equipment, normally present in traditional PCB assembly, to move into backend packaging industry. As a result, Assembléon, supplier of PCB assembly tools, has announced it will attend SEMICON West 2013 and SEMICON Taiwan 2013 to present its hybrid solutions to the semiconductor manufacturing community.

According to Assembléon, its Hybrid system has a unique proposition in the PCB assembly market, as it is the only system incorporating a single/pick single/place concept. The advantage of such a system is that it can be fully optimized, monitored and controlled during the complete pick, dip and place cycle. The incorporated low-force closed-loop placement process reportedly ensures that even the thinnest devices are placed accurately and its incorporated impact control takes care that no impact forces are applied during placement. Assembléon claims it is therefore the only system that has very high production yields with an established placement defect rate lower than 1 defect/million placements (< 1 dpm). Besides the placement quality, it brings the traditional ingredients of the PCB assembly, such as application flexibility, very high speed, accuracy, efficiency and cost control, along into the back-end market.

The company claims this cross-over platform combines high speed passive placement with high speed flip chip placement with reported accuracies at less than 10µm at any location on the PCB at any angle. The controllable placement Z-axis adapts its placement height search algorithms for different heights, optimizing its placement force for 2.5D mounting, package on package (PoP) or embedded passive and active device applications.

During the SEMICON West Exhibition, Assembléon representatives will discuss the concepts, advantages, current references, and technology roadmap of its hybrid equipment.

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