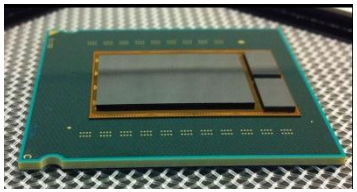
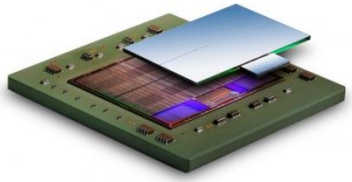
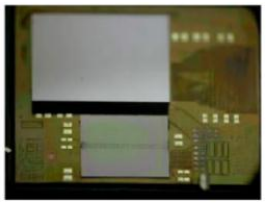
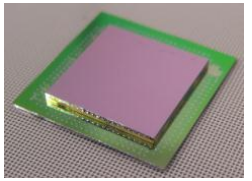
3D Silicon & Glass Interposers

August 2012

Sample

YOLE Développement

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This is our second edition of this report

3D integration has been on everybody's minds for over 5 years throughout the semiconductor industry, and it fast met commercial success for a few applications including MEMS, sensors and power amplifiers. However, past this initial euphoria, and even though technical developments comforted most observers that mass volume adoption of 3D was not out of reach, some technical and supply chain hurdles proved higher than anticipated.

2.5D integration by means of 3D glass or silicon interposers was then exposed by experts as a necessary stepping stone to full 3D integration. In our first report on 3D interposers and 2.5D integration in 2010, after listing the various applications of this technology trend and their drivers, we showed that glass and silicon interposers were expected to become high volume necessities rather just high performance solutions for a few niche applications.

In this 2012 edition of the report, we show more evidence of our findings from 2 years ago: after refining the applications and drivers of 3D interposers and 2.5D integration, thanks to detailed forecasts, Yole Developpement estimates that far from being a stepping stone technology to full 3D integration, 3D interposers and 2.5D integration is emerging as a mass volume long-lasting trend of the semiconductor industry.

What's new since our 2010 report on interposers?

- In 2010, we started the report by asking « are 3D glass/silicon interposers a myth, a high-end solution for niche applications or a high volume necessity? », and we concluded that it was nothing like a myth, and that it was already entering high volumes for a limited number of applications

- As of 2012, we confirm this conclusion from 2 years ago, especially since we collected many proofpoints: press releases, investments, company packaging roadmaps,… All concur that 3D silicon/glass interposers are becoming a key piece of the 2010-2020 semiconductor technology puzzle

- Drivers by application are now clearer than 2 years ago, which allowed us to accurately forecast the growth of this industry trend.

- First demonstrators have been made in 2011, especially the Xilinx Virtex 7 FPGA, supported by motivated supply chain leaders (TSMC and Amkor), which proved not only feasibility of such complex 2.5D modules, but also their benefits: higher bandwidth, higher integration capacity, lower power consumption, managed thermal dissipation.

- The remaining questions are: how fast and at what, and for which exact applications and through which players is this trend going to succeed? These are the main focus points of this 2012 report

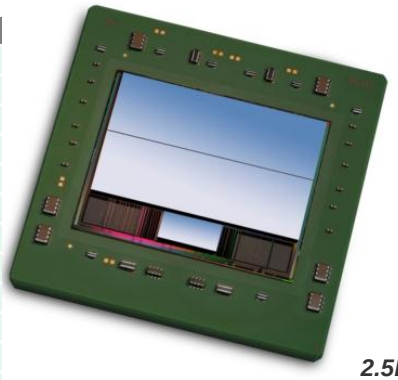
Recent key press announcements

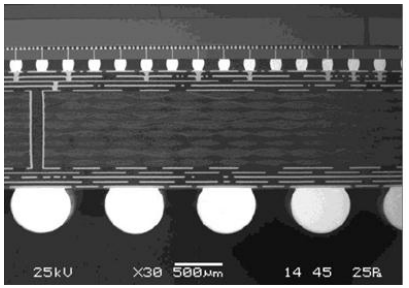
linked to 2.5D silicon / glass interposer concepts

/-Micronews — THE DISRUPTIVE SEMICONDUCTOR TECHNOLOGIES WEBSITE

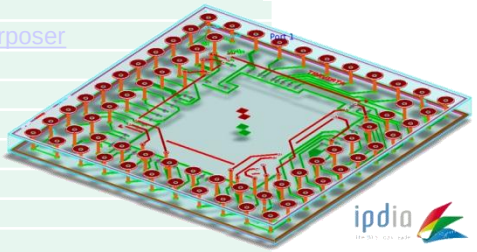
- **Below is a non-exhaustive list of articles related to 2.5D/3D interposers recently published on www.i-micronews.com (Yole's industry news website)**

Date	Announcement
2012	Xilinx ships world's first heterogeneous 3D FPGA using 2.5D silicon interposer
2012	Are silicon interposers "luxury" solutions?
2012	2.5D interposers look increasingly like the near term, high performance solution
2012	UMC's new 300mm fab to propose leading foundry services for BSI, 2.5D interposer and 3DIC
2012	Focus on Qualcomm 2.5D Interposer and 3DIC roadmap
2012	2.5D Interposer and 3DIC seen as innovation enabler!
2012	2.5D Interposers with stacked FPGA enable silicon convergence
2012	Altera and TSMC develop heterogeneous 3DIC test vehicle with 2.5D Interposer
2012	AGC reveals high speed drilling technology for 2.5D glass interposer
2012	IBM demonstrate voltage regulator integration on 2.5D silicon interposer platform
2011	TSMC and Arteris to develop 2.5 silicon-interposer-based NOCs
2011	SiBDI to commercialize Silicon interposer HB-LED submount
2011	VisEra enters LED lighting sector with silicon wafer level package interposer
2011	CEA-Leti & Shinko to partner on Silicon interposers development
2011	A*STAR and Tezzaron to develop 2.5D & 3D Silicon Interposers
2011	TSMC latest developments on TSV and Silicon Interposer
2011	2.5D interposers: a closer look
2011	Xilinx 2.5D FPGA's coming off the production line: a closer look
2011	Betting on through silicon vias in glass substrates
2011	Through-Silicon via supplier ALLVIA attains ITAR registration
2011	Xilinx and Amkor discuss 3D interposer programs
2011	IME & Elta Systems to develop TSV silicon interposers for Power Amplifier applications
2011	PlanOptik presents holed Glass carrier substrate for Thin wafer Handling of TSV wafers
2010	IBM & Semtech team up for 3D TSV interposers
2010	ALLVIA to present advanced logic applications for silicon interposers
2010	NEPES silicon interposer module contains IPD and TSV
2010	Xilinx brings 3D TSV interconnects to commercialization phase in digital FPGA world
2010	Why the secrecy surrounding TSI development?
2010	TSMC reveals plan for 3DIC designs based on Silicon interposers & TSV
2010	ALLVIA integrates Thin-film IPD capacitors in Silicon interposers
2010	ASE gears up for 2.5D, 3D IC commercialization
2010	IPDIA opens multi-parties 3D TSV Silicon Interposer Program
2010	ALLVIA, completes reliability testing of silicon interposer for stacked semiconductors
2009	TSV foundry ALLVIA & SunSil ready to commercialize 3D Silicon interposers
2008	R&D Consortium readies for Low Cost WLP of Silicon Interposers
2008	Silicon Interposers Wait for an Application
2008	New 3D-consortium formed focusing on Si-interposer technologies

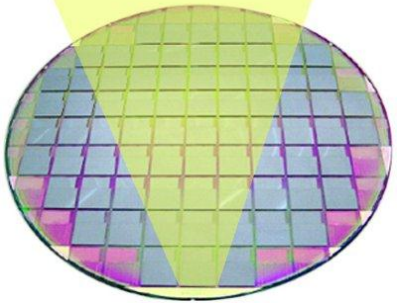




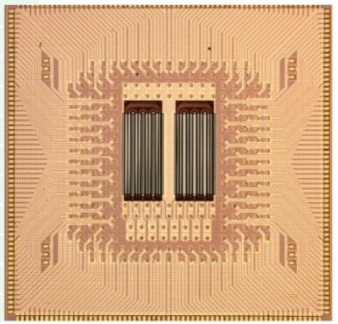
Xilinx Virtex7 FPGA
2.5D silicon interposer design



Ipdia's silicon interposer open platform



Altera's FPGA supported by TSMC's CoWoS 2.5D interposer platform



IBM's silicon interposer with integrated power inductors

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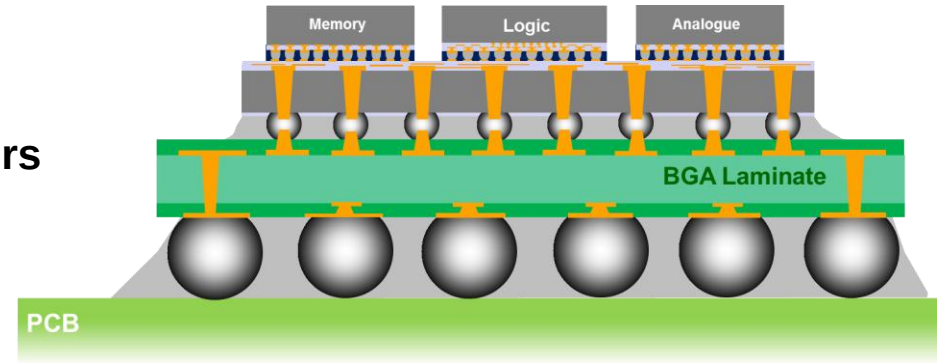
Choosing between 2.5D & 3D

- 2.5D « system partitioning » interposers will be used in the long term for those applications which cannot go the full 3D integration way due to high power losses of the logic die, neigboring and thus affecting the memory ICs

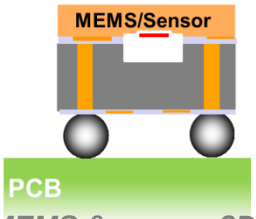
	several standard packages	2.5D SiP	3D SiP
Technology and infrastructure maturity as of Q3 2012	+	-	--
Electrical bandwidth	-	+	++
Power consumption	-	+	+
Heterogeneous integration	-	+	+
Size	-	+	++
Thermal Management	++	+	-

Silicon/Glass 3D Interposer Technology Segments

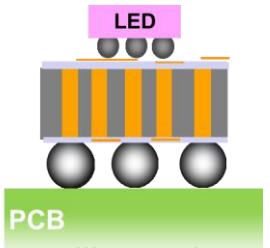
- **We identified the following technology segments for 3D interposers:**
  - MEMS and sensors 3D capping interposers
  - "System partitioning" interposers
  - Interposers for CMOS image sensors
  - 3D LED silicon substrates
  - 3D Integrated Passive Devices (IPDs)
  - Miscellaneous interposers



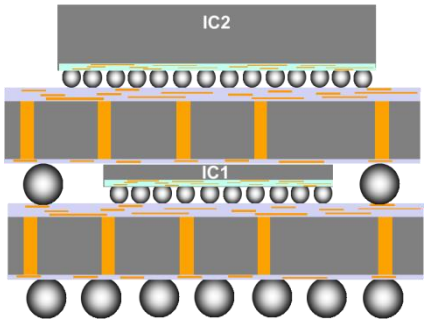
« System partitioning » interposers



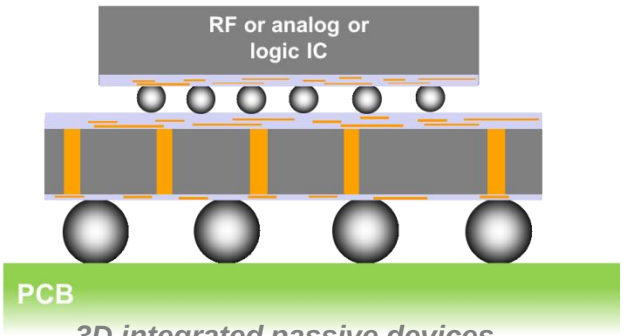
MEMS & sensor 3D capping inteposers



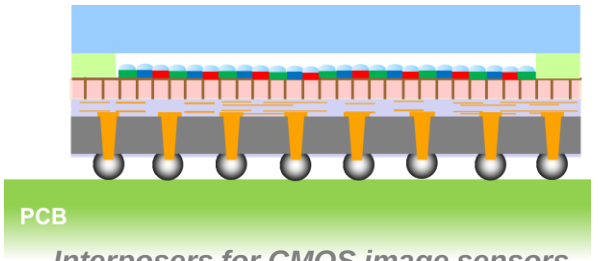
3D LED silicon submounts



Miscellaneous interposers



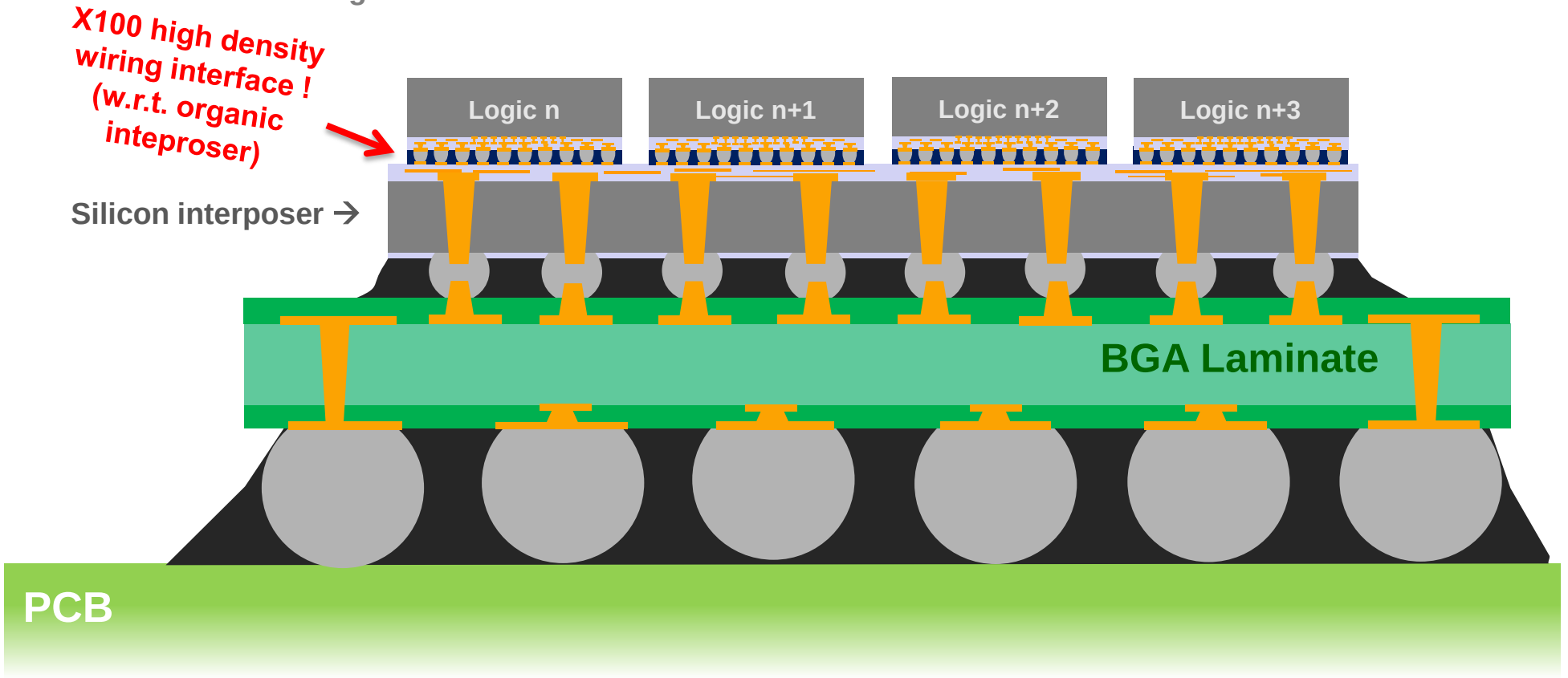
3D integrated passive devices



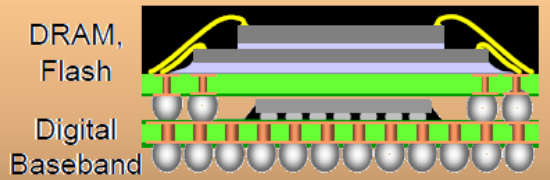
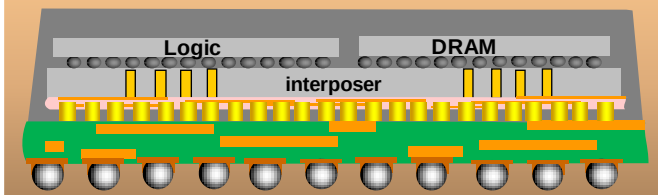
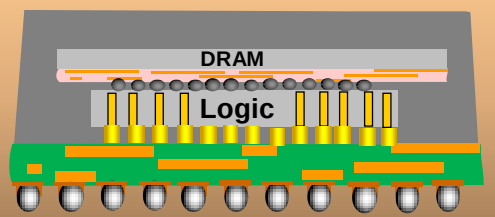
Interposers for CMOS image sensors

2.5D interposer solution
for Large die Logic applications *(FPGA, ASICs, DSP, etc…)*

- **Several 'slices' instead of one die: 3D-SOC re-partionned logic design**
  - **Increase CMOS manufacturing yield (because of smaller die size)**
  - **High density wiring at the surface of the 4 layer copper damascene silicon interposer wafer**
    - → **breakthrough in COST versus POWER CONSUMPTION versus PERFORMANCE**

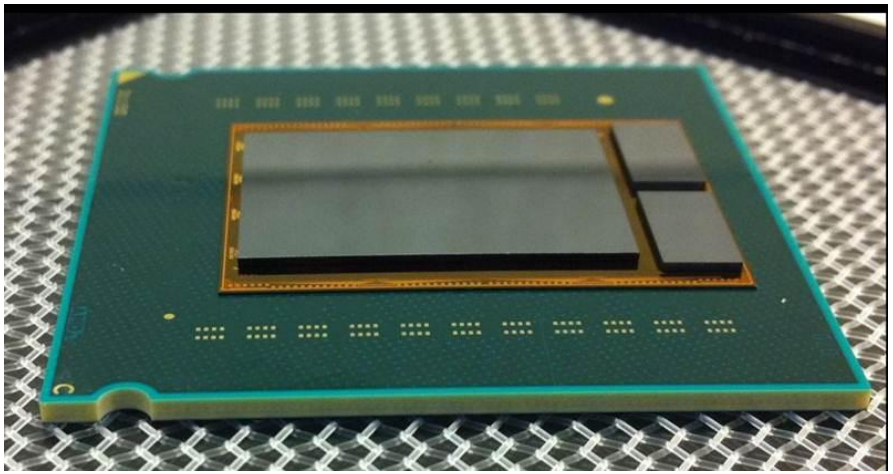


Logic + memory integration:
competing solutions

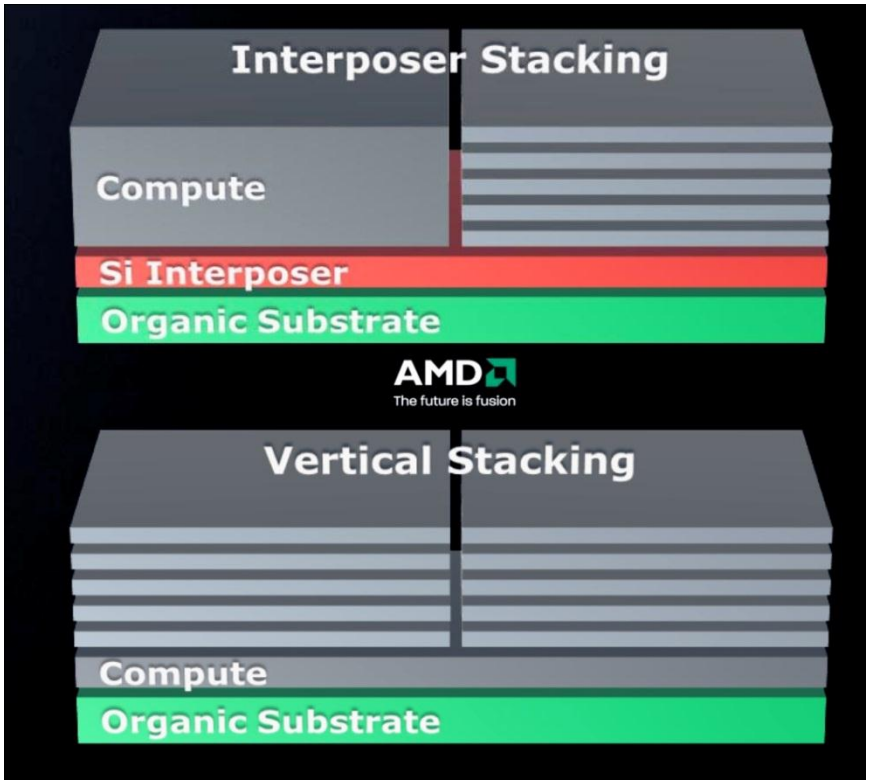
	pros	Cons	Apps
PoP 	•Clear cost ownership: bottom package belongs to logic manufacturer, top package goes to memory manufacturer, 3D integration by OEM •Flexible sourcing of DRAM •Flexible test of each separate stack	•Package height •Long path DRAM to logic = limited bandwidth •Narrow IO interface	Baseband ICs
2.5D with Interposer 	•Short DRAM to Logic interconnections for high frequency memory access •Wide IO interface for memory access with high bandwidth •Low package height •Thermal management	•Cost of interposer •Large package footprint area	Networking & storage ASICS, CPU, GPU
3D 	•Very short interconnections DRAM to logic •Very wide IO interface for high bandwidth memory access	•No DRAM sourcing flexibility before IO standardization • Thermal management: heat propagation logic to DRAM •Cost of RDL on DRAM (before standardization)	Application Processors for tablets & smartphones

Example of performance driven 2.5D integration
GPU for gaming

- **Sony PS4 (to be released for the 2013 holiday season or in 2014) will have a GPU on interposer with a 512-wide data bus and on interposer memory**
- **Will probably be an AMD chip**
- **Future gaming platforms will offer 3D imagery, which requires fast & high bandwidth computing power.**
- **2.5D is unanymously praised as the solution for this purpose**
- **"GPU-RAM Bandwidth is the key factor for rendering performance" – Sept 2011,** Teiji Yutaka , SVP Technology Platform, Sony Computer Entertainment

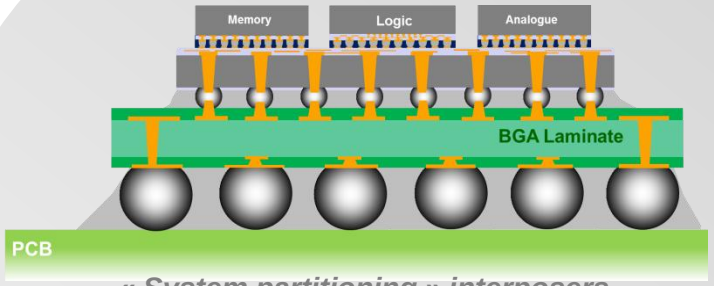


An interposer module for (Yole assumption) an AMD GPU demonstrator
Courtesy of Global Foundries, 2012



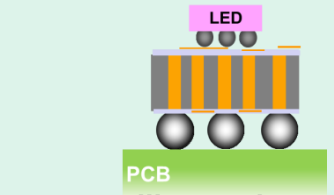
2 types of interposers

Fine-pitch Interposers

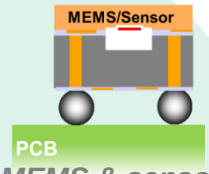


« System partitioning » interposers

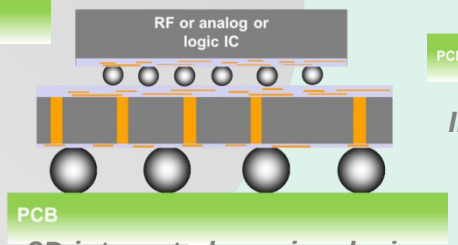
Coarse Interposers



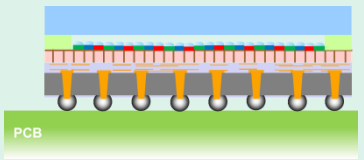
3D LED silicon submounts



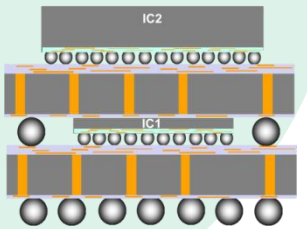
MEMS & sensor 3D capping inteposers



3D integrated passive devices



Interposers for CMOS image sensors



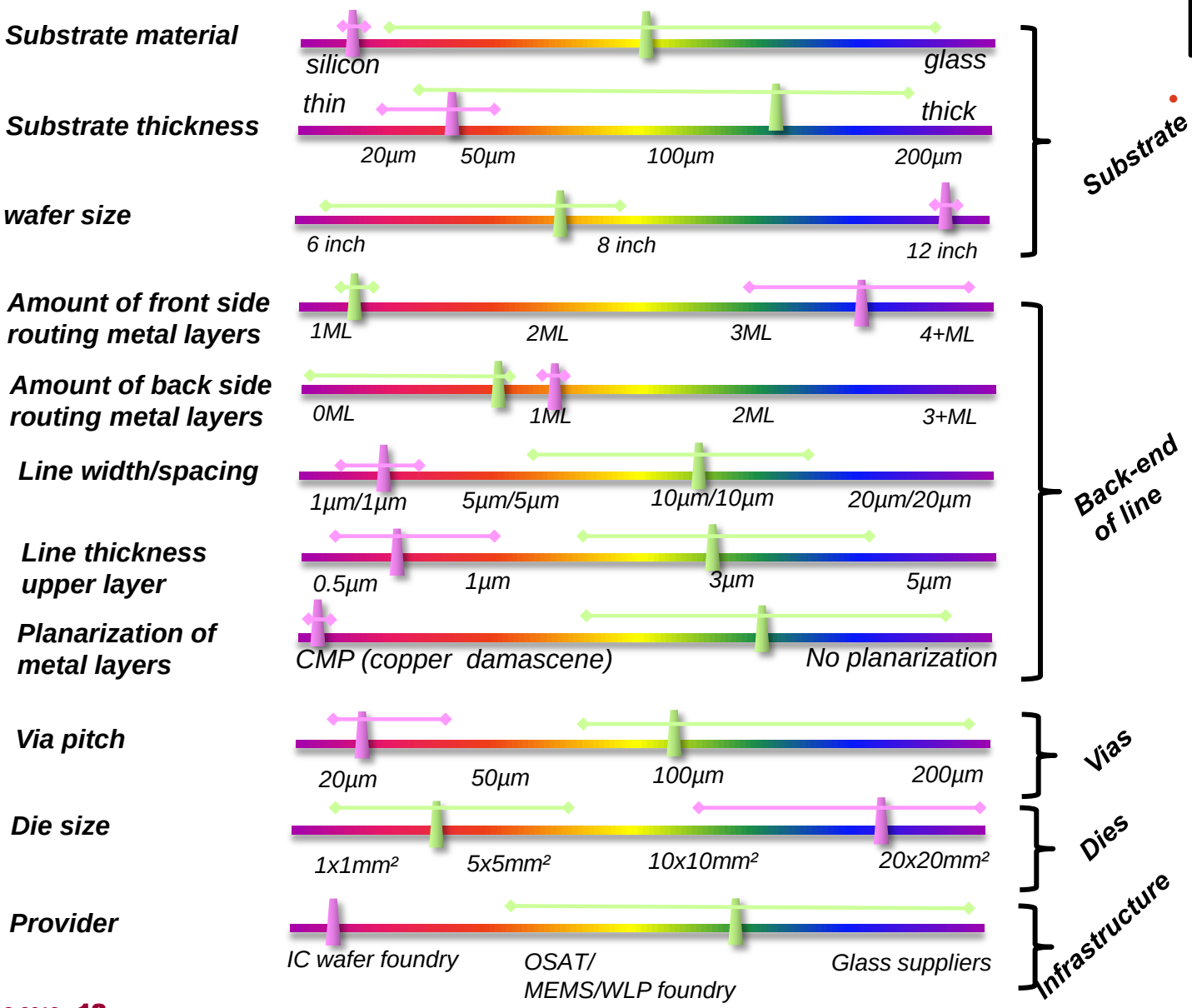
Miscellaneous interposers

- **High-end and high power logic applications (GPU/CPU/FPGA/ASIC)**
  - Performance (bandwidth & energy consumption) driven
  - thin (50-100µm) & fine-pitch (via diameter 10-15µm), microbumping below 50µm
  - Fine line/spacing below 3µm/3µm
  - Manufactured by CMOS foundries on 300mm silicon wafers with design rules close to the back-end-of-line (BEOL) of CMOS 65nm

- **Analogue/MEMS/Sensors/Lighting**
  - Size and cost driven
  - Any thickness: 20µm to 500µm, large via diameter (30µm-500µm)
  - Line/spacing above 3µm/3µm
  - Manufactured by MEMS foundries or OSATs or IDMs or glass manufacturers on glass or silicon wafers or panels

Coarse versus Fine-pitch Interposers

characteristics As of 2012



- **We generally consider that there technically are 2 types of interposers**
  - **Fine-pitch interposers for high-end and high power logic applications (GPU/CPU/FPGA/ASIC)**
    - They feature fine geometries down to 1µm
    - They are manufactured by IC wafer foundries (on CMOS 65nm 300mm diameter type of wafers)
    - Dies are generally larger (larger than 100mm²)
  - **Coarse interposers for Analogue/MEMS/ Sensors/Lighting**
    - They feature larger geometries
    - They are manufactured by OSATs, glass suppliers or WLP foundries

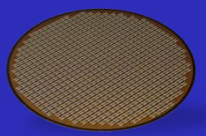
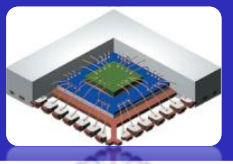
3D silicon/glass interposers

Who is doing what? Main players

Coarse pitch interposers

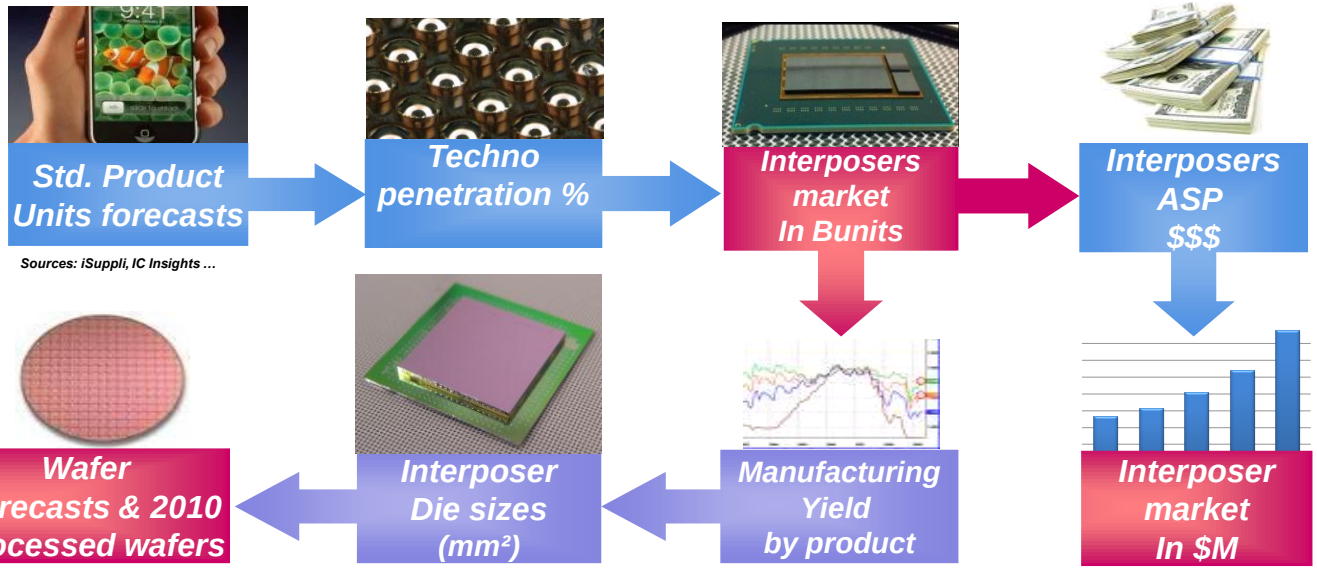
Fine pitch interposers

any

	Wafer /panel supply	TSV/TGV making	RDL	test of interposer	Bumping	Packaging and assembly	final test
							
Silicon substrate makers							
Glass substrate makers	HOYA						
IC wafer foundry		GLOBAL FOUNDRIES		UMC		tsmc	*New TSMC model*
MEMS wafer foundry (or IPD wafer foundry)		DALSA		silex MICROSYSTEMS		imt	
OSATs		STATSChipPAC, Amkor Technology		STATSChipPAC, Powertech Technology Inc., Amkor Technology, SPIL			
PCB manufacturers		SHINKO, IBIDEN CO.,LTD.					
IDMs			intel	ST		SAMSUNG	

Yole's Market Forecasting Methodology

- **Yole's market forecasting methodology is based on the "top-down meets bottom-up" analyses**
  - **2 complementary analyses are carried out and cross-checked:**
    - The top-down analysis derives the wafer forecasts from an analysis of the end products where 2.5D interposers are expected, application by application, taking into account the penetration rate of the technology for each product type, as well as their yields and die sizes

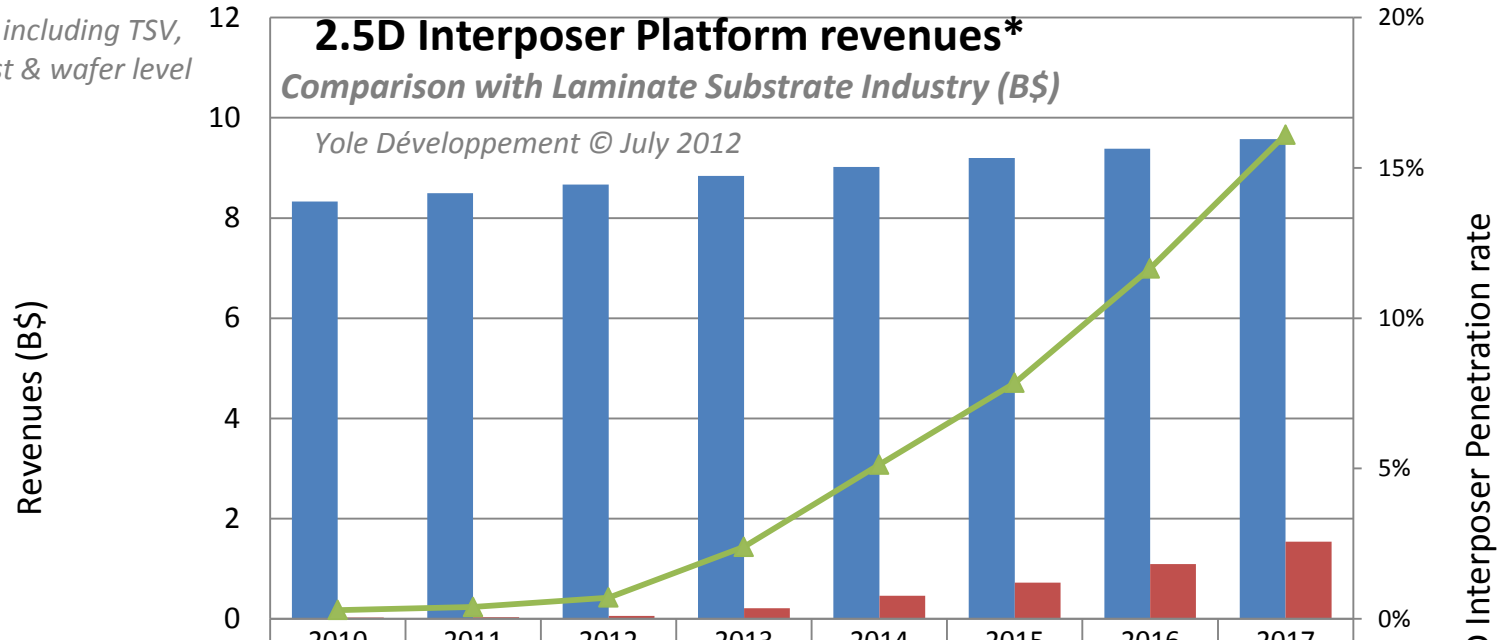


    - The bottom-up analysis is based on the evaluation of the worldwide production capacity evaluated through interviews of industry players (foundries, OSATs, equipment and material makers) and company revenue reports.

    - Throughout the following market forecast slides, we show forecasts from our top-down analysis, followed by the 2011 status of the processed interposer wafers through our bottom-up analysis

Interposers revenues within the context of IC Packaging substrates

** Middle End activity revenues including TSV, Filling, RDL, Bumping, wafer test & wafer level assembly*

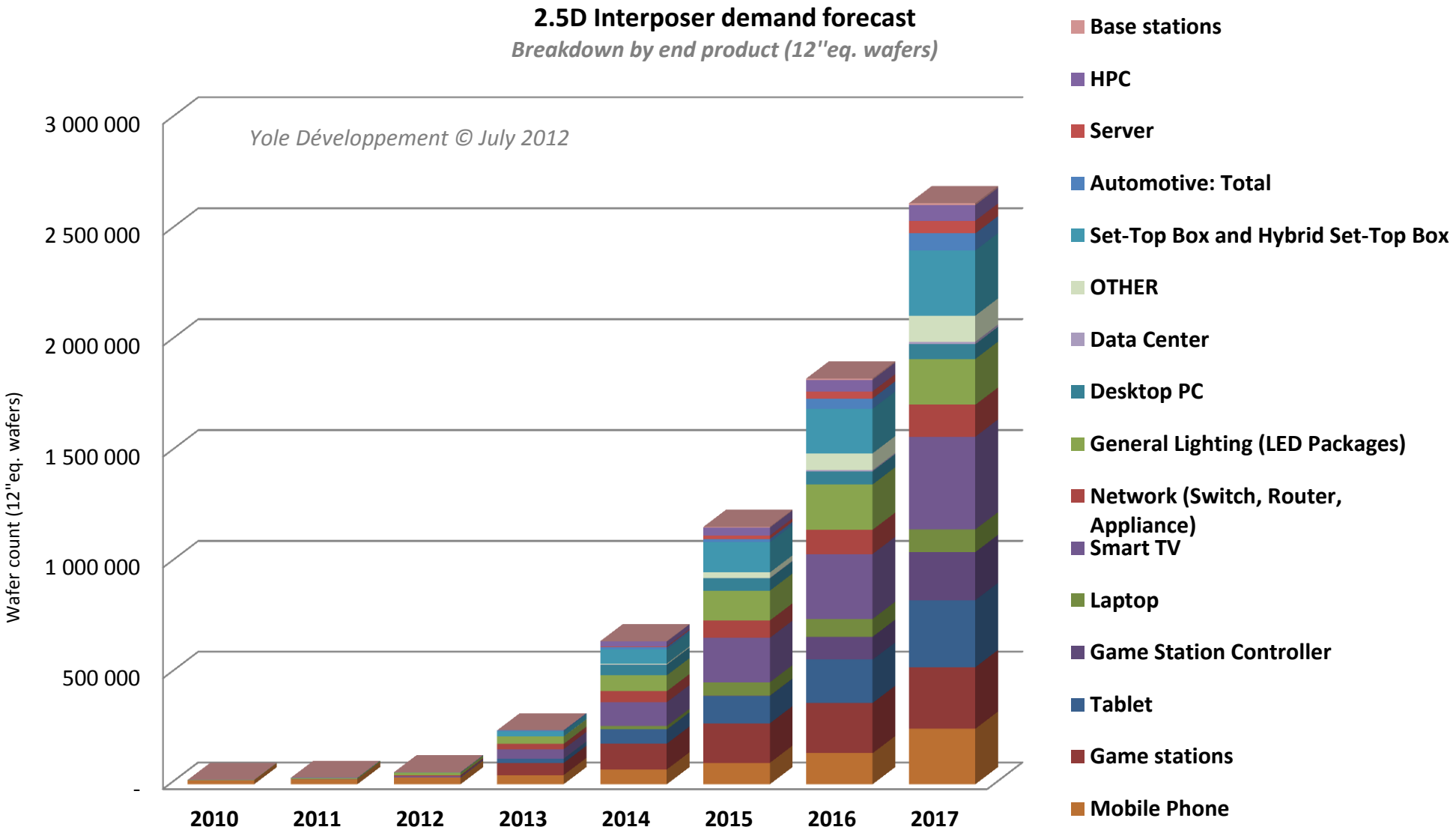


	2010	2011	2012	2013	2014	2015	2016	2017
IC Packaging Substrate Revenues	$ 8.3 B	$ 8.5 B	$ 8.7 B	$ 8.8 B	$ 9.0 B	$ 9.2 B	$ 9.4 B	$ 9.6 B
2.5D Interposer "Middle-End" Revenues	$ 0.0 B	$ 0.0 B	$ 0.1 B	$ 0.2 B	$ 0.5 B	$ 0.7 B	$ 1.1 B	$ 1.5 B
2.5D Interposer Technology penetration rate	0.3%	0.4%	0.7%	2.4%	5.1%	7.9%	11.7%	16.1%

- **Another way of looking at 2.5D expected revenues is – even if arguably – to compare them to the wide established market of IC Packaging substrates: after all, 2.5D/3D interposers are just another layer of vertical and horizontal interconnections inside the package**
- **This comparison speaks for itself: as of 2017, Yole expects the 2.5D/3D interposer revenues to reach 15% of the packaging substrate market value**

2.5D/3D interposer 2010-2017 wafer forecasts

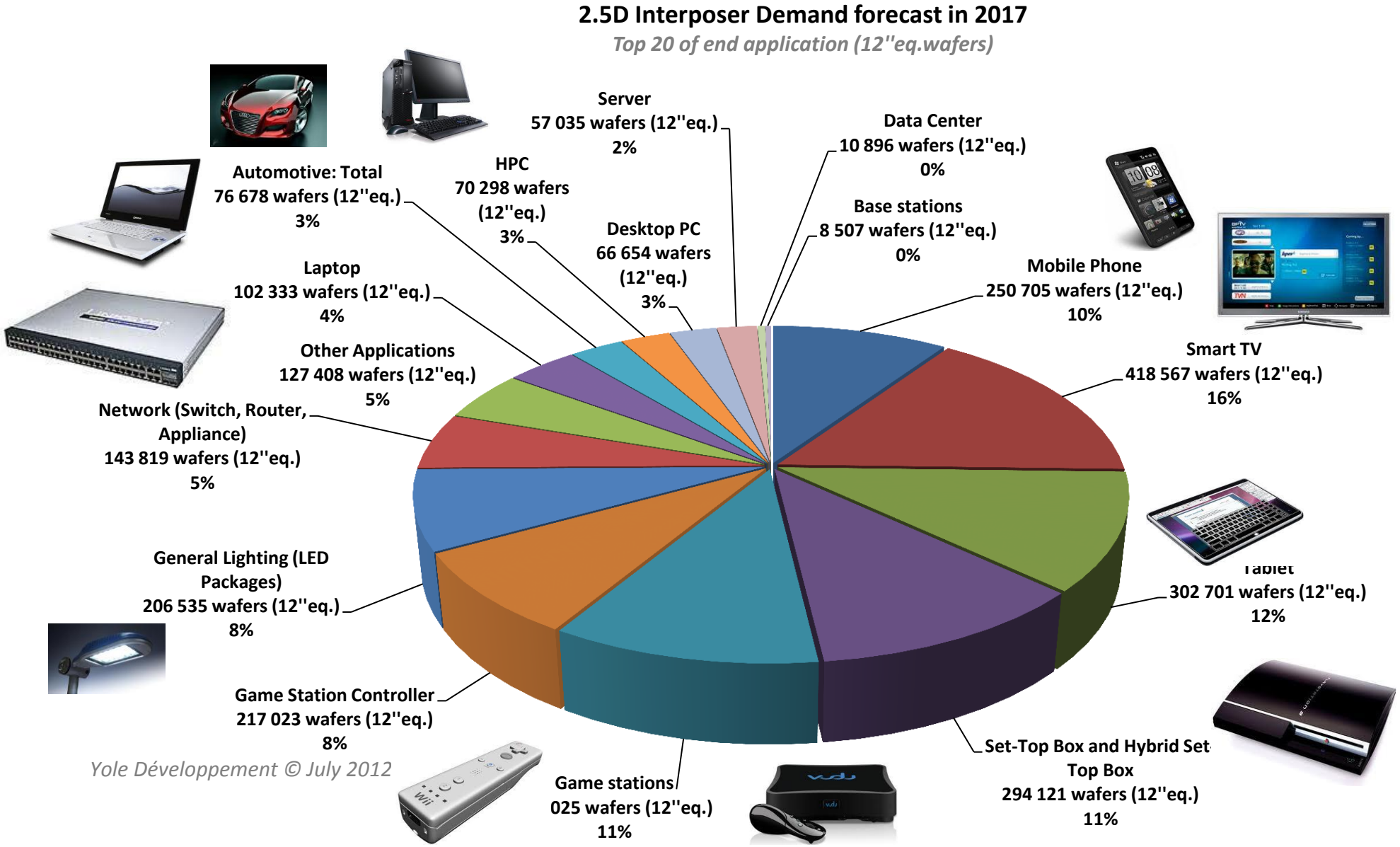
breakdown by end product



** Other = Missile, Machine Vision, Helicopter, Drone, Defense UAV, Civil UAV, Drilling systems, Guided munitions, Professional imaging, Infantry gear, Camera pill, Implantable CRM, Camcorder, Hearing aids, ATE, Trucks, Buses, PMP, MP3, PND, DSC, SLR, Femtocell, 3G Dongle*

2.5D/3D interposer wafer demand forecast in 2017

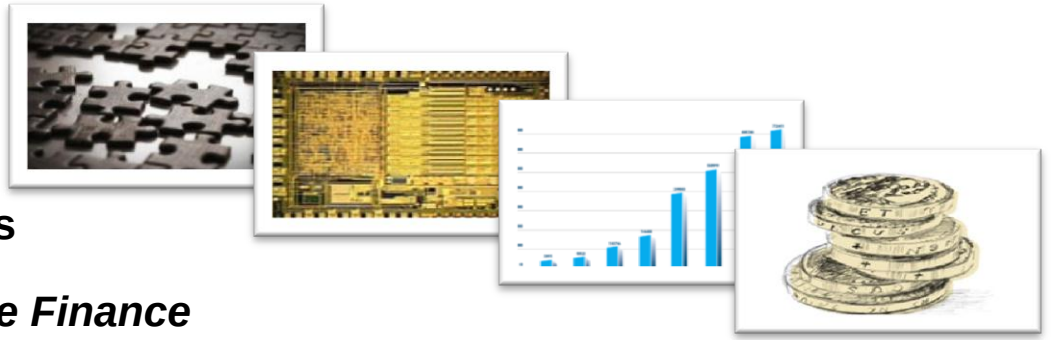
breakdown by end product



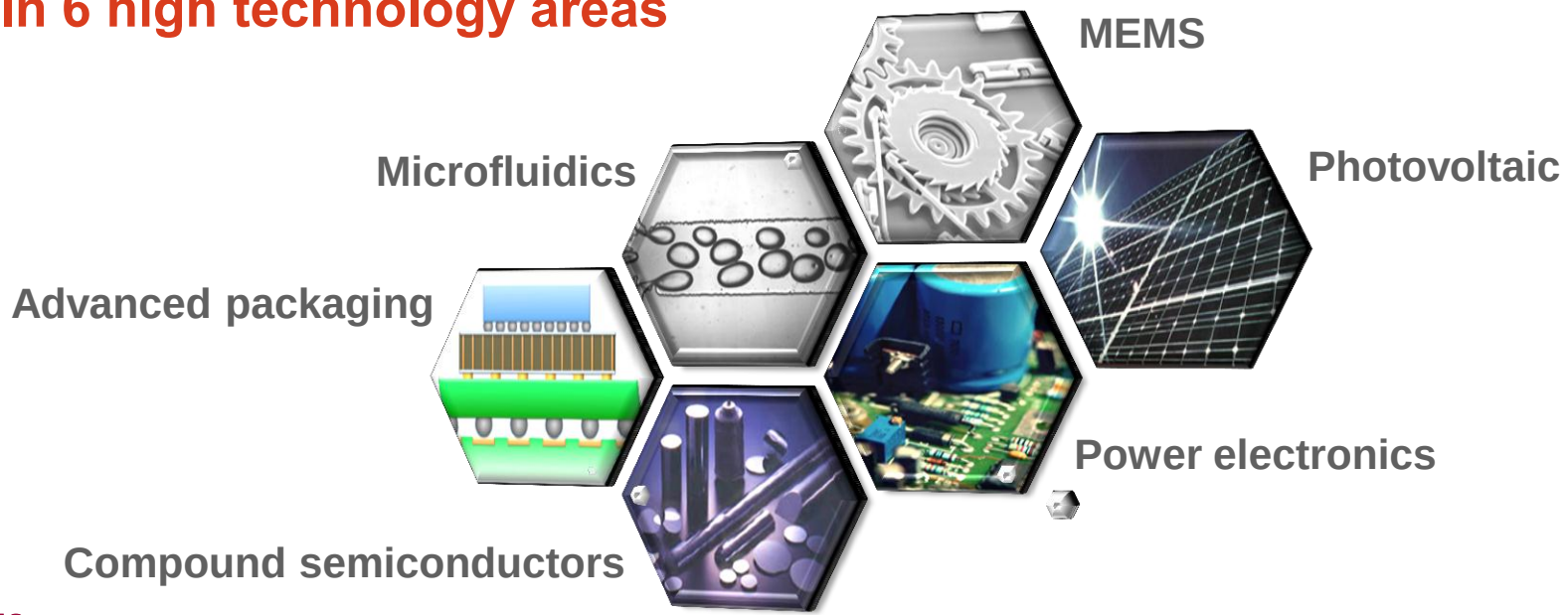
Presentation of Yole's activities

Yole Développement activity & services

- **Yole Développement provides powerfull tools and services…**
  - **Strategic analysis**
  - **Technology evaluation**
  - **Market Research & Marketing analysis**
  - **Specific services for investors by *Yole Finance***



- **…In 6 high technology areas**

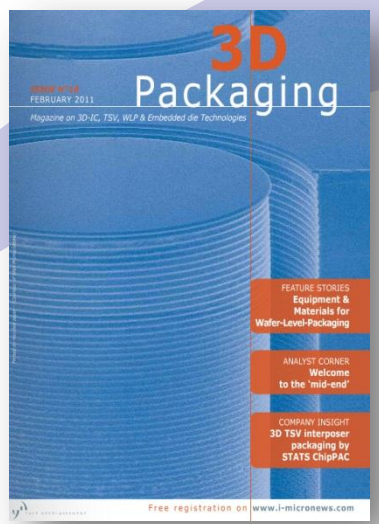


Yole activities in Advanced Packaging

YOLE DÉVELOPPEMENT

Media business

News feed / Magazines / Webcasts



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Reports

Strategy

Consulting services

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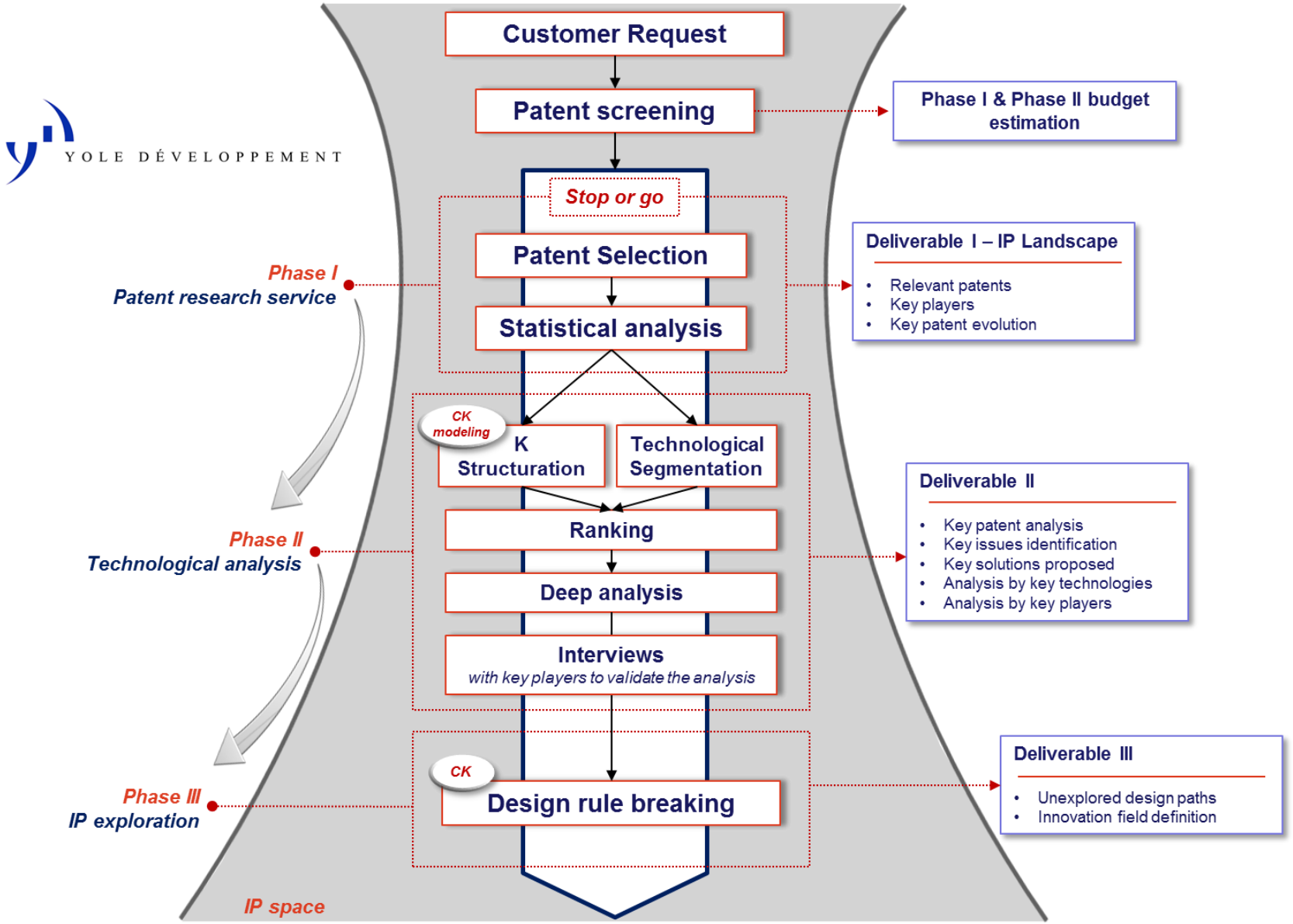
YOLE Développement

NEW service: IP analysis



Phase II depends on Phase I results. Phase III depends on phase II results.

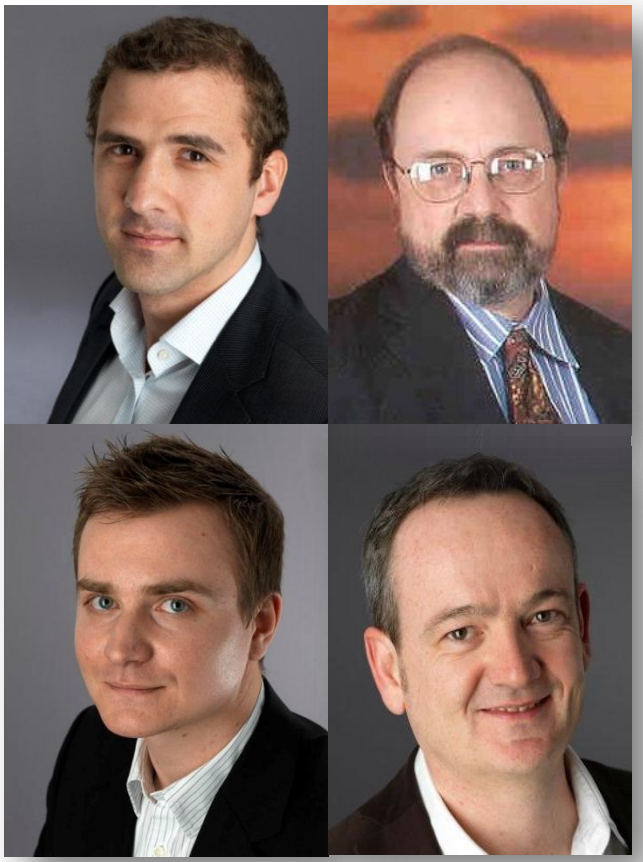
About Yole's Advanced Packaging Analysts team *(1/2)*

Jerome Baron

– Jerome is the business unit manager of the semiconductor packaging market research at Yole Developpement. He has been following the 3D packaging market evolution since its early beginnings at the device, equipment and material levels. He was granted a Master of Science degree from INSA-Lyon in France as well as a Master of Research from INL – Lyon Institute of Nanotechnology
Contact: *baron@yole.fr*

Lionel Cadix

– Lionel joined Yole after the completion of several projects linked to the characterization and modeling of high density TSV and 3DIC chip stacking in collaboration with CEA-Leti and STMicroelectronics during his PhD. He is author of several publications and 8 patents in the field of 3D Integration
Contact: *cadix@yole.fr*



Phil Garrou

– Phil recently joined Yole Développement forces as senior technical advisor in the fields of advanced packaging. Phil as more than 20 years extensive experiences in the semiconductor industry where he mainly served as global marketing manager for DOW Chemical's BCB polymer business

Contact: *garrou@yole.fr*

Jean-Marc Yannou

– Jean-Marc joined Yole Développement as technology and market expert in the fields of advanced packaging and Integrated Passive Devices. He has 15-years of experience in the semiconductor industry. He worked for Texas Instruments & NXP semiconductors where he was Innovation Manager for System-in-Package technologies

Contact: *yannou@yole.fr*

About Yole's Advanced Packaging Analysts team *(2/2)*

Amandine Pizzagalli

– **Amandine recently joined Yole Development Advanced Packaging and MEMS manufacturing teams after graduating as an engineer in Electronics, with a specialization in Semiconductors and Nano Electronics Technologies. She worked in the past for Air Liquide with an emphasis on CVD and ALD processes for semiconductor applications**

Contact: *pizzagalli@yole.fr*

Eric Mounier

– **Dr. Eric Mounier co-founded Yole Developpement in 1998. He is in charge of technology analysis for MEMS related manufacturing technologies within the company. In the 3D Packaging area, Eric has developed a unique Cost modeling tool "TSV+" able to simulate to the cost of ownership of several different Through-Silicon-Vias and 3D integration scenarios**

Contact: *mounier@yole.fr*