

Chip Scale Review®

ChipScaleReview.com

The Future of Semiconductor Packaging

Volume 24, Number 2

March • April 2020

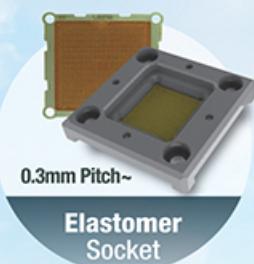
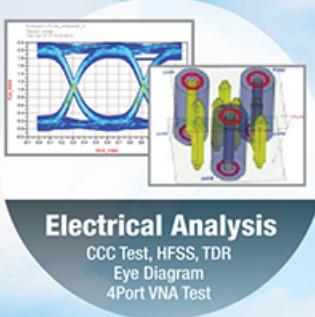
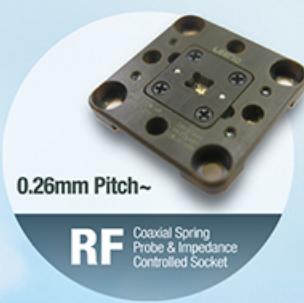
Antenna in package (AiP) technology for 5G growth
page 12

- Laser assisted flip-chip bonding
- Maskless lithography for MEMS and AP
- Post Moore's Law and quantum electronics
- Die-to-wafer hybrid bonding for 2.5D and 3D integration
- Holistic approach to improve the reliability of sub-5µm L/S Cu RDLs

Subscribe



LEENO's 100% In-house Manufacturing Provides its Customers with the Best Quality & Delivery.



CONTENTS

March • April 2020
Volume 24, Number 2



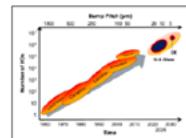
Implementing 5G technology requires transmission of large amounts of data, reliable connections, quicker response time, and better coverage. Fully-integrated RF front-end modules using a system in package (SiP) that includes antenna in package (AiP) technology, double-sided assembly, advanced wafer-level redistribution layer (RDL), passive component integration, and sophisticated RF shielding techniques provide the most advanced 5G package.

Image courtesy of Amkor

DEPARTMENTS

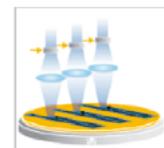
5 Post-Moore's Law electronics: now, until quantum electronics

Rao R. Tummala
[Georgia Tech]



9 Maskless lithography for MEMS and advanced packaging

Paul Lindner
[EV Group]



54 Industry News



Amkor has the capabilities and experience to ensure **automotive success**.

Automotive customers require suppliers that have the highest levels of experience, technical capability and quality.

As a stable, long-term OSAT, Amkor partners with semiconductor customers supplying automotive Tier 1s and OEMs.

We provide technology expertise, intelligent package design, quality systems based on automotive standards and highly capable automotive-grade facilities.

Enabling the Future

www.amkor.com ► sales@amkor.com





invent

innovate

implement

www.EVGroup.com

ACCELERATING HETEROGENEOUS INTEGRATION

- EV Group establishes Heterogeneous Integration Competence Center™ to accelerate new product development fueled by heterogeneous integration and advanced packaging
- Open access innovation incubator for EVG customers and partners across the microelectronics supply chain, guaranteeing the highest IP protection standards
- Combining EVG's world-class wafer bonding, thin-wafer handling and lithography products and expertise, as well as pilot-line production facilities and services
- Leveraging the state-of-the-art cleanroom facilities at EVG's headquarters in Austria, supported by EVG's worldwide network of process technology teams

GET IN TOUCH to discuss your manufacturing needs
HeterogeneousIntegration@EVGroup.com



STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Lawrence Michaels Managing Director/Editor

lmichaels@chipscalereview.com

Debra Vogler Senior Technical Editor

dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Steffen Kröhnert - Advanced Packaging

steffen.kroehnert@esp-consulting.com

John L. Lau, Ph.D - Advanced Packaging

john_lau@unimicron.com

Ephraim Suhir, Ph.D - Reliability

suhire@aol.com

Rao R. Tummala, Ph.D - Advanced Packaging

rao.tummala@ece.gatech.edu

EDITORIAL ADVISORS

Andy Mackie, Ph.D (Chair) - Indium Corporation

Rolf Aschenbrenner, Dipl.-Phys. - Fraunhofer IZM

Arun Gowda, Ph.D - GE Global Research

John Lau, Ph.D - Unimicron

Leon Lin Tingyu, Ph.D - National Center for Advanced

Packaging (NCAP China)

SUBSCRIPTION—INQUIRIES

Chip Scale Review

All subscription changes, additions, deletions to any and all subscriptions should be made by email only to subs@chipscalereview.com

Advertising Production Inquiries:

Lawrence Michaels

lmichaels@chipscalereview.com

Copyright © 2020 Haley Publishing Inc.

Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. In the U.S. subscriptions by first class mail are \$125 per year. Subscriptions outside of the United States are \$225 per year to other countries.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January–February, March–April, May–June, July–August, September–October and November–December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine P.O. Box 2165, Morgan Hill, CA 95038

Printed in the United States



Volume 24, Number 2
March • April 2020

FEATURE ARTICLES

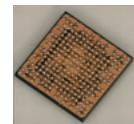
12 Antenna in package (AiP) technology for 5G growth

*Curtis Zwenger
[Amkor Technology, Inc.]*



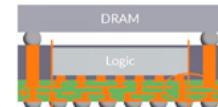
17 Advanced FOWLP for small form factor and high-performance microcontroller apps

*Gaurav Sharma
[NXP Semiconductors]*



23 Holistic approach to improve the reliability of sub-5µm L/S Cu RDLs

*Ralf Schmidt
[Atotech Group]*



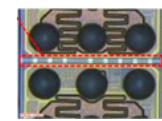
29 Die-to-wafer hybrid bonding for 2.5D and 3D integration

*Laura Mirkarimi
[Xperi Corporation]*



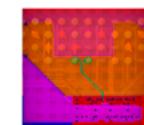
36 Navigating dicing on increasing complex shrinking die

*M. Todd Wyant
[Texas Instruments]*



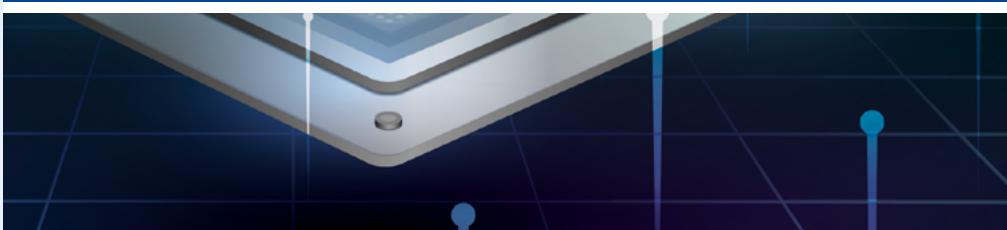
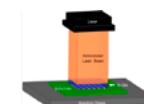
41 Going beyond traditional scaling with SiP

*Yoko Fujita
[Zuken]*



45 Laser assisted flip-chip bonding

*Nokibul Islam
[JCET]*



TestConX
Official Publication Sponsor

ECTC
Official Media Sponsor

IWLPC 2020
17th International Wafer-Level Packaging Conference
Co-Host & Organizer

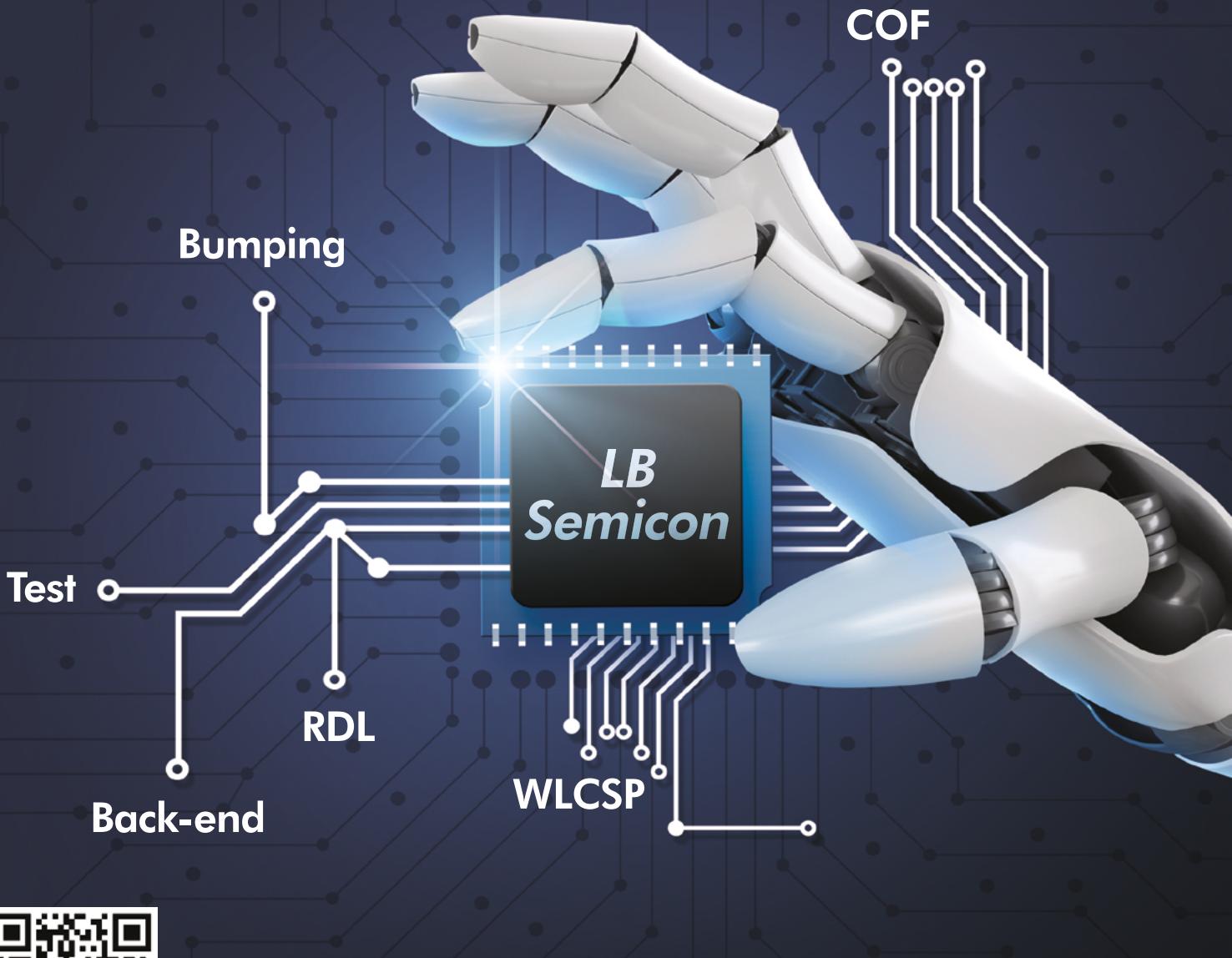
World No.1 Specialized Packaging Company



LB Semicon

We create abundance in life through technology
Always your business partner,

LB Semicon



► Webpage QR code
www.lbsemicon.com

www.facebook.com/lbsemicon

138, Cheongbuksandan-ro, Cheongbuk-eup, Pyeongtaek-si, Gyeonggi-do, Korea
TEL +82-31-680-1600 FAX +82-31-680-1798

GUEST EDITORIAL



Post-Moore's Law electronics: now, until quantum electronics

By Rao R. Tummala [Georgia Tech]

Moore's Law has been the driving engine for science, technology, manufacturing, hardware, software, systems, and applications, contributing to the prosperity of thousands of individuals, and hundreds of corporations in dozens of countries during the last six decades [1]. As Moore's Law begins to come to an end for not only fundamental reasons, but also for computing performance, power, cost, and investments [2] (see **Table 1**), it is becoming clear that a different vision for electronics systems must emerge.

The first step in this new vision is a shift from Moore's Law for integrated circuits (ICs) to Moore's Law for Packaging by using package interconnections (I/Os) in 2D, 2.5D and 3D between smaller chips with the same or higher transistor density, as well as other components. The next step is a shift to optoelectronic package interconnections. As these transistor- and interconnections-based electronics begin to come to an end, quantum electronics is expected to take over. This concept is shown in **Figure 1**.

A new vision

This paper describes a shift from transistor scaling with the most number of transistors in a single large chip [3], driven by Moore's Law, to the package and system scaling concept that relies on the most number of interconnections (I/Os) between smaller chips in the short term, and to quantum computing in the long term. So, while transistor integration to a 20-billion transistor chip on individual ICs was the basis of Moore's Law for ICs to date, it can be extended by a different vision. In the short term, this vision involves new paradigms in electronic and optoelectronic package interconnections in 2D, 2.5D and 3D (**Figure 2**). Unlike

in the past with transistor scaling as the primary focus, this new vision is referred to as package and system scaling—its focus is on miniaturization of active and passive components and interconnecting them to form modules and systems.

Just like Moore's Law has both the doubling of transistors and simultaneous cost reduction from node to node every 18-24 months, Moore's Law for package interconnections can do the same. Interconnections have been driven by computing systems, and within computing systems, between logic and memory, consistent with Von Neumann's architecture. The new era of artificial intelligence mimicking the human brain, with several orders

better computing performance at lower power than current electronics, is yet another reason for the end of Moore's Law. The human brain is the ultimate system of interconnections for the highest performance in the smallest size with

11 reasons to replace Moore's Law	
1.	Fundamental limits, such as leakage, are being reached.
2.	There is an increased number of transistors from 20B now, to 50B in the future, adding to slower performance and higher cost.
3.	Transistor performance is slowing down by a factor of three.
4.	The cost of transistors is going up.
5.	Future wafer fab cost is going up.
6.	On-chip interconnect performance is going down due to increased RC delay.
7.	Low system performance vs. high device performance due to ultra-high interconnect length at the system level.
8.	Future computing architecture needs a different approach than current logic to memory.
9.	High computing power as transistors are increased.
10.	Low power efficiency to achieve higher bandwidth.
11.	Emerging heterogeneous and homogeneous integrations require a different approach than Moore's law.

Table 1: Eleven reasons to replace Moore's Law.

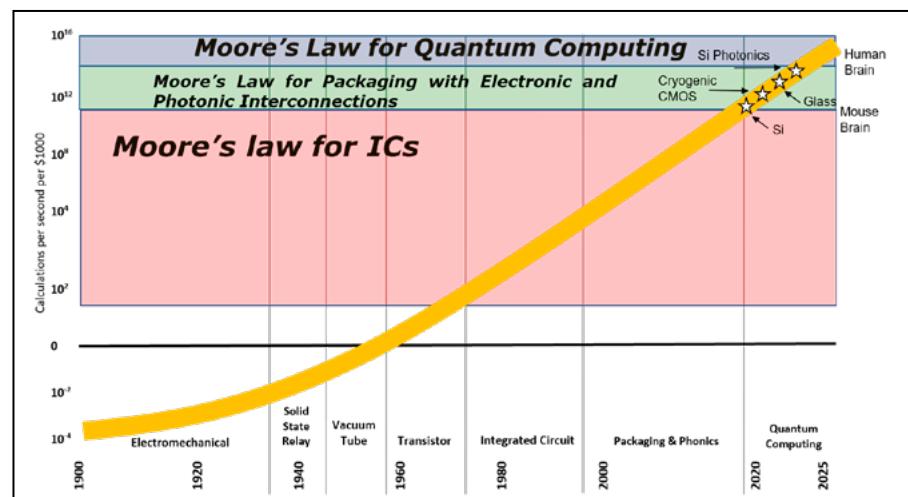


Figure 1: Computing performance driven by Moore's Law and post-Moore's Law technologies.

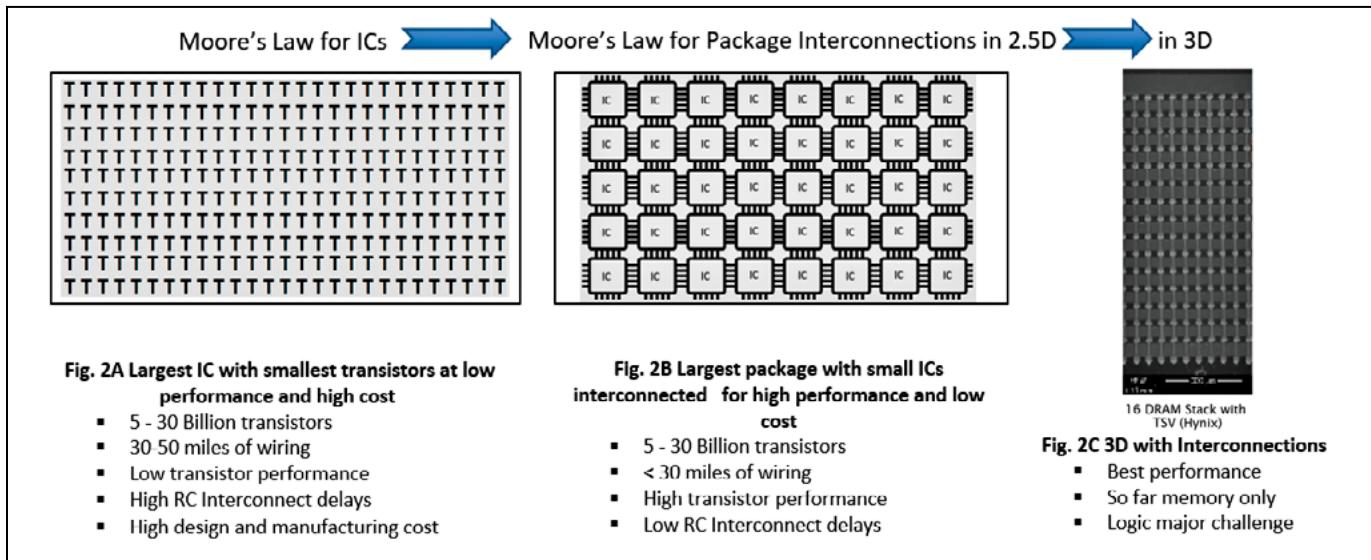


Figure 2: Moore's Law for: a) ICs b) Moore's Law for package interconnections in 2.5D; and c) Moore's Law for package interconnections in 3D.

the lowest power and is the new standard in system scaling and interconnections, and in computing performance-power efficiency. This is a lot more than current 3D electronic architectures can deliver. A typical human brain has about 90 billion nerve cells interconnected by trillions of synapses, providing trillions of pathways for the brain to process the information, along with a petabyte of memory. The electronics today are more like 200,000 interconnections. A new Moore's Law must, therefore, duplicate this human brain architecture.

Moore's Law for package interconnections has historically evolved, dramatically, from dual-in-line ceramic packages in the 1970s with 16 I/Os, to plastic quad flat packages in the 1980s with 64 I/Os, to ceramic packages in the 1990s with more than 1,000 I/Os, to organic laminate built-up packages in excess of 20,000 I/Os, and silicon and embedded packages approaching 200,000 I/Os. Artificial intelligence mimicking human brain may need several orders of magnitude more [4,5].

Silicon packaging

Currently, silicon packaging is the most leading-edge packaging, as measured by number of I/Os. Therefore, the best Moore's Law for package interconnections currently is with wafer-based silicon packaging, but silicon-

based packaging has many limitations at the material, device, interconnect, and system levels (Figure 3).

At the material level, silicon is limited by its ultra-high loss and high dielectric constant (11.4). It is also limited by small, 300mm wafer sizes, unlike packages and system boards that are manufactured in large panels, typically about 500-1000mm. In addition, silicon packages need to be ground from 800mm-thick wafers down to 30-100mm thick substrates. Silicon substrates with their coefficient of thermal expansion (CTE) of 3PPM/ $^{\circ}$ C, while perfectly matched to ICs, they are totally mismatched to the organic board's thermal coefficient of expansion (TCE) around 17PPM/ $^{\circ}$ C. This, in turn, requires an additional package in between Si packages and organic boards.

At the interconnect level, Si packages are typically manufactured with back end of line (BEOL) lithographic materials, processes and sub-micron wide, thick structures. These structures tend to be highly resistive and capacitive, thereby contributing to so-called RC delays that impact the final bandwidth performance. Almost all the high-performance packages, such as Intel's EMIB, AMD's Fiji and Nvidia's –

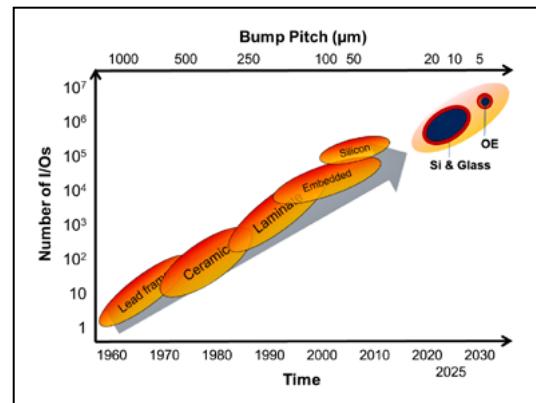


Figure 3: Moore's law for package interconnections: a new approach to Moore's Law.

are manufactured and used for artificial intelligence (AI), cloud computing and high-performance servers.

Glass packaging: the next best packaging

Glass packaging is being pioneered and developed by Georgia Tech and its large number of industry partners as the best next-generation of packaging with the goal of overcoming the shortcomings of silicon, described above. At the material level, glass is superior to silicon in electrical loss, dielectric constant, any TCE between 3 and 9PPM, as well as in production and availability in ultra-thin and ultra-large sizes, without having to grind and polish. At the



SUSS MICROTec - SHAPING THE FUTURE

SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring applications from R&D to high-volume production. We provide excellent process and maintenance support for you at any stage of your development and manufacturing cycle.

Our task is to contribute to the advancement of next-generation technologies such as 3D integration, imprint lithography and key processes for MEMS and LED manufacturing.

- + Photomask Equipment
- + Coater and Developer
- + Mask Aligner
- + Metrology
- + Imprint Lithography
- + Wafer-Bonder
- + Micro-Optics

SUSS MicroTec
info@suss.com
www.suss.com



interconnect level, we have developed materials and processes to minimize RC delays with lower resistance and lower capacitance redistribution layer (RDL) wiring. At the system level, it can be directly assembled to both Si ICs and organic boards, without another layer of packaging—unlike with Si packages. A number of new packaging paradigms developed in the Georgia Tech consortium include large-panel processing (in excess of 500mm sizes), development of 1-micron lithography tools, low dielectric constant polymer dielectric materials and processes with a high aspect ratio of conductors with lower resistance and a high degree of planarity without chemical mechanical polishing (CMP), and barrier metals to improve electromigration of closely-spaced conductors. In addition, a new 3D package architecture, referred to as 3DGPE, that advances 3D by embedding with ultra-short and low-RC interconnections, helps achieve higher bandwidth than with Si interposers.

Optoelectronic packaging

Photonics has long been viewed as providing higher bandwidth at lower power in smaller and lighter packages than electronics. It is also immune to electromagnetic interference (EMI). The technology has been used not only for long-distance communications, but also for systems to systems interconnections. As electronics reach bandwidth limits on account of Moore's Law limits as described above, optoelectronics becomes a necessary solution to achieve bandwidths towards 1Pb/s. Within optoelectronics, there are many ways to improve bandwidth including multiplexing: more links per optical channel, wavelength-division multiplexing (i.e., an approach that uses multiple wavelengths over the same medium), as well as modulation methods, such as pulse amplitude modulation—an approach that provides more bits in the same amount of time.

While there are many ways to fabricate optoelectronics modules, the most desirable technology is one that is made of silicon, as silicon is the most studied and used in microelectronics. This is referred to as Si photonics, whereby electronic

and photonic devices are integrated onto one single silicon chip using CMOS fabrication techniques. While there are many advantages to this technology, including smaller size (400nm waveguide width) and mature CMOS manufacturing processes, it also has many challenges that include fiber coupling and the fact that Si doesn't lase, requiring alternate on-silicon light sources.

Quantum electronics

Quantum physics has been a branch of physics for decades with many branches of study within it that include quantum chemistry, quantum simulations, quantum machine learning, quantum algorithms, and quantum communications. Quantum computing (QC) has been a topic of research for more than two decades. As Moore's Law-driven electronics begins to slow down in terms of its ability to provide increased computing at lower power, scientists at companies like IBM began to explore quantum devices. Unlike current digital systems that are programmed with bits as data units, either 0 or 1, quantum computers use qubits, which can represent a combination of both 0 and 1 at the same time, based on the principle of superposition. This difference makes quantum computers exponentially faster than current mainframes and servers.

In addition, quantum computers can do multiple calculations with multiple inputs simultaneously, unlike today's computers that can handle only one set of inputs and one calculation at a time. With 50 qubits, for example, the computing power can be 2 to the power of 50. When the industry gets to 1000 qubits that becomes 2 to the power of 1000. Currently, qubits are at about 50, but even at these low numbers, the computing power has been demonstrated well in excess of the best supercomputers at much lower power. Two factors driving qubits are quality and number. Currently, the most visible and dominant companies include IBM, Microsoft, and Google. All the large semiconductor and systems companies are known to have large internal programs [6].

Applications for quantum computing are many and include: 1) Rapid R&D for chemicals and pharmaceutical materials with simulations; 2) Supercomputing

power for autonomous vehicles with quantum AI to reduce fatalities to zero; and 3) Eliminating cybersecurity issues.

Quantum computers are expected to be developed in a Moore's law-like fashion—every year from 50 today, to about 5-10,000 by 2030. Amazon Web Services, Microsoft Azure, IBM, and others have already announced quantum offerings. Initially, quantum computing adoption will be a hybrid approach, in which parts of the problem would be handled by classical computing, and other parts by quantum AI. Mimicking the human brain may be the ultimate AI.

References

1. R. Keys, "Physical limits of silicon transistors and circuits," *Rep. prog. physics*, 68, 2701-2746, 2005.
2. G. E. Moore, "Cramming more components into integrated circuits," *Electronics*, 38(8), 1965.
3. R. H. Dennard, *IEEE J. Solid State Circuits*, SC-9, 256, 1974.
4. P. Ruch, et al., "Toward five-dimensional scaling: How density improves efficiency in future computers," *IBM J. R&D Vol. 55(5)* 151-157, 2011.
5. H. Moravec, "When will computer hardware match the human brain," *J. Evol. Technology*, online transhumanist.com/Moravec.htm
6. Alexandre Ménard, I. Ostojevic, M. Patel, D. Volz, "A game plan for quantum computing," *McKinsey Quarterly*, Feb. 2020.

Biography

Rao Tummala is a Distinguished and Endowed Chair Professor Emeritus at Georgia Tech, USA. Prior to Georgia Tech, he was an IBM Fellow. He has published about 800 technical papers and invented technologies that resulted in 100 patents. He has written seven books including the first modern Handbook in packaging, *Microelectronics Packaging Handbook* (1988), and the latest undergrad textbook, *Fundamentals of Device and Systems Packaging* (2019). He was a past President of IEEE EPS and IMAPS and is an IEEE Fellow and member of the National Academy of Engineering. Email rao.tummala@ece.gatech.edu

TECHNOLOGY TRENDS



EV Group takes on maskless lithography for MEMS and advanced packaging

CSR asked Paul Lindner, Executive Technology Director at EV Group, to comment on the company's developments in maskless lithography.

CSR: EVG is using maskless lithography to address future back-end lithography needs for advanced packaging and microelectromechanical systems (MEMS), among other applications. What is it about these applications that drove the design of your company's technology?

EVG: A very exciting development in the overall semiconductor industry is the shift toward 3D integration and heterogeneous integration within advanced packaging. Mobile processors have triggered a first growth cycle in 3D/heterogeneous integration. We expect this growth cycle to continue as high-performance applications such as artificial intelligence and 5G gain traction in mobile devices, but also due to other megatrends such as the Internet of Things. All of these trends facilitate advanced packaging, demanding new manufacturing technologies to support greater flexibility for varying designs, to increase performance and to lower the system design cost. Lithography in particular is demanding greater flexibility in terms of needing to address local alignment variations and non-linear shrinkage, to name a few requirements for molded wafers. At the same time, interconnect bandwidth demands denser lines and spaces. These challenges

in lithography triggered our development of the maskless exposure technology (MLE™) to meet critical requirements of design flexibility and minimal development cycles in the high-volume-manufacturing (HVM) world by eliminating mask-related difficulties and costs. The new technology enables high-resolution (<2µm L/S), stitch-free, mask-free exposure of the entire substrate surface with high throughput and low cost of ownership (CoO).

CSR: You have pointed out that the technology is highly scalable. How so?

EVG: The system scales according to user needs by adding or removing ultraviolet (UV) exposure heads in order to facilitate rapid transition from R&D to HVM mode, optimize throughput, as well as adapt to different substrate sizes and materials. MLE achieves the same patterning performance regardless of photoresist due to a flexible and scalable high-power UV laser source that offers multiple wavelength exposure options. This makes it ideal for processing a variety of substrates from small silicon or compound semiconductor wafers to panel sizes. While wafer specifications for fan-in packaging are rather standardized with low variations, this is not the case anymore for

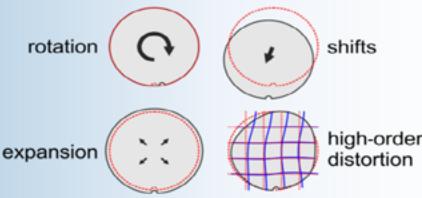
wafers in advanced packaging, where epoxy materials or carrier-mounted thin wafers for interposers add up to several millimeters of bowing and warp variation. Handling such wafers needs adaptable equipment handling platforms (see **Figure 1**). In MEMS, on the other hand, topography patterning is a frequent requirement. In both cases, MLE design features permit the patterning with less than 2µm feature sizes.

CSR: Some of the future challenges for back-end lithography are short development cycles and immediate ramp up from R&D to HVM. Please flesh out the details about the challenges related to immediate ramp-up. For example, how is this future challenge substantially different from previous time-to-market drivers?

EVG: The flexibility of MLE allows users to achieve faster innovation cycles and faster time to market using the same technology in development as later on in high-volume production. The technology employs clustered multi-wavelength laser light sources operating at 375nm and/or 405nm wavelengths. This, in turn, enables thin-resist patterning, including positive and negative resists, polyimides, dry-film resists and printed circuit board (PCB) patterning.

Compensates

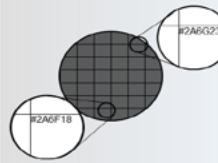
- Mechanical die placement and stress-induced inaccuracies via adaptive registration
- High-order substrate deformations, e.g., thick wafers, glasses and organic substrates



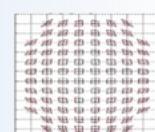
Enables

- Die & wafer level design patterns
- Individual die layouts (serial numbers, encryption keys)
- Mix & match with minimal switch-over
- Stitchless exposure

Serial Numbers & Encryption Keys



Stressed substrates



Delivers

- In-line capability, long lifetime, cost-efficient light sources
- Mask-less flexibility
- Multiple wafers or rectangular substrates (panels) for a multitude of processes

Box-in-box rerouting

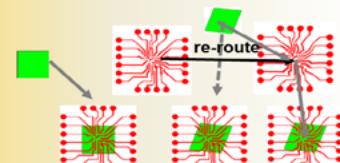


Figure 1: Key performance indicators of EVG MLE technology. SOURCE: EVG

System in package technology roadmaps



Roadmap described here based on an expected average of the different technologies in the market.

Figure 2: Lithography patterning roadmap for fan-in and fan-out wafer-level packages until 2025. SOURCE: Yole Développement (Yole)

Also enabled are thick-resist exposures supporting high aspect ratios typically seen in wafer-level packaging, MEMS structuring, microfluidics and integrated silicon photonics applications.

The application space for maskless exposure is very wide. For specialty and low-volume products, such as multi-project wafers in photonics, mask costs for design and tape-out changes are rather high, and here MLE provides a very cost-attractive alternative. Overall, performance and flexibility are two drivers for heterogeneous integration. At the same time, die placement and shrinking interconnect pitches for multi-chip modules emphasize the importance of maskless exposure.

CSR: Could you delve further into the improved scalability of the technology?

EVG: The HVM capability of maskless exposure is a major game changer for end users. Previously, back-end lithography results achieved during R&D using direct imaging equipment lacked the technological resilience for HVM lines equipped with steppers. The industry now, however, will see increasing product mix as chiplets and segmented dies will be a driver for continued performance scaling, as well as variability of applications, triggering the need for dynamic patterning at various resist thicknesses and dose levels (see [Figure 2](#)). MLE provides a high depth of focus at 2µm production resolution leveraging the physical diffraction limit established by the optics. At the same time, the scalability of MLE is broad in scope. Combining these highly flexible and volume-proven handling platforms allows

patterning of materials such as silicon, mold, glass, polymers and laminates using the same optics. It even compensates for substrate bow and warp, which is especially important for applications like fan-out wafer-level packaging (FOWLP). This delivers continuous, high-yield lithography at high throughput.

CSR: Could you please provide additional background details with respect to advanced packaging requirements that drive the need for maskless lithography?

EVG: Reconstitution of wafers is a central element of advanced packaging, joining dies from various wafer manufacturers, as well as various sizes. Die placement and die shift by overmolding add an additional layer of difficulty with which current lithography steppers and other mask-based systems cannot cope. In addition, reticle size is limiting large die interposer fabrication, where stitch lines in the redistribution layer can alter electrical properties. The ability to use a stitchless exposure method for interposers exceeding 55mm in length is increasingly important for high-performance compute devices needed for advanced graphics processing, artificial intelligence (AI) and 5G.

MLE technology is able to adapt to high-substrate stress, bow and warp thanks to integrated dynamic alignment that allows it to adjust to substrate material and surface variation while actively compensating for mechanical die placement and stress-induced inaccuracies (such as rotation, shift, expansion and high-order distortion errors). In parallel, MLE allows real-time digital/'binary'

wafer-level layout and individual-die layout patterning simultaneously—in particular, ad hoc individual die annotation, serial number or encryption key implementation. Programmable modulations of UV dosage during the patterning process enable resist thickness level variation after the development process. This feature enables the fabrication of complex 3D multi-level resist patterns applicable in future MEMS, novel photonic devices or micro-optical elements (refractive, diffractive). The digital programmable die/wafer layout can be stored in numerous industry standard vector file formats (e.g., GDSII, Gerber, OASIS, ODB++, or BMP). The vector layout with any given pattern complexity is computationally processed (rasterized) within a few seconds and stored in bitmap format. As a result, neither resist type (positive/negative), exposure dose level, nor any given design layout complexity have any impact on the speed of the patterning process.

Biography

Paul Lindner is Executive Technology Director of EV Group, St. Florian, Austria. He has more than 30 years of semiconductor, MEMS and related process experience. In his current role, he heads EVG's R&D, product and project management, quality management, business development and process technology departments. Customer orientation throughout all steps of product development, innovation and implementation in a production environment are among the main goals of EVG's technology groups headed by Lindner. Email: P.Lindner@EVGroup.com.



From Lab-to-Fab, **YES** is the Answer!

Cure.



PB Series
for manual polyimide
vacuum cure



VertaCure
for automated
polyimide vacuum cure

Clean.



G Series
for plasma cleaning



RFS Series
for R&D plasma
strip/descum



ÉcoClean
for automated plasma
resist strip/descum

Coat.



TA Series
for HMDS vapor prime
and image reversal



LabCoat
for R&D silane molecular
vapor phase deposition



ÉcoCoat
for silane molecular vapor
phase deposition

Yield Engineering Systems, Inc.

Call: **1-925-373-8353** (worldwide) or **1-888-YES-3637** (US toll free)

www.yieldengineering.com/csr

Antenna in package (AiP) technology for 5G growth

By Curtis Zwenger, Vik Chaudhry [[Amkor Technology, Inc.](#)]

Antenna in package (AiP) or antenna on package (AoP) simplify challenges associated with mmWave applications and expedites system design. Today's AiP technologies can be implemented through standard or custom system in package (SiP) modules. This article provides an in-depth look at the different AiP options, shielding, material selection, and best use cases in emerging 5G applications.

5G applications and projected growth

The driving forces for implementing 5th generation new radio 5G (NR) or simply 5G technology, include the transmission of large data rates as well as the need for more reliable connections, quicker response time (low latency) and better coverage. In mmWave applications, signal loss becomes critical and design challenges increase in complexity. In addition to emerging 5G smartphones, other applications that operate at very high frequencies and demand a small size include wearables, small cells, security cameras, radar units in autonomous vehicles and numerous Internet of Things (IoT) appliances.

By 2023, over 1 billion mmWave units will be produced annually according to Gartner, Inc. market research. With AiP technology, the antenna is no longer a separate component within the wireless device but is integrated in a SiP with radio frequency (RF) switches, filters and amplifiers. According to consulting firm Yole Développement, the total RF front-end (RFFE) module SiP market is projected to reach US \$5.3 billion by 2023, representing an 11.3% compound annual growth rate (CAGR) ([Figure 1](#)).

Another market forecast projects the 5G mmWave market to increase tenfold by 2025 [1]. The supporting base station and small cell infrastructure will require a tremendous amount of semiconductor packaging and system integration support. Outsourced semiconductor assembly and test (OSAT) suppliers are typically best suited to invest in the package

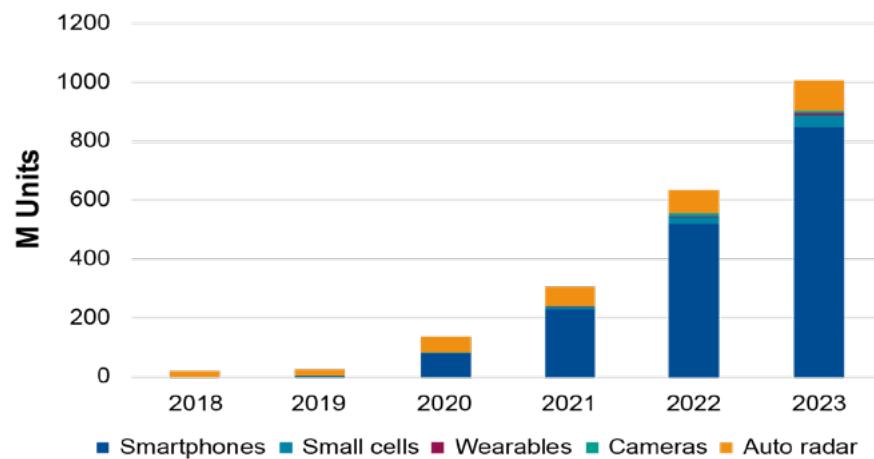


Figure 1: The market for mmWave devices is expected to grow to 1 billion units by 2023. SOURCE: Gartner, Small cells market status report, December 2018

development and production scaling for such applications by leveraging their broad customer and supply base.

5G AiP technology

Instead of separate power amplifiers (PA), low-noise amplifiers (LNA), switches, transceivers, filters and a discrete antenna, today's fully-integrated RFFE module is completely achieved with AiP technology in a SiP. The integration is accomplished using SiP technologies, including double-sided assembly, advanced wafer-level redistribution layers (RDL), passive component integration and sophisticated RF shielding techniques to provide the most advanced 5G package solutions available today.

In addition to the reduced size required for handheld and other small mmWave devices, AiP provides improved signal integrity with reduced signal attenuation and addresses the range and propagation challenges that occur at higher frequencies. Among the changes occurring with the transition from 4G long-term evolution (LTE) to the 6 to 60GHz of 5G are increased RF switch and band complexity (from 40 bands x3 carrier aggregations [CAs] to 50 bands x5 CAs) and increased antenna design and tuning complexity (from 8x8 multiple input and multiple output [MIMO] to 68x4 MIMO). To achieve the promised improvements of 5G (see [Figure 2](#)), many of the technical challenges must be addressed at the package level.

		3G	4G	5G
	Deployment	2004-05	2006-10	2020
	Bandwidth	2 mbps	200 mbps	>1 gbps
	Latency	100-500 milliseconds	20-30 milliseconds	<10 milliseconds
	Average Speed	144 kbps	25 mbps	200-400 mbps

Figure 2: The use of 5G technology provides significant advantages over previous generations. SOURCE: Raconteur



ATOTECH

Semiconductor Advanced Packaging solutions

Electrochemical plating portfolio



Spherolyte® Cu

High speed, pure and reliable
pillar and RDL plating



Spherolyte® Ni

Diffusion barrier for pillar
plating



Spherolyte® Sn/SnAg

Lead free, pure and uniform
soldering



Aurolyte® Au

Gold plating

Packaging applications:

FOWLP, WLCSP, flip chip, power ICs, memory, CI

End User markets:

Mobile applications, 5G technologies, IoT, sensors and processors, automotive

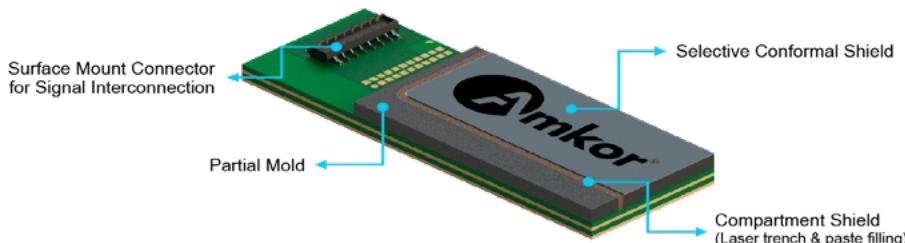


Figure 3: With an AiP design, the antenna is not a separate device, but is integrated in the device package.

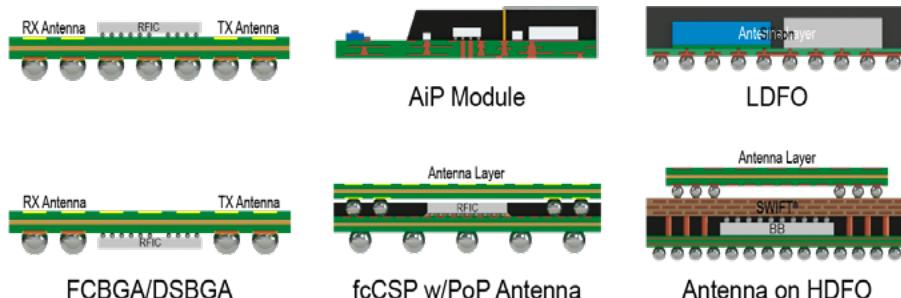


Figure 4: A technology toolbox for integrated antenna includes several different package platforms.

Implementing AiP technology

The type of integrated antenna or specific AiP platform designed into a specific application involves several factors. In addition to the antenna structures, an AiP package may also include a power amplifier (PA), low-noise amplifier (LNA), switch and transceiver integrated circuits (ICs). Depending on the frequency range, different platforms are used for both the antenna and the IC package. The integrated antenna can be mounted on the package, on a substrate, or in a SiP mmWave antenna module. The AiP approach itself can also vary from package to package. **Figure 3** shows an example of an AiP implemented with a SiP approach.

For some cost-sensitive applications, a flip-chip ball grid array (FCBGA) or double-sided ball grid array (DSBGA) are two AiP possibilities. **Figure 4** illustrates the extensive technology toolbox for integrated antennas. For mobile and infrastructure applications, the design options include:

- Antenna in substrate;
- Antenna module;
- Dual-side die mount packages (DSBGA);
- Low density fan-out (LDFO) with integrated antenna layer substrate;
- High-density fan-out (HDOF) with antenna on package; and
- Antenna on mold.

For other applications, the antenna could be an SiP module antenna or a flip-chip chip-scale package (fcCSP) with package on package (PoP) antenna. The different design options include: 1) SiP mmWave antenna module; 2) partial molding; 3) passive/filter integration; 4) array antenna design; and 5) small form factor.

Shielding

For higher levels of system integration, advanced SiP and RF shielding technologies are employed. RF SiPs can contain the complete RF to base-band system functionality with an integrated antenna and antenna matching circuitry. The result is a fully-integrated AiP where all the elements of at least one complete RF system is included in the format of a single semiconductor package.

RF shielding techniques include dual-side mold, conformal shield, compartment shield using laser trench and paste filling technology, partial molding, selective conformal shielding, and hybrid SiP designs. These techniques implement a variety of materials including conductive lids, cored, coreless and low coefficient of thermal expansion (CTE) substrates and innovative conformal shielding materials. **Figure 5** shows key technologies to implement different shielding techniques.

The type of shielding in the AiP can have a significant impact on performance. **Figure 6** shows how a SiP with a sputtered conformal shield outperforms an unshielded SiP, thereby substantially improving the electromagnetic compatibility/ electromagnetic interference (EMC/EMI) performance.

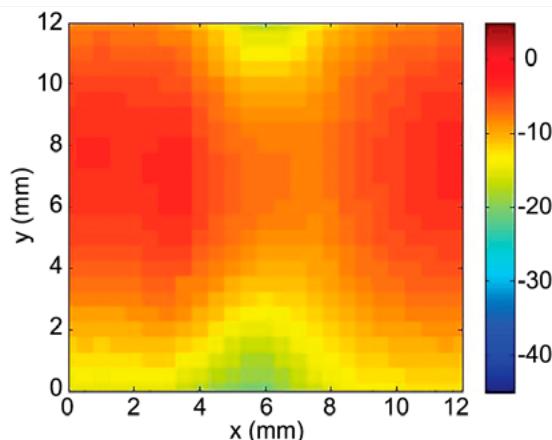
	Wire Fence	Wire Cage	Vertical Wire	Trench and Filling
Fixture				
Key Technology	High loop wire bonding	High loop wire bonding	Vertical wire bonding and wire reveal	Laser trench and paste filling

Figure 5: A variety of SiP RF shielding techniques address different design requirements.



Unshielded SiP

Unshielded DUT - Ex Magnitude Maximum Radiation



SiP with Sputter Conformal Shielding

3 μm Cu - Ex Maximum Radiation

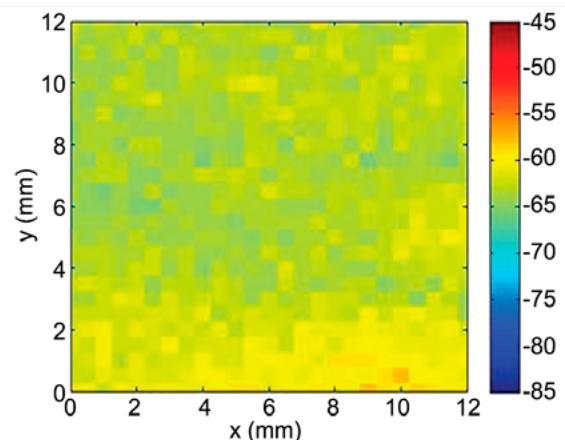


Figure 6: Near-field conformal shielding performance measurements from 100MHz to 6GHz.

Materials

Similar to shielding, material selection also has a significant impact on AiP design and performance—a variety of materials provide design options to meet different performance levels. In addition to materials for mmWave shielding, an antenna substrate can have:

- Asymmetrical stack-up;
- <3.3 dielectric constant (Dk) materials;
- <0.005 dissipation factor (Df) materials;
- Ra >300nm (Cu trace surface roughness); and
- Low Dk/Df solder resist.

Wafer-level processing and LDFO packages include:

- Low Dk/Df passivation and mold/ electromagnetic compatibility (EMC);
- Thick passivation development;
- Multi-layer RDL for T-line/ waveguide; and
- Wafer-level magnetic shield.

Advanced, high-frequency discrete antenna/transceiver applications employ wafer-level package technologies, where the metal RDLs that form the antennas' elements are high precision, repeatable, and easily tuned for the application. Specific AiP platform implementations include: 1) Top layer assembly; 2) Double-side assembly; 3) Double-side molded assembly; and 4) Double-side molded assembly with exposed die.

Choosing the right package platform for a specific design typically involves discussions between OSAT package

designers and original equipment manufacturer (OEM) system designers. Design considerations for 5G substrates must account for different package-level signal losses including: conductor, dielectric loss, leakage and radiation losses. Conductor losses must address plating, skin depth, surface roughness, and via (structure, pitch and placement). Key elements affecting dielectric loss include the substrate materials' dissipation factor and dielectric constant. The substrate materials' thickness stack-up also has a direct effect on signal integrity (e.g., core, prepreg and solder mask thickness). The epoxy mold compound may also come into play for structures where the mold compound is used as a dielectric. Leakage losses can occur within the plane due to under-etched seed layers and between substrate layers because of RDL and via patterning defects. Radiation losses can occur because of:

- Circuit configuration: stripline, complainer and microstrip;
- Via stub (radiation and reflection);
- Impedance transition and discontinuities; and
- Spurious resonance frequency spectra.

Another design factor that can improve antenna performance is to optimize the substrate stack-up (see **Figure 7**). Direct connection with receive/transmit (RX/TX) signals reduces signal mismatches that can negatively impact the receiver signal sensitivity and increase power consumption at the transmitter.

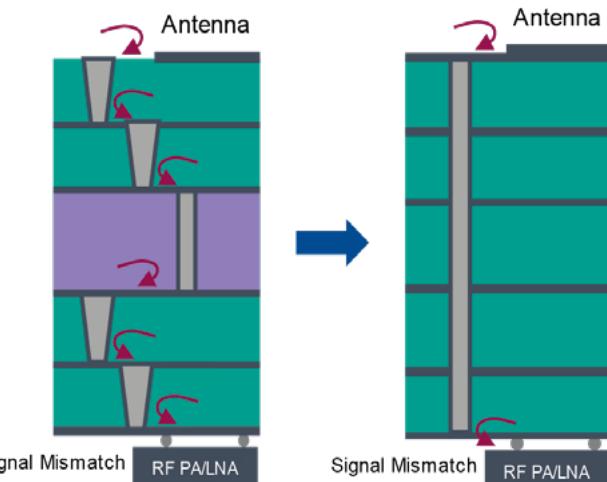


Figure 7: Optimized substrate stack-up and RDL/via routing can improve antenna performance by reducing signal mismatch.

Specific implementations of different design aspects in a variety of packaging technologies for AiP include:

- Body sizes up to 23.0mm with several form factor options;
- Up to 14 substrate layers; and
- Thin-film RDLs and dielectrics for 77GHz and higher applications.

For mmWave applications, the right AiP design provides several essential system advantages. With AiP technologies, system designers get:

- A smaller footprint-phased antenna array design to minimize space;
- Reduced signal attenuation for mmWave products;
- Lower power consumption;
- Improved range for devices; and
- A design proven and qualified by the supplier.

As signal loss to the antenna is reduced, this may help reduce the power requirements compared to the conventional antenna. In addition, AiP reduces the engineering effort and required resources for the OEMs because the design and product are qualified by the supplier. With this qualification, OEMs can feel confident about introducing a robust product in the market much quicker with the integrated antenna. In fact, with proven materials up to 77GHz, Amkor's AiP packaging technologies are shipping products today with over 60GHz operation.

AiP use cases

A variety of AiP use cases exist today, including:

Smartphones. 1) High speed 5G connectivity to mobile phones; 2) Samsung Galaxy S10 contains 3 AiP products; and 3) Several new phones coming to market in 2020 with 5G enabled (sub-6GHz).

Small cells. 1) Antenna arrays for small cells for indoor and outdoor applications; 2) Last-mile connectivity to bring high-speed networks to homes; and 3) High-speed connectivity in office buildings; and 4) Connectivity in public spaces like stadiums, airports, etc.

Security camera. 1) Connecting 5G-enabled security cameras to a network; 2) Reduced form factor benefits because of AiP.

Autonomous vehicle. 1) Cars will require multiple connectivity modes for Infotainment, advanced driver-assistance systems (ADAS) and over-the-air (OTA) updates; 2) High-bandwidth 5G connection for infotainment; and 3) Navigation with 3D images and rich content.

AiP design services/design capabilities

Addressing all AiP technologies calls for an extensive toolset to maximize circuit density and support the sophisticated packaging formats required for high-volume production of 5G and any mmWave design. Based on the application requirements, whether 5G or low-power wide-area network (LPWAN) or other connectivity, customers should be able to select low dissipation factor/dielectric constant substrates, thermal interface materials (TIMs) for heat dissipation, and a wide array of different package architectures to provide high levels of system and sub-system integration. These design options require sophisticated models for electrical, thermal and mechanical simulations for customers, as well as services for design, signal integrity simulations, test and characterization.

In addition to an advanced multi-die integration toolbox and RF SiP design and simulation know-how, other capabilities should include:

- Extensive fcCSP, WLCSP, LDFO and HDFO portfolios for multi-die designs;
- An established and reliable supply chain; and
- Global assembly scale and system test investments.

Finally, a complete set of design guidelines for system designers allows them to confidently engage the OSAT that will fully meet their needs.

5G in the palm of your hand

There are many package options to incorporate AiP in next-generation designs. For the quickest and easiest implementation, the OSAT's package or SiP must have high-volume production capacity to support design of next-generation mmWave products.

With many of the discussed packages already in production, we have been supporting 5G mmWave AiP applications in high-volume manufacturing for over five years. This includes both conventional and advanced packaging techniques that integrate a laminate substrate-based antenna element with a transceiver and the associated components and circuitry to address both sub-6GHz and true mmWave products.

Summary

Amkor has developed an extensive toolset to maximize circuit density and address the sophisticated packaging formats required to enable 5G applications – such as double-sided assembly, embedded die in substrate, thin-film RDL and dielectrics and various types of RF shielding techniques. This toolset, combined with expertise in RF and antenna package design enables partnering with customers who want to outsource the challenges and high investment associated with combining multiple ICs with advanced package assembly and test technologies for 5G networks. As demand for packages that support 5G starts to ramp up, we are already well underway with the successful implementation of AiP technology.

Reference

1. “Millimeter Wave (MMW) Technology Market, Industry Report 2018-2025,” Grand View Research; <https://www.grandviewresearch.com/industry-analysis/millimeter-wave-mmw-technology-market>



Biographies

Curtis Zwenger is VP, Advanced Package & Technology Integration at Amkor Technology, Inc., Tempe, AZ. He holds a BS in Mechanical Engineering from Colorado State U. and an MBA from the U. of Phoenix; Email curtis.zwenger@amkor.com

Vik Chaudhry is Sr. Director, Product Marketing and Business Development at Amkor Technology, Inc., Tempe, AZ. He holds a BS in Electrical Engineering from National Institute of Technology, Bhopal, India, and a Master's in Electrical Engineering and an MBA from Arizona State U.

Advanced FOWLP for small form factor and high-performance microcontroller apps

By Gaurav Sharma, Nishant Lakhera, Mollie Benson, Andrew J. Mawer [NXP Semiconductors]

Over the past few years, the fan-out wafer-level package (FOWLP) platform has gained a lot of traction for consumer and hand-held electronic applications. Key FOWLP benefits are:

1. Absence of packaging substrate or reduced substrate layer count enables smaller foot print area and package thickness.
2. Lack of an organic substrate leads to a shorter heat dissipation path from die to printed circuit board (PCB), thereby enabling better thermal performance of the package.
3. Wafer fab-like processes leads to excellent process tolerance for high-density and fine-pitch package interconnects.
4. A low-loss and tightly controlled package interconnect scheme also enables excellent electrical performance of integrated packages, with significantly reduced package interconnect parasitic loss.

There are different flavors of FOWLP that have been developed and exist in the industry today [1-4]. A traditional wafer-level fan-out structure is a die-first, die-down FOWLP that has been in volume production for low-end baseband, PMIC, Codec, Wi-Fi, and RF types of applications [1]. A die-up high-density fan-out package process was developed that found adoption for mobile phone processors and DRAMs in a package on package (PoP) format [4]. For the high-density fan-out package, multiple redistribution layers at relatively fine-pitch and high interconnect density are used.

To date, the majority of the traditional wafer-level fan-out products are limited to single-package interconnect layers. FOWLP also has limitations in achieving good board-level reliability (BLR) performance. During board-

level temperature cycling (BLR-TC), both fan-in and fan-out wafer-level packages have solder joint cracking as the dominant failure mode (**Figure 1a**). Solder joint cracking results from the cyclic fatigue stress on the solder ball interconnects during board-level temperature cycling. The stress arises on account of the coefficient of thermal expansion mismatch between the wafer-level package and the printed circuit board. Stiffer solder alloys have been evaluated to minimize the fatigue damage caused by cyclic stress, and thereby improve the solder joint fatigue life [5]. However, the higher stiffness of the solder moves the induced cyclic stress and failure from the solder joint to the package redistribution layer (RDL) trace (**Figure 1b**) [6]. Wafer-level packages for advanced silicon nodes have fragile low-k and extremely low-k (ELK) back end of line (BEOL) dielectric layers that can crack or delaminate because of cyclic fatigue [7].

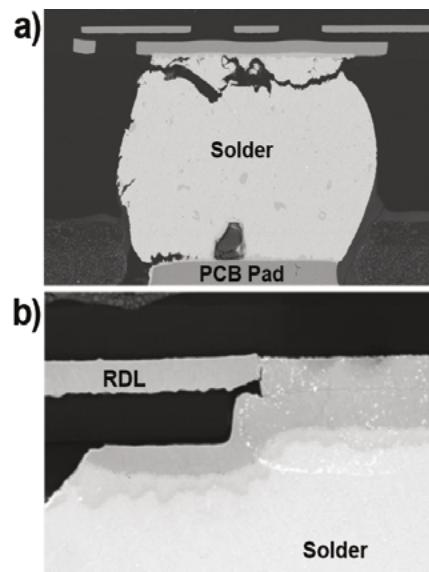


Figure 1: Common board-level reliability testing failure modes in wafer-level packages: a) normal solder joint cracking at package or PCB interface; and b) package RDL trace cracking with stiffer solder alloy.

Fan-out package process development

Figure 2 shows the overall fan-out package process flow used in the development work described in this article. The incoming silicon wafer was background to the desired silicon thickness followed by a laser groove and mechanical saw process. For the

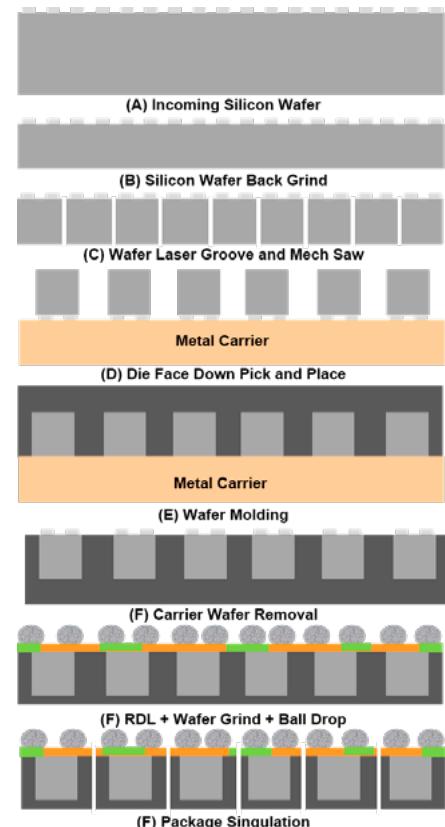


Figure 2: Overall FOWLP process flow.

advanced node silicon used in the work with ELK/LK BEOL layers, both laser groove and mechanical saw were used to ensure BEOL integrity and a defect-free die saw process. After die saw, the known good die from the fab wafer map were picked and placed active side down on the metal carrier wafer.

The die placement and spacing on the metal carrier was determined by the final FOWLP design. After die pick and place, the wafer was molded and the carrier wafer was removed. This step is followed by a package RDL fabrication process with five or six lithography layers to form either the under bump metallization (UBM), or no UBM design version, respectively.

After RDL formation, the mold wafer was background to the final package thickness, followed by solder ball drop and package singulation into individual units. **Figure 3** shows the FOWLP package developed in this study. The package size is 7x7mm with 249 solder balls at

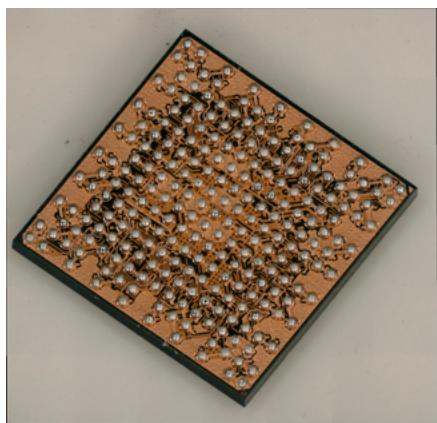


Figure 3: Developed FOWLP: package size = 7x7mm, solder ball pitch = 0.4mm, ball count = 249.

0.4mm solder ball pitch. The unique solder ball map (shown in **Figure 3**) with depopulation at the outermost row is the result of product silicon/package/board co-design. Solder ball depopulation at the outermost row increased the reliability risk during BLR-TC testing. To overcome BLR-TC and the other associated package reliability risks, different solder alloy and package RDL stack-up design of experiments (DOE) were evaluated. **Table 1** illustrates the different DOE. The developed FOWLP had two copper metal redistribution layers (RDL) and three repassivation (REP) dielectric layers.

Both no UBM and UBM options were evaluated. SACA and SACB were the two lead-free solder alloys used. Diel 1 and Diel 2 are two different repassivation (REP) dielectric materials. In conjunction with the different solder alloys, appropriate package interconnect stack-ups were evaluated to optimize reliability stresses across different levels of interconnects ranging from silicon BEOL, package RDLs and package, and PCB solder joint.

Figures 4 and **5** show scribe line structures from the front (active) and back sides of the silicon wafer from high-metal

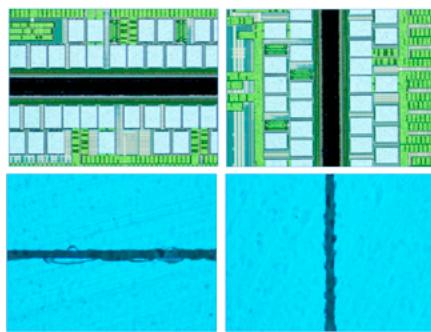


Figure 4: Optimized wafer saw process at a scribe line high metal density location: a) (top panels) Front silicon (circuit) side; and b) (bottom panels) Silicon back side.

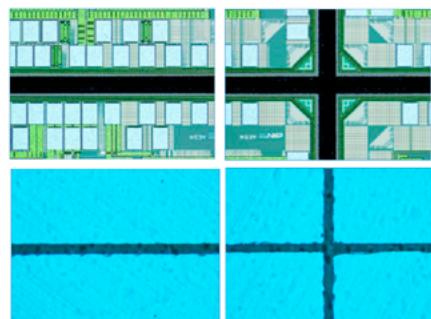


Figure 5: Optimized wafer saw process at a scribe line low metal density location: a) (top panels) Front silicon (circuit) side; and b) (bottom panels) Silicon back side.

and low-metal density regions, respectively. For advanced node silicon with low-k and ELK dielectric layers in BEOL, laser grooving needs to be applied followed by mechanical dicing. Direct application of

mechanical dicing to fragile BEOL layers leads to their delamination and cracking. Laser groove was performed first to separate the BEOL layers, followed by mechanical blade dicing. The scribe lines had varying metal densities in different locations, so a laser groove recipe was developed over a series of DOE to optimize the process parameters that achieve all the following objectives: 1) no peeling/delamination of LK/ELK BEOL; 2) removing all metal from high-density metal locations (to eliminate the potential for metal debris in the scribe line); and 3) optimum laser groove depth.

After optimizing the laser groove process, the blade dicing process was fine-tuned to meet product specifications related to front side (circuit) chipping/peeling/delamination, side wall crack/chipping, and back side crack/chipping. These scribe line related defects have led to premature failures during the assembly process, and during surface mount and package reliability testing [8,9]. For wafer-level packages, these scribe-related defects are quite critical because the packages are directly mounted on the board with no substrate present to enhance package strength.

DOE and reliability testing

Table 2 shows the reliability test conditions used in this study. The FOWLP was subjected to MSL3 preconditioning prior to highly accelerated stress testing (HAST) and application-level temperature cycling (AL-TC) reliability tests. The optimized FOWLP passed all the reliability tests. BLR-TC is one of the most challenging reliability testing conditions

Test	Condition	Zero fail criteria	Result
Moisture Sensitivity Level 3 (MSL3)	30 °C/60% RH	168 h	Pass
Highly Accelerated Stress Test (HAST)	110 °C / 85%RH/3.3V	528 h	Pass
Application-Level Temperature Cycling (AL-TC)	T _a = -40 °C to 125 °C	600 cycles	Pass
High Temperature Storage Life (HTSL)	T _a = 150 °C	2000 h	Pass
Board Level Temperature Cycling (BL-TC)	T _a = -40 °C to 125 °C	500 cycles	Pass
Drop Impact Test	1500 g / 0.5 ms	30 drops	Pass

Table 2: Reliability test conditions that the developed FOWLP passed and qualified.

for wafer-level packages. Unlike substrate-based packages, both fan-in and fan-out wafer-level packages are directly mounted on a PCB and BLR-TC leads to significant

Solder	REP1	RDL 1	REP2	RDL2	REP3	UBM
SACA	Diel 1	Copper	Diel 1	Copper	Diel 2	No
SACA	Diel 1	Copper	Diel 1	Copper	Diel 2	Yes
SACB	Diel 2	Copper	Diel 2	Copper	Diel 2	No
SACB	Diel 2	Copper	Diel 2	Copper	Diel 2	Yes

Table 1: Different solder alloy and package interconnect stack up combinations that were evaluated for the FOWLP.

Besi Enables “More than Moore”

*The World Leader in Advanced
Packaging Process Equipment*

ThermoCompression Bonding

- *Proven HVM TC Bonder*
- *8800 TC^{Next}*
- *Die size up to 70x70 mm*
- *1.5µm, 3σ accuracy, theta: 1 mdeg 3σ*
- *Inert bonding ambient option*
- *Superior Tilt Control*

Die to Wafer Hybrid Bonding

- *8800 Chameo^{ultra plus}*
- *Ultra High Accuracy C2W Bonder*
- *Advanced Cleanliness by Design*
- *Highest Throughput*
- *200nm, 3σ accuracy*
- *> 2000 CPH*

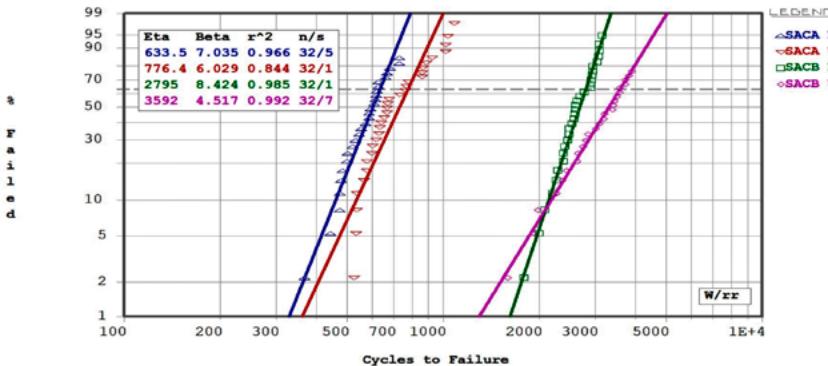


Figure 6: Weibull plots from BLR-TC test for different DOE legs for FOWLP: SACA no UBM, SACA UBM, SACB no UBM, and SACB UBM.

coefficient of thermal expansion (CTE) mismatch between package and PCB, which in turn stresses the solder ball interconnect between the package and PCB. Typical failure modes are depicted in **Figure 1**. For fan-in wafer-level packages, this stress is most severe where the Si is bonded to the substrate because there is a large difference in CTE between the Si and the PCB (~3ppm for Si and ~15-20ppm for the board). The FOWLP body is a composite of silicon plus the mold compound, so the package CTE is relatively higher than that of only silicon. Still, however, the CTE mismatch is quite large between package and PCB [10]. During temperature cycling, creep of the solder interconnects occurs at the elevated temperature of the thermal cycling.

The mean characteristic life during BLR-TC can be modeled and predicted by either the accumulated creep strain energy density, or the accumulated creep strain model [11,12]. Accumulated creep strain and creep strain are direct representations of the creep damage that the solder joint undergoes during BLR-TC. For the same package structure, using a stiffer and stronger solder alloy and UBM results in significant improvement in mean characteristic life [5]. In this work, four DOE legs were built with SACA and SACB solder alloys with, and without, a UBM. **Table 3** shows the properties of solder alloys that were evaluated. Greater tensile strength of the solder has been known to increase the lifetime of the solder during cyclic bending in BLR-TC testing [6].

Properties	Unit	SACA	SACB
Tensile Strength	MPa	49	91
Elongation	%	61	37

Table 3: List of material properties of investigated solder alloys.

to SACB. Usage of underfill was also evaluated to improve FOWLP BLR-TC life. The SACA/no UBM case leg had the first fail at 369 cycles when no underfill is used. However, when underfill is used, the first failure was observed at 5,147 cycles, and only two fails were observed by testing up to 6,994 cycles. When a stiffer solder alloy is used, the BLR-TC failure mode often moves from the solder to the package RDL and silicon die BEOL cracking [6,7]. To overcome these package reliability risks across different levels of interconnects, the RDL stacks' designs were optimized for the different solder alloys and no UBM and UBM metallizations. This resulted in improved package reliability for all the different interconnect levels ranging from the silicon BEOL, the package RDL interconnect, to the package/PCB solder joint. In addition to BLR-TC, AL-TC was also performed where the device product was mounted on board and underwent temperature cycling. Full product functional testing (FT) was used to detect failures. No FT fail or product performance degradation was observed up to 1500 AL-TC cycles.

Figure 7 shows the experimental BLR-TC data for the different DOE legs: SACA no UBM, SACB no UBM, and SACB UBM. The Weibull plot shows SACB solder alloys have significantly improved FOWLP BLR-TC performance. **Table 4** lists the characteristic life cycles for the different DOE legs. SACA and SACB alloys with UBM have between 23%- 29% improvement in characteristic life versus no UBM. For no UBM, changing the solder alloy from SACA to SACB leads to a 341% improvement in BLR-TC characteristic life. For the UBM case, the improvement in BLR-TC characteristic life is 363% when the solder alloy is changed from SACA

Solder Alloy	No UBM	UBM
SACA	633 cycles (x)	776 cycles (1.2x)
SACB	2795 cycles (4.4x)	3592 cycles (5.7x)

Table 4: BLR-TC characteristic life (~63% fail) for different solder alloys and no UBM, UBM case. Values in parentheses indicate relative characteristic life values, with SACA no UBM as the reference.

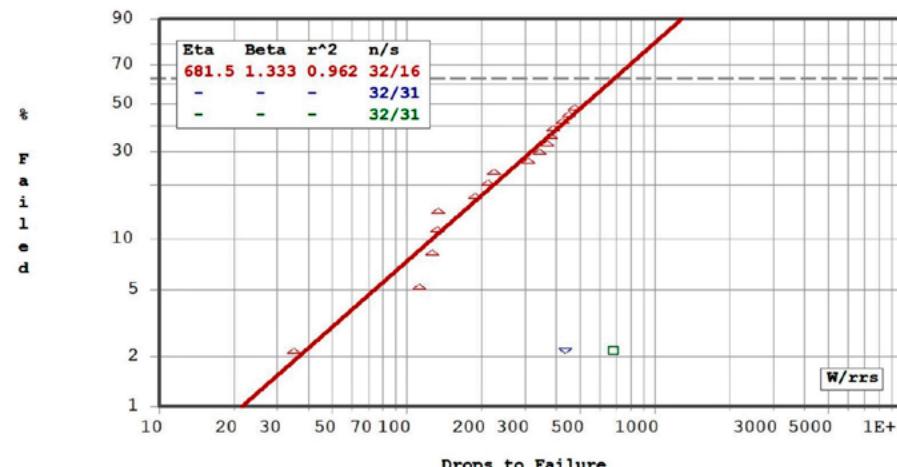


Figure 7: Drop test Weibull plot: a) △ - SACA/no UBM; b) ▽ - SACB/no UBM; and c) € - SACB/UBM.

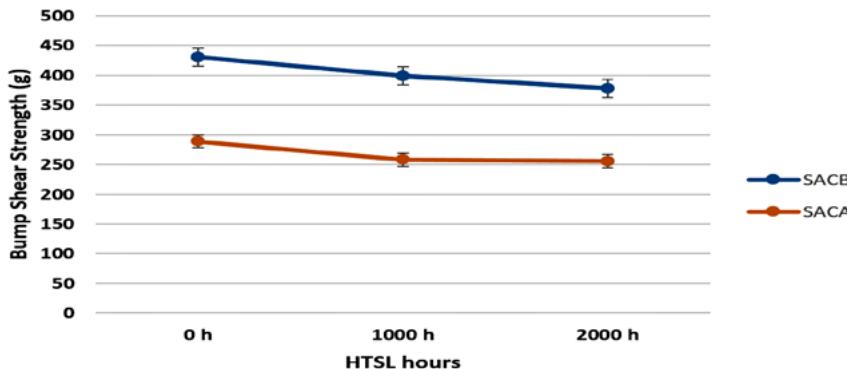


Figure 8: Bump shear strength variation with 150°C high-temperature storage hours for SACB and SACA solder alloys.

high-temperature storage at 150°C. As expected, both solder alloys show some degradation in bump shear strength after 150°C aging for 1000h and 2000h that is attributed to intermetallic formation. However, even after 2000h, SACB solder alloy shows a 50% greater bump shear strength in comparison to the SACA alloy.

Figure 9a shows a cross section of SACA no UBM leg solder alloy after 475 cycles of BLR-TC. The first solder ball to fail is the package corner ball. Bulk solder ball cracking on the package side was the failure mode. Some crack initiation was also observed at the solder ball/PCB pad interface. **Figure 9b** is a cross section from the SACA UBM leg after 525 cycles. The first solder ball to fail is the package corner

ball. The failure mode is again in the bulk solder, however, it is at the solder ball/PCB pad interface. The presence of UBM improved the strength of the solder ball/UBM interface joint so the primary failure mode, in turn, shifts to the solder ball/PCB pad interface. However, some crack initiation can also be seen at the UBM/solder ball interface. **Figure 10a** shows a FA cross section overview of the SACB no UBM leg after 3,164 cycles of BLR-TC. As expected, corner ball failures can be seen with bulk solder ball cracking. **Figure 10b** is a magnified cross section view of the outermost corner ball that shows quite significant solder ball distortion because of the relatively large number (3,164) of thermal cycles and the associated CTE

mismatch between the FOWLP and PCB. The primary crack and failure mode can be seen to be concentrated on the package/solder ball interface. Some cracks were observed at the solder ball/PCB interface. The failure mode stays the same for the SACA no UBM, and SACB no UBM cases of BLR-TC. However, **Table 4** shows the BLR-TC characteristic life increases by ~341% when changing from SACA to SACB solder alloy. This improvement in BLR-TC life is because the SACB is stiffer than SACA, and also because of the incorporation of an optimized RDL stack up for SACB solder alloy that prevents RDL cracking, which had been reported in a previous study with stiffer solder alloy [6].

RDL stress modeling showed that with the appropriate package RDL stack up, RDL stress decreased when using the stiffer SACB solder alloy in comparison to the SACA. The SACB solder alloy legs passed all reliability tests including daisy chain-based BLR-TC and drop tests, as well as functional product-based AL-TC, biased HAST (BHAST), and high-temperature storage life (HTSL) tests.

Summary

FOWLP using traditional fan-out package process flows were used to develop optimized packages that passed, and significantly exceeded product reliability testing requirements of BLR-TC, drop test, BHAST and AL-TC tests. The stiffer solder alloy SACB in combination with an optimized package RDL stack up led to significant improvement in BLR-TC characteristic life and drop test reliability. After 3,164 BLR-TC cycles, the failure mode for SACB solder alloy was still bulk solder ball cracking, which is indicative of excellent chip package integration across all silicon-package-board interconnect levels. Drop test reliability was also significantly improved with SACB solder alloy with only one failure observed at 1,000 drops.

References

- M. Brunnbauer, “Embedded wafer-level ball grid array (eWLB),” Proc. of 8th Elec. Packaging Tech. Conf., 10-12, Dec. 2006, Singapore, pp. 1-5.
- G. Sharma, “Design and development of multi-die embedded micro wafer-level packages with laterally-placed and vertically-stacked thin dies,” IEEE Trans. on Adv. Packaging, Vol. 1, Issue 1, 2011, pp. 52-59.

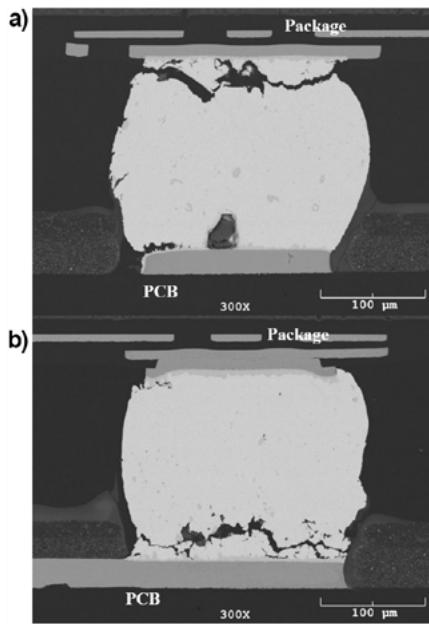


Figure 9: a) (top) Solder ball cross section after BLR-TC 475 cycles for SACA — no UBM leg; and b) (bottom) Solder ball cross section after BLR-TC 525 cycles for SACA UBM leg.

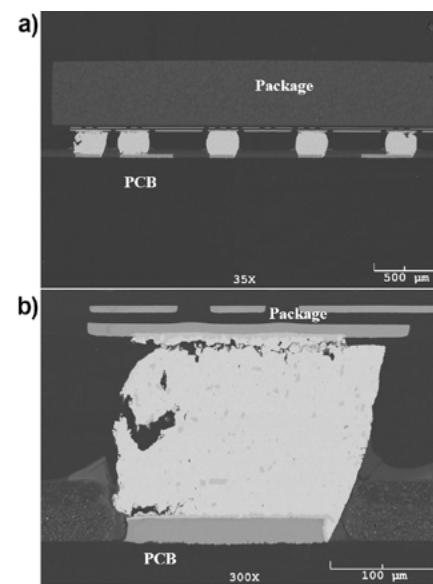


Figure 10: a) (top) Package cross section showing corner ball fail after BLR-TC 3164 cycles for SACB — no UBM DOE leg; and b) (bottom) Magnified corner ball cross section showing bulk corner solder ball cracking primarily at the package side, as well as some crack initiation at the PCB side.



LEADERS IN MICRO DISPENSING TECHNOLOGY

SMALL REPEATABLE VOLUMES ARE A CHALLENGE, BUT NOT IMPOSSIBLE IF YOU HAVE BEEN CREATING THEM AS LONG AS WE HAVE.

TO DO IT WELL, WE PROVIDE THREE THINGS:

Dispensing Expertise in a variety of microelectronic packaging applications.

Feasibility Testing & Process Verification based on years of product engineering, material flow testing and software control.

Product Development for patented valves, dispensing cartridges, needles, and accessories.

Our Micro Dispensing product line is proven and trusted by manufacturers in semiconductor, electronics assembly, medical device and electro-mechanical assembly the world over.

www.dltechnology.com.

216 River Street, Haverhill, MA 01832 • P: 978.374.6451 • F: 978.372.4889 • info@dltechnology.com



3. R. Huemoeller, "Silicon wafer integrated fan-out technology," *Chip Scale Review*, Mar/Apr issue 2015.
4. C-F. Tseng, "InFO (wafer-level integrated fan-out) technology," IEEE 66th Elect. Comp. and Tech. Conf. (ECTC), 31 May – 3 June 2016, Las Vegas, NV, USA, pp. 1-6.
5. W. Lin, "SACQ solder board-level reliability evaluation and life prediction model for wafer-level packages," IEEE 67th ECTC, May 30 – June 2, 2017, Lake Buena Vista, FL, USA, pp. 1058-1064.
6. C. K. Yu, "A unique failure mechanism induced by chip to board interaction on fan-out wafer-level package," IEEE Inter. Rel. Physics. Symp. (IRPS), 2-6 Apr. 2017, Monterey, CA, USA.
7. P. H. Tsao, "Board-level reliability enhancement of WLCSP with large chip size," IEEE 68th ECTC, May 29 – June 1 2018, San Diego, CA, USA, pp. 1200-1205.
8. W. Fitzgerald, "Advanced low-k die singulation defect inspection and pre-emptive singulation defect detection," 37th Inter. Elec. Mfg. Tech. Conf., 20-22 Sept. 2016, George Town, Malaysia.
9. Z. Wang, "300mm low-k wafer dicing saw development," IEEE Trans. Compon. Packag. Technol. Vol. 30, No. 4, Oct. 2007, pp. 313-319.
10. M-K. Shih, "Parameters study of thermomechanical reliability of board-level fan-out package," Inter. Conf. of Elec. Packaging, 19-22 Apr. 2017, Yamagata, Japan, pp. 66-70.
11. A. Syed, "Updated solder fatigue life prediction models for SnAgCu solder joints," SMTA, 2006, pp. 939-945.
12. R. Darveaux, "Effect of simulation methodology on solder joint crack growth correlation," IEEE 50th ECTC, 21-24 May 2000, Las Vegas, NV, USA, pp. 1048-1058.



Biographies

Gaurav Sharma is a Senior Principal Packaging Engineer at NXP Semiconductors, Austin, TX USA. He has fifteen years of industry experience in advanced semiconductor packaging and holds a PhD in Materials Science and Engineering from Pennsylvania State U. and an MBA from National U. of Singapore. He has published more than forty papers in international journals and conferences. Email gaurav.sharma_3@nxp.com

Nishant Lakhera is Package Development Manager at NXP Semiconductors, Austin, TX USA and holds a PhD in Mechanical Engineering from the U. of Wyoming. He is responsible for development and implementation of electronic packaging solutions for automotive and non-automotive applications.

Holistic approach to improve the reliability of sub-5µm L/S Cu RDLs

By Ralf Schmidt, Jan Knaup, Ulrich Memmert, Jens Palm, Cornelia Jäger, Stefan Pieper, Uwe Kirbach, Thomas Beck [Atotech Group]

Advanced packaging technologies enable faster, thinner, and more efficient mobile devices. In particular, fan-out wafer-level packaging (FOWLP) allows for higher performance, decreasing form factor, and significant cost reduction [1]. Redistribution layers (RDLs) serve as rerouting of the connections within such packages (**Figure 1**). While scaling of this technology appeared to be straightforward in the past, next-generation FOWLP will require new solutions. The need for higher I/O counts requires miniaturization and decreasing thickness of the copper RDL traces. On the other hand, artificial intelligence (AI), high-performance computing, and automotive applications will pose challenges to the reliability and yield of the packages. Decreasing copper thickness and lines/spaces (L/S) result in a strong decrease of the reliability of the RDL. FOWLP involves a combination of different materials and the respective mismatch in coefficients of thermal expansion (CTEs) may lead to stress impact between the components upon thermal load.

In a typical FOWLP, die and mold compounds make up the majority of the device volume. Hence, these components exert such large forces upon the comparatively thin RDL stack that it must essentially follow the dimensions of the former. From the perspective of the RDLs, thermal fluctuations impose a defined strain upon both copper and dielectric. Therefore, copper and dielectric should exhibit excellent mechanical properties in order to fulfill the reliability requirements of the industry. **Figure 2a** illustrates a typical stress-strain curve of a high-quality copper layer undergoing a tensile test from which the mechanical properties of

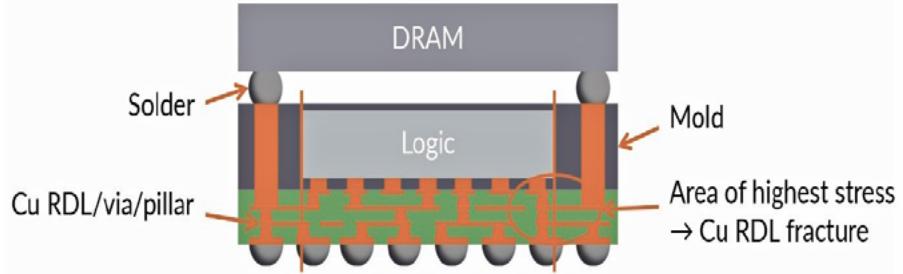


Figure 1: Schematic representation of a FOWLP. The circle highlights the areas of high stress impact upon the thermal load.

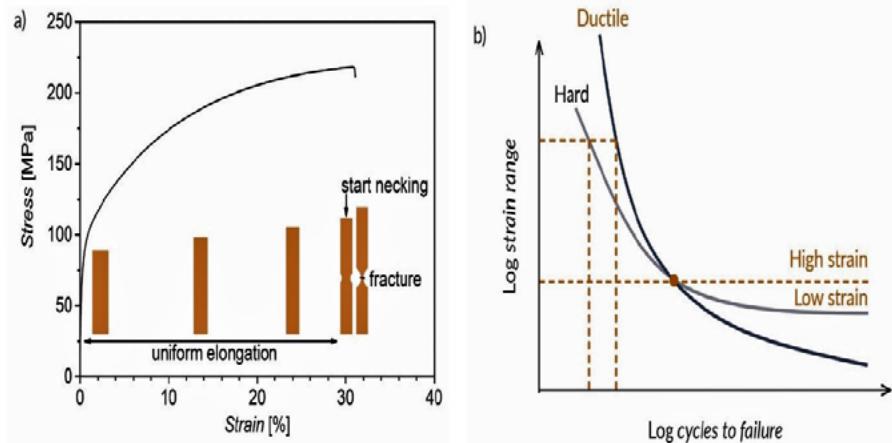


Figure 2: a) Stress-strain diagram of a copper deposit and schematic representation of the corresponding elongation and necking during the tensile test experiment. b) Schematic Wöhler analysis for copper deposits with high tensile strength and high ductility.

the deposit can be obtained. During stretching of the sample, uniform elongation will take place initially. In case the material is stretched further, it will experience necking, which means that the elongation is no longer uniform, but concentrated in a small area. The localization of the deformation may be caused by microscopic inhomogeneity of the material, which, in turn, may originate from impurities within the deposit, voids, or grain boundaries. The sample becomes locally thinner and ultimately fracture will occur in this area. The total elongation at fracture is called

the ductility of the material. The maximum stress a material can sustain is referred to as its tensile strength.

Failure mechanism of copper RDL traces

Thermal load may occur during production or operation, both leading to repeated heating and cooling of the package. Such repeated thermal cycles, therefore, induce cyclic mechanical loading and unloading, i.e., cyclic mechanical strain. It has been known since at least the 19th century that cyclic mechanical loading can eventually lead to fracture of the

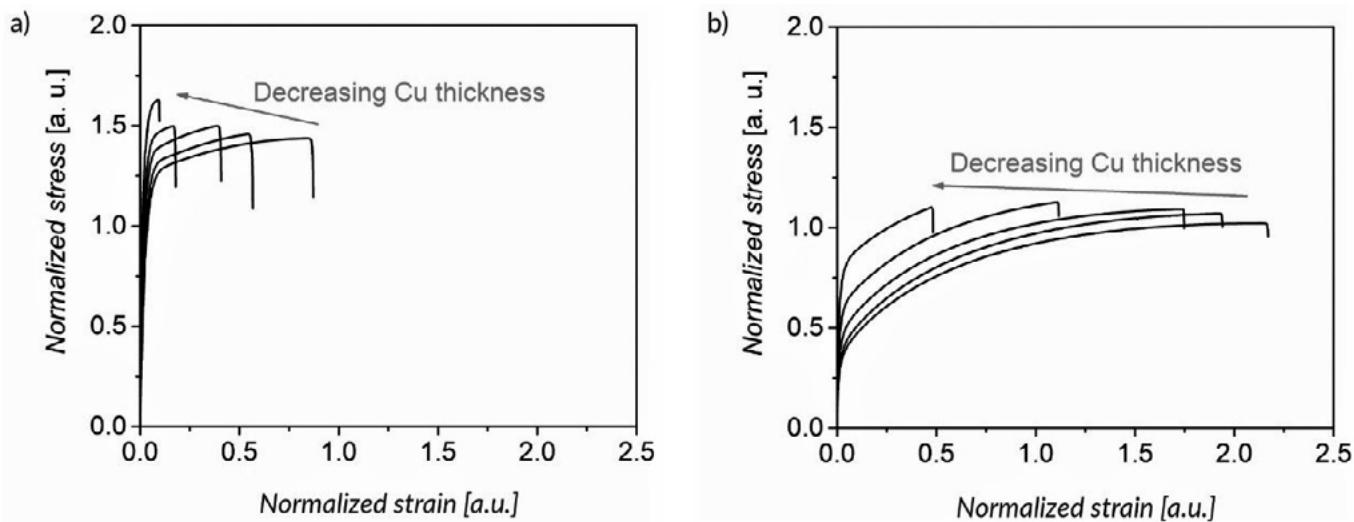


Figure 3: Stress-strain diagrams for a) medium and b) high-purity copper as a function of the deposit thickness.

affected part, even if each load cycle remains well below the part's limits of mechanical strength. This effect is referred to as fatigue fracture, or as metal fatigue, because the effect is especially visible in metal parts. If the mechanical loading takes the form of an externally imposed strain, as opposed to imposed stress, it is called strain-controlled fatigue.

One of the most useful tools to analyze the strain-controlled fatigue behavior of materials is the Wöhler experiment, in which pieces of the material are subjected to cyclic loading of defined strain amplitude and the number of cycles until failure is counted. These experiments are repeated for different strain amplitudes and the results plotted in a strain range over cycles to failure plot, called the Wöhler diagram. Figure 2b shows idealized curves for two hypothetical copper deposits: a hard and a ductile material. In the low-strain regime, the deformation is predominantly elastic, and the strain a given sample can sustain at a given number of cycles is proportional to the tensile strength of the material. In contrast, fatigue life in the high-strain regime is determined by the ductility of the material. As shown in Figure 2b, a more ductile material will withstand more cycles of a large given strain amplitude than a hard material with high tensile strength. Therefore, under the strain imposed onto RDLs during thermal cycling, high ductility will lead to improved device reliability.

Chemistry solutions to improve reliability

Optimization of the reliability may be obtained by improvement of the individual materials with regard to ductility. The mechanical properties of the individual copper material were shown to be impacted by the purity of the deposit, which can be controlled by proper design of the organic plating additives [2]. Figure 3 compares the properties of medium- and high-purity copper obtained from tensile tests at different layer thicknesses. The respective ductility values at a given thickness were significantly larger in the case of high purity. In general, a strong increase of the ductility and correspondingly improved reliability was observed with increasing purity of the copper.

Despite optimization of the individual properties of the deposited copper, a scaling issue was identified for both high- and medium-purity materials. In this context, a strong decrease of the ductility was observed with decreasing deposit thickness (Figure 3). This results in an increasing susceptibility to fracture upon decreasing the RDL L/S. In order to overcome this scaling issue, a holistic approach may be adduced. As schematically depicted in Figure 1, multilayer RDL packages

consist of copper traces and dielectric layers. The reliability of the package might be improved by considering the copper lines and the surrounding dielectric as strongly interconnected, therefore, as a whole, and not anymore as an individual material. Such interconnection would ideally result in the formation of a composite of the various materials. In this case, the mechanical properties of the composite, and no longer those of the individual materials, should determine the whole package.

Composite formation depends on creating strong adhesion between the materials. For this purpose, stacks of electrodeposited copper and polyimide dielectric both in the absence of, and in the presence of different adhesion promoters, were prepared and characterized in

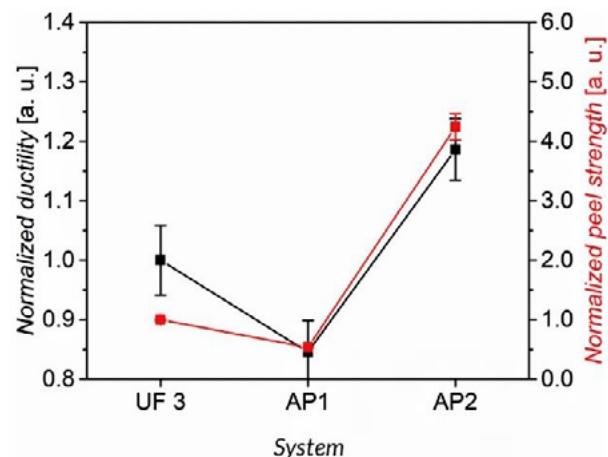


Figure 4: Normalized ductility of copper-dielectric stacks in the absence (UF 3) and presence of adhesion promoters (AP1, AP2), as well as corresponding normalized peel strength between the materials of the stack.

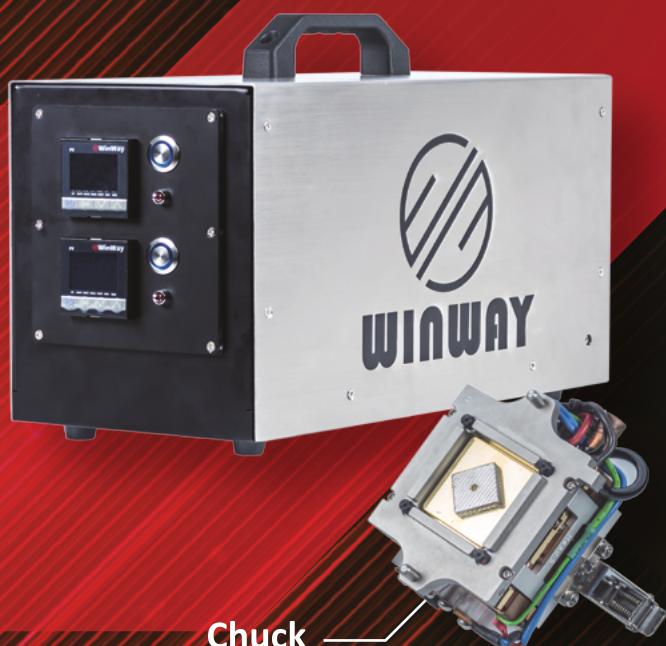


High Heat Density Thermal Lid

- Air-Cooled & Water-Cooled solution
- High performance cooling module
- Customized lid design
- Device power up to 1200W

Active Thermal Controller

- 800W Heat dissipation solution
- Active thermal management for DUT
- Mass production for Handler
- Stand-alone operation



sales@winwayglobal.com



www.winwayglobal.com

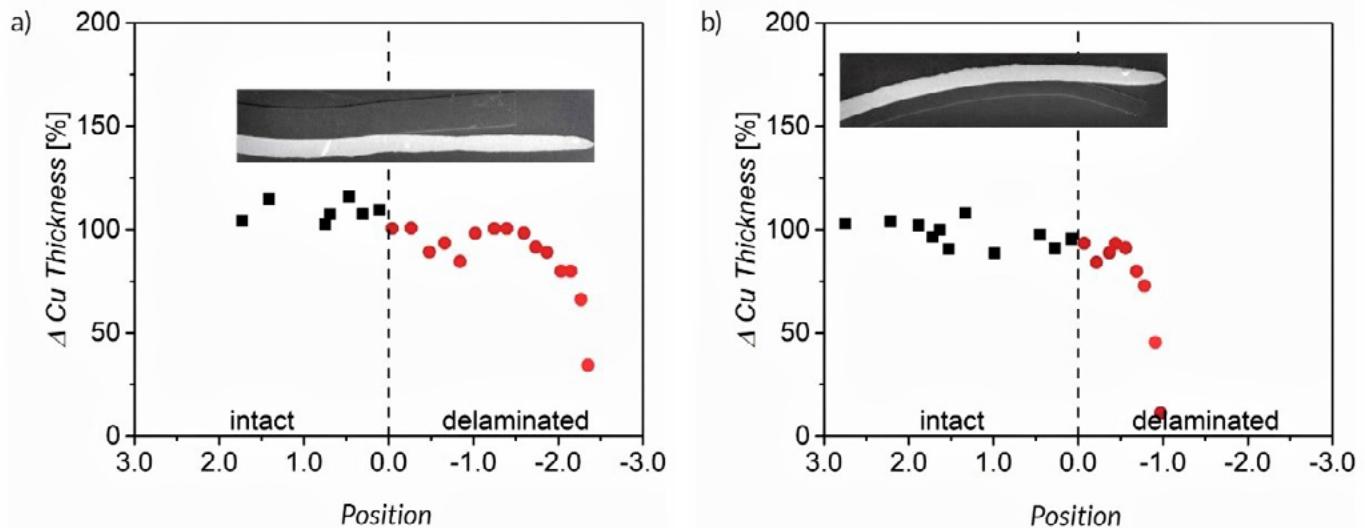


Figure 5: Copper thickness in the area of fracture for deposits obtained a) without an adhesion promoter, and b) with AP2. The insets show SEM micrographs of the area of fracture.

terms of adhesion and ductility. As expected from the considerations above, a correlation between the ductility of the system and the adhesion between the individual materials could be observed (**Figure 4**). The peel strength was used to characterize the adhesion and could be obtained by measuring the required force per unit area to separate two bonded materials, whereas the angle of separation was 180°. Adhesion promoter one (AP1) resulted in a decrease of the adhesion between the materials accompanied by a decrease of the ductility. In contrast, a strong increase of adhesion and ductility of the stack could be obtained with adhesion promoter two (AP2).

Scanning electron microscopy (SEM) cross sections were employed to generate a mechanistic understanding of the improvement of the mechanical properties upon formation of the composite. **Figure 5** shows the failure mode of Cu-dielectric stacks in tensile test experiments in which the copper-polymer interface was either left untreated (a), or treated with AP2 (b). In both cases, the interface underwent delamination around the fracture point and the shape of the metal tip shows ductile failure of the copper. Additionally, both samples exhibited significant curling after failure, indicating that the copper layer was permanently elongated by plastic deformation, while the more elastic polyimide reverted to its initial dimensions. At the untreated interface, the delamination zone is significantly larger than at the interface with adhesion

promoter. The copper in the long delamination zone of sample (a) is thinned out and exhibits significant necking in an area between the onset of delamination and the fracture point. In contrast, sample (b) exhibits much more uniform copper thickness close to and behind the delamination point. These observations indicate that the beneficial effect of increased adhesion on the composite ductility is caused by suppression of the necking instability in the copper. As soon as the adhesion fails at any location, this effect is lost, leaving the copper free to undergo necking in the delaminated zone.

Figure 6 shows SEM images at comparable scales of focused ion beam (FIB) cross sections of the untreated interface between electrochemical deposition (ECD) of copper and dielectric (**Figure 6a**), the interface treated with AP2 (**Figure 6b**), and for comparison, a Cu-dielectric interface treated with a roughening adhesion promoter (**Figure 6c**). The non-roughening adhesion promoter works by inserting a thin, nonconductive layer between the copper and polymer. Because it is non-

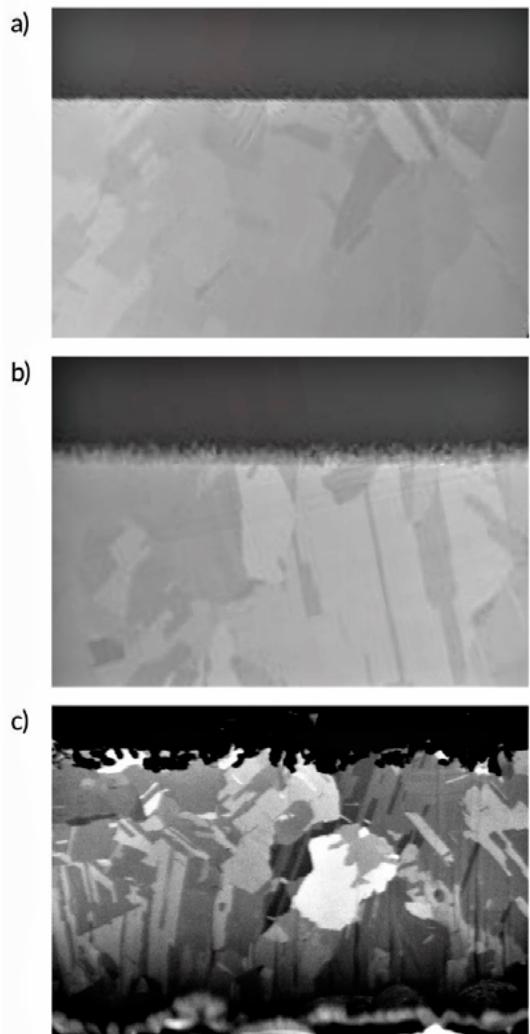


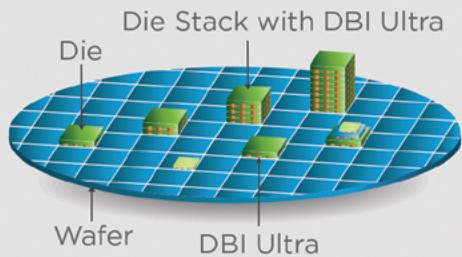
Figure 6: SEM micrographs of high-purity copper a) without adhesion promoter, and b) treated with AP2, as well as c) copper treated with a roughening adhesion promoter for comparison.



DBI[®] Ultra Die to Wafer Hybrid Bonding

The Ultimate 2.5D & 3D Integration Technology
for High Performance Computing

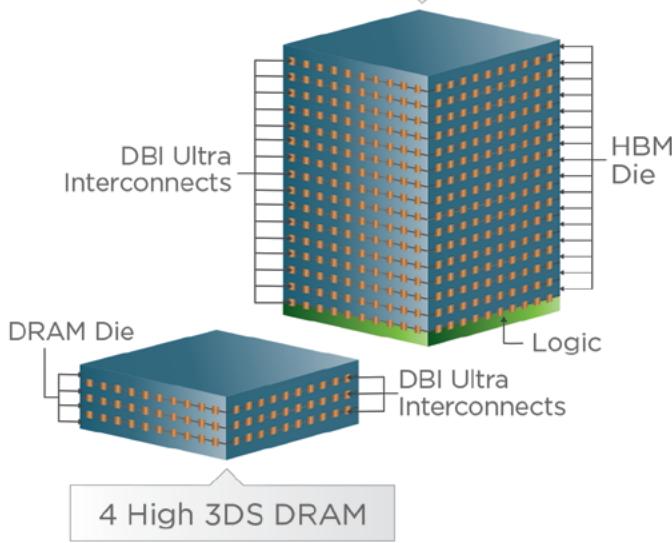
High Bandwidth, High Capacity, Thin Profile, Low Power, Low Cost



Ultimate Integration Flexibility
Accommodates various die sizes,
wafer sizes, process technology nodes, etc.

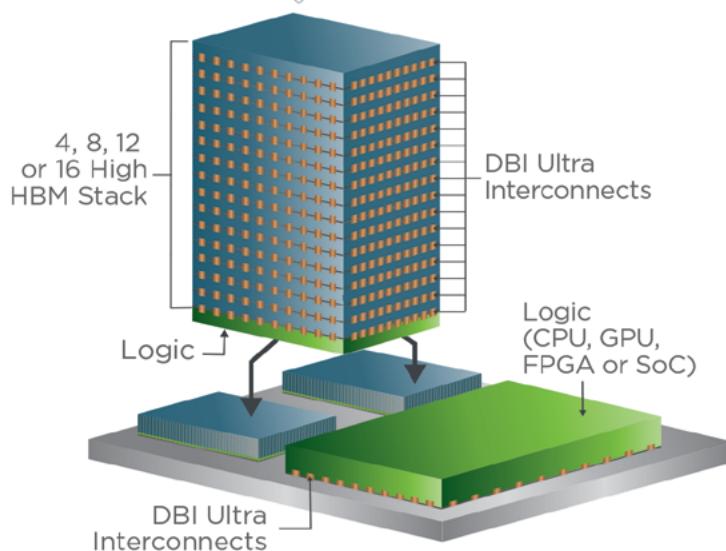
Enabling 3D Stacked Memory Solutions

4, 8, 12, 16 or more high HBM2, HBM3 & beyond



Enabling Next Generation High Performance Computing

2.5D Integration with DBI Ultra



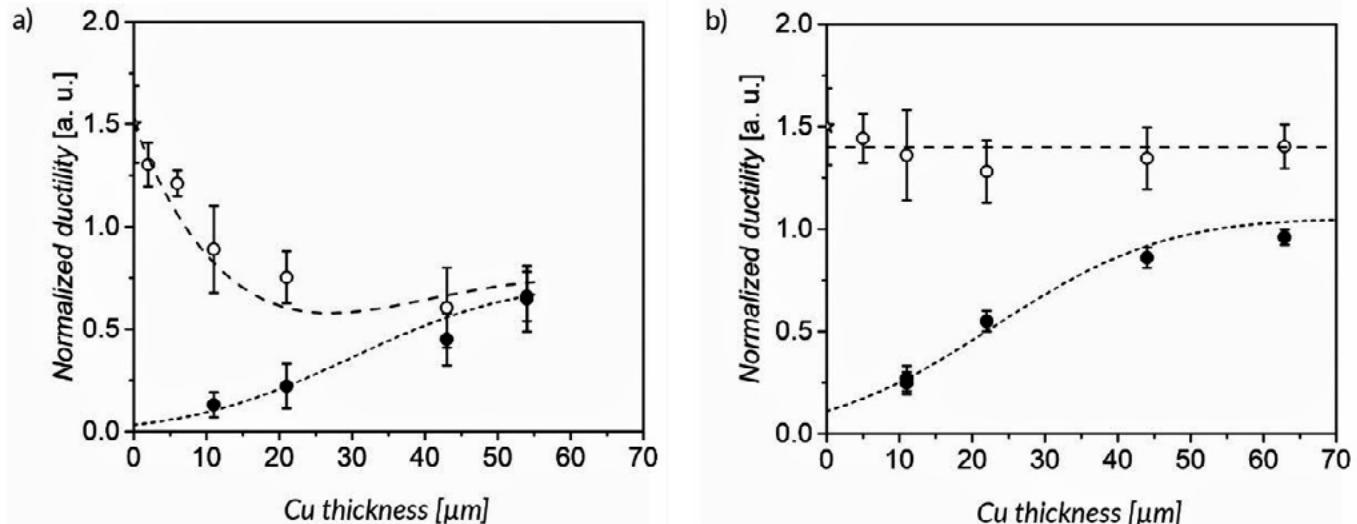


Figure 7: Normalized ductility of a) medium; and b) high-purity copper as a function of the deposit thickness for copper only (●), as well as a composite of copper and dielectric (○).

conducting, the roughness of the polymer-facing side of the adhesion promoter does not lead to elongation of the high-frequency signal path on account of the skin effect. Other than with a roughening adhesion promoter, with AP2 the conductive copper surface retains the flatness of the as-deposited surface, ensuring the same suitability for 5G, radar, and other high-frequency applications.

The effects of the copper deposit thickness on ductility, the corresponding scaling issue, and the approach to overcome this issue upon composite formation are summarized in **Figure 7**. A comparison of copper deposits without dielectric once more shows lower ductility values of medium purity (**Figure 7a**) in comparison to high purity (**Figure 7b**). The decrease of ductility upon decreasing deposit thickness was referred to earlier as a scaling issue. In general, a strong stabilization of fine copper structures by proper composite formation with the dielectric was observed. This could be deduced from the strong increase

of the ductility of the composite in comparison to the individual copper materials. The reinforcement was much more pronounced for high-purity copper deposits. While the benefit in case of medium-purity copper started smaller at low deposit thickness and diminished upon increasing thickness, the ductility became virtually independent of the thickness in the case of high-purity copper.

Summary

Chemistry solutions can help to optimize the reliability of copper RDL traces, especially at decreasing L/S dimensions. Optimization of the individual copper material may be achieved by increasing the purity of the deposit via proper design of organic additives. Further significant reinforcement of the mechanical properties may be obtained by using a holistic approach, i.e., using synergies with the surrounding materials within the package. Proper adhesion between copper and dielectric allows composite formation. Therefore, the various

materials of the package may no longer be considered as individual, but as a whole. This approach allows significant reinforcement of the mechanical properties upon a combination of high-purity copper material with a suitable adhesion promoter.

References

1. C. Melvin, R. Massey, *Chip Scale Review* 2017, 21, 40-44.
2. R. Schmidt, T. Beck, R. Rooney, A. A. Gewirth, “Optimization of electrodeposited copper for sub-5 μm L/S redistribution layer lines by plating additives,” IEEE 68th Electronic Components and Tech. Conf. (ECTC), 1220-1225 (2018).



Biographies

Ralf Schmidt is Manager R&D Semiconductor at Atotech Group, Berlin, Germany. He holds a PhD in Organic Chemistry and joined the company in 2011. Before his current position, he was team manager in the central R&D department at Atotech. Email ralf.schmidt@atotech.com

Thomas Beck is Regional VP, South East Asia at Atotech Group, Berlin, Germany. Prior to his current position, he was Global Product Director Semiconductor—responsible for the definition of R&D projects, integration/introduction and marketing-related activities for ECD (pillar/RDL) and electroless (ENEPIG) processes, respectively, and lead frame and connector products.

Die-to-wafer hybrid bonding for 2.5D and 3D integration

By Laura Mirkarimi, Guilian Gao [Xperi Corporation]

As Moore's law is reaching a physical limit, continued market pressure drives the interconnect density higher, requiring finer pitch wafer package technology with stacking solutions. While solder flip-chip technology has enabled continuous die and package pitch scaling over the past five decades, it appears to have reached its limits around 40 μm for volume manufacturing. Shrinking solder volumes much below a 40 μm pitch creates a yield loss at assembly from solder bridging or opens, and at environmental stress tests due to fatigue failures from embrittlement of the solder. The industry consensus has settled on the need for a new, all-solid and preferably all-Cu interconnect technology. An all-Cu interconnect is particularly attractive for its high current carrying capability and resistance to reliability failures. With a single component interconnect, there is no driving force for inter-diffusion, unlike solder-based interconnect structures like solder-capped/Cu/under bump metallization (UBM). However, historically an all-Cu interconnect was believed to require thermal budgets of 400°C to join the Cu pads, which would exclude a large number of products that require maximum temperatures near 250°C.

The technology that addresses each of the challenges noted above is Direct Bond Interconnect (DBI®) hybrid bonding. The benefit of this interconnect stems from its simplicity—a barrier metal layer with Cu interconnect embedded in a dielectric layer formed at back end of the line (BEOL). Interconnect formation at BEOL wafer fabrication offers sub-micron pitch scaling at the die-to-die (D2D) interconnect. The proving ground for this technology was wafer-to-wafer (W2W) image sensor applications and it revitalized image sensor product applications. Image sensor manufacturers leveraged this technology to dominate the market by offering novel multi-functional image sensor products year after year [1].

The die-to-wafer (D2W) hybrid bonding technology we describe promises to revolutionize the packaging industry. Currently, two application areas are the focus of the industry. The first application area is in 3D stacking of high-bandwidth memory (HBM)/dynamic random access memory (DRAM) to replace the thermal compression solder-capped microbump in the sub-40 μm pitch range. The second application targets an ultra-high density interconnect at a 1 μm pitch for compute-intensive chipsets. Interconnect scaling to sub-micron pitch between die will enable widespread disaggregation for high-bandwidth applications in the future. In the near term, the transition from solder to all Cu for current 3D and 2.5D stacking applications offers a more reliable interconnect formed at 200°C, with exceptional electrical performance because of the smaller parasitics associated with each Cu interconnect [2].

We review the DBI Ultra technology with a 40 μm pitch test vehicle and compare it with the current solder microbump technology. As with any new technology, the barriers to adoption are lowered when it is compatible with the industry supply chain. We discuss the compatibility of this technology with advanced packaging in high-volume manufacturing (HVM) today.

Challenges with solder interconnect/fine pitch

Significant height variations can be realized across wafers prepared in standard processing, because each step of making the die and substrate ready for bonding introduces thickness variations. For example, the plated bump height uniformity across a wafer can vary by 5 to 10% because of electroplating process nonuniformity. In addition to the local solder height variation, the die may have an overall warp from the unbalanced build-up differences on each side of the die (i.e., solder ball on one side and not the other). A flip-chip solder ball connects the top and bottom pads of an interconnect pair during solder melting and solidification. Because the liquid solder can be deformed easily in the molten stage and retain the deformed shape upon solidification, the soldering process compensates for some degree of height variation. When the height difference of the opposing joints are beyond the solder deformation limits, over compression can cause the neighboring solder balls to bridge and form a short circuit failure, while excessive stretching can cause the solder ball to break and induce an open circuit failure. Some of the factors contributing to height variations are illustrated in Figure 1 [3].

Die Assembly Elements and Height Variation

- Microbump die bump co-planarity
- In-situ interposer or substrate module warpage
- Non-parallelism between head and stage
- Z-position control accuracy

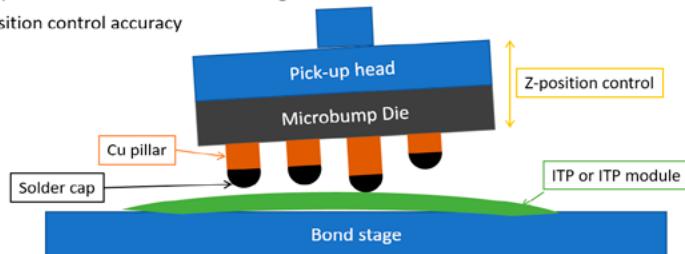


Figure 1: A schematic of a die bonding to an interposer or module has inherent height variation issues, which can be reduced or enhanced with the bonder capability.

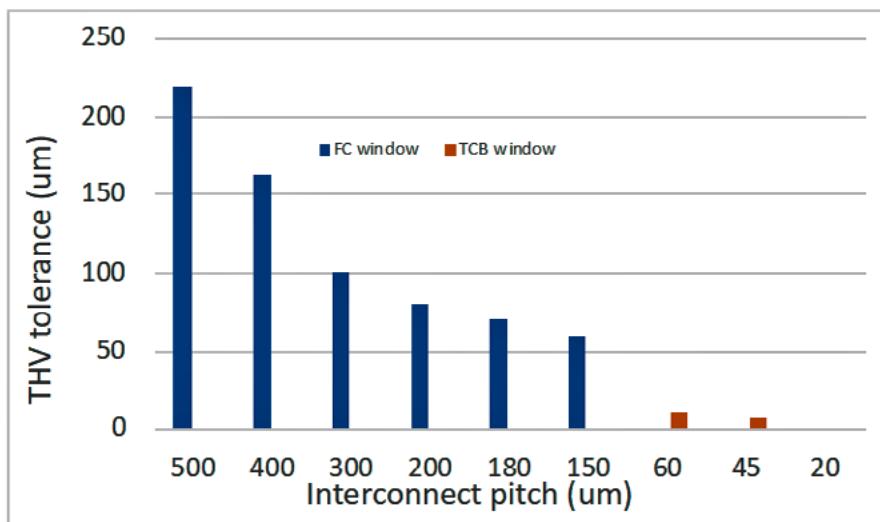


Figure 2: Total height variation tolerance is shown as a function of interconnect pitch for solder-capped Cu interconnect.

The total height variation (THV) tolerance is defined as the height that may be accommodated by the soldering process [3]. As shown in **Figure 2**, the THV tolerance is a function of the solder interconnect pitch. As the pitch shrinks to around 60 μm , the solder-capped microbump is required to reduce a short circuit failure due to solder bridging. However, adding a Cu post to the joint substantially reduces the solder volume and the THV tolerance. At 20 μm pitch, the THV tolerance is only 1 μm . Because the electroplated solder-capped microbump alone has a height variation exceeding 1 μm , such a process is unlikely to lead to high assembly yield. The fact that the solder interconnect pitch has been stalled around 40 μm for several years appears to support Arkalgud's, et al., analysis [3].

The packaging industry has been actively exploring alternative all-solid interconnect technologies in the past decade. Among the options explored, DBI Ultra, a low-temperature D2W and D2D hybrid bonding interconnect technology, has emerged as a winner and is the most promising for high-volume adoption.

Technology details

DBI Ultra is an extension of the mature W2W DBI bonding technology to D2W and D2D bonding applications. The DBI technology was invented by Ziptronix (now Xperi Corp.) [4-6]. It is a low-temperature hybrid bonding technology with all-solid metal interconnects that are hermetically sealed by the surrounding dielectric material. The most commonly used material combination for this hybrid bonding is

Cu interconnect with silicon oxide. The BEOL infrastructure in wafer foundries is leveraged for the Cu damascene process to fabricate the bonding layers.

The new technology has numerous advantages. It is an all-Cu interconnect with high current carrying capability. The all-inorganic material stack behaves like a single Si die for heat dissipation and for thermal-mechanical reliability. While thermal compression bonded stacks with underfill suffer from a significant temperature gradient between die 1 and die 4, a hybrid-bonded 4-die and 8-die stack has a minimal temperature gradient [2]. Additionally, the small size interconnect creates a greatly reduced parasitic resistance, capacitance, and inductance, which is ideal for high-frequency applications [2]. Additionally, the DBI hybrid bond forms a hermetic seal around the Cu interconnects, making it ideal for a harsh environment, such as automotive or corrosive environment.

As illustrated in **Figure 3**, the DBI bonding is a two-step process. The first

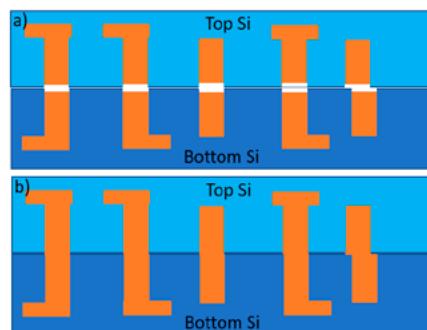


Figure 3: Schematic drawing showing the DBI a) spontaneous dielectric-dielectric bond; and b) the Cu-Cu bond at elevated temperatures.

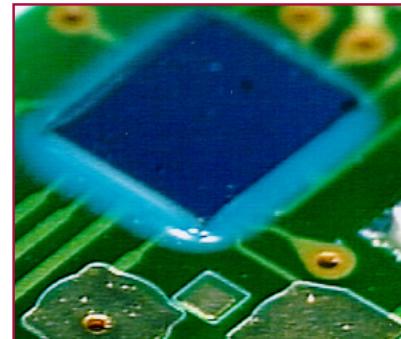
stage of bonding (**Figure 3a**) includes the ultra-smooth oxide surfaces that bond spontaneously on contact, forming a protective seal around the metal pads at ambient. The metal pads are purposely recessed from the oxide surface to avoid interference with the oxide bonding. The bonded structures then go through a heated batch anneal. During the anneal, the metal pads expand to close the narrow gap between the top and bottom pads and metal diffuses across the interface to form permanent all-Cu bonding (**Figure 3b**). High assembly yield requires a surface topography of smooth oxide for the spontaneous dielectric-to-dielectric bonding and a uniform bond pad recess across the entire wafer. A pristine surface during bonding is critical to ensure a void-free bond interface. Finally, in order for the technology to be adopted in high-volume manufacturing, the assembly process must have a high throughput and be compatible with the supply chain in the packaging industry today. We have addressed these challenges with our engineering development team and share some of the highlights below.

Surface topography control with chemical mechanical polishing (CMP). Standard BEOL CMP requirements do not match those required for hybrid bonding and are known to have a dependence of the Cu recess upon the feature size. For hybrid bonding, the CMP process should repeatedly provide topographic control across the entire wafer within the nm-scale range. Sufficient surface topography control was demonstrated with our CMP processes for ultra-fine pitch (1.6 μm) in the wafer scale back in 2009 [5]. However, for the 40 μm pitch application space it was critical to develop a robust CMP process for a bond pad size as large as 15 μm , given the pick and place equipment resolution in HVM at +/-7 μm 3 σ in 2017. We developed a robust CMP process to achieve Cu recess uniformity across both 200 and 300mm wafers with only a few nanometers of variation. These CMP processes have been successfully transferred to our partner and licensee facilities with similar results. While the dicing process generates a large number of particles; the die surface must remain free of particles to promote good bonding. Our thin die handling process was qualified with both saw dicing and laser stealth dicing in our test vehicle.

Cleanroom environment. A clean environment for wafer and die processing is required to maintain clean surfaces during material preparation and bonding.

Laser Assisted Bonding

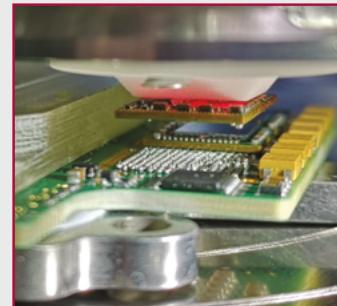
The LAPLACE-system provides an integrated solution for flip chip assembly, the laser reflow will be done during the placement - all in one step. The laser assisted assembly can be applied for soldering, ACF and NCP interconnections. The optional dispensing unit in the flip chip assembly platform allows a maximal flexibility for flux, solder paste and/or ACF, NCP dispensation.



New Applications

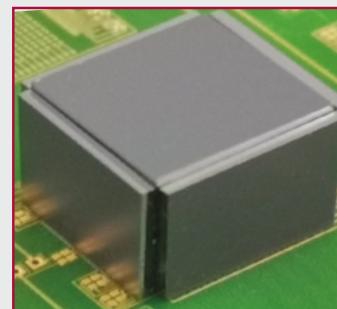
Selective Chip Rework

- Selective removal of bad die
- In-situ replacement & reflow
- Cost saving for high density fan-out packaging



3D Packaging

- In-situ die placement & reflow
- Lowest thermal & mechanical stress
- High chip stack uniformity



3.5D Multilayer Die Stacking

- Horizontal & vertical chip assembly
- No requirement for TSV structures
- Simplification of complex package design



ISO 9001
IATF 16949
ISO 14001
ISO 50001

www.pactech.com
sales@pactech.com



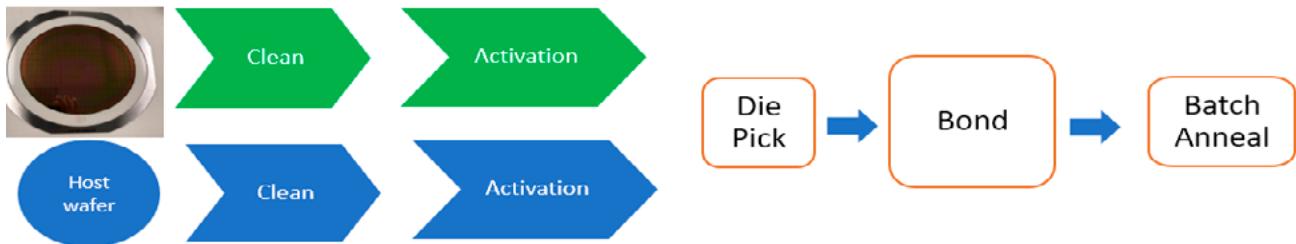
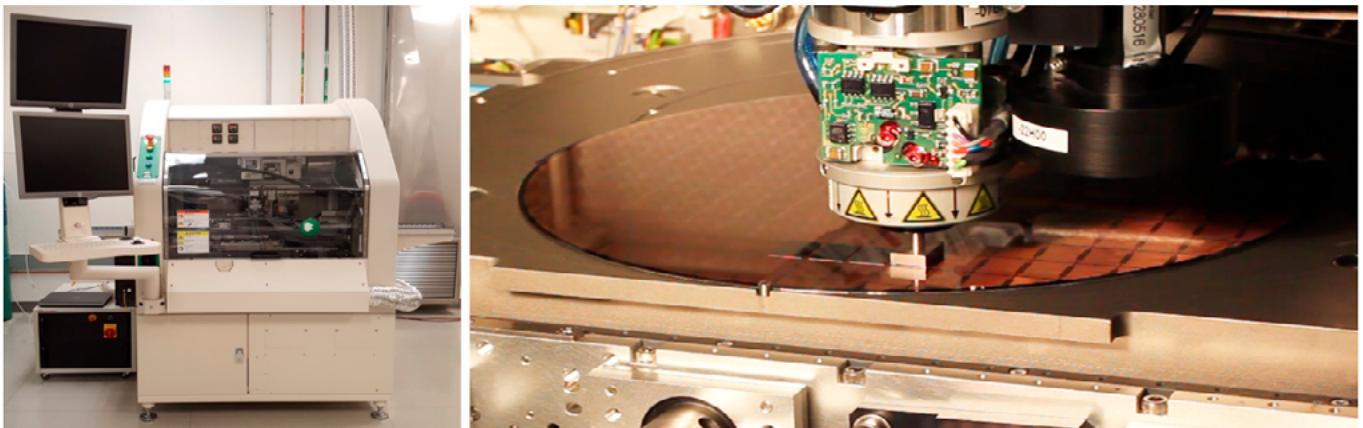


Figure 4: Process flow schematic for DBI bonding.

	TCB with NCF	TCB with NCP	DBI (Besi-Evo)
Mat'l handling (s)	10	1.5	1.1
Bonding (s)	30	8	0.1
Total time (s)	40	9.5	1.2
Throughput (UPH)	90	379	3000

TCB = thermal compression bonding

NCF = is non conductive underfill film

NCP = is non conductive underfill paste

Table 1: Throughput comparison table for various bond techniques.

Advanced packaging facilities have realized the importance of micro-environments for enhanced yield. DBI Ultra assembly requires a minimum of 1K cleanroom environment. Some equipment should provide a higher cleanliness requirement, such as the bonder. We currently retrofitted a flip-chip bonder with a class 100 clean kit for our bonding experiment.

Assembly throughput and assembly cost. The new bonding process is essentially a no-flux pick-and-place process. The oxide bonding is spontaneous once the die surface touches the mating surface. Therefore, a high-throughput

bonding process is possible. **Table 1** shows a side-by-side comparison of bonder throughput for thermocompression bonding (TCB) with nonconductive underfill film (NCF), TCB with nonconductive underfill paste (NCP), and DBI Ultra [7]. The very short bonding time of DBI Ultra is well-suited for high-volume package assembly. In our assembly process, we slow down the bonder to approximately 1600 die/hour using a single bond head to achieve better alignment accuracy.

The high bonding throughput is enabled by a die preparation process carried out on a dicing frame. With this process, the

diced wafer is cleaned on the dicing frame and fed directly into the flip-chip bonder for pick and place. The method not only simplifies the die preparation process to reduce cost, it also minimizes die handling to prevent die breakage and contamination.

Figure 4 illustrates the assembly flow including wafer and die preparation and bonding. With this process, we have achieved assembly yield >90% with 8x12mm size die, as shown in **Figure 5**.

Assembly process window assessment. A wide assembly process window is critical for a high-volume assembly process. Three factors are critical for the assembly process window. The first is the plasma process to enhance the bond energy of the dielectric surface, the second is the ability to control Cu recess, and the third is the queue time between wafer and die processing and bonding. Material held in inventory for up to 12 months that is able to bond with no issue indicates a broad process window with no special inventory control.

Pitch scaling limitation. Currently, the pitch scaling for DBI Ultra is limited by the alignment accuracy of the pick and place bonder. We have demonstrated 40µm pitch bonding using a flip-chip bonder with 7µm alignment accuracy, and 10µm pitch bonding using a bonder with a 1µm alignment accuracy [8]. High-throughput bonders with sub-µm alignment accuracy are currently

DIE BONDING AND DISPENSING SOLUTIONS

SCALE WITH US

R&D/
MEDIUM
VOLUME



MRSI-705

MRSI-M3

HIGH
VOLUME



MRSI-HVM

1.5
MICRONS

MRSI-H

- Sensors
- Photonics and Optoelectronics
- Microelectronics
- Microwave and RF

MRSI
MYCRONIC

+1 978 667 9449 | sales@mrsisystems.com | mrsisystems.com

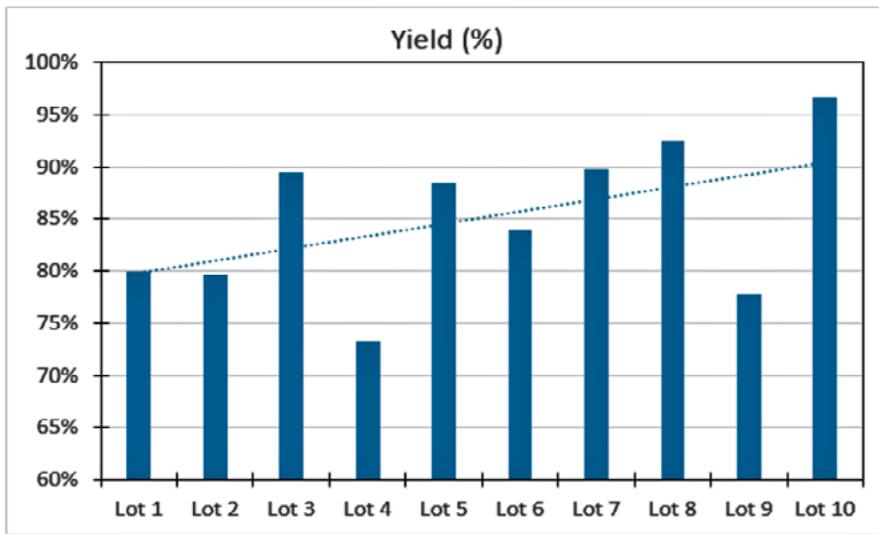


Figure 5: Yield of lots shown in time sequence.

Process Step	Solder Capped Micro-bump	DBI Ultra
Passivation opening	Yes	Yes
Lithography	Yes	Yes
Adhesion layer, Cu seed layer	Yes	Yes
Cu electroplating	Yes	Yes
Ni electroplating	Yes	No
Solder electroplating	Yes	No
Resist strip	Yes	No
Wet etch (Cu + adhesion layer)	Yes	No
Solder reflow	Yes	No
Cu CMP	No	Yes
THV across a wafer	Several micron	Several nm

Table 3: Comparison of the device side bonding surface fabrication process steps for solder-capped microbump and DBI Ultra.

Process Step	Solder Capped Microbump	DBI Ultra
TSV reveal CMP	Yes	Yes
UBM (Adhesion layer, seed layer)	Yes	No
Lithography	Yes	No
Cu electroplating	Yes	No
Ni electroplating	Yes	No
Resist strip	Yes	No
Wet etch (Cu + adhesion layer)	Yes	No
THV across a wafer	Several micron	Several nm

Table 4: Comparison of the back side bonding surface fabrication process steps for solder-capped micro bump and DBI Ultra.

in development. The next generation of bonders will push bonding pitch to the ultra-fine region where revolutionary 3D-IC integration can be enabled.

Fine-pitch example

Future HBM and DRAM packaging is expected to scale below 40µm. Our new bonding method can enable at least two generations of pitch scaling and the alignment accuracy can be met with existing high-precision flip-chip bonders. The two challenges addressed in our development are low-temperature anneal and multi-layer stacking. We have demonstrated solid Cu-to-Cu joints after a 200°C/1 hour anneal with very high yield, as shown in Table 2 and Figure 6 [9]. This proof point of low thermal budget anneals for an all-Cu interconnect suggests widespread applications of hybrid bonding. Conventional direct Cu-to-Cu thermal compression bonding requires bonding

Build	Sample ID	Anneal Temperature (C)	# Die Pass/# Die No Defect	% Yield
1	#1-1	200	24/26	92
2	#2-1	200	20/20	100
3	#3-1	200	19/19	100
3	#3-2	200	13/13	100
3	#3-3	200	15/15	100

Table 2: Electrical test results of samples annealed at 200°C for 1 hour.

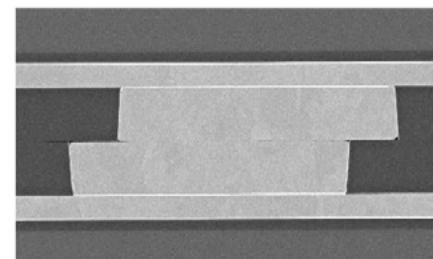


Figure 6: Cross section of a DBI interconnect formed at 200°C.

temperatures of 350°C to 400°C. Various approaches have been explored over the years to find the right solution to reduce the anneal temperature, as reviewed by Panigrahi and Chen [10]. However, no options reviewed in the paper appear to be worthy of high-volume production.

Test die of 8x12mm with 31,356 DBI links were used to measure the die assembly yield at low temperatures. The main daisy chain that we tested for the yield in

Table 2 occupies 50mm² of bonding area, which is approximately 10 times the size of the through-silicon via (TSV) area for the HBM2. If any one of the 31,356 links does not close, the entire chain fails the electrical continuity test. The 90+% yield built in multiple process lots shown in **Table 2** demonstrates that the DBI Ultra is capable of low anneal temperature applications. We have also demonstrated Cu-to-Cu bonding after a 175°C anneal.

As a means to compare the costs between stacked HBM with a DBI interconnect and a solder-capped microbump interconnect, the process steps for fabrication of the front and back side are compared in **Tables 3** and **4**. The new bonding method offers significant process simplification. The device side bonding surface for the DBI Ultra die uses a BEOL CMP process to replace the following process steps in the microbump die: Ni plating, solder plating, photoresist strip, wet etch, and solder reflow. For the back side die processing, the new process eliminates the following

process steps that are carried out on the microbump die: adhesion layer deposition, seed layer deposition, lithographic process for pad definition, Cu electroplating, Ni electroplating, photoresist strip, wet etch for seed layer and adhesion layer removal. Additionally, the new method eliminates the underfill assembly process. The significant process savings in wafer-level fabrication coupled with the elimination of the underfill process is attractive from a cost perspective.

Figure 7a shows the side by side comparison of TSV solder microbump joints and DBI Ultra joints with TSV. We have demonstrated that joints made with the new process showed no sign of resistance increase even after extended testing at the automotive JEDEC specification temperature cycling, high-temperature storage and autoclave test [11].

Acknowledgement

The authors thank the 3D-IC development team members at Xperi for their technical contributions presented in this paper.

References

1. H. Tsugawa, H. Takahashi, T. Nomoto, et al., “3.2 Pixel/DRAM/Logic 3-layer stacked CMOS image sensor technology,” IEDM, Dec. 2017.
2. S. Agrawal, G. Huang, G. Gao, L. Wang, J. DeLaCruz, L. Mirkarimi, “Thermal and electrical performance of direct bond interconnect technology for 2.5D and 3D integrated circuits,” IEEE 67th Elec. Comp. and Tech. Conf. (ECTC), pp: 989-998, 2017.
3. S. Arkalgud, G. Gao, B. Lee, “Addressing challenges in 2.5D and 3D IC assembly: assembly process window analysis,” 3D ASIP, Burlingame, CA, Dec. 2014
4. P. Enquist, “High-density direct bond interconnect (DBI) technology for three-dimensional integrated circuit applications,” MRS Proc., 970, 0970-Y01-04. doi:10.1557/PROC-0970-Y01-04, 2006.
5. P. Enquist, G. Fountain, C. Petteway, A. Hollingsworth, H. Grady, “Low cost of ownership scalable copper direct bond interconnect 3D IC technology for three-dimensional integrated circuit applications,” 2009 IEEE Inter. Conf. on 3D System Integ., 3DIC 2009; 1-6. 10.1109/3DIC.2009.5306533.
6. P. Enquist, “Advanced direct bond technology in 3D integration for VLSI systems,” S. Koester, C. S. Tan, K. N. Chen Eds., CRC Press, 2012, pp.: 175-214.
7. G. Gao, L. Mirkarimi, G. Fountain, L. Wang, C. Uzoh, T. Workman, et al., “Scaling package interconnects below 20µm pitch with hybrid bonding,” IEEE 68th ECTC, p. 314, 2018.
8. G. Gao, G. Fountain, P. Enquist, C. Uzoh, L. F. Wang, S. McGrath, et al., “Development of hybrid bond interconnect technology for die-to-wafer and die-to-die applications,” IW LPC, San Jose, CA, Oct. 2017.
9. G. Gao, L. Mirkarimi, T. Workman, G. Fountain, J. Thiel, G. Guevara, et al., “Low temperature Cu interconnect with chip to wafer hybrid bonding,” IEEE 68th ECTC, p. 314, 2018.
10. A. K. Panigrahi, K. N. Chen, “Low temperature Cu-Cu bonding technology in 3D integration: an extensive review,” Jour. of Elec. Packaging 140(1), Nov. 2017.
11. G. Gao, L. Mirkarimi, T. Workman, G. Guevara, J. Theil, C. Uzoh, et al., “Development of low temperature direct bond interconnect technology for die-to-wafer and die-to-die applications—stacking, yield improvement, reliability assessment,” IW LPC, San Jose, CA, Oct. 2018.

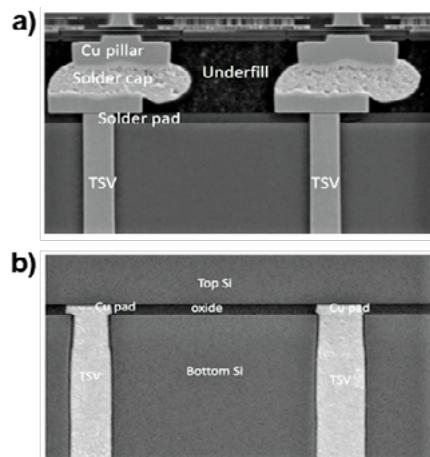


Figure 7a: Cross section image from two die joined with a) solder-capped Cu pillar (courtesy System Plus Consulting Report, “AMD Radeon Vega with HBM2,” Nov. 2017), and b) DBI Cu pad bonded to TSV interconnect.

Biographies

Laura Mirkarimi is VP of 3D Portfolio and Technology at Xperi Corporation, San Jose, CA. She received a PhD in Materials Science at Northwestern U. With 15 years of experience in electronic packaging, Dr. Mirkarimi leads the 3D team at Xperi. Prior to joining Xperi, she developed electronic devices including ferroelectric memory, transparent conductors and photonic crystal resonators at Hewlett Packard Laboratories for 12 years. Dr. Mirkarimi holds 43 patents and more than 40 publications. Email laura.mirkarimi@xperi.com

Guilian Gao is Distinguished Engineer in 3D Technology at Xperi Corporation, San Jose, CA. She received her PhD in Materials Science from the U. of Cambridge. Dr. Gao has 30 years of experience in electronics packaging technology development, materials, processes and reliability engineering. Before joining Xperi, she was a Senior Technical Specialist at Ford Motor Co. and was awarded the Henry Ford Technology Award. She holds 42 US patents and has more than 30 publications.

Navigating dicing on increasing complex shrinking die

By M. Todd Wyant [Texas Instruments]

In semiconductor manufacturing, all circuits are placed onto the wafer with an applied street width between component structures, enabling a process that cuts the wafers into individual pieces following wafer fabrication processes. After spending so much time and effort creating complex and challenging circuits, it can be frustrating that the first processing step during assembly uses various techniques to singulate individual circuits, as those steps can create potential damage to such delicate circuits. Nonetheless, mechanical dicing of wafers has been the process of record for many years. Mechanical dicing utilizes a high-speed diamond blade to remove unwanted silicon between circuits. This diamond blade can be adjusted and changed to meet many differences with silicon technologies, metal densities and configurations.

Mechanical dicing has long been a significant challenging manufacturing process step for any semiconductor operation. Mounting pressures to push die per wafer increases, in an effort to lower costs, create a situation where narrow scribes in a growing complexity of devices is normal. These increasing improvements also require the same quality levels within the fracturing location. This shifting complexity continues to weigh heavily on the mechanical dicing operation, creating a delicate balance that continues to be important to the overall success of any manufacturing operation. This article covers many key inputs that directly affect the dicing operation.

Understanding the dicing process

There is a key relationship between dicing parameter interaction, the intrinsic material properties, and material technologies created by internal device fabrication monitoring requirements within the factory.

Step one in any fabrication process is aligning wafers consistently to enable accurate pattern placement in

generation of silicon semiconductor products. Typically, this is dependent on the fabrication alignment used and is generally determined by alignment among equipment vendors to maximize process capabilities. In most cases, back up patterns and multiple placements are performed to enable alignment stability over the course of time and compensate for manufacturing and equipment variability in wafer fabrication areas.

Figure 1 shows an example shot map, and the red box locations show the estimated alignment locations as laid

out for a typical device produced. The entire map shows how the stepper is used to layout the wafer for maximum efficiency of the equipment utilized to align and build products. These structures are critical to fabrication wafer-to-shot alignment capabilities and necessary to enable production in high-volume manufacturing. The structures are typically composed of metal build ups shown in **Figure 2**.

These structures consist of via and solid metal covers comprised of each of the individual fabrication layers, with up to six metal thickness layers

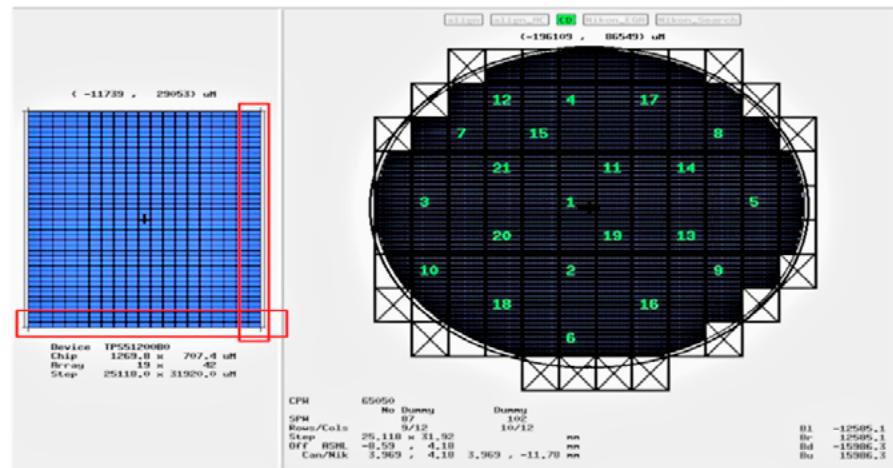


Figure 1: Standard shot map alignment locators.

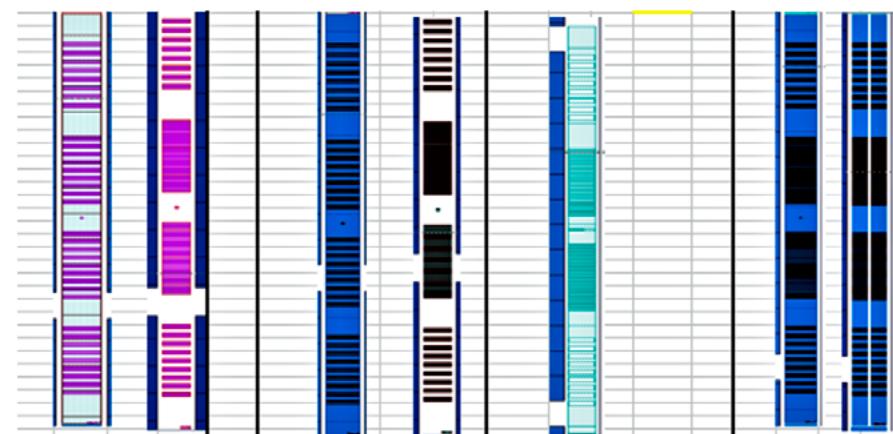


Figure 2: Typical aligner markers for fab production.

in total. The metal areas are up to 6 microns in thickness and are of varying metal types in random locations in each reticle shot field. As metal levels and structures increase in complexity, the metal density increases. Increasing metal density creates more difficulty in loading mechanical dicing blades, resulting in increases chipping, blade wear and quality losses.

The next challenge is process control in the wafer fabrication process. To incorporate process controls, the wafer streets are designed with features to enable the capability to do live probe, metal thickness measurements, as well as film measurements during processing. All these steps assure that the wafers built meet the electrical requirements needed, but they also require additional film, metal boxes for metrology measurements, as well as test pads to probe during processing. These are needed for each metal/fabrication layer that is placed, and they are stacked in the dicing street to save silicon for active die and maximize die per wafer increases.

Figure 3 shows an example of testing pads' locations on the die during wafer fabrication processing. These pads typically encompass all oxides, as well as each metal layer, with increasing thicknesses across the scribe street during manufacturing as a need for quality control. As metal layers and complexity increase, so do the number of test locations required to monitor and control wafer fabrication facilities. The structures are also complicated with moves to copper back end of line (BEOL) structures to increase device performance. Past work has been focused on optimizing mechanical dicing for use on aluminum pads and features, but the move to copper structures has required significant blade composition changes and process optimization to level set the dicing operations.

The last key factor impacting dicing capabilities is die size interaction as shown in **Figure 4**. As die sizes increase, dicing street loading with metallization also increases as fab processing typically requires the same test structures on smaller versus larger devices. As a result, this constant component load requirement loads the entire step field layout with metal streets. This layout technique, in turn, causes entire dicing streets to be loaded with metallization in both the horizontal and vertical scribe locations. Metal-filled

dicing streets create issues where the mechanical saw dicing blades' diamond cutting surfaces are fully embedded with metallization. High metallization filled dicing streets create dicing issues with metal loading of the dicing blades that decrease process capabilities.

The dicing process typically involves a self-sharpening dicing blade that constantly wears and exposes new diamonds. In the case of blade loading

with metal, the blades' self-sharpening mechanism can be defeated, and the blade begins to push into the silicon. Metal interaction then surfaces, and can create damage during cutting. This damage creates yield issues and is compounded during production operations. Blade dressing increases, not fully solving the problem, and therefore long term blade breakage and product damage can result.



THE BURN-IN WITH TEST COMPANY



The worldwide leader in test with burn-in systems, Micro Control offers solutions for high-power burn-in test applications requiring individual temperature control and logic/ memory burn-in test applications for lower power devices.



Micro Control Company's burn-in systems feature a pattern zone per slot, multiple temperature zones and independent temperature control per DUT. With up to 64 M of vector memory behind all 128 independent I/O channels, Micro Control systems can handle many different functional tests.



Have other needs?
Micro Control Company provides burn-in boards, prescreen stations, carts, and continuity testers.

7956 Main Street NE | Minneapolis, MN 55432 | 800.328.9923 | microcontrol.com

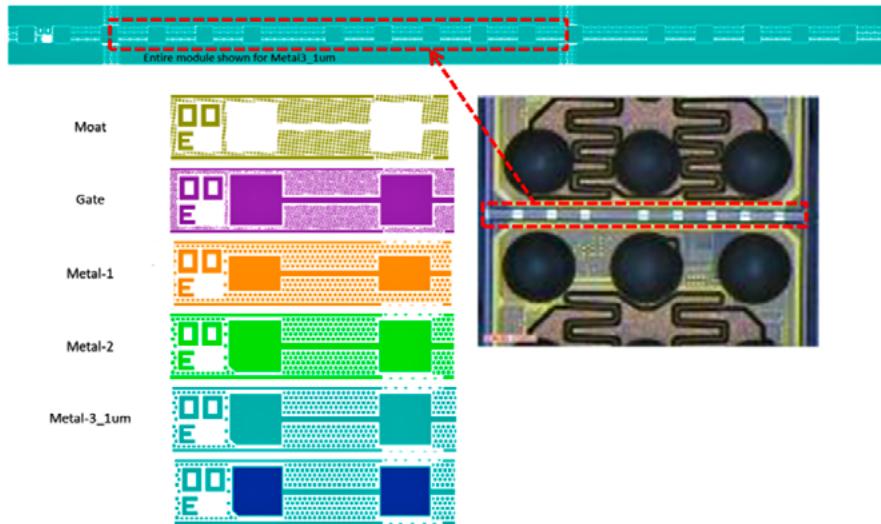


Figure 3: Probe pad example.

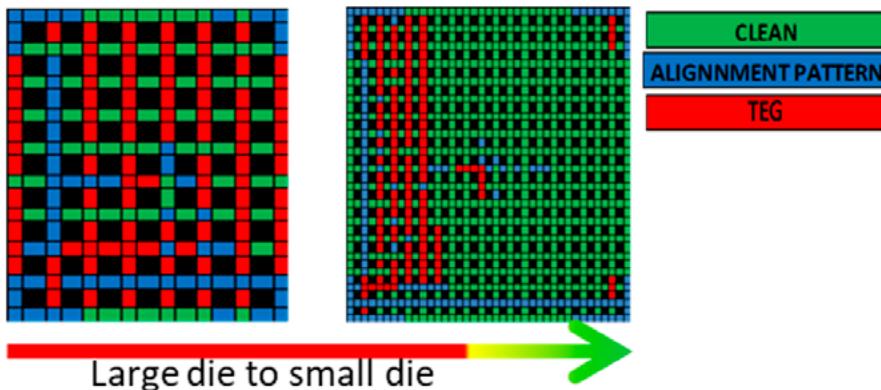


Figure 4: Die size interaction to open streets.

Driving improvements

As die sizes shrink, improvements in structure layout and placement can enable improvements in dicing and chipping. However, there is not one rule—it's all standard as technology, metal layers, and device composition will drive further complications on loading impact to mechanical dicing.

Street width is a large factor in the design process. Typically, streets are designed to enable placement of all necessary structures required for alignment, test, and statistical process control within the wafer fabrication areas. If room on prohibited streets are sometimes fitted with double and triple scribes, metallization and placements can be spaced out to improve and lower density of dicing street areas. In this manner, there is a die per wafer loss and improvement in dicing capability.

Another option is to utilize die drop-in reticle shots. This is counter intuitive in the wafer fabrication area, as it incorporates complex techniques, called blading, that increase mask cost, and can impact one or the highest cost processes in a wafer fabrication facility. Blading enables drop-in die that are designed to incorporate all of

the test pads and wafer fabrication features into a subset of the wafer. Blading enables a die loss and product cost increase, but eliminates many modules from the dicing streets. Removing the modules creates a clean area for cutting and loading that improves problems associated with mechanical dicing. There are other complications that interact, such as films used, and wire bond versus a bumped device, but the major items discussed here are the driving reasons for mechanical dicing complications.

Packaging requirements and interactions

Now that we have covered wafer fab complications, let's now move on to packaging requirements and interactions, wafer dicing challenges associated with package type, and finally, interaction with scribe structures that need to be considered during the design phase.

For example, if your device is for the automotive market, you should consider asking the following questions: Does it have burn-in? Is the package prone to high stress? Knowing your end customer's requirements and asking these questions are normally considered during a design phase review. However, many times parts are multi-purposed and can be sold across many different package types, families and end user types. This situation complicates the process further. Don't panic if you are a dicing engineer. The daily challenge of the job is to review in advance and predict metal density capabilities, and then adjust and work to solve complex dicing challenges prior to them happening.

Figure 5 shows a very challenging dicing situation. This is the output of a new and challenging design type released. Shown in the figure is a six metal layer example of a dicing street structure with

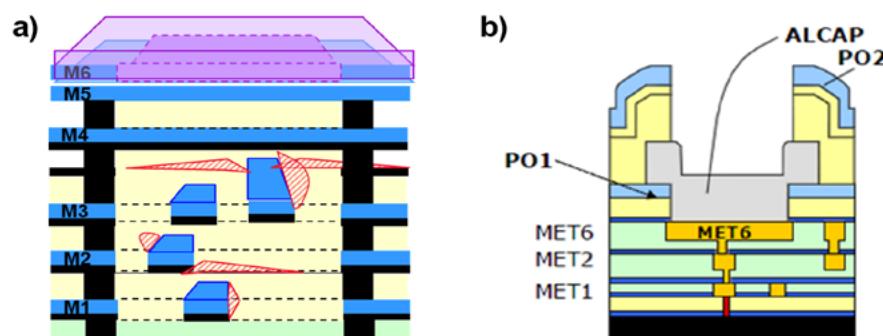


Figure 5: Cross section of 6-metal layer device.

Microsystem Integration SiP Solutions

the metal stacks highlighted. Between each metal layer is a dielectric or low-K type of material that is stacked for device performance improvements. This device design has >5 microns of metal thickness in total. The stack up of the layers, along with each mask step in the wafer fabrication facility, leads to 38 stacked layers of interfaces at the end of processing.

The red areas in **Figure 5** indicate examples of possible inclusions from dicing or potential damage that is sub-surface during dicing of the wafer. These sub-surface interaction points can create failures as they can propagate to create damage across the scribe seal into the active device circuitry. Blade dicing these 38 layers happens in one or two passes of the mechanical dicing blade. Complexities arise when trying to find a blade composition that is adequate to handle all the individual material layers and still enable a singulated part that will not generate a defect during operation in the final product.

Figure 6 shows the introduction of increased complexity of the current 38 layers with a copper BEOL process. Copper is added to improve device performance capabilities. The copper is thicker and much more difficult for mechanical dicing operations. Copper tends to load dicing blades via a new failure mode.

The blades used for dicing are constructed of electroplated nickel alloy with synthetic diamonds embedded into the plating process. With aluminum back end of line, use of the blades is designed to remove aluminum and during dicing the blades are self sharpening. In conjunction with heat generated during dicing, the copper removed tends to bond to the nickel allowed at elevated temperatures, and then it is solidified in place during rotational cooling. This reduces blade life, increases chipping and dicing associated problems.

New dicing machines are incorporated with an inline-type dressing block that can periodically be used to free blades from loading with metals. The alloy of copper nickel created during dicing is much more difficult to address with auto dressing techniques, and leads to risks and more failures for mechanical dicing.

New blades are dedicated to improve dicing for copper, but limitations still exist that were not associated with aluminum BEOL stack up in the past. An evolution is underway to improve blade technologies for copper cutting, but new limitations and increasing costs are associated with copper solutions. With wafer interactions, there are many variables that affect chipping. **Figure 7** shows the major impacts to chipping during mechanical dicing. Best-case wafer process design requires use of many of these interactions to drive the appropriate wafer fabrication design standards for long term success of any wafer design.

From a mechanical dicing standpoint, there are also multitudes of dicing inputs impacted by the silicon and package design. Dicing interactions with inclusion of the silicon design aspects called out in **Figure 8** combine to create vast complexity that should be

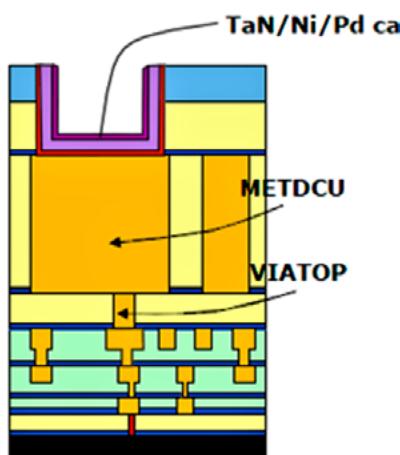
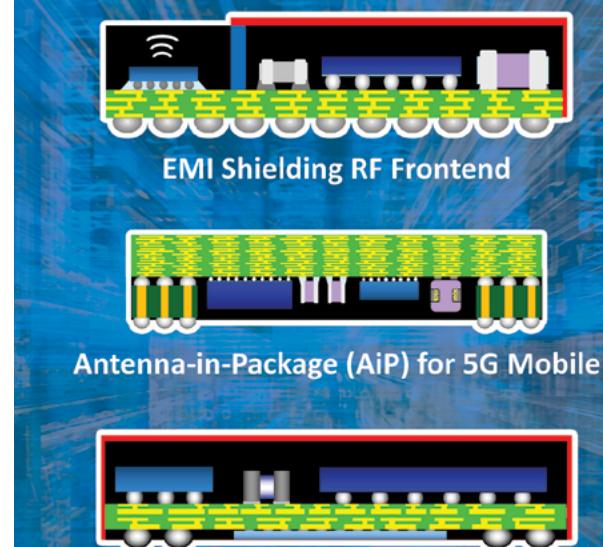


Figure 6: Copper back end heavy metal cutting.



Double-Sided Molding 5G RF Frontend SiP



www.jcetglobal.com

monitored and reviewed to positively impact design improvements as a process plan of record. This shows the importance of design for manufacturability and the critical component for feedback. All of these inputs combined show the complexities and critical interface loop between designs for manufacturability purposes.

Summary

To keep unwanted defects from escaping, sound practices of design for manufacturing should be used and implemented within all design centers. As noted, dicing streets are becoming more complex with increasing device functionality needs, and this interacts with die size reductions and the drive for smaller dicing streets while still meeting end user requirements.

There is not one common direction or decision that can be made on what is in the dicing street any longer, as it really is driven by far too many factors that enable negative results from the dicing standpoint. The key is having a solid manufacturing review process and feedback loop to the design

tts

TestConX 2020 / Hilton Phoenix, Mesa
May 10 - 13, 2020 | Booth #28

Semicon China 2020 / SNEC, Shanghai
June 27 - 29, 2020 | Booth #4721, Hall N4

P0.15mm WLCSP PROBE HEAD

• www.tts-grp.com •

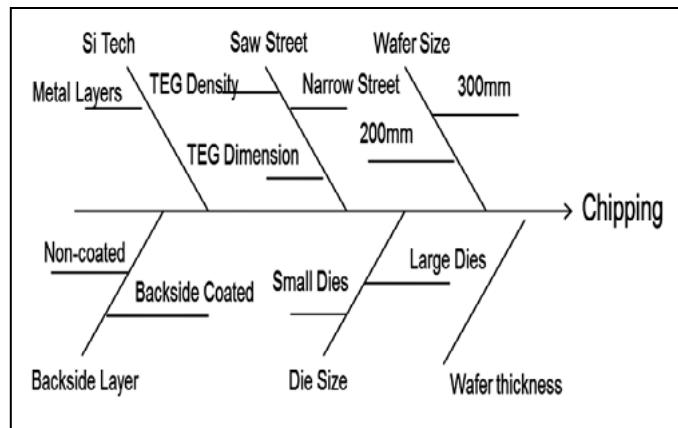


Figure 7: Silicon interaction to chipping.

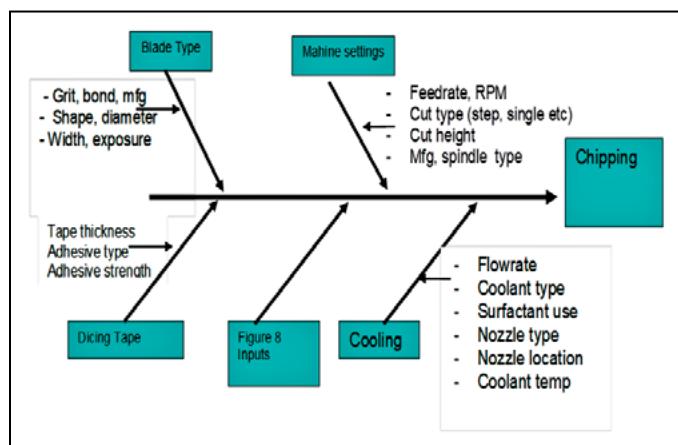


Figure 8: Dicing assembly interactions.

teams so that design for manufacturability based on lessons learned is incorporated for long term success.

The best case is to design for the worst case technology challenges and enable the best process design up front and design process capabilities accordingly. Formulating lessons learned and utilizing a test chip strategy early with new silicon releases will eliminate unwanted surprises as complexities grow and continue to grow over the life of a silicon node or platform.

Reference

1. M. Todd Wyant, "Wafer chip-scale package cost reductions," Mar/Apr 2015, *Chip Scale Review*, Vol. 19 No. 2, pp. 54-56.



Biography

M. Todd Wyant is Sr. Member of the Technical Staff, Semiconductor Packaging Organization, Dallas, TX. His career spans 25+ years and includes roles at Chrysler Corp., General Motors, and Delphi Electronics before he joined TI. He earned a BSME in Mechanical Engineering from Purdue U. and a Six Sigma Black Belt from AIT. Email m-wyant@ti.com

Going beyond traditional scaling with SiP

By Yoko Fujita, Tuan Hoang [Zuken]

Moore's law no longer rules electronics' miniaturization [1]. Today, companies are turning to system-in-package (SiP) design instead of the traditional flip-chip approach. The drive towards SiP, however, presents new challenges. Engineers must assess performance against cost factors early and throughout the development process. This article details a new method of gaining such insight, relying on simulation conducted early and throughout the design process, even merging into physical tests. As a result, engineers make better, more informed decisions at each stage of development.

The Internet of Things (IoT) is coming to a product near you. However, it may not arrive in a form that many expected. Many assumed that chips would continue to follow the improbable miniaturization of Moore's Law: the number of transistors in dense integrated circuits will double every two years. Recent news shows that the industry is diverging from that prediction. On August 2018, GLOBALFOUNDRIES announced a halt to all 7nm chip development, opting instead to focus on specialized processor work [2]. In December 2018, Qualcomm introduced the 7nm, 5G ready Snapdragon chip [3]. A report from Yole Développement [4] characterized the broader trend in the industry that these two moves represented, predicting that the growth of fan-out wafer-level packaging (FOWLP) would outpace the traditional flip-chip (FC) packaging so tightly associated with Moore's law (Figure 1). It is clear that the future of electronics no longer lies in pure miniaturization. Going forward, SiP design approaches are critical to the successful advancement in the industry. However, significant challenges lay ahead.

Making the SiP choice

Today, the life cycle of every product is getting shorter. As a result, launching or delivering products on time is paramount. That leaves little time to make several

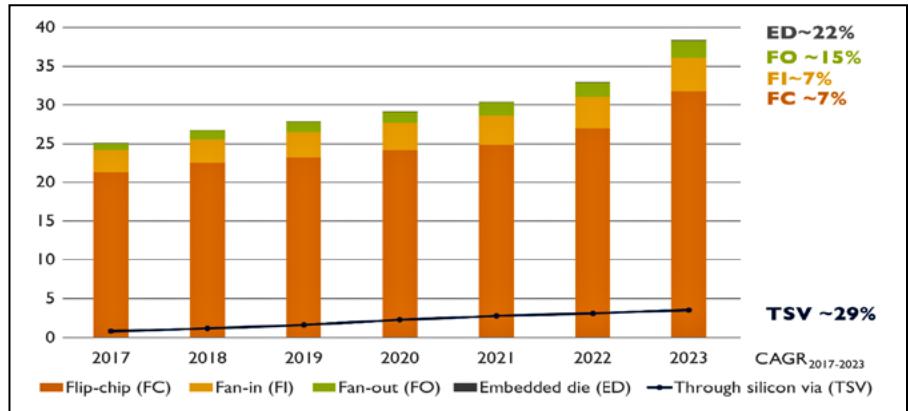


Figure 1: Advanced packaging revenue by platform in \$B. SOURCE: "Status of Advanced Packaging Industry 2018," Yole Développement 2018

	Legacy node 1 chip	Fine node 1 chip	Chip partitioning Multi chip
Packaging	Chip PKG	Chip PKG	Chip 1 Chip 2 PKG
Cost	Chip (Legacy) PKG (single)	Chip (Fine node) PKG (single)	Chip 1 (Legacy) Chip 2 (fine node) PKG + (single)
Performance	Low	High	Middle, High(CPU, GPU, SerDes etc)

Figure 2: Chip partitioning.

crucial decisions about SiP designs. One important decision is picking the correct chip size. In most cases, the smaller the chip, the lower the chip cost and the higher the package cost. Understandably, with larger chips, the cost of the chip climbs and the package cost drops. Choosing the right architecture depends on finding the right balance between these factors. That, however, is not the only consideration. In fact, making an architecture decision based on cost is the easy part.

The hard part of choosing the correct SiP architecture is verifying desired electrical characteristics (Figure 2). As the chip gets smaller, the bump pitch becomes narrower, causing the number of package layers to increase. With

this increased complexity, many signal integrity and power integrity issues manifest. That, in turn, directly affects the fulfillment of requirements for high-frequency applications.

The SiP architecture decision, however, does not only rest on cost factors. Heterogeneous integration affects the performance of the entire system. As a result, it is critically important to verify performance alongside this architecture decision, very early in the development cycle.

Verifying electronic characteristics

The traditional approach to verifying electronic characteristics lies in system-level prototyping and testing. A prototype

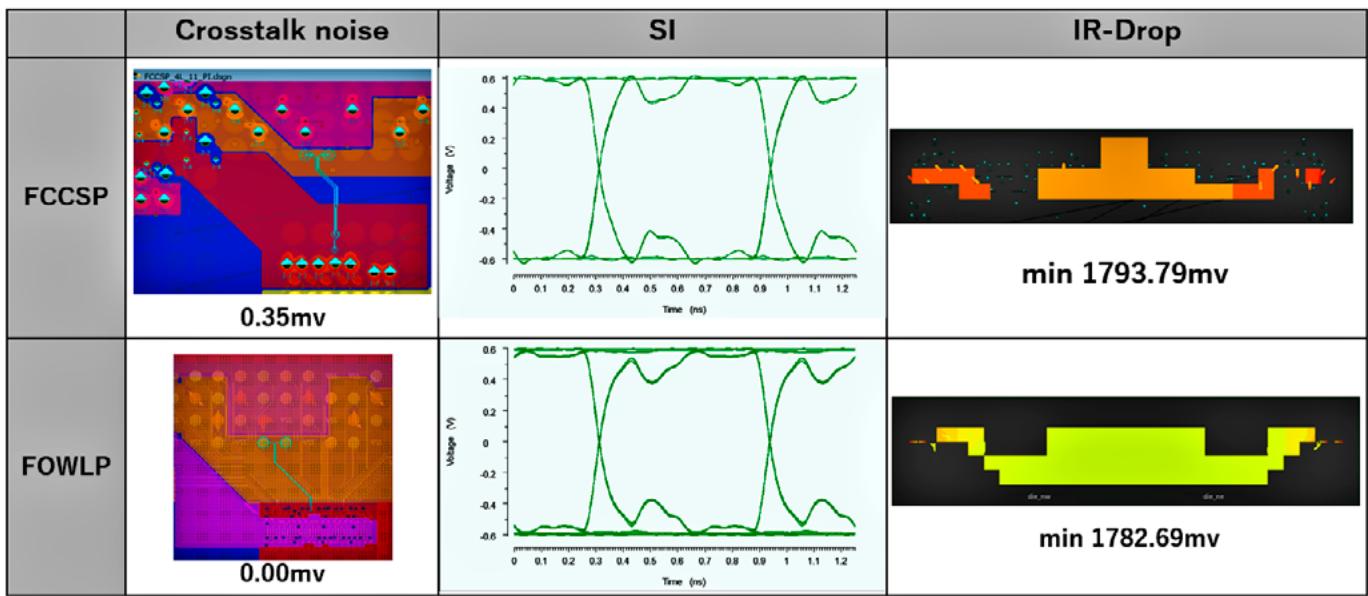


Figure 3: Comparison of SI/PI.

of the SiP is fabricated and then put through its paces to check performance. The problems with this approach, though, are the associated costs and required time. Remember, shorter life cycles are driving the need to launch or deliver products far sooner. There simply isn't time to build and test one prototype, much less multiple iterations if the initial architecture fails to perform as expected. It simply isn't feasible early in development.

Fortunately, there is an alternative approach. In 2019, we partnered with Socionext Inc., to develop an approach called prototype design [5]. This method uses design and simulation tools early to verify and iterate on SiP designs (Figure 3). The idea is to use digital methods to virtually test performance, long before any prototypes are built. When the initial prototype is built, it passes physical testing the first time. The process uses the following steps:

- Engineers in concept design determine the component sizes, placements, and connectivity;
- Engineers using the prototype design method confirm electrical characteristics, connect critical signals, shielding, as well as power and ground planes; and
- Engineers in detailed design prepare the production-ready design data.

Not only does this approach enable crucial verification early, it also reduces reliance on prototyping and testing throughout the development process. It

shifts the verification activity left, far forward into development through digital methods. This eliminates costly rounds of prototyping and testing. It also reduces the overall costs of development.

The short turnaround time environment

It is uncommon for the first iteration of any architecture to work the first time. That's the nature of engineering. An engineer can try one architecture and verify that it fails to meet requirements. The engineer then iterates to develop a new architecture to verify. The process continues until a successful design is

discovered. The same is true of SiP designs. This exploration of the design space allows engineers to make better, more informed decisions about design. Conducting a feasibility study early in development is key to success.

Also in conjunction with Socionext, we developed a quick prototyping environment (Figure 4) for feasibility studies using CR-8000 Design Force, Zuchen's 3D multi-board system design software. It starts with the definition of a product specification that drives large scale integration (LSI). That, in turn, drives the detailed definition of the package. That package is then used for the analysis, enabling the direct verification of the

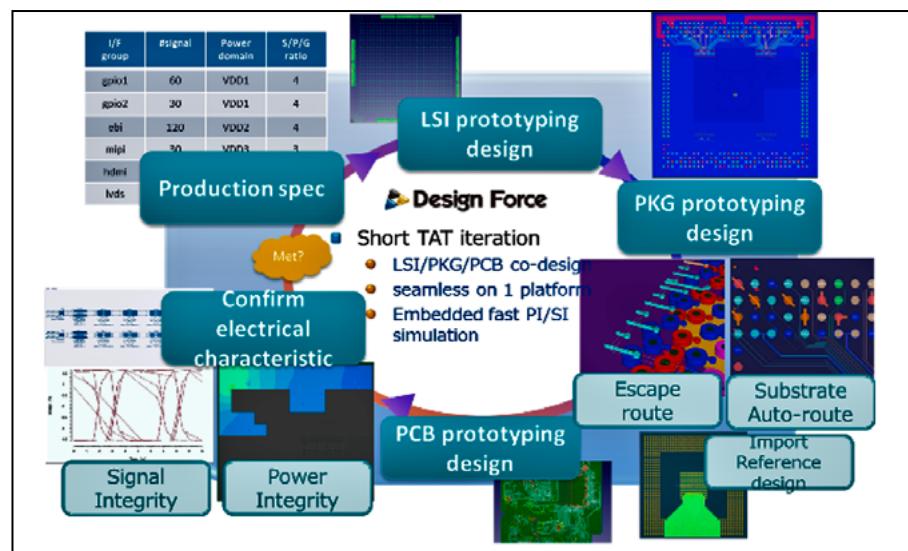


Figure 4: Quick prototyping design environment.

requirements in the product specification. The results of the analysis are used as a basis for design decisions to make changes to the LSI. Furthermore, engineers use this environment to compare and contrast completely different designs, such as FOWLP and FCCSP architectures.

This closed-loop approach can be executed quickly, empowering engineers to explore a wide array of architectures. Engineers use these iterative analyses to assess costs and verification of electronic characteristics. With deep insight into the design space, engineers make optimal SiP decisions.

Cross-company collaboration

Of course, few SiP architectures are developed solely by a single company. It is more frequent that one company is responsible for LSI design, another develops the board system, and another is accountable for the package design. In these more common circumstances, the definitions of each design are spread across many companies. This presents a challenge. As each company explores potential changes to the design of their aspect of the SiP architecture, they must synchronize their efforts with those of all the other designs.

Fortunately, the LSI Package Board (LPB) format solves the challenge (**Figure 5**). The LPB format is authorized by IEC 63055/IEEE 2401 for sharing and optimizing LSI, package, and printed circuit board (PCB) design. Design Force can import both C-format, G-format, and N format-based designs as an LSI component that includes placement consideration, net assignment, and design iteration.

The LPB format also allows multiple companies to perform signal and power integrity analyses, and verify electric characteristics with G-format. It enables portability across all of these companies. Multiple companies can exchange their designs, allowing each to conduct their own analyses and, as appropriate, contribute to a holistic simulation. Using this format eliminates the challenges associated with synchronization of efforts, enabling cross-company collaboration.

Adding detail progressively

Early in development, only portions of both LSI designs and packaging designs might be available. Fortunately,

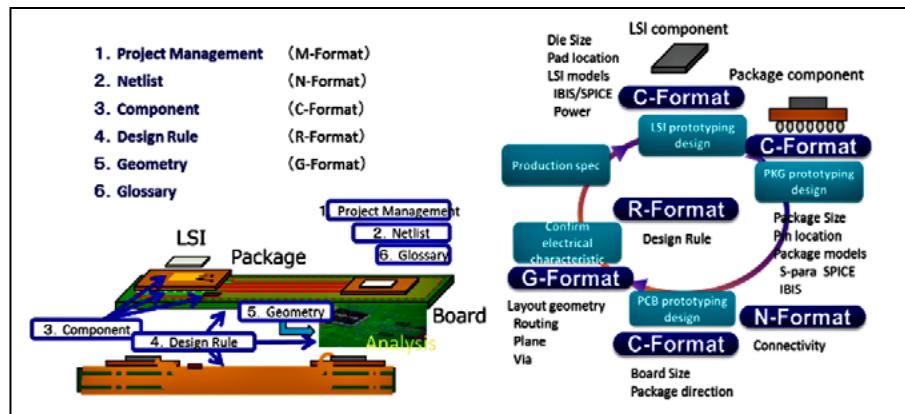


Figure 5: LPB format.

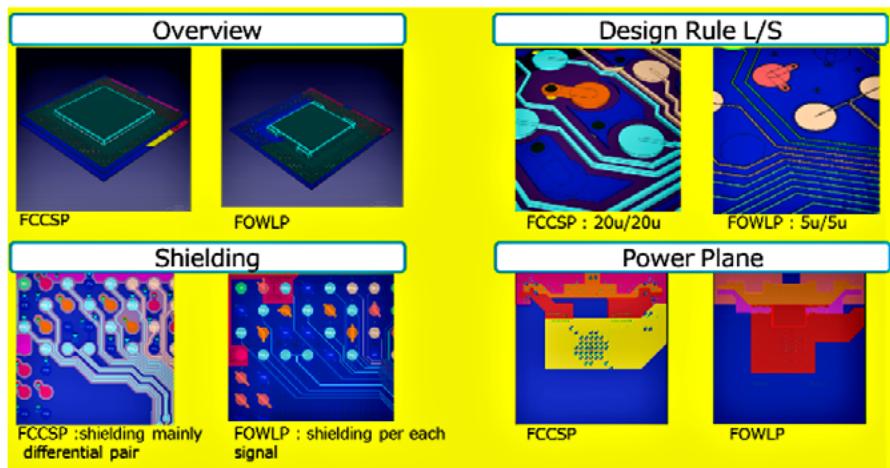


Figure 6: Prototype design.

the prototype design approach allows engineers to progressively add more detail to their analyses as they emerge as follows:

- The earliest steps start with the LSI prototype design. Initially, this only requires a minimal amount of information such as the product specification, the signal number of each function, and the power-to-ground ratio. The quick prototyping environment uses this information to generate the chip floor plan with the input/output cell, bump placement, and net assignment.
- Next up is package prototype design. In this step, the net is automatically assigned to package ball pins. It also defines escape routings from bumps and auto-routes the package substrate. Engineers can reuse existing reference designs.

- As a next step, electrical characteristics can be verified with tool embedded, high-speed power integrity and signal integrity simulation. This confirms the power supply characteristics and noise immunity.

This progressive approach requires minimal definition and information at each step while providing insight into performance. As the SiP design progresses, engineers get a more detailed picture of the tradeoff between cost and performance. This method doesn't just occur at a single stage of the design process—it happens progressively.

A better way to determine SiP architectures

Early decisions, influenced by costs and driven by verification, are crucial for SiP architectures. Traditional prototyping and testing approaches break down because of cost and time

BGA & QFN Sockets

Quick-Turn Custom Designs

- Bandwidths to 94 GHz
- Industry's Smallest Footprint
- Ideal for Prototype and Test
- Simulation Models Available
- Multi Level Stacked Sockets
- Five different contactor options
- BGA and QFN
- Sockets for ALL Xilinx, Microsemi, & Intel Chips
- Pitch 0.3mm to 1.27mm
- SMT Options



**Ironwood
ELECTRONICS**

1-800-404-0204

www.ironwoodelectronics.com

factors. Once again, we partnered with Socionext to develop prototype design approach based on a quick turnaround time design environment to solve these needs (**Figure 6**). The solution uses simulations of electrical characteristics from prototyped design as the design becomes more detailed. It is a closed-loop approach where the design definition drives the simulations that influence the design. The solution also supports multi-company collaboration and contribution for analyses. It leverages the IEC 63055/IEEE 2401 authorized LPB format. Additionally, it supports short turn around time (TAT) iteration, chip floor planning, pin assignment, substrate auto-route, and reuse reference design on the package. Ultimately, the prototype design approach allows engineers to answer key, early development questions in a new, faster way. This method empowers better decisions and provides other benefits throughout the development process

References

1. "Moore's law slows while costs continue to increase," <https://fuse.wikichip.org/wp-content/uploads/2017/12/amd-iedm-2017-23-1024x579.png>
2. "GLOBALFOUNDRIES halts 7nm work," <https://www.eetimes.com/globalfoundries-halts-7nm-work/#>
3. "Qualcomm announces 5G Snapdragon 865 chip," <https://www.theverge.com/circuitbreaker/2019/12/4/20995562/qualcomm-snapdragon-865-5g-camera-gaming-artificial-intelligence-improvements>
4. Yole Développement: http://yole.fr/AdvPackaging_Industry-A SETechForum.aspx#.XIQMWhKiU1
5. Y. Fujita, K. Koga, S. Ohtani, D. TsuTsui, "Quick prototyping design for More than Moore era," 2019 15th International Conference and Exhibition on Device Packaging.



Biographies

Yoko Fujita is a Senior Partner in the EDA Business Unit at Zuken, Inc., Yokohama, Japan. She is responsible for driving the R&D activity of chip/package/PCB co-design solutions. Before joining Zuken, she was a manager at an EDA startup company where she was responsible for product development of semiconductor design tools. Prior to that she worked at NEC Electronics focusing on the development of CAD for semiconductor design. Email yoko.fujita@jp.zuken.com

Tuan Hoang is an Application Engineer at Zuken, Inc., San Jose, CA. He has been in the EDA industry for more than 20 years, specializing in packaging and PCB design and has been part of the Zuken, Inc. team since 2016.

Laser-assisted bonding for fine-pitch cost-effective interconnection

By Nokibul Islam, KyungOe Kim, Chris Scanlan, Choon Heung Lee [JCET Group]

Advanced semiconductor packaging requirements for higher and faster performance in a thinner and smaller form factor continue to grow for mobile, network, high-performance computing (HPC), and consumer devices. The advanced node of the Si wafer drives fine-pitch bumping processes. A significant reduction of the bump pitch has been observed over the last few years, moving from 40nm Si to 5nm Si wafers. A further reduction in pitch is expected in the near future.

The adoption of fine-pitch copper (Cu) pillar bump has been growing as the solution for high-performance and low-cost flip-chip packages. Higher input/output (I/O) density and very fine-pitch requirements are driving small feature sizes such as small bump on a narrow pad, or bond-on-lead (BOL) interconnection. At the same time, higher performance requirements are driving increased current densities, thereby assembling such packages using a standard mass reflow (MR) process while maintaining its performance is a serious challenge. Thermocompression bonding (TCB) using non-conductive paste has been used to mitigate the assembly risk, up to a certain extent, of die size and package body size. On the other hand, the TCB process results in a significantly higher assembly cost because of very low throughput. For this reason, the cost-sensitive semiconductor market is not ready to adopt the TCB process.

To address the need for fine-pitch Cu pillar bumps, a new method of attaching fine-pitch bumps called laser-assisted bonding (LAB) has been successfully introduced in flip-chip packages. In this method, a laser (as thermal energy) is used to melt the solder cap, thereby joining with the substrate pads. No additional reflow process or excessive compression force is required. It's a very localized process and requires only a few seconds to join

the chips with the substrate. Because of the very fast process thermal budget and materials, thermal expansion mismatch is much lower than with MR or TCB, which results in less package warpage and less die-level stress. However, the laser scanning length of LAB is still limited to a certain size. As a result, throughput is about half that of MR, but compared to TCB, it is 2 to 3X higher. In this paper the pros and cons of various package assembly processes and comprehensive reliability data for fine-pitch packages, along with relative cost data, will be discussed.

Introduction

Chip interconnection pitch has scaled down significantly over the last few years mainly due to the need for higher bandwidth and more computing power in a smaller form factor system. As chip technology gets more and more advanced along with the goal of more product miniaturization, the need to reduce the chip package form factor while increasing chip performance is clear. Fine-pitch Cu pillar bumps are widely used for high-performance packages. Certainly, fine-pitch bumps do often encounter some assembly challenges in the chip attach process with traditional mass reflow. However, various chip attach processes have been introduced in the assembly line to overcome these challenges with advanced Si nodes ($\leq 14\text{nm}$ or 7nm).

MR continues to be the mainstream process for flip-chip packages, while TCB with non-conductive paste (NCP) used to be the best solution for finer bump pitch flip-chip die in the last few years. TCB certainly provides better chip attach yields with higher alignment accuracy, however it is a very slow process and quite often the bump shape becomes an issue because of excessive bond force. Other issues are die cracking, higher die/package warpage, etc.—LAB is the most

attractive alternative to overcome these issues. In this process, thermal energy from the infra-red (IR) laser heats up the die and makes the joint between the die and substrate using a fine interconnection. With Cu pillar, it melts the solder cap and makes the joints with the substrate pad. The laser beam used for this process is similar to the die size so the entire die can be heated up in one shot of a laser scan. A typical LAB schematic process is shown in **Figure 1**.

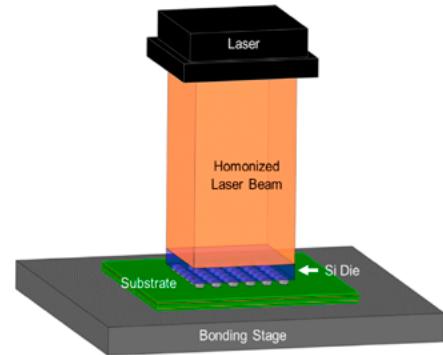


Figure 1: LAB chip bonding process. COURTESY: link.springer.com

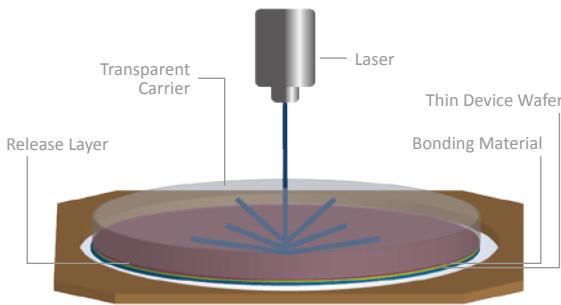
LAB pros and cons

There are various advantages of the LAB process over conventional mass reflow, for example: 1) it is a very quick chip joining process (only a few seconds); 2) no additional reflow process is needed; 3) it has a higher yield with less die stress and warpage; and 4) it has the capability to use a much finer pitch, as well as a thin platform package with either a thin core or a coreless substrate, etc. Detailed pros and cons among MR, TCB, and LAB are listed in **Table 1**. Some may raise concern for the power density of the LAB process. Typically, a 300 to 500W/cm^2 power density is used in the process, which is much lower than what is used in a plasma marking process or an evaporation process, so device-level functionality is

Creating Safe Environments

Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with: 308 nm 343 nm 355 nm

no longer a concern for the LAB process. The evolution of various chip attach technologies from MR to LAB is shown in **Figure 2**.

Items	MR	TCB	LAB
Source of Heating	Global heating in the substrate and die	Local heating only to specific die area	Local heating only to specific die area
Force	No external force applied	Very high applied force to the die from the TC bond head	No external force applied
Temperature control	By oven heating element/belt speed	By TC bonder	By IR laser power
Environment control	Environment controlled by N ₂ or O ₂	No Environment control	No Environment control
U/A accuracy	Less accuracy due to high CTE mismatch	High accuracy due to less CTE mismatch	High accuracy due to less CTE mismatch
ELK stress issue	High ELK stress due to large CTE mismatch	Low ELK stress due to small CTE mismatch	Low ELK stress due to small CTE mismatch
Warpage	High warpage due to global heating	Less warpage due to local heating	Less warpage due to local heating
UPH	High UPH	Low UPH	Medium UPH
Investment	Low	Medium	High

Table 1: Pros and cons among MR, TCB, and LAB.

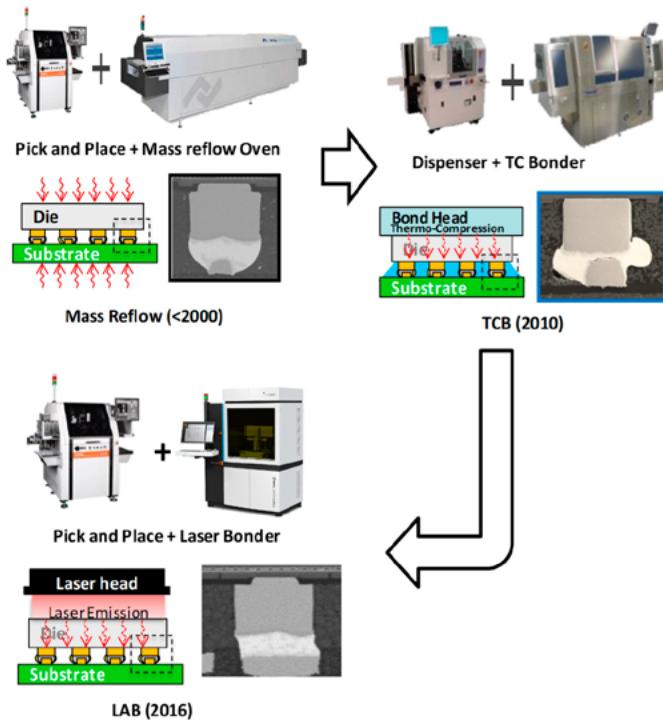


Figure 2: Evolution of various chip joining technologies from traditional mass reflow (MR) to thermal compression bonding.

Thermomechanical simulation results

As stated earlier, the thermal mismatch in LAB is lower compared to that of MR because of the substrate staging temperature in LAB. Typically, in LAB, substrates are held at 145°C and die at 250°C, respectively. The effective temperature difference between die and substrate, which causes higher warpage and stress, is significantly smaller in LAB. A few simulations were conducted to verify the results. One simulation was done on a 35X35mm package with a 20X14mm die size using Cu pillar bump at 130µm pitch. Results found an approximately 60% lower die stress with the LAB process than with MR as shown in **Figure 3**. A similar study was conducted for other test vehicles (TVs), which found a similar trend.

Tensile stress, S₁, is typically used to identify the severity of die stress in the package. An infra-red (IR) laser is used to heat up the

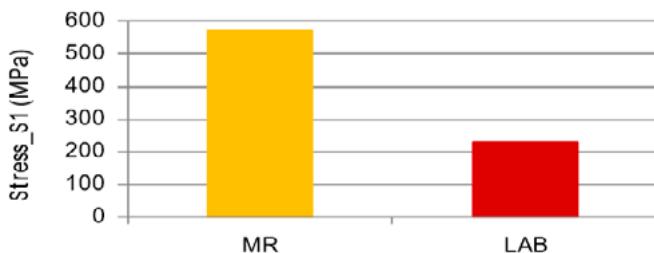


Figure 3: Die stress simulation result between MR and LAB.

die and bump during the chip joining process, which takes a little over a second to complete. During the process, the temperature reaches around 230°C. However, the time it takes to complete the solder joining process is exceptionally short (a fraction of a second). As a result, the coefficient of thermal expansion (CTE) mismatch between the die and the substrate is not substantial. Substrate laminate material has a viscoelastic nature, whereas solder itself is a viscoplastic material that is sensitive to time and temperature. Both of these kinds of materials don't get enough exposure time at high temperature to deform inelastically. A study was conducted to capture the chip joining temperature and time as shown in **Figure 4**. In the chart, the solid black line represents an already joined chip, and the yellow line is for an unjoined chip. From the chart it is clear that formation of the solder joint takes place at 230°C at a time of about 0.3s.

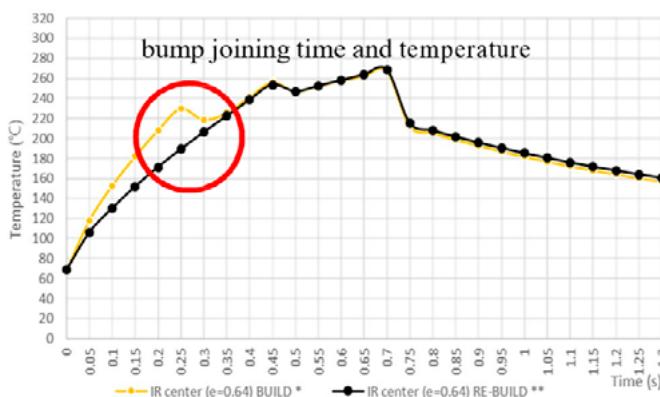


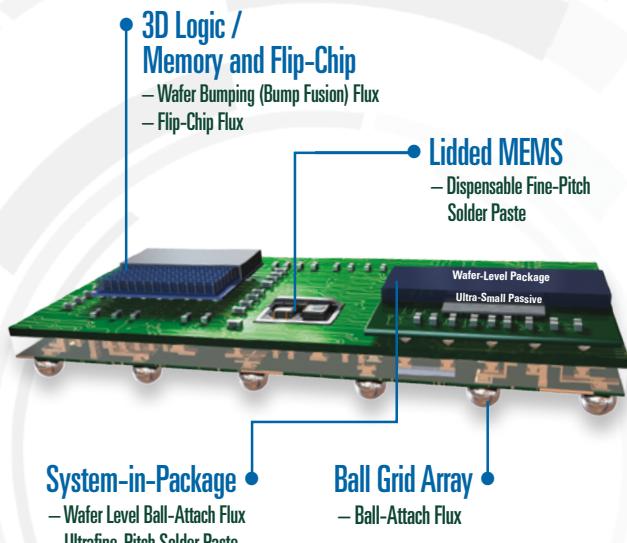
Figure 4: LAB chip attach profile using an IR laser.

In this study, time is measured before and after solder joint solidification. **Figure 5** shows that at 0.25s, the bump was not yet joined, whereas at 0.3s, solidification was completed. Chip-package interaction (CPI) performance is much better in LAB than with MR for the same reason as above. A numerical calculation has been conducted to predict and compare bump displacement after the chip attach process between the MR and LAB processes. In this analysis, a small flip-chip package with a 12X12mm body size, a 5X5mm die size, and a 4L embedded trace coreless substrate was used as a TV. A volume average technique is used to calculate the CTE of the substrate stack up.

In the MR process, the entire package (die, substrate, etc.) was subjected to a temperature of 220°C during the chip attach process, whereas for the LAB process, the substrate was held to a temperature of 145°C. In our numerical analysis, 220°C and 145°C are considered stress-free conditions for MR and LAB, respectively. Calculation

THE POWER OF EXPERIENCE

Proven Materials. Technical Expertise.



NEW

WS-446HF
*one-stop solution
for flip-chip and ball-attach*

Check out our wide portfolio of soldering materials for Heterogeneous Integration & Assembly:

www.indium.com/CSR/HI

askus@indium.com

**From One
Engineer
To Another**

©2020 Indium Corporation



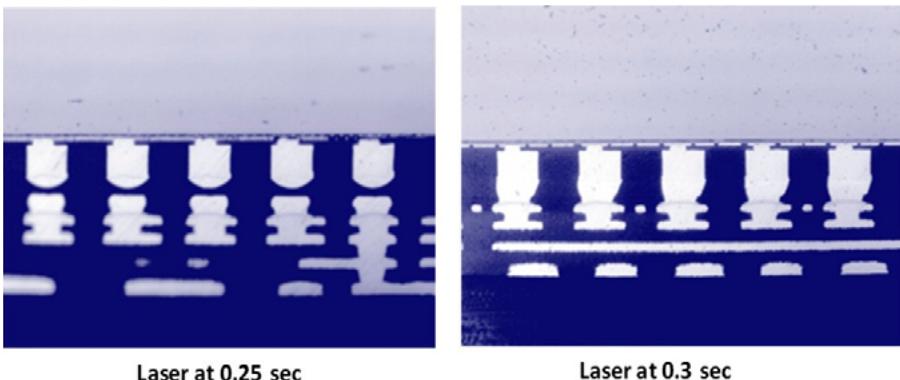


Figure 5: IR laser time before and after solder joining.

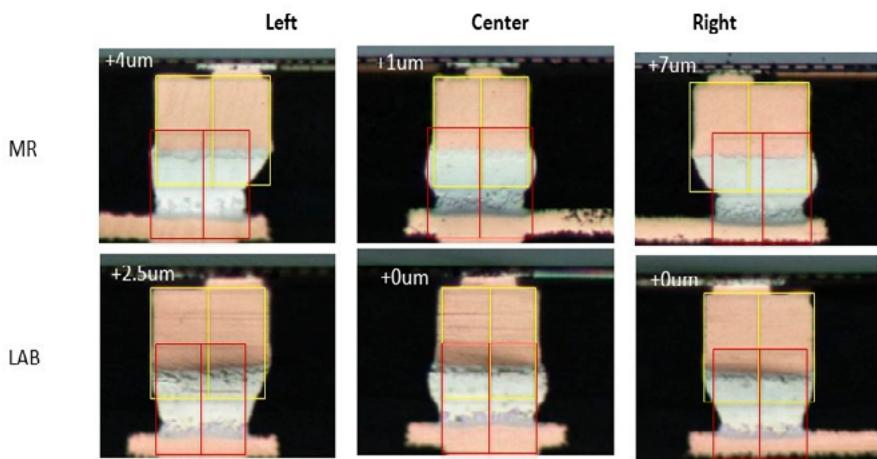


Figure 6: Bump joint displacement data between MR and LAB. Data are measured at die left, center, and right locations.

Analysis type	Process	CTE		Temperature load (°C)		Displacement from DNP
		Substrate	Die	RT	HT	
Calculation	MR	11.6ppm	3ppm	25	220	22.57um
	LAB	11.6ppm	3ppm	25	145	13.89um
Empirical	MR	11.6ppm	3ppm	25	220	14.2um
	LAB	11.6ppm	3ppm	25	145	9.9um

Table 2: Bump offset /displacement data comparison between MR and LAB processes.

predictions are listed in **Table 2**. Empirical displacement data was also collected from the actual package cross section after the chip attach process. A very small bump offset or displacement was observed in LAB over MR as shown in **Figure 6**. Absolute displacement numbers between calculations and empirical results may not match, but trend wise, good correlation has been established between calculations and empirical data as illustrated in **Table 2** and **Figures 5 and 6**.

Process characterization: design of experiments

Since early 2016, numerous studies have been conducted on actual packages to make sure that LAB data does indeed indicate a substantial benefit over standard MR and TCB processes before ramping into mass production. In terms of the assembly process, there is no difference between MR and LAB except that the MR reflow process is interchanged with LAB (**Figure 7**). Both capillary underfill (CUF) and molded underfill (MUF) can be used in the LAB process. LAB process substrates don't need to be heated to a very high temperature like what is needed for MR, therefore, it only takes a few seconds to heat up the die and perform chip joining.

In one of the early studies, two TVs (one flip-chip fine-ball grid array [fcFBGA] and one flip-chip ball grid array [fcBGA]) were selected for LAB process qualification. Fine-pitch Cu pillar bump with bond on lead (BOL) pads were introduced in the substrate design. One of the great advantages of a BOL pad is that it allows for very relaxed design

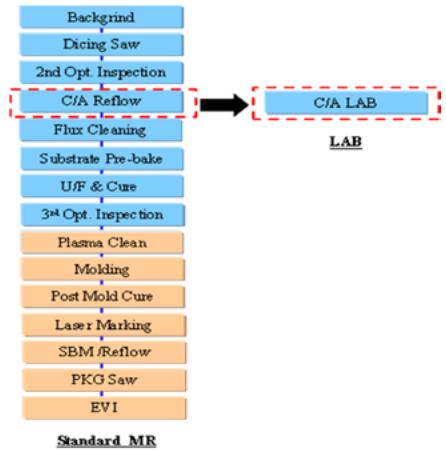
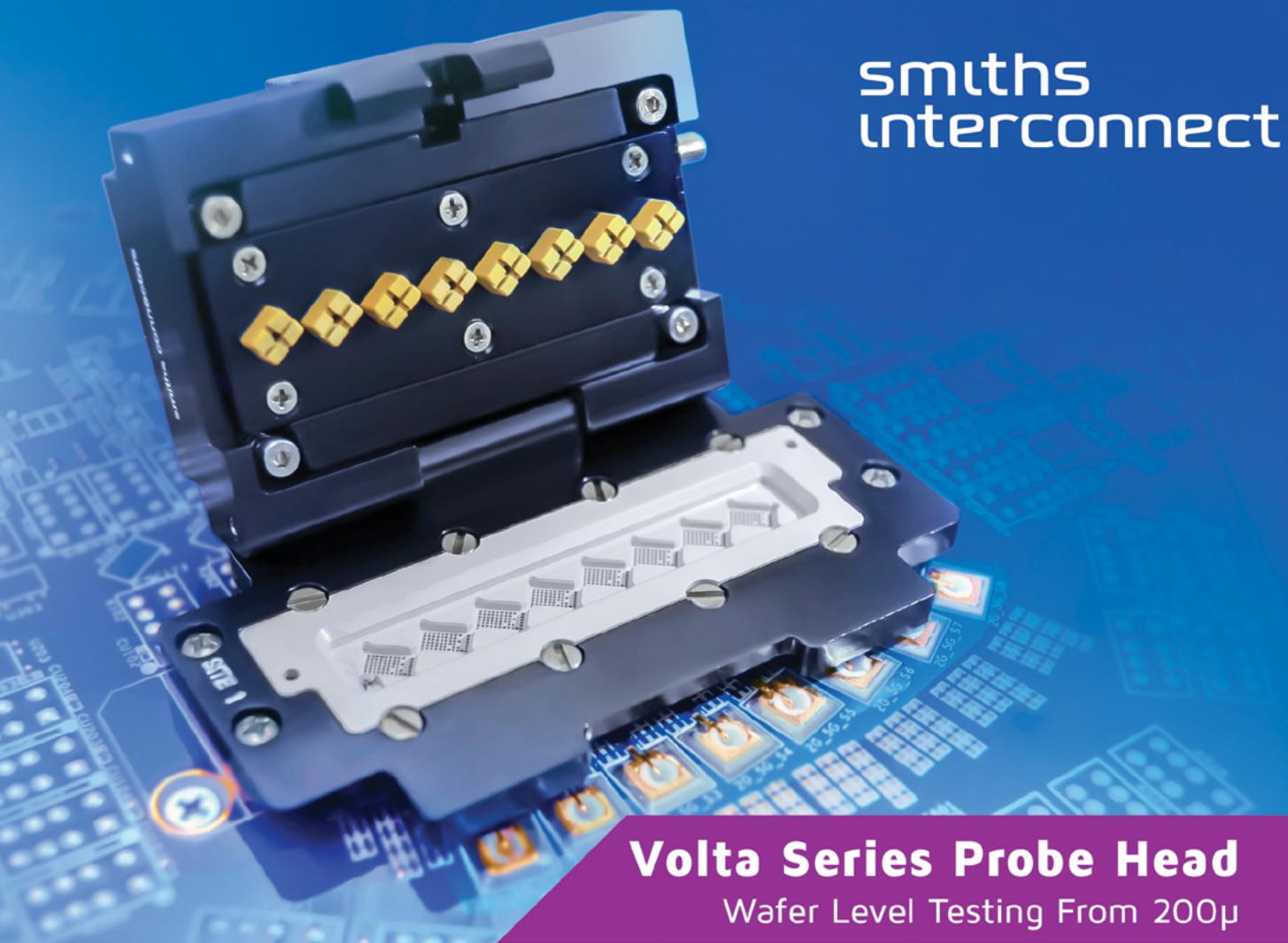


Figure 7: Typical assembly process difference between MR and LAB for a fcFBGA molded package.

Package type	Die /bump info						Substrate
	Type	Size (mm)	Si Node	Die T (um)	Die size (mm)	Bump pitch (um)	
fcFBGA	15x15	10N	200	13x12	60	30x50	ET/S/BOL
fcBGA	13x22	28N	340	10x13	180	60	ET/S/BOL

Table 3: TV package attributes for the LAB study.



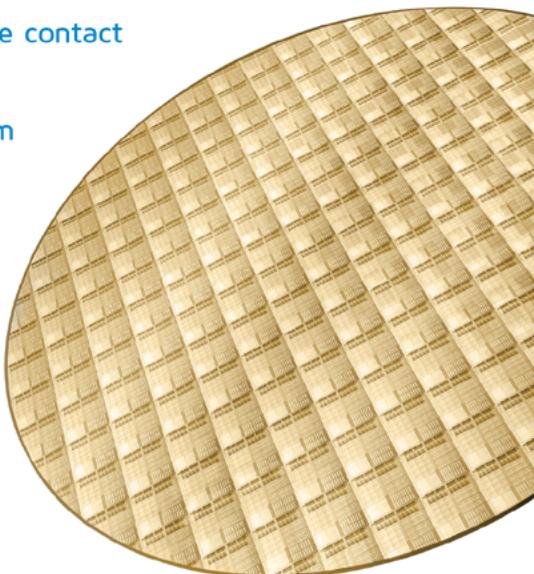
Volta Series Probe Head

Wafer Level Testing From 200 μ

Increased Throughput, Reduced Test Time

Smiths Interconnect's Volta Series Probe Head provides improved efficiency in high reliability WLP, WLCSP and KGD testing.

- Extremely short signal path ($\leq 3.80\text{mm}$) enables low and stable contact resistance, high current carrying capacity and longer life cycle
- Enhanced planarity allows increased site to site test parallelism
- Reduced test set-up time, simple maintenance and field replacement ensure lower cost of ownership
- Allows sorted die test of all sites simultaneously resulting in increased test yields in a shorter time



Package type		Die /bump info					QTC (-40 to 60C)	
Type	Size (mm)	Si Node	Die T (um)	Die size (mm)	Bump pitch (um)	UBM Size (um)	MR	LAB
fcFBGA	15x15	10N	200	13x12	60	30x50	20/20 (Fail@20X)	0/20 (Pass 60X)
fcBGA	13x22	28N	340	10x13	180	60	2/20 (Fail@10X)	0/20 (Pass 40X)

Table 4: QTC data for MR and LAB DOE.

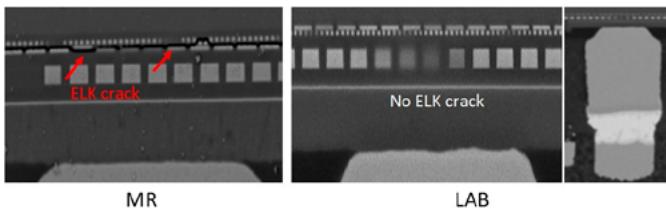


Figure 8: Die ELK crack data after QTC 20X. There is no ELK cracking with LAB up to 60X QT.

rules, which, in turn, allows for a lower substrate price. Additionally, it helps to release die stress from the die side to the tiny substrate pad side and it also improves the extreme low-K (ELK) crack margin in the die. Some generic package

cracking, and other potential die- and bump-level failures. A 30X50mm UBM size with a 60 μ m bump pitch was used in a thin fcFBGA package. For the fcBGA, it was a round bump at a much coarser pitch (180 μ m). White bump or ELK cracks

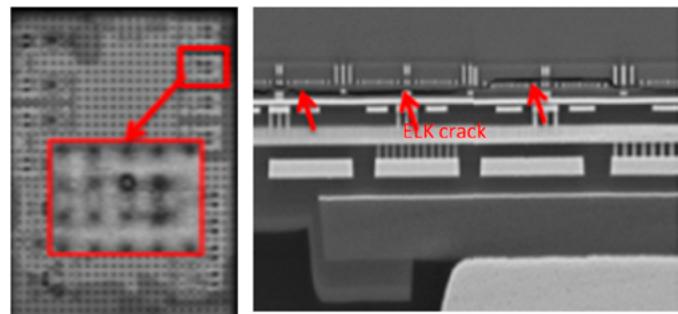


Figure 9: Cracks in the fcBGA ELK after 10X QTC with MR.

attributes for both packages are described in Table 3.

Smaller under bump metallization (UBM) is always a concern for ELK cracking, bump

were observed as early as 20X QTC (-40 to 60°C per cycle) cycles for MR legs, no crack was observed for the LAB leg up to 60 QTC cycles. Similar data was found for the fcBGA package as shown in Table 4. Extensive failure analysis, including bump and die cross sections, were conducted to identify the failure mode. Very clear cracking or rupturing were observed in the die ELK layer for the MR leg, whereas no visible cracking was found with the LAB leg as shown in Figures 8 and 9 for fcFBGA and fcBGA data, respectively.

Die thickness effects were also captured in our CPI study with LAB. Typically, a thinner die is much more compliant than a thicker die. However, thin die will increase the risk of excessive warpage in the package. Handling thin wafers or die could be another potential issue in addition to the wafer backgrinding cost. In this study, a fcBGA TV was used to conduct the die thickness effect CPI work. Package details and results are shown in Table 5.

Most fcBGA applications use a full thickness (~775 μ m) wafer because there is no strict restriction on package height. Some of the applications require thin fcBGA where die thinning is needed. In this CPI work, 340 μ m and 200 μ m thin dies were used to conduct the study. Similar to other CPI work, QTC tests were also conducted to figure out robustness of bump joints and die. Die thickness effect results are shown in Table 5. No ELK cracking or delamination was observed for 200 μ m thin die with either MR or LAB. On the other hand, ELK cracking started at the 20X read point for 340 μ m die thickness when using the MR process, and no anomaly when using LAB until 60X. Results again proved that the LAB process has a much higher margin of ELK crack resistance, and therefore, greater CPI robustness.

One of the most challenging tasks for



Chip Targets
ISO9001:2015
Certified

Independent FA Lab Since 2003

Fast and Accurate Failure Analysis By
Experienced FA Engineering Team With
In-House State of The Art Equipment

Announcement: Chip Targets completed the installation of the Nexsa XPS and the Jiaco MIP Decapsulator

In-House Capabilities	In-House Equipment
2D and 3D X-ray CT Analysis	Dage XD7500VR CT X-ray
XPS/ESCA Analysis	Therm Fisher Nexsa with Depth Profile and REELS
SAM Analysis	Sonix ECHO VS System
Cross-Section Analysis	1)Hitachi IM4000 Ion mill Cross-Section and Polish 2)FEI Strata 400S FIB/SEM/STEM
Global Isolations	1)Hamamatsu PHEMOS1000 EMMI and OBIRCH 2)Quantum Focus Thermal Hot spot, IR mapping, and TIVA
Decapsulations	1)Laser Ablation 2)Nisene Copper Protect Acid Jet Etcher 3)Tepla 100E CF4 + O2 Plasma Etcher 4)Jiaco Microwave Induced Plasma (CO2 gas)
FIB Edits	FEI V600 with CAD navigation
SEM and EDX	FEI Strata 400S SEM/STEM and Oxford EDX
Bond Pull/Shear and Die Shear	Nordson Dage Optima Bond Tester
Optical Inspections	Keyence VH7000 with Nomarski
Contactless Profilometer	Keyence VK-X260 Laser Confocal Microscopy
Wire Bonding, Repair, Ball Attach Services	K&S Wire bonders; Electrovert 10 Zone Reflow Oven
Electrical Testing and Hardware Designs	Digital Curve Tracer and Test Hardware Design and Assembly








sales@chiptargets.com (972) 470-9290
www.chiptargets.com
 1400 S Sherman Street #212 Richardson TX 75081

the MR process is to attach fine-pitch die with a small under bump metallization (UBM) bump. It experiences very high stress from the CTE mismatch between die and substrate. A typical failure mode for a small UBM bump is delamination or UBM cracking. Using LAB, we comfortably qualified a 90 μ m pitch with a UBM size as small as 25X30mm without any yield loss. Detailed package attributes along with a bump cross-section picture for 25X30 μ m UBM are shown in **Table 6**.

Extensive long-term package-level reliability with the LAB chip attach process were successfully completed for fcFBGA and fcBGA packages. This technology is currently in mass production for fine-pitch and small UBM packages. Based on the reliability data, no noticeable concern has been raised so far. After reliability tests, some of the packages were sliced to make sure no anomalies were present in the die, in the ELK layer, bump, or substrate layers. **Figure 10** shows some of the cross-section data after package-level reliability tests. LAB has been used to attach double data rate chip-scale package (DDR CSP), and other passive components with the system on chip (SoC) package without any performance degradation of the SoC die. Recently, dynamic random access memory (DRAM) packages were attached with baseband or application processor die in a package on package (PoP) structure. With the help of LAB, package pre-stacking can be done very smoothly at much higher yields. Pre-stacking packages with LAB are already qualified for mass production. Extensive package characterization data found that solder joint integrity looks much better than with traditional MR. **Figure 11** shows some cross-section pictures of a PoP where LAB was used for top and bottom package attachment. This process has been widely used for mobile and consumer package attachment.

Summary

With the phenomenal expansion of various fine-pitch interconnection technology offerings and manufacturing footprints, assembly suppliers are positioning themselves to support the strategic need for very cost-effective, high-performance packages for a number of fine-pitch applications. With the evolution of new flip-chip attach technologies, it is expected that significant cost can be

associated with the new technology to overcome assembly-related yields. Standard MR, TCB, and the latest LAB attach technologies were described in this paper. TCB used to be one of the key technologies for fine-pitch interconnection attachment. However, because of very low throughput and excessive bonding pressure that sometimes raise a concern for bump joint shape, it is no longer an attractive solution for the industry. There are certain niche applications where TCB is still popular, however. LAB came to the fore in a big way to capture TCB marketshare. LAB has overcome most of the issues that the industry had with TCB. It improves throughput 2 to 3X higher

Package	Package size	17X17mm
Die	Si node	28N
	Die Size/Thickness	6X5.5X4mm/ 200 and 340 μ m
	Bump pitch/UBM size	180 μ m/60 μ m
	Bump H (Cu/Ni/SnAg)	75 μ m(42/3/30 μ m)
Substrate	Stackup	6-2-6L, 1.2mm
	Bump pad finish	CuOSP

Process	Die thickness	QTC (-40 to 60C)				
		T0	10X	20X	40X	60X
MR	200 μ m	0/20	0/20	0/20	0/20	0/20
		0/20	0/20	0/20	0/20	0/20
LAB	340 μ m	0/20	2/20	1/18	-	-
		0/20	0/20	0/20	0/20	0/20

Table 5: CPI effect for die thickness with MR and LAB.

Package detail					Substrate thickness	Yield
Body size	Die size	Bump pitch	UBM size	Bump height		
15X15mm	12X11 mm	90 μ m	25X30 μ m	25/3/15 μ m	2L, 150 μ m	100%

Table 6: Package attributes for 25X30 μ m UBM.

QUALITY IS EVERYTHING

Your yield. Your profitability. Your reputation depends on 100% quality assurance for every wafer, device and package.

Sonix is the leader in ultrasonic technology and expertise for inspecting wafer bonds, device interconnects and package integrity.

Find smaller defects faster, at any layer. Learn more and request a free sample analysis at Sonix.com.

sonix™

© 2016 Sonix, Inc. All rights reserved.



Figure 10: A SEM cross section of the packages after long-term reliability tests.

than TCB, but is still lower than standard MR. It fixes most of the problems that we have in MR and TCB. Cost wise, LAB is comparable with MR for most designs. As the pitch size shrinks with the Si node, LAB is expected to be the “must have” technology for the 5nm and 3nm devices of the future.

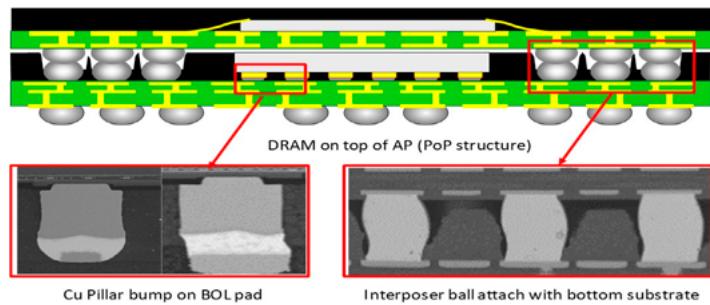


Figure 11: LAB used to attach DRAM with AP. Cross-section data shows very good solder joints.

Acknowledgments

The authors would like to thank the R&D team of JCET group, Korea, and our customers for their continued guidance in the study. The authors also want to express gratitude to the individuals at our partner companies that helped design the advanced packages and process.

References

E-tec Interconnect is pleased to present its new Clamshell Open Top Socket

- **High reliability** up to 500k insertion cycles
- **High frequency** up to 27 GHz in pogo pin (up to 40GHz validated, with Elastomeric contact technology)
- Thru-hole technology, SMT, Solderless Type
Also pluggable into adapter MiniGridSocket series (see E-tec catalog TS01)
- All kinds of packages, even your latest special custom packages



E-Tec Interconnect AG, Mr. Pablo Rodriguez, Lengnau Switzerland
Phone : +41 32 654 15 50, E-mail: p.rodriguez@e-tec.com

EP Patents 0897655, 1385011, 0829188, US Patents 6249440, 6190181, 6390826 and Patents in other countries



Biographies

Nokibul Islam is currently serving as Director of Field Applications Engineering at JCET Group, with the main focus in product business development and marketing for the company. Before joining JCET, he was part of Amkor Technology’s Research and Development team. He has over 17 years of experience in the semiconductor industry and received his PhD in Mechanical Engineering from Auburn U., AL. Email nokibul.islam@jcetglobal.com

KyungOe Kim is a Director in R&D at JCET Group Korea.

1000

SEMI STANDARDS & COUNTING



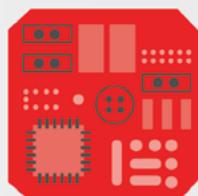
From wafers to packaging to everything in between...

The microelectronics industry counts on SEMI standards to drive innovation in every aspect of product design and manufacturing.

Explore the wide variety of SEMI standards and get involved in setting standards for your segment with our open, consensus-based process.

Learn more and get involved at:

semi.org/standards



INDUSTRY NEWS



2020 ECTC to focus on the latest technologies, emerging applications

By Rozalia Beica, AT&S, 70th ECTC Program Chair

As we monitor the COVID-19 outbreak, normal preparations are underway for the 70th ECTC to be held May 26-29 at the Walt Disney World Swan and Dolphin Resort in Lake Buena Vista, Florida. Visit ectc.net for latest status.

On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE's 70th Electronic Components and Technology Conference (ECTC). We are very excited about the 2020 program and we are welcoming our colleagues from all over the world to join us. The 70th edition of ECTC, sponsored by IEEE/EPS, will take place at Walt Disney World Swan and Dolphin Resort in Lake Buena Vista, Florida, USA from May 26-29, 2020.

Considered the premier electronic packaging conference of the industry, with over 1500 attendees, ECTC is continuing its tradition in bringing the latest IC packaging, components and microelectronic system technologies. This international

annual conference brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses and foundries, outsourced semiconductor assembly and test (OSAT) service providers, substrate makers, equipment manufacturers, material suppliers, research institutions, and universities—all under one roof.

Over 200 volunteers and industry experts, from across the supply chain, have put together an exceptional program consisting of 380 technical papers in 36 technical sessions and 5 Interactive Presentation sessions, 18 Professional Development Courses and several panels, special sessions, receptions and networking opportunities. The conference will address various

important topics and industry trends, from mobile, wearables and automotive applications, flexible and printed electronics, to high-speed communications, wireless, photonics, high-performance and quantum computing, and artificial intelligence (AI) hardware. The oral presentations and panel discussions will feature a wide range of packaging technologies, from wire bonding, wafer- and panel-level packaging, flip chip, 2.5D and 3D integration, to advanced substrates and interposers, embedded technologies, system in package and heterogeneous integration. New ideas, designs, characterizations, simulations and

reliability studies will bring new perspectives and challenges from materials and processing perspectives, integration, interconnections, assembly and manufacturing. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 70th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry.

This year we have increased the number of special sessions and panel discussions. The conference will feature seven special sessions with invited industry experts that will cover emerging technologies and applications. On Tuesday, May 26 at 9:30 a.m., Pavel Roy Paladhi and Nicholas Bronn will chair a special session covering "Bridge to Quantum Computing." On the same day at 7:30 p.m., the ECTC Panel Session will be chaired by IEEE EPS President Christopher Bailey and Board of Governors Member Karlheinz Bock. This will be a session where selected young researchers will have the opportunity to share their visions of future packaging technologies and participate in discussions with experts in the field.

Our prestigious luncheon keynote presentation on Wednesday, May 27, will feature Douglas Yu from Taiwan Semiconductor Manufacturing Company. Dr. Yu will focus on innovative heterogeneous integration technologies starting a new semiconductor era.

We are continuing our tradition and bringing back the networking events focused on young professionals and diversity. Adeel Bajwa will chair on Tuesday, May 26, from 6:30p.m. the Young Professional Panel. This is a great networking opportunity for young engineers, researchers, and students, to meet senior EPS members and professionals, learn more about industry activities, receive career guidance, and engage through a series of activities.

The Diversity special session – started a few years ago as a women-focused panel – has now evolved into a Diversity and Career focused Panel and Reception, jointly organized by ECTC and iTerm. The panel, chaired by Kitty Pearsall and Cristina Amon, will have a focus on some of the specifics

PLASMA ETCH
PROGRESS THROUGH INNOVATION

PLASMA IMPROVES BONDING!

Our fully automated plasma cleaners offer:

- Improved Markability
- Enhanced Adhesion
- Better Bonds
- Easier Assembly
- Surface Modification

100% removal of organic contaminants with a low environmental impact!

STARTING AT ONLY
\$ 5,900 USD

TO LEARN MORE, VISIT www.PLASMAETCH.COM
OR CALL 775-883-1336

of inclusion in a diverse workforce and will take place on Wednesday, May 27 at 6:30 p.m. After this panel, starting at 7:30 p.m., Michael Mayer will chair the ECTC Plenary Session entitled, “3DIC: Past, Present and Future.” In this plenary session, experts will address the evolution and challenges of 3D integration, new applications, and opportunities driving further adoption of 3DIC technology across the value chain.

Following the industry trends and a growing interest in photonics, we are increasing our activities in this area. This year we are bringing two Special Sessions focused on photonics, in addition to the presentations offered in the technical sessions. On Tuesday, May 26 at 2 p.m., Rena Huang and Harry Kellzi will chair the 1st Special Session entitled, “Cutting-Edge Technology on Integrated Photonics and Packaging.” On Thursday, May 28 at 9 a.m., Xiaoming Yu will chair the 2nd Special Session on Photonics entitled, “Research, Manufacturing and Applications of Advanced Photonics Technologies within Florida Photonics Cluster.” The program will offer several opportunities for the photonics community to learn about the recent developments and progress related to the design, research, manufacturing, and applications of photonics technologies.

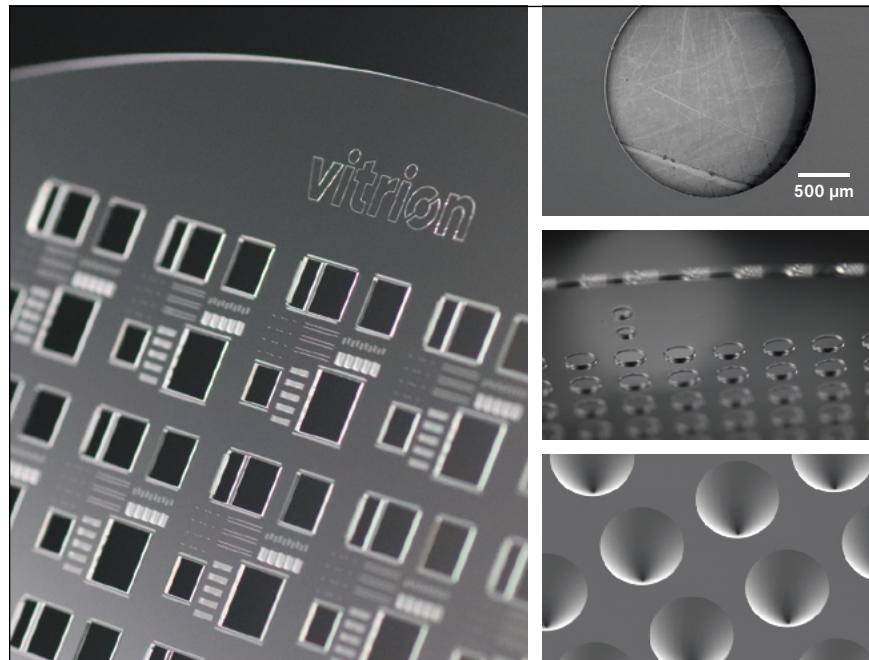
On Thursday, May 28, at 8 p.m. our colleagues from Japan, Yasumitsu Orii and Shigenori Aoki, will be chairing the IEEE EPS Seminar entitled, “Future Semiconductor Packages for Artificial Intelligence Hardware.” The seminar will focus on brain-inspired devices and integration technologies.

In addition to the technical and special sessions and panels, the 70th ECTC event will also offer several professional development courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE iTherm Conference, the 70th ECTC will offer eighteen PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 26 and are taught by distinguished experts in their respective fields. The Technology Corner exhibits will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or a business and marketing

professional or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. As the Program Chair of this premier event, I invite you to make your plans now to join us and to be a part of all the exciting technical and professional opportunities offered at this event. I would

also like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 70th ECTC a success. I look forward to meeting all of you in Lake Buena Vista, Florida, on May 26–29, 2020.



Precision Glass Processing Service

Vitrian's Laser-Induced-Deep Etching (LIDE) technology enables the economical production of deep microfeatures in technical glasses. With our production service we address customers with any production quantities. We are happy to support you with your R&D projects.

Unlock the Full Potential of Glass:

- Through Glass Via (TGV) Wafer
- Embedding Wafer
- Spacer Wafer
- Capping Wafer

Find out more:

www.vitrian.com/semiconductor

LIDE Samples

R&D and Qualification

Volume Production



vitrian



October 13-15, 2020
San Jose, California, USA

Submit your abstract today!

Save the Dates

Technical Papers Due: August 28
Conference Begins in San Jose: October 13
Professional Development Courses: October 15

www.iwlpc.com

September 16, 2020
Milpitas, CA

Known Good Die W O R K S H O P

2020

- Metrology & Inspection
- Test & Handling
- Big Data & Analytics
- Business Model
- EDA & CAD Tools

MEPTEC

ADVERTISER INDEX

Amkor Technology	www.amkor.com	1
Atotech	www.atotech.com	13
Besi	www.besi.com	19
Brewer Science	www.brewerscience.com	46
Chip Targets	www.chiptargets.com	50
DL Technology	www.dltechnology.com	22
E-tec Interconnect	www.e-tec.com	52
EV Group	www.evgroup.com	2
Indium Corporation	www.indium.com/CSR/HI	47
Ironwood Electronics	www.ironwoodelectronics.com	44
IWLPC	www.iwlpc.com	56
JCET	www.jcetglobal.com	39
Johnstech	www.johnstech.com	IBC
LB Semicon	www.lbsemicon.com	4
Leeno Industrial	www.leeno.com	IFC
Meptec	www.kgdworkshop.org	56
Micro Control	www.microcontrol.com	37
MRSI	www.mrsisystems.com	33
Onto Innovation	www.ontoinnovation.com	OBC
PacTech	www.pactech.com	31
Plasma Etch	www.plasmaetch.com	54
SEMI	www.semi.org/standards	53
Smiths Interconnect	www.smithsinterconnect.com	49
Sonix	www.sonix.com	51
SÜSS MicroTec	www.suss.com	7
Test Tooling Solutions Group	www.tts-grp.com	40
Vitron	www.vitron.com/semiconductor	55
Winway Technology	www.winwayglobal.com	25
Xperi Invensas	www.invensas.com	27
Yield Engineering Systems	www.yieldengineering.com/csr	11

May June 2020

Space Close May 15th
Materials Close May 20th

For Advertising Inquiries
ads@chipscalereview.com

Johnstech®

Providing our customers accuracy, reliability and a solid partner to deliver today's and tomorrow's test solutions.



FOR MORE INFO, VISIT JOHNSTECH.COM

© 2020 Johnstech International

ISO 9001:2015
CERTIFIED



innovation.[™]
onto

Are you onto innovation? We are.

Built upon the rich legacies of Nanometrics and Rudolph Technologies, Onto Innovation stands alone in process control with our unique perspective across the entire semiconductor value chain from bare silicon to leading edge fabs to advanced packaging. We are on a relentless quest to deliver the best comprehensive manufacturing process solutions to the world's most advanced manufacturers through collaboration and innovation.

**Onto higher yield
Onto higher productivity
Onto Innovation**

ontoinnovation.com