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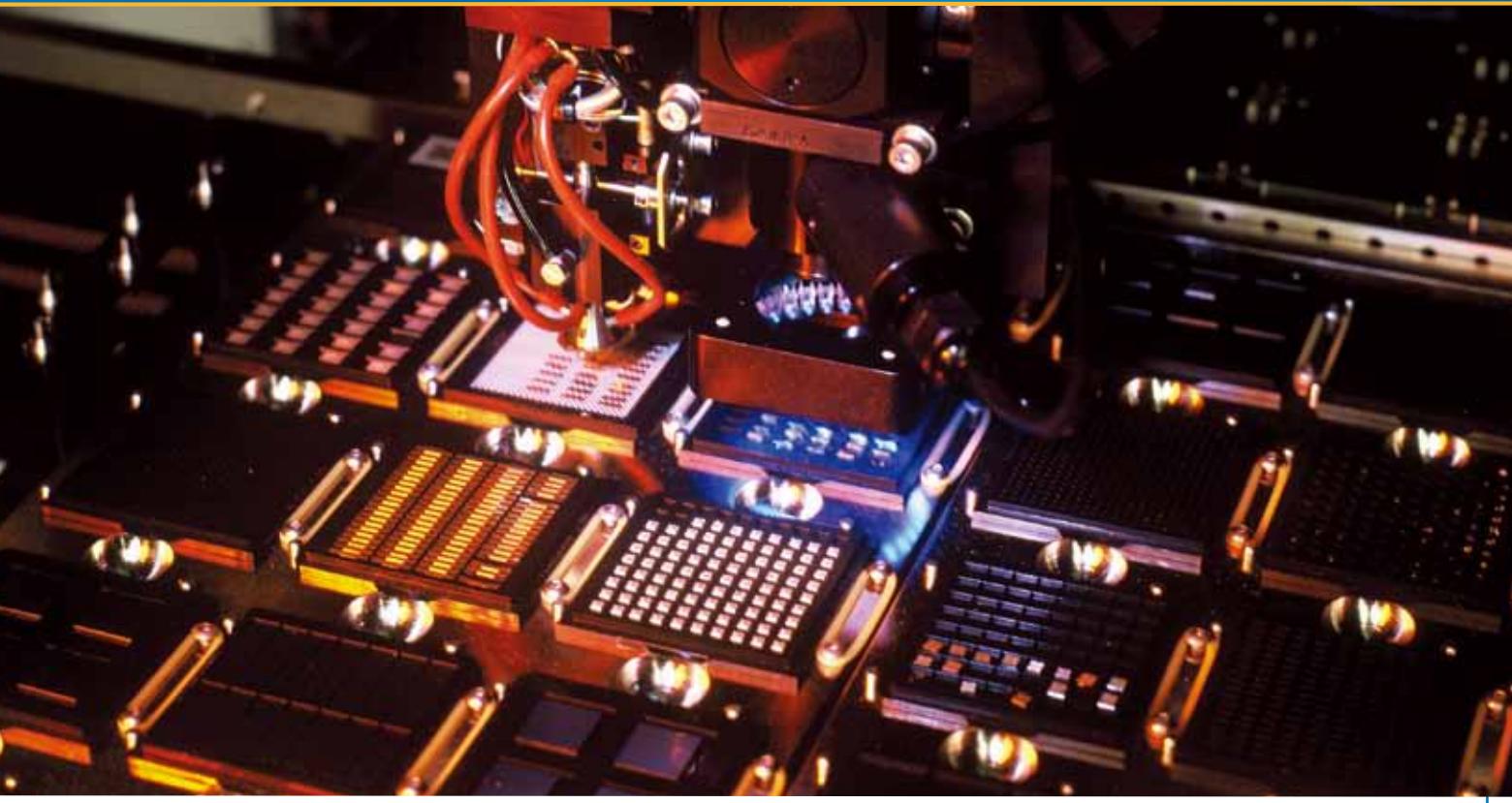
The International Magazine for the Semiconductor Packaging Industry

Volume 16, Number 2

March-April 2012

- 2012 OSATS/ IC Packaging Foundries Update
- International Directory of IC Packaging Foundries
- Heterogeneous Integration
- Plasma in WLP
- MEMS - Standards in a Maturing Industry
- Thin Wafer Processing of 3D ICs





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Welcome to the annual OSATS edition. Once again, OSATS are the forefront topic of this issue and so the front cover artwork provided by Adrian Grosu depicts a global perspective into the world of the OSATS. The Market Trends feature ahead in this issue interviews the executives at the top 5 firms representing 50% of OSATS market share and the outlook ahead for them and the other OSATS.

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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

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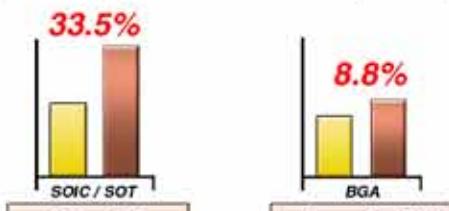
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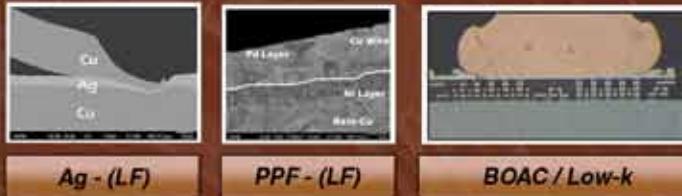
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Current Process

Process Solutions for Various Packages

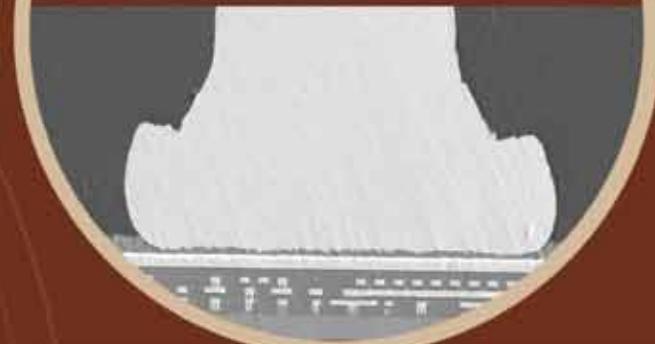


Process Solutions for Various 1st and 2nd Bond Surfaces



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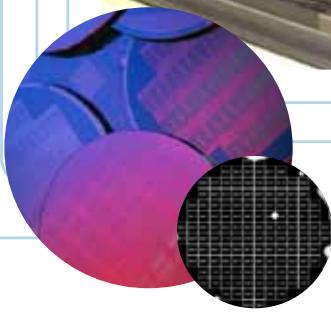
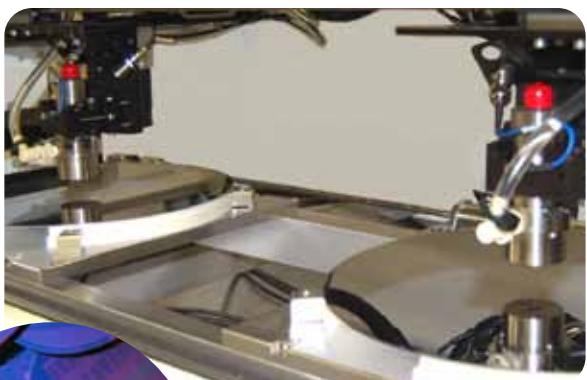
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FROM THE PUBLISHER



SMTA Pan Pacific, Technology Roadmaps and Recent Advances

I was fortunate to attend the SMTA Pan Pacific Microelectronics Symposium on Kauai during February 14-16, and in addition to catching up with many industry colleagues from around the world in a casual and relaxed atmosphere, I learned about some recent advances, as well as what's going on with microelectronics technology roadmaps from some of the world's leading researchers, academics, executives and industry veterans.

The program of 40 papers was organized into nine technical sessions, a special Technology Roadmap plenary session of 6 papers, and two invited keynote speeches. Dr. Kyung W. Paik of the Korea Advanced Institute of Science and Technology (KAIST) received the Best Presentation Award for his paper titled "Recent Advances in Anisotropic Conductive Adhesives (ACAs) Technology", which described how nanofiber can be coupled with conductive ACA particles to improve performance.

During the Technology Roadmap plenary session, representatives of the IPC International Technology Roadmap for Electronic Interconnections, the JISSO Electronics Technology Roadmap, and the 2011 iNEMI Technology Roadmaps presented reports, and additional speakers covered the future of through silicon vias (TSVs) and the risks and importance of roadmaps with respect to product competitiveness. Overall, the session was well received and plans are to include the topic again next year.

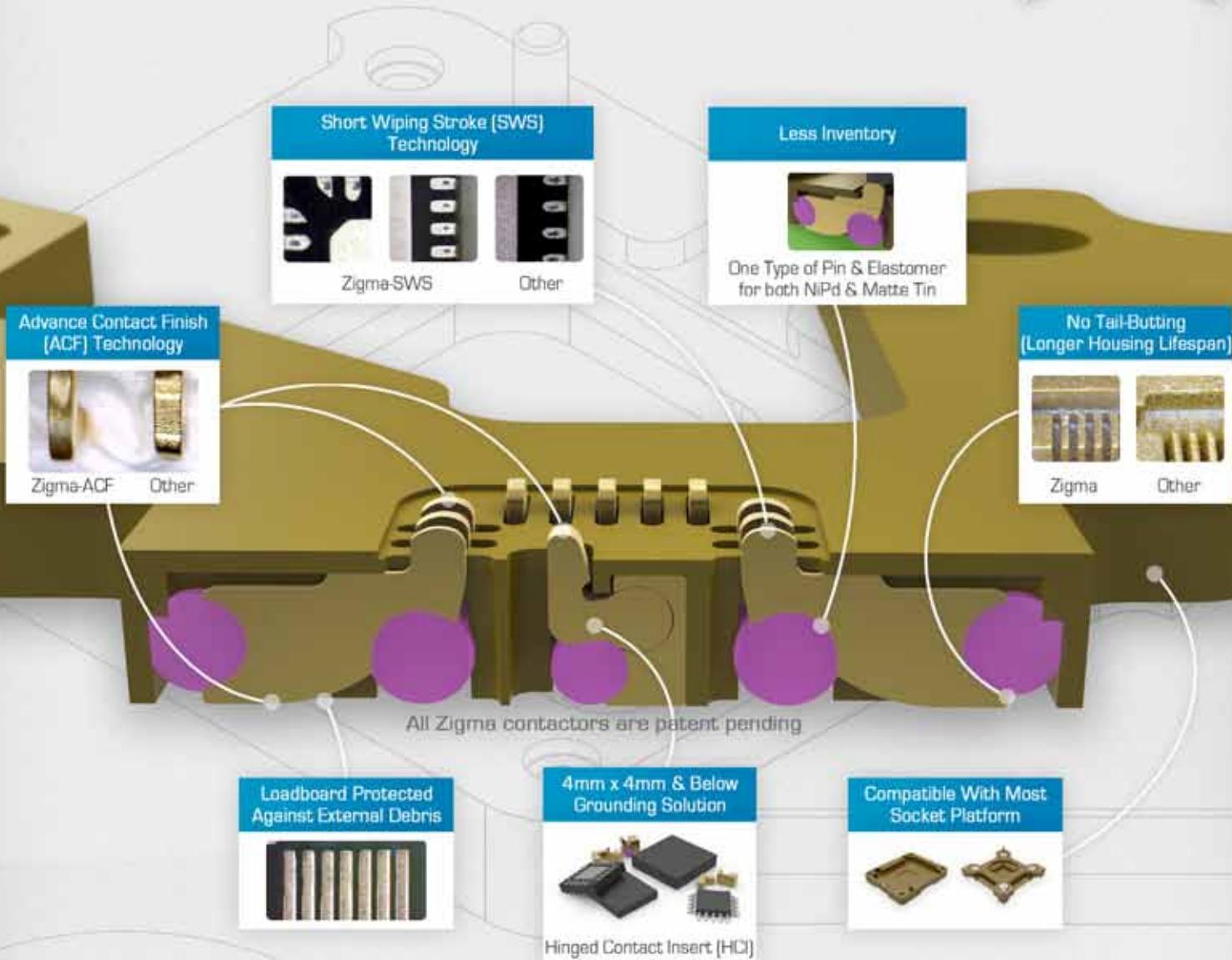
Keynote speaker, Chris Bailey from University of Greenwich spoke about "EU Electronics Research and Development Direction; Highlights of Framework 7 and Expectations for Framework 8." Tetsuro Nishimura, President of Nihon Superior Co., Ltd. talked about "Pushing the Limits of Lead-Free Soldering." Next years event will be held on Maui Jan 22-24, 2013. Be sure to mark your calendars for this event in early 2013!

While I was in Hawaii, our senior technical editor, Francoise von Trapp, was visiting Fraunhofer IZM-ASSID in Dresden, Germany, where she learned all about the 3D program there from program director, M. Juergen Wolf. The work being done there involves heterogeneous integration of multi-functional electronic devices into one wafer-level system-in-package (SiP). You can read more about in the article found on page 21 of this issue titled, Innovation Driver of the Next Decade: Heterogeneous Integration, contributed by Fraunhofer IZM's Harald Pötter and team. Francoise also visited EV Group's world headquarters in Schärding, Austria, to tour their recently expanded facility. She also learned more about the ZoneBond process for temporary bond and debond, which is featured in the article, The Material Breakthrough Towards Standardized Thin Wafer Processing by Thorsten Matthias and his team at EV Group found on page 17 of this issue. These are just a few of the top quality technical features our readers have come to expect from the pages of Chip Scale Review. We hope you enjoy them all.

Kim Newman
Publisher

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GUEST EDITORIAL



Standards for a Maturing MEMS Industry

By Tom Di Stefano [[Centipede Systems](#)]

Any technology requires standards to grow into an industry in which many suppliers, products, services and customers work together seamlessly. As MEMS products progress from university prototypes to mainstream products, standard protocols must evolve for reliability and testing. The diverse technologies encompassed by MEMS products present a challenge for consolidation of standards. Yet there are areas shared by all, from specialized instruments to high-volume consumer products. Reliability testing and back-end handling protocols are commonly shared problems where standardization will improve productivity for the benefit of all.

Many MEMS technologies evolved from university laboratories, retaining many academic aspects along the way. With double-digit growth to more than \$10B this year, somewhat more attention must be paid to manufacturing protocols. According to Benedetto Vigna, VP of STMicroelectronics, “Testing, assembly, and reliability are the most important items for MEMS industrialization and account for the biggest part of their development time, but most researchers do not consider them an interesting research activity. Usually researchers prefer to focus their attention on design since they believe they can better express their creativity. Honestly, I believe that the three topics I’m referring to represent an excellent area where innovation has to take place for the success of MEMS.”¹

Ramping up high-volume production of a MEMS device often presents formidable challenges in the assembly and test areas because of the diversity of methods peculiar to the technology. Product test is an important competitive factor for high value MEMS devices, accounting for 20

- 50% of manufacturing cost. While the processes and devices of each may be quite unique, all have in common the need for a handling protocol and reliability testing at set temperatures. This complex scenario presents an opportunity to standardize elements of back-end assembly and test, while leaving the truly unique features of each MEMS type to custom solutions. The key is recognition of those elements that are susceptible to standardization across a broad range of MEMS applications. Shared solutions enable efficiencies in equipment and processes needed for high-volume production.

Areas of MEMS production ripe for standardization include a universal handling protocol and a thermal management system. We can take our cue from the wafer fab, where standardization on front opening universal pods (FOUP) as a wafer carrier enables “lights out” automation throughout the process. With the FOUP, each equipment supplier knows the format and protocol for handling wafers presented to this process. Of course, setting a universal handling protocol for MEMS is difficult because of a broad range of device types, sizes and test protocols. Nevertheless, the potential gains in efficiency, flexibility and throughput derived from a standard handling and transport protocol are compelling.

A test-in-tray format can be adapted to all MEMS device types from flip-chip to DIP to allow handling on reconfigurable, flexible modules of automation. Trays customized for a specific MEMS device are held in universal carriers² adapted to fit standard automated handling equipment. An automated line transports trays held on these carriers throughout, independent of the device type held in the trays. The somewhat onerous job of building an automated handling and transport system

for a new MEMS device is replaced by the simple task of configuring standard modules, leaving the custom engineering for the truly unique challenges of processing and testing the device.

In the typical test-in-tray configuration shown in **Figure 1**, a tray holds 32 BGA devices in a 4 x 8 array. An ESD plastic tray is supported by balanced flat springs on the standard carrier formed from a single sheet of spring steel. The carriers are transported and handled using similar automation equipment as a packaging leadframe. One standard size for the

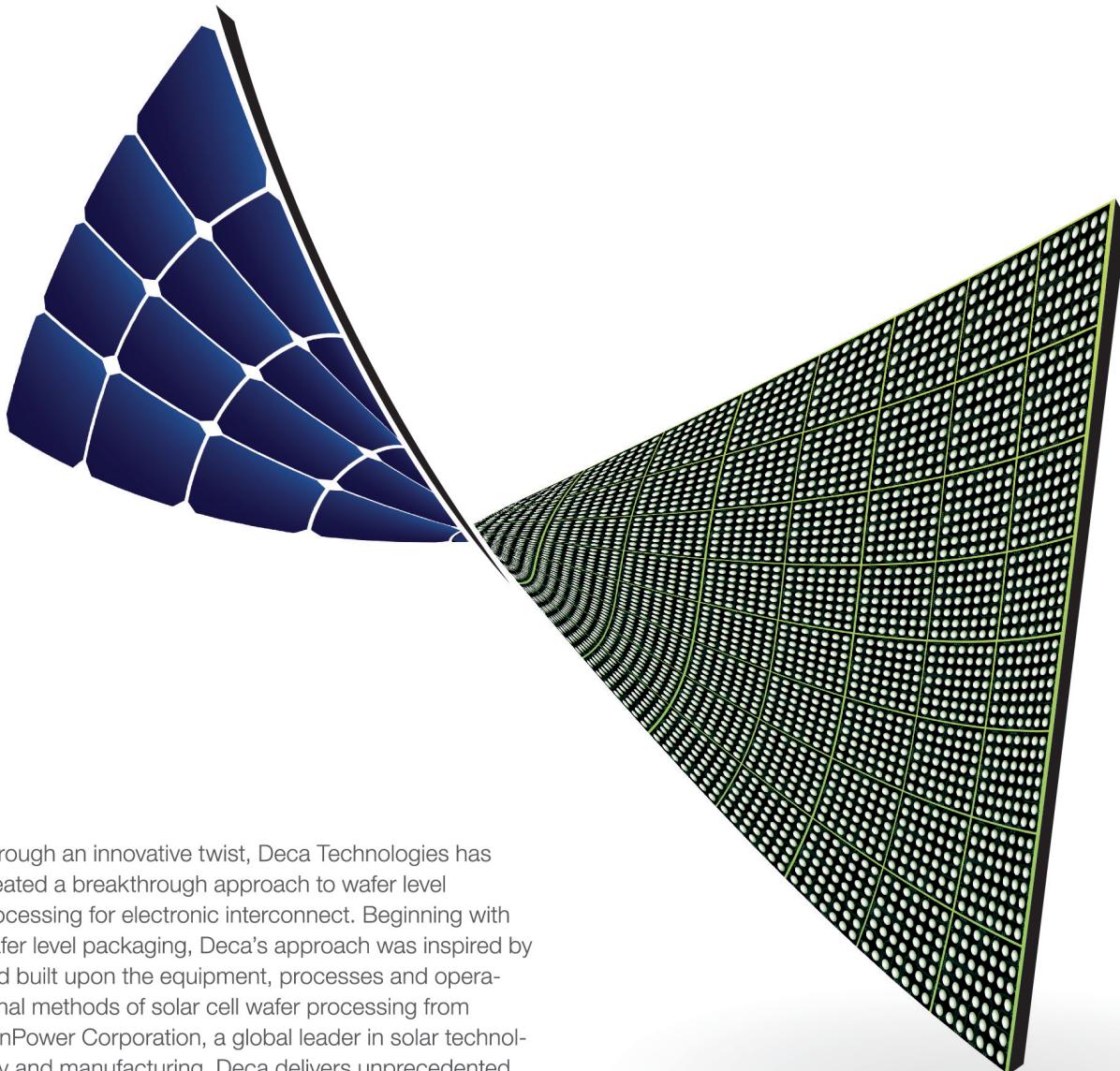


Figure 1: A tray of 32 BGA devices in a FlexFrame carrier

carrier has a 100mm x 200mm outline that supports parallel testing of MEMS for volume production. The carrier outline includes alignment notches and features to facilitate fast indexing and alignment. These carriers, held in magazines like one in **Figure 2**, are fed into and out of equipment by automatic feeders. MEMS devices remain in the tray throughout back-end processing and testing operations and are touched by hands, human or robotic, until finished.

Trays can be made to hold virtually any type of MEMS device imaginable to test pressure sensors, gas sensors, gyros, accelerometers, magnetometers, oscillators, microphones, cameras, switches, displays and innumerable others. Devices may be packaged in DIP, QFP, QFN, TSOP, BGA, CSP, WLP, flip-chip, or bare dice. All can use the same basic

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Figure 2: A magazine of 20 trays, showing a tray for QFN gyro devices

modules of automation. A line can be reconfigured from one type to another because the automatic handling portion remains the same.

Transport and alignment of trays is done mechanically. Notches and alignment features on the carrier facilitate mechanical alignment. After preliminary alignment, a tray of devices is pressed down (or up) into a mating contactor. The balanced flat springs guide the tray vertically to

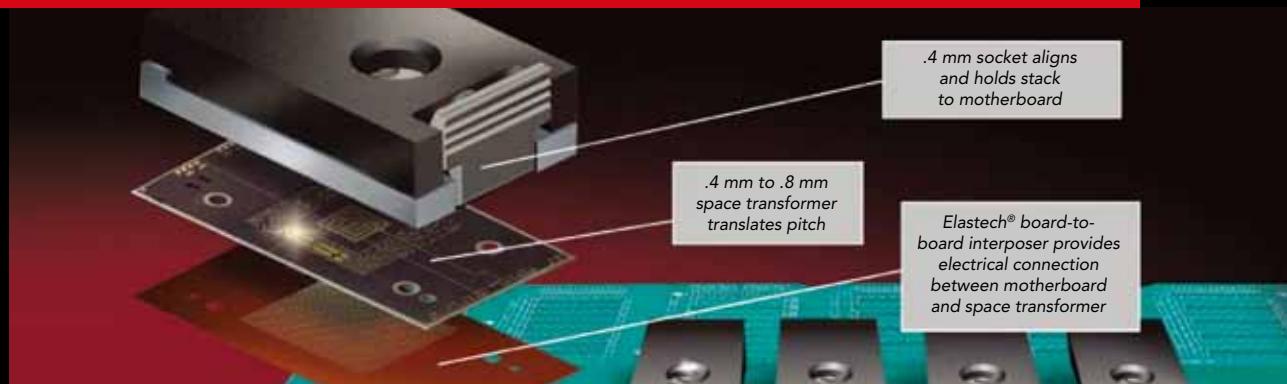
allow precise mating of each device with its contactor. After test, the pressure is released, allowing the tray to spring back into position and ready for indexing to the next position. The carrier and tray assembly withstand thermal shock and peak temperatures³ to 260°C so that the tray is useable through most processes.

Thermal management during MEMS test is also a candidate for a standardized treatment. The various regimes for thermal stress during MEMS testing are quite diverse, with no widely accepted standards. Many classes of MEMS devices are targeted for automotive applications, where thermal stress testing is rigorous. Here, tri-temperature testing is commonly done at temperatures of -40°C, +25°C and +150°C. In the future, test temperatures are projected to go from -55°C to +160°C or higher. The same device, when used in a medical application, is tested at different temperatures, sometimes in a temperature ramp. For certain applications, tests are made while device temperature is ramped

up and down. For others, testing is done on a staircase of temperatures. At the other end of the spectrum, high-volume consumer products are simply tested at room temperature, and sometimes at hot conditions. All this can change as entertainment products find automotive applications, where more rigorous reliability requirements apply. In this blizzard of drifting test requirements, there is one certainty: a need for a flexible system for thermal management during test.

An example of a thermal management system for test-in-tray applications is illustrated in **Figure 3**. Trays containing 32 MEMS pressure sensors are indexed into a mini-chamber, where temperature is controlled between -55°C and +150°C. The computer controlled temperature is sequenced through a series of set-points and ramps, where precise measurements are taken. Programmability of the system allows any arbitrary set of thermal stress profiles for qualification as well

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Figure 3: Automated MEMS pressure sensor test system, courtesy Centipede Systems

as production. This flexible thermal management system will support MEMS test for any application, with a minimum of custom engineered solutions. The same system can be used to test consumer products as well as high reliability MEMS devices for automotive uses.

At the heart of the thermal management system lies a mini-chamber shown in the open position in **Figure 4**. In operation, a tray of devices is indexed into position between the top of the mini-chamber and the contactor assembly below. The top is then lowered onto contact with the tray,

pressing the tray down to the contactor. Sealing surfaces around the mini-chamber and the contactor seal respectively to the top and bottom surfaces of the tray on a band circumscribing the array of devices. When mated, the assembly of the top of the mini-chamber, the tray, and the contactor form a sealed environment surrounding the devices. Dry nitrogen or other gas is introduced into the mini-chamber during test. For precise thermal control, helium may be used to increase thermal coupling. Control of temperature, gas and pressure



Figure 4: view of open mini-chamber in MEMS pressure sensor test system

within the test environment supports a broad range of MEMS test applications with a standardized set of thermal management capabilities.

As the MEMS industry matures, it will of necessity settle into standardized protocols for handling and testing devices of all types. A test-in-tray approach greatly facilitates standardized automation. Further, a new test system *ab initio*, perhaps it is time for the industry to grow up and drive toward standards in this critical area.

References

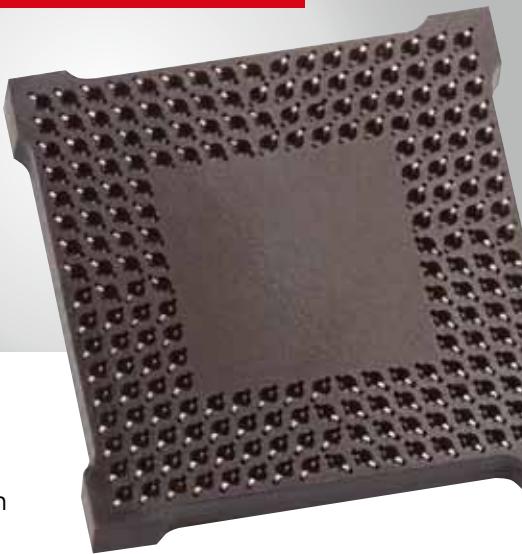
1. Benedetto Vigna, interview published in MST News 2005.
2. FlexFrame is a trademark of Centipede Systems, Inc.
3. Ceramic filled ESD Controlled PEEK polymer

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Silicon Interconnect for the Masses

By Chris Scanlan, [Deca Technologies]

In 1909, Henry Ford declared “I will put a car in the hands of every American.” It was Ford’s vision to democratize the automobile, which he succeeded in doing with the Model T. Up until then, the automobile industry was a niche market at best, serving only those who could afford such a luxury. Although Ford introduced several important technical improvements to the automobile, such as the use of vanadium steel, his vision to create a car for the masses was realized by fundamentally changing the manufacturing methods used to produce the product rather than by making radical changes in product design and function. What if, a century later, the same could be said for silicon interconnects in the semiconductor manufacturing industry? Silicon interposers and substrates have been in development for decades, and the technical benefits are well known. However the cost to manufacture them is still prohibitive for most applications. This article examines new developments in manufacturing solutions for silicon interconnects, which when fully realized, promises to be the game changer that would make them available for mass market applications.

Silicon Substrates vs. Silicon Interposers

Silicon interconnects can be divided into two distinct categories, each with its target applications. Silicon substrates provide interconnect between the active semiconductor device and the system board and are typically mounted directly to a PCB using an SMT assembly process. They effectively replace laminate or ceramic substrates. Routing layers are typically greater than $8\mu\text{m}$ line and space, and through Si via (TSV) diameter can be greater than $30\mu\text{m}$. Bottom side interconnect pitch must be compatible with SMT processes, so is typically greater than 0.3mm . Applications include

LED submounts, backside illuminated (BSI) CMOS image sensors, flat panel displays, etc. They also have the potential to be used for package-on-package (POP) applications to make true 3D packages at a reduced height.

Silicon interposers differ from silicon substrates in that they typically provide high density interconnect between one or more active die and a package substrate, which is in turn mounted to a system PCB. Today’s high performance interposer applications require multiple interconnect layers on the top side with $0.5\mu\text{m}$ to $2\mu\text{m}$ line and space and via diameter of $10\mu\text{m}$ or less. Top side interconnect array pitch can be as small as $40\mu\text{m}$, which necessitates thermocompression flip-chip assembly processes for active die attach. Bottom side interconnect is typically about $150\mu\text{m}$, which is compatible with today’s placement and reflow package assembly processes (Figure 1).

Silicon Interposer

Xilinx’ Virtex FPGA, for example, utilizes a silicon interposer with TSV interconnect to integrate multiple identical FPGA die (Figure 2). The FPGA is “sliced” into a series of smaller rectangular die, and then mounted side-by-side onto a high density silicon interposer fabricated using a 65nm fab process. The Xilinx architecture enables very high bandwidth, low latency interconnect between ICs and lower power

consumption.^{1,2} This approach is often referred to as 2.5D interconnect because active die are placed side-by-side on a passive interposer rather stacked vertically using TSVs within each of the active

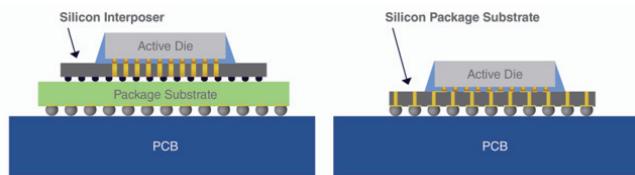


Figure 1: Silicon interposers are typically assembled into a semiconductor package; silicon substrates are mounted directly to the system PCB.

die. Thermal management is critical, and the side-by-side placement of die on an interposer allows for effective heat sinking of all die. By contrast, 3D integration of multiple high performance devices using TSV interconnect within the active die makes thermal management much more difficult.

More generally, silicon interposers are being considered as an alternative to 3D TSV stacking for high bandwidth logic plus memory integration in high-end processor applications such as NPUs, CPUs and GPUs. Here again, thermal management and power efficiency constraints are limitations. For most high performance processor + wide I/O memory applications a silicon interposer approach seems most viable.

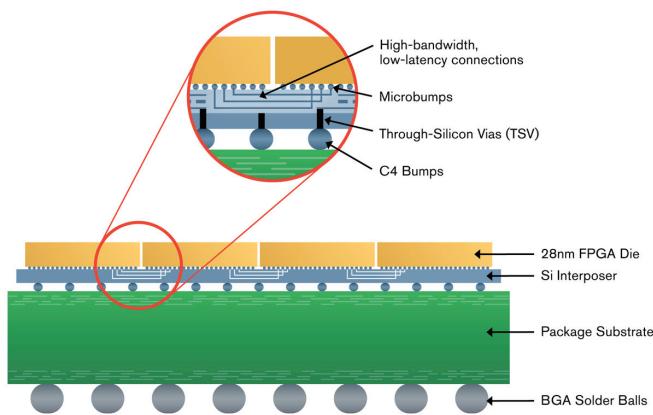
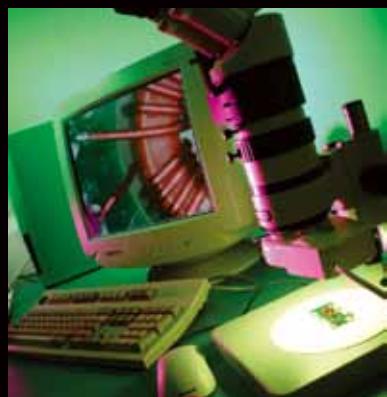


Figure 2: Xilinx FPGA device utilizing silicon interposer



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Silicon Substrates for Package on Package (PoP)

Package on Package (PoP) is widely used for 3D integration of logic plus memory in mobile handsets. Package warpage has been a primary technical challenge since PoP was introduced in 2004. In the first PoP implementations, the perimeter of the bottom package was left exposed while the package center was encapsulated. The resulting structure was unbalanced and tended to warp during SMT reflow. In recent years techniques such as through mold via (TMV) have been used to encapsulate the entire top surface of the bottom PoP package while still providing for top side PoP land pads. In parallel, an increase in interconnect density and performance of the logic device has driven a transition to flip-chip interconnect. However, laminate PoP based technologies will be challenged to meet application requirements in the future. Higher interconnect density and fine-pitch flip-chip interconnects require up to 6 layer HDI laminates for some applications, driving thickness and cost in the wrong direction. Thin silicon substrates for high-density flip-chip CSP and PoP could provide the solution (**Figure 3**).

Potential benefits of a thin Si substrate for bare die flip-chip CSP and PoP packages include:

- Substrate CTE closely matching that of the flip-chip die will provide better warpage control over the SMT reflow temperature profile
- Reduced stress on advanced ELK devices
- Higher routing density can be achieved compared to laminate substrates
- Reduced package thickness
- Possibility to incorporate decoupling capacitance within the package substrate

Cost Related Process Challenges

The high cost to manufacture silicon interposers and substrates using conventional semiconductor processes and equipment has prohibited their use in all but a few niche applications. At today's market prices, the incremental cost per unit area to produce a single routing layer

on Si using a 300mm Cu BEOL fab process at 1 μ m line and space is roughly 2x the cost required to add a 20 μ m line and space routing layer to both sides of a laminate flip-chip CSP substrate. The cost to add a single routing layer to Si using a conventional WLCSP plated Cu RDL process is roughly at the midpoint.

Additionally, process challenges with handling ultra-thin wafers have not been ironed out. In most cases, Si interposers and substrates are processed sequentially with the 2nd side of the wafer processed after wafer thinning. Expensive wafer support mechanisms are typically used to facilitate handling of thin wafers through standard semiconductor tools, adding process steps and indirect materials cost to the manufacturing process.

Finally, forming vias in silicon is still considerably slower and more expensive compared to via formation in organic substrates. The Bosch process that is most commonly used in high density interposers and 3D ICs requires expensive and slow semiconductor fab tools. Although progress has been made in improving throughput and quality of TSVs, processes are still too expensive and slow.

Most efforts to resolve these challenges involve the application of expensive semiconductor fab tools to create unique structures. To enable broad adoption of these technologies there needs to be manufacturing innovation in patterning, wafer handling and via creation.

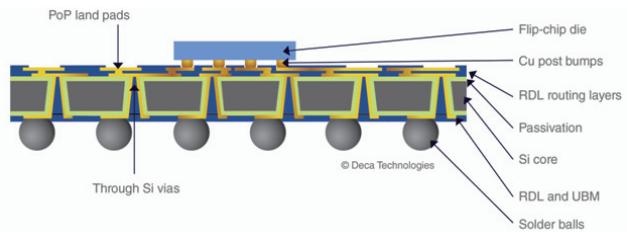


Figure 3: Flip-chip PoP based on Si substrate

technology derived from SunPower's unique solar cell fabrication process. In order to compete in the highly competitive solar market, SunPower needed to rethink the way in which semiconductor wafers are fabricated. Traditional semiconductor tools were replaced with high throughput, highly integrated production lines. The result is a manufacturing capability capable of churning out hundreds of millions of wafers per year. As it turns out, the back-end of the SunPower solar cell fabrication process is very similar to the process of creating high density routing layers on semiconductor wafers for WLCSP and flip-chip bumping. By emulating the SunPower manufacturing approach, and adding additional innovation to address the unique challenges associated with IC wafers, Deca has been able to demonstrate a fundamentally different approach to manufacturing wafer level CSPs. The benefits include inherently shorter cycle time, higher capital productivity and a high level of flexibility to introduce new products within a standardized manufacturing flow. These benefits are realized without major changes in the form, fit or function of the product. This same manufacturing capability can be applied to silicon substrates and interposers as well (**Figure 4**).



Figure 4: First example of solar manufacturing technology ported to a semiconductor interconnect foundry

Rethinking Thin Wafer Handling

Silicon substrates require dual sided processing of very thin wafers, which poses an additional challenge. Solar wafers are also two sided structures, but with the added complexity of semiconductor diode fabrication processes. Here again, the solar industry has figured out how to handle thin wafers without expensive, non-value added wafer support processes such as temporary bond and debond. Evidence of this is the several 100M solar device wafers manufactured each year with native thickness in the range of 150 μm . What if these manufacturing processes could be leveraged to the semiconductor industry for silicon interconnect wafers?

Via Creation Process Options

TSVs are typically formed by deep reactive ion etch (DRIE) for high density, fine-pitch applications or laser drilling for lower density applications. The majority of development has been focused on the DRIE process due to its capability of producing high aspect ratio and small diameter vias to enable high density interconnect. The most common DRIE method known as the Bosch process uses alternating SF₆ plasma to isotropically etch Si and then C₄F₈ to polymerize the via walls. Low energy ions are used to clean the C₄F₈ off the bottom of the via and the SF₆ is introduced again to etch the exposed Si off the bottom of the via. High aspect ratio (>1:50) TSVs have been demonstrated using this process, but 1:10 via aspect ratios are more typical in practice. The Bosch process tends to form scallops at the via sidewalls, which can complicate the down stream processes of side wall passivation and seed metal deposition. The scalloping can be reduced by employing a slower etch process that results in higher cost.

An alternative to the Bosch process is the “steady state” DRIE process. This process adds O₂ into the SF₆ plasma to passivate the sidewall and the bottom of the vias. The directional ions remove the oxide from the bottom of the vias and allow F ions to continue etching away Si vertically. This process results in tapered vias with smooth sidewalls at a higher etch rate, but undercut is difficult to control,

resulting in lower via aspect ratio.

Laser ablation has been proposed and used in a limited fashion as an alternate method for via creation. However, throughput is slow and minimum via diameter is 20 to 30 μm greater than the 10 μm (or less) diameter required for high density logic plus memory interposers. The percussion laser drilling process focuses a sequence of laser pulses on the same spot to drill the vias sequentially

(Figure 5). Laser via formation could be a viable option for silicon substrates where via density is low and larger vias are acceptable.

Researchers at Georgia Tech’s Packaging Research Center have launched efforts to develop cost-effective 3D systems based on glass substrates. This approach is based on an ultra-thin, double-side 3D interposer, made of either low-cost ultra-thin



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polycrystalline silicon or low-cost ultra-thin glass, not only in 200-300mm wafer form but also in large, 450-700mm panel form.⁴ As part of this work they have demonstrated a high throughput, fine pitch laser ablation process capable of producing through vias at 30µm pitch though 55 µm thick glass. Rather than drilling holes sequentially, they used an excimer laser with a mask projection technique that allowed formation of over a thousand vias in parallel. By forming through vias in the glass, subsequent back-side thinning and reveal steps are eliminated.⁵

Conclusion

Silicon interconnect has not yet been widely deployed to mass market applications, but adoption of high density interposers will accelerate over the next few years, driven by high performance logic plus memory devices that can't be realized without fine pitch silicon interconnect. However, standardization around the silicon

interconnect structure, design rules and materials coupled with innovation in manufacturing methods to drive down cost is needed to enable broad adoption of silicon interconnect. Just as Ford delivered on his promise to democratize the automobile by challenging conventional manufacturing methods, so must there be delivery on the promise of silicon interconnects for the masses. ^{SR}

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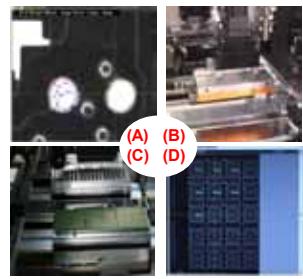
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The Material Breakthrough Towards Standardized Thin Wafer Processing

By Thorsten Matthias, Juergen Burggraf, Daniel Burgstaller, Markus Wimplinger, and Paul Lindner [EV Group]

3D stacked ICs (3D-ICs) have been a hot topic for several years, but recent announcements from leading image sensor and memory manufacturers show that 3D-ICs are finally moving into high-volume manufacturing (HVM).

The main difference between a standard 2D wafer fab and a 3D-IC wafer fab is the ability to process both sides of an ultra-thin wafer and to manufacture through silicon vias (TSVs). Wide I/O DRAM is currently targeting 20 μm thin wafers. The most obvious reason for thin wafers is the reduced form factor, which is especially important for handheld devices. However, perhaps even more important is that thinner wafers enable significant cost reduction for TSVs. The silicon real estate consumed by TSVs has to be minimized for the final device to provide a performance advantage compared to traditional 2D devices. The only way to reduce area consumption by TSVs is to reduce their diameter. For a given wafer thickness, the reduction of TSV diameter increases the TSV aspect ratio. However, the cost and cycle time of the main TSV manufacturing process steps (etching, barrier/seed layer deposition and plating) increases significantly with higher aspect ratios. Thinner wafers enable smaller TSV diameters and lower TSV aspect ratios—thereby enabling lower cost for TSV manufacturing.¹

Implementing thin wafer processing in high-volume memory manufacturing has brought a significant change of process and equipment requirements. In the past, early adopters of thin wafer processing in the fields of power electronics and compound semiconductors designed the backside process flow around the ability to handle and process a thin wafer. Today, for stacked memory applications, the compatibility with standard processes at highest yield is a must. Today's thin wafers

usually have microbumps on both sides. To ensure high yield for thermo-compression microbump bonding, the thin wafers have to fulfill wafer fab cleanliness requirements after debonding. In a nutshell, the industry demands standardized processes for thin wafer handling. A revolutionary low temperature proprietary temporary bond and debonding* technology achieves just that through standardized and material-independent processes and equipment.

Thin wafer processing by temporary bonding

Thin wafer processing is enabled by temporarily bonding the device wafer to a rigid carrier wafer (**Figure 1**). After front-side processing of the device wafer is completed, it is bonded face down to a rigid carrier wafer.

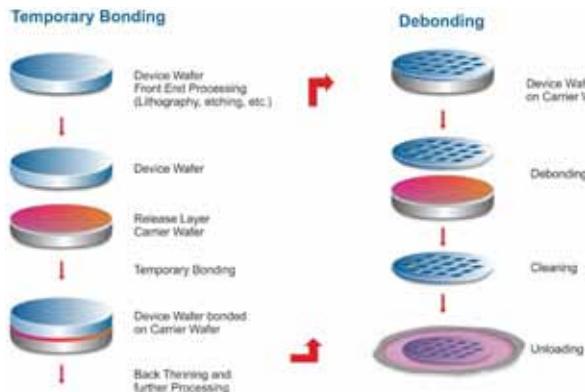


Figure 1: Principle of thin wafer processing using temporary bonding to a carrier wafer.

A temporary adhesive is used for wafer bonding. Silicon or glass wafers are the most common choices as carriers. The carrier wafer gives mechanical support for the device wafer during backgrinding and all subsequent backside processing steps. After the entire backside processing of the thin device wafer is completed, the thin wafer is debonded from the

carrier and mounted on a dicing tape on a film frame.

For many applications, the device wafer will have topography (e.g. microbumps) on the front side, which have to be embedded in the adhesive layer. **Table 1** shows the three main topography ranges used for thin wafer processing and 3D-ICs. For wafer thinning, the adhesive should

Topography	Interconnect	Application
<10 μm	Bonding Pads	Die to Die Various
~30 to 40 μm	Microbumps, Cu-pillars	Die to Die Die to Interposer
~80 to 90 μm	Bumps	Die to Substrate Interposer to Substrate

Table 1: Product wafer topography for various interconnect levels

be rigid at room temperature; otherwise, the difference in compressibility between a rigid bump and the soft adhesive results in dimples during backgrinding. It is important to avoid entrapped gas in the bond interface, which expands during high temperature processes and can potentially burst the thin wafer. To enable smooth TSV reveal processes after thinning, the post-thinning total thickness variation (TTV) of the device wafer has to be

minimized. The adhesive layer coating uniformity, the temporary bonding process, and the thinning process all impact the post thinning TTV. **Table 2** shows the roadmap for adhesive layer TTV as a

Bondline Thickness	TTV today	Q2 / 2012	Q4 / 2012
20 μm	1.5 μm	1 μm	1 μm
50 μm	3.5 μm	3 μm	2 μm
100 μm	5.5 μm	4 μm	3 μm

Table 2: Roadmap for adhesive layer TTV

function of the bondline thickness. For backside processing it is important for the device wafer to be well aligned to the carrier wafer. The SEMI spec for wafers allows significant wafer diameter variations. To compensate for these variations, a mechanical center-to-center alignment is applied, which achieves <50µm (3σ) alignment accuracy. Such precise alignment accuracy is necessary to achieve high die yields at the wafer edge. For integration schemes where high-end photolithography scanners are used, it is important that the die are immediately within the field of view; otherwise, the expensive scanners would waste time searching for the start position. As pre-alignment is based on the positions of notch and the wafer edge—which in the case of a temporarily bonded wafer stack are the notch and the edge of the carrier wafer—it is important that the device wafer and carrier wafer are accurately aligned.² For these applications, an optical alignment with alignment keys is applied with alignment accuracies of ≤1µm (3σ).

Debonding – the key for reliable thin wafer processing

Up until now, the adhesive properties, carrier properties, and debonding method were closely linked, imposing severe limitations on manufacturability. Laser-induced debonding required a glass carrier. For solvent release adhesives, the carrier had to be perforated to provide access for the solvent to the bond interface. The perforation of the carrier caused the thin Si wafer to flex above the holes during backgrinding and polishing, which resulted in thickness non-uniformities (“dimples”). Combining thermoplastic materials with perforated carriers can lead to adhesive squeezing out through the carrier perforation during wafer bonding and other processes at elevated temperatures. For thermally induced slide-off debonding, a thermoplastic adhesive is used. Heating the adhesive to the debonding temperature reduces the viscosity of the material, which allows it to slide off the thin wafer without mechanical stress. Of course, the debonding temperature has to be lower than the reflow temperature of the bumps. The higher the temperature,

the lower the adhesive viscosity and its ability to withstand the internal stress of the thin wafer. Therefore, for most slide-off adhesives, the maximum operating temperature is only 50-100°C higher than the debonding temperature. Therefore, the debonding method has defined the choice of carrier and adhesive and imposed severe limitations on the adhesive properties.

A revolutionary new temporary bonding and debonding technology has been developed to break this link between debonding method and adhesive properties. With it, the debonding process is no longer a function of the adhesive, but has become a function of a novel carrier design (**Figure 2**). This carrier has two zones, which differentiate by the degree of adhesion between the adhesive and the carrier. The adhesion in the center zone is reduced, whereas full adhesion is at work in the edge zone. While the adhesion in

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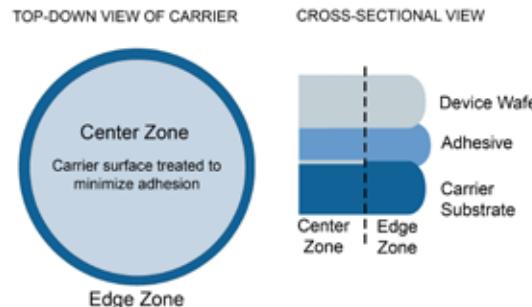


Figure 2: Left: top-down view of a specially designed carrier, Right: cross section of a same carrier; the carrier surface of the center zone is treated such that the adhesion is reduced.

the center zone is reduced, it still needs to stick to ensure a good thermal conductivity through the wafer stack and to keep the wafer flat during high-temperature processes. As the wetting mechanism varies for different adhesive classes, the center zone treatment has to be adjusted accordingly. The physical and chemical properties of the center zone must not be impacted by the thermal exposure during backside processing. Center zone treatments have been qualified, and are stable up to 425°C for multiple hours. It is important to note that the device wafer's surface does not have to be treated for this

technology, which makes it compatible with any kind of surface passivation. This is especially important with regards to assembly after thin wafer processing. Debonding methods that rely on device wafer surface modifications can cause adhesion problems with the underfill material during die bonding.

Figure 3 shows the debonding principle using this carrier. During the first step, the adhesive in the edge zone** is dissolved. The center zone with the reduced adhesion is now the only connection between the thin device wafer and the carrier. The device wafer is separated from the carrier during a proprietary debond** step with a pure mechanical separation at room temperature. It is important to note that the actual separation happens between the adhesive layer and the carrier wafer. This means that the debonding is totally independent of the top passivation layer of the device wafer. The debonding is also totally independent of topography in the bond interface (spherical bumps or pillars; 35µm or 80µm feature size, even for stacked dies on an interposer). Since the debonding process happens at the boundary between adhesive layer and carrier, the topography does not have any impact on the debonding process. During the debond step the bumps in the bond interface are embedded in the adhesive layer. No vertical or shear force is applied to the bumps during debonding, which eliminates the risk of bump damage. After

1st Step: Edge Zone Release (EZR®)



Release adhesives at the stack edge

2nd Step: Edge Zone Debond (EZD®)

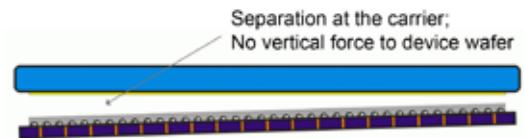


Figure 3: During the release step the adhesive edge zone is dissolved; the thin device wafer is separated from the carrier during the debond step.

debonding, the device wafer is cleaned in a dedicated thin wafer cleaning module. Thermoplastic adhesives are removed by solvent stripping. Solvent cleaning has the advantage of working well with spherical bumps—no force is applied to the bumps during adhesive layer removal.

Figure 4 shows the entire debonding process flow as it is implemented in a production debonding system***. The bonded wafer stacks are delivered to the system in a FOUP. First, the edge zone release step is performed as a single wafer process. As a result, a thin free standing wafer edge is created. Putting the wafer stack into a FOUP after the release step can result in edge chipping. Combining the release and debond steps into one system is necessary for high yield debonding. Then the wafer stack is mounted on a film frame. Performing the edge zone release

process prior to film frame mounting allows using dicing tapes, which are not compatible with the solvents used for this process. This gives foundries and OSATs full freedom of choice for the dicing tape. The edge release cycle time depends on the adhesive properties as well as on the process technology. With optimized process modules, cycle times of less than 10 minutes per module have been qualified for several adhesives that were optimized for this technology. For HVM, the bond tool system is configured with up to nine process modules. After debonding the device wafer has to be cleaned. During cleaning, the dicing tape is protected from exposure to the cleaning chemistry. The thin wafers on film frame are unloaded into a cassette.

The analysis of the process sequence shows that the debonding is completely

independent of the adhesives properties. This opens up a new field for adhesive engineering. Taking away the necessity to design the debonding process into the adhesive enables greater focus on the other success criteria for a temporary adhesive. The adhesive has to be solid at low temperature to enable backgrinding without dimples. It has to withstand the thermal and chemical exposure during backside processing. After debonding, the adhesive has to be cleanable according to the requirements of a wafer fab. There must not be any residue or modification to the device wafer surface to allow standard underfill processes during assembly. This novel debonding process works with all kinds of materials: dedicated thermal release adhesives, dedicated laser release materials and dedicated solvent release materials. Debonding is now a standardized process independent of the specific temporary adhesive, and represents a major milestone in thin wafer handling.

For the introduction of a new

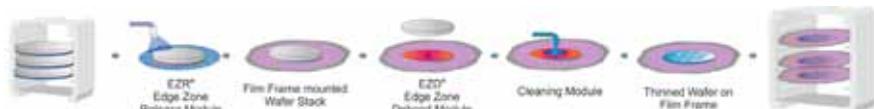


Figure 4: Full debonding process sequence.



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manufacturing technology like thin wafer handling, another important milestone is a versatile supply chain in which customers have complete freedom of choice in regards to the temporary adhesive. Any type of adhesive from any supplier can be used, thereby providing investment protection. In the future there will be exciting new developments in temporary adhesives—the standardization of the debonding process ensures that today's equipment will work with tomorrow's adhesives.

An open platform has been established in Europe, the U.S. and Asia for all parties in the thin wafer ecosystem to provide the infrastructure for adhesive development and qualification on the newest equipment generation. A standardized qualification procedure for new adhesives has been developed and its temperature capability evaluated by thermal treatment of bonded wafers instead of open surface TGA measurements, since even very little outgassing in the bond interface can result in thin wafer defects. The coating uniformity and edge bead are qualified pre- and post bonding. The adhesive's ability to enable ultra-thin wafer thinning is qualified by post-thinning TTV measurements and thin wafer-edge quality assessment. In regards to HVM, the cycle time of edge zone release and edge zone debond processes is determined. **Figure 5** shows the temperature capability of various high-temperature materials. Adhesives have been qualified for the high temperature processing range up to 320°C specifically targeting power device manufacturing. For memory applications, a key criterion is to keep the bonding temperature well below

200°C. Due to the described standardized debonding process and equipment it is now possible to develop and implement application specific adhesives.

The availability of carrier wafers is another important aspect for a reliable and versatile supply chain. For pilot line and low-volume production, carrier preparation modules are available that can be integrated into the temporary bonding system. For high-volume manufacturing, a dedicated carrier manufacturing system is available. Standard silicon or glass wafers can be used as carrier wafers, which give long-term cost clarity

(Figure 6).

Wafer logistics is an important aspect as wafer bonding is different from any other fab process. Two incoming wafers are bonded and typically unloaded into a dedicated receiving cassette. This means that three FOUPs are used just for one processing cycle. For continuous mode of operation it is necessary to have six FOUPs on the tool, which has been implemented with a local FOUP storage system. The same applies to debonding, where three cassettes (1x incoming wafer stack, receiving cassette for the carriers, receiving cassette for thin wafer on film frame) are used for one processing cycle. An integrated metrology module ensures seamless integration with the TSV reveal processes after thinning.³ The wafer-to-carrier alignment during

temporary bonding achieves better than 50 µm (3σ) alignment accuracy. This prevents downstream problems with the thin wafer edge, but also ensures uniform backside process results.

breakthrough in thin wafer processing. It enables room temperature debonding, which is independent from the properties of the temporary adhesive. As a result, it enables a standardization of the debonding process and debonding equipment since it is material independent. Additionally, an open platform has been established to enable a versatile supply chain with multiple adhesive suppliers. Manufacturing of the carrier wafer is integrated in the high-throughput temporary bonding/debonding production platform. 



Figure 6: This production platform for temporary bonding and debonding can accomodate up to 9 process modules.

Acknowledgements

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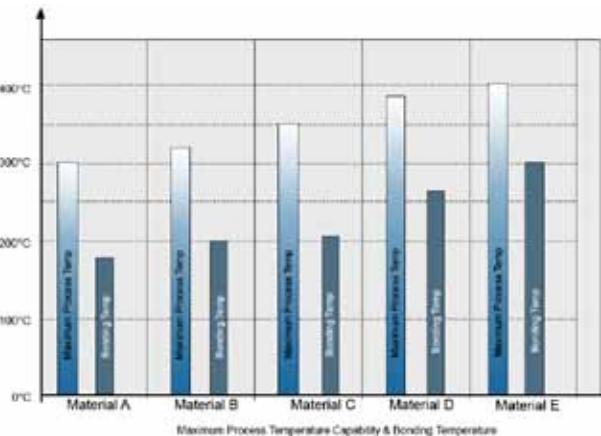


Figure 5: Various adhesives with high temperature capability.

Innovation Driver of the Next Decade: Heterogeneous Integration

By Prof. Dr.-Ing. Klaus-Dieter Lang, Harald Pötter, Rolf Aschenbrenner, Karl-Friedrich Becker, Lars Boettcher, Oswin Ehrmann, Martin Wilke, Dr. Michael Toepper [Fraunhofer IZM and Technische Universität Berlin]

Using micro-level integration technologies to manufacture high-end microelectronics, microsystem technology and sensor technology has increased dramatically around the world. Little wonder, as their potential for application is almost infinite. Development is advancing particularly within the automotive and mobile communications industries. The trend towards increasing the benefits of a product is also leading to growing demand for integration of miniaturized sensors, autonomous power supplies, and standardized communication functions in other sectors, such as safety and security, energy and medical engineering.

This change is reflected in national and international technology and product road maps, such as those of the German Electrical and Electronic Manufacturers' Association (ZVEI) and the US-based IEEE. Optimally adapting electronics to the product and its typical application environment is a basic requirement in such developments. Further high-tech products are expected from systems that are developed across sectors, such as wireless, miniaturized sensor and transmission systems for medical or living environment monitoring that are combined with security and identification systems.

Two trends are helping to shape the ongoing development of system integration technologies. First of all is the increase in the number of functions directly included in a system combined with the demand for higher reliability and longer system lifetime. Second is the increasingly seamless merging of products and electronics, which necessitates adapting electronics to predefined materials, forms and application environments. Only by these means, systems sensors—which are often installed in extremely harsh

environments—and signal processing can be implemented near to the point where signals are occurring.

The Status Quo and Trends in Electronic System Integration

The European semiconductor industry has largely abandoned the development of CMOS technology. Instead of broad-based applications, European companies like Infineon, ST and NXP are successfully pursuing the development of customer-specific, multifunctional systems with the largest possible lot sizes. The key to such products is integrating customer-specific components with various digital functions (such as memories and processors) into extremely small build spaces, and/or including non-digital functions such as power electronics, high-frequency electronics or optoelectronics. Using standard CMOS technologies for such tasks is too expensive or risky, and in some cases may be technological impossible. Consequently, developers are turning to heterogeneous and hybrid integration technologies.

Heterointegration technology is used to develop customer-specific solutions that can also be manufactured cost-efficiently at

medium lot sizes. A wide range of industry sectors stand to benefit from this approach of turning ideas into products.¹ However, in the past, heterogeneous integration was too focused on developing stand-alone systems, in which components are retrospectively integrated into the overall system (such as vehicles and machines). In the future, we can expect seamless merging of multifunctional electronics and the overall system (Figure 1).

Targeting Application-Oriented Multifunctional Electronics

It follows that the heterointegration approach to developing application-oriented multifunctional electronics will begin with the end-product and its functional requirements. The synergy between application industries and suppliers of electronic functionalities is expected to give rise to great potential for innovation. This is especially the case for Germany's industry, which strength lies in the development of intelligent and customer-specific products.

Comprehensively implementing this approach necessitates new technologies and changes to the product development process.¹ In the integration of electronics

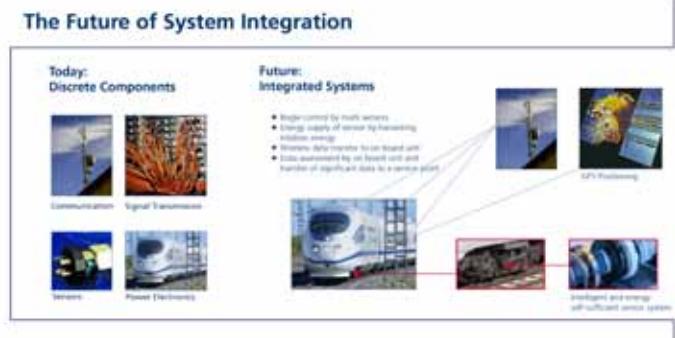


Figure 1: Future system integration: Embedding of electronics in products, operating procedures and service concepts (Source EPoSS – European Platform for Smart System Integration)

and microsystems into the product, conventional technologies and processes can no longer meet the demands of extended functionality and expected product price. An increasing number of difficulties are arising, particularly where non-electronic information or optical, mechanical, fluid or chemical signals have to be processed in often harsh application environments.² Merging the electronics with the overall system will see traditional system boundaries in research and the development of new products begin to dissolve. This includes a seamless communication along R&D interfaces as well as improved manufacturing logistics between companies throughout the supply chain. To realize this, the application industry, such as the medical, safety and security or energy sectors, will have to be included at the very beginning.

Technologically, the approach includes a wide range of processes for physically integrating electronics into an application or product environment. Both simple components and microsystems can be used as subsystems and can be integrated into diverse environments, such as planar build spaces. Another possibility is adapting extremely miniaturized systems into high-end products for innumerable purposes, such as securing quality, performance, lifetime, and originality.

As EMSs often only manufacture such products in small or medium lot sizes, but at the same time want to price the product affordably, all these technologies and manufacturing processes have to be optimized and integrated to meet the specifics of each company's manufacturing environment and needs.

In micro- and nanotechnology, an efficient and optimized interplay between the material properties and the packaging technology is needed to meet the various application challenges outlined above. Partial measuring and testing is generally not possible due to the complexity and tight integration of varying system components. Consequently, successful development is only possible if the functional system design, material, and technology optimization and design for reliability are coordinated with each other at the beginning of the development

process. This article discusses two main packaging technology areas set to play key roles in the future: wafer-level packaging (WLP) and embedding technologies for polymer substrates.

Heterogeneous Integration at the Wafer Level

In the broadest sense, WLP is a synonym for adding layers on active electrical components like CMOS- or MEMS-wafers for the next level of interconnect. Optimally, these packages can be used directly after singulation in the system assembly, as it has been done for nearly twenty years with flip chips. In the case of sensors, for example with front side illuminated imagers as example, the flip chip approach is not possible because the optical active side of the die is the same on which the electrical contacts are located. Flip chip bonding such a device on an opaque substrate would therefore block the photodiodes from incoming light. Therefore, image sensors were wire bonded for a long time, even though flip chip technology was already commercially available for consumer products.

With the development of through silicon via (TSV) technology, it was possible to redistribute the electrical contacts to the backside of the device, making WLP accessible for image sensors, and they became the first products in which TSVs were industrially applied.^{5,8} For the fabrication of a complete camera system, the assembly of multiple optical elements such as lenses, and apertures is necessary. Commonly used optics involves mounting optical elements in a lens barrel that is screwed into a mount after the image sensor is electrically connected to the substrate. The optic assembly is therefore a serial process and ongoing efforts

are heading to wafer level manufacturing to save manufacturing time and costs. The development phases of WLP from basic redistribution technology to fully integrated wafer level cameras with TSVs are shown in **Figure 2**.

Figure 3 shows a two-part process flow for manufacturing and integrating wafer level cameras. In the sensor wafer process path, the CMOS wafer is permanently bonded to a glass wafer (3/Bs), which must be part of the optical design. Subsequently the TSVs, the backside redistribution layer, and the bumps are formed (3/Cs). The key enabling technology for WLP of camera systems based on top-side illuminated imagers are TSVs because these allow a redistribution on the backside of the wafer, while the active side remains unaffected and is completely usable for the optic assembly. These process steps are discussed in detail by Wilke et al.^{2,3}

In the lens process path, one or multiple

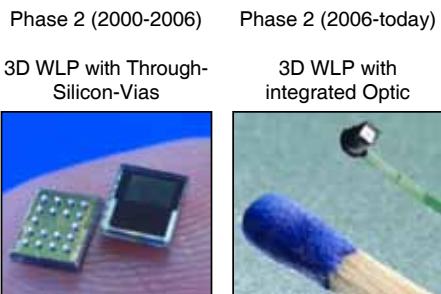


Figure 2: Development Phases in Wafer-Level-Packaging. (Right handed picture courtesy of Awaiba.⁷)

lenses are manufactured on wafer level (**Figure 3**). The wafer level fabrication of the lens components is predominantly based on UV-replication. Here, an array-like tool accommodating the molds of

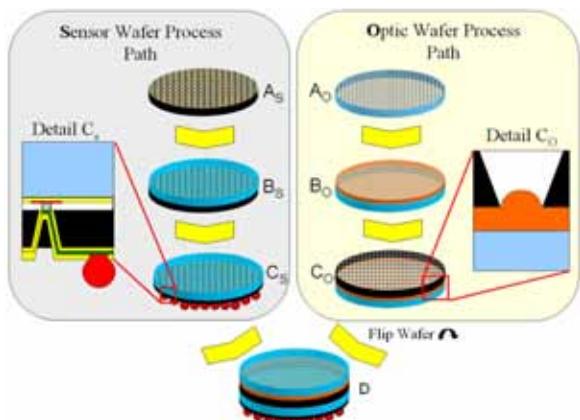


Figure 3: Manufacturing concept of wafer level cameras.

the individual lens surfaces is brought into contact with a liquid polymer which hardens under exposure to UV-radiation. The integration of the optical elements requires aligned wafer bonding. Since the optical elements in the cameras need a tight vertical positioning to each other, some kind of spacer structures are needed. Depending on the optical design, this requirement can be met with spacer wafers or by micromachining spacer structures directly in the lens wafer. **Figure 4** shows a packaged and diced lens cube consisting of three lens and one aperture layer with thinned CMOS imager.



Figure 4: Packaged and diced lens cube consisting of three lens and one aperture layer with thinned CMOS imager.

Heterogeneous Integration on System in Package Level

Integration on wafer level with a focus on TSV technology is one of the most challenging topics in the packaging market today. However, the technology gap between standard chip interconnection technologies and TSV interconnects has to meet many requirements posing multiple challenges. Therefore systems-in-package (SiP) are a highly competitive solution for heterogeneous designs, in which different functions have to be integrated. Because SiPs can rely on standardized processes, there are fewer obstacles to expect on the levels of property issues, yield, testability and especially cost, as costs rise significantly for WLP with higher

complexity of the system.⁷

Within the SiP approach, embedding technologies offer the advantages of improved electrical performance, capability of 3D-stacking, reduced package thickness, and enhanced thermal performance for components assembled on thermal interfaces and heat sinks. The emergence of embedding packages steadily changes the packaging value chain and consequently sets new roles

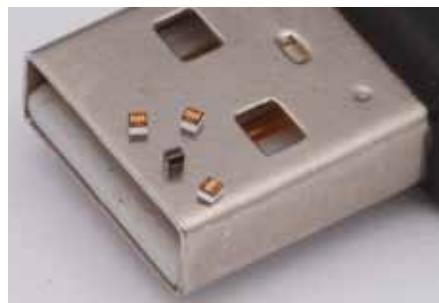


Figure 5: Wafer-Level-Camera in comparison to a USB connector

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for all players in the whole packaging value system.⁴ The initial value share of substrate suppliers for production of FCBGA devices was about 20%, but now with embedded technologies, the substrate suppliers can also perform component assembly before embedding and thus count for 55% of the embedded package value.⁵ However, it should be underlined that the shift to embedding technologies requires adaptations to the supply chain, which will potentially burden the value system. For instance, the necessity of RDL layer for chip pitch enlargement that makes chip components compatible with existing embedding capabilities or copper pad deposition should be definitely accounted for before the shift in embedded packages. Initial applications for embedded packages will be low-cost, low-pin-count applications such as analog and power devices (DC/DC converters, Power MOSFETs etc.)⁶ There are forecasts for a \$0.5B extended market by 2015.⁵

The dominating technology for power chip embedding is a face-up technology.

Chips are bonded with their backside (drain contact) to a copper substrate using highly conductive adhesive or solder (**Figure 6**). The combination of two or more embedded dies e.g. MOSFET or diodes, but also controller chips, results in embedded power SiPs (**Figure 7**). Here, the embedding technology offers a variable technology platform for the realization of a large variety of packages on the same process line.

New developments have started toward the realization of complete and more complex power systems (**Figure 8**). The drivers here are the high potential of compactness, robustness and high reliability of such systems. In the EU project “HERMES”, one project goal aims to realize an embedded “control integrated power system” as an embedded power system. Parts of the system operate at voltages of 600 V and electric currents of 5-50 A, whereas other parts of the circuit operate at the moderate voltages and currents of state-of-the-art CMOS. Such systems are used as motor controls

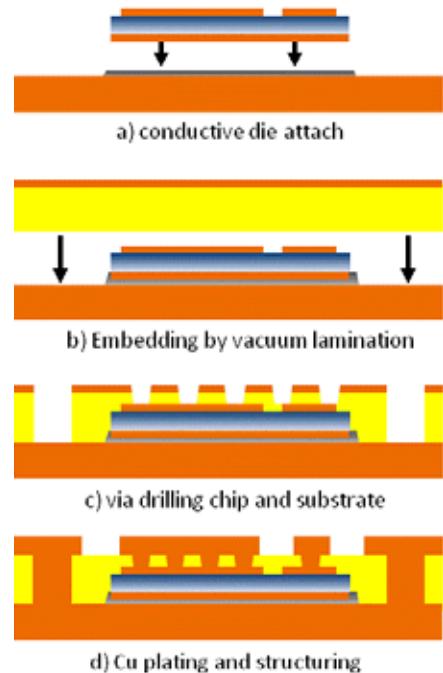


Figure 6: Process flow for face up power component embedding for variable speed drives in industrial application such as washing machines and air conditioners.

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Figure 7: Embedded Power SiP

Conclusion

Heterogeneous integration bridges the gap between microelectronics and its derived applications. Emerging device technologies and new application requirements drive progress in this area. New technologies and architectures are arising to bring this progress made in microelectronics, microsystem technologies, and bio-electronic or photonic component technologies into application. The future belongs to integration technologies that combine several components into a highly integrated assembly in one package.

WLP processes will play a key role in this context. Due to

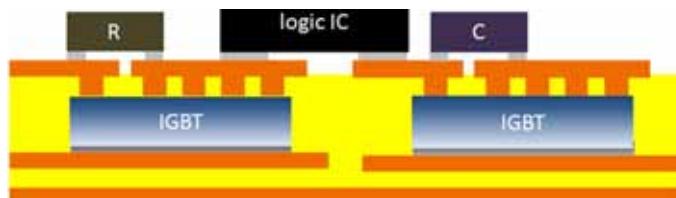


Figure 8: Embedded Power System

signal propagation delays, wiring density or confined available space many future applications require considerably more compact components. 3D integration can help overcome this bottleneck. Examples of 3D integration start with silicon 3D integration and go up to stacking of packages or modules at all technological levels.

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(continued on Page 43)

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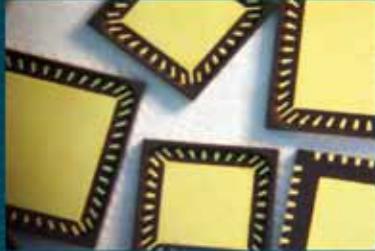
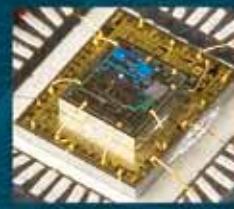
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MARKET TRENDS

Status of the OSAT Industry

By Ronald J. Molnar, [AZ Tech Direct, LLC]

After enjoying a substantial 35-40% growth in 2010, outsourced semiconductor assembly and test (OSAT) suppliers were hampered in 2011 by the slow global economic recovery coupled with two natural disasters. The magnitude 8.9 earthquake and subsequent tsunami that struck Fukushima, Japan in March 11, 2011 not only damaged several nuclear power plants in the area but disrupted the manufacturing of several key materials in the supply chain for several months. Additionally, torrential rains in southeast Asia caused massive flooding in and around Bangkok, Thailand in late October 2011. Manufacturers of hard disk drives felt most of the impact.

Forecasts for the semiconductor industry began to be revised downward by mid-year. Foundry overcapacity, inventory correction, and slowing demand reduced growth expectations for 2011 and 2012. According to Joanne Itow, Sr. analyst at Semico Research, "semiconductor revenues increased a paltry 0.4% and units actually dropped by 0.1%." Likewise, Jim Walker, Research VP of Semiconductor Manufacturing at Gartner, noted, "2011 saw very limited growth due to the overall world economic problems. Even with that, we believe the SATS market grew a few percent." IC Insights reports that the semiconductor market grew only 2% from \$314.2B in 2010 to \$319.5B in 2011.

Top 5 OSATS Represent 50% Market Share

The 2011 financial numbers are still being compiled, but it is safe to say the five largest OSAT firms will remain the same: (1) ASE, (2) Amkor, (3) SPIL, (4) STATS ChipPAC, and (5) Powertech Technology. Together they account for about 50% of the OSATS revenue market

share, whereas the next 15 largest firms account for another 25% share.

Executives from each of the top five OSATs were asked to comment on the past year and to give us a glimpse of what is to come this year.

Rich Rice, Sr. VP, Sales and Engineering, ASE

Competitive Advantage: Over the past decade, ASE has firmly established itself as the world's leading OSAT, driven by technology expertise, manufacturing prowess, and significant capital expenditure investment. Strategically located in key semiconductor geographies, ASE is well positioned to meet customer requirements across extensive end-use applications. Our expertise and scale in advanced and legacy technologies, and our ability to integrate solutions into turnkey services allow us to benefit from the accelerated outsourcing trend and better serve our existing and potential customers.

New Capabilities: ASE is proud of its R&D heritage; focusing spending on technology development, low-cost package pipelines, and expansion in copper wire-bond and high-density low-pin-count packages. To date, we have shipped over 6.7B units of copper wire-bonded packages and have installed the largest copper wire-bond capacity in the world. In addition, ASE has seen rapid expansion in wafer bumping, FCCSP, WLP, and copper pillar technologies (**Figure 1**). We will increase our investment in advanced packaging technologies from \$90M in 2011 to \$200M in 2012.

Future Outlook: With 2011 revenue of US\$4.5B, ASE achieved 9% growth year-on-year to strengthen our OSAT market leadership position.

With current inventory at much lower levels and an improving market climate,

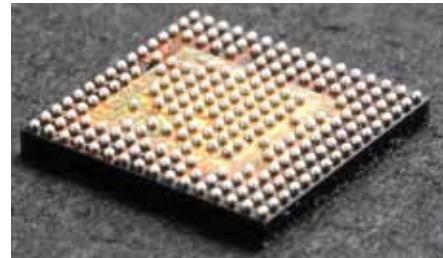


Figure 1: ASE invests in rapid expansion of wafer bumping, fcCSP, WLP, and copper pillar technologies.

we are optimistic that 2012 will be a better year than 2011. ASE intends to strategically expand production capacity, with a focus on providing customers cost competitive and innovative solutions. We believe that growth will come from both our copper wire bonding and advanced packaging technologies, as well as our low-pin and discrete portfolios.

Lee Smith, VP, Business Development, Amkor Technology

Competitive Advantages: As an OSAT, Amkor has been a pioneer in our industry, with over 4 decades of innovation and technology leadership. Over the past decade, Amkor made strategic investments in advanced packaging technologies for the communications market that have yielded significant results (**Figure 2**). "During the

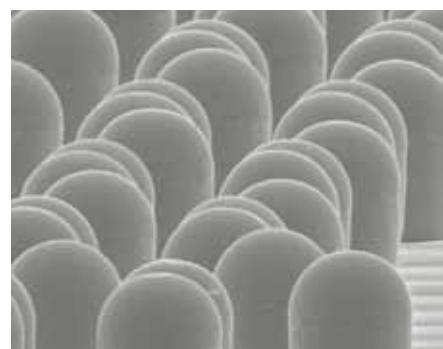


Figure 2: An array of copper pillar pbumps at 40µm pitch. Each pillar possesses a SnAg cap (photo courtesy of Amkor Technology, Inc.)

fourth quarter we saw record quarterly sales in our wireless communications end market driven by strong demand for smartphones and tablets," said Ken Joyce, Amkor's president and CEO.

New Capabilities: Through mold via package-on-package (TMV® PoP) and fine-pitch flip chip with copper pillar bumps—two of Amkor's latest advanced package platforms—reached significant milestones, surpassing 100M units shipped in the fourth quarter of 2011.

For high performance networking applications, Amkor qualified a complex 2.5D package architecture requiring high density Cu pillar micro-bumps to 40 μ m pitch and FC stacking for 28nm low- k devices onto a through silicon via (TSV) silicon interposer based FC BGA.

Even the mature PBGA platform saw innovation last year through the transition from corner gate to center pin-gate molding, providing cost, quality and performance benefits. This enables high wire density devices to maintain wirebond designs and benefit from 28nm die shrink and electrical performance gains.

Future Outlook: Demand for smartphones and tablets is expected to remain strong for 2012, and we continue to add capacity in support of customer demand in the communications sector.

On the technology front, we are seeing tremendous demand in development of new 3D package architectures with TSV and copper pillar micro-bump interconnects. These technologies will serve our industry for decades forward and are changing the model on how the supply chain collaborates in developing and deploying new IC device, interconnect and packaging technologies.

Alex Chenok, VP, Strategic Marketing, Siliconware Precision Industries (SPIL)

Competitive Advantages: SPIL continues to be one of the go-to partners for full turnkey bump/assembly/test services. Our consistent financial health and focused customer base enables customers to enjoy

a partner capable and willing to make mutually beneficial investments to grow and penetrate markets together. These investments include internal resources, facility expansion, and co-development of next generation package platforms.

New Capabilities: 2011 was a

significant year for us as we brought up 3D-IC, enhanced PoP, copper wire mass production, and system-in-package (SiP). Each of these technologies benefit the customer, either in reducing the package footprint, enhancing device performance and reliability, or long-term cost reduction

The advertisement features the Wells-CTI logo at the top left, consisting of a stylized blue and white graphic followed by the company name. Below the logo, the text "Worldwide leader in Thermal Solutions, Burn-in Sockets & Cres Testers" is displayed in a serif font. The central part of the ad shows several thermal test equipment components arranged on a blue background with radiating lines: a "Thermal Control Unit" (a handheld device), a "Thermal System Controller" (a rectangular box), a "CR-2601" unit (a small rectangular device), and three different series of burn-in sockets: the "773 Series", the "860 Series", and the "730 Series". At the bottom, there is a large image of the "Zephyr Thermal Control System", which is a tall, industrial-looking metal cabinet with a control panel and a flexible probe arm. The text at the bottom right reads: "WELLS-CTI is proud to introduce the Zephyr Thermal Control System to our line of Direct Touch Technology products for precise control of DUT temperature during qualification test and characterization." At the very bottom, it says "Find out more!" and provides the website "www.wellscti.com".

to protect against the uncontrolled materials price.

Future Outlook: Based on our focused customer base, we're still very strong in the mobile wireless and processor markets; but waiting to ride the recovery wave back up on the HDD controller market that was impacted by the floods in Thailand. Our copper wire assembly volume is on track to exceed even our own expectations. We expect our business to pick-up by June.

Steve Wofford, Sr. Director, WW Marketing Communications, STATS ChipPAC

Competitive Advantages: As a leader in the OSAT industry, STATS ChipPAC is focused on technology differentiation, full turnkey assembly and test solutions, and operational excellence. The company has invested heavily in development and manufacturing capabilities for advanced wafer level technologies including embedded wafer level ball grid array (eWLB) (**Figure 3**), wafer level chip scale packaging (WLCSP), integrated passive devices (IPD) and TSV as well as advanced copper column flip chip technology (fcCuBE™). These technologies position the company to continue to meet customer requirements for increased performance and functionality in a smaller footprint for sophisticated mobile devices.

New Capabilities: In 2011, STATS ChipPAC introduced the second generation of its eWLB technology. Additionally, shipments of the original generation of eWLB approached 200M units. The initial offering of next-gen eWLB will include multi-die and multi-layer configurations further leveraging the unique value of this technology as a robust integration platform, and the thinnest 3-D packaging solution in the industry. Other new capabilities included enhancements to STATS ChipPAC's innovative fcCuBE™, introduction of 300mm mid-end processing of TSV and interposers for 3-D and 2.5-D applications, and enhancements to its copper wirebond capabilities including finer bond pad pitches, thinner wire diameters, stacked die packaging and

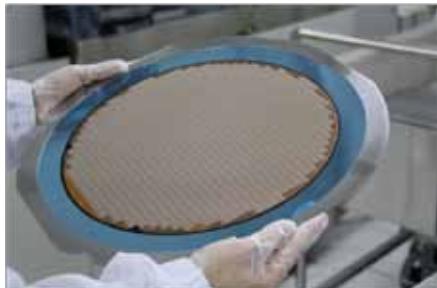


Figure 3: STATS ChipPAC eWLB wafer die-to-die bonding.

Future Outlook: 2012 is expected to offer opportunities for new growth in 2D, 2.5D and 3D packaging needs of high-performance communications products. STATS ChipPAC will continue to invest and innovate to meet both the advanced packaging needs with its wafer level and flip chip technologies, and the need for cost-effective mainstream solutions with its copper wirebond technology.

J. S. Leu, Sr. V.P., Packaging Operations, Powertech Technology Inc. (PTI)

Competitive Advantages: PTI was built on a strong engineering foundation and continues to leverage this capability as we expand our customer base and product offerings (**Figure 4**). As a key supplier to top Japanese semiconductor companies, PTI has invested in the most advanced manufacturing tools available with close

attention to cost control, allowing us to become the largest manufacturer in the world in the highly competitive memory assembly and test business. These factors have allowed the company to seamlessly move into a number of high-volume non-memory programs with top semiconductor companies around the globe.

New Capabilities: In 2011, PTI introduced smart NAND packaging with

8 stacked memory die and a controller in a 1.0mm thick package and drove the 4 die stack PoP top package used in high end mobile phones down to 1.0mm thickness to enable thinner phone profiles. PTI also installed and qualified 300mm copper pillar bumping, copper RDL, and WLCSP packaging in 2011. We began volume shipments of copper pillar flip chip parts with 50µm inline perimeter pitch using mass reflow for the lowest possible cost. We believe this is a first for the industry.

Future Outlook: PTI will continue to invest in TSV, silicon interposer, and 3D-IC stacking in 2012. We plan to qualify via-last middle-end-of-line (MEOL) early in the year and via middle MEOL shortly after that. Our 3DIC die stacking with micro bump interconnect and silicon interposer assembly is maturing and we expect to begin shipping production volumes in 2012. In conventional packaging, we plan to introduce more fine-pitch FC applications into production and deliver PoP packages to support the increasing data rates for mobile processors and modems.



Figure 4: Powertech Technology's headquarters

OSATs Look to Rebound in 2H12

Revenue Growth: "End products continue to have richer semiconductor content, more memory, more radios, more MEMS," says Joanne Itow. "Although the economy is still sluggish, electronic goods continue to be a priority on both consumer as well as business wish lists. Due to the floods in Thailand and the hard disk drive shortage, a surge in sales will occur in the last 2 quarters of 2012. Semico

is forecasting 10% revenue growth in 2012. This will translate into 11.6% wafer growth. Unit sales continue to increase. Semiconductor products such as MEMS, DRAM, Flash and communication will see double digit or high single digit growth in 2012."

Bill McClean, President at IC Insights, recently noted, "The growth of the IC industry in 2012 is forecast to be highly dependent on GDP growth. Near average 2012 worldwide GDP growth is expected to drive 7% IC market growth."

Unit Growth: Sandra Winkler, Sr. Analyst at New Venture Research, sees OSATS continuing to assemble and test more of the world's semiconductor packages. "OSATs collectively will have a unitary CAGR of 11.8% for the years 2010 through 2015. This compares with a CAGR of 7.5% for the total worldwide IC package unit growth for the same period," she says.

Capital Expenditure: Jan Vardaman, President of TechSearch International, says she expects OSATs to spend much of their 2012 CAPEX on the advanced packaging—WLPs, and flip chip bumping/assembly for a variety of packages including fan-out and conventional WLPs, PoP, and flip chip in CSPs including PoP.

Capacity Utilization: Walker anticipates, "Utilization rates for OSATS for 2012 will be very dependent upon package mix, and which products will use the various packaging schemes. Wire bonding utilization will be in the 70% range for the first half of the year. On the other hand advanced packaging, such as flip chip, will be near full utilization in the high 80% to low 90's."

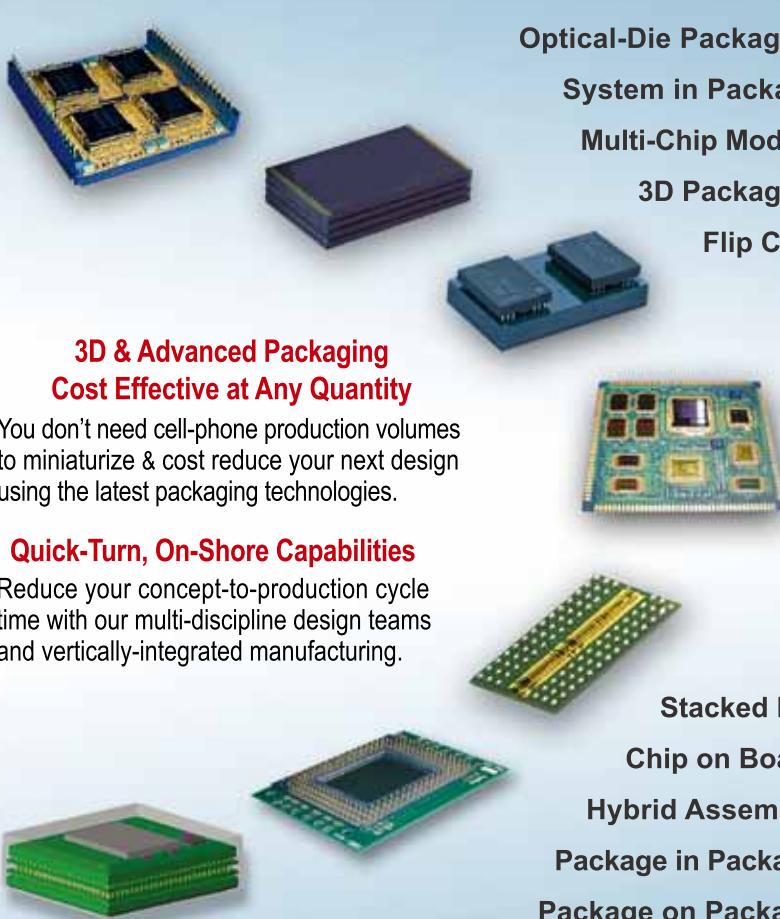
Growth Opportunities "Applications for higher growth will be smart phones and tablets. Slower growth will be in consumer (games) and PCs," says Walker. Vardaman agrees. "Wafer level packages will continue double-digit growth of 12.5% driven by strong growth in smart phones and tablets," she says. "IDC predicts that smartphone shipments will grow from 472M units in 2011 to 982M by the end of 2015. Shipments of tablets

will exceed 50M units in 2012. These products make use of PoP configuration where the top package typically contains wire-bonded memory and the bottom package contains logic such as a processor. Increasingly, the logic device in the bottom package is using

flip chip, including copper pillar. More than 500 million PoPs shipped in 2011 and the number continues to grow." 

Ronald Molnar of AZ Tech Direct, LLC may be contacted at rmolnar@aztechdirect.com.

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Microelectronic Packaging Dresden GmbH Grenzstrasse 22 Dresden 01109, Germany Tel: +49-351-213-6100 www.mpd.de	DE(1)	CL, CN PL, PN PC	WD, WT AS	AD, WB FC, UF GT, BA
Millennium Microtech Thailand* 17/2 Moo 18, Suwintawong Rd., Tambon, Saladang, Bannumprielu, Chacherngsao 24000, Thailand Tel: +66-38-845-530 www.m-microtech.com	TH(1)	CL, PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, ED WB, MP LP, HS
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Overcoming the Price Performance Barrier in Wafer Level Packaging Applications

By David Foote and Jack Zhao, Ph.D. [\[Nordson MARCH\]](#)

Wafer-level-packaging (WLP) has emerged as an attractive solution for chip-scale packaging because of form factor and cost attributes. Wafer level chip scale packaging (WLCSP) is completely assembled on the wafer prior to dicing, with an assembly that includes redistributed solder bumps, passivation and polymer layers. It is a true chip-scale packaging technology since the resulting packaging is practically the same size as the die. Likewise, WLP using fan-out reconstitutes the wafer form factor using known good die (KGD) mounted on a wafer sized substrate enabling the use of front end process tools and techniques. Regardless of implementation and due to economies of scale, packaging costs are minimized when compared to traditional packaging methods. However, cost reduction of front-end semiconductor processing tools needed for backside processes is an impediment.

WLP technology makes use of passivated wafers and/or reconstituted die to redistribute I/O for improved form factor and performance of the end product. Spin-on dielectrics are used to isolate the product's bond pads from subsequent metallization processes as well as act as a stress relief layer. These dielectrics are also used as masks for copper pillar and/or solder bump formation. Polyimides and poly-benzocyclobutene (BCB) have been used extensively while Polybenzobisoxazole (PBO) has been used more recently. Ease of process integration as well as thermal and mechanical properties drives product selection for these dielectrics. Photo-sensitive materials allow mask-less feature definition for reduced costs and leaner manufacturing flows. Higher

temperature processing requirements for lead-free applications also drive polymer performance with more stringent requirements. Processing challenges using these films involve adhesion to the substrate, de-scum of the patterned film, etching and/or stripping the polymer.

Other challenges include cleaning aluminum bond pads, modifying passivation layer on the wafer to promote adhesion, de-scum of residual photoresist, stripping photoresist for redistribution, and removing the contamination and residues prior to wafer bumping. Due to environmental issues with wet chemical processes, environmentally benign plasma cleaning processes have been the primary focus by WLP engineers. The remaining challenge is to implement cost-effective plasma solutions without hampering process performance.

Plasma is an electrically neutral, partially ionized gas mixture consisting of ions, electrons, free radicals, neutral byproducts, and photons. It is capable of both physical work via ion-assisted sputtering and chemical work through radical or byproduct chemical reaction. As a result, plasma can perform numerous surface modification processes including surface activation, contamination removal, crosslinking, etch by chemical reaction, and physical bombardment.

Plasma has been successfully used for pre-wire bond treatment for better bond reliability and yield,^{1,2} pre-mold treatment for enhancing interface adhesion, and surface modification for tailoring surface energy for fluid wettability and surface adhesion. It improves the pull strength and uniformity of wire bonds; increases fillet height and uniformity as well as increases underfill adhesion for flip chip devices; and alters

surfaces for better adhesion in mold and encapsulation processes³⁻⁵. This article discusses the usefulness of plasma for resist descum, metal oxide reduction, PBO film etching, roughening polyimide and show the effects of temperature on photo-resist etch processes.

Descum

Low-power oxygen plasmas are used to clean up the residues around the base of the resist patterns and conditions are set such that resist removal from the pattern is minimal. Process control and repeatability demand the etch rate and within-wafer uniformity of the descum process to be of the highest performance. The resist removal rate is not so critical for the descum process because the amount of film removed is on the order of 100nm or less. In situations where the oxidation of materials exposed during the descum process are concerned, the use of hydrogen chemistries are preferred. Hydrogen plasmas etch resist polymers similarly to oxygen plasmas but at slower rates.

One known tool's descum process is both repeatable and uniform, with within-wafer non-uniformity values consistently below 1%, 1σ (**Figure 1**). Using the



Figure 1: Nordson MARCH FlexTRAK™-WR plasma system

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identical hardware configuration with hydrogen chemistry, similar repeatability and uniformity values are found. The hydrogen etch rate is less than that of the oxygen process while still delivering within wafer non-uniformity values near 1%, 1σ as well. (Figure 2)

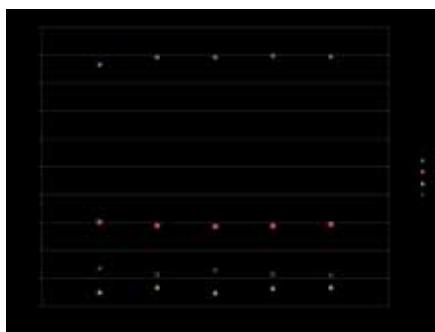


Figure 2: Hydrogen Oxygen descum comparisons.

Copper Oxide Reduction

Copper metallization in the form of pads and/or studs easily oxidize due to the thermal and plasma processes of WLP, and the oxide is a hindrance to subsequent metal interconnects or solder attachment. The uses of plasmas containing hydrogen mixtures in argon have been found to adequately reduce the copper oxides. The plasma process mechanism is twofold, taking advantage of the physical ion bombardment of argon ions on the surface and the chemical reduction process of hydrogen radicals. Figure 3 compares the total copper oxide thickness vs. plasma time using three concentrations of hydrogen in argon. The oxide is a mixture of both cupric and cuprous oxide and the reduction reaction drives the cupric oxide to cuprous to copper as it proceeds. This mechanism and metrology variations explain the slight increase in apparent

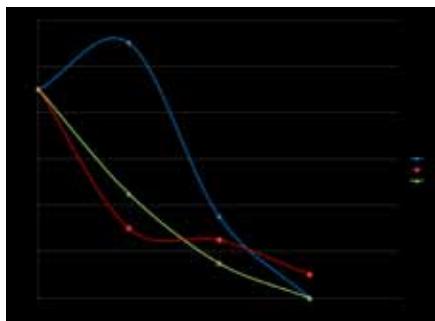


Figure 3: Plasma copper oxidation reduction.

oxide thickness as the reaction progresses. It is interesting to note that regardless of the hydrogen concentration, the total reaction times to reduce the oxides are similar. In similar experiments success has been shown using as little as 3% hydrogen.

PBO Etching

Polybenzobisoxazole (PBO) films are photo-definable stress buffer films used in WLP due to their optimum mechanical properties, low moisture uptake, and because they can be cured as low as 200°C. PBO films are photo-defined and the images are developed using aqueous chemistries. A plasma descum is required to remove the residuals following the develop process. The etch rates and within-wafer uniformities for descum of the PBO are comparable to production-proven resist descum applications (Figure 4). The descum process temperatures are typically maintained at room temperature to maximize process control uniformity and repeatability. High temperature descum processes are not able to maintain the tight controls required so as to maintain the pattern integrity.

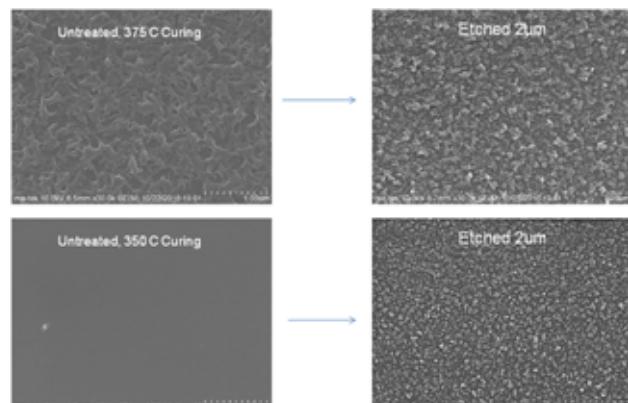


Figure 5: Effects of cure temperature on surface roughness both before and following the plasma treatment process.

was to increase the roughness enough to increase the surface area but not so much that interlayer leakage became a problem due to pinholes in the film.. It is important to understand the interactions between the cure and etch in order to optimize the integration resulting in the best metal adhesion without the pitfalls of leakage.

Temperature Effects of Resist Etch Rate

Descum requires excellent uniformity while etch rate is not critical. The opposite is true when it comes to resist strip applications. Back-end systems optimized for descum uniformity can be upgraded with the addition of wafer heating to enhance the rate of bulk resist strip processes. Figure 6 shows the etch rate enhancement by heating the wafer from room temperature to 130°C.

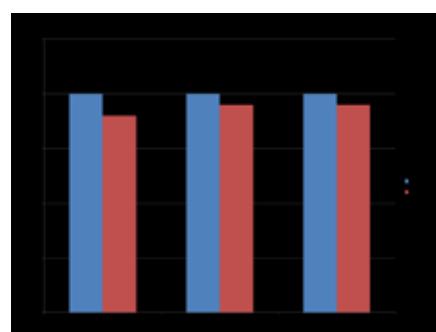


Figure 4: PBO vs. resist descum etch.

Polyimide Roughening

The adhesion of sputtered metals to the surface on the polyimide is challenging without some form of surface treatment. Oxygen plasmas will etch the polyimide films and enhance their roughness. Surface roughness of

Cost of Ownership Considerations

WLP is attractive due to the economies of scale of assembling packages by the hundreds or thousands at a time; and also because processing equipment is readily available from the wafer-front end fabrication facilities. However, processing requirements in the front-end are more stringent than the back-end because features are measured in the tens

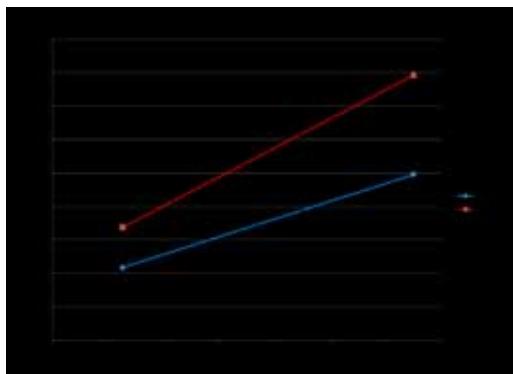


Figure 6: Etch rate enhancement by heating the wafer from room temperature to 130°C.

of nanometers rather than tens of microns. The use of front-end process hardware for backend applications is overkill and the associated costs are a deterrent. Front-end process equipment costs range from \$1M to \$5M or more. It is imperative for the WLP community to develop alternative hardware offerings that achieve process requirements for the backend yet are not cost prohibitive.

Conclusions:

WLP is an increasingly popular packaging technology due to its cost and form factor benefits. The wafer form factor allows leveraging of front-end processing technologies for back-end packaging applications. The costs associated with front-end processing platforms can be prohibitive for backend applications but there is equipment designed specifically for the back-end that alleviate those high costs. ^{3,4}

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(continued from Page 25)

solutions, advanced functionalities are also integrated on package or module level using established technologies. Either several components can be integrated into a single molded package or one or several unmounted components can be embedded in a PCB or another type of substrate. Development to date has demonstrated that both passive and active components can be integrated. The approach promises higher integration densities, improved RF and thermal properties and increased reliability. Depending on the assembly and supply chain, manufacturing costs may also be reduced. ^{SP}

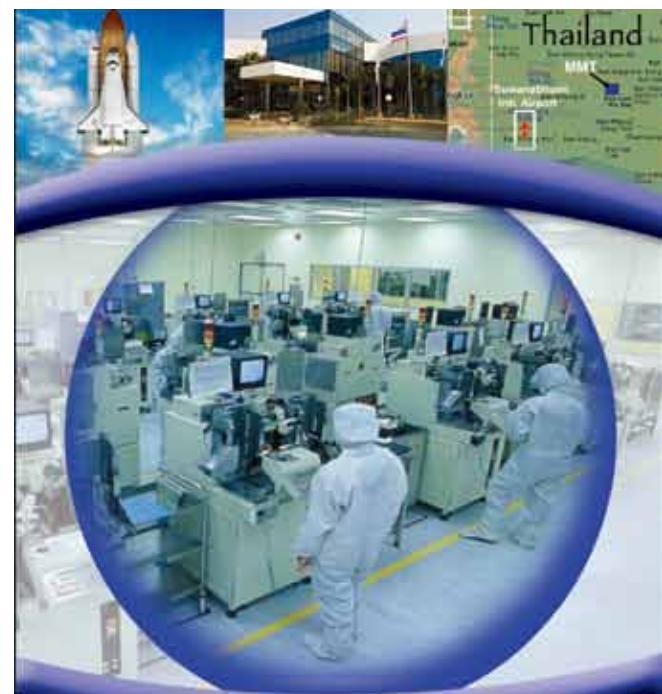
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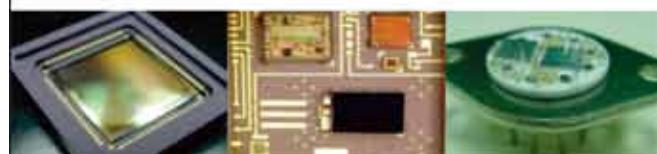
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INTERVIEW

Interview: Indium Corporation's Dr. Andy Mackie Talks Shop about Processes and Materials

By Chip Scale Review Staff



Last year, semiconductor packaging materials was a \$22.8 billion market, and according to a report from SEMI and Techsearch International, it is expected to grow to \$25.7 billion by 2015, with the emphasis on ever-smaller feature sizes, ultra-thin wafers, and 2.5D and 3D packaging. To find out more about how next-generation materials are developed, *Chip Scale Review* talked to Dr Andy Mackie, Global Product Manager for the Semiconductor and Advanced Assembly Materials division of Indium Corporation, based in Clinton NY.

CSR: Can you explain why semiconductor materials play such a vital role in the quest for smaller, cheaper, faster device packages?

Mackie: First of all, I think the ‘smaller, faster, cheaper’ mantra isn’t really the case for consumer devices anymore. ‘Mobility, customizability and coolness’ is really the trend. Quality and consistency of semiconductor assembly materials are very important. Fluxes, bond-wire wire, solders, polymeric materials, and emerging nanotechnology-based materials are becoming critical for enabling these cooler devices. “Cooler” should also be taken literally; reduction of energy consumption and thermal management is also critical. Materials have to be semiconductor grade quality and enhance reliability.

CSR: How are today’s packaging materials different than those of 10 years ago? Are materials becoming more critical to the process?

Mackie: As a supplier, we are seeing a smorgasbord of challenges: from the old lead-free (Pb-free) requirements; to halogen-free; to phosphorus- and antimony-oxide-free (for overmolding

compounds); and low and ultra-low alpha (ULA) particle requirements because the closer assembly materials come to the chip surface, the greater the chance of altering the transistor state. Our customers want to lower their costs as well. As a supplier, we have to manage the supply chain and prove it is free of potential human rights violations in tantalum, tungsten, tin and gold (TaWSnAu), as defined by the Congo Conflict Minerals Act.

Changes in materials can not be made without effects on functionality. One of our biggest customers recently told us that they were pulling back from a “totally halogen-free” drive because the materials were simply not as effective. It is therefore important to manage our customers’ green requirements against pragmatic considerations, and each customer often has their own set of criteria, which is sometimes complicated by contradictory standards. For “halogen-free” at least with the next version of the JEDEC/EIA JS-709, we will see this pragmatic document giving a “Low Hal” definition that the entire electronics industry can agree on.

CSR: What is the role of a Product Manager at a materials manufacturing company in handling these issues?

Mackie: For me, as Product Manager at a specialty materials company like Indium Corporation, it’s more like drawing on sets of different disciplines in my “mental tool kit”, whether it is college training, personal experience, personal interaction, or understanding different cultural business practices. In addition to overseeing product development from a specification viewpoint, I handle price management from a P&L perspective and might end up standing toe to toe with a customer in Asia negotiating over price increases necessitated by the customer’s emerging quality needs. I also contribute to product marcom, working with the marcom team to draw up collateral material such as product brochures, data sheets, visuals for a tradeshow, feature/benefit PowerPoint® presentations, and even blogging about new materials. I also handle some manufacturing concerns; for example with a material that requires a new manufacturing procedure, or a new set of quality criteria. I will often be the one who interacts with the standards organization or a specific manufacturing or test equipment vendor. In any one day, I’m drawing from a plethora of different skill sets, always while trying to keep my sense of humor intact, of course.

CSR: What comes first, the process or the material? In other words – how do you identify the need for a new product?

Mackie: Usually, the process and reliability needs of the final assembled unit are the primary drivers; however, with emerging technologies, there is a lot of iteration between materials and processes. We are in some exciting times:

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with 2.5D and 3D now out of the lab and hitting the production floor, new and emerging assembly processes are driving the need for new materials, and other new materials are also allowing the extension of established assembly technologies into smaller pitches.

We are seeing a lot of simultaneous changes: 14nm processes are coming out of the lab and ramping up to production. Thinned wafers (down to 20µm or less) will dominate the market by 2016, and are becoming mission-critical even in some power semiconductor applications. What we have now is a “perfect storm” of thinned wafers; wafer- and chip-stacking; fragile ultra low-*k* dielectrics; finer pitches; the advent of 450mm wafers and so on. Add into the mix the need for reliability of the final component, and you have a complex challenge ahead of you.

We work with customers, equipment suppliers, and industry organizations on a holistic basis. It's important to understand the process, and if you want to become the supplier of choice, you need to work alongside all of these guys. With emerging technologies, there's ignorance across the board about which is the best process. Materials suppliers, equipment vendors and customers are all scratching their heads trying to figure it out, and only together can we come to a final answer.

CSR: What are the steps involved, from R&D to product introduction, in developing a new material and what role do you play as Product Manager to bring this to bear?

Mackie: It's my job to identify the critical customers and turn specific customer requirements into measurable, or at least verbally-well-defined, parameters. It is important to define the parameters of functionality; What does the material look like? How does it cure, reflow, and perform? What does it need to interact with? What are the limitations to the material sets defined by customer standards? I make sure we're meeting

all the reliability requirements; assist in the scale-up, pricing, and data sheets; and promote the product by blogging or writing articles for publications. I also work with industry thought-leaders like Dr. Ning-Cheng Lee to define the critical roadmap for these materials. I have had the personal advantage of working at three companies that span microelectronics manufacturing, beginning with Cookson, where I worked in R&D and technical services in the surface mount technology (SMT) world, focusing on solder paste. At Praxair, I developed an understanding of semiconductor assembly, working on ultra-high purity gas supply. Finally, at Indium Corporation, I guide the company into the “in-between” world of semiconductor assembly, with the incredible advantage of being able to see things from both the FEOL/BEOL perspective and the board-level reliability aspects.

CSR: In your opinion, what are some of the most significant material advancements that have enabled next generation packaging technologies?

Water-soluble bump-fusion fluxes; void-eliminating flip-chip fluxes; ultralow residue or near-zero residue (ULR/NZR) no-clean fluxes; LA/ULA solder pastes and fluxes; emerging nano-particle based conductive materials; high-melting Pb-free solder pastes... oh my!

Add to this the simple fact that all of this has been done while meeting

both emerging quality and legislated/environmental needs, as often defined uniquely by our myriad customers.

CSR: Looking ahead, do you have any game changing materials in the hopper that you can talk about?

Mackie: We have some very interesting technologies in the hopper, in regular flip-chip and 2.5D and 3D assembly, as well as power semiconductor assembly. We are positioned for future growth with at least three major upcoming mobile technologies, with which we are very pleased.

Suffice it to say we're very excited about the future of semiconductor packaging materials, and we believe we are uniquely positioned to assist our customers in bringing next-generation devices to market. ☺

The advertisement features a large image of the PE-50 plasma etching system, a white rectangular unit with a control panel featuring a digital display and several buttons. The background is green with white text. At the top, it says "PLASMA ETCH" and "PROGRESS THROUGH INNOVATION". Below that, it says "AFFORDABLE PLASMA ETCHING SYSTEM". A sub-headline states "THE PLASMA ETCH, INC. PE-50 IS OUR LOWEST PRICED PLASMA SYSTEM". Another section highlights "SURFACE ENERGY MODIFICATION WITH PLASMA TREATMENT YIELDS IMPROVED MARKABILITY, ADHESION AND EASE OF ASSEMBLY WITH A LOW ENVIRONMENTAL IMPACT". A third section mentions "REMOVES ORGANICS AND IMPROVES BONDS". To the right, the model name "PE-50" is displayed above the text "STARTING AT \$ 10,950". At the bottom right, it says "TO LEARN MORE VISIT OUR WEBSITE OR CALL US TODAY!" followed by the website "WWW.PLASMAETCH.COM" and the phone number "775.883.1336". The address "3522 ARROWHEAD DRIVE CARSON CITY NV. 89706" is also listed.

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