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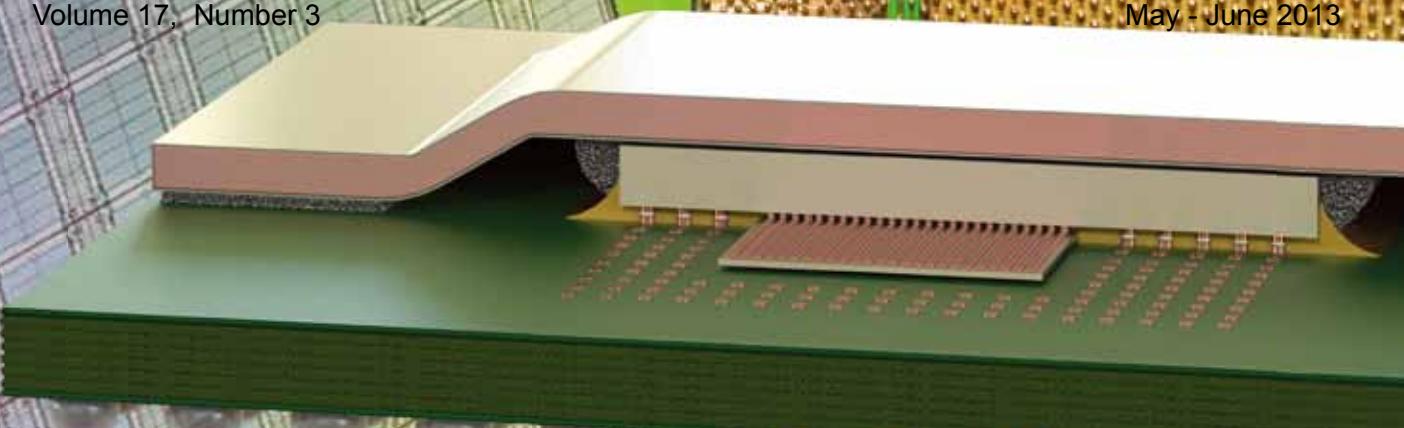
REVIEW

ChipScaleReview.com

The International Magazine for the Semiconductor Packaging Industry

Volume 17, Number 3

May - June 2013



Cover Feature

Realizing 3D IC Integration with Face-to-Face Stacking

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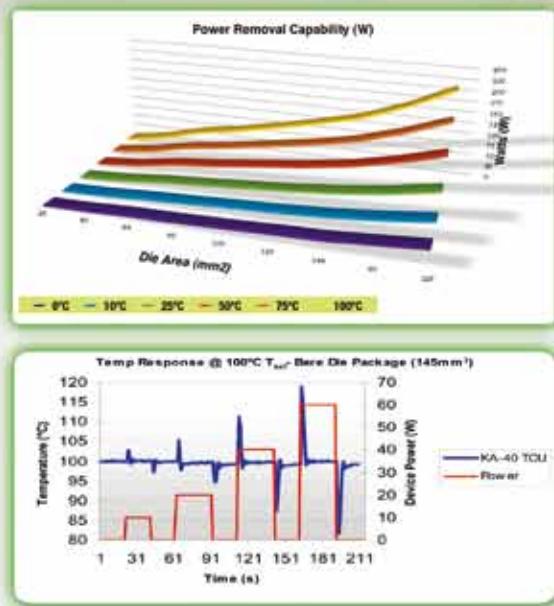
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The cover photo shows Altera's Stratix® IV 40-nm wafer and a close-up of a Stratix® V GT 28-nm die. Stratix® devices are high performance, high density FPGAs. The illustration, showing Amkor's POSSUM™ packaging approach, depicts the FPGA flip chip mounted to the substrate with a thinned ASIC attached underneath. The two devices are assembled face-to-face through a 40µm array of Cu pillar micro-bumps. The ASIC is joined to the substrate through thicker Cu posts + solder microballs at a conventional solder bump pitch.

Chip Scale
REVIEW

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

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FROM THE PUBLISHER



The Road Ahead

I

In this issue, we present another compilation of sharp editorial that showcases essential information for the professionals of the semiconductor packaging industry. Our cover story presents the topic "Realizing 3D IC integration with Face-to-Face Stacking." This alternative approach to a stacked chip-on-chip arrangement is a must read.

From the leading institutions of the academic world, our contributors deliver a double feature of articles on integrated silicon photonics fabrication and systems scaling for smart mobile systems. We also investigate the cleaning (and reliability) challenges presented by the tight gaps beneath components. WLCSP reliability, as it is impacted by solder joint geometry optimization, is evaluated in a series of experiments.

We all need test and burn-in sockets, so we investigate what they are by interviewing a general manager of a socket manufacturing company with well-known Swiss precision, how we can apply test sockets for MEMS, and where to find them with the International Directory of Test & Burn-in Socket Suppliers.

This issue of Chip Scale Review will be widely circulated at ECTC 2013, May 28th – May 31st in Las Vegas, Nevada, as CSR is once again the official media sponsor for that event. Chip Scale Review staff will review the sessions and meander the exhibits with our reviews presented in the following issue of CSR which will be available at SEMICON West in July.

It is time to consider your conference and exposition schedule by looking into these following events, the upcoming ECTC, SEMI's Networking Day at Nanium, June 27, in Porto Portugal, and as mentioned, SEMICON West. The International Wafer-level Packaging Conference (IW LPC) is a must attend event in November. Make your plans, register, and make it happen!

The key objectives of CSR are to bring our loyal readers the latest in packaging innovations, both from a technical and business perspective, and to give global visibility to our advertisers. To all the product marketing, sales managers and corporate executives that benefit from our content delivery in this industry, reach out to your CSR sales representatives and support the publication that supports your business.

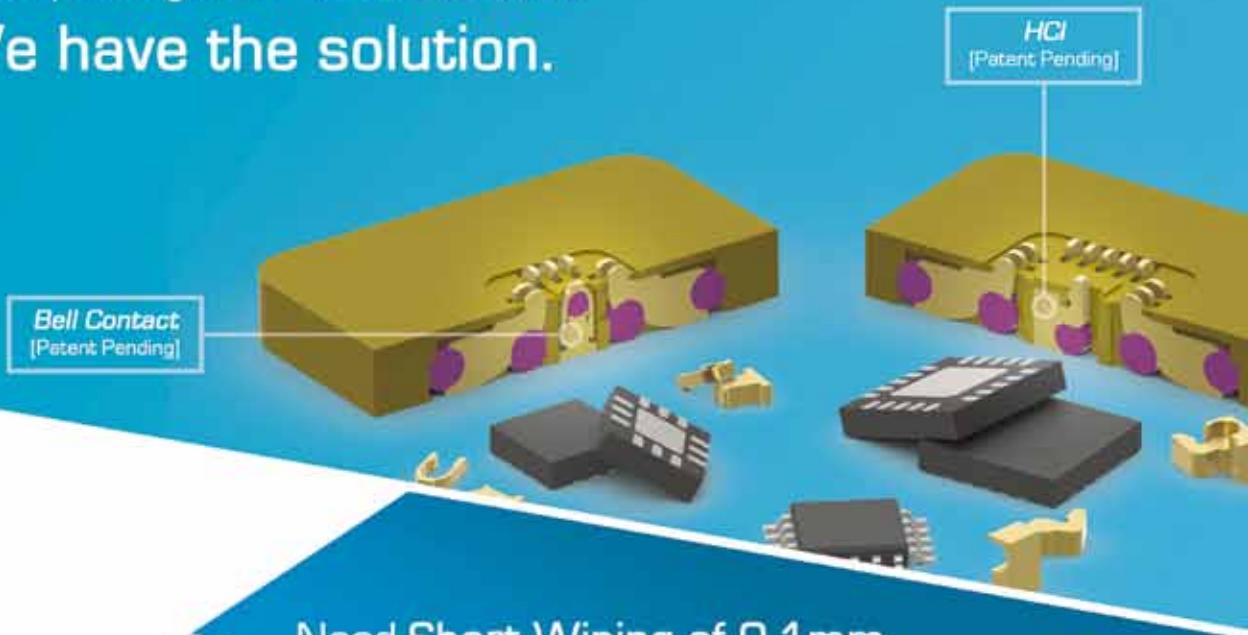
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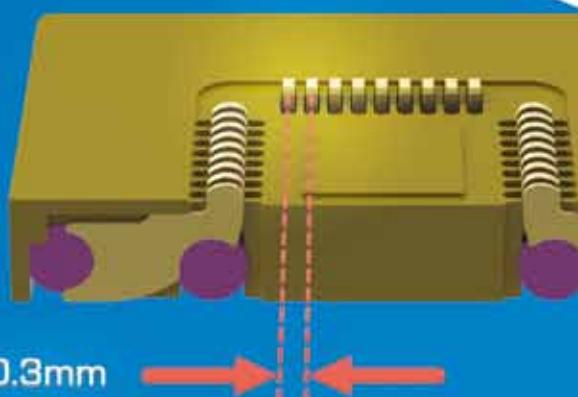
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MARKET TRENDS



Memory Packages Adapt to Demand Shifts

By Jim Handy *[Objective Analysis]*

The ballooning bandwidth requirements of today's processors are being dealt with by increasing the number of buses feeding the CPU. Two buses and even three-bus systems are becoming increasingly common. What is not obvious is that the size of the memory in PCs is limited by economics: The PC's main memory doesn't double or triple every time a new bus is added, it has to remain at the same size to be price-competitive with lower-bandwidth PCs. The system satisfies its bandwidth need by using a larger number of packages with very low density (i.e., inexpensive) chips inside. This causes lower-density DRAM chips to remain in the market longer than they have in the past. As the price of the lower-density chips decreases, the overall average selling price (ASP) of DRAMs slides (**Figure 1**) putting phenomenal pressure on the price of DRAM back-end processes (package and test) as these two elements contribute to an increasing share of the total cost of the memory system.

Meanwhile, the opposite has been occurring in the second-biggest memory market – NAND flash. The average memory size of NAND flash applications has been increasing faster than the density of the chips in these systems, yet the form factor of the system (whether a phone handset or other mobile device) has been steadily shrinking. Thanks to these two conflicting trends, NAND flash makers have had to stack chips in increasing numbers to satisfy consumer demand for mushrooming flash capacities in shrinking product form factors. Two-chip stacks, which were uncommon as

recently as 2000, have been superseded by 4-die and 8-die packages. Although 16-die packages ship today, the 8-die stack is the tallest stack currently shipping in volume, but that might change over the next few years.

Naturally, since these are consumer products, there is significant pressure to keep prices down. NAND makers have found a way to drive all of the cost out of these stacked parts, thanks to a lot of challenging work performed by packaging engineers. I find it amazing that an 8-high stack of 16Gb NAND dice commands no price premium over eight individually-packaged 16Gb NAND chips, or four 2-die stacks, or even two four-chip stacks. In flash cards, such stacks now very commonly include eight NAND chips plus a controller.

All this has been given a more pronounced impact by the fact that buyers appear to be putting off PC purchases in favor of mobile devices such as smart phones and tablets. Mobile devices, in turn, are usually NAND rich and use only the smallest DRAM. The market is undergoing important changes that will create even greater turmoil for chip makers than they have witnessed in the recent past.

Today's technologies have gone about as far as they can, though. Sixteen-layer NAND stacks have low yields that cannot reach price parity with 8-chip stacks. Today's DRAM packages

can't support significant increases in signal frequencies and the addition of buses multiplies the capacitive loading on the processor and drives up power dissipation. The market will have to undergo a revolutionary conversion over the next few years.

The shifts the market has recently undergone pale in comparison with what's coming up. Some exciting new packaging technologies are being developed that will provide more bandwidth and denser products while

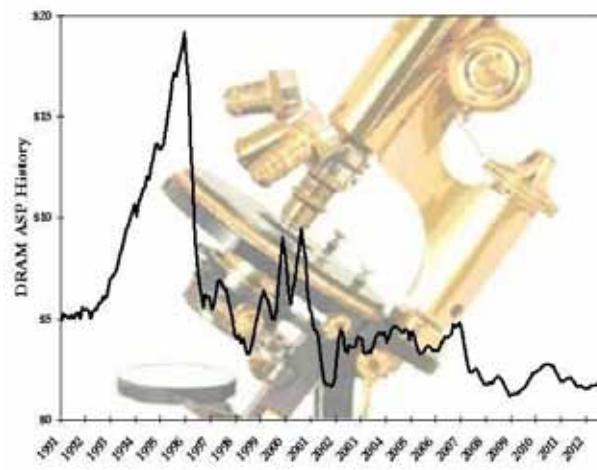


Figure 1: DRAM average selling price is steadily decreasing.

the market for these chips will be undergoing very dramatic changes. Let's see what is ahead in the world of memory packaging.

What Does the Future Hold?

Three important emerging trends will drive even more extreme packaging over the longer term: 1) Through-silicon vias; 2) Hybrid Memory Cube; and 3) NAND adoption in PCs. Let's examine

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each of these in turn.

Through-Silicon Vias. Through-silicon vias, or TSVs, hold the promise of simplifying inter-chip bonding for stacked dice. It's not difficult to understand that the sheer complexity of bonding a 16-die stack using bonding wires alone poses great manufacturing challenges that lead to yield losses.

By moving to TSVs, all wire bonding of the upper chips can be eliminated, and this is expected to significantly improve yields for die stacks of increasing heights.

Although today TSV technology is not widely used, and presents new challenges of its own, the same was true of the standard 2-die MCP (multichip package) in the middle 1990s. This is a technology that should mature and develop to drive out all cost and yield challenges over time. It is unclear how high of a stack can be economically manufactured using TSV technology – we may see stacks of 100 chips or more over the long term. Imagine the impact this will have on the density of a NAND package.

Hybrid Memory Cube. Since the TSVs mentioned above can be used for inter-chip signaling that doesn't need to exit the package, chip designers can design I/O pins that don't have to drive a PC board trace or be handled during board assembly. This means that high-speed drive transistors can use low currents (making them much smaller than today's I/O transistors), and that there does not need to be space-consuming electrostatic discharge (ESD) protection on these I/O pins. In addition, the TSVs replace bulky bonding pads, further reducing the size of the chip's I/O.

The inventors of the hybrid memory cube (HMC) took this opportunity to drive an architecture that is likely to be adopted in all higher-end computing systems over the longer term. The HMC stacks a number of DRAM chips atop a logic die; the logic die is the only

chip that communicates external to the package. This means that this is the only device that must have high-current drive transistors with ESD protection. Furthermore, it is manufactured using a logic, rather than a DRAM, process – DRAM processes aren't good at driving high currents, so high-current DRAM transistors are much larger and more expensive than their logic-process counterparts.

But there's more to the story! Because the I/O drivers on the DRAM chip are now much smaller than those of a standard DRAM, there can be more of them without penalizing die area. Without large high-current transistors, ESD protection, or bonding pads, these I/Os are so small that today's HMC prototypes use thousands of DRAM I/O pins to communicate between the DRAMs and the logic chip, increasing bandwidth substantially.

The HMC uses a point-to-point external signaling interface to communicate with the processor. This gives the system designer considerably more control over bus capacitance than exists in today's DIMM-based systems, and this capacitance is also much lower. This allows the bus to be run at vastly higher frequencies than can be done in today's systems, which should help the memory keep up with the ever-accelerating processor bus. Over time, Objective Analysis anticipates that the HMC could be used for all DRAM in PCs and servers.

NAND Adoption in PCs

In 2011, Objective Analysis published a report: "How PC NAND will Undermine DRAM." Through a series of nearly 300 benchmarks we found that (after a certain minimum size DRAM was achieved) one dollar's worth of NAND flash improved a PC's performance more than one dollar's worth of DRAM. This is something that the IT community has known for years. Data center managers routinely

use solid-state drives (SSDs) as a way of reducing their DRAM requirements, cutting both cost and energy consumption at the same time.

Although PCs have not yet adopted this trend, it will occur over time, with DRAM main memory sizes stagnating and new NAND dual in-line memory modules (DIMMs) replacing the smaller SSDs now commonly seen in Ultrabooks. Users who wish to improve their system's performance will simply upgrade their NAND DIMM. As this happens, DRAM will migrate away from a removable format and will be soldered down. The HMC is very likely to become the standard way in which DRAM is built into the PC. DRAM will become a cache to the NAND main memory.

Summary

We have seen important changes in memory packaging technology, moving from single-die packages to multiple-die packages in NAND while experiencing a shift from low package counts to high package counts in DRAMs. Both have put significant pressure on packaging costs that have led to important innovations.

Although we are now approaching the limits of today's technologies, new approaches in the form of TSVs and the HMC, are on the horizon that should move us well past today's limits allowing packaging advances to propel the two disparate goals of increasing bandwidth for DRAMs while increasing NAND flash package density faster than Moore's Law supports. 

Acknowledgment

Ultrabook is a trademark of Intel.

Biography

Jim Handy received his Bachelor's in Electrical Engineering from Georgia Tech and an MBA from the U. of Phoenix; he is a Director at Objective Analysis; email Jim.Handy@Objective-Analysis.com.

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GUEST EDITORIAL



Systems Scaling for Smart Mobile Systems Requiring a New Packaging Platform

By Prof. Rao R. Tummala [3D Systems Packaging Research Center, Georgia Institute of Technology]

Transistor scaling, starting with the invention of the transistor in 1947, made electronics the largest single \$1.5T global industry serving a variety of individual industries that span computing, communications, consumer, automotive, bioelectronics and others. The basis for this industry is a result of singular focus in transistor scaling, leading to a 5B-transistor chip, involving dozens of semiconductor companies around the globe. But the electronics landscape is changing dramatically, driven by a new industry that integrates all these individual industries into so-called “smart mobile systems” and promises to perform every imaginable function in the smallest size and lowest cost that almost every global person could afford. Such a new frontier, however, requires revolutionary technologies referred to as system scaling, in contrast to transistor scaling during the last 60 years. Smart mobile systems are expected to drive unparalleled electronics technology paradigms in system miniaturization, functionality, and cost. These system scaling technologies are many that need to be explored, developed, integrated, interconnected, tested and manufactured. These include new electrical, mechanical and thermal designs, new system substrate materials and processes, integration of ultra-thin actives, ultra-thin passives, miniaturized and innovative thermal structures, thin-film power storages such as batteries, and interconnections between all of these. **Figure 1** illustrates the current size scale in millimeters, showing the

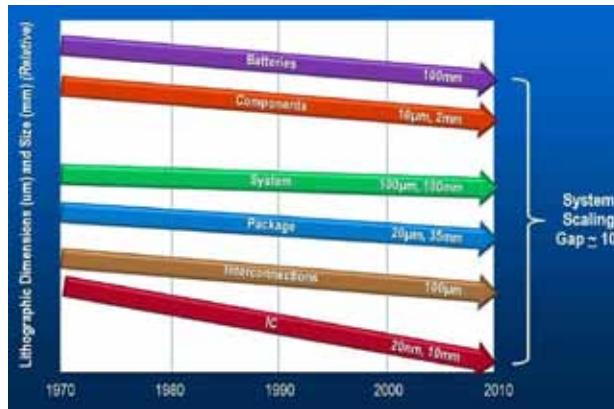


Figure 1: System scaling gap from transistor scaling at 20nm node to system scaling to 100mm size.

10^6 gap between transistor scaling and system component scaling.

System Scaling Vision of Smart Systems

The Georgia Tech PRC vision is to explore system scaling technologies from current milli- to micro-scale in the short term and to nano-scale in the long term, thus providing a revolutionary path to milli- to- mega-functional smart mobile systems, as implied in **Figure 2**.

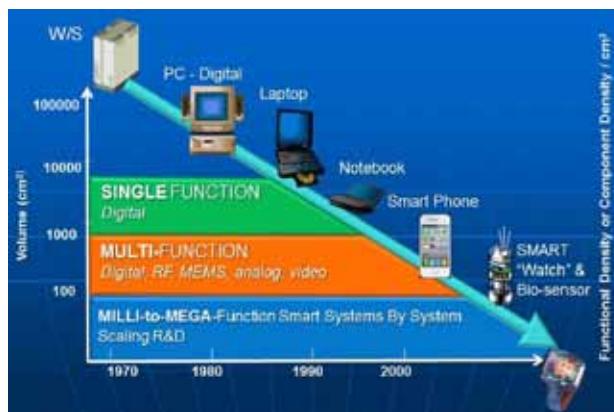


Figure 2: System scaling vision from milli-to mega-functional smart systems.

Such advances will lead to unparalleled circuit and system functions that range from digital, analog, power, RF, wireless healthcare, bio, MEMS and network sensors.

Current hardware approaches involve packaging of individual and stacked ICs that range from processors, memory, RF, MEMS and sensors as well as

passive components and batteries. While some of these are packaged as two-dimensional MCMs and 3D wire bond and stacked packages, there is very little system scaling. As such, mobile system companies see an eventual limit to functionality driven by the thickness limit of about 6000 μm, as shown in **Figure 3**. Such a limit doesn't allow other functions requiring other ICs to be added. This limit can be largely eliminated by changing the current hardware platform that involves packaging of ICs on flexible or rigid organic packages and organic system boards, which present four main limitations for smart systems of the future: 1) I/O pitch to less than 50 μm with lithographic ground rules below 5-10 μm line lithography, 2) thermal performance, 3) mismatch in temperature

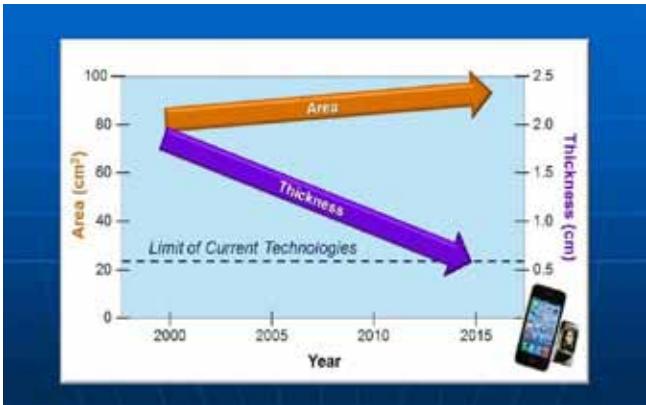


Figure 3: Functionality limited by thickness of current system scaling technologies (Courtesy of Qualcomm).

coefficient of expansion (TCE)-driven, and moisture-driven reliabilities, and 4) warpage, as these organic packages are miniaturized in thickness below 100 μm , as ultra-thin packages. The I/O pitch and line lithography limitation

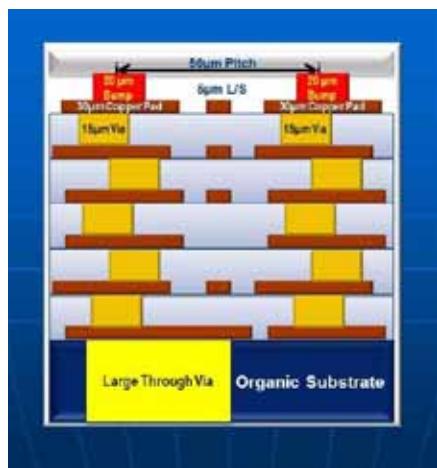


Figure 4: Area array I/O pitch of a) current organic packages at 120 μm pitch and b) low TCE organics at 50 μm pitch.

is a result of via on top of via misregistration from layer to layer due to the visco-elastic nature of polymers as these are processed at or above their glass transition temperature and thus are expected to be limited to about a 50 μm area array pitch, as shown in **Figure 4**. The thermal conductivity of polymers is about two-three orders of magnitude less than silicon. The mismatch in TCE between Si and organic is huge, creating

stresses on both the interconnections and the ultra-low-k on-chip dielectrics. The warpage is due to many factors including low modulus. Inorganic packages made out of glass or silicon address all these fundamental problems and thus extends I/O pitch much below 50 μm to as much as 10 μm . The new generation

Summary

Georgia Tech proposes to offer an industry consortium, involving the entire global chain for R&D and manufacturing, with a focus on many system scaling technologies that include the electrical design of glass, silicon and organic interposers for power, signal, noise and bandwidth, mechanical design for warpage and reliability, panel-based low cost glass, organic and polysilicon interposers and packages, 2-5 μm large area lithography and wiring layers, 10-30 μm pitch off-chip and low temperature Cu-Cu interconnections, silicon, organic and glass package-to-board level surface

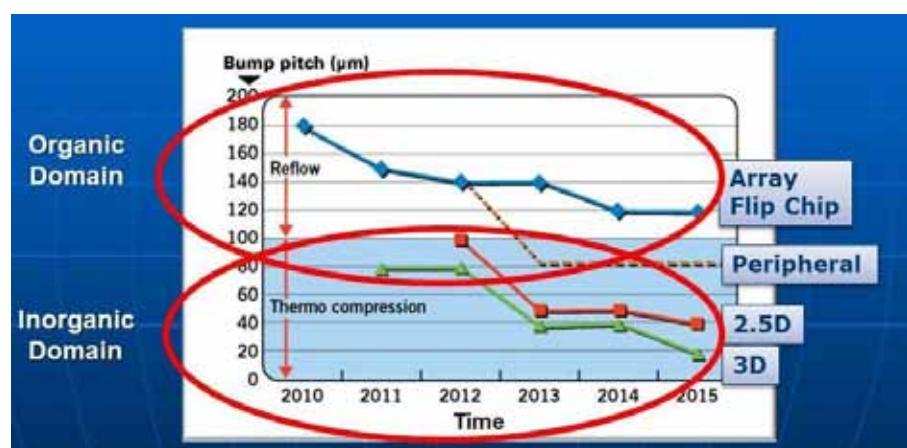


Figure 5: I/O pitch need and organic vs. inorganic regimes for emerging 2.5D and 3D packages(Courtesy of Globalfoundries).

of low TCE organic laminates, however, offer an opportunity to extend the I/O pitch from 225 μm pitch in 1987 to their current value at 120 μm pitch and, in the near future, to about 50 μm pitch. **Figure 5** shows two regimes therefore, one with extending flip-chip with organics, and the other with inorganic platforms in extending I/O pitch to new levels, much below 50 μm . These can be combined appropriately and selectively with ultra-thin and special component technologies made of polymers for dielectrics, liners and stress-relief members; nanomagnetics for antennas and power components and ultra-high surface area electrodes, along with high-permittivity dielectrics for capacitors.

mount technology (SMT) assembly, 3D glass photonics, 3D integrated passive and active components, among others. Georgia Tech's PRC involves about 20 cross-disciplinary faculty and dozens of graduate students.

Biography

Rao R. Tummala received his PhD in Materials Science and Engineering at the U. of Illinois and is the Joseph M. Pettit Endowed Chair in Electrical and Computer Engineering and the Director of the Packaging Research Institute at the Georgia Institute of Technology. He was an IBM Fellow prior to Georgia Tech; email rao.tummala@ece.gatech.edu

INDUSTRY NEWS

SEMI Europe Networking Day to Focus on Embedded Packaging Technologies



SEMI Europe announced a new Networking Day focusing on embedded packaging to be held on June 27, 2013 in Portugal. Hosted by Nanium, in Vila do Conde (Porto, Portugal), the event will feature speakers from companies involved in fan-out wafer-level packaging (FO-WLP) and in embedded die in laminate substrate.

Driven by consumer markets and mainly by smartphone products, embedded packaging solutions provide the best power, performance, and area system tradeoff by integrating more functionalities into a smaller and thinner package. With annual growth forecast at more than 25% by market analyst firms such as Yole Développement, these technologies are already implemented in high-volume cellular phones and are critical for enabling future innovative solutions, including 3D packaging solutions.

The Networking Day will combine presentations from companies that influence the industry and offer unique add-ons such as the visit of Nanium's clean room, the largest FO-WLP 300mm facility worldwide, and several networking opportunities including the Speed Networking Session and social evening events. Speakers from ASE Group (Taiwan) and STMicroelectronics (Switzerland) will keynote and share the latest results of their work in embedded packaging and their respective strategies. ASE Group was a very early adopter of the first-generation of FO-WLP (licensed eWLB technology developed by Infineon), starting with 200mm capabilities, and

now very active in embedded die in substrate. STMicroelectronics, one of the founding members with Infineon and STATS ChipPAC, of an R&D alliance in Singapore to advance the eWLB platform back in late 2009, developed a wide range of technology options around FO-WLP to serve its various product groups addressing multiple market segments.

Presentations from TechSearch (USA) and Yole Développement (France) will describe the technology landscape, market and main players. Additional speakers from Intel Mobile Communications, AT&T, and NXP are confirmed.

"We are pleased that we developed such a strong lineup of speakers from the main players designing, manufacturing and selling embedded packages all over the world," said Heinz Kundert, SEMI Europe President. "We are still at an early stage, many additional business opportunities in embedded packaging are still upfront for equipment and materials companies. Embedded packages have the potential to become the new packaging platform beyond the BGA solution."

The full event program is online and registration is open. Anyone involved in advanced packaging is invited to register. The Networking Days are a SEMI Europe initiative to support start-ups, SMEs, laboratories and large companies and to get "up to date" on hot topics that appeal to people across the semiconductor supply chain. SEMI Networking Days, held on a quarterly basis in industrial sites, are prime events to connect with the people who influence the industry and to initiate preliminary partnership and business relationships. The Networking Days are open to anyone and free of charge for SEMI member companies. For more information about the event, please visit www.semi.org/eu/node/8481 or contact Yann Guillou in the SEMI Europe

Grenoble Office (yguillou@semi.org).

SEMI: Memory, Foundry, and LED Markets Drive Fab Spending in Southeast Asia

In early April, SEMI reported that increased spending in NAND and flash by Micron, LEDs by Philips and Osram, and continued investments by Globalfoundries, will create new opportunities for equipment and materials suppliers in Southeast Asia. The trade group noted that, for the Southeast Asia region, capital equipment investment will see some pickup in the second half of 2013 followed by a strong recovery in 2014. Overall, front-end fab equipment spending is expected to double next year from \$810 million in 2013 to \$1.62 billion in 2014. Foundry and memory are the two major sectors that invest most in the region. The Globalfoundries expansion plan at Fab 7 will be completed by mid-2014, while UMC continues to upgrade its Fab 12i capacity to the 40nm process.

The Southeast Asia region's capacity growth for front-end fabs shows a 2% increase this year and an expectation of higher growth, 8%, in 2014, exceeding overall global capacity growth of 5% according to the SEMI World Fab Forecast. The growth will mainly be driven by memory sector, specifically from NAND flash capacity as Micron gears up for further expansion at its Singapore NAND flash facility next year, plus ongoing capacity conversion from DRAM to NAND flash at Fab 7 (Tech). Singapore is emerging to become the third largest NAND flash manufacturing country in the world by the end of 2014. The conversion and the expansion projects will drive related semiconductor investment in the region in 2013 and 2014.

For the assembly and test sector, Southeast Asia has long been the focal point of the industry with a large installed capacity from both IDMs and

OSATs. This position contributes to the region being the largest packaging materials consumption market in the world, representing a market size of \$6.6 billion in 2013 and \$6.8 billion in 2014. The region's back-end equipment investment remains significant with over \$1 billion spending each year throughout 2012 to 2014, accounting for about 17% of worldwide share according to SEMI's WWSEMS.

Aside from manufacturing capacity, the Southeast Asia region is now extending its value proposition to IC design and R&D areas with more joint development projects between multi-national corporations (MNC) and local institutes. SEMI expects to see a more robust semiconductor ecosystem arise from the region as a result of these endeavors and as companies seek ready

access to customers throughout Asia-Pacific and South Asia.

Currently, Singapore has 14 wafer fabrication plants, including the world's top three wafer foundries. Singapore also has 20 semiconductor assembly and test operations, including three of the world's top six outsourced assembly and test companies. There are about 40 IC design centers that comprise nine of the world's "top 10" fabless IC design companies.

Imec Reports 6.7% Growth for 2012 Fiscal Year End

Imec reported financial results for fiscal year ended December 31, 2012. Revenue for 2012 totaled 320 million euro, a 6.7% increase from the previous year. The 320 million euro figure includes the revenue generated

through collaborations with more than 600 companies and 200 universities worldwide, a yearly grant from the Flemish government totaling 48.2 million euro, and a 8.2 million euro grant from the Dutch government to support the Holst Centre. "We continued to expand and renew our R&D partnerships on semiconductor technology scaling, as well as on new emerging areas such as the biomedical field," said Luc Van den hove, CEO of imec. "Our robust growth last year is a testament to the strength and value these partnerships add to the development of next-generation technology and its applications."

In 2012, imec's talent base grew to 2,051 people, representing 75 nationalities. Of these, 377 were residents, visiting researchers from

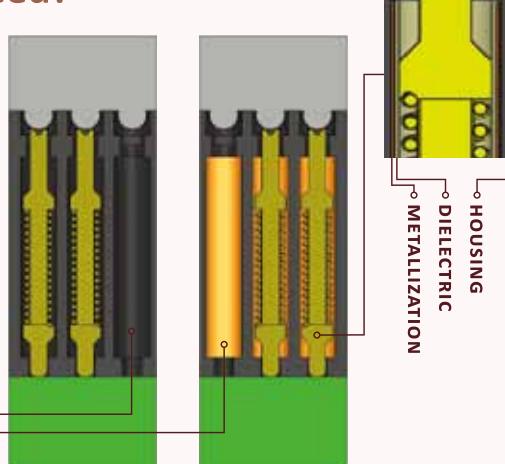
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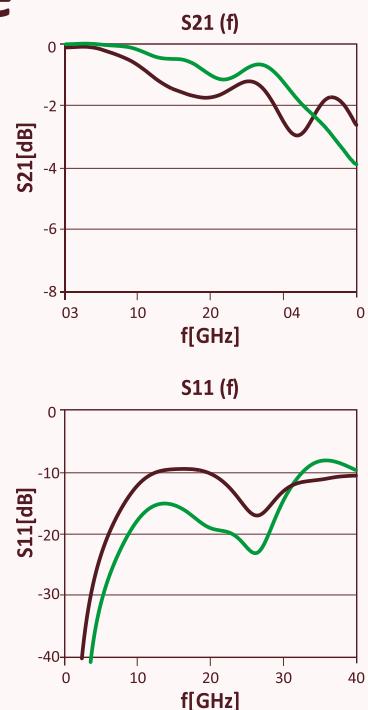
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- Want Impedance Tuning
- Need Shielding
- Want to Match Current Footprint
- Don't Want to Change my Mechanical Interface



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partner companies and institutes, and 276 were PhD researchers. One-hundred twenty-two employees are based at the Holst Centre, an open-innovation initiative between imec and TNO located in Eindhoven, the Netherlands.

"Given the current challenging economic backdrop, I am thrilled with the steady growth we have realized the last two years," said Van den hove. "Thanks to the efforts and talent of our employees, as well as the strength of our strategic research partnerships, we achieved significant breakthroughs in all our research areas."

Among the highlights of the 2012 R&D report include: 1,064 peer-reviewed articles published, 161 patents awarded, 133 patent applications submitted, and the successful renewal of the IOS9001 quality certification.

Yole Développement Issues Forecasts in MEMS and Glass Wafers

Recent forecasts by Yole Développement covered the MEMS pressure sensor market, and the glass wafer market:

MEMS Pressure Sensor Market

After years of limited growth, Yole Développement reported that the MEMS pressure sensor market is growing due to consumer electronic applications and is expected to show a 22% CAGR. Pressure sensors are playing an important role today in modern industries. MEMS pressure sensors are already widely adopted in different applications for their high-performance, low cost and small size.

In its new report "MEMS Pressure Sensor," Yole Développement gives a detailed overview of the MEMS pressure sensor markets, technologies and players. This report details the main applications in automotive, consumer, medical, industrial and high-end segment, and the main players in the industry. It also analyzes the current pressure sensor technologies including

MEMS technologies, and gives a detailed MEMS pressure sensor market forecast by application.

Emerging consumer applications are boosting the growth of the MEMS pressure sensor market and reshuffling the main players

The MEMS pressure sensor is one of the very first MEMS components appearing in the microsystem world. The technologies are quite mature and the market is big and expected to grow from \$1.9B in 2012 to \$3B in 2018 (**Figure 1**). "The MEMS pressure sensor for consumer applications, especially for smartphones and tablets, is following the model of accelerometers and gyroscopes. Adoption of this model will help the MEMS pressure sensor market to boom again! We believe, this huge opportunity will result in the global volume of the MEMS pressure sensor market hitting 2.8 billion units by 2018," announced Wenbin Ding, Technology & Market Analyst, MEMS Devices & Technologies at Yole Développement. "Consumer pressure sensors will represent 1.7 billion units and will overtake automotive as the market leader in volume," she added.

Even though the consumer application has a much lower ASP than other applications, this promising segment

will bring more than 8% CAGR to the global MEMS pressure sensor market. The report consolidated market data for 2012 and provides forecasts until 2018.

Automotive applications are still dominating the MEMS pressure sensor market. TPMS, MAP and BAP will be the biggest sub applications in this field, noted Yole. Automotive, medical, industrial and high-end markets are growing 4% to 7%, however, the consumer market is growing 25% in value (38% in volume) because of new opportunities in smartphones and tablets.

The MEMS pressure sensor finds new applications in each domain, for example: in-cylinder pressure sensing for automotive, the CPAP (continuous positive airway pressure) machine for medical use, smartphones (Samsung Galaxy SIII for indoor navigation) and tablets for the consumer electronics industry, etc. All these emerging applications are still in their infancy, but they appear promising and Yole Développement's analysts believe the MEMS pressure sensor will find new ways to satisfy end users in each domain.

Glass Wafer Market

Yole Développement recently announced results from its glass substrates for semiconductor manufacturing report. The research firm noted that over the last few years, glass has gained considerable interest from the semiconductor industry due to its very attractive electrical, physical and chemical properties, as well as its prospects for a relevant and cost-efficient solution. The application scope of glass substrates in the semiconductor field is broad and highly diversified. End

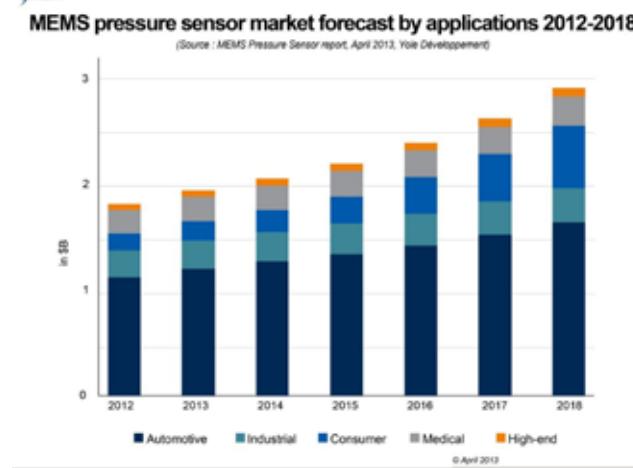


Figure 1: MEMS pressure sensor market forecast by applications 2012-2018.
SOURCE: MEMS Pressure Sensor report, April 2013, Yole Développement.

applications include: MEMS, CMOS image sensors, LED, memory and logic ICs, RF/analog ICs, power, micro-batteries, optoelectronic components, and microfluidics. Functionalities include support substrate, WLCapping, 3D through-glass via (TGV)/2.5D interposer, carriers, and micro-structuring.

Mainly driven by the wafer-level packaging industry, Yole expects the glass wafer market to grow from \$158M in 2012 to \$1.3B by 2018, at a CAGR of ~41% over the next five years (**Figure 2**). “Initially driven by CMOS image sensor and MEMS applications, this growing industry will be supported by relevant end-applications such as LED, memory and logic IC, where glass is on its way to being commercialized,” said Amandine Pizzagalli, Market and Technology Analyst, Equipment & Materials Manufacturing, at Yole Développement. “In terms of wafers shipped, a 4X glass wafer growth is expected in the semiconductor industry over the next five years, achieving more than 15M 8” EQ [wafer starts per year] WSPY by 2018.”

The glass WLCapping platform is a mature functionality already adopted with significant volume in CMOS image sensors, where more than 3.3M glass caps were shipped in 2012. This market is expected to grow slowly, with a CAGR of 14% from 2012-2018, mainly supported by MEMS devices impacted by the request for further miniaturization. On the flip side, the glass market for WLOptics will likely decline from 2015-2018 because of the development of competing technologies.

Despite the above considerations, Yole expects to see strong growth in the glass market, mainly supported by two emerging WLP platforms: with a CAGR of 110% and 70% respectively, the glass-type 2.5D interposer emerging platform and the carrier wafer will be glass’s fastest-growing fields over the next five years, because glass offers

the best value proposition in terms of cost, flexibility, mechanical rigidity and surface flatness.

If glass is qualified for 2.5D interposer functionality, the glass market could exceed \$1B in revenue by 2018. However, it’s still unclear

how back-end-of-line (BEOL) wafer fabs will choose glass over the current silicon technology used for logic IC applications (for the 2.5D/3D system-on-chip (SoC) and system partitioning areas), but the glass variety of 2.5D

(continued on Page 46)



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Realizing 3D IC Integration with Face-to-Face Stacking

By John Xie [Altera Corporation] and Deborah Patterson [Amkor Technology, Inc.]

Semiconductor process scaling, as driven by Moore's Law, has been the key driving force behind the evolution of today's high-tech industry. But increasingly, traditional process scaling alone can no longer meet system performance, throughput and power requirements. Although side-by-side monolithic silicon (2D structures), package-on-package (PoP), and package-in-package (PiP) platforms allow for two or more chips to be bonded together, they do not offer enough density, bandwidth or power to meet the requirements of next-generation product roadmaps.

The trade-offs between placing more functions on a chip (system-on-chip, SoC) versus placing more functions within a package (multi-chip package, MCP, or system-in-package, SiP) must be fully evaluated. Optimizing overall performance as well as total cost-of-ownership are equally important. And perhaps one of the most significant issues is accelerating time-to-market, as it is a strategic enabler to the end users.

To properly assess the above trade-offs in terms of effective silicon usage vis-à-vis functional integration (node optimization), die yield considerations from ramp to production, and the influence of the packaging strategy on signal integrity – ideally the package would be invisible to the signal while providing protection, thermal dissipation, etc. – both 2.5D and 3D packaging are being actively investigated.

An example of a 3D integrated circuit (IC) is represented by stacked ICs with through-silicon vias (TSV). In a 3D IC stack, solder bumps are used to join one die on top of another to allow the signals to travel between the die. 3D IC stacks

can be packaged independently or can be connected side-by-side on a substrate to other ICs. A 2.5D IC package, in contrast, is defined by the use of a multilayer passive silicon interposer as a substrate to interconnect multiple active die or die stacks in a side-by-side configuration. TSVs are used to route the signals through the silicon interposer down to flip-chip solder bumps located on the interposer's bottom side. The ICs themselves use much smaller copper (Cu) pillar micro-bumps for assembly onto the silicon interposer.

Using silicon as a platform for interconnecting the active ICs preserves signal integrity far better than conventional substrate materials and, in fact, enables new ways of thinking about SoC versus MCP trade-offs. The 2.5D package offers silicon-grade interconnect density and greatly reduced signal latency because of the short interconnect path between the active silicon die. Power consumption is also reduced because of I/O drivers that can be designed with Si-Si direct interconnect and reduced Joule loss on the interconnect path. 2.5D stacking also has a time-to-market advantage because 3D ICs require longer lead times to implement design and manufacture at the component level, and then to coordinate their concurrent assembly. The performance advantages of stacked ICs are illustrated in **Figure 1**, which compares the relative interconnect density, thermal resistance, and power usage between monolithic, 2.5D, and 3D IC packages.

The advantages of 2.5D stacked

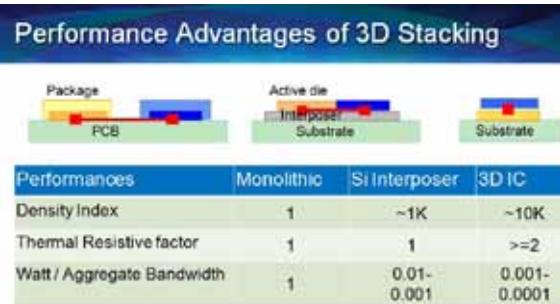


Figure 1: Comparison of the relative interconnect density, thermal resistance and power usage between three types of stacked multi-chip packages.

packaging have ushered in a new mindset on how to approach SoC versus MCP packaging and their combined impact upon near- and long-term silicon and package functional integration roadmaps. Aside from 2.5D and 3D semiconductor packaging approaches, there are still other innovative ways to increase function and performance while keeping package footprints small and supporting time-to-market goals.

Realizing that an optimized stacking configuration, coupled with a proper design and manufacturing flow can enable a relatively low cost stacked structure, Altera Corporation and Amkor Technology collaborated on the project roadmap for functions: for example, whether to use an SoC, or to re-architect a device, separating it into pieces to increase die yield.

Introducing an 'About Face'

Stacking innovation is a key focus for many semiconductor suppliers as well as packaging and assembly companies. Altera's internal R&D organization has produced a five-year roadmap for stacking technology. Similarly, Amkor's advanced development team supports numerous stacked manufacturing and

assembly approaches involving both wire bond and flip chip solutions.

A “face-to-face” packaging approach represents one type of stacked chip-on-chip (CoC) arrangement. Two die are joined face-to-face through copper pillar micro-bumps in order to make the connection between the active circuitry on each die closer - without having to add any TSV processing. One die must be sufficiently larger than the other (mother) such that all of its die-to-substrate flip-chip bumps are placed around the larger die’s perimeter, with the smaller die (daughter) attached inside. The daughter die and its bonded Cu columns must be thinner than the collapsed flip-chip bumps surrounding it, to ensure sufficient clearance between it and the next assembly surface. **Figure 2** illustrates an example of this structure, dubbed the POSSUM™ package configuration by Amkor.



Figure 2: Illustration showing a face-to-face chip-on-chip assembly that brings the active circuitry on each IC as close as possible without the use of TSVs. The larger die (mother) is assembled to the BGA substrate through flip-chip solder bumps (shown) or Cu pillar bumps/posts and the smaller die (daughter) is joined to the mother die through copper pillar micro-bumps.

The key feature of this packaging style is that it bonds two active ICs directly using Cu pillar micro-bumps without the need for TSVs or a silicon interposer. In fact, the structure uses established flip-chip substrate and assembly technology. It offers almost all of the true 3D IC stacking advantages: the stacked chips talk directly to each other with reduced latency, better signal quality, and additional power savings as compared with a 2.5D structure. The footprint is reduced and the stack does not grow in the Z-axis. Integration cost is also much lower than in 2.5D stacking. The face-to-face flip-chip structure also negates the complicated design and high manufacturing costs associated with integrating TSVs into active silicon.

Face-to-face stacking offers several packaging options. In addition to face-

to-face flip-chip chip scale package (CSP) or ball grid array (BGA) packaging, lead frame packaging has also been demonstrated (**Figure 3**). Face-to-face PBGA represents the most advanced of these packages as it utilizes a POSSUM™ mounted die assembled to the face of a larger die.

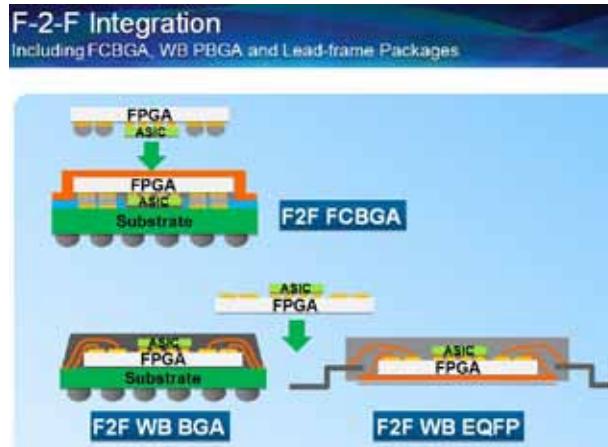


Figure 3: Illustration of three different face-to-face chip-on-chip package configurations.

Applications of Face-to-Face Stacking Technology

There are a number of semiconductor combinations that will benefit from a face-to-face stacking approach. For example, a high-density FPGA may be bonded with an ASIC to provide a combination of ASIC performance and FPGA flexibility in a specific application space. Perhaps the most obvious use is to combine two dice fabricated in different technologies, such as an RF front-end die and an FPGA die. Face-to-face bonding gives sufficient bandwidth between the two devices to allow for direct digital interaction with the RF circuitry. Similarly, bonding an FPGA to an external memory die can greatly

expand the FPGA’s access to low-latency memory without incurring the energy costs of high-frequency chip crossings.

As system throughput demands and working-storage bandwidths increase, the memory energy issue looms large.

Figure 5 compares the switching power needed per I/O channel for different memory solutions. It shows that face-to-face SRAM stacking offers essentially the same power and bandwidth advantage as a true 3D IC stack.

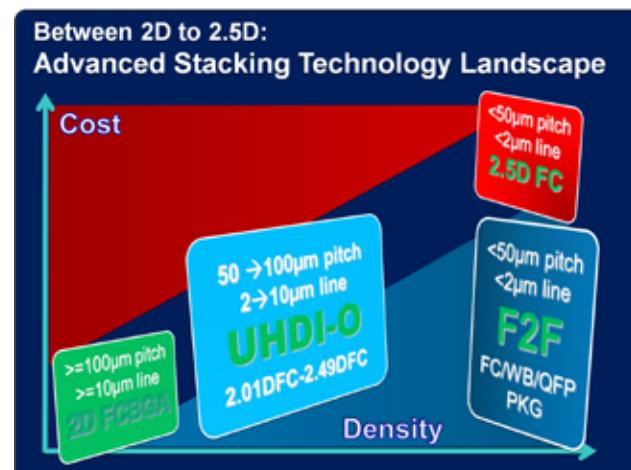


Figure 4: Illustration of packaged IC cost progression as I/O density increases.

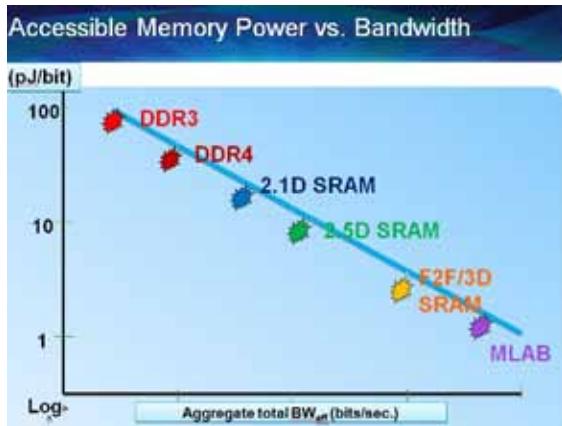


Figure 5: Simulated data demonstrating that face-to-face assembly of an SRAM onto an FPGA offers the same power and bandwidth advantage as a 3D TSV stacked die structure (MLAB is referring to embedded memory or the SOC option).

Nurturing a 3D Packaging Alternative

Consideration of the design and response of semiconductors and their packaging in parallel is important and greatly influences downstream technical direction, especially when the design must concurrently optimize total cost-of-ownership, product performance, and time-to-market. This awareness supports early partnering between the IC supplier and the OSAT (outsourced semiconductor assembly and test service provider). This broad combination of expertise, resources and experience is required in identifying viable packaging technologies that support aggressive product roadmap objectives.

The face-to-face POSSUM™ package provides an example of this blending of expertise. The structure was chosen due to its ability to join two or more die with closer coupling for shorter, faster communication. Less inductance, cross talk and parasitic resistance meant that the method was suitable for high frequency, high bandwidth applications. And the package was based on established process flows that were already in production, such as Cu pillar micro-bumping, flip-chip solder bumping, chip-on-chip mass reflow and/or thermo-compression bonding, chip-to-chip wire bonding, or chip-to-substrate flip-chip or wire bonding, as appropriate. In addition, the package could be ramped to high-volume manufacturing

without introducing complex wafer handling processes.

Face-to-Face Chip-on-Chip Assembly

The platform supporting CoC assembly is a direct result of the combination of copper pillar wafer bumping know-how and its advanced fine pitch assembly. The specifics of the bumping are tailored to the product design and assembly process flow.

After the copper pillar micro-bumps are applied to mother and daughter wafers, back grinding and dicing are performed. There is the option to separate the mother die or for it to remain in wafer form, depending on process flow optimization. The daughter die is then joined to the mother die using Cu pillar micro-bumps. Various bump structures, interconnection materials and processes to control bump standoff (e.g., non-collapsible core) are being investigated to provide for optimal reliability, electrical, and thermal performance. Cu pillar micro-bumps are in high-volume manufacturing at 40µm peripheral and 80µm staggered pitch, and in low-volume production at 30µm peripheral and 60µm staggered pitch.

Multi-Bump Height Flip-Chip Implementation

For the current face-to-face configuration, a taller Cu pillar micro-bump is created on the daughter die and a shorter height bump is formed on the larger mother die. **Figure 6** illustrates a close up of the concept where the dual size bumps are joined between mother and daughter die.

Note that the structure also utilizes

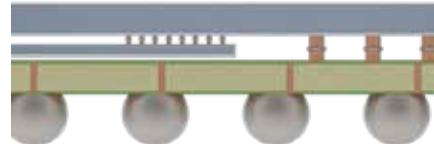


Figure 6: Close-up view of the dual size copper pillar micro-bumps used to join the mother (top) and daughter (bottom) die in a face-to-face configuration (not to scale).

advanced dual height bumping for the larger mother die. The CoC die pad region is bumped with the shorter bumps while the peripheral region outside the CoC bonding area is bumped with the taller copper pillar micro-bumps.

Assembling a 3D Package Without TSVs

There is a choice of two chip attach assembly processes for face-to-face Cu pillar bonding. The first is mass reflow with capillary underfill (MR+CUF), which is typically used for bump pitch >80µm with migration to >50µm.

The second chip attach assembly process is thermo-compression bonding with non-conductive paste (TC+NCP). This process is currently used in high-volume manufacturing production for die with 40/80µm I/O pitch for die-to-laminate substrates and has been found to be high yielding and reliable.

The TC+NCP assembly process is employed to join the mother and daughter ICs. Upon completion of this face-to-face assembly, the bonded dice are then attached to the substrate through a mass reflow process. It is critical to maintain a proper underfill flow that is uniform across the gap between the mother and daughter ICs in order to avoid the formation of air pockets after underfill cure. The process was refined to ensure void-free underfill and proper gap collapse between the mother and daughter die. Both variation of the die and substrate warpage are taken into consideration. The assembly of the devices onto the substrate is then followed by lid attach, ball attach, laser marking and test. **Figure 7** shows a cross-section and various close up views of the assembled package.

On-going development continues to advance the sphere of influence of chip-on-chip assembly. Chip-on-Wafer (CoW) processing, which utilizes equipment and process methods where the smaller die is attached directly to the larger die while it is still in wafer form, are in development. CoW also provides for the support of wafer-level chip scale packaging (WLCSP) within the POSSUM™ platform. Advances

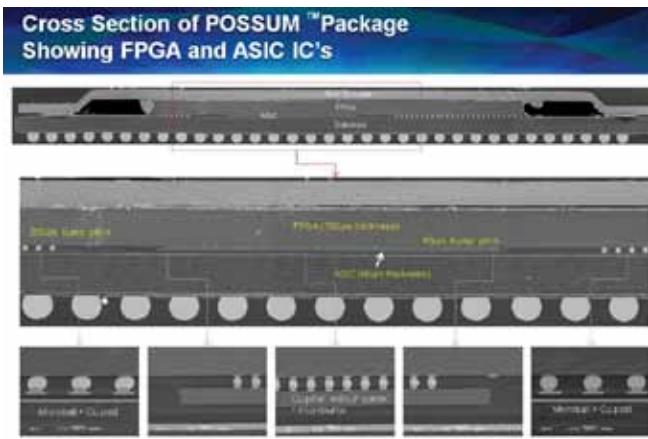


Figure 7: Cross-section of a FPGA die (mother) with a thinned 60µm ASIC die below (daughter). The two devices are assembled face-to-face through an array of 40µm Cu pillar micro-bumps. The ASIC is joined to the substrate through thicker Cu posts + solder microballs at a pitch of 200µm.

in materials across all 3D platforms are similarly adoptable to CoC application as they become available.

Temperature cycle tests have been conducted on packages using the Cu + SnAg solder caps. The packages have passed -55°C to 125°C for 2000 temperature cycles (JESD22-A104D, Level B). Other packages using Ni bumps + SnAg that are joined to Cu pillar + SnAg have withstood -55°C to 125°C for 3000 temperature cycles.

Summary

Upstream concurrent IC and package development allows for the assimilation of cost effective packaging solutions that optimize the right set of features in order to support the varied and aggressive requirements of end users.

In a short period of time, the joint development team has made tremendous progress on silicon bump design and manufacture, substrate structure and process, and assembly BOM and manufacturing flow. The team is pursuing several other types of stacking approaches and their integration into established packaging platforms (e.g., from wire bond and flip-chip to BGAs and lead frames).

The POSSUM™ configuration illustrates how face-to-face packaging can be optimized to leverage high performance in a multi-chip assembly without the use of expensive 2.5D or 3D TSV constructions. Although full

important for devices with the programming flexibility of FPGAs where ever increasing functionality and decreasing size and weight are required.

Acknowledgements

The authors would like to thank MJ Lee, Yuan Li, Zhe Li and the Altera

3D IC integration with TSVs remains an industry target, there are clever ways to address low-cost stacking in the near term. Face-to-face flip-chip packaging is expected to produce complex, highly integrated, and high performance products for a vast array of computing, communications, automotive and consumer products. This is especially

packaging R&D team in both San Jose and Penang, as well as Jemmy Sutanto, DongHe Kang, Michael Oh, Kwang-Seok Oh, KyungRok Park, Sa Yun Ma, Robert Lanzone, Dave Hiner, Ron Huemoeller and their advanced product development teams from Amkor Technology and Amkor Technology Korea for their joint contributions to this project. 

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Integrated Silicon Photonics Fabrication on a 300mm Platform

Douglas Coolbaugh, Thomas N. Adam, Gerald L. Leake, Phung Nguyen, Michelle L. Pautler [College of Nanoscale Science and Engineering] Jonathan Bradley, Ehsan Hosseini, Michael Watts [Research Laboratory of Electronics, Massachusetts Institute of Technology]

The College of Nanoscale Science and Engineering (CNSE) working in collaboration with the Massachusetts Institute of Technology (MIT) has developed a full flow photonics process on 300mm silicon-on-insulator (SOI) and bulk wafers. This offering encompasses multi-level low-loss silicon and silicon nitride waveguides, high speed germanium detectors, and active electro-optical components that can be co-integrated with advanced 65nm low power CMOS base technologies using 3D integration (**Figure 1**). These derivatives were developed for integrated photonic solutions and other optoelectronic applications. State-of-the-art industry-leading 193nm immersion photolithography and a fully equipped 300mm research fab enabled the successful incorporation of nanophotonic elements with high-end CMOS base technologies and a fully developed 3D integration process. Basic and advanced process flows were employed for standard photonics applications in conjunction with CMOS

and 3D integration. In addition, research level photonics can be modified for specific customer requirements, and novel materials and prototype devices can readily be developed and tested.

Integrated CMOS-compatible Waveguides

Integrated photonics circuits require waveguides that transport optical signals between components on one chip as well as on and off the chip. While signal dispersion can be neglected for these relatively short distances, the lowest absorption is needed to balance the low detector sensitivity and small optical gain in on-chip amplifiers and sources of today. In addition, a wide range of wavelengths (633nm to 1550nm) is needed for specialized applications that require guiding, mixing, or pumping with sources using shorter wavelengths. Most common integrated waveguides and resonators are of rectangular or ridge geometry and fabricated in silicon (single- or poly-crystalline) or silicon nitride. Single-level designs for components test applications were built using either silicon or silicon

nitride as the waveguiding layer. Two-level designs were implemented to determine coupling efficiencies and test modulators, switches, and optically pumped components. Multiple-level photonics circuits were integrated with full-build CMOS logic to demonstrate fully functional opto-electronic circuits. Leading-edge 193nm immersion lithography with sub-60nm resolution and advanced reactive ion-etching was used to pattern waveguides with minimal loading effects, negligible inter-level misalignment, and nearly perfect rectangular shape (sidewall angle of 90 ± 1 degrees). The residual sidewall roughness caused by line-edge variations during the lithography process as well as random geometric fluctuations stemming from reactive-ion etching was eliminated using a combination of dose and focus offsets, tone reversal, and thermal and oxidation/etching processing. As depicted in **Figure 2**, sub-100nm features (gaps, holes, lines) were obtained without optical proximity correction (OPC) while a resolution of 50nm and below can be achieved applying OPC models. Furthermore, advanced UV lithography is available for printable features of 20nm and below.

Dielectric Waveguides. Traditionally, low-pressure chemical vapor deposition (LPCVD) nitride on top of micrometer thick thermal oxide was used in photonics circuits owing to extremely low losses in the visible and infrared spectrum [1]. However, co-integration with CMOS or bipolar circuitry is prohibitive due to the excessive thermal budget and consumption of silicon during oxidation. Therefore, combinations of low-temperature and

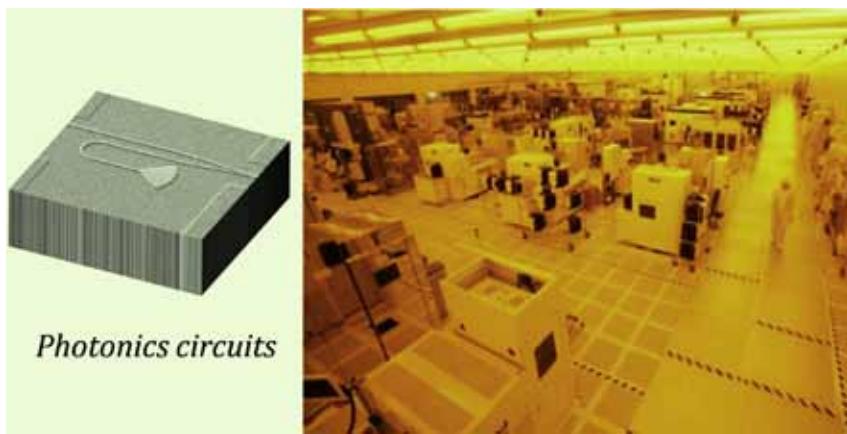


Figure 1: Fully equipped 300mm CMOS and photonics cleanroom facilities.

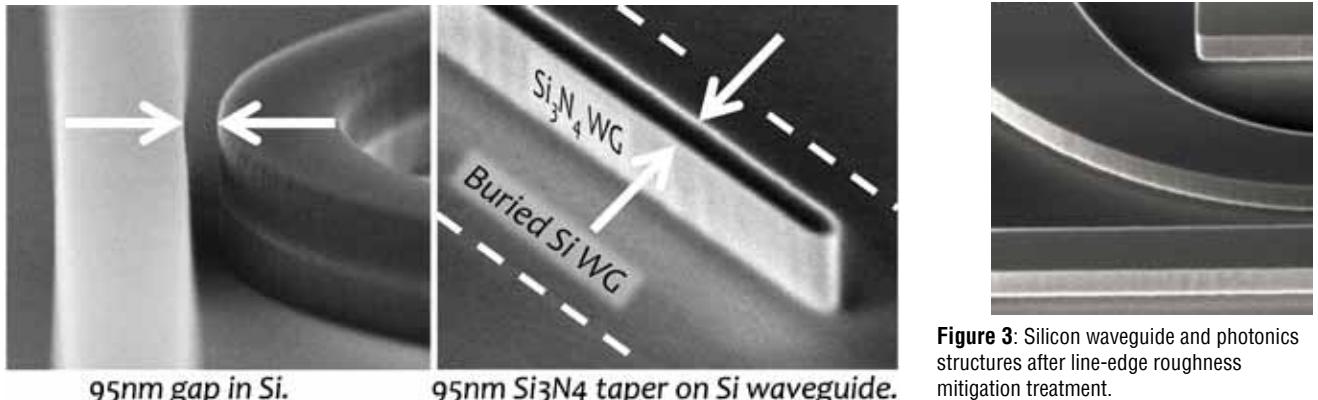


Figure 2: Features defined by immersion lithography without optical proximity correction. a) (Left) 95nm gap between waveguide and micro-ring resonator before softmask removal; b) (Right) 95nm silicon nitride waveguide on buried silicon waveguide.

low-loss deposited nitride and oxide have become an attractive alternative that allow logic-first co-integration. We have developed plasma-enhanced Si_3N_4 waveguides fabricated on micrometer thick plasma-enhanced tetraethyl orthosilicate SiO_2 (pTEOS) cladding with processing temperatures restricted to 500°C and below. This allowed the monolithic integration of optical components in both the front-end (Cu not yet on the wafer) and back-end (Cu metallization present). For front-end co-integration, LPCVD nitride on top of pTEOS can also be used to further reduce the propagation loss. Final line-edge roughness (LER) mitigation included thermal oxidation and wet chemical oxide removal. Residual hydrogen incorporated during the plasma deposition resulted in weak absorption peaking at 2db/cm near 1520nm. Annealing in an inert atmosphere for extended durations [2] permitted the reduction to 0.4db/cm. Comparable low absorption values were observed in the range between the infrared and visible wavelengths. Single and multiple levels of dielectric waveguides were produced using repeated planarization and patterning.

Silicon Waveguides. Single and multi-mode rectangular and ridge-type silicon waveguides (WG) were fabricated on standard and thick-oxide SOI substrates using CMOS-compatible lithography and non-scalloping reactive-ion etching techniques. Depending on the desired WG and cladding

thicknesses, soft masks (resist) or hard masks (dielectric material) were used to protect the top silicon during etching. The use of SOI substrates facilitates optical confinement and improved process repeatability and control (endpoint tracing and thickness control using ellipsometry). Calibrated angled high-resolution inline scanning electron microscope (SEM) and scatterometry were employed to determine and control the sidewall roughness and angle. Typically, substrates with 2 μm buried oxide (BOX) and 220nm top silicon thickness were utilized, and ridges as well as terminating edges were defined using standard silicon dry etching chemistries in high-density plasma etchers. The residual line-edge roughness was reduced using a thin medium-temperature dry or wet oxidation step [3] followed by a removal of the resulting oxide in a brief immersion in dilute HF (**Figure 3**).

Resonators, Filters, Couplers

Optical components such as resonators, modulators, filters, splitters, and couplers complete the functional design of an integrated photonics application. Important parameters are quality factor, resonance frequency, insertion and coupling loss, bandwidth,

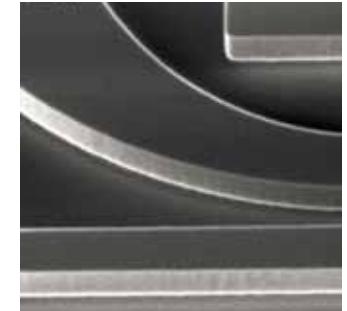


Figure 3: Silicon waveguide and photonics structures after line-edge roughness mitigation treatment.

and tuning range. While most of the design parameters are determined by geometry, i.e., lithography and pattern transfer, secondary effects such as sidewall roughness, pattern proximity, and reactive ion etch (RIE) lag complicate design targeting. As an example, evanescent wave couplers require tight control of the gap dimensions and geometry in order to function at the desired wavelength. This imposes new constraints on OPC models for photonics components that are computationally intense compared to their standard CMOS counterparts.

Figures 4 and 5 depict a selection of

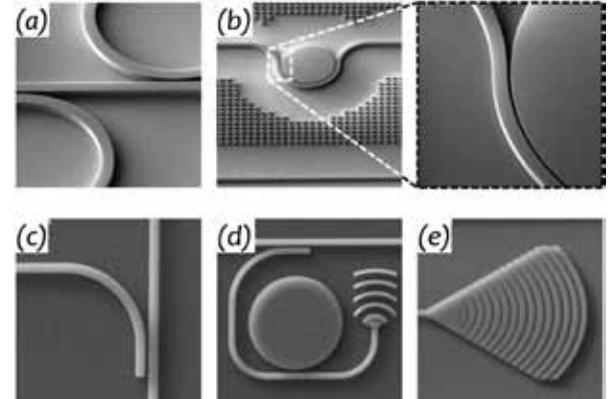


Figure 4: Photonic elements fabricated in silicon on SiO_2 and silicon nitride on SiO_2 : a) Microring filter structure; b) Microdisk resonator in 95nm proximity of waveguide; c) Splitter; d) Splitter + microdisk resonator + phased-array emitter; and (e) Grating structure for surface coupling.

photonic components fabricated in silicon and silicon nitride core materials. Because of the high resonator quality factors and low propagation loss, very narrow peak widths were obtained in resonators and filters as displayed in **Figure 6**. As can be seen, small variations in geometry (gaps, grating

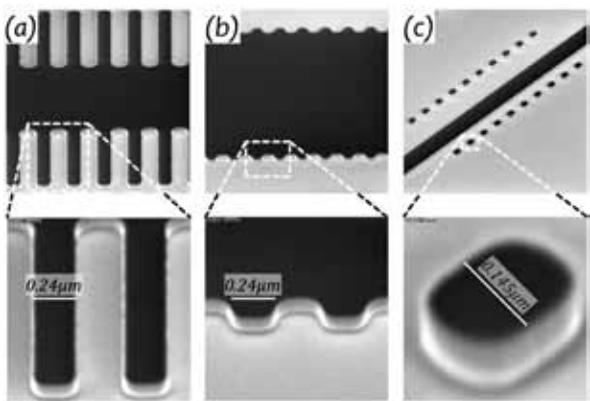


Figure 5: Silicon nitride waveguides with linear distributed feedback line structures: a) Deep gratings; b) Shallow gratings; c) External proximity gratings. The features were rounded due to the absence of optical proximity correction.

periods, etc.) resulted in substantial shifts of resonance frequencies and as a result, additional resonance tuning beyond lithography defined set-points are needed to dynamically match various photonic on-chip components. Electro-optical effects, and more recently, thermal modulation, provide the necessary tuning capability on the microscopic scale.

In order to couple the light from the fiber to the chip, grating structures and fiber trenches were developed. For the purpose of lateral fiber end-coupling, trenches (as deep as approximately half the fiber diameter) were fabricated using cyclic deep reactive ion etching (DRIE) prior to chip dicing. Sidewall tapering, control of final depth, and sloped bottom topography make this approach challenging for final fiber alignment. In contrast, in-plane grating structures were readily fabricated in silicon and silicon nitride by shallow non-cyclic reactive ion etching in a single or array-type coupling arrangement. In combination with integrated modulators,

of light, silicon is a poor detector material for $1.55\mu\text{m}$. In contrast, the bandgap absorption edge in germanium is near $1.58\mu\text{m}$, and even though Ge is an indirect semiconductor, it provides sufficient photo-response for optoelectronic applications using 1.3 and $1.55\mu\text{m}$ carrier wavelengths. In this report, we present results from p-i-n Ge diode detectors. The Ge detectors were embedded in low-temperature deposited oxide (between 0.5 and $1.0\mu\text{m}$ thick) by blanket deposition, patterning with RIE, and Ge CVD growth and planarization. Bottom contacts were achieved by p-type ion implantation while top contacts were in situ n-type doped poly-crystalline silicon. The growth of Ge was performed using either a low-throughput two-step process similar to that reported by Luan [5] or by a fast high-temperature one-step technique [6]. Both methods required post-growth annealing cycles to reduce the amount of threading dislocations and lower the reverse leakage current into the $\text{nA}/\mu\text{m}^2$ range [7]. Following a planarization step, the Ge was immediately capped, patterned, and contacted using a low-temperature in situ n-type doped polysilicon film. After a spike activation anneal, the top electrode was defined and back-end metallization layers were processed. A

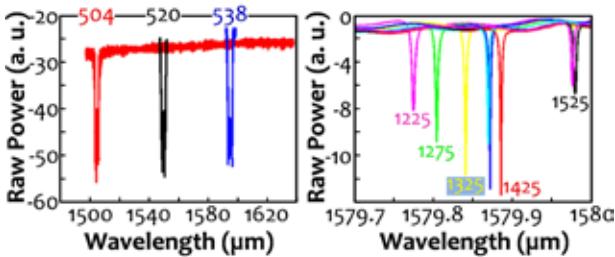


Figure 6: Resonant wavelengths of photonic elements: a) (Left) DBR resonance as a function of grating period (in nm); b) (Right) Microdisk ($R=100\mu\text{m}$) resonance as a function of gap (in nm) to waveguide. Data fitting indicated $Q \approx 500,000$ and $\alpha \approx 0.6\text{db/cm}$.

tunable phased-array emitters were fabricated that allowed beam steering from a 64×64 emitter array embedded directly on a microchip [4].

Modulators and Detectors

Integrated photonic circuits rely on the emission, modulation, and detection of light in the communications band ($1.3\mu\text{m}$ to $1.55\mu\text{m}$). Due to the larger bandgap compared to the energy

cross-sectional transmission electron microscope (TEM) picture is shown in **Figure 7** for a sample with insufficient defect annihilation anneal. While most dislocations are confined to the first few hundred Angstroms, a small number of dislocations still propagated to the top contact. Detectors of this type produced

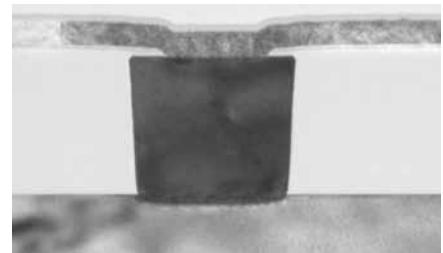


Figure 7: Cross-sectional TEM of Ge detector and top contact (in situ n-type doped polycrystalline silicon).

reverse leakage currents of 0.5 to $2\mu\text{A}/\mu\text{m}^2$ at -1V , while un-annealed Ge resulted in $>10\mu\text{A}/\mu\text{m}^2$. In contrast, $<10\text{nA}/\mu\text{m}^2$ was observed in properly annealed devices. A typical IV behavior (dark and $1.55\mu\text{m}$ -illuminated) and spectral response are shown in **Figure 8**. As can be seen, responsivities $R \approx 0.7\text{A}/\text{W}$ were obtained below the bandgap of Ge, while R reduced to $0.5\text{A}/\text{W}$ at $1.55\mu\text{m}$. Without further optimization by ion implantation or junction tuning, 600nm thick Ge detectors and modulators had a maximum bit rate of 13Gb/sec . Higher modulation speeds are currently under development.

CMOS Logic

A fully qualified low-power 65nm node was used as the base technology for integrated photonic circuits. The technology offering includes low-resistance Cu wiring, SiO_2 gate dielectrics, high-efficiency shallow trench device isolation, silicided contacts, and polysilicon gates. Applications can be designed based on a suite of available CMOS and photonics components, and automated layout and OPC generation. Depending on the functional complexity, up to 5 levels of back-end wiring layers are immediately available.

Acknowledgements

This work was supported in part

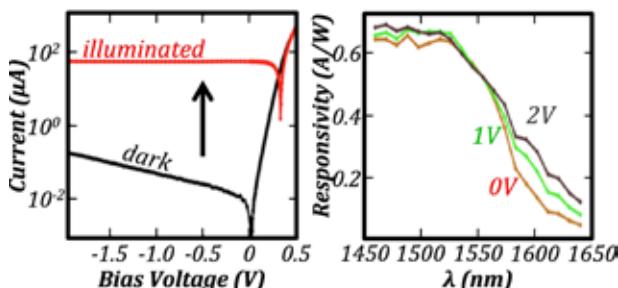


Figure 8: a) (Left) Dark and illuminated IV curve of integrated 1μm-by-9μm Ge detector; b) (Right) Spectral photo-response at various values of reverse bias.

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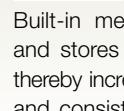
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Cleaning High-Reliability Assemblies with Tight Gaps

By Thomas M. Forsythe [[Kyzen Corporation](#)]

State of the art electronic devices continue to advance at a rapid rate delivering new capabilities to consumers throughout the world. Mobile phones alone account for over 400 million units per quarter, a solid 35% of which are smart phones. Smart phone production volumes now eclipse PC shipments, even with the generous inclusion of tablet sales in the PC statistics.

As even the casual observer is aware, these smart phones are smart indeed and their capabilities are steadily improving. This enhanced performance is a key element driving demand for these devices, not surprisingly as performance improves so does the user's expectations of quality and reliability; if one has their "life on one's phone," we certainly are not happy to see it go up in smoke in any way.

Electrochemical migration (ECM) is a critical risk factor in any electronic reliability analysis. Since every electronic device is powered up to function, and virtually every device does so in the presence of humidity, the sure way to prevent ECM is the absence of ionic residues.

Reducing or eliminating residues starts with a well-designed, validated, well run cleaning process. Such a process has two major building blocks: the equipment delivering the mechanical energy, and the cleaning agent delivering a well matched chemical solution that together remove all undesired contaminants not only from readily accessible surface areas but difficult to reach gaps beneath components and other devices.

The balance between chemical and mechanical elements in the process is critical to robust process design, equally important to a detailed understanding of the assemblies or packages which are to be cleaned.

Those schooled in the art of cleaning know that board density can increase the cleaning challenge, but the critical driver in today's complex designs is the "gap." The gap, also known as the stand-off height, is the distance between the bottom of a device and the board surface; the shorter this distance, the more difficult the cleaning challenge. Not surprisingly, truly flush mounted components present the greatest challenge.

With a sound understanding of the challenges presented by the assembly design, next we turn to the cleaning process itself. This evaluation begins with certain fundamentals developed during decades of research into cleaning technology that can act as a guide during the process:

Increased temperature generally enhances process results. However, the results provided by slightly elevated temperature are often not bettered at very high temperatures. More is not always better, and our data set will guide us to defining the point of diminishing returns.

Higher concentrations of the cleaning agents often enhance performance. As with temperature, there is routinely an inflection point of diminishing returns that should be understood in any process design. Operating concentrations have a linear effect on operating costs and always receive close scrutiny.

The mechanical energy delivery

system is important. It comprises the following: pressure, spray patterns, exposure gaps.

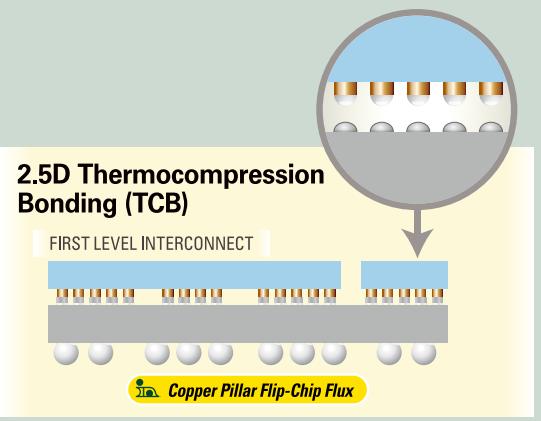
Exposure time to the cleaning agent and mechanical energy is another key factor. Time is always a precious commodity, and frequently subject to arbitrary limits determined prior to the device evaluation. When considering tight gaps or low standoff height device cleaning, a fifth element comes into play: cleaning agent surface tension and propensity for capillary action. In conjunction with the driving force of mechanical impingement, lower surface tension improves capillary action. Together, these forces enhance wetting and penetration of the fluid into tight gaps beneath components.

Experimental Design

The purpose of this designed experiment is to evaluate the effectiveness of a variety of cleaning agents under an array of process conditions. As such, mechanical energy was limited to allow for full understanding of the chemical driving forces at work as evaluated by ion chromatography. This DOE focused on cleaning effectiveness of a selected low gap chip-scale package.

Two commonly used water soluble fluxes typical for this type of package were selected along with three different cleaning solutions plus the commonly used water alone baseline. Three temperatures of 20°C, 40°C and 60°C were evaluated all with minimal agitated soak via mild shaking agitation. Response variables included vision inspection at 100x, and both anion and

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cation evaluation via ion chromatography (IC).

Dozens of studies have been conducted over the past 10 years, evaluating various aspects of new and novel cleaning processes providing a range of perspectives. Generally, they shared a modest number of substrates and resulting data points. This study attempted to address that with a large data set, 82 different points each with IC results to compare and contrast an unusually large body of IC data that we will attempt to analyze thoroughly.

Data Analysis

We begin the data review with our control sample. What is the state of the substrates prior to any cleaning step at all? **Figure 1** provides the anions detail. We have chlorides, nitrates and weak organic acid (WOA) present. WS#2 has generally lower levels of WOA than WS#1. Cation data was similar with generally very low levels with an elevated sodium level.

One challenge with this DOE is that it is a point source analysis. We did not evaluate full assemblies because surface cleaning is generally not very challenging these days. It can be, but cleaning in these tight gaps is the critical success criteria. For this reason, the results are a bit different from other recent studies.

The challenge comes with interpreting the data—current industry standards are logically focused on the acceptability of a full assembly not a single challenging device. The proper approach for scaling down these full assembly acceptable standards is also work that will be addressed in the future.

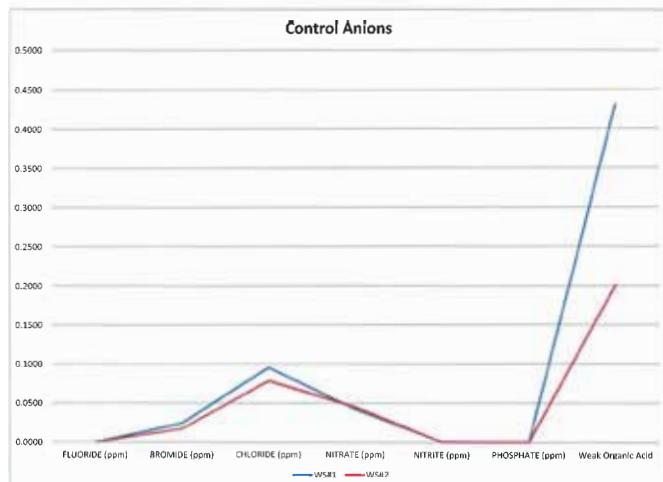


Figure 1: Control anions.

Cations detail is in **Figure 2**. We have sodium, lithium, potassium present. WS#2 also generally has lower levels of cations than WS#1. Water alone was included in the evaluation for one reason: it is the most common cleaning agent used to clean water soluble fluxes throughout the world. The key question is how does it measure up versus the control and the various cleaning agents evaluated. Evaluating the

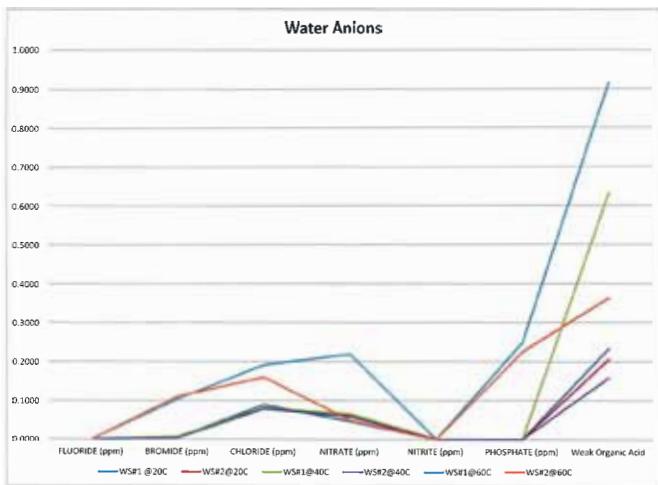


Figure 2: Water only anion results.

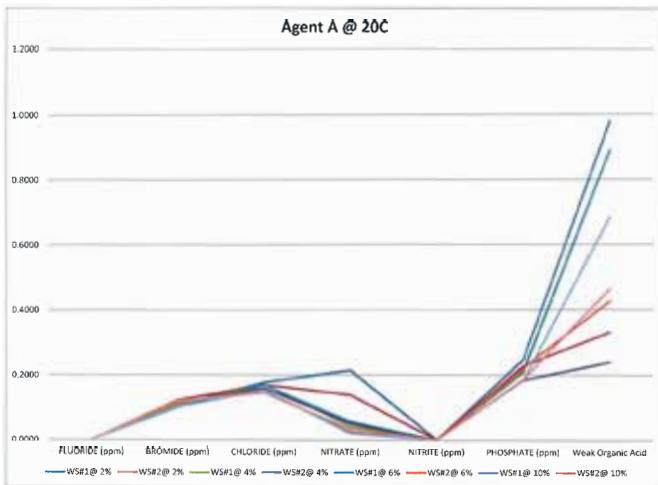


Figure 3: Agent A anions at 20°C.

water only anion results we see that chlorides, bromides, nitrates and weak organic acids are all present, while WS#2 has lower levels of WOA. The results also strongly parallel those found on the controls for both the anion and cations. Now, let's look at the results for the various cleaning agents.

Inferences that can be drawn from the Agent A data (**Figure 3**) include less visual difference between the two fluxes than when exposed to water alone, and cleaning was marginally improved with higher concentration.

Looking specifically at anions, the levels were very low overall. At the lowest temperature point of 20°C, we do see the data spread for WOA as with water and the control. As temperature increases, all the results trend together with WOA reduced to 0ppm as the temperature is increased to 40°C and 60°C (**Figure 4**) while nitrates and phosphates rose slightly at 40°C and 60°C. Cation data presented a similar positive response to temperature.

Interaction and Main Effects Plots

Agents B and C showed slightly better performance, but

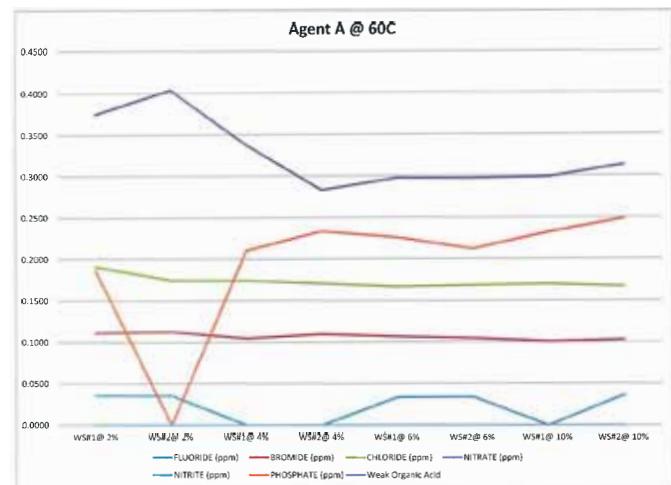


Figure 4: Agent A anions at 60°C.

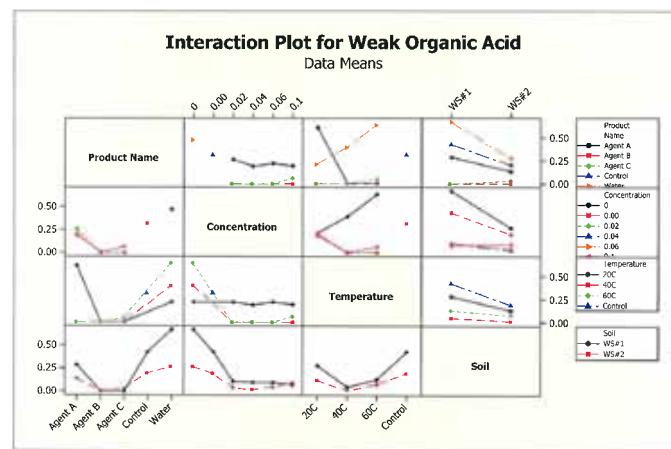


Figure 5: Interaction plot for weak organic acid (WOA).

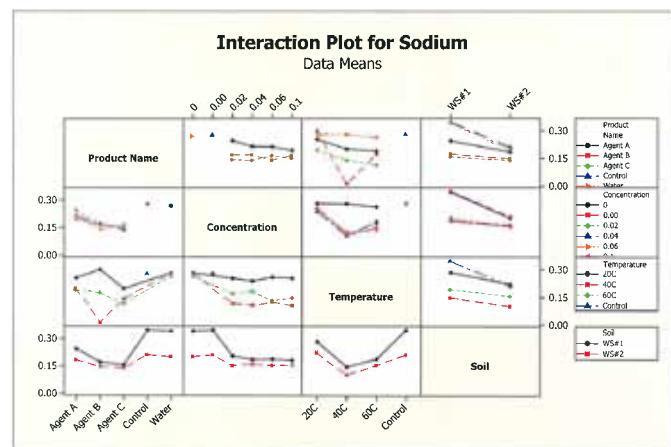


Figure 6: Interaction plot for sodium.

rather than review those data points individually, we will do so through the use of selected interaction and main effects plots to allow easy comparison (**Figure 5**).

Water responds meaningfully to increased temperature

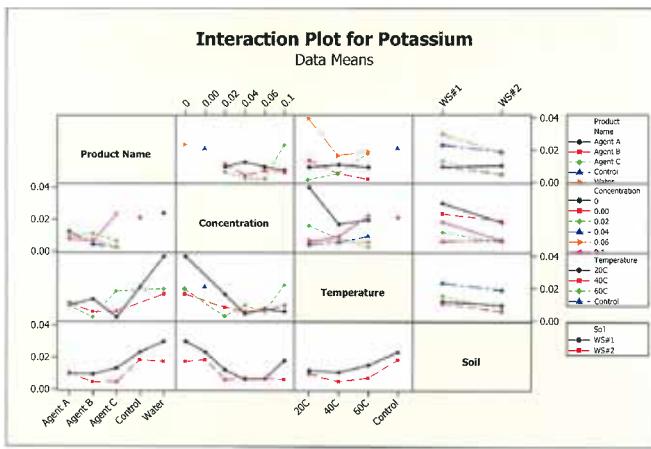


Figure 7: Interaction plot for potassium.

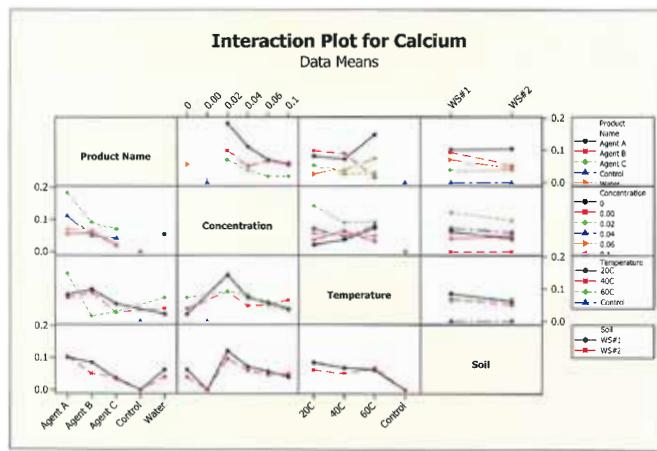


Figure 8: Interaction plot for calcium.

from 20°C to 40°C as one would expect. While WS#2 appears to have lower levels of WOA, the data is skewed by the control and water only results that are meaningfully poorer than all the agent data. This is a meaningful observation. While WS#2 was consistently better than WS#1, it was a slight difference. The major change in the plot was again driven by the control and water points. Sodium also trends better with increased temperature (**Figure 6**). Concentration seems to help, while temperature does not appear very responsive for the potassium ions (**Figure 7**). Agent C once again a clear winner with little difference between

WS#1 & WS#2 (**Figure 8**). With the control data skewed, Agent C breaks out as the winner though temperature and concentration do not trend toward more is better (**Figure 9**).

Summary

The large data package in this DOE makes the analysis rather straight forward. As in most protocols, there are ambiguous results at times and not every data set reaches the same conclusion. This point is key: any particular product life cycle may have unique sensitivities important to its operating for every day of its service life. Detailed data such as this, though expensive and time consuming to generate, can be enormously instructive for such high-value, long-lived devices.

Work such as this has several potential paths forward. One is to include more soils into the current data matrix. Another is to keep the same dataset and move downstream into commercial grade cleaning equipment to evaluate the impact of meaningful mechanical energy. More importantly for the industry, as work such as this propagates, industry standards will need to be developed and validated for these point source contamination levels.

Acknowledgments

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Biography

Thomas M. Forsythe received his BS from the United States Naval Academy, Annapolis MD in Operations Research and Engineering and his MBA from Boston U. in Finance; he is the VP of Sales & Mktg at Kyzen Corp; email tom_forsythe@kyzen.com.

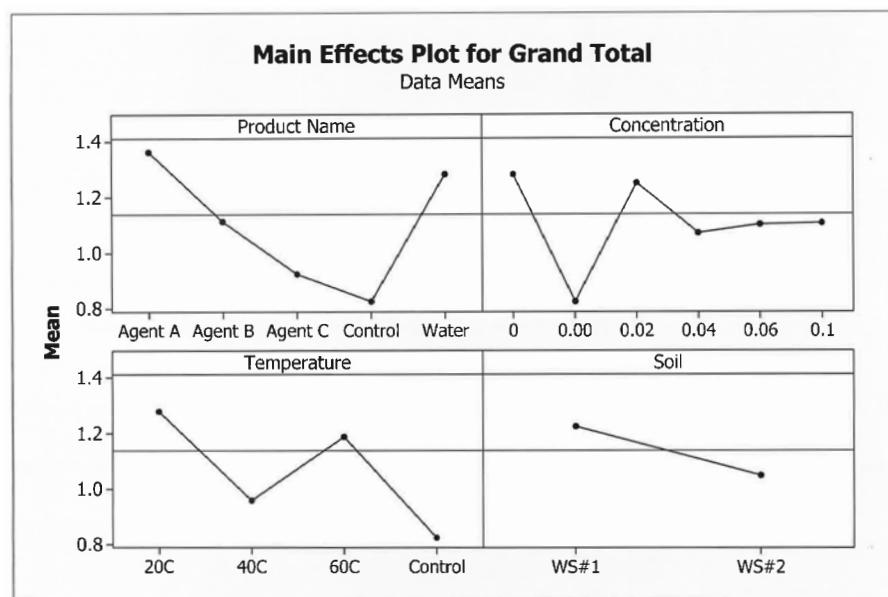


Figure 9: Main effects for grand total.

Latest Developments in Wafer Test

By Michael Huebner [Formfactor]

Those of you who have been around the semiconductor industry for some time may remember when probe cards were fairly simple, with the “cutting edge” probe cards of 15-20 years ago having a couple hundred of probes, one-to-one connections between tester channels and chip signals and relatively easy printed circuit boards (PCBs) – in some cases, even with hand-wired connections.

Things have changed quite a bit. In the last 15 years, probe cards for wafer test have gone through an extraordinary development cycle. The level of parallel test for memory chips, for example, has increased from 16 devices under test (DUTs) to up to 1500 DUTs, with the probe card contacting all devices on a 300mm wafer in one or two touchdowns. The probe count has increased as well, with the most advanced probe cards having up to 100k probes, resulting in high probe forces and with multiplexed tester channels using switching matrixes controlled by FPGAs or microcontrollers. Consequently, printed circuit board assemblies (PCBAs) have become highly complex. At the leading edge of probe card technology, PCBAs can require 50 layers or more. So on top of providing just the interface between tester and wafer, the probe cards of today can also serve as an extension of the tester by expanding its capabilities. At the same time probe card complexity has increased, the required mechanical accuracy has also increased substantially, driven by smaller and smaller pad dimensions and pad pitch. This probe card complexity is further challenged by other wafer test requirements such as test frequency and increasing temperature ranges. This article will focus on the changes in test

strategy and the resulting implications on the PCBA.

Controlling Cost with Parallel Testing

In the memory world, historically the increase in parallel test was driven by the increasing test time per wafer. With increasing memory density, the test time per DUT increased, and with the move to 300mm wafers, the number of die per wafer increased by a factor of 2.5 on top of the shrinks enabled by reduced feature size. However, with the increase in parallelism, the number of touchdowns needed to test all chips was reduced from 100 or more on a 200mm wafer 15 years ago, to 1-2 on a 300mm as of today. This reduction was essential to keep the test cost and time under control and to achieve short cycle time in wafer test. To enable the increase of parallelism, design-for-test (DFT) methods such as I/O compression and address pin reduction, higher channel count testers systems and methods for most efficient use of tester resources through sharing/multiplexing were developed and utilized. These technologies and their implications on the probe card will be described in the following sections.

Fifteen years ago, memory chips were tested as used in the application with all I/O channels and control channels connected. In this test environment, the parallelism was limited by the tester channel count of the automated test equipment (ATE). In contrast to SOC or mixed-signal testers, where all signal channels are bidirectional I/O channels, most memory tester have dedicated

I/O channels to read and write data and drive only channels used for clock, address and other controls. This means that device requirements and the tester capabilities need to be aligned very carefully.

The first step to higher parallelism was enabled by I/O compression, which was needed to test more DUTs with the available I/O channels on the tester. The number of data channels was reduced from typically 8, 16 or 32 channels, down to 4, and later to 2; the “one I/O test mode” will soon become mainstream. While I/O compression helps to reduce the number of the data channels, DFT was also used to reduce the number of control channels needed for chip operation by using address compression or other pin reduction test modes. Internal multiplexers for DC-channels are also commonly used now to reduce the number of DC-signals.

Figure 1 compares the test concept

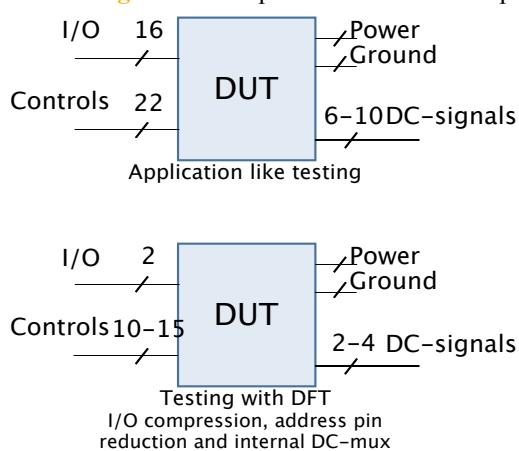


Figure 1: Comparison between application-like test and DFT-based testing for a typical DRAM chip.

from 15 years ago with a typical test concept that has a highly reduced tester channel requirement.

The implementation of DFT also

impacts the probe count. When an application such as test needs probes for all 16 I/Os, all controls, all DCs test pads and many power and ground pins, the probe count per DUT can be as high as 120. With DFT, this probe count can be reduced to the typical 50, which keeps the probe count in a manageable range even at high parallelism. Without DFT, the probe count could easily double. So DFT helps in two key areas. It enables higher parallelism because of the reduced usage of test resources, and at higher parallelism, it helps to reduce the number of probes per DUT, thereby keeping the total probe count manageable.

To use tester channels more efficiently, first tester resources enhancement (TRE) and, later, advanced TRE (A-TRE) were developed. TRE generally refers to the passive splitting of tester channels to connect them to multiple chips at the same time; A-TRE uses "switches" and some electronic circuits to increase the capability of the test systems. When TRE was introduced, two DUTs were sharing the same tester channel for one control signal. Today, up to 16 devices may share the same tester resources. There are, of course, tradeoffs on signal performance at higher frequency when more and more devices need to be controlled by the same tester driver; but at the typical frequencies around 100MHz, the signal performance is good enough for most applications.

In its simplest form, A-TRE is used to multiplex power supply channels and DC resources. One tester resource is again shared between multiple chips. In contrast to the simple sharing of control channels, wafer test requires connecting and disconnecting every chip from the shared tester resource to obtain individual chip data: e.g., current measurements results in the case of power supplies or voltage measurement when the chip manufacturer needs to know the voltage level forced by the chip through a certain DC-channel. A further challenge when sharing these kinds of signals is that in the case of a faulty device, chip manufacturers

need to be able to disconnect this faulty device from the shared resource as it may impact the test results of the other good devices sharing the same resource.

TRE on control channels is pretty straight forward and has no implications on test time other than it may limit the maximum test frequency because of the degradation of signal quality. For sharing of I/O channels, however, other tradeoffs need to be considered. While

I/O channels can be shared when data are written to a chip (parallel write), during the reading back process, only one chip can be connected at any given time to get the required individual chip test results (sequential read). In this case, which may be referred to as I/O TRE, AC-switches are typically used to connect and disconnect the data channels from the chips with the I/O channels from the tester. The test time

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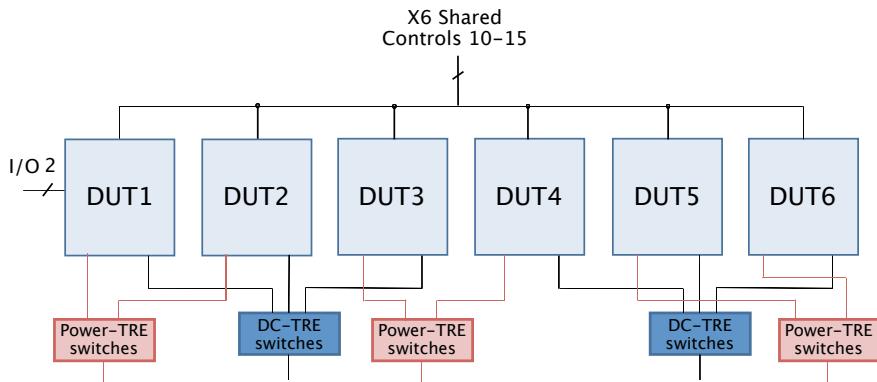


Figure 2: Typical test scenario with x6 signal TRE, x3 DC-TRE, and x2 Power-TRE.

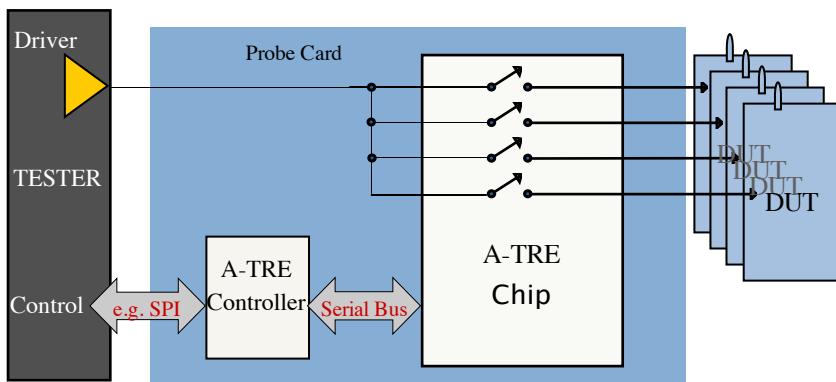


Figure 3: Typical A-TRE architecture using an A-TRE controller and a serial bus to control many A-TRE chips.

impact caused by the sequential read operation generally prohibits the use of such methods for DRAM SORT test. But there are applications like NAND SORT and WLBI (wafer-level burn-in) where I/O TRE has been successfully used. For NAND or NOR, where writing data takes much longer than reading back, the parallel write operation helps to save test time. During WLBI, very limited read back is needed as stressing the DUT is the primary objective of this test insertion, so no sequential read is needed. **Figure 2** shows a typical test scenario with A-TRE.

To support the increasing number for switches required, special test application specific integrated circuits (ASICs) and multi-chip modules have been developed. These ASICs are designed to match the electrical requirements of device test allowing the highest level of integration, and they also have serial control capability, which is essential for the individual switch control needed for many applications. Incorporating individual control

lines to every switch would result in an unsolvable routing problem on the PCBA. A typical A-TRE architecture consisting of an A-TRE controller communicating with the tester on one side and controlling the A-TRE switches through a serial control bus on the other side, is shown in **Figure 3**.

While 15 years ago a leading edge tester had 800 I/Os and driver channels and 64 power supplies to test 16DUTs in application mode, the latest models of today have more than 10k tester channels and up to 2k power supplies. With the massive increase in tester resources, the interface between the tester and the probe card became increasingly complex as the connector density and count had to increase with the channel count. The PCB diameter increased all the way up to 560mm from 300mm some 15 years ago. Besides the increase in tester channels, the mix between I/Os, driver channels, DC channels and power supplies has changed as well to comply with the new test strategies using DFT (as

discussed in the previous section). These evolutionary changes highlight one big advantage of placing electronics on the probe card: extending the useable life of testers. While testers may have a typical life of 10 years or more, test requirements, and consequently the mix of tester channels, can change dramatically during that time. With the use of A-TRE, chip manufacturers have the flexibility to change the tester channel mix (and extend the use of the tester) by multiplexing channels or adding other circuits that will perform these functions.

Traditionally, electronic circuits have been used for system-on-chip (SOC) wafer test. These circuits have been used for loop back, changing of load conditions, and other changes of the electrical environment during test. However, as parallelism was low, these cards were still relatively simple from an electrical point of view. The drive to higher parallelism for SOC has just started as more and more manufacturers are realizing the power of parallelism on productivity and test cost. While it can be challenging for certain applications to leverage the methods developed for memory test due to the different test strategies and concepts, some applications can leverage these techniques. Every SOC application for example, with some embedded memory and a dedicated test insertion to test these parts of the chip, can apply the methods developed for memory chips. In many cases, they even use the same test systems, admittedly not the latest generation test systems, but still 256 or 512 DUTs in parallel are possible using TRE, A-TRE and DFT.

Another area in wafer test where the use of more electronics has started is power. With increasing current requirements, test systems that have been used for many years are now running out of current capability even to maintain the parallel test. Circuits using DC/DC converters have been developed to use the full power capability of the tester power supply at max voltage and get more current at the lower voltages needed for most modern circuits. These

new power supplies/power managing circuits are also placed on the probe card and the same circuits developed for power sharing are used to distribute and multiplex these power supply channels. DAC and ADC are used to control voltage levels and to measure currents and voltages. All these are fairly complex circuits that need to fit into the small available space. A very dense section of a typical PCBA with A-TRE is shown in **Figure 4**.

Summary

As stated in the beginning of this article, in the past probe cards used to provide a simple one-to-one interface. Today, a high-end memory card has FPGAs and/or microcontrollers to manage the communication with the tester and to control the switch matrix to multiplex DC, AC and power resources (10k or more switches have been realized today already). These controllers require firmware to ensure the switches are set correctly and

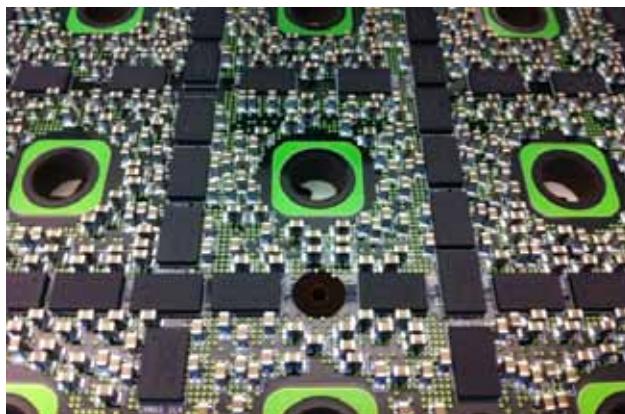


Figure 4: Section of a PCBA with high-density A-TRE switches and many capacitors.

the commands sent from the tester are interpreted correctly. The boards also contain thousands of capacitors, particularly for mobile DRAM test, with 4 bypass capacitors per DUT on the PCBA. In order to fit all this on the probe card, ASICs and multi-chip modules have been developed. These are tailored to the test requirements and enable the required switch density by the highest level of integration.

So a probe card today includes a 440 to 560mm diameter PCBA with 50 or more layers. It is packed with capacitors, controllers and semiconductor switches all squeezed in between the mechanical features and stiffeners needed to maintain the mechanical stability of the card down to μm levels under probe forces equivalent to 100 to 200 kg. This is quite

different from what we used to know 15-20 years ago. ■

Biography

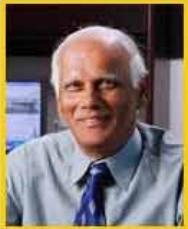
Michael Huebner received his PhD in Technical Physics from the U. of Bayreuth in Germany and is Sr. Director Engineering for Advanced TRE Technology at Formfactor; email MHuebner@formfactor.com



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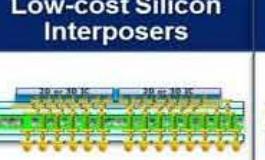
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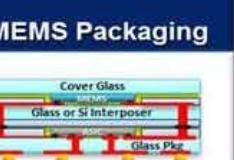
Low-cost Silicon Interposers



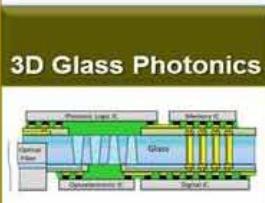
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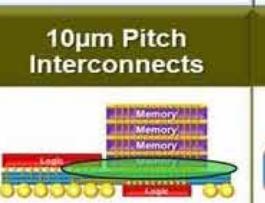
3D Glass Photonics



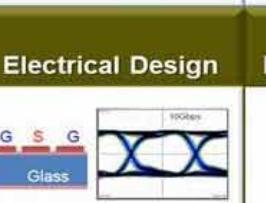
Board-level Interconnects



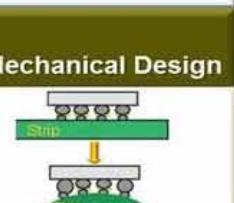
10 μm Pitch Interconnects



Electrical Design



Mechanical Design



Test Sockets for MEMS

By Wendy Chen [King Yuan Electronics Co.Ltd]

The market demand for smart applications used in mobile phones, cars, appliances and personal healthcare devices ramped up rapidly in the last 5 years. These applications are forecasted to increase in volume by several fold in the next 5 years. The MEMS devices dedicated to these markets require smaller package sizes, as well as highly integrated multiple functions such as acceleration, gyroscope, e-compass and pressure sensor, all in one package – either using an SIP or 3DS (3D stacking).

There is a large portfolio of diversified non-electrical MEMS devices based on silicon, but the test challenges are different from the traditional testing methods for semiconductor ICs. There are two significant characteristics of the MEMS manufacturing process: 1) “One product, one process, one package, one testing method;” and 2) Packaging “adds value.”

The challenges that this market presents to test socket designers is how to design a socket that can handle the multiple stimulations such as motion, magnetic field, air pressure (static/dynamic) for mass production volumes, as well as accommodate a large portfolio mix at the lowest cost.

In this article, we will discuss the challenges and potential solutions for designing cost effective sockets to test MEMS sensors/actuators in mass production. We will share our experiences as an early supporter and enabler during the initial period of “smart application” ramp up, which drove the MEMS sensor-manufacturing model to transition from IDMs to the outsourcing supply chain model. During the transition period, we discovered that because of the special conditions required for testing various MEMS products such as sensors, actuators on accelerators, e-compasses, gyroscopes,

microphones, CMOS image sensors, etc., there are no standard design rules nor off-the-shelf sockets, and in general, there is a lack of expertise in design and manufacture of these types of sockets.

The Challenges

When designing sockets for testing ICs (integrated circuits), the major concerns include frequency bandwidth, power consumption, heat dissipation, contact force relative to the device’s pad structure, and lifetime of the socket and pogo pin. In testing a MEMS sensor, there are more conditions to be considered: 1) The accuracy position of the device in the socket is important for testing a MEMS motion sensor; 2) Using a nonmagnetic material is a basic requirement for making test sockets for a magnetic MEMS sensor; 3) When testing a MEMS sensor microphone, noise isolation should be considered.

Aside from the above considerations, the 3D stack assembly process has become a trend in the production of MEMS sensors in which multiple sensing functions have to be integrated. When designing for a 3D stack assembly, the socket designer should consider weaknesses in the device’s structure and the assembly process. The discussion in this article will cover socket design for a MEMS sensor relative to different sensing functions.

The design and manufacture of test sockets for the MEMS market pushes the envelope for the sockets market to new limits from a technical perspective, as well as increases significantly its total available market (TAM). New expertise will be required for design as well as qualifying this type of socket. It is our view that the demand for MEMS sockets will revitalize the test socket market—a market that has been maturing slowly and becoming dominated by a few large competitors as

well as a lot of mom-and-pop shops.

Test Socket for a Sensing Motion MEMS Device

MEMS motion sensors include accelerometers and gyroscopes that detect acceleration in movement and angle velocity. The most stringent specifications for MEMS sockets are related to the fact that handling is the most critical restriction, as is docking to auto-handlers. The electrical test itself is not difficult in most cases, but providing the optimum test environment, and collecting and analyzing the data is very challenging. There are four major issues that need to be addressed: 1) Insuring that the device is properly held and restricted while being tested; 2) Contact force and stress; 3) The tolerance of the rotated angle when being run through the auto handler; and 4) The life time of the socket, including cleaning.

If the position of the device in the socket is changing when the test system applies acceleration or rotation, the sensing data will couple the variation from the socket’s motion into the signal that will be analyzed. It is very difficult to isolate noises due to the socket’s instability from the signal so the test result is corrupted. Increasing the contact force to overcome this problem is not an acceptable compromise because the embedded mechanical structure in either the accelerometer or gyro MEMS device could be easily damaged by external stress and this will compromise the device’s functionality.

An example of the above dilemma can be seen with a comb finger MEMS structure (**Figure 1**). It is worth pointing out that an SIP is the most popular method to package accelerometer devices. There are three chips in the SIP package (**Figure 1**), which includes two MEMS sensing devices – one each for the XY axis and the Z axis.

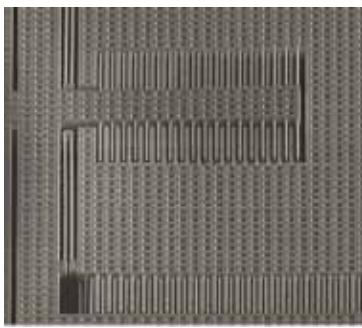


Figure 1: Comb finger MEMS structure.

The Z-axis is the most sensitive to an applied stress.

We can easily identify the probing force exceeding the threshold value—it's the value at which the performance of the device rapidly becomes abnormal. We had been confronted with this kind of problem and **Figure 2** is an example of the measurements resulting from one of the test cases. Besides dealing with the probing force challenge, we had to design a flat surface for the clamp on the socket that is used for holding the device to avoid movement when acceleration and rotation are applied. The clamping structure design also had to take into account the fragility of the package.

Considering that more and more MEMS devices for consumer applications use the CMOS MEMS process with a 3D IC or an SIP package, the flat surface structure of the clamp, which is in contact with the top of the package, must be optimized for different types of packages. The socket must implement special designs to accommodate a suitable geometric surface for the structure of the clamp to accommodate various nonstandard package designs.

As seen in **Figure 3**, individual clamps are designed for different SIP packages.

The physical stimulation of the device is relative to the direction of the force applied. A relatively small deviation in the tolerance of the rotated angle of the part located in the socket during production test (when using automated handlers) will cause offset biased results.

The typical socket design only requires a tolerance on the x, y, and z dimensions. Designing the test socket for a motion sensor, however, which includes an accelerometer and a gyro, needs to consider the tolerances of the x, y, and z dimension, and the rotation angle. The tolerance on the angle is generally only ± 0.1 degree and when allowing for a 0.1mm package size deviation, the task is difficult and requires a very complex structure. Based on our experience, we found that a socket with spring force from the sidewall is currently the most acceptable solution to accommodate various package structures.

Socket for a Magnetic Field MEMS Device

The concept of built-in self-test (BIST) has been successfully adopted by the industry for applications using a magnetic sensor for an E-compass. The design concept is implemented by embedding a coil inside a MEMS device and using the Hall effect phenomenon to generate a magnetic field for self-test. This method does not require the application of an external magnetic field for testing this type of device. When we design the socket for devices that incorporate BIST in the magnetic MEMS sensor, we only need to consider the socket component material—it should be nonmagnetic (i.e.,

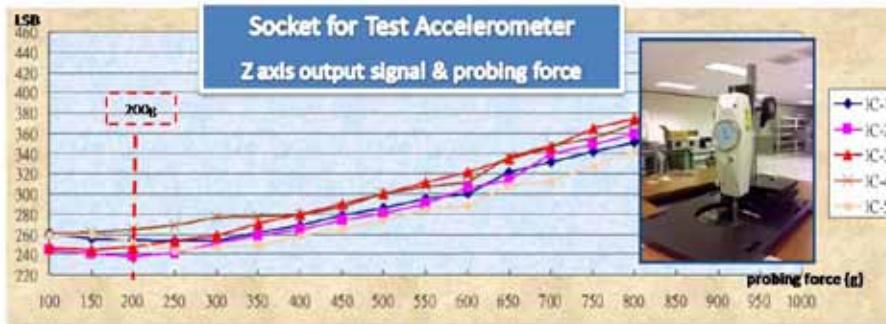


Figure 2: Example of measurement results from a test case in the initial stage of MEMS testing.

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Figure 3: Individual clamps as designed for different SIP packages.

brass spring, alloy screws, nonmagnetic plating, etc.) There are two kinds of socket design concepts for an external magnetic field stimulation test method: the chamber type and the per socket type described below.

Chamber type. In this method, the magnetic field is applied in a large chamber and the test devices are placed in the center of the chamber. As with the previous case, the concern when designing the test socket is that the socket material should be nonmagnetic.

Per socket type. The test socket itself provides a magnetic field in the x, y, and z-axes. We studied and developed the active magnetic field per socket by using coils on 3 axes to take advantage of the Hall Effect (**Figure 4**). This structure could easily dock with a mass production auto handler.

MEMS Devices for Sensing Sound or Air Pressure

The test socket design for testing a MEMS microphone or an air pressure sensor for consumer applications should consider a chamber environment that provides a physical stimulation source and an auto handler at the same time. A discussion about test considerations for both of these devices follows.

MEMS Microphone. The method of testing a MEMS microphone component is to apply sound pressure to the device under test in the near-field range. The design of the test socket should take into account the sound pole of the microphone that detects sound pressure from a stimulus with the proper high signal-to-noise ratio. There are different noise concerns based on which type of auto handler is used, such as gravity, pick and place, turret, and carrier in tray. From our experience, the pick and place handler provides a better handling system for testing multi-sided MEMS microphones and individual chambers.

The key points of socket design in this case are sealing issues, which need to avoid vibration, and vacuum noise from the auto handler system. Also, the socket design should provide a calibrator per side to eliminate unbalance issues with the multi-sided design. The most

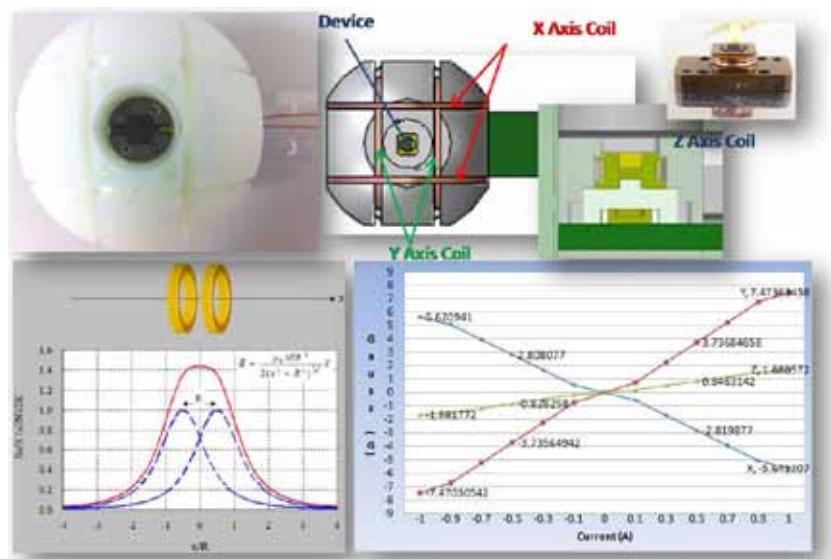


Figure 4: An active magnetic field per socket was developed by using coils on three axes.

advanced handling method is the test in carrier solution. The concept uses air pressure vibrations instead of a chamber with a speaker. This method is still under evaluation, and it will take more time to implement it in volume production.

Pressure sensor. There are two different types of sockets for testing MEMS pressure sensors. The first type uses a pressurized multi-site chamber, which is widely used for automotive applications. For this method, socket reliability is the main concern. The second approach is to integrate the socket into an individual chamber—a per-socket test pressure. This kind of socket design is targeted for low cost MEMS devices and consumer applications. The most important concern with this method is air leakage of the socket base through

the pogo pin; the design must provide a sealing structure to prevent the leakage without degradation to the contact performance.

Summary

Based on a Yole Développement market analysis, between 2011 and 2017, the CAGR will be 12.9% and the volume growth rate will be 20.7%. This information also implies that the unit ASP will decline, but volumes will continue increasing and a combination device will replace a single function device. This situation will drive test

solutions to have high parallelism and reduced insertion cycles for testing such combination devices. It will also increase the difficulties of designing the test socket, especially those used for combination MEMS sensing devices. In the future, considerations when designing test sockets for MEMS sensor devices will not only need to include the key points mentioned in this article, but will also have to consider combination effects and cross-talk problems. ■

Biography

Wendy Chen received her master's in photoelectric engineering from Taiwan's National Central U.; she is the senior director of R&D at King Yuan Electronics Co. Ltd.; email wjchen@kyec.com.tw or Andrei Berar at andreiberar@kyecusa.com

INTERNATIONAL DIRECTORY OF TEST & BURN-IN SOCKET SUPPLIERS

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	SOCKET TYPES	PACKAGE TYPES	SOCKET SPECIFICATIONS
Company Street Address City, State, Country Telephone Website	B = Burn-in D = Development P = Production T = Test Contactor CM = Contact Mfgr.	BA = Ball Array BD = Bare Die LA = Leadless Array SM = Surface Mount TH = Through Hole	CP = Contact Pitch CL = Contact Life OT = Op. Temp. Range FQ = Frequency (Ins. Loss) CF = Contact Force / Pin CR = Current Rating / Pin
Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to +260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to +125°C FQ < 30 GHz CF & CR = CM
Andon Electronics Corporation 4 Court Drive Lincoln, RI 02865 Tel: +1-401-333-0388 www.andonelect.com	P	BA, LA, SM, TH	CP > 1.0 mm CL & FQ = CM OT = -65°C to +240°C CF = CM CR < 1.0 A
AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 4 Merrill Industrial Drive Hampton Beach, NH 03842 Tel: +1-603-926-2517 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
Aries Electronics, Inc.  2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to 155°C CL, FQ, CF & CR = CM
Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
Centipede Systems Inc. 41 Daggett Drive San Jose, CA 95134 Tel: +1-408-321-8201 www.centipedesystems.com	T	BA, LA, SM	CP > 0.3 mm CL > 500,000x OT < +160°C FQ = CM CF = CM CR < 2.0 A @ 150°C
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com	B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A

INTERNATIONAL DIRECTORY OF TEST & BURN-IN SOCKET SUPPLIERS

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Custom Interconnects 7790 E. Arapahoe Rd, Suite 250 Centennial, CO 80112 Tel: +1-303-934-6600 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz CF = CM CR < 5.0 A
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com	B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Enplas Tesco, Inc. 765 N. Mary Avenue Sunnyvale, CA 94085 Tel: +1-408-749-8124 www.enplas-ets.com	B, D, T	BA, LA, SM	CP > 0.4 mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14 - 35) g CR < (0.5 - 1.0) A
Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3 mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30 GHz @ -1dB CF < (15 - 40) g CR < (0.5 - 1.0) A
E-tec Interconnect Ltd. Chemin du Grand-Pré 9A CH-1510 Moudon, Switzerland Tel: +41-21-781-0810 www.e-tec.com	D, P	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (100 - 10,000)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40 g CR < (0.5 - 3.0) A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4 mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40 GHz @ CM CF < (10 - 12) g CR = CM
High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > 0.4mm to 1.27mm CL > 200k insertions FQ Up to 40GHz @ -1.0dB CF 10 - 60g/pin OT -40 to 150°C CR Up to 7amps/pins Continuous
HSIO Technologies, LLC. 13300 67th Avenue North Maple Grove, MN 55311 Tel: 763-447-6260 www.hsiotech.com	D,P,T	BA, BD, LA, SM	CP = ≥ 0.3mm CL = Product Dependant OT = -55° to 155°C FQ > 15-40Ghz @ -1dB CF = Product Dependant CR = 2-4A
High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5 mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0 A

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Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	P	BA, LA	CP > 0.8 mm CR < 10 A CL, OT, FQ, CF = CM
Ironwood Electronics 11351 Rupp Drive Burnsville, MN 55337 Tel: +1-952-229-8200 www.ironwoodelectronics.com	B, D, T	BA, LA, SM	CP > (0.25 - 0.4) mm CL > (2k - 500k)x OT = -70°C to +200°C FQ < (6 - 40) GHz @ -1dB CF < 50 g CR < (2.0 - 8.0) A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
JF Technology Berhad (747681-H) Lot 6, Jalan Teknologi 3/6, Taman Sains Selangor 1, Kota Damansara, 47810 Petaling Jaya, Selangor D.E. Malaysia www.jftech.com.my	B, D, P, T	BA, BD, LA, SM	CP ≥ 0.3mm CL 300K - 1000K OT -40C to 155C FQ -1dB@14GHz CF 30 Grams CR 4.5 A≥
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (300k - 1,000K)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25 - 0.4) mm CL = CM OT = CM FQ = CM CF = CM CR = CM
M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjco.jp	B, D, T	BA, SM	CP > 0.2 mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM

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Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25 - 50) g CR < (1.0 - 3.0) A
Modus Test LLC P.O. Box 56708 Atlanta, GA 31156 Tel: +1-678-765-7775 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3 mm CL > 1,000,000x OT = +200°C Max. FQ < 20 GHz @ CM CF < 35 g CR < 5.0 A
Multitest Elektronische Systeme GmbH Aeussere Oberaustrasse 4 D-83026 Rosenheim, Germany Tel: +49-8031-4060 www.multitest.com	D, T	BA, LA, SM	CP > (0.25 - 0.5) mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5 - 40) GHz @ CM CF < (26 - 55) g CR < (1.8 - 4.6) A
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong, Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0 - 12.4) GHz @ -1dB CF < (7 - 15) g CR < (0.5 - 1.0) A
Paricon Technologies Corporation 421 Currant Road Fall River, MA 02720 Tel: +1-508-676-6888 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1 - 0.4) mm CL > 1,000,000x OT < 150°C FQ < 40 GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtest.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 1,000,000x OT = -50°C to +150°C FQ > 40 GHz @ -1dB CF = 20-45 g CR > 3.5 A
Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
ProFab Technology Inc. 41817 Albrae Street Fremont, CA 94538 Tel: +1-925-600-0770 www.profabtechnology.com	D, T	BA, LA	CP > (0.26 - 0.45) mm CR < 7.0 A CL, OT, FQ & CF = CM
Qualmax, Inc. IT Castle, 1-dong, 1101-ho 550-1 Gasan-dong, Geumcheong-gu Seoul, Korea 153-768 Tel: +82-2-2082-6770 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5) mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0 - 4.0) A

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Rika Denshi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36 GHz @ -1dB CF < (15 - 30) g CP & CR = CM
Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0 A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35 mm OT = -55°C to +150°C FQ < (9 - 10) GHz @ CM CR < (1.0 - 15.0) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Avenue, Suite 100 San Jose, CA 95120 Tel: +1-408-269-2800 www.sanyu-usa.com	CM	CM	CP > 0.2 mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15 - 25) g CR < (4.0 - 5.0) A
Sensata Technologies, Inc. 529 Pleasant Street, P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10 - 25) g CR < 1.0 A
Smiths Connectors IDI 5101 Richland Avenue Kansas City, KS 66106 Tel: +1-913-342-5544 www.idinet.com/synergetix	D,P,T	BA, BD, LA, SM	CP > (0.4 - 0.5) mm CL > (250k - 500k)x OT = -55°C to +150°C FQ < (9.6 - 20) GHz @ -1dB CF < (17 - 85) g CR < (1.5 - 5.0) A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3 - 0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5 - 20) GHz @ CM CF & CR = CM
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3 Bayan Lepas, Penang 11900, Malaysia Tel: +60-4-646-6966 www.tts-grp.com	D, T	BA, LA, SM, TH	CP > 0.2 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 20 GHz @ -1dB CF & CR = CM
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: +1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5 - 1.0) A
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com	D, T	SM	CP > 0.4 mm OT = -40°C to +150°C FQ < (6 - 8) GHz @ CM CL, CF & CR = CM

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Wells-CTI 2102 W. Quail Avenue, Ste. 2 Phoenix, AZ 85027 Tel: +1-480-682-6100 www.wellscti.com	B	BA, LA, SM, TH	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (8 - 80) g CR < (0.5 - 2.0) A
WinWay Technology Co. Ltd. 2F, No. 315, Minghua Road, Gushan District Kaohsiung 804, Taiwan Tel: +886-7-552-4599 www.winway.com.tw	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > (50k - 500k)x OT = -50°C to +150°C FQ < (0.2 - 14) GHz @ -1dB CF < (10 - 41.3) g CR < (1.5 - 3.0) A
Yamaichi Electronics Co., Ltd. 3-28-7 Nakamagome, Ota-Ku Tokyo 143-8515, Japan Tel: +81-3-3778-6111 www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4 mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM

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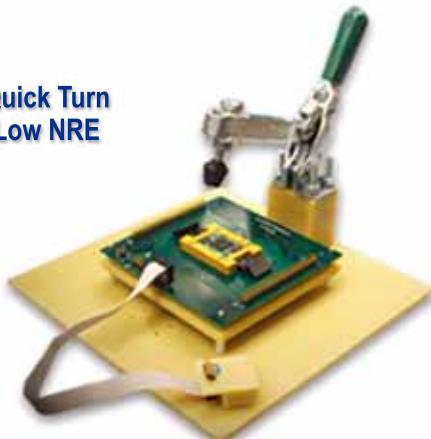
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Solder Joint Geometry Optimization Increases WLCSP Reliability

By Boyd Rogers, Chris Scanlan [Deca Technologies, Inc.]

Wafer-level chip-scale packaging (WLCSP) offers the smallest package form factor and has become a preferred option for the handheld consumer electronics space where portability and increasing functionality are strong drivers. WLCSPs also continue to migrate into other applications requiring small size, high performance, and low cost. In WLCSP technology, chip I/Os are generally fanned-in across the die surface using thick polymer and redistribution line (RDL) buildup layers to produce an area array, and large solder bumps are then formed at the terminals by ball drop or plating. These additive processes allow the chip to be attached directly to a printed circuit board (PCB) with good reliability [1].

The thermal mismatch between the silicon chip and the organic PCB has limited WLCSPs to relatively small die sizes — usually less than $5 \times 5\text{mm}^2$ — so WLCSP suppliers and users are continually looking for ways to improve reliability and extend the size range of chips that can utilize this unique packaging technology. In recent years, the introduction of new polymers and solder alloys as well as the optimization of buildup layer thicknesses in WLCSP construction have extended the usable die sizes into the $5 \times 5\text{mm}^2$ to $6 \times 6\text{mm}^2$ range [2-4]. Further significant increases are likely to require new and novel WLCSP structures and approaches.

Optimizing the solder joint geometry is a relatively simple but effective way to improve WLCSP reliability. Important variables to consider include the via size under the bump on the WLCSP, the size of the WLCSP under bump metallurgy (UBM) pad, and the

size of the corresponding pad on the PCB. Optimizing these factors can lead to performance improvements in thermal cycling, one of the key board-level reliability tests that measures the life of the WLCSP.

This article reports on a study in which an enhancement of nearly 2X was achieved in thermal cycling reliability by solder joint geometry optimization.

Test Vehicle

The test vehicle used to study the effect of solder joint geometry factors on WLCSP reliability is shown in Figure 1. The die was $3.9 \times 3.9\text{mm}^2$, moderately sized for WLCSP applications. The WLCSP build-up layers consisted of PBO polymer and plated Cu RDL at standard industry thicknesses. The solder was SAC405, and the finished WLCSP contained 81 balls in a 9×9 array on a 0.4mm pitch. The test vehicle was a live device with RDL-level daisy chain connections that could be completed on the board side, allowing for real time monitoring during board-level reliability testing.

A non-solder-mask defined solder

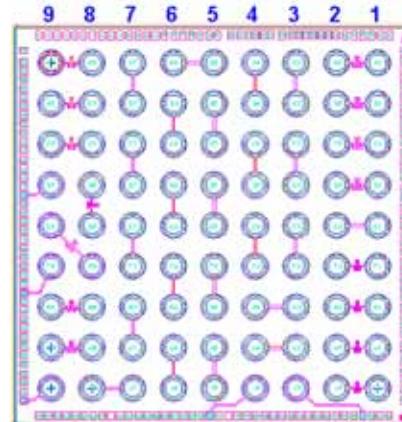


Figure 1: $3.9\text{mm} \times 3.9\text{mm}$ WLCSP daisy chain test vehicle.

joint, typical for WLCSP assembly, is illustrated in Figure 2. The key factors affecting the solder joint geometry are the UBM pad size on the WLCSP, the size of the polymer via under the bump on the WLCSP, and the PCB pad size. In this study, the UBM pad size was fixed and the polymer via and the PCB pad were varied to determine the effects of these changes on WLCSP performance in thermal cycling tests.

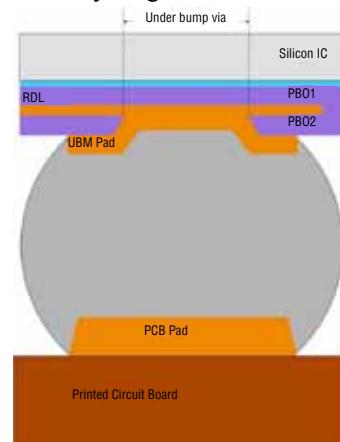


Figure 2: Illustration of WLCSP solder joint, showing main geometric factors: UBM pad, under bump via, and PCB pad.

The PCB board used in this study was an 8-layer, 1mm thick board, and the PCB pads were non-solder-mask defined. Standard JEDEC conditions were used for the temperature cycling (-40 to 125°C, 1 cycle/hr) [5]. Thermal cycling simulations were carried out assuming the above parameters, and then board-level thermal cycling tests were performed to confirm the trends predicted by the simulations.

Simulation Results

An ANSYS model was used to simulate the thermal cycling performance of the test vehicle for various solder joint geometries (Figure 3). Symmetry

was used to reduce the model to 1/4 of the package size. For thermal cycling, the critical joint is at the corner bump, which is the furthest bump location from the neutral point, the package center. The strain energy-density-distribution (SED) for the corner bump at the bump-UBM pad interface can be used to predict the thermal cycle lifetime of the part. By comparing the SED for various bump geometry cases, the effects of the bump geometry on the thermal cycle lifetime was predicted [6,7].

Results of the modeling work for

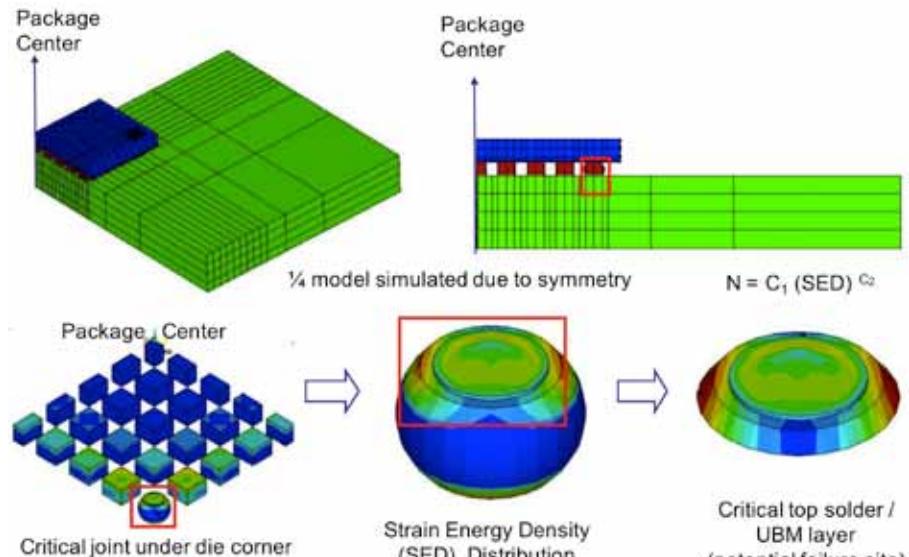


Figure 3: ANSYS model used to simulate our 0.4mm pitch, 81 ball qualification test vehicle.

different bump geometries are shown in **Table 1**. Here, the under-bump-via and the PCB pad sizes are referenced to the UBM pad, which remained fixed. The thermal cycling results are reported as percent improvement compared to the control case. The model predicts that a smaller via under the bump is better for thermal cycling performance. The model also suggests that improvements can be obtained by choosing the proper ratio of the PCB pad to the UBM pad on the WLCSP. The PCB pad should be smaller than the UBM pad for optimized cycling performance.

Board-level Reliability Testing

Thermal cycling testing was performed using the same test vehicle and board design used for the modeling work. Splits were performed to test various

bump geometries. In the experimental splits, the UBM pad size again remained fixed and the under-bump-via and the PCB pad sizes were varied to produce the different bump geometries.

Results of the board-level reliability testing are shown in **Table 2**. Here, the trends predicted by the modeling work are confirmed: A smaller via under the bump is better for thermal cycling performance, and a smaller PCB pad compared to the UBM pad is also important for optimizing thermal cycling results. As a matter of fact,

be obtained in cycling performance by optimizing the ratio of the PCB pad to the UBM pad. The results suggest this ratio should be maintained at less than one for optimal cycling performance.

SEM cross-sections of failed corner joints from splits 1 and 3 after thermal cycle testing are shown in **Figures 4** and **5**, respectively. For both cases, the failure is solder fatigue, which is the desirable failure mode, and as expected, the fatigue is occurring near the bump-UBM pad interface. However, the joint from split 3 with the smaller PCB pad exhibited 82% longer thermal cycling life than the joint from split 1. The reason for the early failure for split 1 can be understood by comparing the two photographs. In **Figure 4**, the PCB pad is equivalent in diameter to the UBM pad. However, because the PCB pad is much thicker than the UBM pad and also is non-solder-mask defined, the wetting out of the solder around this

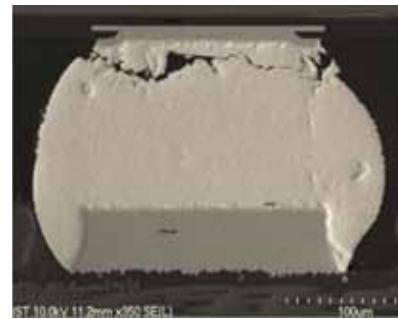


Figure 4: SEM cross-section of failed corner bump from experimental split 1, where the PCB pad = the UBM pad.

comparison of splits 1 and 3, where only the PCB pad has been reduced, suggests that fairly dramatic gains may

Simulation Case	Via Diameter	PCB Pad Diameter	% Improvement in TC Performance
Control	0.8 x UBM pad	1.0 x UBM pad	-
Reduced via diameter	0.65 x UBM pad	1.0 x UBM pad	36%
Reduced PCB pad diameter	0.8 x UBM pad	0.9 x UBM pad	38%
Increased PCB pad diameter	0.8 x UBM pad	1.1 x UBM pad	-28%

Table 1: Simulation predictions of thermal cycling performance for different bump geometries.

Split #	Description	Via Diameter	PCB Pad Diameter	% Improvement in TC Performance
1	Control	0.8 x UBM pad	1.0 x UBM pad	-
2	Larger via, smaller PCB pad	0.65 x UBM pad	0.9 x UBM pad	18%
3	Control via, smaller PCB pad	0.8 x UBM pad	0.9 x UBM pad	82%
4	Smaller via, smaller PCB pad	0.65 x UBM pad	0.9 x UBM pad	100%

Table 2: Experimental results showing thermal cycling performance for different bump geometries.

pad during assembly causes the joint to be larger on the board side than the WLCSP side. This causes the bump to assume more of a truncated pear shape than a spherical shape and drives an earlier cycling failure near the smaller bump-UBM pad side of the joint. On the other hand, for the joint pictured in **Figure 5**, the PCB pad is undersized compared to the UBM pad, such that the two joint sides

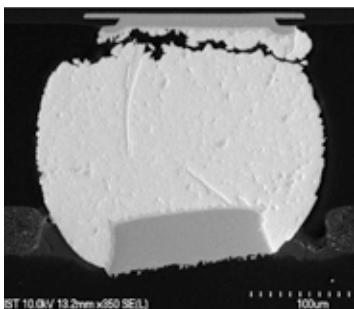


Figure 5: SEM cross-section of failed corner bump from experimental split 3, where the PCB pad = 0.9 x UBM pad.

are almost equivalent in size. This produces a more spherical-shaped bump and tends to delay the solder fatigue failure at the bump-UBM side of the joint. The smaller PCB pad also results in a little more stand-off for the WLCSP from the board, another factor in improving cycling reliability.

It is likely that the smaller under-bump-via results in improved thermal cycling performance by providing more stress buffering under the bump edge. This allows the bump to ‘rock’ more during thermal cycle stressing, with the PBO polymer under the bump absorbing more of the stress and delaying the tendency for solder fatigue failure.

In addition to thermal cycle testing, standard JEDEC drop testing was also performed on all of the experimental splits shown in **Table 2** [8]. All splits exhibited greater than 300 drops to failure, with minimal differentiation between the splits. This suggests that the joint geometry changes discussed here can be implemented and the corresponding thermal cycling benefits obtained without compromising drop performance.

Conclusion

Optimizing the solder joint geometry is a simple but effective way to maximize WLCSP reliability. The results in this study suggest that as much as a 2x enhancement in thermal cycle reliability can be obtained by properly sizing the polymer via under the bump and by targeting an appropriate PCB pad to UBM pad size ratio. In particular, undersizing the PCB pad to produce a spherical joint geometry appears to be very important for optimizing thermal cycling results. In addition, this study indicates that joint optimizations to improve thermal cycling performance can be implemented without compromising drop test performance.

Acknowledgement

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Biographies

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INTERVIEW



Anatomy of a Test Socket



An interview with Pablo Rodriguez, General Manager, E-tec Interconnect Ltd.

CSR: Is E-tec a broad line test socket supplier or do you concentrate on specific market segments—and how do these segments impact the overall cost/performance equation?

PR: We supply sockets to several market segments including prototype development, bench test, production test and failure analysis, as well as end user system level applications. Therefore, it is important for us to learn as much as possible about the customer's application. Smaller/faster/cheaper/better has been the historic mantra for semiconductor chip design and it has had a direct effect on the design and performance of the test socket. Smaller package formats with tighter lead pitch challenge the mechanical design limits of the socket. Requirements for insertion loss of -1dB to higher and higher frequencies require innovative contact designs. Contact current rating and cycle life must also be considered here. Many other factors affect the cost/performance calculation including thermal dissipation, operating temperature, package retention mechanisms and available socket mounting options. These parameters are not independent from each other when optimizing the socket design. Changing one parameter often affects another, which is why we encourage customer collaboration to define the application requirements as completely as possible.

CSR: Can you define the socket recommendation process and the steps that are taken to insure a successful design?

PR: First is the review of the mechanical configuration of the chip

package to be tested; we always require a dimensional drawing of the package. This is a very important step, especially on the small form factor tight pitch packages where tolerance variations could cause misalignment or no alignment of the package leads to the socket contacts. Since the socket will be compressing the package into the socket, knowing the overall thickness and determining the fragility of the package is critical. If it is a solderball package, the diameter and height of the solderballs must be known in advance. The package dimensional drawing will usually answer these questions. We then determine the contact system, socket closure mechanism, PCB mounting requirement and any unique application specific requirements.



E-Tec AG's Headquarters, founded in 1973 at Lengnau, Switzerland is a fully approved ISO 9001 precision manufacturer.

CSR: What determines your specific recommendation for a given contact system?

PR: The contact system (contactor) establishes both the electrical and mechanical capabilities of the socket and is the heart of any test socket design. There are a variety of contact configurations available today from several suppliers, each with their own

unique characteristics. The electrical and mechanical requirements of the application and the attributes of the contact must be coordinated to provide the most cost effective solution.

One of the most often discussed requirements with our customers is insertion loss. To provide maximum transmission speeds for "high-speed" applications, a very short contact path (<1mm) is necessary with an inductance value of well below 1nH and contact resistance of 30milliohm or less. In addition, RF applications will specify an impedance value of the contact system to be 50ohms for these high-speed applications. Often times, high-speed test sockets must also offer high current carrying performance.

Mechanical requirements also impact the contact system design with cycle life at or near the top of the list. The most cost effective design will also have the flexibility to interface with diverse lead configurations like BGA solder balls of various sizes, the flat pads of LGAs and QFNs as well as gull-wing and j-bend leads. The ideal contact would also be scalable to meet the physical limitations of the chip package lead pitch from 1.5mm to 0.3mm while maintaining optimum performance.

We presently offer three contact systems: our patented contact, a high performance probe-pin, and an elastomer interposer series. There are three parameters that must be evaluated to determine proper choice: the insertion loss bandwidth, the package lead pitch and the comparative cost.

Some applications may benefit from two different contact types within the same socket.

Insertion loss bandwidth of our patented contact is specified at -1dB to 3GHz and validated by a recognized independent test lab. Here we can accommodate lead pitch from 1.50mm down to 0.4mm. This solution is cost competitive, especially for larger, higher pin count packages.

The high performance probe-pin is usually chosen when required insertion loss bandwidth of -1dB to 10GHz and higher, dependent on contact pitch. These probes are also available for 1.5mm to 0.4mm package pitch and have a higher relative cost.

Our elastomer interposer series is suited for package sizes of 12x12mm and smaller. Insertion loss bandwidth of -1dB to 6.5 GHz or 10GHz is dependent on package lead type. This series is suitable for any lead pitch down to 0.3mm and is very competitive for these smaller size packages.

The contact system is the core component in the test socket and we have a continuing program in place to investigate and develop innovative contact concepts to satisfy market demands. We welcome customer participation in this effort to identify the requirements and evaluate possible solutions.

CSR: You mentioned earlier that there are functional requirements that often must be considered in the overall socket design. Can you expand on these?

PR: The closure (retention) mechanism for compressing the package into the socket is highly dependent on customer preferences and the parameters defined by the application. For example, a clamshell style socket that requires some "extra" real estate for opening/closing may not be suited for multiple sockets mounted on a high density device under test (DUT) board. Another application may require that a fine-pitch, low-lead count socket be

SMT-mounted to the PCB where stress on the solder joints must be considered when choosing the retention system.

We also offer several options for mounting the socket, each with pros and cons. The thru-hole method provides a robust solution but PCB trace routing may be a problem, especially for high-density footprints. Another choice is solderless compression that can minimize trace routing issues but also may require a backside stiffener plate, which could limit component population on the bottom side of the PCB. Our patented contact design can be supplied with RoHS-compatible tin plated terminals ideally suited for reflow solder surface mount. One common request is to provide a socket retrofitted to an existing PCB. Here we can modify the socket body to accommodate existing mounting holes and/or provide special pins to raise the socket base for clearance. A variety of adapter and socket-on-socket options are also available.

CSR: How have you utilized your ongoing customer collaboration effort to enter new market segments?

PR: I can comment here with two examples. The first, which is at the introductory level and another, that is at the entry-level stage. Over the past few years, we have been working with several customers for the design and manufacture of application specific burn-in sockets. To complement this effort, we have established our standard burn-in socket product line introduced at the recent BiTS Workshop in Phoenix. We have also just completed a socket qualification program designed for continuous 450°C operation. These high temperature applications present a viable market for our business model. Our success here was only made possible with close customer participation resulting in mutual benefit for both as well as for the marketplace in general.

For more information about E-tec Interconnect Ltd., email info-us@e-tec.com

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INDUSTRY NEWS

(continued from Page 15)

interposer substrates is expected to significantly impact future glass wafer demand, and the 2.5D glass interposer will attract many newcomers. The use of glass interposers in packaging will certainly be on the high-volume manufacturing roadmap within a few years, noted Yole.

The top five players in the glass substrate market hold almost 80% of the market according to Yole. In the semiconductor industry, the glass substrate market is split among five main suppliers: Schott (G), Tecnisco

The glass substrate market's overall size in wspy: breakdown by functionality
(Source: Glass Substrates for Semiconductor Manufacturing, Yole Développement, April 2013.)

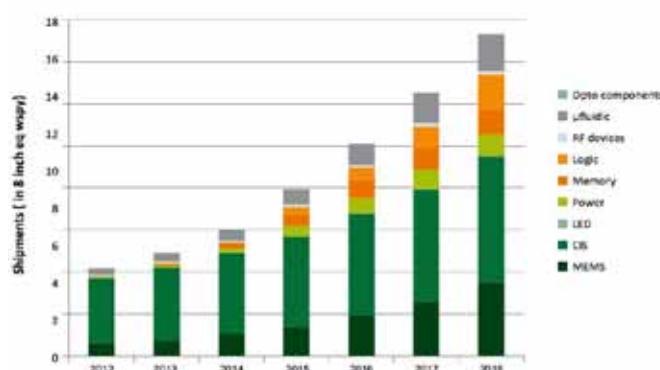


Figure 2: The glass substrate market's overall size in wspy: breakdown by functionality. SOURCE: Glass Substrates for Semiconductor Manufacturing, Yole Développement, April 2013.

(JP), PlanOptik (G), Bullen (US) and Corning (US) will share more than 70% of the \$158M glass substrate market this year, driven mainly by demand for WLCapping.

In the midst of this growing market, semiconductor glass suppliers are trying to differentiate themselves by proposing a variety of glass substrate material properties with a good coefficient of thermal expansion (CTE), solid thermal properties, and no polishing/grinding steps required, which would result in reduced costs.

Many glass substrate suppliers such as AGC, Corning and HOYA are expected to increase their business in the next few years because they are quite aggressive in 2.5D interposers and

glass carrier wafers, and are expected to ramp-up into high-volume production. Since the big players are already deeply entrenched in the glass market, it will be very challenging for a new entrant to break through in the foreseeable future said Yole.

New Venture Research Issues 2013 IC, Packaging, and Economic Outlook



New Venture Research has issued its 2013 IC, packaging, and economic outlook ("The Worldwide IC Packaging Market," 2013 Edition), which is summarized here. After 2009 being the worst depression since the Great Depression in the 1930s through the mid-1940s, the integrated circuit (IC) industry had a boom in the second half of 2010. On the heels of this boom, 2011 began

well, but a slowdown in the market in the second half of that year caused a negative growth rate, a pattern that repeated in 2012. The inventory corrections in these two years did not alter the fact that both 2011 and 2012 still had near-record-breaking unit and revenue figures. The growth rates of 2010, with revenue growing 40% over 2009 and units 35.5%, however, were not sustainable.

Sales of tablets, smart phones, and automobiles are going well, and they are carrying the rest of the

economy forward into recovery. Apple Computer had one blockbuster product after another, with the iPod, iPad, and iPhone. Apple, once the most valuable company in the world, is now number two behind Samsung. Producing portable electronic gadgets that connect people electronically with the world around them is clearly a good business model. Even in the depths of the recession of 2009, electronic gadgets that connected people via the Internet and sold for under \$400 did well.

Figure 3 illustrates IC revenue growth for the entire IC chip market. Revenue growth will be a steady increase through 2017, a similar trend to unit growth, and will have a 5.2% CAGR. The packaging revenue percent of IC revenue is shown at the bottom of this figure. The packaging revenue percent of IC revenue is displayed as well. Though it varies greatly by device type, overall packaging consumes slightly more than 15% of the total chip revenue and will rise to slightly more than 16%.

IPC: Leading Indicators Offer Optimism Despite Disappointing February

While North American manufacturing begins another slow recovery and leading indicators point to modest business expansion in the coming months, the PCB industry has not

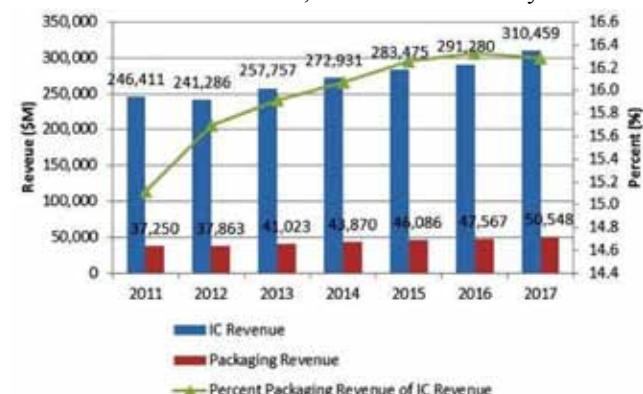


Figure 3: IC and Packaging Revenue Forecast and Percent of Packaging of Total, 2011–2017.

yet felt the effects of this turnaround, according to the latest edition of the IPC North American PCB Market Report. The report shows what market segments underlie the disappointing 10% contraction in February PCB sales versus February of last year.

The flexible circuit segment was particularly hard hit in February after a strong start to the year in January. "Monthly data can be very volatile, especially in the flexible circuit segment of the PCB industry," said IPC Market Research Director, Sharon Starr. "Actual trends only emerge from several months of data." Flexible circuit sales in North America strengthened in the second half of 2012 and the book-to-bill ratio for flexible circuits, while in negative territory, has steadily increased since October 2012.

Bookings increased slightly in the rigid PCB segment in February 2013, pushing the total PCB book-to-bill ratio up to 1.06. After a long, slow decline in 2012, the PCB book-to-bill ratio has been positive since January 2013. The ratio reflects the three-month rolling averages of orders over sales and is a three- to six-month leading indicator for sales growth.

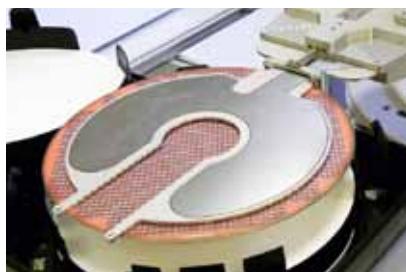
"The decline in PCB sales from January to February was a bit surprising in light of seasonal trends, but it reflects the negative book-to-bill ratios in the fourth quarter of 2012," added Starr. "The ratio has been trending up for the past three months and is now in positive territory. This suggests that the PCB industry's recovery is merely delayed and we hope to see some improvement in the coming months."

Brewer Science Breaks Ground on New High-Volume Manufacturing Facility

Brewer Science, Inc., recently broke ground on a new facility at the Rolla National Airport that will be used to produce advanced materials needed for manufacturing next-generation smartphones, tablet computers, and other microelectronic devices. The groundbreaking ceremony, held at the new site, was attended by many local, state, and federal officials who helped make the project possible noted the company.

The new 25,000 square-foot manufacturing facility will expand Missouri's advanced technology footprint and create 65 new high-tech jobs for the state. Brewer Science, one of the world's leading technology

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companies, is part of Missouri's emerging I-44 technology corridor, which spans the state from St. Louis to Joplin. The construction of the Brewer Science facility is an initial step in a broader plan to transform Rolla National Airport into a manufacturing and transportation hub.

"As the Brewer Science customer base has grown and expanded around the globe, we have continued to grow and expand in Missouri, where we are proud to maintain our global headquarters," said Dr. Terry Brewer, CEO of Brewer Science. "Our new facility will help make possible the next generation of smartphones, tablet computers, and additional high-tech innovations still to come to market. We are excited about the future of technology and Brewer Science's future in Missouri. We are grateful to the local, state, and federal officials with us today who support Missouri manufacturing and the research and development that is the lifeblood of Brewer Science."

"The expansion of Brewer Science is good for private sector job creation and economic opportunity in Missouri," said U.S. Senator Roy Blunt (Mo.). "Brewer Science is consistently at the forefront of high-tech and advanced manufacturing fields, and this new facility continues to advance our shared goal of creating and keeping good-paying, high-skilled jobs statewide."

This newest Brewer Science building incorporates many of the industry's highest standards. Utilizing Leadership in Energy and Environmental Design (LEED) guidelines, the new facility will use geothermal systems for heating and cooling. Designed to be energy-efficient and environmentally sensitive, in addition to conforming to state-of-the-art safety specifications, the building will have the infrastructure to manufacture high-volume products that meet or exceed International Organization for Standardization

(ISO) requirements.

Zestron Adds Arbell Electronics Inc. As New Distributor Within Canada

Zestron recently announced the addition of Arbell Electronics Inc. as its new exclusive distributor within Canada. "Arbell is Canada's largest authorized distributor of production equipment and supplies to our industry," said Michael McCutchen, Vice President Americas and South Asia. "With their national sales team of dedicated product knowledge experts, coupled with Zestron's application technology engineers and R&D support, we will broaden our sales coverage and improve our service and distribution support to our ever growing customer base throughout the provinces." Founded in 1968, Arbell has been serving the electronics industry for over 45 years.

Singapore's UTAC to Co-Develop 2.5D Through-Silicon-Interposer with A*STAR's IME

The Agency for Science, Technology and Research's (A*STAR) Institute of Microelectronics (IME) and United Test and Assembly Center (UTAC) have announced a collaboration to develop a 2.5D through-silicon-interposer (TSI) platform that will enable UTAC to join the list of suppliers in offering fine-pitch 2.5D TSI packaging solutions.

This collaboration builds on the technology expertise of both partners and leverages IME's 300mm through-silicon-via (TSV)/TSI fabrication and assembly infrastructure to develop and prototype 2.5D TSI-based systems. IME will also contribute its R&D experience in design and advanced packaging to develop optimized solutions to address electrical, thermal, thermo-mechanical and reliability requirements for applications including mobile devices, such as tablets and smart phones. The optimized 2.5D TSI technology from this collaboration will be transferred to UTAC for high-volume manufacturing,

enabling UTAC to shorten its time-to-market significantly.

"IME's strong commitment in accelerating industry adoption of 2.5D and 3DIC design and manufacturing, as well as our breadth of expertise in 200mm and 300mm back-end-of-line (BEOL) capabilities, present an attractive value proposition to companies to collaborate with us," said Prof. Dim-Lee Kwong, Executive Director of IME. "IME looks forward to working with our partners to develop innovative 3D IC solutions and carry 3D integration forward toward numerous applications that can be commercialized."

"Leveraging on IME's leading 3D IC capabilities, we believe that we will be able to better respond to market demands and support our customers with services that offer them faster time-to-market, strengthening our leadership in the 3D IC arena," said Dr. William John Nelson, Group President and Chief Executive Officer of UTAC.

IME Launches Copper Wire Bonding Consortium II

The Institute of Microelectronics (IME), a research institute of the Agency for Science, Technology and Research (A*STAR) in Singapore, has launched the Copper (Cu) Wire Bonding Consortium II. The consortium, which follows Phase I launched in 2010, aims to improve the reliability of semiconductor devices by tackling copper wire bonding issues related to corrosion and stress. Members of this consortium span the semiconductor supply chain including Atotech S.E.A., Globalfoundries, Heraeus Materials, and Infineon Technologies.

In releasing the news, IME noted that copper, which offers favorable cost, performance, quality and reliability benefits over gold, has become one of the preferred materials for wire bonding interconnects in microelectronics. Today, however, the industry still faces

many technical challenges in developing copper as the best choice for chip-to-package interconnection. One of the key technical issues is related to copper's hardness relative to gold, which requires bonding parameters to be very well controlled in order to eliminate the risk of damaging bond pads and underlying structures. Another daunting challenge of using copper is its reactivity with oxygen in the surrounding air, which causes corrosion-related problems. These two issues can affect the reliability and quality of semiconductor devices, explained IME.

Against this background, the IME Cu Wire Bonding Consortium II will conduct a study on corrosion and the mechanisms on the effect of various packaging materials. To understand the effects of copper wire hardness when bonding on different materials, the consortium will carry out modeling and characterization of copper wire bonding stress using stress sensors developed under the scope of Phase I of the Cu Wire Consortium to provide an improved technique of measuring wire bonding stress. The outcome of this work will enable semiconductor manufacturers, as well as test and packaging houses, to develop solutions to improve product reliability, especially those targeted at high-reliability applications.

"Globalfoundries is pleased to be in this consortium as the first phase of our partnership has successfully resulted in optimizing 0.7 mil in copper wire bonding on our 40nm product and passed the JEDEC reliability test," commented Mr. K. C. Ang, Senior Vice President and General Manager for Globalfoundries Singapore. "The success has brought us to the next phase of collaboration where the process will be tested on our advanced 28nm product. We see this industry collaboration truly augmenting the value proposition we have on offering

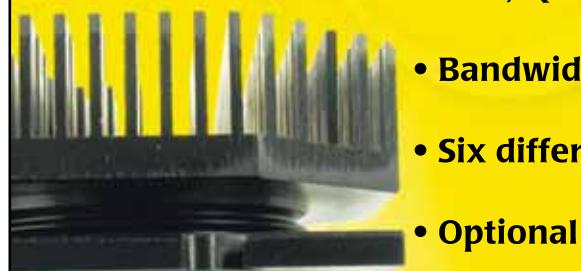
quality and cost effective wafer manufacturing to our customers."

"Infineon has been part of the Copper Wire Bonding Consortium since it first launched in 2010," said Mr. Guenter Mayer, Senior Director, Package Technology and Innovation,

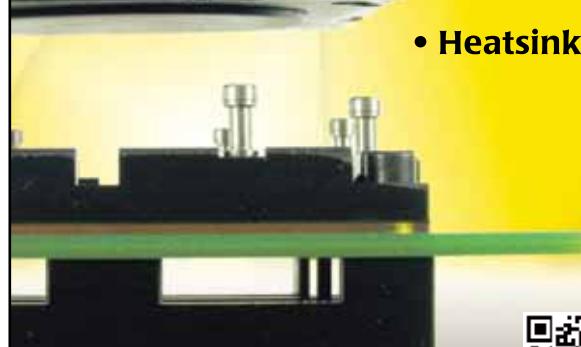
Infineon Technologies Asia Pacific. "Today, our interest lies in copper wire bond interconnect performance and reliability in semiconductors that can meet the stringent quality requirements of automotive and Industrial applications."

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Hermes Testing Solution Inc. and Invensas Corporation Enter Into Long-term Technology and Patent Licensing Agreement

Invensas Corporation, a wholly owned subsidiary of Tessera Technologies, Inc. (Nasdaq: TSRA), announced that Hermes Testing Solution Inc., a subsidiary of Hermes Group headquartered in Taiwan, has signed a long-term license agreement to manufacture and sell xFDTM-based products into the tablet, mobile computing, and data storage markets. Hermes Group and Hermes Testing Solution also has facilities in Singapore, Malaysia and China.

"We are delighted that Hermes has chosen to license our xFD technology portfolio in response to demand from original equipment manufacturers (OEMs) and original design manufacturers (ODMs)," said Simon McElrea, President of Invensas. "Having already licensed xFD at the OEM demand level and memory chip supply level in the first quarter of this year, our next step was to enable the manufacturing and supply chain integration base. Hermes' location in Taiwan, its broad slate of customers, and its established network of Asian supply chain partners made it a perfect candidate."

William Wang, GM of Hermes Testing Solution, said that "xFD is well aligned with Hermes' business model of providing high value-added products and services to the semiconductor industry. The technology enables much smaller and higher performance devices to be built for important growth markets, such as tablets, mobile devices, and next generation servers."

Fox Electronics Signs Global Distribution Agreement with Arrow Electronics

Fox Electronics has signed a worldwide distribution agreement with Arrow Electronics. Arrow will

now offer Fox's range of crystals and XpressO configurable oscillators, through its worldwide network of 120,000 OEMs, contract manufacturers and commercial customers via almost 400 locations in 53 countries, as well as its extensive online product marketplace. In addition to Fox's XpressO configurable oscillators and the XpressO TCXO, Arrow now offers a portfolio of frequency control products, including quartz crystals, clock oscillators, TCXOs, VCXOs, OCXOs, and crystal filters, through the new relationship.

Aries Electronics Has a Distribution Contract with SMD Inc.

Aries Electronics has authorized SMD Incorporated of Irvine, California to distribute the company's full range of electronic connector products throughout the USA through its locations in Southern California, New Hampshire, and Florida. SMD Inc. is a provider of electronics and electrical components, services, and logistic solutions for industrial manufacturing companies in North America. The company offers a variety of products from an authorized supplier base and provides technical and sales expertise on all product lines and commodities.

Plessey Semiconductors Expands Its Distribution Network in China with Alphatec Agreement

Plessey Semiconductors and Alphatec have signed a distribution agreement for the Greater China market. The cooperation will market Plessey's EPIC™ sensors (Electronic Potential Integrated Circuit) in synergy with Alphatec's system solutions for applications in the fields of e-health, automotive, sports, fitness and smart lighting. The latter links in with Plessey's high brightness, MAGIC™ LED technology.

By expanding Alphatec's portfolio with Plessey's RF solutions and power management products (LDOs)

for applications in digital video broadcasting (DVB) and set-top box products, Alphatec will be able to offer more complete solutions that will fulfill advanced customer requirements.

Integra Technologies Celebrates 30 Years

Integra Technologies, LLC, is celebrating its 30th year as a leading supplier of integrated circuit test and evaluation services in the U.S. and Europe. Integra was started in 1983 as part of NCR Corporation with a small test floor in Wichita, Kansas. Today, Integra's test facility in Wichita has over 41,000 square feet of state-of-the-art test equipment and engineering development offices.

Beginning with just 30 employees, Integra has grown to over 200 employees and has been employee-owned since 2008. Integra believes this long-term growth and longevity is due to the loyalty of its customers and Integra's ability to change to meet current market requirements such as the increasing complexity of integrated circuit devices and the ever-growing diversity of end-customer applications.

"The employee owners of Integra would like to thank our customers for their continued confidence in us over the past 30 years and assure them that we will be here to serve them for the next 30 years as well," said Becky Craft, President, Integra Technologies.

Nordson EFD Celebrating It's 50th Anniversary

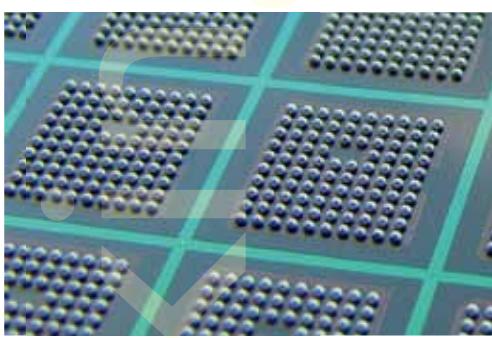
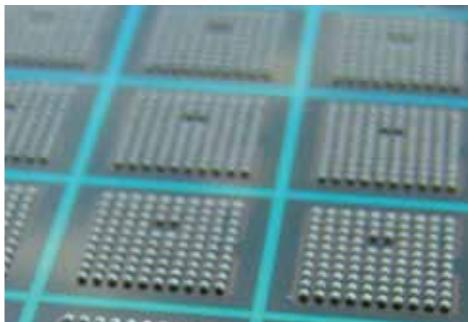
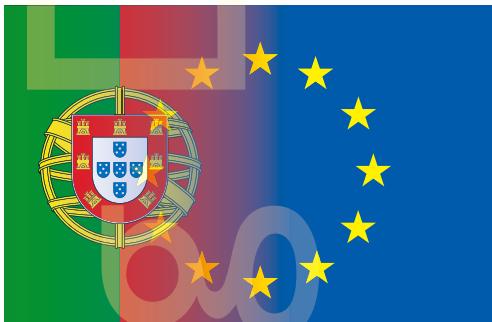
Nordson EFD, a Nordson company (Nasdaq: NDSN), will celebrate its 50th anniversary throughout 2013. "This year marks 50 years of commitment to developing innovative technologies that help our global customers build their own products better, faster and more cost-effectively," said Ken Forden, Nordson EFD Vice President and General Manager. He noted that the company's recent enhancements to

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its PICOTM dispensing systems are an example of its focus on understanding and anticipating the fluid management needs of end users. "We more than tripled the speed so they can operate continuously at up to 500 cycles per second." EFD was founded in 1963; after years of steady growth, the company was acquired by the Nordson Corporation. Today, Nordson EFD has more than 600 employees in more than 30 countries.

Amkor Technology Appoints Steve Kelley President and CEO

Amkor Technology, Inc. (NASDAQ: AMKR) has appointed Stephen D. Kelley to serve as President and Chief Executive Officer and as a director of the company, effective May 8, 2013. Mr. Kelley succeeds Ken Joyce, who previously announced his intention

to retire. Mr. Kelley's appointment follows a comprehensive, six month search process conducted by the Board of Directors with the professional assistance of a global executive recruiting firm.

"We have been investing significant resources in the key packaging and test technologies that support the rapidly growing market for smartphones and tablets, and today we are well-positioned to take advantage of significant growth opportunities in mobile communications and our other end markets," said James J. Kim, Amkor's executive chairman of the board of directors. "Steve Kelley has a wealth of experience helping major global semiconductor companies grow revenues and increase profitability. With his strong record of success, deep customer knowledge and great drive, Steve is the ideal CEO to lead Amkor."

Most recently, Mr. Kelley served as Chief Executive Officer of Scio Diamond Technology Corporation, and as a senior advisor to Advanced Technology Investment Company, the Abu Dhabi-sponsored investment company that owns Globalfoundries. Mr. Kelley, 50, has more than 25 years of experience in the global semiconductor industry, including: Executive Vice President and Chief Operating Officer of Cree, Inc. from 2008 to 2011; Vice President/General Manager - Display, Standard Logic, Linear and Military Businesses at Texas Instruments, Inc. from 2003 to 2008; in various positions with Philips Semiconductors from 1993 to 2003 including Senior Vice President and General Manager; and in various positions with National Semiconductor Corporation and Motorola Semiconductor. Mr. Kelley holds a BS in Chemical Engineering from Massachusetts Institute of Technology and a JD from Santa Clara University.

"I'm very excited to join the Amkor team," said Mr. Kelley. "Throughout its history, Amkor has been a pioneer and technology leader, and I look forward to the opportunity to build on that success."

AG Semiconductor Services Appoints Senior Director of Sales

AG Semiconductor Services, LLC (AGSS), announced that Michael (Mike) Mardesich joined the company in the role of Senior Director of Sales. An industry veteran, Mardesich is tasked with developing sales strategies, managing sales and contract remarketing services and managing AGSS' global sales force.

Mardesich has over 30 years of experience in management, sales and equipment valuations in the electronics manufacturing used equipment industry.

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Prior to joining AGSS, Mardesich was the Senior Vice President of Sales with GE Capital Global Electronics Services. He also held similar positions with Comdisco Electronics Group, where he was a founding member. He was an original board member of the SEC/N used equipment consortium.

"Mike brings energy and intensity that are ideally suited to support the expansion of our global market presence," said Julian Gates, a Managing Director of AGSS. "He is well known throughout the electronics industry; this experience and his skill set will help solidify AGSS as the leading provider of used equipment and customer solutions to the electronics manufacturing industry."

The company also announced that former head of sales, Tim Johnson, will transition laterally to focus on growing AGSS' turnkey services as well

as spearhead development of future revenue channels including products and services that support non-traditional IC manufacturing such as MEMS, compound semiconductor, LED and photovoltaic. In his new role as Senior Director, Johnson will continue to support sales, remarketing and value added services as well.

Endicott Interconnect Technologies, Inc., Announces Retirement of CEO, Jay McNamara

Endicott Interconnect Technologies, Inc. (EI) announced that CEO, Jay McNamara, retired as of Friday April 12, 2013. Mr. McNamara had been the President & CEO of Endicott Interconnect since its inception in 2002 as a divestiture of IBM's Microelectronics Division.

Mr. McNamara took EI from a company with only a few customers,

in a couple of markets, to a company with dozens of customers, in a variety of markets including: high-performance computing, aerospace & defense, medical and industrial. Mr. McNamara's leadership was a critical factor in pushing the company forward and helping EI to become a respected name in the worldwide electronics industry.

"I've had the unique opportunity of working alongside Jay for a number of years and I've always been fascinated with his ability to really connect with both employees and customers alike. He's been the true visionary for EI over the past 10 years and the company would not be where it is today without his outstanding leadership and commitment to the organization. He will be truly missed," stated Chief Technology Officer, Raj Rai. McNamara will be succeeded by Jim Matthews Jr.

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Products News

Rudolph Adds to Product Offerings With Selective Asset Purchase from Tamar

Rudolph Technologies, Inc. (NASDAQ: RTEC) purchased selected assets, including a strong patent portfolio, relating to metrology capability from Tamar Technology, Newbury Park, Calif. The addition of Tamar's advanced metrology technologies to Rudolph's existing inspection and metrology systems will allow the company to address the emerging need for fast, precise three-dimensional (3D) measurement capabilities in the rapidly-growing advanced packaging market sector.

Michael Jost, Vice President and General Manager of Rudolph's Inspection Business Unit, noted, "The purchase of these assets adds new capabilities to our technology portfolio, which addresses an emerging need for 3D measurements to control copper pillar bumping in advanced packaging processes." Jost also said that Tamar's technology is already well known and widely used. "Integrating it into our NSX® and F30™ inspection and metrology platforms adds critical capability and value to an established and reliable tool set." Jost pointed out that several of its customers brought the technology to the company's attention. "It was readily apparent that the acquisition of these assets would significantly enhance the breadth of our advanced packaging solutions. In addition, this purchase gives Rudolph a significant patent portfolio that we plan to fully leverage. The integration work is essentially complete and we expect to receive initial system orders in the coming months."

Rudolph also said that the acquisition aligns fully with its declared strategy to leverage its front-end and back-end expertise in the burgeoning market for advanced packaging process control. Copper pillar bumping for flip-chips has been forecast to grow at a 35% CAGR

from 2010 to 2018, noted Jost. "While copper pillar bumping processes are the most significant immediate application, Tamar's technology portfolio provides uniquely capable critical measurements required in several advanced packaging applications." Jost further explained that one application uses infrared light to measure TSV depth from the backside of the wafer, thus avoiding the limitations on via aspect ratio encountered by most frontside measurement approaches.

Terms of the transaction were not disclosed. However, Rudolph noted that the asset purchase agreement includes an earn-out contingency that, if met, would bring the total transaction value to approximately \$10 million. The company also noted that it expects the transaction to be accretive to earnings within the first 12 months.

Genesem Inc. Launches Its First IC Logic Test Handler System

Genesem, Inc., launched its first IC logic test handler system and commercialized its new business unit. The new model GTHS-2004 test handler is capable of transferring semiconductor devices - four at a time - from the tray loading area and conducting



GTHS-2004 Test Handler

testing and sorting of devices. It can handle 4,700 ICs per hour with 3x3 multi-chip packages (without test time). Synchronized motion control minimizes jamming. The company has systems capable of handling 8, 16, and 32 devices at a time to meet customer needs.

Ironwood Electronics Introduces a BGA Socket for a 0.5mm Pitch BGA 253-pin DDR4

Ironwood Electronics recently introduced a high-performance BGA socket for a 0.5mm pitch BGA 253 pin DDR4. The CG-BGA-5019 socket is designed for an 8X13.5mm package size and operates at bandwidths up to 10GHz with less than 1dB of insertion loss. The socket is designed with an easy open double-latch lid with an integrated compression mechanism. The contact resistance is typically 20milliohms per pin. The socket connects all pins with a 10GHz bandwidth on all connections. The socket is mounted using supplied hardware on the target PCB with no soldering, and uses the smallest footprint in the industry. The smallest footprint allows inductors, resistors and decoupling capacitors to be placed very close to the device for impedance tuning. The CG-BGA-5019 sockets are constructed with a high-performance and low-inductance elastomer contactor. The temperature range is -35°C to +100°C. The pin self-inductance is 0.11nH with a mutual inductance of 0.028nH. Capacitance to ground is 0.028pF. Current capacity is 2A/pin.

Signetics Qualifying Its QFN Solution for Automotive Applications

Signetics is currently qualifying its patented process for creating a quad-flat no-leads (QFN) solution that works for the high-reliability demands of

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the automotive semiconductor market. With a process for solder plating the sides of the leads of the company's standard QFN package, the end user gets a proven solution to meet automotive standards. It allows for automated visual inspection of the solder joints (instead of x-ray) once the assembled package is board mounted. Because the solution is based on high-volume QFN technology, it is very cost effective for automotive applications.

Advanced Thermal Solutions, Inc., Expands Choice of maxiGRIP™ Heat Sink Attachment

Advanced Thermal Solutions, Inc. (ATS) has added to its line of maxiGRIP™ attachment systems for fast, secure mounting of heat sinks to flip chips, BGAs and other hot PCB components. More than 200 variations of maxiGRIP are now available for use on a wide variety of IC packages.



maxiGRIP™ heat sink attachment

The maxiGRIP system features a plastic frame clip that snaps securely around a component's perimeter. A stainless steel spring clip runs through the heat sink's fin field and fastens securely to the plastic frame. As a result, the sink is mounted securely to the component with steady, even pressure. The spring clip is easily removed to allow a heat sink to be detached and re-attached. The frame clip is also removable.

The system provides strong, reliable attachment of heat sinks on vertically-

mounted components and on devices exposed to shock and vibration. Furthermore, the assembled system is very low profile, allowing use in restricted spaces. Unlike alternative screw-on or snap-on attachment systems, there is no chance of over or under-tightening the sink to the processor surface or having the heat sink pop out during transport or installation, or by shock and vibration.

The frame and spring clip designs have a proven thermal interface material such that the heat transfer from the hot chip to the heat sink is optimized and continuous. The system complies with NEBS standards and meets RoHS requirements. Parts are available for a wide range of heat sink shapes and sizes. Additionally, the systems are available with or without the associated heat sinks, from ATS and from Digi-Key.

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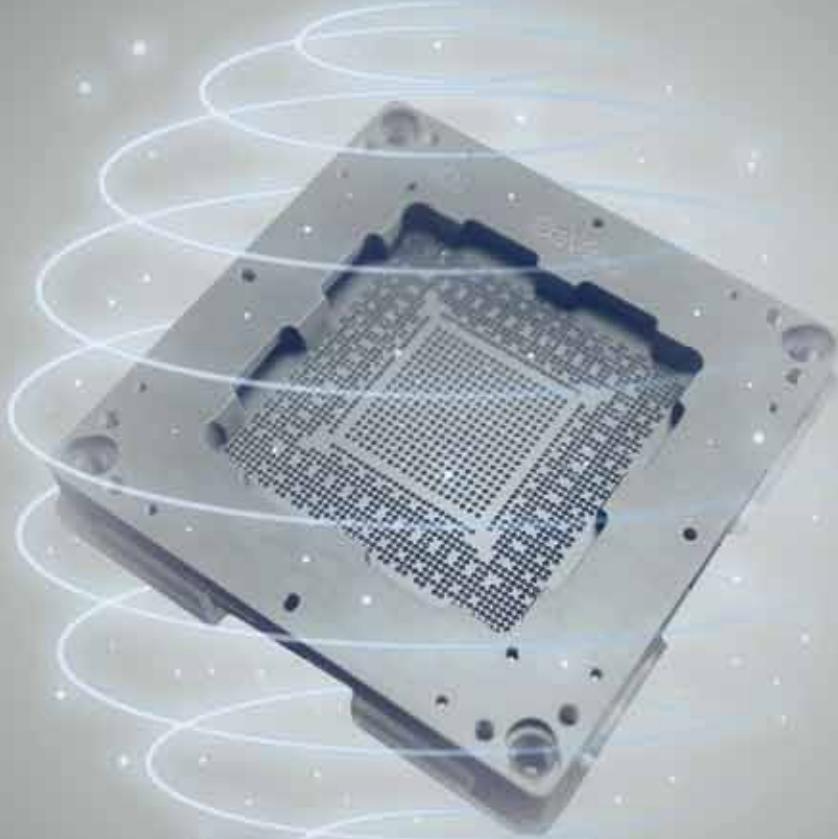
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