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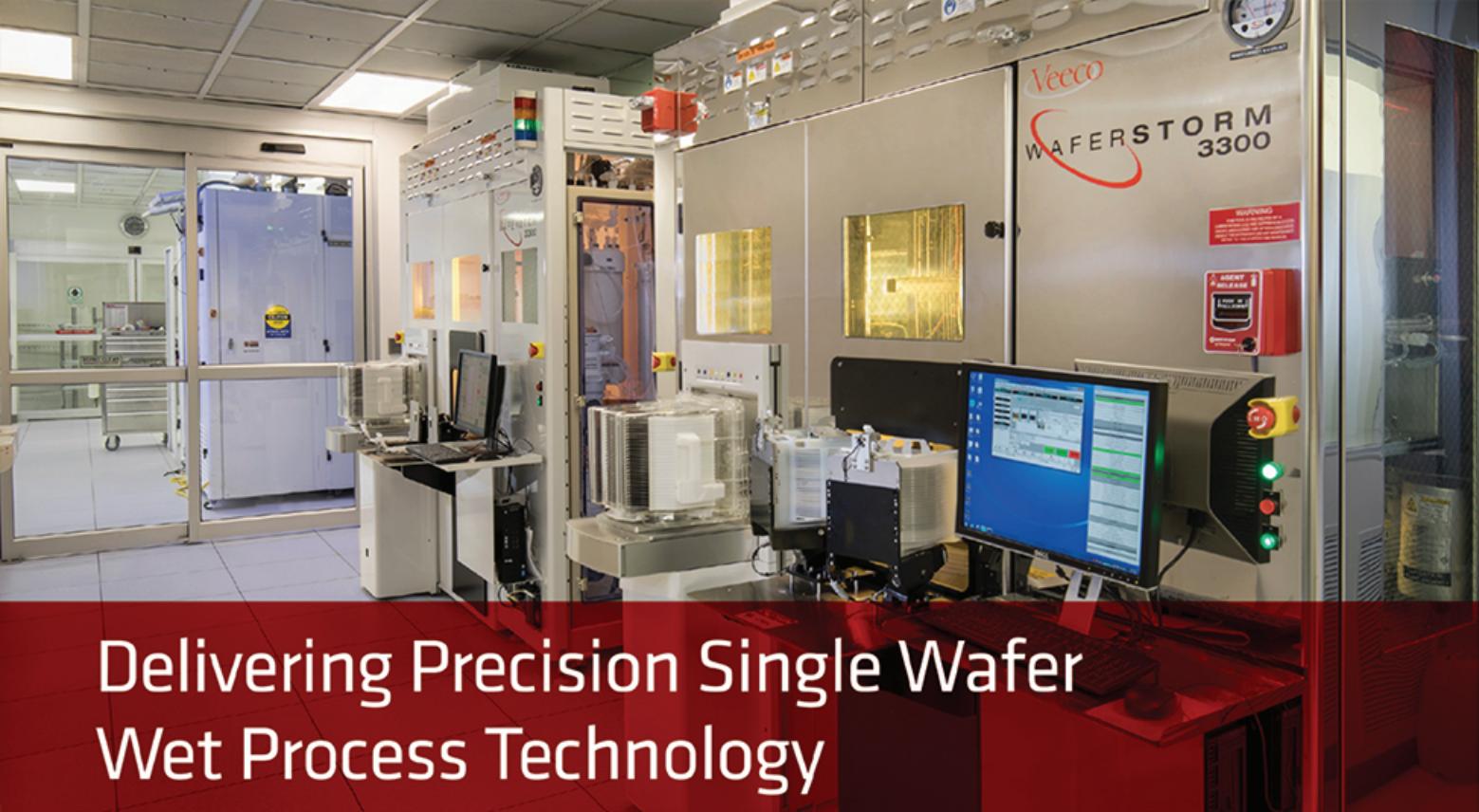
Volume 22, Number 2

March • April 2018

## FO for RDL-first process

Page 10

- Flexible hybrid electronics
- Transition from WLP to PLP
- HDAP connectivity verification
- Designed for manufacturing test (DfMT)
- Localizing defects in 3D chips
- Fan-out wafer- and panel-level technology for advanced LED packaging



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# CONTENTS

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Volume 22, Number 2



The photo is a graphical representation of an intermediate step in the RDL-first fan-out process whereby the dies are placed on top of the redistribution layer (RDL) architecture before overmolding. Prior steps in the process include application of a release layer to the carrier, followed by addition of redistribution layers on top of the release layer. The RDL-first fan-out process offers distinctive advantages in terms of reduced known good die (KGD) loss, improved line/space density, etc.

Cover photo courtesy of Brewer Science Inc.

## DEPARTMENTS

Technology Trends	Localizing defects in 3D chips Kristof J. P. Jacobs <i>imec</i>	7
Industry News		46

## FEATURE ARTICLES

	<b>Sacrificial laser release materials for RDL-first fan-out packaging</b> Ramachandran K. Trichur, Rama Puligadda, Tony D. Flaim <i>Brewer Science, Inc.</i>	10
	<b>Extending plating performance to enable FOPLP</b> Christian Ohde, Henning Hübner, Mustafa Özkök, Ralph Zoberbier, James Welsh <i>Atotech Deutschland GmbH</i>	17
	<b>Fan-out wafer- and panel-level technology for advanced LED packaging</b> Tanja Braun, Ruben Kahle, Stefan Raatz, Pascal Graap, Ole Hölick, Joerg Bauer, Karl-Friedrich Becker, Rolf Aschenbrenner <i>Fraunhofer Institute for Reliability and Microintegration</i> ; Steve Voges, Marc Dreissigacker, Klaus-Dieter Lang <i>Technical University Berlin, Microperipheral Center</i> ; Jürgen Moosburger, Frank Singer, Lutz Höppel <i>OSRAM Opto Semiconductors GmbH</i>	26
	<b>HDAP connectivity verification: what you need to know</b> Tarek Ramadan <i>Mentor, a Siemens Business</i>	31
	<b>Have you designed for manufacturing test?</b> Gerard John <i>Amkor Technology, Inc.</i>	37
	<b>Flexible hybrid electronics: System as package</b> Wilfried Bair <i>NextFlex</i>	43



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The International Magazine for Device and Wafer-level Test,  
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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. In the U.S. subscriptions by first class mail are \$125 per year. Subscriptions outside of the United States are \$225 per year to other countries.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine  
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3

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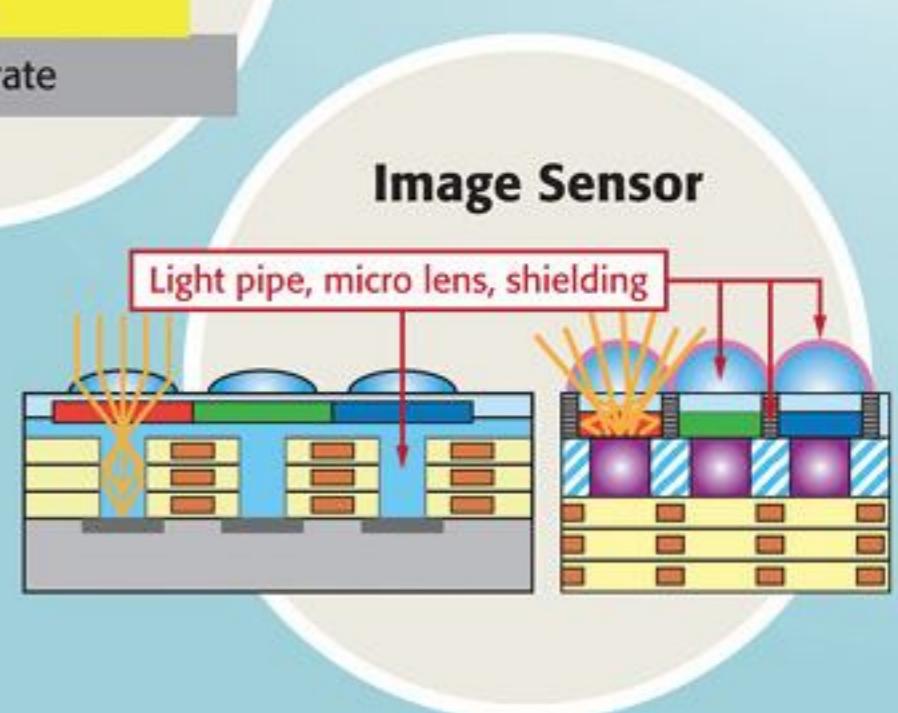
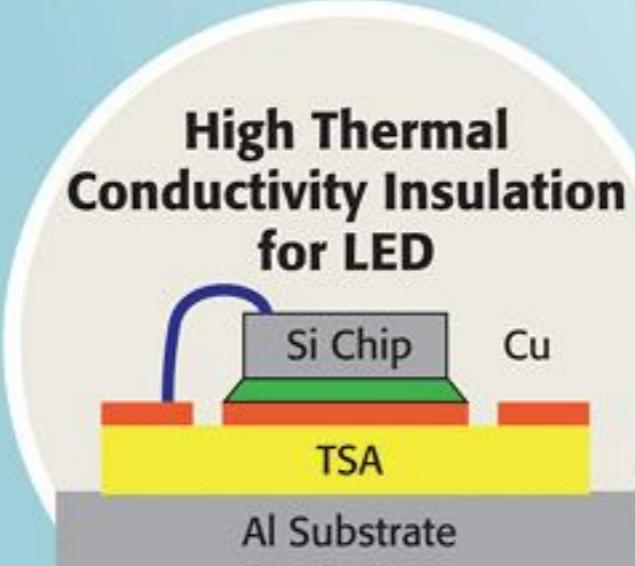
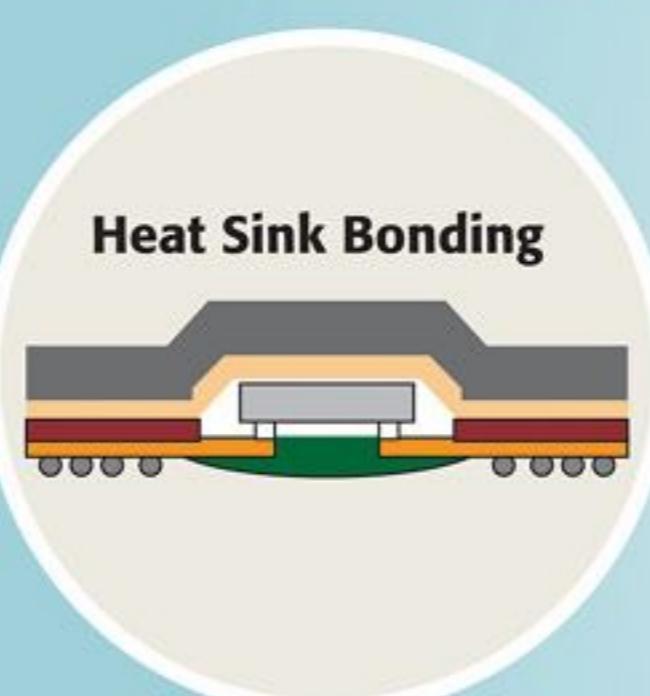
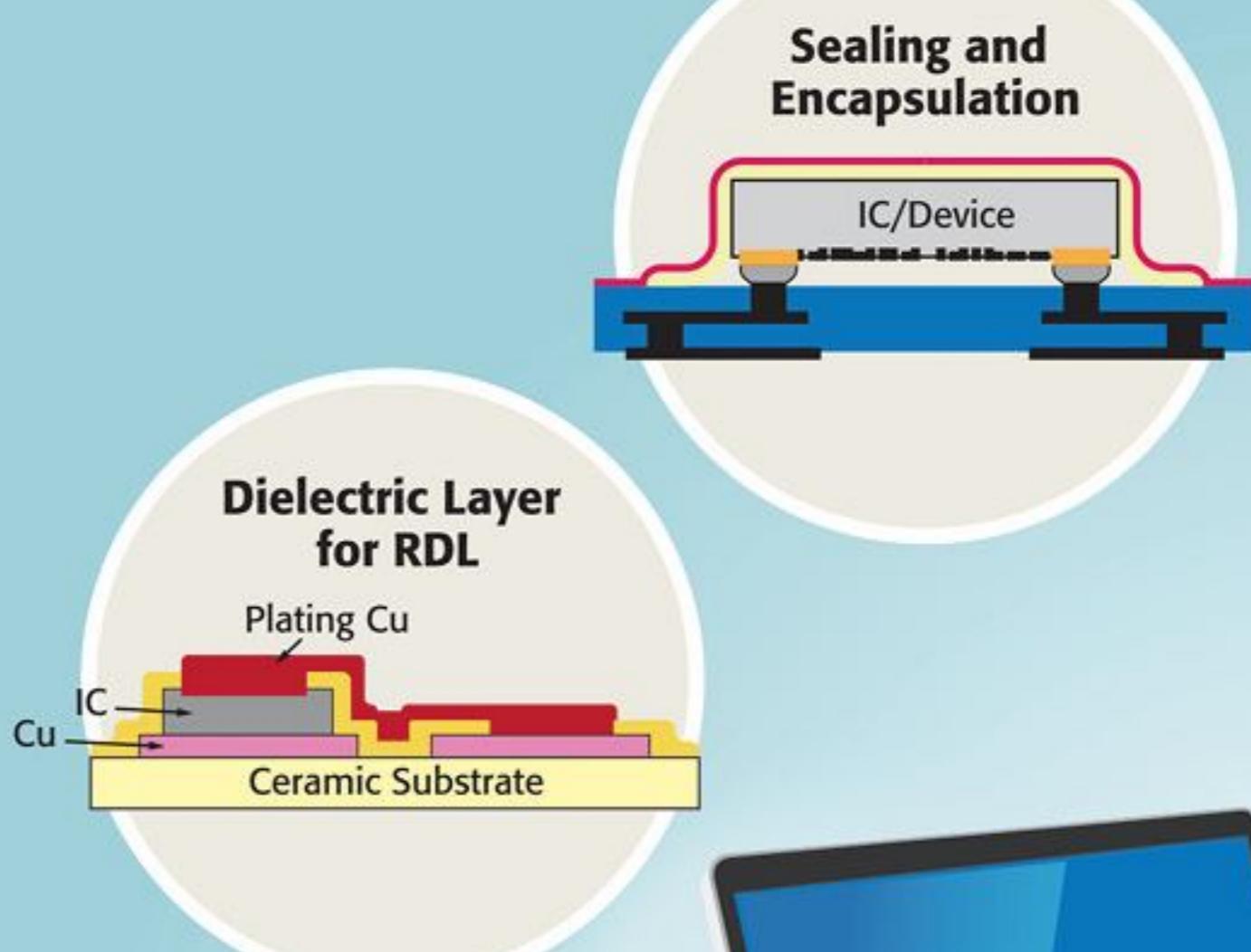
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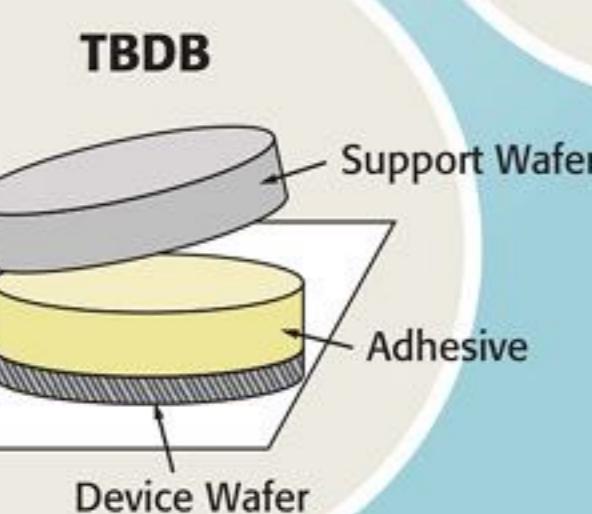
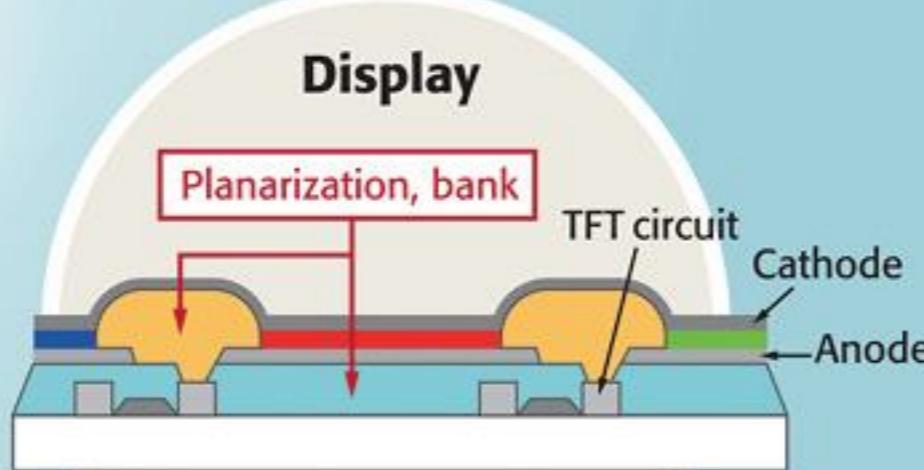
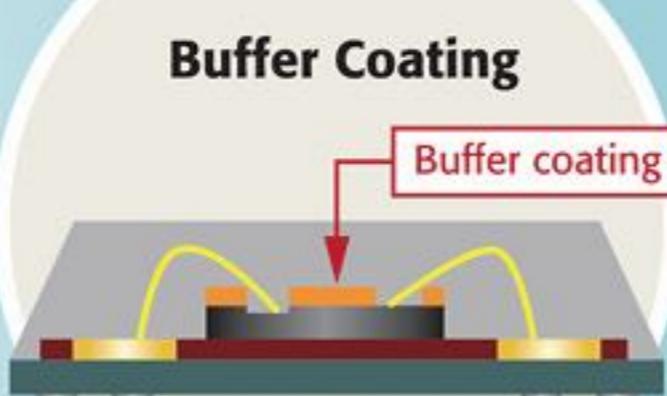
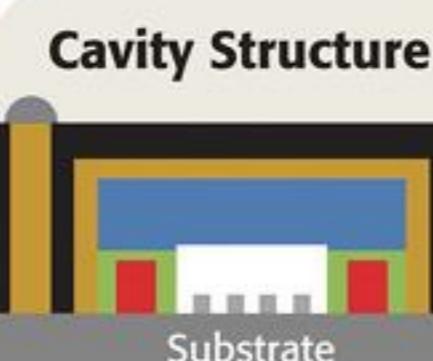
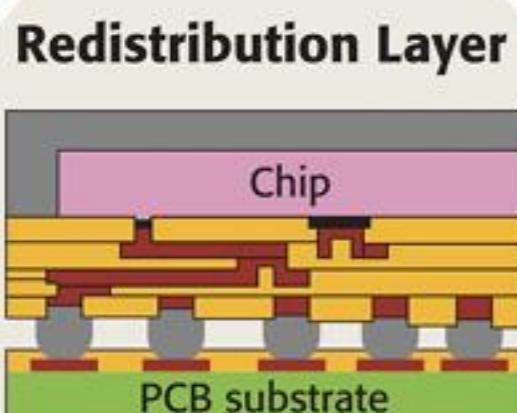
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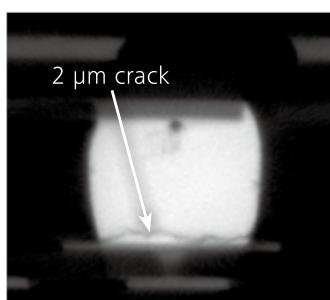


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Image courtesy of AMD Failure Analysis Lab, Singapore

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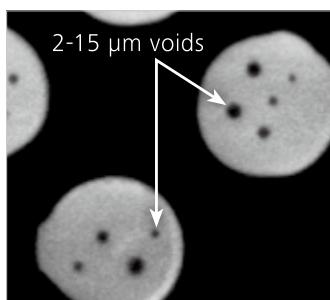


*Virtual cross section*

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*Virtual planar section*





## Localizing defects in 3D chips

By Kristof J. P. Jacobs [imec]

3D chips enable high-performance and cost-effective systems. But, as is the case with every new technology, it comes with new reliability and failure issues. One of these are faults – electrical opens and shorts – in through-silicon vias (TSVs) that interconnect the stacked chips. We have developed a new technique – called light-induced capacitance alteration (LICA) – that can rapidly localize these interconnection failures in a non-destructive and cost-effective manner at wafer scale.

### Through-silicon vias form the heart of 3D chips

Stacking chips on top of each other is a well-known approach to make small high-performance systems, with the possibility to combine different technologies for each layer in the system. 3D chips are used in high-bandwidth handheld products and high-density multi-chip memory. At the heart of the 3D chips are TSVs that provide the shortest chip-to-chip interconnects and the smallest pad size and pitch. The fabrication of these TSVs is a challenge, involving processes such as deep Si etch, chemical vapor deposition (CVD) oxide insulation, metal barrier and seed deposition, copper electroplating and chemical mechanical polishing (CMP).

These 3D specific processes and operations bring new reliability issues and failure mechanisms that require new failure analysis (FA) methodologies as traditional methods are becoming impractical for today's IC complexity. FA forms an important function for chip manufacturing as it provides valuable information for technology advancement and corrective action for quality and reliability improvement.

Today, only a limited number of nondestructive techniques are available to localize interconnection failures in 3D chips. The most promising techniques include magnetic field imaging (MFI), lock-in thermography (LIT), and electro-optical terahertz pulse reflectometry (EOPTR). While each of these techniques has unique characteristics and advantages (as well as limitations), they all require highly specialized and expensive FA apparatus that is not available in many laboratories.

To address the need for rapid, cost-effective, and scalable FA techniques, imec has developed a new method to localize interconnection failures in 3D chips (Figure 1). This technique, called LICA, exploits the effect of light on TSV capacitance for defect localization. Moreover, it only requires a scanning laser microscope, probing station, and capacitance meter, which are all readily available lab tools.

### LICA: defect localization with light waves

When a fault is present in the TSV and the light shines at this position, no change in capacitance will be detected as the electrical connection to the meter is interrupted. As a result, the fault can be localized. The technique builds on the capacitance-voltage (C-V) measurement method, yet also allows one to conduct the measurement on a local level. Unlike scanning capacitance microscopy (SCM), whereby the local capacitance is measured between the sample and a small tip that is scanned over the surface, LICA uses a focused laser beam that is used to induce a change in the TSV capacitance.

The photosensitivity of the TSV capacitance depends on many factors such as light wavelength and measurement frequency. We investigated the effects of these factors to determine the optimal measurement conditions for maximum signal strength. It was found that up to ~70% of the TSV capacitance can be made sensitive to light under optimal conditions. As the signal is typically in the range of a few tens of femtofarads (10-15fF), commercially available capacitance meters can be used for the detection. While the sensitivity of commercial meters may be sufficient for single-die measurements, the associated measurement time is considered too long for wafer-level

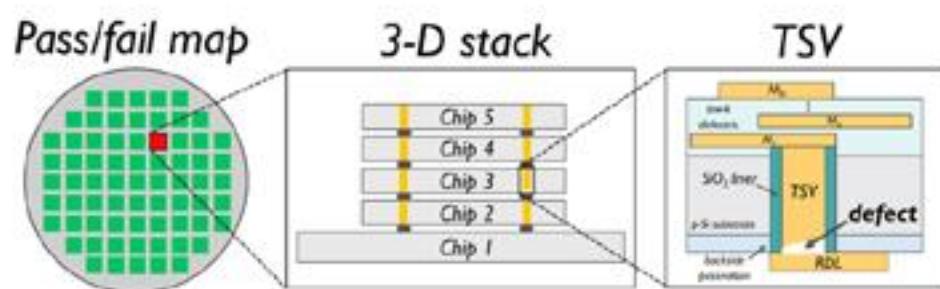


Figure 1: Through-silicon vias (TSVs) are at the heart of 3D chips. TSV failure analysis is indispensable to optimize the production of 3D chips.

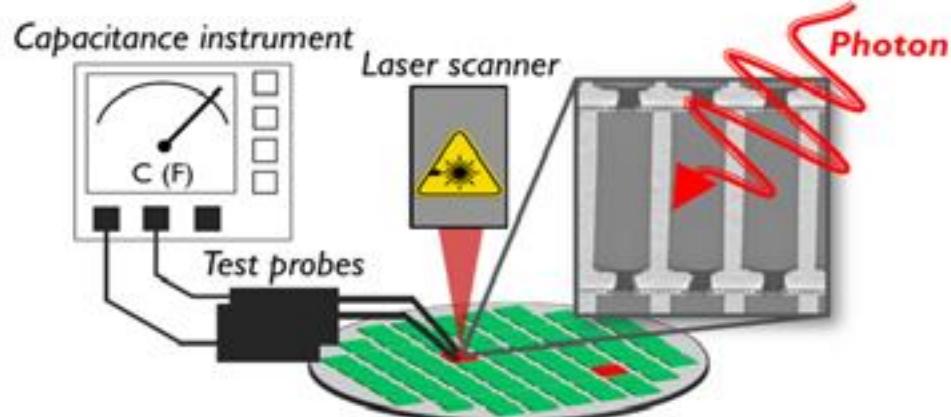


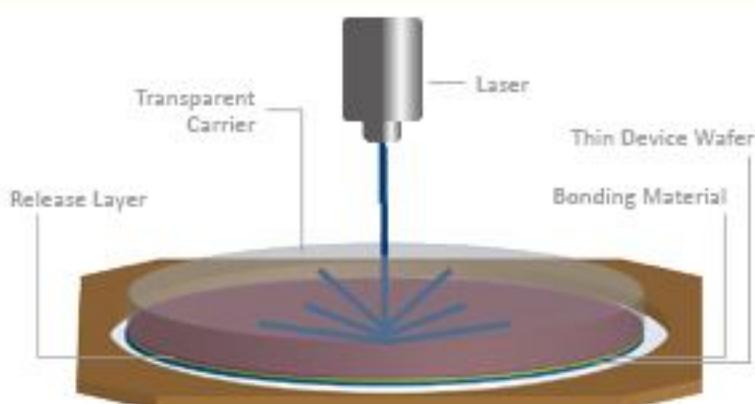
Figure 2: With LICA, the light-induced change in electrical capacitance is measured while scanning a focused laser beam over the 3D TSV structure under test. Test probes provide electrical connections from the structure to the measuring instrument. The location of the defect is marked when a distinctive change in the capacitance response is detected.

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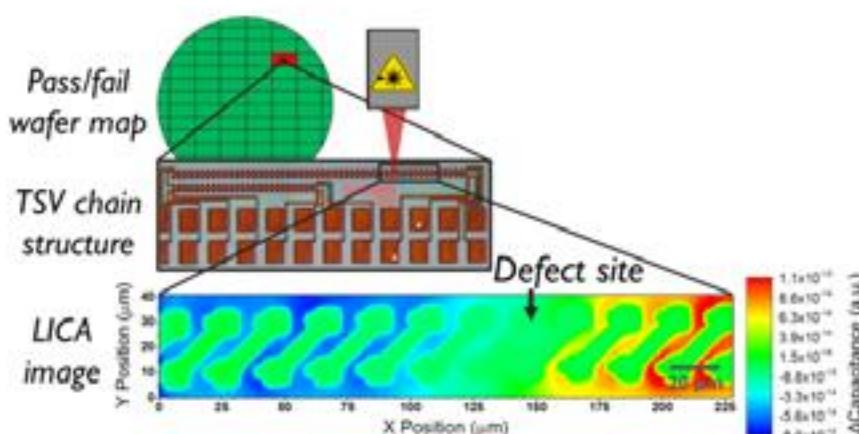
355 nm

defect screening. To address this, we developed an ultra-sensitive measurement instrument that further reduces the measurement time from hours to minutes ([Figure 2](#)).

### Technology demonstration

The technique has been demonstrated on a 5x50 $\mu\text{m}$  via-middle TSV chain structure fabricated in imec's state-of-the-art 300mm cleanroom. The purpose of a TSV chain structure is to evaluate the electrical continuity of multiple TSVs connected in a chain configuration. Measuring the chain resistance may indicate whether the structure is yielding or not, but it provides no information on the location of the defect. Accurate defect localization is required to understand the cause of the failure.

By scanning the focused laser beam over the chain, and applying a differential capacitance measurement technique, we have been able to successfully localize the open defect in the structure down to a single TSV ([Figure 3](#)). The required measurement time to localize the defect was less than five minutes. We expect that the analysis time can further be reduced to less than one minute by instrumentation optimization. Today, the LICA technique is used within imec to assist in the development of 3D integration technologies.



**Figure 3:** The pass/fail wafer map shows the location of the die failures but contains no information on the exact failure location in the structure. With LICA, failures can be localized more accurately down to a single TSV.

### Future work: thermal technique for stacked chips

A limitation of the LICA technique is that the region of interest should be accessible by the laser. Unlike dielectric passivation – which can be transparent to the light – metal layers, underfill, and epoxy overmold can block the path of the light. This can be a problem when stacked chips are being investigated and the faults are in the middle or bottom chips. That's why the imec research team is currently developing a second – similar – technique based on thermal waves (instead of light waves) that have the ability to penetrate through these materials. This technique will enable defect localization regardless of whether the defect is in the top or bottom die.

### Biography

Kristof J. P. Jacobs holds an MSc in Electronic Engineering and a PhD in Semiconductor Photonics from the U. of Sheffield, UK. He is a Postdoctoral Research Fellow from KU Leuven at imec; email [Kristof.J.P.Jacobs@imec.be](mailto:Kristof.J.P.Jacobs@imec.be)



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# Sacrificial laser release materials for RDL-first fan-out packaging

By Ramachandran K. Trichur, Rama Puligadda, Tony D. Flaim [Brewer Science, Inc.]

The semiconductor industry is in a new age where device scaling will not continue to provide the cost reductions or performance improvements at a similar rate to past years when Moore's law was the guiding principle for integrated circuit (IC) scaling. The cost of scaling below 7nm nodes is rising substantially and requires significant investment in capital equipment and R&D spending for next-generation lithography solutions. The demand for higher performance, smaller form factor, denser integration, and lower-cost devices is increasing more than ever due to significant progress made in products and services developed for consumer electronics, mobile devices, cloud computing, automotive, and various other applications. While the semiconductor industry continues to advance scaling of the integrated circuits, it is also turning to advanced packaging technologies to increase performance and integration while lowering costs.

One of the several challenges in heterogeneous integration is to bridge the gap in the I/Os available at the die level and the board level. At the die level, the trend has always been shrinking die sizes with increasing I/O density, so creative packaging technology is required to connect the dies to the board at such high I/O densities. Numerous evolving packaging technologies play a role in heterogeneous integration of devices, among which wafer-level fan-out (WLFO) packaging technology has been emerging as a dominant process. The WLFO process has been commercially deployed for several years with simple single-die designs, a single redistribution layer (RDL) on one side of a reconstituted wafer, and sparse silicon areas on thick reconstituted wafer profiles that resulted in thicker packages.

More recently, to address the performance, integration, and form factor demands from the end users, design and

process complexity of fan-out packages has continued to increase with multi-die packages, integrated passives, multi-RDL layers, and also 3D fan-out packages, while continuously reducing the package dimensions in the x, y, and z directions. As die size, process complexity, and package complexity increase, yield becomes a critical element of the fan-out packaging process. The traditional fan-out process uses a chip-first/RDL-last approach where a reconstituted wafer is built using known good dies followed by RDL build up on top of the reconstituted wafer. As the complexity of the reconstituted wafer and RDL grows, this process is susceptible to yield loss at the RDL level where a known-good die (KGD) is located in a bad RDL location. The yield loss could be due to several factors, including die shift, thermal expansion mismatch, poor lithography alignment, etc., resulting in the loss of an expensive KGD during the packaging process.

To avoid KGD loss during packaging, an alternate fan-out process was developed called RDL-first/chip-last fan-out packaging. In this process, the RDL was first built on a carrier wafer and KGDs were placed on top of a known good RDL location, thereby avoiding KGD loss. The RDL-first process also offers other advantages in terms of finer line/space dimensions for RDL to offer complex routing for denser device integration. In this paper, we present sacrificial laser release materials that support the development of RDL-first fan-out packaging by addressing some of the critical challenges encountered during the process.

## FOWLP technology

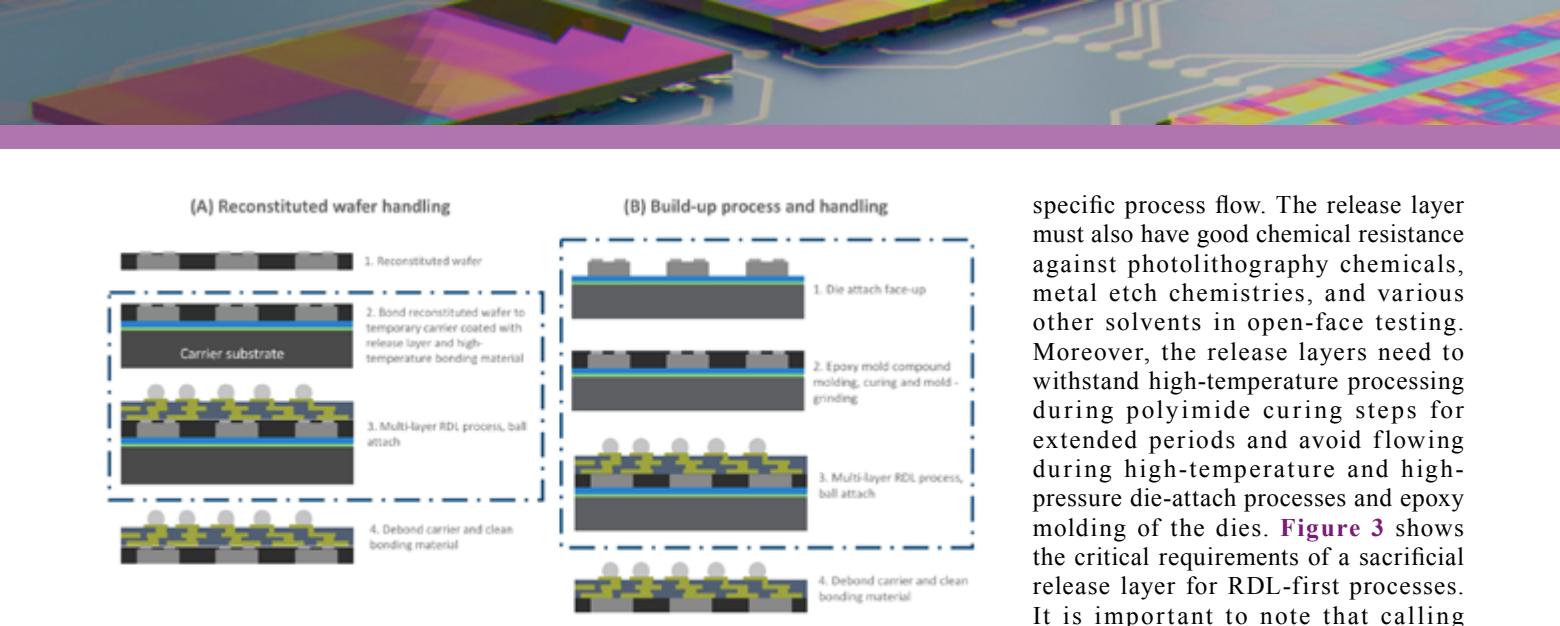
As mentioned above, the fan-out wafer-level packaging (FOWLP) technology broadly has two major process categories (discussed below): 1) chip-first/RDL-last fan-out, and 2) RDL-first/chip-last fan-out. Advanced integration schemes in both of the

process routes require some form of carrier-assisted process using a temporary bonding material.

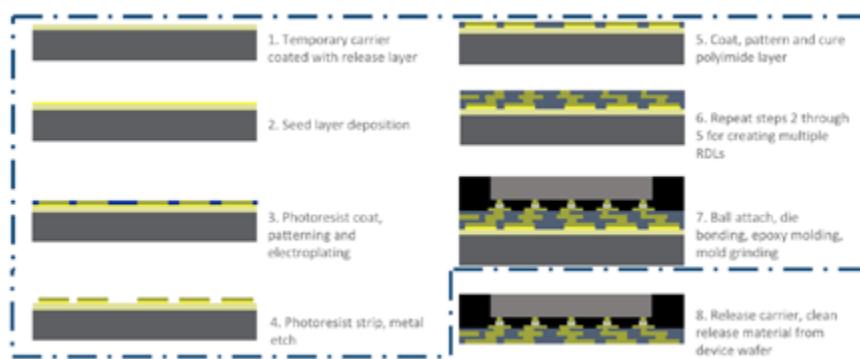
**Chip-first/RDL-last FOWLP.** The chip-first fan-out process utilizes a wafer reconstruction process in which KGDs from the original device wafer are picked and placed on a substrate and then over-molded with an epoxy molding compound and cured to create a heterogeneous and highly stressed substrate known as a reconstituted wafer. If the reconstituted wafers are thinner than 350 $\mu\text{m}$ , these wafers exhibit severe bow due to large internal stresses, and a high-temperature-capable temporary bonding material is essential to support the reconstituted wafer through the process flow [1] to reduce the bow and to alleviate handling problems in equipment and registration errors during alignment for photolithography during RDL build.

The chip-first process flow has two generic process routes, reconstituted wafer handling and build-up process and handling. **Figure 1** shows the general schematic process for both of these process routes. The predominant differences in both of these routes occur during the reconstituted wafer building. In process route A – reconstituted wafer handling – the wafer is built on a separate carrier and then transferred to a second carrier coated with a high-temperature temporary bonding material and a release layer for subsequent RDL-build up and assembly. In process route B, the chip attach, reconstitution, RDL-build, and assembly processes happen on a single carrier coated with a high-temperature-compatible temporary bonding material and a release layer.

The principal challenges for a temporary bonding material used for a chip-first type process include warpage control, die shift, temperature stability, etc., and these were addressed in a previous publication [2]. The chip-first



**Figure 1:** The generic process flow of two predominant approaches for chip-first processes using a carrier-assisted approach: a) Reconstituted wafer handling, and b) build-up process and handling. The dotted boxed region shows the role of temporary bonding material during the process.



**Figure 2:** Schematic process flow for an RDL-first/chip-last process. The dotted boxed region shows the role of temporary bonding material during the process.

fan-out process is now used in high volume with increasing usage to support mobile electronics applications.

**RDL-first/chip-last FOWLP.** **Figure 2** shows the schematic drawing of a RDL-first FOWLP process. Here, the processes for the RDL layer and the assembly processes for die attach are done on a temporary carrier coated with a sacrificial release layer. Typically, a glass carrier is coated with a release layer and then a series of process steps are completed for creating the RDL layer. These steps are repeated multiple times to create a multi-layer RDL structure. After the RDL process is completed, the wafers go through assembly process steps involving die attach, molding, and mold grinding, followed by carrier release. The preferred method for carrier release at the wafer level, for RDL-first type processes, uses a laser release mechanism. Many foundries and outsourced semiconductor assembly and

test suppliers (OSATS) are developing this process for advanced integration at both the wafer level and the panel level.

### Critical requirements for sacrificial release material in RDL-first process

The sacrificial laser release layer is coated on a carrier, and it serves as a layer on which the subsequent redistribution layers, chip-attach, assembly, and molding processes take place. This material serves as a foundational material on which all the other layers are built as opposed to serving a singular function of an adhesive layer or a release layer. Compared to the chip-first process, the RDL-first process is harsher on the sacrificial release layers because the full face of the release layer is open to process chemicals during the early steps of RDL formation. The release layer needs to have good adhesion to metal seed layers and/or polymer dielectric layers depending on the

specific process flow. The release layer must also have good chemical resistance against photolithography chemicals, metal etch chemistries, and various other solvents in open-face testing. Moreover, the release layers need to withstand high-temperature processing during polyimide curing steps for extended periods and avoid flowing during high-temperature and high-pressure die-attach processes and epoxy molding of the dies. **Figure 3** shows the critical requirements of a sacrificial release layer for RDL-first processes. It is important to note that calling this material a sacrificial laser release layer does not capture all the essential functions served by this material.



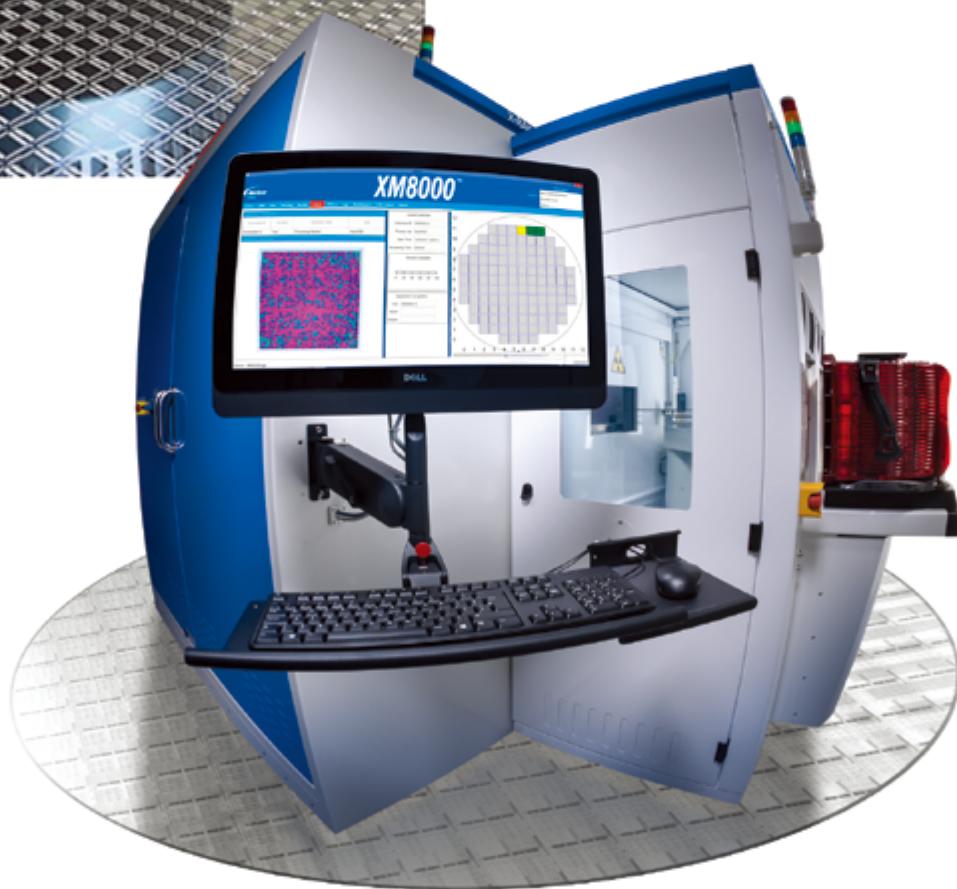
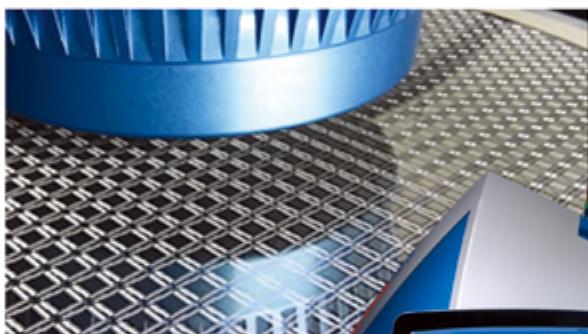
**Figure 3:** Critical requirements of the sacrificial release layer for RDL-first processes.

**Coating process.** The sacrificial laser release layers must be compatible with both wafer-level and panel-level coating techniques. The materials should offer excellent coat quality with uniform total thickness variation (TTV) across the entire substrate. Some of the risks involved are pinhole defects, dewetting spots, nonuniform thickness, etc. These coating anomalies will have a detrimental effect on the downstream processes.

For example, pinhole defects and dewetting spots would cause the subsequent layers coated on top of the release layer, either a polyimide (PI) layer or a physical vapor deposition (PVD) metal, to be in direct contact with the carrier substrate through the pinholes and dewet spots. This will result in poor debonding performance as there will be no release layer in between the carrier and the metal or PI layer to give the release functionality across the defect areas. If the release layer was coated with nonuniform

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thickness, this will impact release functionality and probably affect the laser absorption capability of the release layer, resulting in transmission of high-energy laser light to the active device surface during the debonding process, thereby causing potential harm to the devices.

The sacrificial laser release layers developed by Brewer Science are compatible with spin coating processes for wafer-level application and slot-die coating processes for panel-level application. The materials coat the glass wafers and panels with excellent uniformity without any defects.

**Figure 4** shows the panel-level uniformity of sacrificial release materials A and B coated using a slot-die coating process.

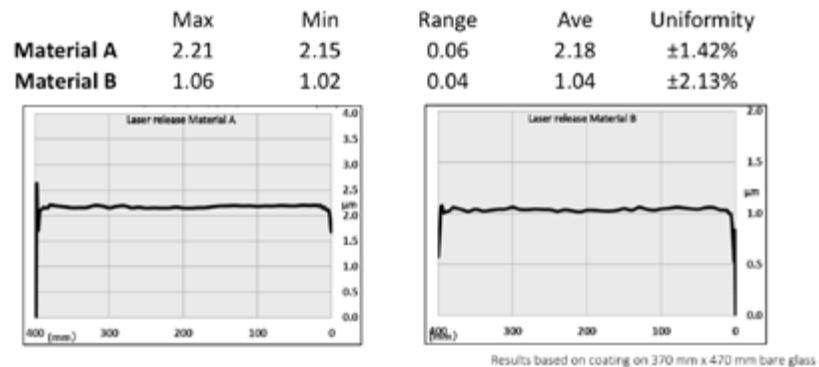
**Adhesion.** The sacrificial laser-release materials must adhere very strongly to glass, organics like polyimide, and metals like Ti and Cu deposited using a PVD process. Poor adhesion strength will result in delamination of redistribution layers or the built-up device substrate during the assembly process. Apart from the characteristic of the release layer, specific metal deposition processes have also been known to have an impact on adhesion strength. Best practices for metal deposition should be followed to improve adhesion to the release layer.

We tested the adhesion of our laser release materials A and B to PVD Cu using a cross-hatch tape test standardized by ASTM-D3359. **Figure 5** shows the results of the cross-hatch adhesion tests of Cu on both materials. A poor adhesion would have resulted in the peeling off of the Cu squares created by the cross-hatch pattern, but here the results show excellent adhesion of all Cu squares to the release layers after the tape test.

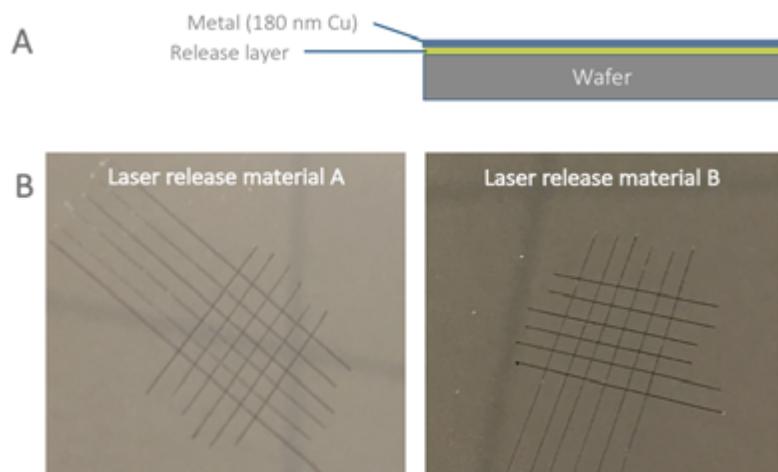
**Thermal and mechanical stability.** Critical requirements for a sacrificial release layer include thermal and mechanical stability through the build-up process. The RDL layers built on top of the release layers require curing temperatures in excess of 250°C for ~1-3 hours per layer. So, a 3-layer RDL structure would expose the release layer to up to 9 hours of high-temperature process cycles. During the thermal cycles, the release layer should not soften or decompose and must remain rigid and stable.

The sacrificial laser release materials A and B are both thermally and mechanically stable materials. Material A is a thermoplastic with a high glass transition temperature ( $T_g$ ) of 320°C and a thermal decomposition temperature ( $T_d$ ) of 410°C. Material B is a thermoset with a  $T_d$  of 270°C, and does not exhibit a  $T_g$  in the temperature range below  $T_d$ . These characteristics cause the material to not soften or decompose during high-temperature processes during PI curing.

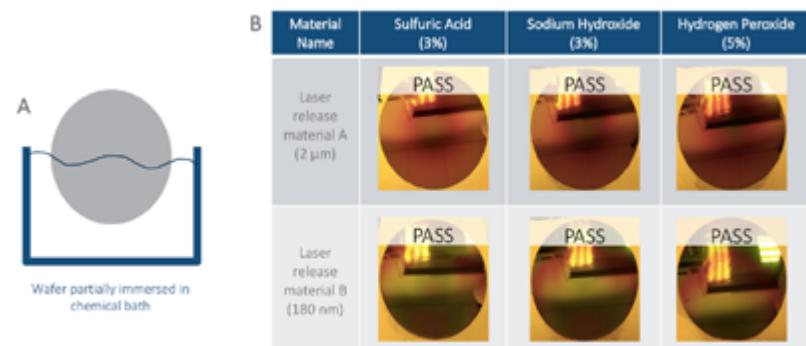
**Chemical stability.** The sacrificial release layers need to withstand harsh chemical conditions, much of it in the open face, as the release layer would come in direct contact with several of the process chemicals including wet etch chemistries during the build-up of RDLs. Typical chemicals would involve solvents, metal



**Figure 4:** Panel-level coating uniformity of sacrificial release materials A and B coated using a slot-die coating process.



**Figure 5:** a) Schematic representation of the test structure for adhesion tests, and b) results of the cross-hatch adhesion tests of Cu on both release materials A and B.



**Figure 6:** Chemical resistance study: a) Schematic representation of a wafer partially immersed in a chemical bath, and b) Photographs of wafers coated with laser release materials A and B after exposure to chemicals.



etch chemicals, resist strippers, plating chemicals, and other assembly process chemistries. The release layers must not dissolve, lose thickness, or contaminate the chemical baths encountered during the process. Common methods to study chemical resistance are visual inspection, thickness measurement of release layer pre- and post-chemical exposure, and measurement of changes in plating rate or etch rate of process baths before and after immersion of substrates coated with release layers to detect any contamination or leaching of release layers into the baths.

We studied the chemical stability of the release layers by coating the release layer on Si wafers, then subsequently immersing the wafer in respective chemicals followed by a visual inspection and/or thickness measurement. For tests involving visual inspection, only one-half of the wafer was immersed in the chemical and to observe any detrimental effects on the coating (color change, adhesion loss, thickness loss, etc.) in the immersed area compared to area that was not immersed in the chemical. **Figure 6** shows the results from chemical exposure study on laser release materials A and B and **Table 1** shows additional chemical resistance studies conducted on material A.

**Laser debonding.** Laser debonding is the preferred debonding method for RDL-first processes and is a critical process leading to the release of the fully built-up device wafer. Any excursion or defect in this process would result in yield loss of the expensive device wafer. The focus of the laser debonding process is to have no damage to the device wafer and have a high-throughput debonding process with minimal residue. Literature suggests that in UV laser-based debonding, ablation occurs predominantly due to photochemical breakdown of the organic laser release material as opposed to a photothermal breakdown that occurs in ablation using a longer wavelength laser source. The sacrificial laser release layers absorb the UV laser light and dissociate chemically to release the carrier from the device wafer. The photochemical ablation process results in less thermal impact on the device wafer and the ablation happens at the interface of the carrier and the laser-release material. The sacrificial laser-release materials developed by Brewer Science are compatible with all

Chemicals	Thickness before	Thickness after	Remarks
NMP 90 °C 25 min	2.44±0.19µm	2.61±0.11µm	pass
2% ammonia 10 min	2.39±0.03µm	2.34±0.03µm	pass
2.5% TMAH 10 min	2.24±0.13µm	2.24±0.32µm	pass
PGMEA 10 min	2.29±0.33µm	2.31±0.33µm	pass
Buffer HF 3min	2.27±0.01µm	2.27±0.02µm	pass

**Table 1:** Expanded chemical resistance study using laser release material A.

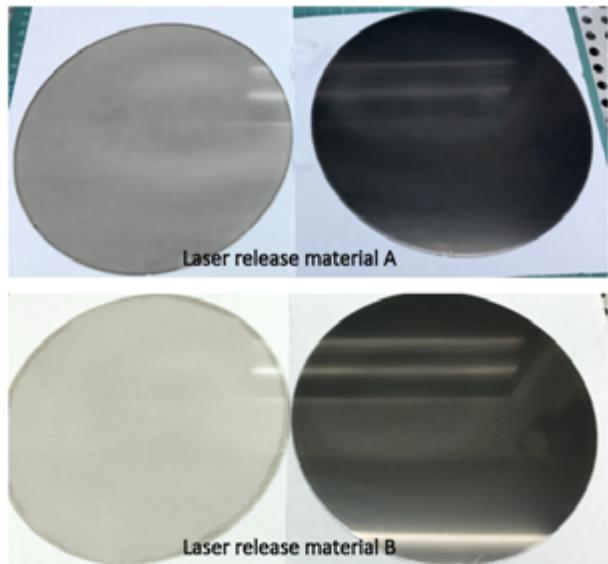
Material	Thickness	Gas (sccm)	Time (seconds)	Power (W)	Pressure (mTorr)	DC-Bias	Results
Material A	2 µm	O <sub>2</sub> -50	600	150	100	396	clean
Material B	180 nm	O <sub>2</sub> -50	60	150	100	396	clean

**Table 2:** Recipe for plasma cleaning of laser release materials A & B.

the common UV laser debonding tools (308nm, 343nm and 355nm) available in the market for wafer and panel debonding. **Figure 7** shows the debonding results of material A and B using the 355nm laser wavelength.

**Post-debond cleaning.** After the laser debonding process is completed, it is essential to clean all the release layer residues from the device wafer. Material A is a thermoplastic release layer and it is compatible with both a solvent cleaning process and a plasma cleaning process. Material B is a thermoset release layer and it is compatible with a plasma cleaning process. The important aspects of the post-debond cleaning process is to completely remove the residues using a cost-effective and short cleaning procedure.

We used a parallel plate plasma etcher to clean the laser debond residues for materials A and B. **Table 2** shows the recipe used for plasma cleaning. Both materials are readily cleaned by oxygen plasma. Material A can also be cleaned using a solvent clean using either NMP



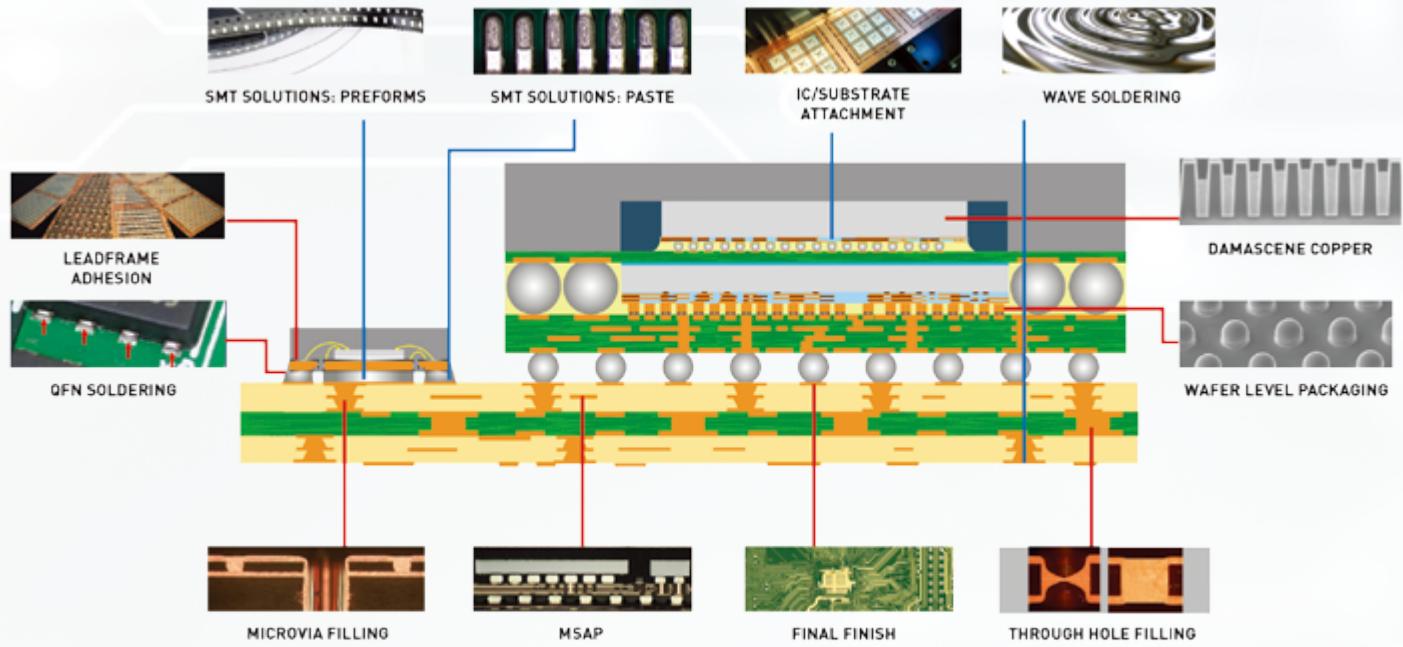
**Figure 7:** Debonding of laser release materials A and B using a 355nm laser source.

or dioxolane as the solvent in a spin- or a spray-cleaning tool.

## Summary

From the above list of process requirements for RDL-first fan-out packaging, it can be easily argued that the laser release layer is one of the critical materials that enable the RDL-first process. The examples in the article showcased the performance of our laser release materials A and B, but

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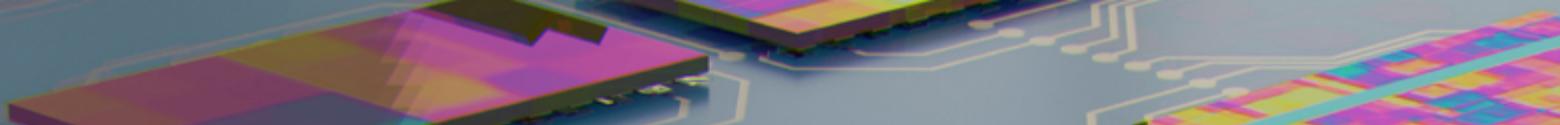
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we have also developed several other formulations and thickness variations to suit the needs of individual customers and process flows. One such material variation was used to demonstrate a full-flow RDL-first process at our partner site, and the results of this full-flow process have also been published recently [3]. The experiment was done at the wafer level using a glass carrier where a multi-layer RDL was built, followed by die attach, molding, debonding, cleaning, and singulation of the dies. The electrical performance of the final device was tested to confirm that no damage occurred to the dies or electrical circuits during the laser debonding process.

As we surpass the age of Moore's law and enter the era of "more than Moore," each electronic device is integrated with multiple functionalities for sensing, processing, data transmission, display, etc. Here, heterogeneous integration and system-in-package (SiP) technologies play an important role in meeting the demands of the end users. Mobile electronics, Internet of

Everything (IoE) applications, and other connected services will continue to drive the performance requirements of semiconductor products, and advanced IC packaging processes will increasingly become essential to meet these needs. As an advanced material supplier and an integral part of the semiconductor supply chain, we understand that transformational innovation in materials is key to sustain and support the development of the next-generation of electronic devices.

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# Extending plating performance to enable FOPLP

By Christian Ohde, Henning Hübner, Mustafa Özkök, Ralph Zoberbier, James Welsh [Atotech Deutschland GmbH]

This paper describes first results of a newly developed plating tool that also uses newly developed electrolytes in order to plate Cu pillars at high current densities and finer lines and spaces on large panels (similar to wafers). These abilities are important in order to transfer wafer-level packaging technologies on larger substrate panels enabling lower manufacturing cost and increased productivity.

Fan-out wafer-level packaging (FOWLP) was introduced many years ago and is now seen as a key advanced packaging platform to meet the technological and cost requirements of the industry. Substrate sizes have increased over the past several years and now substrates larger than 300mm are poised to take advantage of the economies of scale in manufacturing processes. This situation currently drives the industry and the supply chain, i.e., the transfer of FOWLP to fan-out panel-level packaging (FOPLP) and the development of new products and solutions. The move from round to square substrates allows even more dies to be produced in order to further reduce costs. Though this transfer offers new possibilities, it also raises challenges.

A plating tool for panel sizes up to 650×600mm was developed and installed for detailed investigations. This paper describes the use of newly developed electrolytes for high-speed Cu deposition in RDL layer plating with and without microvias, as well as tall pillar plating (package-on-package [PoP] design). The key requirements for both applications are uniformity, feature shape, and process stability. This article will show the improvements achieved for each of the above mentioned requirements during the past two years. Our investigation during that time shows that FOPLP has the potential to be strong competition for WLP for the coming years. But the standardization of panel format is seen as a must in order to achieve the cost-saving potential promised by this technology.

## Introduction

FOWLP had been introduced to the market many years ago as a breakthrough packaging technology to meet the challenges and demands for thinner and smaller electrical devices such as smartphones, combined with higher performance and a higher level of system integration. Since its introduction, the technology has matured for single-chip packaging applications and is mainly used for communication products like RF, baseband, and Bluetooth packages. Over the years, many new fan-out platforms have been introduced with constantly increasing complexity such as through-mold interconnections and multiple RDL layers to ready the technology for additional and more complex products and applications like application processor packaging. Development of the equipment and materials supply chain tends to focus on technological improvements and new solutions to overcome immediate key issues such as severe wafer warpage, die shift, and process reliability.

A key differentiator of this technology is the creation of a new artificial substrate based on known good dies. In theory, the shape and size of this substrate has no limitation as opposed to a traditional 300mm Si wafer. This characteristic offers new possibilities in package design and offers significant cost reduction potential as substrate sizes can easily be enlarged over the traditional 300mm wafer format. Many recent publications are discussing the impact on cost reduction while moving from wafer- to panel-size substrates. In general, the size of the manufacturing substrate is a key driver for the overall cost of the package. However, it has to be considered that the biggest savings will only come from batch activities. While investigating the cost structure of a fan-out package, RDL creation is considered to have the largest impact by approximately 40% of the overall costs [1]. The largest portions of the RDL cost itself are the material cost

(e.g., photo-dielectrics and plated Cu) and equipment related costs for patterning and metallization. While material costs are considered to remain on a similar level, equipment costs per package directly relate to the number of packages per substrate that can be processed with a single process step.

The promise of this cost reduction is currently driving the industry and the supply chain to develop new products and solutions that take advantage of the substrate scaling possibility. The main challenge is to develop a solution that keeps, or even improves the technical performance of the process step manufactured on a much larger substrate, combined with cost-efficient equipment solutions that can keep the output in substrates per hour at a minimal equipment cost increase per panel.

The actual substrate size will strongly impact process performance and equipment costs. A consensus and final standardization of substrate size and format will be required to finally get panel-based packaging technology widely adopted. A broad range of different substrate formats are currently under investigation, i.e., 300×300mm, 370×470mm, 508×508mm, 510×515mm, 600×600mm, or even larger.

Besides photolithography, Cu deposition to create the RDL trace is a key process step for fan-out packaging, both on-wafer and on-panel. Key challenges, latest technology developments, and test results at the panel level will be presented in the following sections.

## Technology challenges for panel plating

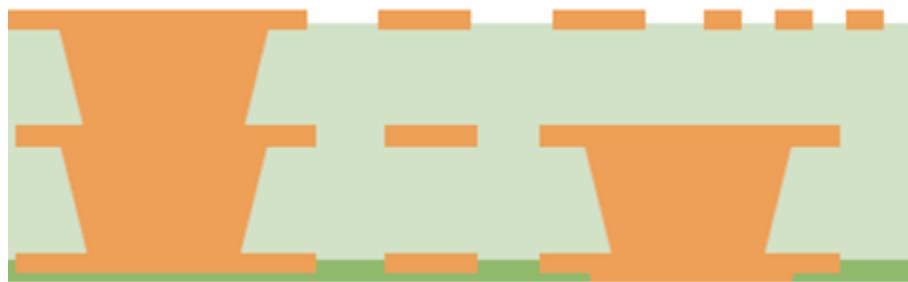
With the transfer of FOWLP to FOPLP, the industry strives to reduce manufacturing costs. However, there are some process challenges associated with fan-out packaging in general that need to be addressed also at the panel level.

During an electroplating process, Cu material is typically deposited into

a mold of thick photoresist or photo-definable dielectric material on top of a seed layer (**Figure 1**). Depending on the structure's function, this can be a large connection pad (up to 250–350 $\mu\text{m}$ ), so-called  $\mu$ Vias with sizes of 10×15 $\mu\text{m}$ , for example, to connect different layers and redistribution layers (RDL) of different sizes (**Figure 1**). The continuous trend of miniaturization and added complexity in electronic devices increases the number of RDL layers and requires decreasing feature sizes. Typical sizes of RDL traces in a fan-out package design are in the range of 8–10 $\mu\text{m}$ . New developments ask for resolution down to 2–5 $\mu\text{m}$ . The key challenge for the plating process is to deliver very uniform Cu deposition across a single layer that includes a wide range of different structures. Different feature sizes and different required Cu thicknesses play a dominant role with respect to the plating result.

Additionally, fan-out packaging enables new embedded chip technology system integration concepts like multi-die packages and package-on-package (PoP). For package-on-package (PoP) technology, tall Cu pillar plating is needed in various dimensions including both standard pillar in the range of 40×50 $\mu\text{m}$  and tall pillars with heights of up to 200 $\mu\text{m}$  [2]. The wide variety of required plated Cu features in a leading edge FOWLP design is displayed in **Figure 2**.

High throughput, high yield and optimal reliability are requirements that need to be met with an optimized Cu pillar process. The purity of the deposit is critical as it influences the voiding performance. Especially with these very thick Cu studs, applicable plating speed becomes a very important parameter that defines not only technical performance but also the manufacturing costs per package. This being said, high throughput can be achieved by high-speed plating. However, it also influences uniformity performance, which impacts the yield. Therefore, the correct Cu pillar process should enable uniform and pure Cu deposition while using high-speed plating. This can be achieved with the right organic additives and high-speed plating equipment that collectively reduce the occurrence of organic co-deposition and optimize uniformity and pillar shape [2]. The key challenge with the move to panel processing is to



**Figure 1:** Schematic illustration of Cu-plated features in a dual RDL package design, including  $\mu$ Vias, RDL traces, and Cu pads.

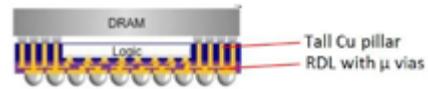
keep similar deposition performance achieved at the wafer level and transfer it to the much larger surface without accepting the disadvantages linked to the increase in area.

To meet the different technology requirements, we have developed specific processes for Cu RDL and pillar plating consisting of high-purity organic additives. The new Innolyte® electrolyte is designed for use in a dedicated panel plating equipment designed for very high-speed plating. Both processes, together with the equipment, satisfy the technology needs by providing a high deposition rate, as well as achieving the requirements for the Cu deposit.

Meeting the process requirements for FOPLP plating requires having the right equipment to achieve those targets. The market of FOPLP consists of a diverse array of substrate materials and sizes as the industry seeks to adapt each participant's particular supply chain and expertise. For the equipment supplier, this results in customized solutions and high development costs to support each player. Customized solutions include the two major topics involving the individual process modules, and the related substrate handling systems and components. The challenge for the equipment supplier is to minimize these costs to deliver an attractive cost-of-ownership (CoO) to support both FOPLP development and adoption of the production process.

### Panel plating processing for FOPLP

The unique approach to panel-level plating for FOPLP involves taking many of Atotech's core competencies and applying them to this emerging market. The approach involves both plating process equipment (including chemical additives) and substrate handling technologies as a complete system solution. Continuous development



**Figure 2:** A fan-out (FO) package-on-package (PoP) example for advanced processor application with tall Cu pillar, RDL and  $\mu$ Via structures [3].

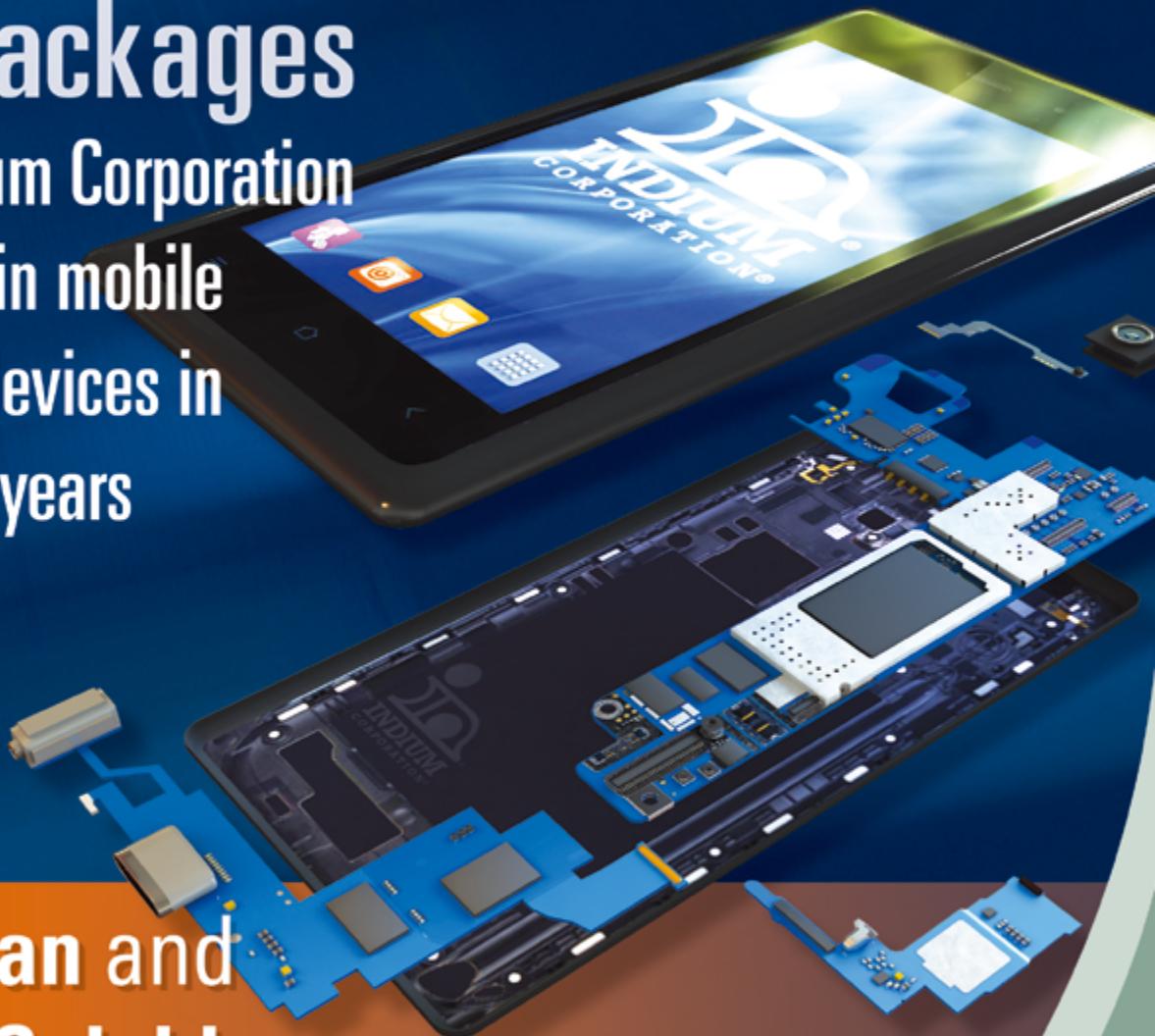
is ongoing as electrolytes are tailored specifically for vertical plating targeting the specific demands of FOPLP products. Likewise, equipment development is realized in concert to achieve the physical parameters required to support the overall process requirements and targets. New substrate handling systems are meeting the substrate requirements considering the various geometric considerations of size, material and warpage.

**Electrolyte and process.** As mentioned in the sections above, there are two major plating requirements of panel-level packaging and for each, specific electrolytes were developed. On the one hand, there is a two-additive electrolyte for tall pillar plating, with the major focus of high applicable current densities of about 20 ASD (A/dm<sup>2</sup>), rectangular pillar shape, and very good within-unit and within-panel uniformity. On the other hand, there is the development of an RDL plating electrolyte focusing on within-unit distribution at current densities of about 4 ASD. It has to be considered that there are various features to be plated in RDL plating (e.g., fine lines down to 2 $\mu\text{m}$  lines and spaces; pads; mass plane areas; etc.) and depending on the application, there are blind microvias, that need to be filled, with a relatively low surface copper thickness of around 2–5 $\mu\text{m}$ . To fulfill these challenging requirements, it was seen that a three-additive electrolyte is needed, where the concentration of each additive can be adjusted individually. In both cases, RDL and

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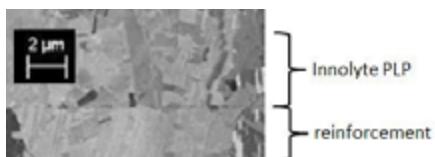
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Application	Products	Dimensions	Target CD
RDL- Plating	<b>3 additive system</b> EXPT Innolyte PLP Accelerator EXPT Innolyte PLP Suppressor EXPT Innolyte PLP Leveller	L/S: 5/5 $\mu\text{m}$ (future 2/2 $\mu\text{m}$ and below) BMVs: 25 $\times$ 10 $\mu\text{m}$ (dia x depth, smaller in future)	CD $\geq$ 4 ASD
Tall	<b>2 additive system</b>	Pillars: 200 $\times$ 200 $\mu\text{m}$ (dia x depth; future 50 $\times$ 200 $\mu\text{m}$ )	CD $\geq$ 20
Pillar Plating	EXPT Innolyte P Accelerator EXPT Innolyte P Leveller		ASD

**Table 1:** Additive and current plating requirements.

tall pillar plating, there is an advantage to use pulse plating, which improves distribution and feature shape in RDL plating and allows the use of higher current densities and improves the pillar shape in tall pillar plating as well. A well-established plating technology to apply pulse reverse plating without the risk of creating surface defects is the use of a  $\text{Fe}^{2+}/\text{Fe}^{3+}$  redox system. The combination of reverse pulse plating, the iron redox plating system, and the additives choices for RDL and tall pillar plating, helps to achieve the future requirements for the PLP market. The summary of additives and current plating requirements for FOPLP applications is shown in **Table 1**. The within-panel distribution (WIPD) is calculated as follows:  $\text{WIPD} = (\pm \text{max-min}/2) \times \text{mean} \times 100\%$ , and here the target is to be better than  $\pm 10\%$ . However, the development goal is to be better than  $\pm 5\%$ .

It is worth mentioning that the copper deposits were investigated according to industry standards. The results showed that in a broad working range, ductility was always well above 20% and tensile strength was above 25 kN/cm<sup>2</sup>. The crystal structure investigations showed an epitaxial growth from the base copper clad with normal polygonal grain structure. This structure can be seen in **Figure 3**.



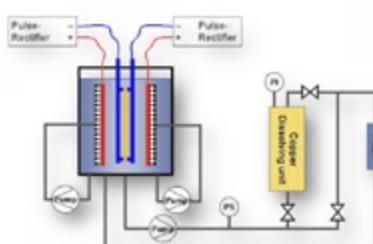
**Figure 3:** Crystal structure of copper deposited with an RDL electrolyte.

**New developments for equipment.** The latest equipment developments can be grouped into three subsets: pre-wet process cells, the plating cell system, and substrate handling. To support the advanced requirements of FOPLP

including RDL and tall pillar plating, the pretreatment process prior to plating requires adequate wetting of the features to be plated. Wetting of standard features is achieved in a specially designed vertical tank under controllable flow conditions of chosen chemistries. These flow conditions are provided by direct jet flow from a flow distribution plate to ensure a uniform and controllable flow environment across the entire panel surface. Advanced wetting of more challenging features is achieved by use of a vertical vacuum cell in which a controlled pressure drop leads to reduced partial pressure of the applied wetting medium. The result is a lowered surface tension allowing complete wetting of the feature. Challenging features in the FOPLP roadmap include small RDL lines and spaces down to 2  $\mu\text{m}$ , and tall Cu pillars with increasing aspect ratios.

The focus of development is of course in the plating cell system. Development topics center on the three principle pillars of plating such as fluid flow, current density distribution, and chemical control, which are discussed below.

**1. Fluid flow:** A novel approach to direct fluid flow to the cathode surface is achieved using a through-anode flow technology utilizing hundreds of jets evenly distributed across the anode segments. Through-anode flow technology shown in the plating cell fluid flow schematic (see **Figure 4**), provides a highly uniform medium across the entire cathode surface without the use of paddles or other



**Figure 4:** Plating cell fluid flow schematic of the multi-plate panel plating equipment.

hardware that can introduce undesired shielding or flow nonuniformities. Further fluid flow manipulation is achieved by physical agitation of the cathode, which adds a very important process parameter. Localized flow phenomena can be distributed in a predictable and repeatable controlled approach using freely-programmable agitation profiles.

## 2. Current density distribution:

Applying a customized current density profile to large rectangular and square substrates is achieved using a through-anode approach with segmented anodes. The number of segments chosen and geometry of each segment is designed to optimize uniformity control for each substrate's geometry. Controlling the current to individual anode segments is a major control knob for optimizing plating uniformity across large panel substrates, especially when coupled with a pulse reverse rectifier. The ability to apply complex pulse profiles across multiple anode segments offers a significant degree of process control.

## 3. Chemical control:

Chemical control is the third pillar of plating. Absolute control of chemistry is accomplished by way of a specially developed version of a  $\text{Fe}^{2+}/\text{Fe}^{3+}$  redox system for Cu replenishment and control. The system consists of a "Cu tower" of pellets through which electrolyte passes for Cu replenishment. The plating system does not use soluble anodes, therefore, the Cu tower is the source of Cu ions. A PID controller working with input data from an inline spectrometer analyzing Cu and Fe concentrations controls both the Cu and Fe content within a defined specification by controlling the amount of flow through the Cu tower. Electrolyte additive concentrations are monitored and dosed via slipstreams taken from the main fluid flow path within a defined sample schedule. The slipstream is connected to a manual sample port or to a fully automated analytical system. Dosing of additives is also accomplished via the slipstream. The combined use of the  $\text{Fe}^{2+}/\text{Fe}^{3+}$  redox system using inert anodes provides both a reduced maintenance system and plating performance stability

as compared to systems relying on soluble anodes that typically deform irregularly and impact the current density profiles.

In this emerging market for FOPLP, an easily overlooked and under-addressed topic is substrate handling. As each player in FOPLP has its own experiences and manufacturing supply chains, each has its own approach to substrate delivery and environmental conditions. While some may utilize open cassettes capable of 15 substrates, others have a more semiconductor fab-like approach with an enclosed FOUP-like substrate carrier. There is no standard approach, and therefore, substrate handling is proving to be a critical technology to be seriously considered. The currently used equipment platform for process characterization and development utilizes both Bernoulli end effectors to handle substrates in a nearly “touchless” approach, and vacuum end effectors in a geometric vacuum approach.

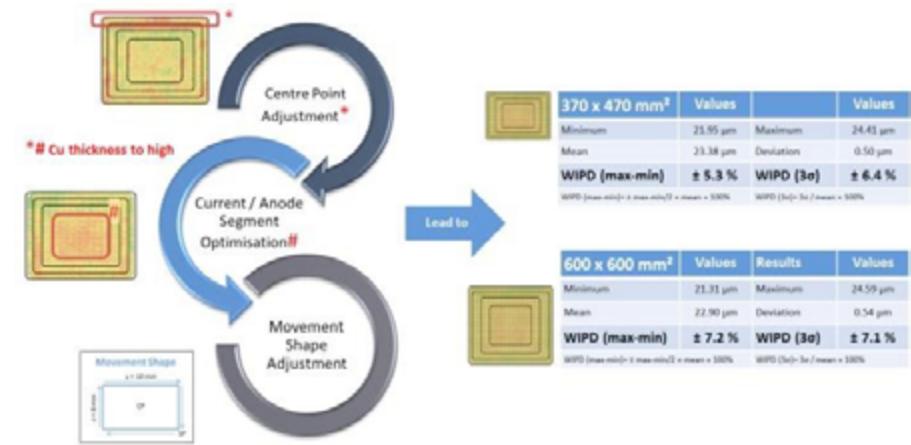
Finally, the latest developments in package designs with through-mold via (TMV) interconnections or double-sided RDL layers require simultaneous plating on both sides of the substrate. This technique is fairly common in PCB manufacturing, but is a new approach in the back-end-of-line (BEOL) industry. Consequently, substrates need to be implemented in a frame or substrate holder to allow plating from both sides.

**Challenges for equipment development.** Managing the high cost of development and meeting current process roadmaps with an acceptable cost-of-ownership (CoO) prove to be the two main challenges for equipment development. Without market consensus or standardized panel size adoptions among the group of early players, customized hardware must be developed at high investment levels for each panel size. Considering the development efforts within 200mm and 300mm wafers, the extrapolation of those investments to the multiple spreads in format area increases among the many panel formats is considerable. The format comparison of wafer and panel illustrates just a sample of the 10+ formats currently in development (**Figure 5**).

## Format Comparison



**Figure 5:** Area comparison of different wafer and panel size formats.



**Figure 6:** WIPD optimization sequence.

To illustrate the extent of the equipment set with the plating module, each format size can require a specific equipment package consisting of a panel holder, anode set, tank, flow distribution box, rectifier, and high-amperage electrical setup. Each piece within the equipment package must be developed to achieve the process roadmap targets at the lowest possible cost. Achieving equipment solutions that meet the CoO target, which justifies the move to larger panel formats, will lead to early adoption of the panel format. The current target for the panel plating equipment CoO advantage over wafer-level plating, which many players are seeking, is greater than 40%.

## Results

A prerequisite to being able to achieve a WIPD below ±10% is a good distribution on panels without any RDL pattern—this is because the distribution that is coming from the RDL pattern itself will come on top of the distribution of a blanket panel. **Figure 6** shows the process flow for the optimization of surface distribution. As it is still unclear which panel size will be the direction for PLP, the optimizations of two panel formats are depicted.

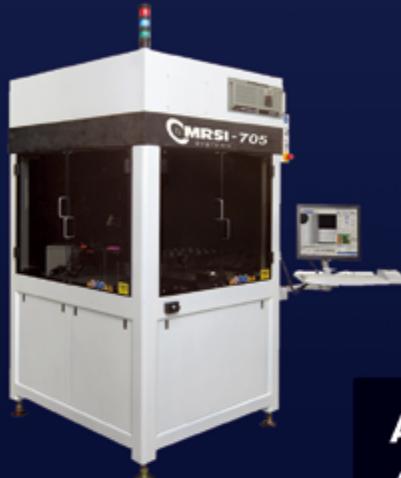
The first step is to adjust the center points of the substrate to the actual plating anodes. Second, current adjustments of the segmented anodes are needed to fine-tune the overall

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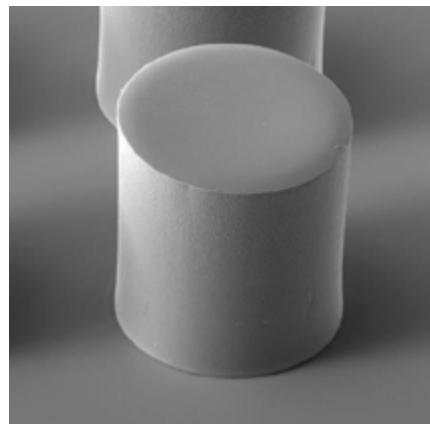
plating distribution. Finally, the definition of the substrate agitation profile is used to optimize the plating uniformity. Using this procedure, it was possible to reduce the WIPD for formats up to  $600 \times 600\text{mm}^2$  close to  $\pm 7\%$ , and further optimization is ongoing. These measurements were done by automated 4-point probe resistivity measurements (e.g., over 3,000 measurement points for  $600 \times 600\text{mm}^2$  panels).

Over the last several months, many plating tests have been performed in cooperation with several industry players on various panel formats. As mentioned above, there is no standard plating format at the moment each potential FOPLP manufacturer seems to have an individual panel format, which is mainly dependent on the manufacturer's existing infrastructure. On top of that, the substrate base material can also be different based on the fan-out process type. On the one hand, there is a process using glass with its nearly independent temperature dimension (low coefficient of thermal expansion [CTE]) in combination with a very even surface. On the other hand, organic substrates, which are more easy to handle and can be made conductive by well-established methods in the PCB industry, are the options of choice, depending on the PLP technique. The PLP technology consists of two key copper plating steps with different plating conditions. One is the "tall pillar plating" and the other is the "RDL plating," which are discussed below.

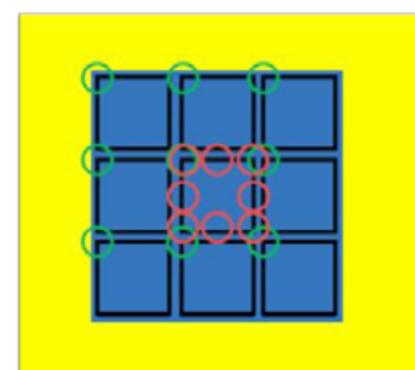
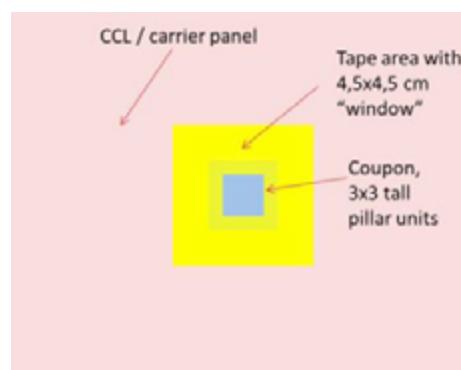
**Tall pillar plating.** The performance of tall pillar plating (pillar thicknesses up to  $200\mu\text{m}$ ) at the panel level is currently under investigation and therefore can't be shown as part of this section. However, full-panel results are expected to be available later this year. The major factors that are in focus for this application are throughput, as long plating times are required, and of course, WIPD.

The plating speed depends on the pillar dimension and aspect ratio, targeted to be faster than 20 ASD, which corresponds to  $4.5\mu\text{m}/\text{min}$ . The WIPU should be  $\pm 10\%$  or below (calculated as follows:  $\text{WIPU} = \pm(\text{max-min}/2) \times \text{mean} \times 100\%$ ). An example of a tall Cu pillar plated in the Atotech MultiPlate Wafer tool at 20 ASD is shown in Figure 7.

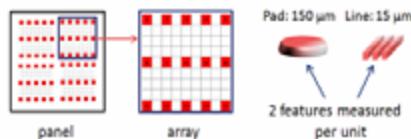
To determine if the same plating rate can be achieved on the panel as it is shown in Figure 7, we started with coupon scale tests in the panel-size plating equipment. For this purpose, a pillar plating coupon was mounted on a carrier board (Figure 8) and plated with similar parameters as in the wafer



**Figure 7:** Example of a tall Cu pillar plated at 20 ASD,  $200\mu\text{m} \times 180\mu\text{m}$  (dxh).



**Figure 8:** a) (left) Tall pillar coupon mounted on a CCL carrier; and b) (right) Measurement locations.



**Figure 9:** Unit locations and features for full-board RDL investigations.

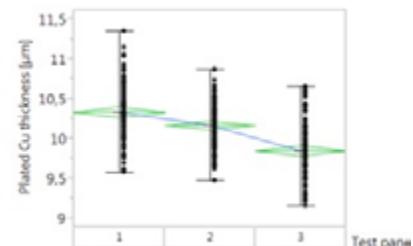
Test #	1	2	3
Mean	10,35	10,19	9,87
WIPU	8,5 %	6,9 %	7,6 %

tool. The tall pillars had a diameter of  $120\mu\text{m}$  and were plated on a CCL carrier with a dry film of  $170\mu\text{m}$ . The plating height target was  $150\mu\text{m}$ , which was achieved with a plating rate of  $5\mu\text{m}/\text{min}$ . The coupon scale test result looks more than promising. The WIUD (calculated on the basis of the red circles) was  $\pm 2\%$  and the WICD (within coupon distribution—calculated on the basis of the green circles) was  $\pm 3.5\%$ .

**RDL plating.** The major focus of the work of the last several months was RDL plating, and as an example, the result of an RDL plating test with lines and spaces requirements of  $15/15\mu\text{m}$  (minimum) is shown in Figure 9. This study was done on an organic substrate with copper clad as the conductive layer. The target of this sample plating was in accordance with the requirements mentioned in Table 1, i.e., a WIPU below  $\pm 10\%$ .

The test panel of  $510 \times 505\text{mm}$  contained 360 units. These 360 units

are organized in four sub-groups, called arrays. In each array, 15 units were evaluated for total panel distribution. In each unit, two features were measured: redistribution lines of  $15\mu\text{m}$  L/S resolution, and a pad of  $150\mu\text{m}$  in diameter. A schematic drawing of



**Figure 10:** WIPU results on a  $508 \times 508\text{mm}$  panel.

Cu thickness evaluated by LEXT (line: 600 points; pad: 3800 points)

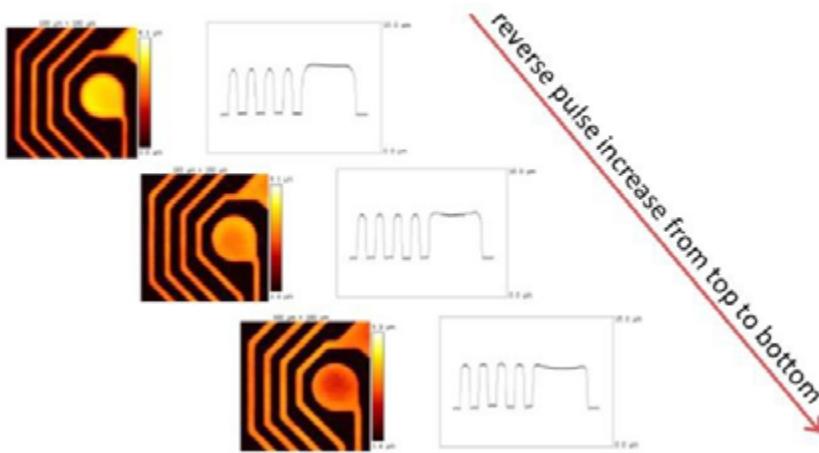


Figure 11: Optimization of WIUD by RPP.



Figure 12: Test patterns for panel plating process qualification and characterization on a glass substrate.

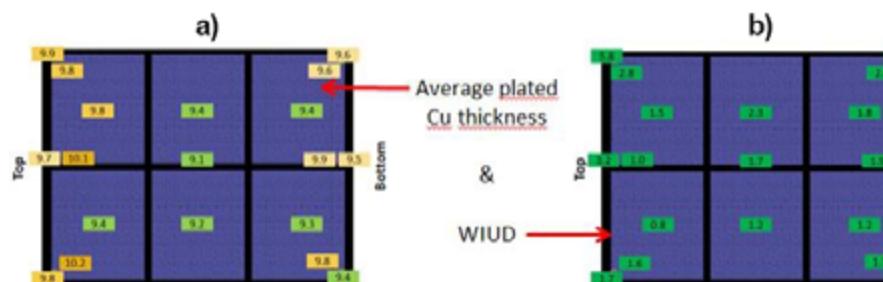


Figure 13: a) Thickness measurement, and b) WIUD on a glass substrate.

the test vehicle is shown in Figure 9. In total, 120 measurement points were considered in order to determine the within-panel distribution (calculated as follows: WIPU =  $(\pm \text{max-min}/2) \times \text{mean} \times 100\%$ ). Figure 10 shows the results of three panels plated with the same parameters. The plating thickness was decreasing a little during the plating tests, but all the WIPU results are in the range of  $\pm 6.9\text{-}8.5\%$ , which is well below the target of  $\pm 10\%$ .

It was already shown how the panel distribution was optimized, but a major

contributor to the WIPD on RDL plating is the RDL pattern itself. This pattern is of major importance for the within-unit distribution (WIUD). In most of the cases the WIUD can hardly be changed, the main knobs for this optimization are the chemical parameters and the current density. Here we would like to show the influence of reverse-pulse plating (RPP) on the WIUD on the features shown in Figure 11 (15 $\mu\text{m}$  line and 150 $\mu\text{m}$  pad). In Figure 11 it is shown that under DC-like conditions, the pad has a higher plating thickness than the traces. By

increasing the reverse current, the thicknesses can be equalized and even changed to the opposite.

As already mentioned, glass is also considered to be a substrate that combines some important benefits (low CTE and a smooth surface). The following passage is dealing with the RDL plating result on a glass substrate. The conductive layer was 0.5 $\mu\text{m}$  of sputtered copper in this case. Once again, the required current density was 4 ASD and the target was to be below  $\pm 10\%$ . For the whole panel, 19 units were investigated, and 6 features have been measured/unit as shown in Figure 12.

In Figure 13a, the average plating thickness of the 6 measured features is shown to vary from 10.2-9.1 $\mu\text{m}$ . The corresponding WIUD, calculated on the basis of the 6 features, is shown in Figure 13b ( $\pm 5.8\text{-}0.8\%$ ).

The overall result of this investigation showed that a WIPU result below  $\pm 8.0\%$  is possible. Of course the RDL panel distribution is highly dependent on the layout itself, but by the use of reverse-pulse plating in combination with the optimized organic additives, an outstanding distribution is possible just by changing the plating parameters, which is to the best of our knowledge, unique in the market.

## Summary

The transfer from round wafer substrates to square panel-based processing for fan-out packaging promises to increase productivity and further reduce manufacturing costs. However, two worlds are colliding: the wafer packaging world with its technical requirements and standards needs to be merged with the PCB and liquid crystal display (LCD) industry with its existing, cost-effective process and equipment solutions. Photolithography, substrate and Cu deposition are the critical areas. The constant drive in higher density packaging and cost reduction requires "More than Moore" solutions, and the first solutions are now being installed in pilot lines for panel-based fan-out technology.

The industry has to find answers to fulfill the promise of more features in smaller packages at a reasonable cost level or to put it succinctly: "faster, smaller and cheaper." In this paper we described the efforts made in plating

materials and dedicated panel plating equipment and proved that solutions for the transfer of wafer-level packaging to panel-based substrates already exist today. The equipment for panel plating was improved based on our existing MultiPlate system, especially the pre-wet process cells, plating cell system and substrate handling. In combination with our chemical plating process, we can meet the challenges that exist for RDL features such as a uniformity distribution of  $<\pm 10\%$ , as well as for the high-speed plating of tall pillar structures of up to 200 $\mu\text{m}$  in height. The latest plating results on substrates with sizes of up to 510 $\times$ 515 mm achieved a WIPU well below  $\pm 10\%$ .

### Acknowledgments

The authors want to thank our business partners for providing FOPLP substrates that allowed in-depth studies and process tests. The authors also thank Holger Schulz, Thomas Reike, Torsten Küssner, Sandra Niemann, Therese Stern, Markus Youkhanis, Oliver Worm, Bert Lin, Oden Hsu, Bruce Lin, Bobby Chen, and additional Atotech colleagues around the globe for collecting market requirements and data included in our studies and the paper.

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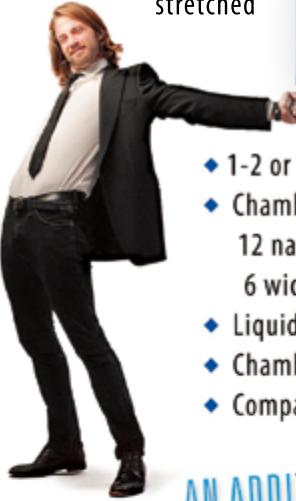
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# Fan-out wafer- and panel-level technology for advanced LED packaging

By Tanja Braun, Ruben Kahle, Stefan Raatz, Pascal Graap, Ole Hölck, Joerg Bauer, Karl-Friedrich Becker, Rolf Aschenbrenner [Fraunhofer Institute for Reliability and Microintegration]; Steve Voges, Marc Dreissigacker, Klaus-Dieter Lang [Technical University Berlin, Microperipheral Center]; Jürgen Moosburger, Frank Singer, Lutz Höppel [OSRAM Opto Semiconductors GmbH]

**F**an-out wafer-level packaging (FOWLP) not only has a high potential for significant package miniaturization with respect to package volume, but also in thickness. It can be used for multi-chip packages for system-in-package (SiP) and heterogeneous integration. Heterogeneous system integration includes also 3D routing of electrical signals and double-sided redistribution layers. Together with the possibility of low thermal resistance, FOWLP might also offer opportunities for LED packaging.

Besides the development to higher 2D and 3D integration, a second trend is the movement from wafer- to panel-level for fan-out technologies, mainly driven by lowering packaging cost. Increasing the embedding substrate size does not only mean an upscaling of the existing technologies, but may lead to a change from using wafer processing infrastructure to that used for panels. This is especially true when moving from round wafer sizes to larger rectangular panel formats. Here also, new materials and processes have to be taken into account [1].

## LED package concept

General lighting by the use of LED chips is one of the strongly growing markets today, and low-cost and large-area packaging is a demand [2]. Therefore, a blue LED with an area of  $1 \times 1 \text{ mm}^2$  and a thickness of  $120 \mu\text{m}$  has been chosen for package development. The LED has one contact pad on the topside and needs an additional electrical connection to the backside. The overall concept for the SMD-compatible single LED package is shown in Figure 1.

The package size was designed to  $1.6 \times 1.6 \times 0.3 \text{ mm}^3$  allowing the integration of a through-mold via (TMV) with a  $100 \mu\text{m}$  diameter routing the contact

from the topside to the surface mount device-compatible (SMD) pads on the backside. The backside of the LED is connected by a blind via with a diameter of  $250 \mu\text{m}$ . To enable subsequent blind via manufacturing, including via drilling through the mold and electrical connection by plating, the LED was prepared with  $5 \mu\text{m}$  Cu on the backside. The backside via also strongly supports the cooling of the LED. Here, larger blind vias or multiple vias could even further improve the thermal concept and design of the package.

## Process flow

For LED packaging, a “mold first” face-down approach has been selected as the light-emitting surface of the LED can be opened by the lithography step in the redistribution layer (RDL). The proposed packaging process flow starts with face-down LED assembly on an intermediate carrier followed by overmolding using compression molding, and debonding of the molded wafer/panel from the carrier. The next step is laser drilling of TMVs to route contacts from front to backside, and blind vias to access the backside of the LED. Before application of the RDL, the vias have to be cleaned of laser ablation residues. A topside RDL is manufactured using a photosensitive dielectric layer and

Cu plating base sputtering followed by a plating step. The backside RDL is applied by direct metallization on the mold, also using sputtering and plating steps. Whereas through-mold and blind-via metallization is done by palladium activation first, and then copper plating. Cu structuring is done by etching for conductor line and SMD pad forming. Finally, a solder mask is applied on the backside and package singulation is done by laser or blade dicing. The schematic process flow is summarized in Figure 2.

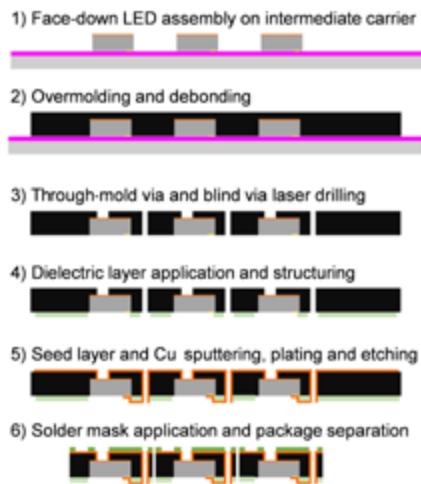


Figure 2: Process flow LED fan-out wafer/panel-level packaging.

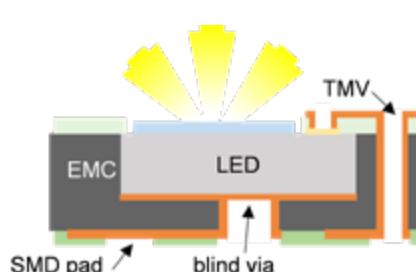


Figure 1: Schematic LED fan-out wafer/panel-level package.

## Package developments at the wafer level

The process developments and the overall proof of concept for the LED fan-out wafer/panel-level packaging approach has been done on  $200 \text{ mm}$  wafers. All materials, equipment and processes have been selected and evaluated for direct upscaling to panel size. Wafer design has been set up to reduce the number of dies and assembly time. Therefore, package density has been reduced without having

to use the full wafer area. The overall process developed at the wafer-level, and transferred to panel-level after, are described in detail in the next sections.

**Assembly.** For die placement, a high-speed assembly machine was used that allows die placement on the wafer, but also on the panel in one step. LEDs and fiducial dies were directly picked from the diced wafer and placed face down on the carrier.

**Wafer-level compression molding.** Compression molding evaluation within this study has been performed on 200mm wafers and with a large-area panel mold machine using a tooling with a cavity size of 457x305mm<sup>2</sup>. For the LED package development, a liquid black epoxy molding compound has been selected with a filler particle top cut of 25μm. Material with a small maximum filler particle size has been chosen to allow laser through-mold and blind-via drilling with precise geometries and smooth via walls [3].

Mold flash on the LED surface and contact pad is the main issue during compression molding. This is especially true as the contact pad is around 5μm lower than the LED surface. Therefore, the overall process has to be optimized to avoid EMC wetting during molding. On the one hand, the adhesive layer of the thermal release tape has to compensate for the chip topography, and on the other hand, the mold process – including pressure and flow profile – has to be optimized to minimize flash. In **Figure 3**, the contact pad of the LED is depicted before process optimization

showing massive flash, and after optimization without flash. A flash-free contact pad is mandatory to guarantee a reliable electrical interconnect.

**Automated layout adaptation.** Die shifting is one of the key challenges during mold-first FOWLP. Due to the different thermomechanical properties of the carrier, the thermo-release tape, and the epoxy molding compound, the dies move such that the die position is shifted with respect to the placement position after cooling down from compression molding. This effect is also influenced by the chemical shrinkage of the molding compound.

Die shifting can be overcome by correcting the initial placement position according to a measured shifting factor so that after the molding process, dies have the correct layout position. Another approach could be to use a fast automated optical inspection (AOI) in combination with maskless processing for die connection and rewiring. This would give the opportunity to tolerate larger die misplacement by adapting the layout to the real die position. The layouts of the proposed processes for through-mold and blind-via drilling by laser and redistribution structuring by laser direct imaging (LDI) can be automatically adapted according to measured die positions. Although these process steps are maskless, they can be highly productive. State-of-the-art laser drill equipment can manufacture more than 50 vias/s and the writing of the wiring with laser direct imaging will take around 1min for a panel as described here.

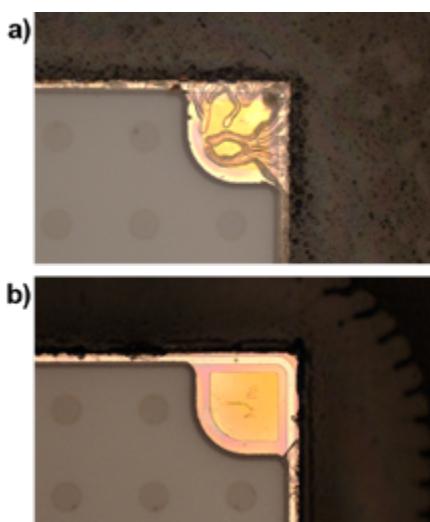
The second approach has been selected for this project. For all processed samples, the exact LED position has been measured. A software

routine has been used to automatically adapt the layout including through-mold and blind-via position, as well as the redistribution layer.

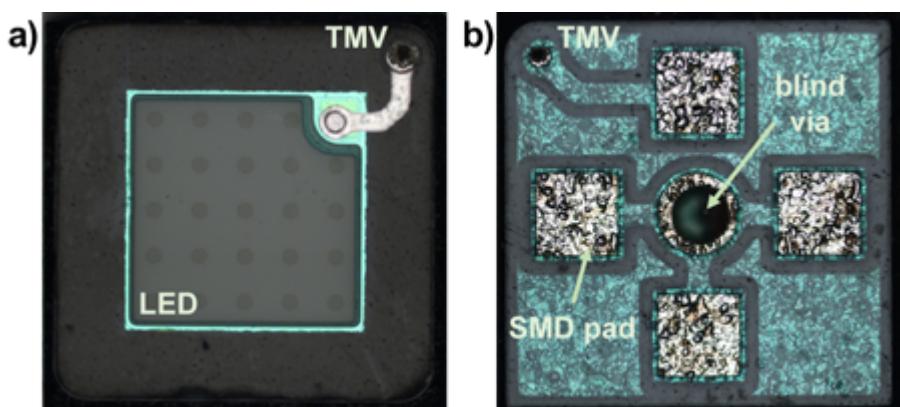
**Through-mold and blind-via drilling.** Before application of the double-sided redistribution layer, through-mold and blind vias have been drilled using a 355nm picosecond laser. For the blind via, drilling the Cu backside metallization acts as a stop layer. The advantage of laser drilling before the first dielectric layer application is that there are less limitations in via cleaning.

**Double-sided redistribution layer.** Topside redistribution is based on thin-film technology. A photosensitive dielectric dry film is laminated and structured by LDI. Dry film allows, on the one hand, the lamination and application on the reconfigured wafer with through-mold vias (TMVs), and on the other hand, the process is directly transferable to panel scale. Metallization has been done with a sputtered Cu plating base followed by Cu plating. Backside metallization has been directly applied on the EMC, also by sputtering the Cu plating base followed by Cu plating. For through-mold and blind-via metallization, a palladium activation has been applied with subsequent galvanic Cu plating. Conductor line and SMD pads have been structured by etching using a dry-film photoresist and again, LDI. As the last step before package singulation, a solder mask is applied and structured on the wafer backside. **Figure 4** depicts the final package from both the topside and the backside.

Packages have been analyzed by cross-sectioning to check interconnect reliability



**Figure 3:** a) (top) Contact pad before flash optimization; and b) (bottom) flash-free after optimization efforts.



**Figure 4:** LED package a) (left) top view, and b) (right) bottom view.

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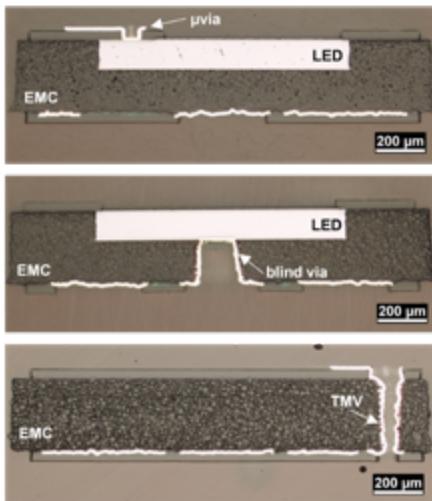
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and via metallization. **Figure 5** shows a microscopic image of the cross sections at different levels. The  $\mu$ via is well



**Figure 5:** Cross sections of an LED package.

positioned on the pad, thereby proving the layout adaptation process. Laser drill processing for the blind via worked well without damaging the die and resulted in a small via wall angle of about 10°. Cross sections also reveal a homogeneous via wall metallization and good connection without delamination or entraptments to the LED backside. TMV via drilling led to nearly straight via walls with a diameter of 100 $\mu$ m and also had homogeneous metallization and good connection to top- and backside metallization.

**Wafer-level demonstrator results.** Four (FOWLP) packaged LEDs to be used for functional testing were assembled on a substrate (**Figure 6**). Standard SMD assembly equipment was used for lead-free solder paste printing



**Figure 6:** Illuminated fan-out wafer-level LED package.

at the board level, as well as for pick-and-place and reflow soldering. LEDs could be successfully illuminated, and thereby demonstrated the overall FOWLP concept. For this study, no

converter layer was applied for white-light conversion. But the overall process flow would also allow adding a converter layer (e.g., by paste printing at the wafer- or even panel-level).

### Process upscaling to panel size

The main driver for moving from wafer sizes to larger panel sizes is a reduction of packaging cost on account of the parallelization of process steps and a higher area yield for rectangular packages on rectangular panels than on round wafers. In **Table 1**, the numbers of LED packages from this study for different wafer sizes are summarized. For example, on a

Wafer/panel size	Number of packages
200mm wafer	8.568
300mm wafer	20.107
450mm wafer	46.506
457x305mm <sup>2</sup> panel	38.236
610x457mm <sup>2</sup> panel	79.134

**Table 1:** Number of LED packages on different wafer and panel sizes.

610x457mm<sup>2</sup> panel, which is a standard printed circuit (PCB) board size, around 10x more packages can be processed as on a 200mm wafer.

When moving from round to panel formats, one can also consider different materials, equipment and processes to further lower cost. In this study, dry-film materials and maskless laser direct imaging technology was used for redistribution layer manufacturing, as one example. Both of these processes are typically used in a PCB manufacturing environment. Based on this approach, a direct upscaling from demonstrated wafer-level processing to larger panel sizes was possible. For panel demonstration, a size of 457x305mm<sup>2</sup> and a package density of about 25% comparable to the wafer-level approach has been selected. Size and package density have been mainly chosen to work with a reasonable number of LEDs.

LED assembly has been done with the same pick-and-place equipment and strategy as that used at the wafer level. Furthermore, assembly is a bottleneck as pick-and-place for one LED needs the same time at the wafer level as at the panel level. This can also easily lead to a couple of hours

of assembly time for only one panel. New strategies such as multiple area and head assembly, or advanced approaches such as collective bonding, or even self-assembly strategies should be considered in the future. Finally, 7,682 LEDs were assembled on the panel carrier, resulting in around a one hour assembly time.

At the wafer level, liquid epoxy molding compounds are dispensed in the middle of the wafer and flow during closing and compression of the tooling to fill the entire cavity. For large-area panel encapsulation, a more complex dispense pattern is needed. Panel compression molding, including EMC application, was done using an automatic liquid EMC dispense unit and a large-area compression mold machine. For encapsulation of the 457x305mm<sup>2</sup> panel, a 9-point dispense pattern was chosen—supported by flow simulations allowing filling without air entraptments and flow marks and welding lines. As a result, the LEDs were encapsulated without significant faults like air entraptments, flow marks or welding lines. The molded 457x305mm<sup>2</sup> panel after debonding is depicted in **Figure 7**.



**Figure 7:** Molded 457x305mm<sup>2</sup> panel with embedded LEDs.

RDL application is done using the same materials, equipment and process flows described above for wafer-level processing. This includes LED position measurement, layout adaptation, laser blind and TMV drilling, as well as double-sided routing. Finally, the process could be successfully scaled up from wafer- to panel-level.

### Summary

Fan-out wafer- and panel-level packaging is one of the latest trends in microelectronics packaging with the potential for miniaturization, but also for heterogeneous packaging. In this study, the mold-first approach has been chosen for

development of an LED package. Process developments and the successful overall proof of concept has been done on 200mm wafers. In a second step, the technology was scaled up to a 457x305mm<sup>2</sup> panel size using the same materials, equipment and process flow to demonstrate the low-cost and large-area capabilities of the approach.

## Acknowledgements

The authors would like to acknowledge the support of the German ministry for education and research [BMBF] and of VDI Technologiezentrum GmbH in the InteGreat project (Förderkennzeichen: 13N13133).

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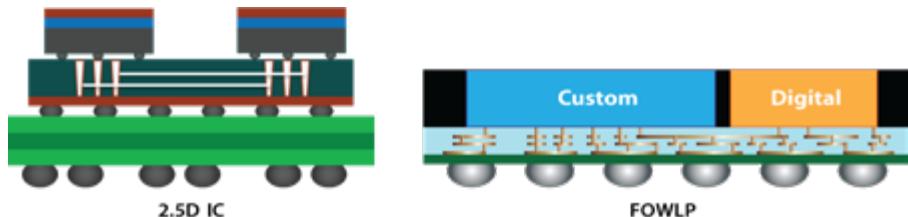
# HDAP connectivity verification: what you need to know

By Tarek Ramadan *[Mentor, a Siemens Business]*

**A**dvanced integrated circuit (IC) packaging has moved well beyond the experimental and prototyping stages [1]. Several leading foundries and outsourced assembly and test (OSAT) companies now offer high-density advanced packaging (HDAP) services to their customers. The most common approaches currently offered by foundries/OSATS are the 2.5D IC (interposer-based) style and fan-out wafer-level packaging (FOWLP) approach (single die or multi die), as shown in **Figure 1**.

Because the interposer in a 2.5D IC is similar to a traditional die (except that it doesn't include active devices), IC design groups usually own the 2.5D IC design, and use an IC-oriented design (Manhattan shapes in the layout database, SPICE/Verilog as the source netlist, etc.) and physical verification (design rule checking, or DRC) sign-off approach. In a FOWLP package, package design groups usually adopt design techniques that use spreadsheets to capture the design intent, and in-design manufacturing checks for physical verification of the package construction. Although the manufacturing steps and owners for every HDAP technology can be different (2.5D IC vs. FOWLP vs. something else), and each technology uses different data formats and tools, the verification process is almost the same.

In both cases, however, the HDAP verification flow traditionally does not include any automated layout vs. schematic (LVS) sign-off. Automated LVS is not historically popular in the packaging world because the number of components and required I/Os is usually small, so a simple spreadsheet or bonding diagram is sufficient for an eyeball check. However, as HDAP evolves and its use expands, the need for an automated flow to detect and highlight package connectivity errors has become apparent.



**Figure 1:** The most common HDAP styles currently in use are the 2.5D IC and the FOWLP.

## Automated HDAP LVS

At the IC level, the LVS process ensures that the physical layout creates the electrical circuits as designed. Further electrical analysis and simulation identifies such factors as parasitic effects, reliability protection, predicted electrical performance, etc.

For an HDAP design, the “LVS” process focuses on verifying the connectivity between all components in the HDAP. An automated HDAP LVS flow in its simplest form should verify that the interposer/package GDSII correctly connects die-to-die (for multi-die systems) and die-to-C4/BGA bumps (for both single-die and multi-die systems), as intended by the designer. Checks that can be used to verify connectivity through an entire assembly stack should include (at a minimum) the following types:

- Interposer/package standalone
  - Identify texted shorts and opens
  - Verify text labels vs. source netlist pins
- Interposer/package + virtual die pins
  - Generate die pins’ GDS from substrate connectivity planning data
  - Use virtual die pins to check connectivity from die-to-BGA through interposer/package
- Interposer/package full connectivity
  - Source netlist = SPICE, Verilog, or substrate connectivity planning spreadsheet
  - User-provided die GDS
  - Use real die pins to check connectivity from die-to-BGA through interposer/package



**Figure 2:** Using different pin names in the source netlist (left) and the layout (right) can make it impossible for the HDAP LVS process to verify the connectivity in the layout.

## Debugging connectivity errors.

Assuming that an automated HDAP LVS flow is in use, it is still a challenge—especially for the package designers—to debug the resulting package connectivity errors efficiently, particularly if the number of highlighted errors is huge. However, there are a few simple questions designers can use to help simplify and speed up the debugging process.

### 1. Do I have pin naming issues in the source netlist vs. the layout?

This is a typical issue in which the designer uses different pin naming conventions in the system source netlist vs. the interposer/package layout (neither includes dummy resistors). For example, **Figure 2** shows two connected pins that are named A (die pin) and B (package pin) in the source netlist. Those two pins are represented by two bumps in the layout: BUMP\_A (die pin) and BUMP\_B (package pin). Although BUMP\_A and BUMP\_B may be connected correctly in the layout, an HDAP LVS flow will not be able to identify this as a correct connection and errors will be flagged, as the names are different. When this issue is present, the HDAP LVS flow

probably highlights hundreds, or even thousands of errors.

## 2. Do I have GDSII export issues?

Database export issues are usually related to packaging-specific flows only (not present in 2.5D IC). Because FOWLP manufacturers require a GDSII, rather than traditional package formats like Gerber, ODB++, etc., most package design tools have now added the capability to export a GDSII of the FOWLP design. However, this capability is not 100% mature in some package design environments, so it is possible that the exported GDSII includes some faulty data. Common examples include: very small slits in the redistribution layers (RDLs) that are reported as opens in an automated HDAP LVS flow, or RDL spikes that can connect two different nets (those nets will be reported as shorts).

Typical DRC may not catch those issues, as it is designed to check manufacturability constraints, not GDSII export issues. However, foundries/OSATS should consider delivering additional DRC checks that are built specifically to detect those issues before switching to automated HDAP LVS flows.

## 3. Do I have text labels issues?

Before trying to resolve the typical opens/shorts connectivity errors in the interposer/package GDSII, it is highly recommended that the user fixes any “text-related” issues for the pins (usually bumps or pads) first (**Figure 3**). These errors are also easier to debug if the automated HDAP LVS flow reports them separately. Examples of these issues include:

- Layout pins (bumps or pads) with no text label attached to them. Fixing such an error eliminates some “opens” errors automatically.



**Figure 3:** Resolving text label issues often resolves open/short errors.

- Layout pins (bumps or pads) with more than one text label attached to them. Fixing such an error eliminates some “shorts” errors automatically.
- Floating text label that is not attached to any layout pin (bumps or pads).

## 4. Do I have ports mismatch issues?

To minimize debugging time, automated HDAP LVS flows should report any port mismatch issues separately from the typical shorts/opens errors. Extracting a layout netlist from the package/interposer GDSII and performing a source ports to layout ports comparison can identify the following issues:

- The number of layout ports is larger than the number of source ports. In this case, the extra layout ports are highlighted to the user. As an example, an extra port is reported if a layout pin has multiple labels.
- The number of layout ports is smaller than the number of source ports. In this case, the missing source ports are reported to the user. As an example, a missing port is reported if a layout pin has no label.

Both extra ports and missing ports will be reported if pins are assigned different names in the source netlist and the layout.

When the above questions have been asked and resolved, most of the connectivity errors will already be gone. The remaining errors are traditional shorts/opens that will require the designer to modify the interposer/package GDSII routing.

**Power/ground connectivity checking.** Because traditional LVS checking is insufficient for HDAP power/ground connectivity checking, designers must consider implementing alternate verification strategies to ensure all package power/ground issues are detected and resolved.

In traditional LVS flows from the system-on-chip (SoC) world, LVS will pass if there is one valid connection for VDD (or VSS), even if there

is a broken VDD (or VSS) connection somewhere else. This happens because of the way LVS engines extract the layout netlist. For example, for SPICE format netlists, multiple VDDs/VSSs in the same “.SUBCKT” are reduced to one VDD/VSS. One reason this LVS checking limitation is acceptable in the SoC world is because a broken VDD/VSS connection that is not detected will be caught in future electrical analysis (power analysis, electromigration analysis, etc.). The electrical analysis flows are well established for SoC design and sign-off.

For an HDAP with a high number of I/Os, there are typically many die VDD/VSS to package VDD/VSS connections. Using the traditional LVS approach results in the same limitation of being unable to verify all power/ground connections. However, because the electrical analysis flows are not yet 100% established for HDAP sign-off, designers can't neglect those power/ground issues by assuming they will be detected downstream. Fortunately, there are some proposed solutions for this limitation, as described below.

**1. Highlight “floating” bumps/pads geometrically.** This approach can be used for a situation in which there is a VSS/VDD open due to a missing interposer or package bump. Using traditional LVS flows, this issue will not be reported, as there are other valid VSS/VDD connections (assuming the rest of the VSS/VDD bumps are correctly connected).

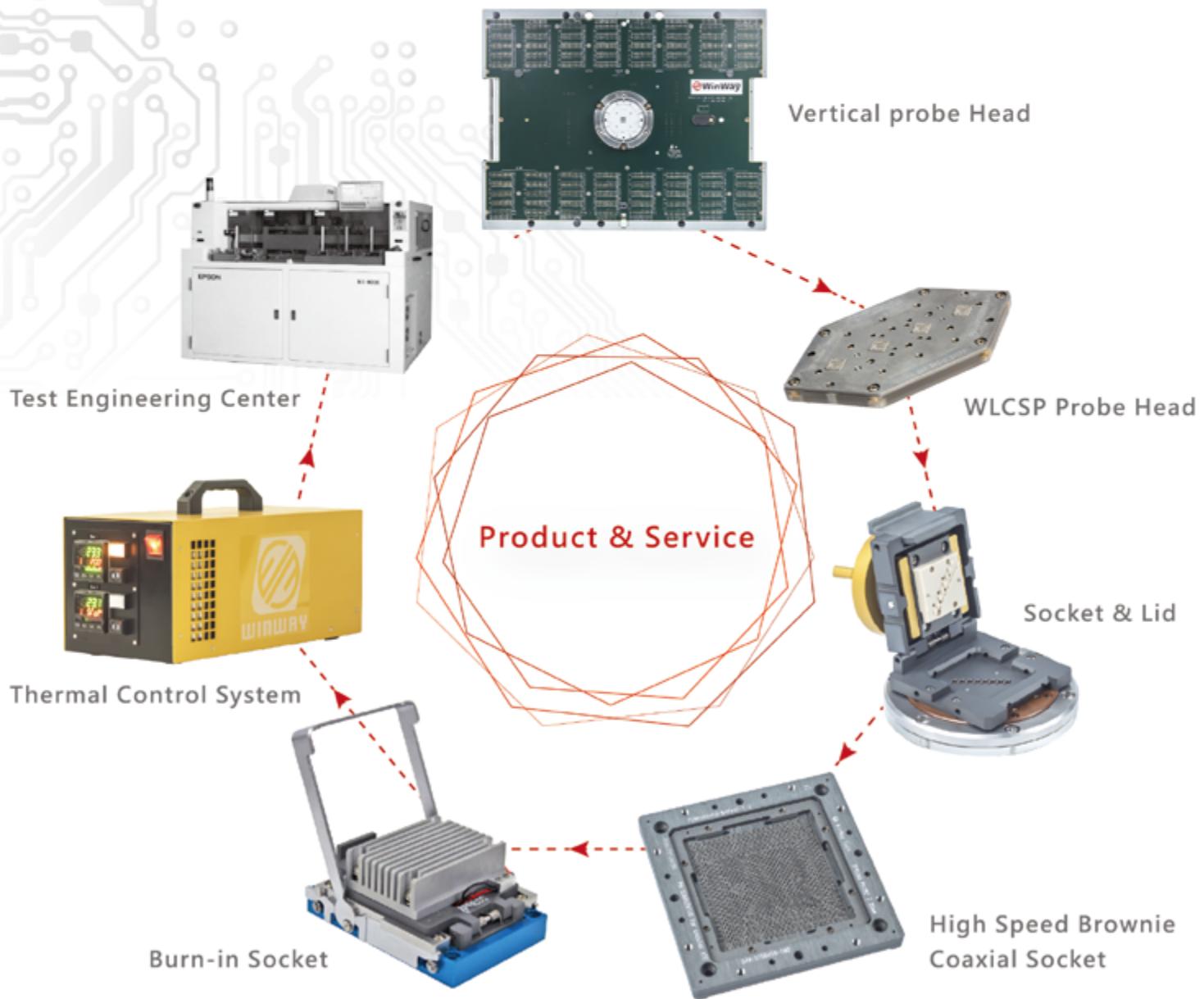
An enhanced HDAP LVS flow relies on a DRC-like approach. It highlights any die bump that doesn't have an interacting interposer/package bump, and vice versa. If there is a missing VSS/VDD die or interposer bump (that causes the open) in the assembly, it is highlighted to the user. In **Figure 4**, the die bumps are aligned on top of the interposer bumps. However, there is a missing VSS interposer bump (bottom left) that is highlighted as an error.

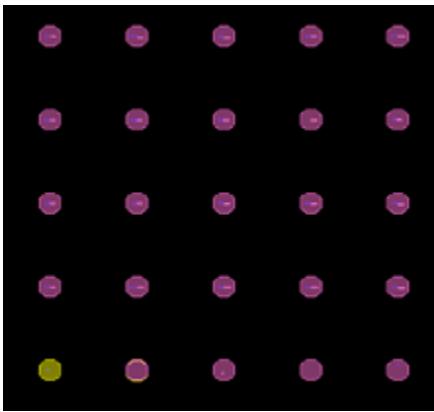
**2. Location checking for interposer/package pins.** This technique uses the same geometric checking approach, but also checks that the text labels on the interposer/package bumps are as intended by the user.



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**Figure 4:** An enhanced HDAP LVS flow can find issues like a missing VSS interposer bump.

Going back to the original source of the problem, which is the layout netlisting (reduction of many VSS/VDD pins into one VSS/VDD pin), an enhanced HDAP LVS flow takes advantage of the other netlist formats in the packaging world, like spreadsheets (comma-separated values [CSV] files) and application integration framework (AIF) files. While most package design environments can export such spreadsheets/AIFs automatically, the most efficient approach is when the enhanced HDAP LVS flow natively supports the spreadsheet netlist format.

In a typical packaging design intent spreadsheet, there are columns representing the pin name, the net name, and the bumps' (x,y) locations (Figure 5). Pin names and (x,y) location information (as intended by the designer) is input to the enhanced LVS flow as the source data. An enhanced HDAP LVS flow compares this source data to the layout to ensure every interposer/package bump is present in its expected (x,y) location in the interposer/package GDSII, and the intended text label (as the pin name) is attached. This way, the enhanced HDAP LVS flow detects any missing interposer/package VDD/VSS pins in the interposer/package GDSII.

**3. GDSII-only opens/shorts checking.** This check also evaluates interposer/package pins, but with the assumption that the die bumps are not available for checking. It can be used when designers want to

Pin Name	Net Name	(x,y) Locations					
Functional Signal	Instance Level Name	Design Name	Instance Name	Pin Number	Ref Des	Pin X	Pin Y
AC_MODE	AC_MODE	Package	C4	PAD0	U1	1802.5	1129
BUMP_AC_MODE	AC_MODE	die1	FCCC1	Bump_9_8	A1	776.755	851.61
BUMP_AC_MODE	AC_MODE	die2	FCCC2	Bump_9_8	A2	1676.755	851.61

**Figure 5:** A package spreadsheet netlist can be used by an enhanced HDAP LVS flow to check for missing interposer/package VDD/VSS pins.

check any VSS/VDD opens in the interposer/package GDSII without including the die pins in the check.

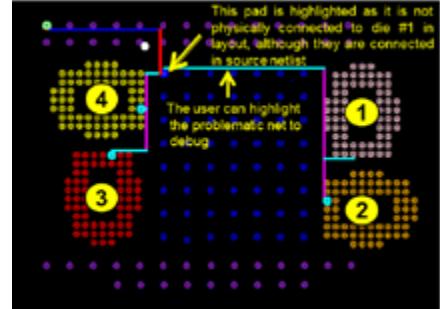
This check uses the text labels in the interposer/package GDSII to check for simple shorts/opens without comparison to a source netlist. If there are two physically connected shapes with different text labels attached to each, the LVS flow reports a short. If there are two shapes that are not physically connected, but have the same text label attached to them, the LVS flow reports an open (this check catches any two VSS/VDD shapes that are not physically connected).

#### 4. Highlight bumps that don't have complete physical connectivity.

Sometimes a VSS/VDD open is not due to a missing interposer/package bump, but is caused by a missing RDL or via polygon in the internal interposer/package connectivity. Traditional LVS flows don't explicitly report such an issue if there are other valid VSS/VDD connections.

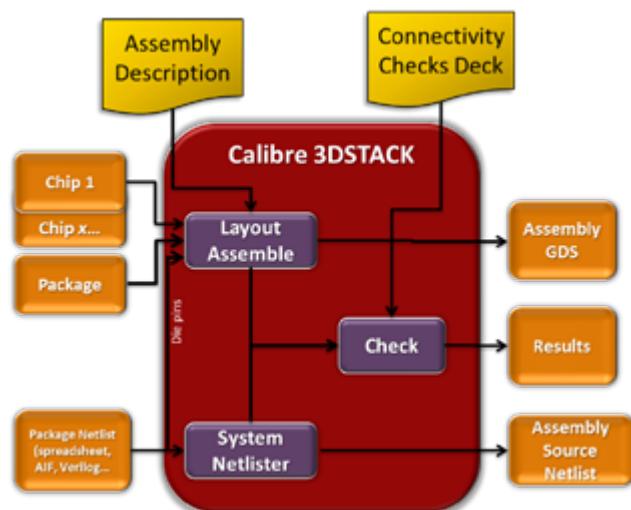
To find the issues noted above, an enhanced HDAP LVS flow checks the layout only, without a comparison to the source netlist. If it finds any interposer/package bump (with a text label attached to it as the pin) without complete physical connectivity to the die (using the interposer/package connectivity stack defined in the HDAP LVS rules), it highlights this bump as an error.

#### 5. Trace all die connectivity through interposer



**Figure 6:** Highlighting unconnected die enables the designer to fix any problematic nets.

**layers.** To ensure full connectivity is properly in place, an enhanced HDAP LVS flow must ensure that all die are connected through the interposer layers. Checking the pins alone would not catch any physical opens in an interposer net. In Figure 6, all four die should be connected through the interposer layers. However, die #1 is not connected (physical open). With the problematic bump highlighted, the user can identify the net that requires debugging.



**Figure 7:** The Calibre 3DSTACK tool checking an embedded wafer-level ball grid array (eWLB) design.

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## Integrated HDAP LVS

An integrated verification solution for HDAP inter-die and die-to-package/interposer DRC and LVS sign-off offers a significant advantage over traditional LVS flows because it can automatically evaluate all of the new challenges created by HDAP connectivity verification requirements. With a single integrated tool for both package assembly-level DRC and LVS, and native support for packaging

file formats (like spreadsheet netlists), users can simplify and speed up their package verification flow. For example, in the HDAP environment, the Calibre® 3DSTACK tool (**Figure 7**) from Mentor®, a Siemens Business, eases connectivity errors debugging as it enables:

- Standalone text-related checks (no\_texts, multi\_texts, floating\_texts, etc.);
- Standalone ports mismatch checks

(extra\_ports, missing\_ports, etc.); and

- Traditional physical opens/shorts detection.

The Calibre 3DSTACK tool also provides solutions dedicated to PWR/GND checking issues, such as:

- Geometrical highlighting of missing interposer/package bumps (floating\_pad);
- Interposer/package bumps (x,y) locations checking (compared to a design intent captured in a spreadsheet-style netlist); and
- Detecting bumps that don't have complete physical connectivity in the layout (dangling\_ports).

## Summary

With the noticeable growth of high-density advanced packaging (HDAP) technologies supported by both foundries and OSATS, the need for an automated LVS-like flow to achieve sign-off HDAP connectivity is increasing. However, using traditional, SoC world LVS flows is not ideal on account of the new challenges presented by HDAP configurations. HDAP-specific LVS flows are needed to ensure full package connectivity and performance. Moreover, these HDAP LVS flows should ideally be enhanced to support package-level designer-friendly debugging techniques. They should also utilize packaging file formats to enable advanced HDAP connectivity checking, such as power/ground connections. Automated HDAP LVS solutions are beginning to emerge to fill these needs, which should enable HDAP designers to reach new levels of confidence in their products' manufacturability and performance.

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# Have you designed for manufacturing test?

By Gerard John *[Amkor Technology, Inc.]*

**C**urrent trends in chip design promote the concept of designed for test (DfT) and designed for manufacturing (DfM). With DfT, designers add scan chains and built-in self-test (BIST) structures, etc., which ease the job of test engineers in silicon fault detection. On the other hand, DfM puts in place rules that will enable very quick ramps to high-volume production with multiple designs in multiple fabs. As noted by Intel's Clair Webb in the Intel Technology Journal, "The design and process have to be manufacturable at the beginning of the ramp. Design rules have to be defined early in the process development work to allow product design to be done in parallel with the process development [1]."

Webb's statements are commonplace in the front end of the chip design process (**Figure 1**), but do not guarantee a design that is ready for manufacturing test or high-volume test. For a chip to be "designed for manufacturing test" (DfMT) early in the process, the designer must consider the capabilities and limitations of the manufacturing test facility and design accordingly. Furthermore, if the designed chip is assembled and tested at an outsourced semiconductor assembly and test (OSAT) factory, it is important for the chip designer to align with the OSAT mindset.

This article describes the OSAT mindset, constraints, and capabilities of the manufacturing test floor. It also discusses several types of testing options such as wafer sort, partially-assembled test, final test, system-level test, and examines how the test specifications and the addition of test insert points can affect the cost of the product.

## Introduction

In his book, *Processes and Design for Manufacturing* [2], Sherif El Wakil states, "Manufacturing can be defined as the transformation of raw materials into useful products using the easiest and least expensive methods. It is not enough, therefore to process some raw materials

and obtain the desired product. It is, in fact, of major importance to achieve this goal by employing the easiest, fastest and most efficient methods. If less efficient techniques are used, the production cost of the manufactured part will be high, and the part will not be as competitive as similar parts produced by other manufacturers. Also, the production time should be as short as possible to capture a larger market share [2]."

Similarly, with manufacturing test, it is not enough to classify parts as pass or fail, but to achieve this goal in the easiest, fastest and most efficient way. A product is considered manufacturable if it can be mass produced following a recipe that produces products with consistent performance, generating little or no rejects, all within the time, resource and cost budgets. With an integrated circuit (IC), the ultimate decider whether the device is production ready is measured by its yield, while the loss associated with materials, and labor have a negligible impact on the viability of the business case.

In the semiconductor industry, DfM and DfT are hot topics with design engineers realizing their strategic importance in the front end of the manufacturing process. However, when a design/development engineer visualizes the process of releasing a device to manufacturing test, the mistaken picture of manufacturing test as involving little more than handing over test hardware, software and accompanied by on-site training comes to mind. Unfortunately, this distorted view of manufacturing test is created and fueled by the shallow and qualitative way by which the subject of manufacturing test is understood. Much of this can be attributed to the secrecy under which most test production floors operate and thereby the limited knowledge of test floor operations.

Manufacturing test refers to the process when a device moves from new product introduction (NPI) to high-volume manufacturing (HVM), where tens of

thousands of parts are tested each day. At HVM, the key elements that govern the cost of testing are equipment cost and time. While the cost for test equipment (testers, probers and handlers) (see **Figure 1**) is fixed and better understood, the time aspect is not. When considering DfMT, one must consider the time that is taken to set up the test cell (setup time), time taken for the decision to be made whether the device under test (DUT) is good or has



**Figure 1:** Test equipment.

failed the test sequences (test time), the time that is taken to retest a device, if the initial data was inconclusive (retest time), and the time taken for the device to be moved from the input medium to the test position (test socket or die location) and then to the output medium (index time).

An IC that follows DfMT will allow the use of the lowest cost tester and an efficient material handler. The design provides a good balance between multi-site operation (parallel test) and tester resources (cost), low setup times employing low-complexity test hardware and software, as well as a handler optimized for binning parts based on the test results. Additionally, if the test requirement calls for testing at other than room temperatures, the design must be robust enough that device performances are not affected by rapid heating and cooling methods employed by the handler to reduce temperature transition times.

## Why test?

In *Fundamentals of semiconductor manufacturing and process control* [3], the authors state, “In semiconductor manufacturing, the input materials are semiconductor materials, dopants, metals and insulators. The types of process that arise in manufacturing include crystal growth, oxidation, photolithography, etching, diffusion, ion implantation, planarization and deposition processes [3].”

Variations and tolerances are inevitably for input materials and processes. These variations and tolerances when stacked up during the fabrication of the integrated circuit, cause subtle, but noticeable, device-to-device performance changes, giving rise to a datasheet specification that for a particular parameter, specifies a range with a minimum, a maximum, or a typical value.

The purpose of test is to exercise the DUT, then conclude if it is operating within the datasheet/design specifications. It is not practical for testing all design specifications in manufacturing for reasons that include unavailability of the needed equipment at the manufacturing test location, or as in the case of typical values, the design guarantees the specification. Typical values are not measured during manufacturing test because they are a statistical value. An IC designer can statistically predict a typical value based on simulation data. Typical values are meant to give general downstream guidance to the circuit designer.

In “Murphy’s Law and the Risks of Designing “Off Data Sheet” [4],” it is noted that, “An example of a parameter that is commonly guaranteed by design is the operating temperature range. The part is tested at one temperature, “room,” meaning anywhere between +22°C to +27°C; it is not tested for every temperature in the device’s published operating range. Rather, design simulation allows us to predict the device’s operation over the entire range of temperature and process variations. Most manufacturers, moreover, set guard bands around the parameters to allow for these variations. Statistically, many manufacturers set a safety wall at “six sigma,” a commonly accepted way to state that the standard deviation has a 99.9997% probability of meeting the specification for that parameter. Guaranteed by design is used for the operating temperature range instead of increasing test time by three times or more [4].”

**Testing options.** Once the fabrication of the IC is complete, there are essentially

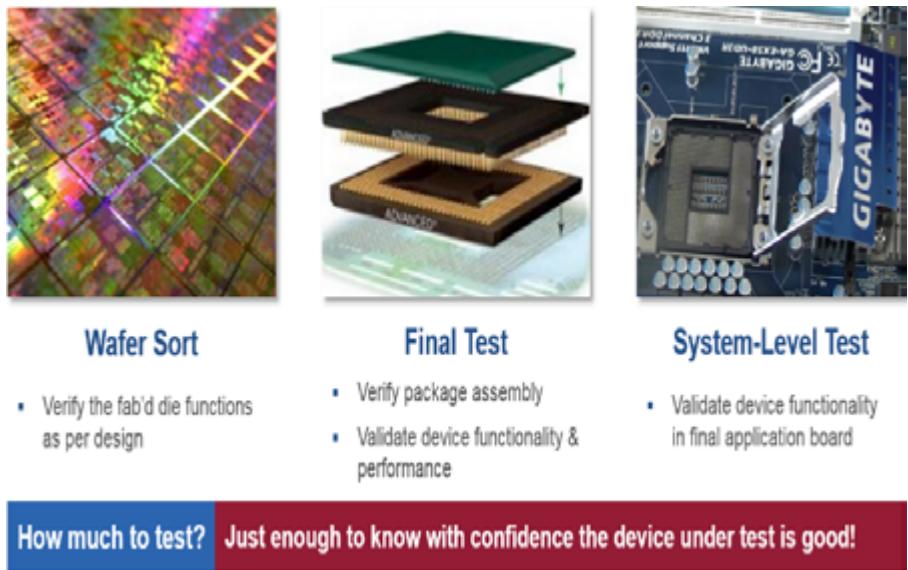


Figure 2: Testing options.

three possible methods by which its functionality can be verified (see Figure 2).

While still on the wafer, the device can be probed with needle-like wires that contact the device pads. Testing at this stage is called wafer-sort or wafer-probe. Sort refers to the process where a wafer map created at the end of all tests, classifies or sorts the dies on the wafer into various functional level bins, based on the test results. After wafer-sort, the wafer moves to the processing area, where it is thinned and diced, separating the individual dies from the others. The individual dies are selected and put into a package that protects the fragile die and allows ease of electrical interconnection to a printed circuit board. At this stage, the device is tested for performance and or functionality either in a simulated environment using automated test equipment (ATE) or tested in mission mode. The ATE option is called final test.

The mission mode option uses a system-level tester. In a system-level tester, the DUT gets mounted in a socket on the final application board. For example, if the DUT were a graphics processor, the device would be connected to a graphics board, where it would receive power, ground and interface signals from the graphics board using a socket. The board would boot up and run a series of programs to verify the chip’s functionality. This approach is particularly useful in testing application specific integrated circuits (ASICs). With the current trend of obtaining more in less (space), multiple integrated circuits are assembled into a single package. In such cases, the need for the partially assembled

unit test is gaining popularity using both final- and system-level test.

## Factory mindset

Daniel Markovitz, author of *A Factory of One*, talks about a key phrase in lean manufacturing “going to the gemba,” where the gemba (Japanese) refers to the place where work is actually done [5]. The gemba for manufacturing test is the test floor. A good understanding of the workings of a test floor lays the foundation for a design geared for manufacturing test.

“Have you designed for manufacturing test?” is the question IC designers face when their design moves from the fab to the OSAT. The answer lies in what handling mechanisms, test environment, test conditions and electrical tools are required for testing it, as discussed in the sections below.

**Handling.** At wafer sort, the handling perspective deals with the mechanical integrity of the wafer. Standard wafer loading equipment is designed to pick up full thickness wafers, i.e., 700 $\mu$ m to 850 $\mu$ m inch thickness. Furthermore, modern equipment is designed for 300mm wafers, but there may be provisions to handle wafers no smaller than 200mm. Handlers for wafer sizes below 200mm are considered obsolete and may only be available at niche test houses at a premium. Additional modifications may be required to handle wafers with excessive warpage (over 1mm across a 300mm wafer).

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From a DfMT perspective, it is important to use the 300mm wafer size and if procuring third-party wafers, specify wafer sizes no less than 200mm. If the incoming wafer thickness is less than full, it should be mounted on appropriate wafer support systems, and systems to prevent damage during shipment.

For packaged parts, a pick and place handler is capable of picking sizes from 2mm x 2mm to 80mm x 80mm. Smaller parts are usually pulled directly off the blue tape. Larger parts require special modification to the handler. Keeping the final product size within equipment capability will ensure DfMT.

**Production test floor.** A production test floor is usually noisy, with a lot of machines operating and associated particle emissions as the parts move through mechanical handlers. Due to the sensitivity of the dies on a wafer and to eliminate foreign material contamination, wafer sort is usually performed in a specially enclosed room within the test floor, maintaining a class 10K particle count with its dedicated environment control system (see **Figure 3**).

Typically, machines of the same type are confined to a particular area (**Figures 4-5**). This grouping of equipment allows the production floor manager to deploy operators based on the skill set needed. Therefore, it is common to see the test floor divided into a final-test or wafer sort area. The final-test floor is zoned as analog, digital, mixed signal, or microelectromechanical systems (MEMS) areas. Conforming the product to fall within the factory production floor layouts could potentially reduce the cost of test and reduce cycle time.



**Figure 3:** Wafer handling.

**Test conditions.** Typically, wafers are tested at room temperature. However, in certain cases, it is not uncommon for customers to require their wafer to be tested at hot (up to +125°C) and cold (below 0°C) temperatures as well. Testing a wafer below room temperature requires special insulation and the injection of dry air to prevent condensation inside the prober. An important point to note for hot testing is that the wafer will need to sit idle on the chuck, in a process called soaking, while the wafer reaches the test temperature.

If a die requires testing at two temperatures, while it seems logical to test the die at first temperature and then test at the next, cycling temperatures per die in a production environment is not practical due to the time lost at soak multiplied by the number of die per wafer. Therefore, in a production flow, the wafer is first tested at one temperature, and at the end of the lot, the prober is set to the second temperature and tested. If the second test insertion requires data obtained for the first, DfMT should address the need for the storage of these values on the die, or if done through software, the creation of a die-level test database that can be accessed by the tester.

**Test equipment.** OSAT suppliers usually have a wide variety of test



**Figure 4:** Production floor.



**Figure 5:** Adapting existing equipment.

equipment offerings. However, they tend to have a larger number of test equipment that caters to the mainstream market. Selecting a tester that is outside this footprint, could result in the product delays caused by equipment allocation issues, or the OSAT may expect the customer to consign custom equipment if required by the device. As seen in **Figure 5**, a production test floor mindset usually likes to have more of the same equipment, looks for multiple uses of the equipment and shuns one-trick ponies. OSAT suppliers however, would look favorably at upgrading equipment.

OSAT suppliers may offer more than the traditional wafer sort or final test. Designs may require multiple stages of assembly that allow potential testing of the partially assembled units using either ATE or system-level test (SLT) (see **Figure 5**). There has been a growing requirement in this area, and OSAT suppliers see value in providing these services. A good practice for DfMT is to request equipment configurations and available quantities at the target manufacturing test location from the OSAT supplier.

## Test structures

The addition of test structures in a die helps in the identification of faults and their causes. These are used extensively in test vehicles to verify a new design or a process's viability. The test structures can include resistors, capacitors, contact chains, via chains, Kelvin structures, van der Pauw structures, serpentine test structures and antenna test structures. These test structures are known as parametric test structures, and their testing is loosely called DC tests, even though the capacitance values are measured using low-frequency AC signals.

Parametric ATE (P-ATE) is designed to meet the test requirements for measurements of parameters such as resistance and capacitance. P-ATE systems are not standard equipment at OSAT suppliers. As a design moves from the test vehicle to the production device, most of these test structures are eliminated, but a key few may find their way into the production design. Often, there is a large time gap between the initial test vehicle design and the final product. Furthermore, a different team may develop the production device, and carry over design rules and test structures. Due to lack of information transfer or full understanding of the design rules, there exists the tendency of leaving test structures in place, without understanding their real purpose. Such legacy test structures should be identified and eliminated if there is no known good reason for their existence. Therefore, DfMT should remove from the production test-list, tests that call for P-ATE, but retain these structures in the design if required as a process monitor during the wafer fabrication process.

### Cost of test

Numerous articles and papers have been published on the cost of test and deal with fixed costs, production costs, production output, i.e., units per hour (UPH), multi-site efficiency and equipment utilization [6-9]. While all the above factors are true and valid, this section focuses on the selection of test points that can reduce scrap costs and the impact of the test specification to the cost of test.

**The sweet spot.** Bailey states, “There is a cost associated with a test-first approach. If you put in 100% unit test coverage, and 100% integration test cover and 100% end-to-end functionality test coverage, then you end up with 300% coverage of your system. Is the cost of maintaining 300% coverage worth it in your system? Can you get away with a grand total of 100% coverage while limiting your system to an acceptable amount of risk? Do you even need 20% coverage to reduce the risk to an acceptable level? Does it make sense to take on a test-first approach for a given feature, system, bug fix, etc.? What’s the risk vs. cost? Is there a mixed approach of getting it done now and writing a test for it later, that will provide both risk mitigation and cost-effectiveness [10]?”

Bailey lists great questions that can be adapted to semiconductor test, paraphrased as, “Are we testing too much?” which goes

back to the test list. When Markovitz talks about lean manufacturing in his book, he refers to waste as anything that does not add value and consumes resources [5]. Therefore, according to lean manufacturing techniques, any test that does not add value and uses the tester resources must be considered a waste and eliminated. To hit the sweet spot in test coverage, DfMT seeks synergy between the design team, the test development team and the applications support team, who, together,

decide which tests are essential and which ones can be eliminated.

**Test insert points.** Through the assembly flow of an IC, there are specific points at which test can be interjected into the assembly flow. The potential interjection points occur when a device moves from one assembly machine to the next, or if the device undergoes substantial change. **Figure 6** shows the test stages of wafer sort, partially assembled final test, partially

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Cost of Test/ Test Time	High	High / Long	High / Long	High / Long	High / Long
Savings by testing at this stage.	1*2*3	1*4*5	1*4*5	1*4*5	Quality
Cost of Test	1*(Hourly Rate / Unit Test Time)				
1 = (100 - stage yield)    2 = Full BOM Cost    3 = Full Assy Cost    4 = Partial BOM Cost    5 = Partial Assy Cost					

**Figure 6:** Yield, test cost and savings.

assembled system test, final test and system test. Assumptions are made on the test escape rate to derive a yield number. While testing at each stage adds cost, it identifies faulty units, which will be excluded from the following stages of assembly. The partially assembled test promotes the lean

manufacturing concept by eliminating the waste of adding further materials to a faulty part. A DfMT design should study the assembly flow, compute the cost of raw materials and compare the cost of a partially-assembled test against the potential savings gained by early detection of failing parts.

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### Summary

While test is only the indicator of product quality, its inclusion in a product manufacturing flow is essential in maintaining outgoing quality standards. It should do so without adding significant costs to the product. Therefore, the concept of “designed for manufacturing test” asks the question if the design allows testing the device in the easiest, fastest and most efficient way.

DfMT considers target tester configurations, material handling equipment while maintaining a right balance between multi-site operation, and required tester resources.

Additionally, DfMT seeks to produce a device that easily conforms to the test floor environment with little or no disruption to a standard production flow.

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### Biography

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# Flexible hybrid electronics: System as package

By Wilfried Bair [[NextFlex](#)]

**W**ith Cisco's and Ericsson's announcement in 2010 of Internet of Things (IoT) objects going to 50B units by 2020, and the upward revision by IBM two years later to 1 Trillion objects — the hype curve had reached its peak. Based on an IEEE Spectrum report published in 2016, the forecast had been reduced to 30 Billion objects by 2020.

One of the many aspects of IoT falling significantly short of expectations and forecasted volumes was the need for low-cost and easily distributable devices and objects. Traditional manufacturing methods are expensive and, in most cases, the resulting devices require additional enclosures and mounting structures to be placed in their respective placement locations, making them ill-suited for IoT applications.

Flexible hybrid electronics (FHE) offers an enabling technology to provide the low-cost, wirelessly connected and ubiquitous objects IoT needs for mass adoption. Whether in the industrial, medical or consumer space, the needs and requirements are very similar. A simple way to think of the attributes needed for FHE is “peel and stick electronics.”

FHE combines the well-established printed electronics technology with the processing power of standard silicon devices. The low cost of additive manufacturing with the high-power density of silicon-based transistors vs. all printed manufacturing approaches takes the best of both worlds.

Instead of packaged ICs, the FHE approach uses direct bare die attach vs. attaching a traditionally-packaged IC leading to smaller footprint and lower cost while maintaining reliability through system-level encapsulation. To achieve conformal bending, flexing, and in some applications, stretching of FHE, the die attach process uses ultra-thin die, as well as solderless interconnect materials and processes. Wafer thinning and dicing of ultra-thin wafers utilizes the technology advances and manufacturing

experience created for the 2.5D and 3D heterogeneous integration approach.

## State-of-the-art for flexible electronics

The current state-of-the-art for flexible electronics is based on copper flex substrates. This is based on a polyimide core substrate and coated with a copper layer. The copper conductive layer is patterned using standard photolithography and etching of the copper layer. A well-established and characterized process, but due to its subtractive nature, an expensive, and in many cases too costly for widespread adoption of IoT objects.

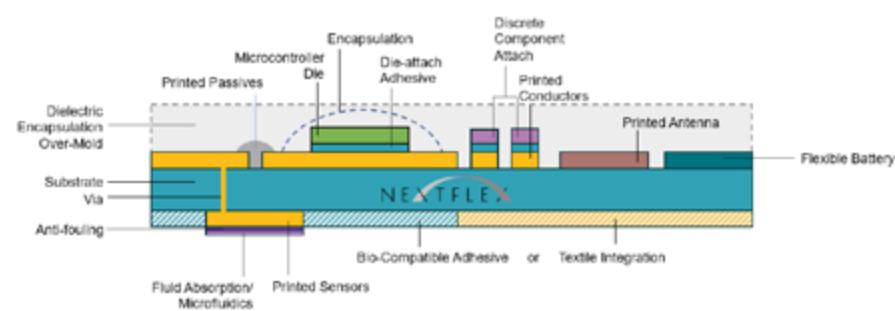
The range of materials and process options for FHE is typically chosen depending on the application and use requirements. For example, while some FHE systems may be disposable after a short period of time (e.g., smart medical patches are typically disposable with expected use periods of up to 24 hours), there are applications in the industrial and asset monitoring space with an expected lifetime of several years. System encapsulation processes and materials are adapted to the specific use case, and manufacturing materials and processes are adapted as well.

The main elements of an FHE system as shown in **Figure 1** are as follows:

**Substrates and printing.** FHE processing starts with a substrate (typically PET unless temperatures higher than 120°C are required) and adds the conductive traces and dielectric layers

using various print methods. Through-substrate vias (TSVs) are created with laser drilling and filled or lined with the silver inks typically used for printing FHE conductors. Typical substrate thicknesses are in the range of 50-200µm. For higher temperature applications polyimide has been established as the FHE substrate of choice. Flexible glass (for temperatures up to 600°C) or flexible substrate (for temperatures up to 1000°C) are available along with the corresponding high-temperature inks for printing. Stretchable applications or in-mold FHE are most commonly based on thermoformed polyurethane (TPU). Some unique materials offer flexibility and can define stretchable and non-stretchable areas within the same substrate. Area definition for stretchable and non-stretchable applications is typically done using UV/lithography processes.

**Print options.** The most common print options include screen printing, inkjet, gravure offset, aerosol jet and microvalve dispense. The various print options are combined with ink curing systems that can be thermal, ultraviolet (UV) or photonic-based in either atmospheric or inert environments. The most common inks used for an FHE system are silver-based inks—either in the form of thick-film polymer inks, or the newly developed category of silver nano inks. In addition, copper inks are moving closer to market release and will offer a material option with which the packaging and assembly space is very



**Figure 1:** Cross section of a basic FHE system.

familiar. Most FHE systems use double-sided printed substrates with the option of multi-layer routing, but preferably mounting all components on one side of the substrate and using the other side to attach the finished FHE system.

**Die attach.** To achieve the ability for the FHE system to conform to 3D surfaces as well as to support continuous flexing with small bend radii, ultra-thin die are used. A total thickness of the silicon die of 50 $\mu\text{m}$  or less is commonly referred to as ultra-thin die. Device thicknesses down to 25 $\mu\text{m}$  are used in volume production for memory stacking. FHE takes advantage of thinning, stress relief and handling developments developed for memory stacking, 2.5D interposer and 3D IC integration, but with the added difficulty of mounting the ultra-thin die onto a flexible and/or stretchable plastic substrate. For most applications a microcontroller – ideally with wireless capability like Bluetooth low energy (BLE) or similar – will be the main die integration component. Depending on the complexity of the final system, multiple die may be integrated on a single FHE system. Depending on the expected FHE system life and environmental use condition, the die will be encapsulated prior to full system encapsulation. A commercially available die bonder has been modified to allow for ultra-thin die pick and placement.

**Additional attachment methods.** Surface mount device (SMD) components, sensors and other functional devices are attached with a combination of anisotropic conductive adhesives (ACA), nonconductive adhesives (NCA) and isotropic conductive adhesives (ICA). Standard assembly equipment for adhesive dispense and component placement are used.

**Printed components.** Considering technical and commercial viability, FHE will use printed components where feasible and place commercial off-the-shelf (COTS) components as needed. Use cases for printed components include antennas, passives, as well as printed batteries.

**System encapsulation.** The front or topside of the FHE device will be encapsulated with a transparent or non-transparent conformal or low-pressure mold protective layer. Some disposable FHE systems with a short use cycle may not require encapsulation, but rather very thin layers as a moisture barrier. Standard dispense systems like slot die coaters or low-pressure molding systems are used for system encapsulation.

**System attachment and integration of printed sensing systems.** The backside of the FHE device may be used to print sensors or place sensing components. For on-body wearables, microfluidic systems are used to analyze body functions. The sensing elements are embedded in biocompatible adhesives that are used to attach the FHE device to the skin. The most common approach for non-medical applications is the use of foam-backed adhesives with the specific type selected to match the desired properties for product lifetime and the environment. With the use of functional (conductive) fibers, a direct integration into smart textiles and clothing can be achieved.

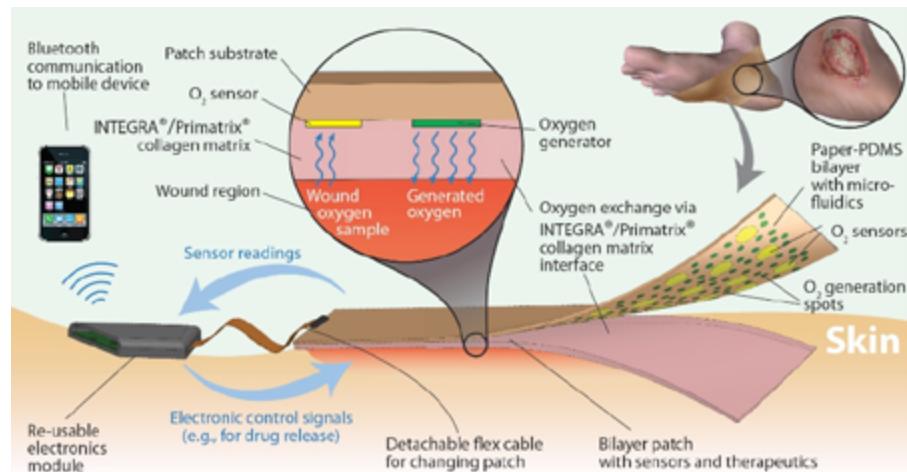
Manufacturing options for FHE are sheet-based or roll-to-roll (R2R). NextFlex has established the initial process for automated handling of sheet-based substrates. Base setup for R2R processing is in place with all key equipment available to be upgraded to R2R processing to accommodate high-volume manufacturing needs.

## Application areas of focus

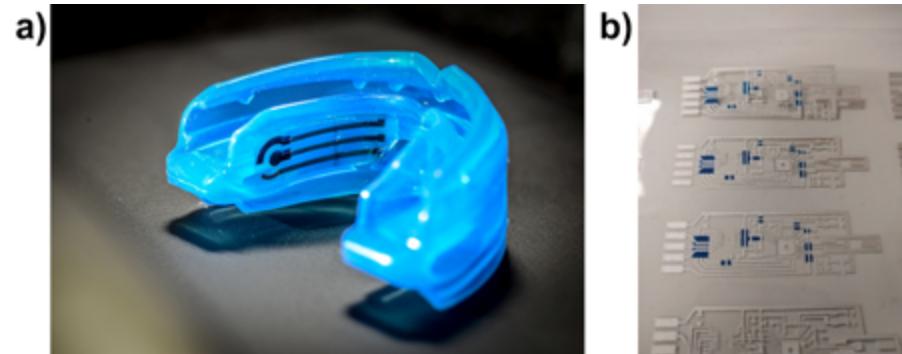
NextFlex is currently focused on four FHE-enabled application areas: 1) Human health monitoring; 2) Structural health monitoring; 3) Printed array antennas; and 4) Soft robotics.

System development activity has been most widespread in the field of human and structural health monitoring. **Figure 2** shows a smart wound dressing with the ability to monitor oxygen levels on the wound, release oxygen to achieve and maintain optimum oxygen levels and wirelessly transmit the oxygen levels to a smartphone. The project is the result of a collaborative effort of NextFlex members Integra Life Sciences, Purdue University, Western Michigan University, and the Indiana University School of Medicine.

The flexible mouthguard shown in **Figure 3** offers continuous remote monitoring of bioanalyte concentrations in saliva to infer hydration, exhaustion and mental engagement levels in higher performing athletes and warfighters.



**Figure 2:** Smart wound dressing.



**Figure 3:** a) A flexible mouth guard; and b) a printed, disposable sensor for a mouth guard.

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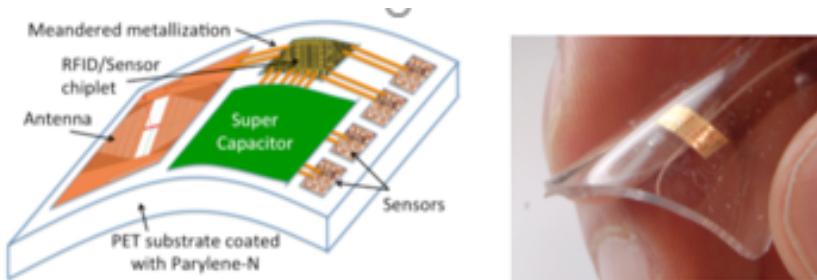


Figure 4: A Smart RFID FHE system.



Figure 5: Flexible antenna arrays.

The development was jointly performed by PARC and the University of San Diego (UCSD).

Structural health monitoring applications are extremely diverse. Primarily used to continuously monitor equipment performance (e.g., Industry 4.0 connected sensing of automated manufacturing tools), the health of safety-critical components (e.g., turbine blades in jet engines) or tracking critical components in high complexity manufacturing environments (e.g., assembly of vertical lift aircraft). **Figure 4** shows a conformal radio frequency identification (RFID) system with environmental data tracking, RF data transmission based on an ultra-low-power design and using energy harvesting of RF energy in combination with energy storage in a printed supercapacitor. This system was developed by Raytheon under the NextFlex program in collaboration with Purdue University.

FHE-based flexible antenna array technology offers significant cost savings for the overall system, as well as reduced weight and conformal application of the antenna structure to contoured surfaces. Examples of flexible antenna arrays developed by Boeing in cooperation with Georgia Tech are shown in **Figure 5**.

The underlying FHE technology enables the use of either conformal attachment of antenna arrays or direct printing of antennas. Although initially developed for military

applications, there is considerable interest in using this technology in the automotive space to support communications infrastructure needs of autonomous vehicles. Antennas can be printed directly on body panels for weight and space savings without the need for protruding antenna elements.

### Summary

Additive manufacturing-based FHE technology offers the next-generation “out of the box” electronics systems with the ability to mass customize electronics to specific user needs. Combined with 3D printing, system creation at the point of use moves closer to reality. NextFlex is funded in part by the Department of Defense to advance FHE technology to high-volume applications, to develop the FHE manufacturing ecosystem, and to inspire the next-generation workforce for the advanced manufacturing sector.

### Biography

Wilfried Bair received his Mag.rer.soc.oec. degree from the U. of Linz, Austria for Manufacturing Engineering, Computer Sciences, Marketing and Strategic Management. He is Sr. Engineering Manager at NextFlex; email [wbair@nextflex.us](mailto:wbair@nextflex.us)

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# ECTC

The 68th IEEE Electronic Components and Technology Conference

## Keynote speaker announced for ECTC 2018

The 2018 IEEE 68th Electronic Components and Technology Conference (ECTC) takes place at the Sheraton San Diego Hotel & Marina, May 29 – June 1, 2018. Attendance at the past three editions of ECTC has consistently topped 1400. Sam Karikalan, the General Chair of the 68th ECTC, noted that with IC packaging increasingly playing the role of performance enabler in integrated circuits, the conference has also rightly gained the attention of major OEMs that are focused on scaling up their system performance. "The 68th ECTC is looking forward to playing the host again for all the world's leading IDMs, wafer foundries, OSAT service providers, substrate and material vendors, equipment manufacturers, research institutions and universities that will be showcasing their cutting edge R&D in the field of microelectronics packaging over four full days," said Karikalan.

### Keynote speaker

The 68th ECTC in San Diego will feature Boon Chye (BC) Ooi, Sr. Vice President of Global Operations at Broadcom Ltd., as its luncheon keynote speaker on May 30th. BC Ooi is a well-known supply

chain guru, with four decades of experience in semiconductor manufacturing, including a long career at Intel followed by a stint at Xilinx as its SVP of Worldwide Operations. He is currently responsible

for managing worldwide manufacturing, outsourcing, procurement and logistics, planning and quality programs at Broadcom. "ECTC is honored to have BC Ooi as our luncheon keynote speaker this year," said Karikalan. "With his vast experience in running semiconductor manufacturing operations in places such as the Americas, Europe, the Caribbean and

Asia, there is no better person than BC to address the global IC packaging industry at this important juncture."

### Compelling technical program

Over 350 technical papers, on topics such as fan-out packaging and 3D/2.5D/flip-chip/wafer-level packaging, have been lined up for presentation at the 68th ECTC, in 36 oral and five interactive presentation sessions. Also, 18 professional development courses are being offered on various packaging topics. The Program Chair of the 68th ECTC, Chris Bower, noted, "As usual, this year's ECTC is packed with special sessions, with invited presentations by industry experts on topics, such as soft materials, advanced assembly, IC/package co-design and high-density packaging. The Wednesday evening plenary session on the topic "Artificial Intelligence: Impact on System Design," should be one of the highlights this year."

A number of social events will also provide ample networking opportunities for everyone at ECTC. Besides the student reception and women's panel that have become regular components of ECTC, there will also be a new young professionals event this year. Both Karikalan and Bower observed that interest in this year's ECTC from sponsors and exhibitors has been outstanding and on behalf of the ECTC executive committee, they offered sincere thanks to all of them for such support.

ECTC is sponsored by the IEEE Electronics Packaging Society. Online advance registrations are now open at [www.ectc.net](http://www.ectc.net).



## Sanjay Jha to pass baton to industry veteran Tom Caulfield

After more than four years as chief executive officer of GLOBALFOUNDRIES, Sanjay Jha will hand over the company's top position to Dr. Thomas Caulfield, Senior Vice President and



# INDUSTRY NEWS

General Manager and a highly-respected industry veteran. Caulfield joined GF in 2014 following a successful career with an impressive track record of results spanning engineering, management, operational leadership and global executive experience with leading technology companies including 17 years at IBM in a variety of senior leadership roles. During his tenure at GF, he successfully built and ramped the company's new 14nm production facility in upstate New York — one of the largest public-private partnerships in the United States.

Over the past four years, GF has established itself as the industry's second-largest pure-play foundry company. In 2015, the company acquired IBM's microelectronics business, bringing a team of more than 1,000 technologists and a portfolio of 16,000 patents. GF leveraged these capabilities to build the New York facility and to accelerate development of 7nm. The company has also pioneered differentiated FDX technology, which provides customers with a low-power,

efficient solution for the Internet of Things and expanded its leadership position in RF that enables connected intelligence. In 2017, the company announced its strategic partnership with Chengdu, China, and broke ground on a world-scale 300mm fab, which is set to begin operations next year.

"It has been an incredible four years," said Jha. "We have transformed GF into a trusted, reliable foundry for our global customer base. The acquisition of IBM's microelectronics business has allowed us to independently develop leading-edge technology including 7nm, as well as expand our leadership positions in differentiated businesses such as RF, ASICS and the FDX platform. Tom Caulfield is the right person to build on this record of success and strengthen GF's position as a leading foundry partner to the semiconductor industry."

"I am honored to be given this chance to lead GF at such an exciting time at the company and in our industry," said Caulfield, incoming CEO of GF. "With exciting new customers coming into the

market, we have the unique technology portfolio and executional track record to reset the competitive playing field in the rapidly-growing foundry segment. And we will continue to change the industry that is changing the world."

"GF is a strategic asset for the global semiconductor industry and our shareholder. We will continue to invest to differentiate and grow the business and further consolidate the industry through partnerships, in a way that allows us to better serve our customers," said Ahmed Yahia Al Idrissi, Chairman of the GF Board of Directors. "Sanjay delivered on strategic milestones, which set the company on the right path, and we would like to thank him for his significant contributions. Tom, with his 25-year track-record of operational excellence and delivering for customers, will take the company to the next level of success."

Jha intends to work closely with the company's shareholder, Mubadala Investment Company, to explore the development and build out of potential future systems businesses.



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\*Technical papers are required\*

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<b>Brewer Science</b> <a href="http://www.brewerscience.com">www.brewerscience.com</a> .....	8
<b>DL Technology</b> <a href="http://www.dltechnology.com">www.dltechnology.com</a> .....	36
<b>E-tec Interconnect</b> <a href="http://www.e-tec.com">www.e-tec.com</a> .....	3
<b>ECTC</b> <a href="http://www.ectc.net">www.ectc.net</a> .....	48
<b>EDA Industries</b> <a href="http://www.eda-industries.net">www.eda-industries.net</a> .....	16
<b>EV Group</b> <a href="http://www.evgroup.com">www.evgroup.com</a> .....	2
<b>IMAT</b> <a href="http://www.imatinc.com">www.imatinc.com</a> .....	35
<b>Indium Corporation</b> <a href="http://www.indium.com/SiP/CSR">www.indium.com/SiP/CSR</a> .....	19
<b>Ironwood Electronics</b> <a href="http://www.ironwoodelectronics.com">www.ironwoodelectronics.com</a> .....	41
<b>IWLPC</b> <a href="http://www.iwlpc.com">www.iwlpc.com</a> .....	47
<b>Johnstech</b> <a href="http://www.johnstech.com">www.johnstech.com</a> .....	IBC
<b>MacDermid Enthone/Alpha Advanced Materials</b> <a href="http://www.macdermid.com">www.macdermid.com</a> ....	15
<b>Micro Control</b> <a href="http://www.microcontrol.com">www.microcontrol.com</a> .....	25
<b>MRSI Systems</b> <a href="http://www.mrsisystems.com">www.mrsisystems.com</a> .....	22
<b>Nordson DAGE</b> <a href="http://www.nordsondage.com/XM8000">www.nordsondage.com/XM8000</a> .....	12
<b>Plasma Etch</b> <a href="http://www.plasmaetch.com">www.plasmaetch.com</a> .....	30
<b>Plastronics</b> <a href="http://www.plastronics.com">www.plastronics.com</a> .....	39
<b>SEMI</b> <a href="http://www.semiconsea.org">www.semiconsea.org</a> .....	45,46
<b>Sonix</b> <a href="http://www.sonix.com">www.sonix.com</a> .....	3
<b>TEL Advanced Packaging</b> <a href="http://www.tel.com">www.tel.com</a> .....	9
<b>Test Tooling Solutions Group</b> <a href="http://www.tts-grp.com">www.tts-grp.com</a> .....	42
<b>Toray Industries</b> <a href="http://www.toray.co.jp/english/electronic">www.toray.co.jp/english/electronic</a> .....	4,5
<b>Veeco Instruments</b> <a href="http://www.veeco.com/PSP">www.veeco.com/PSP</a> .....	IFC
<b>Winway Technology</b> <a href="http://www.winwayglobal.com">www.winwayglobal.com</a> .....	33
<b>Yield Engineering</b> <a href="http://www.yieldengineering.com">www.yieldengineering.com</a> .....	28
<b>ZEISS</b> <a href="http://www.zeiss.com/pcs-csr">www.zeiss.com/pcs-csr</a> .....	6

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