

# Chip Scale Review

## 2016 Editorial Calendar

**(Editorial close date: 11/20)**

**January • February**

*(\* denotes show distribution)*

Packaging trends	<ul style="list-style-type: none"> <li>• <b>SEMI ISS (Industry Strategy Symposium)</b> Half Moon Bay, CA (Jan 10-13)</li> <li>• <b>SEMI European 3D Summit</b> Grenoble, France (Jan 18-20) *</li> <li>• <b>SMTA Pan Pac Microelectronics Symposium *</b> Kohala Coast, Hawaii (Jan 25-28)</li> <li>• <b>SEMICON Korea</b> Seoul, Korea (January 27-29)</li> <li>• <b>BiTS Workshop *</b> Mesa, AZ (March 6-9)</li> <li>• <b>APEX Expo</b> Las Vegas, NV (March 15-17)</li> <li>• <b>IMAPS Device Packaging (DPC) *</b> Fountain Hills, AZ (March 15-17)</li> <li>• <b>SEMICON China* Productronica China</b> Shanghai China (March 15-17)</li> </ul>
Assembly materials	
Advanced underfills for nex-gen flip chip applications	
Wafer carrier solutions	
3D package reliability	
Metrology for 3D integration	
Advances in wafer probing	
Reducing the cost of test	
Socket contact technologies	

**International Directory of Test and Burn-in Socket Suppliers**

**Ad Space Close Jan 22 - Ad Materials Deadline Jan 29**

**(Editorial close date: 12/19)**

**March • April**

MEMS / sensors update	<ul style="list-style-type: none"> <li>• <b>SEMICON South East Asia</b> Penang, Malaysia (Apr 26-28)</li> <li>• <b>MEPTEC MEMS Technology Symposium *</b> San Jose, CA (TBD)</li> <li>• <b>IoT Symposium *</b> San Jose, CA (TBD)</li> <li>• <b>ECTC *</b> Las Vegas, NV (May 31- June 3)</li> </ul>
Cu pillar technology	
Flexible substrates	
FOWLP	
Die-to-wafer stacking	
Heterogeneous integration	
Packaging of high-power devices	
Glass interposers	
TSV technologies	

**Ad Space Close Feb 19 - Materials Close Feb 26**

**(Editorial close date: 3/11)**

**May • June**

Industry market update	<ul style="list-style-type: none"> <li>• <b>IMAPS Advanced Technology Workshop *</b> Dearborn, MI (TBD)</li> <li>• <b>IEEE/SW Test Workshop (SWTW)</b> San Diego, CA (TBD)</li> <li>• <b>SEMI Europe Packaging Tech Seminar *</b> Porto, Portugal (TBD)</li> <li>• <b>SEMICON West *</b> San Francisco, CA (July 12-14)</li> </ul>
Package optimization & failure analysis with 3D X-ray	
Failure analysis methodologies for advanced packaging	
Multi-chip packaging technology advances	
Ultra-thin embedded packaging	
Metrology for advanced packaging	
Packaging materials update	
3D integration for tomorrow's devices	
Lithography challenges	

**Ad Space Close May 20 - Ad Materials Close May 27**