

Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 20, Number 1

January • February 2016

Temporary wafer carrier solutions for thin FOWLP and eWLB-based PoP

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- Wafer probing & burn-in
- Fault isolation with 100nm² resolution
- Defect detection & metrology
- Recent advances in 3D package reliability
- Heat sinking through socket contact technologies

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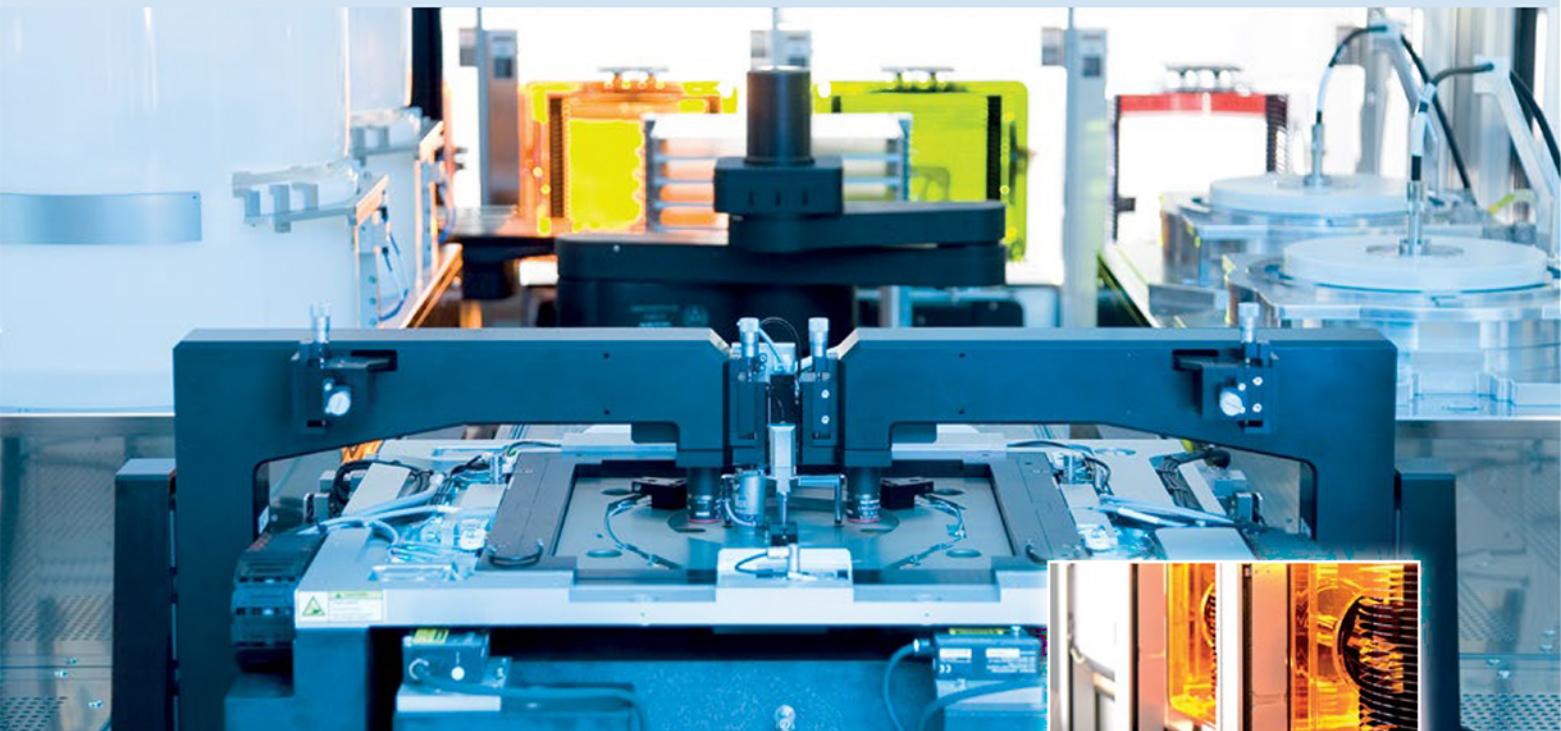
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Fan-out wafer-level packaging (FOWLP) uses mold compound to embed various functional dies. Continuous reduction in package thickness for next-generation mobile devices as well as stacked package-on-package (PoP) demands molded wafer thicknesses of less than 300µm, resulting in high bow and warp values. The successful development of a joint solution of temporary bonding process, material, equipment and fabrication steps, enables flattening and processing of FOWLP reconstituted wafers through standard 300mm lines.

Photo courtesy of NANIUM and EV Group

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MARKET OUTLOOK



Game changers: outlook for the semiconductor packaging materials market

By Dan Tracy [SEMI] and Jan Vardaman [TechSearch International, Inc.]

The semiconductor industry is in an unprecedented era of change and the semiconductor packaging materials segment is no exception. The newly released “*Global Semiconductor Packaging Materials Outlook — 2015/2016 Edition*” report by SEMI and TechSearch International finds that the \$18 billion semiconductor packaging materials market will undergo steady single-digit unit volume growth for many material segments through 2019, including laminate substrates, IC lead frames, underfill, and copper wire. With the decrease in the price of metals combined with intense price pressures and a shift in the type of packages required for mobile products (still the growth driver for unit volumes), the industry is projected to see lower revenue growth in several segments starting in 2017.

FO-WLP: a disruptive technology

Fan-out wafer-level packaging (FO-WLP) is a disruptive technology that will have a significant impact on the electronics industry and the consumption of semiconductor packaging materials in the coming years.

WLP has seen strong growth, especially in the mobile devices, because it provides a low-profile package that meets the requirements of many smartphone makers. As companies move to the next semiconductor technology node, smaller die are possible, allowing a greater number of die per wafer. At the same time the number of I/Os is increasing, and to route them, a conventional WLP would require small diameter solder balls with fine pitch. Qualcomm has published information on the reliability challenges of going to $\leq 0.35\text{mm}$ pitch with a conventional fan-in WLP. Growth in

FO-WLP is shown in **Figure 1**.

The use of a FO-WLP allows a company to continue taking advantage of the powerful economics of die shrink, while also meeting the small form factor, low-profile package requirements of mobile devices. FO-WLP is disruptive technology because there is no substrate and thin-film metallization is used for interconnect instead of bumps or wires. The use of redistribution layers patterned with semiconductor technology makes it possible to achieve much finer feature sizes $\leq 5\mu\text{m}$ lines and spaces, than conventional organic substrate technologies.

With the use of FO-WLP for the logic bottom package in a package-on-package (PoP) configuration, the ultra thin target of $<0.8\text{mm}$ PoP can be met. The only lower-profile PoP with memory and logic is a 3D IC memory and logic stack using through-silicon vias (TSVs). Such an approach is costly, however, and there are no thermal solutions for this stack in mobile applications.

The use of FO-WLP instead of a flip-chip on laminate substrate in the bottom PoP, means that not only will there be less substrates, but also less use of flip-chip underfill material. However, the demand for dielectrics used in the fabrication of the redistribution layer (RDL) will drive growth in the market for dielectric materials.

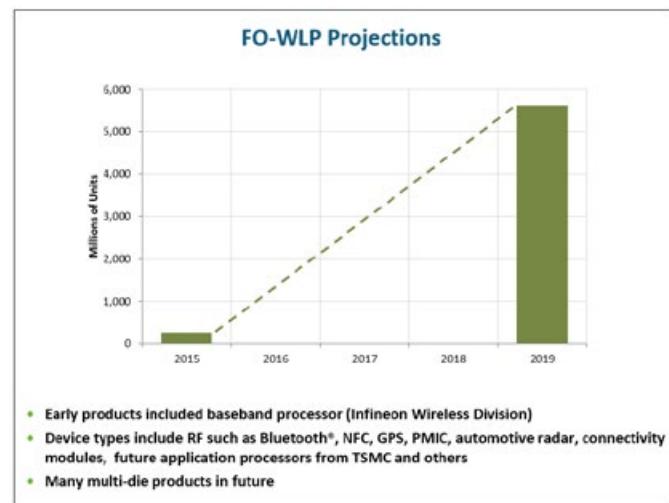


Figure 1: FO-WLP projections. SOURCE: TechSearch International.

Shifts in packaging technology impact material use

The semiconductor industry has undergone radical changes in the types of packages it the past that have resulted in dramatic changes in assembly methods and the materials used in the process. One of the first major shifts was the movement from wire bond to flip-chip interconnect. Flip-chip interconnect was introduced in the 1960s by IBM, and the first version used a copper ball (the process was called SLT) and made famous with the introduction of IBM's evaporation process called Controlled Collapse Chip Connection, often abbreviated as C4.

When Intel shifted from ceramic to laminate technology it helped to drive the flip-chip infrastructure development enabling a more widespread adoption of the technology. On the materials side, demand increased for laminate substrates and many suppliers entered the market. The need for underfill material resulted from the challenge to manage the coefficient of thermal expansion (CTE)



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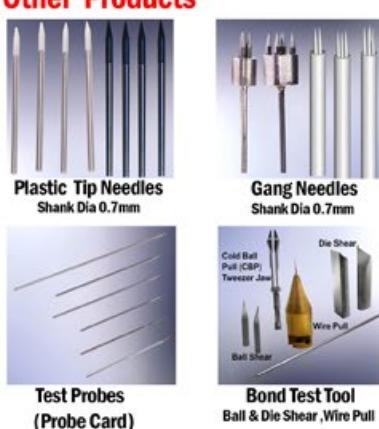
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mismatch between the silicon chip and the laminate substrate.

Another monumental shift occurred when the industry began the transition from solder bump to copper pillar, just as it moved from an evaporated bump to a plated process. In this case, Intel's adoption of a copper pillar has helped to develop the infrastructure.

Even within the wire bond segment, the industry has seen a transition from gold wire to copper, and even silver alloy wire. This transition was driven by the rising price of gold, but has continued even with the recent price declines.

The move to FO-WLP will have as great an impact as Intel's adoption of Cu pillar. This time, however, the players adopting the new technology resulting in the change are TSMC the foundry, and Apple, the end customer.

Slow revenue growth drives M&A activity

The semiconductor industry is maturing and is seeing an unprecedented number of merger and acquisition (M&A) transactions that are consolidating the industry. Several reasons for the increase in M&A activity have been suggested, including:

- Inexpensive capital (interest rates are at historic lows);
- Long-term strategic plans to increase shareholder value by broadening business and need to maintain growth in a maturing industry (revenue growth targets cannot be met by growing internal sales only);
- Rising product development costs and the need to quickly fill gaps in product portfolio to meet anticipated industry needs; and
- Need to acquire new technology or broaden into new product areas.

Constrained industry growth and the trend towards lower-cost electronics has reshaped the packaging material supplier landscape. Changes in material sets, emergence of new package types, and cost reduction pressures have resulted in recent consolidation in different material segments. In addition, material

consumption in some segments is declining resulting in little or no revenue growth. For many companies, the only way to generate strong growth or enter new markets is to merge or seek an acquisition. That is what we are seeing in today's industry.

Packaging materials market outlook

The total semiconductor packaging materials market, including lead frames, organic substrates, bonding wire, mold compound, underfill, liquid encapsulants, die attach materials, solder balls, wafer-level package dielectrics, and thermal interface materials market will remain around an \$18 billion market, despite the fact that many segments will see growing demand for materials in terms of volumes. Many of the material sectors will continue to be dominated by a few large suppliers, with smaller suppliers offering specialty products or regional favorites.

Understanding the changing packaging trends and the material requirements that meet the needs of the industry will be critical to survival. In an industry that is driven by mobile phone volumes where products ramp in four to five months and only have a lifetime of a year, there is no room for mistakes. Darwin's theory rules.

The electronics industry remains in a time of change. Just as consolidation is taking place in the semiconductor companies and assembly and packaging subcontractors, it will also increasingly take place in the materials sector.

Biographies

Dan Tracy received his BS in Chemistry from State U. of New York (SUNY), College of Environmental Science and Forestry; an MS in Materials Science & Engineering from Rochester Institute of Technology; and a PhD in Materials Engineering from Rensselaer Polytechnic Institute. He is a Sr. Director, Industry Research at SEMI; email drtracy@semi.org

Jan Vardaman received her BA from Mercer U., and MA in Economics from the U. of Texas; she is President of TechSearch International, Inc.



Polariscopy reveals TSV stress fields

By Ingrid De Wolf [imec/KU Leuven, Belgium]

Imec, in collaboration with PVA Metrology & Plasma solutions, has explored the use of infrared polariscopy for the failure and stress analysis of Cu through-silicon vias (Cu TSVs) (**Figure 1**). This work

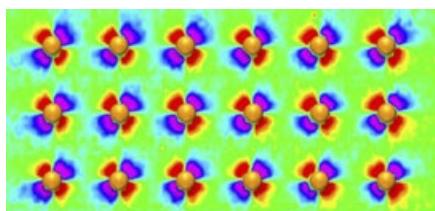


Figure 1: SIREX map of the stress fields near an array of Cu TSVs.

showed that with polariscopy, differences in principal stress components near TSVs can be detected with an unequalled sensitivity of a few kPa. The technique also promises to indirectly detect failures (i.e., voids, delamination) affecting this stress field. The tool will contribute to a better analysis and control of the TSV quality in 3D-stacked ICs. Additionally, it will help the industry to determine a “keep-out-zone,” the zone around a TSV where transistors “feel” the stress from the TSV. The results were presented at the International Symposium for Testing and Failure Analysis (ISTFA 2015).

Cu TSVs: the need for new analysis techniques

The further miniaturization and performance enhancement of electronic systems will more and more require the use of 3D system integration schemes. In this challenging configuration, Si dies are thinned and stacked on top of each other. They are electrically interconnected by Cu nails through the Si, the so-called Cu TSVs.

One of the main problems associated with TSVs is stress induced by the TSV in the surrounding Si. This stress will

affect the electrical properties of nearby transistors. To avoid this interaction, TSVs typically have a keep-out-zone around them. On the plus side, this stress field can be expected to be sensitive to defects in the TSV such as large voids and delamination. Monitoring of the stress can be used indirectly for processing control and failure analysis. The industry is indeed looking for techniques that allow determination of the keep-out-zone, and ways to detect voids and any defects in TSVs as early as possible in the processing sequence.

Most existing techniques for the stress analysis of Cu TSVs are not adequate enough. Micro-Raman microscopy, for example, in combination with finite element models, can provide local information on the stress fields. But for this purpose, the technique is slow, the analysis is complicated, and its sensitivity is rather poor (at best about 10MPa).

Polariscopy

The photoelastic method goes back a long time in history. It is based on the discovery of David Brewster (known better from the “Brewster angle”) in 1816, that, when looking at polarized light through a stressed glass, a color pattern can be seen. Brewster already suggested that this could be used for stress measurements, but only around 1920, especially thanks to the work of E.G. Coker, did it become truly applied.

Timoshenko and Goodier, in their well-known and still extensively used book on the “Theory of Elasticity,” describe the method in more detail, explaining how principal stresses change the velocity of light [1]. The basic principle behind the technique is simple. Assume a monochromatic light beam, polarized along, for example, the direction OA (**Figure 2**). This can be written as a wave with a certain amplitude A_0 and frequency v : $A(t)=A_0 \cos(2\pi vt)$. The x and y components of this wave can be

written as $A_x(t)=A_0 \cos \alpha \cos(2\pi vt)$ and $A_y(t)=A_0 \sin \alpha \cos(2\pi vt)$. If this light is incident on an isotropic transparent plate with thickness d , it will come out after some time $t = d/v$, where v is the velocity of the light. However, this velocity is not necessarily the same for both components. Indeed, if principle stresses σ_x and σ_y are present in the plate, they might change the velocity of the A_x and A_y component of the light in a different way. How much they affect the velocity depends on the stress-optical coefficient, C , of the material. As a result, the velocity of the A_x and A_y component of the light in the plate, and as a consequence, the time the wave needs to travel through the plate, will be different: $t_x = d/v_x$ and $t_y = d/v_y$. So, when the wave comes at the other side of the plate, there will be a phase difference between the two components: $\Delta = 2\pi v (t_y - t_x)$. This phase difference is proportional to the principle stresses and the thickness of the plate: $\Delta = (2\pi d/\lambda) (\sigma_y - \sigma_x)$. Stress variations in such a plate will cause different retardations of the light wave and this causes interference patterns, as was observed by Brewster. For anisotropic materials such as silicon, the theory is a bit more complex, as C will depend on the crystal directions of the material, but the basic principle, that changes in the polarization of the light can be related to stress in the sample, holds.

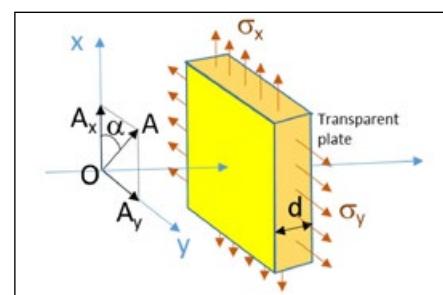


Figure 2: Illustration of the principle of the photoelastic method for stress measurements.

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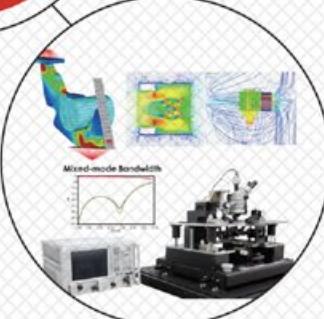
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Polariscope makes use of this photoelastic effect: when stress is present in a photoelastic material such as silicon, the material becomes birefringent. This means that a beam of light passing through the material experiences two different refractive indices. When the incident light is linearly polarized, the light that passes the stressed material, depolarizes. The amount of depolarization depends on the difference between the normal stresses. Imaging techniques that exploit this photoelastic mechanism can, in principle, detect and visualize any stress in Si wafers and devices.

It is clear from the above example that transparent material is required. Silicon is not transparent for visible light, but it is, depending on the doping, for infrared light. For this reason, this technique can be applied to study stress in silicon wafers, using, for example, scanning infrared depolarization (SIRD), a technique whereby a wafer is rotated and scanned with a polarized IR laser beam and the depolarization of the transmitted light is studied. This provides wafer maps as shown in **Figure 3** for two wafers thinned using different procedures, providing information on global and local stress field and changes due to the processing of the wafers (**Figure 3**).

Polariscope: a champion in sensitivity

Imec has explored the use of polariscope as a means to study stress fields near TSVs. In this case, transmission of the light through the silicon was not possible, but the technique also works in reflection.

One such technique is SIREX, a reflection-based polarimeter developed by PVA (**Figure 4**). Scanning infrared stress explorer (SIREX) uses a near-infrared laser diode as a scanning probe. This allows a mapping of the stress fields with a lateral resolution of only a few microns. The technique shows a superior sensitivity for differences in stresses (down to a few kPa) compared to methods such as Raman spectroscopy.

Mapping stress fields near TSVs

The SIREX technique was successfully applied to a processed Si chip containing transistors and TSVs. A depolarization

contrast map of part of the chip clearly visualizes the shear stress fields. In **Figure 5a**, a zoom-in reveals a stress field measured around a 6x6 array of 5 μm diameter/50 μm deep Cu-TSVs. The stress field is visualized as a butterfly pattern. **Figure 5b** is a map of the (shear) stress field near a group of 5 TSVs. Here, the overlapping stresses clearly generate a larger stress field, and hence, a larger keep-out-zone.

To confirm that polariscope indeed detects the TSV stress fields, samples were measured before and after Cu filling of the TSVs. While samples with Cu-filled TSVs clearly show a stress field, no butterfly patterns are visible for samples with empty TSVs. The researchers also find a good correlation between the SIREX technique and Raman spectroscopy data. The results confirm that only the TSV filling steps introduce large stresses in Si.

Void detection

The SIREX technique should also be able to detect anything that affects the stress near TSVs, such as large voids within the TSV. First results indicate that the technique can indeed detect TSV failures (voids) affecting this stress: SIREX shows clear differences between good samples (void free) and defective samples (with voids). And although further research is required to understand the technique's sensitivity and limitations, it shows great promise both as a stress measurement technique, and as a failure analysis and process control technique.

Reference

1. Timoshenko and Goodier, "Theory of Elasticity," McGraw-Hill book company, 1951.

Biography

Ingrid De Wolf received a PhD in Physics from the KU Leuven, Belgium, and is Chief Scientist at imec, and a Professor at KU Leuven, Belgium; email ingrid.dewolf@imec.be

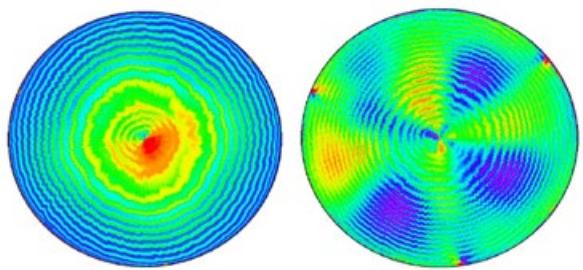


Figure 3: Wafer maps for two wafers thinned using different procedures. These maps provide information on global and local stress fields, as well as changes incurred during processing of the wafers.

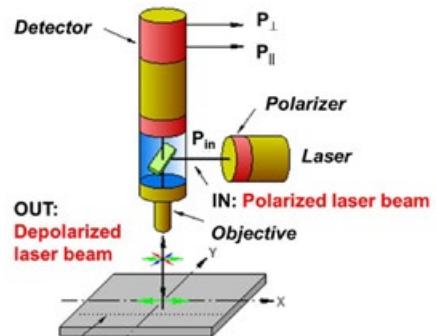
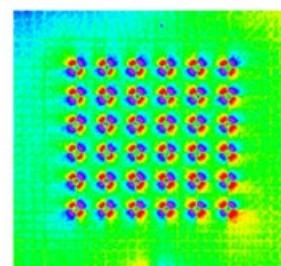


Figure 4: Measurement principle of the SIREX system, as developed by PVA.

a) Array of single 5μm x 50μm TSVs



b) Group of 5 5μm x 50μm TSVs

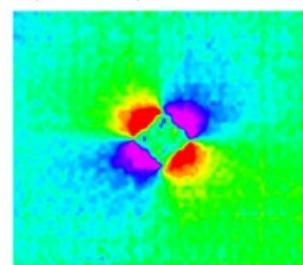


Figure 5: SIREX map of the shear stress equivalent of part of a chip: a) (top) Zoom-in on an array of 5 μm diameter, 50 μm depth Cu-TSVs; and b) (bottom) Zoom-in on a group of TSVs.

High resolution electron beam induced resistance change for fault isolation with 100nm² resolution

By Brett A. Buchea, Christopher S. Butler, H. J. Ryu, Wen-hsien Chuang, Martin von Haartman, Tom Tong [Intel]

ISTFA 2015: Conference Proceedings from the 41st International Symposium for Testing and Failure Analysis, November 1–5, 2015, Portland, Oregon, USA, ASM International. Abbreviated version reprinted with permission of ASM International.

A new fault isolation technique, Electron Beam Induced Resistance Change (EBIRCh) [1], allows for the direct stimulation and localization of eBeam current sensitive defects with resolution of approximately 100nm². Notwithstanding that the full range of capabilities of EBIRCh has not yet been demonstrated it has been shown to be advantageous at capturing both subsurface and surface-level shorting defects with different resistances in FE and BE structures on Intel's state-of-the-art test vehicles and products.

Historically capturing shorts in complex networks is resource intensive. Nanoprobing and DC measurements can be time consuming to perform and frequently allow only for the verification of a short at a given layer, requiring multiple measurement/de-processing cycles for full defect isolation often involving tedious visual inspections. Techniques, such as electron beam absorbed current (EBAC) [2,3], have improved the ability to resolve shorts through subsurface network visualization but still fail to offer

direct defect isolation of shorts. By measuring the resistance change across a defect junction as the beam scans the sample surface, a one-to-one pixel-to-spatial-location bitmap is produced. Overlaying with the SEM image gives a direct visualization of the short location (Figure 1).

EBIRCh has been shown to work over a wide range of defects, significantly decreasing the time required for isolation of shorts through straightforward high resolution imagery, allowing for explicit visual defect isolation.

Electron beam induced resistance change system details

The EBIRCh technique can readily be performed with some alterations to an EBAC capable nanoProber system. The system itself (Figure 2) consists of a SEM, nanoprobe tips, current or voltage source, and a variable gain amplifier. For the system to operate a current or voltage bias is applied across the junction as the SEM scans the sample surface, when the eBeam encounters the defect its resistance is altered. The output of the amplifier is then measured, the amplitude of which is



Figure 1: Sample with a known defect on an Intel Valleyview CPU. Green overlay is the post-processed EBIRCh image; greyscale is the SEM image.

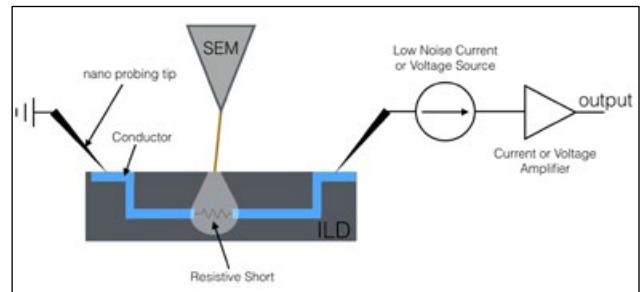


Figure 2: EBIRCh system schematic [1].

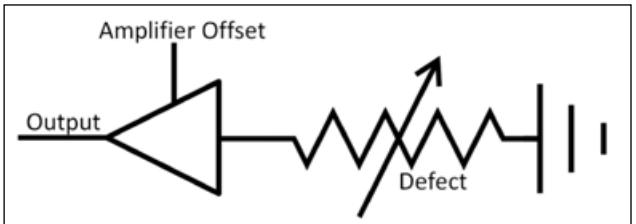


Figure 3: EBIRCh setup for constant voltage supply. The variable resistor represents the defect with a variable resistance as the beam scans across it.

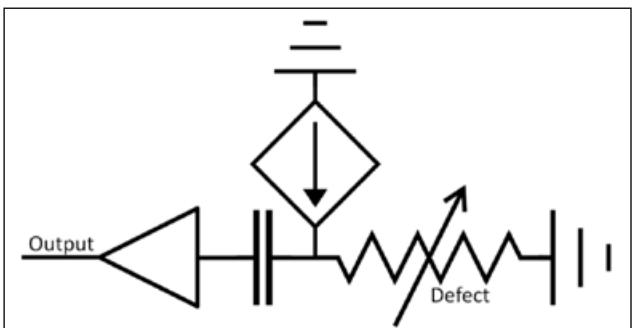


Figure 4: EBIRCh setup for constant current supply. The variable resistor represents the defect with a variable resistance as the beam scans across it.

recorded in a spatially relevant bitmap, and simultaneously the SEM image is recorded for overlay and post processing. For EBIRCh to function the beam needs to be able to interact with the defect in such a way as to alter its resistance thereby producing a small change in the circuit

that can be measured by the amplifier. This requires high beam energy at the depth of interest. In general the larger the beam current the better but variations, or play, with the beam energy are required to find the optimal depth.

Two primary methods were utilized for the EBIRCh measurements, either applying a constant voltage across the defect and measuring variations in current at the amplifier (**Figure 3**), or applying a constant current through the defect and measuring variations in the voltage across at the amplifier (**Figure 4**). In both cases a current amplifier was used. The current amplifier was AC coupled to the circuit when utilizing the current source.

Typically, the resistance of the faulty junction responsible for shorting the two conductors is unknown; therefore initial nanoprobing to electrically characterize the faulty junction can aid in determining the appropriate voltage to be applied to the circuit for the best EBIRCh signal. As the beam interacts with the defect it varies its resistance, which is measured as variations in the current at the amplifier. The primary difficulty with the constant voltage setup is it requires manual adjustment of the bias across the defect to keep the current within a viable range as not to blow the short.

Although it is more difficult to setup and requires additional hardware the constant current approach benefits from a built in feedback loop that keeps the current running through the defect constant and within safe levels (**Figure 4**). As the resistance of the defect varies, the current supply will vary the voltage on its end to keep the current constant. These variations in the potential are measured as current at the amplifier through an AC coupled wire.

Electron beam induced resistance change system results

A state-of-the-art Intel test vehicle was used to test EBIRCh. The first test, **Figure 5a**, is an unknown sub-surface back end defect consisting of two large shorting power and ground nets with a resistance of $40\text{k}\Omega$. After preparation the sample was loaded into a DCG Systems nanoProber and an EBIRCh scan was performed on the test site covering approximately a $100\mu\text{m}^2$ area. Due to the relative weakness of the EBIRCh signal, multiple integrative scans were performed, post-processed and overlaid

with the SEM image, producing **Figure 5a** and isolating the defect to a $<100\text{nm}^2$ area. After de-processing the location of the short was verified in a SEM (**Figure 5b**) and sent for further analysis. The second defect is a diodic front end short with a resistance of $3\text{M}\Omega$ when measured at a constant potential difference of 0.1V . The green and red overlays in **Figure 6** represent the maximum and minimum amplitudes as measured from the output of the amplifier, producing a dipole. The defect exists between the lobes of the dipole and was verified in TEM. This dipole behavior is common with diodic defects.

Conclusions

EBIRCh has been successful at isolating different kinds of front end and back end shorts with a resolution of approximately 100nm^2 . Due to its ease of use, direct defect visualization, and similarity to already existing techniques the effect of EBIRCh on the field of nanotechnology failure analysis will likely be on the order of EBAC and electron beam induced current (EBIC) [2,3]. EBIRCh is expected to significantly improve throughput and resolution on a variety of defect types compared to conventional fault isolation techniques.

Acknowledgments

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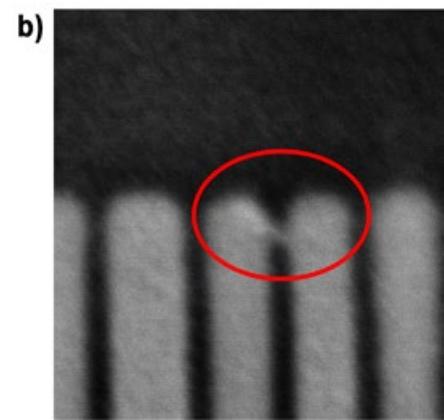
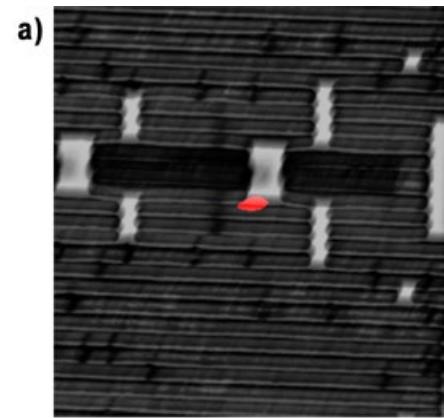


Figure 5: a) Red overlay is the post-processed EBIRCh image; greyscale is the SEM image; blurriness is due to long integrative exposure; and b) SEM image of defect isolated in Figure 5a after de-processing to lower layer.

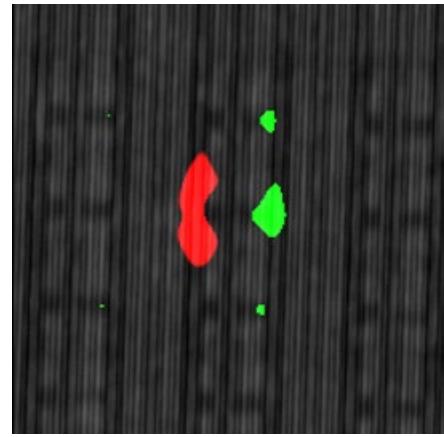


Figure 6: Green and red overlays represent the maximum and minimum peaks from the post-processed EBIRCh image producing a dipole; greyscale is the SEM image. Defect verified in TEM.

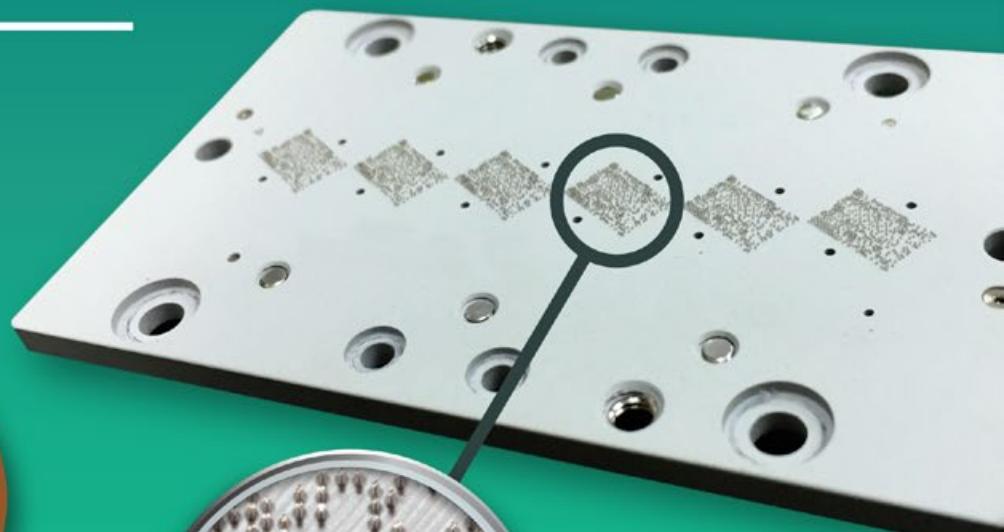
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Temporary wafer carrier solutions for thin FOWLP and eWLB-based PoP

By José Campos, André Cardoso, Steffen Kröhnert [NANIUM S.A.], Jürgen Burggraf, Harald Wiesbauer, Thomas Uhrmann [EV Group]

Semiconductor packaging technology has undergone tremendous innovation over the years. The most visible example is the widespread adoption of wafer-level packaging, which has mainly been driven by the mobile market. One form of fan-out wafer-level packaging (FOWLP) technology – embedded wafer-level ball grid array (eWLB) – has gained particular interest as components designers see in it a solution to their need for small form factor, low-power consumption and enhanced I/O capabilities.

Initially, FOWLP used simple designs with single dies, single RDL layers on a single wafer side, relaxed Si areas, thick wafers and thick package profiles. Today's common designs include multi-die packages with discrete passive devices on a system-in-package (SiP) at the wafer level, multi-RDL layers on one or both sides of the wafer, more demanding levels of Si area, and significant reductions in wafer thicknesses and package profiles.

To be cost competitive with other packaging technologies, FOWLP has used 300mm reconstituted wafers, which create challenges such as wafer bow, wafer warpage and wafer expansion. Today, more FOWLP designs require reconstituted wafers with thicknesses below 400 μm , which does not allow for self-supporting handling. In addition to static wafer bow and warpage, characteristics such as stiffness and shape change with thermal processing become more relevant. As a result, established wafer handling technologies implemented on most WLP equipment can no longer cope with the behavior of these wafers. Adding to this challenge, the need for RDL processing on both sides of the eWLB wafer for 3D and package-on-package (PoP) constructions requires

temporary protection of one RDL side while the other is being built.

The challenges of thin-wafer handling and back/front-side protection are known in the monolithic wafer world and solved with well-developed temporary wafer-carrier bonding solutions. These solutions, however, cannot be copied-exact to heterogeneous eWLB wafers on account of their very high and nonlinear thermomechanical behavior, and also on account of the temperature limitations imposed by the molded material.

This article presents results of temporary bonding for FOWLP 300mm reconstituted wafers. It includes development and testing of different process options, adhesive families, and carrier materials. The integration of these options and materials with the downward FOWLP processes was also evaluated.

FOWLP process

FOWLP technology uses a wafer reconstruction process, where known-good-dies (KGDs) and other types of devices, packages or components are placed side-by-side and embedded with epoxy mold compound. This is followed by thin-film processing, re-passivation and metallization on one or both sides of the reconstituted wafer to fan-out interconnections from original die pads to external pad locations. Finally, typical wafer-level bumping, marking and singulation processes are used, as well as wafer probing.

Challenges. Warpage of reconstituted wafers has been one of the main challenges of FOWLP technology since its initial introduction into high-volume manufacturing (HVM), and brings increased wafer handling difficulties and lower process windows. To address and mitigate this

situation, several boundary conditions must be considered. For example, the reconstituted wafer is composed of materials with different coefficients of thermal expansion (CTEs) (e.g., Si has a CTE of 2.5~3ppm/ $^{\circ}\text{C}$ while a typical epoxy mold compound has a CTE of 7~8ppm/ $^{\circ}\text{C}$), so the wafer will have an intermediate CTE depending on the Si/mold ratio. In addition, die geometries and distances to neighboring dies are usually defined by customer product and package, either in the horizontal (x , y) or vertical axis (z). For the general case of over-molded packages, the z axis is particularly asymmetric, with both dies and mold compound at the front side, while the back side is mold compound only. This asymmetry, set by die and wafer thickness, is a key contributor to wafer warpage. Above all, the final unit cost must be minimized, which is highly dependent on the total number of dies with which a 300mm reconstituted wafer can be populated.

The effects of these boundary conditions are intensified when the total thickness of the reconstituted wafer is further reduced to enable thinner packages. When the thickness drops below 400~450 μm , the reconstituted wafers acquire a flexible behavior that no longer allows self-supporting handling (Figure 1). Also, reducing the wafer thickness often increases z -axis asymmetry, adding nonlinear behavior to the already flexible wafer.



Figure 1: Flexible behavior of a thin FOWLP wafer.

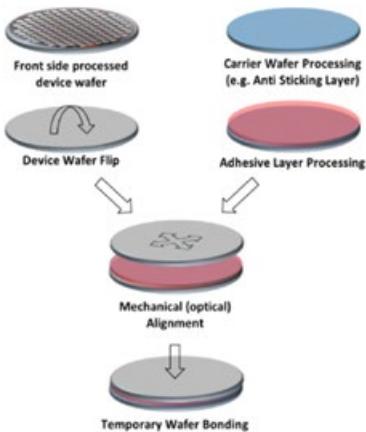


Figure 2: Temporary bonding process flow for multilayer adhesives.

Temporary bonding and debonding

Temporarily attaching the molded reconstituted wafer to a suitable carrier was adopted to overcome the warpage and flexibility by stabilizing the molded wafer and reducing its topography variations. The selection of carrier wafers and its dimensions, as well as adhesive materials, are key elements to a successful temporary bonding and debonding technique. The process is detailed in **Figure 2**.

Prior to bonding, the carrier wafer can be coated with an anti-sticking layer to facilitate debonding. Then, an adhesive is applied on the carrier or through spin-coating or lamination. The nature of the adhesive and its deposition method are crucial to bonding success. As semiconductor processing involves a variety of different chemical, thermal and plasma processes, selecting the right adhesive is essential and very often material properties and functions are contradictory.

Proficiency in temporary bonding and debonding (TB/DB) involves several parameters, the first of which is the initial condition of the wafers. The final bonding quality (i.e., success in attachment and detachment) is dependent on a combination of parameters such as temperature, atmosphere, chemical exposure, and mechanical stress of the post-temporary bonding process, as well as total thickness variation (TTV), presence of particles and voids, bow and warp, and the centricity of the wafers. These characteristics will help define the adhesive and TB/DB process to be used.

Adhesive selection. Polymers are classified into four families: thermoplastic, thermosetting, elastomers and hybrid polymers, which are polymers comprising the other three [1]. Because of their versatility, thermoplastic adhesives are often used in bonding and debonding applications. Their ability to be solidified and re-melted is their key differentiator over thermosetting polymers, whose solidification is irreversible. Thermoplastic residues can be chemically removed after debonding, which reduces contamination for the rest of the process. Operating temperature and required rigidity are the most decisive parameters, as the adhesive layer has to maintain rigidity throughout the process, especially for back-grinding.

TTV after temporary bonding is of central importance to bonding. Any local thickness variation of the temporary adhesive will be transferred to the device wafer. TTV variations mainly stem from spin coating and baking uniformity issues during the application of the adhesive film, and pressure uniformity issues during bonding. Additionally, the adhesive must be compliant with the debonding process, which tends to require room-temperature conditions.

Debonding process. Debonding in HVM is a proven technology. Like bonding, debonding is adapted to the adhesive systems and to some possible parameter restrictions from the device wafers. The debonding process can be classified into two families: thermal debonding (including thermal slide-off and thermal lift-off) and low-temperature debonding (including laser and multi-layer adhesive debonding).

Specificity of FOWLP. The development of bonding processes for FOWLP has been guided by restrictions due to the nature of the mold and to the RDL fabrication process steps. The correlation between increasing mold stress and rising temperature has fostered the adoption of low-temperature adhesives, making thermoplastic adhesives an appropriate solution. Because of the initial warpage of the molded wafer, materials with high adhesion characteristics were

considered to maintain a plain contact between the carrier and the mold, and to prevent delamination. Finally, the RDL fabrication and its chemical environment have also influenced the choice of the adhesive material.

Experimental setup

Experiments were conducted with several material and process options. The main variables under test were: 1) carrier material, 2) carrier thickness and surface quality, and 3) temporary bonding adhesive and thickness.

The initial checkpoint of each run was the warpage measurement on the wafer-carrier set at the beginning of the FOWLP process and the processability assessment. Although a minimum amount of warpage is tolerated, it is the combination of warpage and stiffness that dictates processability (e.g., if a proper latching is achieved on a vacuum chuck).

To assess the ability to withstand the FOWLP process, the steps with higher thermal “aggressiveness” were identified, which included PVD sputtering, dielectric cures, plasma steps (via descum, wafer surface cleaning and leakage descum); and solder reflow. Then, the bonding quality and robustness of each experiment during FOWLP processing was checked in each of those critical steps by: 1) visual inspection for bonding delamination, wafer planarity, process defects, etc.; and 2) Scanning acoustic microscope (SAM) to check internal bonding condition, internal voids and delaminated areas, and total warpage.

Carrier material and thickness. The requirements for the carrier are mainly: 1) thermal compatibility to the FOWLP device wafer to minimize stress upon their interface (CTE) [2]; 2) mechanical properties such

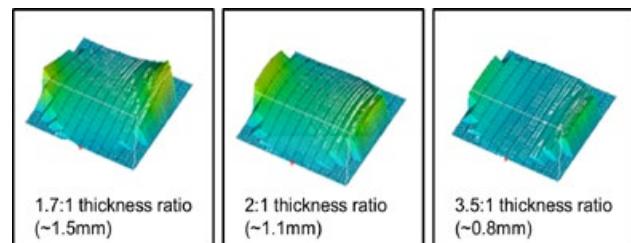


Figure 3: The carrier-wafer thickness ratio affects FOWLP warpage results.



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as high strength and stiffness to ensure sound support and to enforce flatness to the set wafer-carrier; and 3) chemical stability in harsh chemical environments imposed by the FOWLP process such as etching and electroplating [3].

Carrier thickness also impacts the warpage of the bonded FOWLP wafer, as shown in **Figure 3**. Ideally, the carrier should be significantly thicker than the FOWLP wafer. However, process and equipment limitations impose a maximum overall thickness of <1mm. The carrier/wafer thickness ratio spanned from 2:1 to 3.5:1. Several carrier materials with different CTE ranges, elasticity, and thickness were evaluated (**Table 1**), including typical carrier materials like Si and glass as well as others.

Temporary bonding adhesive materials. As referred above, there are different types of adhesive materials potentially suitable for temporary bonding of FOWLP. During this development, different materials were tested that demonstrated significantly different behavior during processing (**Table 2**).

Experimental results

On account of their coefficient of thermal expansion (CTE) mismatch to FOWLP wafers, Si carriers failed immediately at the first curing cycle, showing delamination at the wafer edges. The internal high stress due to this mismatch was also indirectly seen in the inability to latch the wafers on process chucks on account of high stiffness. Although glass carriers have better CTE matching, they failed at the first plasma step and also exhibited localized and distributed delaminations coincident to the Si die locations of the product wafer. Knowing those locations behave as hotspots when the wafer is heated from the top (Si conducts heat much better), a hypothesis for this behavior is the poor thermal conductivity of the glass, transferring those thermal asymmetries to the adhesive.

Carrier type C, which has a higher CTE than Si, but still below mold compound, showed mixed results. In general, the bonding adhesive could not withstand the high thermal stresses induced during plasma and sputtering steps. This was noticed during visual

inspection where the reconstituted wafers started delaminating on the edges from the temporary carrier, and during SAM inspection where internal delaminated areas were visible (**Figure 4**). The extreme warpage of the bonded stack also did not allow for handling or processing (**Figure 5**). In the worst cases, the warpage was already critical immediately after temporary bonding. The best results with carrier type C were achieved with adhesive A and a 1.7:1 thickness ratio.

Successful combination. Following the reasoning that increasing the carriers' CTE reduces induced stress, the type D carrier was identified and tested. This one exhibited a much higher Young's modulus and better thermal conductivity than glass. Further design-of-experiments (DoEs) showed good bonding quality among all processes when using adhesive material D. This configuration enabled a robust, stable FOWLP process condition with no abnormalities identified during visual inspection or SAM, and a very low warpage, as illustrated in **Figure 6**.

Summary

Temporary bonding of 300mm FOWLP wafers was successfully developed based on a set of experiments where different parameters were tested, including carrier materials and thicknesses, adhesive materials and temporary bonding process conditions. The results showed the significant impact that both adhesives and carrier properties have on the bonding quality and on the ability to withstand the very aggressive FOWLP process. Based on the different results obtained during multiple experiments, typical carrier materials were shown to be inadequate and new carrier materials, together with the most suitable temporary

Mechanical Properties	Carrier Material			
	A - Glass	B - Si	C	D
CTE (ppm/ $^{\circ}$ C)	7.8	2.6	~6	>8.0
Young's Modulus (GPa)	74	130	~30	>300
Carrier Thickness Range (um)	700	600-700	570-700	550

Table 1: Mechanical properties of carrier materials used in the experiments.

Temporary Bonding Adhesive	Thickness (μ m)	Bonding Temperature
A	20~25	150-200 $^{\circ}$ C
B	20~25	150-200 $^{\circ}$ C
C	20~25	150-200 $^{\circ}$ C
D	20~25	150-200 $^{\circ}$ C
S - Silicone Based	30, 90	150 $^{\circ}$ C

Table 2: Temporary bonding adhesive materials used during the experiments.

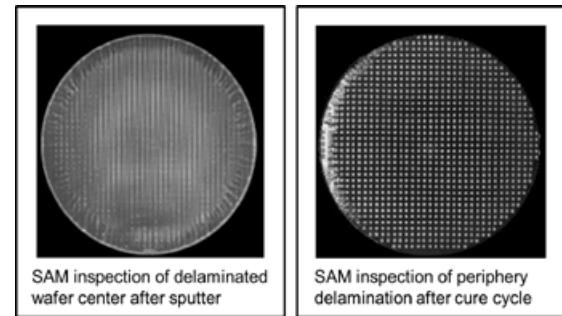


Figure 4: Delaminated areas after critical process steps (carrier type C).

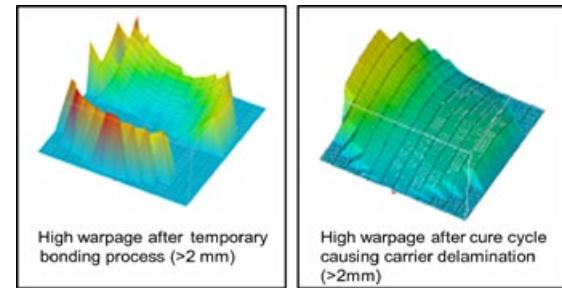


Figure 5: High wafer warpage after a temporary bonding process and during the FOWLP process (carrier type C).

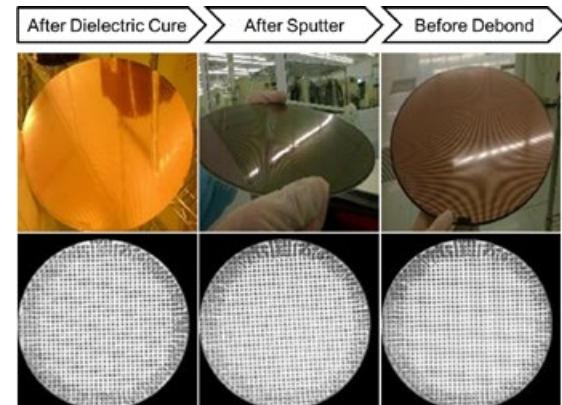


Figure 6: Visual inspection and SAM results on carrier type D and adhesive type D indicate good bonding quality after FOWLP processing.

bonding adhesive and process conditions, demonstrated the existence of an optimal solution. After a careful selection, the best combination of such parameters enabled a robust temporary bonding solution for FOWLP. No visual or internal abnormality was seen on the optimized configuration, and minimum wafer warpage was measured during critical FOWLP process steps.

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Warped wafers “flattened” acoustically

By Steven R. Martell [Sonoscan, Inc.], and Tom Adams [consultant to Sonoscan, Inc.]

As they move through production from front to mid-end processes, warped wafers of silicon and other materials may cause significant problems because of their non-planar contours. A warped wafer is difficult to etch and to dice. It is also difficult to probe a warped wafer because the probe needles may break. Two wafers may not bond well because warping creates two or more points of contact during the direct bonding process. Warped wafers compound the issues with mid-end processes, such as 3D ICs, where chips on a wafer may already have interconnect coplanarity and underfill support integrity issues. Until now, warped wafers have been difficult to image acoustically because some regions of such a wafer are likely to be out of focus.

An example of a reasonably flat 300mm wafer is shown in **Figure 1**. In this case, there is only a 63.5 μm height variation (H) from the lowest point (bright green) to the highest point (dark blue). A flat wafer like this is easy to image with conventional acoustic micro imaging (AMI) technologies. Unfortunately today, many wafers have more significant

warping, and ultrasonic focus cannot be maintained as a wafer is scanned. That was the motivation to develop new technology.

To make it possible to image warped wafers with its automated inspection systems, we have developed a contour following technology that permits the transducer to change its altitude, i.e., Z height, as it scans at its normal speed, which can exceed 1m/s. The transducer precisely tracks all local height variations in the surface of the wafer. Throughout the scanning process, the depth of interest remains in focus and within the gate(s) selected per the scan recipe. The result is an acoustic image and acoustic data that represent the wafer as though it were perfectly flat.

Contour following technology prevents these situations: 1) Damage to the wafer, because the transducer maintains a constant distance from the wafer surface and will not come in contact with high spots; and 2) Missing any features of interest that may go undetected because they are out of focus (gap-type defects such as non-bonds, voids and delaminations, as well as other structural defects) by adjusting the transducer height

on the fly and maintaining the proper imaging gate(s).

The use of automated Contour Surface Acoustic Microscopy (C-SAM®) tools has expanded to include unpolished and fully processed wafers, solar cells (i.e., PERC), MEMS, 3D ICs, sensors, LEDs, lab-on-chip and chip-on-wafer applications. The materials involved include silicon, glass, GaAs, sapphire, and combinations of materials. These materials and applications use many forms of bonding or deposition processes to create layering of materials where the integrity of the structure is important. In addition, unpolished raw wafers can be imaged in order to identify natural flaws that have the potential to become “pinholes” when the wafer is processed further.

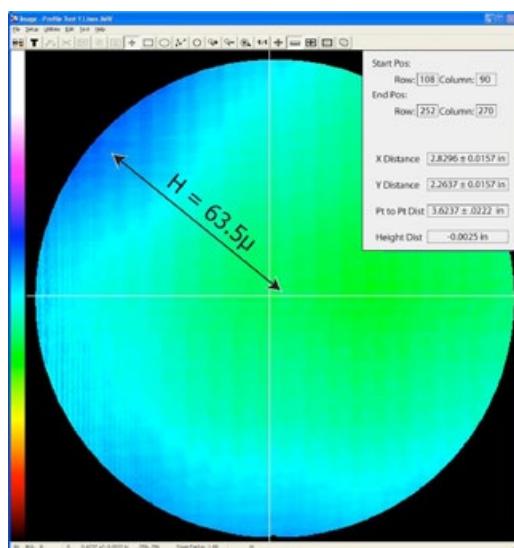


Figure 1: The maximum height difference on this 300mm wafer is 63.5 μm . Colors represent distance from transducer to surface: this wafer is relatively flat.

Background

Acoustic micro imaging (AMI) tools are widely employed to locate and image structural anomalies in a variety of materials and products. The most frequent structural anomalies are cracks, voids, non-bonds, and other gap-type features, but the environments in which they occur are varied. A non-bond, for example, might occur in the solder bumps joining a chip to a wafer, or along the seal around the cavity in a MEMS device.

Conventionally, the ultrasonic transducer of an AMI tool, such as Sonoscan's C-SAM systems, scans back and forth above the surface of the wafer in a flat plane. The transducer is coupled to the surface by an accompanying column of water, needed because the ultrasound at the frequencies typically used does not travel through air. Ultrasound pulsed by the transducer is focused at a depth of interest on or within the wafer structure – the depth where a chip is bonded to the wafer, for example. Echoes from the depth of interest are electronically gated; i.e., they are the only echoes accepted for use as data points for the pixels in the acoustic image. Echoes from other depths are ignored.

A conventional C-SAM tool is good for looking at fairly flat wafers. In the example shown in **Figure 2**, an attempt was made to bond two warped wafers. In this case, the warped wafers touched at two points, causing

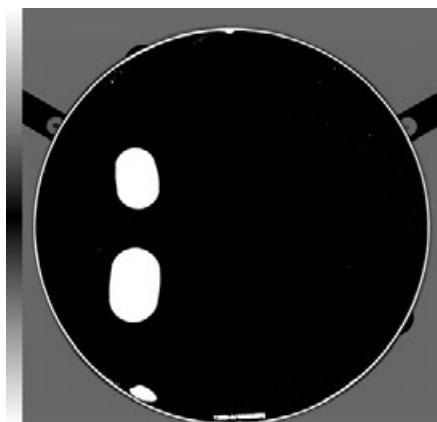


Figure 2: Bonding these two warped wafers resulted in large voids.

voids (white areas) to be entrapped between the wafer pair along the bond fronts. The wafers are currently fairly flat, but the quality of the bond was poor. This is clearly a black (good bond) and white (no bond) situation.

All material interfaces within a wafer assembly structure reflect and transmit some percentage of the arriving ultrasound, depending on the acoustic properties of the materials. A pulse of ultrasound meeting a non-bond, crack or other gap-type defect encounters the interface between a solid material and air. Nearly all of the ultrasound is reflected by the gap and none reaches the far side of an air gap.

The distance that the conventionally controlled transducer is elevated above the part's surface is unchanging (a flat plane) throughout the scanning process, during which echoes from thousands of x-y locations are collected each second. As long as the wafer is flat, or very close to flat, the gated echoes will all be from the depth of interest, and they will all be within the focal depth zone of the transducer, i.e., in focus.

If the wafer is warped, however, some regions of the wafer may lie partly or entirely above the depth of interest, as shown in **Figure 3**, where the contour of the warped wafer has been exaggerated. On a conventional AMI tool, those regions that lie outside the depth of interest, and the features in them, will be imaged ambiguously, or not at all, depending on their actual distance from the transducer. How far out of focus might a depth of interest be? A 300mm wafer structure might be 750 μ m thick. The greatest peak-to-valley elevation

distance yet noted on badly warped 300mm wafers is nearly +/-3mm – around four times the thickness of the wafer itself. The gated depth could be far smaller. It might be as narrow as 50 μ m, or even 20 μ m – values far lower than the depth of interest shown in the diagram in **Figure 3**.

In addition, wafer warpage is typically not limited to a single curved contour, which would be much easier to track. The worst case scenario is a warped “potato chip” shaped wafer, with contour changes in all planes and directions.

How wafers become warped

There are at least three origins for warping in wafers. First, some wafers have large diameters, typically 300mm, but are extremely thin. The silicon or other material is not strong enough to support its own weight. Even without the stresses of handling, these wafers can become warped, typically a bow that looks like the shape of a saddle.

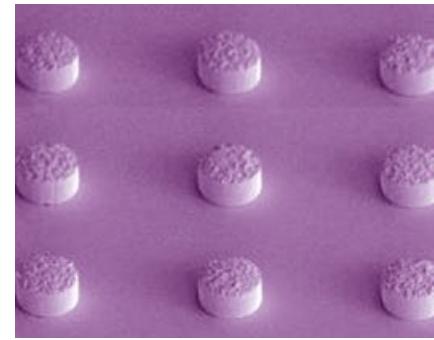
Second, warping can be a consequence of stresses applied to the wafer cut from the crystal ingot or other mechanical processes. The stresses might also be the result of the level of doping, a deposition material/process, or nonuniform heating.

Third, warping can follow localized process of bonding chips or other materials to a wafer. The bonding process and thermal mismatch of materials can set up stresses that lead to warping.

What contour following does

Simply put, contour following does exactly what its name says: it follows the surface contour of the wafer. It puts the transducer at the proper height at each X-Y position of the wafer to image it at the proper depth of interest.

With contour following capability added to a C-SAM tool, the transducer height is continuously adjusted to put the depth of interest in focus and within the gate selected by the recipe (**Figure 4**). The features within each wafer or device will be imaged with the same recipe—only the transducer height is changed as needed. Homogeneous materials (i.e., an unprocessed silicon wafer, or the void-less bulk solder of a solder bump) themselves return no echoes because they contain no material interfaces.



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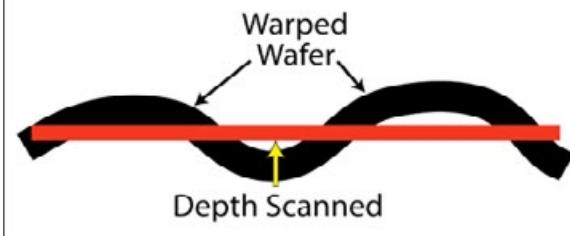
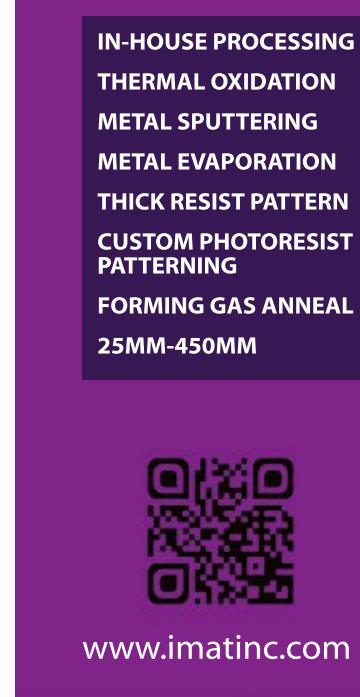


Figure 3: In a warped wafer, some regions may lie outside the focused depth of interest.

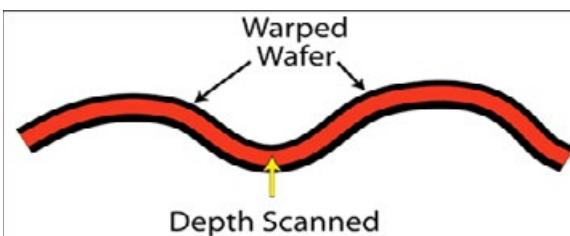


Figure 4: Contour following technology scans a warped wafer as though it were flat to keep all regions in focus.

Well-bonded material interfaces will send back medium-strength echo signals—roughly 20% to 80% of the ultrasound striking the interface. Any gap-type defect (a non-bond, crack, void, etc.) reflects virtually all of the ultrasound. In acoustic images, typically well-bonded interfaces are some shade of gray, while gaps are bright white.

The user of the tool can also include detailed accept/reject criteria within the recipe for each wafer type to be scanned. The seal around the cavity in MEMS devices, for example, might be accepted only if it has a continuous seal of a minimum width or contains extremely small voids that could be expected to cause no loss of hermeticity during the expected lifetime of the device. The solder bumps or underfill of a chip-on-wafer would also be acceptable if they meet the percentage void acceptance criteria set with the recipe.

The 300mm wafer in **Figure 5** was imaged in its “as received” state using Sonoscan’s acoustic surface flatness (ASF) module to

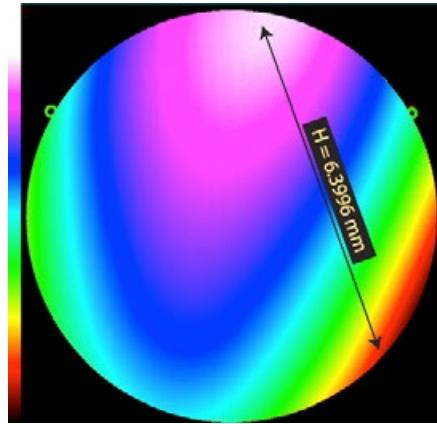


Figure 5: Sonoscan’s acoustic surface flatness (ASF) module is used to demonstrate extreme warping in this 300mm wafer in color.

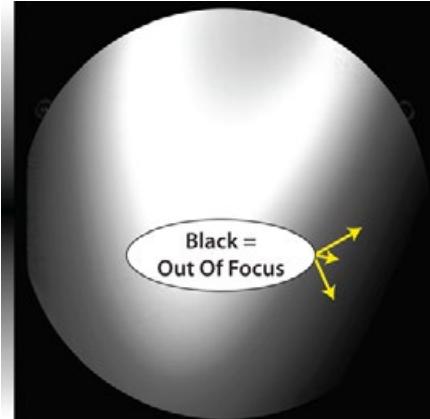


Figure 6: When the wafer in **Figure 5** was imaged with a conventional flat-scanning transducer, some regions (black) vanished because they were outside of both focus and gate.

demonstrate warpage in color. ASF is more typically used on items such as plastic ball grid array (BGA) packages. This wafer exhibits extreme warping. From the high spot (white) to the low spot (red) indicated by the arrow, the height difference (H) is 6.3996mm.

The C-mode image of the same wafer shown in **Figure 6** was obtained using the typical flat scan of an acoustic microscope system. Notice how the surface of the wafer completely disappears (black) at the left and right edges because the surface has dropped out of focus and out of the imaging gate.

The C-mode image shown in **Figure 7** was obtained using a contour following scan. Notice how the surface of the wafer is now uniform with the surface in focus and within the imaging gate.

After the C-SAM system using the contour following has imaged a warped wafer, the acoustic data may be stored locally, in the tool’s memory, or may be transferred to the user’s factory information system. In either case, the wafers and/or devices that do not meet the predetermined accept/reject criteria can be identified and removed from production.

Stacked chip-on-wafer considerations

As suggested earlier, some of the most difficult wafers to image are very thin wafers having large (typically 300mm) diameters. The need to acoustically image these wafers is likely to become more acute because very thin devices, or stacks of very thin devices, are in great demand for hand-held applications. But these are the very wafers most susceptible to warping. Two considerations stand out: First, contour following technology allows the C-SAM tool to identify all of the devices on a wafer that do not meet the user’s requirements. Those devices having voids, non-bonds or other defects can easily be removed from production. Second, contour following technology may offer an advantage in the stacking of very thin devices. Warping is not simply a characteristic of the wafer as a whole, an individual device may also be warped to some degree. If a thin device that is sufficiently warped is stacked with other devices, some area of non-contact is likely. So even if a device passed the user’s basic accept/reject criteria for internal defects, it may be too warped to use.

Can the acoustic data from the contour following identify devices without gap-type defects but with sufficient warping to make stacking impossible? If the user knows the degree of warping that can be tolerated in a

specific application, he/she can also use the acoustic data to exclude those devices having too great a height difference from side to side or from corner to corner.

Contour following with multiple gates

As mentioned previously for single gates, a standard ultrasonic transducer, with its height unchanging during the scan of a flat wafer, can also receive echoes from multiple gates from multiple depths of interest. The contour following can do the same thing when imaging a warped wafer. Suppose the user of the contour following needs to know a) the condition of a chip bonded onto a substrate wafer; and b) the condition of solder bumps bonding a chip to the substrate

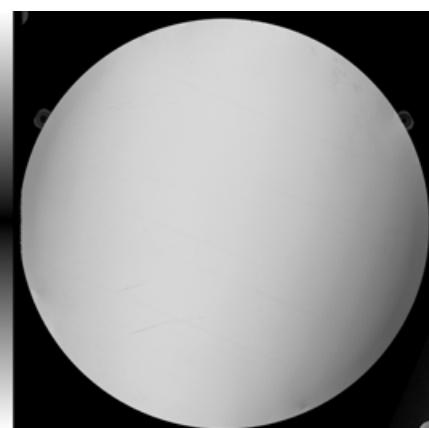


Figure 7: The wafer shown in **Figures 5** and **6** as imaged with contour following.

wafer. The user sets two gates, each of which will receive the return echo signals from one of the depths of interest. At the conclusion of scanning, the result will be two sets of data that will identify all devices having an anomaly in either depth of interest.

Acknowledgment

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Combining defect detection/metrology to accelerate micro-bump/pillar fabrication

By Nicolas Devanciard [CEA-Leti] and Dario Alliata [Rudolph Technologies, Inc.]

The “International Technology Roadmap for Semiconductors” (ITRS2.0) [1] identified the Internet of Things (IoT) as the new driver for the next-generation of smart devices, and three-dimensional (3D) integration technology as a leading candidate for high-volume production of future IoT devices. One of the most challenging process steps in 3D integration is the establishment of reliable interconnections among the stacked chips. Though wire bonding technology is still the most commonly used vertical interconnect solution, through-silicon vias (TSV), copper (Cu) pillars and bumps, or various combinations of these, are likely to become more common and eventually predominate because they can accommodate more input/output (I/O) channels in less area and deliver superior electrical performance [2]. In addition, switching to Cu bumps permits compliance with EU and industry ROHS-6 requirements to eliminate lead. Therefore, there is great interest in developing reliable processes to fabricate fine-pitch, high-density micro-bumps and Cu pillars for stacked chip packages. At this writing, a number of manufacturing challenges have yet to be overcome. Chief among them are coplanarity and single bump/pillar integrity, which can dramatically affect both the physical and mechanical properties of the interconnection, and cross-talk, which can impact the final electrical performance [3].

Developing a new micro-bump process typically requires the use of multiple characterization and control techniques, either inline or offline. This approach is very time consuming and subject to potential errors when trying to correlate information coming from different platforms [4]. To overcome this limitation and to reduce the mean-time-to-discover (MTTD) fabrication

problems, we recently introduced a new characterization approach that tightly integrates automatic visual inspection (AVI) with local 2D and 3D metrology on the same platform; this work also had the objective of accelerating learning to reduce development costs. The essential concept is to intelligently integrate defect detection with metrology by using information from one to direct the activity of the other. This approach was originally introduced to improve the TSV fabrication process [5]. To demonstrate its extension to other applications, we characterized a micro-bump and pillar fabrication process using information from automatic visual inspection to drive the local metrological investigation.

Materials and methods

The inline characterization was performed with the NSX platform from Rudolph Technologies, Inc. that was recently installed at Leti’s 3D/TSV 300mm pilot line and funded by the IRT Nanoelec Program. This integrated inspection/metrology system hosts a monochrome camera for visual inspection and top side critical dimensions (CD), a color camera for review, a white light interferometric point sensor for distance/thickness measurements, and Discover and TrueADC software servers for offline data analysis and automatic defect classification. Reference height

measurements were performed with mechanical profilometry (Tool A) and optical 2D profilometry (Tool B). Their respective accuracies were verified on a certified height sample hosting a trench of $9.96 \pm 0.029\mu\text{m}$. Scanning electron microscope (SEM) images were captured with a FIB-SEM from FEI.

Micro-bumps and complementary pillars were fabricated on 300mm silicon wafers by electroplating either Cu or Cu/Ni metal stacks with SnAg or Au as capping material. The micro-bump metal stack comprises $6\mu\text{m}$ of electroplated Cu capped with SnAg and sitting on a 200nm thick Cu seed layer (**Figure 1**). On this test wafer, the bump/pillar target diameter was $10\mu\text{m}$ and each unit was assembled in arrays at different densities with reticle pitch of $14, 20, 24$ and $40\mu\text{m}$. Micro-bumps were processed for Cu layer removal using a mix of hydrogen peroxide and sulfuric acid diluted in DI water [6].

The characterization was performed before and after wet chemical etching of copper seed. Results of the inspection were used to trigger metrological characterization of test structures only on the area where the test vehicle integrity was validated. There we sampled diameters and heights by using optical CD metrology and white light interferometry, respectively. The wafers were inspected to verify structural integrity

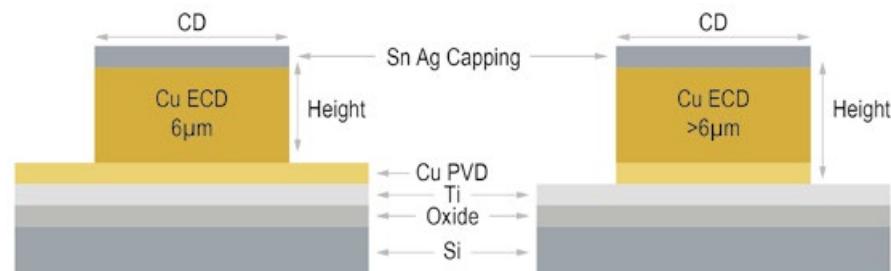


Figure 1: Sketch of the fabricated micro-bump after Cu ECD + resist stripping (left) and post-Cu wet etch (right).

and 2D/3D conformity through the execution of a single process program. The hierarchy of the process program consists of a first inspection pass that looked for missing and defective micro-bumps down to lateral resolution of 2 μm . Defects in each of the four different pitch micro-bump areas were automatically classified with a different code. Following the inspection pass, two metrological scans were automatically executed to measure the diameter and height of four different micro-bumps. Three micro-bumps were located within the array, while one additional micro-bump was chosen in an isolated area, so as to minimize any effect from surrounding micro-bumps. Bump diameter was measured optically at 0.5 μm resolution, based on the gray scale level edge transition method. The height measurement was performed by white light interferometry. The collected results were transferred to a yield management system root cause analysis.

Results

Results can be divided up into two discussions: 1) before etching of the Cu seed layer, and 2) after Cu seed etching.

Before etching Cu seed layer. AVI identified 5,342 defects including a macro scratch across the wafer center (**Figure 2a**), increased diameter (**Figure 2b-d**), missing (**Figure 2e**) and bridged (**Figure 2f**) bumps randomly located over the wafer, and a missing SnAg cap layer (**Figure 2g**).

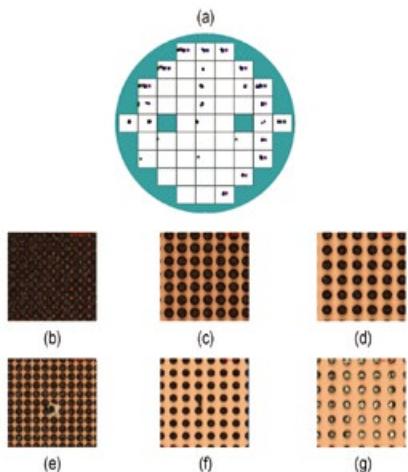


Figure 2: a) Wafer map of total defectivity detected over each bump array area; and b-g) Examples of defects detected by AVI.

When looking at the defect distribution over the wafer as a function of the bump area density, the majority of any detected defects were concentrated in the areas at low bump density (pitch 24 and 40 μm), and close to the wafer edge. The edge defects could be characterized primarily as increased bump width. Even though the number of defective dies is almost the same for pitch 24 and 40 μm , it appears that the number of defects for 40 μm pitch is the lowest. This is consistent with the drop in bump density, where the surface coverage is four times lower than in the 24 μm pitch area. The systematic presence at wafer edge of bumps wider than the target diameter of 10 μm was subsequently confirmed by the lateral CD characterization. **Figure 3** represents the diameter variation over the wafer for the central bump in the 20 μm pitch area. The distribution matches the defect distribution shown in **Figure 4**. The interferometric characterization of bump height revealed a similar behavior. The tallest bumps were measured at wafer edge and mainly located in the areas at lower density (**Figure 5**).

After Cu seed etching. Once the Cu seed was removed by the etching process, the same wafer was re-inspected. The defect count and type remained quite stable, showing a less than 10% drop in the total number of defects detected. Defect count and wafer signature per region also remained stable. We studied the effect of the wet etch process on the bump size by looking at the evolution of the CD average over the whole wafer and the related standard deviation (**Figure 6**).

Analysis

The analysis of the height measurement results revealed taller bumps as a function of increasing pitch and proximity to the wafer edge. This phenomenon is due to two concomitant causes. First, there is a density effect on the electrochemical-deposition (ECD) of copper that is more efficient when there are fewer available growing sites. Second, a non-optimized electroplating process near the wafer edge might favor the chemical reaction by the external anode having a too high current.

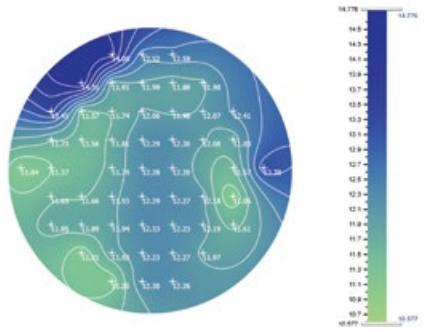


Figure 3: A color contour map representing the micro-bump diameter variation over the wafer (20 μm pitch area/point in center of array).

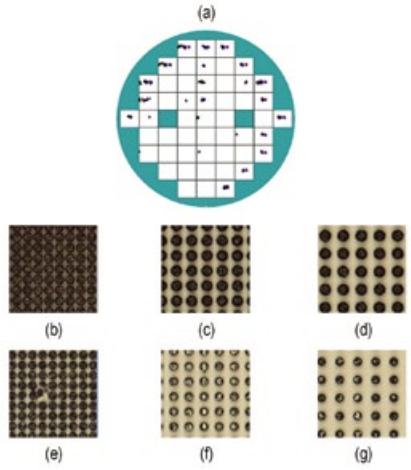


Figure 4: a) A wafer map of defectivity after the Cu removal step; and b-g) Related defect images.

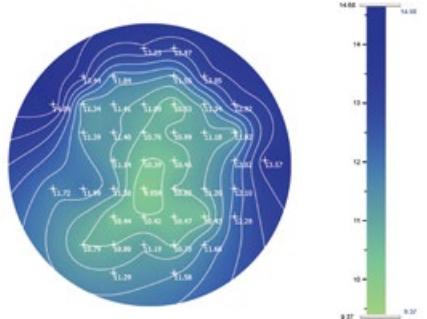
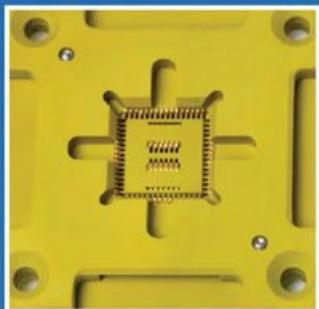
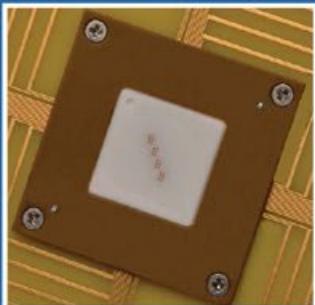


Figure 5: A micro-bump height level representation wafer map for a 20 μm pitch on an isolated point.

After etching, micro-bump height increased about 200nm which is in accordance with the Cu seed layer thickness deposited at the wafer surface, and removed during the process. CD measurements showed similar behavior over the wafer—that is wider micro-bumps for bigger pitches and wafer edge proximity. In this case, the explanation relies on the high proximity of the ECD deposition target and the resist thickness deposited at the wafer surface, which

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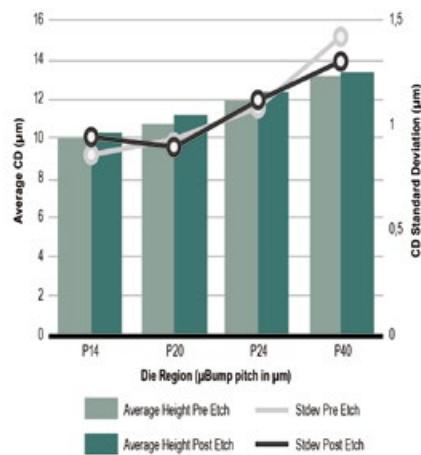
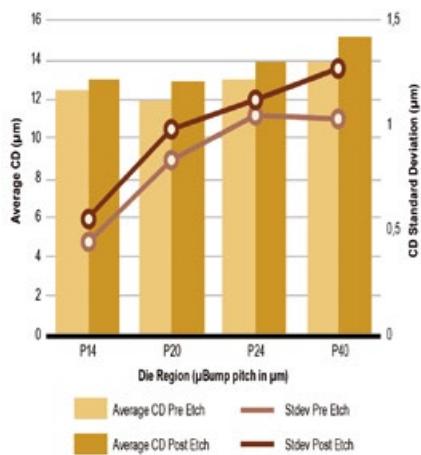


Figure 6: a) (left) Average CD and standard deviation; and b) (right) Average height and standard deviation comparison before and after the wet etch process.

are both at 10 μm , while the ECD target would have been lowered to 8 or 9 μm maximum. Indeed, when the available sites for the ECD are reduced, i.e., for larger pitch, the micro-bump growth goes beyond the resist thickness and continues to grow laterally. This effect is more important at the wafer edge where

ECD reaction is favored. A confirmation of this process effect is found in the FIB-SEM images acquired for micro-bumps in the central die at each pitch (**Figure 7**). On this wafer, the excess of SnAg material will be removed during the reflow process that will ensure a good electrical contact after wafer bonding.

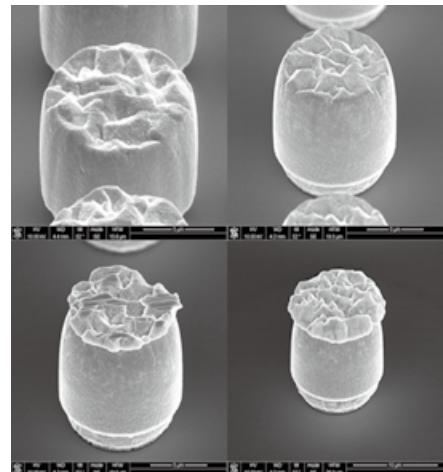


Figure 7: a) (top left) 14 μm pitch; b) (top right) 20 μm pitch; c) (bottom left) 24 μm pitch; and d) (bottom right) 40 μm pitch.

Summary

We successfully demonstrated the potential advantage when running on the same system a defectivity inspection pass that automatically triggers additional metrological passes that are executed in cascade as a function of the defect count limit. As an alternative approach, the process program could be set up to input the sequence of good die or failed die (based on AVI criteria) to be examined in the following metrological passes, so that only die of interest are controlled in micro-bump diameter and height.

Ultimately, the approach that would guarantee the best compromise between the quality of the process characterization and the minimum throughput penalty would be to use information from defect inspection to feed forward smart metrology to characterize the morphology of a defect of interest or a defective pattern of interest. A proper balance of inspection and metrology would be expected to reduce development time, which is crucial in the first phase of the introduction of a new product.

Finally, this flow would not only provide important information to determine the best micro-bump diameter versus density compromise on a test wafer as developed in this paper, but would also ensure a quick and reliable data set to validate many other process steps in 3D IC manufacturing.

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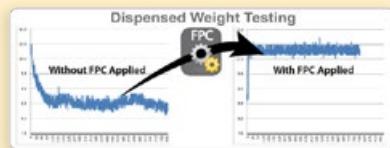
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Recent advances in 3D package reliability

By Craig Hillman [DfR Solutions]

The hard and fast truth is that Moore's law has been dying a slow death for years. When Moore's Law was first released in 1965, transistor count was supposed to double every year. Moore himself modified the law 10 years later, in 1975, to every two years. However, more recent history has indicated that semiconductor performance is not keeping pace. From 2005 to 2012, transistor count has actually been doubling almost every three years (2.8 to be exact [1]), with Intel being the primary driver. And with Intel's last two node size development cycles extended from 2 years to 2.5 years since 2012 [2], Moore's Law is now likely running closer to a doubling every four years.

With this eventual slowing of progress on the silicon side (not to mention the astronomical capital costs) [3], an increasing focus has been on the development of new and innovative packaging to allow semiconductor technology to continue to keep pace with market expectations of performance. The leading approach has primarily been in the area of 3D packaging. But, what is 3D packaging? The term 3D packaging can be more marketing hype than a specific technology or architecture. But to discuss reliability advances, we need to clearly define 3D packaging. In a broad sense, 3D packaging can be defined as: A packaging configuration that consists of more than one plane of active elements. Within this definition, there are four sub-categories of 3D packaging:

Stacked cells/transistors. In this arrangement, the 3D packaging is on a single die. Examples of this technology include 3D NAND Flash being developed by Samsung [4], Toshiba, and Intel/Micron.

Stacked die. This consists of multiple die within a single package and is already common in memory packages, but a new generation is being released that replaces wire bond connections with through-silicon vias (TSV). An extreme example of this 3D package sub-category is Micron's Hybrid Memory Cube.

System-in-package. This sub-category goes beyond simple multi-chip modules (MCM). Instead, envision an encapsulated

device with multiple technologies, including memory, integrated devices, discretes, passives, and magnetics. Some older versions of the Empirion DC-DC converter are excellent examples of this.

Stacked package. For this configuration, two packages with either single or stacked die, are stacked one on top of the other. (Author's note: While there are great images and prototypes of more than two packages stacked on top of each other, commercially, this author is only aware of dual package stacked configurations.)

Separating out each sub-category is critical because reliability is driven by the interaction between materials, geometry, and environment—and each of these sub-categories are different in that regard.

Reliability of stacked cells/transistors

The latest in reliability of stacked cells is better news than often experienced with advances in semiconductor packaging. The major driver for the good news is the increase in feature size that is obtainable with stacked cells. As an example, there are strong indications that the Samsung 3DV-NAND Flash (**Figure 1** [5]) is fabricated at a 40nm process node [6-8], compared to the existing 16nm process node for 2D planar NAND Flash.

The biggest reliability challenges with NAND Flash are the balance between bit density, cell size, and type of cell (single-level (SLC), multi-level (MLC), and triple-level (TLC) [9]). The smaller the cell size and the higher the number of charge levels, the shorter

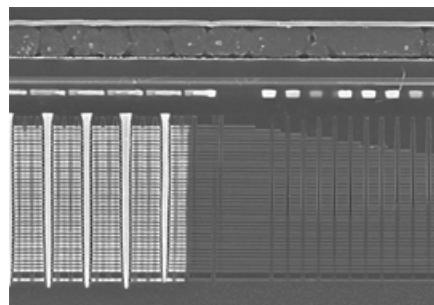


Figure 1: A closer look at the edge of a V-NAND flash array. SOURCE: Chipworks

the lifetime of the NAND Flash and the more prone the cell is to electrical disturbances and single event effects. By allowing larger cell size, through a larger process node, Samsung has been able to extend read/write lifetimes beyond existing 2D planar NAND flash capability. Larger process nodes, as demonstrated by Wyrwas, et al. [10], will also decrease failure-in-time (FIT) rates due to lower stress on the logic aspects of the device (electromigration, dielectric breakdown, hot carrier injection).

It would be nice to make a statement about the reliability of other stacked cell technologies, but they are currently clouded in secrecy, late to market, or both. Toshiba, Hynix, and Intel/Micron are all promising 3D NAND shortly, but have provided little details to determine if, or how, their structure or materials would influence FIT rates or long-term performance. For example, there are indications that the 3D NAND device being proposed by Intel/Micron is using a completely different memory technology (such as resistive RAM).

Reliability of stacked die

If stacking of transistors is not feasible, and this is still the case for semiconductor logic circuits, the next best thing is to stack the silicon itself. The stacking of silicon die is likely the most common category of 3D packaging, with most high-capacity memory devices having two or more stacked dies.

The biggest quality/reliability issue with stacked die is primarily ensuring known good die (KGD). Test coverage can tend to be limited when doing wafer probing. A better understanding of die functionality and defects is often not captured until after packaging. This is why most stacked die packaging comprises no more than four die. The dominant interconnect structure within stacked die is wire bond and will remain wire bond for the foreseeable future as recently shown by Chet Palesko and Jan Vardaman [11]. The reliability challenge for stacked die and wire bonds has been the recent change from gold to copper wire bonds.

Except for corrosion resistance, the material properties of copper wire bonds can be

surprisingly similar to gold. There is a relatively small difference in melt temperature (1085°C vs. 1064°C), so basic diffusion processes would be expected to be about the same (more on this later). Pure copper tends to have a higher yield strength than gold, but this is very dependent on purity levels, anneal temperatures [12] and strain rates [13]. (Author's note: "Tends" is the operative word, as several references have published conflicting values when comparing gold vs. copper wire.) Copper does have a higher modulus (117GPa vs. 74GPa) and a higher coefficient of thermal expansion (17ppm/°C vs. 14ppm/°C), so stresses due to thermal cycling will be higher with copper wire bonds (as much as 2X higher).

While reliability under temperature changes may be compromised, reliability under constant temperature is actually much improved because of the particular behavior of aluminum. Aluminum, which is the bond pad material of choice, has a much higher solubility [14] and diffusion rate [15] in gold than copper. This will greatly extend the time-to-failure (and temperature of failure) for classic wire bond failure mechanisms such as purple plague and Kirkendall voiding.

The greatest risk with copper wire bonds and stacked die, in addition to corrosion/oxidation under humidity and thermal cycling, is preventing defects and damage during manufacturing on account of the narrower process window. For the most part, this expectation has been borne out by published studies on the copper wire bond reliability (**Table 1**). There have been several reported issues with copper wire bond failures in automotive applications that all seem to point back to process or quality control issues [16]. Similar experiences were reported by iNEMI [17].

While the transition to copper wire bonds has been a challenge, the real performance improvement with stacked die (so critical in maintaining Moore's Law) is expected to come with through-silicon vias (TSV). The concept of through-silicon vias has been around almost as long as the integrated circuit, with some of the original proposals patented back in the 1960s [18]. While there is some debate about their first commercial application, until recently, TSVs were limited to silicon-based hermetic packaging (Agilent/Avago's Microcap for film bulk acoustic resonator [FBAR]) and CMOS sensors (Toshiba, Aptina, Sony). One of the challenges in predicting the reliability of TSVs is the broad range of potential processes, materials, and design available. One practical approach is to look

at commercially available technologies using TSVs, such as Microcap and CMOS sensors, and assess their reliability performance.

The original Microcap packaging, patent filed in 1999 [19] and commercially released in 2004 [20], is a die-to-die bonding process used to maintain a hermetic environment around

Leg#	Cumulative Failures during -55/125C Thermal Cycling			
	0 hrs	500 hrs	1000 hrs	1500 hrs
BGA 1 (Au)	3	4	4	4
BGA 2 (Cu)	0	1	1	1
BGA 3 (Cu)	0	0	0	0
BGA 4 (Cu)	0	1	1	1
BGA 5 (Cu)	0	1	1	1
BGA 6 (Cu)	0	2	2	2

Table 1: Cumulative failures of copper wire bonds during thermal cycling between -55°C and +125°C [16,17].

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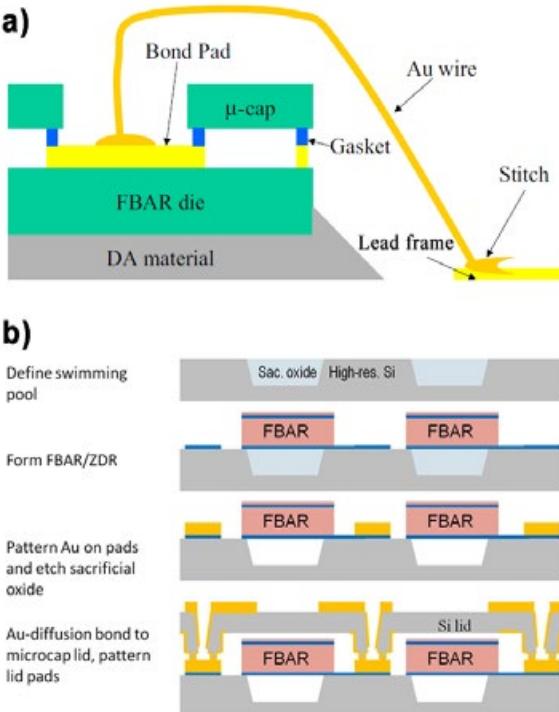


Figure 2: a) The original Microcap package [20], and b) A revised Microcap package that uses TSV architecture [21].

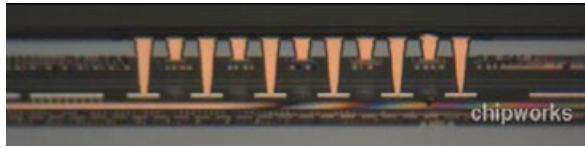


Figure 3: Toshiba's CMOS image sensor using TSVs [23]. SOURCE: Chipworks

FBAR technology. The original design was not a true TSV package as the interconnect was a wire bond connection through a hole in the silicon (**Figure 2a** [21]). However, to ensure a lower profile, the Microcap was then revised with a true TSV architecture (**Figure 2b** [22]). TSVs for CMOS image sensors were first introduced by Toshiba in 2008 (**Figure 3**) [23]. The driver for TSVs was the ability to maximize the pixel area array for the given footprint and it allows for the pixel array and logic circuits to be fabricated with different process nodes.

Do these existing TSV structures demonstrate sufficient reliability for extended life applications? Given the application and design, the field data is likely insufficient. The dominant (think >95%) market for FBAR is cell phones. This is a relatively benign environment (at least from a thermal cycling perspective) and a very short lifetime (2 to 3 years, maximum). Stacked chip image sensors are in a similar situation. For the most part, CMOS image sensors with TSVs are only found in very high-volume manufacturing (think cell phones) [24].

Concerns about TSV reliability in existing

applications is not only driven by the expected use environment, but also by the design. As stated by Caswell [25], TSVs have three primary failure mechanisms: cracking of the plating, cracking of the silicon/change in resistance of silicon, and interfacial delamination of the via wall from silicon (which can result in TSV extrusion). In regards to the Microcap, cracking of the plating is unlikely because the silicon has a lower coefficient of thermal expansion (CTE) than the gold plating. Any increase in temperature, due to hot spots or change in ambient conditions, will place the gold plating under an axial compressive stress. (Author's note: Cold temperatures will place the plating under axial tension and could potentially induce barrel cracking. However, the way most semiconductor manufacturers test their product, -55°C or -40°C to +85°C or 125°C, will NOT induce this failure mechanism. This is because the mean stress under these conditions will be negative, assuming a zero stress state at room temperature, which effectively results in infinite lifetime. Running a thermal cycle test between room temperature to -40°C could result in rapid failure.) The tensile stress then arises circumferentially and could induce cracking along the length of the via, but will not cause electrical failure. Cracking of the silicon is unlikely because the TSV is not filled, which reduces the stress due to differences in CTE.

However, interfacial delamination is very likely. In fact, a recent teardown of a Microcap by System Plus Consulting [26] clearly shows the gold separating from the silicon wall (**Figure 4**, see yellow arrow). The risk of this delamination likely explains the toothed structure of the gold on the cap. This arrangement effectively prevents the interfacial delamination from propagating around the cap and causing a reduction in hermeticity.

The TSV in CMOS image sensors have a very different design than the Microcap. While their TSVs are also likely laser drilled (due to the sloped sidewalls) and plated using electrochemistry (due to the relatively small aspect ratio), the CMOS image sensor TSVs

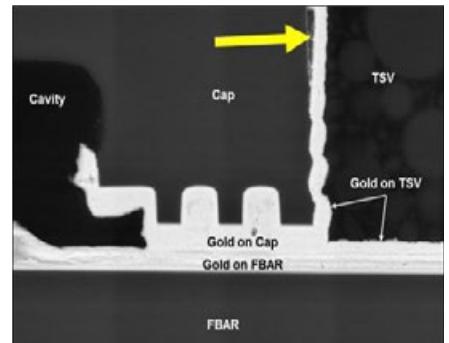


Figure 4: A Microcap tear down analysis view [26].
SOURCE: System Plus Consulting

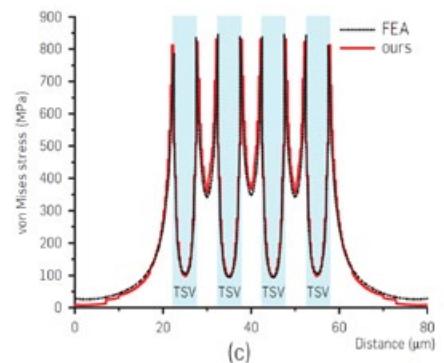


Figure 5: Reported von Mises stress levels in a paper by M. Jung [27].

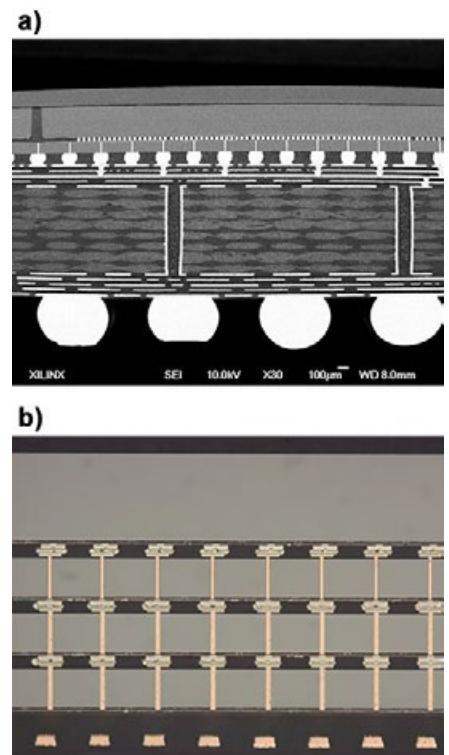


Figure 6: a) A Xilinx Virtex 7 2000T where TSV architecture is used on a silicon interposer; and b) A Samsung DDR4 DRAM DIMM memory with TSVs integrated into the active silicon [31].

observed in tear downs are fully filled. The fully-filled TSVs will effectively eliminate any risk of plating cracks, but does greatly increase the stresses within the silicon. The stresses within the silicon can be approximated using the Lame stress solution for both cylindrical and Cartesian coordinates.

While there is some debate regarding the usefulness of the Lame approximation vs. finite element analysis, both approaches reported by numerous authors have calculated extremely elevated stress levels in the silicon on account of the TSV structure. As an example, a recent paper by Moongon Jung [27] reported von Mises stress levels up to 800MPa in the silicon and in the interface when the TSV structures are spaced approximately 10 μ m apart (**Figure 5**).

Unfortunately, the authors in [27] failed to realize that von Mises stress and the risk of silicon deformation is not the relevant concern. The potential for cracking of the silicon should hopefully be minor, as the device manufacturers would be expected to develop a process that did not induce cracking on a regular basis (and metrology that could pick up any silicon cracking). A more moderate concern is fatigue of silicon. The fracture strength of silicon can be as low as 1GPa and fatigue of silicon has been reported at levels as low as 50% of the fracture strength (**Figure 5**) [28].

However, the greatest risk in regards to TSV is interfacial failure. The stresses, regardless of methodology being used, peak at the interface. The strength and other properties of common interfacial materials (SiO₂ and benzocyclobutene [BCB]) are poorly understood, especially at the length scales relevant to TSVs. And, as with plating cracks, the true reliability of the interface is likely poorly understood by device manufacturers because of their blind reliance on standard thermal cycle testing, which will likely overestimate lifetime because of its tendency to swing stress states from tensile to compressive and back, and potentially lower the mean stress state to levels below those expected in field applications.

Up until now, the uncertainty regarding TSV reliability has not been a concern given the application environment of 99% of devices with TSVs (cell phones). However, two TSV devices with a broader range of applications recently were introduced into the market. Xilinx introduced its Virtex 7 2000T back in 2012, where TSV architecture is used on a silicon interposer (**Figure 6a** [29]). More recently, in November 2015 [30], Samsung introduced a new type of DDR4 DRAM DIMM memory for servers labeled 3DS TSV (**Figure 6b** [31]). (Author's note: This is also an excellent example of the key challenge

for 3D packaging, i.e., price. This new part has 2X the capacity of a similar part, but is 4X the cost.) Unlike the Xilinx part, the TSVs in Samsung's part are integrated into the active silicon.

Not only are the intended use environments different from cell phones (likely enterprise/server), but the fabrication processes are also likely different. The vertical sidewalls suggest an etch process, instead of the laser drill likely with the Microcap and image sensors. Plating the

higher aspect ratio (approximately 5 to 6X) also may require chemical vapor deposition (CVD), instead of the electrochemical processes currently being used. Use of CVD will greatly increase stress states as that process is typically performed at temperatures between 200°C and 400°C (compared to room temperature for electrochemical). However, on the plus side, any temperature cycling will be under a single stress state (and therefore more relevant to extrapolate to field conditions).



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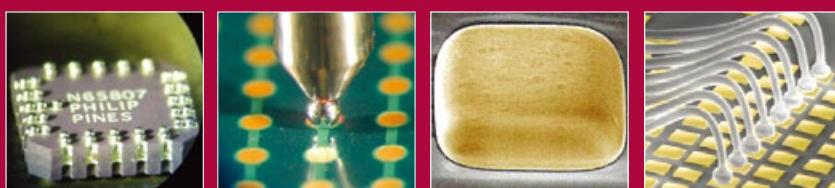
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 Solder Jetting
- Wafer Level RDL (Low
 Volume)
- CSP & BGA Ball Rework

Wafer Backside Metallization

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Reliability of system-in-package

The reliability of a system-in-package (SiP) platform can be very hard to capture (even harder than for TSVs). This is primarily due to the even wider range of potential materials and designs within a SiP. A representative example [32] – an Empirion DC-DC converter – is shown in **Figure 7**. This SiP has wire bonds and semiconductors, but also has ferrite, capacitors, and copper windings.

Because an SiP can effectively be a module or assembly that is miniaturized and encapsulated, all of the standard concerns regarding PCBAs can apply to SiPs. However, one unique aspect of SiPs, and one that is getting harder all the time, is the effect of the encapsulant material.

Traditional encapsulant material used in semiconductor packaging, and by default in SiP packaging, is typically filled epoxy. The fillers are fused silica spheres with typically a bimodal or even trimodal distribution to ensure up to 90% filler content by weight (approximately 82% by volume). (Author's

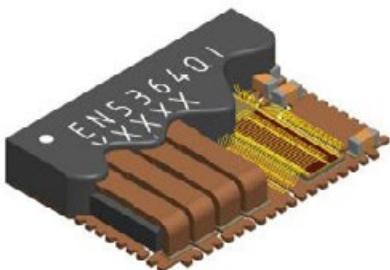


Figure 7: An Empirion DC-DC converter [32].

note: The theory of random close packing (RCP) states that the maximum volume percentage of spheres with similar size is 63.4% [33, 34]. However, a bimodal distribution can theoretically reach 93% by volume if the second distribution is approximately 10X smaller than the first.) This very high level of filler (current molding compounds are pretty much fused silica with an interconnecting network of epoxy) is driven by market demands for low coefficient of thermal expansion (fused silica has a CTE of ~1 ppm/ $^{\circ}$ C) and low levels of moisture sensitivity (MSL 3 or less).

The very high level of filler cited above can cause other issues, especially in regards to rheology of the mold flow and elevated levels of mechanical stresses as the molding compound shrinks and hardens during the curing process. To help compensate, an increasing number of molding compounds manufacturers have started to inject epoxy formulations with lower glass transition temperatures (T_g). These formulations not

only provide some protection from mechanical damage, they can also help balance the other 20+ performance requirements [35]. As seen in **Table 2**, Mold Compound D, with the lowest T_g , has one of the lower flex moduli and hot hardnesses, but also has the lowest conductivity and chlorine levels.

The problem with low T_g molding compounds is the change in material properties as the use or test temperature comes close to or passes through the T_g . The T_g is a critical inflection point because it is an amalgamation of changes to the polymeric structure driven by differences between intramolecular bonding and intermolecular attraction [36]. As the epoxy approaches the T_g , the increase in atomic vibration starts to overcome the secondary bonding forces (i.e., van der Waals) that constrain the polymer chain segments. This results in an increase in the free volume, which drives an increase in CTE. Once the vibration levels reach a critical level, the chains have sufficient energy to undergo significant rotational and translational motion. This results in a significant decrease in modulus. Because lower levels of energy are required to increase free volume compared to increases in movement along the polymer chains, the CTE changes before the modulus (**Figure 8**).

This change in CTE before the change in modulus can result in circumstances where the molding compound greatly expands without any reduction in stiffness, resulting in a significant rise in stress on the internal components that make up the SiP architecture. A simple compatibility of displacements exercise shows that stresses at or close to the T_g can be up to 5X larger than at temperatures on either side of the T_g (**Figure 9**).

This change in material properties can also result in a change in the mode of the stress state. Most reliability models and test plans assume primarily a shear, or Mode II, stress direction. However, these changes in material properties can drive an increase in the tensile, or Mode I, stress direction, which can greatly

Parameters	Mold Compound A	Mold Compound B	Mold Compound C	Mold Compound D	Mold Compound E
Filler content (wt%)	90	87	85	84	82
Spiral Flow (cm)	116	102	110	115	190
Hot Hardness	86	80	84	78	70
T_g ($^{\circ}$ C)	120	125	130	100	120
CTE (ppm/ $^{\circ}$ C)	7	9	11	13	15
Flex Modulus (GPa)	26	24	21	22	21
Conductivity (μ S/cm)	50	60	60	25	60
pH	7.0	6.5	7.3	6.0	7.7
Chlorine (ppm)	15	15	10	8	19

Table 2: Mold compound attributes.

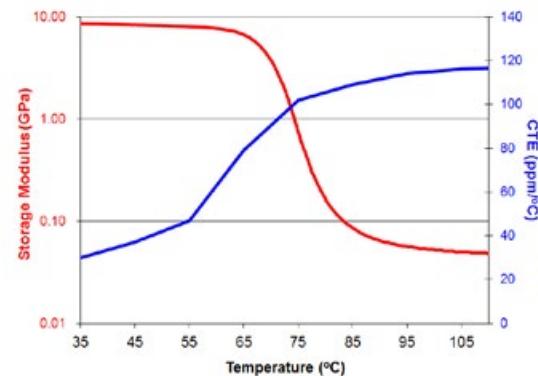


Figure 8: Change in CTE and modulus as a function of temperature for a low T_g epoxy.

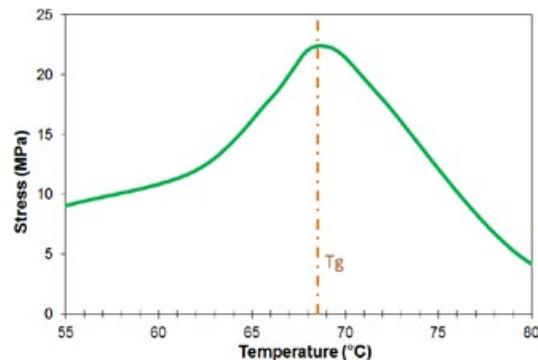


Figure 9: A simple compatibility of displacements exercise.

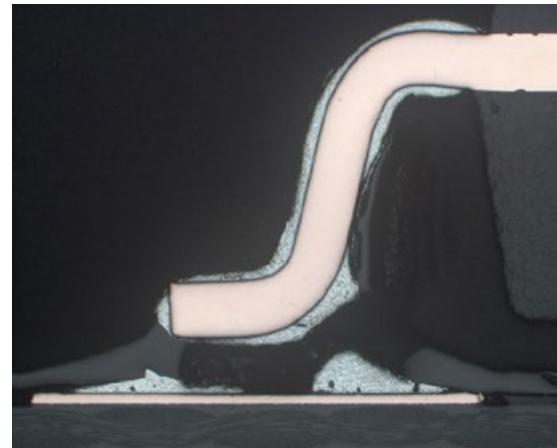


Figure 10: Fracture of components/interconnections are greatly increased with the increase in tensile, or Mode 1 stress.

increase the risk of cracking or fracture of the components or interconnections (wire bond, solder) (**Figure 10**).

The real challenge in regards to SiP reliability is correlating test conditions to actual field usage. Because there is a rapid change in stress and direction, test conditions, just like with TSVs, can induce a mean compressive stress that would extend lifetime almost indefinitely, while field use could have a mean tensile stress that would cause failures rapidly. Selection of the mold compound for SiP packages therefore becomes a critical step in ensuring reliability of 3D packaging.

Summary

The revolution of 3D packaging is exciting and critical for maintaining pace with Moore's Law (even though it has slowed quite substantially). However, success with this new approach to component performance requires meticulous understanding of the thermal and mechanical risks of this new architecture. Both component manufacturers, outsourced semiconductor and test suppliers (OSATs) and OEMs must develop knowledge as to the potential risks of a "test-first" mentality

and over-reliance on qualification activities. Through the judicious use of physics of failure, designers, manufacturers, and users can develop high confidence in 3D packaging of all stripes, and the technology revolution built upon device performance can continue on into the indefinite future.

Biography

Craig Hillman received a BS in Metallurgical Engineering and Material Science and Engineering and Public Policy from Carnegie Mellon, a PhD in Material Science from the U. of California Santa Barbara, and was awarded a post-doctoral fellowship at Cambridge U. in England. He is CEO and Managing Partner of DfR Solutions; email chillman@dfrsolutions.com

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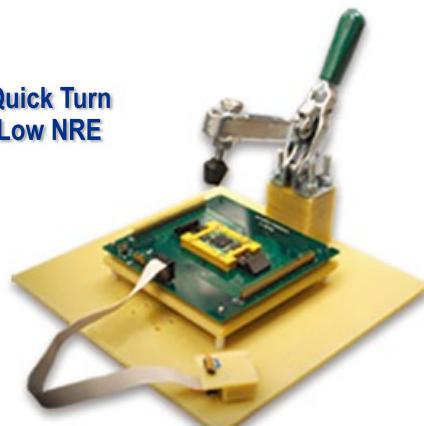
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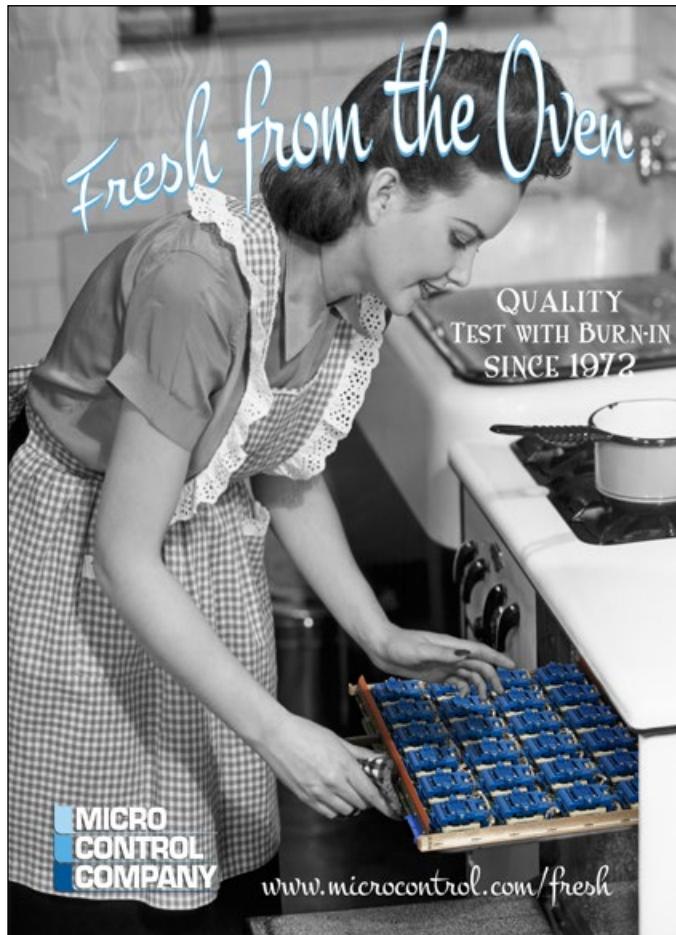


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Heat sinking through socket contact technologies

By Ila Pal *[Ironwood Electronics]*

The classic function of a socket is to provide a connection mechanism from the integrated circuit (IC) to the circuit board with as little electrical load as possible. This allows the IC to function as it is soldered into the PCB (printed circuit board) but can be replaced by another IC to upgrade or test multiple ICs. With the advent of power devices getting into the tens of watts, perhaps even 50-100W, the socket needs to accommodate removal of the heat due to this power, or the IC will self destruct, or worse. For the most part, heat is removed from the top side of the device by adding fins/plates with air circulation. With the introduction of quad flat no-leads (QFN) packages and quad flat packages (QFP) with exposed pads (ePad), heat needs to be removed from the bottom side as well. Power devices are designed such that the center pad acts as both electrical grounding and as a medium for thermal dissipation. When soldered down, heat from the center pad is dissipated via the PCB ground copper plane layer. When placed inside the socket, heat has to pass through the socket contact. This article describes experimental methods to determine heat dissipation through socket contact technologies.

Socket overview

Two of the most common high-frequency contactors for a socket are elastomer and spring pin with bandwidths of >40GHz and <30GHz, respectively. The socket comprises contactors that interconnect QFN pads to the target PCB pads. The socket body has alignment features that precisely place the IC over the contactors and the socket lid has a compression mechanism to apply the down force to compress the QFNs into the contactors. In a high-power application, the compression mechanism needs to perform double duty by also acting as a heat sink that pulls the heat out of the IC. A backing plate on the bottom side of the PCB may be needed to provide the rigidity for the contactors to work

reliably. This need is dependent on the size of the chip, the required flatness, PCB material, and PCB thickness. In addition to the heat dissipation from the top side, there is some amount of heat dissipated through the socket contacts down to the PCB. Depending on the chip design, function, and construction features, heat dissipation through the bottom side via socket contact down to the PCB is very critical. A methodology was developed to measure and understand heat dissipation through the various socket contact technologies.

Modes of heat transfer

Heat transfer can be defined as the transmission of energy from one region to another as a result of a temperature difference. Heat conduction is a property of matter that causes heat energy to flow through the matter. Heat convection is due to the property of moving matter (naturally or under force) that is able to carry heat energy from a higher temperature region to a lower temperature region. Heat radiation is the property of matter such that it is able to emit and absorb different kinds of electromagnetic radiation. Any energy exchange between bodies occurs through one of these modes or a combination of them. We have focused on heat conduction through various socket contact technologies. An experiment was added to compare conduction versus radiation effects in the socket contact heat dissipation process as well.

Thermal resistance

Thermal resistance is the temperature difference, at steady state, between two defined surfaces of a material or construction that induces a unit heat flow rate through a unit area. Thermal resistance is the critical parameter in our experiment and is directly proportional to the thickness of the material, and inversely proportional to the thermal conductivity of the material. In our experiment, thermal resistances of various socket contact technologies

are measured. Thermal resistance can be calculated as shown in **Equation 1**:

$$Tr = (T1 - T2)/P \quad (\text{Eq. 1}) \quad \text{where:}$$

Tr = Thermal resistance of the socket contact in °C/W;

T1 = Top side temperature in °C;

T2 = Bottom side temperature in °C; and

P = Power dissipation in W.

Experimental setup #1

Three different socket contact technologies were considered for this experiment: 1) embedded gold-plated wire inside the elastomer contact (SG), 2) stamped spring pin contact (SBT), and 3) embedded silver ball column inside the elastomer contact (SM).

The SG elastomer comprises a fine-pitch matrix (0.05 x 0.05mm) of gold-plated wires (20µm diameter) that are embedded at a 63° angle in a soft insulating sheet of silicone rubber. The insulation resistance between connections with 500VDC is 1000Mohms—it is ideal for high-current (50mA per filament) applications where a thin, high-density anisotropic connector is required. The gold-plated brass filaments protrude several microns from the top and bottom surfaces of the silicone sheet. The operating temperature range for the SG elastomer is -35 to +100°C. When compressed using the socket mechanism, multiple gold-plated wires from the SG elastomer connect the IC surface pads to the bottom PCB pads.

The SM elastomer is a unique contact that has precise silver balls held together by a proprietary conductive formulation. These conductive columns (diameter optimized for 50 ohm impedance) are suspended in a nonconductive flexible elastomer substrate with a patented solid core for enhanced durability and reliable performance over time, temperature, and cycles. This flexible substrate is compliant and resilient—qualities that enable the conductive columns to revert back to their original shape when the force is removed. When compressed by an external force, silver particles inside the column connect with each other. This creates an

electrical path, which in turn connects the IC surface pads to the bottom PCB pads. The insulation resistance between silver columns with 500VDC is 1000Mohms. The typical contact resistance is 20milliohms per silver column, and the current carrying capacity is 4A.

The SBT contact is a stamped contact with an outside spring, as well as an inside leaf spring that provides a robust solution for low-contact resistance. SBT contact technology has a three part system that includes a top plunger, a bottom plunger, and a spring. The beryllium copper plungers are stamped and assembled to a stainless steel spring that provides optimum force. The insulation resistance between SBT contacts is provided by PEEK plastic. When 500VDC was applied between SBT contacts, a resistance of 1000Mohms was measured. The typical contact resistance is 30milliohms per SBT contact, and the current-carrying capacity is 8A.

The heat source is supplied by an HT15W 1/8"x1/2", 15W heating element rod. The HT15W is a miniature 15W cartridge heater that can be used for many applications requiring small areas to be heated. When voltage is applied between the leads, heat is

generated at the lead exits. The heater element is calibrated by supplying 6V, 12V, 15V, 20V, and 24V. The values of the corresponding wattage generated were documented. After calibration, this heater element is integrated into the top of the compression plate slot inside the socket (**Figure 1**). One thermocouple was installed on top of the socket contact, and the other thermocouple was installed on the bottom of the socket contact. The socket lid is closed and a downward force is applied by turning the central compression screw (see **Figure 2**). The temperature reading in **Figure 2** shows 28°C as there is no heat generated. When voltage is applied to the heater element, heat is generated. The initial applied voltage is 6V and the corresponding power reading is 0.9W. Temperature data is collected after steady state is reached as indicated on both of the thermocouples. Using the formula in **Eq. 1**, the thermal resistance is calculated. Similarly, thermal resistance data is calculated for various power levels by changing the applied voltage. The data is presented graphically in **Figure 2** with the power applied shown on the X-axis, and thermal resistance on the Y-axis. The experiment is then repeated for the other two socket contacts.

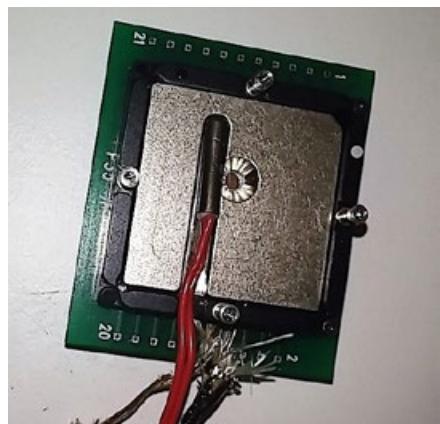


Figure 1: Experimental setup showing the heater element rod integrated into the socket compression plate.

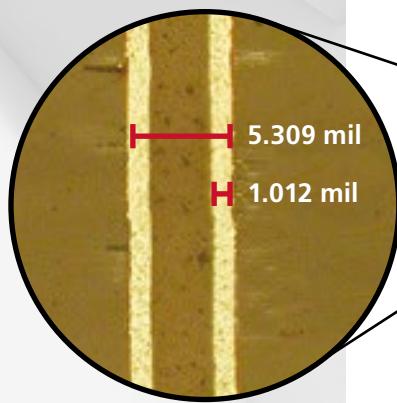
Results and discussions #1

Thermal resistance curves are represented in graphical format for three socket contact technologies in **Figure 3**. It can be seen from the graph that the SG contact (i.e., the blue-colored curve) has low thermal resistance at a low power of 1-4W. Heat passes through the contact with very low resistance. Around 5W, the temperature change is approximately 3°C/W; this means the total temperature rise

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is 15°C for 5W of power. The SG contact maximum operating temperature is 100°C. If the IC's rated power is 5W, then the SG socket maximum operating temperature is reduced to 85°C on account of the thermal resistance phenomenon. Otherwise, the SG contact will be damaged by overheating.

The SM socket curve is shown in red (**Figure 3**) and has a high thermal resistance at low power. The thermal resistance got better at a higher power value, e.g., at 15W. In the SM socket, the thermal conductive

path is through silver particles. With low heat, the temperature difference is 3.5°C for 1W. Heat passes through various small silver particles before it reaches the other end. With high heat, the temperature difference is 2°C/W at a power level of 15W. At higher temperatures, the silver particles expand, which causes the contact between particles to be more efficient. This allows the smooth flow of heat causing a drop in thermal resistance. The SM contact maximum operating temperature is 155°C. At 15W of power, the thermal resistance is 2°C/W, and the temperature rise is 30°C. The SM contact can be operated in an environment up to 125°C when the IC power is 15W.

The SBT socket curve is presented in green in **Figure 3**. It is an almost flat curve showing a thermal resistance between 2.5°C and 2°C. The SBT contact is made of a copper alloy with an external spring. The length of the contact is 2.5mm and it has a rectangular cross section of 0.2x0.6mm. The thermal resistance is inversely proportional to the cross sectional area and directly proportional to the length. Because the SBT contact has a uniform cross sectional area, the change in thermal resistance is very minimal due to the power change between 1W and 15W. The maximum operating temperature of the SBT contact is 180°C. At 15W of power, the thermal resistance is 2°C/W, and the temperature rise is 30°C.

The SBT contact can be operated in an environment of up to 150°C when the IC power is 15W.

Experimental setup #2

Contacts will transfer heat when compressed—this is a conduction phenomenon. When not compressed, there is some heat transferred due to radiation. The SM contact alone was used for this experiment in order to compare heat transfer through conduction vs. through radiation. The experimental setup is the same as the previous one. Two SM sockets were used for this purpose. One SM socket is compressed by applying the recommended torque to the compression screw. The second SM socket is not compressed. The thermal resistance

data was calculated for various values of power by changing the applied voltage for both of the SM sockets. **Figure 4** shows the data is presented graphically with the power applied shown on the X-axis, and the thermal resistance on the Y-axis.

Results and discussions #2

In **Figure 4**, it can be seen from the graph that the two curves are very similar with an offset in thermal resistance values. The compressed SM socket shows a thermal resistance from 3.5-2°C. The SM socket (not compressed) shows a thermal resistance from 5.5 to 3.5°C, which is an indication of the amount of heat transferred through radiation. Heat transfer caused by emission of electromagnetic waves is known as thermal radiation. Heat transfer through radiation takes place in the form of electromagnetic waves - mainly in the infrared region.

Summary

Thermal management of a QFN socket is an all-inclusive method involving the material selection, design, analysis, optimization and verification of a cooling system both on the top side via a heat sink and an axial flow fan, and on the bottom side via a socket contact technology for the purpose of producing a reliable socket for testing high-power devices. In the above discussion, heat dissipation through various socket contact technologies were compared over a range of power dissipation values. Also, the heat dissipation of various socket contact technologies is compared with conduction and radiation phenomena. For high power, SM and SBT contacts provide better heat dissipation through the PCB side. For low power, the SG contact has the lowest thermal resistance. The socket selection process typically involves parameters, such as electrical bandwidth, contact resistance, current capacity, temperature range, etc. Based on the above discussion, the thermal resistance of the socket contact plays a significant role when considering contact selection.

Acknowledgement

The author thanks Vinayak Panavala for his support in experimental preparation, setup and data collection.

Biography

Mr. Ila Pal received his MS degree in Mechanical Engineering from Iowa State U., and an MBA degree from the U. of St. Thomas; he is COO at Ironwood Electronics Inc., USA; email ila@ironwoodelectronics.com



Figure 2: Experimental setup showing the compressed socket with heater element rod connected to a power supply and a thermocouple connected to a multimeter.

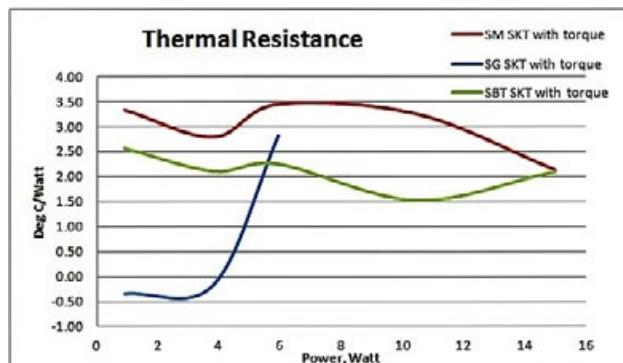


Figure 3: Comparison of thermal resistance for three different socket contact technologies.

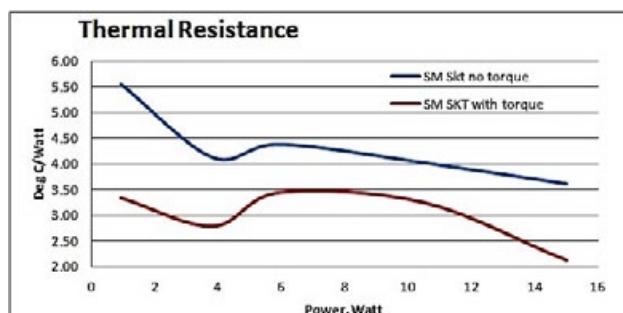


Figure 4: Comparison of conduction versus radiation phenomena when heat is dissipated through socket contact technology.

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Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to + 260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to + 125°C FQ < 30 GHz CF & CR = CM
Andon Electronics Corporation 4 Court Drive Lincoln, RI 02865 Tel: +1-401-333-0388 www.andonselect.com	P	BA, LA, SM, TH	CP > 1.0 mm CL & FQ = CM CT = -65°C to 240°C CR < 1.0 A
AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 130 Ledge Road Seabrook, NH 03874 Tel: +1.603.474.1760 Fax: +1.603.474.1765 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
Aries Electronics, Inc. 2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (100k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to +155°C CL, FQ, CF & CR = CM
BeCe Pte. Ltd. Blk 5000, #03-09 Ang Mo Kio Ave 5. Singapore 569870 Tel: +(65) 6853 1065 Fax: +(65) 6853 www.bece.com.sg	T	BA, LA, SM	CP = CM CL = CM OT = CM FQ = CM CF = CM CR = CM
Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
C2WIDE Co.,Ltd Rm705,84,GaSanDigital 1Ro, GeumCheonGu Seoul, Korea(153797) Tel: +822-364-1878 www.c2wide.com	B, D, P, T	BA, LA	CP = 0.4/0.5/.065/0.8/1.0 mm CL = 300,000 OT = -55° to 130°C FQ > -0.63dB@20GHz CF = 25~35g CR = 3A Continous
Cascade Microtech, Inc. 9100 SW Gemini Drive Beaverton, Oregon 97008, USA Tel: 1-503-601-1000 Fax: 1-503-601-1002 www.cascademicrotech.com	D, P, T	BA, LA, SM	P > (0.35 - 0.8) mm CL > (50 - 300,000)x OT = -45° to 175°C FQ < (9.4 - 40.0) GHz CF < (15 - 55) g CR < (1.0 - 4.0) A

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C.C.P. Contact Probes. 5F, No. 8, Lane 24, Ho Ping Rd., Panchiao District, New Taipei City 220, Taiwan R.O.C. Tel +886-2-29612525 www.pccp.com.tw	B, D, P, T	BA, LA, SM	CP > 0.2 mm CL > 500k OT = -50~170 FQ = > 10 GHz CF = 15~45 grams CR = > 3A
Centipede Systems Inc. 2906 Scott Boulevard Santa Clara, CA 95054 408.321.8201 phone 669-342-7812 fax www.centipedesystems.com	T	BA, LA, SM	CP > 0.3 mm CL > 500,000x OT < + 160°C FQ = CM CF = CM CR < 2.0 A @ 150°C
Cohu Inc. 12367 Crosthwaite Circle Poway, CA 92064 USA Tel: 1-858-848-8000 www.cohu.com	 D, P, T	BA, BD, LA, SM, TH	CP = Contact Pitch > 0.35mm CL = up to 1 Million OT = Temprange -60°C - 175°C FQ = Frequency = < 24GHz CF = Contact Force 20 - 40 gram Current rating / pn = < 3A
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com	B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1 - 34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A
Custom Interconnects, LLC 7790 E. Arapahoe Rd, Suite 250 Centennial, CO 80112 Phone: 303.934.6600 Fax: 303.934.6606 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz @ -1dB CF = CM CR < 5.0 A
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com	 B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30GHz @-1dB CF < (15-40) g CR < (0.5-1.0)A
E-tec Interconnect AG Friedhofstrasse 1 2543 Lengnau Switzerland Tel: +41 32 654 15 50 Fax: +41 32 652 26 93 www.e-tec.com	 B, D, P, T, CM	BA, BD, LA, SM, TH	CP = 0.3mm CL = 10K - 500K OT = -55C to +300C FQ = 40GHZ @ -1dB CF = 20 - 40 gm CR = 3.0A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40GHz@CM CF < (10-12)g CR = CM
Gold Technologies, Inc. 2360-F Qume Drive San Jose, CA 95131 Tel: +1-408-321-9568 www.goldtec.com	B, D, T	CM	CP > (0.4-0.5)mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6-16.0) GHz@-1dB CF & CR = CM

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High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > (0.5-0.8)mm CL > (50k - 250k)x FQ < (4.4 - 10) GHz @ -1dB CF < (30-50)g OT & CR = CM
High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0A
HSIO Technologies, LLC. 13300 67th Avenue North Maple Grove, MN 55311 Tel: +1-763-447-6260 www.hsiotech.com	D, P, T	BA, BD, LA, SM	CP = ≥0.3mm CL = Product Dependant OT = -55° to 155°C FQ >15-40 Ghz @ -1dB CF = Product Dependant CR = 2.4A
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	P	BA, LA	CP > 0.8mm CR < 10A CL, OT, FQ, CF = CM
Incavo Otax, Inc. 4407 Bee Cave Road, Suite 512 Austin, TX 78746-6496 Tel: 1.512.328.2220 Fax: 1.512.328.2228 www.incavo.com	B, D, P, T, CM	BA, BD, LA, SM, TH	CP > 0.01mm CL = 300K to 1000K OT = -55°C to 155°C FQ = 3.0~40 GHz @ -1dB CF = 6g to 50g CR < 6.0A
Ironwood Electronics 1335 Eagandale Ct Eagan, MN 55121 Tel: +1-800-404-0204 www.ironwoodelectronics.com	B, D, T	BA, LA, SM	CP > (0.25-0.4)mm CL > (2k - 500k)x OT = -70°C to +200°C FQ < (6-40)GHz @ -1dB CF < 50g CR < (2.0-8.0)A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3-0.4)mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	D, P, T	BA, BD, LA, SM	CP > 0.3 mm CL > (300k - 1,000k)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8-6.7)A
Leeno Industrial Inc. 10 105 beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea Tel: +1-408-313-2964(US) / 82-51-792-5641 www.leeno.com	LEENO B, D, P, T, CM	BA, BD, LA, SF, TH	CP > 0.1mm CL = >200K OT = -55C~150C FQ = 6ghz ->50ghz @ -1dB CF = 6g-50g CR = <<3.0A @0.4p
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25-0.4)mm CL=CM OT = CM FQ = CM CF = CM CR = CM

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M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjc.co.jp	B, D, T	BA, SM	CP > 0.2mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM
Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25-50)g CR < (1.0-3.0)A
Modus Test LLC 1241 N. Plano Road, Richardson, TX, 75081 Tel: (972) 914-7866 Fax: (972) 534-1208 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3mm CL > 1,000,000x OT = +200°C Max FQ < 20GHz @ CM CF < 35g CR < 5.0A
Multitest Electronic Systems 4444 Centerville Road, Suite 105 Saint Paul, MN, 55127-3700 Tel: +1-651 407 7726 www.multitest.com	D, T	BA, LA, SM	CP > (0.25-0.5)mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5-40) GHz @ CM CF < (26-55)g CR < (1.8-4.6)A
NHK SPRING CO., LTD. 3-10 Fukuura, Kanazawa-ku, Yokohama, 236-0004, Japan Tel. +81-45-786-7511 Fax. +81-45-786-7599 www.nhkspg.co.jp/eng/products/it/communication	D, P, T	BA, BD, LA, SM	CP > 0.135mm OT = -75°C to +200°C FQ < 20GHz @ -1dB CL, CF & CR = CM
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong, Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4-0.5)mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0-12.4) GHz @ -1dB CF < (7-15)g CR < (0.5-1.0)A
Paricon Technologies Corporation 500 Myles Standish Blvd. Unit 103 Taunton, MA 02780 Tel: (508) 676-6888 Fax: (508) 676-8111 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1-0.4)mm CL > 1,000,000x OT < 150°C FQ < 40GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtest.com	D, T	BA, LA, SM	CP > 0.4mm CL > 1,000,000x OT = -40°C to +150°C FQ < 40GHz @ -1dB CF < 25 g CR < 3.5 A
Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
Precision Contacts Inc. 990 Suncast Lane El Dorado Hills, CA 95762 Tel: +1-916-939-4147 Fax: +1-916-939-4149 www.precisioncontacts.com	D, T	BA, LA, SM	CP < (0.4 - 0.5)mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0-4.0) A

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Qualmax, Inc. 3003 North First St. Suite 340 San Jose, CA 95134 Tel: 1-408-519-5748 Fax: 1-408-490-1820 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5)mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0-4.0) A
R&D Altanova 3601 So. Clinton Avenue South Plainfield, NJ 07080 Tel: +1-732-549-4554 Fax: +1-732-549-1388 www.rdaltanova.com	 D, P, T	BA, BD, LA, SM	CP < 0.3mm CL = 150,000x OT = -40° to 150°C FQ > 38GHz @ -1dB CF = 15g CR = 4A
Rika Densi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36 GHz @ -1dB CF < (15-30)g CP & CR = CM
Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3-0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35mm OT = -55°C to +150°C FQ < (9-10) GHz @ CM CR < (1.0-15.0) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Ave., Suite103 San Jose, CA 95120 Tel: +1-408-269-2800 Fax: +1-408-269-2006 www.sanyu-usa.com	CM	CM	CP > 0.2mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15-25) g CR < (4.0-5.0) A
Sensata Technologies, Inc. 529 Pleasant St. P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	 B	BA, LA, SM	CP > (0.4-0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10-25) g CR < 1.0 A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3-0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5-20) GHz @ CM CF & CR = CM
Smiths Connectors 5101 Richland Avenue Kansas City, KS 66106 913-342-5544 www.smithsconnectors.com	 D, T	BA, BD, LA, SM	CP > 0.2mm CL > 250k-1M OT = -40° to 150°C FQ < 25GHz @ -1db CF = 8 - 85grams CR = 1.5 to 5 Amps
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3, 11900, Bayan Lepas, Penang, Malaysia. Tel: 604-646 6966 www.tts-grp.com	 D, T, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5-1.0) A
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: 1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5-80) g CR < (0.5-1.0) A

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Yamaichi Electronics Co., Ltd. 1F Technoport Mitsui Seimei Bldg. 2-16-2, Minamikamata, Ota-ku Tokyo 144-8581, Japan www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Manufacturing of America 4081 Leap Road Hilliard, OH 43026 Tel: (614) 921-2700 Fax: (614) 921-2705 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM

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The image shows two large, grey, industrial-grade test systems labeled "AEHR TEST SYSTEMS" and "FOX". A person in a blue protective suit and mask is standing next to one of the units, interacting with its control panel. To the right of the units, there are several stacks of silicon wafers, each consisting of multiple wafers. Below the wafers, a text overlay reads: "Process up to 15 wafers simultaneously in each FOX system". At the bottom of the image, the website address "www.aehr.com" is displayed.

AEHR
TEST SYSTEMS

A new look at multi-probe testing strategies

By Al Wegleitner [Texas Instruments]

Over the last decade, the semiconductor test industry has reinvented the way multi-probe testing is approached and the requirements that are necessary to test the high complexity and high mix of devices inside supported digital, analog, and mixed-signal product lines. The embedding of logic, core memory, and analog signal processing has significantly increased the number of channels and inputs/outputs per device. It has also in turn increased the test cell requirements to support the complexity of the individual test programs.

Traditional device testing has moved from testing x1 or x2 die layouts to x128 and higher mixed-signal die counts during multi-probe testing. **Figure 1** illustrates the shift in quantity of die testing in parallel at multi-probe for non-memory types of devices. The first distribution shows the average number of die tested by site count from 1995 to 2005, clearly indicating that the increase to quad-site mixed-signal testing was the majority of the parallel testing effort during that time.

The second distribution represents the period from 2005 to 2015. It shows a marked increase in the number of sites being tested indicating that 32- and 64-site parallel testing has become the norm, with further increases growing beyond 128 sites in parallel.

The need for change

Device complexity continues to rise as new features are introduced and integrated into single-chip solutions. This integration of capabilities and features increases overall test time requirements per die. Increasing test times continues to pressure the cost of each unit tested. Furthermore, traditional industry cost modeling drives test cost to less than 10% of unit cost and strives to get below 5% of unit cost.

Automated test equipment (ATE) suppliers have kept pace with the additions of front-side bus speed increases, power supply, and memory increases, which

have advanced the capability of the tester itself. These increases in architecture have improved parallel test efficiencies into the upper 90% level. This efficiency increase has allowed for the development of higher multi-site testing solutions, which were prohibitive in previous generations due to serial latency time offsets between die tested in parallel and total available resource instrumentation.

The common industry metric - parallel test efficiency (PTE) - has been the key enabler for higher multi-site testing (see **Eq. 1**). The target of parallel test efficiency is for all sites to test in parallel at the same speed as an individual die without loss of efficiency in timing or data transfer rates. The end efficiency target is to get to 100% efficiency with all sites under test during the same time interval. The premise is that all sites are good and all sites are testing.

Any lost efficiencies would be indicative of instrumentation or processing delays.

card layout requires instrumentation to be shared by site count.

The need to drive lower test cost per unit forces strategic decisions to be considered in regard to the total number of test cells required versus the level of multi-site capability. Test cell cost can easily reach \$1 million when maximum resources are installed, while multi-site probe cards can exceed \$150,000 in the mixed-signal world. Attaining maximum parallel test efficiency has to be at the forefront of testing strategy and test cell or test program development efforts.

New challenges

The increased site counts have created significant challenges to the probe card design and infrastructure required to support massive multi-site assemblies. They have also imposed significant mechanical and electrical challenges when designing probe cards.

Common industry metric is Parallel Test Efficiency (PTE), defined as . . .

$$PTE = \left(1 - \frac{\text{Testtime}(\text{Maxsites}) - \text{Testtime}(1 \text{ Site})}{(n-1) \cdot \text{Testtime}(1 \text{ Site})} \right) \quad \text{Eq. 1}$$

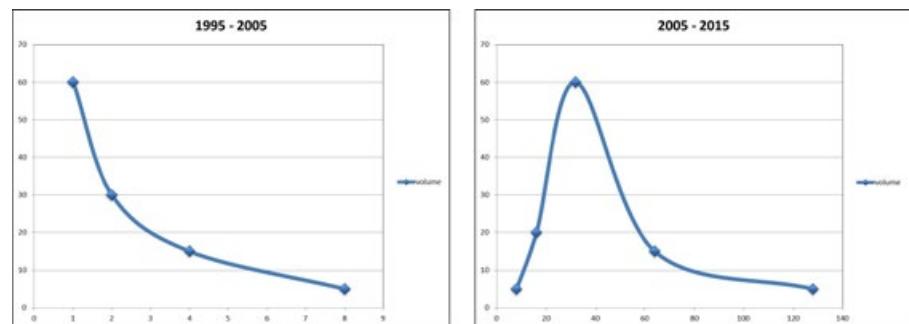


Figure 1: Volume by site count.

In reality, we will never see 100%, but we should target greater than 96%. The loss of efficiencies can be attributed to serialized testing sequences where tester resources are shared during test, test sequences where sampling rates are waiting on data return versus a pass/fail, or where probe

As the industry has increased the number of sites being tested in parallel, it has magnified the probing forces to the breaking point of probe cards and probers. Test head manipulators, test head docking assemblies, and probers have all had to increase in size and scale to support the

higher multi-site requirements. Prober equipment suppliers have increased the baseline probing-over-travel applied force from 100kg to 350kg to keep pace with higher pin counts. These higher forces are needed to compensate and overcome the spring force of the probe cards. A typical high multi-site probe card will often have at least 20,000 pins, with each pin exerting from four to eight grams of force. This easily translates into 160kg of static force that the prober must overcome during multi-probe testing.

These significant forces in the upward direction by the prober create bowing and twisting of the probe cards, which can easily be greater than 200 μm in deflection. This deflection away from the die reduces the electrical contact during testing, which creates contact fails. Normally, between 75 μm and 100 μm of over-travel is applied during testing as the baseline operation.

We use the terms “programmed-over-travel” (POT) to describe the settings in our case of 100 μm – POT = 100 μm . We would expect the probe card to apply 100 μm of force to the die, but if the deflection is 200 μm , many of the probe needles are not touching the die. We call this “applied-over-travel” or (AOT). Thus, for many of the needles, the AOT is 0. To compensate for this, we have to add thick metal, stainless steel, or aluminum stiffeners to the probe cards to minimize the deflection. Even when we add these stiffener assemblies we still see deflections in the 20 μm ranges. So, if we use our POT = 100 μm and our AOT = 80 μm , from the real measurements we are seeing about a 20% loss of force. This requires us to increase POT to 120 μm or higher to compensate for the loss. **Figure 2** illustrates the forces and how they are overcome. **Figure 3** shows an example of the mechanical stiffener assembly and the mass required to resist the probing forces.

Probing forces continue to increase with the size of the probe cards and higher pin count devices. A typical microcontroller device will see approximately 500 pins per die, while an embedded microprocessor will see 7,000 pins per die. These numbers quickly translate into 20,000 to 40,000 pins for a probe card assembly. These increasing forces require significant early design work to compensate for negative impacts. The high forces require us to find and design lower force pin options and to depopulate the probe card where feasible to assist in lowering the total applied force.

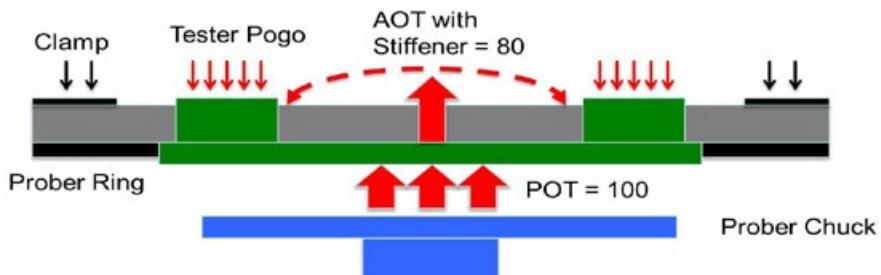


Figure 2: Probe force deflection model.

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Figure 3: A probe card stiffener hardware example.

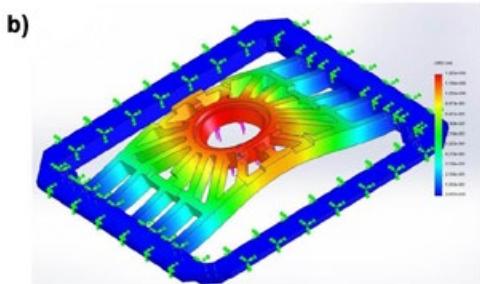
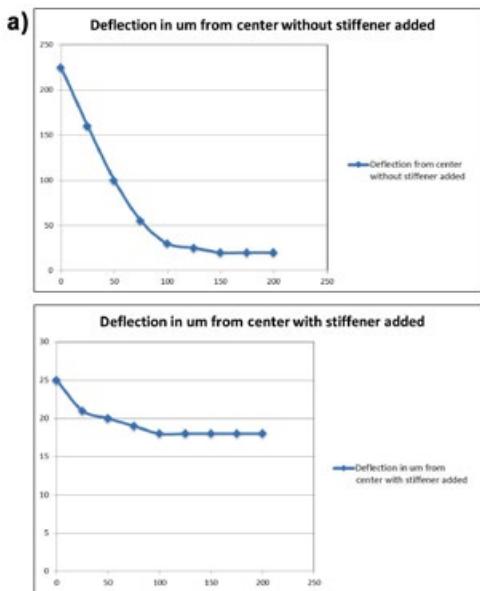


Figure 4: a) Measured probe card deflection without and with stiffener applied; and, b) An example of finite element analysis applied to probe card design.

Engineering solutions

To mitigate the higher forces and loads noted above, we must implement finite element analysis on probe card designs to pre-model stresses and provide early learning on potential failure mechanisms. **Figure 4** shows an example of finite element analysis (FEA) for a probe card assembly design that models the deflection properties before any probe card hardware is built.

Multiple iterations are modeled until we can be confident that the assembly

will be successful in the production environment. The high multi-site FEA modeling data has allowed us to prevent production failures and has forced us to change our build specifications to align to all the enhanced information gained from the models.

These high-force probe cards increase the risk of die cracking between dielectric oxide or sub-bond pad metallization layers. Validation requires mechanical and chemical de-processing of the bond pad structure to detect potential failure modes and pressure points prior to volume production releases.

High force multi-site probe cards are not enough of a test engineering challenge – we must add temperature extremes into the equation. In today's testing environment, it is very common to have multiple test insertions and multiple temperatures. We see iterations at -40°C, 30°C, 85°C, 125°C, 140°C, 155°C, 175°C, and 200°C in production environments, and 300°C in laboratory reliability-type settings. These temperature extremes create very chaotic mechanical movements of the probe card assemblies. We see typical thermal movements in the 110µm ranges at 125°C and movement increases as temperatures elevate.

Probe needles move up or down as they come into contact with the heat source of the prober chuck movement under the probe card. This distorted movement creates excess bond pad damage and rejected die for post-inspection quality results. Compensation of the distorted movement is achieved through several iterative improvements. The probe card stiffener assembly is modified to allow the center section of the probe array to be mounted or fixed to the stiffener mechanically. The printed circuit board (PCB) is allowed to flex under temperature and not force the probe array to move as radically under the thermal load changes.

The prober controls movement by performing an optical needle inspection at a fixed time interval that is matched to the test time of the die and number of steps the prober moves. This optical check realigns the prober position in the Z-height axis to compensate for the movement up or down from the last reading.

Control of Z-height to within 10µm of baseline settings are required to provide sufficient electrical contact during testing. Longer test time devices make this setting critical to maintain and require more frequent compensation through automation control. Advanced stepping maps are created to minimize the stepping distance traveled away from the thermal heat source and to keep the probe card centered as much as possible to provide uniform heating and cooling. Rather than the standard x serpentine probing movement, y-axis probing, spiral-out or spiral-in movements can be deployed to assist in thermal budget management.

Probe card metrics with respect to the card lifetime are maintained to judge performance standards and baseline expectations. The higher cost of massive multi-site probe card assemblies requires lifetime numbers to constantly improve beyond the historical 1 million touchdowns, to more than 4 million today.

Vertical technologies and metallurgical combinations are continuously being evaluated and fanned-out in an effort to increase current carrying capacity and lifetimes. Cleaning medias and cleaning routines continue to drive lifetimes higher in support of the metallurgical improvements. Mean-time-between-failures (MTBF) and overall equipment utilization (OEU) are closely monitored to ensure that the test cell is achieving the expected output.

Summary

Massive multi-site mixed signal device testing has created significant challenges to the multi-probe testing infrastructure. Retooling the testers, probers, and probe card systems has presented significant changes to support the growing mechanical and electrical demands of testing 128 die simultaneously and beyond. We should expect this trend to continue as we look for more efficient ways to drive the cost-of-test downward, while continuing to increase the complexity of the systems and devices themselves.

Biography

AI Wegleitner received his BS/MS in Electrical Engineering from Morehead State U. and MBA from the U. of Texas at Dallas. He is a member of the Test Technology and Product Engineering Group at Texas Instruments, and leads the Probe Test Solutions team; email a-wegleitner@ti.com

Silicon photonics packaging and optical interconnection at the board level

By Lars Brusberg, Markus Wöhrmann, Dionysios Manessis, Marcel Neitz, Henning Schröder, Tolga Tekin, Klaus-Dieter Lang
[Fraunhofer Institute for Reliability and Microintegration (IZM)]

Optical signal transmission offers superior bandwidth benefits compared to copper-based electrical signal lines that will be very important in data centers and high-performance computers for high-speed and short range interconnects in the near future. Multi-channel fiber-based optical links are already used as interconnection in racks or between racks. State-of-the-art optical links are active optical cables with a pluggable electrical connector at the board edge, electro-optical transceivers inside the connector package, and fiber-based cables between the two connectors. Because of the very high I/O bandwidth of high-performance computing multi-core processors, electro-optical transceivers have moved closer to the processor units to reduce the electrical interconnection length [1]. Mid-board transceivers and optical fiber links reduce the electrical path length, but if the number of fibers or circuit complexity increases dramatically, then optical waveguide layers integrated in the printed circuit board will become important.

Silicon photonics offers unique bandwidth possibilities because of wavelength division multiplexing. For multiplexing, board-level optical interconnects have to be single-mode. Today, worldwide research focuses on implementing all important photonics building blocks in silicon such as the laser, modulator, switch, filter, and detector. On the other hand, there is a lack of single-mode optical interconnection between silicon photonics devices assembled on printed circuit boards (PCB).

Our ongoing research activities comprise the development of a single-mode PCB for fabrication of optical line-cards and backplanes. Also in progress is the development of optical coupling interfaces to photonic ICs and pluggable optical connectors. Fraunhofer IZM is targeting development of a single-mode electro-optical circuit board (EOCB) for

high-precision flip-chip assembly and e/o interconnection of silicon photonics components and optical interconnection with single-mode optical fibers.

A new packaging concept

The electro-optical interface between silicon photonic components and underlying substrates is not standardized and different research approaches have been reported in the past [2-4]. Our packaging concept consists of planar glass waveguides and electrical pads patterned on glass. The silicon photonic interposer will be assembled above a cut-out area in the optical glass layer. A coupling element will be assembled underneath in the glass cut-out and in front of the waveguide facet for optical interconnection between the optical ports of the silicon photonic interposer

and the glass waveguide array. The board-to-chip interface consists of a free space optical path with a concave mirror element for beam deflection and refocusing of the signal as shown in **Figure 1**. The photodetector and laser will be hybrid-integrated on the silicon interposer. An array of vertical-cavity surface-emitting lasers (VCSELs) and photodiodes are flip-chip assembled on the interposer's bottom side. The light of the VCSELs is coupled by grating couplers into the silicon-on-insulator (SOI) waveguides. In our concept, grating couplers are the optical I/Os for interconnection with the EOCB. Additionally, backside illuminated flip-chip assembled photodiodes underneath the interposer will be receiving optical signals for O/E conversion. The active area of the photodiodes is not on the same focus level

as the grating couplers—a fact that has to be considered. Additional ASICs can be mounted on the top side of the interposer and electrical signals are routed by through-silicon vias (TSVs).

The glass is the core layer in the EOCB stack-up. The transparency, thermal stability and low coefficient of thermal expansion (CTE) are the main benefits for promoting the concept of embedding a glass layer into a PCB. Windows in the stack-up above and underneath the glass layer provide access from both sides to the glass core layer for assembly on glass. An EOCB was designed

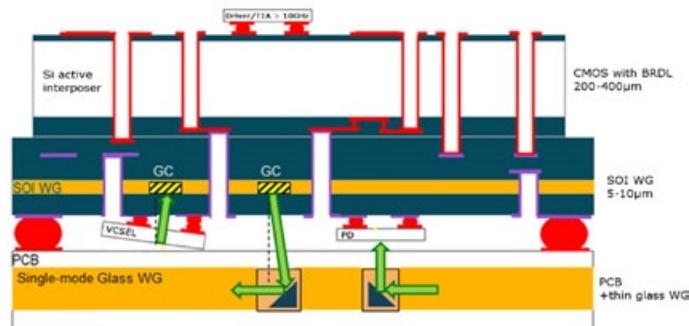


Figure 1: Schematic of the electro-optical interface between the silicon photonic interposer and the electro-optical circuit board.

to prove out our concept and evaluate the necessary technologies for fabrication. The board size was defined to be 233 x 303mm², having two areas for silicon photonic interposer assembly as shown in **Figure 2**. The 500μm glass panel with

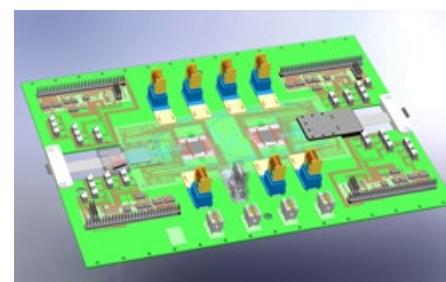


Figure 2: Concept view through the assembled EOCB with optical waveguides (turquoise lines), electrical circuitry (rose lines) and prepreg and FR4 layers (green).

optical waveguides (turquoise lines) and electrical circuitry (rose lines) has an area of $84 \times 181.5\text{mm}^2$ and is embedded as the core layer between FR4 prepregs (green) and patterned copper (rose lines) layers. On the four sides around the glass panel, the optical interfaces are defined for board-to-board and fiber-to-board waveguide termination.

Electro-optical circuit board fabrication

A 200mm wafer-level process was selected for development of optical and electrical integration of interconnects on glass. A two-step thermal silver ion-exchange waveguide process has been applied for planar waveguide integration. The refractive index profile is characterized by an elliptical cross section with the index a maximum in the waveguide center $5\mu\text{m}$ below the glass surface [5]. The waveguide layout is defined by an aluminum thin-film mask. The mask opening width directly influences the lateral waveguide dimensions. Lithography and wet-chemical etching is applied to defining the waveguide layout with mask openings of $3\mu\text{m}$. The process is performed at the wafer level because of the resolution limitation of our in-house laser direct-imaging (LDI) system (the Orbotech Ultra-200 with $8\mu\text{m}$ line width and $12\mu\text{m}$ spacing). Improving panel-level lithography for this system is currently under investigation. A $5\mu\text{m}$ PVD glass cladding layer was deposited over the full area as an optical cladding layer. A $7\mu\text{m}$ CTE compensation layer made of polyimide was patterned in the area between the electrical copper lines and the glass. Then the electrical circuit was patterned by thin-film metallization with copper lines of $5\mu\text{m}$ height. For increasing the distance between the glass and the silicon photonic interposer, and for the underneath flip-chip assembled components, $50\mu\text{m}$ copper pillars with bondable surface finish were additionally patterned on glass for the interposer attach process. The manufactured wafer is shown in **Figure 3** with dual-layer embedded single-mode waveguides on both sides and electrical circuitry with bond pads on one side. Finally, the glass wafer was cut to smaller panels of $84 \times 181.5\text{mm}^2$ in size, and two cut-out inserts between the electrical pad rows for later placement of the optical mirror

underneath the silicon photonic interposer.

The resulting glass panel ($84 \times 181.5\text{mm}^2$) is placed as an inlay in a pre-prepared glass frame ($233 \times 303\text{mm}^2$) for achieving a full area symmetrical PCB stack-up. The intricate glass frame was precisely processed by laser cutting. For the frame, glass was selected instead of FR4, which showed high warpage of the EOCB after lamination due to the CTE mismatch. Cavities in the four corners of the glass frame were filled with FR4 inlays of the same size to allow through-via drilling with standard mechanical PCB equipment without destroying the glass. By using this process, and also because of the use of copper plating of the through-vias, benefits accrue because a standard chemical pre-treatment for copper plating is used instead of depositing an adhesive layer inside the vias. Copper circuits were successfully patterned on different stack-up materials such as glass, FR4, and prepregs, and were interconnected by vias as shown in **Figure 4**.

Automated assembly routine for optical chip-to-board coupling

The assembly routine is defined by solder bonding of electrical components, thermocompression (TC) bonding of the silicon photonic interposer directly on glass, and active alignment and adhesive bonding of fiber-to-board and chip-to-board interfaces. Coupling

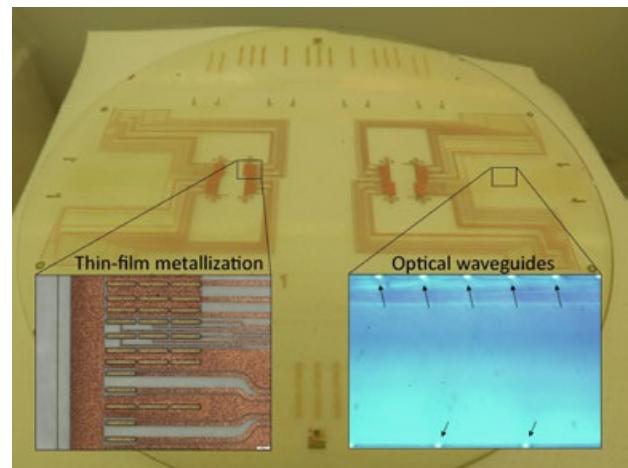


Figure 3: Optical dual-layer waveguide integration and thin-film metallization on the 200mm wafer level.

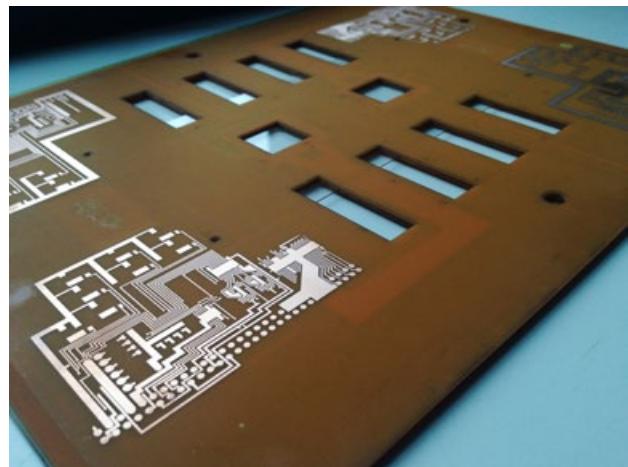


Figure 4: An electrical PCB with an embedded optical glass layer (EOCB).

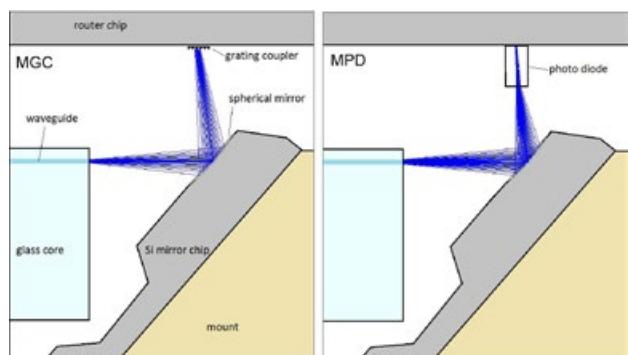


Figure 5: Deflection and refocusing of an optical beam (blue lines) between the grating coupler and glass waveguide facet (left) and photodiode and glass waveguide facet (right).

of single-mode optical interconnects requires a highly accurate assembly technology with sub-micron capabilities to achieve best results. The developed coupling element has 56 bidirectional optical channels, board-to-grating couplers, 12 one-direction optical

channels, and coupling from board to the photodiodes. The coupling principle is to redirect and to focus the divergent outgoing ray with a concave mirror as shown in the schematic cross section in **Figure 5** for the grating coupler and photodiode I/Os. The grating couplers on the silicon photonic interposer have a radiation angle of 10° to the plumb line. That means that the mirror face needs to lie in a 50° angle relative to the waveguide plane of the EOCB.

The coupling element is made of a glass mount and a silicon mirror chip. The concave mirrors were etched into a silicon wafer by combining 3D lithography and reactive ion etching. To decrease the possible distance between the mirror and waveguide facet, a ditch was etched into the chip by KOH-etching. The surface of the chip was gold sputtered for high reflectivity of the mirrors. After dicing the silicon wafer to a chip size of 5 x 15mm², the chip was assembled by an adhesive bonding pick-and-place process to a glass mount. At Fraunhofer IZM, ficonTEC AL-500 pick-and-place machines are used to achieve low insertion loss by active alignment and short processing time. The combination of feature-based machine vision with high magnification telecentric camera optics, a highly precise mechanical multi-axis system, integrated optical measuring system, adaptable manipulation of components (gripping), and UV-curing adhesive, provides the flexibility that is inevitable for our optical assembly approach.

One of the exceptional strengths of the developed pick-and-place process is active optical alignment, which finds the best possible component position making mechanical tolerances less of a factor. The basic principal here is a closed-feedback loop, which has optical characteristics as measurement parameters and axis-positions (up to 6 DOF) as the controlled condition. For waveguide arrays, the alignment becomes quite complex and requires an assembly routine that is able to cope with various starting conditions and with the huge dimensions of the coupling element vs. coupling tolerances. Because EOCBs do not provide any active optical components, the efforts required to establish an optical interconnection are quite high.

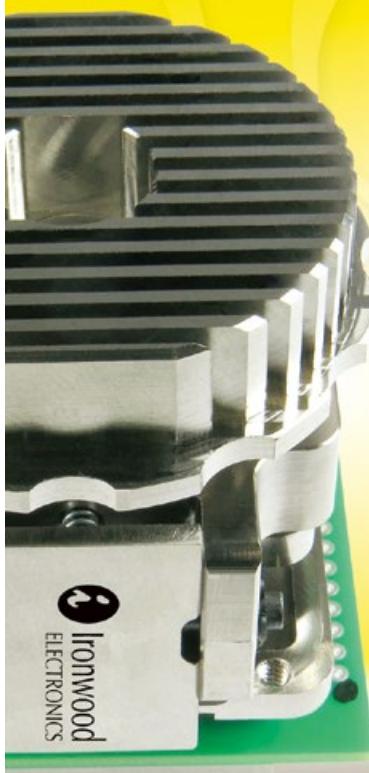
The technological problem at hand requires the coupling of optical energy through grating couplers (chip-side) in and out of the integrated waveguides (board-side). Therefore, the optical signal is deflected in a 10 degree angle by the mirror of the coupling element.

The advantage of using the closed optical loop in the silicon photonics chip for active alignment of the two outer optical channels, is that only

one manipulation stage is needed for accomplishing the coupling task. Therefore, it will be reducing the complexity of the assembly stage, as well as the cost of investment. The developed assembling process consists of three major steps: 1) component feature detection and picking, 2) pre-alignment (by fiducials) and dispensing of adhesive, and 3) active alignment (by measuring insertion loss), including UV-

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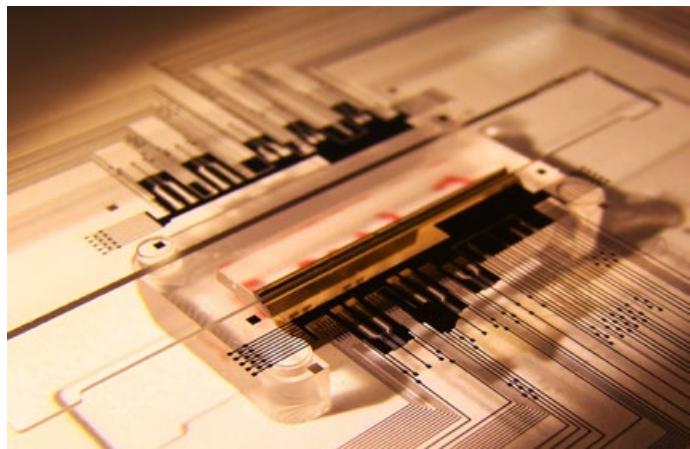


Figure 6: A coupling element fixed on the glass layer of the EOBC. The mirror element provides a ditch to bring the spherical mirrors closer to the optical glass edge. Later, there will be the silicon photonics chip covering the deflection mirror.

curing. An assembled coupling element inserted into the glass cut-out between the electrical pad rows is shown in **Figure 6**.

Summary

We have developed a new single-mode planar glass-based electro-optical circuit board technology providing a silicon photonic IC platform for data center and high-performance environments. A process has been presented and elaborated for fabrication and embedding of an electro-optical glass core in a PCB. Additionally, a generic optical board-to-chip coupling interface has been developed and board-level assembling technologies have been successfully proven. Ongoing work focuses on the full demonstration of a single-mode EOBC with assembled silicon photonic ICs that are directly interconnected at the board-level with data rates up to 40Gbit/s per channel.

Acknowledgements

Author Lars Brusberg wrote this article while at Fraunhofer IZM prior to December 2015. The research leading to these results has received funding from EU ICT within the European project PhoxTrot (Ref. 318240). Financial support is greatly appreciated.

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Finer solder paste powder sizes enable new assembly technologies

By Jason Fullerton *[Alpha Assembly Solutions]*

Solder paste is an essential material for printed circuit board (PCB) assembly. Widely used since the 1980s, this primary assembly material is the subject of a significant amount of innovation due to the current advances in miniaturization of surface mount technology (SMT) devices.

The traditional SMT manufacturing process involves the application of solder paste to the PCB by squeegee printing through a metal stencil that matches the PCB design. There are a variety of different properties of solder paste that enable the use in stencil printing; most notably, the rheologic properties of the flux medium and the powder size of the metal alloy. Some de facto standards exist with respect to what a typical SMT process utilizes: the stencil will be 4 or 5 mils thick laser cut foil, the ratio of the aperture opening area to the sidewall surface area (area ratio or A/R) will be larger than 0.66, and the solder paste powder size will be Type 3 or Type 4. Many users of solder paste intrinsically understand that “smaller powder prints better,” but may not understand the full details regarding how solder paste powder sizes are defined.

Solder paste powder size distribution (PSD) is defined by IPC J-STD-005A, “Requirements for Soldering Pastes.” (There are other PSD specifications, notably Japanese Industrial Standard JIS Z 3284, in use worldwide.) J-STD-005A defines a number of particle size distributions from the coarsest Type 1 to the finest Type 8. Many users shorten the specifications to simple particle diameter ranges, such as equating Type 3 with “25–45 micron diameter” and Type 4 with “20–38 micron diameter.” However, there are a number of requirements related to

the distribution of the particle sizes. J-STD-005A defines the following requirements on the particle size distribution:

- Maximum size (<0.5% larger than);
- Particle size (80% minimum within range): Types 1–3;
- Particle size (90% minimum within range): Types 4–8; and
- Minimum size (<10% smaller than).

These requirements are designed to define a bell-shaped (or normal) distribution of the solder particle diameters represented by a specific PSD Type. **Table 1** summarizes the particle size ranges for all particle size distributions defined.

Note that some PSD Types overlap with their nearest defined type. For example, Type 3’s average range is 25–45 microns, whereas Type 4’s average range is 20–38 microns. These overlapping distributions result in an effective incremental change in solder paste properties that are a result of alloy PSD. In contrast, Type 5’s average range is 5–15 microns, which does not overlap with Type 3. This results in a more significant shift in solder paste properties when changing from Type 3 to Type 5.

The increasing miniaturization of SMT devices leads to significant challenges with the standard stencil printing technology. The traditional rule of thumb for stencil aperture A/R has been 0.66 or greater. Finer powders provide printing performance that enables stencil designs that push beyond this traditional limit on printing capability.

Powder Size	Particle size, micron (80%/90% range)
Type 1	75–150 (80%)
Type 2	45–75 (80%)
Type 3	25–45 (80%)
Type 4	20–38 (90%)
Type 5	15–25 (90%)
Type 6	5–15 (90%)
Type 7	2–11 (90%)
Type 8	2–8 (90%)

Table 1: Particle size range summary.

Aperture (micron)	A/R (100 µm foil)	Type 4		Type 5	
		%TE	Cpk	%TE	Cpk
180	0.45	15	0.0	80	1.4
190	0.48	20	0.4	80	1.2
200	0.50	35	0.6	80	2.1
210	0.53	50	1.4	90	2.2
220	0.55	60	2.8	95	1.9
230	0.58	60	2.9	90	2
240	0.60	60	3.1	95	1.7
250	0.63	60	3.4	95	1.7

Bad
Good
Excellent

Table 2: Comparison of Type 4 and Type 5 PSD printing performance.

The data in **Table 2** demonstrates the performance difference, summarized from an experiment that compared the printing performance of Type 4 and Type 5 powder using identical solder paste formulas, identical stencils, and identical printing process inputs.

This experiment considers any transfer efficiency % (TE%) less than 50% to be “Bad,” TE% greater than 75% “Excellent,” and the intermediate range (50–75%) as “Good.” The Cpk value, which is an index that measures variation relative to a specification range for TE%, considers less than

1.0 to be “Bad,” greater than 1.67 to be “Excellent,” and the intermediate range (1.0–1.67) to be “Good.”

The important result to take from this data is that the Type 4 powder did not meet even the lowest standard of acceptability until an area ratio of at least 0.53. In contrast, the Type 5 powder was capable of printing with excellent results with an area ratio as small as 0.50. It should also be noted that the TE% and Cpk for the Type 5 powder exceeded that of Type 4 in all cases in these unusually small apertures. This is a good demonstration of the ability of small PSDs to enable printing at area ratio values that have been considered impossible under traditional rules that advise area ratios greater than 0.66.

Other applications enabled by PSDs

There are other solder paste application processes that are enabled by the use of small PSDs. Solder paste dipping is an example. This assembly technology is used primarily in two scenarios.

PCB assembly. The first example of the need to utilize solder paste dipping is when a package used on a PCB assembly that requires printing through smaller apertures than the normal solder paste in use would allow. This is typical when ultra fine pitch area array packaged devices, such as flip-chip and chip- or wafer-scale packages, are installed at SMT along with other traditional (larger) SMT devices. The need to provide sufficient solder paste for the larger devices limits the ability to reduce stencil foil thickness to achieve a useful area ratio value for the ultra fine pitch device. In this scenario, the stencil is designed to optimize for the larger devices and solder paste dipping is utilized for application of solder paste to the ultra fine pitch device.

PoP. The second example of a situation where solder paste dipping is useful to implement is assembly of package-on-package (PoP) stack

devices. PoP stacks can be assembled together on the PCB assembly or can be assembled as a subassembly for future installation to a PCB. In both cases, the upper package is dipped in solder paste prior to assembly to the lower package.

Dipping solder pastes utilize smaller powders (Type 5 and smaller) than the typical pastes used for printing in order to minimize the risk of bridging to adjacent interconnections and to maximize the particle density (and thus, solder material) surrounding the package bumps when dipping. The dipping process is facilitated by the use of dipping hardware in the SMT pick and place equipment. Depending on the hardware configuration used, the process inputs involve controlling the dip thickness, dip hold time, and dip rise velocity (Figure 1). Dip depth is typically dependent on the ball diameter, where dip hold time and dip rise velocity are dependent on the properties of the dipping solder paste material (Figure 2).

Jetting. A third technology that has emerged for solder paste application is jetting. There are a variety of manufacturers that have introduced jetting equipment to the market in the past five years. This type of solder paste application provides a number of advantages when used in conjunction with, or as a replacement for, stencil printing. First, a jetting application can be used to rework deposits identified as insufficient during post-printing solder paste inspection without having to reprint the entire PCB. Jetting

equipment can be used in conjunction with stencil printing to enable a mix of traditional large SMT devices and ultra fine pitch devices together, without having to compromise on providing sufficient solder for large devices or attempting to print very difficult small apertures. Finally, jetting can be used as a replacement for stencil printing in situations such as prototype development, where very small batch sizes and frequent stencil design changes are common.

One characteristic of pastes used for jetting are the use of small powder sizes, most frequently Type 5 and smaller. This is driven by the relationship between PSD and minimum feature size supported. Clearly, the smaller the solder particles used in the solder paste, the smaller the single dot that can be created by the jettler, and the smaller the feature that can be printed. Solder paste jetting, when used in conjunction with smaller solder PSDs, is a technology that enables the installation of miniature SMT devices that are too difficult or impossible to install with traditional processes and materials.

Solder paste development, just as most facets of the SMT process, continues to be driven by the increasing miniaturization of SMT devices on modern electronics. Smaller solder particle sizes have enabled new assembly technologies to emerge beyond the traditional SMT process. The capability to print through apertures considered unsuitable using traditional guidelines, package-on-package assembly, and the emergence of jetting as a solder paste deposition technology, are all enabled by the availability of solder paste particle size distributions smaller than the traditional Type 3 and Type 4 materials.

Biography

Jason Fullerton received his BS in Manufacturing Systems Engineering from GMI Engineering & Management Institute (now Kettering U.) and is a Customer Technical Support Engineer at Alpha Assembly Solutions; email JFullerton@Alent.com

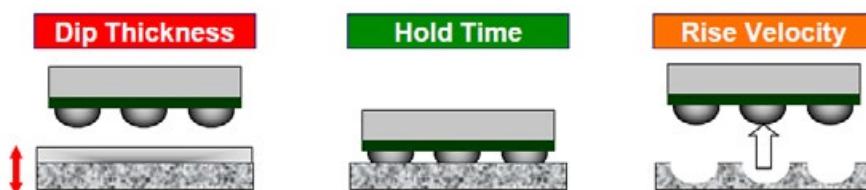


Figure 1: Solder paste dipping process variables.

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GUEST EDITORIAL



ICPT 2015: Klaus Beyer and the invention of chemical-mechanical planarization

By A. Scott Lawing *[Kinik North America]*

The 2015 International Conference on Planarization/CMP Technology (ICPT) took place in Chandler, Arizona at the Wild Horse Pass Hotel and Casino (Sept. 30 – Oct. 2). It was jointly hosted by the CMP User's Group of the Northern California Chapter of the American Vacuum Society, Clarkson University Center for Advanced Materials Processing (CAMP), and the Institute of Electrical and Electronics Engineers (IEEE). ICPT rotates between multiple global locations annually and represents the collaborative effort of CMP Users Groups from all six major semiconductor technology regions of the

world (USA, Japan, South Korea, Europe, Taiwan and China).

The 2015 conference was extremely well attended, with 374 paid registrations—a record attendance for an ICPT Conference. Papers covered a wide variety of topics in CMP and alternative planarization methods, also being drawn from all over the world. The papers were characterized by a high degree of technical rigor, driven by a stringent review process. Including a special section modeled after the annual CAMP conference and organized by

Professor S.V. Babu of Clarkson, there were two keynote speeches, 10 invited talks, 39 submitted oral talks, and over 50 poster papers. The proceedings of the conference will be published by the IEEE. The C M P v e n d o r community was also well represented with a level of support including four platinum level sponsors, 10 gold level sponsors, 13 silver and copper level sponsors, and 30 exhibitors, including almost all of the sponsors.

The technical sessions were exemplified by a good mix of academic and industrial, applied and theoretical. On the fundamental side, Duane Boning from MIT presented an



Dr. Klaus Beyer delivering his keynote address at ICPT 2015.

interesting talk on the “Pad in a Bottle” approach to CMP, where the role of the conventional pad is replaced by polyurethane beads and a stiff counterface, providing a mechanism to decouple variables in a way not demonstrated previously. Wen and Lu from Tsinghua University presented a molecular dynamics simulation of the CMP process at the abrasive/wafer interface in an effort to elucidate the removal mechanism in its most basic

terms. From a more applied perspective, Zhan Liu from Dow provided some insight into models for statistical characterization of conditioner performance parameters, highlighting one of the primary drivers of instability in CMP processes and sharing some tools to quantify it. During the special CAMP session, Suresh Ramakrishnan of Micron and Michael Wedlake of Samsung Electronics both gave excellent talks on CMP process integration issues and challenges from the end user perspective, informing and raising the bar for their colleagues and suppliers in attendance. On the boundaries of CMP applications, Viorel Balan from CEA-Leti gave an update on their innovative work on CMP applied to direct wafer bonding. A market report from the Techcet group pointed out the importance of the Internet of Things (IoT) in driving growth in the CMP consumables market and the unexpected resilience of older technology nodes in this context.

While most of the conference was focused on forward-looking technology, there was also time to reflect on the birth of CMP and how far the industry has come. The first Planarization Lifetime Achievement Award was given to Dr. Klaus Beyer, formerly of IBM. Dr. Beyer invented what we now call CMP in 1983. He was formally recognized by, and told his story to, the CMP community for the first time—and what an interesting and enlightening story it was.

While working in silicon wafer production at IBM, Dr. Beyer was tasked to come up

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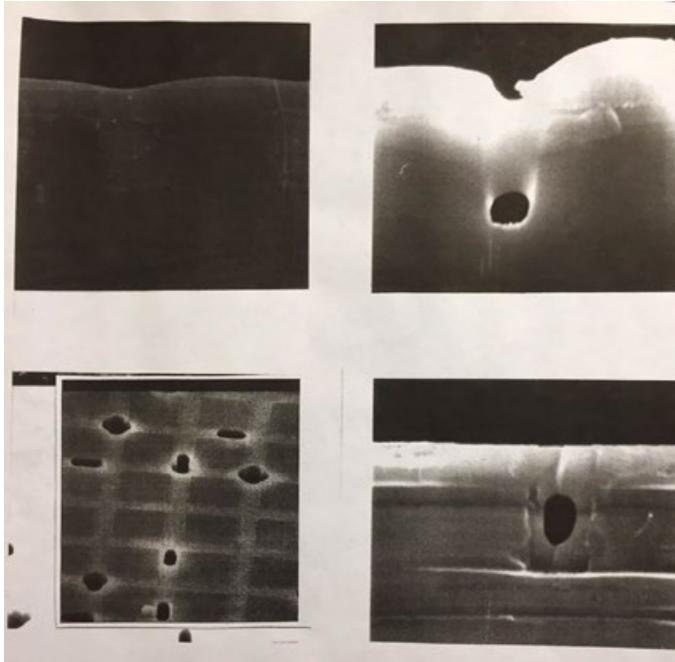
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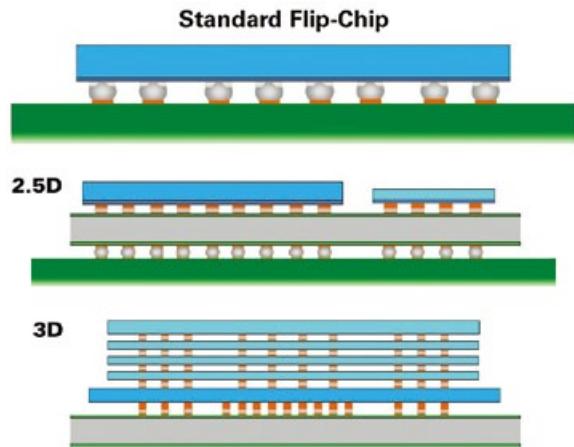


Some of Dr. Beyer's SEM micrographs illustrating the planarization performance of the first CMP process.

with a solution to the problem of post-polish cleaning of prime silicon wafers. Silicon wafers are sawed from a boule and then subjected to a grinding process to remove the damage caused by the sawing process. While CMP had not yet been adopted, or even conceived, polishing in silica slurry was already being used to obtain a smooth surface after the wafer grinding process. After that process, the wafers were cleaned with bristle brushes to remove the slurry particles that adhered to the wafer surface. The problem was that the brushes would frequently become loaded with particles, which led to scratching of the pristine wafer surface. Initially stumped, Dr. Beyer happened upon a brief article describing a new technology for particle removal from surfaces: megasonic cleaning. After contacting the inventors, Dr. Beyer convinced his superiors to bring the technology in house and megasonic cleaning was successfully implemented for prime wafer cleaning at IBM.

In parallel, Dr. Beyer had been asked to join the team working on glass fill in deep trench isolation (DTI). It seems that the glass fill being used in this process caused residual stresses and having studied these types of thin-film stress problems before, Dr. Beyer was asked to help out. As his cleaning experiments were also progressing well, he was charged to work on both projects at the same time. Rather than splitting his time between the projects, he was basically working two full time jobs, causing significant personal stress, but putting him in a unique position to bridge the gap between the two areas. In his keynote address, Dr. Beyer titled his presentation "The Arduous, Strenuous and Lonesome Project," in reference to the long hours he was forced to work and the time away from his wife, family and friends that it demanded.

Dr. Beyer noticed - following a decrease in trench dimensions - that the reflow process designed to smooth out the spin-on glass deposited as a trench fill resulted in a surface that was far from smooth. In fact, the glass tended to bunch up in bulges, caused by surface tension effects in the film. As Dr. Beyer was not aware of any existing planarization project that could flatten these bulges, he seemed to be once again at an impasse.



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Or was he? Now that he had a robust method to remove particles from wafer surfaces without damage, he surmised that a polishing process might successfully planarize the glass bulges he was observing from the trench fill. Under cover of darkness, he snuck some wafers through a polishing tool and a megasonic clean (after all this was a crazy idea was it not?). He taught himself enough of how to use a scanning electron microscope so that he could do his own analysis of the cleanliness of the wafers. To his amazement, the wafers were not only clean, but the trench oxide surface was almost perfectly flat. In another fortunate coincidence, Dr. Beyer's second-level manager had resigned giving him a direct line to upper management. He was able to secure support for an effort to develop a DTI integration based on a CVD trench fill combined with his new CMP. This resulted in the first use of CMP in manufacturing barely a year later. With a department now dedicated to this new process, "CMP" (as it

has come to be known) spread like wildfire throughout IBM and became one of the most quickly adopted, and enabling processes in the history of the company, not to mention the industry as a whole. As Paul Feeney, co-chair of ICPT, said, "Klaus' talk was amazing. I started learning CMP in 1989 at the same IBM location where it was invented and I had never met him. Over the years, I had heard his story many times, but always second-hand or third-hand. Not only was the story fascinating, but it led to a standing ovation afterwards. I cannot think of another time that I have ever seen a standing ovation at a technical conference."

Dr. Beyer's story is one of cross-disciplinary innovation, hard work and serendipity. An individual at the right place and the right time, with the right set of skills, knowledge and experience to solve a set of seemingly insurmountable problems with a unique set of solutions. Would anyone else have had the insight to smother a wafer with particles in a "dirty" polishing process if they

had not also had the requisite cleaning process in place? Maybe eventually someone might have, but certainly not at that time. We can thank Dr. Beyer's perseverance and unique set of skills for laying the ground work for a revolutionary process technology that has become an industry in itself. Dr. Beyer's talk was certainly the highlight of ICPT 2015.

The ICPT 2016 conference will be hosted by the CMP User's Group-China (CMPUG-CN) and held October 17-19 in Beijing, China, which will be another first for the event. Given the steady improvement in ICPT over its 12 years, many people are already looking forward to next year's event.

Biography

A. Scott Lawing received his BS and MS degrees from the U. of Rhode Island, and a PhD from the Massachusetts Institute of Technology. He is Technical Director at Kinik North America, and the Communications Chair for ICPT 2015; email slawing@kinikna.com

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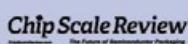
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