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The Future of Semiconductor Packaging

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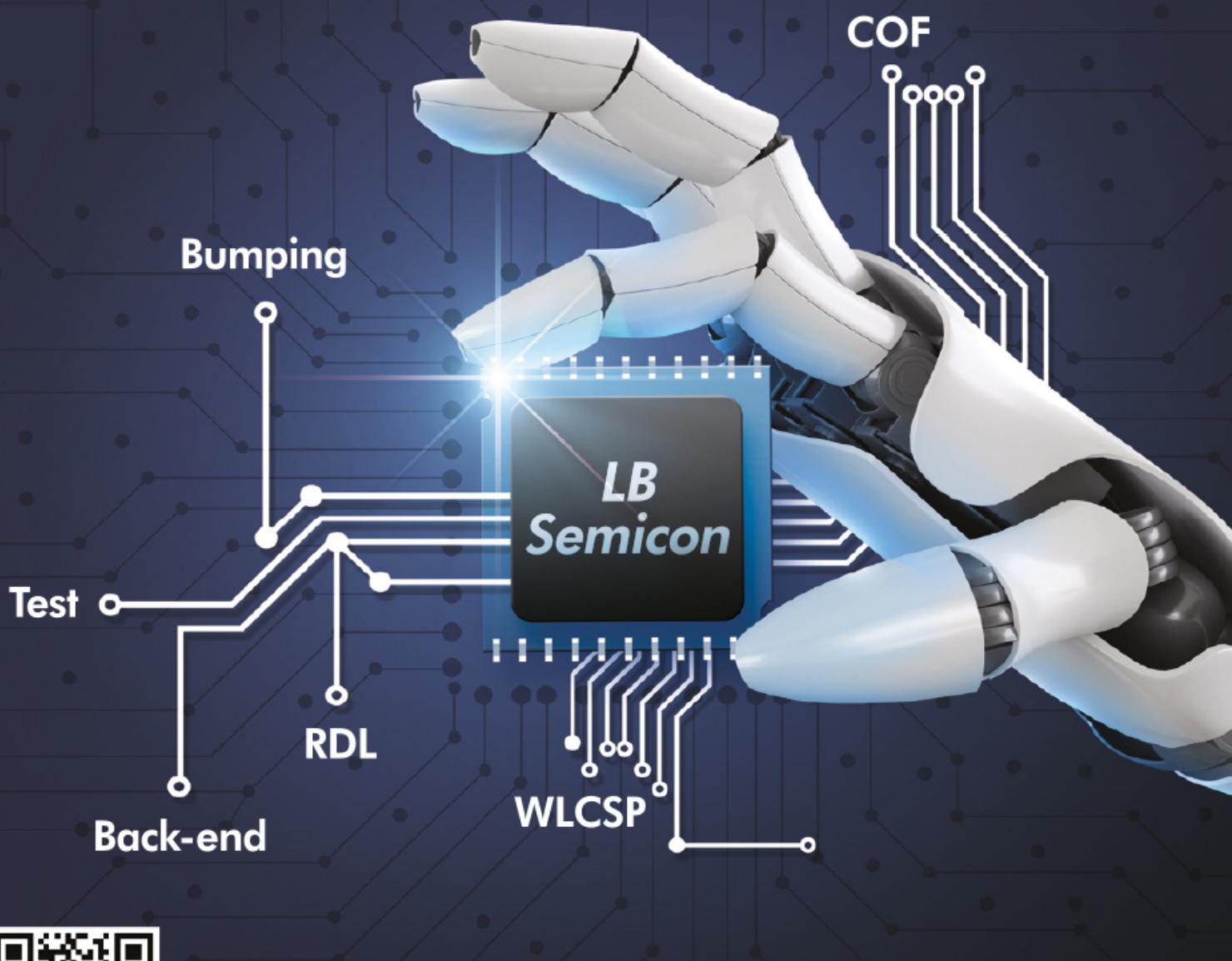
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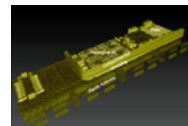
Wafer geometry is vital for process control at the front end of line, and ultimately, device yield. Additionally, as wafer thinning becomes ever more critical at the far back end of line, so too, is being able to quickly measure wafer geometry (e.g., nanotopography, roughness) on the entire wafer. Not only has wavefront phase imaging been shown to be a good candidate for FEOL and FBEOL applications, it is also showing promise for global wafer geometry measurements on patterned wafers during BEOL processes.

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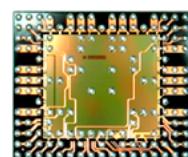
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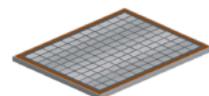


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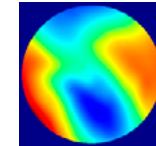
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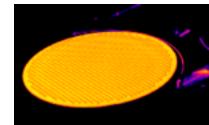
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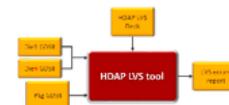
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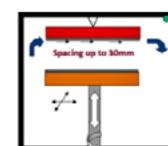
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Antenna in package (AiP): disrupting wireless communication and HMI

By Stéphane Elisabeth [[System Plus Consulting](#)], Cédric Malaquin [[Yole Développement](#)], both part of the Yole Group of Companies

Any wireless system requires antennas to convert the electric energy into radio waves traveling through the air. Whether it is for wireless sensing or broadband communication between at least two points, multiple types of antennas have been developed depending on the targeted application. Monopole, dipole, yagi, dish, patch, etc., are some of the existing configurations. Recently, a new type of system configuration, called antenna in package (AiP), has appeared and is becoming more and more popular, at least in the consumer market. In this article we will review the market drivers and the state of the art, as well as the market potential for AiP.

Advanced packaging: innovation for consumer connectivity apps

In the consumer market, the main technology deployed for cellular and Wi-Fi connectivity is based on relatively low frequencies, the so-called sub-6GHz frequency range. Because of the sparse and poor spectrum holding from network providers, complex technologies such as carrier aggregation and multiple-input multiple-output (MIMO) have been deployed to comply with the never-ending increasing demand for data consumption. In the meantime, RF board allocation has shrunk in the mobile handset because of restricted space with a larger battery size and new features added. This strategy has put pressure on RF front-end module makers and outsourced semiconductor assembly and test (OSAT) companies to develop very complex packaging technologies. An example of dense RF component integration is shown in [Figure 1](#).

The Apple iPhone® Xr features one or another module for dual-sourcing reasons (shown in [Figure 1](#)). Both modules are pin-to-pin compatible and include all necessary RF components: acoustic wave filters (in red), RF switches (in green), a power amplifier (in purple), a low-noise amplifier (in yellow) and a power management integrated circuit (PMIC) (in blue). Because

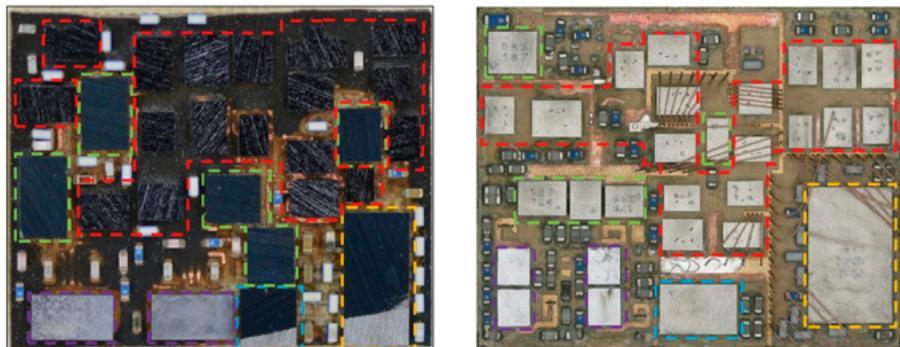


Figure 1: State of the art of the 4G and Sub-6 RF Layout; Qorvo QM76018 (left) [1] and Broadcom (AFEM-8092) (right) [2]. SOURCES: [1,2]

two different frequency domains (mid band and high band) are utilized in this device, complex electromagnetic interference (EMI) shielding techniques have been employed to isolate the different bands. In Qorvo's module, EMI shielding is using the package laminate substrate with a ground trace, whereas Broadcom uses grounded palladium-coated copper (PPC) wire bonded onto critical components to be protected. As RF component integration density is still increasing, the latest RF system-in-package (SiP) modules found in the Apple iPhone® 11 now come in double-sided ball grid array (BGA) packaging with EMI shielding [3]. For low-end smartphones, where cost is more important than the form factor, the mainstream packaging is SiP using long grid array (LGA) [4,5].

In fact, the iPhone® 11 still is an advanced LTE phone. With the 5G roll out, the densification trend of RF components in a mobile handset will extend to sub-6GHz frequencies. But the story is different for 5G mmWave applications. In the sub-6GHz world, antenna integration is not possible on account of the size and location of the antenna. Instead, antennas are connected to the modules with a coaxial cable, printed circuit board (PCB) or flex PCB. A basic requirement for the consumer market is that, whenever possible, antenna size needs to be shrunk down to comply with the stringent system integrator requirements. For sub-

6GHz frequencies, that means an antenna tuner is increasingly becoming a key component. At millimeter wave frequencies, however, AiP and antenna-on-package (AoP) comes into play. At millimeter-wave frequencies, antenna size reaches the RF integrated circuit's (RFIC) form factor. In addition, RF losses are such that integrating the antenna along with the RFIC is no longer an option, it is now mandatory.

5G mmWave has democratized AiP technology

AiP is a relatively new concept that has already made its way to the market. The most notable example is Samsung's flagship phone, the S10 5G commercialized in the US market for Verizon's 5G ultra-wideband (UWB) subscribers. The device currently supports 26, 28 and 39GHz bands thanks to the combination of a baseband processor (X50M) along with three AiP modules (QTM052) integrated into the phone case. Two generations of AiP have been used for this phone [6]. The first one, as shown in [Figure 2](#), features a PMIC, several passive components, and a transceiver on the bottom side of the PCB. The transceiver is connected to two types of antennas through the package laminate substrate. The first type of antenna consists of eight dipoles embedded in the layer of the laminate substrate and isolated from the transceiver by a compartment shielding.

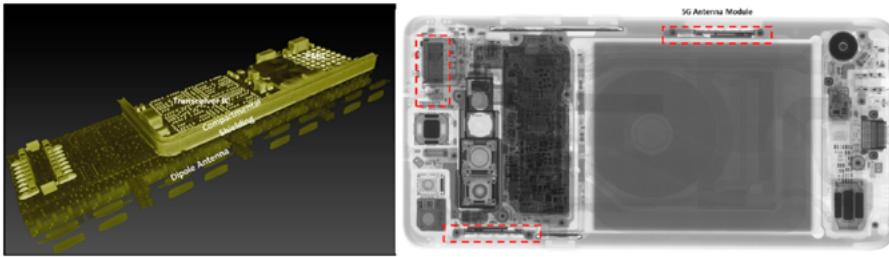


Figure 2: Tomographic imaging of the AiP module for 5G mmWave (left) and integration in the Samsung Galaxy S10 5G US (right).

The second type of antenna is made up of four dual-polarized antenna patches. The four patches are built on the top part of the laminate substrate. A complex routing from the transceiver down to these antennas through the package substrate ensures efficient radiation by the antennas for all the supported frequency bands.

The second generation of AiP has no dipole antenna. Indeed, the removal of the dipole area enabled a 20% form factor reduction, so it can be easily integrated into the phone case. The cost also has been reduced by 10%. To achieve this breakthrough technology, Qualcomm worked with its OSAT partners: Siliconware Precision Industries Co., Ltd. (SPIL) and Amkor Technology, Inc.

Verizon 5G UWB is a starting point and anticipates that other carriers will roll out 5G mmWave services worldwide. Therefore, the AiP market for mobile handsets is poised for substantial growth in the next five years [7] as depicted in **Figure 3**.

We can expect 5G mmWave AiP development will not only be of benefit to mobile phones, as it can also be found in

5G customer premises equipment (CPE) for fixed wireless access (Inseego, Netgear, etc.). It could also certainly extend to tablets and laptops soon. Previous attempts for AiP integration in consumer products had been made through the 60GHz WiGig technology, however with less emphasis than 5G. For the WiGig technology, Qualcomm co-developed with Murata a double-sided molding technology for the baseband processor, and created the first AiP device for a cell phone using a laminate substrate, a single mold, copper pillar, and through-molding vias (TMV) [8].

It's worth noting that system-on-chip (SoC) market leaders Qualcomm, Intel, HiSilicon, Samsung, and MediaTek, are paving the way for 5G mmWave AiP targeting the consumer market. The analog domain is investing in the RF world for such applications. Indeed, advanced technology nodes, such as 28nm CMOS, enable a good compromise between cost, size and performance for the transceiver, which also includes the RF front end in that case. The high cutoff frequency in the range of 250GHz makes this type of technology

suitable for a device operating at 28GHz or 39GHz. But the question mark remains on the device efficiency, as the power amplifier must drive enough power (15 to 20dBm) to comply with the device radiation power requirements. The antenna array is small (4x1 elements), therefore the gain is relatively low. We can expect innovation to solve this issue. In addition, mmWave AiP will also benefit from the roll out of high-density small cells that network providers must create to deliver the service.

AiP footprint to extend with radar-based HMI

AiP technology not only found application in the broadband communication use case, but also in wireless sensing. Infineon and Google set the stage with a human-machine interface (HMI) feature based on radar sensing through the Soli project [9]. The two companies joined forces to include a revolutionary gesture control system based on radar sensing in a flagship phone for the first time. Indeed, the Pixel 4 is equipped with an AiP radar sensor beside the front camera module, as shown in **Figure 4**.

The 60GHz broadband radar technology measures velocity and distance from objects in the millimeter range, while the power consumption is in the milliwatt range. Motion sensing is then converted into wireless control functions thanks to machine learning. This technology could extend far beyond the mobile phone throughout the consumer market, for instance in TV sets, gaming, smartwatches, headsets, etc., for which a camera-based HMI is less applicable than a radar-based one.

AiP: industrial, automotive and medical

The consumer market is not the only one in which AiP technology can apply. Indeed, it also makes sense in industrial applications such as building automation, factory automation, traffic monitoring, and so forth. For example, a tiny radar sensor with integrated antennas could easily be included in a light pole for vehicle counting, thereby helping in optimizing traffic management. The same concept could also apply for automatic door opening, counting people in buildings, and detecting their presence. Radar sensing has some technical advantages to compete with legacy imaging and infrared technologies, but the form factor and the overall system cost could not

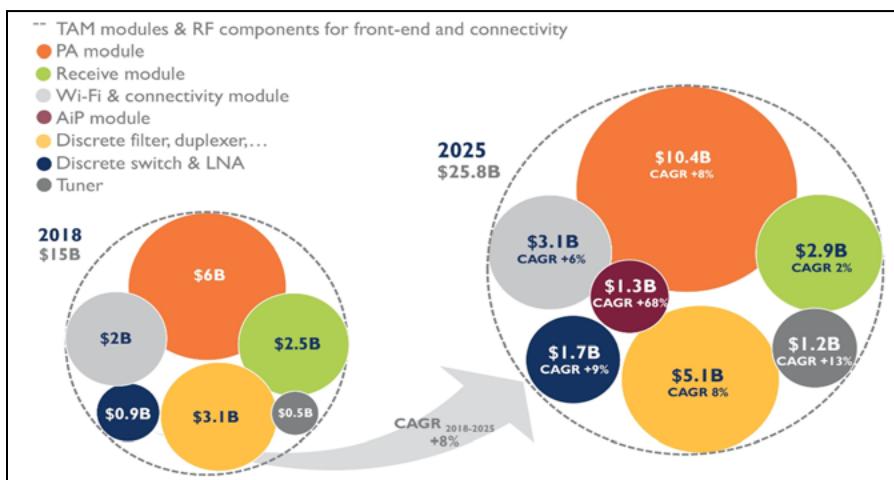


Figure 3: RF Front end market forecast for mobile handset – new market opportunities for AiP. SOURCE: [7]

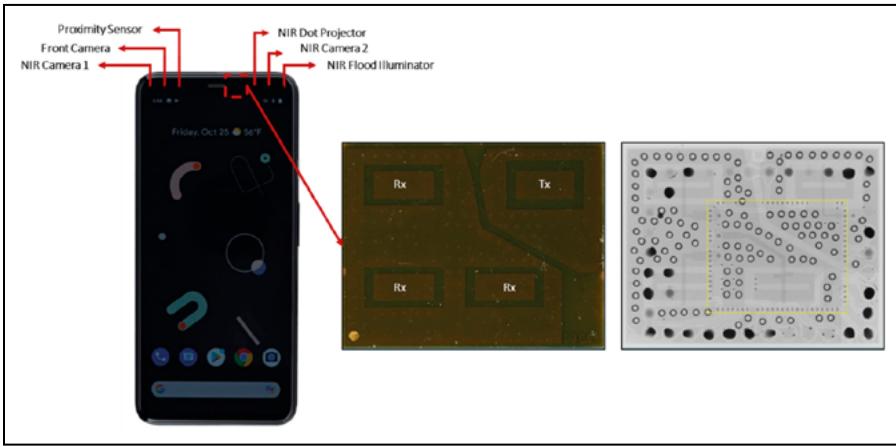


Figure 4: R. AiP From Google/Infineon for HMI feature integrated in the Google Pixel 4 XL. SOURCE: [9]

conform with the requirements of these types of applications so far. Now, however, AiP technology is maturing and it is becoming possible to shrink the size of the sensor and to reduce the cost to levels acceptable to the industrial market. And that's exactly what the current market leaders, such as Infineon or Texas Instruments, are doing. Both players are working on radar sensors with integrated antenna in the package targeting these applications.

The status is quite different in the automotive industry. Radar-based sensors have been a legacy technology since the beginning. The progressive transition from 24GHz to 77GHz helped in reducing the sensor size, but further scaling of the sensor is difficult on account of the wide antenna aperture required for high resolution and long range at the same time. AiP has therefore not penetrated this market so far.

A potential use case for automotive radar AiP would be the replacement of ultrasonic sensors for highly automated valet parking features as the range is less of a concern for this application. A typical range requirement for this application is below 10 meters, which makes small antenna design possible. Because the quarter wavelength at the operating frequency of 79GHz is in the millimeter range, it's interesting to integrate antennas with the RFIC, and it's even more interesting if the signal processing is embedded in the RFIC because it would remove the need for an external microcontroller unit (MCU). This approach has been followed by Texas Instruments, among other companies. In addition, the sensor could be hidden behind bumpers, thereby improving the car design. So far, this type of solution has not been adopted

because of the significantly higher cost. The Texas Instruments AoP radar costs around 50% more than its counterpart without an integrated antenna [10]. A cost breakdown analysis, as shown in **Figure 5**, highlights the fact that the main extra cost share is at the packaging level. The penetration rate of such a device will be strongly linked to the capability of companies involved to reduce the cost, unless it brings added value for safety or enables a new functionality, such as a secure and automated trunk opener to be implemented.

Other applications in the automotive space are driver monitoring, in-cabin occupancy detection, as well as a health monitoring system. A child presence detection system is already mandatory in Italy and will be required elsewhere soon, opening opportunities for radar AiP to enter the automotive market.

Finally, it's worth noting that multiple research projects in medical focus on noninvasive health monitoring with radar technology. Whether AiP will benefit from future product development will depend on the frequency that is used. Beyond 100GHz, interconnects become a limiting factor and it is more interesting to integrate the antenna directly onto the chip. As an example, imec developed a vital sign monitoring concept based on a 140GHz radar with an on-chip antenna configuration, thereby removing interconnect losses. In addition, the medical device market is quite difficult to penetrate as it requires FDA or CE approval.

Summary

Mm-wave AiP found a good fit in the consumer market both for 5G mobile broadband and gesture recognition HMI applications. The market penetration will be governed by regulation policies: 5G mmWave is only available to a fraction of the U.S. market at the moment and the 60GHz unlicensed band cannot be used worldwide. Attempts to translate the AiP concept into the automotive, industrial and medical markets are underway. However, the entry barrier is high for automotive and medical because product qualification cycles are far longer.

Acknowledgments

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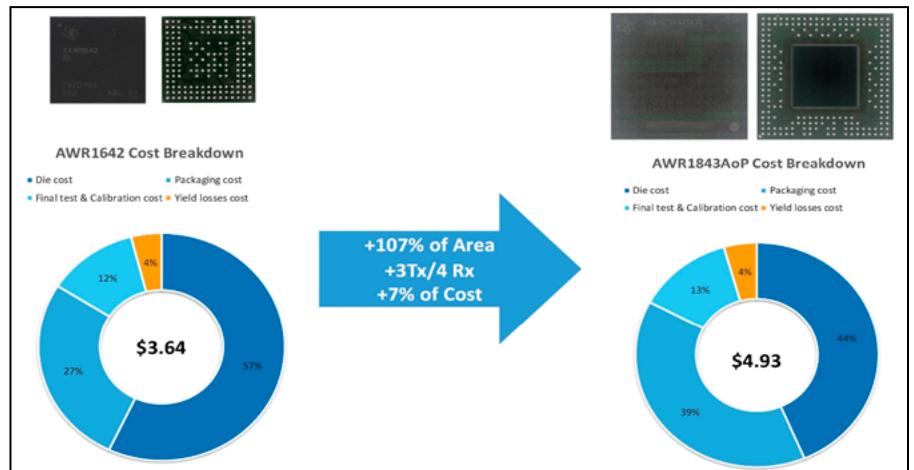


Figure 5: AiP From Texas Instruments for automotive (right) with cost comparison with stand alone version (left). SOURCE: [10]

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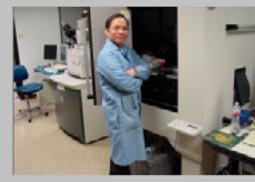


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	2) FEI Strata 400S FIB/SEM/STEM
Global Isolations	1) Hamamatsu PHEMOS1000 ENMMI and OBIRCH
	2) Quantum Focus Thermal Hot spot, IR mapping, and TIVA
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Reliability and performance of wafer-level fan-out packaging for automotive radar

By Walter Hartner, Martin Niessner, Francesca Arcioni, Markus Fink, Christian Geissler, Gerhard Haubner, Maciej Wojnowski [Infineon Technologies AG]

Automotive radar technology at 77GHz for advanced driver assistance systems (ADAS) and autonomous driving requires a package solution, which provides both superior RF performance and fulfills the strict automotive reliability requirements. In the past, the automotive industry used predominantly very mature semiconductors and packages. Today, however, a car will need to use the latest packaging technology to provide the best solution for ADAS sensors. One example of this trend is the embedded wafer-level ball grid array (eWLB) package. Infineon was the first company to introduce the eWLB package technology to the automotive market in 2012 [1], only three years after introducing this technology to the consumer market [2].

Characteristic to eWLB package technology is the signal routing directly on top of the silicon device and package body by using thin dielectric layers for electrical insulation and thin copper film layers for electrical redistribution. These characteristics offer low parasitic inductances, shorter signal pathways, and together with more freedom in designing the layout of the redistribution layers (RDL), they provide an excellent RF transition. Frontend Si-technologies and processes became standard for this backend package technology. Today, this low-cost wafer-level eWLB packaging solution with its attractive RF performance is now used in our second-generation automotive radar technologies and is also widely used by others for many automotive radar systems at 77GHz.

In the following sections, we describe how the eWLB technology fulfills the demanding performance and reliability requirements of automotive radar sensors. Three important topics will be addressed: 1) Thermomechanical behavior (i.e.,

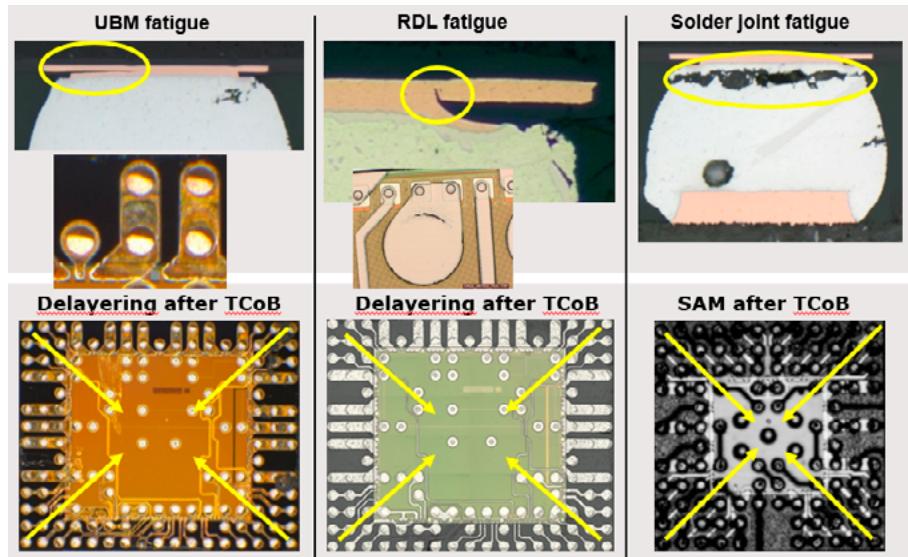


Figure 1: Typical fatigue modes evolving during TCoB cycling to release thermomechanical stress, and its radial orientation with respect to the package center.

what drives thermo-mechanical lifetime behavior and what fatigue modes do we have?); 2) RF performance (what will impact the RF-performance?); and 3) Thermal performance (how to set up thermal management and what will change thermal behavior?).

Thermomechanical behavior

The eWLB package with its short interconnection means there is no material layer at the package side that is able to buffer any coefficient of thermal expansion (CTE) mismatch. The solder balls are exposed to the full CTE mismatch between the printed circuit board (PCB) and the eWLB's main components (silicon and molding compound).

Cross sections of typical fatigue modes are shown in the upper part of **Figure 1**. Under bump metallization (UBM) fatigue, RDL fatigue and solder ball fatigue evolve during temperature cycling on board (TCoB) to release thermomechanical

stress. In addition to the 2D analysis of the fatigue modes, new analysis techniques have been developed to investigate the 3D orientation across the entire package (see lower portion of **Figure 1**). Scanning acoustic microscopy (SAM) and new delayering methods are applied to reveal the solder ball fatigue and the UBM-RDL interfaces, respectively. For all fatigue modes, the orientation of the fatigue modes is radial from the edge of the package to the center.

With trends like increased die or package size and the demand to withstand a higher number of cycles on thicker or stiffer board stacks, several measures of the eWLB technology are needed in order to improve the TCoB robustness. In **Figure 2**, a few examples of those measures are listed and rated.

Besides introducing underfill or corner bond, reducing the size or adding redundant balls have the most positive effect on TCoB. The min/max temperature

difference used for cycling also has a big impact on TCoB. A ball's size, as well as the composition of the balls are of great importance for increasing the TCoB robustness. By adjusting the package thickness, only a minor impact is seen. On the other hand, choosing the wrong RF board-sheet or -stack, may have one of the biggest impacts on reducing the TCoB reliability. The type of RF laminate used with the hybrid PCB is one of the major factors determining the solder joint lifetime [3,4]. For setting up the application system, attention must be paid to the TCoB differences of a free test board compared to a PCB within a real system housing. Solder mask defined (SMD) pads on board versus non-solder mask defined (NSMD) pads typically yield lower numbers for TCoB cycling. Finally, yet importantly, introducing UBM shows a major advantage compared to solutions without a UBM layer. For all possible measures, the consistency of the fatigue modes always has to be studied and verified.

For analyzing UBM fatigue, the loading at the liner interface is investigated using thermomechanical finite element simulation. The highest tensile normal loading is at low temperature, which is reasonable because the solder material of the balls creeps less with lower temperature allowing for higher elastic stresses at lower temperature. On account of the tilt of the solder balls, the tensile normal stresses are located at the side of the interface oriented towards the perimeter of the package (**Figure 3**). This finding correlates with experimental results from delayering (**Figure 1**).

For understanding RDL fatigue, the RDL layer is included in the simulation model and the first principal stress in the copper is investigated. As seen with the UBM fatigue, the highest RDL stress loading occurs at low temperature and at the sides of the tear drops oriented towards the perimeter of the package (see **Figure 4**). Furthermore, the stress on the RDL is higher for wider RDL connections. This finding correlates with experimental results (**Figure 1**).

Solder fatigue is analyzed by calculating the accumulated strain increment. This describes the amount of inelastic work done on the solder material per cycle (referred to as "damage parameter"). The higher the damage parameter, the earlier the solder balls

	lower	Thermo-mechanical performance (TCoB)			higher
Underfill/CB		w/o			
Package size& redundancy	x1,0 no red.	x0,9 2-fold	x1,0 2/3-fold	x0,6 no red.	x1,1 3-fold
ΔTemp.	ΔT=190K	ΔT=165K			ΔT=125K
Ball size	x0,8	x1,0			x1,2
UBM+alloy-ball		UBM + SAC ball		alloy-ball	
Package thickness		x1,0	x0,5		
w/o UBM+ alloy-ball					
w/o UBM	w/o UBM	w/ UBM			
Board housing	with housing	free board			
SMD on board	SMD	NSMD			
RF board material	C	B	A		

Figure 2: Overview of typical TCoB characteristics.

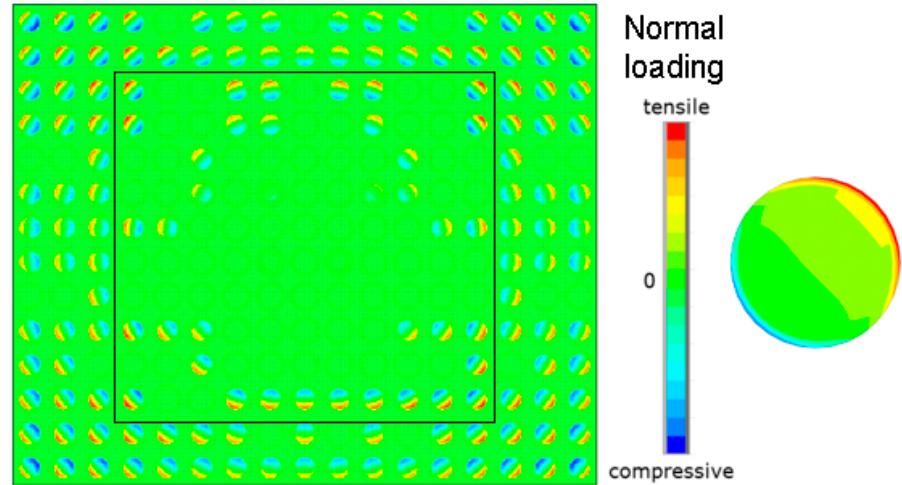


Figure 3: UBM loading analysis plot showing a view of the normal loading at the liner interfaces across the package at -40°C. Tensile stresses (in red) are located at the side of the interface oriented towards the perimeter of the package. At the right of the plot is a close-up view of a single interface (at a different scale).

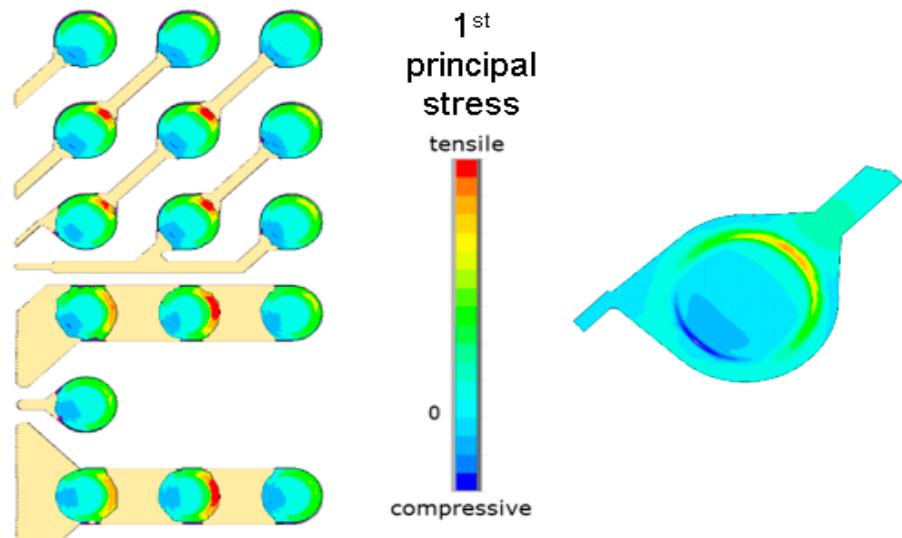


Figure 4: RDL loading analysis plot. The left side of the plot shows the first principal stress in the RDL layer for a part of the package at -40°C. Tensile stresses (in red) are located at the side of the RDL layer oriented towards the perimeter of the package. The right side of the figure shows a close-up view of a single tear drop (at a different scale).

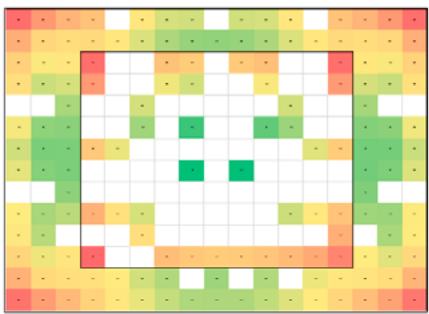


Figure 5: A heat map showing the distribution of the damage parameter across the package with respect to solder loading. Red indicates high loading and green indicates low loading.

will fail, and vice versa. The heat map in **Figure 5** shows the distribution of the damage parameter across the package:

- The damage is high at the balls located at the package corner. This is because the corners have the maximum distance to the package center and, therefore, have the highest thermal strain mismatch.
- The damage is high below the perimeter of the silicon chip and especially below the chip corners. This is because the silicon chip is considerably stiffer than the molding compound and has a lower CTE resulting in high damage loading similar to the level near the package corners.

In general, the findings discussed above are in agreement with results from cross sections of devices after solder joint reliability experiments. To evaluate whether a respective fatigue mode is able to cause end-of-life of the assembly or not, the “driving force” of each fatigue mode is analyzed as listed in **Table 1**.

Because the magnitude of all three driving forces depends on the geometry and the material parameters of the assembly, simulation is used to analyze how the magnitudes change with increasing levels of fatigue, i.e., opened UBM interface area, length of RDL, and solder ball crack. As a result, detailed sub-modeling of a ball at a selected location of the package is done and

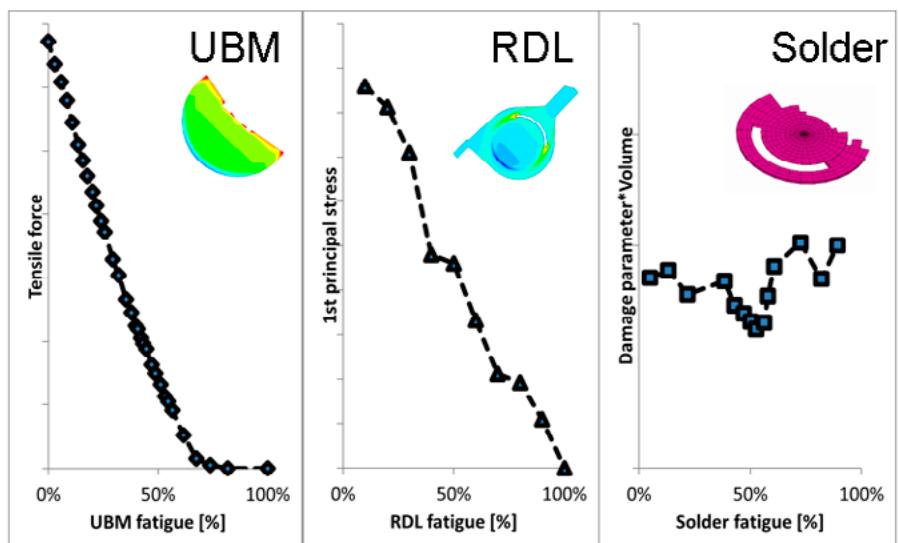


Figure 6: Plots showing the driving force of each mode versus its fatigue level. Only one fatigue mode is considered in each simulation.

combined with a script, which subsequently changes the respective fatigue level. Separate simulations are done for each fatigue mode.

The results of the analysis show that the driving forces of both UBM fatigue and RDL fatigue reduce with increasing levels of fatigue (see **Figure 6**). This is because the assembly of package and ball gets more compliant with an increased level of fatigue. The reduced forces may eventually no longer be able to drive the UBM and RDL fatigue modes when dropping below the critical values needed to propagate the fatigue. Consequently, neither the UBM nor the RDL fatigue mode may cause end-of-life of the assembly for the investigated loading.

The solder fatigue mode shows a different behavior: The driving force does not reduce with increasing fatigue level, but remains constant, and/or increases. The interpretation is that solder fatigue will always continue and eventually cause end-of-life of the assembly.

RF performance

Electromagnetic (EM) simulation is used to optimize the chip-package-board transitions, to increase system efficiency, or to evaluate different use cases, which cannot be easily produced or measured. The last one is the case for evaluating the RF performance for different fatigue levels as described above.

RF characterization and optimization are performed using the ANSYS HFSS full-wave EM simulator that solves the full system of Maxwell equations. RF

performance of transitions is evaluated using scattering parameters (S-parameters). The S-parameter matrix is a frequency-dependent matrix that relates reflected and transmitted EM waves. This description takes into account all EM phenomena and interactions inside the simulated 3D structure. In particular, the return loss on board and chip side (S_{11} , S_{22}), and insertion loss (S_{21}), are important parameters, which need to be characterized and optimized.

To evaluate the impact of the fatigue on RF performance, RDL, UBM, and solder ball fatigue modes are evaluated. Simulation results show that fatigue modes have negligible impact on levels of return and insertion loss independently from fatigue modes and their extent. Because of different surface current distributions in the case of fatigue modes, the electrical length of the transitions may slightly change. In **Figure 7**, the surface current distribution is shown for two RF transitions. The left side of the figure shows results without any fatigue, and the right side of the figure shows RDL,

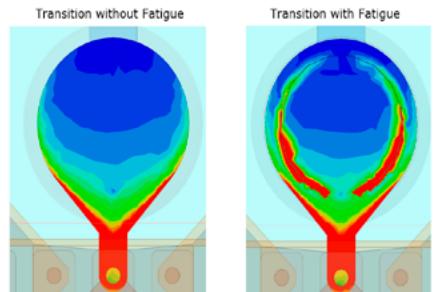


Figure 7: Surface current distribution without, and with RDL, UBM, and solder ball fatigue.

Table 1: Fatigue modes and their driving force.

Fatigue mode	Driving force
UBM fatigue	Tensile normal force at interface
RDL fatigue	Tensile 1 st principal stress
Solder fatigue	Damage parameter



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UBM and solder ball fatigue. This slightly different electrical length will cause a small difference in phase $\Phi(S21)$ of the insertion loss, which is undesirable in radar applications. It is therefore important to demonstrate that none of the fatigue modes and their combinations lead to a phase shift exceeding the specified limit.

In **Figure 8**, the effects of each single fatigue mode (RDL, UBM, and solder ball fatigue) and two combinations of them are summarized. The phase shift $\Delta\Phi(S21)$ is evaluated against the reference of an RF transition without fatigue. For fatigue levels up to 90%, the phase shift stays within specification (the white area in **Figure 8**) considering RDL, UBM, and solder ball fatigue separately. Also, the combination of up to 90% of RDL plus UBM fatigue results indicate acceptable phase shift. Only for an unlikely mix of all three fatigue modes with 90% RDL, UBM, and solder ball fatigue,

shift caused by fatigue will eventually be less than the specified limit.

Thermal performance

Typical power consumptions for automotive monolithic microwave integrated circuits (MMICs) are in the range of 1-3W. To remove the heat associated with this power consumption, the thermal resistance of the MMICs must be sufficiently low in order not to exceed typical thermal boundary conditions (e.g., 85°C for the sensor ambient temperature, and 125°C for the Si chip bulk temperature). Therefore, the heat must be conducted via the solder balls to the metal layers on the PCB, which are connected thermally to the sensor housing.

To improve heat dissipation, thermal balls have been implemented in the MMIC design. These thermal balls are located in areas of the Si chip that are not critical for

the RF functionality. To achieve a low thermal resistance from the balls to the Si chip, metal – as much as possible – is used in the semiconductor back end of line (BEOL) stack in the area of the thermal balls. Thermal simulation shows that the thermal balls on the silicon chip area are very effective and conduct almost 70% of the generated heat. Balls located on the fan-out area of the package are not very effective in lateral heat transfer on account of the long distance from the silicon chip to the solder balls and the limited

thickness of the Cu RDL redistribution layer (**Figure 9**).

One might ask, “How do thermal measurements fit to the thermal simulations, and how does the thermal behavior change over the lifetime of the package?” Temperature-driven fatigue modes as described above, are leading to a loss in contact area, and as a consequence, to an increase of temperature and thermal resistance (R_{TH}). An assessment of that fatigue behavior on thermal performance is done by simulation. Thermal simulation and optimization are done via steady state thermal simulations with the ANSYS V19.1 software tool.

The thermal performance, or response, for different use cases is plotted in **Figure 10**. The corresponding use cases with different degradation or fatigue levels of the balls are shown in **Figure 11**. Assuming 50% degradation on average for all thermal balls, an increase in R_{TH} of up to about 30% is seen. However, not all thermal balls are located at critical TCoB positions like the die edge. Therefore, R_{TH} change will be typically less than 30%.

Summary

Typical fatigue modes after TCoB are solder ball fatigue, UBM fatigue, and RDL fatigue. Both standard and new analysis methods reveal that all fatigue modes are oriented radially from the edge of the package to the center. Typical measures to improve the TCoB robustness for the eWLB technology were listed and rated. The UBM, RDL and solder fatigue modes were analyzed using thermomechanical finite element simulation. The results show that the driving forces of both UBM fatigue and RDL fatigue reduce with increasing level of fatigue and do not cause an end-of-

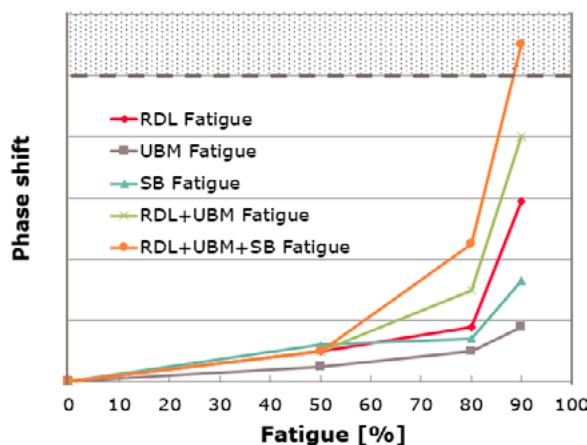


Figure 8: A plot of phase shift vs. fatigue for single fatigue modes (RDL, UBM and solder ball fatigue), for RDL + UBM-fatigue, and for RDL + UBM + solder-ball-fatigue.

the phase shift may exceed the specification limit (the gray area in Figure 8). The case of more than 90% fatigue (e.g., 100%) does not need to be considered because 100% will cause an electrical DC open. Reliability testing for an electrical DC open is done by standard TCoB testing, which needs to fulfill the customer-specific TCoB requirement anyway.

In summary, possible phase shifts of the specified limit have to be applied to the tolerances by setting up the system. The RF ports, however, are not located at critical TCoB positions such as package or die corners, and therefore, have significantly less than 90% fatigue. This is why the phase

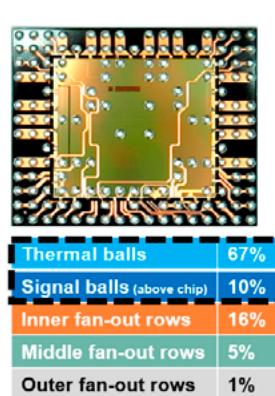


Figure 9: Contribution of each solder ball to the overall heat dissipation for a typical eWLB radar package.

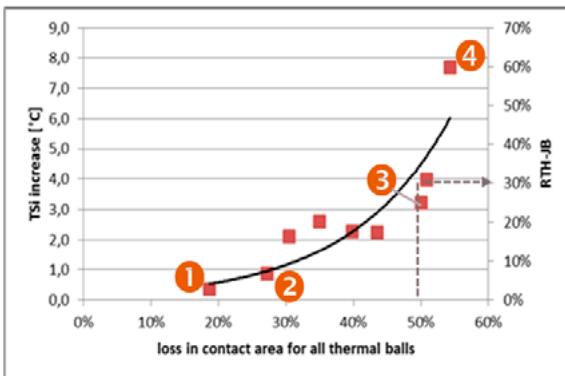


Figure 10: Thermal simulation results for various use cases as shown in Figure 11 for a power consumption of about 3.3W.

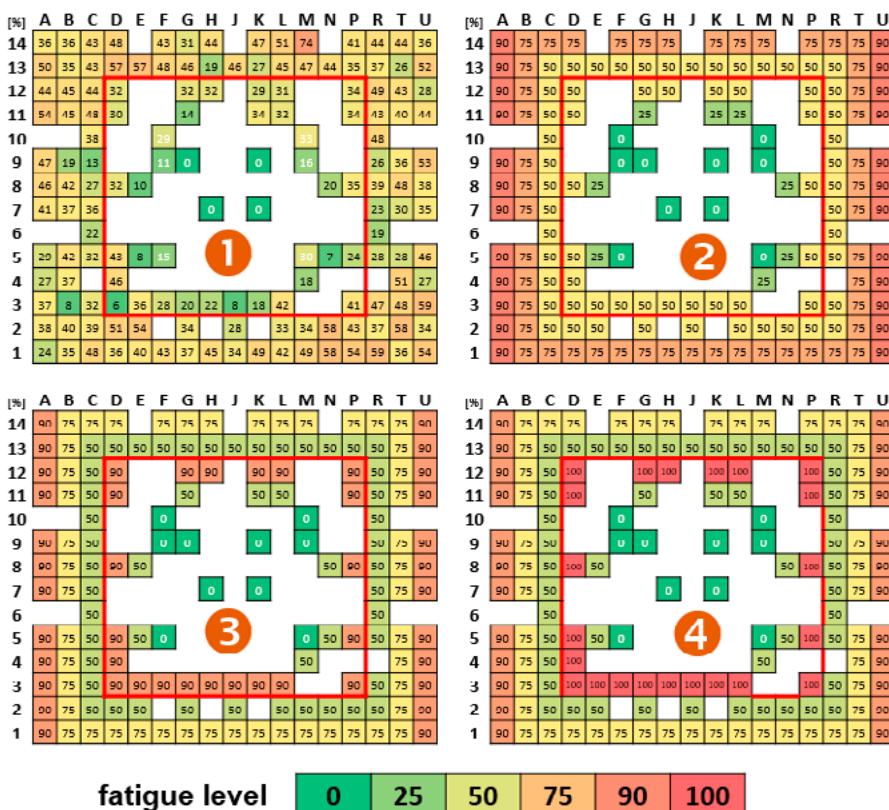


Figure 11: Various use cases 1-4 with different fatigue levels of the balls showing an assessment of the thermal behavior of the package.



Biographies

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life failure. For solder fatigue, the driving force does not reduce, but remains constant and eventually causes an end-of-life failure.

For evaluating the fatigue modes on the RF performance, the phase shift on the RF transmission $\Phi(S21)$ was analyzed. For fatigue levels up to 90%, the phase shift stays within the specified limit considering RDL, UBM, and solder ball fatigue separately.

Thermal simulation shows that the thermal balls on the silicon chip area are very effective and dissipate almost 70% of the generated heat. For assessing several different use cases with a different level of fatigue for each ball position across the package ball out, thermal simulation shows that, for example, assuming 50% degradation on average for all thermal balls, an increase in RTH of up to about 30% is seen.

Acknowledgment

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Overcoming FOPLP die placement error

By Keith Best *[Onto Innovation]*

It is well understood that advanced packaging applications require high performance, low cost, increased functionality and improved reliability that 2.5D and 3D packaging solutions provide. Fan-out panel-level packaging (FOPLP) is one of the technologies that has the potential to meet these packaging requirements. Similar to fan-out wafer-level packaging (FOWLP), FOPLP processes reconstitute die on a substrate, in this case a rectangular platform that can be significantly larger than the standard 300mm diameter wafer form. In the reconstitution process, die are displaced from their nominal grid locations during the epoxy molding compound process and sometimes during subsequent processing steps. This fan-out technology delivers more space for redistributed I/O connections, providing increased flexibility for homogeneous and heterogeneous integration. Importantly, the larger panel format can support more packages per substrate than the 300mm wafer form, and the final package size can be increased by adding space between the die.

Although FOPLP processing has many advantages, it also faces significant challenges. One critical challenge is die placement error, which occurs when die are positioned during the reconstitution and molding process. These placement errors are amplified with the larger panel format when compared to reconstituted wafers, and errors of 50 μ m or more are not unusual. In order to guarantee acceptable yield, these errors must be corrected during the lithography process using site-by-site corrections. Conducting metrology and site-by-site exposures on the lithography system is very time consuming. Substrate alignment and error correction may be calculated using global alignment, but this correction does not accommodate nonlinear die placement errors. It has become clear that only site-by-site corrections can deliver the overlay required to maintain good yield. Executing site-by-site alignments in the stepper reduces throughput and increases cost enough to make that approach to FOPLP processes impractical. A new approach uses an external metrology

tool to capture die placement error data from a panel and feeds that information forward. The “feed-forward” solution optimizes the stepper, site-by-site, for X, Y and rotation offsets, during exposure. Visualization of the metrology data allows the user to characterize upstream and downstream processes. Moreover, analytical capabilities predict yield as a function of exposure field size, thereby allowing the user to balance throughput against yield in real time. This solution can significantly increase stepper throughput, reduce cost and increase productivity while ensuring high yield.

Die placement challenges

Generating reconstituted panel substrates creates translational and rotational die placement errors. The “pick and place” process itself introduces initial errors that are exacerbated during the mold process, and by instability of the mold compound throughout repeated processing cycles. With redistribution layer (RDL) features currently achieving dimensions as small as 2 μ m, die

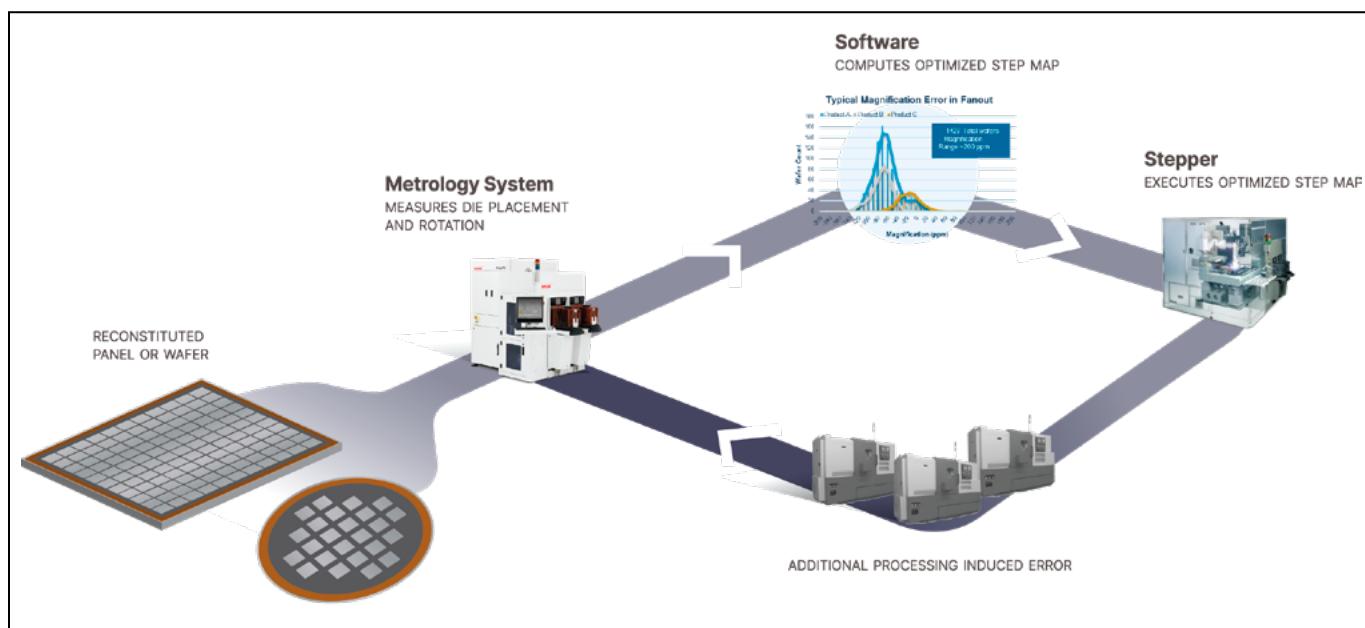


Figure 1: The optimized stepping process loop includes: 1) measurement of die displacement errors outside the stepper; 2) Site correction calculations/yield modeling; and 3) exposure.

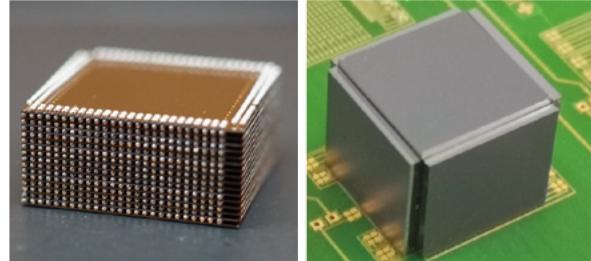
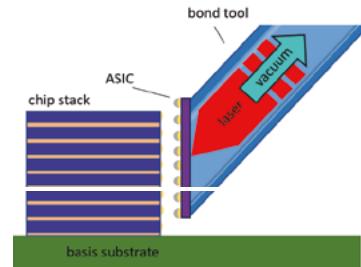


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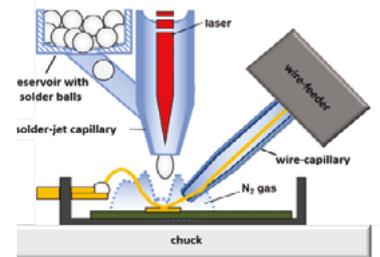
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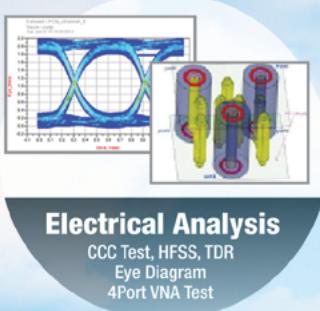
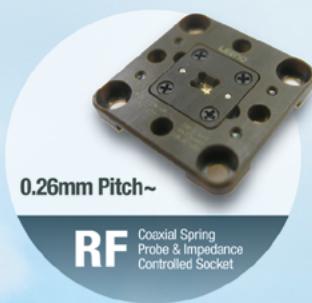


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placement measurements and pattern overlay registration requirements are continuing to tighten. As a result, the position of the die must be measured before each exposure in the lithography system to ensure accurate registration with the underlying layer. Displacement errors can be measured in the lithography tool, but these measurements are slow, typically taking as much time as the exposure itself. Transferring the measurement operation to a parallel, independent metrology system and feeding corrections to the stepper, however, can double throughput. **Figure 1** illustrates the use of this exposure/measurement loop to increase productivity. The die placement measurements and analysis can be repeated, if required, after each layer is exposed, to correct for any errors introduced in that step. In addition to feed-forward corrections, the software algorithm analyzes the displacement errors to predict yield (based on a user designated limit for acceptable registration error) for exposure fields of varying sizes. The method requires tight integration of the stepper and measurement system with the controlling software algorithm.

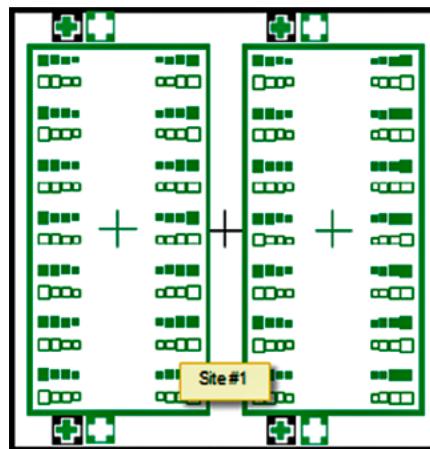


Figure 2: Pad test pattern showing two die.

same method as the wafer study. The test reticle used a single die “Pad” image, which was patterned across the entire panel. The pad test pattern (**Figure 2**), with no offsets, was then measured using the stepper and AOI system at two points per die (top and bottom).

The lithography system (JetStep System, Onto Innovation) supports panel sizes up to 720mm x 600mm.

It uses pattern recognition alignment, allowing the user to train the system to recognize and align on any unique pattern within the field of view. The alignment system can measure the X, Y position of die patterns across the panel, a process often referred to as “mapping.” The AOI system (Firefly System, Onto Innovation) uses a similar pattern recognition alignment method to assess die placement error. Using the stepper and AOI alignment site measurements from the test vehicle panel, a mathematical algorithm was applied to align the stepper and AOI coordinate systems. Once a common grid coordinate system was established, the stepper stage was considered as the reference and the AOI system was compared to this reference using simple scatter plots (**Figure 3**). The measurements were repeated three times to confirm repeatability. In all three cases, accuracy of the AOI system was within +/-2.3 μ m of the stepper reference. **Figure 4** shows histograms of the dX and dY distributions for R1. **Table 1** summarizes the statistical data for each run.

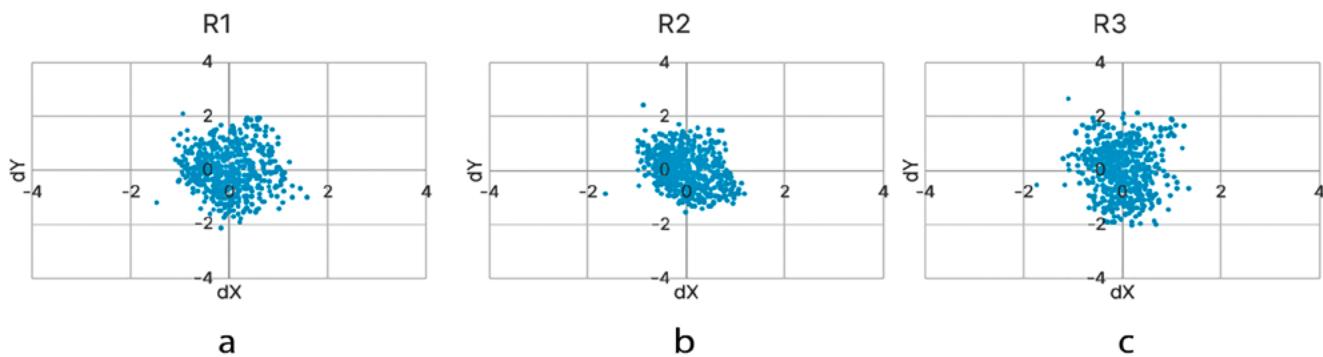


Figure 3: Scatter plots stepper vs. AOI, for three runs: a) R1, b) R2, c) R3.

Coordinate systems; measurement accuracy

A previous study [1] looked at wafer substrates and focused on proving that automated optical inspection (AOI) feed-forward data could correct for the predefined die placement offsets. It established the AOI feed-forward accuracy to be within +/-2 μ m. The work described below uses a 510mm x 515mm x 1.1mm rectangular glass panel as the test vehicle to match the stepper and AOI panel stage grids and measure the AOI accuracy. The test panel was patterned using the

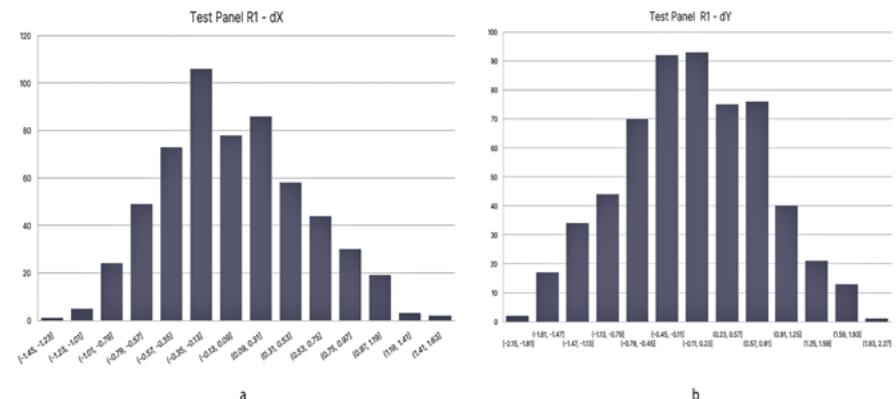


Figure 4: Test vehicle AOI error distributions R1 for a) dX, and b) dY.

R1	MEAN	MIN	MAX	RANGE	STD
dx	3.9E-08	-1.4487	1.5897	3.0385	0.5174
dy	8.9E-08	-2.1498	2.0835	4.2334	0.8043

R2	MEAN	MIN	MAX	RANGE	STD
dx	4.5E-06	-1.6298	1.1914	2.821	0.4670
dy	4.2E-07	-1.5700	2.4130	3.9831	0.6828

R3	MEAN	MIN	MAX	RANGE	STD
dx	-2.3E-07	-1.7213	1.3792	3.1005	0.4412
dy	-1.9E-08	-2.0548	2.6228	4.6776	0.9118

Table 1: Summary of dX, dY error statistics for R1, R2, R3.

Die placement error measurement

With the accuracy of the measurements and the correspondence between the exposure and measurement coordinate systems established, it is possible to evaluate the placement errors of die on FOPLP panels. Dummy die embedded in molding compound to form a FOPLP substrate were supplied courtesy of ESWIN. Measurements of two points for every die, top and bottom, allowed the system to calculate translation (X,Y) and rotation (Θ) offsets for each. The software algorithm generates

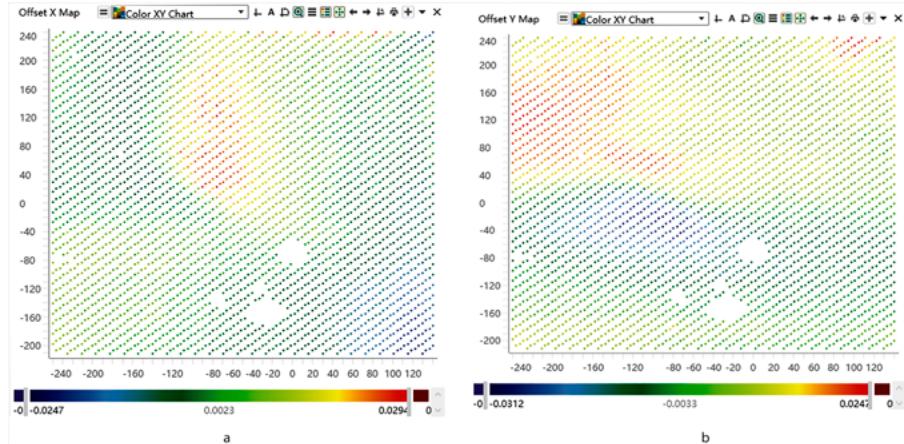
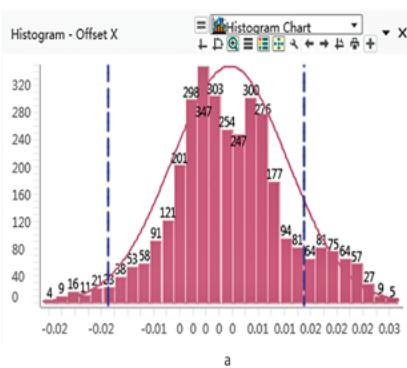


Figure 5: Die placement error (mm) a) dX, and b) dY heat maps.

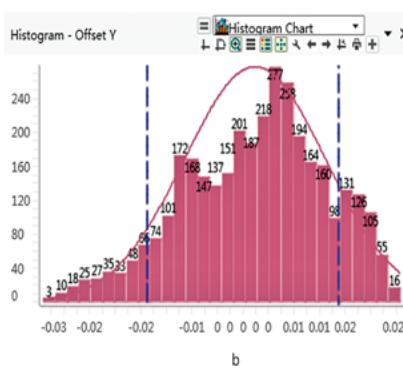
processing. The disruptive EMC curing effect renders the typical global alignment solution used by lithography tools useless, as it assumes linear corrections for scaling, rotation, orthogonality. Only site-by-site corrections can accommodate these types of errors. To apply site-by-site corrections, each exposure needs to be matched to the local errors to provide good overlay.

Data analysis, yield prediction and throughput

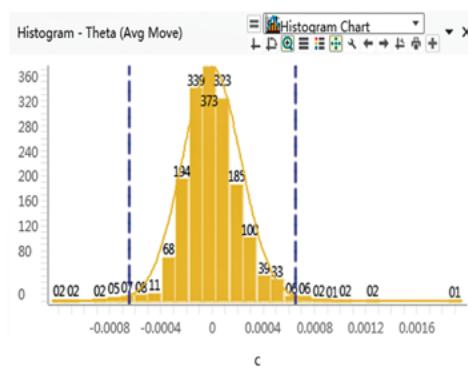
The process specifies overlay errors less than $\pm 15\mu m$. As long as the measured errors are within the correction capability of the stepper, it is possible to yield 100% by correcting each die, so called “die-by-die” exposure individually, but this imposes an unacceptable penalty on stepper throughput. Increasing the size of the exposure to cover multiple die will



a



b

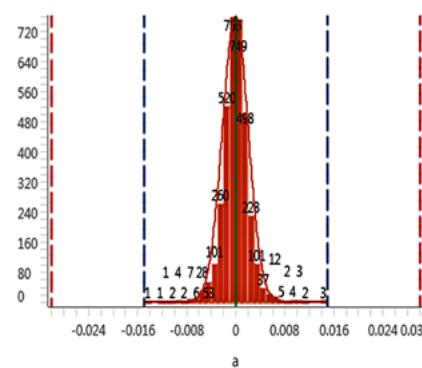


c

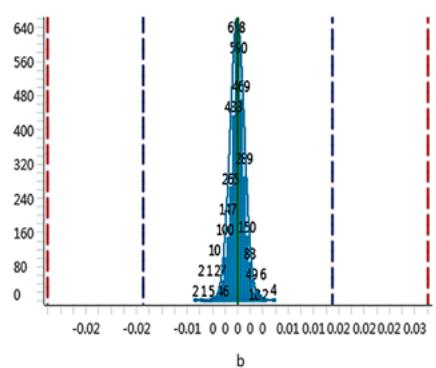
Figure 6: a) dX (mm), b) dY (mm), and c) rotation (rad) data histograms.

“heat maps” that visualize the dummy measurements before corrections are applied (Figure 5). Histograms of the X and Y placement errors and rotational errors (Figure 6) show the distributions of these measurements.

The multimodal distributions of the dX and dY histograms reflect the nonlinear die placement errors observed in the heat maps. This nonlinear error can be attributed to the epoxy molding compound (EMC) curing process, which is typical for most FOPLP reconstituted panel



a



b

Figure 7: Predicted a) dX and b) dY overlay data histogram (mm) for 3 X 3 field, 100% yield.

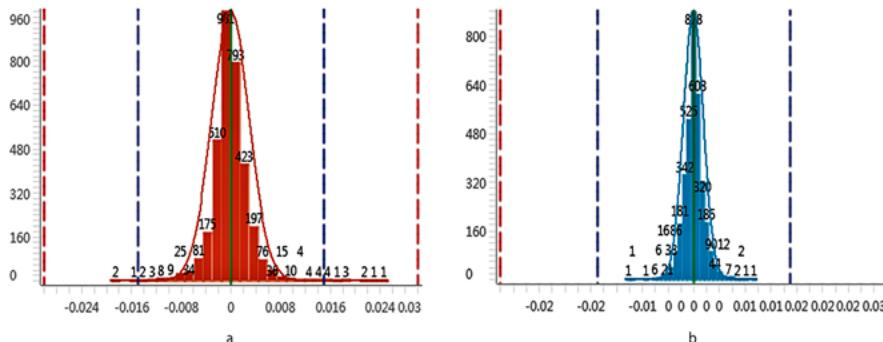


Figure 8: Predicted a) dX and b) dY overlay data histogram (mm) for 6x6 field size, where some die are out of specification, thereby reducing yield.

increase throughput, but reduces the ability to correct for individual die placement errors. By evaluating virtual exposures for different field sizes – and with each exposure corrected to optimize yield within the exposed field – it is possible to maximize process yield (defined as the percentage of die that will meet the overlay specification) and quantitatively evaluate trade-offs between yield and throughput for different field sizes. Only by having real-time data analysis can the user identify the correct settings and react to out-of-control situations without impacting yield.

For the panels evaluated, the software algorithm predicted 100% yield with a field size of 3x3 (**Figure 7**). The dX data was worse than the dY data, but all die placements were within the +/-15µm via to pad overlay specification. As the stepper field size was increased to 6x6 die, the yield drops to 99.42% as some of the die dX overlay errors exceeded the +/-15µm specification (**Figure 8**).

The software algorithm's yield prediction has been compared to actual customer product overlay measurements, confirming the accuracy of the prediction is within 0.2% of final overlay results. This result provided the user with confidence that AOI pre-measurement of panels with product die can be used to determine the optimum field size, throughput and yield prior to coating the panel with polyimide or photoresist. This has significant advantages in both cost

and process development. For example, polyimide processing is normally a non-reworkable process step and overlay errors at this stage result in scrapped die. Typically, if there is a die placement error that exceeds the specification of the multi-die exposure field it will only be observed after fully processing the polyimide lithography and measuring overlay. By this time, it would be too late to recover, requiring the die to be scrapped. With the ability to pre-measure and predict the yield with the AOI system and software algorithm, low yield could be avoided by reducing the field size. Moreover, the heat map and histogram data could be sent “upstream” to the EMC process engineer to address the root cause of molding process die placement error excursion.

Summary

It is clear from the experimental data that the calculated feed-forward site corrections provided the stepper with the ability to automatically compensate for die placement error. This is a significant improvement over the industry standard, where steppers use a simple linear model approach. Application of the site corrections, with larger field sizes during stepping, increased the lithography throughput significantly from 3 x 3 to 6 x 6 with low impact on yield, 100% to 99.42% respectively. This will naturally deliver commensurate reductions in cost of ownership.

The visualization of the die placement data using heat maps, histograms, vector plots, etc., provides the process engineer with the ability to optimize and predict the impact of stepper field size on production yield and throughput. Moreover, this revolutionary capability provides foresight, enabling the user to quickly feed data to upstream and downstream processes to prevent costly rework and scrapped product. Future software developments will provide a method to dynamically balance throughput with yield.

Acknowledgements

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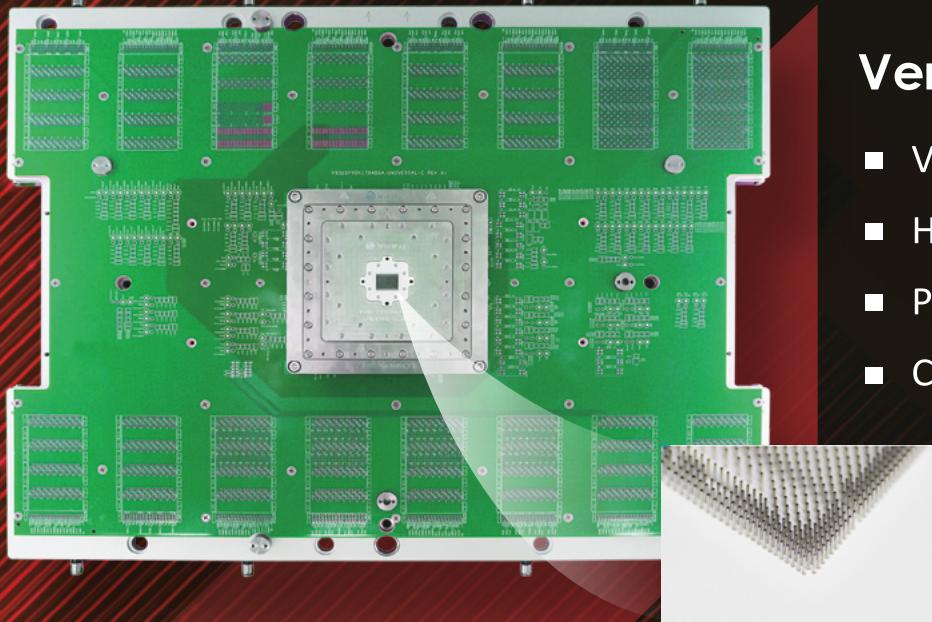
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Biography

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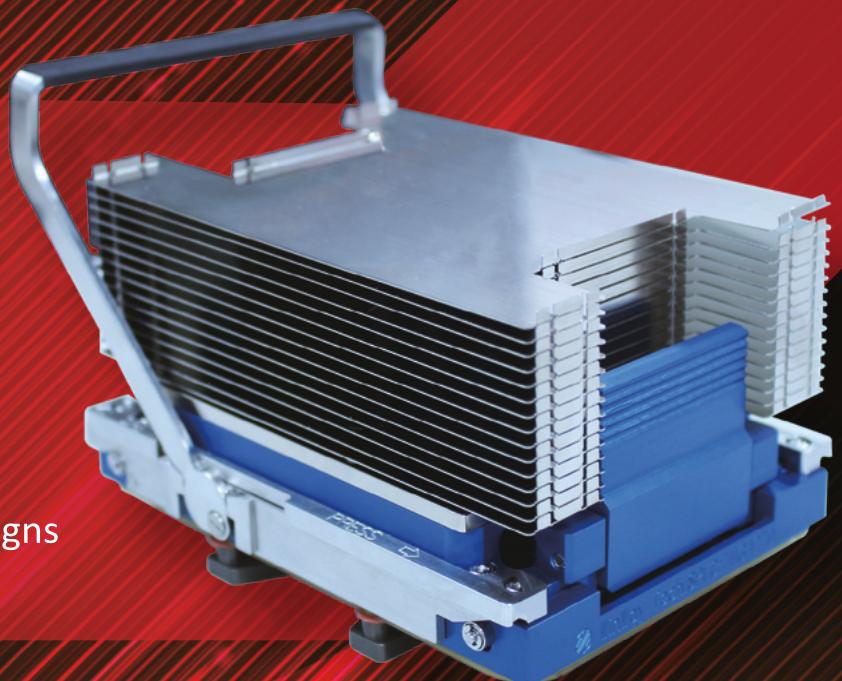


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Wavefront phase imaging for global and local wafer geometry

By Juan M. Trujillo-Sevilla, Jose M. Ramos-Rodríguez, Jan Gaudestad [Wooptix]

Wavefront phase imaging (WFPI) is a new technique to measure wafer geometry on a full wafer in a single image snapshot providing depth information for every pixel. The number of topography data points for the entire wafer will be proportional to the number of pixels in the image sensor, allowing for millions of data points to be acquired in less than a second. Sub-nanometer depth resolution is achieved by using two cameras with optics that image the entire wafer, with the exact same field of view, at different conjugation planes. Monochromatic incoherent light is illuminating the wafer and lateral resolution is determined by the lenses used for a specific field of view and the number of pixels offered by the image sensor.

As WFPI is an obvious candidate for incoming wafers at the front end of line (FEOL, i.e., the fab process up to when active devices (transistors) are made on the silicon wafer but before metal layers are deposited) on account of its high speed and high lateral resolution. However, it may be an even more important tool for the far back end of line (i.e., FBEOL starts when metal layers have been added to the silicon wafer and associated interconnect structures forming the connection between on-chip and off-chip wiring) where the silicon wafers are thinned, polished and then stacked as 3D integrated circuits (ICs) [1]. During the thinning and polishing steps, it is critical to measure the nanotopography (NT) and roughness of the wafer. As there are many candidates for measuring NT and roughness, none have the speed to measure an entire wafer within the time frame required in a semiconductor manufacturing line allowing the fab engineer to only measure small sample areas in the range of about a square millimeter providing single-digit micron resolution. WFPI, on the other hand, can image the entire wafer, thereby providing millions of data points with single-digit micron lateral resolution and sub-nanometer height resolution (amplitude) with a single snapshot in less than a second.

Introduction

The geometry of unpatterned silicon wafers used as substrates for IC manufacturing is critical for process control and ultimately, for device yield. Wafer geometry has many characteristics that have been classified based on spatial wavelength (λ_s) and amplitude (Z height resolution) (Figure 1) [2]. Nanotopography (NT) is defined as height variations with amplitudes in the tens of nanometers at the wafer surface and within λ_s in the range of

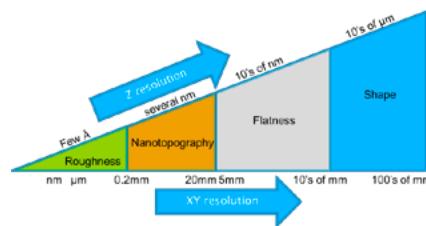


Figure 1: Definition of wafer geometry.

200 μm –20mm. Beyond NT lies roughness, with amplitude in the single-digit nanometer to sub-nanometer range and λ_s in the range of tens of nanometers to microns. Shape and flatness have typically been measured optically using confocal microscopy or laser interferometry. Such systems (one or the other), however, have not been able to measure NT and roughness on account of their poor spatial resolution [2,3].

Description of WFPI

The working principle of WFPI is based on registering the intensity distribution at two different optical measurement planes. The intensity distribution is recorded by a conventional imaging sensor. The wavefront phase is defined as the surface perpendicular to the direction of propagation of the light rays. The sensor assumes geometrical propagation of light, and in this regime the light can be considered as a collection of light rays that bends according to Snell's law and reflects

on a surface keeping its angle with respect to the surface normal. The reflected beam will carry the wavefront phase, where the value is proportional to the surface height map. In our case, we are using a collimated red ($\lambda = 650\text{nm}$) light beam that reflects onto the surface—the reflection angle of each ray is exactly two times the angle of the surface normal [4].

There exists a value that defines the surface height range, which can be measured for a certain configuration; this is the limiting surface angle ($\alpha_{lim} = \tan p/d$), which is given by the

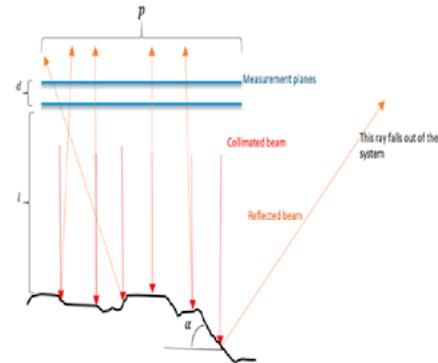


Figure 2: Limiting surface angle defines the height range for a given configuration where p is the side length of the measurement planes, d is the distance between measurement planes, and l is the working distance.

maximum angle that a light ray can be reflected and still be recorded by the imaging sensors (Figure 2).

This estimation gives the maximum measurable absolute surface angle, but does not give a measure of the maximum height range for a certain configuration. The maximum range is important because it defines the maximum warpage of a sample to be measured. In this case, it has been found that a surface angle that causes 1% of the maximum displacement is within the measurable range. Then, following a geometrical approximation, the range $R=p^2/(100\cdot d)$. The height resolution is defined by the minimum measurable

slope, which also depends on d and on the pixel size n given by $r_{max} = n^2/(4d)$. It is worth noting that for a given imaging sensor, the maximum range and the height resolution can be modified by varying the distance between measurement planes. For instance, it may seem that by increasing d , the resolution can improve indefinitely. The limit for the distance d is defined by the range in which geometrical optics are still valid. The Fresnel number is widely accepted as an indicator of optical range given by $F=r^2/(L\lambda)$ where r is the aperture radius, L denotes the propagation distance and λ represents the wavelength of the light. When $F \gg 1$ the range is considered geometrical. We have empirically found that a value of $F \geq 100$ guarantees the correct working of WFPI. This condition sets the maximum value that the propagation distance can take ($L_{max} \leq r^2/(100\cdot\lambda)$), in WFPI, the maximum propagation distance is defined by the sum of d and l [4].

Implementation of WFPI

The reflected light beam, which carries the wavefront phase information of the sample surface profile, is de-magnified by a telecentric lens. For image acquisition, two paired imaging sensors were used, each one placed at a different optical plane allowing the pair of images to be acquired at the same time. With this setup, a single image snapshot collects the wafer topography of the entire wafer with the same number of pixels as being present in the imaging sensor [5].

The WFPI system used in our experiments can measure samples up to 50mm in diameter. However, the technique is easily applied on larger sample sizes by using proportional optics, meaning that the lens must be equal or larger compared to the sample size being measured. The cameras and the general setup stay the same independent of the sample size. The optical path length will be chosen according to the lens specifications. The device under test (DUT) is placed flat onto a horizontal sample plate with no vacuum to avoid sample flattening beyond the force of

gravity. The specifications of the system are summarized in **Table 1** [4] (also, see **Figure 3**).



Figure 3: Render of the prototype for 50mm diameter (max) samples with two cameras and one lens.

Lateral resolution of WFPI

Getting an accurate value of the maximum lateral resolution is more difficult for WFPI than in conventional imaging systems because in conventional systems, the modulation transfer function (MTF) is obtained measuring the contrast of several line groups at different resolutions. In WFPI, on the other hand, the wavefront phase map must first be calculated, and then one can measure the different contrast values relative to the known resolution values in a given target.

From a theoretical point of view, WFPI is considered as a coherent optical system, and so, its transfer function consists of a flat response with a value up to its cutoff frequency [6]. The cutoff frequency value depends on the criterion chosen. Here we have chosen Abbe's criterion ($f_c = 1/(N\cdot\lambda)$) because it is more restrictive than other popular criteria such as Rayleigh or Sparrow [7]. Applying the f# of 7.5 and using a red (650nm) light emitting diode (LED) setup, one gets that the theoretical resolution limitation of this system is 4.875μm.

For the measurement of the actual frequency response of the prototype, we used a USAF-1951 test target (Air Force MIL-STD-150A standard of 1951 and provided by Applied Image item number

T-22-2-N-CG). This test target comprises a glass substrate with a deposition of chrome that forms line pairs with lateral frequencies up to 512 cycles per mm (cy/mm), one cycle being 2 pixels side-by-side with different contrast ratios. Because the chrome deposition layer creates surface topography, it can be used to measure the performance of WFPI in terms of lateral resolution. The process consisted of placing the test target in the WFPI measurement system and running a single measurement of an area that contains line groups with spatial frequencies in a range valid for this study [5].

On account of the two cameras and the magnification of the telecentric lens arrangement used, the pixel size in object space is 24μm (Table 1.), which translated to a frequency that is equivalent to approximately 20cy/mm (1mm/(2×24μm)≈20). A phase image of the test target was acquired in an area that covered frequencies from 1cy/mm to 20cy/mm. The measured WFPI was used to calculate the phase information and measure the local contrast. In **Figure 4**, the results are summarized and plotted against the theoretical contrast limitation, giving a cutoff frequency of 103cy/mm (1mm/(2×4.875μm)≈102.56)).

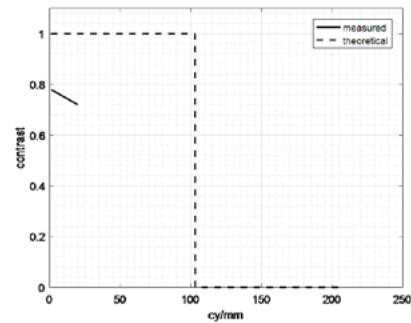


Figure 4: Comparison of measured and theoretical contrast response versus lateral resolution.

However, with the current pixel size (24μm), the system can only measure up to 20cy/mm.

A large difference between the predicted and the actual frequency responses is observed. It is important to note that the theoretical behavior is only valid with an optical system that is completely free of aberrations; any wavefront error in the lenses of the instrument contributes to a poorer frequency response. However, looking

Lens f#	7.5
Image Sensor	2680 × 4024 (10.8MP)
Data points (50mm round)	≈ 4.34 million
Pixel Size (50mm image)	24μm

Table 1: Specifications of the demo system for a 50mm diameter sample size.



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at the slope, one can expect this to continue close to linearly, indicating that increasing the number of pixels by using a higher resolution camera setup enables one to reach the optical lateral resolution limitation of the system ($4.875\mu\text{m}$) [5].

Z-height resolution: amplitude

A key aspect in determining the minimum amplitude that can be measured by a system is the noise level. The noise level for AFM is about 0.1nm and the noise level for an optical profiler is on the order of 0.4nm . However, both techniques struggle with speed and a very small field of view [8].

A noise simulation was done where two circular images were generated and noise levels ranged from 20dB to infinity (meaning infinite exposure time). The two noisy images were then put into the WFPI measurement algorithm and analyzed as if the two images had been acquired using the WFPI system. The noise is given in nanometer root-mean-square (RMS) with its standard deviation (σ). The noise level is summarized in **Figure 5**.

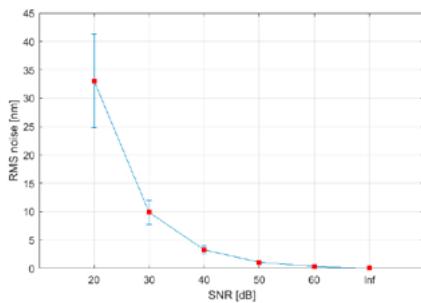


Figure 5: RMS noise (nm), standard deviation (nm) and signal-to-noise-ratio (dB).

The noise in the camera image sensor used in the WFPI system was 62dB , which translated to an RMS noise level at 0.3nm with a standard deviation of 0.1nm . Combined with a $24\mu\text{m}$ lateral resolution, WFPI is a good candidate among optical techniques for measuring NT and partly, roughness.

Global wafer geometry

Chromatic confocal scanning microscopy is a commonly used technique for measuring global wafer geometry, such as warp and bow, by using a white light point source that is focused

#	Type	Company	Model	Curvature r (m)	warpage (μm)
1	Flat	Edmund Optics	69-249	∞	0
2	Concave	Lambda	PCCM-5006B-3000	3	98.01

Table 2: Specifications for the 2 mirrors reported in this paper. All mirrors were 50.8mm in diameter with aluminum coating.

over the sample using a lens that exhibits a large longitudinal chromatic aberration [9]. Because the chromatic aberration causes different wavelengths to focus at different heights, there will be a specific wavelength (λ_0), for which the focus lies on the surface sample. The reflected light from the sample passes back through the lens and is derived using a spectrum

analyzer. Any light coming from out-of-focus reflections will be rejected by the pinhole aperture. Finally, by detecting the peak wavelength, the sample position can be found.

The technique described above has been used in metrology because of its capacity of measuring a large variety of surfaces. Its main limitation comes from

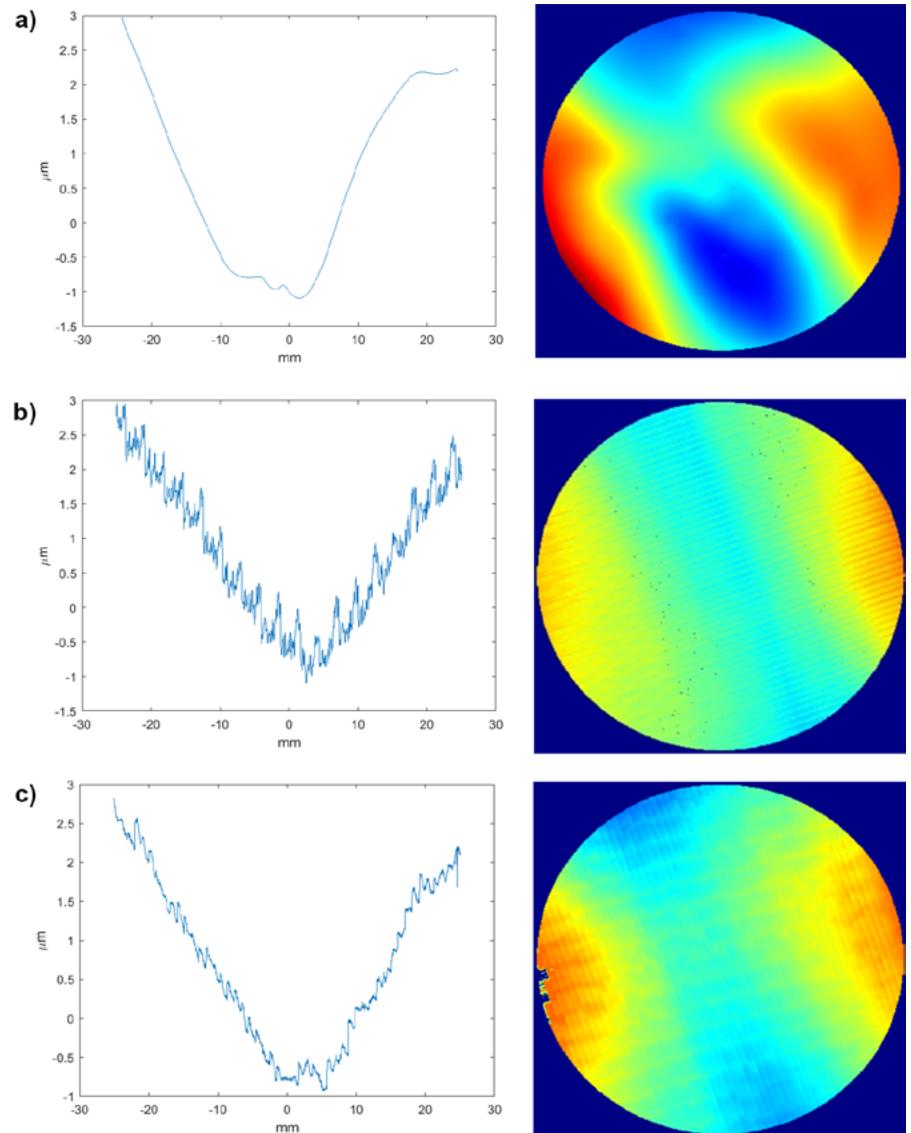


Figure 6: Comparison of reference mirror measurement using three instruments. All data is shown with a false color image and a line scan through the center of the mirror sample. a) (top): WFPI snapshot (100ms); b) (middle) Chromatic confocal microscopy at higher speed raster scanning #1 (2min); and c) (lower) Chromatic confocal microscopy with lower raster scanning speed #2 (11min [11]). aluminum coating.

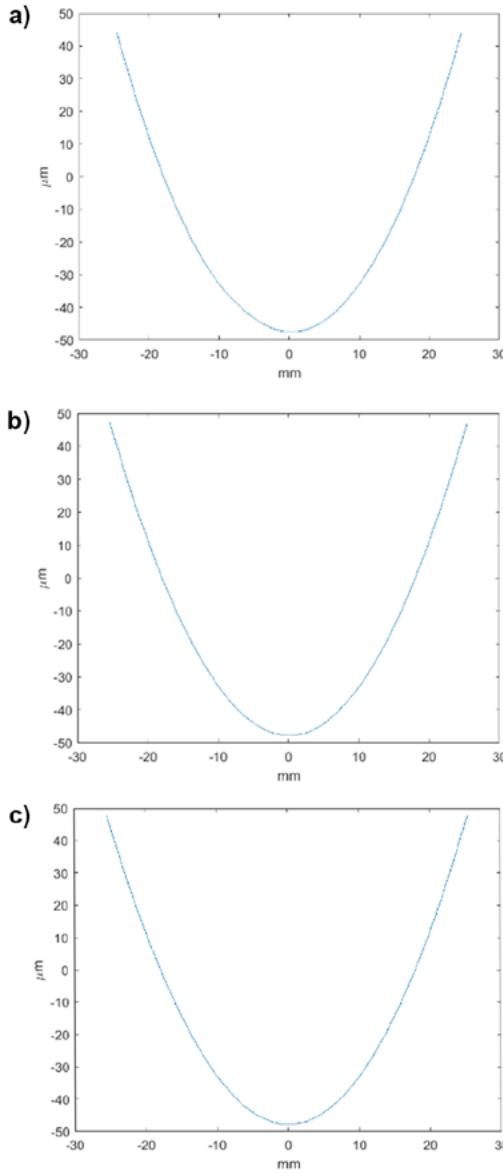


Figure 7: Comparison of reference mirror measurement using three instruments. All data is shown with a false color image and a line scan through the center of the mirror sample. a) (top) WFPI snapshot (100ms); b) (middle) Chromatic confocal at higher speed raster scanning #1 (2min [10]); and c) (lower) Chromatic confocal microscopy #2 with lower raster scanning speed (11min [11]).

being capable of only measuring one point each time—needing a translation stage when acquiring a surface profile [9,10]. Several commercial reference mirrors (**Table 2**) with a known bow were used as target samples to compare the performance of WFPI against two commercial chromatic confocal microscopes [11,12]. The first set of data was done on a flat mirror, which means there is no bow (i.e., radius of the bow is infinite, ∞) (see **Figure 6**).

Some bow and warp are to be expected even on a flat surface as a result of temperature changes, among

other factors. In all data sets of the flat sample, one can clearly see there is some warp in the single-digit micron range. However, this warp is still within the specifications of these samples. It is also clear that when a raster scanning system acquires data faster, the raster scanning noise increases. No raster scanning noise can be seen when using WFPI.

The last sample had bow of $98.01\mu\text{m}$ from the center low point to the edge high point (radius of the bow is 3m, a smaller radius gives a higher bow and a large height difference between the lowest and highest points) (see **Figure 7**).

The data demonstrates a strong correlation between WFPI and chromatic confocal microscopy. In the current WFPI system, the data acquisition is fast (less than a second), however, the data analysis can take up to 2s. Most of the time used for data analysis is spent acquiring the amplitude of the light.

Local wafer geometry

To measure local variations (NT and roughness), a 2-inch blank silicon wafer with specifications according to SEMI standards [13] was used for WFPI measurements. Two images were acquired with the WFPI system: an intensity image (**Figure 8a**) and a global topography image. From the topography image, a global depth map and a 3D map (**Figure 8b**) were generated. A double Gaussian high-pass filter was applied on the global topography map of the wafer to remove low-frequency spatial resolution, which revealed roughness with a spatial resolution equal to the

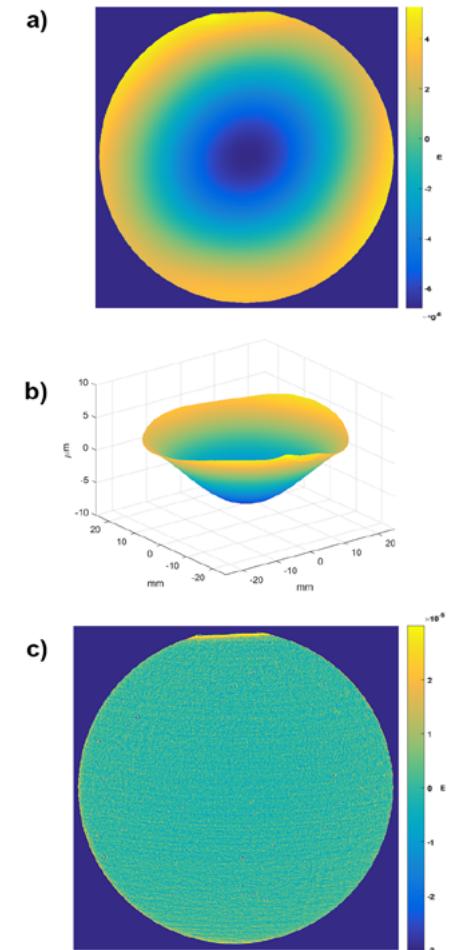


Figure 8: Images of: a) intensity map, b) 3D depth map and c) high-pass filtered NT and roughness.

pixel size ($24\mu\text{m}$) (Figure 8c). The data was collected in a single snapshot with an exposure time of 0.1s.

The data collected using the above procedure was analyzed through the WFPI algorithm to calculate the wavefront phase and the associated amplitude (Z height). The filtered topography data reveals the higher spatial frequencies, and clearly showing the low-amplitude depth map associated with NT and roughness caused by wafer polishing.

Summary

The comparison between WFPI and chromatic confocal microscopy was done using standard mirrors with known bow. The results showed that WFPI has higher speed and lower noise than the chromatic confocal microscopy methodology. The current demo system is made for samples with a maximum diameter of 50mm. However, with different optics one can easily make a system that works on a full 300mm diameter sample. Also, to improve the number of data points, one can use a higher pixel image sensor without increasing the data acquisition time very much—this is something that will help when collecting data for a complex warpage situation.

WFPI was proven to reveal roughness by applying a high-pass filter on the global topography data to analyze the higher spatial frequencies. WFPI has a lateral resolution of $24\mu\text{m}$ and an amplitude sensitivity at 0.3nm . This means that, while collecting data on the entire wafer in a single image snapshot, WFPI has the potential to become the only wafer geometry technique capable of revealing NT and roughness of the entire wafer at a speed fast enough to satisfy

the demands of full-production wafer fabs. The current WFPI system is made for samples with a maximum diameter of 50mm. With different optics, however, one can easily make a system that works on a full 300mm diameter sample, which is currently being built, that will collect more than 10 million data points on a 300mm wafer.

As WFPI has shown to be a very good candidate for FEOL and FBEOL applications, using the correct spatial filtering technique, it can also perform global wafer geometry measurements on patterned wafers during the BEOL process to help process-induced overlay errors during lithography steps [1]. This work is currently in progress with very good initial results; the first official results are expected in the first half of 2020.

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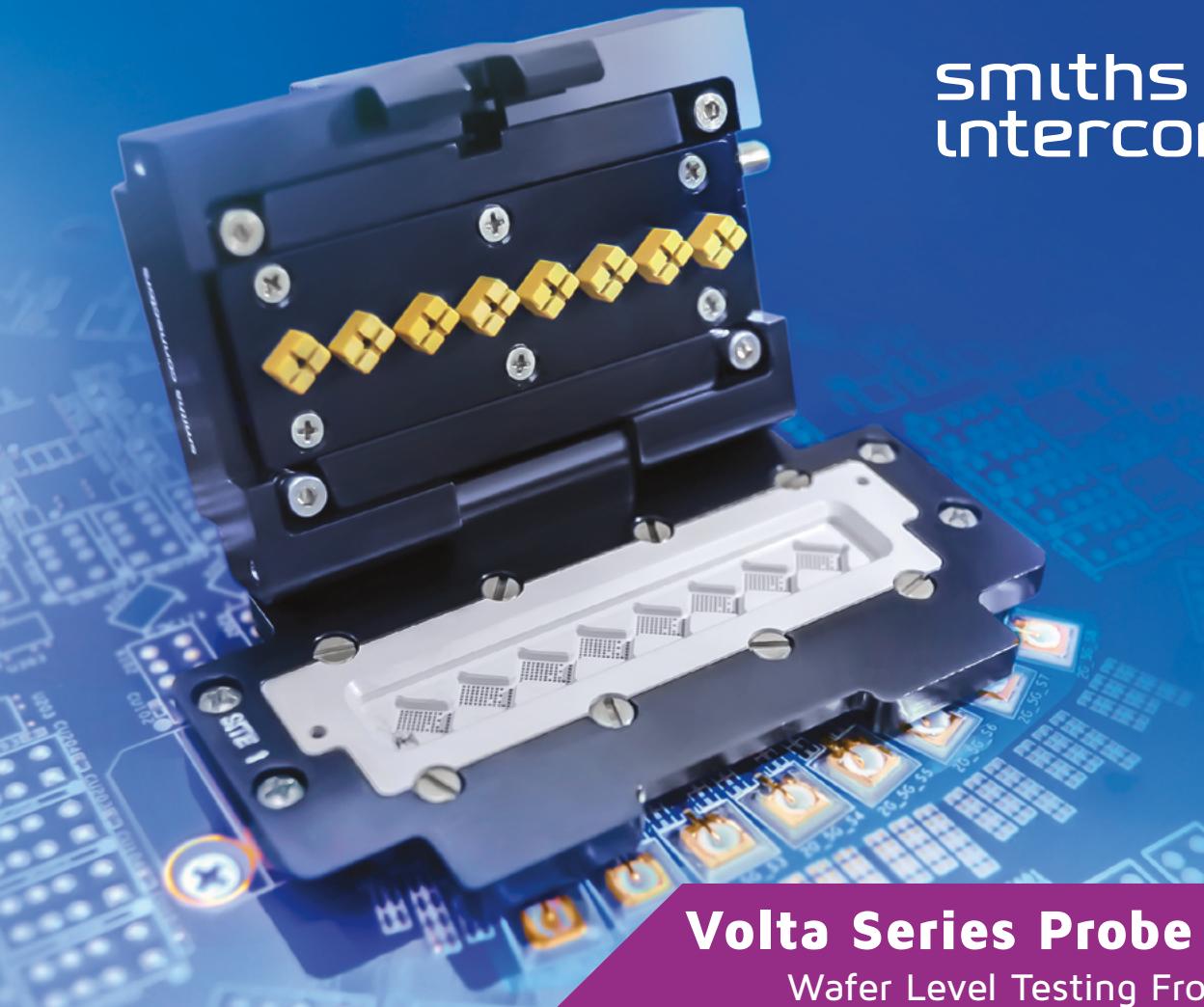


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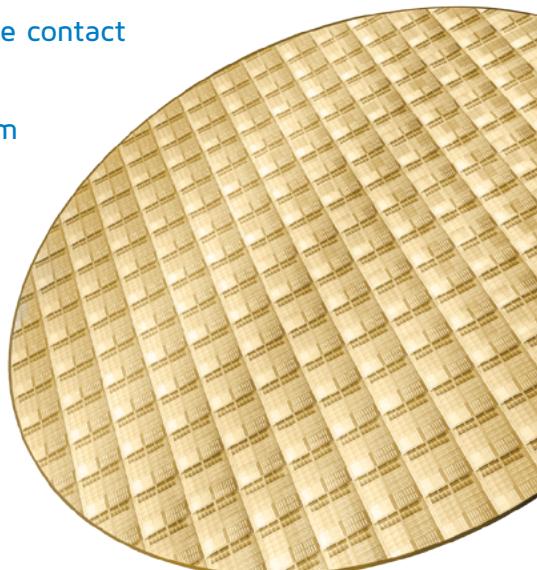
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Using laser-induced deep etching to enable microfeatures in glass

By Roman Ostholt, Norbert Ambrosius, Jean-Pol Delrue, Rafael Santos, Daniel Dunker, Stephan Schmidt [[LPKF Laser & Electronics AG](#)]

This article was edited from papers respectively presented at the IMAPS Conferences in Pisa, Italy in Sept. 2019 and in Boston, USA in Nov. 2019.

Glass is arguably one of the most interesting materials for heterogeneous integration. Whether it is for its radio frequency (RF) properties, high surface quality, hermeticity, tunable coefficient of thermal expansion (CTE) or low cost, there are several reasons to favor glass for advanced packaging applications. Unfortunately, and up to now, processibility of glass has not been among those reasons. This is because current glass processing technologies typically induce micro-cracks and stresses, which contribute to glass's reputation of being prone to brittle fracture. In contrast, glass without surface defects has excellent mechanical properties as can be demonstrated when it is processed by laser-induced deep etching (LIDE).

LIDE is a two-step process using a fast laser beam, which modifies the glass with a single pulse, followed by a chemical etching. As previously shown by the authors [1,2], LIDE technology is capable of generating high aspect ratio and high-quality microfeatures in various alumino-boro-silicate glasses. Therefore, this technology is regularly used in applications such as through-glass vias (TGV), glass spacer wafers, and microfluidics.

Passive die alignment in GEFOP

The following sub-sections discuss various considerations with respect to glass embedded fan-out packaging (GEFOP).

Glass embedded fan-out packaging (GEFOP). Fan-out packaging has become a major driver of advanced packaging in recent years. In order to use this packaging technology for future generations with higher I/O densities and multiple dies, new techniques to reduce

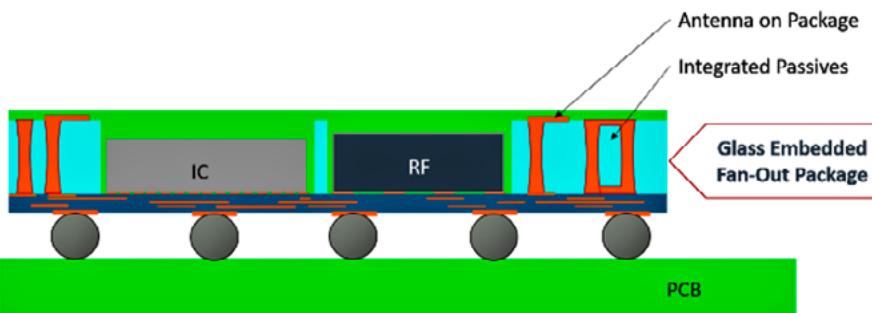


Figure 1: Schematic drawing of the GEFOP concept [2].

the die position error and warpage need to be developed. As such, research is being carried out to take full advantage of the properties of glass for advanced packaging [1,3]. One of these solutions is GEFOP [2]. A schematic drawing of GEFOP is shown in Figure 1.

Precision glass processing is used to manufacture a mounting wafer with multiple open die embedding cavities together with micro-holes for TGVs and integrated passive devices (Figure 2).

Dies are placed in open cavities before filling them with a dielectric material. After this material – an epoxy molding compound (EMC) – is cured, the dies are fixed in the mounting wafer and the substrate can be further processed like a normal reconstituted wafer. In contrast to conventional fan-out packaging through transfer molding of the EMC, reconstituted wafers processed using the GEFOP concept presented here do not show a critical warpage.

Typical glass embedding wafers have a diameter of 300mm (Figure 3), but substrates with a size of 500 × 500mm² can also be produced. Depending on the application, embedding glass wafers can have a nominal thickness between 100µm and 500µm.

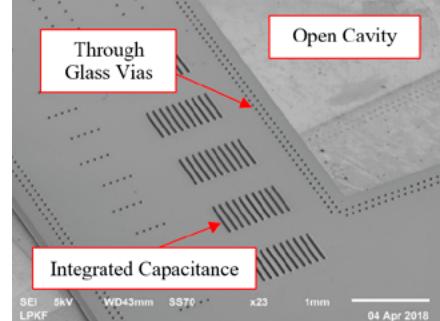


Figure 2: A scanning electron microscopy (SEM) micrograph of the mounting wafer.



Figure 3: LIDE-produced mounting glass wafer with a 300mm diameter.

The GEFOP concept discussed so far represents a solution for the two most pressing problems in fan-out packaging: warpage and die

shift during transfer molding. However, this concept does not solve an essential cause of die alignment inaccuracies: the die placement.

Modified GEFOP by passive die alignments. The modified GEFOP presented here is based on the usage of passive die alignment structures. The spring-like die alignment features are placed on two adjacent sides of the open cavities (**Figure 4**). When the dies are placed, the alignment devices spring in and precisely align the die in relation to the mounting substrate. As in the conventional GEFOP concept, after the die placement all gaps are filled with the EMC, which is then cured and processed like a normal reconstituted wafer.

Methods. There are two main considerations for modified GEFOP wafers with passive die alignment features: 1) Design of such features, and 2) Accuracy measurement of die position. Both are discussed below.

Glass is prone to brittle fracture if not free of surface defects such as micro-cracks. Therefore, it may not be normally seen as a structural material for

mechanical components, such as springs. However, by considering glass fibers for the alignment structures, this perspective changes: for glass fibers without surface defects, fracture strengths greater than 1GPa can be found in the literature [4].

The primary objective of this investigation was to reduce the alignment error after die placement. In order to

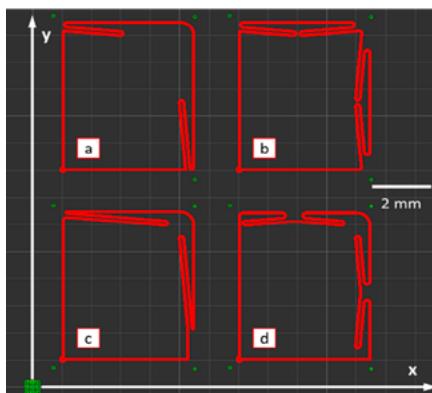


Figure 4: Schematic drawings of the GEFOP designs tested in this work (in red color). At the bottom left of the image (in green color) are alignment marks used as reference for the measurement of the cavity and the test die position.

quantify the die positioning and its accuracy, TGVs were produced in the test dies and the mounting wafer substrates to be used as alignment marks (**Figure 4** and **5**). The metric used for qualification of the alignment error of each of the designs shown in **Figure 4** was the standard deviation of the die position measurements.

Results. First, the spring elements shown in **Figure 4** were examined for their suitability. For this purpose, a glass substrate was processed with

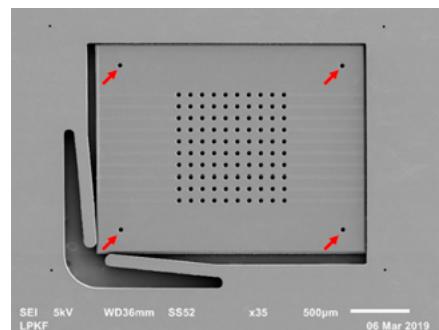


Figure 5: A SEM micrograph of glass die mounted in the glass substrate with passive alignment features. The red arrows indicate the alignment marks used in the measurement of the die position.



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each design repeated 16 times. Test dies were manually placed in the total of 64 cavities and their position within the cavity measured. The standard deviation of the die position for each design is shown in **Figure 6**.

The design B (**Figure 4**) with two centrally acting spring elements showed the smallest positioning error and was, therefore, chosen to be used for further investigations. A series of five substrates

with 64 cavities each of design B were manufactured, where the test-dies were mounted and their alignments measured. No significant deviation was detected between the substrates. The positional error of all dies in the X direction is shown in **Figure 7**, while **Figure 8** shows the positional error in the Y direction.

Conclusions on LIDE-generated passive die alignment features. LIDE technology can be used to produce

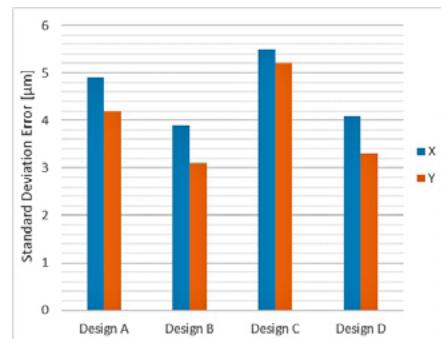


Figure 6: Standard deviation of the measurement of the positions of the alignment marks in the test dies in relation to the ones in the substrate wafer, for each die cavity design with integrated passive alignment structures.

defect-free passive die alignment structures at the edge of open cavities in glass mounting wafers. Even though this was solely an early-stage study, LIDE's on-the-fly laser process enabled the production of each cavity in approximately two seconds, making it already a high-throughput technology. Cycle times are, therefore,

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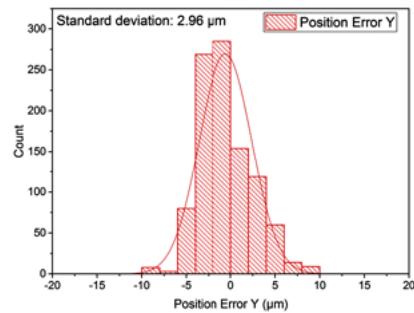


Figure 7: Die positional error in the X direction.

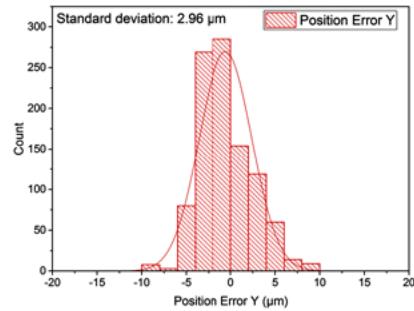


Figure 8: Die positional error in the Y direction.

expected to be greatly improved with a completely optimized process. Theoretical derivations and practical tests have shown that if the spring elements are suitably designed, they remain intact while in operation. In the

case of the spring elements examined here, the double-acting structures proved to be advantageous on account of their structure and likely due to the spring force, which is approximately twice as great in comparison with the other designs.

Glass wafer-level packaging enabled by LIDE of closed cavities

The following sections demonstrate how LIDE technology can manufacture closed pockets for glass capping wafers without having the drawback of under etching, which is usually associated with mask isotropic wet etching.

WLP with glass capping wafer. Wafer-level packaging (WLP) is an established low-cost and high-volume production technology [5]. Glass capping wafers are usually made with an etch mask (typically chromium) and subsequently wet etched. This process is associated with under etching of the etch mask, resulting in capping wafers with closed cavities that have a pronounced fillet at the bottom and limited to aspect-ratios below 1 (**Figure 9**).



Figure 9: Schematic of wafer-level packaging with a standard glass capping wafer.

Glass capping wafers made by LIDE. LIDE enables the manufacture of cavities with steep sidewalls (i.e., high aspect ratios). For this purpose, the process is controlled in such a way that the laser-induced modifications are intentionally not introduced over the entire thickness of the substrate. Usually, the modifications are arranged in a hexagonal pattern to

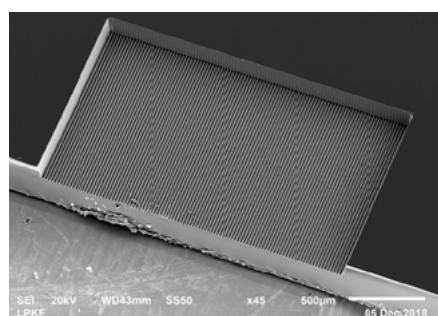


Figure 10: A closed glass cavity made by LIDE.

produce a surface that is as flat as possible. A scanning electron microscopy (SEM) image of a closed cavity made by LIDE is shown in **Figure 10**. The sidewalls have a taper angle of approximately 1°.

The advantages of using a capping wafer manufactured by LIDE for WLP essentially result from the favorable cross-section profile. This profile fits better to the rectangular silicon dies and enables higher population densities as it can be seen in the comparison between **Figure 9** and **Figure 11**.



Figure 11: Schematic of wafer-level packaging with a LIDE-processed glass capping wafer.

Variation of pitch between laser-induced modifications. The roughness of the cavity mainly depends on the distance between the individual laser modifications of the glass. To evaluate the cavity roughness, the pitch of the

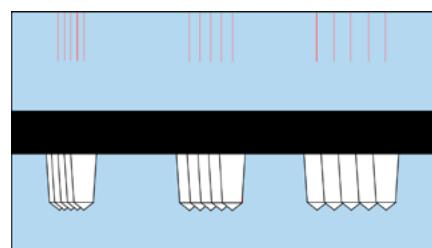


Figure 12: Schematic of the cavity shown in Figure 11.

laser modifications was progressively changed. A schematic visualization of the laser modifications and the resulting etched profile are shown in **Figure 12**. **Figure 13** shows different SEM pictures

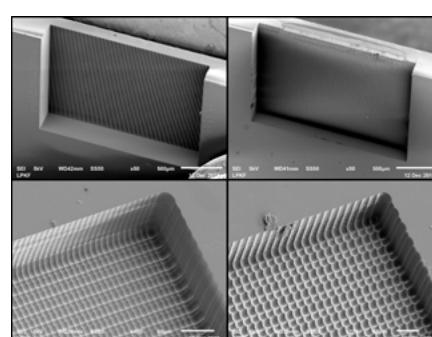


Figure 13: SEM pictures of closed cavities.

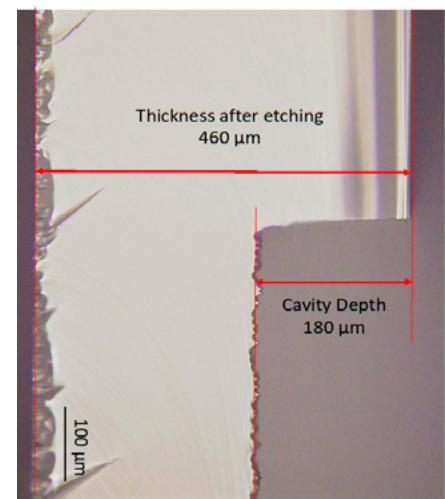


Figure 14: Light microscopy image of a cross section of a cavity made by LIDE.

of the closed cavities with different roughnesses. Roughness measurements of the bottom of the cavities will be addressed later in the measurement results paragraph where we will show that a longer etching time leads to a better bottom cavity roughness. To measure the cavity depth, the glass panel was cut with a diamond scribing wheel. The cutting facet was then inspected with a Keyence VK X210 microscope and the glass thickness and cavity depth were measured (see **Figure 14**).

As it is shown in **Figure 15**, if etched longer, the spikes at the bottom of the cavities are reduced, as is the roughness. So, the etching time parameter can be used to achieve the requested roughness down to a Ra of $\approx 0.5 \mu\text{m}$.

Discussion. The positional accuracy of closed cavities made by LIDE is within what was expected, as the laser tool specification is within $\pm 5 \mu\text{m}$ ($Cpk > 1.33$). The width and height of the cavities are defined by the same direct writing process.

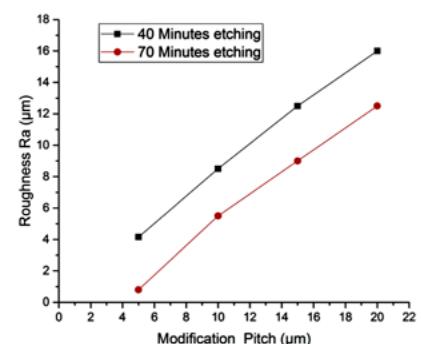


Figure 15: Measurement results of the roughness of the bottom cavities versus the laser pitch applied for two different etching times.

As such, the size tolerance equals the positional tolerance values.

The lowest roughness value obtained by LIDE is approximately $R_a \approx 0.5\mu\text{m}$. Although the bottom surface of the pockets created by LIDE does not meet optical standard requirements, most capping applications do not require such a low roughness.

Cavity depth shows a standard deviation of $3.9\mu\text{m}$ and is therefore significantly larger than the other tolerances. The reason for this is suspected to be insufficient control of the mechanically-guided laser head relative

to the substrate. Further investigations will show whether and to what extent better cavity depth tolerance can be achieved.

Cost contributions. To evaluate a new manufacturing process, it is essential to consider its cost and, in particular, to understand its influencing factors. Even though LIDE is a very fast manufacturing process, it remains a direct writing technology. The pulse pitch is the main contributor to the overall cost. Fortunately, there is a tradeoff between an acceptable bottom surface roughness and a manufacturing cost to choose an optimal

pulse pitch. In addition, wet etching used in LIDE is typically a batch process and does not contribute significantly to the overall process costs.

Summary

Glass capping wafers with steep side walls have been achieved with the help of laser-induced deep etching (LIDE) technology. The size tolerances of the cavities, their depth value ($>300\mu\text{m}$), as well as their position tolerance, have been measured. They are within specifications to accommodate WLP packaging. The bottom pocket surface roughness is $R_a \approx 0.5\mu\text{m}$, well within what is necessary to accommodate the dies.

In conclusion, we believe that LIDE technology is a good candidate to manufacture closed cavities for WLP, taking into account the fact that the steep side walls achieved allow higher population densities of the die packing.

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Eliminating warpage for FOWLP during debonding

By Debbie Claire Sanchez, Klemens Reitinger, Miguel Adolfo Resendiz Jimenez,
Sophia Oldeide, Kang Zhao, Wenxuan Song, Ibrahim Khwaja [ERS electronic GmbH]

The increasing demand for smaller and more cost-efficient packaging in the portable electronic area has increased the discussion about fan-out wafer-level packaging (FOWLP). Advantages of FOWLP technology include: 1) Good electrical performance; 2) Supporting increasing demands for I/O count; 3) Enabling dual-die or multi-die package configuration; and 4) Providing a supporting fine redistribution layer (RDL) traces $\leq 10\mu\text{m}$ line/space. Alongside the mass production, two critical issues surfaced for FOWLP: die shift and wafer warpage.

Die shift results from misplacement of the die with regards to its designed position. Warpage is due to the mismatch of the coefficient of thermal expansion (CTE) between silicon and the epoxy molding compound (EMC). EMC, having a higher CTE value, results in an imbalance, which will cause the wafer or panel to warp. Applying the correct thermal treatment process, however, results in a warpage profile $<1\text{mm}$, which allows succeeding processes to run smoothly. The idea is to treat the wafer with a temperature higher or equal to its T_g until the mold compound softens, and then transport it onto a cooler chuck. As the wafer sits on the cool vacuum chuck, it conforms to its flatness. The transportation from the debonding station to the cooling chuck plays a significant role, requiring several critical items.

Types of fan-out structures

There are two process flows for fan-out structures: chip-last and chip-first. The chip-last process is depicted in **Figure 1**, beginning with the building of the RDLs onto a temporary carrier followed by the die bonding process and molding.

The reconstructed wafer/panel with RDL is then debonded from the carrier. The process then moves to back-end processing. Solder balls are placed on top of the RDLs, which serve as an electrical conduit between the dies and board.

The chip-first process (**Figure 1**) is more widely used by companies like Infineon, ASE, and Deca Technologies,

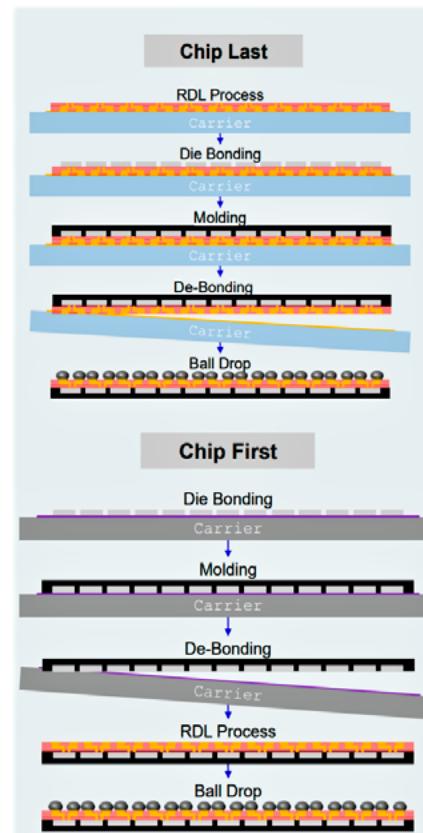


Figure 1: Chip-last and chip-first structures.

and has a reverse order compared to the chip-last process flow. The process starts with die bonding, molding, debonding, and then RDL processing, respectively. Details of the process are explained in the following sections.

Die bonding. The process starts with the picking of known good dies (KGD) from a sawn silicon wafer, which are then placed onto a temporary carrier laminated with a thermal or ultraviolet (UV) sensitive tape.

Molding. The compression molding process is commonly used for this structure. It starts with weighing the right amount of EMC and dispensing it on top of the carrier. The machine then starts closing the cavity in a controlled speed.

Debonding. The debonding process is the separation of the reconstituted wafer from the carrier, via the application of heat, or laser exposure. The sensitive (thermal or UV) tape layer softens and loosens adhesion to aid separation of the wafer from the carrier. Once the wafer is separated from the carrier material, any characteristic imbalance will be evident, leading to warpage. Warpage appears on account of mechanical stress caused by the CTE mismatch of the reconstituted wafer.

For a thermal debonding process, thermal uniformity is critical to ensure no wafer excursion occurs. The thermal sensitive tape needs to activate across the entire surface before mechanical separation of the carrier and the wafer. At this point, the warpage becomes evident. In the chip-first structure, this process is the launching pad for interconnect build-up. If warpage is not reduced, warpage-induced defects will increase as the wafer goes through the line.

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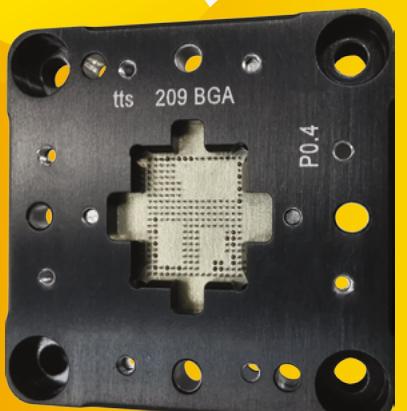


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Common issues for fan-out

FOWLP has piqued the interest of the semiconductor industry because of its high-performance level and flexibility for multi-die configuration. However, die shift and warpage have remained the top challenges of high-volume production both with respect to yield and cycle time. Multiple research studies from both equipment makers and material suppliers have been conducted to resolve these issues.

Die shift. The die location plays an important role for both package design and manufacturing. The dies have predefined location and pitch for specific package sizes. This information is needed during the making of the photomask for the lithography process. Die shift is a defect in which the die placement has an offset from the predefined location by a certain distance. This offset, if high enough, will cause a lithography or patterning issue in which the bond pads do not align with the mask, thereby causing open/close electrical interconnects.

Warpage. Warpage is one of the defects that is inherent to the structure. Because the wafer/panel becomes a heterogenous material on account of the combination of silicon and molding compound, the materials' properties will act on each other. In this case, the CTE mismatch creates an imbalance in the expansion and contraction of the material when processed through thermal treatment. This affects both 1) productivity, which creates issues regarding handling and automation, and 2) yield, where it potentially causes high thickness variation during the coating process, or pattern defect during exposure.

Understanding warpage and its impact. Research has been done by John Lau, et al. [1], regarding the top six process stages that are hugely affected by wafer/panel warpage. For the chip-first structure, once the wafer is debonded from the carrier, warpage immediately becomes apparent. In the face-down version commonly referred to as embedded wafer-level ball grid array (eWLB), the process that suffers warpage post-debond is the photo process. This process, aside from handling issues, will encounter yield problems when warpage is not minimized. In the face-up version, the process affected post-debond is the top-grinding process. The surface grinding process is performed to expose the connection embedded in the molding compound, and with warpage (to a certain degree), the wafer/panel becomes unprocessable. It is critical that warpage is at its minimum post-debond.

The ease of handling warp wafers/panels is affected by two factors: 1) the warpage degree, which can be calculated as:

$$\text{warpage} = RPD_{\max} - RPD_{\min};$$

and 2) warpage profile, which is the surface topography of the wafer.

The warpage profiles in the reconstituted wafer change depending on several factors, such as the silicon-to-mold density, the die shape (i.e., square and rectangular), and the number of RDLs, and for the panel level, the array arrangement as well (see **Figure 2**). To ensure that the profile does not significantly affect the handling system, it is crucial to reduce the warpage to <1mm after debonding so that the RDL or top grinding process can take place.

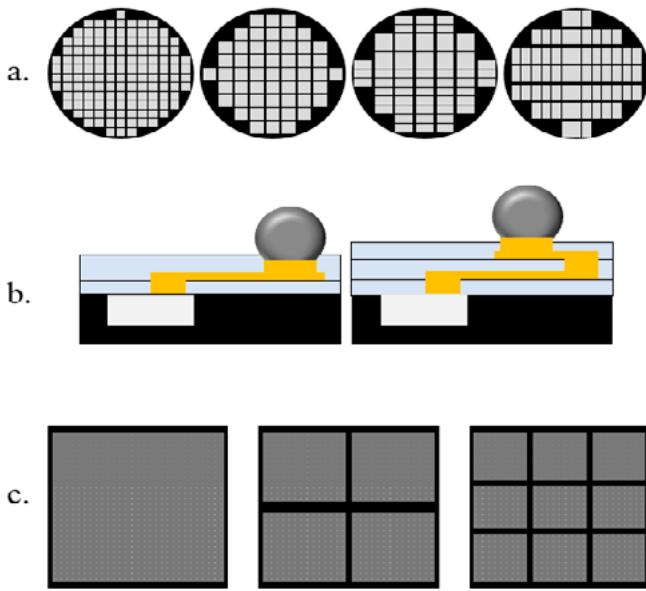


Figure 2: Causes of different warpage profile behavior: a) Die shape and silicon-to-mold density; b) Number of RDLs; and c) For panel format/array arrangement (e.g., single array, 2x2 array or 3x3 array).

As the FOWLP technology gains recognition in the advanced packaging sector, it has become increasingly used in high-volume manufactured products. This issue can be costly and very inefficient. Therefore, controlling the warpage in the reconstituted wafers is essential for semiconductor packaging applications and roadmapping.

Warpage adjustment method

The warpage adjustment concept evaluated in this paper is known as “shock and lock.” The wafer is subjected to a temperature that is equal or higher than its Tg for a predetermined dwell time, in which there is more expansion on one side of the wafer. After the wafer is exposed to heat, it should be transported to a cold thermal chuck, and the profile locked by constraining it to a vacuum chuck. Temperature uniformity and transport techniques are critical factors in this process.

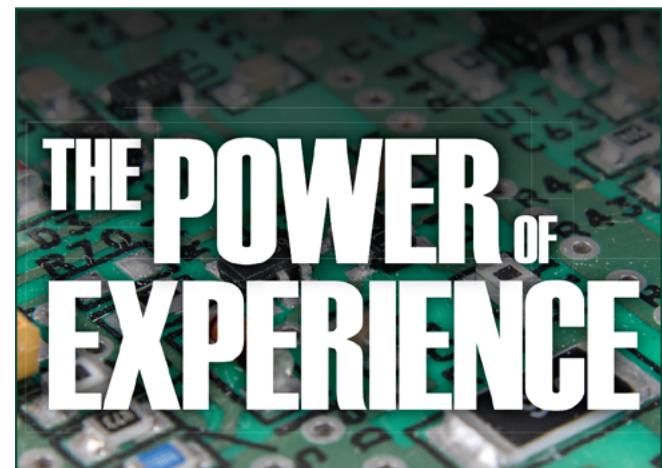
Test methodology

The next sections discuss the scope, material, and parameters of the test methodology.

Scope. The evaluation will cover the debonding and warpage adjust process for chip-first 200mm wafers. Uniformity of the chuck used for the comparison is pre-examined and has a set point tolerance of $\pm 2^\circ\text{C}$. **Figure 3** shows the heat distribution and statistics across a 300mm chuck at different temperatures.

The debonding parameter is also set to 190°C at 40s for the thermal release tape, ensuring good debonding quality and repeatability, as well as no residue encountered during the detaping process. Parameters used are based on an initial investigation by ERS [2] as detailed in **Table 1**, adding 20s soak time, so it replicates the detaping time.

Material. A 200mm wafer will be used for the experimentation on a 300mm chuck. The wafers have already been debonded from the carrier and initial warpages are known. This will allow comparison of warpages pre- and post-processing. The wafer has the following attributes: 1) Thicknesses: $900\mu\text{m}$ and $600\mu\text{m}$; 2) Die size: 5mm x 5mm; and 3) Pitch: 6mm x 6mm.



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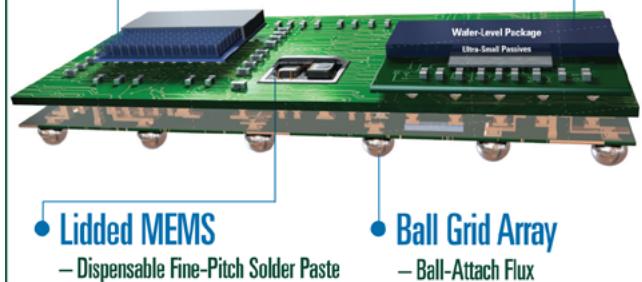
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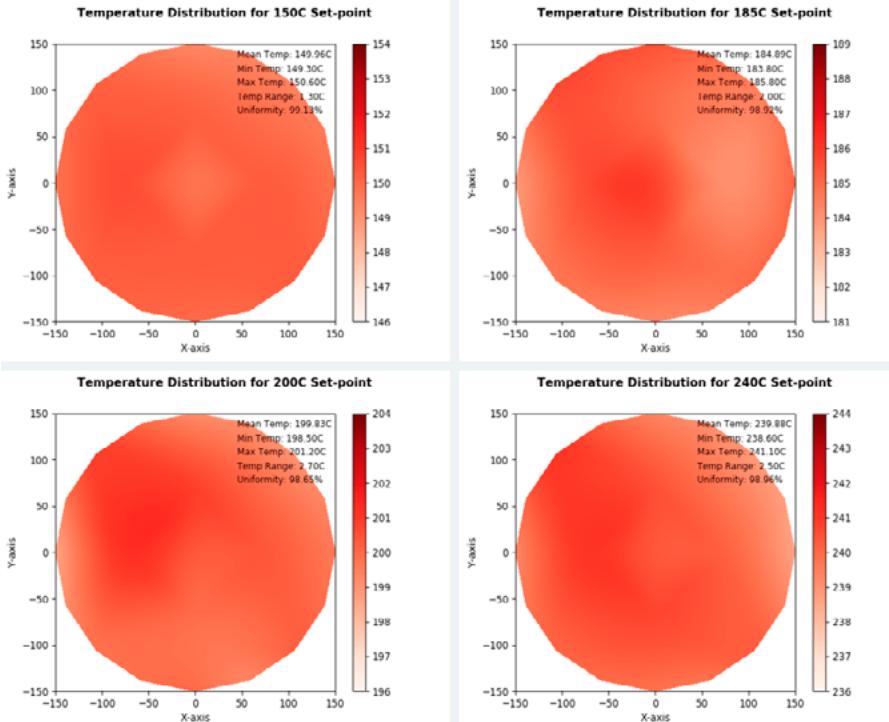


Figure 3: Heat map of the 300mm chucks at 150°C, 185°C, 200°C, and 240°C.

SN	TEMP (°C)	HANDLING METHOD	INITIAL WARPAGE
THICKNESS 1 (900um)			
W# 1	150	Contactless	2.3mm
W# 2	170	Contactless	1.9mm
W# 3	200	Contactless	2.5mm
W# 4	150	Pick and Place	3.2mm
W# 5	170	Pick and Place	2.6mm
W# 6	200	Pick and Place	2.3mm
THICKNESS 2 (600um)			
W# 7	150	Contactless	1.9mm
W# 8	170	Contactless	1.6mm
W# 9	200	Contactless	1.8mm
W# 10	150	Pick and Place	1.7mm
W# 11	170	Pick and Place	2.0mm
W# 12	200	Pick and Place	2.3mm

Table 1: Initial warpage on wafers at different temperatures.

Parameters. The experimentation will have three parameters: 1) Warpage adjust temperature: 150°C, 170°C and 200°C; 2) Wafer thickness; and the 3) Wafer handling method. The handling method is the technique used to transport the wafer to different chucks. Wafer transport is critical in three areas of processing as shown in **Figure 4**.

Contactless transport, as the name itself implies, is transportation without contact. Examples of this method are the Bernoulli handling and AirCushion system. For this experiment, the contactless transport utilizes ERS' AirCushion and TriTemp slide system. For pick-and-place, a conventional end-effector was utilized (see **Figure 5**).

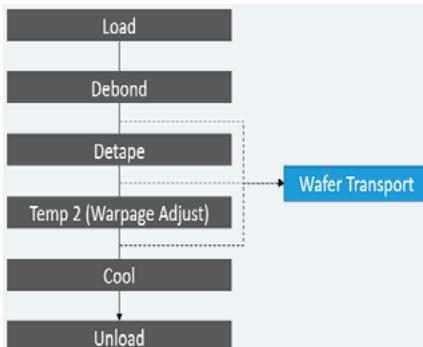


Figure 4: Process flow of the experimentation.



Figure 5: Simple end-effector for semiconductor automated machines.

Debond Temperature (°C)	Debond Time (sec)	Foil release (%)
180	10	2
180	15	75
180	20	98
190	10	80
190	15	95
190	20	100
200	10	90
200	15	95
200	20	100

Table 2: Foil release vs. debonding temperature and time parameter setting [3].

Results

Warpage improvement has been observed in all the samples processed. The significant observations are as observed in **Figure 6** and **Table 3**:

- For contactless transport, increasing temperature from the warpage adjust temperature leads to increased improvement on the warpage.
- The pick-and-place method shows reduced impact on warpage at higher temperatures and thinner wafers.

SN	INITIAL WARPAGE (mm)	OUTPUT WARPAGE (mm)	ΔWARPAGE (mm)
W# 1	2.3	2	0.3
W# 2	1.9	1.1	0.8
W# 3	2.5	1.5	1
W# 4	3.2	2.6	0.6
W# 5	2.6	1.9	0.7
W# 6	2.3	1.8	0.5
W# 7	1.9	1.5	0.4
W# 8	1.6	0.8	0.8
W# 9	1.8	0.9	0.9
W# 10	1.7	1.2	0.5
W# 11	2.0	1.7	0.3
W# 12	2.3	2	0.3

Table 3: Warpage impact of the experimentation.

It was also observed that the heat dissipation is very uniform during contactless transport from hot to cool chucks, compared to a pick-and-place method. In pick-and-place, the end effector affecting the wafer temperature before cooling is very evident in **Figure 7**.

Summary

The chip-first type FO can benefit from thermal treatment to reduce warpage. A contactless handling method during the debonding and warpage adjustment process

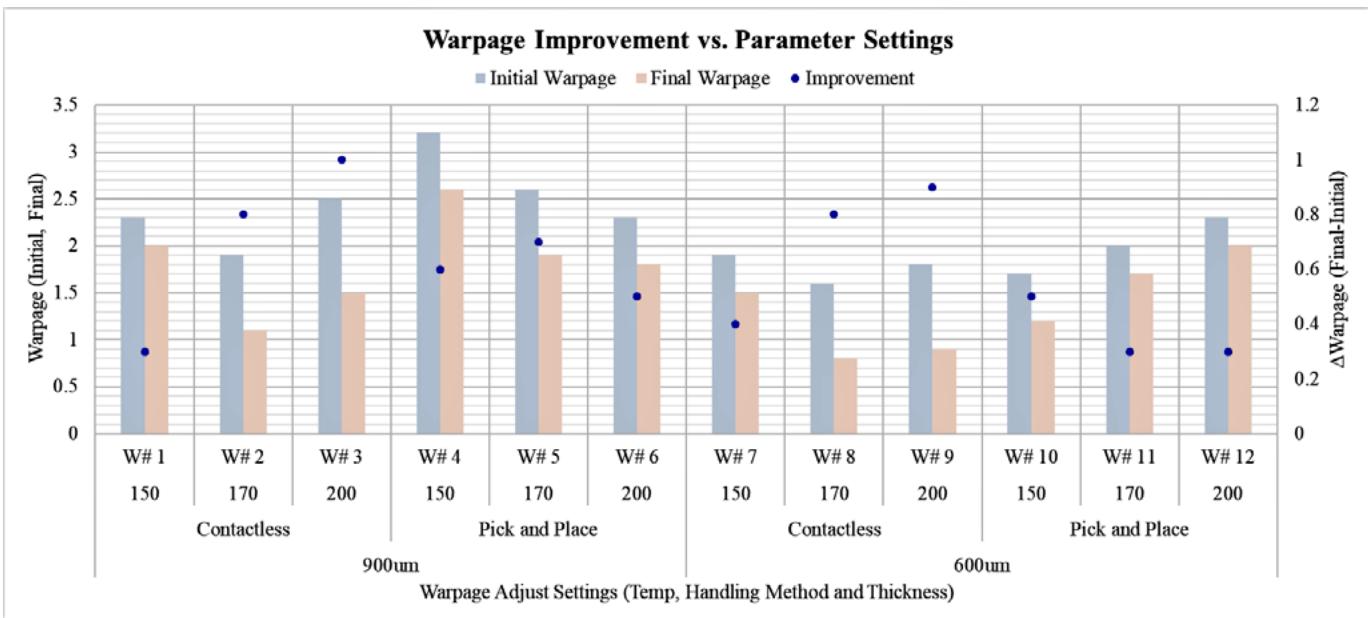


Figure 6: Graph of warpage improvement vs. parameter settings.

allows minimum, to no introduction of warpage, as shown in the 200mm wafer experiment. Further investigation, however, is needed to see if contactless transport proves to be more efficient compared to a pick-and-place method.

Acknowledgment

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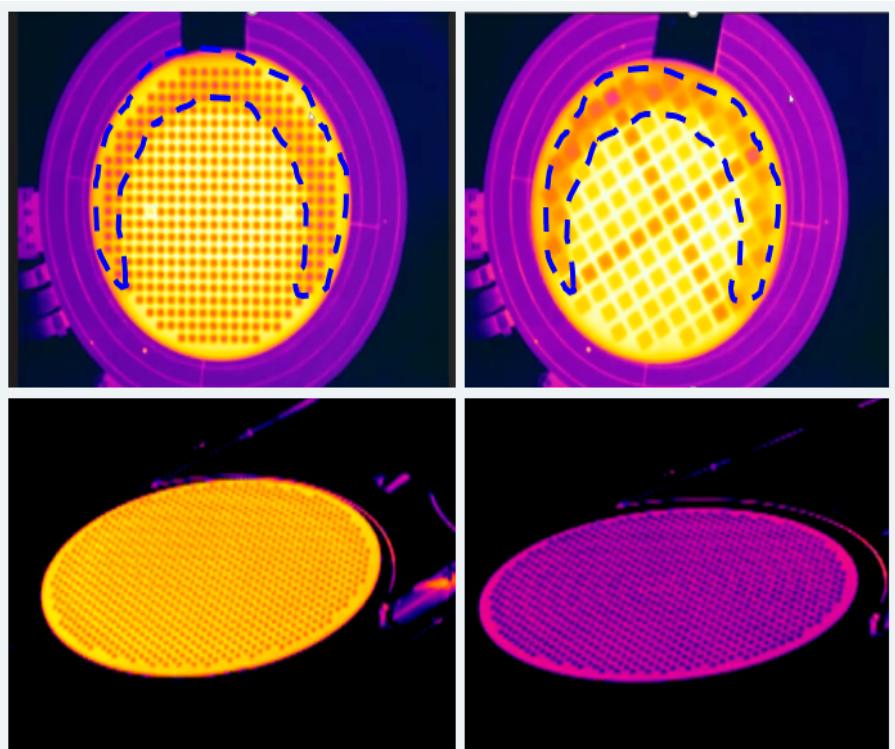


Figure 7: Heat dissipation between contactless vs. the pick-and-place transport method.



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Where are we with HDAP LVS verification?

By Tarek Ramadan [*Mentor, a Siemens Business*]

High-density advanced packaging (HDAP) combines multiple integrated circuit (IC) dies in a single package. This heterogeneous integration provides an improved form factor and enhanced functionality when compared to other packaging technologies, but presents some tricky verification challenges, because each of those die may be built using a different technology node.

Like any electronic product, HDAP designs require extensive verification to ensure they will perform as intended, and can be reliably manufactured in sufficient quantities to meet market demand. Unlike traditional ICs, system-on-chips (SoCs), or printed circuit boards (PCBs), however, automating HDAP verification requires combining elements of both IC and package verification. This has proved to be somewhat challenging for the electronic design automation (EDA) industry, though it has invested a significant amount of time and research into categorizing the issues and developing solutions, and progress is being made.

To begin with, the general concept of qualified assembly design kits (ADKs) that are similar to foundry-qualified process design kits (PDKs) for ICs [1-3] has become at least a limited reality [4]. Assembly-level layout vs. schematic (LVS) verification for HDAPs [5-6] now has at least one EDA solution [7]. The value of post-layout simulation for analog and post-layout static timing analysis (STA) for digital flows for HDAPs is now well-understood [8], as is the need for an automated approach that generates HDAP system-level connectivity while accounting for die, package, and die/package interface parasitics [9].

While the maturity and scope of the processes needed to make HDAPs a viable market option may still be in development, this seems a good time to assess where we are. To get an idea of how far we've come, and where we need to go, let's take a closer look at one particular process—package LVS

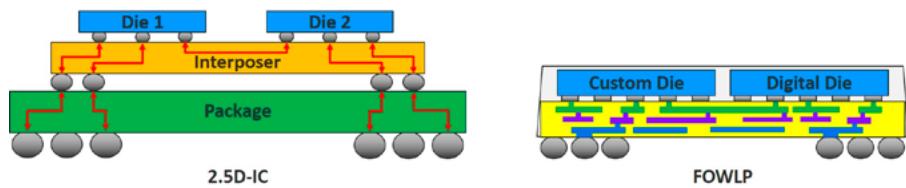


Figure 1: 2.5D interposer-based and FOWLP designs are the HDAP technologies currently used most frequently.

verification—using the two HDAP designs that are currently the most popular: 2.5D (interposer) and fan-out wafer-level packaging (FOWLP), shown in **Figure 1**.

HDAP LVS verification

We all know that an SoC can't be submitted to manufacturing unless the geometries that are present in the physical layout implement the connectivity and circuit performance created in the schematic/design intent. LVS verification is a mature, well-established, highly-automated flow in the SoC design world. To support the automated LVS process, LVS tools require a consistent set of data: 1) Layout database (GDSII, OASIS, or LEF/DEF); 2) Source netlist (SPICE or Verilog); and 3) LVS rule deck (format depends on EDA tool used).

The layout database and source netlist are created by the design company for each SoC design, while the LVS rules deck is typically created and provided by the foundry, and is independent of any single SoC. Design companies, foundries, and EDA suppliers all understand and agree that SoC LVS verification can't happen without some combination of these three inputs.

When we start to look at HDAP LVS verification, we immediately see major differences. The most obvious and most critical is that design companies, foundries, outsourced assembly and test suppliers (OSATS), and EDA suppliers are neither in alignment, nor agreement, on the set of inputs required for an HDAP LVS flow. This disconnect exists for three reasons: ownership, data availability, and design dependence.

Process ownership

Because HDAP is still an emerging technology, the responsibility for HDAP verification can vary from team to team and company to company. For example, some design companies see 2.5D design and verification as a “more SoC, less packaging” activity, and assign design and verification tasks to SoC and/or computer-aided design (CAD) teams experienced in SoC verification requirements and formats, but with limited packaging experience. FOWLP design and verification, on the other hand, is viewed as a “less SoC, more packaging” activity, so responsibility often goes to a packaging team that is less familiar with SoC verification requirements and formats. The bottom line is that foundries, OSATS, and EDA companies cannot impose a single, uniform set of processes and conditions when supporting HDAP design companies using diverse methodologies and requirements. Flexibility is essential to success.

Data

To run full-package LVS verification, all the data for all the HDAP components must be available. For example, in a FOWLP design, designers require: 1) Die1 through DieN layout design databases; 2) FOWLP design database; and 3) FOWLP system source netlist (in some form).

So what happens if the FOWLP design database (owned by the packaging team) is ready, while the individual die databases (owned by the SoC teams) are still being developed? If the FOWLP designer has to wait until all the dies are built and verified to run the FOWLP LVS and find out that the FOWLP design database is full of shorts,

opens, and other errors, the schedule is already blown. HDAP designers must have something they can do during early verification to fix obvious HDAP LVS issues, even before the full LVS verification can be completed. To enable and support this kind of early verification in a timely manner, they need an automated methodology for HDAP LVS checking that can be run without all the final components.

Design dependence

In SoC LVS verification, the LVS rules deck is only dependent on the SoC technology node information (i.e., GDSII layers). HDAP LVS adds another complexity: die placements. While an HDAP LVS rule deck is obviously dependent on the GDSII layers of the interposer, die1, die2, etc., it is also dependent on where the dies (and interposer for 2.5D) are placed in the HDAP design itself. However, it would be an exhaustive, and nearly impossible, process for the foundry/OSATS to build HDAP LVS rule decks that account for all possible die and interposer placement combinations. Even if such rules were possible for a “two dies on an interposer” design, it quickly becomes impractical as the number of dies and substrates increase in HDAPs.

So, with the acknowledgment that HDAP verification flows on the design side are far from mature, the EDA companies have to ask: What level of HDAP LVS verification can be achieved with different levels of package knowledge and expertise, and different types of available data? The answer might surprise you. Let’s explore what HDAP LVS verification might look like in different flows for different cases.

HDAP LVS options

The following sections discuss various HDAP LVS verification flow options.

Package/interposer connectivity checking without a schematic/design intent. The concept of a “source netlist” in a standard format is still relatively new to package designers. Traditionally, they use manual spreadsheets to plan the connectivity from die to package to external I/O on a PCB design. Although it’s difficult to apply this methodology to HDAP verification, some HDAP designers still use spreadsheets, whether it’s because the pin count number is so low that it is practical, or they’re simply resistant to change. However, the format and organization of those spreadsheets varies from one company

(or even designer) to the next, making it virtually impossible for EDA companies to support all possible spreadsheets.

But if using these different spreadsheet formats isn’t practical, there’s still a package design database, isn’t there? Is there no way to do simple opens/shorts checking just with this data? Actually, there could be. EDA tools can implement a simple automated approach that still provides useful information to designers:

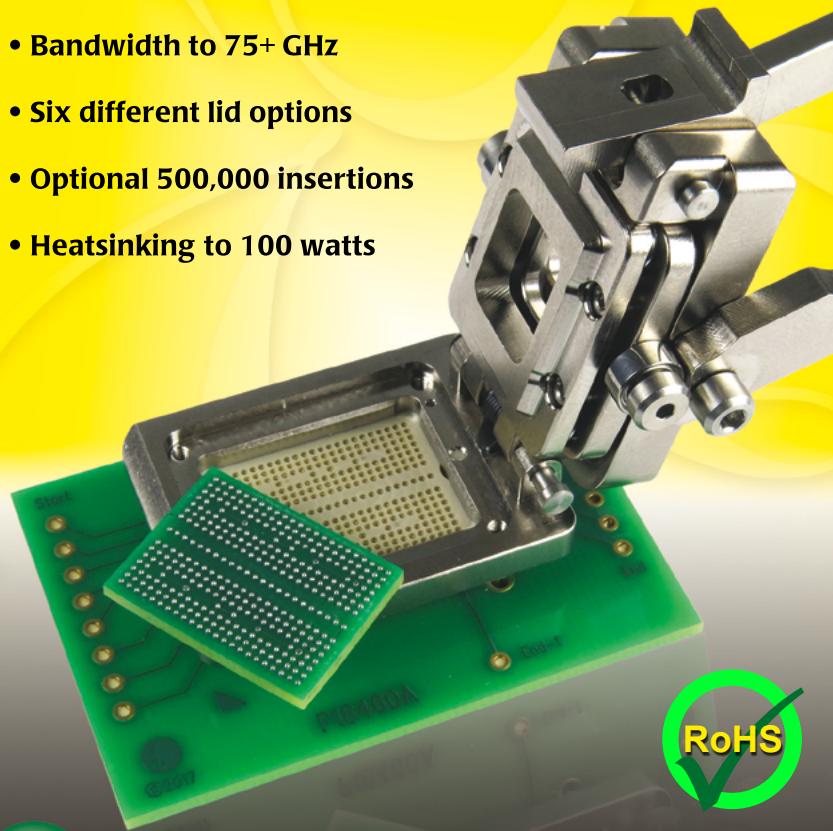
- If two shapes in the package design database have the same text labels while they are physically disconnected, this is reported as an “open,” and
- If two shapes in the package design database have different text labels while they are physically connected, this is reported as a “short.”

Although this certainly isn’t comprehensive LVS verification (as there is

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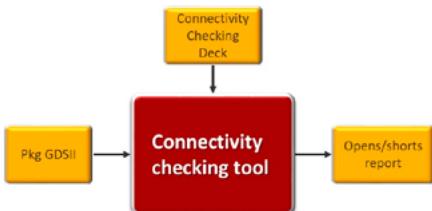


Figure 2: HDAP connectivity checking without a design intent.

no design intent with which to compare), it's still a valuable open/short checking process that can be used without a source netlist (yet). **Figure 2** shows the block diagram of this simple open/short checker.

Package/interposer LVS without die pins. In the next case, the verification data includes both a package design database and a source netlist, so HDAP designers should be able to run a true LVS verification. While their first thought is probably to use the same LVS tools and methodologies used for SoC LVS, thinking a little further reveals that that approach is not suitable for this specific process. The concept of LVS in an SoC is dependent on the existence of “devices” in both the SoC layout design database and the source netlist. These devices can be active (transistors) or passive (resistors, capacitors, etc.). Because most 2.5D-IC and FOWLP designs don't include any devices (just metal routing), SoC LVS tools simply aren't practical.

The more viable solution is to use assembly-level LVS tools that, by default, account for the non-existence of devices in packages. However, these tools require more than just the package layout design database for assembly-level LVS—they also require the layout design databases for the dies. But there's a solution! As long as the input spreadsheet netlist includes die bump (x,y) coordinates and pin names, the functionality in assembly-level LVS tools can be enhanced to automatically generate “placeholder” die bumps (representing the die). This “die placeholders” design database can then be used in the assembly design database to successfully run HDAP LVS using only the package layout design database and input spreadsheet netlist. A block diagram for the HDAP LVS without die pins flow is shown in **Figure 3**.

Although the flows described above provide obvious value to the customer (capturing any physical shorts/opens in the package design database), the full HDAP assembly still can't be guaranteed to function successfully. What if there is a misalignment between a die and the package in the HDAP?

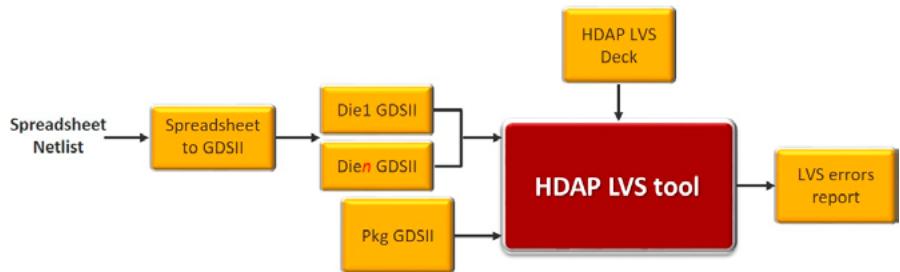


Figure 3: Running HDAP LVS without die pins.

Assembly-level LVS/alignment verification. In an HDAP, alignment verification is equally important as LVS, especially when rotation or scaling is required (e.g., a die is shrunk by 10%, rotated 90°, then placed on the package). HDAP designers must ensure that, even after such processing, there is still sufficient overlap between the package bumps and die bumps. There are two levels of alignment verification possible, depending on what data the HDAP designer can obtain.

Geometrical die interface only. If HDAP designers only have access to the die interface (bumps) GDSII layer, they can still perform both alignment and package LVS verification. Designers can use EDA tools to automatically place the die(s) on top of the package/interposer and verify the alignment (as required). However, if an extra pin exists in the SoC design database or in the package design database, it is not captured when using this flow.

Geometrical die interface + logical die pins. In this flow, all interface information (geometry and pins) from the die(s) is available. HDAP designers have all the required data for comprehensive HDAP LVS/alignment verification, and can run this flow as a sign-off flow. Designers can validate all possible violations: 1) assembly-level LVS; 2) assembly-level alignment; and 3) extra/missing pins.

From a connectivity perspective, however, there is an issue of which designers should be aware when including both the die(s) and the package in assembly-level LVS. If the SoC team uses a different naming methodology for the die pins/nets than the package team, the SoC layout design database may contain a die pin called “A,” while in both the system source netlist and the package design database, the pin is referred to as “A_B.” Such disparities result in many false LVS violations. This issue was irrelevant in the geometrical die interface only flow, because the only data the HDAP designer imported from the die was the

“interface physical geometry,” not the “interface logical pins.” As for solving these pin names/net names mismatches between the SoCs and HDAPs, EDA companies are supplying novel approaches to accommodate such issues without creating false LVS violations. For example, HDAP designers can denote such inconsistencies as waivers on input. **Figure 4** shows the assembly-level LVS/alignment with die pins flow.

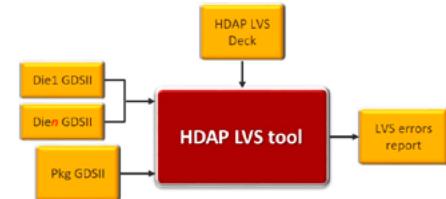


Figure 4: Full assembly-level sign-off LVS/alignment, including die pins.

Summary

As HDAP technologies become mainstream, designers require qualified design rules from foundries/OSATS, and reliable sign-off automated verification flows from EDA companies. The development of package ADKs is addressing the first requirement. While current HDAP verification flows are far from mature when compared to well-established SoC verification flows, EDA companies are providing automated tools and flows that can take into account the various levels of data availability, while still enabling HDAP designers to perform useful and valuable HDAP LVS/alignment verification flows.

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Biography

Tarek Ramadan is a Technical Marketing Lead for Calibre Design Solutions at Mentor, a Siemens Business, based in Cairo, Egypt. He supports Calibre physical verification solutions for 2.5D-IC, 3D-IC, and wafer-level packaging applications. Tarek holds BS and MS degrees in Electrical Engineering from Ain Shams U., Cairo, Egypt. Email: tarek_ramadan@mentor.com.

Bonding processes for wafer-scale vacuum encapsulation

By Tony Rogers, Anna Draisey, Roger Dyer [Applied Microengineering Limited]

Over the past few decades, microelectromechanical systems (MEMS) technologies have been implemented in the sensors and actuators industry to vastly improve the price:performance ratio for a wide range of devices. For many of these MEMS devices, it has been necessary to include a wafer bonding step in the fabrication sequence, in particular when there is the need to incorporate a sealed cavity into the device design. For some devices (e.g., pressure sensors, bolometers), the sealed cavity needs to contain a vacuum, whereas for others (e.g., accelerometers and atomic clocks) it is necessary to encapsulate a gas at a defined pressure. Although the wafer bonding step is a key technology in the design and, importantly, enables the concept of wafer-level packaging to be utilized, there are many other necessary building blocks required in the wafer-scale packaging of encapsulated devices. These necessary technologies include: 1) Wafer bonding; 2) Provision of electrical feedthroughs; 3) Interconnection; and 4) Maintenance of vacuum (or gas composition) in sealed cavities.

For the wafer bonding step, there are numerous available processes and it is often necessary to define the optimum technique based on the required device characteristics and the application limitations. A selection of available techniques is listed in

Table 1. Note that for CMOS compatibility, the wafer bonding process temperature needs to be <400°C.

For long-term hermeticity, which is an essential requirement for encapsulated devices, it is necessary to use a metal-based bonding frame. No matter what type of bonding process is used, however, it is essential to ensure that the two wafers are bonded in such a way that a high-quality vacuum is established in the sealed cavities. To achieve this, it is essential that the vacuum chamber can achieve $<10^{-5}$ mbar, and most importantly, that the wafers are thoroughly outgassed prior to contacting. This requirement puts specific demands on the wafer bonding equipment, which must comply with the following:

- Wide gap between the platens to ensure fast and efficient pumping of the cavities;
- Capability of in situ oxide removal via a surface chemistry process;
- Ability to heat the platens to different temperatures (e.g., for getter activation or outgassing); and
- Ability to back-fill with a gas and hold the pressure to a defined value (e.g., for damping of accelerometers).

The longer-term maintenance of the vacuum level in the sealed cavities is best dealt with by the inclusion of a thin-film getter.

With regard to electrical feedthroughs, the use of vertical vias embedded in the wafers is the most space-efficient method for enabling electrical signals in/out of the sealed cavities and it is possible to keep development costs low by utilizing arrays of feedthroughs already embedded in bought-in wafers. Examples of these are Hermes wafers (tungsten pins embedded in glass wafers from Schott) [1], and polysilicon vias embedded in silicon wafers from Silex and Icemos [2].

Examples of wafer-level encapsulation

Some of the building blocks discussed in the previous section are utilized in the following production examples of wafer-level encapsulation.

Pressure sensor. In this application, an aligned, anodic-bonding, vacuum encapsulation process is performed at the wafer-level to realize an absolute pressure sensor. The device works as an absolute pressure sensor by incorporating vacuum reference cavities into each chip on the wafer. The vacuum level inside each cavity is then maintained by the incorporation of a getter. Unfortunately, the 500°C activation temperature of the getter was higher than the maximum temperature limit for some aspects of the device design. To overcome this restriction, the device was designed such that the temperature-limiting components were on one wafer, whereas the thin-film getter was included on the other wafer. A suitable aligner bonder (Model AWB from Applied Microengineering Limited) was then used to perform the sequential getter activation followed by wafer bonding steps. This aligner-bonder system features differential heating and a large platen separation. Additionally, this capability allowed the getter activation followed by wafer bonding to be successfully performed – and after the activation process, the getter wafer was allowed to cool down to the

Wafer bonding Process	Temperature Range (°C)	Benefits	Drawbacks
Direct	1000°C anneal	No interlayer	High T anneal needed
Low T direct	RT bond 300°C anneal	No interlayer	
Anodic	300 - 450°C	High strength, low cost hermetic bond	Glass substrate needed
Thermo-compression	RT – 400°C (material dependent)	High hermeticity	High bonding force needed
Eutectic / SLID	160 - 450°C depending on materials	High hermeticity	Need to remove surface oxides
Glass frit	300 - 450°C depending on frit type	Mature process	Not area efficient, and many temperature dwells are required to remove binder
Adhesive	RT – 200°C	Low T processing	Poor hermeticity

Table 1: A selection of wafer bonding techniques suitable for wafer-level encapsulation.

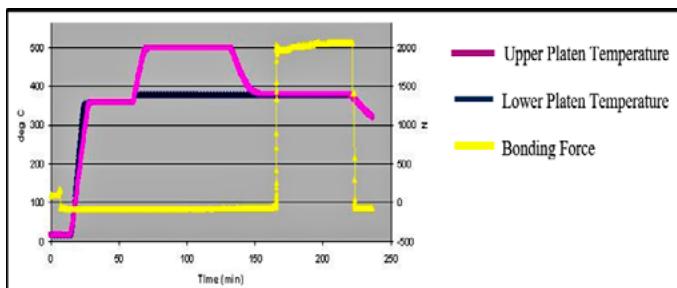


Figure 1: Temperature and force time profiles for the getter activation and bond.

bonding temperature without breaking vacuum. The temperature profile for the above procedure, plus other bonding parameters, are shown in **Figure 1**. Note that during the heating and wafer bonding steps, the pressure in the process chamber was $\sim 10^{-5}$ mbar. Subsequent evaluation of the resulting MEMS absolute pressure sensors determined that the pressure in the vacuum reference cavities was $< 10^{-2}$ mbar.

Vacuum encapsulation of a bolometer. This device, first presented at IWLPIC 2016 [3], required the development of a CuSn SLID bonding/wafer-level packaging process for thermal imagers and the resulting devices demonstrated performance equal to that of similar devices packaged using conventional individual die-level methods. However, the wafer-level vacuum encapsulation process technology enabled dramatic improvements in size, weight and cost of the thermal imaging devices and the same process technology offers similar advantages to other MEMS sensors requiring vacuum or hermetic packages. The process is summarized in **Figure 2**.

Cu-Sn SLID Bonding

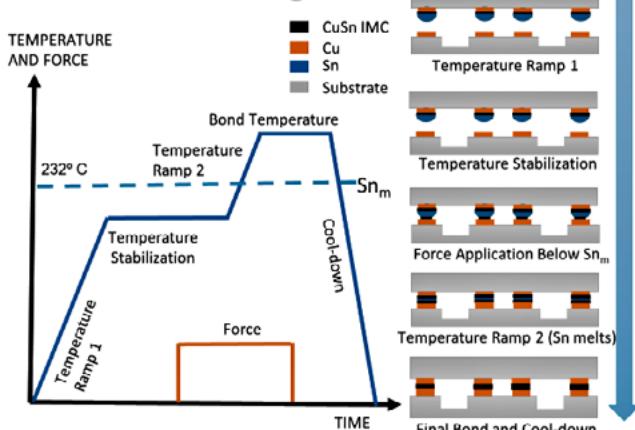


Figure 2: Temperature/time profile for wafer-level device fabrication. SOURCE: Used with permission of Allan Hilton/Micross [3].

The degree of vacuum in the devices is key to successful operation and a good vacuum ($< 10^{-2}$ mbar) is required for the following: 1) To thermally isolate pixels from their surroundings; 2) Improve detector sensitivity; and 3) Improve signal-to-noise ratio.

In order to achieve the above features, the device design included a thin-film zirconium alloy patternable getter for maintaining the vacuum level in the cavities. The thin-film getter materials are products specifically designed for vacuum packaging of MEMS. Companies such as SAES offer a variety

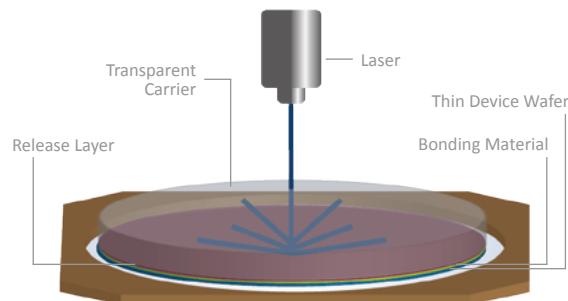


Creating Safe Environments

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of different solutions that enable high-vacuum performance, long-term stability and device reliability. The getter films are a common and technically-accepted way to maintain and control vacuum in hermetically-sealed MEMS used in a large number of applications, such as defense and security, automotive, industrial and consumer. The getter features and applications are as follows:

Getter features: 1) High vacuum; 2) Long-term stability; 3) High sorption capacity for all active gases; 4) Activation temperature compatible with all main packaging procedures; 5) Different patterning methods; and 6) Particle free.

Getter applications: 1) Uncooled IR sensors; 2) Gyros; 3) Resonators; 4) Time frequency devices; and 5) High-end pressure sensors.

To prevent premature activation, the getter should not be heated above 250°C and the device fabrication exploited the large gap between the two platens in the bonder process chamber to enable thorough outgassing before the in situ alignment step (required to align the patterns on the two wafers to be bonded) and subsequent contacting and hermetic sealing of the two wafers. The getter was then activated during the 260°C wafer bonding step.

Discussion

Neither of the above examples of wafer-level encapsulation could have been achieved without the use of an aligner wafer bonder capable of in situ alignment. The in situ aligner bonder is best described with reference to **Figure 3**, which shows a schematic of the process chamber.

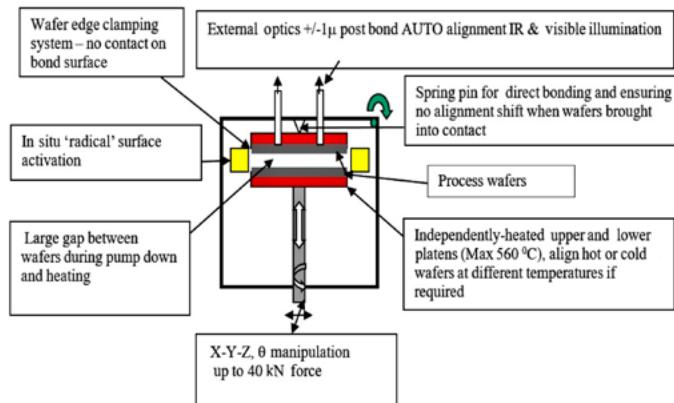


Figure 3: Schematic of the process chamber of the aligner wafer bonder.

A key feature of the in situ aligner wafer bonding system is the large gap between the platens. This difference between the aligner wafer bonder and conventional wafer bonding tools is key for wafer-level encapsulation applications.

Figures 4-7 demonstrate the essential differences between conventional wafer bonding equipment and the design of the AML aligner wafer bonder with regard to the following: 1) Capability for in situ chemistry; 2) Capability for differential platen temperature; 3) Simultaneous heating, alignment and fast vacuum pumping; and 4) Outgassing of the process wafers and accurate measurement of chamber pressure.

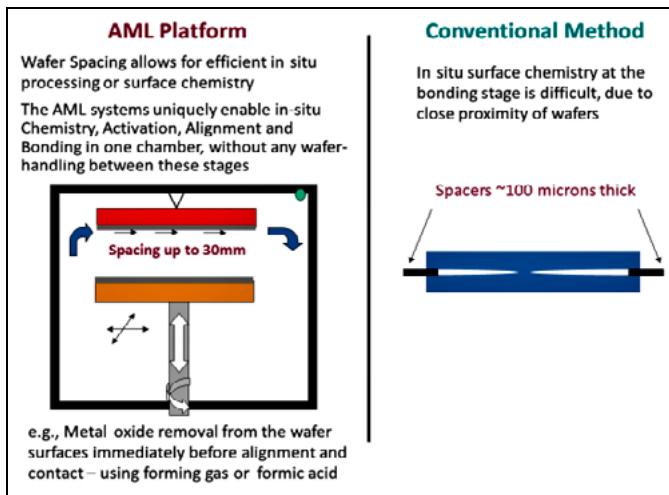


Figure 4: Comparison of aligner wafer bonders and conventional wafer bonders for performing in situ chemistry [4,5].

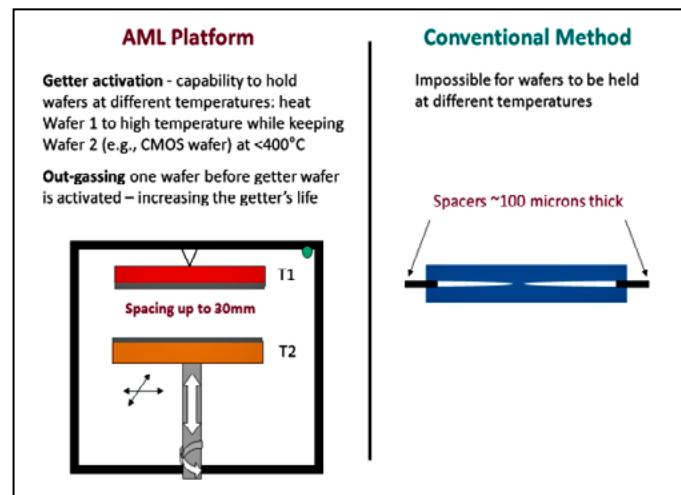


Figure 5: Comparison of aligner wafer bonders and conventional wafer bonders for maintaining a temperature differential between the two platens.

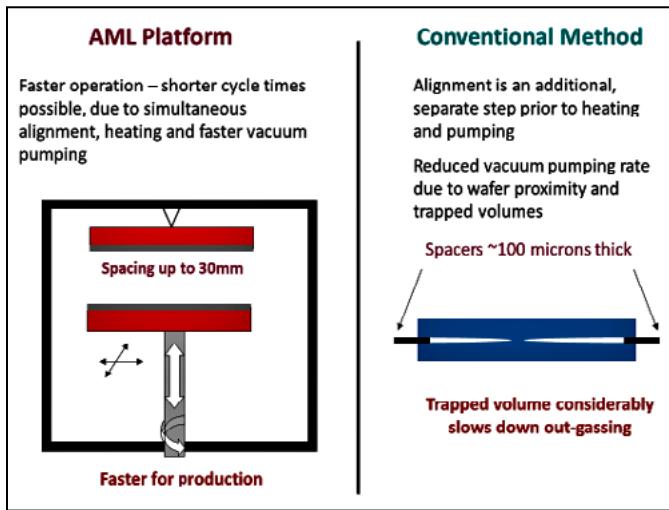


Figure 6: Comparison of aligner wafer bonders and conventional wafer bonders for heating, alignment and vacuum pumping.

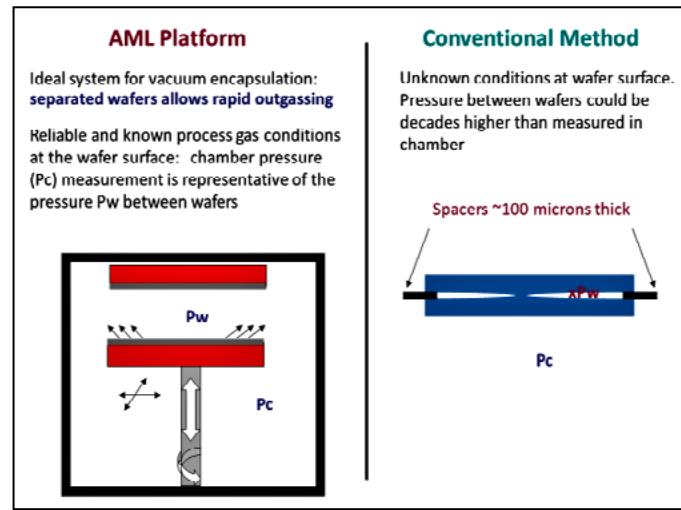


Figure 7: Comparison of aligner wafer bonders and conventional wafer bonders for outgassing.

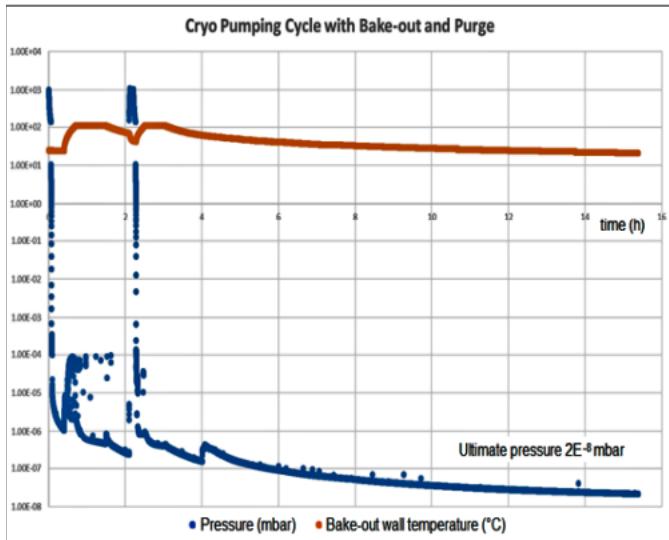


Figure 8: Pump down performance.

AML bonders have been extensively used for many years for vacuum encapsulation applications for which their in situ align and bond design is ideally suited. However, the systems have previously been limited to vacuum levels of 10^{-6} mbar, which has excluded their use in some application areas. To address this, the latest system design allows integration of an optional cryopump and enables ultra-high vacuum (UHV) levels to be achieved. One important, high-growth area that requires UHV conditions is quantum computing for which vacuum levels in the low 10^{-8} mbar range are required. Other applications that benefit from the UHV capability are surface-activated bonding and thermal imaging, especially when using vacuum encapsulation wafer-level packaging. **Figure 8** shows the vacuum performance of the new UHV bonder.

The purge step was included in the pump-down procedure because this spreads the heat from the internal bake-out heater more effectively around the chamber to promote more outgassing, resulting in a slightly faster pump-down time. For pressure control, the UHV bonder also includes a turbomolecular pump, and this makes the bonder compatible with the AML radical activation/surface etch tool for which pressures of 1mbar are required.

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Following this procedure, the machine can be switched back to cryo pump mode to achieve UHV conditions, thereby opening up the possibility for surface-activated bonding (SAB) applications.

Summary

The following conclusions can be made from the data presented in this work:

- The AWB system is well-suited for wafer-level vacuum encapsulation of MEMS;
- Numerous wafer-bonding processes exist that can be used to achieve vacuum encapsulation;
- The support infrastructure exists for procurement of items such as feedthrough wafers and getter materials that facilitate wafer-level vacuum encapsulation;
- The AWB system is suitable for MEMS applications requiring encapsulated vacuum levels of $<10^{-2}$ mbar; and
- For UHV applications, a cryo-pumped version of the AWB bonder is available.



Biographies

Tony Rogers is Technical Director and a founder of Applied Microengineering Limited, Didcot, Oxfordshire, UK. He graduated with a 1st class honors degree in Applied Physics from Brunel U. in 1976 and has spent the majority of his career working in MEMS, with a focus on wafer bonding. Mainly working on development of new bonding processes and equipment, Tony has also written and presented numerous articles on wafer bonding. Email Tony@aml.co.uk

Anna Draisey is an Application Engineer at Applied Microengineering Limited, Didcot, Oxfordshire, UK. She received her MSc degree in Electronics Engineering, MEMS faculty, in 2006 from Wroclaw U. of Technology in Poland. Since 2008, Anna has been working for AML, has extensive experience in wafer bonding and is involved in R&D on bonding processes and development of Aligner Wafer Bonder machines. Anna works closely with AML customers on bonding demonstrations, training and customer support.

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INDUSTRY NEWS

TestConX 2020 Preview

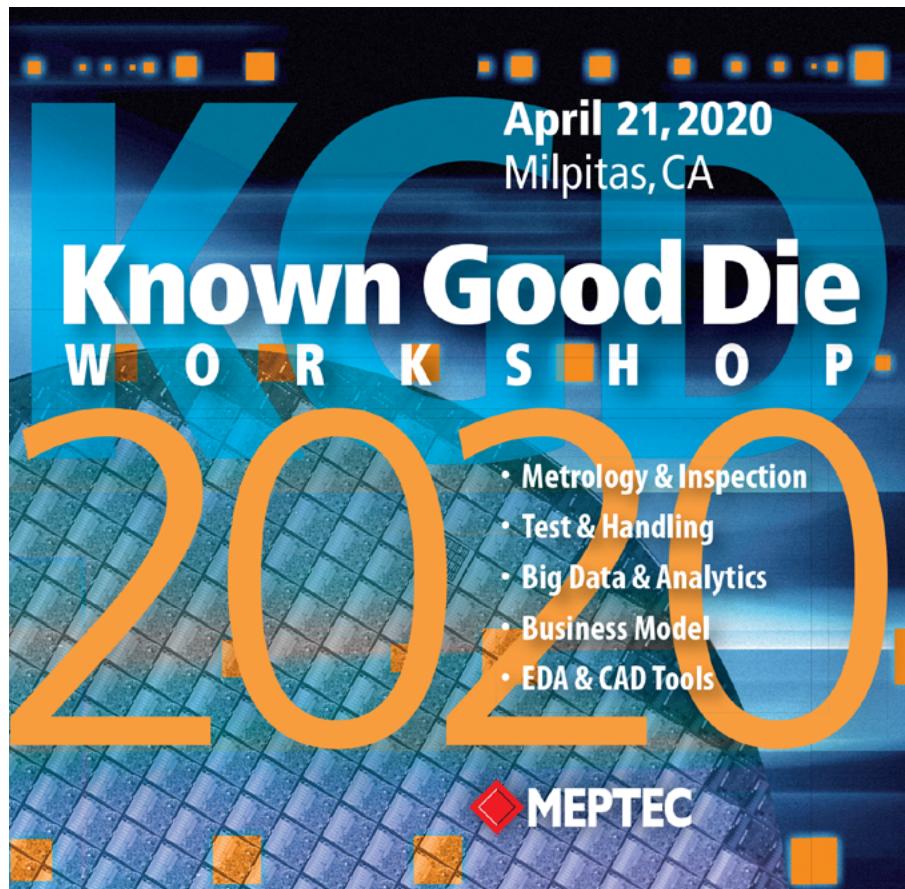
Ira Feldman, General Chair

TestConX returns to Mesa, Arizona on March 1-4, 2020 for its 21st year. The workshop focuses on *connecting electronic test professionals to solutions*. And this year is no exception with the hottest topics being 5G and millimeter-wave testing. As the mobile operators build out 5G networks and consumer demand increases for compatible smartphones, manufacturers have started to build the supply of next generation baseband solutions. Not only are the silicon die challenging to test at mm-wave frequencies many are being deployed in Antenna-in-Package (AiP) advanced packaging that incorporates one or more antennas. Testing just the die is usually insufficient and robust test solutions need to be developed and deployed to test the device in the AiP. TestConX 2020 will feature two technical sessions on mm-Wave and AiP test solutions.

As the number and types of advanced packaging are rapidly increasing in the era of More Than Moore and Heterogeneous

Integration, test engineers and test solution providers need to understand not just the configuration of the device to be tested but the packaging technology itself. Ross Berntson, President and COO of Indium Corporation, will provide the keynote address "Materials Science Innovation in Advanced Packaging" describing new enabling interconnect and thermal technology.

Other technical sessions at TestConX 2020 include printed circuit board (PCB) design and fabrication for test applications, silicon validation, test cell integration, signal integrity, thermal challenges for test, and contact solutions. The tutorial program on Sunday includes three presentations: two on big-data and machine learning for test and one on socketing for mm-wave applications. Sixty-one exhibitors will show the latest in test consumables and hardware at the popular TestConX EXPO. Add a poster session, numerous networking breaks, and a social event to round out the four-day event.



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