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Chip Scale® REVIEW

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The International Magazine for the Semiconductor Packaging Industry

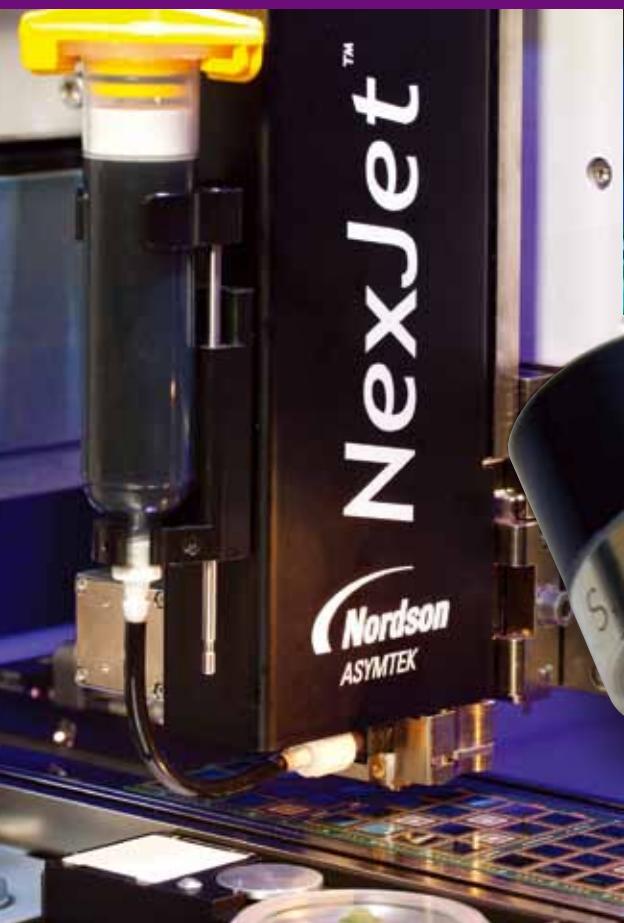
Volume 16, Number 5

September - October 2012

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- **Singulation of QFN/MLP Packages**
- **Solder Paste Dipping & Reflow with PoP Packages Part I**
- **Power Overlay Packaging Platform for High Performance Electronics**
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MEMS sensors currently represent a multi-billion unit market that is growing 24% yr. Along with shrinking footprints, such growth creates challenges for MEMS testing including the fact that packaging affects MEMS performance to a much larger extent than traditional ICs. MEMS devices must also be subjected to physical stimuli, making the move to testing at the wafer level more difficult. But with major challenges come great business opportunities. Cover image courtesy of Fairchild Semiconductor.

Chip Scale
REVIEW

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
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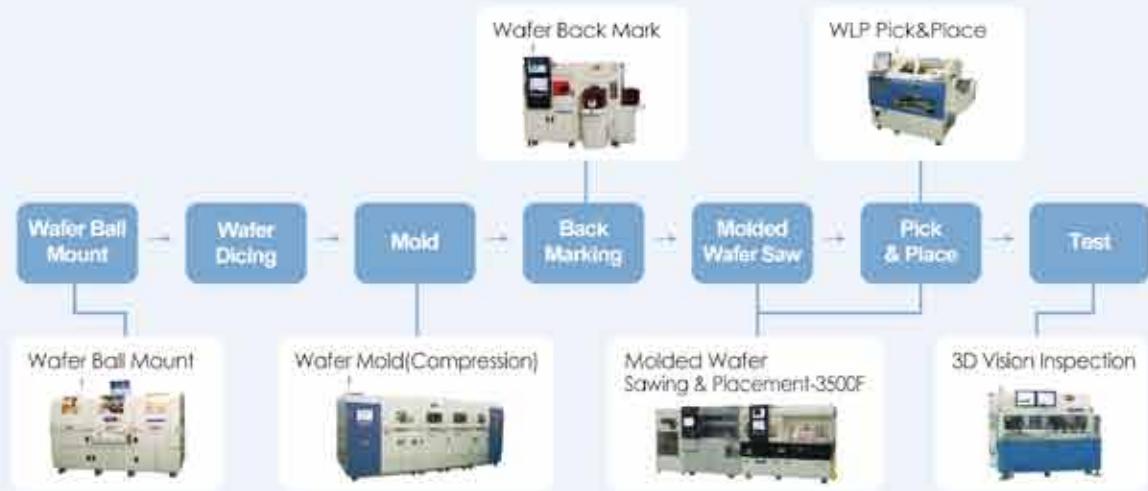
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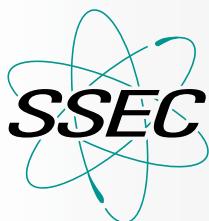
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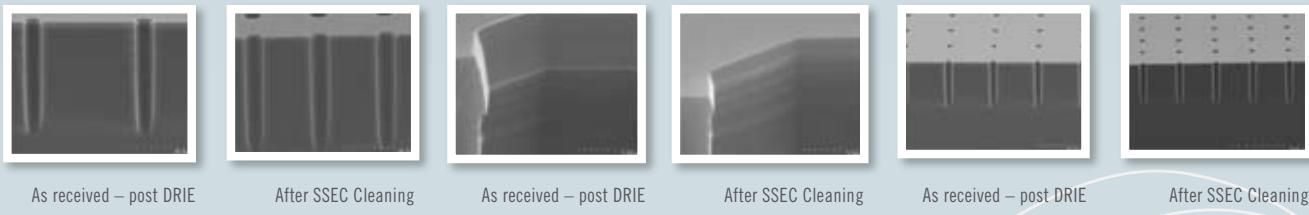


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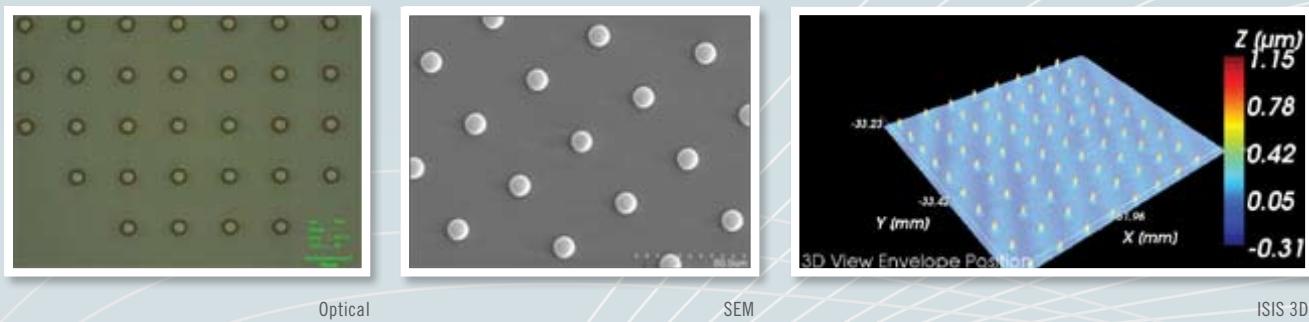
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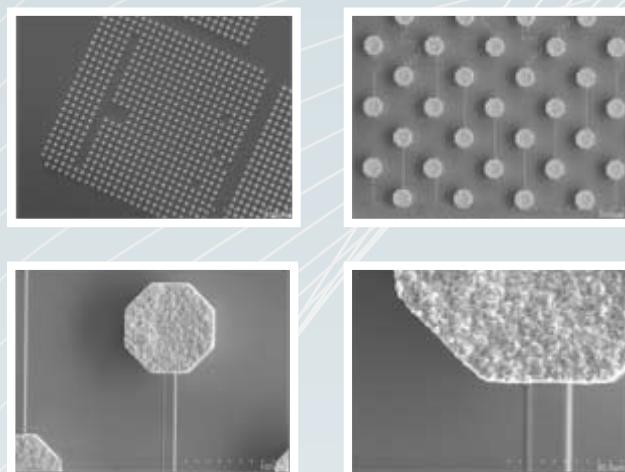
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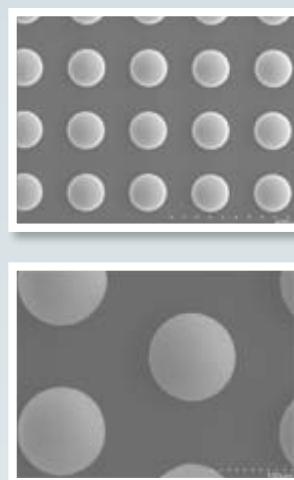
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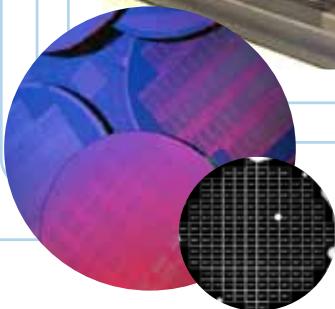
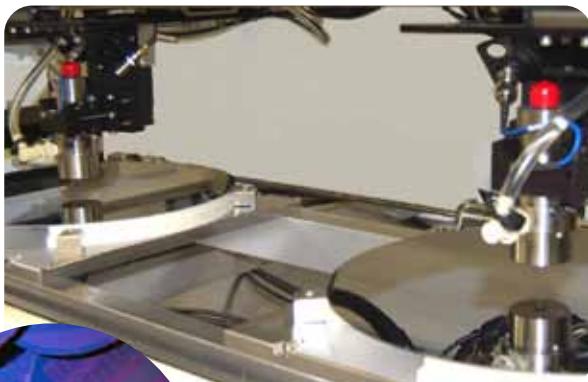
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FROM THE PUBLISHER



Leave Summer Behind - Gear up for Fall

S

eptember signals that it's time to get out of vacation mode and back to the real world. What better way than to open up the September/October issue of CSR and find a variety of technical features that cover MEMS testing, singulation of QFN/MLP packages, power overlay packaging for high-performance electronics, and PoP packaging.

The cover feature describes the dramatic changes taking place in MEMS test systems as a direct result of the MEMS volumes created by the explosion of sensor applications in the mobile market. The result is that the MEMS testing industry is now adopting the handlers and data acquisition systems used for high-volume ICs to address its needs.

We also have two features on the topic of package-on-package, including one on through-mold via technology, and another on solder paste dipping and reflow. Challenges associated with PoP technology arise, not surprisingly, from the constant need for miniaturization driven by mobile applications, along with power electronics (e.g., vehicle electrification and energy efficient products).

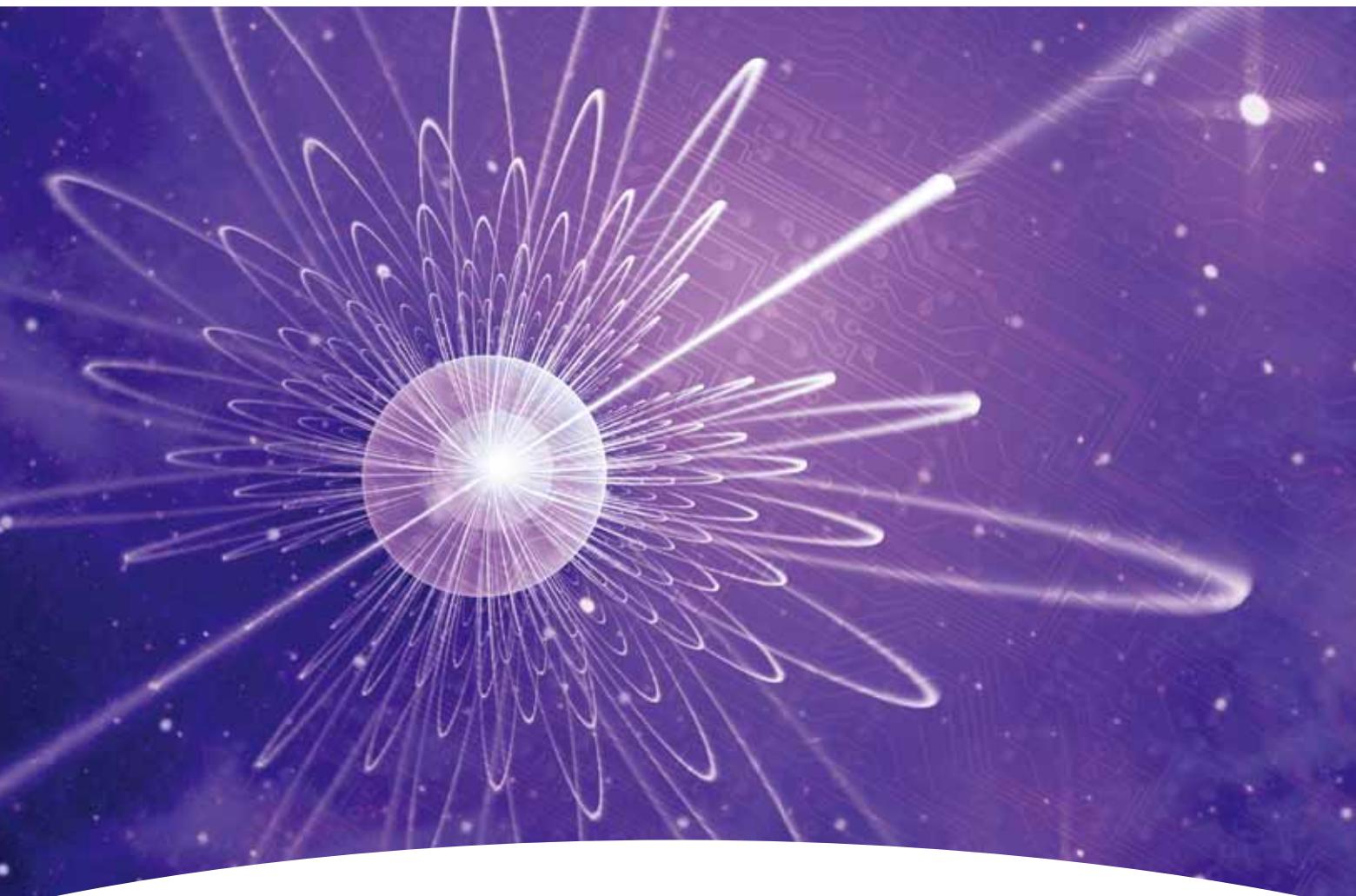
Rounding out the issue is an article on the singulation of QFN/MLP packages that covers the basic substrate characteristics. A comprehensive discussion of factors that impact cut quality, as well as substrate geometry and material characteristics, are presented.

Fall also begins a new "season of shows." Start planning now to attend the 9th annual SMTA & Chip Scale Review co-sponsored event - International Wafer-Level Packaging Conference (IWLPC) Nov 5-8 which will focus on three major technical tracks: wafer-level packaging, 3D integration and MEMS packaging. This four day event will include technical presentations, expert panels, tutorials, and two days of exhibits showcasing the latest technology from 50 leading companies. The keynote dinner speaker, John Ellis, is the best-selling author of *Dormant Curse*. John will present the threat of Cyber-Physical Terrorism in your Smartphone - a very possible threat in the near future. You won't want to miss this keynote! Read more on the keynote in The Industry News section on page 12. Register for IWLPC through the website. The technical conference package is \$600, which includes the keynote dinner. Go to www.iwlpc.com for complete registration details. The early bird rates with savings up to \$100 are in effect through October 5.

In closing, I'd like to take the opportunity to welcome Debra Vogler as senior technical editor of the magazine. Debra brings 12 years of experience as a journalist covering the semiconductor manufacturing industry, and a 20-year career as a reliability engineer. She has interviewed hundreds of industry executives and written about every facet of semiconductor manufacturing processing.

Kim Newman
Publisher

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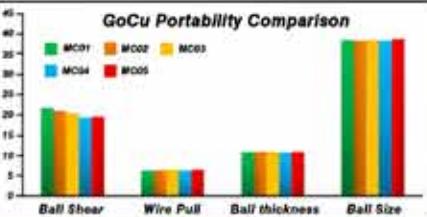
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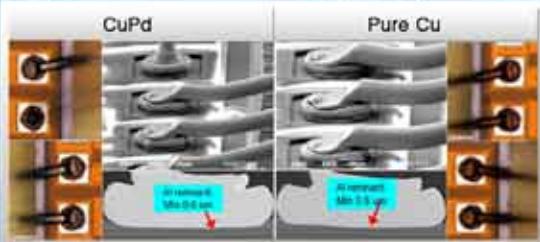


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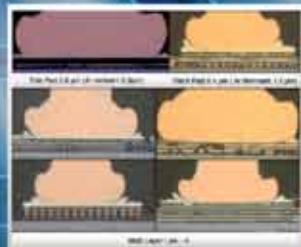
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MEMS Testing: Transition from Millions to Billions to Trillions

Janusz Bryzek [*Fairchild Semiconductor*], Shad Roundy [*University of Utah*]

Sensors, specifically MEMS-based, have created multiple market tornados over the past 40 years. Most recently there has been a market explosion driven by the widespread adoption of MEMS sensing devices in mobile consumer applications. In the past 5 years the worldwide market has grown from roughly 10 million to 3 billion sensors in mobile devices, representing a growth rate of over 200%/year. The total market is expected to grow to at least 16 billion sensors in the next 5 years, and a trillion sensors in 10 years.

So far, this increase in volume has been driven to a large extent by accelerometers, microphones, gyroscopes, magnetic sensors, light sensors, proximity sensors and pressure sensors. Future growth is expected to bring a broad range of new sensors, such as humidity, color, biosensors, lab-on-chip, chemical sensors, and other devices.

The accelerated growth is expected to be driven not only by the mobile market, but also by other global waves, such as the Internet of Things, Central Earth Nervous System, Sensory Swarms, Smart Business, Context Computing and mobile health applications. Multiple sources forecast the accelerated growth of sensors for such Smart Systems to trillions of units by 2022. (Smart Systems are defined as a fusion of computing, communication and sensing. Smart Systems are considered the biggest business opportunity in the history of business, supporting solutions of global issues and problems.²)

Test Challenges

The world of MEMS sensors is far more diverse than the world of ICs. Each type of MEMS device typically must be subjected to physical stimuli during testing. Thus, the test systems

for each class of device are generally fairly unique, as each requires generation of different precise stimuli, such as pressure, acceleration, rotation, magnetic field, chemical density, optical field, fluidic exposure, etc.

In addition to the increased diversity of devices, MEMS presents other test challenges as worldwide volumes move into the many billions and trillions of devices per year. For one, packaging affects the performance of MEMS devices to a much larger degree than traditional ICs. This fact, combined with the fact that a MEMS part must be subjected to physical stimuli, makes it more difficult to move testing to the wafer level. Additionally, temperature compensation is more commonly needed for MEMS, which may require multiple temperature testing at the final package level. Emerging sensors may need to be compensated from other cross-sensitivities, such as vibration or pressure, which complicate test systems.

Other aspects of MEMS that pose test challenges include the fact that sensor package size continues to shrink, creating difficulty in making reliable contact with sensors under physical stimulus and over temperature. The smallest packaged sensors already approach a 1x1 mm footprint. Also, the evolution of sensors is driving improvement in performance, further compounding test difficulty.

While the industry has shipped billions of selected sensors, transitioning to trillions will create a challenge for both existing sensors and, to a higher degree, for emerging sensors. Sensors have become multi-sensory systems in a package. In addition to package-level testing, providing known good die (KGD) in a wafer form becomes a very important yield management component. Sensor testing in a wafer

form is dramatically underdeveloped, thus representing an emerging business opportunity. Validation of correct sensor fabrication in a wafer form requires verifications of non-electrical functions, such as uniformity of wafer bonding. While IR and ultrasound imaging techniques have emerged, more sophisticated wafer probing techniques will need to be developed to enhance KGD validation, such as 3D IR tomography with sub-100nm resolutions.

Existing Test Infrastructure

Prior to this latest market surge, MEMS test solutions were typically custom-developed in-house systems. The last five years have seen tremendous progress in the availability of standardized test solutions because of the large growth in volumes driven by the inclusion of sensors in mobile devices, particularly for inertial, pressure, and magnetic sensors. Several vendors have developed semi-standard systems to support high-volume testing.

Most high-volume sensors are built as multiple dice (MEMS and ASIC) in a package. The simplest configuration includes one MEMS die and one ASIC die; more advanced configurations may include multiple ASIC and multiple sensing dice. Achieving high yield for a final product necessitates using KGD. While the IC industry already offers this, the KGD concept in the sensor industry is emerging.

There has been significant progress in wafer-level testing, where standardized testers that perform MEMS-specific measurements have become available. For example, in addition to testing electrical parameters, several wafer-level test systems enable mechanical tests such as resonance frequency, quality factor (Q level), C-V curves, and quadrature (for

gyros). Unfortunately, wafer probe level stimulus has started to emerge for only a limited set of physical variables and doesn't yet exist for emerging sensors.

Progress in package-level testing is even more impressive, with multiple vendors expanding IC test systems to enable MEMS testing. Typically, such systems include three components: 1) handler, 2) sensor stimulus generator, and 3) the data acquisition and control system. Recently, sensor stimulus generators started to enable the testing of combo sensors. For example, SPEA's systems (**Figure 1**) enable high-throughput testing of sensors including 9 degrees-of-freedom (9DOF): tri-axial acceleration, tri-axial rotation, and tri-axial magnetic. Such a configuration makes the cost of MEMS testing comparable to the cost of IC testing.

Standard solutions are not yet available for most emerging mobile sensors such as humidity, chemical or biomedical. Therefore, test systems for these products must still rely on in-house or custom-developed solutions.

The majority of high-volume sensors now have embedded electronics and digital outputs. Going forward, this trend will only accelerate, so difficulties associated with testing of analog outputs, such as noise and parasitics, are quickly becoming a thing of the past.

The presence of sensor-embedded smart-test electronics enables lowering the test cost and improving the quality of testing. The addition of test-specific circuitry on the ASIC may cost little in terms of ASIC area, but it can have a significant payoff for product performance and production efficiency. For example, many MEMS devices can be electrically excited and measured directly from the embedded circuitry. This capability by itself may not be enough to eliminate the need for package-level calibration and verification, however, when combined with information about the specific MEMS device gathered at wafer probe, this capability offers the opportunity for a significant reduction of test time (cost) and an increased confidence level about sensor quality.

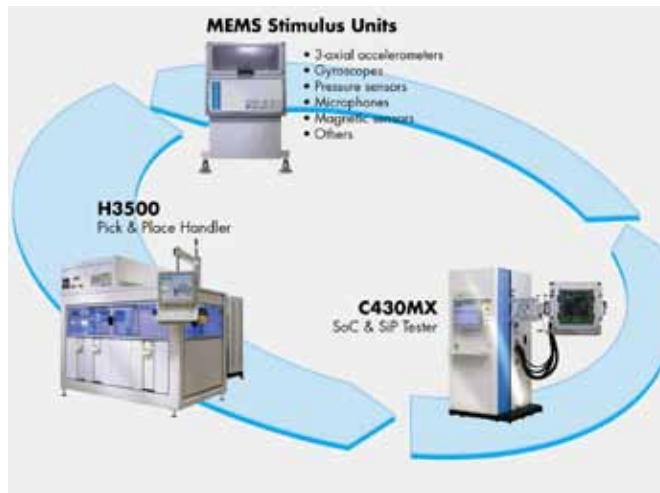


Figure 1: Integrated MEMS test system from SPEA provides a high-speed test environment to test stand alone and combo sensors (multiple degrees of freedom in a single package) including acceleration, rotation, pressure and magnetic. SOURCE: <http://www.spea.com>

As MEMS performance can be highly dependent on package-level stresses, it is sometimes necessary to recalibrate sensors after they have been soldered to the final product PCB. For example, selected cell phone manufacturers test the entire cell phone to recalibrate the embedded acceleration sensor. This practice can be costly (standard test systems are not available) and highlights the sensitivity of MEMS devices to package constraints. Again, more sophisticated test circuitry on the embedded ASIC has the potential to both improve in-field performance by performing on-the-fly calibration adjustments and potentially reduce the need for testing and calibration during the system manufacturing.

Explosive adoption of sensors in mobile devices created a new class of users for sensor test systems: mobile apps developers. As of Q1 2012, only about 0.5% (~5,000) of all iPhone™ and Android™ applications used sensor output. It is expected that within the next few years the penetration will significantly

increase, to perhaps 100,000 apps from maybe 25,000 developers. Factoring proliferation of new sensors in mobile devices, this will create additional testing challenges and opportunities for creative solutions for perhaps 30 types of embedded sensors by 2017, representing a significant market for new test systems for mobile devices.

Sensor Fusion

Sensor fusion combines and processes outputs from multiple sensors through advanced algorithms, such as Kalman filters. The objective is to improve system performance. For example, navigation applications use input from accelerometers, magnetometers, gyroscopes, pressure sensors and GPS to give higher accuracy location and orientation information than would be possible from the information from each of these sensors used individually. An example of Windows 8™ sensor fusion is shown in **Figure 2**. This Windows 8™ sensor fusion includes a tri-axial acceleration sensor (to measure motion, orientation, inclination), a tri-axial gyro sensor (to measure rotation), and a tri-axial magnetic sensor (to provide compass function and orientation).

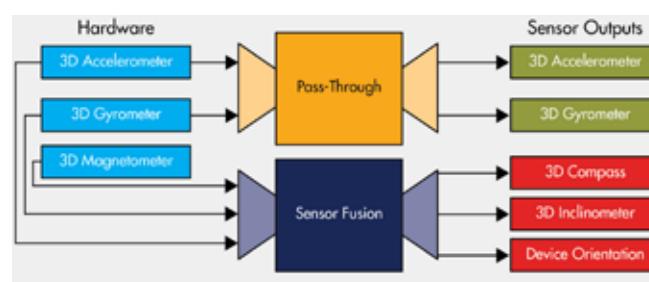


Figure 2: Sensor fusion in Windows 8™ integrates 9 degrees-of-freedom to sense motion components. SOURCE: <http://www.geek.com/articles/chips/microsoft-develops-9-axis-sensor-fusion-system-for-windows-8-tablets-20120125/>

sensing). Fusion of data from three sensors overcomes the shortcomings of each sensor type, significantly improving system performance and eliminating jittery movement. These improvements, in turn, enable tilt-compensation and improve accuracy for measurement of yaw, pitch, and roll. Applications benefitting from such fusion include compass apps, augmented reality interaction, casual game control, and 3D gaming. The first test system enabling validation of this type of performance improvement was just introduced.³

An alternative dumb implementation would require much more accurate sensors (perhaps 100 times more expensive) consuming significantly more power (perhaps 100x more).

The emergence of sensor fusion will require test systems to enable application of different physical stimuli to the same multi-degrees-of-freedom device with embedded sensors (e.g., acceleration, rotation, magnetic, pressure) and measurement of mobile system performance (such as the Windows 8TM example above), further complicating test systems.

Summary

The explosion of sensor applications in the mobile market over the last five years has brought dramatic progress for MEMS test systems. These systems have started to adopt the high-volume IC infrastructure, specifically handlers and data acquisition systems, with custom-designed sensor stimulus units.

Forecasted growth of sensors to trillions of units over the next 10 years will bring many new sensors for which a high-volume test infrastructure doesn't yet exist. This will create major challenges and business opportunities to test the industry. 

Acknowledgments

Android, iPhone, and Windows 8 are trademarks of Google Inc., Apple Inc., and Microsoft Corporation, respectively.

References

1. www.TSensors.org (website launch Oct 2012)

2. <http://harborresearch.com/smartsystems/>
3. <http://www.spirent.com/Solutions-Directory/SimSENSOR>

Biographies

Janusz Bryzek received his PhD from Warsaw U. of Technology and completed the Executive Management Program

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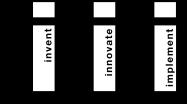
Shad Roundy received his PhD and MS degrees from the U. of California at Berkeley, and his BS degree from Brigham Young U. and is an Assistant Professor at the U. of Utah



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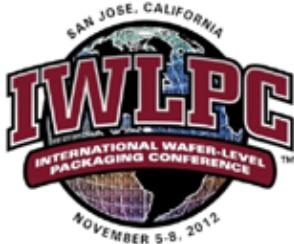
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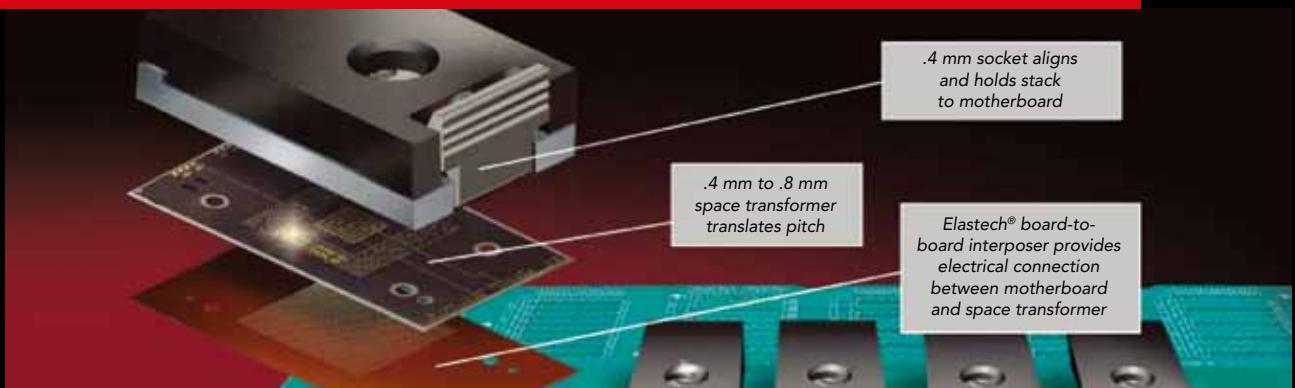


John Ellis

a decade at Sandia National Labs, where he led projects ranging from nuclear weapons testing, to early MEMS accelerometer and gyro development, to cruise missile guidance systems. He currently provides technology and economic consulting to high-tech firms, government agencies, and not-for-profit corporations. John's concern about the use of malicious (Trojan) circuitry against the U.S., particularly via 3-D

and 2.5-D integrated circuits, recently led him to write a highly-rated cyber terrorism techno-thriller, *Dormant Curse*. As a result of the book's success and its plausibility, John was recently asked by the Defense Advanced Research Projects Agency (DARPA) to develop a white paper detailing a concept to quickly find Trojan circuits in semiconductor parts before they enter the global supply chain. John also serves as editor of chipsecurity.org and 450mm.com. At IWLPC, John will present the threat of Cyber-Physical Terrorism in your Smartphone - a very

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Georgia Tech to Launch Industry Consortium in MEMS Packaging

Two research centers at Georgia Tech, the Center for MEMS and Microsystems Technologies (CMMT) and the 3D Systems Packaging Research Center (PRC) have proposed a joint industry consortium on MEMS Packaging to address some of the biggest challenges impacting the success of MEMS in consumer, medical and industrial applications. The research focus will be on development of new platform technologies for low cost, hermeticity and high reliability, resistance to moisture, minimal stress on the MEMS devices and low temperature assembly.

Faculty and inter-disciplinary experts from both centers will work collaboratively with industry to address a series of technical and economic challenges that include, but are not limited to: 1) Low-cost wafer-level MEMS packaging; 2) Stress isolation elements: modeling, design, fabrication and characterization; 3) Stress-free molded MEMS packaging; 4) Low-via-resistance and low-cost interposers for MEMS packaging; 5) Low-temperature hermetic packaging; 6) Packaging of ultra-thin MEMS; 7) Chip scale packaging of MEMS; 8) 3D packaging and interconnections (e.g., die on edge); 9) Packaging of fluidic, chemical and optical MEMS; and 10) System-level thermo-mechanical stress modeling.

The specific industry programs will be developed during the next 12 months in consultation with industry and academic experts. They are expected to fall under two types of industry programs: individual company projects on a single, specific technical challenge, and consortia projects involving multiple companies in one or more strategic themes that include: automotive applications, smart consumer applications,

medical applications, and industrial applications.

Companies interested in this industry consortium are encouraged to contact Prof. Farrokh Ayazi at ayazi@gatech.edu or Prof. Rao Tummala at rao.tummala@prc.gatech.edu.



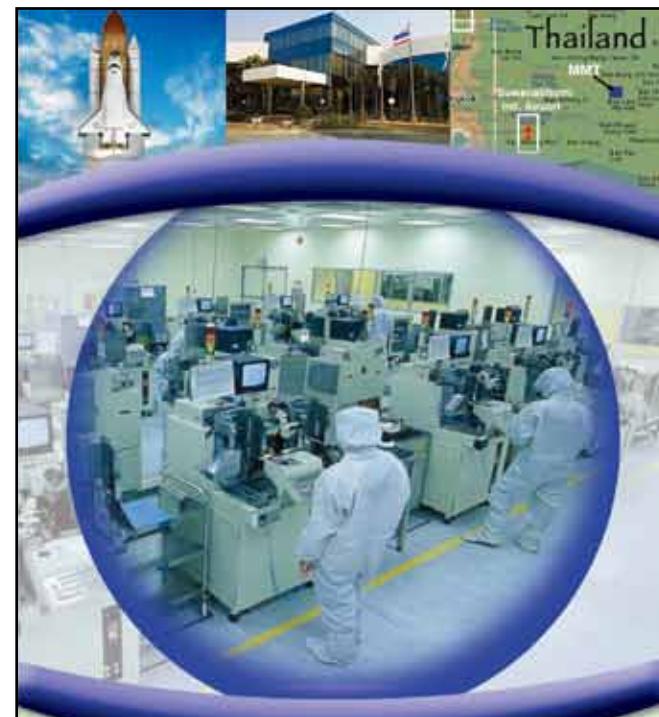
Prof. Farrokh Ayazi



Prof. Rao R. Tummala

F&K Delvotec in Top Spot in VLSI Research's 2012 Customer Satisfaction Survey

VLSI Research announced that 2012 was the first time F&K Delvotec, a wire bonder supplier, captured a top spot in its 2012 Customer Satisfaction Survey. Competing against all focused semiconductor equipment manufacturers in the world, F&K Delvotec beat them in ten categories. The company increased



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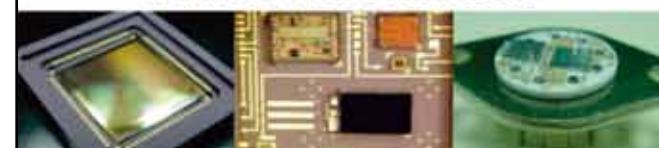
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its rating 7% this year to 8.51 against THE BEST Assembly Equipment Suppliers.

VLSI Research noted that F&K Delvotec is able to improve its rating because it has an engineering group in Singapore dedicated to customizing the automation systems on bonders to specific requirements. The company also

recently expanded its support network with new offices in China, Malaysia, the Philippines, Taiwan, Korea and Japan. These teams are key reasons why customers rated F&K Delvotec best in field engineering support and support after sales, both at 9.0 on a scale of 1 to 10, noted VLSI Research.

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Change of Direction for R&D Circuits

R&D Circuits, a turn-key manufacturer of advanced printed wiring boards for the ATE industry, has announced it will focus its resources on the emerging needs that very high performance devices place on socket and interconnect technology. According to President and CEO, James Russell, the socket and ATE load board markets are rapidly moving toward interconnect technologies that require sub-100ph interconnects for power and signal integrity performance. "After long and careful technical evaluation, we have concluded that this cannot be accomplished with traditional monolithic or spring probe contact designs," said Russell. "By dedicating our resources to technologies that can meet and exceed these challenging requirements, R&D Circuits will be able to deliver a technology that leapfrogs today's products and will meet the market's needs for the next several years."

A final buy notice will be issued for all Grypper®, G40, G80, BGA65, QFN40, QFN35 and LGA50 products in order to focus capacity on newer technologies. The company will introduce its next-generation products in mid-September, 2012. Many will offer direct footprint-compatible replacements with much higher frequency performance.

Micro Control Company Reaches a Milestone

Micro Control Company, a designer and manufacturer of automatic test equipment and burn-in/environmental systems, recently celebrated its 40th year. Founded in 1972 by Harold Hamilton, the company started out as a test equipment manufacturer for memory boards and devices before expanding into testing complex logic chips. The company later added burn-in and environmental test systems and followed up with burn-in-with-test systems for high-power devices.

STATS ChipPAC Advances Through-Silicon Via Capabilities

STATS ChipPAC announced that it has advanced its through-silicon via (TSV) capabilities with the qualification of 300mm mid-processing and low-volume manufacturing. Expanded capabilities in mid-end and back-end TSV manufacturing enable increased 2.5D and 3D packaging integration. The company said that it is firmly engaged with multiple strategic customers on TSV development programs that support the semiconductor industry's shift to 2.5D and 3D packaging integration for the mobile, wireless connectivity, and networking market segments. The company's current 3D TSV development and customer qualification activities include devices at the 28nm silicon node, application processors (AP),

and graphic processors utilizing TSV for the high performance wide input/output (Wide I/O) memory interface required by higher bandwidth applications for the mobile market.

The company's BEOL services include chip-to-chip and chip-to-wafer assembly with stealth dicing and fine-pitch micro-bump bonding down to 40 μ m. Since April 2011, it has been rapidly expanding its TSV offering with 300mm mid-end of line (MEOL) processing capabilities. According to EVP & CTO, Han Byung Joon, the need for higher levels of integration, improved electrical performance, reduced power consumption, faster speed, smaller device sizes, and shorter interconnects is forcing a shift to more complex 2.5D and 3D package designs utilizing TSV technology. He also noted that TSV technology will be a key requirement in the convergence of

mobile communication and computing functionality in devices such as smartphones and tablets. The company expects this trend to drive rapid growth and adoption of TSV technology.

The mid-end TSV process flow occurs between the wafer fabrication and back-end assembly process supporting the advanced manufacturing requirements of 2.5D and 3D packaging including wafer-level, flip-chip and embedded technologies. The company provides MEOL assembly services including micro-bump technology down to 40 μ m, temporary bond/de-bonding, backside via reveal, isolation and metallization.

SSE LLC Gets Nod from *Inc.* Magazine

Inc. magazine recently ranked Solid State Equipment LLC on its sixth annual Inc. 500/5000 - a ranking of the nation's fastest growing private companies.

Inc. editor, Eric Schurenberg noted that, "Now, more than ever, we depend on Inc. 500/5000 companies to spur innovation, provide jobs, and drive the economy forward. Growth companies, not large corporations, are where the action is."

Dow Corning Names Peeters VP Electronics Solutions



Eric Peeters

Dow Corning announced that it has appointed Eric Peeters as Vice President, Electronics Solutions, effective September 1, 2012. According to Robert D. Hansen, President and CEO of Dow Corning, the company continues to grow and invest in its portfolio of silicon-based solutions that enable technologies such as LED lighting, power electronics, and semiconducting



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devices. He added that customers will benefit from Peeter's ability to understand their needs while driving new technology to market.

Peeters takes over for James Helwick, who has led Dow Corning's Electronics Business since 2010. Helwick has been asked to lead the extensive and

quickly growing Electronics innovation portfolio, building on his vast application and technology expertise.

Peeters joined Dow Corning in 1992, and most recently served as Vice President of Solar Solutions & Wind Energy Solutions. In his more than 20-year career at Dow Corning, Peeters has

served in various science and business leadership roles in the United States and Europe. Eric has a master's degree in chemical engineering from the Catholic University of Leuven, Belgium, and a Master in Technology Enterprise degree from the IMD in Lausanne, Switzerland.

Shaffer Joins Panasonic Factory Solutions Company of America



Glenn Shaffer

Panasonic Factory Solutions Company of America announced that Glenn Shaffer joined its team as New Business Development Manager. Shaffer previously served as

National Sales Manager at the Assembléon Division of Philips Electronics where he managed the North American sales team of direct employees and channel partners, led business development, and created numerous internal programs and processes during his eleven year tenure. He has also held roles as Assembléon Regional Sales Manager and Account Executive and Document Management Consultant with Reynolds & Reynolds. He has participated in many industry councils and earned a Bachelor of Science in Business Administration degree from Bowling Green State University in Marketing.

Deca Technologies Selects Meikle as Managing Director in Philippines

Electronic interconnect solutions provider, Deca Technologies, announced a strategic expansion of its executive management team with the appointment of Iain Meikle as Vice President of Operations and Managing Director of the Company's Philippines operations. He joins Deca from Carsem where he served as Vice President of Manufacturing, overseeing operations at factories in Malaysia and China.

Since its launch in November 2011, Deca has been steadily ramping up operations within its Philippines manufacturing base. Originally from

(continued on Page 46)

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Kimberly D. Pollard, Richard Peters, Travis Acra, Don Pfetscher, Josh Cummins, Diane Scheele, [\[Dynaloy LLC\]](#)
Spencer Hochstetler, Peter Shang, San Sutanto, [\[Eastman Chemical Company\]](#)
Thorsten Matthias, Thomas Glinsner, Martin Schmidbauer, [\[EV Group\]](#)

T

he use of negative dry film or negative spin-on film photoresist has been very common in semiconductor packaging processes. Film thicknesses ranging from 10 μm to 120 μm have been incorporated into processes ranging from redistribution to solder bump application. Removal of these films at rates reasonable for manufacturing processes has always been challenging, usually requiring 1) processes that are between 20 and 120min in length, or 2) a plasma gas-based etch process followed by a wet clean to complete. A process flow diagram is shown in **Figure 1**.

As a result of requirements for these process flows, immersion cleaning developed so that multiple wafers, typically 25 to 50 at a time, could be processed simultaneously and increase the tool throughput while still accommodating the long process time. The success with this type of processing allowed thick negative films to be successfully incorporated throughout the packaging process. However, this solution to increase throughput, although providing a more

reasonable cost-of-ownership (CoO), has been accommodated by trade-offs in other areas of the overall process.

As wafer feature dimensions continue to be scaled down, the trade-offs have a greater and greater impact on the process. For example, when batch immersion processes are run, the photoresist strip solution is reused to clean multiple batches, using a standard unchanging recipe defining the process time and temperature, solution recirculation rates, rinse solutions, etc. The best photoresist removal solution (chemistry) to match the static process conditions would be a static strip solution in which the composition would not vary, despite the number of cleaning processes that had been done. Practically, this condition cannot be met with an immersion process. Photoresist removal solutions behave differently throughout their lifetime due to 1) resist being dissolved in them, which can change further resist dissolution rates, possibly requiring extended clean times; 2) evaporation at the operation temperature, which changes component concentration

and can affect cleaning efficiency or compatibility characteristics; 3) consumed reactive components that can create concentration changes leading to less effective stripping performance or changing compatibility with permanent materials on the wafer surface; 4) undissolved resist build up that provides a continuously growing source of particles; and 5) surface finish of the wafer after the strip process, which, if altered, may require additional processing to be integrated into the packaging process. Additionally, the traditionally long process times for batch immersion clean processes create additional challenges when rework is necessary.

Long processes provide extended contact of strong chemical solution with the wafer surface. Even solutions that have an etch rate for a permanent material, for example Cu, that is in the range of 5 $\text{\AA}/\text{min}$, will lose ~450 \AA in a 90-minute process. If that wafer was processed in a strip solution that has a non-linear Cu etch rate as a function of process time and/or solution lifetime, then more Cu could be lost. If rework is required, then an additional process will be necessary. In the above example, ~1000 \AA of Cu could be lost, possibly exceeding the maximum allowable loss specification. In addition, even if the Cu loss is within process guidelines, it may be removed from the surface unevenly, thereby creating integration issues as the wafer moves to subsequent processes.

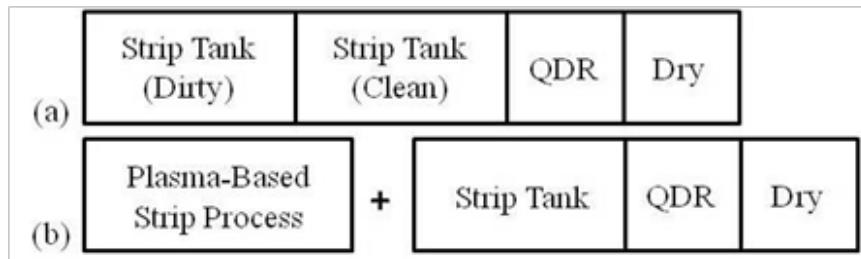


Figure 1: Process flow diagram. **a)** batch immersion strip process, **b)** plasma plus batch post-etch residue removal process

Reducing Variability

All the issues discussed above describe opportunities for reducing variability in production cleans processes, which is a source of yield loss. The goal of this paper is to discuss a new technology that can improve on the trade-offs while maintaining a competitive CoO. Combining the capability to develop wet chemical resist removal solutions with an understanding of process and tool requirements has led to the development of a single-wafer cleaning technology for photoresist removal. This technology targets the existing and developing needs in wafer-level packaging: removing thick cross-linked films such as photoresists and fluxes, while maintaining the pre-clean integrity of the solder bump, exposed metals, and dielectrics. The platform, called CoatsClean™, enables the manipulation of chemistry to a degree that allows for significantly reduced chemical usage and short process times in a single bowl tool. In addition to environmental sustainability, the reduced chemical usage allows the use of fresh, unused solution on every wafer leading to improved wafer-to-wafer consistency and a CoO that can be lower than other immersion or single-wafer tool processes. This technology platform provides flexibility in cleaning processes including the ability to balance resist removal with materials compatibility, increased stability of chemical formulations, increased formulation possibilities, and the ability to run multiple wafer types and chemistries on the same tool.

Figure 2 shows images of a variety of electroplated solder bumped 200mm and 300mm wafers cleaned using the new technology, consisting of the EVG301RS tool, resist strip solution, and process. The optical images illustrate cleaning results after the removal of thick resist and again after the subsequent field metal etch process, indicating that the surface is finished in a manner that can be integrated into the next process step. Additionally, the scanning electron microscope (SEM)

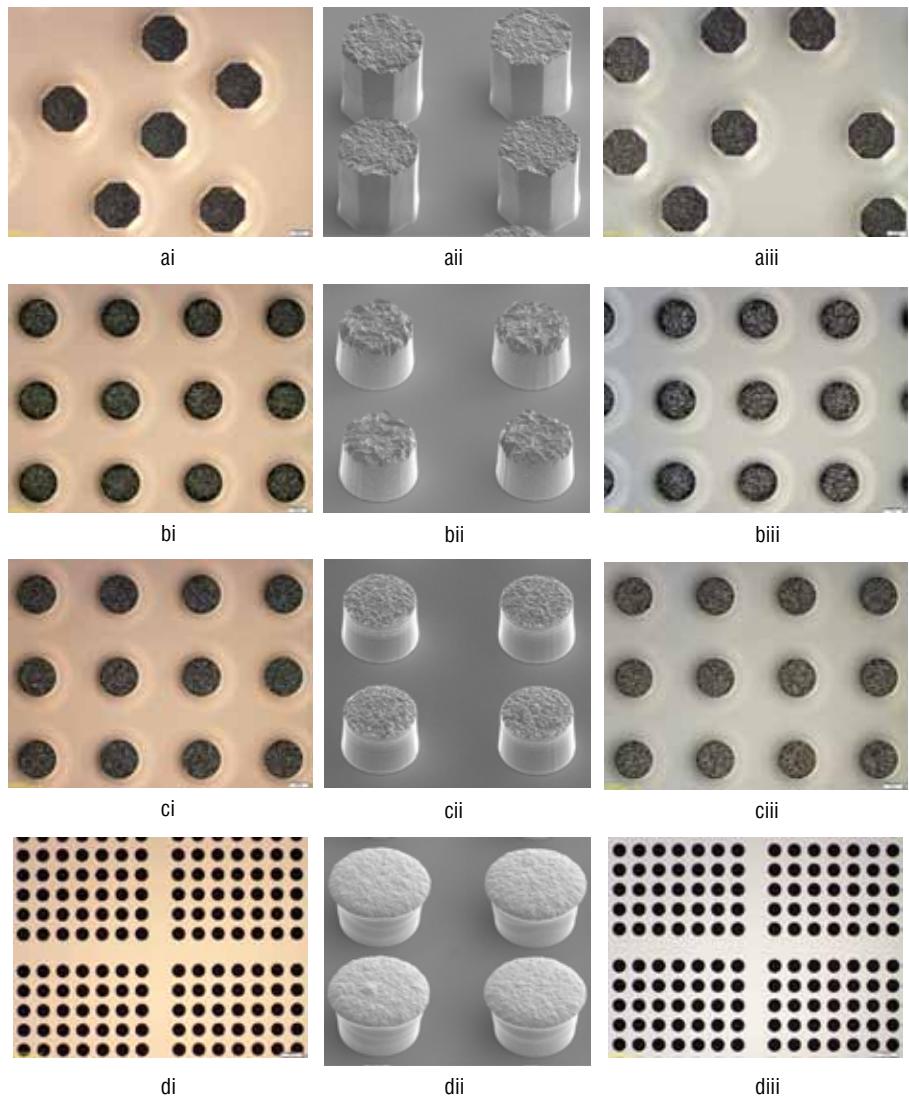


Figure 2: Images i) optical, after resist strip, ii) SEM, after resist strip, iii) optical after field metal etch. a) Resist removed 120µm TOK 50120, solder, SnAg; b) Resist removed 80µm Asahi Sunfort CX8040, solder SnAg; c) Resist removed 80µm Asahi CX8040, solder Cu pillar, LF cap; d) Resist removed, 55µm AZ4620, solder eutectic

images show a more detailed view of compatibility with the solder bump and Cu field metal surface after the photoresist removal step.

CoO Considerations

As discussed previously, CoO was

a large driver in the development of batch immersion processes for thick resist removal. This is particularly true for negative tone resists because additional cross-linking occurs during exposure, making the polymer more challenging to remove, especially when

Step 1	Step 2	Step 3
Low volume of room temp. CoatsClean solution dispensed onto wafer surface	Solution rapidly heated to activation temperature. Resist is stripped	Rinsed with water and dried in a single bowl

Figure 3: a) Process flow in a CoatsClean™ tool

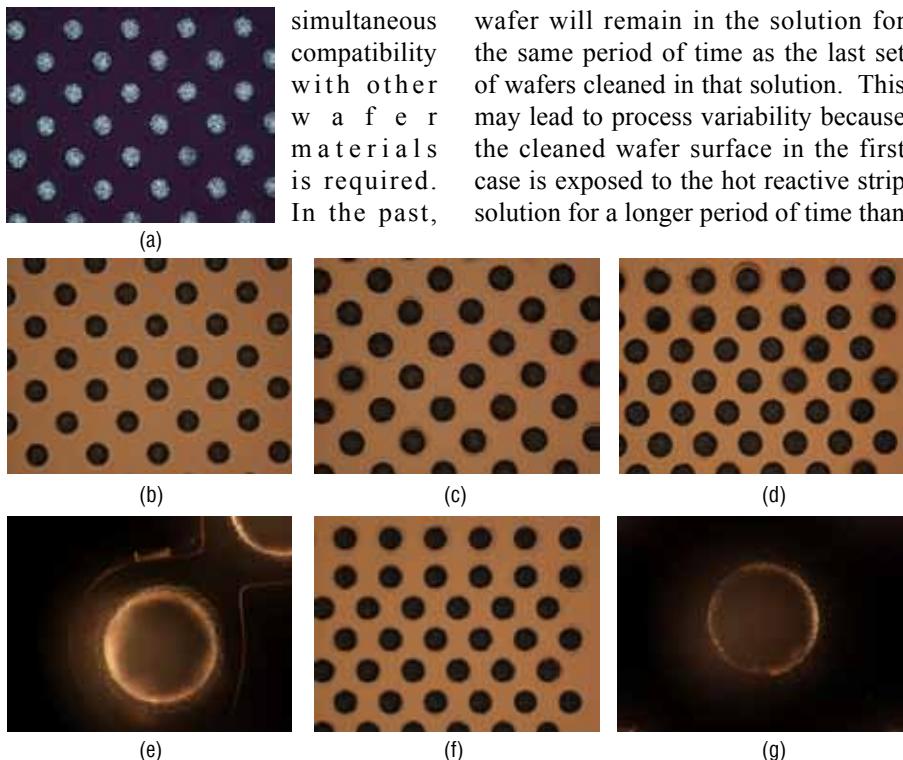


Figure 4: Optical images of a batch of dummy wafers, cleaned with different process conditions. **a)** unprocessed wafer; **b)** wafer processed in fresh typical resist strip solution, 60°C, 30min, front of cassette; completely clean **c)** wafer processed in fresh typical resist strip solution, 60°C, 30min, middle of cassette; showing residue **d)** wafer processed at end-of-resist-loading in a typical resist strip solution, 60°C, 30min, showing residue remaining where there was none for the same test in a fresh solution; **e)** dark field of bump area for image shown in d); **f)** wafer processed at end-of-resist-loading in a typical resist strip solution, 60°C, 60min, showing time required to complete cleaning of the surface; **g)** dark field image of bump area for image shown in f)

single-wafer process tools and processes were considered an uneconomical choice because of the long process time (20–120min) and large volume of resist stripping solution (often > 1L) to process a single wafer. **Figure 3** shows a process flow for wafers cleaned using the new technology. 300mm wafers are processed using substantially reduced volumes of solution per wafer to remove resist in a single bowl, single-wafer clean process and using 3–10min (dry-dry) process times including processes to remove thick negative resists.

Optical images depicting the change in cleaning time as a function of wafer position and resist loading in the solution for a batch immersion process are shown in **Figure 4**. A process recipe is developed in which a process time is selected to be the same throughout the bath lifetime. Even if the fresh solution removes the resist more quickly, the

wafer will remain in the solution for the same period of time as the last set of wafers cleaned in that solution. This may lead to process variability because the cleaned wafer surface in the first case is exposed to the hot reactive strip solution for a longer period of time than

The thermal gravimetric analysis (TGA) is shown in **Figure 5**. From the plot, the evaporation rate of DMSO was calculated as 2%/min. This rate is considered an upper limit of the rate of evaporation because of the high surface to volume ratio. Additionally, in a photoresist removal solution, other components modify the evaporation rate, decreasing it from that reported in the figure. With surface area to volume ratios and air flow across the surface, etc., being equal, a 100% DMSO resist strip solution would be evaporated completely through a 12hr operation period. In practical terms, the evaporation rate is not that high but still significant. It is common practice to replenish resist removal solutions during the lifetime of the solution so batch levels do not get too low. Between evaporation of solvent and replenishment of solution through the course of the bath lifetime, there are changes in the resist strip formulation component ratios, changing the balance between the critical components. This change in balance may result in changing the solubility of resist, or it may change the effect of the solution on the exposed wafer surface.

The increase of particles in solution as multiple batches of wafers are processed is shown in the graph in **Figure 6**. When fresh solution is used for each cleaning step, the dissolving capability of the resist strip solution is

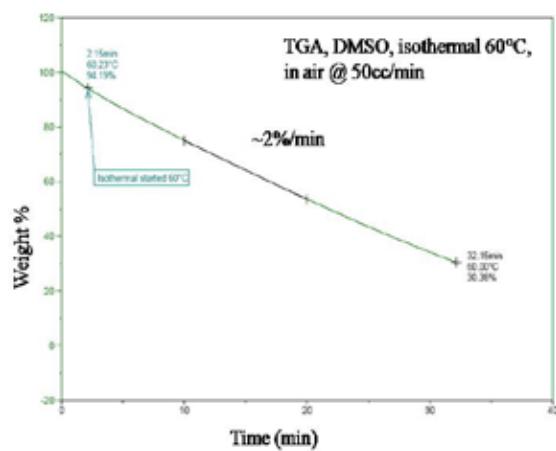


Figure 5: Thermal gravimetric analysis of DMSO. The evaporation rate can be calculated based on this experiment and illustrates that evaporation of even high boiling point solvents, such as DMSO, can affect the resist strip solution composition.

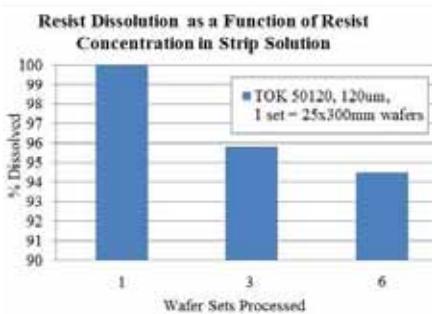


Figure 6: Resist dissolution, measured using particle analysis before and after resist strip of one set of wafers showing decreased dissolution and therefore increased numbers of particles in solution.

at a maximum, allowing for greatest dissolution. Maximum dissolution decreases the possibility of particles in solution redepositing onto the wafer surface and causing yield issues or requiring rework processes.

The continued increase in importance of wafer surface finish after cleans was predicted years ago and was described as being one of the next key challenges for the industry to address.¹

The challenge was tied to continued device shrinkage, and because scaling has continued, the prediction has been realized. An example of the increasing importance of the wafer surface finish has been found in lead-free solder bumping processes. It has been shown² that electroplated lead-free solder bumped wafers that have been stripped of photoresist show an increased probability of yield issues in the subsequent field metal etch process, even when they pass inspection. As a result, many line engineers have developed strategies to overcome the problems by changing the post-strip surface finish. The short process times of the tool discussed above offer an opportunity to have a surface finish that can be integrated with the field metal etch process step.

Summary

The advantages of a single-wafer tool that utilizes relatively small volumes of stripping solutions for thick resist

removal were discussed in combination with the justification from a CoO perspective. The multidisciplinary approach effectively couples the chemistry for resist removal, the wafer clean process and the tool platform simultaneously, to deliver a flexible single bowl clean process. Cleaning and etch results from bumped 200mm and 300mm wafers with up to 120μm-thick negative dry film using a new single-wafer clean tool and process were demonstrated. ☺

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2. K. Pollard, A. Rector, N. Wheeler, Chip Scale Review, Jan-Feb 2011, V15(1), pp. 22-26.

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Power Overlay Packaging Platform for High Performance Electronics

Arun Gowda, Shakti Chauhan, Paul McConnelee, Chris Kapusta, Yongjae Lee, [GE Global Research]

There has been significant advancement in integrated chip (IC) packaging over the last couple of decades and continues with 3D and embedded packaging. In contrast, areas such as power electronics and heterogeneous system-in-packages (SiPs) have seen notable advancement in their packaging technology only recently. These advancements are driven by the industry segments and semiconductor device trends. For example, recent advancements in the power electronics industry are driven by emerging, high-growth segments like vehicle electrification, energy efficient products, etc. These applications demand high efficiency miniaturized systems that are capable of operating across expanding temperature ranges. The emergence of SiC and GaN power devices and the improvement in existing silicon power devices address some of these application needs; suitable packaging, however, is essential to realize the full entitlement of these devices. Power overlay (POL) packaging is an example of a disruptive packaging platform that provides high-density, high-efficiency, and reliable device-level interconnects to yield improved module-level electrical, thermal and mechanical functionality. POL has been demonstrated in several areas and levels of implementation, for power devices and modules, radio frequency (RF) modules, application specific ICs (ASICs) and microprocessors, sensing devices, and embedded electronics. The attributes of POL packaging technology and key performance advantages with respect to power electronics, embedded

electronics, and RF electronics applications are discussed in more detail in this article.

POL Structure and Process Flow

The main feature of POL technology is a planar, copper interconnection structure, using vias through a polyimide-adhesive layer to make direct connection to the device contact pads. This interconnect structure replaces conventional wire bonds and flip chip interconnects. The technology offers significantly reduced parasitic inductance and resistance, while providing a thin profile, higher density packaging and the ability to interconnect active and passive devices of significantly different feature sizes with a single interconnect platform. Multiple interconnect layers can be built-up as needed with the option to co-fabricate passive elements such as inductors, resistors, and capacitors within the process flow. The technology also allows for embedding die completely in an ultra-thin structure with dual-side I/Os. The platform leverages standard equipment and processes used in semiconductor fabrication, PCB fabrication, and surface mount assembly.

Figure 1a shows the cross-section of a typical POL Cu via, through a dielectric layer composed of a polyimide and adhesive, made directly

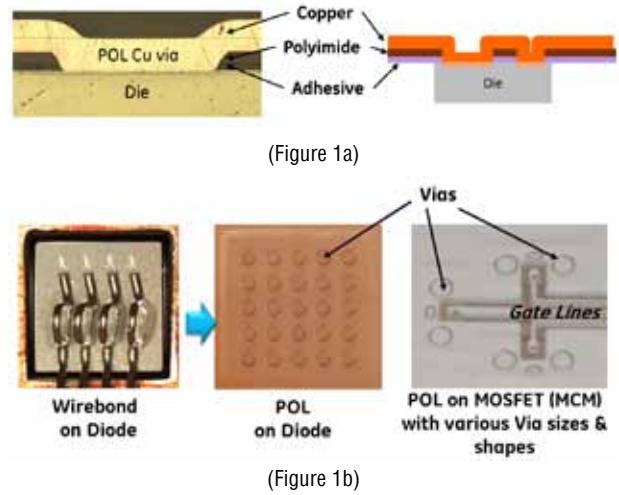


Figure 1: a) Basic one polyimide layer representation of POL interconnect; b) Wire bond and POL examples (top view)

to the die bond pads where a highly reliable metallurgical joint can be obtained with standard die metallization (Al, Cu, etc.). As illustrated in **Figure 1b**, POL Cu interconnects replace conventional wire bonds with an array of vias to the die and metal lines on the polyimide that are spatially arranged to conform to the device-type and contact pad geometry and are designed with electrical, thermal, and mechanical functionality in mind.

Figure 2 illustrates a generic version of a one-polyimide-layer POL process flow. The dielectric film (typically polyimide) is stretched over a metal frame and is the foundation on which the modules are constructed. These frames can be of many sizes (**Figure 3** shows an 18-inch x 18 inch frame suitable for high-volume processes) and are designed to provide dimensional stability throughout the fabrication process. After the application of an



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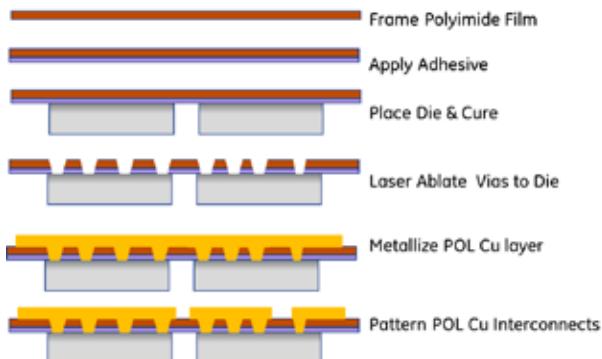


Figure 2: Schematic illustration of a POL intelligent power module (IPM)



Figure 3: Double-sided cooled 1200V/200A POL power module

adhesive layer, the devices are placed on the adhesive layer and cured. Vias are then formed through the polyimide-adhesive layers using a laser-drilling/ablation process to expose the device bond pads. Finally, the POL Cu interconnect layer is metallized and patterned to form the interconnects. A metal layer can also be applied on the die side of the polyimide layer to provide a second layer of routing or added functionality. For multiple layers, the process of lamination of a polyimide layer with an adhesive, drilling, and metallization are repeated. Depending on the diameter of the vias, they can be formed before or after the attachment of the die. For large via sizes ($125\mu\text{m}$ and higher) as used for typical power devices, via openings can be formed using a laser before attachment of the

die and for smaller vias ($125\mu\text{m}$ and smaller, typically for ICs), via openings are formed after the attachment of the die through a via ablation process. Depending on the electrical/RF performance, routing density, device pad sizes, and reliability requirements, the dielectric materials and thickness ($13\mu\text{m}$ to $125\mu\text{m}$), copper thickness ($4\mu\text{m}$ to $150\mu\text{m}$), via sizes ($25\mu\text{m}$ to 2.5mm), line width and spacing (down to $25\mu\text{m}$, depending on Cu thickness), and layer count required are used.

These process steps are foundational to the POL packaging platform and constitute the “1st-level” interconnection scheme. Depending on the die/module type and application, the rest of the process can include the attachment to a substrate and encapsulation. In the case of an embedded system, the layers on the front side are replicated on the back side to form a balanced double-sided structure.

POL for Power Electronics

Aluminum wire bonds have been the “standard” interconnects for power devices for several decades. However, they typically limit system performance through high conduction and switching losses and offer limited system integration potential because of their non-planar form factor.¹ Copper wire bonds and ribbon interconnects overcome some of these limitations and are becoming commercially more available. Recently, several “wirebond-less” interconnect schemes have been proposed. One example that has been commercially introduced is where the wire bonds are replaced by solder interconnects on both sides of the power device¹⁻⁵. While the complete elimination of wire bonds through “wirebond-less” interconnects has shown improved electrical and thermal performance, several additional

challenges related to “wirebond-less” interconnects have become apparent including the need for non-standard die metallization and high processing temperature/pressure (for sintered silver interconnects⁶, high die-level stresses,^{2,3} and limited potential for miniaturization and integration of control electronics. POL packaging, as an alternative WBL interconnect scheme, overcomes these limitations and provides higher densities, higher electrical performance, and higher levels of integration.

In typical power modules, large diameter (5-20mils) aluminum wire bonds are used to connect to one surface of the devices (e.g., source and gate in the case of MOSFETs) while the opposite surface (drain in the case of MOSFETs) is soldered to a direct bond copper substrate or lead frame. In the case of intelligent power modules (IPMs), the gate driver and control circuitry are included in the module. This additional functionality requires additional packaging such as gold wire bonds, adhesive die attach, and in some cases, a printed circuit board. POL replaces the aluminum wire bonds, and in the case of intelligent power modules, integrates both power and control circuitry using a single interconnect platform. The use of copper as the interconnect material with optimized via geometry for high die contact area (as in **Figure 1b**) and reduced and controlled interconnect lengths provides for significantly reduced parasitic package resistance. The low profile interconnects and the ability to tailor current paths for magnetic flux cancelation further allows for lower parasitic inductances. These features of POL technology reduce conduction and switching losses and consequently result in higher efficiency power devices and modules. Lower parasitics also help reduce voltage overshoots, oscillations, the need for snubbers, and improve current sharing.⁷ In cases where several power devices are connected in parallel to obtain higher current modules, unmatched parasitic components can adversely affect current sharing and switching

performance of the individual devices. As a result, substantial temperature gradients can exist in such systems that limit overall reliability and lead to premature failure. POL interconnects can help mitigate such failures by allowing tailored parasitics for each device in the electrical design through photo-lithographically defined, and thus precisely controlled, trace lengths and shapes. In a one-to-one comparison study with wire bond interconnects, POL interconnects showed 70% lower electrical resistance, 60% lower inductance, as high as 2X power density, and >10X surge current capability. A comparison of power modules with POL and wire bond interconnects showed as much as 40% lower voltage overshoots and 22% lower switching losses.⁷

Figure 4 illustrates a POL implementation of an IPM where power devices, gate driver ICs, passives, and thermistors are all integrated within one miniature package using a common POL platform. Relative to a conventional wire-bonded IPM in the 600V range, POL IPM can provide up to 4X package volume reduction through smaller area (>2X reduction) and up to 2X lower body thickness. The POL IPM module also enables new system integration topologies, as in surface mount compatible IPM BGA I/Os illustrated in **Figure 4**.

Another key advantage of having a planar interconnect system is improved thermal performance. The planar copper via interconnects provide the ability for double-side cooling and also can help spread and control heat dissipation paths. The robust copper vias and planar copper circuit provides a very low thermal resistance path to the device for efficient near-junction heat transfer. Inherently, the lower resistance of the POL interconnects reduce joule heating. **Figure 5** shows a single-side and double-side cooled POL module (200A/1200V) using integrated heat sinks. Improvement in thermal resistance up to 40% can be achieved, depending on the efficiency of bottom side (DBC side) vs. top side (POL

side) cooling and the thermal interface between the POL and the top side cooler.⁸

POL technology is also of particular interest for the packaging of SiC devices, where low and matched parasitics are critical to enable very high switching frequencies. Initially, SiC device sizes and current ratings are expected to be limited compared to their silicon counterparts, due to lower

yields. POL provides the ability to build high current modules using many small die, without compromising significantly on current sharing and switching losses.⁹

POL for Embedded Electronics

Embedded electronics offer significant improvements in miniaturization and electrical performance. The platform being discussed in this article can be

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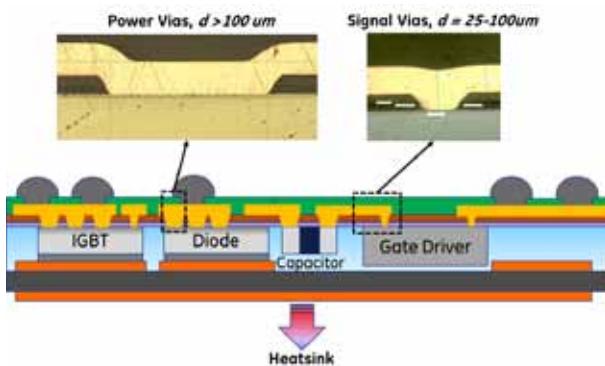


Figure 4: Schematic illustration of one-polyimide layer POL process flow



Figure 5: 18-inch square example of a POL frame

extended to completely embed or bury a single die or a multi-chip module to form a SiP with dual side I/Os. The interconnects to the die and between layers are made directly through the use of copper vias. The dielectric layers are built symmetrically on either side of the embedded devices to obtain a balanced structure. **Figure 6** shows an example of an embedded package fabricated with five metal layers, embedding a 674 I/O, 50 μ m die, for a total thickness of 200 μ m. The figures show both sides of the substrate with the embedded die and an example where a BGA package has been attached to this substrate.

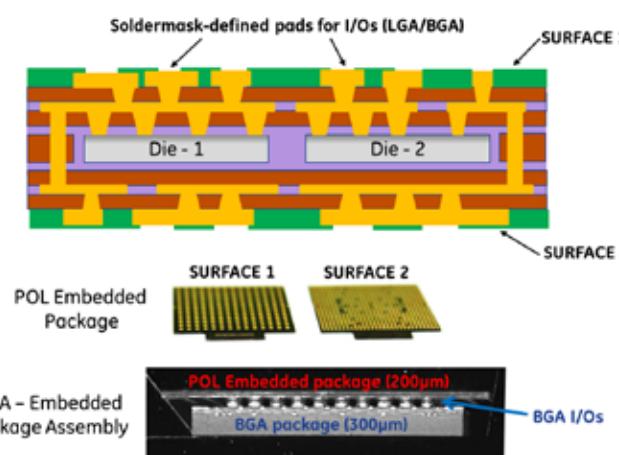


Figure 6: Embedded die package with POL interconnects

All interconnections to the die are made by laser drilling directly to the aluminum pads on the die, without a redistribution layer. The platform is capable of incorporating discrete passives or directly co-fabricating the passives using the embedded technology process.

module.¹⁰ The die is mounted to a shim using an epoxy. The area around the die is filled with a low loss plastic filler to passivate and seal the device. A shielding metallic layer is provided as needed. The figure also shows the packaged driver for a Mach-Zehnder device. It consists of input launch, a 50 ohm transmission line followed by the encapsulated monolithic microwave integrated circuits (MMIC). The RF output is also connected to a 50 ohm transmission line and output launch pad. The power supply is fed into the MMIC via a broadband conical inductor. The MMIC operates from 1 to 50GHz and the packaged module provided similar performance relative to an unpackaged bare die without losing its bandwidth. Specifically, the 8dB of gain was flat out to 50GHz with a properly selected gate bias (-0.65V). Also, the input and output impedance over the 50GHz bandwidth is in good match (better than 15dB).¹⁰ This indicates the capability of POL technology to enable good RF packaging on the drive performance with low RF parasitics.

POL Reliability

POL packaging provides long-term reliability at the component level and at the system level. The choice of dielectric material, particularly its in-plane (XY) and through-plane (Z-axis) coefficients of thermal expansion (CTEs) and respective moduli, and via aspect ratios (via diameter to dielectric-adhesive thickness ratio) can be tailored based on the required electrical/RF performance, thermo-mechanical reliability and operational temperature range. POL Cu interconnects with polyimide dielectric and via diameters ranging from 50 μ m-1.5mm and metal thickness from 35 μ m-125 μ m have demonstrated reliability in thermal cycling (>1000 cycles at -55°C to 150°C), high temperature storage (>1000Hrs at 175°C), power cycling (10⁶ cycles with $\Delta T = 50^\circ\text{C}$), vibration and mechanical shock, and unbiased highly accelerated stress testing (HAST) (96 Hours, 131°C, 2atm, 85% RH). The via structure temperature limits

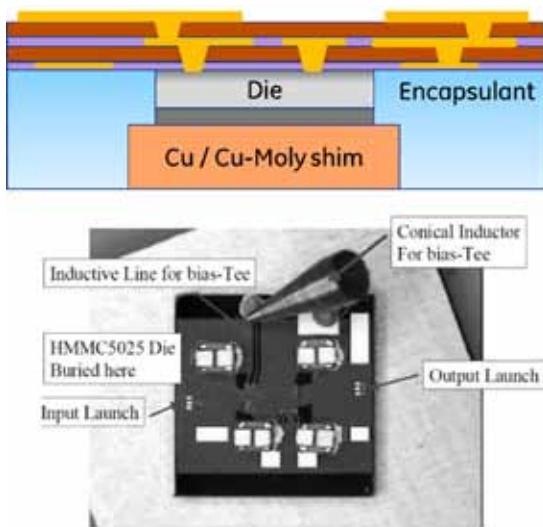


Figure 7: RF module with multi-layer POL interconnect structure

are further extendable with higher temperature polyimides and adhesive systems. This capability is particularly important to enable next-generation wide-band gap semiconductor power devices (SiC/GaN) for high temperature power conversion applications. In addition to the thermo-mechanical structural integrity of the POL structures, the low electrical parasitics put lower stresses on the devices. For example, in the case of power electronic modules, the lower voltage overshoot, better current sharing, lower joule heating of the interconnects, etc., in turn improve the reliability of the power modules.

Summary

The POL packaging platform enables highly efficient and miniaturized electrical systems through the use of direct copper via interconnects to the device bond pads. The platform has been demonstrated and can be applied across various device technologies and applications. In this article, the power electronics, embedded electronics, and RF application spaces were addressed. However, as a platform interconnect scheme, it can be applied across other applications such as automotive electronics, lighting, sensing, imaging, etc.

While POL is one example of a disruptive platform, more such

Multi-layer POL Interconnect Structure

platforms are needed to keep pace with the advancement in device technologies (power, ICs, photonics, MEMS, etc.) and the increasing heterogeneous nature of multi-chip modules and SiPs.⁸

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Singulation of QFN/MLP Packages

Gideon Levinson [ADT - Advanced Dicing Technologies]

QFN/MLP substrates behave much differently from most known materials in the microelectronics industry, and therefore present challenges for the dicing process. This paper will cover basic substrate characteristics and various singulation topics including: substrate geometry and material characteristics, substrate design and parameters affecting the cut quality, quality specifications to which the industry aspires, dicing on tape and tape-less mounting, optimizing the dicing process, and the constant demand for increasing units/hr (UPH) while maintaining cut quality. These factors create real challenges, not only in the dicing process, but also with the blade design, which will also be addressed.

Substrate Geometry/Material Characteristics

QFN (quad flat no lead) and MLP (micro lead frame package) substrates consist of two major materials: 1) copper lead frame coated with PPF (Ni/Pd), or with tin (Sn) plating; and 2) polymer molding. These composite materials have different hardness and brittleness characteristics that in a high-volume production mode are challenging. The final die sizes vary from 1x1mm up to 12x12mm. A die size smaller than 3x3mm creates mounting challenges, which will be discussed later. **Figure 1** illustrates the geometry of a common QFN/MLP-type substrate.

The lead frame in most cases is a copper alloy C-194 or Eftec 64T with a hardness of ~135-145 HV (½ hard). The copper material is relatively soft

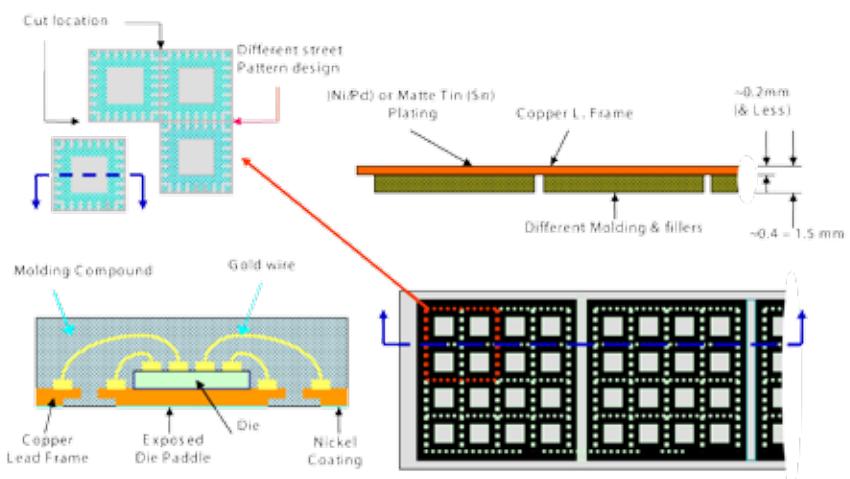


Figure 1: Common QFN/MLP-type substrate

and mainly ductile, which during dicing, causes burrs and smearing. The polymer molding compound is reinforced by silica particles (Si_2O_3) in the range of 30-70 μm in size. The molding compound is relatively brittle compared to the copper lead frame, and chipping on the molding part is another problem during dicing. In general, the combination of a ductile material with a brittle material in the same dicing process creates major challenges. The generic plastic deformation graph in **Figure 2** shows the difference between a brittle material and a ductile soft material (copper in this case).

The silica particles in the polymer-molding compound are used as a stabilizer to minimize stresses and to control the flatness of the substrate. The size of the silica particles affects the chipping size; the larger the silica particles, the larger the chipping on the molding. The silica grit pull-out generates small craters that will create edge chipping after the dicing

operation.

Substrate Geometry Design Affects Cut Quality

Both the geometry of the copper lead frame and the outside geometry of the substrate have a major impact on blade loading, which affects cut quality. In general, minimizing the amount of copper the dicing blade faces while dicing through the leads and at the outer rim of the substrate is a key factor to be considered for substrate

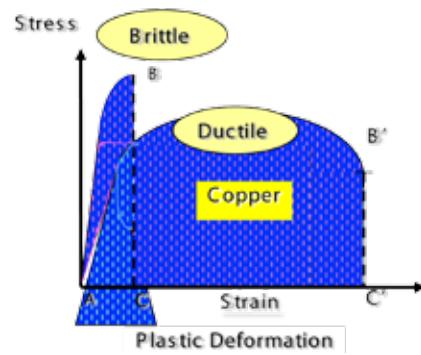


Figure 2: Plastic deformation

design. Minimizing the copper would reduce the load on the dicing blade and subsequently enable a higher feed rate (increased throughputs) and better cut quality (higher yield). The copper amount and geometry is decided by the conductivity and power through the leads, so the design places more consideration on the functional requirements. The production-related difficulties, however, should also be considered. **Figure 3** shows the major elements involved in a QFN-type substrate. The lead cross section at the dicing area needs to be as small as possible. A small square lead cross section is a better design than any other irregular shape. A large lead cross section can cause copper smearing between the leads, and this may cause electrical shorts.

Minimizing unsupported copper around the QFN/MLP substrate is fairly crucial as it can easily break the blades and consequently affect the productivity. The best solution is to

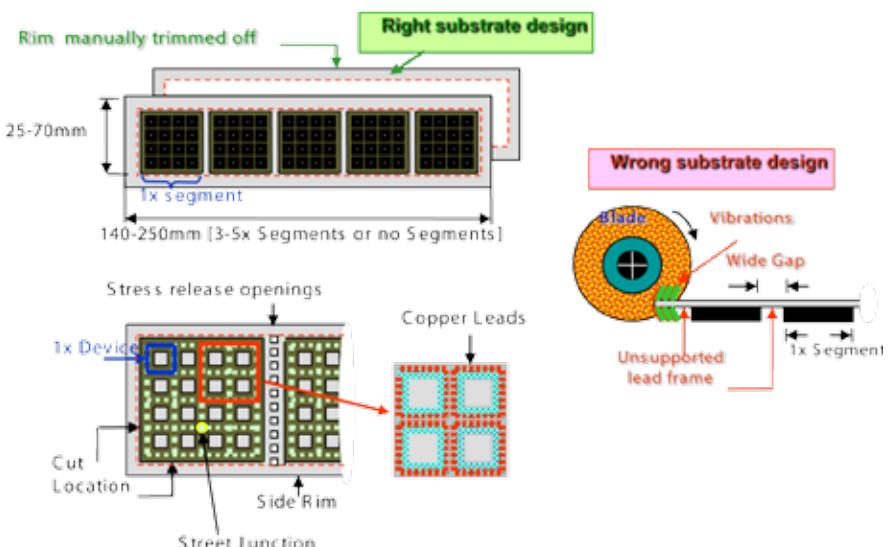


Figure 3: QFN/MLP glossary

design the outer lead frame rim in a "snap off" form that can be manually removed before dicing. If a segment design is applied (**Figure 3**), the area between the segments should be minimized and it should include large stress release openings. It is also

desirable that the molding be as close as possible to the lead frame edge. Half-etched lead frame design has become common in the industry. Such a design is more favorable to dicing and contributes to an improvement in the cut quality, as well as blade life. The

idea is to reduce the amount of copper that the blade needs to remove from the substrate. In general, the larger the etched area, the smaller the load exerted on the blade during the dicing process. Half-etched substrates can be diced with harder blades resulting in longer blade life while maintaining good cut quality.

Effect of Lead Coating/Plating on Cut Quality

The microelectronic industry is driven towards implementing environment friendly "green" products and processes. Conventional QFN leads are lead/tin (Pb/Sn) or nickel/palladium (Ni/Pd) plated. To reduce costs and comply with environmental standards, these materials are now being gradually replaced by matte tin (Sn) plating. Visually, substrates with matte tin plating appear dull compared to the shiny finish of the conventional plated substrates. These types of substrates are also subject to potential damage during conventional dicing due to the possibility of leads melting as the matte tin melting temperature is lower at 232°C compared to the materials used in conventional substrates (Figure 4). To overcome this problem, the blade and the process should be optimized for minimum load. This minimization could be realized by a softer blade, using lower spindle speeds within the range of 15k-20krpm (for 2" O.D. blades), and in some cases, chilling the water to about 12°C. The above parameters should be optimized according to the application.

Quality Criteria and Specifications

Most end users have rather similar quality criteria. The quality specification is a function of the QFN substrate design and the end product requirements. Many parameters affect the quality of the singulation process. The main parameters are: 1) substrate geometry (total thickness, copper thickness, device size, i.e., smaller devices may shift during dicing due to relieved mounting force); 2) outside substrate rim design, unsupported or

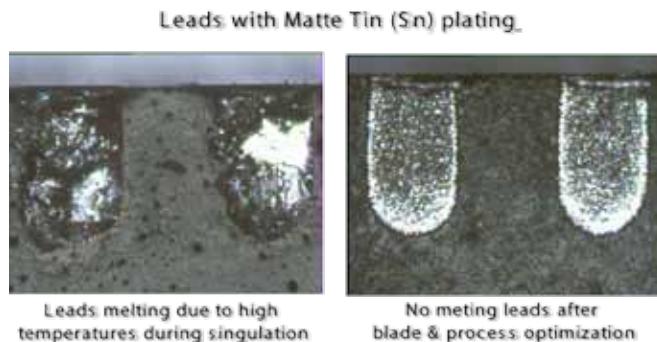


Figure 4: Lead melting

trim design (Figure 3); 3) number of leads; 4) lead coating type; 5) lead cross section geometry; 6) type of mounting; 7) UPH requirements/feed rates, and 8) blade type.

Figure 5 illustrates the different quality criteria. Typical quality specifications are: 1) Y burrs: 0.050mm, 2) Z burrs: 0.050mm, 3) X burrs: 0.050mm, 4) lead smearing: max 25% of the lead pitch (may vary among users); 5) no delamination of leads; and 6) no melting of lead coating. Additionally, many users require 0.020–0.030mm on the X, Y and Z burr dimensions.

The above quality specification is mainly used for QFN products ranging from 0.9mm to 1.2mm in thickness. Thin QFN (typically 0.4mm–0.6mm thick) requires tighter quality specifications. Other QFN products, such as "POWER QFN" are

much thicker – up to 4.0mm. Thick QFN substrates made with much thicker copper lead frames of >0.500mm introduce singulation difficulties; they require different quality requirements per application. However, the POWER QFN niche

is smaller compared to the standard QFN market.

Dicing on Tape and Tape-less Mounting

There are two different mounting methods used in QFN singulation: tape mounting and tape-less mounting. In general, QFN/MLP substrates are not as flat as other microelectronic substrates. In many cases, this nonuniform flatness complicates the singulation process. In today's singulation lines, end users typically want relatively high feed rates of up to 100mm/sec, which adds to the difficulties associated with consistent mounting.

Tape Mounting

Most end users need UV tapes of various thicknesses and adhesion force. Typical thickness may vary from 0.100mm to 0.200mm depending on the

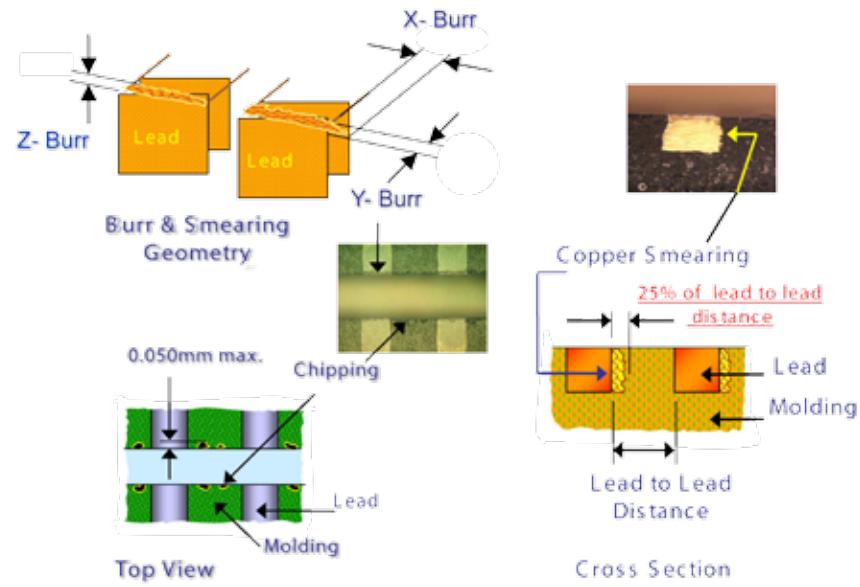


Figure 5: QFN quality criteria

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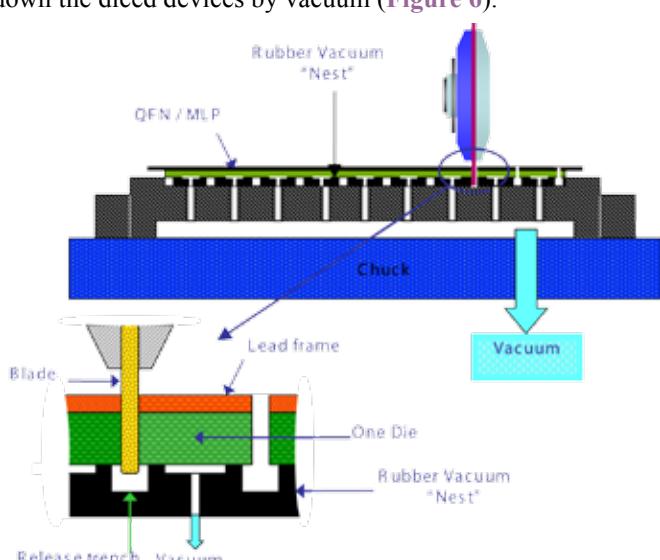
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Figure 6: Tape-less chuck concept

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The main limitation of the tape-less jig is its ability to hold devices smaller than 3x3mm. The reason for this limitation is the insufficient surface of each device to be held up to the jig solely by force of the vacuum. In those cases, a tape mounting is the only practical alternative. Still, there are advantages of a tape-less mounting system: 1) shorter handling time, 2) cost savings - no need for expensive UV tape, 3) cut depth is less critical as opposed to tape mounting, 4) a tape mounter and UV station are not needed, 5) a mechanical support for the side/rim copper edges can be designed, 6) can be used in a fully automated production line, and 7) much higher throughput.

Disadvantages of a tape-less system include 1) less flexibility - a special jig for each device size is required, 2) it can only handle devices down to 3x3mm, 3) less durable with respect to vacuum-related failures such as die fly off, and 4) it requires expensive and complicated equipment compared to stand alone dicing systems.

Optimizing the Dicing Process

Any dicing process optimization requires a close look at the dicing saw process parameters and in parallel, optimizing the dicing blade. QFN/MLP applications differ from user to user. Most users have a variety of QFN substrates with different geometries, layout thicknesses, device sizes, number of copper leads, lead designs, etc. The vast majority of these attributes derive from the product's functionality. The main dicing parameters to be optimized, aside from the blade selection, which will be discussed later, are listed below.

Mounting. For tape: tape thickness, hardness, UV adhesion tackiness, adhesion force, adhesion relief, and cost. For tape-less: jig design to fit the device size, proper vacuum condition to handle the device.

Cooling. Type (regular water, D.I., additives), temperature, cooling nozzle design/coolant pressure and flow.

Blade dressing and override. Use of feed rate built-up profile.

Spindle RPM and feed rate. Cut

depth (relevant for both tape and tapeless); dicing sequence (cut map) – normally the shorter cut length is to be diced first; alignment, kerf check, and kerf position correction.

Blade Optimization

Besides the dicing equipment, the blade is probably the most important part involved in the singulation process. The QFN materials composite requirements challenge the blade to have conflicting capabilities, practically impossible to blend in a single blade type. Such a blade is expected to be suitable for very ductile materials and very brittle materials at the same time. This contradiction can only be addressed by a trade-off analysis that weighs various requirements such as, quality, blade longevity, and cost.

When QFN/MLP was introduced into the industry, the initial feed rate was ~5mm/sec. Today, the majority of the market is using 70-80mm/sec and some users are even running at 100mm/sec. This high feed rate has become possible partially as a result of improved QFN/MLP substrate geometry (using half-etched lead frames), but mostly because of optimizing the dicing blade matrix. The most common blade used today for QFN singulation is a phenolic resin matrix. Metal sintered blades are also used, but to a much lesser extent. Users continue to demand faster feed rates, longer blade life, and cut quality, while maintaining feed rate and blade life. Along with these considerations, users also strive for low cost.

The main goal of any blade used for

singulating QFN substrates is the ability to maintain a long blade life while maintaining its kerf size. This attribute is essential for the tight tolerance to which the final device/package size is subjected. Any side wear on the blade will eventually affect the device size. Users, however, are less keen at compromising on feed rate and/or quality to achieve the blade life. Resin type blades do have a higher radial wear, which helps maintain a good kerf profile, and at the same time, the right device size. Metal sintered blades do have less radial wear, but they are prone to side wear over time. Such wear would eventually be reflected in the device size as shown in **Figure 7**. Metal sintered blades are harder and tend to result in larger burrs.

Optimizing a blade matrix for either quality or throughput would require a sound understanding of the 1) substrate structure, 2) comprehensive knowledge of the dicing process as maintained on site, and 3) blade formulations and manufacturing techniques.

Most blade parameters do change from user to user depending on the substrate geometry structure and the quality requirements. **Tables 1** and **2** list a few general blade parameters used in the QFN market.

Increasing UPH While Maintaining Cut Quality

The QFN application has been in the market for about a decade and a half with a continuous demand to improve both quality, but mainly UPH. The Initial production feed rate was ~5mm/s

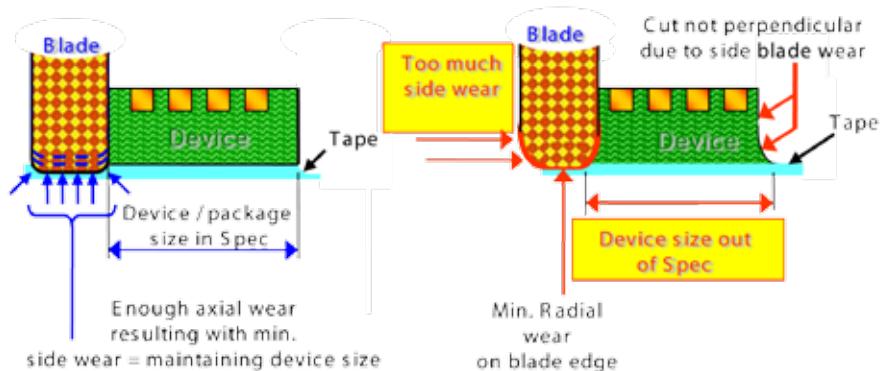


Figure 7: Effect of too much side wear

Substrate thickness (mm)	Device size (mm)	Mounting	Blade Matrix	Blade thickness	Diamond grit size (μm)
0.8 - 1.2	1 x 1 up to 12x12	Tape	Resin	.008"- .020" 0.200-0.508mm	45 - 88
0.8 - 1.2	3 x 3 up to 12x12	Tape-less	Resin & Sintered	.008"- .020" 0.200-0.508mm	45 - 88 - Resin 40 - 53 - Sintered

Table 1: General blade parameters for standard QFN packages

Substrate thickness (mm)	Device size (mm)	Mounting	Blade Matrix	Blade thickness	Diamond grit size (μm)
0.4 - 0.6	1x0.6, 1x1 up to 4x4	Tape	Resin	.008" - .012"	45 - 53
0.4 - 0.6	1x0.6, 1x1 up to 4x4	Tape	Metal Sintered	.008" - .012"	35 - 45

Table 2: General blade parameters for thin QFN packages

with a life span of about 200-300m. Today, end users are dicing standard QFN production at up to 100mm/s with a life span of about 2,000m. There is unrelenting pressure from the industry to further increase the UPH. In pursuit of higher UPH to maintain competitiveness, blade manufacturers continually invest in R&D programs aimed at developing new blade matrices, i.e., new resin formulations,

diamond types and fillers, in order to meet demanding requirements.

Recently, we developed new resin formulations (called T-T07) with better performance than currently available. **Figure 8** compares the new matrix blade wear to previous matrices and other blades. This phenolic resin matrix has been shown to comply with the quality requirements while maintaining a longer life. 

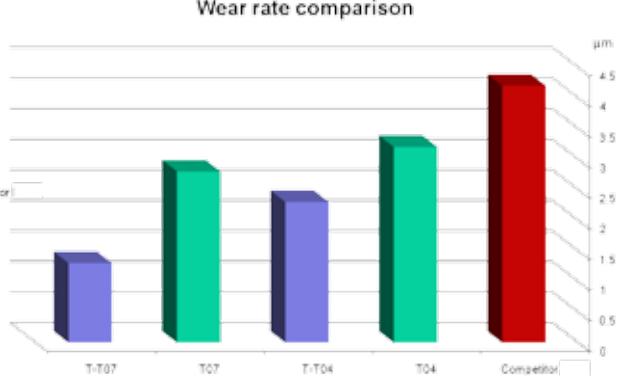


Figure 8: Wear comparison

Biography

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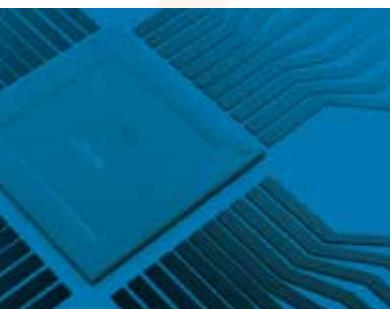
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J. P. Sercel Associates 220 Hackett Hill Road Manchester, NH 03102 Tel: +1-603-518-3200 www.jpsalaser.com	<p>Method: Laser</p> <p>Automation: WA, CM</p> <p>WD: CM</p> <p>FR: CM</p> <p>Models (1)</p>		<p>Method: Laser</p> <p>Automation: LU, WA, CM</p> <p>WD: 300 mm</p> <p>FR: CM</p> <p>Models (2)</p>
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Solder Paste Dipping and Reflow using 0.4mm-Pitch PoP Packages (Part 1)

Christopher Nash, Maria Durham, *[Indium Corporation]*

The electronics industry's trend toward miniaturization of electronic assemblies necessitates smaller pitch and bumps on chip-scale-packages (CSP) and package-on-package (PoP) components. This has led to the need for novel solder paste characteristics. A solder paste's flux vehicle rheology, powder size, and metal load all play a crucial role in its dipping and reflow performance. Additionally, it is equally important to understand the role of the actual dipping and reflow processes with regard to performance of the material.

When the solder balls (spheres, bumps) of a PoP component are dipped into solder paste then soldered, the dipping processes add flux to the soldering process, solder volume to the solder joint, and the paste deposit helps bridge any gaps between the warping components and boards. The paste's solder powder enhances the formation of robust solder joints, even when the substrate twists and gaps form between the solder sphere and the substrate.¹ The reliability of a solder joint created with solder paste is greater than that of a solder joint created with just tacky flux because of the extra volume of solder provided to each joint. "Based on previous works done on the relationship between BGA solder joint quantity and solder joint strength and reliability, greater solder quantities generally result in greater joint strength."² The PoP and CSP assembly processes, however, require a special solder paste. Testing shows the differences between normal SMT solder pastes, and solder pastes specifically formulated for a dipping process are critical for optimum process performance. More specifically, testing shows there are key differences between solder pastes with different

flux vehicles, powder sizes, and metal loads. Process set-up also plays a significant role.

Design of Experiment

The goal of this experiment was to determine which type of paste, and what process settings, provide optimum results for 0.4mm pitch PoP dipping processes. The desired results, post dipping, are a monolayer of solder paste evenly covering ~1/2 to 2/3 of the component's solder balls, and, post-reflow, solder joints with good coalescence, wetting, and ball collapse.

The first portion of this experiment focused on the solder paste's coverage of the component ball to understand the roles of the flux vehicle, mesh size (powder size and powder size distribution), and metal load. It then determined which combination of these factors would provide the best dipping performance. Equipment and process also had to be understood and optimized to obtain the best overall results. Critical control parameters, such as the dip height, dwell time, and retraction speed, were reviewed and adjusted to optimize the process.

The second part of this experiment focused on the reflow performance of the best performing solder pastes. Assembled boards were reflowed in both air and nitrogen (~100ppm oxygen) atmospheres using typical lead-free (Pb-free) reflow profiles to determine the best performing solder paste and reflow environment. The boards (**Figure 1**) are described as follows: 1) Practical Components Part #: PCB250-14mm-TMVDT-OSPHT (PN: 15110); 2) Board size: 5.196" x 3.031", 8-layers, 0.039" thick; and 3) 15 daisy-chained pad placements; and 4) OSP Finish. **Figure 2** shows the following: 1)

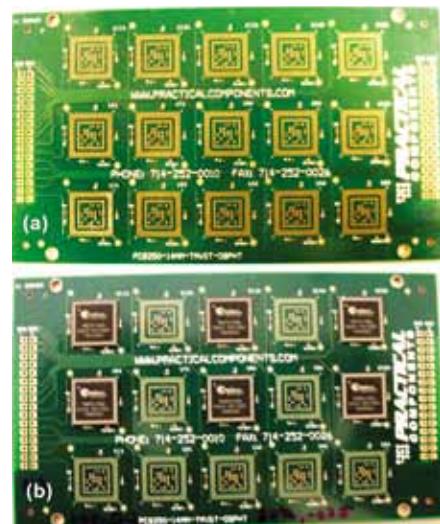


Figure 1: a) Bare board and b) Populated board

Amkor 0.4mm Pitch TMV® PoP (Through Mold Via Package-on-Package), 2) Practical Components Part #: A-TMVPSvfBGA620-.4-14mm-DC-125 (PN: 31558), and 3) bottom package only.

Solder Paste Measurement Techniques

There is currently no pick-and-place equipment that provides optical or laser measurement of solder paste volume on dipped CSP or PoP bumps. This lack of equipment presents a challenge for fine pitch (0.4mm) bumped components. A slight change in solder volume from a variation in the amount of solder paste can have a significant negative effect on bump co-planarity. Too little solder



Figure 2: a) Component top and b) Component bottom

paste on one bump could cause an open. Excessive solder paste on a bump could form a bridge. Given the lack of measurement capability, our solder paste volume was evaluated in two ways: 1) Subjectively: by eye under magnification, and 2) Quantitatively (indirectly): weight measurements of the component were taken before and after the parts were dipped into solder paste. The solder paste weight deposited onto the solder bumps is shown in **Table 1**.

Based on weight, these conclusions were made: 1) Surprisingly, a higher solder paste metal load (solder weight as a percent of solder paste weight) yields less solder paste transferred to the component bumps; and 2) A solder particle size distribution (PSD) of 5 μm -15 μm (particle diameter range) delivered a smaller amount of solder to the part than did an open-ended PSD (e.g., <20 μm solder particles in the paste).

Current pick-and-place equipment

also does not measure the thickness of solder paste within the dipping reservoir, making this metric equally challenging. Some dipping reservoirs

have a fixed depth (machined into a tooling plate) while other reservoirs employ a doctor blade set to a certain height. Either way, it is difficult to be confident of, or know, the depth of the solder paste in the reservoir and whether the paste is evenly distributed across the reservoir. Consequently, it is challenging to control or measure dip height.

We used a wet film gauge to measure the solder paste depth within the reservoirs. This tool is designed to measure the wet film thickness of paints, inks, adhesives, gel coats, and many other products. It may be difficult to accurately and repeatedly measure

Metal Load (%)	79	80	81
Average Paste Weight for <20 μm (g)	0.0059	0.00465	0.00453
Average Paste Weight for 5 μm -15 μm (g)	0.00427	0.00415	0.00372

Table 1: Solder paste weight deposited onto solder bumps

solder paste with this tool because of the powder particles within the paste. The powder particles inhibit the bottom of the wet film gauge from touching the reservoir's bottom, resulting in an inaccurate solder paste depth measurement. The measurements, shown in **Table 2**, were taken with the wet film gauge. These measurements show that the solder paste thickness is not always equal to the actual depth of the reservoir.

Electrical resistance was measured after reflow to detect electrical continuity. This measurement was performed by testing the daisy chain from the "in" and "out" pins on the

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Depth of the Reservoir (mils)	Measurement of the Wet Film Gauge (mils)
7	5 – 6
5	3 – 3.5

Table 2: Solder paste depth measurement data

board, and also by testing the daisy chain net that was created just for the bottom package (which can be tested on the back side of the board). Based on these resistance measurements, a few conclusions were made and are discussed in the upcoming electrical resistance measurements section (part 2 of this series).

Understanding the Dipping Process

The dipping process seems simple in concept, but in actuality it is not.³ Dipping performance depends on a number of aspects, including the depth of the solder paste in the reservoir, dwell time (time the component is in contact with solder paste), and retraction speed (the speed at which the component is removed from the reservoir). A successful process also depends on the accuracy and repeatability of the placement of the components onto the board, or the bottom package in the case of a PoP process.

Dipping Reservoir. There are several solder paste reservoir styles, depending on the pick-and-place equipment. Rotary and linear reservoirs are the most common, although different equipment manufacturers have their own twist on each. Each style has a slight difference in performance characteristics and may affect the performance of the solder paste material.^{4,5}

Dip Height. Dip height, or the solder paste thickness within the reservoir, helps define the amount of solder paste transferred to each solder ball on the package. Solder paste should evenly coat or cover 1/2 to 2/3 of the ball height with a monolayer of solder spheres, as shown in **Figure 3**. To achieve an even coating, the solder paste depth within the reservoir should be optimized and properly measured/maintained. The coverage will also

depend on the dwell time within the solder paste and the solder paste properties.

Dwell Time.

Dwell time is the time that the component is in contact with the solder paste in the reservoir. Longer dwell

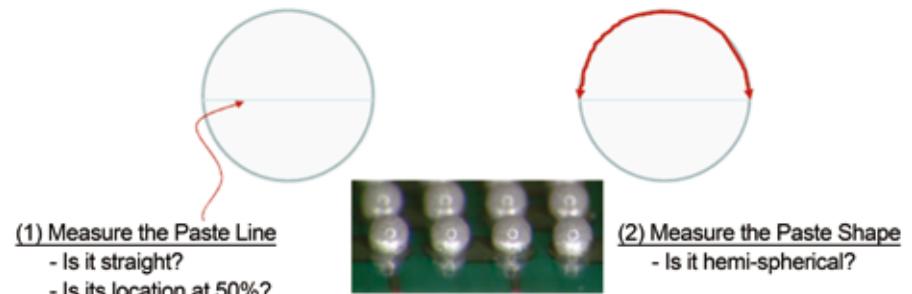


Figure 3: Coverage on solder balls

times allow the solder paste to wet the component balls. This provides better paste coverage, especially on the ball sides. **Figure 4** depicts the differences in solder paste coverage with different dwell times.

Figures 4a and **4b** show dipping results with a short dwell time. The dwell time used was the pick-and-place equipment's default setting (the shortest setting for the equipment, 30 to 50 milliseconds). The pick-and-place nozzle dipped the component into the solder paste until the solder balls

touched the reservoir's bottom. Once the bottom was reached, the component was immediately retracted from the reservoir. Inspection revealed that the solder paste did not fully cover the component ball sides evenly and that there were gaps between the solder paste particles.

Figures 4c and **4d** show the dipping results using a medium dwell time (250ms). This allowed the solder paste to wet the component balls more evenly than the short dwell time. **Figures 4e** and **4f** depict the dipping results with a long dwell time (500ms). There was

no observable difference between the coverage for the medium and long dwell times. Since the long dwell time would slow the process down, but gave no extra process quality benefits, only the short and medium dwell times were used for the remainder of the testing.

Retraction Speed. Retraction speed is the rate at which the component is

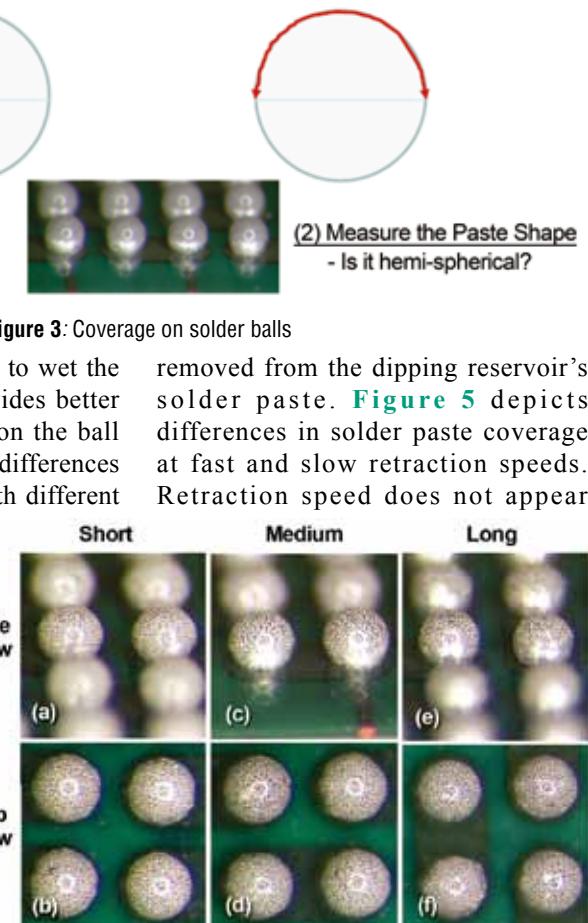


Figure 4: Solder paste coverage with different dwell times

removed from the dipping reservoir's solder paste. **Figure 5** depicts differences in solder paste coverage at fast and slow retraction speeds. Retraction speed does not appear

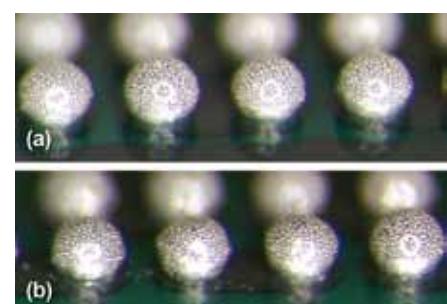


Figure 5: a) Fast retraction speed and b) Slow retraction speed

fast retraction speed was used for the remainder of the testing.

Understanding a Solder Paste's Attributes

The solder paste dipping process is significantly different from the conventional SMT (surface mount technology) printing process in several ways: 1) Dipping paste release is tensile in nature versus shearing; 2) Slump is not a critical parameter; 3) Tack must be low to enable component release; and 4) Solder paste that has been designed for the SMT printing process must have a high thixotropic index so that the solder paste will maintain a "brick" shape and not slump when it has been printed onto the circuit board. Solder paste designed for a dipping process must have a low thixotropic index so that it can coat the component bumps with a tightly-packed monolayer of solder paste particles.⁶

From previous experiments, solder paste designed for SMT printing

cannot be used in a dipping process for packages with $\leq 0.4\text{mm}$ pitch. This necessitates a different approach to the rheological design of the flux vehicle for PoP pastes. To determine the optimal performance, two new solder paste flux vehicles were used in this testing and they were compared to a typical SMT printing solder paste. Powder size had the largest effect on the solder paste coverage of the component bumps. Bump size (required due to the small pitch) have a limiting effect on the size of the powder that is used in the solder paste. Smaller powder particles will coat/cover the bumps more uniformly than larger particle sizes. A test matrix of three flux vehicles and two powder sizes was developed ($<20\mu\text{m}$ powder and $5\mu\text{m}$ -

$15\mu\text{m}$ powder). Details are depicted in Figure 6.

Solder paste A was originally developed for stencil printing. With both powder types, this paste forms cone shape deposits due to its thixotropic nature, which is undesirable due to a possible variation in solder volume. It is important that the "break point" (point at which the solder paste ends and the bump begins) is even across all bumps on the component to minimize variation

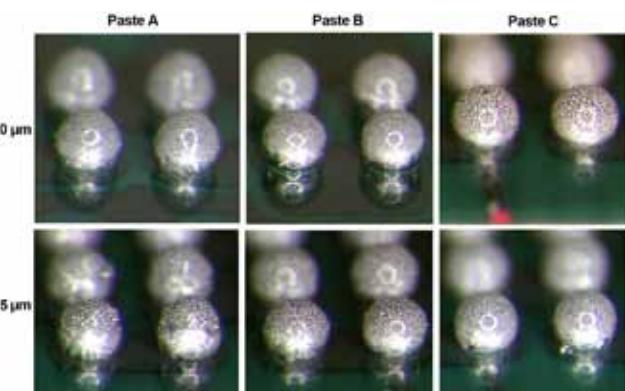


Figure 6: Flux vehicle vs. powder size

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in solder volume between bumps. Paste A, with the <20 μm powder size, shows less than 50% coverage and has a wavy, rather than straight and uniform, break point. Paste A with a 5 μm -15 μm powder diameter exhibits enhanced uniformity in coverage and a more defined and even break point.

Solder paste B was developed specifically for the dipping process. This low thixotropic index paste coats the component bumps with an even monolayer of powder particles. Paste B with <20 μm powder exhibited slight variations in the break point from bump-to-bump and had some spots on the side of the bumps where a few powder particles were missing. Paste B with 5 μm -15 μm powder was uniform across all of the bumps and evenly coated the bumps without noticeable missing powder particles.

Solder paste C (similar to solder paste B with regard to dipping performance) exhibited superior break point performance (more linear) when compared to paste B. This was true for both the <20 μm and the 5 μm -15 μm when comparing paste B to paste C. Comparing paste C with the <20 μm powder to paste C with the 5 μm -15 μm powder, the solder paste coverage was more uniform, and the break point more linear, with the 5 μm -15 μm paste.

Solder pastes containing larger solder particles require a greater reservoir (paste) depth to accommodate the dipping obstruction caused by the particles at the reservoir's bottom. The <20 μm solder paste required 0.007" paste depth to provide 1/2 to 2/3 bump coverage. The 5 μm -15 μm solder paste required 0.005" paste depth to provide the same bump coverage.

Metal Load

Metal load is defined as solder as a weight percent of the paste. Three different metal loads were tested for each solder paste. **Figure 7** depicts solder paste C with 5 μm -15 μm powder. A slight metal load change did not make a noticeable difference in the solder paste coverage of the component bump with any of the solder paste flux

vehicles or powder sizes.

Summary

Creating a constant, uniform, and accurate solder height on the solder balls examined in this experiment is obtained by optimizing the dwell time, retraction speed, and reservoir height (paste film thickness). For this experiment, the optimized settings included a dwell time of 250msec and a fast retraction speed. The solder paste film thickness was more dependent on the solder paste material properties. For dipping applications, a low thixotropic solder paste is desirable because it allows the solder paste to evenly coat the component bumps with a monolayer of solder paste particles. A closed-end particle size range covers the balls more uniformly than an open-ended particle size range. The 5 μm -15 μm powder provided a more uniform coverage, and evenly coated component bumps while providing a more defined and linear break point across all the component bumps (vs. the <20 μm powder). Solder paste particle size determines the solder paste reservoir (dip) depth. Pastes made with larger solder particles require deeper reservoir depths to provide the desired 1/2 to 2/3 coverage of the solder bump. Metal load does not make a noticeable difference in the solder paste coverage of the component bump.⁸

Acknowledgments

This paper appears in two installments. Part 1 addresses the design of experiment, the metrics and data, and the package-on-package solder paste dipping process. Part 2 addresses the package-on-package solder reflow process, the overall conclusions, and suggestions for future study. This paper was originally presented at SMTA 2012 Toronto.

References

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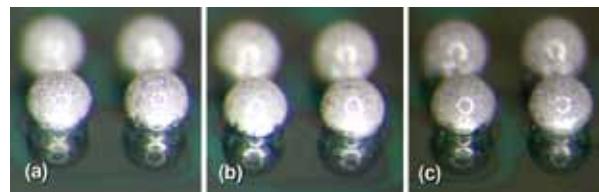


Figure 7: Solder paste C with 5 μm -15 μm powder a) 79%, b) 80%, and c) 81%

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Biographies

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Advancing 3D PoP with Through-Mold Vias

Luz Meneses-Santos, Shawn O'Connor, [Texas Instruments]

3

D package-on-package (PoP) technology has experienced tremendous growth, delivering reduced form factors and miniaturization to semiconductor products used in a range of consumer and portable electronic products. Amkor Technology, Inc.'s through-mold via (TMV®) plays an important role in advancing PoPs and solving key challenges related to warpage, substrates, and flexibility by stacking two dies and/or more than one loop heights for thin PoP packages. This via technology can enable silicon stacking at a lower substrate cost while maintaining, or even reducing, package thickness. With the ability to interconnect another package through a drilled mold cap, this technology also delivers: 1) Lower cost package compared to cavity PoP; 2) Stable molded/exposed ball grid array (BGA) that provides better test handling; and 3) Better surface mount technology (SMT) process. This technology is also well-suited to address PoP challenges and can be used across a number of configurations, including single die, stacked die, and staggered wire bonding to meet a range of application needs.

Lower Cost Package

The emerging need of stacking two or more dies is increasing for most of the package types, including PoP. Cavity PoP allows packaging a two-

die stack for more product functionality (**Figure 1**), but this approach has faced limitations. Cavity PoP uses pin gate mold, allowing the cavity to be filled with mold encapsulates, which exposes the BGA pads for the memory package stack. The cavity PoP package is a five-metal stack substrate with a tall inner via hole (IVH) at the top layer to make up the cavity. The IVH is susceptible to cracking during mechanical stress, which can lead to non-sticking in the substrate's metal structure. The instability of the substrate stack-up does not provide a long term sustainable solution for stacked die PoP.

Through-mold via technology, however, offers a package solution that addresses high-risk areas seen in the cavity PoP¹. This package platform allows for the use of conventional and proven substrate technology, enabling designs with lower cost, higher manufacturability and more consistent reliability package than cavity PoP. The package uses a standard 4-metal layer substrate with a 1-2-1 stack configuration. The advantage in high-density package design is the additional space created for wire bond routing.

The through-mold via PoP package also allows the use of conventional side gate mold processes, comparable to the mold array type of BGA packages. With a side gate block molding and thinner mold, there are potential wire sweep and warpage issues for wire

bonded packages, which is in line with conventional thin mold array packages. The challenge is the cavity PoP package designs use shorter wire lengths to accommodate the cavity, and as a result, limit bond pad locations. The through-mold via package allows greater flexibility in the location of the wire bonds, thereby providing the option for increases in wire lengths. Although this trade lends itself to potential wire sweep issues, the use of smaller filler mold compounds alleviates this concern and continues to keep this wire bond PoP package in a conventional light compared to mold array packages.

There are unique assembly process flows with the introduction of pre-ball and mold laser drill in the development of through-mold via package technology. Now, the pre-ball of the topside memory BGA uses a conventional solder ball attach process and is part of the assembly flow. The mold laser drill process is the newest process technology and is the key to ensuring a non-disruptive package stacking during SMT.

Assembly Challenges

One of the challenges in developing this new technology includes handling of the pre-balled substrate as part of the pre-assembly process. Proper tooling and handling logistics in the die attach, wire bond, and mold processes need to be carefully studied to make sure that the top package BGA balls will not be damaged during the front end assembly.

The right process flow is not easy to identify, especially for through-mold vias. As new processes are introduced, some mature processes will be affected. Laser marking before flux cleaning this new process flow

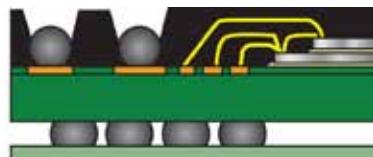
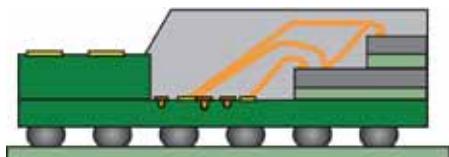


Figure 1: Cavity PoP Structure (left) and PoP through-mold via structure (right)

causes illegible marking, making it hard to read the laser characters. To address this concern, laser marking needs to be repositioned to come after flux cleaning. The highly sophisticated and main process of through-mold via is the mold laser drill process. Being a new process, the following factors are considered: 1) drill hole and depth definition, 2) laser drill machine parameters, 3) automatic inspection methodology, and 4) maintaining top BGA ball cleanliness for good wetting during SMT at the end user.

The via depth, a clearance between top BGA ball to mold surface, is called A-dimension (**Figure 2**). A-dimension process capability is one solution to ensure consistent BGA height and drill hole dimensions. Information about the laser drill hole and depth must be provided in the package outline drawing for end users' reference in optimizing their SMT process for through-mold vias. This, in turn, helps maintain conventional board mount flow.

The post via drill cleaning process

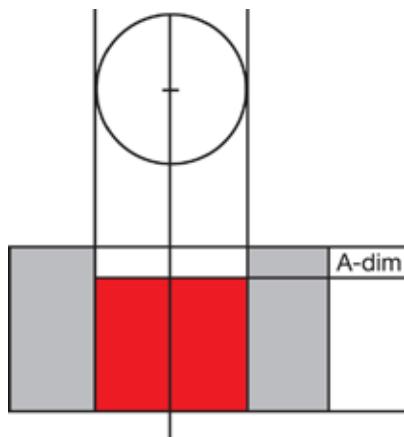


Figure 2: Distance from the solder peak to top surface of mold (A-dimension)

has a significant effect on memory-to-package stacking. Flux or paste applications must ensure 100% coverage on the package BGA ball because inefficient flux/paste coverage on the BGA ball prior to heat excursion can lead to very low yield in stacking memory packages. Machine automation and stencil tooling design play a significant impact on cycle time, and flux/paste application, respectively. The

stencil life and cleaning procedure must be characterized to ensure 100% reflow material coverage. Also, developing a good monitoring of this coverage during in-line processing must be taken into consideration.

Plasma clean process definition is required in through-mold via to ensure the cleanest BGA ball interface for better memory and package stacking. The challenge in defining the plasma clean process is the decision about which plasma gases, or combination of gases, may be required to optimize cleaning. To maintain the quality of the topside BGA ball, in-line SEM inspection is necessary for the through-mold via package to make sure a thin film developed on the BGA ball surface after mold surface drilling is removed during the plasma cleaning process. Although there are challenges with the plasma cleaning process, it is clear that it is more sustainable and doesn't require significant engineering resources.

Test Handling Related Challenges

From a test handling perspective, PoP packages need custom test sockets because of substrate sensitivity to mechanical stress from the variability in the mold cap. The uniform mold cap used in through-mold via technology presents a more consistent test socket contact surface that minimizes package stress, which is typical in mold array packages.

Care must be taken when testing top memory interface pads during development of PoP package test sockets. With a Ni/Au pad finish, interface damage can potentially cause end user issues during the SMT process. Therefore, great care is vital in selecting the right pogo test contact pins and determining optimal contact force conditions. For through-mold vias, use of a topside memory BGA interface is a standard solder ball that can allow the use of more standard test socket components.

A unique challenge of this new via packaging technology is the plasma cleaning process. For top package BGA

balls memory package interconnect, there is a change in the mold surface's roughness that can lead to stuck packages during test release. A test handling approach for through-mold via packages must address these concerns. As package profiles start to decrease, the through-mold via is a preferred platform to use from a test perspective.

Improved SMT Performance

One of the major advantages of PoP packaging is that it allows OEMs to exit the cost intensive memory die market by delivering flexibility to select the best memory for their application. But one major concern with package stacking is warpage level performance of the PoP package. It is critical to manage package level warpage of the bottom package with the performance of the memory package during the SMT process. Because the SMT of two components increases the complexity of the board mounting process, the unfortunate side effect is the need to impose tighter requirements on the PoP package platform to ensure successful package stacking.

The key disadvantage with the PoP package is the presence of the mold cap in a central location on the PoP package, which is also thinner than what is used for stacked die applications. Because of this major limitation, there are few options to address warpage level performance, which primarily focuses on the substrates. This issue becomes increasingly critical with the introduction of copper (Cu) pillar technology. With market trends concentrating on the decrease in package thickness, the single die Cu Pillar enables this requirement.

Through-mold via packaging technology improves warpage performance by extending the mold cap to the edge of the package² (**Figure 3**). This extension helps control CTE differences within the package by limiting the overall amount other package components expand during the reflow cycle, thereby limiting warpage. The simple increase in the mold cap's surface area is a key enabler in

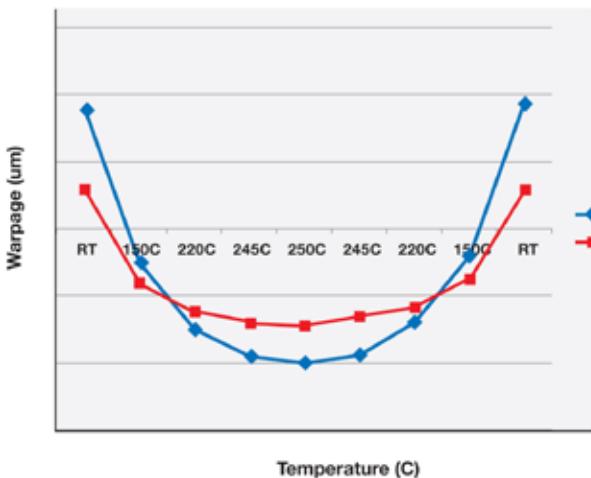


Figure 3: Through-mold via PoP vs. standard PoP warpage

providing a viable method to improve warpage in package stack applications during SMT, while simultaneously creating a window to reduce overall package thickness.

There are two methods of SMT packaging: pre-stack (stacking the PoP and the memory packages prior to board mount) and single-pass (mounting the PoP and memory during the board mount process). The use of a single-pass SMT process is typically a lower cost, preferred option. However, in cases where package warpage performance is relatively poor, the use of a single-pass SMT process becomes less likely – potentially requiring the use of a pre-stack process of the PoP and top package prior to board mount, leading to a likely increase of defects and cost.

The use of a through-mold via package with better warpage control allows end users to continually use current SMT processes to mount the PoP and memory package. Warpage control is an important factor in minimizing the complexity of the SMT process, including: 1) flux dipping of the memory package, 2) screen printing of paste, and 3) stencil design complexity. Warpage control becomes even more critical with finer pitch packaging where warpage can make SMT much more complex as the stand-off height of the solder balls potentially decreases. This is where the new via packaging technology enables a more

traditional SMT process.

Summary

A new through-mold via packaging technology enables die stacking, but also allows package-on-package design with a higher density fine-pitch device that requires multiple loop heights and/or core wire bonding interconnect. Additionally, the arrival of Cu-Pillar

technology enables thinner profile packaging, further increasing package level warpage control challenges for SMT. Cu-Pillar also shares challenges similar to those of wire bonded packages, and through-mold via technology has the ability to improve the warpage performance, further advancing traditional PoP packages. ●

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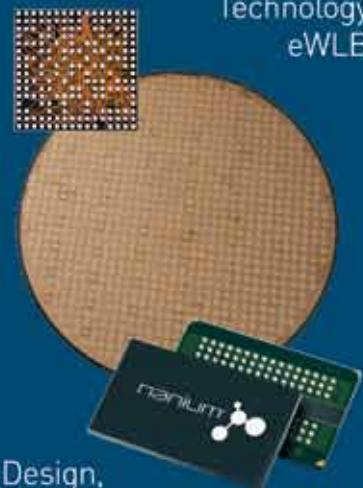
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INDUSTRY NEWS

(continued from Page 16)

Scotland, Meikle has been working in the Asia Pacific region for over 18 years. Initially based in Hong Kong and more recently in Malaysia, he has held positions with Dynacraft Industries,

GEC Plessey Semiconductors, Seagate's semiconductor division; and Burr Brown semiconductors.

In Memoriam

E-tec Interconnect reported the passing of Chris Haffter on August 2, 2012. He was the founder of E-tec Interconnect Ltd. of Moundon, Switzerland. As a long time industry veteran with over 35 years in the electronics business, Mr. Haffter brought a wealth of technical expertise and product. Though E-tec's



Chris Haffter

roots date back to 1973, the E-tec as we know it today was established by Chris in 1992. He will be missed by all who knew him and benefited from his friendship, dedication, experience and ongoing support. He is survived by his wife and two grown children.

Hesse & Knipps' New Wire Bond Head Enables Fine-Pitch/Multi-Stitch Bonding

Hesse & Knipps, Inc., the Americas subsidiary of Hesse & Knipps Semiconductor Equipment GmbH, has added the HBK08 Loop Former Bondhead to its BONDJET BJ935 and BONDJET BJ939 fully automatic heavy wire bonders to support growing requirements for high-density module

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bonding. This heavy wire bond head enables extremely long wire loops, special wire loop formations, and minimal wire distances for fine-pitch bonding, in addition to multi-stitch bonding.

The HBK08 Loop Former Bondhead



HBK08 Loop Former Bondhead

enables the formation of loops or wire bridges with lengths up to 40mm and low loop heights with considerably higher wire stability than previously possible on any heavy wire bonder. A

controlled bend induced into the wire by the loop former of the bond head during the loop trajectory within <50ms creates a considerably steeper loop fall in the back part of the wire bridge compared to conventional loop forms. With this loop formation, the distance of the wire bridge to the neighboring live circuit paths can be increased, creating a positive influence on the design rules of power modules.

Assembléon Introduces Wafer Handling for Flip-Chip Bonder

Assembléon is adding wafer feeding to its A-Series Hybrid. The new DDF Innova Direct Die Feeder converts Assembléon's pick and place machine from a high-speed chip shooter into a high-speed flip-chip bonder, feeding devices directly from

up to 300mm wafers. The A-Series Hybrid reaches controlled die bonding speeds of up to 15,000 components per hour at maximum accuracy, and



Direct-die feeding on A-Series Hybrid

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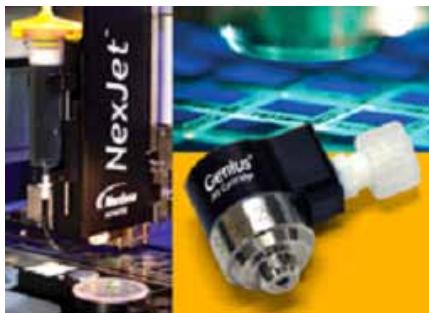


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passive component placements up to 121,000 cph. It is a single-machine solution for applications such as, system-in-package, multi-chip module, flip-chip bonding, and embedding passive and active components into substrates. The DDF Innova feeder supplies bare die products directly from up to 300mm (12-inch) wafers to the A-Series Hybrid. They can be presented in flip-chip (bumps down) or direct-die (bumps up) mode. Wafer mapping ensures that only known-good-dies with sizes from 0.7mm (any edge), are presented to the machine.

Nordson ASYMTEK Releases New Jetting System

Nordson ASYMTEK recently released its NexJet™ jetting system including its one-piece Genius™ Jet Cartridge. The cartridge is the only part of the system that contains fluid, and therefore, that needs to be changed and cleaned. The system can deliver 300 shots of fluid in one second. An RFID transceiver embedded in the dispense system



Nordson ASYMTEK NexJet™ jetting system.

communicates with the stored memory on the cartridge, ensuring that the correct cartridge is installed, and checks to see if the cartridge is within life expectancy - also alerting the operator when the cartridge needs replacement. The system can accommodate a variety of fluids for many applications, such as stacked die, precision coating, LEDs, flat panel displays, lab-on-a-chip, MEMS packaging, and others.

Henkel Reduces FC Package Stress with New Underfill

Henkel Electronic Materials has developed a new underfill system, LOCTITE ECCOBOND UF 8840, that is designed to reduce package stress through controlling die and substrate warpage. The new material targets flip-chip devices.

Because the substrate and flip-chip die have different coefficient of thermal expansion (CTE) characteristics, thermal processing (secondary reflow) can lead to either upward ("smiling") or downward ("crying") package warpage that may ultimately result in poor reliability. The company noted that, as die and

substrates get even thinner, controlling warpage is becoming more critical than ever before, but the new material is designed to effectively control warpage even as die thickness diminishes.

Multitest Offers a 2D Code Reader Option for Full Device Traceability

Multitest announced that it provides a 2D code reader as an option with its MT2168 test handler. The code reader identifies each single package; the package ID can then be used to verify the data with the lot information provided to the handler either by manual HMI input or via a scanned bar code. The ID of each device under test can be read via RS232 or IEEE interface. The reader enables test results to be unambiguously assigned to the device under test ID.

DB Design Lends Hand to Fabless and Start-ups with New IC Handler

DB Design introduced the ATOM IC Handler - a small-footprint automated device handler geared toward small-run engineering, qualification, and characterization processes. The system addresses the needs of start-ups and small fabless manufacturers who need an alternative to hand-test. ATOM IC fills the void in product offerings



ATOM IC Handler

between hand-test and most automated test handler solutions that are intended for higher throughput and faster index times. The system measures 33 x 26 inches and weighs less than 80 pounds. There are up to two standard binning options and throughput is up to 500UPH. The system is available in ATE or SLT/bench configurations and has options for single and tri-temp testing. 

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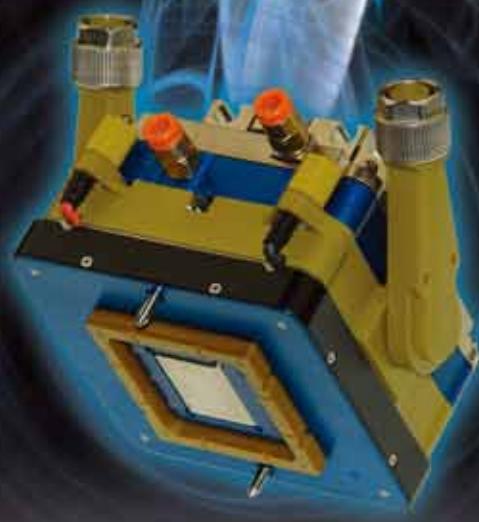
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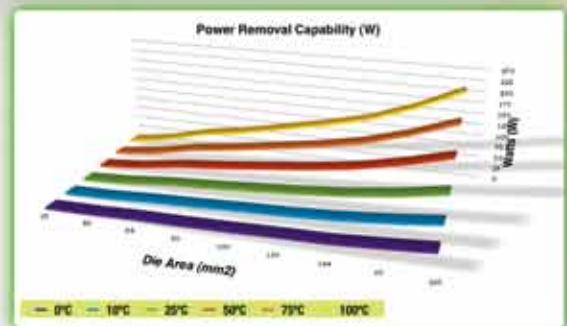
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