

# Chip Scale Review®

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*The Future of Semiconductor Packaging*

Volume 19, Number 5

September • October 2015

Packaging ICs to survive the automotive environment

Page 18

- Out of this world electronics packaging
- Package-level integration of MEMS in IoT devices
- Thermocompression bonding for flip-chip technology
- Bond tester study of CSP reliability through bump analysis
- System scaling: the next frontier for a new era of electronic systems
- Performance of optimized lithography tools in advanced packaging applications





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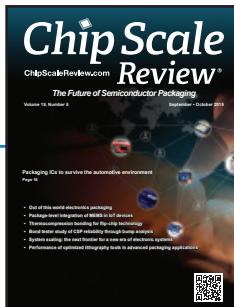
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# CONTENTS

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Electronics packaging is constantly evolving to meet the demands for automotive, medical and consumer products that require improved performance. Automotive electronics are among the most demanding in harsh environments and must meet higher standards in order to ensure reliability and safety. Progressive packaging technologies from lead to surface mount to MEMS, 3D, and die-level packaging will continue to place even more stringent demands on IC packages in these automotive applications.

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## DEPARTMENTS

### Technology Trends System scaling: the next frontier for a new era of electronic systems

Rao Tummala  
*Georgia Institute of Technology*

5

### Market Trends Package-level integration of MEMS motion sensors in IoT devices

Stephen Breit  
*Coventor, Inc.*

10

### Guest Editorial Photonics integration and packaging gaining traction

Hiren D. Thacker *Oracle*  
Stefan Weiss *II-VI Laser Enterprise*

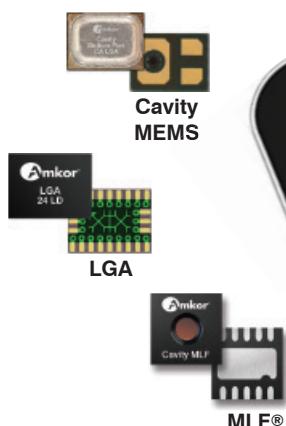
15

### Advertiser Index, Advertising Sales

56

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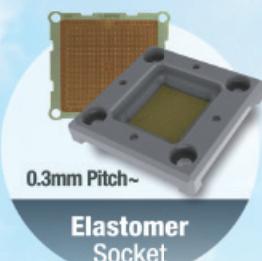
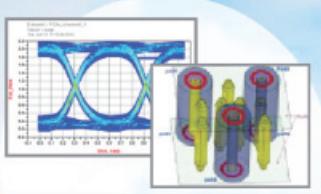
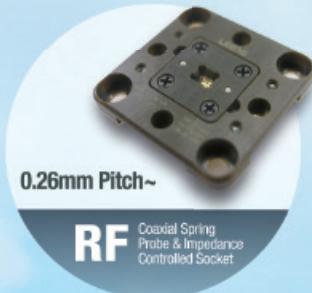
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## FEATURE ARTICLES

	<b>Packaging ICs to survive the automotive environment</b> Prasad Dhond <i>Amkor Technology®</i>	18
	<b>Out of this world electronics packaging</b> Andrew A. Shapiro <i>Jet Propulsion Laboratory, California Institute of Technology</i>	25
	<b>Thermocompression bonding for flip-chip technology</b> John H. Lau, Li Ming, Nelson Fan, Ringo Tse <i>ASM Pacific Technology Ltd.</i>	30
	<b>Using cost modeling to make better design decisions</b> Amy Palesko <i>SavanSys Solutions LLC</i>	37
	<b>Bond tester study of CSP reliability through bump analysis</b> Evstatin Krastev, Ian Christopher Mayes, Chan Myat, Armin Struwe <i>Nordson DAGE</i> Rene P. Zingg <i>Zinan GmbH</i> , Ricardo Geelhaar <i>PacTech GmbH</i>	41
	<b>Solving delamination in lead frame-based packages</b> Rongwei Zhang, Yong Lin, Abram Castro <i>Texas Instruments Inc.</i>	44
	<b>Performance of optimized lithography tools and materials in advanced packaging applications</b> Keith Best <i>Rudolph Technologies, Inc.</i>	49
	<b>New choices for low-temperature dielectric films</b> Robert L. Hubbard <i>Lambda Technologies, Inc.</i>	51



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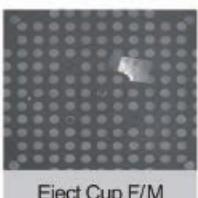


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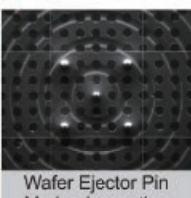
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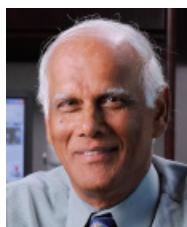


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## System scaling: the next frontier for a new era of electronic systems

By Rao Tummala *[Georgia Institute of Technology]*

**W**hat made electronics the largest global industry at \$1.4T has been the singular focus on transistor scaling. The semiconductor, packaging and systems landscape, however, is changing dramatically. For example, on one hand, ICs, for the most part, are becoming commodities, providing much lower profit margins than ever before, thereby leading to industry consolidation to less than five manufacturing companies worldwide within the next decade. In addition, the cost and complexity of transistor scaling is growing exponentially. There is no longer a cost reduction as the next node is introduced with higher transistor density. It's becoming apparent that transistor scaling is slowing down as well, taking much longer from node to node than previous transitions. In addition, there are two main technical problems with transistor scaling to form the most advanced ICs: in the front end, it is the dielectric leakage, and in the back end, it is the interconnect performance. So-called RC delays, known to be a problem for two decades, are the reason for the performance problem. The average delay due to high-resistance copper interconnections increases by almost 50% from the 45nm to the 7nm node. On top of that, design and process complexity of ICs beyond 14nm go up exponentially, adding to the yield and cost issues. Can system scaling enable better devices?

The second challenge concerns the packaging of devices. Most of the current packaging is to package single devices, such as Intel's processors for PCs and laptops. Traditional packaging is adding

minimal value to these applications by becoming costly, bulky, and in addition, it detracts from chip reliability. In this need, the best packaging seems to be no packaging and assembly at all. This is clearly one of the drivers for chip-first or embedded packaging. Can system scaling address these challenges?

The third landscape change is about the emerging electronic systems. The driving engines for electronic systems are changing dramatically to small systems, such as smartphones, and ultra-small systems such as wearables, like the Apple watch that promise to perform every imaginable heterogeneous function.

On the other extreme, large systems such as automotive, are entering a new era of self-driving, smartphone-like infotainment within the car, as well as in all-electric cars. These systems perform dozens of heterogeneous functions that include digital and wireless communications; wireless sensing, stereo cameras, mm-wave electronics, high-bandwidth electronics or photonics for data processing from 100s of sensors and with data security; and high-power and high-temperature electronics for all-electric cars.

Integration of the above mentioned heterogeneous functions is more than transistor scaling and integration by Moore's Law, and a lot More than Moore's Law (MTM) with stacked heterogeneous integration of ICs, or system-in-package (SiP). Georgia Tech calls this next era of integration System Moore's Law (SM) by system scaling for complete system

integration of electronic systems such as smartphones, wearables, Internet of Things (IoTs), automotive electronics, and cloud computing.

### System scaling R&D at Georgia Tech

The end goal of system scaling is to enable entire system-on-one single package (SOP) in contrast to system-on-chip (SoC) by transistor scaling alone, with a market size as big as all the electronics to date. The progress in system scaling is illustrated in **Figure 1** and shows the gap between transistor scaling as measured by node in nanometers, and system scaling, as

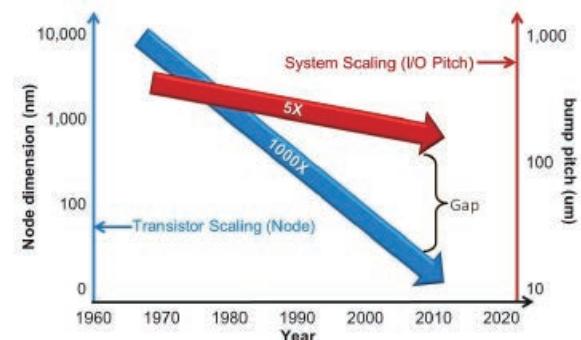


Figure 1: Gap between transistor scaling and system scaling.

measured by off-chip interconnection pitch in microns over the last 40 years.

Georgia Tech has put together a global industry consortium it calls SSI (System Scaling and Integration), to explore and develop the System Moore concept from design to demonstration involving 50 integrated device manufacturers (IDMs), original equipment manufacturers (OEMs), outsourced semiconductor assembly and test services (OSATs), package foundries, and package materials and tools suppliers.

Georgia Tech is pioneering glass-based device and systems packaging

Characteristic	Ideal Properties	Materials				
		Glass	SC Si	Poly Si	Organic	Metal
Electrical	<ul style="list-style-type: none"> <li>High resistivity</li> <li>Low loss and low k</li> </ul>	Good	Fair	Fair	Good	Poor
Physical	<ul style="list-style-type: none"> <li>Smooth surface finish</li> <li>Large area availability</li> <li>Ultra thin</li> </ul>	Fair	Good	Good	Fair	Fair
Thermal	<ul style="list-style-type: none"> <li>High Conductivity</li> </ul>	Fair	Good	Good	Poor	Fair
Mechanical	<ul style="list-style-type: none"> <li>High strength &amp; modulus</li> <li>Low warpage</li> </ul>	Fair	Fair	Fair	Poor	Fair
Chemical	<ul style="list-style-type: none"> <li>Resistance to process chemicals</li> </ul>	Good	Fair	Fair	Poor	Fair
TPV and RDL Cost	<ul style="list-style-type: none"> <li>Low cost Via formation and metallization</li> </ul>	Fair	Poor	Fair	Fair	Poor
Reliability	<ul style="list-style-type: none"> <li>CTE matched to Si and PWB</li> </ul>	Good	Good	Fair	Poor	Fair
Cost/mm <sup>2</sup>	<ul style="list-style-type: none"> <li>At 25µm I/O pitch</li> </ul>	Poor	Poor	Fair	Poor	Poor

**Table 1:** Ultra-thin glass with TSV-like vias as the best system scaling and integration platform.

as the system scaling platform. **Table 1** shows the comparison of glass against single-crystal Si, polycrystalline Si, organic laminate, metal and ceramic packaging. Ultra-thin glass processed as an ultra-large panel (up to 12" x 18") seems to have the best potential to be the system scaling platform with the highest electrical performance, lowest cost, and highest reliability. Such a platform can end up with the highest heterogeneous functionality at the lowest cost in the smallest size that serves both small systems, such as smartphones, and large systems, such as automotive electronics and cloud computing. The reasons for this are many that include the following:

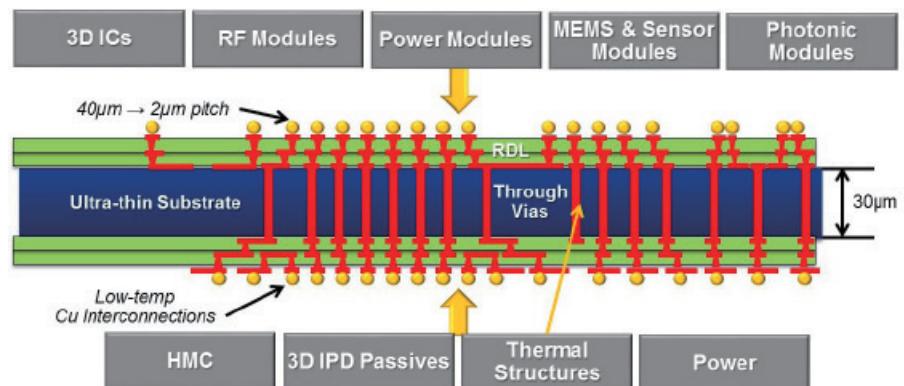
- Outstanding electrical properties: ultra-low electrical loss, low-dielectric constant and ultra-high resistivity;
- Outstanding mechanical properties: intrinsic high strength and high modulus for low warpage;
- Excellent thermal properties: thermal coefficient of expansion (TCE) matching Si, GaN, SiC or GaAs, excellent thermal insulation and excellent thermal conductivity locally with low-cost copper through-vias, slugs and ground planes;
- Excellent chemical properties: no moisture absorption and resistance to chemical processing;
- Excellent Si-like surface finish:

rules so as to end up with an off-chip interconnection pitch in the 5-30 microns range. Any active or passive components including memory stacks, logic processors, WLAN, and LTE modules can be assembled and interconnected on both sides. In this approach for the first time, any two active or passive system components can be interconnected with less than a 100 micron interconnect length.

The fundamentals of SSI with glass packaging are many, and include:

- Short interconnect length for highest performance;
- Ultra-low loss substrates and dielectrics for minimum power consumption in interconnections;
- Ultra-low loss substrates and dielectrics for high-frequency (mm-wave), and data-secure communications;
- Low-dielectric constant dielectrics for high signal speed;
- Through TSV-like vias at fine-pitch for double-side interconnections and assembly of actives and passives to form 3D packages with the same TSV pitch for miniaturization and performance;
- Thick Cu ground planes and large Cu through-vias or slugs for high-thermal dissipation;
- Large panel (510 mm) manufacturing for lower cost than 300mm Si wafers;
- High-performance capacitors and inductors for power; and

The System Moore architecture concept is a 3D system package based on system scaling and heterogeneous integration (**Figure 2**). The fundamental technologies behind this architecture, now and in the near future, are ultra-thin glass, typically 30 microns in thickness; TSV-like vias, typically 5 microns in diameter with a 10-50 micron pitch; and redistribution layer (RDL) with 1-3 micron ground



**Figure 2:** System Moore concept using 3D system package TPV (through-package vias).

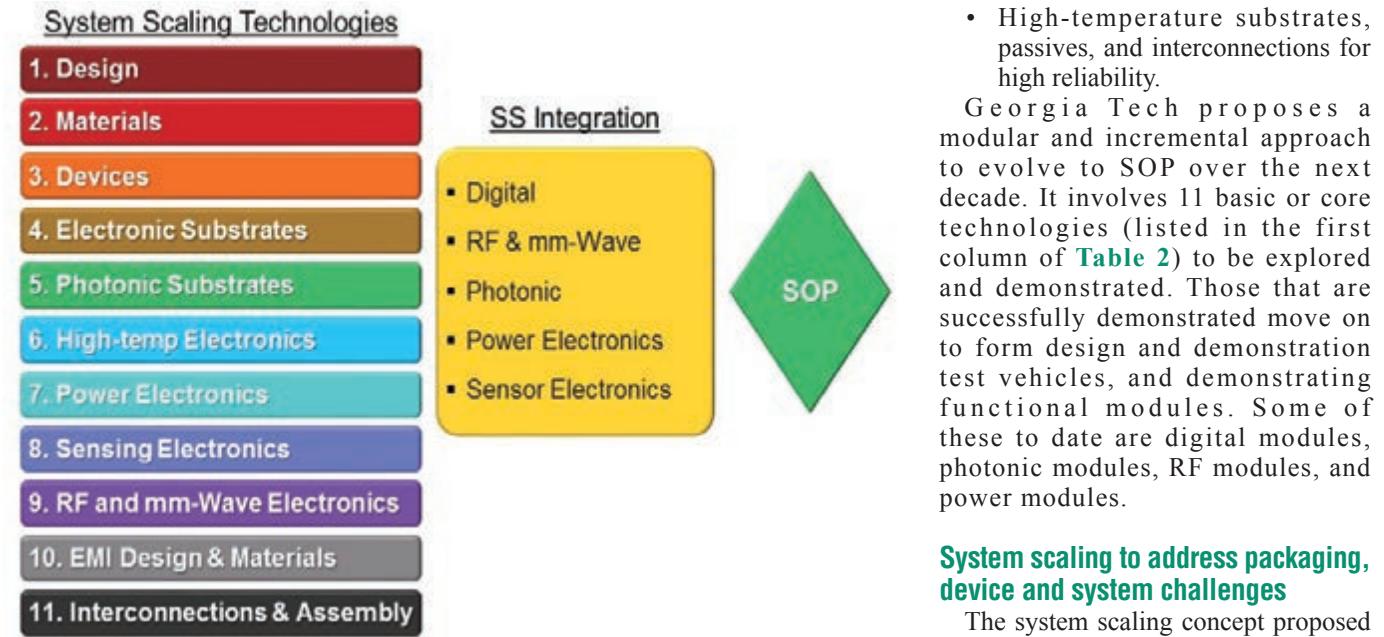


Table 2: System scaling technologies and demonstration TVs.

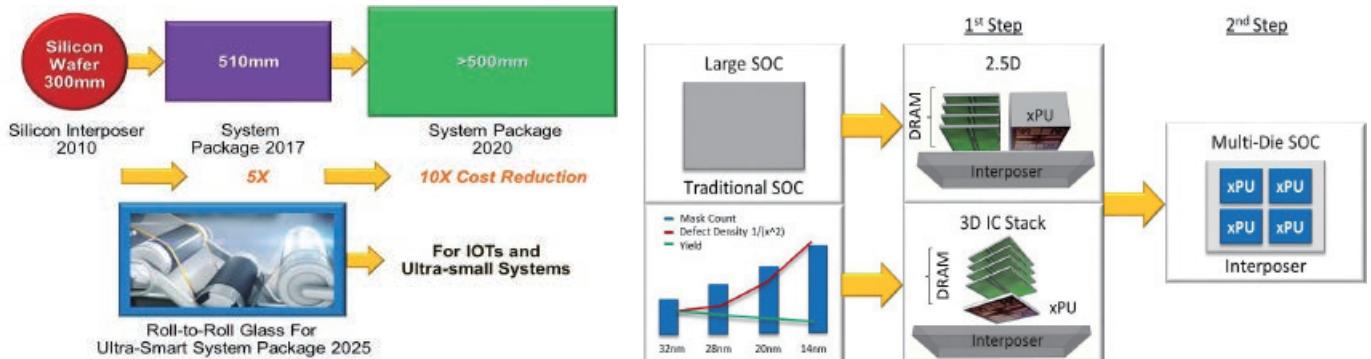
- High-temperature substrates, passives, and interconnections for high reliability.

Georgia Tech proposes a modular and incremental approach to evolve to SOP over the next decade. It involves 11 basic or core technologies (listed in the first column of **Table 2**) to be explored and demonstrated. Those that are successfully demonstrated move on to form design and demonstration test vehicles, and demonstrating functional modules. Some of these to date are digital modules, photonic modules, RF modules, and power modules.

### System scaling to address packaging, device and system challenges

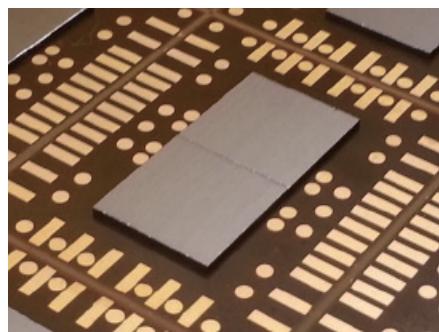
The system scaling concept proposed here is very much in line with the challenges described above in single-





**Figure 3:** Ultra-large area processing for low cost compared to 300mm Si wafers.

**Figure 4:** System scaling to address IC challenges.



**Figure 5:** The first 2.5D glass interposer with two ICs.

chip, multi-chip, and systems packaging as discussed below.

**Single-device packaging.** Georgia Tech believes that ultra-thin glass packaging can lower the cost, improve performance and improve reliability of single-chip devices.

The improved performance is due to ultra-short interconnections between the chip and glass substrate, i.e., about 5 microns. Improved cost is due to ultra large-area processing (**Figure 3**), low warpage and elimination of the organic ball grid array (BGA) package between the glass package and board. The improved reliability is due to TCE match, low moisture absorption, and minimal stress on interlayer on-chip dielectrics (ILD).

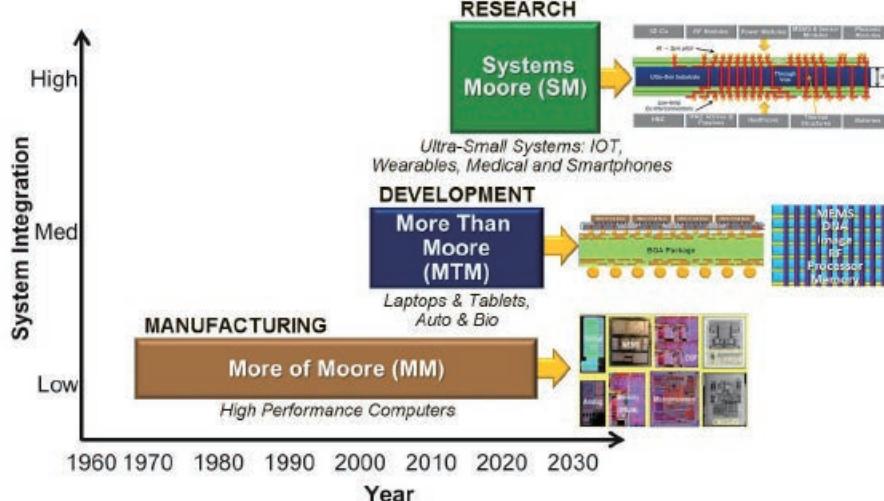
**Multi-device packaging.** Can system scaling address the SoC problems described above and enable better devices? This is one rationale for system scaling, as illustrated in **Figure 4**. System scaling resulting in off-chip interconnections in the 20

micron range in the short term, and 2-5 microns in the longer term, can stitch the four SoCs as if they are one to address yield, cost and performance issues of large ICs. It can also be used at 3-micron lithography now to fabricate 2.5Ds, for packaging 3D ICs with TSVs, and sub-micron lithography for stitching split SOC ICs in the near future **Figure 5** shows the first 2.5D prototype glass interposer designed and fabricated to demonstrate this concept.

**Systems.** **Figure 6** summarizes the system scaling as a new frontier leading to the System Moore concept for ultra-miniaturized heterogeneous small systems, such as smartphones, and large systems, such as automotive electronics and cloud computing. Georgia Tech sees the 3D glass system package architecture as the basis of an all new era of electronic systems.

## Biography

Rao R. Tummala received his PhD in Materials Science and Engineering at the U. of Illinois. He is the Joseph M. Pettit Endowed Chair in Electrical and Computer Engineering and in Materials Science and Engineering at the Georgia Institute of Technology; he is also the Director of the Packaging Research Center (PRC) at the Georgia Institute of Technology; email rao.tummala@ece.gatech.edu.



**Figure 6:** 3D system-on-package for all systems functions on one package.

# BETTER TECHNOLOGY STRONGER TOGETHER

## JCET Completes Acquisition of STATS ChipPAC to Ascend to a Leading OSAT Player Globally

China's leading semiconductor packaging and testing company, Jiangsu Changjiang Electronics Technology (JCET, SHE: 600584), successfully completed the acquisition on Aug 5 2015 of STATS ChipPAC, a leading provider of advanced semiconductor packaging and test services headquartered in Singapore. This USD 780 mn transaction was originally announced on Dec 30 2014, and was conducted through JCET-SC (Singapore) Pte. Ltd., a subsidiary of JCET.

This acquisition will escalate the combined entities to one of the world's top outsourced semiconductor assembly and test (OSAT) players. As a combined group of companies, JCET and STATS ChipPAC offer a broader technology portfolio with significant manufacturing scale in key semiconductor geographies. The acquisition will also improve the competitiveness of the Chinese semiconductor packaging and test industry with a strong intellectual property (IP) and innovation portfolio built around advanced technologies acquired by JCET.

"The completion of our acquisition of STATS ChipPAC is an important step for us, and it presents an exciting win-win opportunity for both companies, supporting our long-term success," said Xinchao Wang, Chairman of JCET. "Post acquisition, the combined entities will provide one of the most extensive product/service portfolios to a highly diversified customer base with wide geographical coverage. Our leadership position in advanced packaging technologies will be further strengthened through the acquisition. JCET and STATS ChipPAC are working together to deliver the substantial revenue and cost synergies for our investors."

For more information, visit [www.cj-elec.com](http://www.cj-elec.com) or [www.statschippac.com](http://www.statschippac.com).



## Package-level integration of MEMS motion sensors in IoT devices

By Stephen Breit [[Coventor, Inc.](#)]

The trend of integrating heterogeneous technologies at the package level is now well underway, and includes MEMS sensors. Heterogeneous package-level integration arguably reached a new milestone with the release of the Apple Watch. A Chipworks teardown [1] shows more than 30 dies in the Apple Watch's S1 package. Curiously, a MEMS inertial measurement unit (IMU) by STMicroelectronics is among the few components not included in the S1 package. The IMU contains capacitive MEMS motion sensors including a 3-axis accelerometer and a 3-axis gyroscope (technically, an angular rate sensor). Surely Apple and other Internet of Things (IoT) device makers will strive to achieve higher-density, package-level integration of MEMS motion sensors in the future, but will need to overcome risks associated with packaging these sensors.

We'll briefly discuss the importance of MEMS to IoT devices, and the motivations for heterogeneous package-level integration. Then we'll describe the key challenge – temperature stability – in packaging capacitive MEMS motion sensors, and a design methodology for addressing the challenge. Understanding this packaging challenge and the design methodology provides insight about the technical and business barriers to package-level integration of MEMS motion sensors. Packaging risks may have deterred Apple from package-level integration of the MEMS motion sensors in its first-generation Watch. Changes in the relationship between MEMS suppliers and IoT device makers will be required to enable denser packaging of MEMS motion sensors in future generations of IoT devices.

IoT spans a wide range of technologies, including smart devices that interact with their environment, wireless technologies, internet infrastructure and protocols, data centers, cloud infrastructure, software infrastructure, and software applications. It is widely acknowledged that low-cost sensors in general, and MEMS in particular,

are a key enabler if not a defining characteristic of IoT. A recent McKinsey report [2] states: "We define IoT as sensors and actuators connected by networks to computing systems. These systems can monitor or manage the health and actions of connected objects and machines. Connected sensors can also monitor the natural world, people, and animals." The report goes on to state, under the topic of technology enablers: "Low-cost, low-power sensors are essential, and the price of MEMS (micro-electromechanical systems) sensors, which are used in smartphones, has dropped by 30–70% in the past five years." Without MEMS, there would be no IoT, or certainly less IoT.

At its heart, heterogeneous package-level integration is about miniaturization and the benefits it provides, namely smaller form factor, lower cost, higher performance, and lower power consumption. Some IoT devices, especially wearables and implantables, will need to use aggressive package-level integration to achieve the form factor, cost, performance and power specifications required for market success. Therefore, the extreme package-level integration seen in the Apple Watch is just the beginning. A recent EE Times article [3] describes the extent to which the semiconductor roadmap has shifted to packaging: "CMOS scaling, once the focus of the ITRS, has become the territory of a handful of consolidated companies now," said Bill Bottoms. "A majority of the improvement in semiconductors going forward will come from heterogeneous integration mainly in complex systems-in-package—bringing things closer together is the only way to get the improvements we need."

In fact, many MEMS parts on the market today already employ heterogeneous package-level integration. A typical 6-axis IMU from a leading supplier such as Bosch, InvenSense or STMicroelectronics includes a 3-axis MEMS accelerometer on one die, a 3-axis

MEMS gyroscope on another die, analog/mixed-signal CMOS on yet another die (bonded to the MEMS in some cases), a digital CMOS microcontroller, and non-volatile memory. A 9-axis IMU adds a 3-axis magnetometer, typically a solid-state Hall-effect device fabricated with a different technology, on yet another die. Heterogeneous package-level integration of MEMS is already happening; it's just a matter of degree and who does the integration. Today, the MEMS suppliers do the integration and provide packaged parts to their customers. In the future, IoT device makers who require even denser integration of MEMS motion sensors will have to do it themselves with assistance from their suppliers (or take full responsibility for the MEMS design).

Most MEMS motion sensors (both accelerometers and gyroscopes) on the market today are capacitive devices. They detect changes in capacitance between a suspended proof mass and stationary electrodes caused by motions of the proof mass in response to acceleration or rotation of the mounted sensor. In-plane motions are sensed by electrostatic comb drives while out-of-plane motions are sensed by planar electrodes attached to the substrate. The proof mass and electrostatic comb stators are connected to the substrate via attachment points known as anchors. Any displacement of the anchor locations causes a change in the relative position of the proof mass to the stationary electrodes and therefore a change in the output capacitance of the sensor.

The key effect of packaging on capacitive MEMS motion sensors is temperature stability. That is, the sensor output versus ambient temperature can only vary within specified limits. MEMS suppliers work hard to design their packaged MEMS components to satisfy temperature stability specifications. To give some appreciation of this challenge, we'll describe the coupling mechanism between the package and temperature stability. The materials that comprise the

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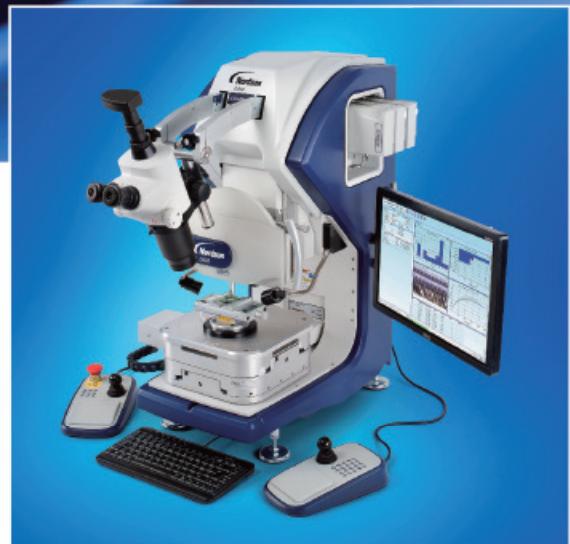
A unique design allows for both multi-function and singulated cartridges to be interchanged in seconds.

## Featured Application

Solder Compound Comparison - The DAGE 4000*Plus* can be used to compare different solder types through standard bond test methods like Shear and Cold Bump Pull. An example would be comparing 3 lead free solders, an SC07, SAC307 and SAC305. For these comparisons where small changes need to be identified, you need a system which has superior accuracy, repeatability and reproducibility.

The 4000*Plus* has a total system accuracy of +/- 0.1% of full scale load and a step back accuracy of up to +/- 0.25 microns allowing for small changes in solder compound to be identified in the measured failure loads.

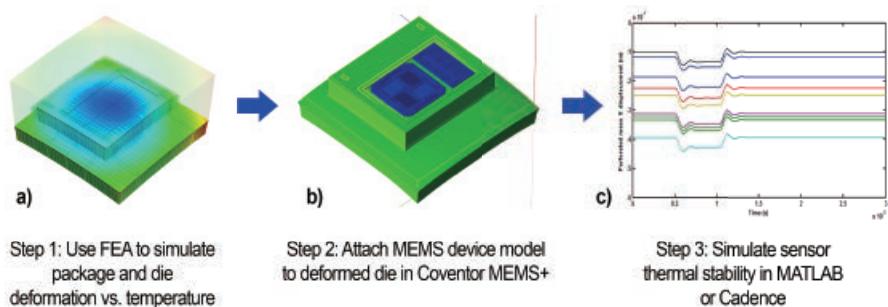
These types of comparison allow for new solder types to be analysed and ensure that the best type is chosen.



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device, substrate, and package expand and contract with temperature in proportion to a coefficient of thermal expansion (CTE). If the CTE for all materials was the same, they would all expand/contract by the same proportions and the relative positions of the proof mass and stationary electrodes (and hence output capacitance) would remain invariant with temperature even though the anchors would be displaced slightly. In reality, the various materials have different CTEs and this mismatch causes the silicon substrate (the die) to warp ever so slightly with temperature changes as adjacent materials expand/contract more or less than their neighbors. The warping changes the anchor locations, affecting, in turn, the relative positions of the proof mass and electrodes and therefore, the output capacitance. If the output varies too much with temperature, the sensor will not meet its temperature stability specs.

For more than a decade, Coventor has worked with leading suppliers of capacitive MEMS inertial sensors to develop a methodology that accurately predicts package effects on temperature stability. The methodology is illustrated in **Figure 1**. The first step is to simulate the static deformation of the package and MEMS substrate for a range of temperature values. This simulation is usually performed by package designers using a general-purpose finite element analysis (FEA) tool such as Ansys Mechanical [5]. Note that the package analysis includes the MEMS substrate and may even include the PC board to which the package is attached, but not the MEMS device itself. The MEMS device is very small compared to the substrate and the package and therefore assumed to have negligible effects on the deformation of the latter. This is an important simplifying assumption because the MEMS device has a lot of structural details that would greatly increase the computing resources required for the finite element analysis. Next, the package simulation results are imported into Coventor's MEMS+® design environment [6] where they are mated with the MEMS device. MEMS+ moves the anchor and electrode locations in accordance with the package results, as shown in **Figure 2**. Finally, the MEMS+ high-order FEA model of the device with displaced locations is simulated in



**Figure 1:** Methodology for simulating package effects on temperature stability of capacitive MEMS motion sensors [4].

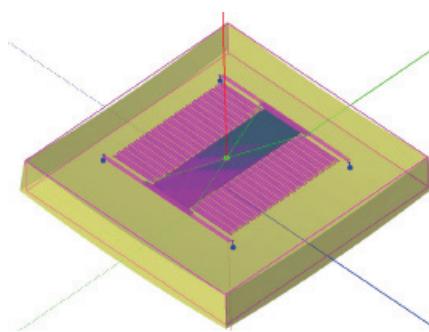
MATLAB, Simulink or Cadence Virtuoso to predict the temperature stability of the sensor output.

With the above methodology in place, the package designers and MEMS designers can explore design modifications that will ensure the packaged sensor meets its temperature stability specs. All is well and good if both the package designers and MEMS designers work for a MEMS supplier and can freely share detailed design information. But suppose an IoT device maker wants to do package-level integration of MEMS motion sensors with many other die, to the extent seen in the Apple Watch? The IoT device maker needs to buy MEMS dies from its MEMS supplier(s) instead of packaged parts and will be responsible for designing the package. To apply the above described package effects methodology, either the MEMS supplier must share details of its proprietary device design with the IoT device maker (highly unlikely), or the IoT device maker must share details of its proprietary package with the MEMS supplier (also unlikely). A meeting point can be found, but will require a new way

of information sharing for both parties and a change in business models as well. We can only imagine the finger pointing that will occur if, after sharing the package effects analysis as described above, the sensor in the IoT device fails to meet temperature stability specs. Evidently, Apple didn't want to take this risk for the first-generation Watch. There can be little doubt that MEMS suppliers and IoT device makers will face and surmount this challenge in the future.

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**Figure 2:** Accelerometer attached to a deformed substrate (die) in Coventor MEMS+. Substrate deformation is exaggerated 100X; blue markers show the displaced positions of four anchors.

## Biography

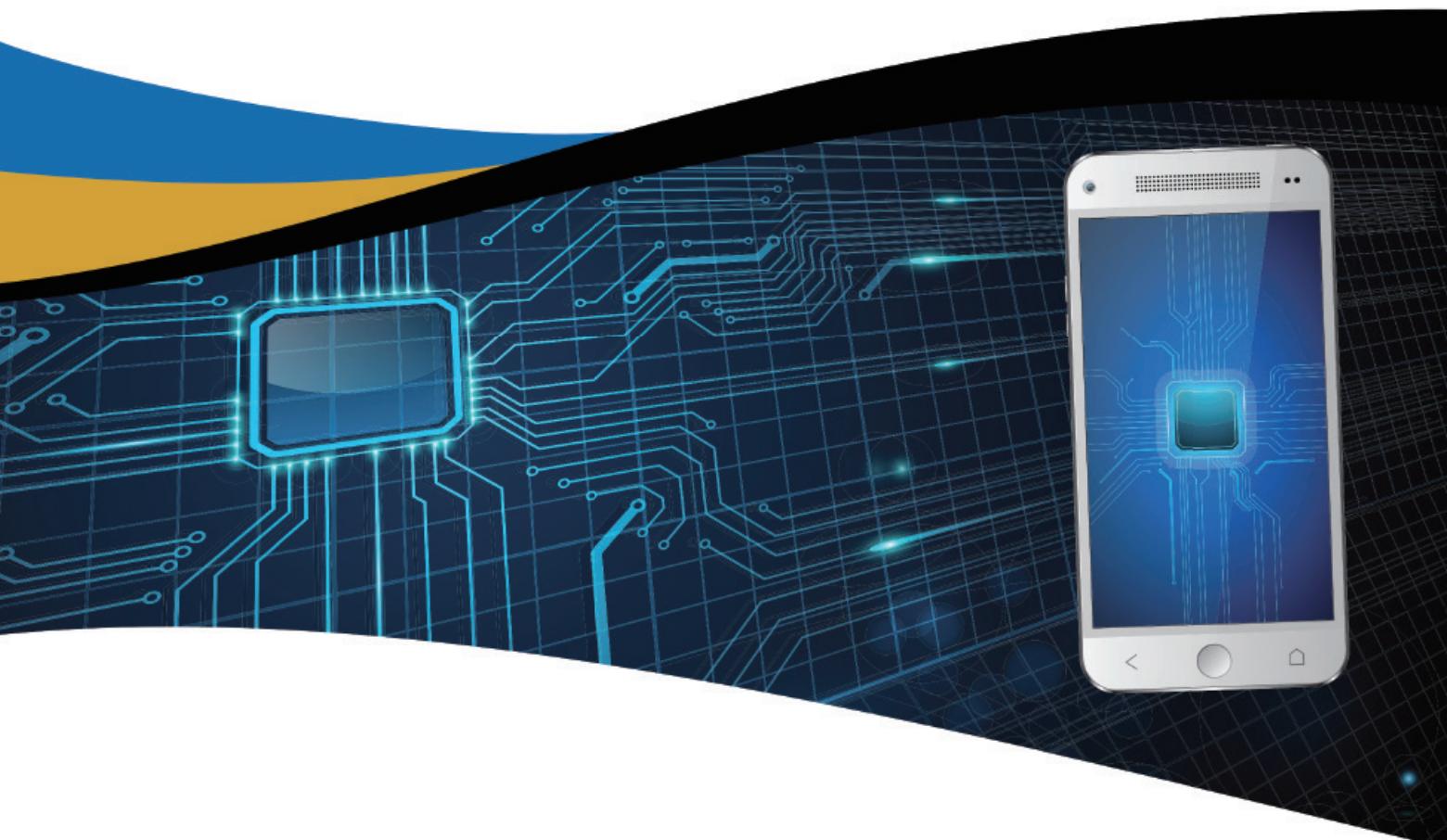
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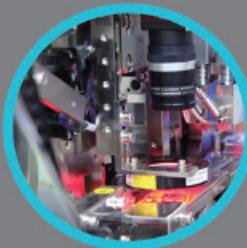
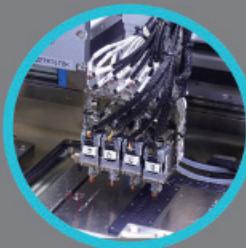
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## Photonics integration and packaging gaining traction

By Hiren D. Thacker [*Oracle*] and Stefan Weiss [*II-VI Laser Enterprise*]

The ever-increasing demand for off-chip bandwidth in high-performance computing systems is continuing to fuel the steady march of optical interconnects from outside-the-box transceiver components, to becoming an integral part of the silicon chipset. The integration and packaging of energy and bandwidth-efficient photonics components, active and passive, have requirements that are much different from those typical to logic and memory ICs. For example, hybrid integrated silicon photonic components require ultra-fine flip-chip interconnects for energy efficiency, single-mode optical interfaces (waveguide-to-waveguide or waveguide-to-fiber) require sub-micron alignment and placement accuracy, and PCBs may require embedded optical waveguides and couplers to facilitate optical ICs. Because these photonics-based communication highways will need to be intimately integrated with their electronic payload ICs, the worlds of photonics and electronic packaging must find a common footing. This trend was on display at the recently concluded IEEE Electronic Components and Technology Conference (ECTC) in San Diego, CA (May 27-30, 2015), where photonics integration and packaging dominated the optoelectronics packaging sessions. The well-attended sessions featured leading researchers in this field from the USA, Europe and Asia, who presented their latest results in topics such as optical multi-chip modules (MCMs), semiconductor optical amplifier integration, optical I/Os, and more. In this article, we summarize these most recent results in the area of photonics/electronics integration and packaging presented at ECTC and expect that this will continue to be a hot-topic for the 2016 ECTC.

### First session: focus on optical interconnects

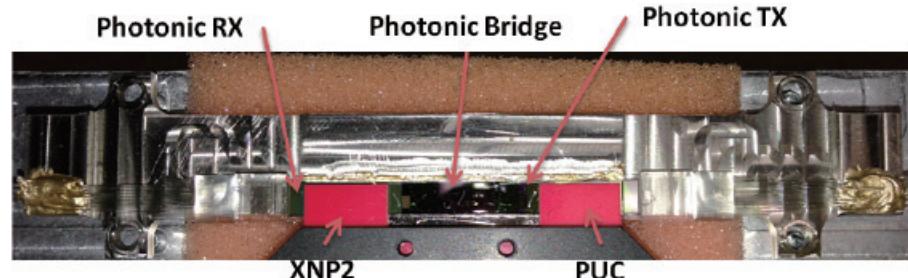
The first session was entitled "Advanced Optical Interconnects." The lead-off paper by Thacker, et al. was a joint publication from researchers at Oracle and Mellanox, wherein the authors described the packaging of a multi-chip wavelength division multiplexed (WDM) silicon photonics interconnect using

an all solid-state single-mode "photonic bridge" transport layer (Figure 1). The WDM link was built with hybrid integrated VLSI and Si photonics components and an off-chip laser; it was shown to successfully operate up to 10Gb/s while consuming <2pJ/bit on-chip power [1]. Following this, Ishigure, et al., of Keio University (Kyoto, Japan), winners of the Outstanding Session Paper at the 2014 ECTC, presented progress in their Mosquito method for fabricating single-mode polymer optical waveguides for board-level silicon photonics IC integration [2]. This unique method 3D prints waveguides, unlike the traditional lithography-based approach. The authors used a novel silicate-based organic/inorganic hybrid material for reducing optical loss and for improved thermal stability.

IBM Yorktown, IBM Bromont, and AFL Telecommunications, presented a joint paper on a manufacturing-capable approach for alignment and edge-coupled assembly of parallelized single-mode optical fiber to silicon photonics ICs [3]. The current implementation, built using methods compatible with high-throughput pick-and-place tooling, can assemble one-dimensional fiber arrays of any size to a V-groove array on a silicon photonics chip. Using in-depth Monte Carlo analysis, they predict this method to yield an expected misalignment of less than 1.3 $\mu$ m between fiber-core and waveguide-coupler during manufacturing, which would be within the acceptable alignment range for single-mode photonics. The next presentation was focused on high-speed and compact optical

transceiver packaging. Researchers from Fujitsu Labs and Fujitsu Components described a double-sided mount card-edge-connected optical transceiver module (DCOM) that integrated an eight-channel optical transceiver using a high-speed FPC connector, inductive peaking line, and an integrated lens on the photodiode built using inkjet technology in a compact package [4]. The module was shown to be capable of 40Gb/s error-free transmission.

2.5D integration using glass and silicon interposers has been a hot topic in the packaging industry. Brusberg, along with his collaborators at Fraunhofer IZM, Contag AG, and TU Berlin, have been at the forefront of developing glass interposers with embedded optical interconnects. Their paper at the 2014 ECTC was winner of the Outstanding Interactive Session Paper Award. At the 2015 meeting, they demonstrated a multi-layer electro-optical circuit board (EOCB) with two embedded thin glass layers, planar integrated gradient-index multimode glass waveguides, a mid-board polymer-based out-of-plane coupling interface, and through-glass vias (TGVs) [5]. The TGVs were fabricated using a laser ablation process in combination with material plugging of the TGVs and mechanical drilling. From 2.5D integration to optoelectronic MCM packaging – the next paper by Tokunari et al., of IBM Japan – presented their work on the assembly and the demonstration of a high-bandwidth density optical MCM comprising bare VLSI and optical chips (VCSEL, photodetector)

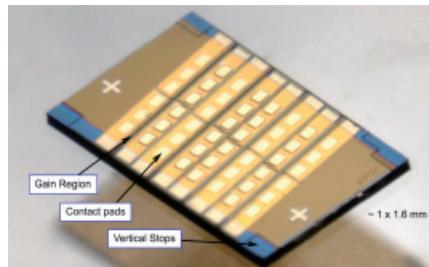


**Figure 1:** Photo of a 5-chip, hybrid integrated energy-efficient WDM silicon photonics solid-state chip-to-chip interconnect subassembly. XNP2 and PUC are the hybrid bonded receiver and transmitter driver ICs, respectively [1]. Photo courtesy of Oracle.

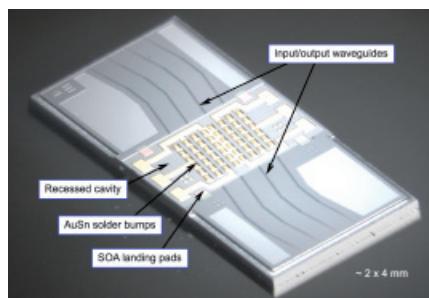
mounted on an optical waveguide-laminated organic substrate [6]. The optical waveguide layer is manufactured via a dry film lamination process, and laser-ablated mirrors formed on the waveguides couple light into and out of the optical chips and newly developed surface normal waveguide-fiber connectors. All channels of the demonstrator MCM package Tx and Rx operated up to 30Gb/s, achieving a bandwidth density of 15Gb/s/mm<sup>2</sup>, nearly eight times larger than that of optical fiber modules. In the final paper of the session, William Vis and his colleagues at the Georgia Tech Packaging Research Center in Atlanta reported on the design and proof-of-concept demonstration of 3D optical waveguides (3D WG) with 45 degree entry and exit planes with respect to optical through-glass vias [7]. They achieved this using a novel inclined lithography technique on an ultra-thin 3D glass substrate. Furthermore, the process enabled inherent alignment of the optical microstructure and the integration for chip-to-chip optical communication.

## Second session: light sources for silicon photonics

The second session was entitled “Silicon Photonics and Light Sources.” The first paper was given by Budd et al., from IBM Yorktown Heights. They designed, fabricated, packaged and characterized a 4-channel semiconductor optical amplifier (SOA) flip-chip bonded to a photonics carrier with monolithically-integrated waveguide layers (**Figures 2 and 3**). Their first samples showed good bond strength of the AuSn solder bumps and a net optical gain greater than 10dB [8]. The second paper by Schneider et al., was a joint publication from researchers of the Karlsruhe Institute of Technology, Germany and the National Sun Yat-sen University, Taiwan. They presented a blue LED module with an optical output power of 235.5W at an optical density of 111.6W/cm<sup>2</sup>. They achieved this by assembling 98 single LEDs with silver sintering onto an AlN substrate, which was cooled by a high-performance micro-channel water cooler. By using glass discs in front of the module doped with variations of phosphor concentration, they could adjust the color temperature [9]. Following this, Shubin et al., from Oracle showed results on a hybrid-assembled WDM photonics transceiver with 8 tunable channels operating at 10Gb/s per channel. The crucial



**Figure 2:** Photo of the semiconducting optical amplifier [8]. Photo courtesy of IBM.



**Figure 3:** Photo of the photonics carrier [8]. Photo courtesy of IBM.

post-processing and packaging details to achieve the all solid-state photonics module were revealed [10]. La Porta, et al., from IBM Rüschlikon presented their first results on the optical coupling of silicon photonics chips and polymer waveguides as a first integration step for system-level assembly of silicon photonics building blocks operating at wavelengths of 1.3μm and 1.55μm. Using highly scalable adiabatic optical coupling, losses as low as 0.85dB for TE propagation at 1.3μm were achieved [11].

In the fifth paper, Uemura, et al., from PETRA, Japan, introduced an array of “optical pins” for a chip-scale parallel optical module. The optical pins are vertical waveguides made from UV-curable resin. A 125μm pitch x 12 channel optical pin array was successfully manufactured using a photolithographic method. This demonstrator showed low coupling losses of 0.41dB for the receiver and 2.3dB for the transmitter. A high coupling tolerance of >25μm at an allowable excess loss of 0.5dB have been achieved. The sixth paper given by Elger, et al., from the Technische Hochschule Ingolstadt, Germany, and Philips, Germany presented new designs for flip-chip bonded LEDs that are directly bonded onto PCB boards. Following the optical and electrical analyses, as well as thermal simulations of different designs,

prototypes have been assembled. The reliability was successfully tested for 1000 hours using thermal shock tests [13]. The final presentation by Wang, et al., from the Leibniz University in Hannover, Germany and the University of Freiburg, Germany, introduced a new packaging technology called “Optodic Bonding.” A low-power laser diode was successfully flip-chip bonded onto a flexible, transparent substrate using a UV adhesive. An additional lamination process strengthens the package [14].

## Summary

The ECTC Optoelectronics Packaging subcommittee solicits papers on all topics pertaining to the design, development, and technology of packaging silicon photonics; optical interconnects; parallel optical transceivers; single mode or multicore connectors; optical waveguide coupling; optical chip-scale, heterogeneous, and microsystem integration; and 3D photonics; optoelectronic integration for the Internet of Things; high-efficiency LEDs and high-power lasers; and integrated optical sensors. Interested authors are encouraged to submit a 750-word abstract by October 12, 2015. Identify “Optoelectronics” as your primary subcommittee. The 2016 ECTC will be held May 31–June 3, 2016 in Las Vegas, NV USA.

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## Biographies

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# Packaging ICs to survive the automotive environment

By Prasad Dhond [Amkor Technology®]

**E**lectronic systems in cars and trucks represent some of the harshest application conditions for integrated circuits (ICs). The packaging for these ICs must withstand a variety of tests that go well beyond conditions prevalent in consumer, commercial and industrial qualifications.

To survive these tests and operate reliably over their expected lifetime in a variety of vehicles and systems, assembly processes for automotive ICs have several unique aspects to ensure packaging reliability and durability. The extent of unique processing and tests depends upon the vehicle system where the IC is employed.

## Getting electronics into production vehicles

Some electronics in vehicles are obvious, while others are somewhat hidden. The obvious systems include infotainment systems, digital displays, instrument cluster, voice/data communications, back-up warning, adaptive cruise control, advanced driver assistance systems (ADAS), cabin environmental controls, navigation systems, lane departure warning, and others in the passenger compartment.

The hidden vehicle systems include engine control, cylinder deactivation, electric power steering, electronic throttle control, airbag deployment, transmission control, anti-lock brakes, electronic stability systems, and more. Many of these hidden systems are mounted under the hood of the vehicle where the ambient temperature can be 150°C or higher.

## Vehicle electronics growth

Over 50 different electronic systems can be found in today's high-end vehicles that implement the most advanced technologies. In fact, the number of automotive electronic systems is increasing due to government safety mandates and consumer demand for more convenience and comfort features.

In addition to the increasing electronic content, the number of vehicles sold is increasing globally, especially in China and emerging markets. In the last decade, new vehicle sales in China have grown at a rate of almost 12% per year.

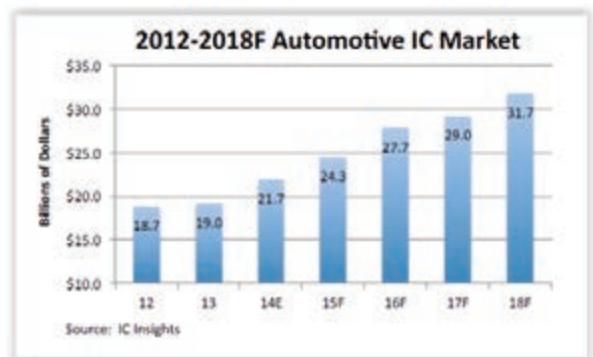
Increasing vehicle sales and higher electronic systems penetration are driving the automotive IC market, which is approximately \$24B in 2015, with a 5-year CAGR of about 9% to 10% (**Figure 1**). Over 70% of the automotive total available market (TAM) is in the area of analog (including linear regulators, power components, DC-DC converters, LED drivers and interface components, such as USB drivers) and microcontrollers (MCUs).

The automotive market is an attractive segment for most semiconductor companies as it provides a more stable application base compared to cyclical mobile or consumer applications, longer product life cycles, and higher returns on investment. However, there are barriers to entry with very high expectations of quality, reliability, handling and processing, all of which must be achieved at reasonable costs. There are also continuously evolving quality and reliability requirements that drive significant capital purchases. Working with the right outsourced semiconductor assembly and test (OSAT) partner can help address many of these challenges effectively.

## AEC-Q100 grades

The Automotive Electronics Council (AEC) has established AEC-Q100, "Failure Mechanism Based Stress Test Qualification for Integrated Circuits" [1], to provide standardized test methodologies for reliable, high-quality electronic components.

Many of the tests in AEC-Q100 are performed by the IC suppliers themselves, but packaging-related tests may be performed by an OSAT as part of the IC qualification. The test requirements vary from "under-the-hood" applications, to passenger compartment, and other vehicle locations.



**Figure 1:** Market experts forecast consistent growth for automotive ICs.  
SOURCE: IC Insights.

AEC-Q100	Ambient Operating Temperature Range
Grade 0	-40°C to +150°C
Grade 1	-40°C to +125°C
Grade 2	-40°C to +105°C
Grade 3	-40°C to +85°C

**Table 1:** AEC-Q100 grades vary based on the operating environment temperature range.

The part operating temperature grades are shown in **Table 1**.

The grades reflect different application profiles from under the hood to inside the cabin mounting locations and apply to IC products including microelectromechanical systems (MEMS) sensors, power devices, signal conditioning, MCUs and more. While Grade 1 is most commonly used in automotive, Grade 0 is for the more stringent applications, while Grades 2 and 3 are more equivalent to commercial qualifications.

## Special considerations for automotive ICs

Semiconductor suppliers are not always aware that a particular IC will end up being used in an automotive application – especially if it's a catalog IC being used in Grade 2 or Grade 3 applications such as after-market infotainment. If an IC is designed explicitly for an automotive application, however, steps must be taken to ensure that it is handled and processed differently than a standard



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- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

#### MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly



commercial or industrial IC. Even a 1ppm component failure rate translates into a 1.5% or 15000ppm failure rate at the car level. To ensure the highest safety standards, we need to have a goal of zero defects.

When a product is identified for automotive use, IC suppliers, especially those familiar with automotive requirements, usually have specific expectations for processing and handling during the assembly process.

## Supplier management

Early in the development process of an automotive IC, one of the major considerations is business continuity planning with respect to raw materials. For instance, there have been major disruptions in the lead frame supply chain with recent accidents and some lead frame suppliers exiting the business. Supplier selection, redundancy, and process audits per automotive standards such as VDA6.3, are very important to ensure continuity and quality of supply for automotive ICs.

## Automotive controls

In addition to ensuring that factories have automotive certifications such as TS16949, automotive products should be subject to tighter controls on the factory floor. Among other things, these controls might include designated automotive equipment (**Figure 2**), specially trained operators, error-proofing systems and hands-free processing systems. Designated automotive lines are usually equipped with higher end models of machines that are maintained at a different standard and subject to tighter  $C_{pk}$  process capability requirements. Certified operators are specially trained to handle automotive devices and have to meet certain minimum requirements to achieve and maintain certification. Process control automation can help ensure that automotive devices are processed only on designated automotive equipment by certified operators.

## Additional process steps

Depending on the application profile, automotive devices could have additional process steps compared to a standard commercial IC to ensure the highest quality and reliability. These typically include more stringent visual inspections during assembly and 100% open-short testing at the end of the assembly process. Some of the other additional process steps could be direct plasma cleaning before wire bonding to ensure a higher quality bond and plasma cleaning before mold.

## Safe launch

Safe launch is a process during the pre-production phase where manufacturers or assemblers inspect the process at each step and verify that the particular step is done correctly before the product moves to the next one. This ensures that any issues with production processes are identified and addressed during the pre-production phase itself, before high-volume production starts. Safe launch is even more important for advanced packages such as flip-chip ball grid array (FCBGA), flip-chip chip-scale package (fcCSP), system-in-package (SiP), etc., which are relatively new to automotive applications. For example, during the assembly process of FCBGA packages, safe launch could include examining cross sections at several different locations after the solder ball attach process to make sure that the metallurgy of the solder joints is robust. Although this represents extra work and time during pre-production runs, the benefit is better quality and a more robust process. It also gives more confidence to both semiconductor suppliers and Tier 1 suppliers about going into production with new technologies.

## AEC-Q100 qualification

AEC-Q100 consists of a suite of tests but only a subset of these tests is directly related to the package and assembly. Some of these are “in process” tests such as wire bond shear (WBS), wire bond pull (WBP), and others that an OSAT can perform. As shown in **Figure 3**, the reliability tests in test group A are the most applicable to an OSAT.

Traditional JEDEC and AEC-Q100 Test group A have various tests including preconditioning, temperature cycling (TC), temperature humidity bias (THB), unbiased highly accelerated stress test (HAST) and

high-temperature storage life (HTSL). **Table 2** shows the differences between the standard JEDEC conditions vs. Grade 0 and Grade 1 automotive reliability test conditions. An OSAT must have reliability labs with capability and equipment to perform these tests.

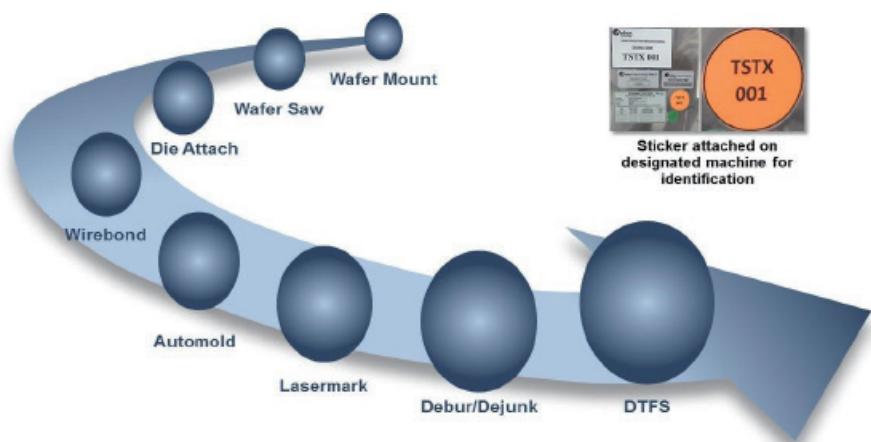
**Figure 4** shows the tests that Amkor typically performs for AEC-Q100 qualifications. Based on equipment availability, or in some cases the equipment’s capability, alternate tests may be acceptable. For example, instead of unbiased HAST, autoclave or temperature humidity (without bias) are acceptable tests. These tests are used to characterize the bill of materials (BOM) for AEC-Q100 Grade 1 and Grade 0 applications. Different package families are evaluated to determine the most robust the most robust bill of materials (BOM) to qualify for Grade 0 and other grades.

## Special BOM considerations

In addition to special processing, automotive applications frequently require special material sets or BOM. For lead frame products, some of the main material considerations are: wire type, epoxy mold compound (EMC), die attach (DA) materials, and lead frame design features.

Lead frames with roughened surfaces are often used to enhance EMC adhesion. Roughened lead frames can be used in combination with unique design features that are etched or stamped onto the lead frame surface to improve delamination performance.

A critical component in being able to achieve aggressive year-on-year cost reductions is to use copper wire on wire bond products. Traditionally, gold has been the wire of choice, but due to cost and high-temperature performance where Kirkendall voiding is observed between the gold and aluminum interface, most new wire bonded automotive devices are using copper wire. Most major



**Figure 2:** Typical wire bond assembly process steps and special identification label for designated automotive equipment.

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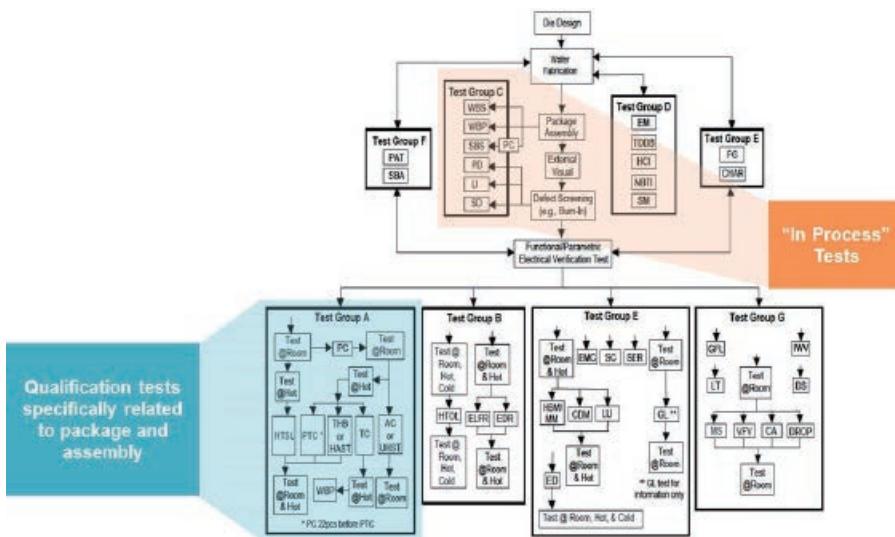
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**Figure 3:** AEC-Q100 qualification test flow [1].

Stress	Standard JEDEC Conditions	AEC-Q100 Grade 0	AEC-Q100 Grade 1
Pre-conditioning	MSL 1: 85°C/85% RH for 168 hours, unlimited floor life MSL 2: 85°C/60% RH for 168 hours, 1 year floor life MSL 2a: 30°C/60% RH for 696 hours, 4 weeks floor life MSL 3: 30°C/60% RH for 192 hours, 1 week floor life	Min Level 3, per J-STD-020	Min Level 3, per J-STD-020
Temperature Cycling	Condition A: -55°C to 85°C Condition B: -55°C to 125°C Condition C: -65°C to 150°C	-55°C to 150°C for 2000 cycles -65°C to 150°C for 500 cycles	-55°C to 150°C for 1000 cycles -65°C to 150°C for 500 cycles
Temperature Humidity Bias	THB: 85°C/85% RH for 1000 hours	Pre-condition before THB: 85°C/85% RH for 1000 hours	
Unbiased HAST	Unbiased HAST: 130°C/85% RH for 96 hours, or 110°C/85% RH for 264 hours	Pre-condition before Unbiased HAST: 130°C/85% RH for 96 hours, or 110°C/85% RH for 264 hours	
High Temp Storage Life	Condition A: +125°C Condition B: +150°C Condition C: +175°C	175°C for 1000 hours or 150°C for 2000 hours	150°C for 1000 hours or 175°C for 500 hours

**Table 2:** AEC-Q100 qualification tests within an OSAT company's scope.

IC suppliers are either already qualified, or are in the process of qualifying copper wire for automotive applications. Lead frame, chip-scale package (CSP) and ball grid array (BGA) packages are in volume production for infotainment and engine control applications, and there is also increasing acceptance in other applications such as powertrain and chassis. Safety applications, however, have been slower to adopt the use of copper wire.

The use of copper wire is not without its own set of challenges. Apart from the usual workability challenges of Cu wire, recent industry testing [2] has raised some concerns related to Pd coated copper (PCC) bond wire for very stringent automotive applications. In these studies, HTSL testing performed at above 150°C showed degradation of bond

pull test (BPT) results seen over time, as well as cracks at the stitch bond area. While PCC wire passes the AEC-Q100 Grade 0 min levels, there are some concerns regarding the margin in very stringent applications where the IC must operate at temperatures over 150°C for extended periods of time.

Further evaluations are necessary to validate the findings of the above-mentioned study and determine the right material set to achieve robust performance for AEC-Q100 Grade 0 and beyond. Amkor has ongoing evaluations to determine appropriate BOMs for various products. The evaluation matrix for lead frame products consists of variations of wire type, EMC and lead frame design features. The primary goal of these evaluations is to develop a BOM recommendation for

AEC-Q100 Grade 0, with secondary goals of extended testing beyond the Grade 0 limits, to achieve zero delamination and meet other stringent automotive criteria.

Some of the Amkor package families that are popular in automotive electronic systems include: SOIC, TSSOP, MLF®/QFN, TQFP, BGA, Stacked CSP, fcCSP, FCBGA and TMV®. Dual lead frame products such as SOICs and TSSOPs represent the highest volume. Quad lead frame packages, as well as BGAs, are popular for automotive MCUs. The increasing use of non-wire bond products such as CSP and through-mold via (TMV®) is occurring in infotainment and ADAS systems.

## Evolving automotive packaging requirements

Increasing innovation in ADAS and infotainment is bringing advanced technologies to the automotive space at a much faster rate than ever before. Growing familiarity with smartphone technology is increasing consumer expectations in the car. Consumers now expect their car to seamlessly talk to their phones, and they want to be able to run the same apps that they are used to running on their phones, in their cars. New safety systems in the cars are slowly transitioning from driver assistance to highly automated, on their way to becoming autonomous. Autonomous operation requires automotive systems to continuously monitor the surroundings and take preventive actions in case an incident happens. In such a system, there are several sensors that feed real time data to a processor, where several algorithms are running and the processor feeds the results to actuators. Since these systems require real time processing, it is critical that the response time be as fast as possible. As a result, systems designers choose either SiP or fcCSP type of packaging to keep the processor and memory as close as possible to each other.

## Assembly solutions for automotive IC packages

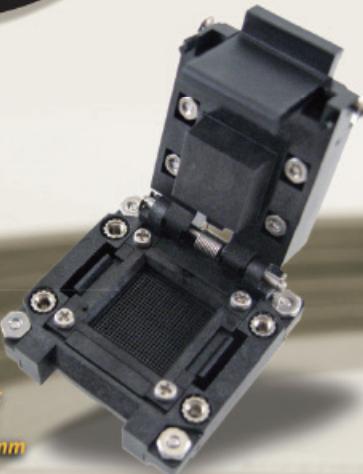
ICs provide the foundation for the technology inside the automotive electronic systems that deliver control features, convenience, connectivity and keep passengers safe and comfortable. To achieve the reliability that automakers demand, IC suppliers must approach IC packaging with considerably different packaging techniques. These include additional controls on the manufacturing floor, additional process steps during assembly, and using the right material set that has been proven to survive automotive reliability tests.

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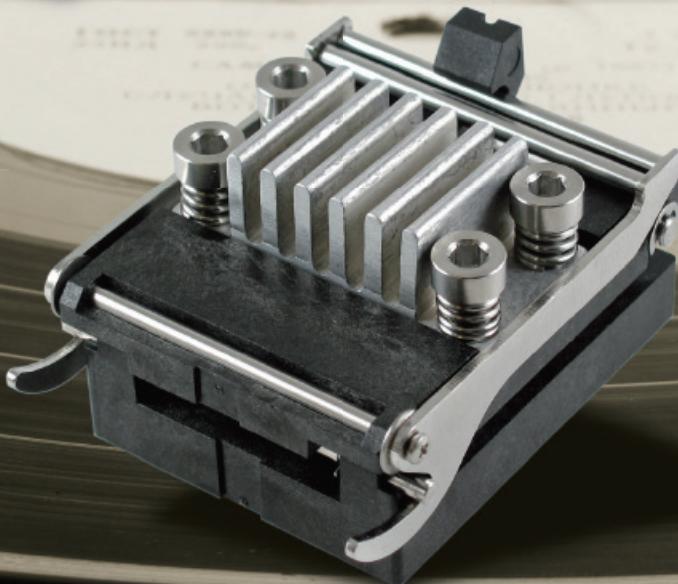
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Pin Count:  
1521 max - 0.80mm  
961 max - 1.00mm

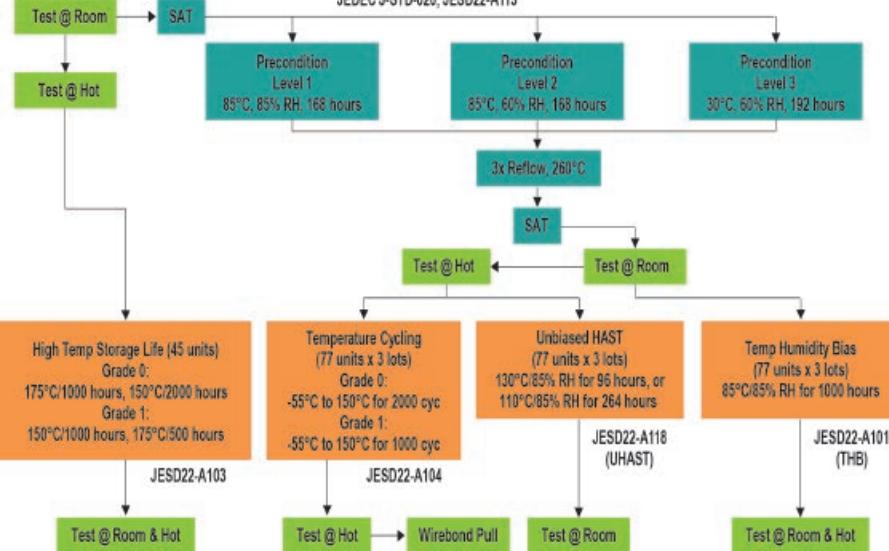


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**Figure 4:** AEC-Q100 Group A tests performed by Amkor Technology®.

As an OSAT supplier with many years of automotive experience, Amkor Technology® has extensive understanding of the requirements of automotive OEMs and Tier 1 suppliers and can provide guidance and direction in assembling automotive products,

especially to customers with limited automotive experience. Our joint venture with J-Devices is expected to expand and provide even greater assembly and test capabilities for automotive customers, as well as access to the Japanese automotive market.

Evolving packaging technologies from lead to surface mount to MEMS, 3D and die-level packaging will continue to place even more stringent demands on IC packages in automotive applications. Working with a seasoned expert OSAT can mean the difference between survival and failure in automotive applications.

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## Biography

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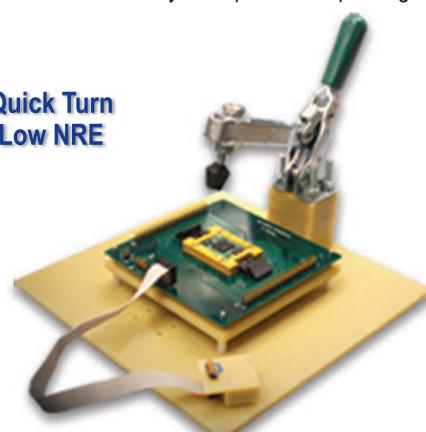
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# Out of this world electronics packaging

By Andrew A. Shapiro [Jet Propulsion Laboratory, California Institute of Technology]

**E**lectronics packaging for space exploration challenges conventional strategies and materials. Venus exploration will encounter extreme high temperatures and pressures with a highly corrosive atmosphere. There is a vast array of environments for operations on frozen worlds, some with no atmosphere, such as Europa, or others, such as Titan, with a cold methane atmosphere and methane lakes. The surface of Mars can have extreme cycles daily. Deep space measurements of the origin of the universe can require electronics measuring less than 1mK. Traditional strategies have often used warm electronics boxes to minimize electronics temperature excursions, however, with the growth of small spacecraft and of nano- or micro-robotic systems, the power budgets for many future NASA mission concepts cannot support warming of the spacecraft electronics. Additionally, surface exploration of icy ocean worlds, such as Enceladus or Ganymede, where power availability may be extremely limited, electronics need to be designed and packaged to operate at or near these extremes.

The electronics and packaging strategies for each of the exploration opportunities listed above can be substantially different from those for terrestrial applications, and can be substantially different from each other. In this article, we will explore a few examples of packaging for environmental extremes. We will look at the systems developed for Venus high-temperature operations, issues facing icy ocean worlds, Martian electronics extreme cycling, and other deep space exploration targets. Images of some of these extreme environments may be seen in **Figure 1**.

## Environments

In this paper, we present some of the environmental extremes encountered in planetary exploration. This is followed by a description of some of the failure modes encountered and a review of generic packaging approaches for working with these extreme applications. Finally, we will provide several specific examples.

The range of packaging challenges for the extremes of planetary and deep space

exploration may be categorized into three primary environments. Extremely hot environments, extremely cold environments, and extreme thermal cycling. These can most easily be understood in terms of specific exploration targets being considered by NASA as recommended by the decadal survey from the National Academy of Sciences [2].

For an extreme hot environment, we can consider the case of Venus exploration. The Venus environment is about 740K at approximately 91 bars. The atmosphere is approximately 95% supercritical CO<sub>2</sub> with the remainder primarily nitrogen with an atmosphere profile containing significant amounts of SO<sub>2</sub> and H<sub>2</sub>SO<sub>4</sub> [3].

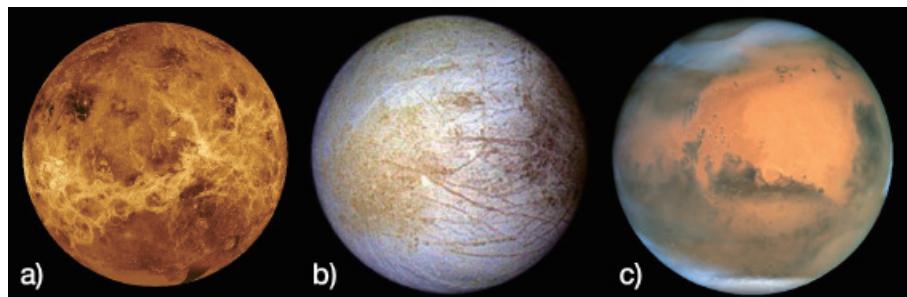
By contrast, several icy ocean world environments are at extremely low temperatures. The Jovian moon Europa has an average temperature of about 100K with essentially no atmosphere and is made primarily of ice [4]. With no atmosphere, the primary method of heat exchange is radiation. Saturn's Titan has an average temperature of approximately 95K and an atmosphere at approximately 1.5 bars of N<sub>2</sub> and approximately 5% CH<sub>4</sub> with the surface of the moon partially covered with hydrocarbon lakes [5]. Similar missions are being contemplated for Ganymede (110K) [6], Enceladus [7] (75K), and Ceres (130-200K) [8].

The third extreme is alternating hot and cold cycles. Mars can cycle between 120K and 293K (a 173K temperature swing) at its surface. Although the Martian daily (24hrs 37 min) cycle temperature swings may be a bit less (186K to 273K, only an 87K swing), electronics exposed

to these environments will need to survive the surface temperature extremes [9]. If a mission is to last five to ten years, it would mean thousands of these extreme cycles.

The traditional approach to extreme environments for spacecraft is to create a local environment around the electronics to have them operate in known temperature regimes. For Mars or Europa this would mean a 'warm' box. Typically, a warm box is one that would keep electronics operating at temperatures where performance of most components have been characterized, generally above the MIL-STD-883 thermal cycling temperature of 218K (-55°C) [10]. Unfortunately, this strategy is power intensive and may result in a significant mass penalty. With certain types of missions using radioisotope power or adequate solar power, this strategy may be the most appropriate. However, as spacecraft get smaller, radioisotope power systems could become a higher percentage of mass and volume with limited potential to scale down. In addition, ocean worlds, such as Europa, are farther from the sun, where solar power could be insufficient. Additionally, even when a 'warm' box is present, it may be for certain electronics, such as sensors, motor controllers, cameras, etc., to reside outside the 'warm' box. The technology then changes to one that is capable of operating in these extreme environments.

Similar arguments may be made for a 'cold' box, which may still be extremely warm, for the exploration of Venus. Typically, the lifetime at the upper operating temperature of the electronics and power would limit the mission lifetime.



**Figure 1:** Images of some of the planetary extreme environments: a) Venus (740K) left, b) Europa (100K) center, and c) Mars (120-293K) right (not to scale) [1].

## Failure modes

In consideration of the performance of the electronics at these extreme temperatures, we have to parse the assemblies into different technologies and assess them. One way to parse the system is into: active devices; passive devices, interconnects, and assembly materials.

Active devices, for example, can include integrated circuits in silicon, III-IV and II-VI devices. Performance at cold temperatures can be substantially different. Clocks can run at different speeds, carriers can freeze out, and mobilities can be substantially different. Space or planetary radiation may have effects on the performance of some devices. At high temperatures, lifetimes of devices can become an issue. Wider band gap materials, such as SiC or  $C_{\text{dia}}$ , may function more effectively.

Passive devices, including integrated passives, can also have substantial changes in performance. The polarization mechanisms used to store charge in capacitors may not be active, thermal coefficients of capacitance (TCCs), and thermal coefficients of resistance (TCRs), can become nonlinear, and in many cases are unknown at the extreme hot or cold temperatures. Magnetic properties for inductor and transformer materials can go below the Curie temperature, or can be excessively noisy at higher temperatures.

Interconnects can also be challenging. In cold environments, Sn-based solders can have issues because Sn undergoes two transitions at cold temperatures. It undergoes an allotropic phase transition at 286.2K—undergoing a  $\text{Sn}_{\beta} \rightarrow \text{Sn}_{\alpha}$  transformation. This transformation includes a 27% volume increase, so in addition to having a new structure, the mechanical integrity is disrupted by catastrophic rupture. This transformation is known to have very slow kinetics, so the transition may occur years after being exposed to temperatures below the transition. Interestingly, Cu can accelerate the transition to occur in just a few hours. With Cu being present in most interconnect systems containing Sn-based solders, the presence of Cu could become a serious issue even with Ni barrier layers [11].

Additionally, if the transition described above is avoided, Sn, and many Sn alloys, will also undergo a ductile to brittle transition (DTBT) at about 150K [12]. This DTBT substantially lowers the mechanical integrity of the Sn and would be likely to cause catastrophic failure of the electronics assemblies if standard techniques are used.

Other common failure modes found in standard electronics assemblies involved cyclic fatigue of Au wire bonds, Sn-based solder joints, and Cu vias in polyimide printed wiring boards. Polymers can fail through brittle fracture in cold environments. In hot environments, thermoplastic polymers soften and in thermoset polymers sublimation, or even burning can be an issue. In both cold and hot environments,

polymers suffer from adhesion loss. Hot environments, can also offer challenges for metals. Diffusion and electromigration are accelerated. Most traditional solders will melt well below the Venus ambient temperature, and many other metal interconnects suffer from changes in properties or crystal structure because of diffusion or creep, which are accelerated at higher temperatures [13].

## Approach

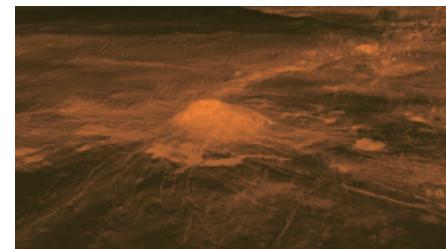
The general strategy for electronics in extreme environmental conditions is to first determine which items need to be maintained inside the spacecraft, and which items need to be exposed to and can operate in the extreme environments. With the current emphasis on smaller, cheaper missions, this balance is changing with more of the electronics being exposed to the extreme environments as the power and mass required to maintain a more benign environment is not available.

The process for evaluation may be thought of in the following sequence: 1) First, review power and mass budgets, select components and interconnects requiring extreme exposure; 2) Next, review the list of materials and components requiring exposure for compatibility with the environment to determine which ones can perform suitably in the environment and which ones require further study; 3) At this point, many of the materials systems for interconnects cannot perform as needed and new materials sets need to be developed taking into consideration minimization of stress and maximizing component and system performance. Also, performance data and even physics-based models of materials and components are often not available at the extremes such as 90K or 740K. New materials sets need to be selected with regard to fundamental physics, and then the selections need to be validated to obtain and to verify cold/hot performance data both individually, and as a system. A few examples are provided in the next section.

## Materials selection for extreme environments

Three examples are reviewed for how materials systems were evaluated for selection to perform in extreme environments.

**Venus electronics.** The Venus environment creates a completely different set of challenges from those faced by most packaging engineers. An image of the Venus environment may be seen in **Figure 2**. The focus of the packaging for Venus surface mission concepts was to construct a small-scale electronic sensing system and transmitter that could function in the 740K, 91 bar ambient. This solution took somewhat more creativity because the



**Figure 2:** The Venus environment (740K) [1].



**Figure 3:** A multiplexer designed for and successfully operated in a simulated Venus environment [14].

standard Si semiconductors cannot function at this temperature. The solution involved not only a new integrated circuit approach using SiC, but a new packaging scheme was needed. Packaging traditionally depends on widespread use of polymers for things like die attach, printed wiring boards, solder masks and conformal coatings. Most of these burn or melt well below the 740K environment of Venus. Traditional solders will also melt well below this temperature. Thick-film circuit interconnects were used with high-temperature solders for demonstration of a combined multiplexer-amplifier circuit that operates at 773K (shown in **Figure 3**) [14]. Alternative approaches included miniaturized vacuum tubes, which have high survivability because of their larger feature size.

**Icy ocean worlds.** Another extreme environment example is the extreme cold of icy ocean worlds such as Titan or Europa. The ice formations on Europa at 90K may be seen in **Figure 5**. There is speculation that a water ocean exists 10km below the surface ice [6]. In order to perform sample measurements, or to have external cameras, some of the electronics would need to be in the ambient environment. The traditional heating of electronics is limited because the solar radiation is too small to make use of photovoltaic cells, and batteries do not perform well in these extreme cold environments. At cold temperatures, there are some issues with CMOS semiconductors including excessive hot carriers and possible device degradation, however, with clever device design, the effects can be mitigated using SiGe technology [15]. Additional issues in the interconnect with traditional Sn-based solders also must be addressed. Careful study reveals that alloying with In nearly eliminates



Figure 4: The Europa surface [1].

this transition [11]. Intelligent design of the DTB circuits can be used to accommodate degradation in performance of passive devices as they go cold.

Even though many of the parametric and catastrophic failure mechanisms are present in the extreme cold operating environment, many materials and device performance properties are completely unknown at 100K. Therefore, a significant test program has to be implemented for both materials properties and device characterization (both active and passive) at the temperature extremes anticipated for the proposed mission.

**Martian electronics and extreme temperature cycling.** In order for a rover to survive several years at various places on the planet Mars, it would need to survive the coldest and warmest conditions on the planet. An image of the rover on Mars may be seen in Figure 4 [16]. Additionally, some of the electronics could be located on one of the drive motors that would heat it to even higher temperatures than the highest ambient. The specifications passed down for these assemblies to meet was 1,500 cycles from 153K to 358K—a 205K temperature swing.

For a variety of reasons, including historical failures, thermal expansion mismatch and materials compliance, a wire bond, chip-on-board approach was selected. Probable failure modes were identified as via failures, wire bond failures, die attach failures, die fracture and encapsulant failures. An extensive statistical design-of-experiments (DoE) was performed with a variety of materials that had a high probability of survival. After a theoretical analysis [17, 18], combinations of substrate materials, encapsulant materials and die attach materials were subjected to an excess of 1,800 extreme temperature cycles [19]. Most of the anticipated failure modes were observed, including via failure, wire bond necking, and wire bond fracture at theoretically predicted locations. Despite the many anticipated failures, many combinations of substrate, die attach and encapsulant materials survived. The most promising of the combinations that were successful included low-temperature co-

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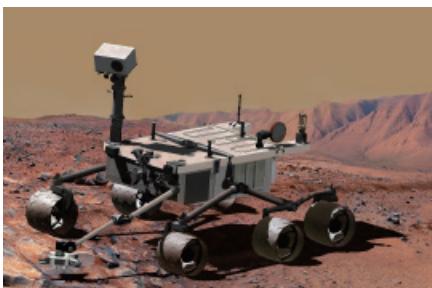


Figure 5: The Mars Science Lander (artist's concept) [16].

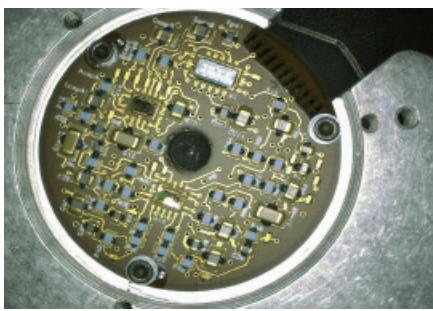


Figure 6: Chip-on-board motor driver assembly developed for the extreme temperature cycling of Mars [20].

fired ceramic (LTCC) substrates, epoxy die-attach and Parylene encapsulant, although  $\text{Al}_2\text{O}_3$  and polyimide substrates also worked

with certain combinations. Assemblies with these combinations were tested through more than 1,800 extreme temperature cycles while continuously operating, demonstrating excellent performance for an extended Mars mission with the packaged electronics exposed to the extreme ambient. Figure 6 shows an example of an assembly for a motor driver designed for Mars rovers that survives these extreme cycles [20].

### Summary

The task of packaging electronics for planetary exploration can experience challenges far beyond those typically encountered in commercial electronics. Understanding the fundamental materials properties and physics-of-failure are absolute necessities for mission success. This understanding is needed to inform the design, build, test and verification of electronics sub-systems. Because most of the materials properties and performance of devices are not well known in many of these extreme environments, significant testing at the environmental extremes needs to be performed in order to obtain the required knowledge to support the design of extreme-survivable electronics systems.

### Acknowledgements

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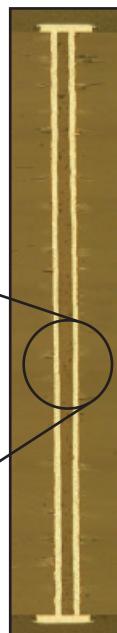
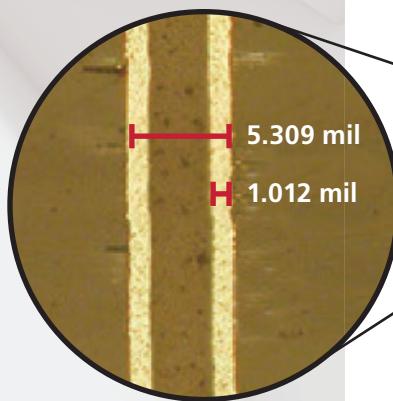
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## Biography

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# Thermocompression bonding for flip-chip technology

By John H. Lau, Li Ming, Nelson Fan, Ringo Tse [ASM Pacific Technology Ltd.]

**F**lip-chip technology has been used extensively for the processors of mainframe computers, servers, personal computers, notebooks, smartphones, tablets, games, etc., the application-specific integrated circuits (ASICs) of networking, telecommunications, etc., and the memories of data storage devices, etc. Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs, and memories increases and their pitch (or the spacing between the pin-out pads) decreases. Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and lower profile package substrates lead to the necessity of the thermocompression bonding (TCB) method for flip-chip assemblies. In this study, various TCB techniques are investigated and a new process is proposed.

## Wafer bumping

Flip-chip technology was introduced by IBM in the 1960s [1, 2], and solder bumps are its most important element. There are many ways to perform the wafer bumping (at least 12 are shown in [3]), and the most common method is by electroplating (as shown in **Figure 1**).

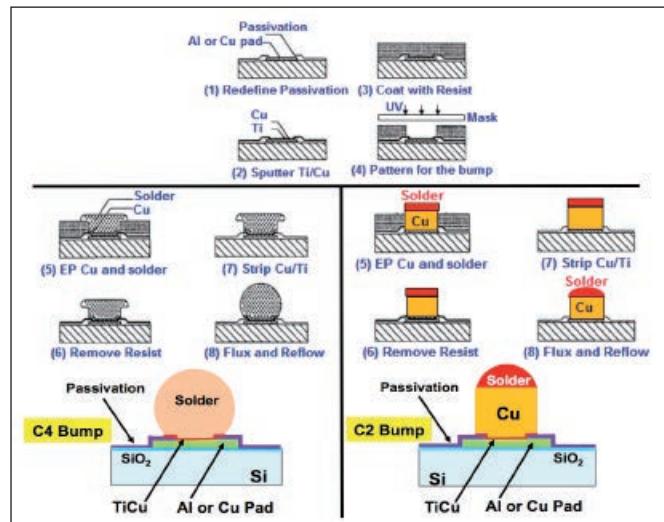
## C4 bumps

Usually the pad size is equal to 100 $\mu\text{m}$  and the target bump height is equal to 100 $\mu\text{m}$ . After redefining the passivation opening (usually it is not required), either Ti or TiW (0.1 to 0.2 $\mu\text{m}$ ) are sputtered over the entire surface of the wafer first, followed by 0.3 to 0.8 $\mu\text{m}$  of Cu. Ti-Cu and TiW-Cu are called under bump metallurgy (UBM). In order to obtain 100 $\mu\text{m}$  bump height, a 40 $\mu\text{m}$  layer of resist is then overlaid on the Ti-

Cu or TiW-Cu and a solder bump mask is used to define (UV exposure) the bump pattern as shown in steps #1-4 in **Figure 1**. The opening in the resist is 7 to 10 $\mu\text{m}$  wider than the pad opening in the passivation layer. A 5 $\mu\text{m}$  layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target (100 $\mu\text{m}$ ), the solder is plated over the resist coating by about 15 $\mu\text{m}$  to form a mushroom shape. The resist is then stripped off and the Ti-Cu or TiW-Cu is removed with a hydrogen peroxide or plasma etching. The wafer is then reflowed with flux, which creates smooth truncated spherical solder C4 (controlled collapsed chip connection) bumps due to surface tension as shown in steps #5 through #8 on the left-hand side of **Figure 1**.

## C2 (Cu-pillar with solder cap bumps)

Because of higher pin-count and tighter pitch (very small spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [4] and Cu-pillar with solder cap [5-7] as shown on the right-hand side of **Figure 1** can be a solution. The fabrication process is basically the same as that of the C4 bumps except electroplating the Cu instead of solder as shown in step #5 on the right-hand side of **Figure 1**. It is followed by electroplating the solder cap



**Figure 1:** Electroplating wafer bumping process for a) C4 bumps (left) and b) C2 (Cu-pillar with solder cap) bumps (right).

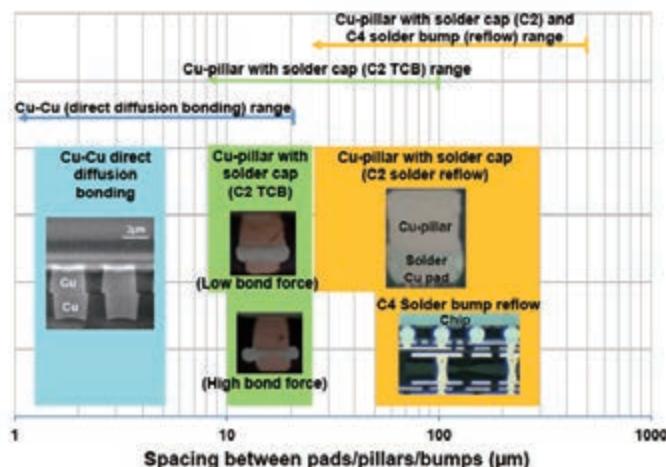
and then reflowing the solder with flux. Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump.

## Flip-chip assembly

**Figure 2** shows some methods of flip-chip assembly and their range (spacing between pads/pillars/bumps) of applications. Basically, there are two groups: one is with an intermediate layer between the bonding pads/traces, and the other is not, i.e., nothing! Flip-chip assembly with intermediate layers such as solder mass reflow and solder by TCB are called indirect bonding. Cu-to-Cu diffusion bonding, which does not have anything between the bonding pads/traces on the chip/wafer is, therefore, called direct bonding.

## Cu-to-Cu TCB direct bonding

Cu-to-Cu diffusion bonding can go down to ultra-fine pitch and pad size (the spacing between pads is 5 $\mu\text{m}$  or



**Figure 2:** Various flip-chip assembly processes vs. spacing between pads/pillars/bumps.

less); sometimes it is even used for larger spacing between pads at 20 $\mu\text{m}$ . In order to reduce the tendency to form native oxides that strongly affect the bonding reliability, Cu-to-Cu is a TCB and usually operates at high temperature (~400°C) and pressure and long process time (60-120 minutes), which are not good for throughput and the device reliability. On the other hand, Cu-to-Cu bonding at room temperature leads to the highest throughput and the least amount of device reliability concerns, as well as very low costs. However, the drawbacks of room temperature bonding are the stringent requirements on: 1) pad/trace/wafer planarization, 2) surface treatment to ensure smooth hydrophilic surfaces for high quality bonding, and 3) the class of clean room is very high. Cu-to-Cu TCB is mainly for wafer-to-wafer (W2W), chip-to-wafer (C2W), and chip-to-chip (C2C) assembly processes.

#### C4 solder reflow

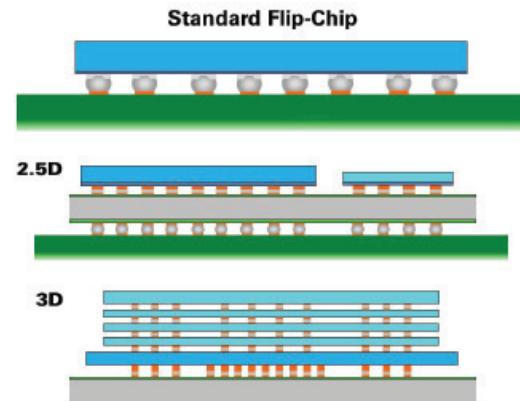
Solder mass reflow has been using for flip-chip assembly for almost 50 years. Most of the solder C4 bumps are mass reflowed on either silicon, ceramic or organic substrates. The assembly process is very simple: 1) Use a look-up and look-down camera to identify the location of the bumps on the chip and the pads on the substrate; 2) Apply flux on either the C4 bumps, or the substrate, or both; 3) Pick and place the C4 bumped chips on the substrate, then mass reflow. Because of the surface tension of the C4 solder bumps during reflow, the process is very robust (self-alignment). The spacing between the bumps on the solder mass reflow of C4 bumped chips can be as small as 50 $\mu\text{m}$  as shown in **Figure 2**.

#### C2 solder reflow

In the past few years, solder mass reflow of C2 (Cu-pillar with solder cap) bumped chips on either silicon, ceramic or organic package substrates has been very popular for high pin-count and fine-pitch flip-chip assembly. The assembly process is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same. The spacing between the pillars on the solder mass reflow of C2 bumped chips can be as small as 25 $\mu\text{m}$  as shown in **Figure 2**.

ASM's high productivity (9,000 UPH) with individual dual flip-chip bonding system AD9212 [8] is specifically designed for solder mass reflow of C4 and C2 bumped chips. The placement accuracy in the xy-direction is  $\pm 5\mu\text{m}$  @ 3 $\sigma$  and die rotation is  $\pm 0.03^\circ$  @ 3 $\sigma$ . The wafer

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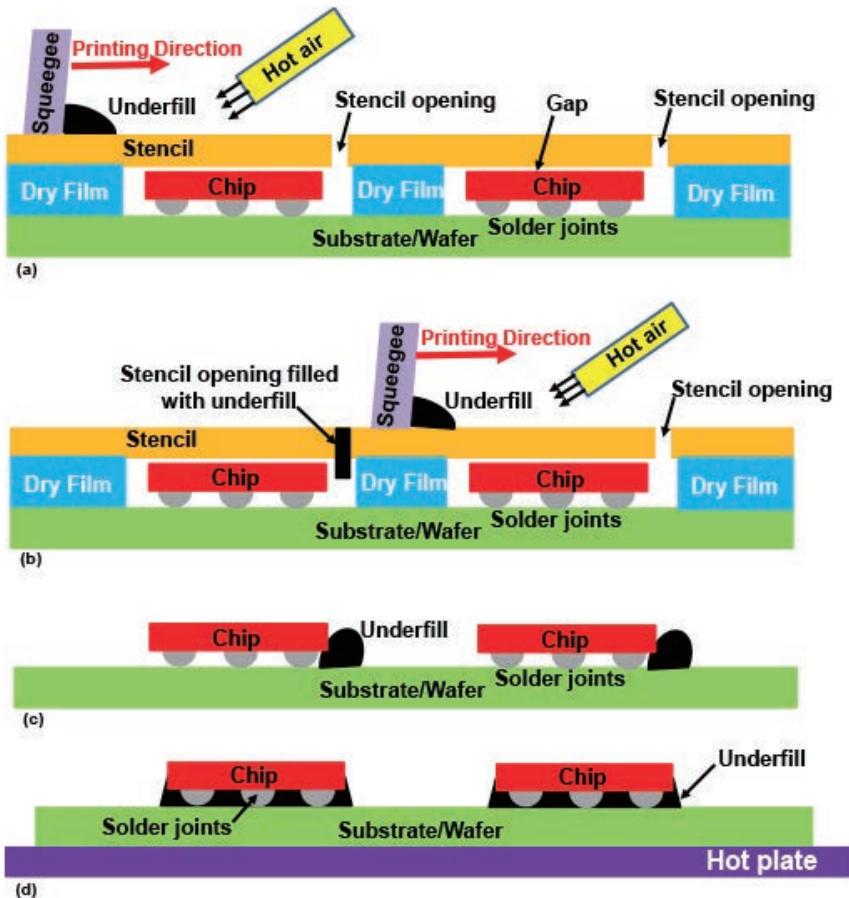


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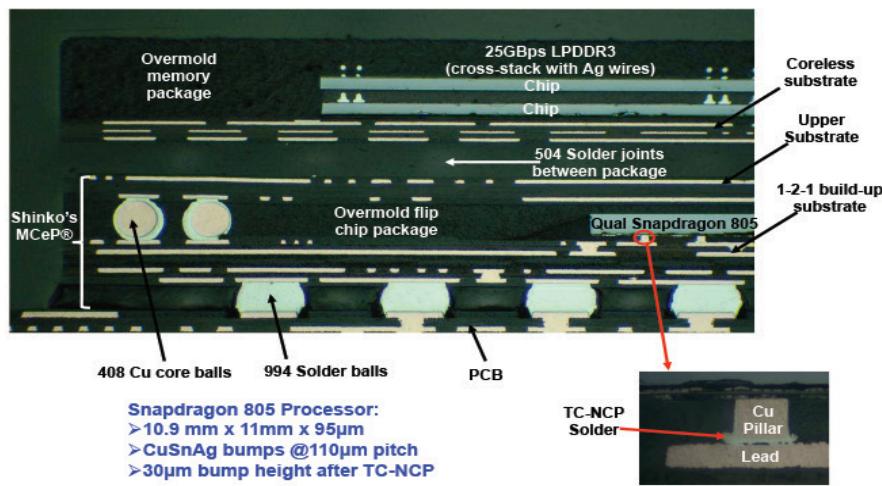
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**Figure 3:** Stencil printing of underfill for flip chips on an organic-panel assembly: a) Before printing; b) During printing; c) After printing; and d) After capillary action (hot air optional).



**Figure 4:** Cross-section image of Qualcomm's SNAPDRAGON 805 processor manufactured using high-force TCB of a C2 bumped chip on substrate with NCP.

handling capability is up to 300mm and the chip size range is up to 30mm x 30mm. It supports a flux dipping flip-chip process and is convertible between flip-chip and die attach processes.

### C2 TCB indirect bonding

In the past few years, TCB of chips with an intermediate layer such as C2 (Cu-pillar with solder cap) bumps on silicon, ceramic or organic package substrates, has been

attracting attentions for high-density and ultra-fine pitch flip-chip assembly. Basically, there are two methods, one is with low bonding force and the other is with high bonding force. For the one with low bonding force, the assembly process is simple: 1) First, use the look-up and look-down camera to locate the position of the C2 bumps on the chip and their corresponding pads on the substrate; 2) Apply flux on the solder cap or on the substrate or both; 3) Pick-and-place the chip on the substrate and then apply temperature to melt the solder and a low force to hold the chip at a certain distance from the substrate. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C2 solder mass reflow process. The spacing between the pillars on the C2 chip by TCB with a low bonding force can be as small as 8 $\mu$ m.

ASM specifically designed a TCB bonder with a low bonding force for use with C2 bumped chips on a package substrate; it has been used for high-volume manufacturing by Intel [9] for thin chips and thin substrates. The process is very simple. First, the thin substrate is pre-applied flux and held flat on the hot pedestal under vacuum. The thin chip is picked up by the bond head, held securely flat, with vacuum. After the chip is aligned with the substrate, the bond head comes down and stops when the Cu pillar of the chip touches the pad of the substrate. A constant force is then applied while the chip is quickly heated beyond the solidus temperature. As soon as the solder melts, the chip is moved further down to ensure good contact. After a certain bonding time, the heater and the solder joints are cooled rapidly below the solidus temperature. The inert environment is less than 100ppm oxygen around the bond head and nozzle, thereby protecting the Cu from oxidation during heat up. The process time is 4 seconds and below, so the UPH (units per hour) is 900 or more [9].

For TCB with a high-bonding force on the C2 chip, the assembly process must be combined with the nonconductive paste (NCP) or film (NCF) underfill, which will be discussed in the next section.

## Underfills

In 1987, Hitachi showed that with underfill, the thermal fatigue life of the flip-chip solder joints on ceramic substrate increased [10]. Five years later, IBM at Yasu proposed the use of a low-cost organic substrate instead of the high-cost ceramic substrate for flip-chip assemblies [11]. They showed that with underfill, the large thermal expansion mismatch between the silicon chip ( $2.5 \times 10^{-6}/^{\circ}\text{C}$ ) and the organic substrate ( $15-18 \times 10^{-6}/^{\circ}\text{C}$ ) is reduced substantially, and the solder joints are reliable for most applications. This opened up the doors for today's very popular solder bumped flip-chip on low-cost organic substrate packages used, for example, in the processors of personal computers, notebooks, smartphones, tablets, etc. Basically, there are two different procedures to apply the underfill, namely pre-assembly underfill, and post-assembly underfill.

## Post-assembly underfill

For post-assembly underfill, the application of underfill is after the flip-chip assembly process, i.e., the flip chip is already on the substrate and the solder joints are already reflowed (either with C2 or C4 bumps) or low-force thermocompression bonded with C2 bumps.

For post-assembly underfill, there are basically two methods, namely capillary underfill (CUF) [11, 12] and molded underfill (MUF) [13]. For CUF, the underfill is dispensed by a needle or jet without vacuum assist on one (or two) side(s) of the flip-chip on the substrate assembly. Because of capillary action, this underfill completely fills the space

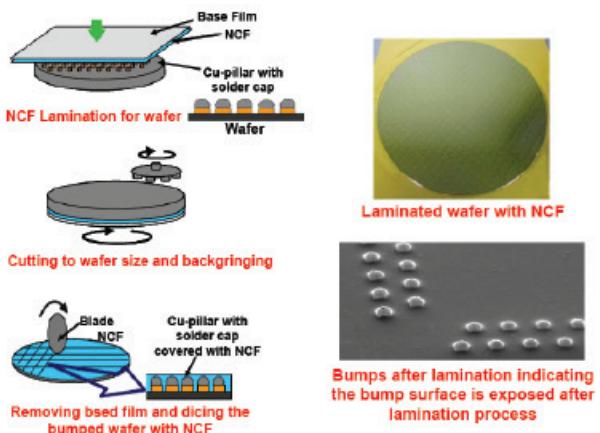


Figure 5: Examples of a C2 (Cu-pillar with solder cap) bumped wafer with laminated NCF: a) (left) By Hitachi; and b) (right) by DOW.

between the chips, solder joints and substrates. The chip and the substrate are then firmly bonded by curing the underfill. CUF is performed one chip assembly at a time, so throughput is an issue.

MUF was first proposed by Cookson Electronics [13] in 2000. For MUF, the modified epoxy molding

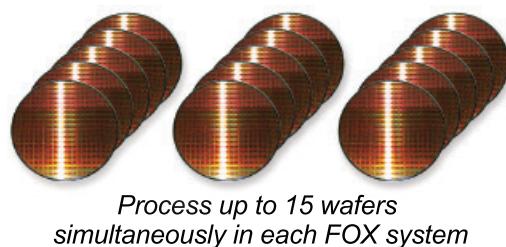
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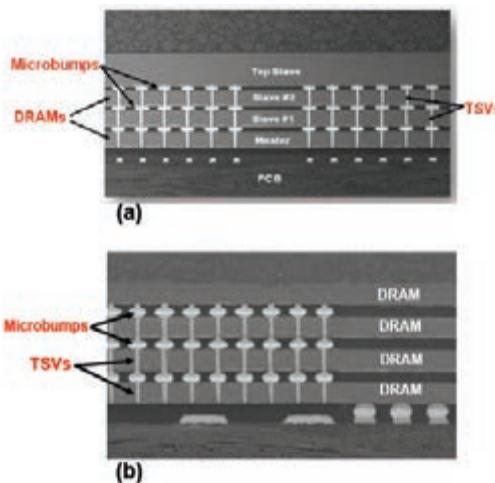
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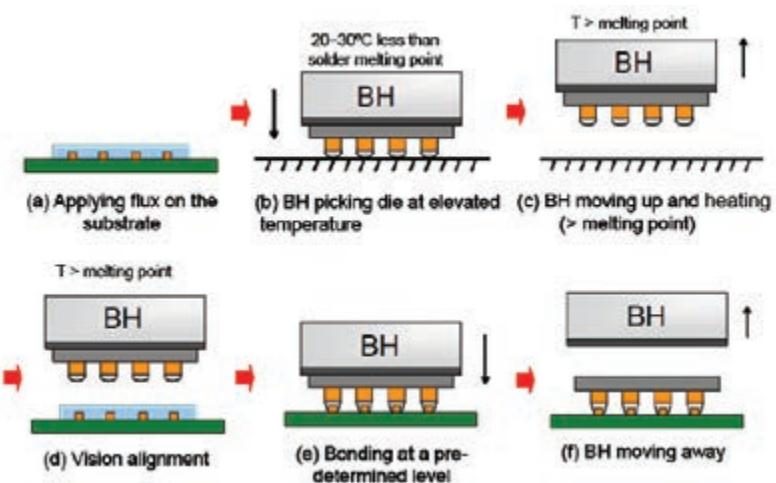


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**Figure 6:** a) (upper image) Samsung's TSV-based DDR4 DRAM; b) (lower) Hynix's HBM of AMD's GPU code-named Fiji.

compound (EMC) is transferred over molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip-chip assembly. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are:



**Figure 7:** ASM's LPC TCB process (IN-press™) flow.

a) the flow of MUF between the chip and the substrate is usually assisted by vacuum; b) the size of the silica filler of the EMC must be very small for flowability; c) the cost of EMC for MUF is much higher than that for package molding; d) package warpage is an issue because of the thermal expansion mismatch among the EMC, chip, and substrate; e) the molding temperature is limited by the melting point of the solder joints; and f) the standoff height and pitch of the solder joints cannot be too small.

In order to increase the throughput of CUF and avoid the drawbacks of MUF, a method of post-assembly underfill has been proposed by [14], where a stencil is designed for printing the underfill material for flip chips on organic panel and Si-wafer assemblies as shown in **Figure 3**. It can be

seen that: 1) a very small rectangular opening of the stencil is designed for each chip and it is located on one edge of the chip; 2) the stencil has a dry film underneath with many rectangular openings (one for each chip) and the size is a little larger than the chip size; 3) there is a gap between the stencil and the backside of the chips; and 4) there is a fixture to apply heat to the stencil and underfill to lower the underfill's viscosity. During printing (**Figure 3b**), the underfill will fill the opening of the stencil and fall into the space between one edge of the chip and the dry film. After printing (usually it only takes a few seconds), remove the assembly (**Figure 3c**) from the stencil printer and place it on a hot plate (~120°C) for the underfill to flow between the chip, solder joints, and the substrate by capillary action (**Figure 3d**). Finally, cure the underfill.

### Pre-assembly underfill

For pre-assembly underfill, the application of underfill is either on the substrate or wafer and is before the flip-chip assembly. Solder reflow of the C4 bumps with underfill on substrates was first proposed by GIT [15] and is called no-flow underfill (NUF). High-bonding force TCB of the C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate was first studied by Amkor [16] and has been used to assemble Qualcomm's SNAPDRAGON 805 processor for Samsung's Galaxy Note 4 as shown in **Figure 4**. The NUF and NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

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By learning from the chip-on-glass (COG) technology, high-bonding force TCB of C2 bumps with nonconductive film (TC-NCF) underfill on wafers have been studied by, e.g., Sanyo [17], Hitachi [18, 19], Tohoku [20, 21], DOW [22], Hynix [23], KAIST/Samsung [24, 25], and Amkor/Qualcomm [26] for 2.5D/3D IC integration. **Figure 5** shows a couple of examples of the lamination of NCF on the Cu-pillar with a solder cap bumped wafer. High-bonding force TCB of the C2 bumps with NCF on wafers (after dicing into individual chips) has been in production for 3D IC integration by Samsung on its TSV (through-silicon via)-based DDR4 (double data rate type 4) DRAM (dynamic random access memory) as shown in **Figure 6a**, and by Hynix on the HBM (high-bandwidth memory) of AMD's GPU (graphic processor unit) code-named Fiji, as shown in **Figure 6b**. The spacing between the pillars on the C2 chip with either NCP or NCF by TCB with high bonding force can be as small as 10 $\mu$ m.

ASM's TC bonder AD93212 [8] is specifically designed for high-bonding force TCB of C2 bumped chips on a substrate with NCP, and for TCB of a C2 bumped wafer with NCF (after dicing into individual chips) on substrate/die. The xy-placement accuracy is  $\pm 2\mu$ m @ 3 $\sigma$  and die rotation is  $\pm 0.001^\circ$  @ 3 $\sigma$ . The bond force is more than 500N. The heater surface temperature is 450°C and is a ceramic pulse heater. The die size range is from 1x1 to 30mm x 30mm (the minimum thickness is 50 $\mu$ m) and the wafer size can be 200 or 300mm.

### High-throughput TCB process

One of the key drawbacks of TCB, comparing with solder mass reflow, is throughput. By adopting the advantages of the machine in [9] and modifying it slightly, a liquid phase contact (LPC) low-bonding force TCB process (IN-press™) is proposed, which has the following operational sequence (**Figure 7**):

- Flux is printed or sprayed on the substrate.
- The bond head (BH) picks up a die from the carrier at an elevated temperature, which is 20 to 30°C below the solder melting point.

c) The BH heats up to a temperature higher than the solder melting point.

- The chip is aligned with the substrate.
- After the vision alignment, the chip contacts and wets on the substrate at a predetermined bonding level.
- After a certain bonding time, the BH moves away at the bonding temperature or cools down to a

temperature below the melting point of solder.

The new machine can be used for low-bonding force TCB of thin C2 bumped chips on thin substrates and thin die stacking [27]. The whole bonding cycle for an LPC process is less than 4 seconds. If the required stand-off height is near the solder equilibrium level, then the cooling



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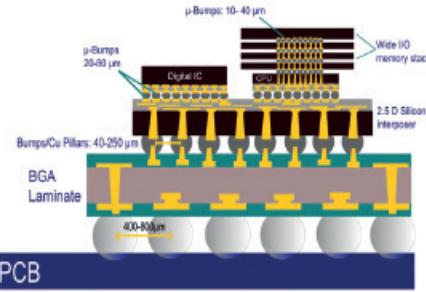
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step can be omitted and the bonding cycle can be further reduced to less than 3 seconds. Since it is in an inert environment, and in some circumstances such as die-to-die bonding, the fluxing step can also be eliminated. In that case, the bonding cycle can be as little as 1 second.

## Summary

TCB for flip-chip technology has been investigated in this study. Some important results and recommendations are as follows:

- For Cu-to-Cu direct diffusion bonding, the spacing between pads is 5 $\mu\text{m}$  or less.
- For mass reflow of C4 bumped chips, the spacing between bumps is as low as 50 $\mu\text{m}$ .
- For mass reflow of C2 bumped chips, the spacing between Cu-pillars is as low as 25 $\mu\text{m}$ .
- For low-bonding force TCB of C2 bumped chips, the spacing between Cu-pillars is as low as 8 $\mu\text{m}$ .
- For high-bonding force TCB of C2 bumped chips with either NCP or NCF

underfills, the spacing between Cu-pillars is as low as 10 $\mu\text{m}$ .

- The post-assembly underfill approach (CUF and MUF) is usually applied to flip-chip assemblies with mass reflow and low-bonding force TCB methods.
- The pre-assembly underfill approach (NUF, NCP, and NCF) is usually applied before flip-chip assemblies with mass reflow (with NUF) and the high-bonding force TCB method (with NCP and NCF). In general, the NUF and NCP are applied on the substrate and the NCF is laminated onto the C2 bumped wafer and then diced into individual chips.
- The advantages of TCB are for higher pin-count, finer pitch, and thinner chips, lower-profile substrates, and controlling warpage and die tilt.
- One of the drawbacks of TCB is throughput (compared with mass reflow). Gang bonding is a possibility to increase the throughput. A larger bonding force on the bond head, however, poses other challenges, such as cracking. The LPC low-bonding force TCB process (IN-press™)

proposed in this study could be one way to enhance the throughput of TCB for flip-chip assemblies.

## Biographies

John H. Lau received his PhD degree from the U. of Illinois, Urbana and is a Senior Technical Advisor at ASM Pacific Technology Ltd.; email john.lau@asmpt.com

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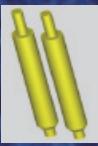
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(continued on page 55)



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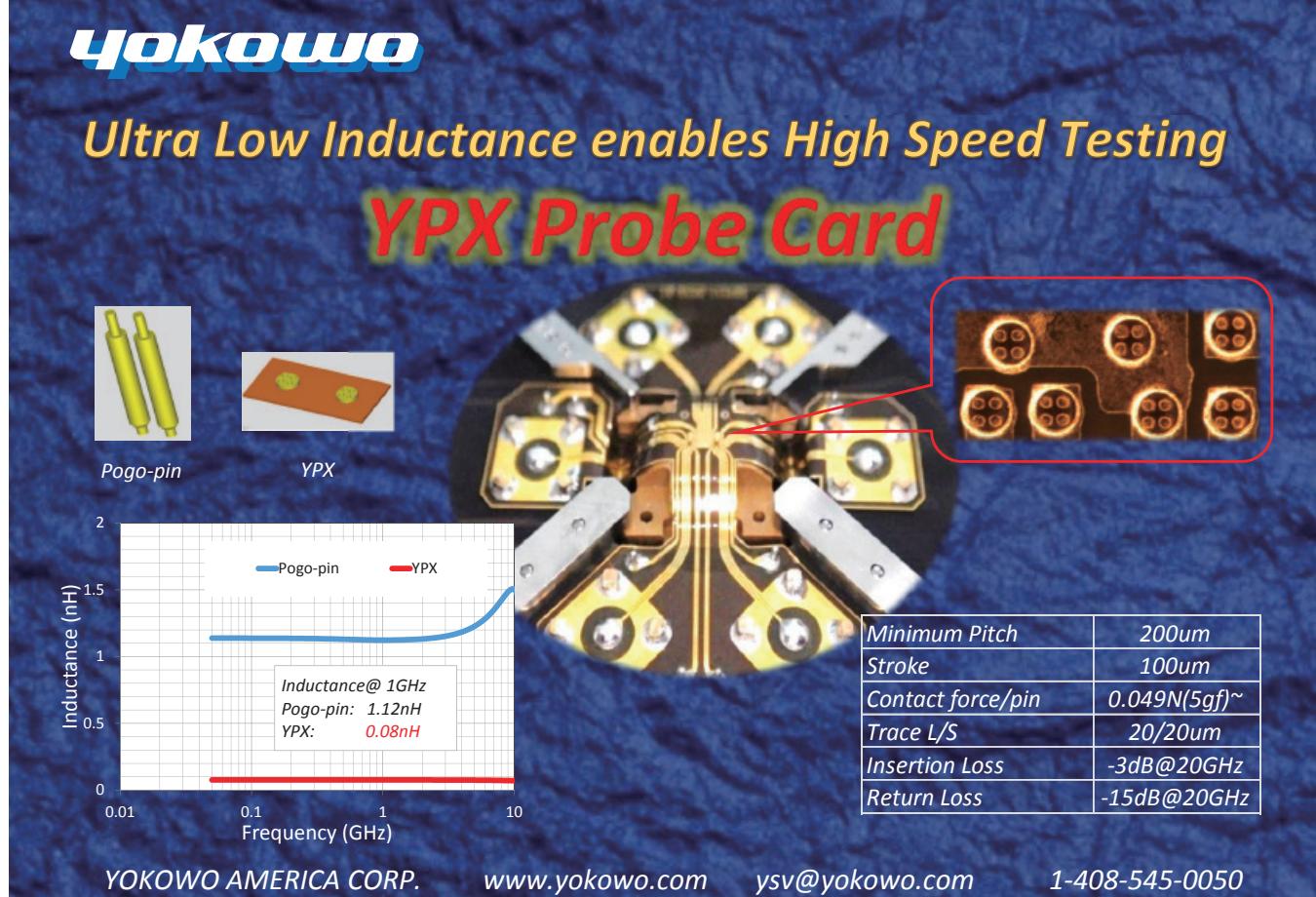
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# Using cost modeling to make better design decisions

By Amy Palesko [SavanSys Solutions LLC]

**T**here are many factors that affect the technology choices engineers, product designers, and managers make. However, at the highest level, there is only one guiding principle in making the optimal decision. The right packaging choice is the one that achieves all product requirements at the lowest cost. Many companies rely on cost modeling as a tool to make this decision. Cost modeling approaches may be as simple as using a spreadsheet with basic process flow information and cost-of-ownership calculations, or as robust as dedicated software.

Once a cost model for a specific design or technology is available, there are multiple ways it can be employed for better decision making. For example, when deciding whether to invest in or promote a new technology, the supplier of the new technology may utilize cost models to determine whether it will be competitive. Cost models are also useful when looking only at existing technology. If the requirements for a product can be met with multiple packaging approaches, cost modeling enables designers to determine the cost of each option before committing to a design. This article explores the methodology behind activity-based cost modeling before shifting into detailed examples of technology cost trade-offs.

## Activity-based cost modeling

Activity-based cost modeling and parametric cost modeling are the two dominant methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model that matches as closely as possible. This “black box” approach, an extrapolation based on historical data, is only appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities. For dynamic trade-offs, activity-based cost modeling is the most accurate cost modeling method because individual activities are characterized and analyzed. Both methods are summarized in **Table 1**.

	Activity Based	Parametric
Creation Method	Model created by characterizing individual process activities and building the process	Model created by statistically analyzing historical data
Best Application	<ul style="list-style-type: none"><li>• New technologies</li><li>• Little or unreliable historical data</li><li>• Knowledge of manufacturing process flow</li></ul>	<ul style="list-style-type: none"><li>• Process is stable/changes slowly</li><li>• Difficult to decompose the process into activities</li></ul>

**Table 1:** Activity-based cost modeling and parametric cost modeling.

Component	Description	
<b>Direct Cost</b>	Measured Cost – May be done at the activity level or at the factory level	Cost models are used to estimate this directly
<b>Indirect Cost</b>	Factory cost that is not directly associated with an activity. Support, quality, manufacturing engineering, utilities, plant, etc.	While all four of these vary widely, their total is driven to a level of consistency by the market. They are usually applied on top of direct cost as a percent and per manufacturing object.
<b>Overhead</b>	Company cost that needs to be covered. Typically Q&A, marketing, engineering, etc.	
<b>Profit Margin</b>	Usually a percentage of total cost	
<b>Risk Factor</b>	A higher than usual margin may be allocated to new technologies	

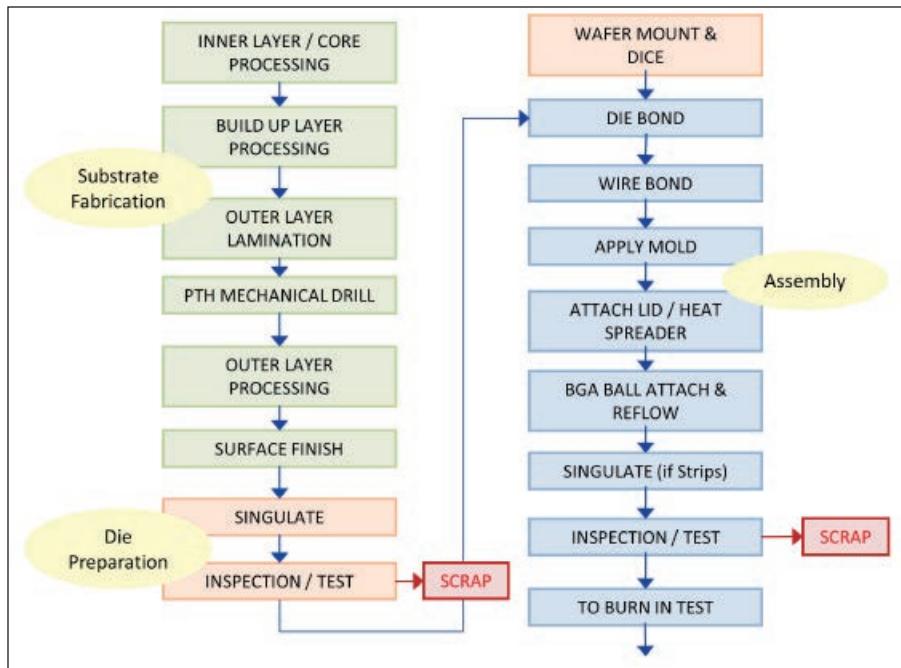
**Figure 1:** Types of costs.

In activity-based cost modeling, the total cost of any manufacturing process is calculated by dividing the process into a series of activities and totaling the cost of each. The cost is determined by analyzing the following attributes: 1) Time required to complete the activity; 2) Amount of labor dedicated to the activity; 3) Cost of material required to perform the activity; 4) Tooling cost for the activity; 5) Depreciation cost of the equipment required; and 6) Yield loss associated with the activity.

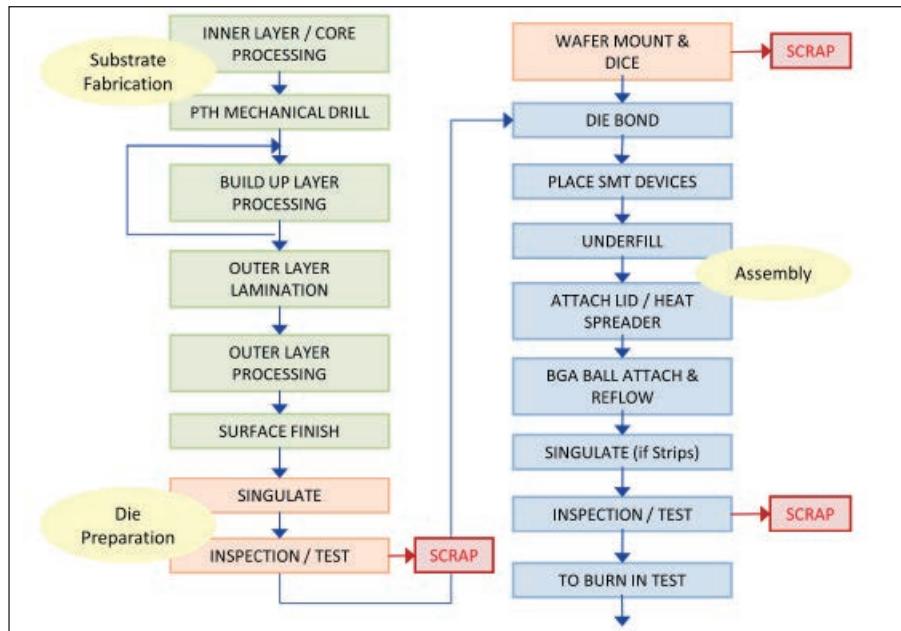
From a results perspective, the attributes listed above break down into the following cost components: 1) Direct labor – determined by the time required multiplied by the percentage of an operator required to perform the activity; 2) Material – both consumable and permanent; 3) Capital – calculated by allocating the equipment depreciation cost based on how long the product uses that equipment; 4) Tooling – usually only a significant cost component

for low-volume product, this is where one-time costs such as nonrecurring engineering (NRE), masks, programming, special fixtures, etc., are captured; 5) Yield hit – for assembly steps, this will be defects per million opportunities; for fabrication steps, this will be defects per square centimeter. Although these defects are not visible until later in the process after testing, they add cost when they are created. These components comprise the direct costs associated with any process. To take the step from direct cost to price, considerations that include indirect costs and overhead must be taken into account (**Figure 1**).

Rather than deep diving into the detailed adjustments that can be made for a single process flow, comparisons are made at the technology level for this article. The goal is not only to understand how cost modeling is used to make technology decisions, but more importantly, to address the question of why a particular technology is more cost effective.



**Figure 2:** Typical wire bond process flow.



**Figure 3:** Typical flip-chip with reflow and capillary underfill process flow.

### Wire bond vs. flip-chip packaging

Industry-calibrated wire bond and flip-chip models were used to analyze the cost of using both technologies to package the same design. Before introducing the designs and results, it's worthwhile to look at the process flows individually.

Wire bonding is a mature technology, so the process is well understood and the cost drivers straight-forward. The main cost drivers are package size, package I/O count, and wire length and diameter (particularly if

using gold wire). Although many of the I/O activities are batch processes, the reason this is still considered a key cost driver is because I/O count correlates directly to the number of wires. Design limitations also need to be kept in mind for any technology. With wire bond, I/O count is limited by the need to have all of the die pads on the periphery of the die instead of in a grid.

Flip chip is also a mature technology. Like wire bonding, package size is a cost driver with flip-chip technology. Unlike wire

	Wire Bond	Flip Chip
Package Size	31mm x 31mm	
Die Size	12mm x 12mm	
Number of I/Os	1000	
Wire Material	Gold	N/A
Substrate	4 layer	3-2-3
Wire Length	2.5mm per I/O	N/A

**Table 2:** Flip-chip and wire bond design parameters.

Flip Chip Results		Wire Bond Results	
Total Cost	\$4.64	Total Cost	\$2.20
Substrate Cost	\$3.31	Substrate Cost	\$0.57
Assembly Cost	\$1.33	Assembly Cost	\$1.63

**Table 3:** Flip-chip and wire bond results.

	% of Total Cost from Assembly Steps	Assembly Material Costs
Wire Bond	74%	\$1.13
Flip Chip	29%	\$0.49

**Table 4:** Flip-chip and wire bond assembly comparison.

bonding, substrate structure has more of a cost impact here. Furthermore, the fact that wafer bumping is necessary is also a major cost adder. A typical wire bond process (**Figure 2**) and typical flip-chip with reflow and capillary underfill process (**Figure 3**) are included for reference. The key design parameters for the comparison selected are listed in **Table 2**, and the results for each technology are shown in **Table 3**.

It likely comes as no surprise that the wire bond package is cheaper than an equivalent design packaged with flip-chip technology. It is general industry knowledge that, if the design goals can be met, it will almost always be cost effective to use wire bonding technology. The reason cost modeling was used for this example was not to determine which packaging choice would be cheapest, but to illustrate how the models allow us to see from where cost is coming. While the majority of the difference is from the cost of the substrate, it's worthwhile to compare the assembly portions as well, even though the difference is only 30 cents.

The main item of interest from an assembly perspective is the percentage of total cost the assembly steps represent. **Table 4** shows how much of the total cost comes from the assembly portion for each flow. Another point of comparison, while not related to percentage of total cost, is the difference between material costs for the two assembly flows. The material costs in **Table 4** are an aggregate of all material cost contributions for all steps in the assembly portion of each process flow. The largest material contributor for wire bond assembly is the cost of the gold wire. The largest material contributions in the flip-

	<b>Labor</b>	<b>Material</b>	<b>Capital</b>	<b>Tooling</b>	<b>Yield Hit</b>	<b>Overhead</b>	<b>Total</b>
<b>Wire Bond</b>	\$0.012	\$0.279	\$0.037	\$0.000	\$0.000	\$0.033	<b>\$0.36</b>
<b>Flip Chip</b>	\$0.052	\$0.550	\$0.037	\$0.398	\$0.122	\$1.402	<b>\$2.56</b>

**Table 5:** Substrate layer cost contributions.

	<b>Flip Chip</b>	<b>Fan-Out WLP</b>
<b>Package Size</b>	10mm x 10mm	
<b>Die Size</b>	8mm x 8mm	
<b>Number of I/Os</b>	625	
<b># of RDLS</b>	N/A	2
<b>Substrate</b>	1-2-1	N/A

**Table 6:** Flip-chip and FOWLP design parameters.

<b>Flip Chip Results</b>		<b>Fan-Out WLP Results</b>	
<b>Total Cost</b>	<b>\$0.822</b>	<b>Total Cost</b>	<b>\$0.862</b>
<b>Substrate Cost</b>	\$0.329	Die Preparation Cost	\$0.008
<b>Assembly Cost</b>	\$0.493	Packaging Cost	\$0.854

**Table 7:** Flip-chip and fan-out WLP results.

chip flow are from the cost of the underfill and the wafer bumping steps.

Contrasting the 30 cent difference between assembly costs, the substrate cost

for the flip-chip package is nearly six times that of the wire bond substrate. What are the expensive activities driving the higher substrate cost for flip chip? Compared to

the relatively simple 4-layer substrate used in the wire bond package, the flip-chip substrate requires a more complicated 3-2-3 structure to support high-density routing through build-up layers from the die to the substrate. In the flip-chip cost model results, there are 62 steps (or activities) beginning with the inner layer and proceeding through to the last of the three build-up layers. In the wire bond process, there are only 30 steps starting with the inner layer and ending with one outer layer. **Table 5** shows how the cost breaks down for those steps.

While flip chip vs. wire bond is an illustrative example of how cost modeling can be used to compare two technologies, with these two selections, cost modeling would probably not have been necessary for a designer in the real world deciding which avenue to take. There is a general understanding already of the benefits of flip-chip and wire bond designs; experienced members of the packaging industry would know inherently that wire bond packaging for a large design like this would be the cost-effective solution if the product requirements could be achieved. Nevertheless, it's useful to understand where and how the cost is driven even in a top level trade-off with unsurprising conclusions.

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	Labor	Material	Capital	Tooling	Yield Hit	Overhead	Total
2 RDLs (FOWLP)	\$0.004	\$0.053	\$0.219	\$0.000	\$0.045	\$0.147	\$0.468
IL, OL (Flip Chip)	\$0.007	\$0.056	\$0.046	\$0.000	\$0.000	\$0.135	\$0.243

Table 8: Cost components of RDL and build-up layers.

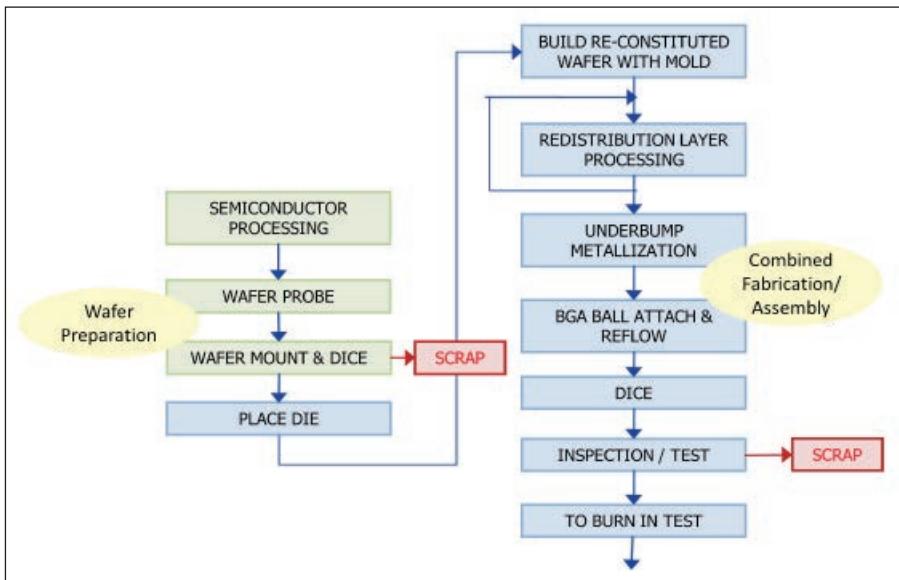


Figure 4: Typical FOWLP process flow.

Technology	Test/scrap die before assembly?	Test/scrap substrate before assembly?	Test/scrap after assembly?	Cumulative Yield
Flip Chip	Yes	Yes	Yes	90%
Fan-out WLP	Yes	No	Yes	81%

Table 9: Yield comparison of flip chip and FOWLP.

Yield	Total Package Cost
95%	\$0.823
92%	\$0.862
90%	\$0.894
88%	\$0.925

Table 10: FOWLP results at different yield points.

## Flip-chip vs. fan-out wafer-level packaging

The next example focuses on a smaller design that can be packaged using flip-chip or fan-out wafer-level packaging technology (FOWLP). The flip-chip process flow and a few of the highlights were already addressed. Before moving into the technology comparison, the FOWLP process flow is introduced in [Figure 4](#). One of the clear advantages with this flow is that there are fewer steps, which makes for a simpler process. On the other hand, there are bigger yield risks associated with FOWLP. Once the die is placed, there is no opportunity to test and scrap until the very end of the flow. This means that any fabrication or assembly defects discovered at that point will require

scrapping the entire package, which may include expensive die as well. Similar to the two technologies previously introduced, package size is certainly a cost driver here. Another notable cost driver is the number of imaging steps. Unlike wire bond and flip-chip technologies, redistribution layers (RDLs) are required to distribute the package I/Os, and these require expensive lithography steps.

The key design parameters used to compare flip chip and FOWLP are outlined in [Table 6](#); [Table 7](#) lists the top-level results. In this case, flip chip is more cost effective than FOWLP but by a narrower margin than in the previous comparison. This flip chip vs. FOWLP example is also more of an apples to oranges comparison. While wire bond and flip chip are very different technologies, their process flows and costs still break down into assembly and substrate portions. FOWLP, on the other hand, doesn't have two distinct portions of the process flow in the same way.

With the technologies being so different, it's difficult to make direct comparisons in many areas. One of the more interesting ways to look at the detailed cost results is to compare RDL steps from the FOWLP flow

to build-up steps from the flip-chip flow. The creation of one RDL can be seen as similar to the creation of one build-up layer, in that each serves the same purpose from a substrate perspective. [Table 8](#) shows the cost components associated with fabricating two RDL layers vs. two build-up layers. The largest contributions to the cost difference come from capital and yield considerations. Yield will be discussed in the following example. As for capital, the increased capital cost for FOWLP is because the lithography equipment required to create an RDL is more expensive than the equipment needed for the build-up portions of a flip-chip package.

The final set of numbers is an example of a key cost factor that should always be taken into account: yield. [Table 9](#) summarizes how the cumulative yield is different for these two technologies even when the incoming yields are the same. The table shows the cumulative yield with the following incoming yield assumptions: 1) 90% die yield; 2) 90% fabrication yield; and 3) 90% assembly yield. To tie this to the design example already given in this section, the cost of the FOWLP package at different cumulative yields was calculated ([Table 10](#)). Note that with this design, if a yield of 95% is achieved, it becomes cost-competitive with the same design in a flip-chip package.

## Summary

Cost modeling is not only a useful tool for determining the lowest cost choice to meet product requirements, but a necessity for understanding the cost drivers. With an understanding of technology cost drivers, everyone from designers to supply chain managers can make more cost-effective decisions.

The technology comparisons in this article provided examples of different ways cost modeling can be used. The wire bond and flip-chip comparison did not provide surprising results overall, but illustrated which characteristics of the process flows contributed to the notable cost difference. The flip-chip and FOWLP comparison was more interesting because the total cost results were closer. This made it an example of how cost-effective packaging choices depend heavily on design parameters.

## Biography

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# Bond tester study of CSP reliability through bump analysis

Evstatin Krastev, Ian Christopher Mayes, Chan Myat, Armin Struwe [Nordson DAGE], Rene P. Zingg [Zinan GmbH], Ricardo Geelhaar [PacTech GmbH]

**M**iniaturization, the drive to lead-free semiconductor products, combined with the increasingly harsh application environments impose stringent requirements on solder bump reliability in chip-scale packages (CSP). In addition to a clear quality specification, there is a need for comprehensive mechanical testing to ensure reliable solder connections over the projected lifetime of the device. Such tests must detect problems and nonconformances as early as possible in the production cycle. A systematic approach to predict product lifetime, monitor ongoing production, process control statistical methods, and failure analysis is needed in order to guarantee high-quality product.

While nondestructive tests like X-ray computer tomography are always desired, they cannot replace the information that can be deduced from standard mechanical bond test methods like shear and cold bump pull (CBP). This paper discusses CSP bump reliability in general, and various bond test methods in particular. A case study evaluating different solder compounds (Sn-0.7%Cu, Sn-3%Ag-0.5%Cu, Sn-3%Ag-0.7%Cu) is also presented in order to illustrate the methodology and discuss the challenges.

## Discussion of bump failure modes in CSP packages

Open, intermittent contact in the final product is the major failure mode. This can be caused by delamination from excessive stress, coalescence of voids formed during assembly, undesirable intermetallic compounds (IMC) formed during reflow of the solder, or void formation through electromigration. Several root causes can also compound, e.g., when multiple IMCs with different electrical resistivity and/or voids cause current-crowding, thereby accelerating electromigration. These problems can be minimized by adequate process control, proper material choice, and design optimization to minimize stress from different coefficients of thermal expansion (CTE). It is important to note that even slight changes in alloy composition of the solder can have a large effect on its mechanical properties.

Shorts or leakage paths between bumps is another typical failure mode. Root causes for this are attributed to insufficient barrier by the underfill to whisker growth and surface contaminations leading to ionic or galvanic leakage paths. This mode is typically more related to underfill and cleaning than to bump composition and formation.

## Process control

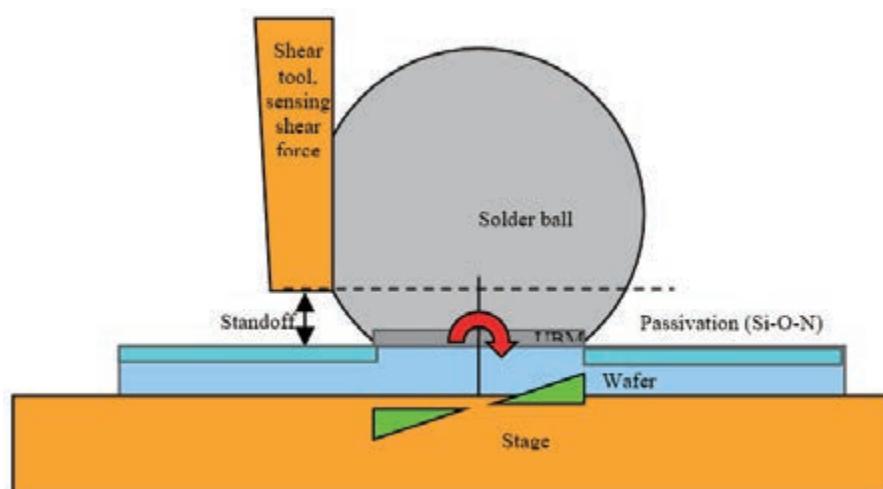
Once the solder composition, pad size and arrangement, and substrate material (under-bump metal choice and thickness) are finalized from finite element modeling (FEM), the assembly process, and its expected variation over substrate space and time has to be considered and examined. Common methods include DoE for process parameters and their variation, x-ray tomography and mechanical cross-sections (saw and polish or focused ion beam). These need to be performed on virgin devices and after accelerated life tests, such as thermal cycling and electromigration testing. The goal of this type of study is to understand the microstructure of the bump (including grain structure, precipitates, phase boundaries, IMC formation at under bump metallization (UBM), and occurrence of voids). In addition comparing samples with and without underfill

will establish if the particular material used fulfills its task of stress attenuation and confinement of bumps to prevent premature delamination. These qualification tests should be regularly repeated as a monitoring program, e.g. on a quarterly basis.

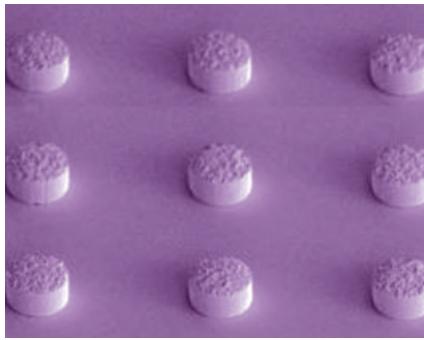
In addition to this qualification and reliability monitoring program, a continuous process control system is needed and since no non-destructive tests exist, bump shear (BST) and bump pull test (BPT) before system assembly, as well as die shear (DST) and die pull testing (DPT) after assembly are widely used. These tests are described in detail in various industry standards and publications. Brittle fail at the IMC interface, extensive voiding, pad lift, i.e., delamination of the metallization under the UBM, are all reject criteria commonly used by the industry. It is very important to test bump quality before and after CSP assembly. This double testing becomes instrumental when trying to distinguish between material defects and assembly-related weaknesses.

## Bond tester techniques for evaluation of bump quality

The three most common techniques for evaluation of bump quality and integrity are bump shear (BST), cold bump pull (CBP)



**Figure 1:** Schematic representation of shear test. The resulting momentum on the bump base is shown as a red arrow; green triangles represent the resulting tensile and compressive forces on the bump base.



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and hot bump pull (HBP). The HBP test was developed to study pad cratering failures as per IPC-9708 standard.

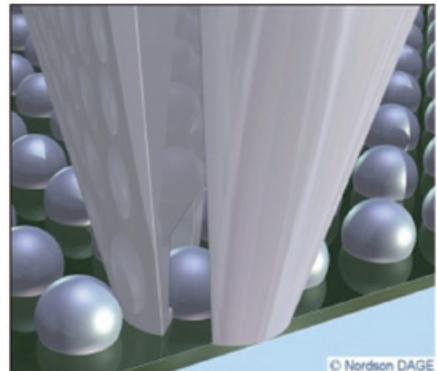
The HBP test is performed by soldering a pin to the solder ball using a pre-defined temperature profile and then performing a pull test. The nature of the grip allows the pull force to be orientated with respect to the pad, simulating real life service conditions. Additional information can be obtained by cyclic loading.

It is well known that BST has complex force distribution (**Figure 1**). In addition, the shear tool imposes a rotational moment proportional to shear force and standoff (shear height), which in turn results in a lifting force at the leading edge of the UBM/bump system.

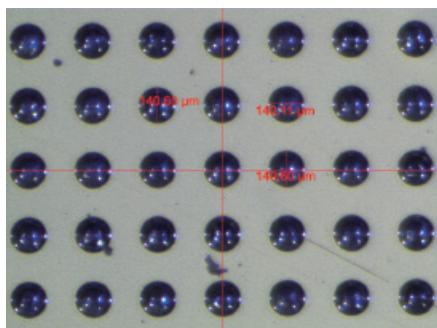
BPT (**Figure 2**), on the other hand, uniformly distributes the test force over the bump base. While BST imposes a significant pull stress only at the leading edge, CBP and HBP tests stress the whole UBM area, both at the IMC interface to the bump above and the pad structure below the UBM.

To summarize the above discussion, both shear and pull tests need to be considered and used when designing the test plan. The shear test is more straightforward and easy to perform and automate, however, in many cases, the pull test provides additional valuable information and failure modes that may not occur in a simple shear test.

There is a clear need to test components, materials and bonds under controlled conditions that generate failure modes similar to those observed in service. In general, bond testing involves pulling or shearing at relatively low strain rates. Solder joints often fail by ductile fracture of the bulk solder and other parts of the joint do not experience the stress levels they would see if the loading on the joint had been more rapid. All joints can be thought of as a chain where the links of the chain represent the various materials that make up the joint. A simple solder joint on a PC board comprises a number of links: bulk solder, an intermetallic layer at the interface with the bond pad, the bond pad, an adhesive layer between the bond pad, and the organic substrate and the substrate itself. The joint is only as good as its weakest link and at low strain rates this is often the bulk solder. It is well known that solders exhibit time-dependent deformation and that their yield point increases dramatically with strain rate. The much higher strain rates associated with impact and board bending result in much higher forces on the bond pad, as for these cases there is less time for the material to flow. High strain rates produce larger bond pad forces. Soldered connections can fail in a brittle manner at high rates of strain. Low strain rate testing cannot pick



**Figure 2:** Illustration of a cold-bump pull (CBP) test. Force geometry is less complex than BST and a uniform tensile stress is projected over the bump base.



**Figure 3:** SAC305 solder bumps after first reflow as used in this study.

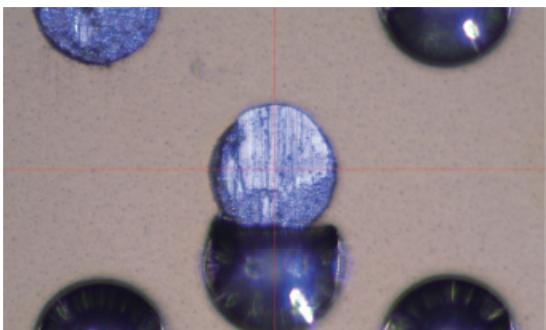


**Figure 4:** Test setup for BST testing. The wafer samples were secured using a vacuum wafer chuck.

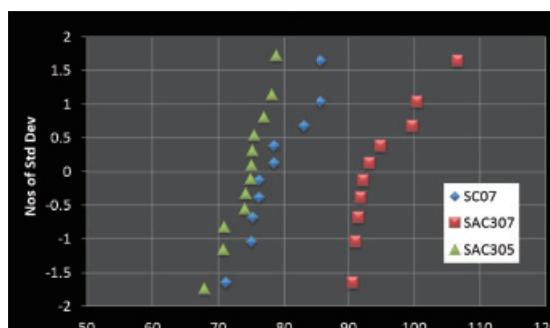
up the microstructural changes that occur at the bond interface responsible for a brittle connection. Low strain rates cannot identify microstructural changes that lead to brittle fracture. Therefore, in order to study brittle fracture failures, we need to employ high strain rate testing in addition to the regular BST and CBP.

### **Case study: low-speed shear test of various SAC alloys**

In order to illustrate the above discussions, we performed a simple bond tester study of various SAC solder alloys. Lead-free solders around the Sn-Ag-Cu eutectic point offer many



**Figure 5:** Ductile failure of an SAC305 bump. The test speed was 500 $\mu$ m/s with a 10 $\mu$ m shear height (standoff).



**Figure 6:** Cumulative distribution of a ball shear test for three lead-free solder compounds.

choices of parameters critical to assembly, such as melting point or range, thermal expansion coefficient, ductility or hardness. The specimen consisted of 125 $\mu$ m solder balls of SAC305 (Sn-3%Ag-0.5%Cu), SAC307 (Sn-3%Ag-0.7%Cu), SC07 (Sn-0.7%Cu) that were placed on pads of 120 $\mu$ m diameter. The under bump metal (UBM) consisted of 5 $\mu$ m-thick Ni coated with an Au anti-oxidation layer. After reflow, the solder balls formed 90 $\mu$ m-high bumps with a diameter of about 140 $\mu$ m (**Figure 3**), indicating a slight sag compared to a perfectly spherical bump (97 $\mu$ m-high, 134 $\mu$ m maximum diameter).

HBP tests showed exclusively solder failure, while CBP tests showed solder extrusion failures in some cases. We therefore concentrated on a simple shear testing experiment in order to evaluate the three different solder alloys. BST was performed using a 150 $\mu$ m-wide flat chisel at 500 $\mu$ m/s with a 10 $\mu$ m shear height (standoff). The wafers were secured using a vacuum wafer chuck. The test setup is shown in **Figure 4** and a typical ductile failure mode is shown in **Figure 5**.

**Figure 6** shows the shear test results on a normalized distribution plot. The narrow distribution indicates a fairly well controlled process with random process variation. Based on this, it can be concluded that SAC 305 and SC07 perform in a very similar way. However, only slight variation in composition (increasing Cu content by 0.2% in SAC307) results in a

significantly stronger solder alloy. Thus, the Sn-Ag-Cu system can offer many interesting material property variations around its eutectic point (SAC, close to SAC378 or Sn-3.75%Ag-0.8%Cu). These can be effectively studied using the bond tester methods discussed above.

## Summary

As a general conclusion, we want to reinforce that there is a clear need to test components, materials and bonds under controlled conditions that generate failure modes similar to those observed in real life. A simple solder joint can fail due to multiple factors and the weakest link could be in the bulk solder, the intermetallic layer at the interface with the bond pad, the bond pad itself, the adhesive layer between the bond pad, and the organic substrate and the substrate itself. This implies that a test methodology comprising standard BST and BPT, as well as high strain rate testing and HBP, provide a comprehensive set of test results that can be used to monitor quality and optimize design and materials. In addition, camera-assisted automation of the bond testing process permits large statistically significant data sets to be acquired in a short period of time, and minimizes operator dependency.

## Biographies

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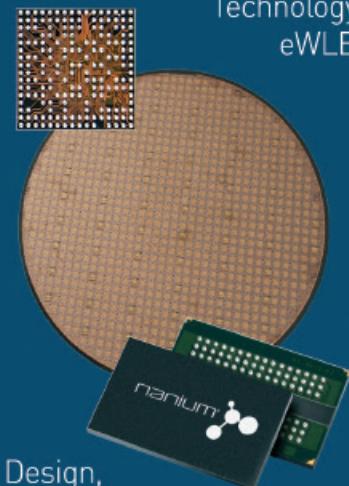
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# Solving delamination in lead frame-based packages

By Rongwei Zhang, Yong Lin, Abram Castro [Texas Instruments Inc.]

**D**elamination at various interfaces in lead frame-based packages, such as small outline integrated circuit (SOIC), thin-shrink small outline package (TSSOP), quad flat package (QFP) and quad-flat no-leads (QFN), remains one of the most critical reliability issues in plastic-encapsulated IC packages. In plastic-encapsulated IC packages, there are many interfaces adhered together. These interfaces include mold compound to die, die to die attach material, die attach material to lead frame, mold compound to die pad, mold compound to lead finger, and die pad backside to mold compound in an SOIC package (Figure 1).

When an IC package is exposed to a humid environment, mold compound and die attach materials (polymer composites)

will absorb moisture in two ways: 1) through bulk mold compound, and 2) through interfaces between the mold compound and lead frame. This absorption will influence material properties in several ways; first, mold compound and die attach materials will expand, while the die and lead frame do not. This expansion induces the hygostresses within packages. Second, the absorbed moisture can change the modulus and glass transition temperature ( $T_g$ ) of polymer materials to lower values. Third, moisture ingress through the interface and accumulation of water at the interface will degrade the interfacial adhesion caused by water bonding to polymer chains, especially where secondary bond forces dominate the adhesion.

During system board assembly, if the plastic packages with absorbed moisture are subjected to a reflow process, large thermal stresses are induced along the interfaces owing to differences in the coefficient of thermal expansion (CTE) of the packaging materials. Meanwhile, as temperature increases during reflow (peak temperature up to 260°C), the absorbed moisture will vaporize resulting in a high vapor pressure, and the interfacial adhesion will further decrease. The combined effect of high vapor pressure, stresses, and decreased adhesion can lead to interfacial delamination and package cracking during reflow (also known as “popcorning”). Therefore, the delamination at different interfaces is generally driven by the mismatch of different material properties such as CTE, hygro-swelling, vapor pressure-induced expansion during the reflow process, and adhesion degradation caused by moisture absorption and/or temperature increase [1, 2]. Delamination at different interfaces is usually detected by C-mode

scanning acoustic microscopy (C-SAM), through transmission scanning acoustic microscopy (TSAM), and scanning electron microscope (SEM). Figure 2 is an example of detecting the delamination between die attach material and lead frame using SEM.

## Factors affecting delamination

Many factors can contribute to interfacial delamination in lead frame-based packages. These factors mainly include package structure, packaging material, assembly process, and reliability test condition. Factors contribute to the delamination at different interfaces could be different. Here, we will focus on polymer-based packaging materials and assembly process.

**Package structure/geometry.** Many package structure factors, such as package dimension (x, y, z), die dimension, die pad dimension, lead frame design, number of leads, the distance from die edge to pad edge, have a significant effect on package delamination. Packages with exposed die pad are more prone to delamination due to the unbalanced encapsulation of the package. This unbalanced encapsulation increases the mechanical stress at the die-to-die pad interface during IR reflow, which can lead to an increase in die pad delamination [3].

**Packaging materials.** Packaging material properties play a key role in package delamination. In particular, CTE, modulus, the amount of moisture absorption, and moisture diffusion rate of both mold compound and die attach material are major factors contributing to the stress during reflow. Ideally, selecting the material with CTE equal or close to the bonding material, and with lower modulus, lower moisture absorption and fast diffusion rate would result in better delamination performance. Additionally, the ability of the package materials (mold compound and die attach material) to maintain their high adhesion strength post moisture absorption and thermal stress, is another important factor. By nature, polymer composite material properties are not ideal and have to be compromised to

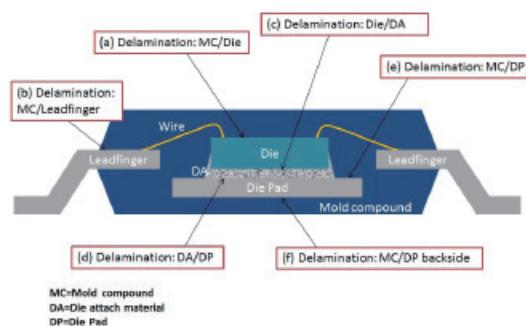


Figure 1: Delamination at different interfaces in an SOIC package.

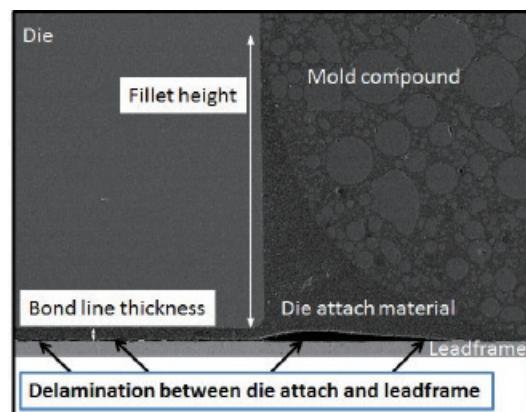


Figure 2: A SEM image of the interfacial delamination between die attach material and lead frame in a lead frame-based package.

meet a specific manufacturing process and delamination requirement.

Examples of the tradeoff can be seen in both die attach material and mold compound. At first thought, it would be ideal to select a low modulus die attach material to improve delamination performance; but if the material is used in conjunction with a copper wire bonding process, high bonding temperatures dictate that the die attach material have a relatively high modulus to prevent energy dissipation from the active bonding area. With respect to the mold compound, higher adhesion mold compound is preferred from a delamination point of view, but this is limited by the molding process—too high adhesion could result in manufacturability issues. Selecting or developing a polymer material with key balanced properties meeting a specific manufacturing process and delamination requirement is critical for successful material qualification.

**Assembly process.** The assembly process is another key factor affecting delamination because packaging material properties can be significantly changed by it. Examples are discussed below.

The delamination between die backside and die attach material can be affected by wafer backside surface roughness. The interfacial adhesion can be improved with higher roughness of the die backside thereby improving the delamination at the interface between die backside to die attach material.

In the die attach/cure process, several variables exist. The time between die attach paste dispense and die placement (open time), and the time between die placement and curing (staging time) are critical to prevent voiding and adhesion degradation. Curing temperatures and time will also drive differences in die attach material properties, resulting in the same die attach material demonstrating different delamination performances. Some lower curing temperatures may be applied to lower the modulus of die attach materials for large packages to absorb the stress, while in other cases, higher temperature may be applied to improve the adhesion. Other parameters in the die mounting process that result in different bond line thickness (BLT), fillet height and coverage of die attach materials will affect the delamination. Thicker BLT, higher fillet height without contaminating the die surface, and more coverage are preferred to improve delamination.

Assembly innovations in wire bonding and molding have influenced die attach delamination in heretofore unobserved

ways. As the industry moves from gold wire to bare copper wire and palladium-coated copper wire (PCC), the impact of wire bonding processes on die attach delamination becomes increasingly significant due to higher bonding temperature. This impact is accelerated as the industry moves toward larger lead frame strips (100mm x 300mm) and package miniaturization because the strips are exposed to more time at the higher wire

bond temperatures. During the molding process (typically transfer molding) at 175°C, mold compound will cross-link and form polymer networks, which will decrease the mold compound volume (called “cure shrinkage”). Cure shrinkage will induce stresses. After molding, post-mold cure (PMC, typically at 175°C for 3-6 hours) is performed to further cure the mold compound. During PMC, material properties are changed and further cure



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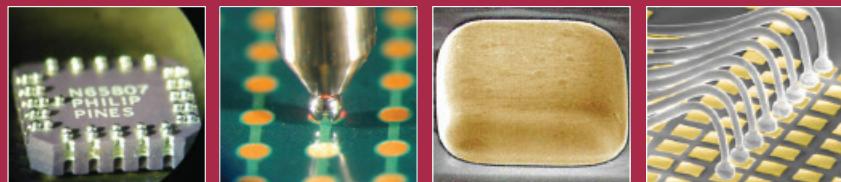
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shrinkage can occur. Subsequent processes such as degating, deflashing and singulation can exert high stress on the package and cause delamination.

External factors, such as contamination, from the assembly process can also induce delamination. Many contamination cases were reported to induce delamination at different interfaces. For example, the residuals transferred from back grind tape can cause die top to mold compound delamination. During the curing of die attach material, the deposit of outgassing from die attach material can contaminate the lead fingers and potentially cause the delamination at the interface of the mold compound to lead frame. Many technologies are available to detect the contaminants which include, but are not limited to, Fourier transform infrared spectroscopy (FT-IR), time-of-flight secondary ion mass spectrometry (TOF-SIMS), SEM, X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), and contact angle measurement.

**Reliability test conditions.** Package reliability tests that can induce delamination typically include moisture sensitivity level (MSL), thermal cycling, high-temperature storage, and autoclave. In these tests, different humidities, temperatures and other environmental factors, when applied to a package, can affect the material properties and interfacial adhesion to a different extent, and thereby resulting in different levels of delamination.

### Impact of delamination

Delamination at different interfaces can cause various failures, which are discussed below.

- Delamination between die active surface and mold compound (**Figure 1a**) can cause the ball bond to be mechanically lifted, thereby leading to electrical failure during thermal cycling. The delamination is a key trigger for passivation cracking, so delamination at the interface of the active die surface and mold compound is usually not allowed.

- Similarly, the delamination at the interface of the lead finger and mold compound (**Figure 1b**) can cause the stitch bond to break and result in an open circuit. Bare copper or PCC wires are more susceptible to broken stitching as they are harder than gold wire. Therefore, as bare Cu wire or PCC gets more popular in the industry, improving mold compound delamination (**Figures 1a, b and e**) becomes increasingly critical to manufacture reliable Cu wire-based packages. Moreover, as mold compound delamination occurs, moisture and contaminants (such as corrosive ion Cl<sup>-</sup>) can easily enter the package. With moisture, the mobility of corrosive ions like Cl<sup>-</sup> can significantly increase, which will accelerate Cu wire corrosion and lead to electrical failures at ball bonds and stitch bonds. The mobile ions entering the package can also cause current leakage [1, 4].

- For thermally enhanced packages, there is a thermal requirement. Die attach delamination (**Figures 1c and d**), which includes the delamination at the interface between the die and die attach material and between die attach material and lead frame (**Figure 2**), reduces the contact area of the die to the lead frame, and therefore, increases the thermal resistance of the package. As a result, if the die operating temperature exceeds the maximum junction temperature, the device can shut off because of overheating. The maximum acceptable percentage of delamination will be highly dependent on device power and power distribution over the die surface [5, 6].

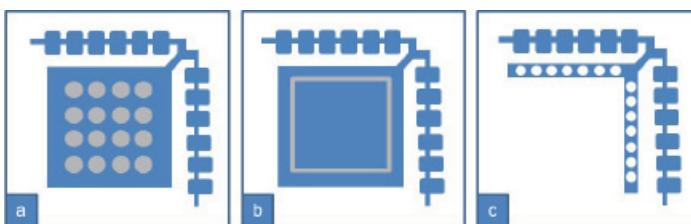
It should be pointed out that not all types of delamination are a major reliability problem. The delamination between the mold compound and die pad (**Figure 1e**) may not be regarded as serious if there is no down bond on the die pad. With down

bonds, the delamination between the mold compound and the die pad should be avoided. Because of the CTE differences between the die pad, the silicon die, and the mold compound, the movement of mold compound can cause the wires to break.

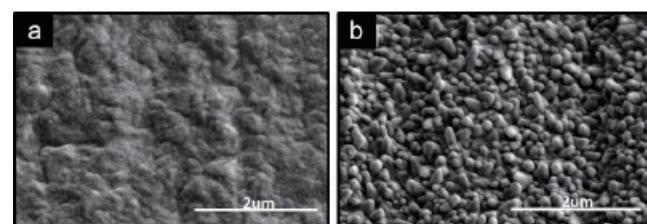
### Solving delamination

In order to manufacture a reliable and robust package without delamination, many factors, such as package design, packaging materials, assembly process, environmental or application conditions, are needed to be carefully considered and optimized. There are many approaches to improve the adhesion and thereby solving the delamination problem, or at least improving the delamination performance. These approaches include selecting or developing new packaging materials, creating dimples/grooves/holes on the lead frame, plasma cleaning, modifying lead frame surface chemistry, such as coating the lead frame with adhesion promoters, and roughening the lead frame.

- Selecting new packaging materials is the typical way that industry takes to eliminate the delamination. In many cases, however, there is a limited choice of materials. Additionally, existing commercial materials may not be fully optimized to meet specific applications and therefore, may offer marginal reliability performance, while developing new materials is typically very time- and resource-consuming.
- Another way to improve the delamination is to incorporate various structures on the lead frame surface, such as dimples, grooves and through-holes, to enable mechanical interlocking and enhance adhesion. Examples of lead frames with different features are shown in **Figure 3**. These mechanical enhancements do not require a change in packaging materials, but may not be applicable



**Figure 3:** Examples of lead frames with a) dimples, b) grooves, and c) through-holes.



**Figure 4:** SEM images of the surfaces of a) a standard lead frame, and b) a roughened lead frame.

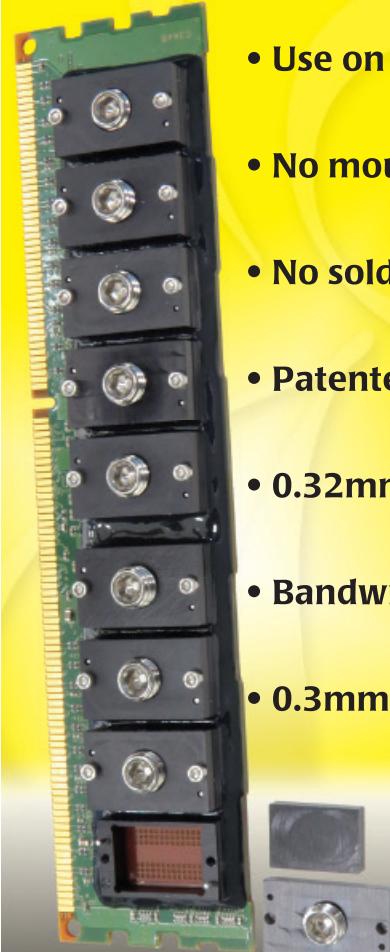
- to small packages where there is not enough space to make structures. Furthermore, if the feature of the structure is too small, there may be concerns with respect to manufacturing and filling the structure with mold compound.
- From a process standpoint, plasma cleaning seems to be the most convenient process to implement. The most commonly used gases for plasma cleaning are argon (Ar), oxygen (O<sub>2</sub>) and their mixtures. In many cases, plasma is applied post wire bonding to remove the contaminants and enhance the wettability, thereby improving adhesion. But in other cases, the improvements may not be significant enough to eliminate the delamination, especially on a NiPdAu lead frame surface. Additionally, plasma cleaning may not be a feasible way to improve die attach delamination. Plasma cleaning increases the surface energy of the lead frame, which will make die attach pastes more prone to bleeding.
  - Modifying lead frame surface chemistry has been used to improve delamination. Oxidizing Cu surfaces of a Cu lead frame is one way to modify the surface and improve the adhesion through enhanced chemical interaction between the mold compound and the Cu lead frame, and increased surface roughness. It is observed that maximum adhesion strength was obtained when the oxide thickness is about 20nm [7]. Further oxidation to increase oxide thickness will dramatically decrease the adhesion. Alternate methods include coating lead frames with an adhesion promoter. An adhesion promoter is typically a bifunctional molecule, with one functional group interacting with the lead frame and the other with the mold compound and/or die attach material. Selecting the right functional groups that can strongly bind to the metal lead frame and cross-link with the mold compound and die attach to form covalent bonds is key to improving the adhesion. Spraying the adhesion promoter post-wire bond is a typical process because applying an adhesion promoter before the die attach process can lead to a wire bonding issue called non-stick on pad (NSOP).
  - Another effective way to improve mold compound and die attach

adhesion is to roughen the lead frame surface. This can be done through a plating process, etching process, or laser texturing [8]. These processes enhance mechanical interlocking and increase surface contact area. **Figure 4** shows the surface comparison between a standard NiPdAu lead frame and a roughened NiPdAu lead frame. The roughened lead frame is typically coated with an

anti-resin bleed out (RBO) material to prevent resin bleed out. The disadvantage of a roughened lead frame includes higher cost and the potential requirements for process and material optimization to meet the manufacturability requirements. A future lower cost option might be achieved through the use of laser texturing based on the proliferation of laser techniques in the industry.

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## Summary

Delamination remains a challenging issue in semiconductor packaging industry. This article provided the understanding of how delamination occurs, factors affecting delamination, impact of delamination, and methods utilized to solve the problem. Several of these methods may be combined to provide solutions. In particular, roughening the surface, combined with other methods as needed, seems to be the most effective and promising way to eliminate delamination. With a roughened lead frame, low cost mold compound and die attach materials can potentially be used to lower the total package cost while improving delamination. Meanwhile, with a roughened lead frame, thinner BLT of die attach material can be implemented to improve package thermal performance without affecting delamination, which also reduces the cost because of a smaller amount of materials used. These will be promising solutions to the delamination challenge to meet the requirements of package reliability, performance and cost.

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# Performance of optimized lithography tools and materials in advanced packaging applications

By Keith Best [Rudolph Technologies, Inc.]

**R**ecent years have seen rapid development in the area of advanced packaging. In general, advanced packaging processes are concerned with the interconnection of multiple chips in a single package to provide increased functionality and performance in a smaller volume. Often advanced packaging processes are adaptations of front-end processes. Their development is being driven primarily by the rapid growth in mobile handheld devices such as smartphones. A number of technologies are in development or in production including wafer-level chip-scale packaging, copper pillar bumps on through-silicon vias (TSVs), fan-out wafer-level processing (FOWLP), and many more.

One technology that has gained rapid acceptance is 2.5D packaging. Similar to the multi-chip-modules (MCMs) of the past, 2.5D packaging processes use an interposer to route signals between the device die and the package substrate. The interposer is a multilayered “circuit board” fabricated on a silicon substrate and using through-silicon vias to pass signals from multiple die to the package substrate. 2.5D packages using high-density interposers can be a cost-effective, high-performance alternative to significantly more complex 3D or system-on-chip (SoC) integration schemes. Most estimates project growth for 2.5D/interposer packaging faster than the industry as a whole.

A key enabling technology for interposers has been the development of copper pillar bump technology to provide the high-density interconnection between the interposer and the die. Copper pillar bumps provide a number of advantages over the solder bump technology they are supplanting. They can deliver fine pitches down to 50 $\mu\text{m}$  in-line and 40/80 $\mu\text{m}$  when staggered. They can reduce costs by reducing the number of layers required in the substrate. They provide superior electromigration performance for high-

current carrying capacity applications. They permit electrical test at wafer-level prior to copper pillar bump. They are compatible with bond pad opening/pitch and pad metallization of die designed for wire bond, which enables quick time-to-market for conversion to flip chip.

## Lithography challenges for 2.5D integration

Lithography is a key component of 2.5D integration schemes, however the requirements for interposer exposure systems differ significantly from the requirements of front-end lithography tools. In particular, 2.5D lithography faces specific challenges in regard to resolution, overlay, sidewall angle, exposure field size, depth-of-focus, warped substrate handling and backside alignment.

Current resolution requirements are in the single-digit micron range. The need for sub-micron resolution is not anticipated in the foreseeable future. A suitable lithography systems should offer an N/A of 0.1 to 0.15 in order to meet the line/space (L/S) resolution requirement while also preserving a reasonable depth-of-focus (DOF).

Overlay is a combination of the following: stage accuracy and repeatability; alignment microscope capabilities; translation, rotation and magnification compensation. As a rule of thumb, overlay accuracy should be about one-third of the resolution limit of the optical system. For interposer applications with a resolution limit of 1.5 $\mu\text{m}$ , overlay accuracy should be at least 0.5 $\mu\text{m}$ . Full-field exposure systems, as well as 1x steppers, are typically limited in overlay accuracy, resulting primarily from their use of a double telecentric optical system that prevents them from compensating for magnification errors. A single-sided telecentric lens system combined with a 6-axis reticle positioning system provides complete freedom to adjust for optical errors, including real-time variations, such as those caused by thermal

expansion.

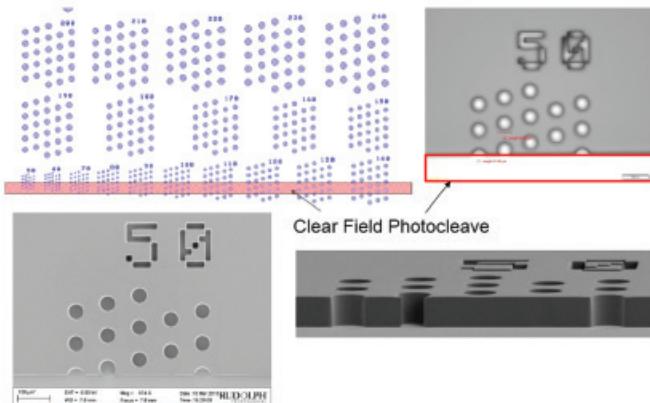
When processing thick photoresist or photo-definable dielectrics, well controlled sidewall angles are a critical requirement, and in some cases, a challenge. Although sidewall angles are primarily a function of the photosensitive material and its processing (pre-bake, post-bake, developing, etc.), the exposure system plays an important role. Accurate focus control across the wafer or substrate is required to achieve tight CD control and consistent sidewall behavior.

One of the most important reasons why sub-micron front-end lithography systems, such as deep-ultraviolet (DUV) steppers and scanners, are not suited for interposer manufacturing is their limited depth-of-focus, a design tradeoff made to obtain the high numerical apertures required to resolve features measured in tens of nanometers. Without a DOF in the 10 $\mu\text{m}$  or greater range, patterning the thick layers used in 2.5D integration is challenging at best.

The exposure field size is yet another important parameter for interposer manufacturing. The size of the exposure field should at least cover the full interposer. Although it is possible to stitch multiple exposures together, stitching is inherently slow and imposes a significant throughput penalty. Although there are no standard interposer sizes, they tend to get larger as they combine and interconnect more chips and passive components.

Interposers have through-via interconnects from the top side to the bottom side. The lithography step to define via locations must be referenced to the other side of the wafer or substrate—so called front-to-back alignment. In the case of silicon, an infrared microscope is required to look through the substrate and see backside features.

Double-side processing causes substantial substrate warpage that front-end lithography systems are not designed to handle. Their limited depth-of-focus adds to this problem. Equipment solutions with warped handling



**Figure 1:** The exposure pattern and the technique of “photocleaving” to provide cross-sectional views of the developed holes. Photo courtesy of TOK.

features, such as switchable and compliant vacuum gaskets on chucks and handlers, are needed for lithography and other processing steps. Equally important is “on-the-fly” focusing that adjusts the wafer position at each exposure to obtain optimal focus.

### Cu pillar bump example

Lithography for copper pillar bumps can be particularly challenging. The pillars are electroplated into openings in a thick layer of photoresist. The exposure system must provide the resolution to create the fine-pitched openings while at the same time delivering sufficient depth-of-field to expose through the full layer, maintaining top and bottom CDs and straight perpendicular side walls.

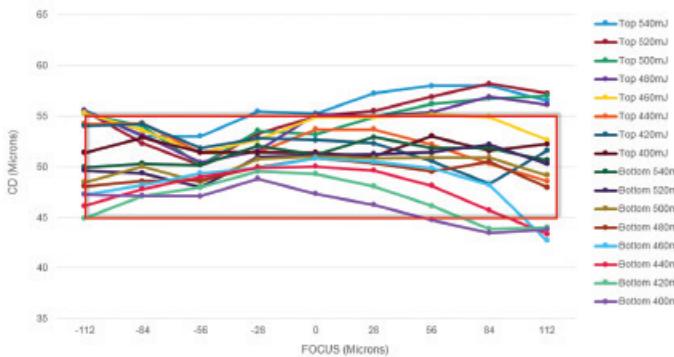
The work described below was performed using a JetStep® lithography system and the latest generation photoresist PMER P-CE5000 from TOK. The photoresist is specifically optimized for this application, offering significant performance advantages when compared to the previous generations, including robust crack resistance, high leach resistance during electroplating, large

single-coat film thickness range, uniform coating thickness over topography, and imaging of vias with high-aspect ratios.

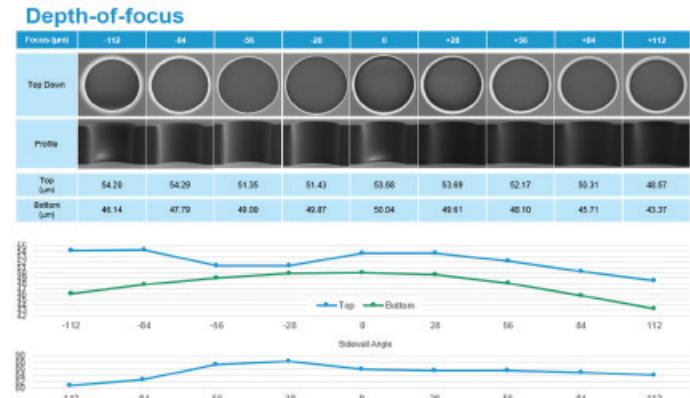
The photoresist film thickness in this example is 50 $\mu\text{m}$ . It was soft-baked for 300 seconds at 145°C, post-exposure baked (PEB) for 180 seconds at 100°C, and developed with TMAH 2.38%, 4 X 60 second puddle. The exposure pattern consisted of groups of holes, with all the holes in each group having the same diameter. Different groups had different diameters, ranging as low as 50 $\mu\text{m}$ . Some holes were “photocleaved” by precisely positioning a slit in the reticle over the holes during an additional exposure step, thereby exposing the side walls for inspection when developed (Figure 1). Focus and exposure were varied to create a classic focus exposure matrix. View the depth-of-focus, process window and exposure field size results in Figures 2-4.

### Summary

We have discussed the dramatic growth in advanced packaging processes, in particular 2.5D processes that use silicon interposer



**Figure 3:** Top and bottom CDs for all exposure values plotted against the process window.



**Figure 2:** Top-down and cross-sectional view of several holes at different focus values with top and bottom diameter. Top and bottom diameters, and sidewall angle are also plotted at the bottom of the figure. Photo courtesy of TOK.

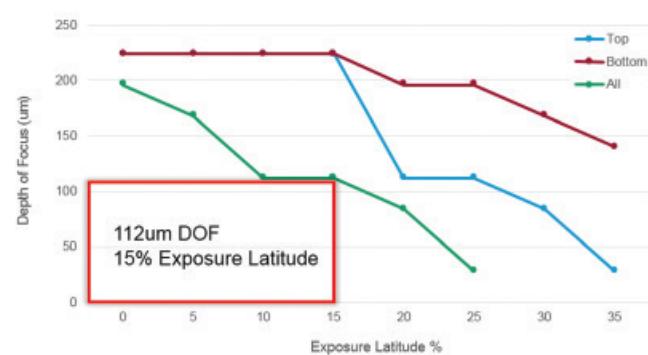
and copper pillar bumps. Although many of the processes used in the process are similar to front-end processes, the differences are significant. Requirements for advanced packaging photolithography were reviewed and we looked at an example of the photolithography process used to define the copper pillars. The example used an exposure tool and photoresist specifically optimized for advanced packaging processes. It demonstrates very good performance and process latitude for both CDs and sidewall angle on a 50 $\mu\text{m}$ -thick film.

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**Figure 4:** The optimal values for both top and bottom are identified as 112 $\mu\text{m}$  DOF and 15% exposure latitude.

# New choices for low-temperature dielectric films

By Robert L. Hubbard [Lambda Technologies, Inc.]

In a recent editorial of this magazine [1], the cost advantages of lower temperature curable polymer dielectrics for wafer-scale packages were pointed out. The material suppliers of the most commonly used polymers, including polyimides (PI), polybenzoxazoles (PBO), and epoxies have been pushed for decades to produce new materials with cure temperatures of 200°C or lower. The dilemma of the chemist is that the customer requirements for product reliability (dielectric, chemical, thermal, and mechanical properties) push the cure temperatures above 300°C. Every degree lower in cure temperature decreases the stress in assemblies between polymer composites, metals, and ceramics with their widely differing coefficients of thermal expansion. Assembly processes could also be simplified with polymer cure temperatures nearer to, or below solder reflow (260°C).

Recent advances have been made in lower temperature versions of PBOs and other materials with cure temperatures at 250°C or below but with some expected trade-offs in adhesion, stress fractures, via shapes, Tg (softening temperature), chemical resistance, outgassing, and process latitudes. The chemical and thermomechanical stability of these films must be retained to provide reliable product quality for increasingly complex final packaging structures. The best solution would be the direct reduction of cure temperatures on existing commercially proven dielectric materials. This would also avoid requalification cost and delays for new chemical materials.

## What does “cured” mean?

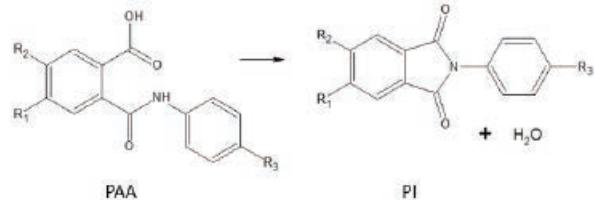
There is some confusion about what constitutes a “cured” dielectric film. In the case of the early polyimides, the completeness of the cyclization reaction of the polyamic acid (PAA) to the thermoplastic PI structure was the simple answer (**Figure 1**). With the need to increase the Tg of PBO films, the cure now includes both cyclization and cross-linking reactions as an example shows in **Figure 2**. The cyclization reaction is more important for dielectric properties and chemical resistance while the cross-linking is more important for thermomechanical stability. Yet another reaction in photosensitive materials is the removal of the photosensitizer by-products left in the films. For epoxies, there is generally only cross-linking, which has its own complications.

Just to make this all the more challenging, the cure processes have a direct effect on the film adhesion and the shape of vias. Despite the new complexity of the word “cure,” a film is often judged by just one measurement, say Tg, percent solvent retention, or cyclization (by Fourier transform infrared [FTIR] spectroscopy). It is best to have a more complete understanding of the relevant set of property measurements suitable to the application.

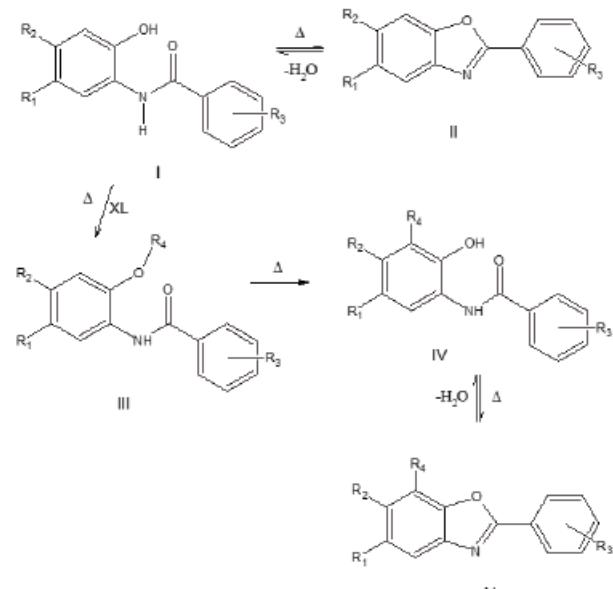
## Variable frequency microwaves

The first thought of microwaves is usually speed, followed by arcing and nonuniformity. When variable frequency microwave (VFM) technology was developed two decades ago, the arcing and uniformity issues were solved as evidenced by hundreds of production systems currently in use for electronics production worldwide. The surprise benefit was the significant reduction in cure temperature of most chemical reactions. The unique heating mechanism of microwaves involves the dielectric relaxation to rotation of dipoles in molecules, such as the rotating carbonyl drawn in **Figure 3**, rather than the simple collisions of whole molecules from conventional heating. A resulting cure temperature reduction of 50-150°C is accompanied by a cure cycle time of 2-10 times shorter. The higher collision frequency (Z) and steric factor ( $\rho$ ) in the collision-modified Arrhenius equation (**Eq. 1**) predict the high reaction rates and the low reaction temperatures with microwaves.

$$k = Z \rho e^{-\frac{E_a}{RT}} \quad (\text{Eq. 1})$$



**Figure 1:** Cyclization reaction of PI cure.

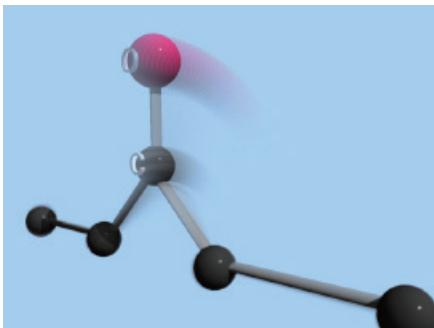


**Figure 2:** Cross-linking and cyclization during PBO cure.

The effectiveness of the microwave absorption depends directly on the polarizability of the reactants. This also explains the selective heating of just the uncured sample and not the air, chamber, or fixtures. The two-meter penetration depth combined with very fast sweep frequencies explain the high field uniformity and resultant lower cure stresses in all axes with VFM.

## Lowered cure temperature curing of PI and PBO

A recent comparison [2] was made between the standard 5 hour, 375°C curing cycle of the HDM photosensitive polyimide precursor HD4100 and a matrix of VFM cures of 1-3 hour cycles at 230°C - 270°C. The essentially identical film property ranges are shown in



**Figure 3:** Dipole rotation heating mechanism of microwaves.

**Figure 4.** This photosensitive PI precursor is an example of cyclization cure. As an example of the speed of the VFM process, it was previously reported [3] that the same HD4100 could be cured with identical film properties at 350° in only five minutes. Another polyimide precursor, PI 2611 (HDM), produces a unique PI film with a coefficient of thermal expansion (CTE) of only 5 ppm/ $^{\circ}$ C to match that of silicon. VFM cure of PI 2611 has been reported at 200°C with a CTE of 3 ppm/ $^{\circ}$ C [4].

The more complex “cure” of a conventional low-temperature PBO was studied to determine the relative contributions, or even competition,

between cyclization and cross-linking as portrayed in **Figure 2**. Comparisons were made using a time at the highest soak temperature of 30 minutes for both oven and VFM as depicted in **Figure 5**. The cyclization (**Figure 6**) by oven cure is only 70% complete at 200°C even if the soak time is increased to 60 minutes. It can be seen that VFM achieves a 96% cyclization by 200°C with the 30 minute soak. The cyclization with VFM cannot be said to significantly increase between 200°C and 250°C considering measurement error at this level. The extent of cyclization in both cases is directly measured with FTIR by comparing the decrease in the amide peak of the starting material to a phenyl absorption that is a constant reference.

The cross-link reaction is more complex, and might better be considered mostly a chain-extension process. For several reasons, the extent of cross-linking was measured by FTIR as an adjusted ratio of the decrease of the cross-linker to the phenyl reference absorption as shown in **Figure 7**. Cross-linking in the oven appears to increase steadily up to 250°C, whereas the VFM cured samples increased to more than twice that level by 200°C and leveled off. It appears that even though the cyclization is essentially complete at 200°C by VFM, the chains are getting longer at the same rate and are also finished at 200°C. The potential “competition”

between cyclization and cross-linking as suggested in **Figure 2** may not be as significant with the VFM cure process. All of this data refers to a 30-minute soak, so it would be interesting to see if these reactions would both be completed with VFM at temperatures below 200°C with longer soak times.

### Epoxies are a very different matter

The term “epoxy” is often used when referring to other highly cross-linked thermosets like polyhydroxystyrenes and novolacs as well as mixtures with a percentage of epoxides added. There are two basic components to an “epoxy” mixture, including an epoxide resin and a “curing agent” or “hardener,”

which could be an amine, anhydride, or phenol. The important feature is that the starting materials are monomers (or short ionomers) that react with each other to make a highly cross-linked product resembling a chain link fence. As dielectric films, the “epoxies” have much higher moduli (harder) and much lower elongation to break than the long chain PI and PBO films. They are also less expensive and lower in cure temperature and Tg. Often they incorporate elastomers or elastomer fillers to improve their stress properties, and silica filler to improve CTE values. With Tg values of 100-150°C and cure temperatures of 150-250°C, they fill the need for temperature-sensitive processes with a trade-off of thermal, chemical and mechanical stability.

It is important to understand the term “cure” again here. As the two components react to form links, there is a point in time (and temperature) that they become substantially rigid, called gelation. At this point, there is so much chemical rigidity that further reactions between unreacted components and between chains that the rate of cure drops rapidly and finally stops. A “fully cured” thermoset may only be 50% reacted, but there is not enough mobility either between chains or agglomerations that no further reactions can take place at that temperature. Measurement of the Tg at this point is a maximum and is referred to as “ultimate” (Tg $\infty$ ). Only by raising the cure

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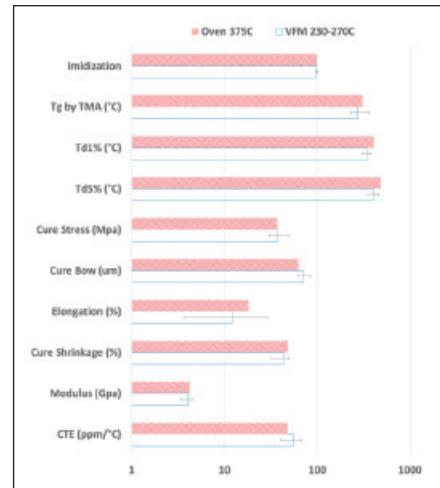
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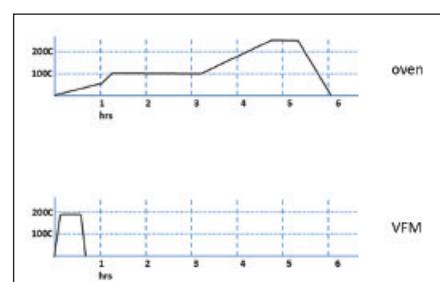
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**Figure 4:** Film property comparison of oven and VFM cure of PI (HD4100).



**Figure 5:** Cure process profiles for oven and VFM cure of a PBO.

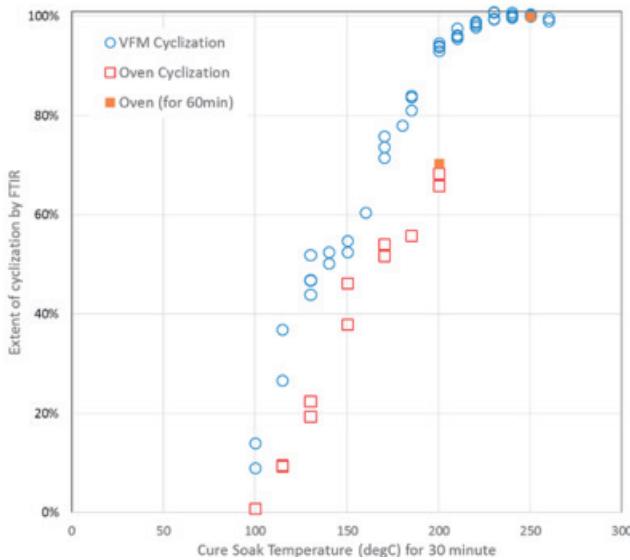


Figure 6: Cyclization of a PBO with oven and VFM curing to 250°C.

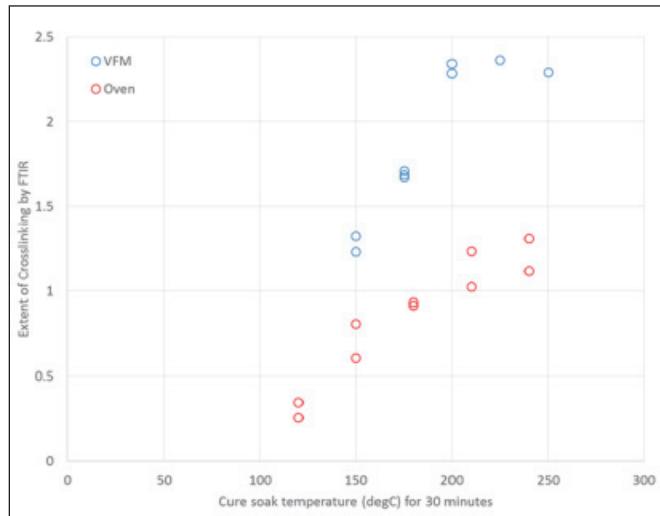


Figure 7: Cross-linking of a PBO with oven and VFM curing to 250°C.

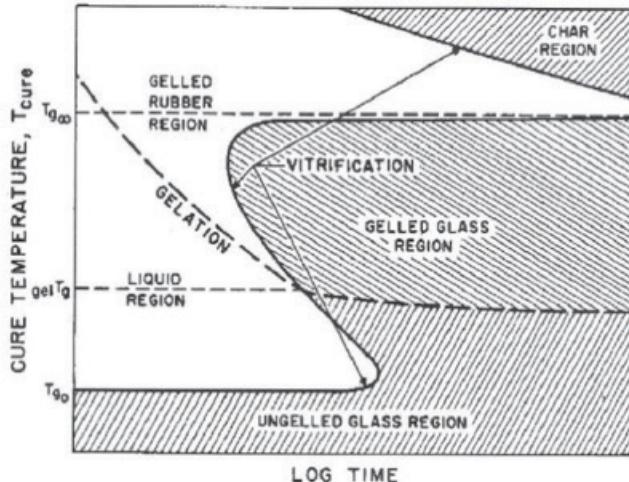


Figure 8: Phase diagram of thermoset curing.

temperature could the  $T_{g\infty}$  be increased, but at the risk of decomposition. The cure temperature of thermosets is therefore always chosen higher than the  $T_{g\infty}$ . This is important because if the film is not fully cured, but is taken to a higher temperature later, for example at solder reflow, the  $T_{g\infty}$  will change and the film properties will change. If the cure temperature is chosen below the  $T_{g\infty}$ , the material will return to a glassy solid (vitrify). At this point, the rate of cure drops by 2-3 orders of magnitude (stops) as shown by the grey area in Figure 8 [5]. Another reason to set the cure temperature above  $T_{g\infty}$  is to accomplish adhesion at all surfaces. All of this is important to understand to avoid failures or hidden problems in assemblies with multiple heating steps.

With this background, it should be very surprising to read recent articles about VFM curing of epoxy underfills. At ECTC-2010 this author produced data showing epoxy underfill curing with VFM at cure temperatures well below the  $T_{g\infty}$  with lowered warpage, lowered modulus, and full cure ( $T_{g\infty}$ ) [6]. With careful DOEs (statistically designed experiments), and two different underfill chemistries (Henkel FP4527 and UF 8830) it was shown that cure temperatures of 85°C could replace the standard cure temperature of 165°C and produce 20%-88% lower warpage of substrates and dice. The storage modulus ( $\epsilon'$  below  $T_g$ ) of UF 8830 with VFM was 3X lower than the oven cure at 165°C, which indicates a 3X lower cross-link density (3X longer chain lengths). Later publications confirmed that Namics and ShinEtsu underfills performed similarly. IBM followed in 2013 [7] with a comparison of three underfills cured with oven and VFM to find 22% lower warpage and twice the reliability of a microprocessor package. Their cure was at 110°C rather than 165°C, and the modulus was reduced by 30%. They attributed the lowered warpage and increased reliability to the lower VFM cure temperature and the reduction in modulus.

The relationship of stress to cure temperature of thermosets can be seen in Figure 9 where the shrinkage in the solid state (from gelation back to room temperature) is directly proportional to that temperature difference [8]. Now

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the VFM cure temperature can be lowered without vitrification and leaving incomplete cure. At lower cure temperatures, several commercial epoxy adhesives have been VFM-cured and shown to have significantly lower cross-link density (modulus).

The use of VFM curing on three JSR epoxy-based dielectric films was shown [9] to reduce cure temperature from 250°C to 160°C with a reduction in wafer bow of 50%. The equivalent extent of cure was measured by the resistance to absorption of NMP solvent at 40°C.

The exact mechanism for these effects in thermosets is under investigation, although the same results (lowered cure temperature and modulus) have even been found for ethylene-vinyl acetate rubbers, which involves a very different radical-based reaction mechanism.

## Summary

A promising cost-effective method of reducing the cost of curing polymer dielectrics would be to change the method of cure rather than changing (and qualifying) new chemistries. Even more effective would be if the lower cure temperatures could be performed with shorter cycle times. It would be better still if the film properties were at least as good, and even better with regard to stress and warpage. With the use of variable frequency microwave technology, the cure temperatures of PI, PBO, and epoxy-based dielectric films can be significantly reduced, in shorter cure cycles, while achieving the same extent of cure. The unique heating mechanism of microwaves produces equivalent cyclization and cross-linking of these polymers, as well as assuring the same chemical and thermomechanical stability as the standard oven cure at higher temperatures. For cross-linked thermosets like epoxies, not only is vitrification avoided at low cure temperatures, but lower modulus and lower cross-link density is produced.

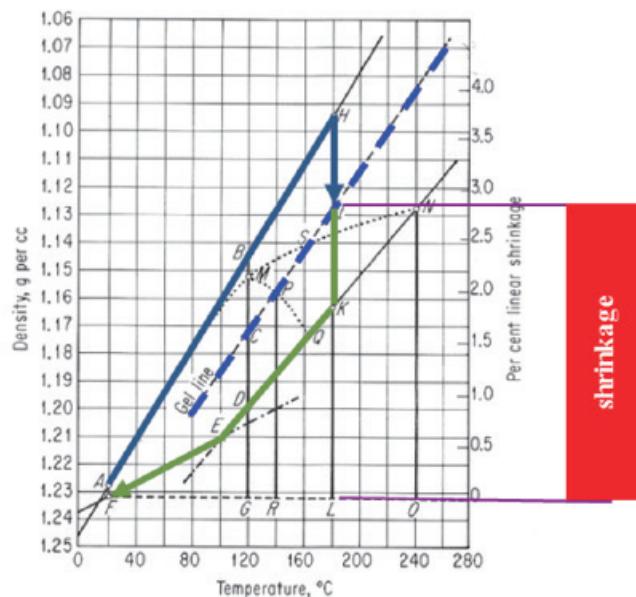


Figure 9: Comparison in epoxy shrinkage between two cure temperatures.

VFM technology is used for production microelectronics processing already and is now moving to high-volume production at the wafer scale.

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## Biography

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(continued from page 36)

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<b>Amkor Technology</b> <a href="http://www.amkor.com">www.amkor.com</a> .....	1
<b>Aries Electronics</b> <a href="http://www.arieselec.com">www.arieselec.com</a> .....	48
<b>DL Technology</b> <a href="http://www.dltechnology.com">www.dltechnology.com</a> .....	29
<b>Ellsworth Adhesives</b> <a href="http://www.ellsworth.com">www.ellsworth.com</a> .....	53
<b>E-tec Interconnect</b> <a href="http://www.e-tec.com">www.e-tec.com</a> .....	3
<b>Emulation Technology</b> <a href="http://www.emulation.com">www.emulation.com</a> .....	24
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<b>Indium Corporation</b> <a href="http://www.indium.us/E042">www.indium.us/E042</a> .....	31
<b>IPG Photonics</b> <a href="http://www.ipgphotonics.com/IX280MLCSR">www.ipgphotonics.com/IX280MLCSR</a> .....	17
<b>Ironwood Electronics</b> <a href="http://www.ironwoodelectronics.com">www.ironwoodelectronics.com</a> .....	47
<b>JCET</b> <a href="http://www.cj-elec.com">www.cj-elec.com</a> .....	9
<b>Johnstech</b> <a href="http://www.johnstech.com/criticaltest">www.johnstech.com/criticaltest</a> .....	IBC
<b>Lambda Technologies</b> <a href="http://www.microcure.com">www.microcure.com</a> .....	34
<b>Leeno</b> <a href="http://www.leeno.com">www.leeno.com</a> .....	2
<b>Mi Equipment</b> <a href="http://www.mi-eq.com">www.mi-eq.com</a> .....	14
<b>MRSI Systems</b> <a href="http://www.mrsisystems.com">www.mrsisystems.com</a> .....	19
<b>Micro Control Company</b> <a href="http://www.microcontrol.com">www.microcontrol.com</a> .....	39
<b>NANIUM</b> <a href="http://www.nanium.com">www.nanium.com</a> .....	43
<b>Nordson DAGE</b> <a href="http://www.nordsondage.com/4000plus">www.nordsondage.com/4000plus</a> .....	11
<b>PacTech</b> <a href="http://www.pactech.de">www.pactech.de</a> .....	45
<b>Plasma Etch</b> <a href="http://www.plasmaetch.com">www.plasmaetch.com</a> .....	52
<b>Plastronics</b> <a href="http://www.plastronics.com">www.plastronics.com</a> .....	23
<b>R&amp;D Altanova</b> <a href="http://www.rdalanova.com">www.rdalanova.com</a> .....	28
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<b>Teikoku Taping System, Inc.</b> <a href="http://www.teikoku-taping/en">www.teikoku-taping/en</a> .....	54
<b>Yokowo America Corporation</b> <a href="http://www.yokowo.com">www.yokowo.com</a> .....	36

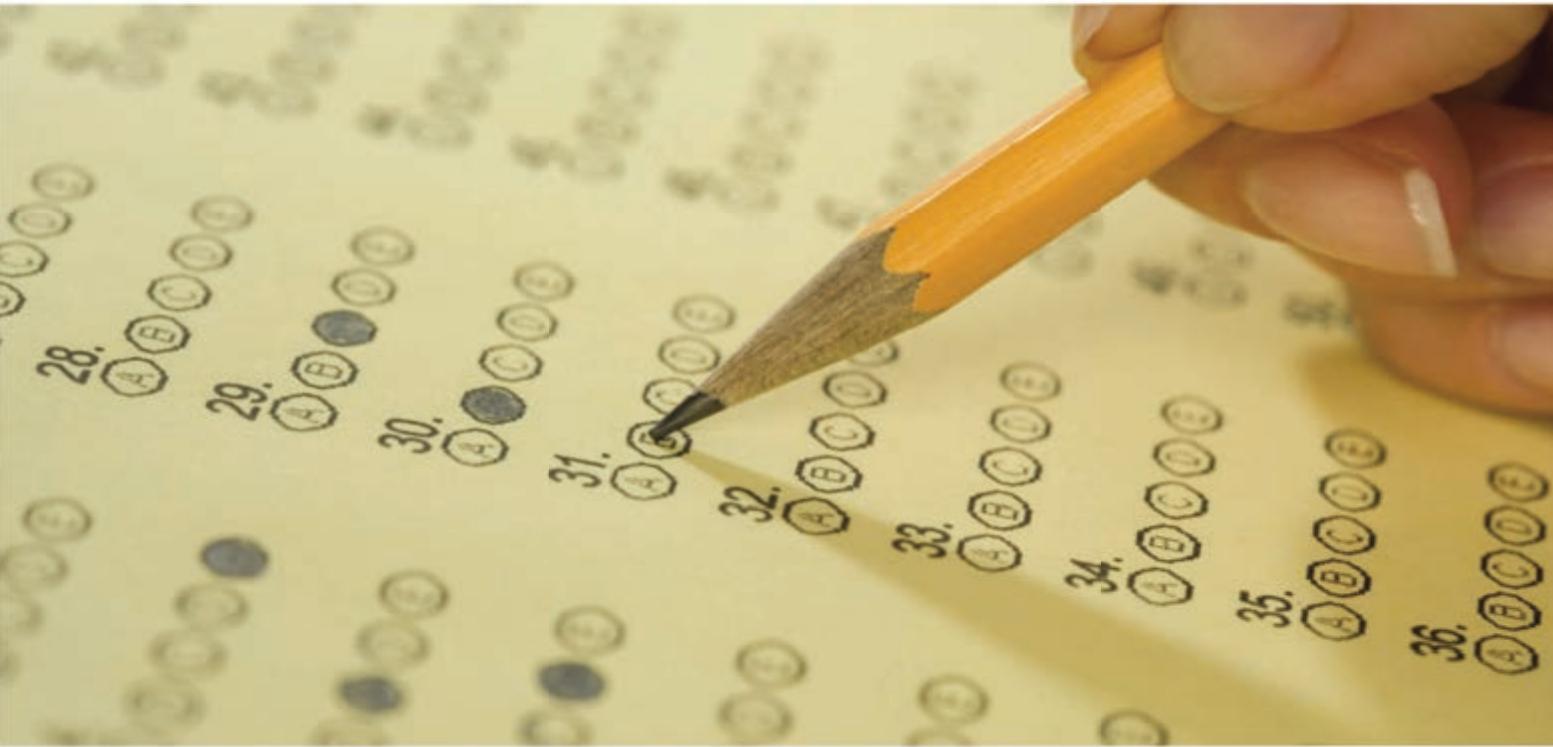
**November December 2015**

Space Close October 10 | Materials Close October 16

**For Advertising Inquiries | [ads@chipscalereview.com](mailto:ads@chipscalereview.com)**

# When it comes to semiconductor test, it is either pass or fail.

There is no room for error.



## Increasing demands. Increased risk.

The increasing design complexities of semiconductor devices continuously demand innovative process nodes that tend to increase the uncertainties of test engineering: controllability and observability.

For example; connectivity and automotive safety devices are now in the mm-wave operating regimes that were once limited to the specialized and low volume defense sector.



*The cost for undetected failure in test  
is accumulated x10 for every stage\**

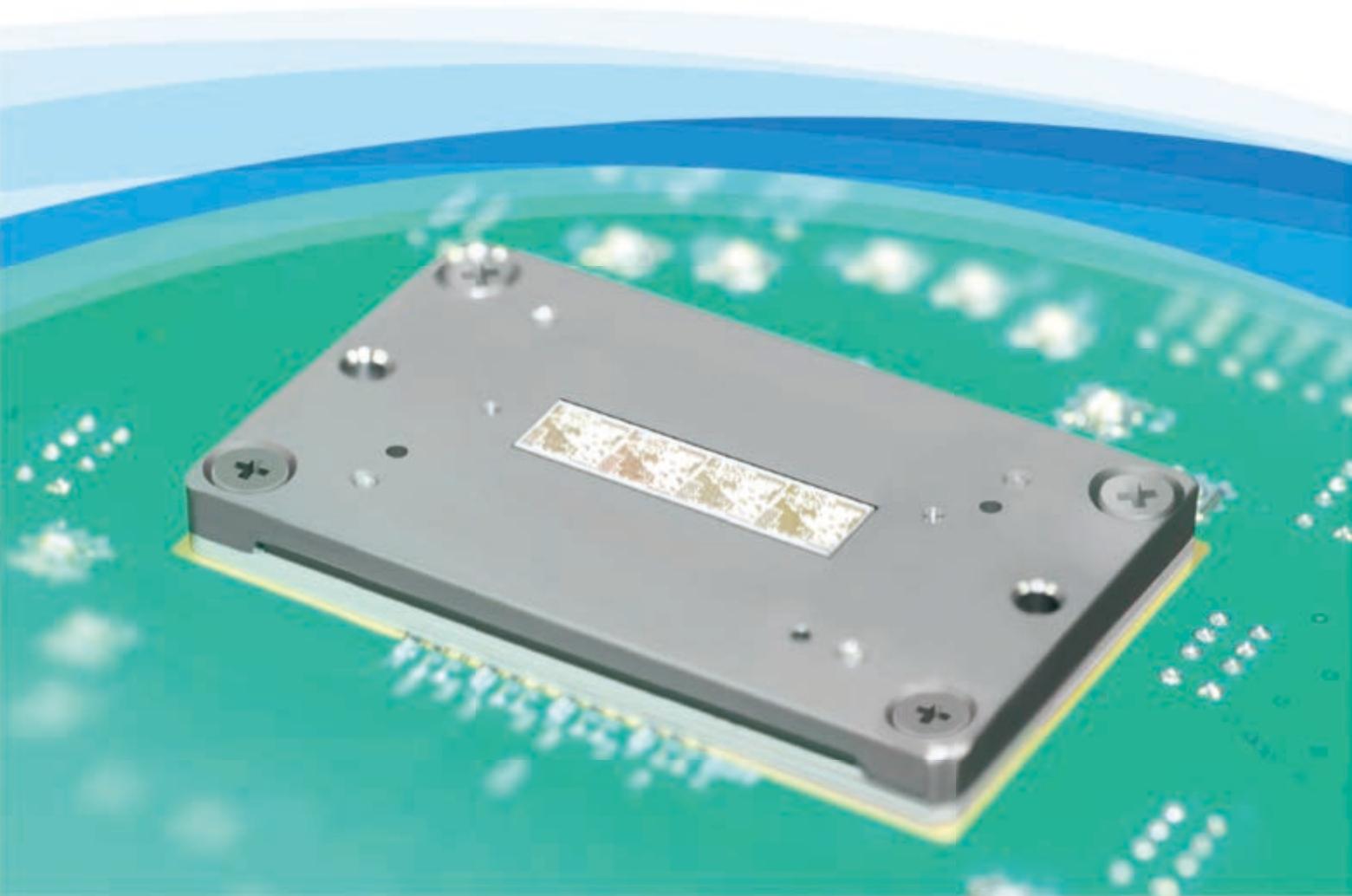
Today, test engineers and test hardware providers face the uncertainty of providing mass production at-speed test solutions for these mm-wave devices that, within a year, will soon be widely implemented in end-products.

Be prepared and manage the uncertainty.

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# smiths connectors



## The Monet Solution

*Delivering robust performance to 200 µm pitch*

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Driven by the market need for finer pitches, Smiths Connectors, the world leader in spring contact probe technology, has developed the patented Monet series of probe heads for WLCSPs. Monet's innovative designs combines all of the conventional advantages of spring probe technology with robust performance on pitches as fine as 200 µm.