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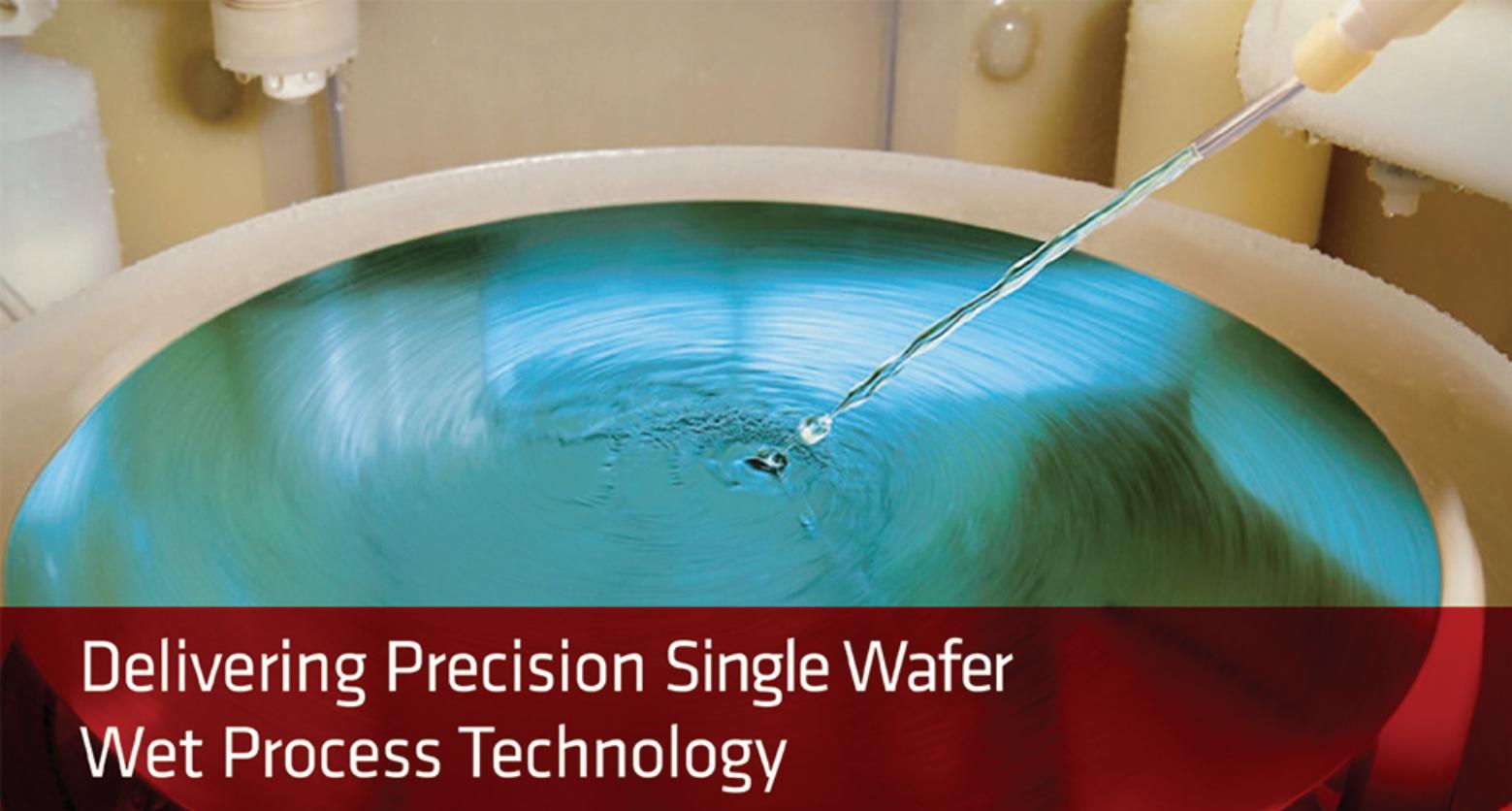
Volume 22, Number 1

January • February 2018

## Challenges of ECD panel FO in HVM

Page 9

- 3D bump inspection
- Laser debonding for WLP
- Reducing wafer test time
- Sensors for automotive apps
- 3D IC heterogeneous integration by FOWLP
- Surface analysis as a “blueprint” for manufacturing



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Flux Clean	✓			
PERR		✓	✓	✓



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# CONTENTS

January • February 2018  
Volume 22, Number 1



A 300mm wafer and a 510 x 515mm panel are about to be electroplated for packaging. Electroplating at the panel scale is no longer a barrier for form factor adoption in packaging. Tokyo Electron has partnered with customers to develop cutting-edge processing equipment, such as the StratusTM P300 and P500 that can process the substrates shown to create fine packaging features at superior uniformities.

Cover photo courtesy of Tokyo Electron.

## DEPARTMENTS

Technology Trends	Fan-out panel-level packaging proceeds apace, regardless of standards Paul Werbaneth <i>Intevac, Inc.</i>	5
Guest Editorial	Trends in test Ira Feldman <i>Feldman Engineering Corp.</i>	7

## FEATURE ARTICLES

Challenges of ECD panel fan-out in high volume and potential solutions Jon Hander, Demetrius Papapanayiotou, Robert Moon, Arthur Keigler, Michelle Schulberg, Mani Sobhian, Bryce Chen, Tyler Barbera, Cristina Chu <i>TEL Advanced Packaging</i>	9
3D IC heterogeneous integration by FOWLP John H. Lau <i>ASM Pacific Technology Ltd.</i>	16

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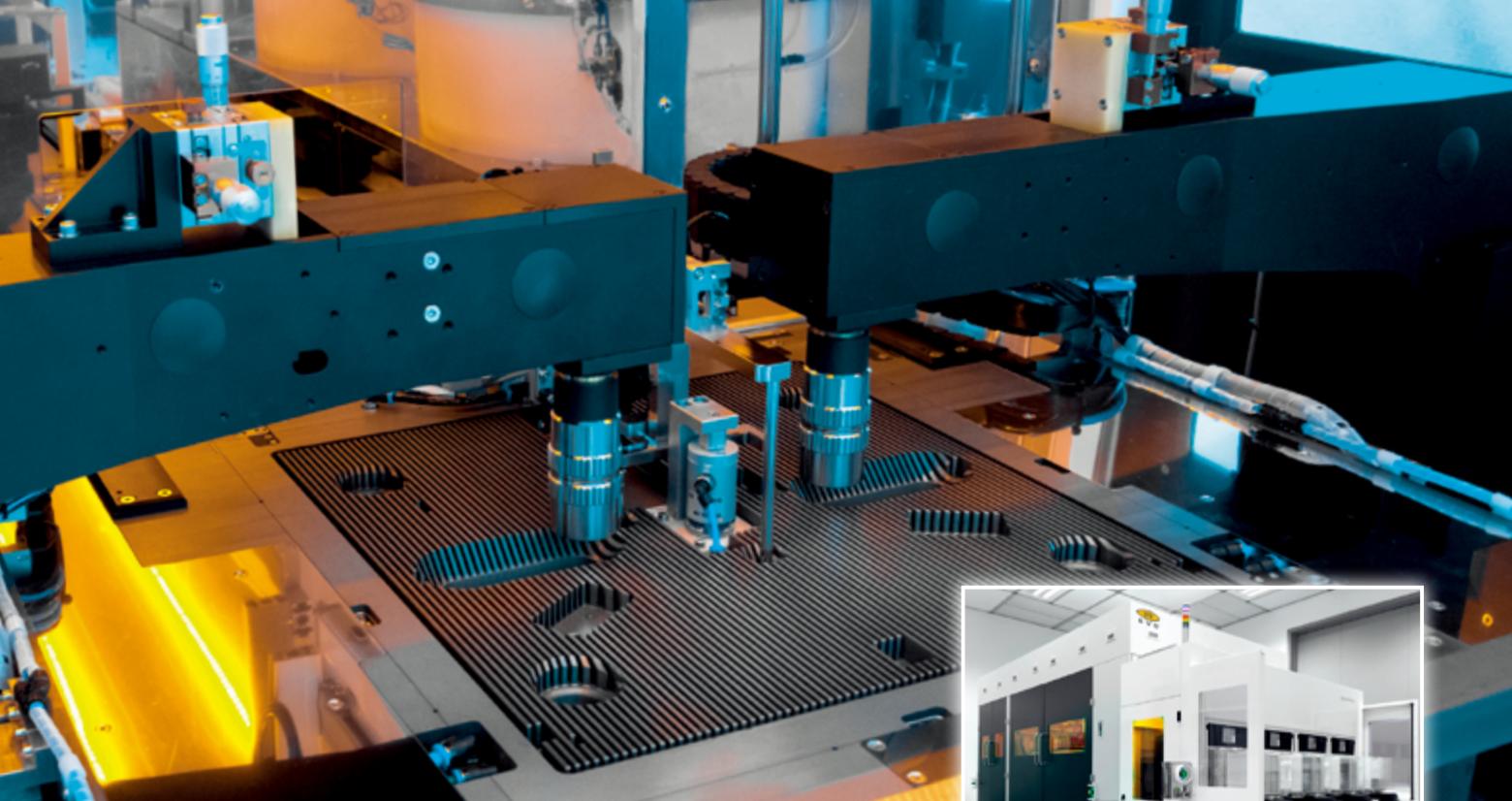
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## FEATURE ARTICLES *(continued)*

### Laser debonding processes enable wafer-level packaging advances

Thomas Uhrmann, Boris Považay, Mathias Pichler, Florian Schmidseder, Daniel Burgstaller *EV Group*

23

### Surface analysis as a "blueprint" for semiconductor package manufacturing

Jaimal Williamson *Texas Instruments*

28

### Total control of the bump process to ensure reliability of stacked devices

Matt Wilson *Rudolph Technologies, Inc.*

32

### Reducing wafer test time

Klemens Reitinger *ERS electronic GmbH*

36

### The "More than Moore" semiconductor industry is changing the transportation paradigm

Jérôme Azémar, Guillaume Girardin, Yohann Tschudi *Yole Développement*

39

### Epoxy adhesives: mechanical versatility by design

Jonathan Knotts, Daniel Morgan *Creative Materials, Inc.*

43

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## Fan-out panel-level packaging proceeds apace, regardless of standards

By Paul Werbaneth *[Intevac, Inc.]*

**T**here is compelling historical evidence for the notion that industries of various persuasions enjoy greater success in aggregate, as industries, once they have converged around common sets of standards, than they did when acting as ecosystems comprising disjointed players. The fan-out panel-level packaging (FOPLP) industry should be no different.

Alissa Fitzgerald, PhD, of A.M. Fitzgerald & Associates, in her talk on “The Business Case for MEMS Standardization” from SEMICON West 2015, gave several examples of industries that have benefitted from standardization over the last 150 years, including the steam boiler/pressure vessel industry, the aircraft industry, and the aerospace industry [1]. Fitzgerald proposed that, once accepted standards come into being, standards have positive benefits in many areas important to commerce, including these: interchangeability of components (improved); public safety (better); communication of essential information across language and cultural gaps (smoother); and overall market efficiencies (enhanced).

SEMI, the industry organization we often think of only in terms of its highly visible public face, namely its calendar of trade shows and conferences, has another function—the setting and keeping current semiconductor manufacturing standards. These activities have done as much to ensure the semiconductor manufacturing industry’s vibrant success than just about any other single factor of consequence contributed since the time of our industry’s beginning. According to SEMI, “Standards increase industry efficiency by reducing/eliminating duplication of efforts, defining new markets, and promoting competition by lowering barriers to entry [2].” And the proof is all around us.

Attendees and participants at recent and upcoming conferences devoted to semiconductor device packaging are

hearing more and more about the success fan-out wafer-level packaging (FOWLP) has achieved to date. There are forecasts for a rosy future in a variety of applications, including further inroads into smartphones and wearables, increased traction in automotive applications, and fan-out’s suitability for 5G communication when that rollout occurs. From a manufacturing perspective, FOWLP lives pretty much in a post-standardization world. Wafer dimensions are fixed, and a capital equipment supply chain, for example photolithography tools, coating systems, and the like, is already up and running to serve the packaging houses that provide commercial fan-out packaging services.

For those following FOPLP, however, it’s a different story. It’s a pre-standards world. FOPLP, of course, enjoys the benefit of a running start because the basic process flow(s) for it already exists – FOPLP will be die-first, or die-last; there will be mold compound molding; there will be wafer stepper stepping, and PVD sputtering, and electroplating plating; and there will be reconstituted panel singulation, and the singulated fan-out die will ship to customers, just as in FOWLP today. The quandary though for FOPLP is that, unlike FOWLP and its standardized 300mm round wafer, panel-level packaging is still considering its options when it comes to a standard panel size. This situation is creating market inefficiencies, real or imagined.

Nonetheless, panel-level packaging proceeds apace. Among the proposed or actual panel sizes you will observe in the FOPLP wild are: 320mm x 320mm; 510mm x 410mm; 300mm x 300mm; 610mm x 456mm; and others [3]. FOPLP is racing to market even without a body of standards covering details as basic as the size of panels. This leaves the FOPLP supply chain in a bit of a quandary. Very often, it is the first mover who ends up defining industry standards, if only because the first mover moved first. However, if the “tells” aren’t

clear, from a capital equipment supplier’s perspective, on which of the first, or early, movers is it best to place development bets?

Between FOWLP and FOPLP the choice could be, “From an architecture standpoint, it’s probably a piece of equipment that addresses the wafer format applications...And then, it’s another piece of equipment that is panel directed. If an equipment vendor is doing what’s right for their customers, you would try and make it as universal as possible, so you could do multiple applications in the same platform [4].” But why even make separate process tools for FOWLP and FOPLP, or, within FOPLP, tools that work for only one panel size?

As heard recently during its talk at SEMICON Japan 2017, Shibaura Mechatronics, maker of automated die bonders, spoke of bonding die to panels of various sizes, without discrimination, following the lead of each of the three FOPLP “launch” customers (identified as Deca Technologies, “Original1” and “Original2”) whom Shibaura is following.

Lithography tool suppliers are of a similar mind regarding panels. For example, Rudolph Technologies supplies a 2X reduction stepper capable of producing photo patterns on square or rectangular panel sizes up to and including 650mm x 720mm, the format known as Gen 3.5 in the LCD industry, a cousin of sorts to panel-level packaging.

From the perspective of materials suppliers, for example Nagase ChemteX, also heard from during the recent SEMICON Japan series of technology seminars, the liquid molding compound (epoxy mold compound, or EMC) used for wafer-level fan-out packaging is the same as used in panel-level, any size panel, with perhaps some additional dispense optimization required to accommodate relatively larger substrates.

At Intevac, Inc., our thinking is that for the PVD steps that create the barrier/seed

layers in fan-out packaging upon which redistribution layers (RDLs) are formed, why not just use a carrier-based linear transport PVD system that works for both 300mm round (and larger) fan-out wafers and for fan-out panels too? Even for panels up to and including sizes like 600mm x 600mm square, exemplifying, at least in the PVD tool space, the spirit of “Equipment as universal as possible, doing multiple applications in the same platform [4].”

Having a standard panel size, in the case of Shibaura, Rudolph, Nagase, or Intevac, would make life easier perhaps in general, but even lacking standards as yet, this part of the FOPLP supply chain is proceeding apace. In parallel, recognizing the importance of, and the need for, standardization in the FOPLP industry, SEMI began a new effort, in November 2017, to just such effect. SEMI recognizes that FOPLP technology has the potential to significantly improve manufacturing efficiencies and reduce

costs. However, the wide range of substrate sizes and form factors is hampering widespread implementation of FOPLP in semiconductors.

According to James Amano, Senior Director, International Standards at SEMI, “SEMI recently surveyed the industry, and a strong majority of respondents were in favor of developing a standard substrate specification, and work is now underway in the newly-formed Fan-Out Panel Level Packaging (FOPLP) Panel Task Force.” At SEMI’s 3D Packaging & Integration (3DP&I) North America Technical Committee Chapter Meeting, held on November 7, 2017, the committee approved the formation of a new task force to develop standards for the panels used for FOPLP, with initial focus on panel dimensions. The Task Force will also consider other parameters suggested by the wider community as being appropriate for standardization. Expect more to come.

In the meantime, Intevac has developed sputter deposition processes for barrier/seed layer applications in the fan-out packaging market using our carrier-based linear transport PVD system, and demonstrated successful PVD results on both 300mm round wafers and on 600mm x 600mm glass panels, changing only the transport carriers used to hold the material – no in-vacuum changes were performed, nor were they required. Other members of the FOPLP supply chain have made similar progress for the other unit operations, or materials, used in panel-level packaging. Work by these first movers in FOPLP may end up defining industry standards, or not, but we’re likely making progress on the improved interchangeability of components, smoother communication of essential information across language and cultural gaps, and enhanced overall market efficiencies that are surely coming, indeed are inevitable, for panel-level packaging. But even before the standards are complete, fan-out panel-level packaging proceeds apace.

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### Biography

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# GUEST EDITORIAL



## Trends in test

By Ira Feldman [[Feldman Engineering Corp.](#)]

**T**est: the necessary evil! From the early days of vacuum tube logic, test has been an essential activity performed under intense cost pressure. Meanwhile, product- and technology-specific test requirements have continuously changed, forcing the development of new test methodologies and operational approaches. It is important to understand recent and potential future changes to make sure the right test solutions are available. The wrong approach or technology can doom the success of any product. Test quality, cost, and time-to-market need to be balanced to ensure smooth product validation, debug, product ramp, and on-going product quality.

While electronic test basics have remained the same, its application has changed. Test is based upon a stimulus and response model. Electrical stimulus – i.e., an arbitrary electrical signal – is presented to a device under test (DUT) such as a packaged semiconductor or die on a wafer in a repeatable fashion. The response of the DUT is then measured and compared to the expected value to determine pass or fail.

The rapid rise in non-electrical stimulus testing illustrates the magnitude of test technology changes. As smartphone sales grew exponentially, an entire market of microelectromechanical systems (MEMS) sensors was born. These MEMS devices, such as accelerometers, gyroscopes, compasses, and microphones, are all tested using non-electrical stimuli including motion, rotation, magnetic fields, sound waves, etc. Each sensor (DUT) converts the stimuli into an electrical signal, which is then measured for correctness. Specialized automatic test equipment (ATE) and material handling was developed or adopted for these devices but the fundamentals of test remained the same.

The explosion in data generation and consumption by personal mobile devices drove the development of mega data centers and the unsatisfied desire for increased bandwidth. In response, high-speed fiber-optic data connections were brought to market with ever faster

optical transceivers in development. These transceivers and their components are tested using light-based stimulus and response. Eventually, the light is converted back to/from electrical signals. Hence, the test fundamentals remain the same regardless of the signal domain.

More recent statistical-based approaches have significantly altered test operations. Many devices have changed from 100% test to sampling methods, adaptive testing to dynamically select tests, and inferring device quality based upon “neighbors,” among other approaches. Burn-in (temperature-controlled accelerated testing) quickly moved to sampling or outright elimination for many classes of parts significantly reducing total test time and cost. What is notable is that recently, more sophisticated 100% burn-in has “returned” for some devices in high-reliability applications, such as automotive.

New test technologies are often developed to support new package types. Wafer-level chip-scale packaging (WLCSP) has disrupted the market to achieve extremely small package sizes and higher performance with significantly lower packaging costs. Beyond the challenges of shrinking connection (pad, ball, bump) pitch, test solutions for WLCSP have similarly disrupted the test consumables industry. The dominant WLCSP solution is now spring-pin based “contactors” deployed in wafer probe by traditional socket companies. And several alternative handlers such as test-in-tray and strip have been introduced to further address quality and cost issues. It will be exciting to see how these solutions change as panel-level processing (PLP) demand grows.

Recently, system-level test (SLT) has been developed for ultra-high-performance devices that cannot be cost-effectively tested on traditional ATE. SLT is also being used for at-speed subsystem testing for system-in-package (SiP) devices and memory/processor package-on-package (PoP) stacks. These and other new test solutions will need to address the exploding number

of semiconductor devices driven by the increase in electronic products and greater “silicon” content per product.

Current wireless test challenges include everything from ultra-low-cost ultra-high-volume Internet of Things (IoT) devices to millimeter wave devices (77 GHz and above) for 5G mobile connectivity and automotive radar. These applications are in their infancy with many additional challenges ahead as production volumes increase.

Test engineering is a “practical art.” Roadmaps like the International Technology Roadmap for Semiconductors (ITRS) and its successor, the Heterogeneous Integration Roadmap (HIR), are great at identifying the trends and high-level requirements. Academic papers and internet research are good for theory. However, a test engineer requires solutions that are an exact fit for a specific product. And suppliers need to cost-effectively provide the right hardware – capital equipment (ATE, handlers, wafer probers, burn-in chambers, etc.), consumables (sockets, contactors, load boards, wafer probe cards, etc.), and services. A great way to gain practical knowledge is to attend a test-focused event such as the Burn-in & Test Strategies Workshop (BiTS 2018) March 4-7 in Mesa, Arizona. BiTS provides a casual environment in which one can learn how others have solved emerging problems, network with colleagues, and meet vendors for hands-on discussions of your organization’s test challenges.

*As Publication Sponsor of BiTS, Chip Scale Review has arranged a \$50 discount on Professional Registration using code “CSR50” at <https://bitsworkshop.org/register>.*

### Biography

Ira Feldman earned BS and Master of Engineering degrees from Harvey Mudd College. He is a principal consultant at Feldman Engineering Corp. and supports clients with technical marketing and product generation processes. Mr. Feldman is the General Chair of the Burn-in & Test Strategies (BiTS) Workshop; email [ira@feldmanengineering.com](mailto:ira@feldmanengineering.com)

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# Challenges of ECD panel fan-out in high volume and potential solutions

By Jon Hander, Demetrius Papapanayiotou, Robert Moon, Arthur Keigler, Michelle Schulberg, Mani Sobhian, Bryce Chen, Tyler Barbera, Cristina Chu /TEL Advanced Packaging

Multi-chip packages using fan-out assembly techniques continue to approach the size and performance offered by heterogeneous through-silicon vias (TSVs) at a fraction of the cost. The electronics industry has historically delivered cost reductions, as well as performance improvements at a steady pace, and manufacturers are still striving to supply lower prices for 300mm wafer-based fan-out substrates than are currently available. This situation has slowed the adoption of fan-out technology in high-volume commercial products such as mobile devices, processors, and memory. Migration from 300mm wafer substrates to larger 510 x 515mm panel substrates could deliver the cost-down required for high-volume adoption of fan-out technologies, but the technical challenges associated would have to be overcome.

When plated Cu feature sizes shrink, thinner seed layers are required to electroplate trenches and vias. This results in a terminal effect, a new challenge for panel-level plating that is well-known in wafer-level processing. The terminal effect can cause increases in Cu thickness near the electrical contact zone in an electrochemical deposition (ECD) tool resulting in poor cross-panel uniformity. Some wafer-level solutions for the terminal effect can be applied to panel ECD tools, but their efficacy can be diminished on account of the scale and shape of the panel. Two solutions that show promise are the adoption of multi-zone anodes and the placement of dummy structures near the contact terminals.

Within-die uniformity becomes more challenging as feature sizes shrink and more complex design rules change feature shape morphology. Wafer-scale chemistries make the fabrication of the finer fan-out features possible, but adoption of these requires complete isolation of anodes. Organic additive packages that actively

compensate for local layout variation can be used to deliver within-die uniformity improvements. One drawback of these advanced chemistries is that they are by nature more reactive and can degrade over time. In wafer-level processing, Cu chemistry typically represents about 30-40% of the total cost of an ECD deposition step. Plating costs can be minimized and process control can be extended over the life of the plating baths by using plating cells with ion-exchange-membranes. A transition from 300mm wafer-scale fan-out production to a panel scale would require the use of membranes for stability and cost savings. TEL Advanced Packaging believes that the ECD process will not be a barrier to high-volume fan-out panel-level packaging manufacturing.

## Introduction

TSV has been a viable advanced packaging technology for several years [1]. The technical advantages of TSV are compelling, but our industry is still seeking lower price-to-performance ratios for packaging solutions for high-volume commercial products. Fan-out is one solution for multi-chip packages that is growing faster than originally predicted on account of its significant cost advantages.

**Figure 1** shows several market forecasts for growth two years from any given date. A comparison of three sets of estimates shows that on every occasion TSV growth was pushed out another two years and adjusted down, while fan-out growth increased dramatically. In the case of TSV,

forecasted growth early on was high because of the technical capabilities this packaging method offers. In subsequent years however, forecasts slumped as the cost and a few technical issues stagnated the growth outlook. This trend is similar to the front-end-of-line low-k dielectric outlook in the late nineties. In that case, dielectric materials were originally projected to be the leading solution for RC constant reduction. The barriers to this strategy were uncovered, and the transition from aluminum to copper emerged as the solution at the 130nm generation [2].

Fan-out has existed as a single-chip packaging solution for roughly 20 years [3]. With recent adoption of the technology, it has emerged as a low-cost, multi-chip solution. Performance and scaling improvements are not quite as significant as those offered by TSV, but the cost and ease of integration make fan-out more attractive for moderate cost high-volume commercial products. **Figure 1** shows fan-out market forecasts have increased eightfold since 2012 while the TSV market forecast has decreased.

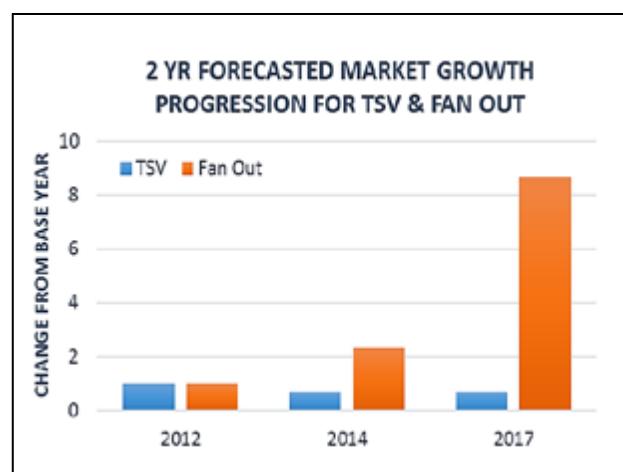
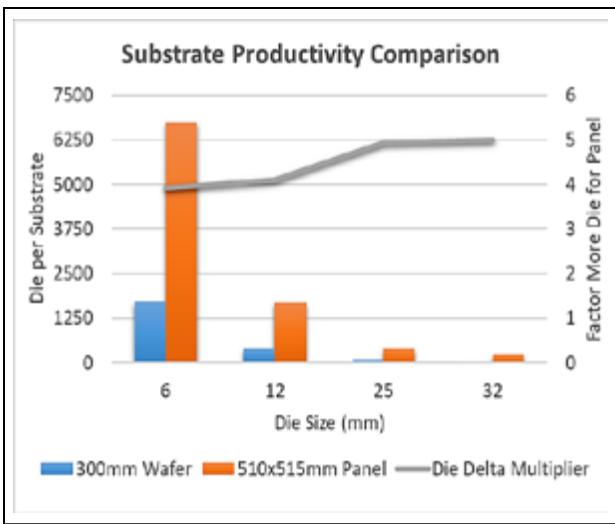
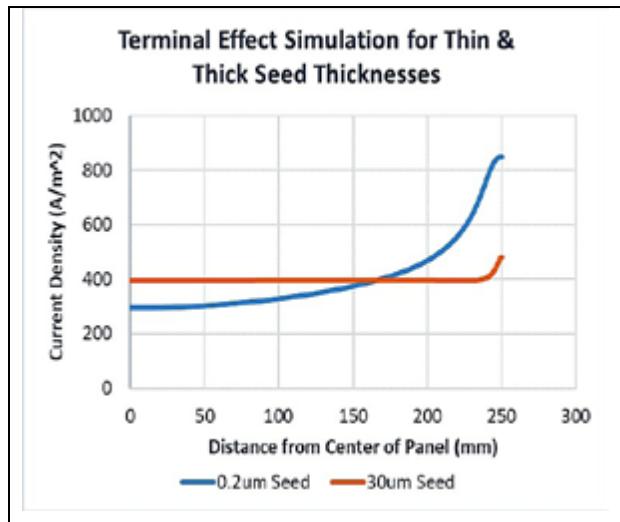


Figure 1: Comparison of market expectations for TSV and fan-out from 2012–2017.



**Figure 2:** Productivity comparison of a 300mm wafer with a 510 x 515mm panel for various die/package sizes.



**Figure 3:** Current density profile across 250mm half-panels (i.e., from center of panel to edge) plated at the same average current; 30μm seed and 0.2μm seed.

Wafer-level fan-out packaging represents a substantially lower price point compared to TSV [4], but it is still cost prohibitive for many products especially for multi-chip packages that are typically greater than 20mm in size. An increase in substrate size has been one way the integrated circuit (IC) industry has delivered significant cost reductions historically [5]. Fan-out technologies would enable this trend to continue at the package level even though wafer substrates seem to have reached a plateau at 300mm. Panel substrates 510 x 515mm in size represent a greater than three-fold increase in substrate area for less than a 50% increase in cost. This multiplier

in number of die or packages per substrate for panel compared to wafers increases as the size of the unit grows. This is particularly important for multi-chip fan-out structures, which by their nature are larger than single-die packages. This is plotted in **Figure 2** for 6mm die up to 32mm die.

The cost reduction is compelling for a transition from a 300mm wafer to a 510 x 515mm panel, but meeting the technology requirements now and in the future [6] for high-yielding panel-level fan-out must be proven. Cu line formation is one of the more demanding applications prohibiting the transition from wafer- to panel-scale fan-out manufacturing. High density interconnect (HDI) printed circuit board type panel-scale electroplating tools can support a 10μm line/space (L/S) feature size, but 5μm L/S is now required.

Also gaining traction in the next few years, multi-chip fan-out technical requirements will include a feature size reduction from 10 to 2μm L/S and cost reduction achieved through a substrate transition from wafer to panel substrates. For this reason, the design features commonly found on wafer-level ECD tools will need to be ported to panel-scale equipment. Thin-seed plating hardware (<5000Å) compatible with advanced chemistries will be critical to deliver improved within-die performance.

### Thin seed plating

There is a trend towards greater heterogeneity in advanced packaging structures, which leads to pattern and density variations that present challenges to uniform deposition across the panel substrate. Concurrently, the market is moving towards smaller features, which require thinner seeds. However, these thinner seeds can pose greater uniformity challenges for deposition because there are higher resistances in thin seed plating that lead to greater terminal effect. Two strategies can combat these panel plating challenges: 1) multi-zone anodes, which provide the capability to fine tune currents on specific areas of the panel, and 2) the use of dummy die, which move higher deposition areas away from active die.

**Terminal effect.** The terminal effect is a phenomenon that occurs due to the resistance of the seed layer on the substrate. There are typically localized higher current densities at the edge compared to the center. These higher current densities lead to thicker deposition.

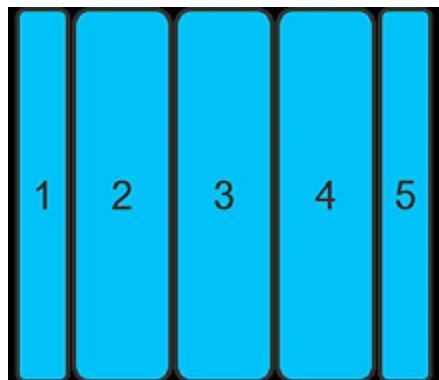
As linewidths shrink below 10μm, Cu seed layer thicknesses in ECD must reach sub-micron levels. This transition causes what is known as a terminal effect, where the thickness near the contact area has a significantly lower resistance than the areas located farther from the contacts resulting in increased ECD thickness. This phenomenon is modeled in **Figure 3**.

**Multi-zone anodes.** Multi-zone anodes provide the ability to adjust current density to fine tune deposition to specific sections of the panel to accommodate a variety of patterns.

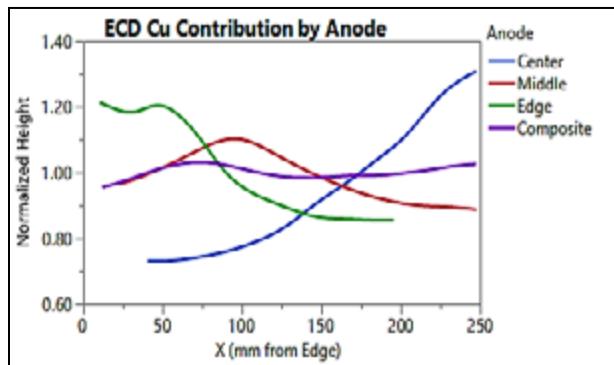
The terminal effect in conjunction with changes linked to the dummy die near the edge of the wafer can cause large shifts in the plated Cu thickness near the contact region. **Figure 3** shows the variation in near-edge film thickness for a thin-seed and thick-seed condition. Because the productivity of panel-scale ECD tools for multi-chip fan-out is so high, it is unlikely that there will be enough manufacturing demand for dedicated process tools that can be statically configured to support a single seed thickness or dummy structure. Therefore, there is a need to dynamically adjust the ECD cell to provide uniform plating thickness independent of seed thickness or dummy structure.

One way to deliver this dynamic tuning capability is with multi-zone anodes. Multi-zone anodes provide the ability to adjust the current density within a certain area of the substrate independent of current crowding effects observed with shielding. Multi-zone anodes also offer the flexibility to make panel-to-panel adjustments or even achieve a desired plated thickness profile during the plating of a single panel. A five-zone anode array may be arranged as shown in **Figure 4**.

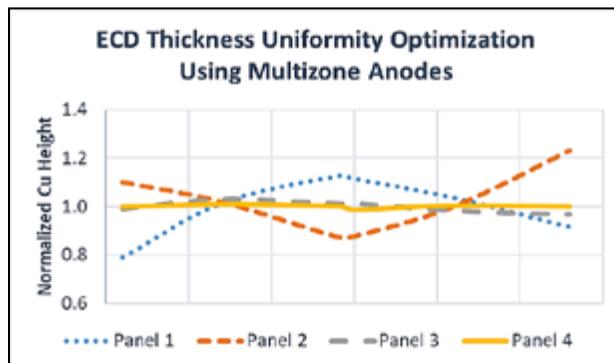
The current to the edge anodes can be adjusted lower than the center three anodes to correct the high plated thickness associated with the terminal effect in the configuration of multi-zone anodes shown in **Figure 4**. Alternative anode configurations are also possible. **Figure 5** shows how each anode arranged in a vertical fashion contributes to regional deposition and how the composite profile is flat.



**Figure 4:** Vertical multi-zone anode arrangement for dynamic current density adjustment to improve edge thickness variation differences in seed thickness or the effects of dummy die.



**Figure 5:** ECD deposition thickness contribution from each segment of a five-zone anode and the composite thickness.



**Figure 6:** Patterned panel thickness optimization shows progressive improvement with each adjustment to the anode current distribution keeping the total current fixed.

On patterned panels, multi-zone anodes arranged in a similar fashion can fine-tune the current density profile to meet required bump height performance values of <5% R/2M. In the case shown in **Figure 6**, a severely thin edge was observed when plating the first panel with a uniform plating current density profile across all five anodes. The second panel was adjusted to gauge the sensitivity of this device to the power density variation and resulted in an edge thick profile. Anode current density was then adjusted to achieve improved thickness uniformity. Final adjustments to the current density were made for the fourth panel run to deliver a within-panel bump height uniformity of <5% R/2M.

While similar results as those shown in **Figure 6** could hypothetically be achieved using a single anode in combination with an appropriately designed shield, the optimization would apply only to a specific panel layout and pattern density. Any changes in layout or pattern density, within the process flow of a single multi-layer panel product, could render a given static shield useless. A set of dynamically-tuned anodes can be rebalanced in response to substrate variations without requiring the down time associated with shield changes.

The geometric configuration of the anodes, in particular, their location and shape, determines the capability of multi-zone anodes to tune uniformity. “Dimensionally-stable anodes,” or insoluble anodes, are the most desirable for uniformity control. However, certain chemistries are not compatible with dimensionally-stable anodes. In these cases, anodes can change shape during processing and compromise uniformity results. While a number of options are available, iridium-oxide-coated titanium anodes have worked well for many copper plating chemistries.

Insoluble anodes also offer benefits that directly impact high-volume manufacturing (HVM):

- Anode replacement is practically eliminated;
- No “black film” maintenance is required for P-doped Cu anodes to be effective, thereby eliminating long burn-in times; and
- A node-generated particle contamination is eliminated.

There are a number of methods to maintain metal concentrations. CuO dosing is convenient in this regard because it inherently balances the acid generated in the anodic oxygen-evolution reaction.

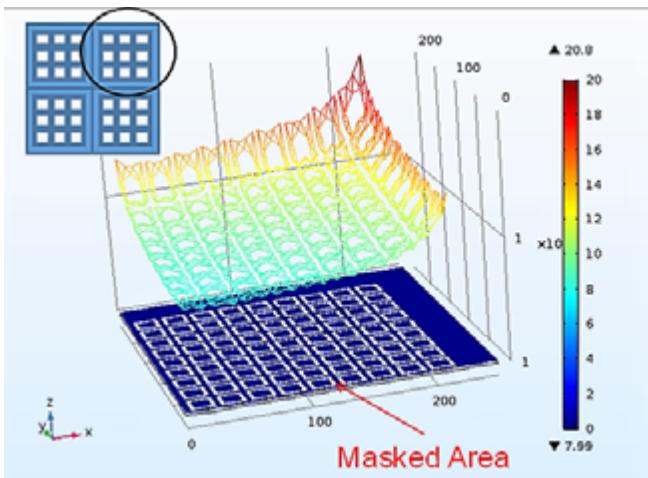
### Within-die coplanarity

For many devices (die) fabricated on traditional wafer-level ECD tools, it is often convenient to decouple considerations of within-wafer uniformity from those of within-die uniformity. For many packages fabricated on panels, this decoupling is not as straightforward: die are often large enough that gross within-panel nonuniformity gradients significantly impact within-die uniformity over at least some of the die or package units.

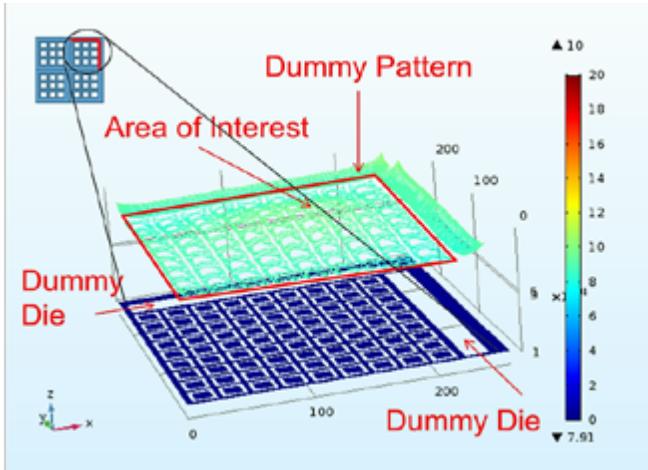
Thin seeds and overall cell geometries are long-recognized factors affecting plating uniformities, and methods to cope with these are generally understood. In the wafer space, an additional complicating factor has been the impact of die layout, more specifically the necessity to fit rectangular die onto a round substrate (the wafer).

Panel geometry potentially allows for more efficient exploitation of the available surface. However, it is often the case that the entire panel area cannot be utilized for die. Upstream or downstream integration requirements often dictate that die are excluded from areas of the panel. In many cases, these excluded areas (major streets), pose an opportunity for patterning of so-called “dummy patterns.” Judicious use of such dummy patterns facilitates uniformity tuning across a panel, often with beneficial impacts to within-die uniformity (or coplanarity).

**Figure 7** shows a panel quadrant with a hypothetical pattern (an array of die, each die consisting of a periphery of patterned metal surrounding an un-plated (resist-coated) inner area). The figure shows the pattern (a 9 x 9 array) plated with an exclusion zone consisting only of resist.



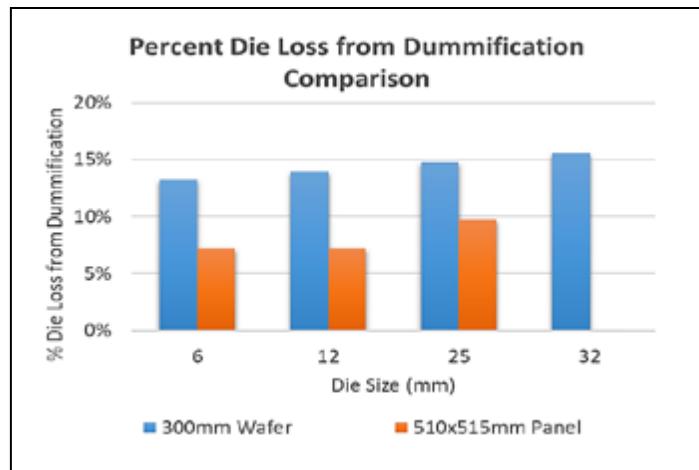
**Figure 7:** Simulation of plating of a 9 die x 9 die array. Note: Z height topography exaggerated for visual clarity. Plateable area of projected die is shown in yellow. The solid blue color corresponds to photoresist.



**Figure 8:** Same die array as in **Figure 7** but with added patterned dummy structures at the outside edges of the quadrant.

The nonuniformity is pronounced (both within-panel and within-die). Also, the figure highlights the marked impact of within-panel nonuniformity on within-die coplanarity; this interaction is obviously more pronounced for larger (packaged) die.

**Figure 8** shows the same array, plated under the same conditions, but with a horizontal and vertical dummy pattern along the outside edges. The areas in blue show the photoresist, while the adjacent areas in white are targeted for plating. The addition of a dummy pattern increases the proportion of how much of the overall area of the panel will be plated. This figure demonstrates how the topography in the region of interest, the product-dice area, becomes more consistent across the panel. Terminal and current crowding effects are corrected. The dummy structures deliver a greater than



**Figure 9:** Calculation of die lost as a function of substrate and die size.

5x improvement in uniformity in addition to a coplanarity improvement that provides higher yields.

The cost of using of dummy structures to improve process control is significantly lower on 510 x 515mm substrates than 300mm wafers on a unit area basis. The area advantage of panels is significant, and provides a 30-50% reduction in cost per die, which is the main driver for any substrate size increase. Large die, or packages, are more conducive

to fitting in panel geometries without the productivity losses associated with a wafer's circumference. **Figure 9** shows a comparison of percent die loss when a 10mm dummy structure is incorporated into wafer- and panel-scale fan-out processing for different die sizes. Aside from the intrinsic cost savings associated with a larger substrate, the added cost of dummy structure placement on a panel can be up to twice as much for a wafer.

### Advanced chemistries

Within-die coplanarity (or general uniformity) specifications become more demanding as the number of metal layers increases. These tightening specifications coupled with larger density spans from smaller features represent a substantial reduction in plating rates, or call for the

adoption of a more reactive additive package. Inherently more reactive additives require specially-built ECD hardware to minimize the breakdown of the additives, which can cause poor yields, extended maintenance times, and increase costs.

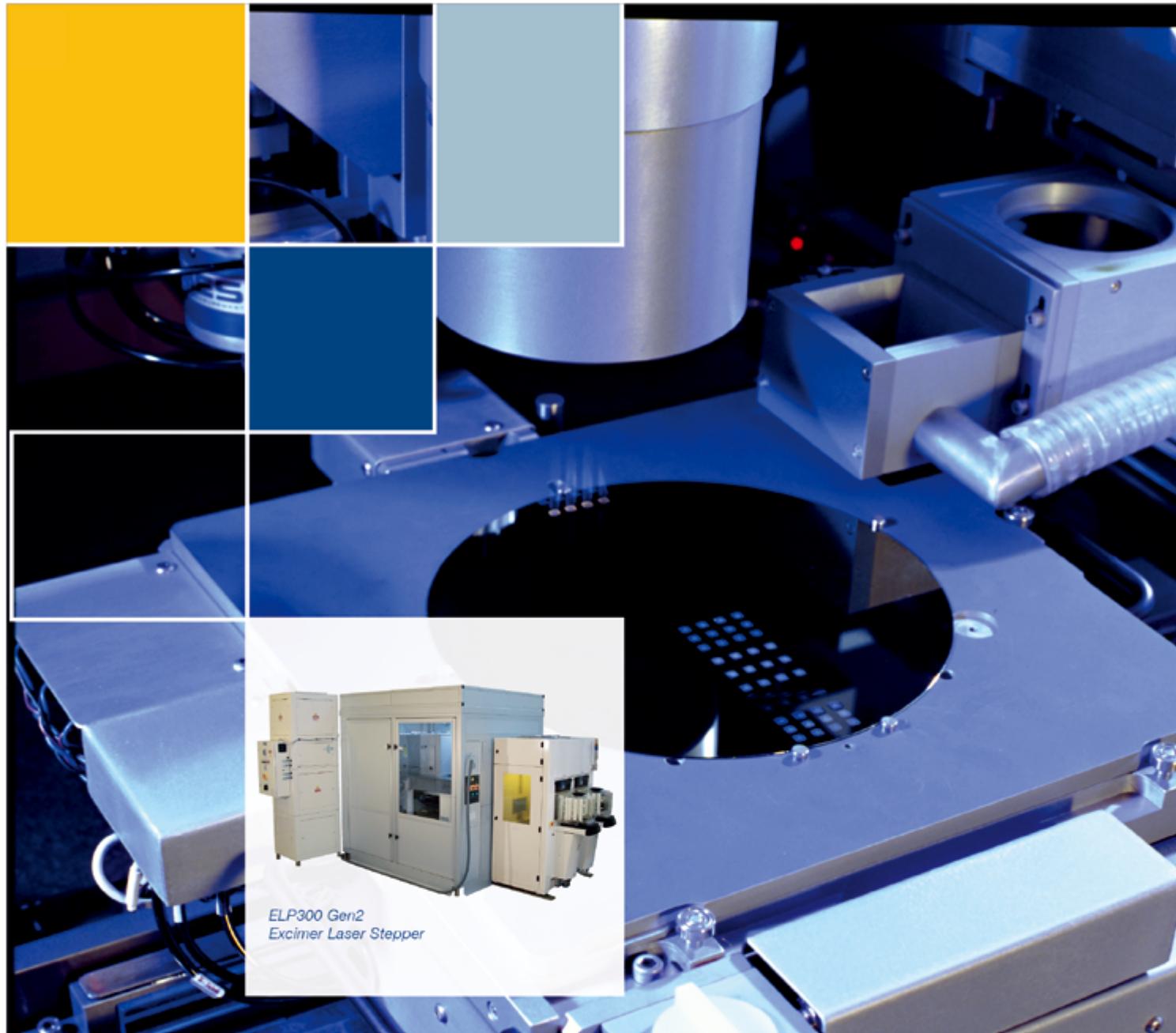
As features become smaller and pattern densities increase, the performance of the plating chemistries becomes an increasingly important factor in meeting product specifications. Many of the more capable additive suites are also more sensitive to decomposition byproducts and require careful process control.

While the specific byproduct formation pathways vary depending on the chemical nature of specific additives, many additives react adversely to anodes in the plating bath, either during electrolysis or when the cell is idle. Therefore, isolation of the anode from the bulk plating bath is often advantageous. Ion exchange membranes and discreet anolyte and catholyte chemistries can be an effective way of meeting isolation requirements.

### By-product management

Ion exchange membranes prevent the reaction of organic additives with Cu anodes, the evolving oxygen associated with insoluble anodes, or direct oxidation at either type of anode. Chemistry selection can once again be based on process performance criteria, rather than considerations of undesired additive breakdowns at the anode or substrate.

Accelerator and leveler are two common classes of organic additives used in Cu electroplating for advanced packaging. Breakdown of these additives occurs in the presence of Cu, which is useful at the substrate, but not at



## EXCELLENCE IN LASER PROCESSING

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The ELP300 Gen2 platform represents a highly attractive one-step patterning solution that meets the technology driven requirements of the Advanced Packaging and 3D industry. The laser stepper is designed for high throughput and is ideal for complex microstructuring, handling both 200 mm and 300 mm

wafers. This laser processing system is a technology enabler for patterning and other non-patterning applications in wafer-level packaging, including directly removing seed layers for redistribution layers (RDLs) and UBM, laser debonding for thin wafer handling, as well as resist ablation.

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anodes. Unwanted breakdown can also occur in the presence of plating solution supersaturated with oxygen from insoluble anodes. Traditional vertical continuous plating (VCP) tools cannot protect from additive breakdown at the anode, thereby restricting additive selections to formulations with minimal breakdown rates. If a dual reservoir bath exists that isolates the chemistry at the anode from that of the cathode, size exclusion membranes can be used to prevent migration of leveler additives into the anolyte chemistry and subsequent reactions with the anode. However, accelerator additives are more diffusive in nature, so these membranes do not prevent their breakdown. Ion exchange membranes can completely isolate the organic additives in the catholyte from the anolyte chemistry, which eliminates breakdown at the anodes or from evolved oxygen in the anolyte. A comparison of accelerator and leveler breakdown rates for a planarizing advanced packaging chemistry is shown in **Figure 10**. There is roughly an eightfold reduction in additive breakdown for an ion exchange membrane cell compared to a traditional VCP tool. Introduction of size exclusion membranes along with the separation of anolyte and catholyte approaches the leveler consumption performance of an ion exchange membrane tool, but does not help with the accelerator additive.

A number of suppliers offer many different ion exchange membranes. The uses for these membranes are diverse, and electroplating of semiconductors is not a significant market for these products. For this reason, selection of these membranes can be difficult. Selection

criteria include mechanical and chemical factors. Mechanical considerations that determine whether or not a membrane can be used in HVM include: mechanical strength, wear, cracking, resistance, and shrinkage. Chemical selection criteria such as diffusion rates, fouling, resistance uniformity and stability, and additive reactivity determine whether the membrane can be used at all. Certain membranes have demonstrated benign behavior with certain organic additives, while reacting vigorously with others, so ion exchange membranes need to be paired with specific organic additive packages.

### Modular tool approach

VCP tools typically utilize single large bath volumes that often exceed 20,000 liters/bath. These sizable bath volumes result in large initial pour-up costs, increased tool size, weight, containment costs, and significant overall chemical running costs. Furthermore, running chemical additive design of experiment (DOE) studies or next-generation chemical evaluations is proportional to the bath volume and therefore cost prohibitive on large chemical bath systems.

In contrast, a modular plating tool used most often in wafer plating systems allows for an approximate 100 times reduction in bath volume as compared with a typical VCP system. This reduction in overall bath volume along with the ability to add single cell baths within a high-volume manufacturing system greatly reduces development costs and increases the overall flexibility of the plating system.

In addition, a modular type architecture approach has additional potential benefits such as multi-metal stack capability within a single plating system (i.e., Cu/Ni/Au) or different additive mixtures or bath temperatures on different plating baths located within the same tool, which would provide enhanced process tuning capability.

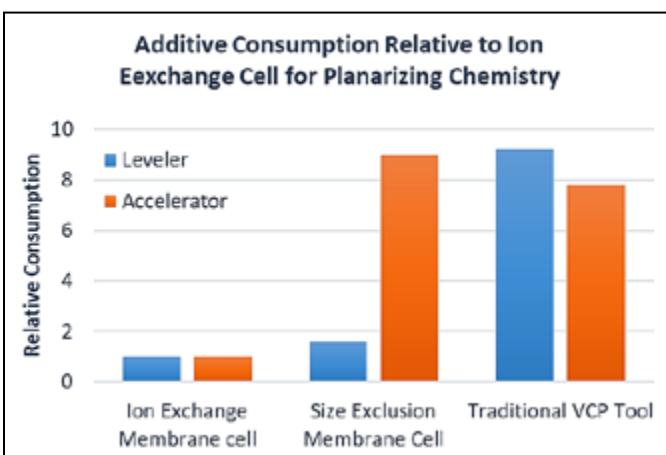
### Feature-scale plating performance

The nature of the various fan-out and wafer-level packaging (WLP) or panel-level packaging (PLP) products, both under production and under development, requires that an ECD tool be capable of delivering RDL, microbump, macrobump, blind-via fill, and through-via fill. Depending on the product type, and layer (in the case of build-up processes), combinations of features may even be present at the same step (e.g., blind via and fine line). To ensure high yields, plating must meet the required fidelity to all of these features (fill, height, shape, finish) with minimum variation across the die.

Plating chemistries often determine whether or not a feature-level plating specification can be met or not. As an example, for Cu, the levels of the inorganic constituents affect the plating capability of the bath to some extent. More importantly, however, are the levels and types of organic additives. The organic additives can determine the shape of plated features, whether void-free fills can be accomplished, the surface roughness of critical features (lines, bumps), and the overall coplanarity of plating across a die.

### Summary

IC packaging has traditionally played a supporting role in the continuous struggle to deliver more advanced technologies and cost improvements at the pace set by Moore's law. Substrate size changes such as the transition from 200 to 300mm wafers have made significant contributions to cost reductions. Material transitions, such as the shift from aluminum to copper wiring, have similarly improved performance while reducing costs. The introduction of technologies such as multi-chip fan-out packaging has been called "more than Moore" and offers many new manufacturing techniques. One way to deliver higher performance in smaller packages at lower cost is to migrate to a larger substrate size. 510 x 515mm panels have been used in the high-density interconnect market and could deliver a significant cost reduction to advanced packaging products as compared to 300mm wafers. This shift from wafer-scale to panel-scale could deliver the cost savings needed to justify HVM for fan-out processing.



**Figure 10:** Organic additive consumption of planarizing advanced packaging additives for different ECD cell generations.

As fan-out package features sizes continue to shrink, there are certain challenges to creating those features at a panel scale. Because wafer-scale chemistries must be used for finer feature development and these often require membranes, panel-plating tools must accommodate membranes to keep these chemistries stable. Additional panel-scale process improvements can be made by strategically adding dummy structures to panels and using multi-zone anodes.

TEL Advanced Packaging believes that the ECD process will not be a barrier to high-volume fan-out panel-level packaging manufacturing. A modular ECD tool can effectively produce multi-metal stack fan-out applications because each reservoir can be dedicated to a given metal layer. Multi-zone anodes can help counter the process challenges that stem from the terminal effects associated with larger substrate areas and rectangular geometries. Finally, lower volume plating reservoirs can significantly reduce chemical costs when compared to conventional vertical continuous plating equipment. Applying all of these techniques, membrane plating cells, multi-zone anodes and strategic dummy die placement could deliver the cost-down required for high-volume adoption of fan-out, as well as resolving many of the technical challenges associated with panel-scale plating.

## Biographies

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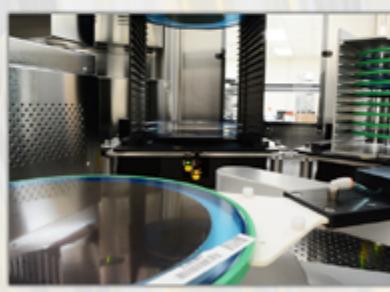
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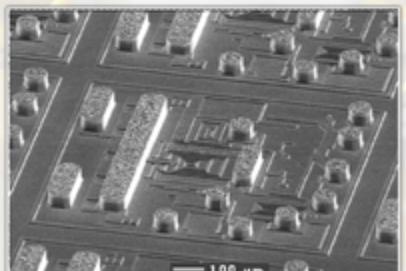
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# 3D IC heterogeneous integration by FOWLP

By John H. Lau [ASM Pacific Technology Ltd.]

## I

In this study, two 3D IC heterogeneous integrations by fan-out wafer-level packaging (FOWLP) technology are presented. The emphasis of the first such method is on the design, and of the other method, the emphasis is on the manufacturing method.

### System-on-chip

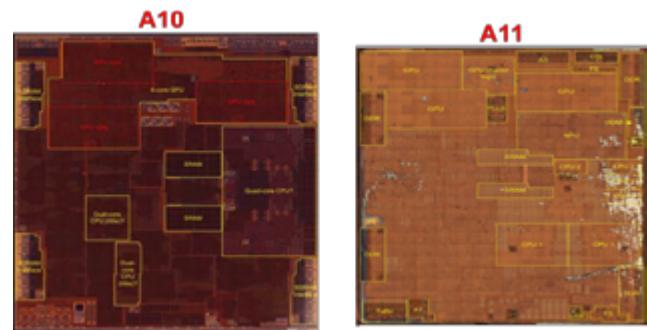
Moore's law [1] has been driving the system-on-chip (SoC) platform. Especially in the past 10 years, SoCs have been very popular for smartphones, tablets, and the like. SoCs integrate different-function ICs into a single chip for a system or subsystem. Two typical SoC examples are shown in **Figure 1**. The application processor A10 is designed by Apple and manufactured by TSMC using its 16nm process technology. It consists of a 6-core graphics processor unit (GPU), two dual-core central processing units (CPUs), 2 blocks of static random access memories (SRAMs), etc. The chip area is 125mm<sup>2</sup>. The application processor A11 is also designed by Apple and manufactured using TSMC's 10nm process technology. The A11 consists of more functions, including a tri-core Apple-designed GPU, etc. However, the chip area is about 30% smaller than that of the A10 because of Moore's law, i.e., the feature size is from 16nm down to 10nm.

### Heterogeneous integration

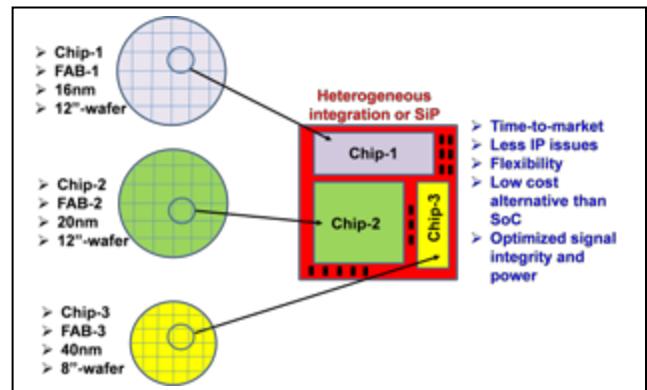
Why is heterogeneous integration of such great interest? One of the key reasons is because the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make SoCs.

Heterogeneous integration contrasts with SoCs as follows. Heterogeneous integration uses packaging technology to integrate dissimilar chips with different functions from different foundries, wafer sizes, and feature sizes (as shown in **Figure 2**) into a system or subsystem, rather than integrating most of the functions into a single chip and going for a finer feature size. For the next few years, we will see

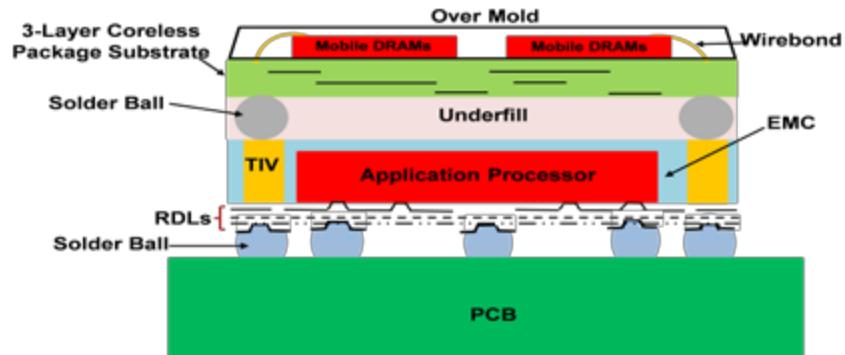
more of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost. Heterogeneous integration is going to take some of the market share away from SoCs on high-end applications such as high-end smartphones, tablets, wearables, networking devices, telecommunications, and computing devices. How should these dissimilar chips talk to each other, however? The answer is: redistribution layers (RDLs)! How should those RDLs be made? In this study, we use FOWLP technology.



**Figure 1:** SoC platforms for the A10 and A11 application processors.



**Figure 2:** Heterogeneous integration or SiP.



**Figure 3:** PoP for packaging the application processor and mobile memory.

### 3D IC heterogeneous integration by FOWLP

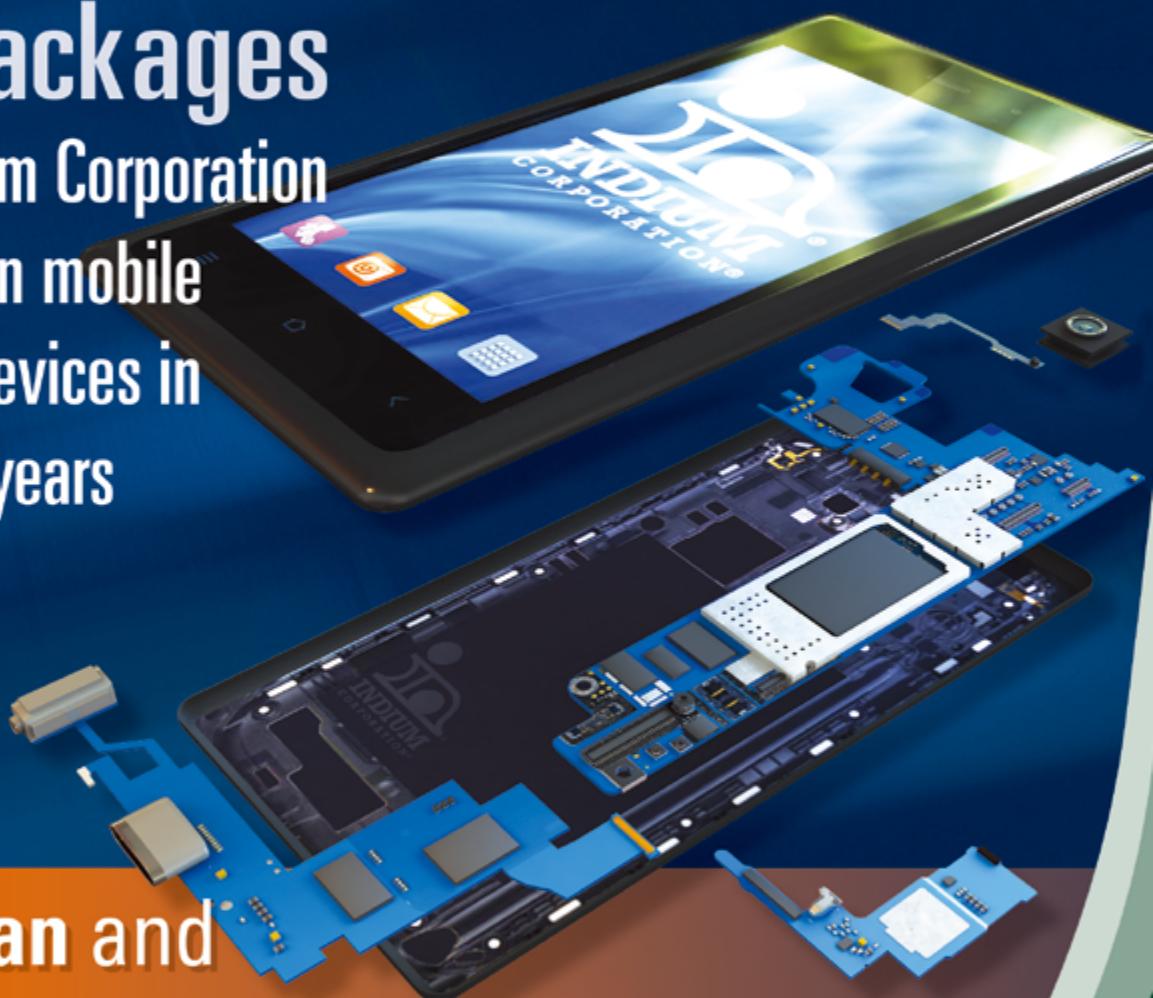
The A10 and A11 application processors are packaged using TSMC's InFO (integrated fan-out) wafer-level packaging method [2-5]. The mobile

dynamic random access memories (DRAMs) are wire bonded on a 3-layer core-less package substrate and the substrate is area-array solder balled on top of the application processor package – a package-on-

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## SiP Packages

Used Indium Corporation materials in mobile FEM SiP devices in the last 2 years

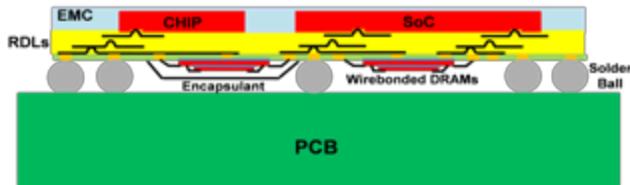


## No-Clean and Water-Soluble soldering solutions

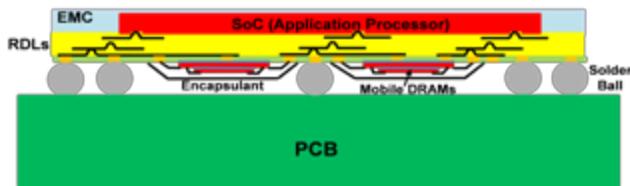
Contact our engineers today: [techsupport@indium.com](mailto:techsupport@indium.com)

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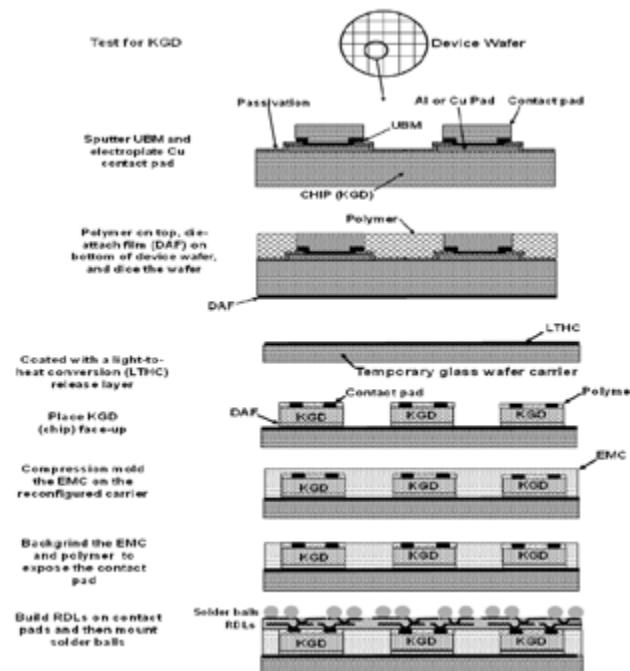




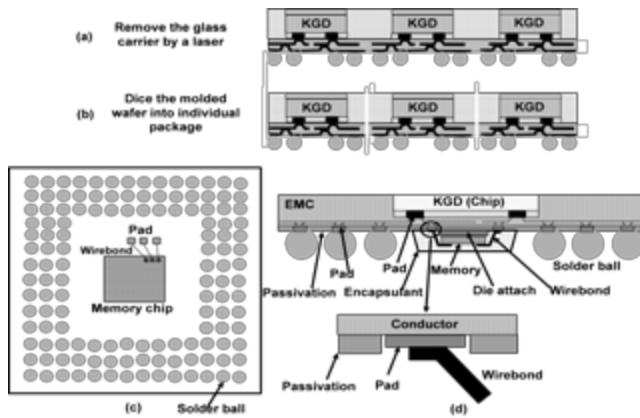
**Figure 4:** 3D IC heterogeneous integration by FOWLP.



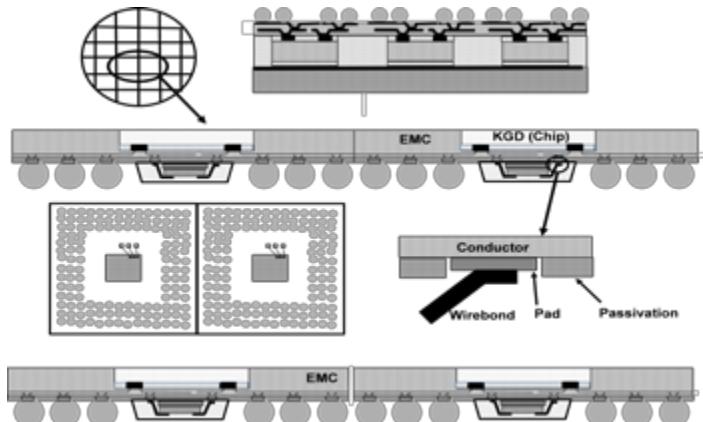
**Figure 5:** 3D IC heterogeneous integration to package the application processor chipset.



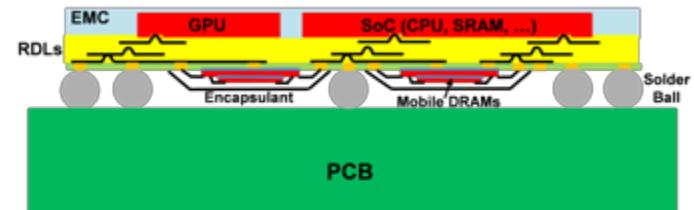
**Figure 6:** Manufacturing process for 3D IC heterogeneous integration to package the application processor chipset.



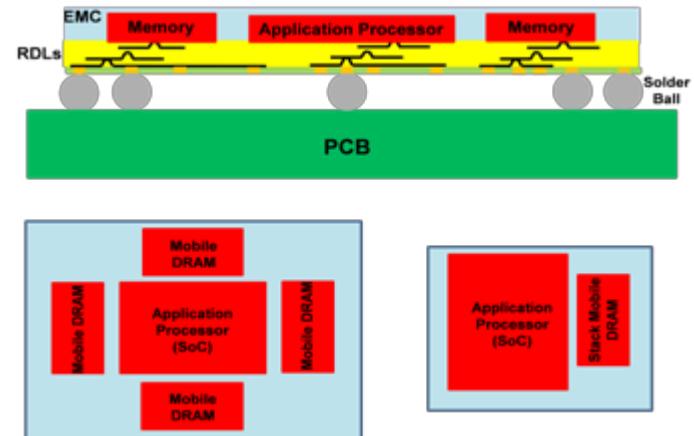
**Figure 7:** Wire bonding memory chip at the bottom of the individual application processor package.



**Figure 8:** Wire bonding memory chip at the bottom of the application processor package on a wafer.



**Figure 9:** 3D IC heterogeneous integration to package the application processor chipset.

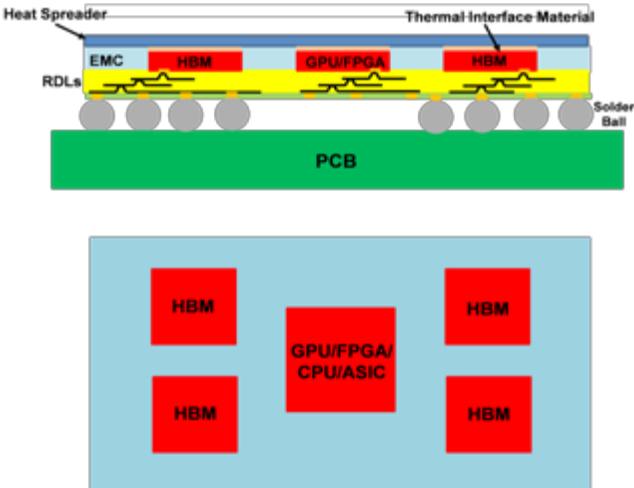


**Figure 10:** 2D IC heterogeneous integration to package the application processor chipset.

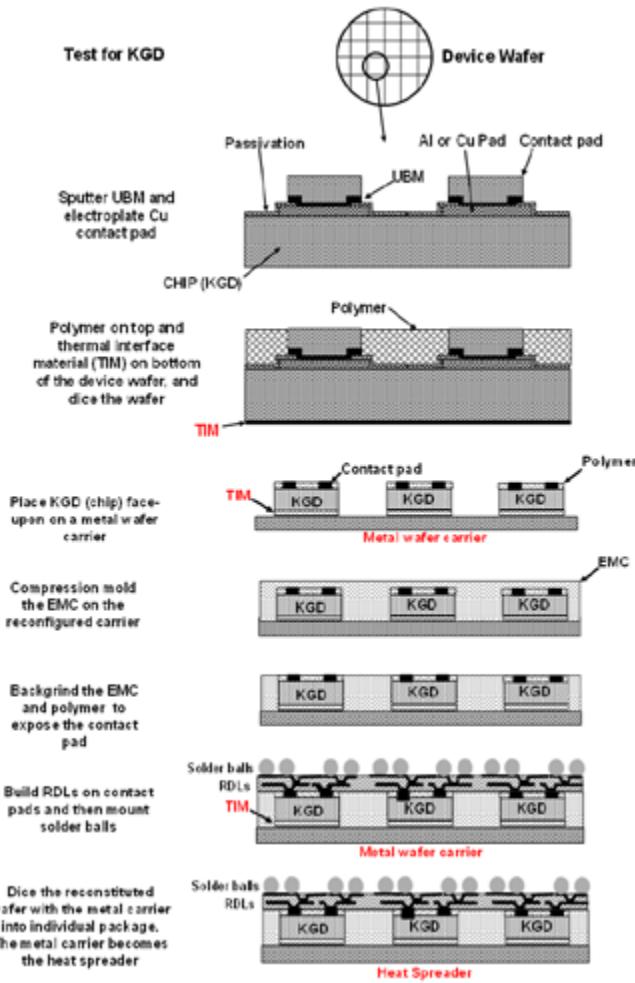
package (PoP) format as shown schematically in **Figure 3**. The interconnections between the application processor and the mobile DRAMs are mainly through the RDLs, through-InFO vias (TIVs), solder balls, and core-less substrate.

A new 3D IC heterogeneous integration by FOWLP, as shown in **Figure 4**, is proposed in this study. It consists of the SoC, chips, and the mobile DRAMs. Their interconnections are mainly through the RDLs, which can be fabricated by the FOWLP method. Depending on the number of layer of the RDLs, usually the total thickness of a 3-layer RDL is about 40 $\mu\text{m}$ . The DRAMs ( $\leq 50\mu\text{m}$ -thick) are cross-stacked with wire bonds and then encapsulated. The diameter of the solder ball is usually 200 $\mu\text{m}$ .

**Figure 5** shows a special case of **Figure 4** (when there is no other chip and the SoC is the application processor). Comparing



**Figure 11:** 3D IC high-performance heterogeneous integration by FOWLP.



**Figure 12:** Manufacturing method for 3D IC high-performance heterogeneous integration.

the new design (**Figure 5**) with that of **Figure 3** (the 3D IC heterogeneous integration vs. the PoP), it is obvious that: 1) the new design leads to a lower package profile; 2) the new design has less interconnects; 3) the new design is more reliable because

of less interconnects; 4) the new design has better electrical performance; and 5) the new design leads to lower cost.

The manufacturing process of the proposed 3D IC heterogeneous integration is very simple. First, the device wafer has to be modified by sputtering an under bump metallurgy (UBM) and electroplating a Cu contact pad (for building the RDLs later), as shown in **Figure 6**. This step is followed by spin coating a polymer on top of the device wafer and laminating a die-attach film (DAF) at the bottom of the device wafer. Meanwhile, a light-to-heat conversion (LTHC) layer is spin-coated onto the temporary glass carrier wafer. Then the individual known-good die (KGD) (chip) from the device wafer is placed face-up on the LTHC carrier. This step is followed by epoxy molding compound (EMC) dispensing, compression molding, and finally, post-mold cure (PMC). These steps are followed by backgrinding the EMC and polymer to expose the Cu-contact pad for making the RDLs and for mounting the solder balls, as shown in **Figure 6**. This is the conventional FOWLP method to package the application processor [2-12].

There are two methods to attach the mobile DRAMs to the bottom of the application processor fan-out wafer-level package. The first method comprises the following steps: 1) removing the glass carrier by a laser (**Figure 7a**); 2) dicing the reconstituted wafer carrier into individual packages (**Figure 7b**); 3) wire bonding the memory chips to the bottom side of the individual package (**Figures 7c** and **7d**); 4) and then glob topping the wires and memory chips with an encapsulant (**Figures 7c** and **7d**).

The second method to attach the mobile DRAMs to the bottom of the application processor fan-out wafer-level package comprises the following steps: 1) wire bonding the memory chips to the bottom side of every package on the reconstituted wafer carrier; 2) glob topping the wires and memory chips with an encapsulant; and 3) then dicing the reconstituted wafer carrier into individual packages (**Figure 8**).

**Figure 9** is a special case of **Figure 4**. This is when it is difficult and costly to reduce the feature size to make the SoC. Therefore, some of the function (for example, the GPU) is not integrated into the SoC and the GPU chip is placed side-by-side with the SoC.

In [13] we asked the question: “What if there is no PoP for the application processor chipset?” We proposed to place the application processor and the mobile DRAMs side-by-side on a build-up package substrate. The memory chips can be either cross-stacked or individually placed by wire bonding. Also, the memory chips can be placed individually by solder bumped flip chips. The memory chips can even be stacked and have TSVs. In this study, because we used the FOWLP method to construct the RDLs for the interconnections between the SoC and mobile DRAMs as shown in **Figure 10**, the build-up package substrate was eliminated.

## Achieving high-performance

**Figure 11** schematically shows a 3D IC high-performance heterogeneous integration by FOWLP technology. It can be seen that it consists of a GPU, a FPGA (field-programmable grid array), CPU, or a high-performance application-specific integrated circuit (ASIC), and is surrounded by high-bandwidth memory (HBM) cubes. Each HBM cube

consists of four DRAMs and a logic base with through-silicon vias (TSVs) [14-16] straight through them. Each DRAM chip has >500 TSVs. The interconnections between the GPU/FPGA/CPU/ASIC and HBMs are through the RDLs. The major heat path of this structure is from the backside of the GPU/FPGA/CPU/ASIC to the heat spreader. A heat sink can be added on top of the heat spreader if it is necessary.

In this case, the emphasis is placed on the manufacturing method (process) of this structure. This method comprises these steps: 1) testing for KGD of device wafers; 2) sputtering UBM; 3) electroplating the Cu-contact pad; 4) spin coating a polymer on top of the device wafers; and 5) painting a thermal interface material (TIM) on the bottom (backside) of the device wafers (**Figure 12**). The last step is different from the conventional method (the first case), which is laminating a DAF on the bottom of the device wafers.

After the steps outlined above are completed, the following are done: 1)

the individual KGDs are picked and placed face-up on a metal such as copper, aluminum, steel, and an alloy 42 (with thermal expansion coefficient = 8 to  $10 \times 10^{-6}/^{\circ}\text{C}$ ) carrier about 1mm-thick; 2) molding the EMC on the reconstituted wafer is accomplished by using the compression method and then post-mold curing (PMC) of the EMC; 3) backgrinding the EMC and polymer to expose the Cu-contact pad; 4) building up the RDLs; and 5) mounting the solder balls. Then, the reconstituted wafer is diced into individual packages (**Figure 12**). (Note: this process is different from the conventional method, which used a glass carrier and was coated with an LTHC release layer).

It should be emphasized that unlike the conventional method, there is no debonding of the carrier. The metal carrier becomes the heat spreader of the individual high-performance heterogeneous integration package. This new method of manufacturing high-performance chips and memory cubes in a heterogeneous integration

scheme with the FOWLP technology results in fewer assembly steps, lower cost, faster time-to-market, and higher assembly yield. Also, because of the metal carrier, the warpage is reduced during all the process steps. Furthermore, because of the metal carrier, the individual package size can be larger.

## Summary

Two 3D IC heterogeneous integrations by FOWLP technology have been presented. The first 3D IC heterogeneous integration is emphasized on the design and the other 3D IC high-performance heterogeneous integration is on the manufacturing method. Some important results and recommendations are as follows:

- A 3D IC heterogeneous integration of the application processor chipset has been proposed. The interconnections between the application processor and mobile DRAMs are through the RDLs, which are fabricated using the FOWLP



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- method. The manufacturing processes for making the 3D IC heterogeneous integration have also been presented.
- When it is difficult and costly to reduce the feature size to make the SoC, one way is not to integrate some of the functions (for example, the GPU) into the SoC and instead place the GPU chip side-by-side with the SoC.
  - The simplest heterogeneous integration of the application processor chipset is to place the application processor and the mobile DRAMs side-by-side on RDLs. One consideration is that the package size could be too large to be reliable. One of the alternatives is to stack up the mobile DRAMs.
  - A 3D IC high-performance heterogeneous integration of GPU/FPGA/CPU/ASIC and HBM/HBM2 by FOWLP technology has been proposed. Emphasis is placed on a simple and effective manufacturing method to fabricate the structure. Unlike the conventional method, there is no debonding of the temporary carrier. The metal carrier becomes the heat spreader of the individual high-performance heterogeneous integration package.
  - The advantages of heterogeneous integration are time-to-market, performance, form factor, power consumption, signal integrity, and cost.
  - In order to lower the package profile of the application processor chipset for mobile applications such as smartphones and tablets, the current PoP format should be eliminated.

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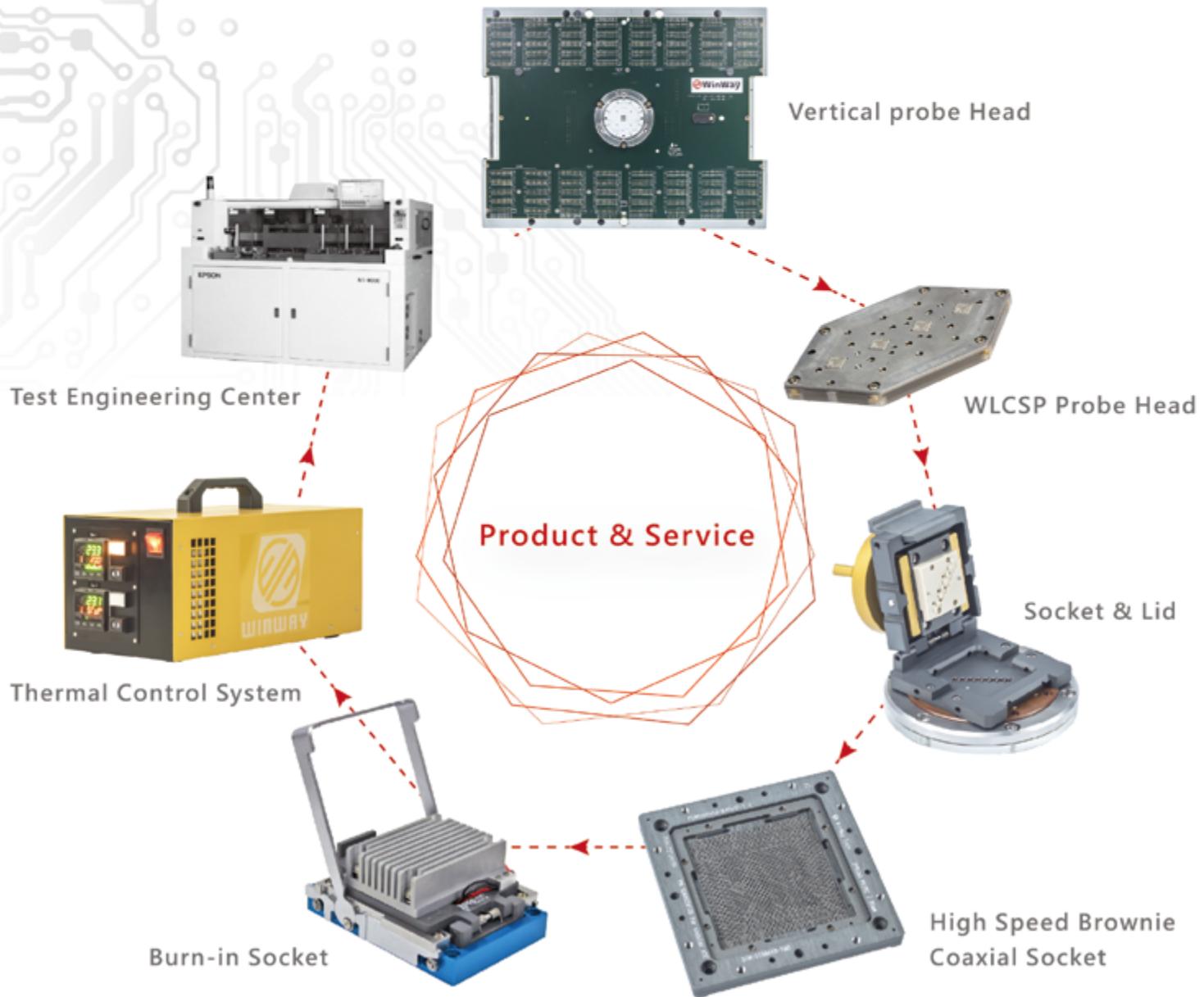
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# Laser debonding processes enable wafer-level packaging advances

By Thomas Uhrmann, Boris Považay, Mathias Pichler, Florian Schmidseder, Daniel Burgstaller [EV Group]

**T**emporary wafer carrier technologies have gained considerable importance in the semiconductor industry over the past several years in response to the increasing adoption and proliferation of new packaging architectures, including stacked (3D) packaging, to support increased device functionality. The initial approach to 3D-packaging using through-silicon vias (TSVs) that allow the functionalization and stacking of thin device structures has experienced slower-than-expected adoption due to relatively high process costs. As a result, only a few high-performance devices with TSVs have thus far passed the threshold to mass manufacturing. More cost-sensitive applications have driven the development of alternative integration processes better suited to their cost requirements. Fan-out wafer-level packaging (FOWLP), in particular, is well-suited for a majority of mobile applications due to its ability to simultaneously address performance, form factor and cost needs. Other devices, such as those in the radio frequency (RF) space, also followed this trend, enabling RF front-end functionality of band selection, filtering and amplification modularized within a single package, thereby reducing cross talk and RF compatibility issues in mobile devices [1-3]. Whereas early FOWLP devices contained individual dies with the need to expand area for redistribution, in recent years, FOWLP became a universal packaging platform.

Temporary wafer bonding is an essential step to support advanced packaging approaches, such as FOWLP, by enabling the mounting of product wafers onto carrier wafers for wafer thinning and back-side build-up, or to serve as a processing platform for redistribution-layer (RDL) first processes.

FOWLP process flows typically fall under two basic integration categories, called chip-first and chip-last. With the chip-first approach, individual chips

are embedded into epoxy mold, forming freestanding mold wafers as a basis for redistribution and bumping. This process is frequently referred to as embedded wafer-level ball grid array (eWLB). In the chip-last approach, redistribution layers are processed first, before the dies are individually attached and over-molded. In both process flows, temporary wafer carrier technologies play a

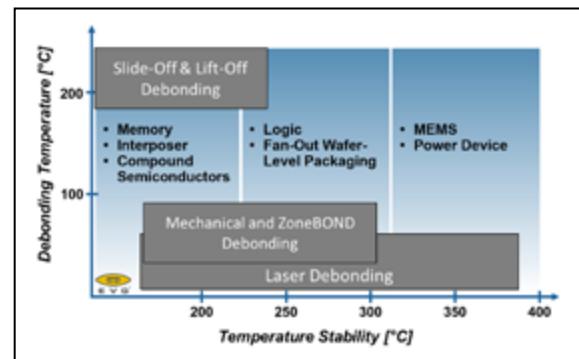


Figure 1: Selection of temporary bonding processes differentiated by application, temperature stability and debonding temperature.

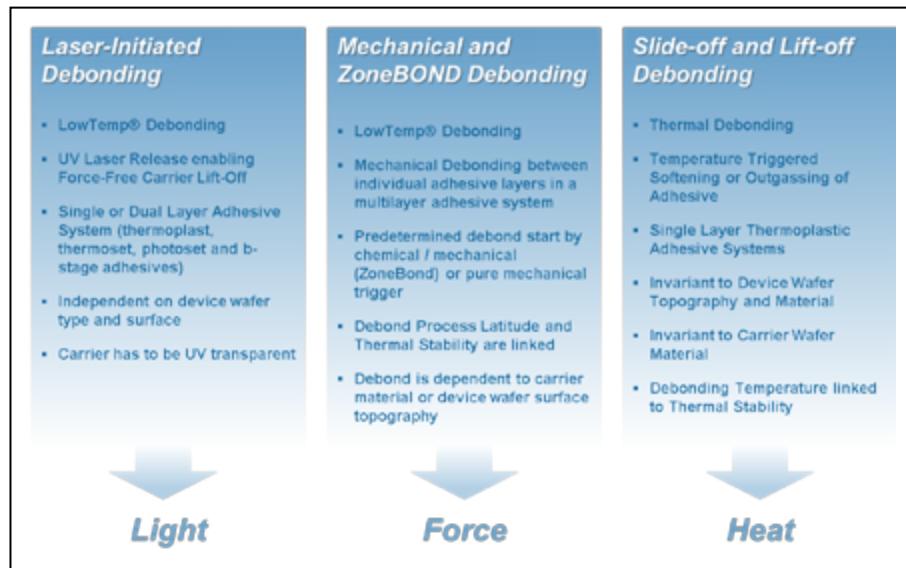


Figure 2: Classification of temporary bonding and debonding processes.

crucial role. For chip-first (or RDL-last), temporary carriers are used for package-on-package (PoP) technology, where thinning device wafers below 400µm does not allow for the use of freestanding mold wafer handling, as discussed by Campos, et al. [4-6]. Here, temporary carrier technology is used to handle thin wafers throughout the full redistribution process. Slide off debonding has been found to work reliably within the mold

wafer process flow. Contrary to this, chip-last is a pure build-up process, where the temporary bonding step forms the base layer. The package is built successively on top of the carrier wafer, and UV laser debonding is the final process step separating the devices from the carrier. Therefore, fundamental knowledge of critical process parameters for UV laser debonding is key to ensuring a high overall process yield.

## UV laser debonding

Temporary wafer bonding can be classified by the mechanisms that break the temporary bond interface and their point of interaction: 1) direct chemical bond release by laser radiation (laser debonding) via ablation or gas generation; 2) direct or indirect mechanical force (mechanical debonding); or 3) elevated temperature to soften or at higher levels to thermally dissociate the adhesive layer (slide-off and lift-off debonding). As shown in **Figure 1**, these debonding approaches have different temperature stability and debonding temperature characteristics for the device, which influence the type of applications for which they are best suited. Notably, the debonding temperature is only linked to the debonding mechanism for slide-off and lift-off debonding, while mechanical, ZoneBOND and laser-initiated debonding decouple the debonding mechanism from the global process temperature. **Figure 2** provides more detail on each debonding process.

UV laser debonding has several advantages over other debonding techniques that make it an extremely flexible debonding process. For example, the laser debond process is completely decoupled from the material requirements of the embedding layers for all available adhesive systems. This way, the individual process requirements, including high temperature, tension or pressure can be supported when selecting the optimal adhesive combination. Further flexibility can be achieved by adding functionality to the debond layer that also protects the substrate from side effects like thermal or mechanical stress, non-planarity, or contamination. In contrast to mechanical or slide-off debonding, the adhesive in laser debonding has no additional function for the debonding process. The only exceptions to this rule are polyimides. Their chemical structure allows for both bonding of the materials as well as UV laser debonding. This process latitude or temperature process window allows the use of polyimides with very high thermal temperature stability (approaching 400°C). This strong independency of the laser debond process from the rest of the process flow, compared to mechanical or slide-off debonding, allows for a much more straightforward integration of temporary carrier technology.

Another key benefit of UV laser debonding is its insensitivity to different substrates types, passivation layers and metals. Other debonding techniques rely

on surface energy and adhesion properties of the bonded surfaces to ensure proper debonding, while UV debonding relies solely on the selective decomposition of the laser release layer. The substrate is kept at room temperature during debonding, meaning that no thermal activation is needed. This allows for the use of a wide variety of temporary bonding adhesives types, which can be made with very low adhesion properties because the separation of the product wafer from the carrier wafer is force-free after debonding. The combination of this instantaneous bond release, avoidance of the thermal activation step, as well as high scanning speed associated with UV diode-pumped solid-state (DPSS) lasers, allows up to a 5X increase in debonding throughput compared to other debonding techniques.

A drawback of laser debonding is that it requires a UV transparent glass carrier in order to allow the laser light to initiate the laser debond process at the bond interface. However, where sodium ion contamination or mismatch of glass properties have been issues with this approach in the past, glass manufacturers can now offer suitable glasses that eliminate this obstacle.

## Influencing parameters for DPSS laser debonding

To limit the thermal input associated with laser debonding, UV DPSS lasers are used for the debonding step, which provide the benefit of rapid absorption of the UV light immediately at the glass release layer interface. Ideally, release layer materials feature a high absorption coefficient in the relevant regime at the laser wavelength, typically situated around the frequency-tripled Nd:YAG laser at  $\lambda \approx 355\text{nm}$ . In this case, penetration depth of light is designed to be less than 200nm for most commercially available debond materials. Furthermore, due to the lower peak power of these lasers it is essential that the transmittance towards the bond interface is high and radiation can be concentrated to reach the required irradiance. The beam quality factor of single mode DPSS lasers is typically close to  $M^2 \approx 1$ , which means that the beam cross-section has a unidirectional Gaussian beam shape reaching the maximum possible power density.

Because the photochemical dissociation is energy dependent and bleaches the debond material that can locally increase penetration depth, there is only a slim process window for scanning Gaussian spot ablation. Depending on the individual

process, local heating or stress necessary for debonding may occur at medium and higher power settings. At the beam center, however, significant overexposure can lead to pronounced carbonization. Carbon locally increases absorption and scattering, which nonlinearly increases the local temperature and leads to even further carbonization. Together with the exposure profile, pulsed exposure leads to inhomogeneous ablation, but also has the advantage of confining local heating to the debond layer, if the thermal pulse propagation stays within the exposure field during optical energy deposition. On the other hand, the tails of the Gaussian distribution are below the threshold, which leads to unnecessary global heating. Beam shaping optics of the single-mode beam is one way to flatten the central energy distribution and reduce the tail length. The fine tuning of the spot-shape towards a so-called flat-top beam profile together with exact relative laser spot positioning efficiently leads to homogenization and reduces overexposure effects. This flat-top beam profile facilitates low maintenance and running cost of DPSS lasers and provides an optimal approach to laser debonding [7].

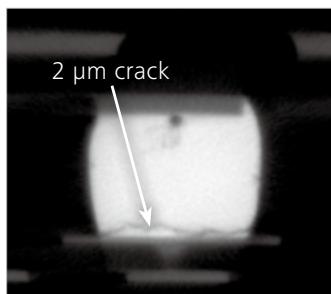
On account of the complex, but well predetermined, effects during the debond process, the outcome is not only controlled by the laser beam shape but also by the deposited laser fluence or radiant energy (measured in energy per area) per pulse. This important parameter impacts the debond result by controlling the microscopic photochemical and photothermal dynamics as well as the debond forces that appear due to the gas generation and heating within the debond material. Both laser power and pulse length determine the amount of energy per pulse. While the laser power can be easily tuned, pulse length is typically given by the specific laser source. Once these settings are optimized and controlled, and the process window for the individual shot area is set, the laser scanner parameters are fine-tuned to reach the optimum overlap between successive shots or even via multiple, shifted scans. This means that the exposure pattern is key to the process outcome. Depending on the release layer and the mechanism of response, either the full debond fluence can be applied in an individual shot, or multiple shots may be overlapped to deposit the required energy for photochemical decomposition and successful debonding to find the optimum arrangement for homogeneity, residual ablation roughness, gas generation, heat distribution and carbonization. In comparison to longer wavelengths in the green or infrared

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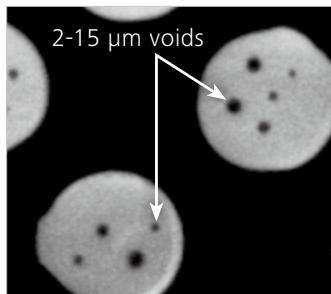


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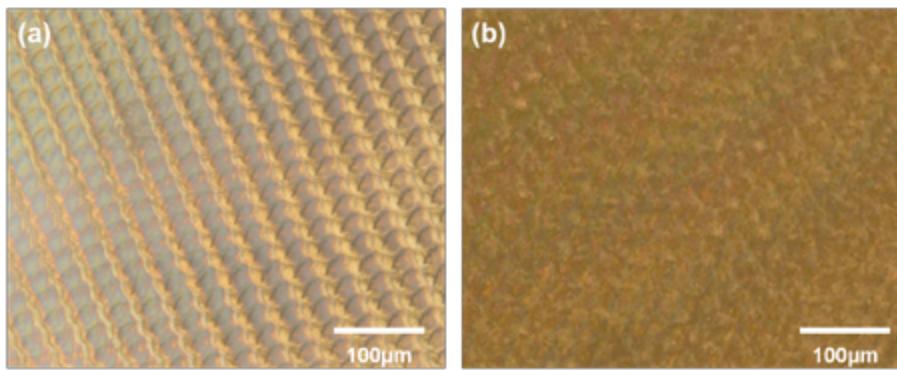
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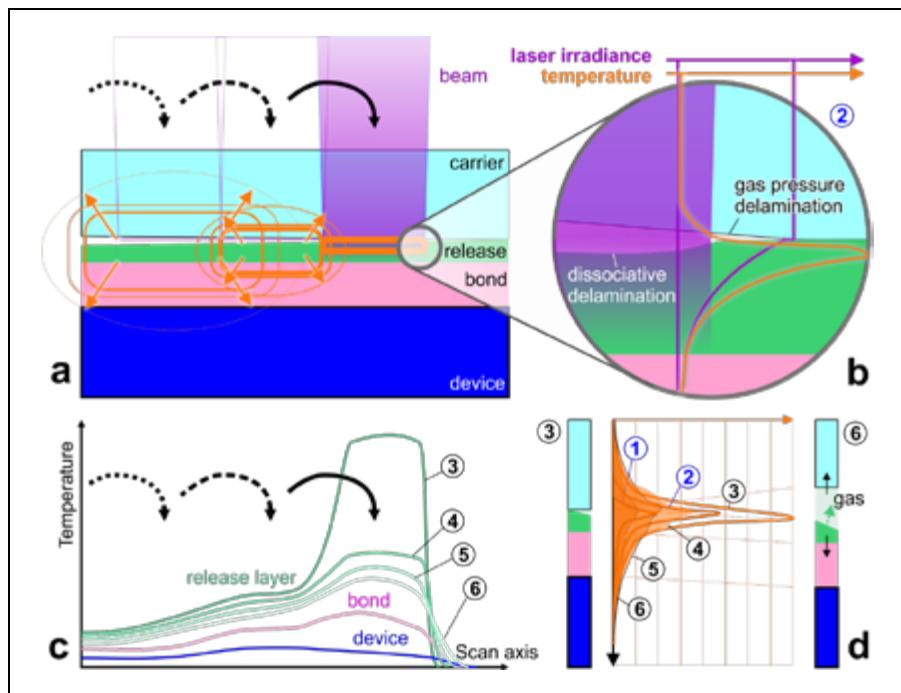


Virtual planar section





**Figure 3:** a) Bright-field microscope images of UV debonding without overexposure showing successful debonding without thermal carbonization; b) Laser fluence exceeding the allowed carbonization limit when increasing overlap for better homogeneity without beam shaping.



**Figure 4:** Schematic of the temperature evolution during UV DPSS laser debonding.

spectrum, where debonding is only related to photothermal decomposition, UV wavelengths decompose the material into the gaseous state directly, as well as thermally, which significantly enlarges the process window without carbonizing the interface or inducing excess heat. A comparison of an optimally-tuned UV laser debonding process versus an overexposed photothermal carbonization is shown in **Figure 3**.

Even though laser debonding is a room temperature process, it still introduces a thermal component that can vary with wafer parameters. The laser debonding process described above, utilizing both a release layer and bond layer, is schematically shown in **Figure 4** in order to highlight the thermal

component of the debonding process. Depicted in **Figure 4a** is a cross section with individual laser scan shots progressing from left to right. The absorption of the laser is shown in purple in **Figure 4b**, where the laser penetration depth is inversely proportional to the absorption coefficient of the release layer. It should be noted that the thermal peak close to the interface is directly related to the energy deposited by the laser. As the laser is absorbed in the topmost layers of the debond layer, the heat is conducted into the surrounding material and temperature rapidly decays away from the glass/release layer interface as well as laterally from the heated spot. **Figure 4c** and **4d** depict the temperature evolution during debonding, including how the temperature generated at

the glass surface diffuses through the stack, delaying the temperature input to the device surface by several laser shots. Phases 1 and 2 are displayed at a different time interval (in the ns-range) where the pulse still heats the release layer, while phases 3-6 are in the  $\mu$ s-range when the heat dissipates.

The smaller size of DPSS laser spots is beneficial for this debonding case, since the field size is of the same order of magnitude as the layer thicknesses. Therefore, heat diffusion occurs in all directions in space, and the in-plane component reduces the temperature increase of the other layers considerably. Measurements have shown that this heating of the device surface is less than  $+30^{\circ}\text{C}$  due to the fast heat dissipation into the surrounding regions. On the other hand, with large area exposure such as generated by excimer lasers, this 3D heat diffusion model is not applicable anymore. Due to the large debonding area at low repetition rate, the generated heat can only diffuse orthogonal to the sample surface, as the perimeter of the debonding area is comparatively small. In other words, controlling the temperature impact is much easier in the small spot case.

Concentrating the energy in time and space drastically improves efficiency, especially in thermal-dominated materials like polyimides, and improves the debond speed to more than  $1000\text{mm}^2/\text{s}$  by covering large areas at lower laser energy. As a result, both throughput and thermal exposure of the sensitive components are positively affected.

The debond gap opens not only due to the ablation process and the removal of material, but also due to the gas pressure build-up, which can introduce local debond forces of variable strength that are given by the material and are controlled by laser settings such as pulse energy, spot size, spot overlap and the timing. Again, the control of the laser parameters and their fine tuning to the material is crucial for a successful and homogenous delamination across the whole substrate by exactly controlling the debond force on a microscopic level. In practical terms, a successful and stable laser debond implies fine and precise control of the laser process parameters, continuous monitoring, and detailed and fast strategies to map out the process window that is individually tailored to the product requirements.

In addition to maintaining exact control of the debonding process, the cost of debonding must be minimized. UV DPSS lasers for debonding feature a high pulse repetition frequency, which results in a high debonding throughput. Depending on the type of adhesive, the required dose as well as spot size, typical debonding can be achieved in

less than one minute for 300mm wafers. For panels, the debond time scales according to the panel size.

## Summary

UV laser debonding is a universal debonding process that is applicable to a very wide range of devices, wafer types and surfaces. It offers high process latitude and temperature stability to ease the integration of temporary carrier technology into the wafer production flow for stacked device applications. The high repetition frequency, low consumable costs and high throughput of DPSS lasers, and high uptime and small footprint of the source, coupled with precise and stable beam-shaping optics, provides a reliable and efficient combination that enables debonding for cost-sensitive advanced package types, such as FOWLP.

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## Biographies

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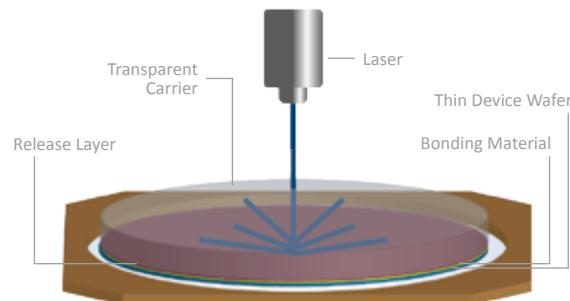


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## Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



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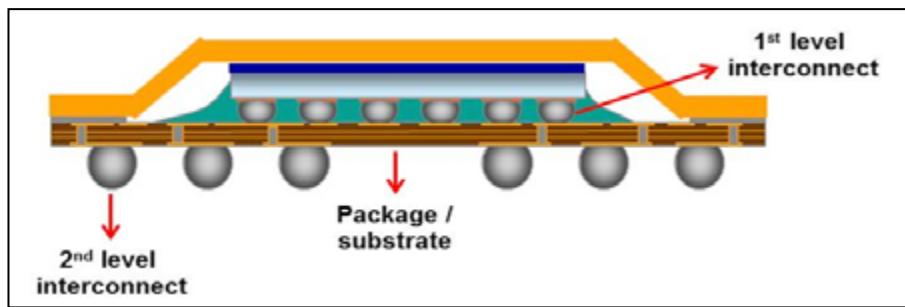


# Surface analysis as a “blueprint” for semiconductor package manufacturing

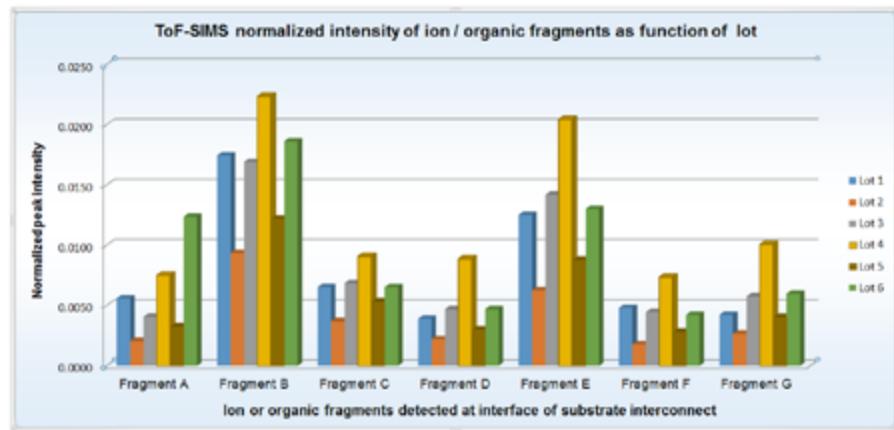
By Jaimal Williamson [[Texas Instruments](#)]

**V**arious analytical tools popularized by what seem like myriad primetime crime-scene investigation (CSI) television shows have glamorized aspects of materials science and its prowess in discovering clues to a mystery. Similar to a CSI, use of analytical tools like time-of-flight secondary ion mass spectrometry (ToF-SIMS) and X-ray photoelectron spectroscopy (XPS) can reduce the time gap to problem solving. For instance, on account of the surface sensitivity of ToF-SIMS and XPS, these tools can guide a packaging engineer from the ostensibly impossible “finding a needle in a haystack” scenario to a more positive outlook of finding the “elephant in the room” based on tool detectability at the nanometer and monolayer scale. In this analogy (and focus of the article), the needle in the haystack scenario is finding the source of organic contamination forming between metallic layers within a flip-chip ball grid array (FCBGA) build-up substrate (see **Figure 1**), where the contamination degrades bonding strength. Like a CSI where many instrumental tools are used to solve unknowns about a case, the aforementioned surface-sensitive analytical techniques facilitated mapping a blueprint for the elusive organic species under investigation. Specifically, leveraging the advantages of the surface analytical techniques enabled mapping a blueprint to decipher chemistry of the contamination despite limited chemical information from the chemical supplier due to intellectual property restrictions.

The FCBGA substrate manufacturing process is an intricate series of sequential steps where the plethora of organic materials used to form the composite structure can create a labyrinth of challenges in meeting stringent reliability requirements for automotive and commercial devices. Interfacial adhesive quality between



**Figure 1:** Example of an FCBGA device.



**Figure 2:** Chart illustration of ToF normalized intensity vs. organic fragments or ions detected at the anomalous substrate interconnect structure.

layers of the FCBGA substrate is of utmost importance to ensure reliable metal-to-metal or polymer-to-metal bonding. Critical interfaces within the composite substrate between polymeric dielectric and copper layers and copper-to-copper interfaces (that are embedded within substrate interconnect structures) are examples where organic contamination can form and become detrimental to the reliability of the aforementioned interfaces.

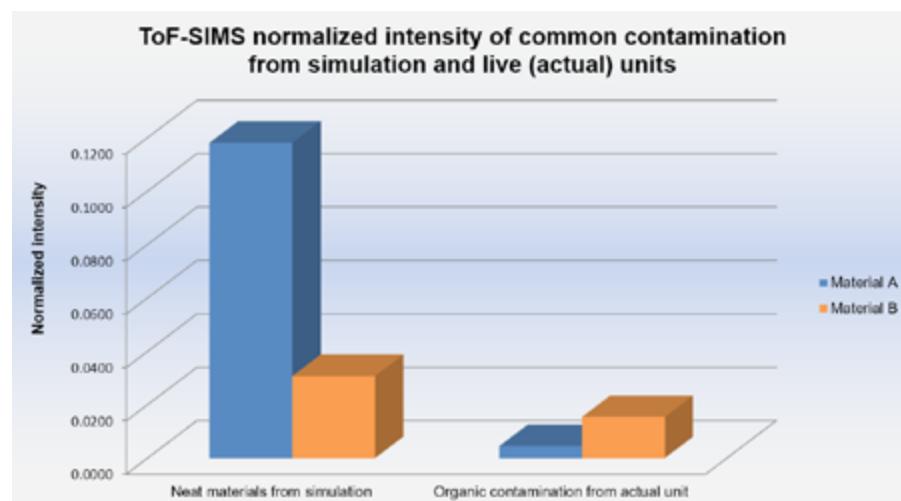
Employing the use of surface-sensitive analytical tools like ToF-SIMS and XPS enabled a synergistic approach to elucidate surface chemistry between layers where interfacial quality was questioned. Specifically, anomalous substrate interconnect structures

were inspected, where ToF-SIMS and XPS identified surface contamination revealing organic fragments and chemical functionality associated with specific process steps of the FCBGA manufacturing process. With chemical structure partly known, these details were correlated to chemistry found in the material safety data sheet (MSDS) pertinent to the process step of interest. This article focuses on unearthing the source of organic contamination at a substrate interconnect structure within an FCBGA substrate. Surface analysis aided in narrowing the source of the organic contamination manifesting itself during a front-end FCBGA substrate manufacturing process step.

## Surface analysis results

Multiple sets of ToF-SIMS analyses were performed to study the normalized intensities of different fragmented organic compounds/elements detected at an anomalous substrate interconnect structure (i.e., connecting layers within the substrate). The goal was to correlate the organic contamination to the specific front-end FCBGA substrate process step causing the issue. Based on ToF-SIMS results (see **Figure 2**) the surface chemistry detected was similar across multiple process lots at the substrate interconnect structure of interest. Because the ToF-SIMS results showed commonality in surface chemistry across multiple lots, this narrowed the focus of the investigation to two specific manufacturing process steps as the source of the organic contamination.

To supplement the findings noted above and drive manufacturing process improvements, a back-door approach of isolating the neat organic materials from the aforementioned two process steps (i.e., suspected of contamination) was repeated through ToF-SIMS analysis. Specifically,



**Figure 3:** Chart illustration of ToF normalized intensity showing commonality of neat materials forming at the anomalous substrate interconnect structure.

dedicated samples were prepared directly after each of two process steps that were suspected as sources of contamination for ToF-SIMS analysis. This approach was carried out to isolate the chemistry associated with the two process steps suspected as sources of contamination from

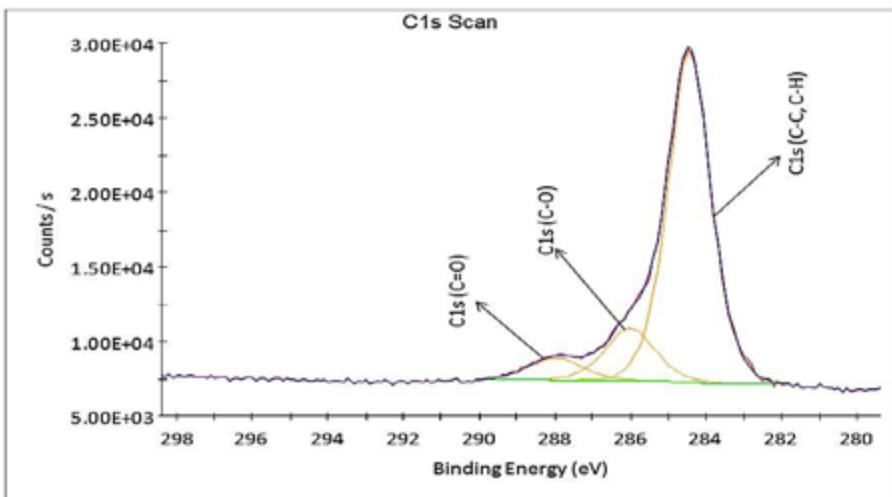
subsequent process steps. This approach enabled a more precise correlation of the surface chemistry at the anomalous substrate interconnect structure. The key point of isolating the neat materials was to analyze the materials in their purest form and enable a process of elimination

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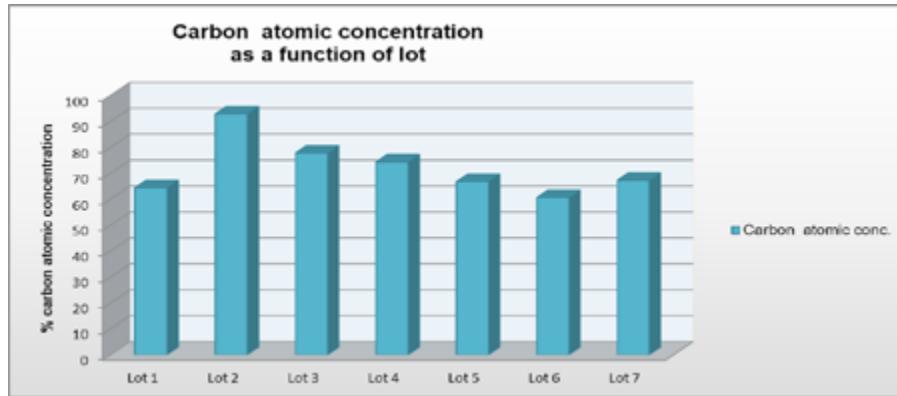
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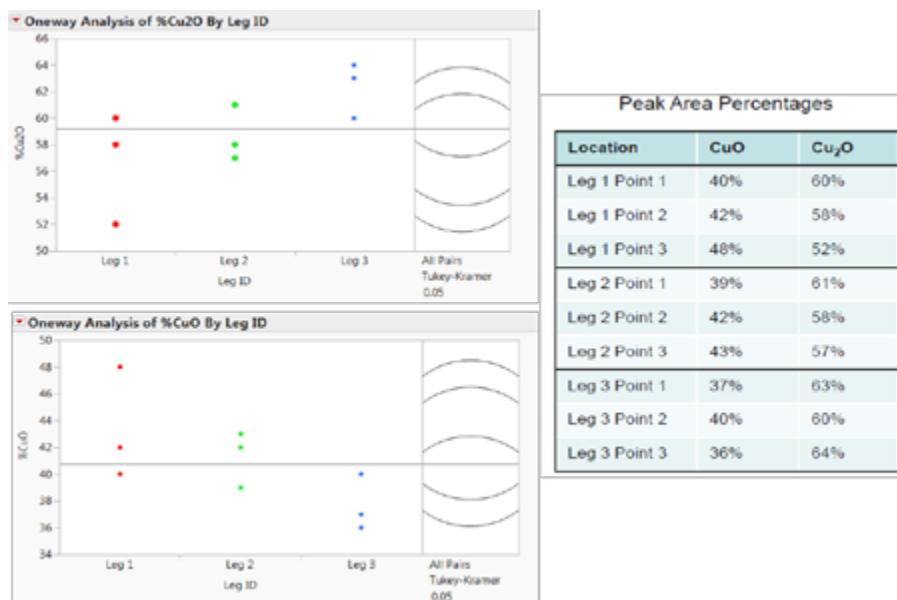
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**Figure 4:** Example of XPS high-resolution C1s peak.



**Figure 5:** Chart illustrating the atomic concentration of carbon across different lots.



**Figure 6:** Statistical data showing no differences in copper oxide formation based on different test conditions.

to distinguish the contamination from the plethora of organic materials used in the

FCBGA manufacturing process. These simulations, organized on a dedicated test

vehicle, helped correlate surface chemistry of the neat materials to chemistry of the contaminant at the anomalous substrate interconnect structure within an actual unit. **Figure 3** provides an illustration of the results showing commonality in the surface chemistry of neat materials, as simulated on a test vehicle, to organic contamination from actual units. For example, material A and material B are neat materials specific to the two aforementioned process steps, which were also detected at the anomalous substrate interconnect structure. These results provided evidence that the two process steps suspected of the organic contamination are contributors to compromising the integrity of the substrate interconnect structure.

XPS was used to study the atomic concentration of carbon at the anomalous interface as well as identify chemical states of the organic contaminant by comparing chemical functionality produced from the high-resolution carbon 1s scans (refer to **Figure 4**). Comparing the percentage of carbon atomic concentrations at the anomalous substrate interconnect structures was used as a gauge to understand the magnitude of the organic contamination as a function of lot. Variation in the percentage of carbon atomic concentration across multiple process lots is illustrated in **Figure 5**. Results in **Figure 5** confirmed that an organic material was the dominant source of contamination based on the high percentage of carbon detected. More detailed inspection of the high-resolution carbon 1s scans confirmed similar chemical functionality of the organic contaminant as detected from ToF-SIMS analysis.

In addition, XPS was used to quantify the efficacy of the process improvement implemented, where the atomic concentration of copper oxides was studied to ensure no deleterious effects. In particular, both copper oxides of cuprous ( $\text{Cu}_2\text{O}$ ) and cupric ( $\text{CuO}$ ) were studied with observation of photoelectron and Auger lines from XPS spectra [1,2]. This investigation enabled distinguishing the copper metal from copper oxide based on the Cu LMM Auger line in the XPS spectra. As a result, **Figure 6** shows that no statistical differences were observed in copper oxide formation at substrate interconnect structure based on the different conditions evaluated for process improvement. Data points were collected and measured via XPS across the diagonal

surface of a specially prepared squared-shaped test vehicle to compare any variation in atomic concentration of copper oxide values.

## Summary

ToF-SIMS and XPS were used as complementary surface-sensitive analytical tools to methodically investigate organic contamination at an anomalous substrate interconnect structure. These surface-sensitive tools enabled a path to circumvent the inability for full disclosure of the source of the organic contamination due to supplier intellectual property restrictions. The chemistry obtained from ToF-SIMS and XPS at the anomalous substrate interconnect structure provided a blueprint to map the chemical functionality to components in the MSDS to discover the source of the organic contamination. ToF-SIMS analysis was carried out on neat materials associated with two process steps in the front-end of the FCBGA substrate manufacturing process, which were suspected as the

source of the organic contamination. Surface analysis results provided corroborating details to the root cause of organic contamination as the chemistry of the neat materials matched the chemistry at the anomalous substrate interconnect structure. These findings enabled a process improvement to be implemented. XPS was used to quantify the atomic concentration of carbon at the anomalous substrate interconnect structure to understand the magnitude of the organic contamination across multiple process lots. To ensure the process improvements did not cause any deleterious effects in the quality of the substrate interconnect structure, the atomic concentration of copper oxide was studied via XPS. XPS confirmed no statistical difference in copper oxide formation before and after process improvement.

ToF-SIMS and XPS are well-known surface-sensitive analytical tools used in various aspects of microelectronics characterization at both silicon and package levels. Each tool has specific outputs based on the fundamentals of its application, but when used in tandem, its synergy can find

the proverbial needle in the haystack where chemical identification can be impeded due to proprietary restrictions.

## Acknowledgments

The author would like to acknowledge the Physical Electronics team and Aaron Clubb of Texas Instruments for surface analysis support.

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## Biography

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# Total control of the bump process to ensure reliability of stacked devices

By Matt Wilson *[Rudolph Technologies, Inc.]*

**A**s electronic devices become ever more pervasive in our daily lives, ensuring their quality and reliability has become not just desirable, but in some cases, a life or death requirement—consider the possible consequences of a catastrophic failure in a medical device or the control system of an autonomous car. Electronics manufacturers are under growing pressure to build quality and reliability into their devices and that pressure is magnified by the increasing criticality of the applications. Although this is not a new demand, it is made more challenging by the appearance of new process and packaging technologies that pack greater functionality into less space through vertical integration. All of these technologies require connections in the third dimension, above or below the die, thus adding, quite literally, a new dimension to inspection and metrology requirements.

## Reliability

Consumer tolerance for device failure is at an all-time low, as they demand more functionality and more convenience from their electronic devices. The results of failure range from minor inconvenience – a wait in a long line because a dead cell phone could not retrieve a boarding pass – to catastrophe from a failed pacemaker or wrecked car. The automotive industry is an excellent example. Its relentless focus on reliability is driven not only by the cost of failure in human terms, but also by market forces such as costly recall and foreign competition implications. When cars contained only a few electronic components, a failure rate of one in a million might have been acceptable. Autonomous cars may each have tens of thousands of electronic components, making one-in-a million not nearly good enough.

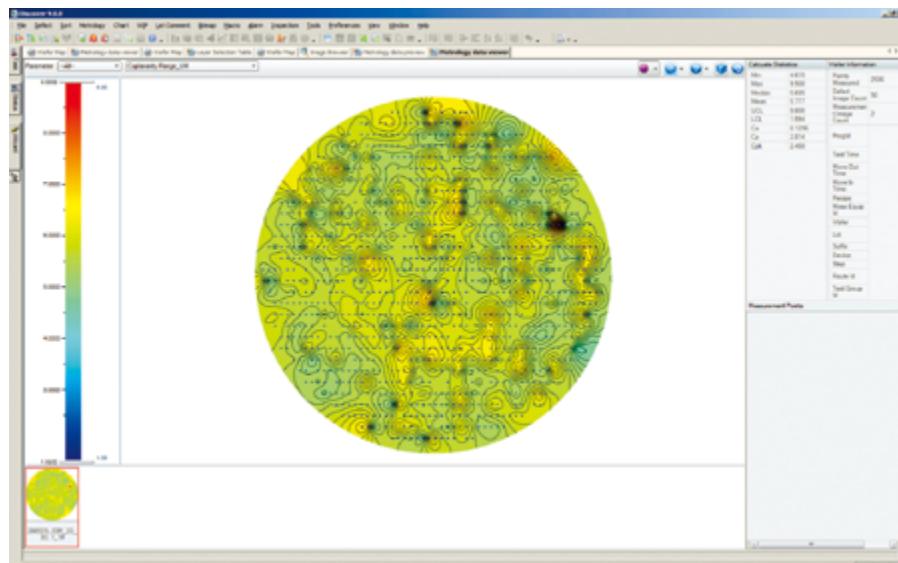
## Vertical integration

The microelectronics industry has followed a familiar narrative since its birth—put more computing power and functionality in less space; only now it has entered, quite literally, a new dimension—vertical.

Packaging these vertically-integrated die requires the need to provide interlayer connections that are as small and reliable as the multilayer interconnect technologies used within the chip. This need for vertical connections has created a whole new class of technologies – advanced packaging – with a whole new lexicon of terms (and acronyms): through-silicon vias (TSVs), redistribution layers (RDLs), bumps, pillars, nails, under bump metallization (UBM), wafer-level packaging (WLP), fan-in, fan-out, and many more. All these technologies serve the purpose of providing reliable, electrically isolated, vertical connections, and most, at some point, involve the creation of a conductive “bump” protruding through an insulating layer to carry the signal to the next layer above or below.

## Total bump process control

As these bumps have become smaller and denser, fabricating them reliably has required the adoption of process control technologies, including extensive inspection and metrology. Total bump process control refers collectively to the 2D/3D inspection and metrology requirements of this class of technologies. Controlling these processes is critical to ensuring the reliability of the finished device and requires the combination of standard 2D techniques with a new class of 3D technologies. As dimensions shrink, repeatability and resolution requirements will increase, surpassing the capability of white light techniques and requiring the use of laser-based technologies. But total bump process control requires more than just new sensors, it requires a comprehensive approach using advanced analytics—distilling classified, usable results from the torrent of raw data created by these new technologies. As shown in **Figure 1**, software to visualize bump coplanarity gives users a powerful tool to quickly assess various bump heights within a set tolerance. In addition, inspection and metrology systems must have the flexibility to control

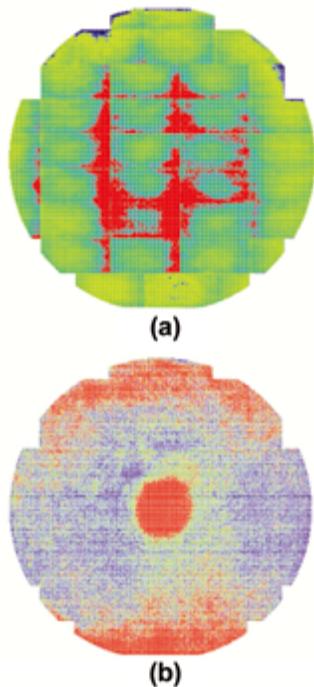


**Figure 1:** Coplanarity wafer map visually alerts users when bump height tolerances are too high or too low.

all kinds of bumping-related processes: wafer-level chip-scale packaging (WLCSP), ball drop, micro-solder, Cu pillar, RDL height, UBM height, and more.

Total bump process control requires both 2D and 3D technologies to fully understand the process (**Figures 2-3**):

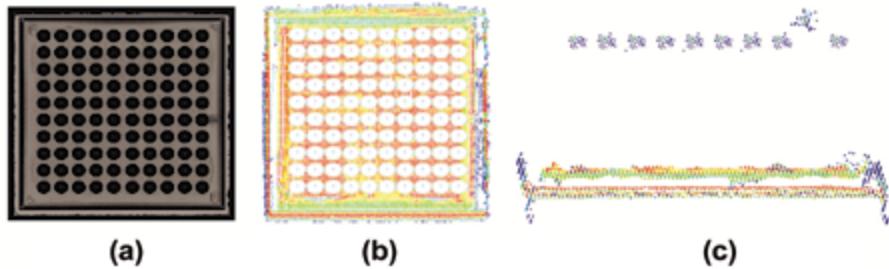
- 2D defect detection – voids and shorts, foreign material, misprocessing;
- 2D metrology – bump diameter, bump position, bump presence;
- 3D inspection – bump too tall, bump too short, statistical process control (SPC); and
- Auto classifications – data must make sense and be easy to interpret.



**Figure 2:** a) 2D bump diameter summary; b) 3D bump height summary.

#### Resolution: TSV in stacked memory

Feature sizes continue to shrink in all dimensions, requiring ever-increasing resolution capability for inspection and measurement. TSVs are no exception. Although TSVs have not found the broad application they were initially expected to achieve, they have been embraced by memory manufacturers in devices that stack multiple chips to achieve increased storage density. One type of TSV process creates the TSV by etching the via, filling it with conductor and then revealing the TSV with a backside polishing process. The



**Figure 3:** a) Sample die with bumps; b) die data view (top); and c) die data profile view showing that the bump is too tall.

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The advertisement features a large metal DDR GHz socket component on the right, showing its complex internal contacts and mounting hardware. To the left, a green printed circuit board (PCB) is shown with a square chip carrier package mounted on it. A circular logo in the bottom right corner contains a checkmark and the text "RoHS". At the bottom, there is contact information: a stylized 'i' logo, the text "Ironwood ELECTRONICS", the phone number "1-800-404-0204", and the website "www.ironwoodelectronics.com".

height of the revealed TSV nail is critical. In advanced processes, the height may be only a few microns with a diameter of less than 10 $\mu\text{m}$ , requiring a laser-based optical system. In this case, white light provides insufficient resolution and throughput.

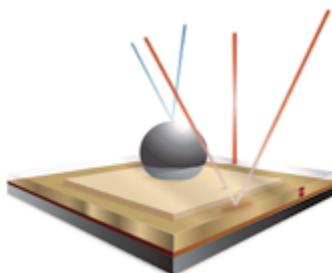
### Determining true bump height

Solder bumps are another technology used for vertical connections. They achieved wide acceptance in flip-chip processes and are transitioning to wafer-level chip-scale packaging (WLCSP). Some recent predictions have WLCSP surpassing conventional flip-chip as soon as 2018. Widely known, bump height and coplanarity are critical to ensuring reliable connections. A bump that is not high enough will not connect, while one that is too tall may prevent connection by neighboring bumps. Even the slightest bump height variations can cause weak connections leading to detrimental field failure at the consumer level, becoming more costly in the end through recalls and field returns.

Bump height measurement has become more challenging with the introduction of processes that eliminate the UBM layer, which is used in conventional WLCSP to improve the bond between the solder ball and the copper redirect pad. WLCSP packages have been limited in chip size and ball pitch by the fragility of the solder ball/redirect connection. The intermetallic compounds (IMC) formed there are mechanically weak and subject to fracture under the thermally-induced mechanical stress generated by the different expansion coefficients of the silicon die and the package substrate. UBM-free integration (UFI) eliminates the UBM and the solder connects directly to the redirect pad. A thick polymer protection layer (PL), usually polyimide (PI) or polybenzoxazole (PBO), helps secure the solder in place and provides stress relief between the chip and the substrate. In addition to eliminating the IMC as a source of failure, UFI reduces package cost and cycle time by eliminating layers, and allows a significant reduction in final package thickness. Unfortunately, the PL layer, which is semitransparent and varies in thickness, introduces errors in bump height measurements [1].

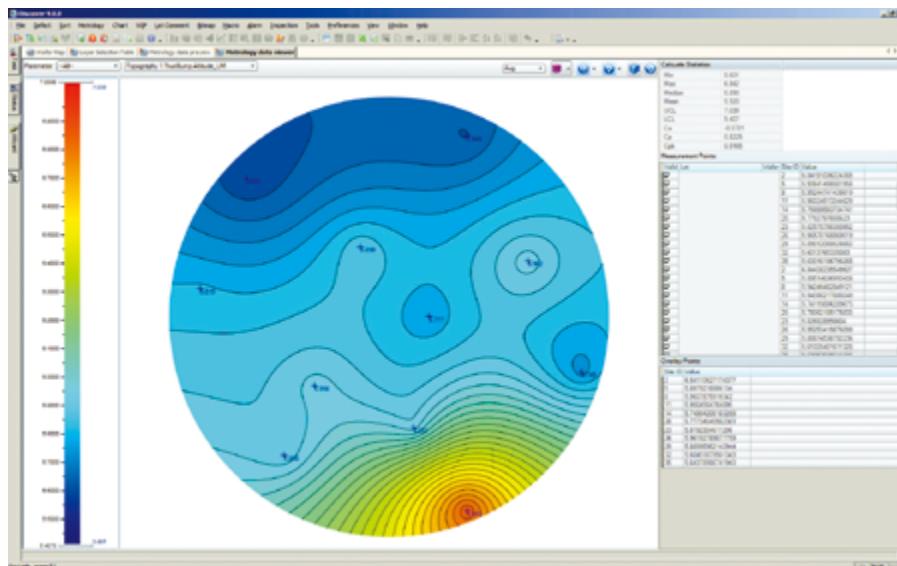
A new approach to bump height measurement uses an interferometric technique to accurately measure bump height and PL thickness at representative locations across the wafer, and then calculates offsets to apply to subsequent high speed, 100% inspection (Figure 4).

The laser-based sensor combines the principles of interferometry and reflectometry to accurately detect the top of the bump, the top of the PL and the bottom of the PL. It

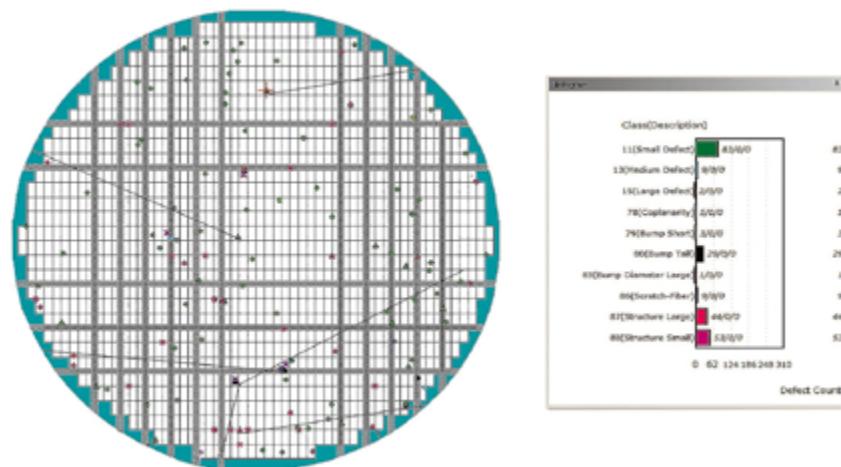


**Figure 4:** Laser-based measurements of the bump through the protection layer gives accurate bump height where white light techniques fail.

can also measure step heights at the edges of opaque materials underlying a transparent layer. The sensor is capable of nanometer scale accuracy and repeatability. It is particularly strong, relative to other measurement technologies, such as chromatic confocal (CC), in its ability to measure thin films. As films become thin, the intensity peaks returned by CC measurements begin to overlap, making it difficult to distinguish top and bottom. PL films are typically in the 3-6 $\mu\text{m}$  range—too thin for accurate CC measurements. In contrast, the peaks returned by the laser-based sensor are sharp and easily distinguished on films of this thickness. Figure 5 shows results of the true bump height measurements amid the PL, accurately measuring from the top of the bump to the bottom of the PL.



**Figure 5:** Bump height wafer map returns accurate bump height measurements amid the protection layer.



**Figure 6:** Automated binning and classification delivers easy to interpret charts and wafer maps call attention to problem areas.

## Throughput

3D inspection has typically been a bottleneck for process control in advanced packaging. To achieve broad acceptance, 3D techniques must achieve production-worthy throughputs. The higher frequency/shorter wavelength of the new laser-based sensor and the elimination of the spectral noise generated by broadband (white light) technologies not only improves resolution, but also greatly increases throughput. The laser-based technique can offer throughput up to twice as fast as pre-existing technologies that have been broadly available and accepted in the market to date.

## Repeatability

As dimensions shrink, so also do repeatability requirements for measurement systems. Generally, to be considered “gauge capable,” a system must demonstrate  $3\sigma$  repeatability less than 10% of the process tolerance. A  $20\mu\text{m}$  feature with a  $\pm 2\mu\text{m}$  process tolerance requires metrology that is capable of  $0.2\mu\text{m}$  repeatability or better, which is well within the precision capability of the laser-based sensor discussed here. It is not unusual to see precision to tolerance ratios below 5% on many applications.

## Automatic classification and analytics

Metrology and inspection systems can generate raw data at an incredible rate, but the data is useless without advanced analytics that can quickly extract significant, actionable information from the data stream. For inspection, this means automatic classification of detected defects to immediately direct operators’ attention to important process excursions, helping to identify probable root causes and suggest pathways to problem resolution. For metrology, this means real-time binning of measurement data that falls outside of the acceptable range. As shown in **Figure 6**, the ability to seamlessly integrate both classified inspection data and binned metrology data into a single analysis enables meaningful decision-making about process optimization changes.

## Summary

As advanced packaging processes follow the familiar path to smaller, denser features, they will require increased process control to remain within the process window. A unique feature of these processes is the use of bumps to provide vertical connections. We have described the types of inspection and metrology bumps require, and shown results from a new system (Dragonfly™ System) designed to provide the comprehensive 2D/3D measurements needed for total

bump process control. The system includes a laser-based optical system to provide sufficient resolution, new sensors for 3D measurements specific to bump process (Truebump™ Technology), automatic defect classification, extensive data analytics, and can provide production-worthy throughput.

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## Biography

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# Reducing wafer test time

By Klemens Reitinger [ERS electronic GmbH]

**D**uring a typical thermal wafer test set up, the temperature will influence every other boundary condition, like the mechanical accuracy or electrical performance. There are different ways to deal with these influences, but they all require long “adaption times” in which the test cell is just waiting for the system to reach the right temperature. This article will explain why it is so important to generate new solutions that reduce the expensive waiting time in the overall test process, and how ERS’ new thermal wafer test chuck system is designed to improve this longstanding issue. Data and discussion about a new generation of thermal chucks will be presented that will confirm how the technology can help shorten the time needed for a test set up to be “ready for test.” The article concludes with a discussion of the outlook for the future of semiconductor testing in general, and also as it relates to emerging products such as microelectromechanical systems (MEMS) and sensors.

## Background discussion

Wafer test is an integral part of every wafer fabrication line today (**Figure 1**). There are numerous steps performed on a silicon wafer – 300mm diameter being the industry standard today – until the devices are fully functional. A common characteristic of all these process steps is that they are performed at the wafer level, so every process step creates

hundreds or even thousands of chips, which is cost-effective. However, as soon as the wafer is singulated into individual devices, the subsequent development becomes substantially more expensive. The next steps are usually performed on a tiny piece of silicon, which is a time-consuming process operated by intricate and costly machinery.

To know the status and performance of every die on the wafer previous to singulation is an important element to improve yield. Therefore, the wafer has to go through a process called wafer test, that ensures that only the good dies are further processed. The wafer test is performed in a test cell, which consists of an electrical tester (the most expensive piece of equipment), an electromechanical interface to the wafer (a probe card), a wafer chuck (in this case, the source of temperature for the wafer test) and a wafer manipulator, also called a wafer prober. As we are talking about semiconductors, it is obvious, that temperature is a key parameter for this test. Today, there are many tendencies suggesting that temperature is getting more and more important, and that, at some point it may even become the most important parameter of all. Additionally, the temperature range is getting wider and wider, as many of the microelectronic devices are now being used in rougher environments, for example, for autonomous driving, Internet of Things (IoT), or power electronics for regenerative energy harvesting.

However, dealing with temperature is one of the less explored areas in electrical testing of a device, one of the reasons being that a testing process usually means a lot of nonproductive time. In the past, the test time was very simply calculated by the time the chuck needs for the temperature transition, e.g., from 25°C to 200°C. Now, as the structures are getting

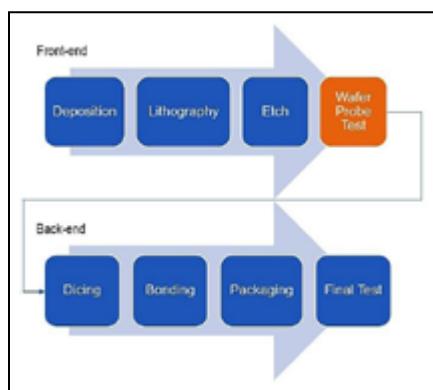
smaller and smaller, the simple transition time of the chuck is subject to temperature influences that significantly slows down the process. With an increasing demand for smaller measurements, the industry is now facing complex challenges to a much greater extent than before.

## Mechanical accuracy

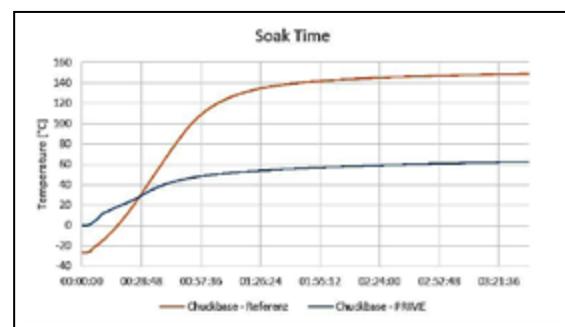
If you change the temperature on the chuck top from 25°C to 200°C, the environment, especially the bottom side of the chuck, will also get very hot. This leads to mechanical thermal drift in the area of the wafer prober and probe card. One might think this temperature range is too “small” to have any major effect on the wafer test, however, this is not the case.

The linear coefficient of thermal expansion (CTE) for different materials is very low, especially for ceramics or metals. The value for stainless steel is  $14 \times 10^{-6} \text{K}^{-1}$ , which means that by changing the temperature of a 1mm piece of steel by 1°C, the length will change by 0.000014mm. This might not sound like a lot, but if you calculate a temperature change of 100°C on a 100mm long device, it will amount to a 0.14mm change, which is 140µm. If you assume that a pad size of 50µm has to be contacted by a needle, it becomes obvious that this is far too much for a stable operation.

Today, there are multiple ways to deal with the problem noted above, and the



**Figure 1:** A typical semiconductor manufacturing process.



**Figure 2:** Soak time comparison of a regular chuck system and the new solution.

three most common ways are: passive shielding in the wafer prober or at the probe card, pre-soaking, and optical realignment to contact the pads after temperature change. The AirCool® PRIME solution goes one step further: an active, dynamic shield is integrated inside the wafer chuck and eliminates the influences of temperature directly at the source. The result is a much lower heat dissipation into adjacent parts that significantly reduces the time needed to reach the thermal balance (**Figure 2**).

Although the solution described above improves the accuracy of the machine, it does not manage to get rid of the problem entirely, as the heat transferred from the chuck top/wafer into the probe card is still there. To avoid this from occurring to such an extent, the aforementioned active shield can be attached to the probe card or the wafer prober's head plate to considerably reduce this influence. Field studies have shown that the number of realignments can be reduced from 71 realignments to 13 realignments per wafer. The shield, called DTS (Dynamic Thermal Shield), is different from passive thermal shielding in that it reacts to the position of the hot chuck during probing. Because this position is very hard to predict, the passive shieldings are only able to reduce the temperature influence, and can therefore not fully cool down the overheated areas. When you are able to cool the probe card exactly at the position where the heat is brought in, you can avoid a nonuniform temperature distribution and provide mechanical stability (**Figure 3**). These examples show the thermal impact on mechanical behavior. But there are more issues to discuss as noted below.

## Electrical accuracy

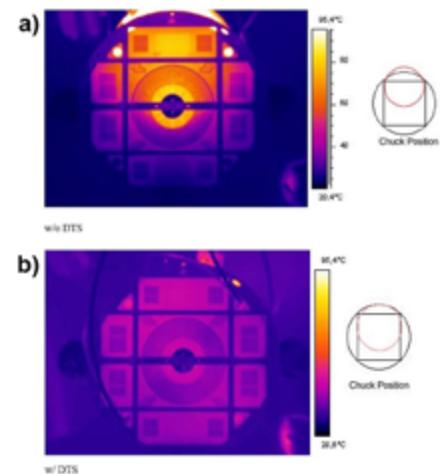
Some of the devices tested in wafer test are highly sensitive. Very low currents are measured, sometimes as low as into the femtoampere range, which is  $1 \times 10^{-15}$  A. To achieve this ability, both components close to the wafer (the thermal chuck and the probe card) use very advanced materials for electrical isolation and shielding. Common to all these materials, which are mostly highly-engineered plastics or ceramics, is the degrading of their electrical properties at higher temperatures. Alumina ceramic, for example, has a specific resistance of  $1 \times 10^{12} \Omega\text{m}$  at 20°C and only  $1 \times 10^{10} \Omega\text{m}$  at 200°C—only one hundredth of its desired value. This means that if you cannot reduce the temperature influence of the required test temperature, the electrical performance of the whole system will rapidly decrease.

There are materials that have good electrical properties at elevated temperatures. However, the disadvantage of these materials is their hygroscopic behavior, meaning the tendency to absorb/attract moisture from the air. Consequently, if customers want to take full advantage of the electrical performance, they will first have to “bake” their chucks at high temperatures until all humidity is removed, which, again, is a very time-consuming task. With the new AirCool® PRIME technology, thanks to the dynamic shielding and thermal isolation, the “pollution” of heat in the environment is reduced. Additionally, the new solution offers a controlled environment inside the wafer chuck, which eliminates the need for tedious baking cycles.

## Temperature accuracy

The current IC devices need much higher absolute temperature accuracy during testing. This is not only true for temperature sensors—there are also a lot of other devices that require a high-temperature precision while being tested for other parameters. Think of pressure, gas or humidity sensors—all these measuring sizes are very strong depending on temperature.

During a test, equipment touching the wafers (needles or contactors) or other activity in close proximity to the wafer,



**Figure 3:** a)Comparison of thermal impact on mechanical behavior between a chuck without, and b) with the Dynamic Thermo Shield.

will affect the temperature accuracy of the device, especially at higher test temperatures. For example, if you test at +150°C with a contactor contacting the device with more than 200 needles, the first device tested will surely have a lower test temperature than the last

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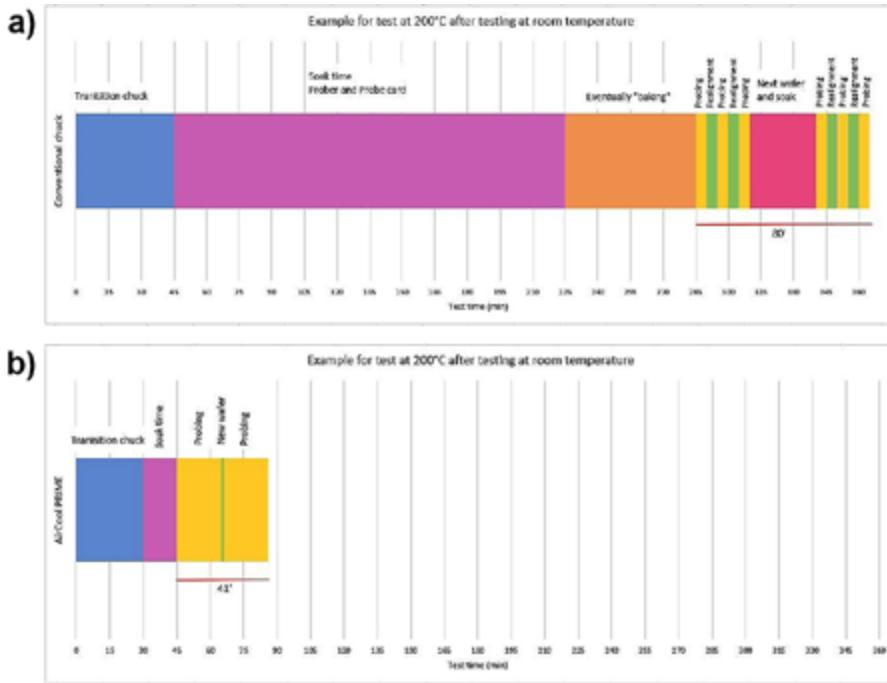
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**Figure 4:** Total time needed after temperature change for the chuck to be ready-for-test: a) comparison of a regular chuck, and b) the new solution.

one, just by warming up the needle during the test. Furthermore, air flow around the wafer can have an effect on the temperature accuracy across the wafer. As in a chimney, cold air will flow at the edge of the wafer and will cause lower temperatures than in the center of the wafer.

### Thermal Transition Time

Of course, the thermal transition time of the chuck itself is still a big portion of the idle time of the test equipment. In a production environment, it is typically less important because the test temperature is rarely changed compared to the volume of wafers tested. However, reducing waiting time from one hour to 25 minutes, might still be considered a significant difference.

In analytical probing, during characterization or in development labs, the amount of waiting time is critical. One device is frequently tested at different temperatures, and therefore the transition time has a big influence, and may even determine whether a test can be made in one day instead of two.

With our technology, this transition time is kept as low as possible (**Figure 4**). The thermal mass in the chuck is kept low and the already described shielding technology gives

an additional impact. As the parts close to the chuck are getting less hot, they consequently are not using the energy for heating, which means all heating energy can go directly into the chuck top, ultimately reducing the transition times.

All the issues noted above were taken into consideration when we were working on the AirCool® PRIME design. Additional components, like the aforementioned DTS, or a cooling device, can be connected to the PRIME temperature controller and thereby take care of environmental influences such as the probe card temperature. A special thermal guard is implemented into the chuck design to eliminate the temperature difference between the center and the outside ring of the chuck at high-temperature tests.

### Summary

There are indications that temperature test at the wafer level is getting more important than ever. Additionally, new products for automotive, IoT and renewable energy have to be tested over a very broad temperature range. All the present solutions on the market that deal with the challenges resulting from this need for temperature testing are mainly made by machine manufacturers. What

these solutions have in common is that they try to deal with the influences that the temperature creates. A lot of these solutions are optics (camera and realignment of the position) in combination with software. You can, for example, program a machine to optically check the contact's position from time to time and make an automatic correction if the contact is in the wrong position.

Another possible solution is the so called "pre-soaking," where all machine components are brought to the expected final temperature, e.g., by external heaters.

The current solutions are therefore relatively time-consuming workarounds, like optical realignment, software compensation and automated soak time calculation. In addition, most of the available solutions today are not dealing with the heating problem at its source. The concept of our solution is different: it practically removes the disturbing effect of the temperature to the whole set up and offers additional control features for the components close to the device under test.

We think that, with this method, the time needed to be ready for test after a temperature change, will be considerably shorter. Additionally, we believe it will create the mechanical, electrical and thermal accuracy needed for future products.

We expect that a lot more chip testing will be moved to wafer test. As the packaging of such components is a quite expensive process, we assume that the importance of testing devices before they are further processed, will increase. We also expect an increase in demand for temperature testing at the wafer level. The range will increase from todays -40°C up to +150°C, to -55°C up to 250°C, or even above. A concept that deals with the temperature influences at its source and not with the heat distribution will most likely be able to offer better and faster solutions.

### Biography

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# The “More than Moore” semiconductor industry is changing the transportation paradigm

By Jérôme Azémar, Guillaume Girardin, Yohann Tschudi [Yole Développement]

Over the past one and a half centuries automobile technology has revolutionized many industries and impacted the evolution and creation of new trends in our daily lives. Today, another revolution is in progress in the automotive world, with a race for “More than Moore” semiconductors, that started just a few decades ago.

What's been happening with automobiles over the years? The semiconductor industry has started to flood cars with electronic injection chips, partly in response to environmental efficiency requirements. This was followed by security features, which have been the biggest driver ever since, with the addition of anti-lock brake systems (ABS), electronic stability control (ESC), tire pressure monitoring systems (TPMS), etc. The new trend for electrification has given a new thrust to the automotive semiconductor market by trying to solve the environmental issue for good. The advent of digital connectivity with smartphones has given rise to new business models and a different approach to the transportation

paradigm, with its opportunities for shared mobility (Figure 1). This leads us to the fashionable autonomous car, which is seen as the Holy Grail of the automotive market, but the situation is considerably more complex than was first thought. Two major automotive trends are evolving in parallel.

**First, automated cars “as we know them.”** Based on our traditional automobile, these vehicles will evolve through different stages of automation, from level 1 to level 5, through the addition of pre-embedded sensors, including radars and cameras, and new ones such as light detection and ranging systems (LiDARs), helped by powerful computing capacity that will solve problems and ensure the car reacts effectively to any situations occurring on the roads. These features, known as advanced driver assistance systems (ADAS), are currently focusing all the attention of original equipment manufacturers (OEMs) and tier one suppliers.

**Second, there are “robotic cars.”** Based on a robotic approach, these cars are being developed by Google, Uber,

Lyft, and Baidu and will address new types of use. Born as a level 4, or even 5, these “sensitive” robots are created with one objective: to fulfill the autonomous driving (AD) requirements of being able to drive everywhere, as a new type of personal transportation. These vehicles are expected to become fully operational in restricted areas before evolving to a true level 5 (Figure 2). Autonomous driving is arguably the most exciting development in the industry today and the future of the automotive industry is clearly to address these new challenges.

## “More than Moore” semiconductors for sensing

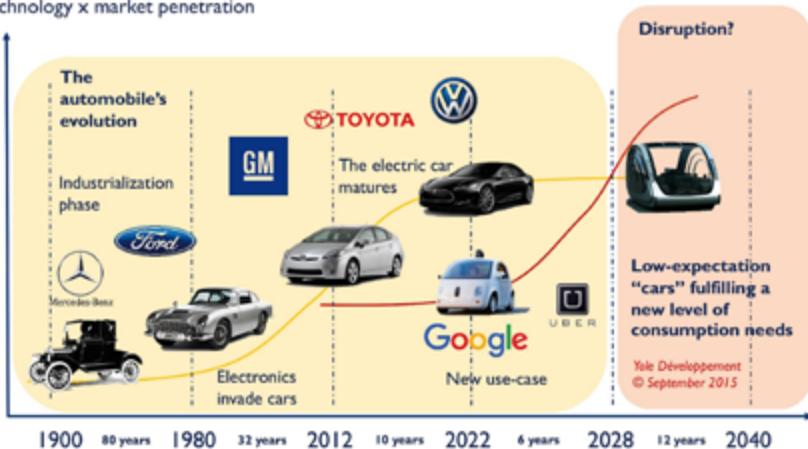
Let's take a look at the current battlefield. A majority of automotive industry players are currently developing sensor-based solutions to increase vehicle safety in high and low speed zones. These ADAS systems use a combination of advanced sensors combined with actuators, control units and integrating software. They enable the driver and car to monitor and respond to the surroundings. Some ADAS features are already available. These include lane keeping assist (LKA) and lane keeping warning (LKW), adaptive cruise control, back-up alerts and parking assistance. Many others are still under development. To reach the fully-automated level, advanced sensors combined with actuators, control units and integrating software will have to be fully mastered. Sensing, computing and actuating are the three major blocks at the heart of this revolution. Let us focus on the first two, as automotive players have already mastered the last one.

For many years, the semiconductor industry has been focusing on the “Moore approach.” The advent of the “More than Moore” semiconductor industry has led us to the sensing era and the proliferation of sensors in the



Figure 1: "Automotive market macro trends;" SOURCE: Imaging Technologies for Automotive report, Yole Développement, 2016.

Technology x market penetration



**Figure 2:** Automotive evolution: from the Ford Model T to autonomous vehicles. SOURCE: MEMS & Sensors for Automotive report, Yole Développement, 2017.



**Figure 3:** Big picture of LiDAR market opportunities timeline. SOURCE: MEMS and Sensors for Automotive - Market and Technology Trends report, Yole Développement.

automotive and consumer space. Indeed, the number of sensors used to perform ADAS functions in cars is expected to increase from 12 sensors on average per car, to 25 sensors per car by 2030. The current big picture of the market shows equal revenues from the US\$ 3 billion radar and US\$ 3 billion camera businesses, enjoying a 20% and 24% compound annual growth rate (CAGR), respectively, over the next five years [1].

### Growth in ADAS was primarily the result of camera use

Cameras were initially mounted for ADAS purposes on high-end vehicles, with deep learning image analysis techniques promoting early adoption. Israeli company Mobileye has been instrumental in bringing this technology to market, along with ON Semiconductor, which provided

the CMOS image sensor. Copycat competition will probably pick up as the market now justifies initial investment in design and technology. It is now a well-established fact that vision-based auto emergency braking (AEB) is possible and saves lives. Adoption of forward ADAS cameras will therefore accelerate. Growth of imaging for automobiles is also being fueled by the park assist application, and 360° surround view camera volume is therefore skyrocketing. While it is becoming mandatory in the United States to have a rearview camera by 2018, that uptake is dwarfed by 360° surround view cameras, which enable a “bird’s-eye view.” This trend is of particular benefit to companies like Omnicron at the sensor level and Panasonic and Valeo, which have become two of the main manufacturers of automotive cameras.

### Next came radars...

Radar-based sensors are among the oldest addressed by the automotive industry and have been embedded in vehicles for almost 30 years. For the record, in 1989 Toyota was first to introduce a blind spot feature using radar detection. However, due to performance limitations (field of view) and reliability issues (mechanical parts), radar-based sensors have not had much success in the automotive field so far. Since then, radar-based sensors have evolved, thanks to the solid-state approach combined with beam-steering and beam-forming technology. With frequencies from 24GHz or 77GHz, and even 79GHz for more accurate object detection, combined with a SiGe or CMOS approach, we anticipate good growth for the radar business in terms of both technological opportunities and financial revenues. Finally, the ultimate configuration for autonomous cars could present four adaptive CMOS-based radar-based sensors at 77/79 GHz, each with a 150° field of view, for short/medium/long range detection covering all the car’s surroundings. From US\$3 billion by 2017, we expect a US\$6 billion market value by 2022, mostly driven by ADAS features such as AEB, ACC and blind spot detection.

### ...and LiDARs

LiDARs are currently undergoing a technological and industrial revolution, thanks to companies like Velodyne, Quanergy and SensL. This major component of Level 4 and Level 5 driverless cars is in very short supply. Many OEMs from around the world are racing to fill the LiDAR production, price and performance void, either by organic development, inorganic development, or acquisitions, which have escalated in recent months as follows:

- November 2017: Innoviz Technologies extended Series B funding to US\$73 million;
- October 2017:
  - General Motors acquired Strobe, a start-up focused on driverless technology;
  - Autoliv acquired Fotonics, a LiDAR and time-of-flight (ToF) camera specialist;
  - Ford acquired Princeton Lightwave, makers of LiDAR sensing

devices, one year after it had invested in Velodyne;

- August 2017: Oryx Vision raised US\$50 million to build a groundbreaking coherent LiDAR for autonomous vehicles;
- July 2017: Osram invested in LiDAR expert LeddarTech;
- May 2017: TriLumina collaborates with Analog Devices on a next-generation flash LiDAR illumination module; and looking ahead, perhaps more to come.

Production of LiDAR sensors is seeing months' long production bottlenecks, and suppliers are finding it difficult to deliver the technology on time. Currently, most of the solutions available are based on a mechanical approach (microelectromechanical [MEMS] micro-mirrors and prisms), but progress is being made thanks to a solid-state approach, which is expected to drive down the solution's cost. By becoming solid-state, they can be considered as true imaging devices, and cost reduction will be a key driver as the push for semi-autonomous driving is felt more strongly by car manufacturers. As the price point of LiDAR-based systems will fall quickly, they will consequently be adopted by the top end of the automotive market (**Figure 3**). They will become central to vehicles with semi-autonomous features, with a market value forecasted at US\$7 billion by 2030.

#### **...and then there is computing**

Even when the sensing block is fully mastered, only half of the problem will be solved (**Figure 4**). The amount of data sent by the sensors has to be dealt with/analyzed and, as a consequence, a command must be selected. This is where the computing block plays a leading role, supported by a whole new artificial intelligence (AI)-based technology. For the past few years, improvements in AI technologies have made it possible for machines to perform heavy-duty computing tasks. However, this situation still needs high-performance computing, and the need to couple multiple and redundant information from completely different types of



**Figure 4:** ADAS\* growth and value. SOURCE: Smart automotive: latest trends in LiDAR & sensors - A SEMI & Yole Développement webinar, 2017.

sensors has led to a sensor fusion approach (see **Figure 5**) adopted by giants like Intel, Renesas, Nvidia and Qualcomm/NXP. The ecosystem is growing rapidly, with innovative fusion methods and incredibly high computing performances, but there is

still much to be done. Indeed, because most of them use cameras as primary information gatherers and radars and/or LiDARs for redundancy, low luminosity, or bad weather conditions are still a huge challenge to reaching Level 5 autonomy.

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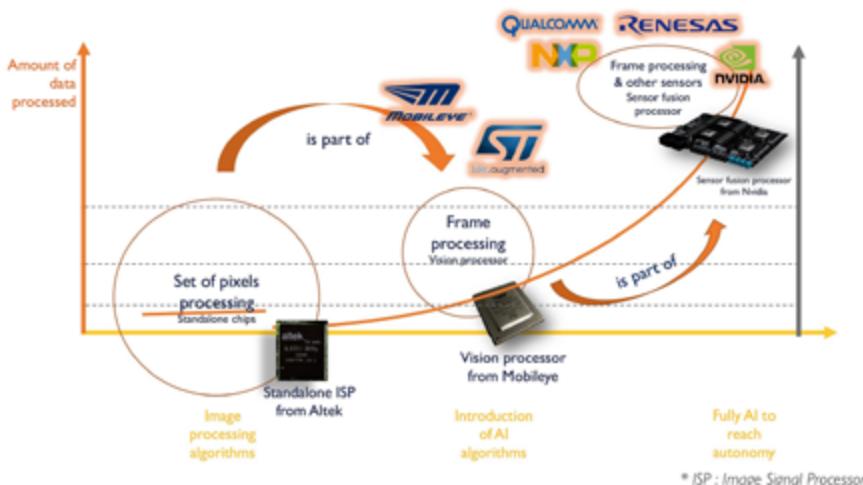
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**Figure 5:** From ISP\* to sensor fusion processor. SOURCE: Smart automotive: latest trends in LiDAR & sensors - A SEMI & Yole Développement webinar, 2017.

### Packaging challenge requires mastering talent to solve this giant puzzle

With the development of new sensing and computing capabilities, electronic module perception is going one step further. And going one step further implies major changes and challenges regarding the packaging too. This had been observed by many players in the advanced packaging business. Many questions remain unanswered, however, such as how to integrate the complexity and diversity of needs while satisfying automotive specificities and high standards. Indeed, packaging, and more generally microelectronics, have been significantly focused on the mobile industry in recent years, and, consequently, associated innovations were too. Unfortunately, these innovations do not suit the harsher automotive environment and the higher need for lifetime reliability and performance, the consequence of an application dealing directly with human safety.

With larger volumes of electronics in the automotive industry and a more diverse range of electronics to embed, packaging solutions will have to evolve in order to address demanding requests. The changes have already begun in some areas: an illustrative example would be the spread of fan-out packaging for radars. The move towards SiGe-based radars, as mentioned earlier, did not only occur at the IC level. In order to benefit from the high-frequency capabilities of SiGe chips, leading companies

such as Infineon and NXP pushed for optimization at the package level too. Additionally, fan-out packaging was introduced together with SiGe, replacing gold-based wire bonding packages that were more expensive and offered lower performance. The automotive industry being a cautious market, this technology took several years to penetrate, but has now convinced major radar suppliers and created a sustainable business. Infineon aims to ship 30 million fan-out packaged chips in 2018.

The evolution and focus of the automotive industry in terms of packaging will be more and more critical in the coming years because acceptable performance and cost will be achievable only with optimum packaging platforms. Following the trends in applications described earlier in this article, it will take different directions as noted below:

- Automated cars “as we know them” will require improvement of existing packaging applications. Electrification of cars has already seen efforts being made at the powertrain level, with power module packages for start and stop systems, hybrid car traction, and soon, more widely, for fully electric cars. Radars will keep improving, with small form factor, high electric performance and high integration solutions. Fan-out is a good candidate at the moment. Sensors in general will require better packages that can interact with the environment while being reliable

and cost-efficient. In general, the trend in the automotive industry is to have increasing integration of different components/functionalities in one system, and this trend will be addressed by system-in-package (SiP) technology. Some existing platforms like quad flat no-lead (QFN) are being further developed to address these integration needs.

- For “robotic cars,” and, more generally, highly connected and highly autonomous cars, processing power will become a priority. This will be achieved through state-of-the-art packaging solutions, enabling optimum connections between components for higher bandwidth and lower latency. In this area, 3D through-silicon via (TSV) packaging and 2.5D approaches are very likely to appear, while numerous cost-reducing alternatives (fan-out on substrate, etc.) are currently under investigation.

Technical breakthroughs are expected in the automotive industry in order to sustain high expectations for the cars of tomorrow—and they are starting to appear. Exciting times are coming and Yole Développement will follow them closely.

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### Biographies

Jérôme Azémar received his Master’s in Microelectronics and Applied Physics and is a senior member of the Advanced Packaging & Manufacturing team of Yole Développement; email azemar@yole.fr

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Dr. Yohann Tschudi has a PhD in High Energy Physics and a Master’s degree in Physical Sciences from Claude Bernard U; he is a Software & Market Analyst at Yole Développement, and is a member of the MEMS & Sensors business unit.

# Epoxy adhesives: mechanical versatility by design

By Jonathan Knotts, Daniel Morgan /Creative Materials, Inc.]

In a world held together in metals and plastics, epoxy is a recurring theme. Many people, even industry professionals, use the term epoxy and adhesive interchangeably. Epoxies are used in a wide variety of applications including medical, aerospace, construction, electronics, and even for home owner projects and repairs. While metals, often used for soldering and welding, can be alloyed or annealed to adjust the mechanical properties, they have a very narrow range in physical properties. Even metals that are more ductile can only tolerate small cyclic elongations. Unlike other materials, epoxies can be customized and tailored based on the individual mechanical demands of the application.

Designing an epoxy for nearly any set of requirements is possible with enough experience and with access to the wide array of ingredients available. Epoxies have an array of uses as they can be designed to be as hard as metal, as soft as silicone, or anywhere in between. This is possible as epoxies are composed of many different sets of building blocks and there are more possible combinations of ingredients for epoxies than any other material used for bonding applications.

Chip-level bonding in microelectromechanical systems (MEMS), optoelectronics, and 3D interconnects requires very specific mechanical properties that are unique to each construction. The variety of materials that are bonded have different coefficients of thermal expansion, surface energies, and are often fragile or are affected by stress.

## Applications using epoxies

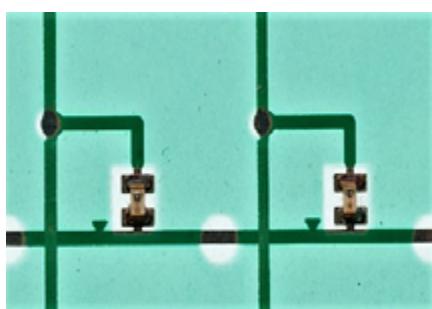
Because of the highly customizable nature of epoxy products, they are used in a large range of applications requiring highly tailored functionality. Epoxies can be modified for increased adhesion to difficult to stick to substrates, such as indium tin oxide

and gold, for potting and mechanical attachment of stress sensitive components, for highly flexible traces, and can be used in electrically conductive, electrically insulating, thermally conductive, or thermally insulating applications (**Figure 1**).



**Figure 1:** Conductive epoxy vias.

Epoxy systems are used in circuit board and other electronics manufacturing to connect and bond components. Electrically conductive adhesives based on epoxy technology are used to connect conductive pads to components in the manufacturing of components, optoelectronics, and chip bonding on circuits. Epoxy materials are also used in the manufacture of printed resistors, static dissipative coatings, and in the manufacture of touch sensors and medical electrodes, and as a seed layer for plating (see **Figure 2**).



**Figure 2:** A chip bonded to conductive circuitry.

Thermally conductive epoxies can be used to insulate and protect conductive traces from stress, abrasion, and harsh chemicals, but can also be used to bond components and housings that require electrical insulation including applications such as hermetic lid sealing, mounting of copper or other heat sinks, and replacing thermal interface materials.

Flexible epoxy systems have much of the mechanical strength of a typical epoxy system, but can enable technologies on flexible substrates such as PET, polycarbonate, Nomex and Kapton for printed electronics and stretchable technologies when properly modified (**Figure 3**). Epoxies have the benefit of increased resistance to abrasion over most other polymers. Epoxies offer benefits such as lower processing temperatures and a wider range of mechanical properties when



**Figure 3:** A rigid LED bonded to flexible traces.

compared to hard materials such as polyimide technology.

Lower modulus epoxy-based chemistries enable potting and encapsulation of stress-sensitive devices and bonding of mismatched coefficient of thermal expansion (CTE) surfaces such as glass and aluminum, gold and nickel, and silicon to polyimide. Fragile sensors, electronics, and other devices can safely be encapsulated by low modulus epoxies. Stress from bonding of materials with mismatched CTEs can be mitigated by bonding with low modulus epoxies.

Epoxies have high thermal stability and chemical resistance, which enables

use in applications requiring extreme exposure to the harshest conditions. Other highly specialized applications for epoxy include adhesives for ovens and thermal analysis equipment, protective coatings for storage tanks, radiopaque marking inks for X-ray analysis, and n- and p-type layers for electroluminescent panels.

## Defects

There are several types of defects that commonly cause failures. Much of the terminology becomes very specific

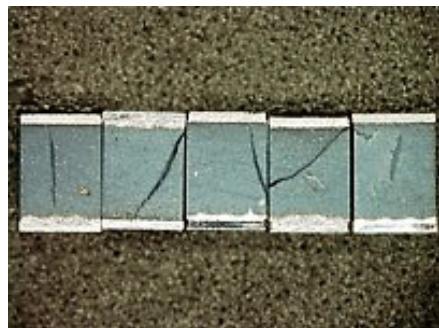


Figure 4: Stress fractures on components.

to the fabricators and assemblers. Common issues include microcracking, delamination, low peel or shear strength, and warpage.

Microcracking is a type of cohesive failure characterized by when separation occurs within one of the materials. When the material pulls away from itself, it allows moisture ingress, which in turn causes loss of mechanical strength or the fracturing of vital components (Figure 4). This failure is prevalent when hard materials and strong bonding are unable to be mitigated or absorbed by compliant materials. The cracks in the material often initiate at stress centers like sharp edges or corners, or planar separations parallel to the bond line.

Delamination is a clean separation at a boundary between the adhesive and one of the substrate surfaces. Delamination is an adhesive failure that occurs when the stress at the interface overcomes the strength of the bonding. Proper surface preparation, substrate porosity, and surface roughness can often be overriding

concerns even when the adhesive is well designed.

Low peel or low shear strength is typically a cohesive failure where the material does not provide required levels of resistance to pushing or peeling forces. It can also indicate a problem with delamination if the bonding is weak (see Figure 5). Rejection due to low peel or low shear is often more of a failure to



Figure 5: Cohesive failure due to poor bond strength.

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meet criteria set by downstream users and is less often a true failure mode realized by parts in use. In attempts to designate the reliability of the bonding, many original equipment manufacturers (OEMs) will require certain levels of shear or peel forces be met by conducting destructive testing of the bonded construction. In assemblies where there are moving parts with bonded connections, these requirements can be indicative of the real performance requirements.

Warpage is a common defect when shrinkage of the adhesive causes a mechanical deformation of a chip or substrate. Warping a device can cause significant changes in performance as signals and outputs will shift as the chip is flexed. Warpage is a common defect when thicker layers of adhesive are used with thinner or weaker substrate materials.

## Mechanics

Consideration for mechanical requirements is critical for performance and longevity of the epoxy and of the part. The modulus of the epoxy will dictate the maximum elongation (strain) or maximum force (stress) that will cause a failure. For parts that are subjected to mechanical forces such as a peeling or pulling action, a higher modulus adhesive is needed to provide the bond strength required to overcome these forces. For materials bonding mismatched CTE substrates and surfaces, a lower modulus adhesive will allow for the higher strains required.

Understanding your application's potential failure modes and identifying the limits for both stress and strain allows for an acceptable range of modulus to be defined.

Many constructions involve delicate layers such as ultra-thin chips. Stress is transmitted from more dimensionally-stable layers to layers with less dimensional stability. The transmission of stress dictates that thickness, as well as the modulus of the bulk material, needs to be taken into consideration. Because the adhesive layer rarely has a function based on the dimensions, it is best to have the stresses absorbed as strain in the adhesive layer. This requires the dimensional stability to be lowest in the adhesive layer. By reducing the modulus of the adhesive, it will compress and elongate to relieve the stress from the surrounding materials.

Most chip-level adhesives are used on components, which will later be bonded into housings or onto boards, where other stresses than shock or vibration mechanical stresses are unlikely. Many of the common failure modes are due to expansion and contraction causing strains. It is possible to match CTEs from lower than 15 ppm/ $^{\circ}\text{C}$  to greater than 200 ppm/ $^{\circ}\text{C}$  (see **Figure 6**) through compositional controls allowing for gaps to be maintained or stress to be managed. If the materials to be bonded have CTE values that are close to each other, simply matching the adhesives' CTE will avoid failures caused by thermally-induced stress. If the substrates have differing CTE values, splitting the difference is often not enough and decreasing the modulus then becomes necessary. Epoxies are also able to take advantage of a property known as the glass transition temperature ( $T_g$ ). At temperatures below  $T_g$ , the modulus is higher, and once the  $T_g$  is exceeded, the modulus drops. When stresses approach a critical limit as a result of temperature change, choosing a  $T_g$  just below the temperature where failures will occur can avoid catastrophic events. This property works similar to a pressure relief valve or expansion tank by allowing for a shift in properties.

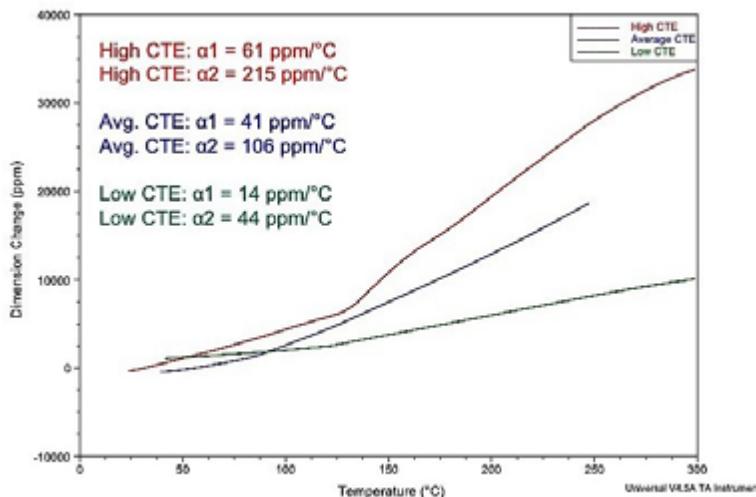
## Epoxy formulation

The potential for epoxy formulations is nearly infinite. Controlling properties through epoxy formulation is possible due to the wide variety of polymers, monomers, oligomers, modifiers, and fillers that are available. It is common for chemists working with epoxy to spend entire careers studying and developing new types of epoxies. The considerations for balancing the requirements for an epoxy are numerous and experienced epoxy formulators draw on generations of experience to finely craft unique and intricate adhesives. Among the mechanical considerations discussed in this paper, properties such as rheology, ionics, cost, cure rate, shelf life, and many others, are important considerations in epoxy design.

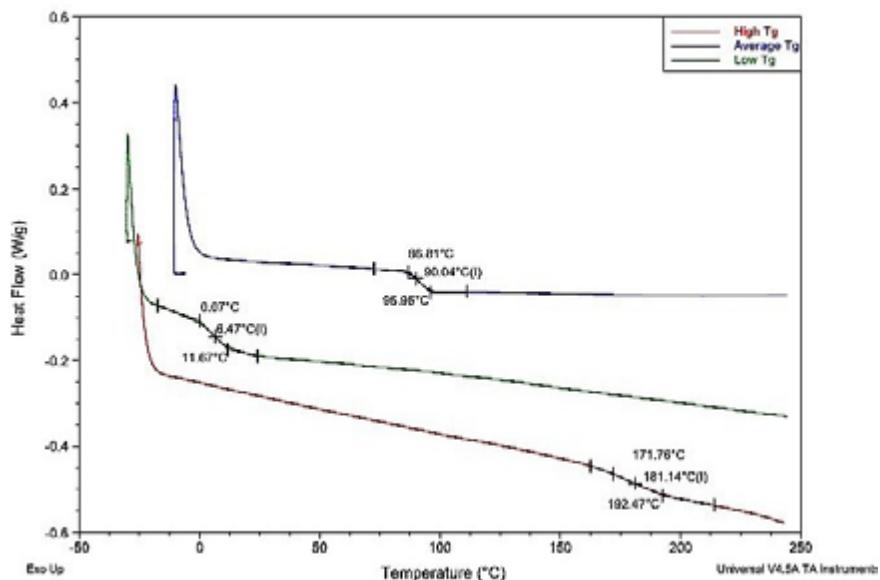
Glass transition temperatures for epoxy can be specified at less than 10°C or more than 180°C depending on the performance requirements. Formulators are able to program the  $T_g$  by restricting or freeing the mobility of the backbone. It is the movement of the polymer chains once thermal energy enables rotation around bonds that moves the epoxy

from a hard, glassy state into a soft, rubbery state. This change does not cause any degradation and moving regularly from one state to the other is not a negative condition. Traditional characterization for glass transition temperature is performed by running differential scanning calorimetry (DSC). Results for  $T_g$  are most clear when running a modulated DSC to ensure the heat of transition is reversible (see **Figure 7**).

The ability to compress the epoxy to a repeatable bond line is limited from a process and equipment point of view, but formulators can include spacers for bond line thickness control. The incorporation of spacers allows the user to compress at a high force and be assured that the spacer will limit the compression to an identical bond line from part to part, and even batch to batch. Removing a bonded part and checking the thickness of the remaining adhesive with a micrometer or by implementing other profilometry techniques allows for easy verification of the effectiveness of using spacers.



**Figure 6:** CTE comparison via TMA.



**Figure 7:** T<sub>g</sub> comparison via DSC.

Cure shrinkage can often be difficult to accurately detect and measure, but casting a larger part will allow for easier characterization. A challenge in making quality test parts is voiding, typically

caused by volatiles in the epoxy system, excess gas from the manufacturing process, or poor application technique. Minimizing the voiding in a part can be achieved with a ramped cure

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schedule, degassing the material prior to application, and with care in the application of material. It is possible to increase or decrease the shrinkage of an epoxy by two mechanisms. First is the ratio of the concentration of reactive components to the concentration of nonreactive components. Second is the change in bond length of the initial and final state of the bonds that were changed by the chemical reactions during the curing phase. It is possible to both shrink or expand at as low as parts per million, or as high as several percent.

Coefficient of thermal expansion requires careful consideration of the overall composition of the epoxy adhesive composite. The CTE of a material with a T<sub>g</sub> is different above and below T<sub>g</sub>. Values for CTE under T<sub>g</sub> are referred to CTE alpha 1, and CTE values above T<sub>g</sub> are referred to as CTE alpha 2. The CTE alpha 1 is always lower than CTE alpha 2 as more mobile polymer chains increase their effective volume more rapidly than constrained polymer chains. Although a wide range of CTE values is possible, this property is more constraining on other performance criteria when pushed to extreme high and extreme low values. Bond strength and flow properties will suffer when high demands for customized CTEs are requirements. Running thermomechanical analysis of the epoxy is the typical method for measuring and monitoring CTE values.

Working with skilled and experienced epoxy formulators, as well as studying mechanical requirements will allow designers to create robust and reliable constructions bonded with epoxy adhesives. Specifying glass transition temperature, bond line thickness, modulus, and CTE for an epoxy will prevent warpage, delamination, and microcracking in MEMS, optoelectronic devices, and devices built with 3D interconnects.

### Biographies

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<b>Brewer Science</b> <a href="http://www.brewerscience.com">www.brewerscience.com</a> .....	27
<b>C&amp;D Semiconductor</b> <a href="http://www.cdsemi.com">www.cdsemi.com</a> .....	15
<b>DL Technology</b> <a href="http://www.dltechnology.com">www.dltechnology.com</a> .....	35
<b>E-tec Interconnect</b> <a href="http://www.e-tec.com">www.e-tec.com</a> .....	3
<b>ECTC</b> <a href="http://www.ectc.net">www.ectc.net</a> .....	48
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<b>Sensata Technologies</b> <a href="http://www.qinex.com">www.qinex.com</a> .....	4
<b>Smiths Interconnect</b> <a href="http://www.smithsinterconnect/volta">www.smithsinterconnect/volta</a> .....	29
<b>Sonix</b> <a href="http://www.sonix.com">www.sonix.com</a> .....	6
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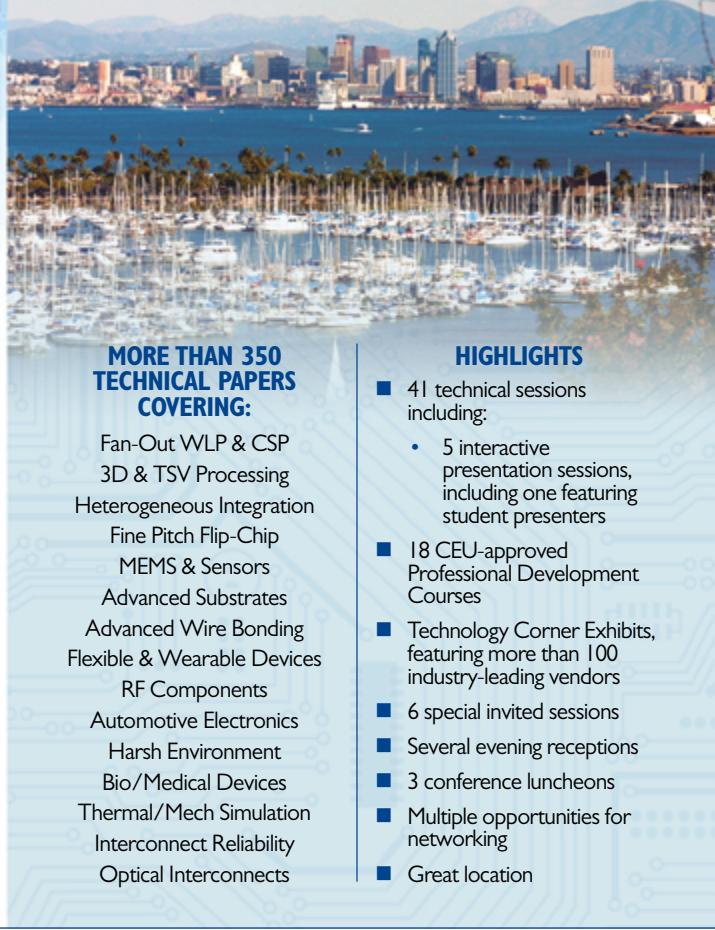
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<b>E-tec Interconnect</b> <a href="http://www.e-tec.com">www.e-tec.com</a> .....	3
<b>ECTC</b> <a href="http://www.ectc.net">www.ectc.net</a> .....	48
<b>EDA Industries</b> <a href="http://www.eda-industries.net">www.eda-industries.net</a> .....	20
<b>EV Group</b> <a href="http://www.evgroup.com">www.evgroup.com</a> .....	2
<b>Indium Corporation</b> <a href="http://www.indium.com/SiP/CSR">www.indium.com/SiP/CSR</a> .....	17
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<b>IWLPC</b> <a href="http://www.iwlpc.com">www.iwlpc.com</a> .....	44
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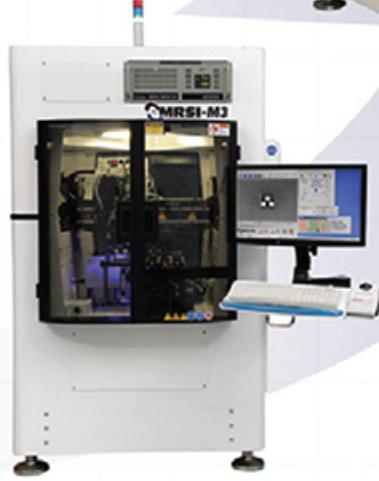
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