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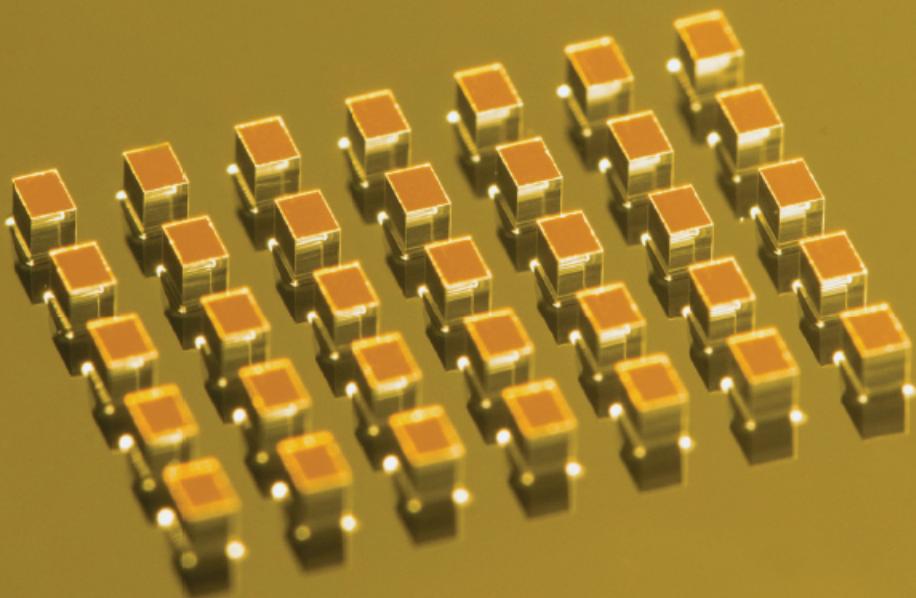
*The Future of Semiconductor Packaging*

Volume 22, Number 6

November • December 2018

**Collective D2W bonding for heterogeneous integration**

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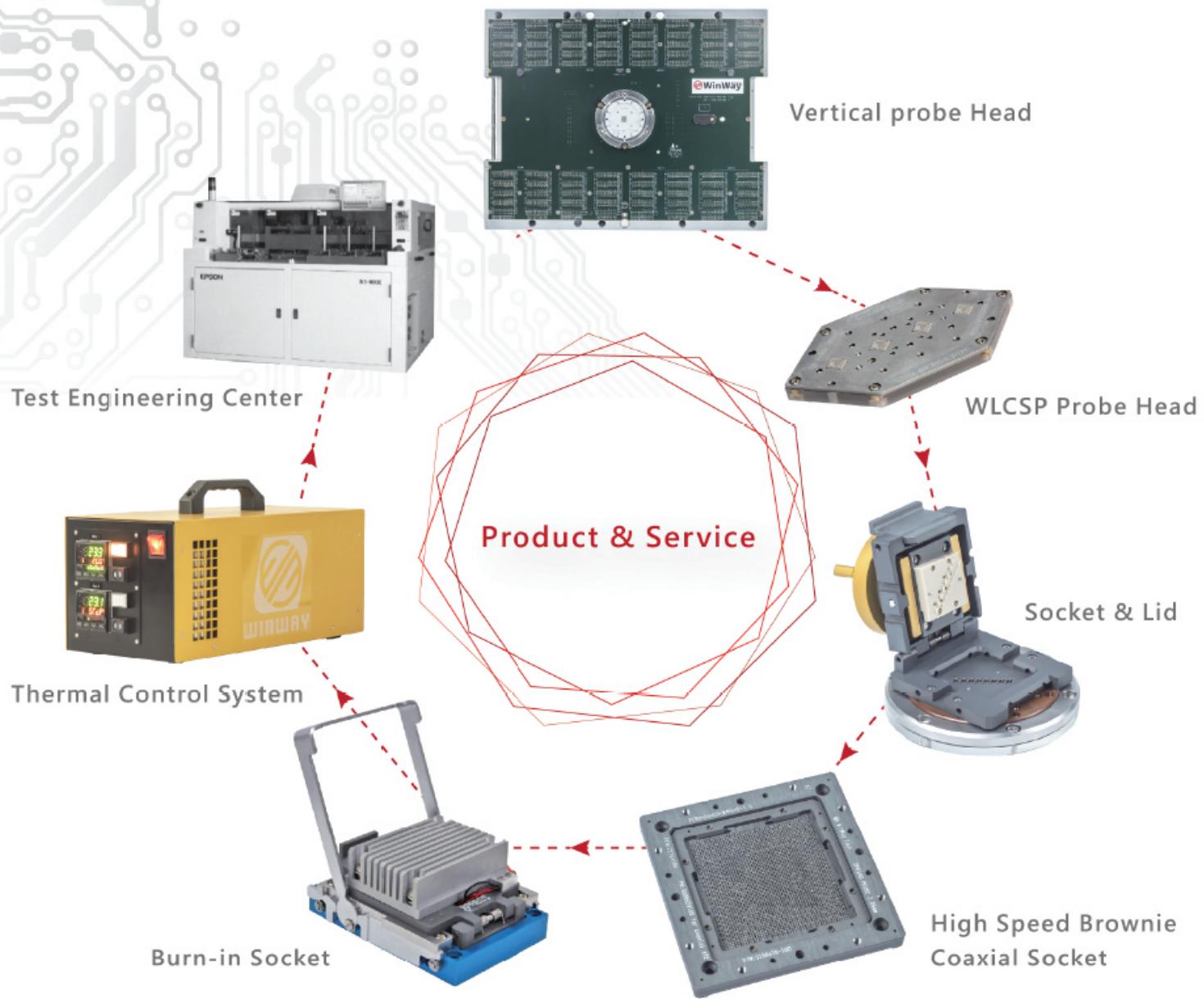
- Integration madness
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Collective die-to-wafer bonding enables heterogeneous integration of dies from different sources through the use of fusion/hybrid, adhesive or thermocompression bonding by a die carrier. The photo shows a group of compound semiconductor dies after successful transfer to a 300mm silicon wafer for further processing.

Cover image courtesy of EV Group

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## STAFF

**Kim Newman** Publisher

[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)

**Lawrence Michaels** Managing Director/Editor

[lmichaels@chipscalereview.com](mailto:lmichaels@chipscalereview.com)

**Debra Vogler** Senior Technical Editor

[dvogler@chipscalereview.com](mailto:dvogler@chipscalereview.com)

## CONTRIBUTING EDITORS

**Dr. John L. Lau** - Advanced Packaging

[john.lau@asmpt.com](mailto:john.lau@asmpt.com)

**Steffen Kröhner** - Advanced Packaging

[steffen.kroehnert@amkor.com](mailto:steffen.kroehnert@amkor.com)

**Dr. Ephraim Suhir** - Reliability

[suhire@aol.com](mailto:suhire@aol.com)

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**Lawrence Michaels**

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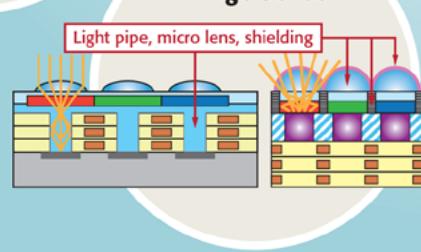
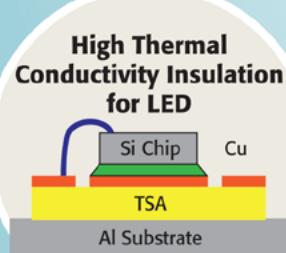
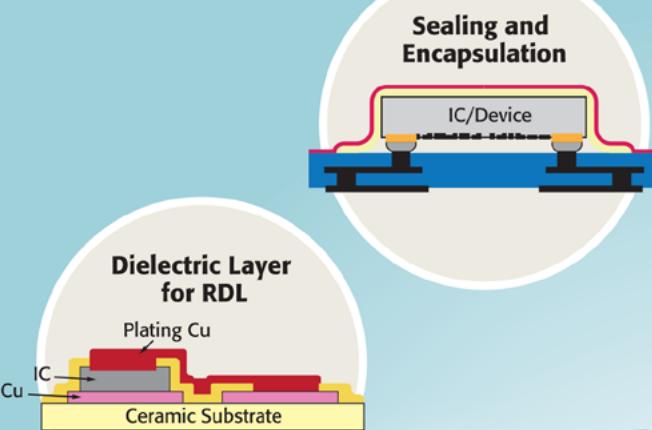
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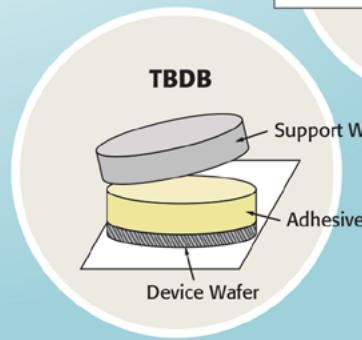
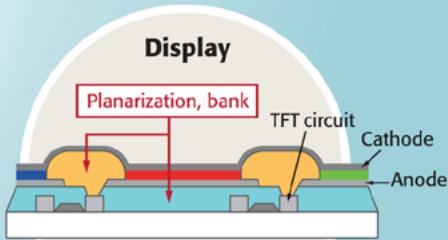
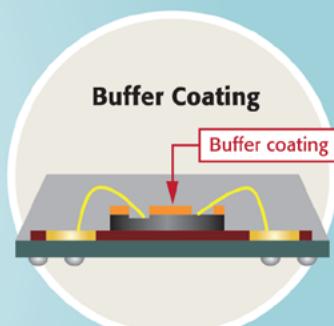
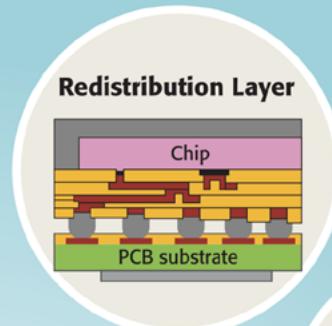
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# MARKET UPDATE



## New opportunities in bonding and lithography equipment markets

By Amandine Pizzagalli *[Yole Développement]*

Numerous megatrend market drivers, such as 5G (wireless infrastructure and mobile), mobile (including additional functionalities), voice processing, smart automotive, augmented reality/virtual reality (AR/VR) and artificial intelligence (AI), are today the heart of “More than Moore” (MtM) wafer volume evolution. These drivers will contribute to growth in MtM devices, with an expected compound annual growth rate (CAGR) of 10%, 2017-2023. Power devices accounted for more than 60% of overall MtM wafer starts in 2017, and with the growing demand for electric vehicles/hybrid electric vehicles (EVs/HEVs), they will continue dominating the MtM industry over the next five years.

Meanwhile, new antennas required for 5G will result in a rise of demand for radio frequency (RF) components like RF filters, power amplifiers (PAs), and low-noise amplifiers (LNAs) to ensure access to the radio networks of tomorrow.

Smart automobiles are also expected to support consistent growth of CMOS image sensors (CIS) and sensor wafer production over the next five years, fueled by the expanding integration of high-value sensing modules like radar, imaging, and light detection and ranging (LiDAR).

Technically speaking, megatrend applications drive the development of MtM devices to a new level of complexity along with further miniaturization and better performance, as well as extra functionality.

### MtM: opportunities in both bonding and lithography equipment markets

Fabrication of the next-generation of MtM devices requires new specifications leading to more miniaturization, additional functionalities, alignment upgrades, and smaller feature sizes. These stringent requirements for MtM devices need equipment with new features and technical specifications with respect to permanent bonding and lithography, as well as

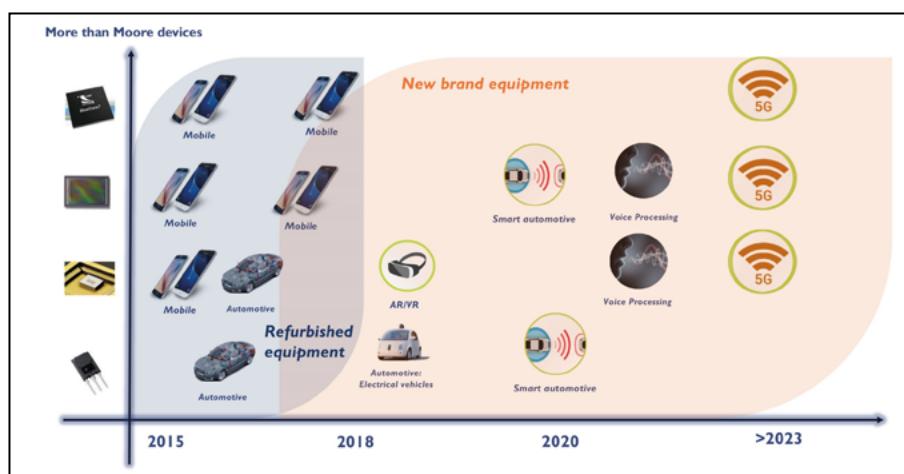


Figure 1: Lithography and bonding equipment type investment vs. mega trends. SOURCE: [2]

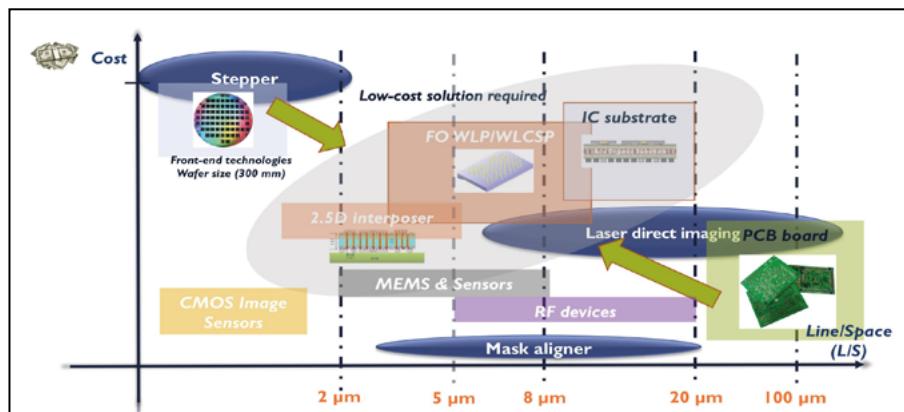


Figure 2: More than Moore features size: technical gaps between the wafer and PCB infrastructures. SOURCE: [2]

temporary bonding and debonding, thereby resulting in new investments (**Figure 1**).

Technical needs required for MtM devices are very different compared to the “More Moore” or mainstream semiconductor industry with respect to resolution, overlay, depth of focus (DOF), wafer bow and backside alignment (**Figure 2**). Specific to MtM devices, however, customer specifications are much stricter in the advanced packaging area with respect to resolution, overlay, sidewall angle, DOF, wafer handling for wafer bow and backside alignment

compared to microelectromechanical systems (MEMS) and CIS, RF and power devices. For instance, the current minimum resolution required is below 2 μm for some advanced packaging platforms, such as fan-out wafer-level-packaging (FOWLP) and wafer-level chip-scale packaging (WLCSP). A lot of effort is being made to reduce overlay issues caused by shifting dies and obtain vertical sidewalls for flip-chip and WLCSP.

Although established MEMS and sensors power layers have more relaxed specifications where the mask aligner

is mostly adopted to provide sufficient performance at lower cost, the road to megatrend applications driving devices to meet more stringent requirements such as sub-1 $\mu$ m, or devices requiring very accurate layer-to-layer alignment below 1 $\mu$ m, will pave the way toward higher adoption of stepper tools over the next few years.

In the case of light-emitting diode (LED) devices, lithography layers are typically in a range of 3 $\mu$ m-4 $\mu$ m and above except for the patterned sapphire substrate (PSS). This layer is the most critical of LED lithography layers as it needs finer features and higher resolution in a range of 1 $\mu$ m and therefore, it will require stepper tools.

On the other hand, W2W bonding is fueled by MtM devices, as it has already been adopted in MEMS devices, LED, silicon-on-insulator (SOI) manufacturing, and massively for CIS applications [1]. However, W2W bonding is still limited for use in 3D stacked memories.

Mostly, supported today by CIS based on fusion bonding (3D-stacked back side illumination [BSI]), W2W process growth will be led mainly by the potential wider adoption of hybrid bonding for the new generation of CIS imaging products, requiring a post-bond alignment mismatch below 0.2 $\mu$ m (**Figure 3**). Nevertheless, increasing performance demand has driven the development of innovative and alternative W2W techniques such as hybrid bonding, which does not need the use of through-silicon via (TSV) interconnects. This W2W method has already entered the BSI CIS market in the CMOS image sensor for the Samsung Galaxy 7 and will remain very attractive to enable full phase difference auto focus (PDAF) pixels. Besides, hybrid bonding is a promising solution for image sensors used in advanced driver-assistance systems (ADAS) and new, accelerated CIS approaches such as global shutter and time-of-flight (ToF) technologies. Meanwhile, Yole Développement had expected W2W production to pick up earlier for 3D dynamic random access memory (DRAM) stacked memories. However, in reality, cost and technical aspects today firmly limit adoption of W2W to replace die-to-wafer (D2W) assembly methods.

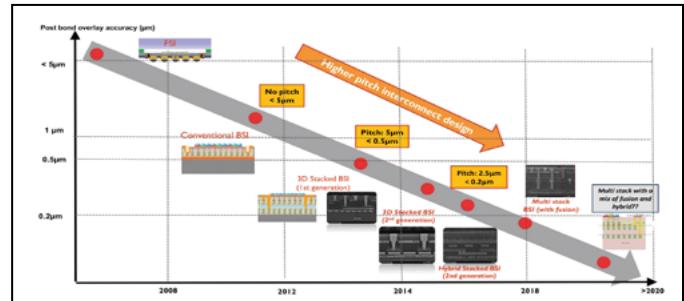
Looking ahead, although the W2W

process is fueled by MtM devices, emerging mainstream products such as 3D NAND memory and 3D system-on-chip (SoC) devices are expected to reshuffle the W2W business in the next few years. They could replace D2W and wire bonding in order to maximize the number of memory cells and yield, and also to solve stacking layer limitations.

In a nutshell, MtM devices could disrupt bonding and lithography technology adoption in the mainstream arena. From a market point of view, compared to the overall semiconductor equipment market, which is worth several billions of dollars, the permanent bonding, temporary bonding and debonding, as well as lithography equipment for the MtM industry, is a small niche representing millions of dollars. However, with the megatrends (5G, smart automotive, advanced mobiles, artificial intelligence, etc.) having triggered the market, the high growth in adoption of MtM devices has resulted in a strong investment in new lithography, permanent bonding and temporary bonding and debonding equipment to fulfill the new technical specifications required. Consequently, the total equipment market for permanent bonding, temporary bonding and debonding, and lithography process steps for the MtM industry generated revenue of more than US\$500 million in 2017 and is expected to reach more than US\$900 million by 2023, with a 10% CAGR over this period [2].

Supported by the increasing demand for advanced features, the growth of a new lithography equipment market for MtM devices at almost 10% CAGR is mostly due to the advanced packaging applications, which account today for almost 60% of the overall MtM lithography tools market and will continue dominating the MtM lithography industry.

With respect to MEMS and sensors, CIS and power devices, a high percentage of the lithography equipment revenue generated for these applications comes from reused/retrofitted equipment from the mainstream front end semiconductor industry. However, megatrend applications



**Figure 3:** Wafer-to-wafer bonding technical roadmap: CIS technologies. SOURCE: [2]

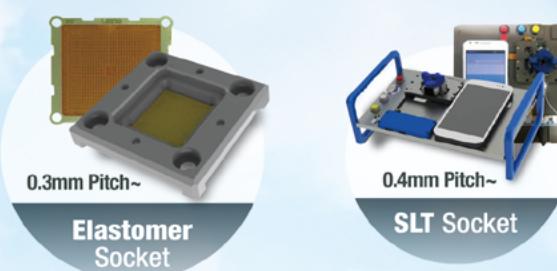
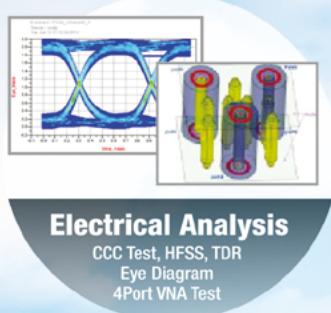
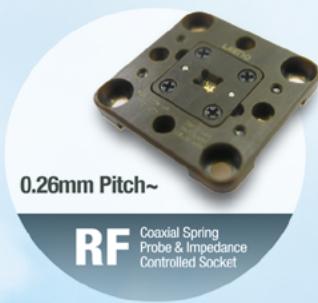
will push investments in new lithography equipment to meet the upgraded alignment and feature sizes required for the next generation of devices where older tools will no longer be efficient.

From the permanent bonding point of view, although the W2W permanent bonding market is mostly driven by CIS imaging, it is expected to be fueled by the emerging CIS products. Meanwhile, new mainstream semiconductor applications such as 3D NAND and 3D SoC will also strongly push the growth of the W2W bonding market over the next five years.

Although the temporary bonding and debonding segment still represents a rather small niche of the overall semiconductor equipment market, it has already been applied in a variety of "More than Moore" devices such as 3D TSV platforms, FOWLP, MEMS and sensors, power devices, and photonics, with high potential in numerous areas. Indeed, the temporary bonding and debonding market generated revenue of more than US\$55 million in 2017, mostly driven by 3D TSV, including 3D stacked memories and 2.5D interposers, as well as FOWLP. It will continue to grow over the coming years driven by the memory manufacturers to support the ramp-up of their latest high-performance stacked memory devices, HBM2, expected in 2019 [2].

Technically speaking, choosing the most suitable technology will depend not only on cost and process performance, but also requirements and capabilities of internal fabs. From a technology point of view, laser technology represents the dominant debonding method, widely used today for FOWLP and 2.5D interposer. It is expected to remain the leading process, mainly fueled by the major memory manufacturers such as Samsung, SK Hynix and Micron. The leading memory manufacturers are expecting to move from mechanical

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debonding or slide-off debonding, to laser debonding for the next generation of HBM2 on account of yield issues and to support the future high-volume production forecast by the end of 2019.

## Next-gen MtM devices broaden bonding, lithography landscape

When looking at the competitive landscape, the MtM equipment market is quite broad and diversified with different groups of vendors coming at solutions from different angles. A variety of equipment suppliers are involved in permanent bonding, as well as temporary bonding and debonding markets considered as niche applications compared to the overall semiconductor equipment market. However, both bonding markets are highly concentrated under the control of specialist equipment vendors such as EV Group and SUSS MicroTec (**Figure 4**).

Both companies have developed expertise in very specific equipment lines where legacy equipment suppliers do not have the capabilities to support such processes. Generally speaking, front-end suppliers are not really involved in those markets. Indeed, it does not justify the technology efforts needed to gain market share in a small field. However, Yole Développement sees some exceptions like Tokyo Electron (TEL), which is very active in the permanent bonding equipment market having initially developed these emerging technologies for its Asian customers.

Comparatively, the lithography equipment landscape for MtM devices is fragmented in a different way because it is served by two main groups of companies: 1) Specialist equipment vendors like EV Group, SUSS Microtec, SMEE, and Veeco offering brand new lithography tools, especially for the MtM industry; and 2) Top-tier semiconductor equipment suppliers including ASML, Canon, and Nikon coming from the front-end area, which mostly support the refurbished equipment.

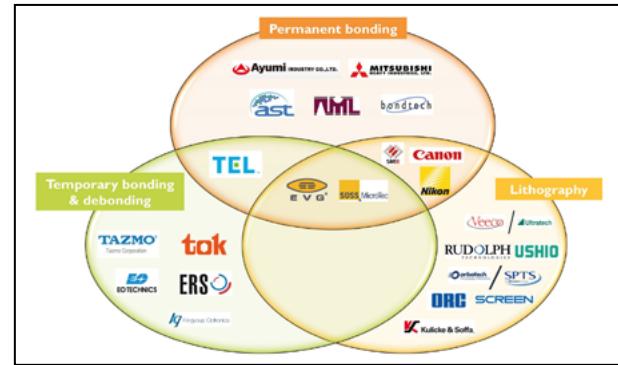
The equipment landscape, however, is currently evolving toward greater product portfolio diversification in both bonding and lithography business. For instance, the Asian equipment vendors have recently created a climate of strong price pressure, especially in China. New Chinese local players have entered the market and started competing with the top players. Among them, SMEE has been identified today as the dominant Chinese bonding and lithography systems manufacturer. SMEE

benefits from healthy subsidies from local governments. Indeed, thanks to this impressive support, the company has focused on the Chinese market (with its strong customer support). SMEE today, with its LED lithography solution, holds more than 70% market share (in volume) within this domestic market segment. This leading Chinese company provides low-cost bonding and lithography equipment for MtM applications.

Within the context of the above discussion, some other Asian equipment suppliers such as EO Technics, a Korean company, and Kinyoup Optronics, a Taiwanese company, are offering laser debonding processes mostly dedicated to FOWLP and could thereby shuffle the temporary bonding and debonding equipment market.

Meanwhile, in the quest to acquire market share in the MtM industry, large semiconductor front-end or back-end equipment suppliers have adopted a different strategy, expanding their lithography activities to reduce the gap between performance and cost in the “More than Moore” market through acquisitions of other companies, such as:

- The acquisition of Liteq, a spin-off of ASML, by Kulicke & Soffa allows the company to diversify and complete its lithography product portfolio in the advanced packaging area.
- The acquisition of Ultratech, a leader in lithography for advanced packaging, by Veeco, enhances its product technology portfolio while actively addressing advanced packaging applications. As a consequence, Veeco, originally involved in the front-end area, became the key leading supplier of new projection systems for Advanced Packaging applications.
- KLA Tencor, the leading front-end equipment vendor for inspection and metrology tools, acquiring Orbotech/SPTS gives it more of a presence in the back-end lithography area and advanced packaging equipment market. Finally, Canon, coming from the front-end



**Figure 4:** Technical gaps between the wafer and PCB infrastructures.  
SOURCE: [2]

area and a key lithography equipment vendor that also leads in refurbished equipment for power and CIS devices, has selected another strategy to capture further market share in the MtM lithography and bonding market. The company has developed a strategy aimed at improving its product portfolio through brand new dedicated MtM tools at a more reasonable cost compared to front-end lithography tools. In addition, the company attempted to skip a step in the bonding business by leveraging its physical vapor deposition (PVD) capabilities to recently launch a permanent bonding tool based on metal interface.

The varied strategies of the equipment suppliers discussed above are likely to create a strong challenging environment over a broad, stimulating landscape.

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## Biography

Amandine Pizzagalli graduated from CPE Lyon (France), with technical expertise in Semiconductor & Nano-Electronics, and holds an Electronics Engineering degree followed by a Master’s in Semiconductor Manufacturing Technology from KTH Royal Institute of Technology (Sweden). She is a Technology & Market Analyst, Equipment & Materials - Semiconductor Manufacturing, at Yole Développement (Yole); email pizzagalli@yole.fr

# Heterogeneous integration by collective die-to-wafer bonding

By Thomas Uhrmann, Jürgen Burggraf, Mariana Pires, Martin Eibelhuber [EV Group]

**I**ncreasing integration of technology, sensing and real-time data analysis using artificial intelligence are at the same time changing chip design and integration. Where a continuous evolution in feature scaling has historically been the right approach to chip designs for information and data storage centric environments, the current emphasis on connectivity, big data analysis, artificial intelligence, augmented reality and autonomous vehicles favors different chip designs, materials and technologies that are not fully compatible [1]. In addition, the multitude of new applications enabled by these industry drivers, along with the need for faster development cycle times and high-volume scaling, are introducing further challenges to overcome. In recent years, the semiconductor industry has been experiencing a new revolution of heterogeneous integration, whereby interconnection and advanced packaging technologies are supplanting lithographic scaling as the main contributors to improved device performance [2].

Heterogeneous integration describes the coalescence of multiple developments of the past decade. For example, 3D integration technologies have emerged and are widely available in high-volume manufacturing environments. In addition, several advanced packaging technologies, such as fan-out wafer-level packaging (FOWLP) and interposers, are also moving to high-volume production. Depending on the device architecture and level of integration, several integration methods at different manufacturing levels will play a major role in heterogeneous integration. In particular, increasing requirements for minimum latency and low-power consumption will drive the industry to new chip design concepts where integration of multiple functions such as sensing, photonics, RF communication, and even power devices on a single chip will be crucial. In other words, the chip design and functional integration will be key.

Silicon processing will certainly play a key role in enabling heterogeneous integration. However, silicon by itself does not provide all of the necessary functionality of heterogeneous integration. Therefore, material transfer and functional die transfer technologies involving different materials will be increasingly important to simultaneously enable silicon processing and close integration of the compute, sensing and connectivity portions of a fully functional system on chip (SoC).

Wafer bonding—especially fusion and hybrid wafer bonding—is readily available in mass production at major foundries and integrated device manufacturers, and is beginning to be adopted among system integration-oriented packaging houses. While the current driving forces for wafer-to-wafer (W2W) fusion bonding are 3D integration processes for stacked memory and image sensors, W2W bonding requires matching die sizes.

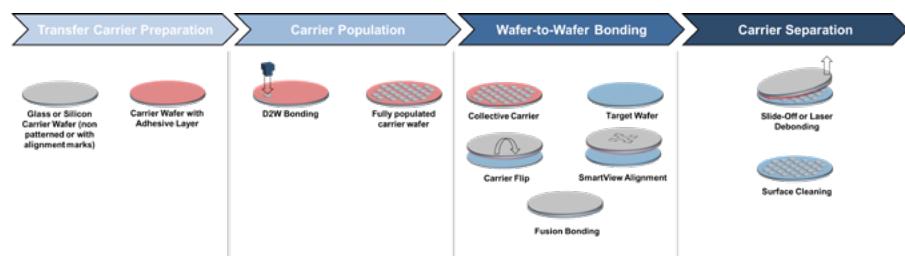
In order to efficiently build heterogeneous systems, several dies with different sizes have to be joined, which means integration on the chip level. This in turn means that different silicon nodes, compound semiconductors for photonic and power devices or RF filters coming from different fabs on different wafer sizes all need to find their way onto the same silicon base substrate. While fusion and hybrid bonding are compatible with front-end manufacturing, sequential die-to-wafer (D2W) approaches are not. In many cases, D2W processing involves several

hours of placement time, which exposes the process to particle generation. This makes it difficult to integrate with particle sensitive processes such as fusion bonding. While particle requirements as stringent as ISO 1 can in principle be mastered inside the equipment, the D2W population time and the act of moving the bond heads over the wafer will influence yields considerably. Therefore, D2W equipment will be detrimental for heterogeneous integration. How, therefore, does one surmount this dilemma?

## Collective die-to-wafer bonding

The only logical solution is a collective bonding approach. In this way, process separation of die placement and fusion bonding enables high bonding yields while keeping D2W equipment complexity at a manageable level. The process flow of collective D2W bonding is depicted in **Figure 1**. The initial step is the preparation and surface conservation of the source wafer prior to dicing. Because dicing processes are prone to heavy particle generation on the wafer surface and can even generate surface defects on the nanometer scale, the fusion bond interface needs to be conserved by a protective film. In addition to being smooth and having homogeneous thickness, the protective film has to be cleanable and not leave behind any organic residues.

In a subsequent step, each die is placed on a carrier substrate using D2W equipment. Depending on the



**Figure 1:** Schematic process flow for the collective die-to-wafer bonding process.

application and integration process, required alignment accuracies can vary between sub-micrometers to several micrometers. After these preparation steps, the collective carrier wafer and the receiving wafer are both loaded into a fully-automated EVG GEMINI production bonder. In this way, all further handling and preparation steps are under a particle-controlled atmosphere. After cleaning the dies to remove the protective film, both wafers undergo the same activation and cleaning procedures, before wafer-to-wafer alignment and bonding. Next, the wafers are subjected to slight heat and pressure to ensure leveling of the dies and high transfer yield of all dies. **Figure 2** gives an overview of the input parameters for a collective D2W bonding process.

After the steps outlined above, the wafers undergo a debonding process, where the carrier wafer is debonded from the bond stack, and both wafers are cleaned and unloaded from the bond cluster for further processing steps. Process development and evaluation of different material combinations have proven to work for multiple die areas and shapes between 800 $\mu\text{m}$  x 800 $\mu\text{m}$  up to 10mm x 10mm. Larger die sizes in this range are usually silicon, while the smaller die sizes are typically compound semiconductors such as InP, GaAs, GaN or SiC.

### Transfer carrier preparation

A central aspect of the overall D2W bonding process is the engineering of the collective die carrier. Apart from holding the dies safely during cleaning and preparation for the subsequent bonding step, several other functions have to be considered for the overall process. Initially, the intended debonding process should be selected, which determines the carrier wafer material. Another consideration is the adhesive material type and thickness for the die attach. Here, die size as well as thickness variation after grinding, greatly influence the layer stack and thicknesses of the adhesives. Last but not least, the adhesive multilayer should be optimized for subsequent alignment accuracy requirements. Mainly due to the embedding needs of the adhesive due to die height variations, die movement during collective bonding may occur and needs to be controlled via material design.

<b>Die Properties</b>	<b>Target Wafer</b>	<b>Pick and Place</b>
<ul style="list-style-type: none"> <li>- CMP / surface roughness</li> <li>- Die size</li> <li>- Edge properties</li> <li>- Die thickness uniformity</li> </ul>	<ul style="list-style-type: none"> <li>- CMP / surface roughness</li> <li>- Protrusion / Dishing of Cu in case of hybrid bonding</li> <li>- Pad dimensions</li> </ul>	<ul style="list-style-type: none"> <li>- Placement accuracy (x, y)</li> <li>- Die rotation</li> <li>- Die tacking temperature</li> </ul>
<b>Bond Process</b>	<b>Transfer Plate</b>	<b>Debond and Cleaning</b>
<ul style="list-style-type: none"> <li>- Die and target wafer surface activation</li> <li>- Alignment</li> <li>- Cleaning</li> <li>- Bond force, temperature and time</li> </ul>	<ul style="list-style-type: none"> <li>- Transfer plate materials</li> <li>- Adhesive thickness and uniformity</li> </ul>	<ul style="list-style-type: none"> <li>- Debond technology</li> <li>- Cleaning solvent</li> <li>- Cleaning time</li> <li>- Solvent compatibility</li> </ul>

**Figure 2:** Input parameters for the collective die-to-wafer bonding process.

### Carrier population

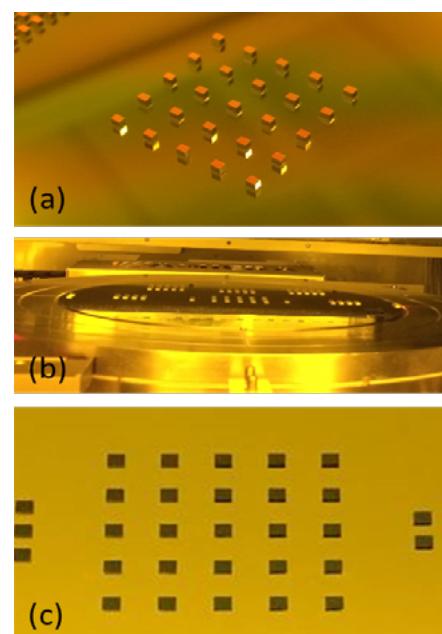
After carrier setup, carrier population is done using D2W bonding equipment. Depending on the alignment accuracy needs for transferred dies, the die placement is done using global or local alignment on the carrier. In the case of global alignment, the stage accuracy of the D2W bonder may suffice for subsequent placement needs. Mainly for engineered substrates with compound semiconductor material transfer, this low accuracy is good enough, as patterning is done on the receiving substrate by lithography in a later step. Local alignment, however, is becoming key for die stacking with fusion and hybrid bonding as is typically needed for 3D integration. In this case, 1 $\mu\text{m}$  (3 sigma) and tighter alignment is needed, which is only possible using a lithographic patterned carrier wafer, allowing a local fine alignment before tacking of the die.

### Wafer-to-wafer bonding

Subsequent to population, transfer bonding of the dies is done using standard W2W bonding equipment. Collective D2W bonding allows a wide bandwidth of bonding processes for transfer, including any adhesives such as underfills, low-temperature solder bonds typically used for solder bumps, as well as metal thermocompression bonding, such as gold-to-gold or copper-to-copper. For thermocompression bonding, a minimum metal roughness below 1nm is required for a high transfer yield.

The main focus for collective D2W is in fusion and hybrid bonding (**Figure 3**). In this case, both the receiving and donor wafers need to be cleaned and activated prior to joining. Plasma activation is essential to lower the bonding temperature to CMOS- and even memory-compatible levels. The low-temp plasma activation process modifies the wafer's surface and

generates a high level of hydroxyl groups. These chemically reactive species are, in combination with water, coming from a cleaning process after activation as an effective link for hydrogen bridge bonds. The higher the hydroxyl density, the higher the initial bond strength and the higher the die transfer yield from bonding. As hydrogen bridge bonds are still weak in comparison to covalently bonded dies, the wafers have to undergo an annealing directly after pre-bonding. Typically, the annealing process is split into two steps, where an intermediate temperature up to 250°C hardens the bond, but still conserves the properties of the adhesive films on the donor wafer. Only after debonding of the carrier wafer is the final annealing step accomplished, including the contacting in hybrid bonding [3-6].



**Figure 3:** Images of collective D2W bonding at different stages of the process: a) after carrier population with die face up; b) during alignment in the face-to-face bond alignment system; and c) after successful die transfer.

## Carrier separation

For the carrier separation process, a full range of debonding techniques is available, using either light, force or heat for debonding. In the case of collective D2W, the bonding level is not at a final stage, therefore, the debonding process should be gentle and exert a low vertical force to keep damage and potential die delamination risks low. With the above considerations in mind, mechanical debonding introduces a further process risk. Successful implementation of the process has been shown for thermal slide-off debonding as well as UV laser debonding using diode pumped solid-state lasers [7-8].

In the case of thermal slide-off debonding, thermoplastic adhesives serve as compliant adhesion layers of the dies on the carrier wafer. The wafer stack is heated above the softening point of the adhesive, and both substrates are horizontally slid against each other using active control of sliding speed and sliding force.

In the case of laser debonding, an additional laser release layer is added to the glass carrier wafer that enables the low-force detachment. A galvo scanner provides tight beam control, which allows the laser to selectively address specific wafer regions, enabling the selective debonding of only the die area, or even selected dies. In the case of both thermal slide-off and laser debonding, both the receiving and carrier wafers are cleaned to remove any organic residues before undergoing a batch annealing step to finalize the wafer bond.

## Alignment considerations

Typically, alignment accuracies enabled with collective bonding are propagated through die placement on the collective carrier, W2W alignment and potential shifts during thermal annealing. While alignment accuracies of less than 100nm (3 sigma) have been shown by face-to-face bond alignment in W2W bonding, the major limitation of the process is in the die population accuracy. Depending on the equipment and alignment strategy, 1µm is a typical D2W alignment value achieved by currently available equipment on the market. Therefore, die placement accuracy marks the dominant value in the overall error propagation for collective D2W bonding. However, the impact of this limitation depends on each application.

For packaging applications where contact pitches are typically in the 5µm to 10µm range, such as memory devices, interposers or application processors, the compound alignment values are well within the performance range of the process. For other applications where tight alignment (well below 1µm) is needed, such as image sensors or die segmented devices, either W2W fusion or hybrid bonding should be used, or the die transfer process integration must be moved further upstream in the manufacturing process chain. Therefore, the interconnect is done after die transfer bonding. Furthermore, sub-µm alignment of the interconnect via can be done using lithographic patterning, which enhances the alignment accuracy of commercially available die bonders. In addition, for other devices, such as those used in telecom or photonic applications, patterning is done after compound semiconductor transfer bonding in order to enable the best overlay matching to underlying photonic components in silicon.

## Summary

The semiconductor industry's continued migration to heterogeneous integration in order to increase device performance and capability adds new levels of manufacturing and integration complexity, which drive the need for material transfer and functional die transfer technologies. Collective D2W bonding is an ideal approach that enables high bonding yields while keeping wafer bonding equipment complexity at a manageable level. High transfer bonding yields and electrical die yield is enabled by process separation and effective protection of the die surface during die placement. Surface activation by plasma treatment, die transfer bonding, as well as debonding and cleaning of the dies, are all implemented in a bond cluster tool to maintain a particle-controlled atmosphere. Collective D2W bonding can be implemented with various die sizes, materials (such as silicon or compound semiconductors), as well as different bonding processes, making the process universally suited for heterogeneous integration.

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## Biographies

Thomas Uhrmann holds an Engineering degree in Mechatronics from the U. of Applied Sciences in Regensburg, and a PhD in Semiconductor Physics from Vienna U. of Technology. He is Director of Business Development at EV Group; email T.Uhrmann@EVGroup.com

Jürgen Burggraf received his Engineering Diploma in Industrial Engineering from the U. of Applied Sciences in Mittweida, Germany and is Process Technology Manager – Wafer Bonding at EV Group.

Mariana Pires received her Master's degree in Physical Engineering from the Aveiro U. in Portugal and is a Process Technology Engineer – Temporary Wafer Bonding at EV Group.

Martin Eibelhuber received his PhD in Physics and Nanoscience from Johannes Kepler U. (JKU) Linz and is Deputy Head of Business Development at EV Group.

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# High-temperature survivability and the processes it enables

By Michelle Fowler, Christopher Apanius, Kimberly Yess [Brewer Science, Inc.]

**W**ith all the improvements in the advanced packaging landscape, what more could the industry ask for? After addressing performance expectations: total thickness variation (TTV), stress/warpage control, high throughput and low cost of ownership, what could possibly be left? Extreme temperature survivability, perhaps? Industry applications today are requiring devices to be thinned down well below 30 $\mu\text{m}$ , which ultimately will require a carrier system for handling fragile, high-value substrates through the subsequent downstream processes including high-temperature anneal and deposition. The challenges that occur at the packaging level are well understood. We have developed technologies to overcome these challenges at the wafer level before the thinned device chips ever make it to packaging—further adding value and performance while reducing cost of ownership. The objective of this article is to explain and show examples of new high-temperature-compatible materials and in-process solutions during fabrication of the device. These new materials have demonstrated improved performance beyond any other solutions known today. Applications that benefit from using higher-value chips fabricated using this enabling new technology will be explored along with examples.

## Wafer-level challenges

Wafer-level packaging (WLP) technologies have been widely adopted for large-scale production and used for the manufacturing of consumer products such as smartphones, tablets and various other hand-held devices. Higher-performance packaging, lower cost, smaller form factor and a higher level of integration can be achieved using various packaging platforms. Wafer-level chip-scale packaging (WLCSP) is attractive due to its cost and performance ratio and substrate-less package, however, its use is limited by die size. As an alternative, fan-out wafer-level packaging

(FOWLP) technology is being widely developed and used in the packaging industry because I/O density can be increased by “fanning” out interconnects to external pad locations, achieving smaller form factor and decreasing power consumption. Semiconductor packaging technologies with heterogeneous integration, such as system-in-package (SiP) and package-on-package (PoP) infrastructures are facing significant challenges due to increased complex integration. The demands for improved system performance, functionality, lower power and smaller form factor are the drivers of today’s packaging technologies.

Substrate handling of the thinned device is a major challenge for the manufacturing flow for many of these technologies. Thinned silicon wafers <50 $\mu\text{m}$  or redistribution layers (RDLs) created using an RDL-first process are delicate and expensive to manufacture. Handling requires the use of support substrates processed using temporary bonding materials along with an applicable debonding (TBDB) technology to facilitate the construction of complex packaging infrastructures [1].

Temporary bonding materials created using high-viscosity, low-T<sub>g</sub> thermoplastic polymers are commonly used in TBDB processes. When used with a carrier substrate, they offer thermomechanical stability and improved ease of handling of the thin device substrate. At higher temperatures these materials behave more like a liquid and lose mechanical stability as the melt viscosity decreases allowing the material to soften, thereby weakening bondline stability. Deformation and delamination of the device wafer can occur, causing issues for downstream processes [2].

Both chip-first and chip-last process flows require the use of high-temperature and high-vacuum processes to create the RDLs. Today’s FOWLP processes require materials that can survive high temperatures and harsh chemical environments while maintaining mechanical support for the device substrate.

## Chip-first or chip-last?

For chip-first processes, singulated dies are placed onto a substrate processed with temporary bonding material or thermal release tape (TRT) prior to being overmolded with epoxy mold compound (EMC) in a thermocompression process. High-temperature dielectric processing induces stress and leads to warpage between the carrier wafer and EMC. Die-shift and die stand-off due to substrate warpage and bonding material softening during EMC processing creates RDL misalignment to the embedded die [3].

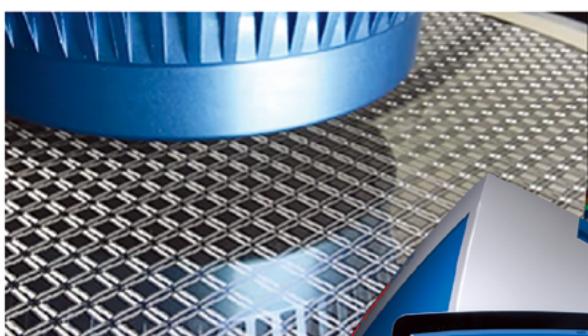
In a chip-last process flow, glass carrier wafers are coated with a removable laser release material upon which the RDL will be built. The laser release material needs to possess good thermal, mechanical and chemical stability to survive thinning and backside dielectric and deposition processes.

## Materials for FOWLP

BrewerBOND® T1100 thermoplastic bonding materials and BrewerBOND® C1300 curable bonding materials represent the next-generation bonding system to offer increased throughput with high thermal stability. These materials offer improved mechanical stability at elevated process temperatures, good chemical resistance, room temperature bonding and debonding for both wafer-level and panel-level processing. The low total thickness variation (TTV) coupled with the increased mechanical strength of this system allows for ultrathin backside wafer thinning, achieving post-grind wafer thicknesses of <50 $\mu\text{m}$ . **Figure 1** shows confocal scanning acoustic images (CSAM) of a bonded wafer pair after thinning to 50 $\mu\text{m}$  and subsequent heat treatment at 400°C for 30 minutes under vacuum. These images show a defect-free bondline without damage to the thin device.

# XM8000

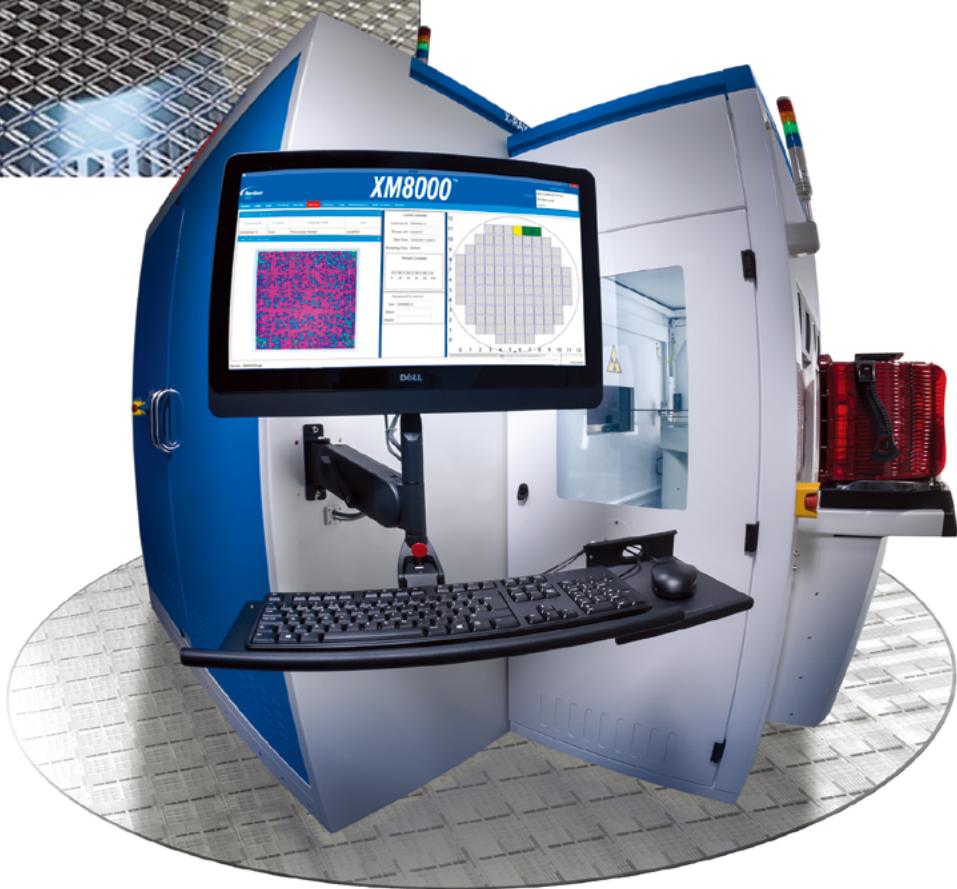
Intelligent X-ray Metrology



## Complexity Simplified

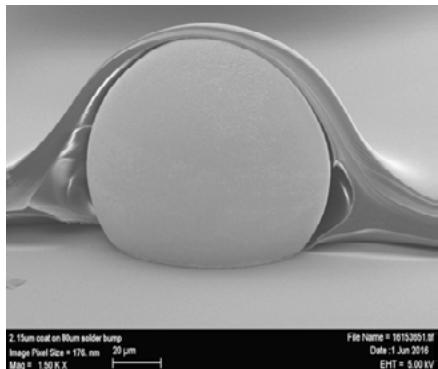
The semiconductor market demands increasingly complex devices that are enabled by technologies such as TSV, PoP, 2.5D and 3D integration.

These complex products demand a new level of metrology. The XM8000 system delivers fully automated, non destructive, radiation safe defect detection for all complex devices.



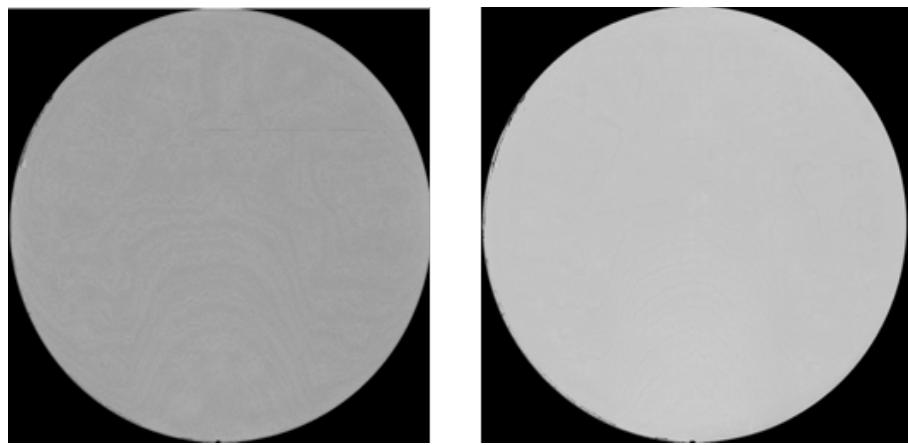
The system discussed above is comprised of a low- $T_g$  thermoset material, which is applied to a glass carrier wafer and then bonded to the device wafer that has been processed with the corresponding high- $T_g$  bonding material. After bonding at room temperature, the bonded pair can then be either UV exposed or hotplate baked to cure the thermoset material (**Figure 2**).

When processed below 350°C, the thermoplastic bonding material remains solvent-soluble and has little to no melt flow up to 300°C. When coated, this material is highly conformal and even as a thin coating can cover severe topography. Using a scanning electron microscope (SEM), **Figure 3** is a cross section of a 2.15μm film of thermoplastic bonding material processed over 80μm solder bumps.

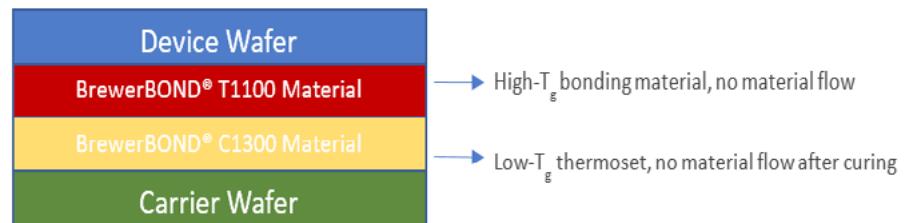


**Figure 3:** Conformal coating of BrewerBOND® T1100 material.

The curable bonding material has a high melt flow (low  $T_g$ ) and acts as a liquid prior to curing. This enables bonding to the thermoplastic bonding material at room



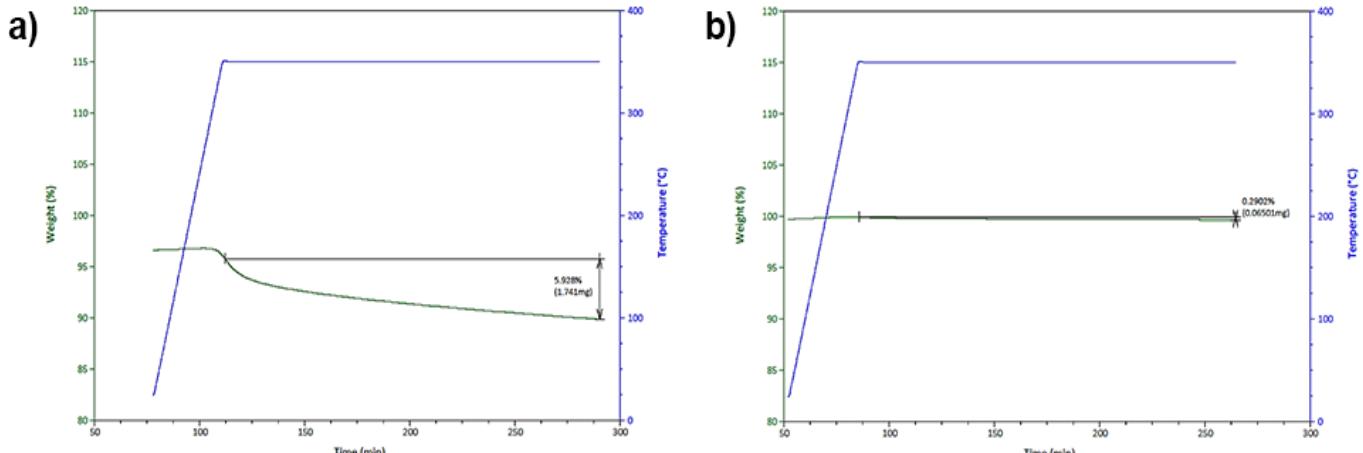
**Figure 1:** Confocal scanning acoustic images (CSAM) under: a) no heat treatment; and b) after 400°C, 30 minutes under vacuum.



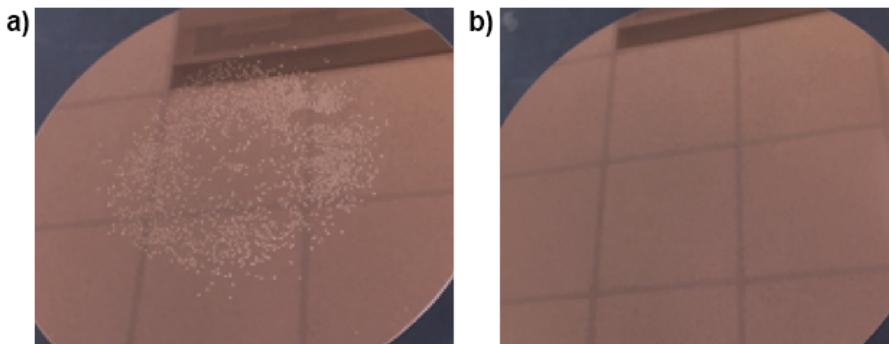
**Figure 2:** Typical process flow for the BrewerBOND® dual-layer system using the thermoplastic and curable bonding materials together.

Property	Curable Material	Bonding Materials		
		BrewerBOND® T1107	BrewerBOND® T1105	BrewerBOND® T1101
Solution viscosity	4262 at 100°F 4960 cP at 24.5°C	228 at 100°F 350 at 24.5°C	85 at 100°F 140 at 24.5°C	70 cps at 100 °F
Target thickness	20-60 μm	2 μm	2 μm	2 μm
Young's modulus	3.3 MPa	2900 MPa	2900 MPa	2550 MPa
CTE	390 μm/°C (above $T_g$ )	28 μm/°C (below $T_g$ )	28 μm/°C (below $T_g$ )	43 μm/°C (below $T_g$ )
$T_d$	420 °C	465 °C	465 °C	375 °C
$T_g$	< -50 °C	328 °C	328 °C	225 °C

**Table 1:** Material properties.



**Figure 4:** Isothermal TGA data for a) BrewerBOND® T1105 material, and b) BrewerBOND® C1301 material.



**Figure 5:** Copper deposition on bonding materials with a) poor adhesion showing defects, and b) good adhesion without defects.

Bonding Material film thickness	166 nm	275 nm	596 nm	729 nm	869 nm	1.0 $\mu$ m	1.5 $\mu$ m	2.0 $\mu$ m	2.8 $\mu$ m	4.6 $\mu$ m	5.4 $\mu$ m
Transmittance at 308 nm	47%	38%	11%	8%	4%	1%	0.3%	0	0	0	0
Transmittance at 355 nm	83%	77%	60%	56%	51%	38%	30%	19%	11%	2.3%	1.2%

**Table 2:** Transmittance data vs. film thickness for BrewerBOND® T1100 series materials.

temperature with low force. After bonding, this material requires a cure process, which sets the bondline. This property allows this system to possess high mechanical strength even at elevated temperatures (**Table 1**).

Dielectric processing, metal deposition and anneal are processes that require the use of high temperatures. This next-generation of materials described in this article maintain bondline integrity without decomposing, outgassing or reflowing. Isothermal thermogravimetric analysis (TGA) of these materials post-processing, heated at 350°C for 3 hours in a nitrogen atmosphere, show less than 6% weight loss (**Figure 4**). Material adhesion to organic and inorganic substrates and metal layers is also necessary in FOWLP technologies. The new bonding materials have demonstrated excellent adhesion to both copper laminate and epoxy mold compound (EMC) (**Figure 5**).

While bonded, the thermoplastic bonding material coupled with the curable bonding material has shown resistance to common downstream wet chemical processes. Once processing has been completed, the carrier substrate can be removed from the thinned device using either mechanical release or a laser ablation technology. Both processes are done at room temperature and are low-force technologies suitable for use with thin substrates. When using a laser ablation process, the thermoplastic bonding materials are thick enough to block the energy created during the laser ablation process for debonding at both 308nm and 355nm, which

prevents direct laser damage to the device wafers (**Table 2**).

After debonding has been completed, the thermoplastic bonding material can be removed from the device substrate using solvent or an oxygen plasma etch process. The curable bonding material can be removed from the carrier substrate using Dynasolv™ 220 material, a commercially available cleaner from Dynaloy.

## Developments for RDL-first creation

BrewerBUILD™ materials are single-layer, high-absorbing materials for RDL buildup and assembly and are designed for use in laser ablation processes. These materials have increased absorbance at wavelengths between 308nm and 355nm and offer increased protection to the device wafer during laser ablation. In addition to the increased performance during laser ablation, this new generation of materials also offers strong solvent resistance, high adhesion to many materials, and effective solvent cleaning after ablation [4].

## Summary

When used as a system, the new temporary bonding materials and processes that facilitate FOWLP technologies described above impart improved mechanical stability to thinned, bonded wafers that undergo processes using high vacuum and high temperatures. Chemical resistance, coupled with room-temperature bonding and debonding

technologies, provides added value and improved performance while reducing cost of ownership. For RDL-first, we recently introduced BrewerBUILD™ materials for build-up and assembly, offering a better alternative to thermal release tapes. These new materials facilitate low-energy laser debond processes thereby providing improved protection for the device wafer with low carbon residues.

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## Biographies

Michelle Fowler has 30+ years of industry experience in roles spanning quality assurance, applications engineering, and research and development. She is a Principal Applications Engineer for Wafer-Level Packaging Materials at Brewer Science; email [mfowler@brewerscience.com](mailto:mfowler@brewerscience.com)

Christopher Apanius has developed and commercialized many new materials for industrial, MEMS and consumer electronics applications with 20+ years in the industry and is Applications Manager for Wafer-Level Packaging Materials at Brewer Science.

Kimberly Yess received a BA in Chemistry & Biology at Central Missouri State U., and an MBA from Webster U., St. Louis Missouri. She is Technology Director for the WLP Business Unit at Brewer Science.

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<b>Palomar Technologies, Inc.</b> 2728 Loker Ave. West Carlsbad, CA 92010 USA Tel: +1-760-931-3600 Fax: +1-760-931-5191 <a href="http://www.palomartechologies.com">www.palomartechologies.com</a>	Wedge Bonders Eutectic Die Bonders	Ball Bonders, stud bumpers, manual Die Bonders
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<b>Semiconductor Equipment Corp.</b> 5154 Goldman Avenue Moorpark, CA 93021 USA Tel: +1-805-529-2293 Fax: +1-805.529.2193 <a href="http://www.semcorp.com">www.semcorp.com</a>	Flip Chip Bonder	Pick & Place Systems, Cleaning Systems for: FOUPS, SMIF Pods, Cassettes, FOSBS & EUV Pods
<b>SET Corporation SA</b> Smart Equipment Technology 131, Impasse Barteudet 74490 Saint Jeoire France Tel: +33 (0) 450 35 83 92 Fax: +33 (0) 450 35 88 01 <a href="http://www.set-sas.fr/en">www.set-sas.fr/en</a>	Die Bonders, Flip Chip Bonders	Large device bonders and non-imprint

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# INTERNATIONAL DIRECTORY OF BONDING EQUIPMENT FOR 2.5D AND 3D ASSEMBLY

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# Integration madness

By Wolfgang Sauter, Mark Kuemerle [Avera Semi, a wholly owned subsidiary of GLOBALFOUNDRIES]

**W**hile package integration has revolutionized the handheld application space, the infrastructure market has remained comparatively conventional. Yet change begins now! Sparked largely by the complex packaging required by high-bandwidth memory (HBM), new architectures have emerged utilizing appreciably advanced integrated solutions. In this article we will investigate the factors driving this new direction, and what types of chip-to-chip I/O will be required.

Package integration has recently driven stunning innovation in the handheld application space. The complex fan-out packages being used for today's cell phone processors are extremely small, and feature an integrated package height that is thinner than the substrate alone was a few years ago. In addition to the processor chip, memory components and sophisticated power supply networks are now being integrated in these increasingly complex packages.

Packaging innovations also drive changes in chip architectures: the design blocks on a chip that enable communication between different chips ("interface intellectual property [IP]") are evolving to allow the short connections in a low-power, and bandwidth-efficient way. Interface IP blocks must now be designed to match, and take advantage of specific package technology integration schemes.

So what does this mean? Is packaging to rule the next wave of innovation? This remains to be seen. At the highest level, we can separate the market into two application spaces:

1. The high-volume, space-constraint consumer market with fairly low reliability requirements. (Do you own a cell phone that is more than 3 years old?)
2. The low-volume, high-reliability infrastructure market (networking, etc.), requiring large package sizes, yet need to survive in the field for 10 or more years.

As consumer applications have evolved through greater package integration in

the last decade, networking and compute applications remained in much more conservative package solutions, primarily (if not exclusively) single-chip modules. There have certainly been package technology changes and innovations driven by HSS (SERDES) speed and performance requirements, but suffice it to say, the majority of these changes have been evolutionary: larger chips (up to reticle size), larger packages (up to 75mm), and newer materials with lower loss dielectrics.

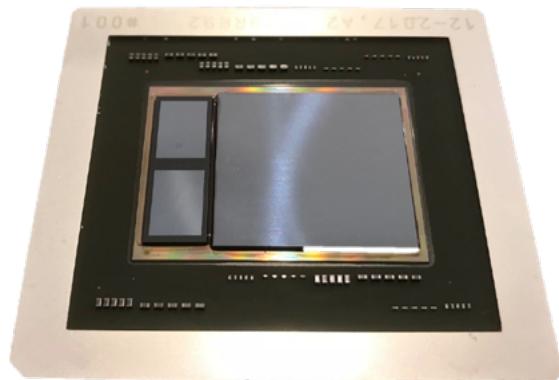
The slow, steady growth described above has been supported by ever-increasing SERDES data rates and novel serial memory solutions like the hybrid memory cube (HMC). Yet recently there has been a marked shift in package complexity for these applications driven largely by HBM integration, a massive shift in system complexity and risk beyond previous applications. It seems that HBM's requirements have broken through system-level constraints in a way that this market has never before seen. Larger-than reticle size interposer solutions with HBM integration as shown in **Figure 1** serve as examples of products entering the market this year.

While there are no objective measures that can be used to quantify the increase in complexity of these new applications, we can calculate a rough

complexity increase factor by multiplying some of the major parameters, such as package size, silicon size, thermal, and power challenge. **Table 1** shows the magnitude of these combined changes.

This shift toward more complex integration is further illustrated through industry participation in conferences: the growth of the leading packaging conference (ECTC) has more than doubled in the last decade. The five leading sessions this year focused on complex fan-out, or wafer-level packaging – with more than twice the attendance of the flip-chip or materials sessions that have historically dominated the conference.

A momentous change is happening with visibly significant shifts reaching the (traditionally conservative) networking market, as 2.5D and remarkably complex multi-chip module (MCM) configurations



**Figure 1:** Example of 2.5D integration on a stitched silicon interposer.

System constraint	Previous constraint	Reason for constraint	Current solutions	Increase in complexity
Package body size	65x65mm <sup>2</sup>	L2 attach risk	>/=75x75mm <sup>2</sup>	33%
Silicon size	None	L1 attach risk	Stitched interposer	88%
Thermal limit	125°C	Max component T <sub>j</sub>	105°C	19%
Max power	150W	Max system power	250W	66%
<b>Combined complexity factor</b>				<b>5X!</b>

**Table 1:** Increased package complexity of solutions within the last product generation.

Memory Integration	Past	Past/Current	Current	Future	Next Gen
Memory	DDR	HMC	HBM	More HBMs	3D
Comment	Too many pins & too much power	Limited supply	Must make HBM work	Need even more HBMs (4-6 HBMs)	Will need more bandwidth than HBM
Image					

**Figure 2:** Evolution of network processor architectures.

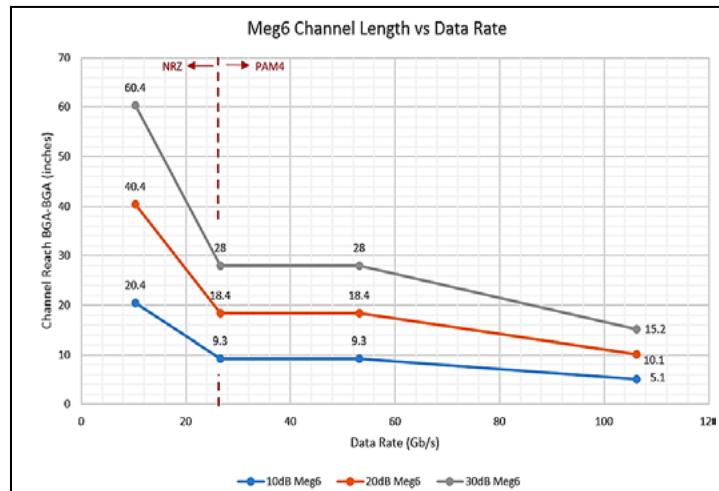
appear in most companies' product plans and roadmaps. To understand this, we must first take a look at what drives package integration for the infrastructure market described in the sections below:

**Memory bandwidth.** There is an insatiable desire for more and more memory access at lower and lower power. For a networking application-specific integrated circuit (ASIC) to double its ability to process traffic, it must double the bandwidth to external memory for packet buffering and table lookups. Unfortunately, commodity memory has been unable to keep up with ever increasing speed requirements. The only current option meeting this need is HBM, with a large number of simple, low power, and high density signals. To explain this in numbers: While a traditional DDR4 memory component integrated on the board supports ~100Gbps of memory access, the on-module integrated HBM2 memory component supports ~2Tbps (or as much as 20 DDR4 components) at roughly one order of magnitude lower power per transferred bit.

The downside of the HBM integration is the complex (and costly) packaging solution on a large silicon interposer. (Would anybody have predicted 5 years ago that we will be joining >1,000mm<sup>2</sup> pieces of silicon to organic substrates?)

HBM (or other solutions with high-bandwidth/low-power memory interfaces) is here to stay. We can't reverse direction with memory bandwidth. But the final solution is still unclear. 2.5D will reach its limits – probably at 6 memory components integrated in a 2.5D package, and at a data rate of ~3-5Gbps. The likely next step is 3D integration of the memory component with significantly increased interconnect density by the use of more through-silicon vias (TSVs) and a shorter interconnect length. Such 3D memories are expected to enable a 10x bandwidth increase at substantially lower power than the current 2.5D solution, but with additional package complexity if paired with 2.5D solutions. **Figure 2** shows the evolution of memory integration from past (DDR), to current (HMC, going to HBM), to future and next-generation (3D) integration schemes.

**SERDES roadmaps and physical limitations.** SERDES are high-speed interfaces enabling communication between modules on a board: short-reach SERDES for modules in close proximity on the same board, and long-reach SERDES from a module on one board to a module at the other end of the same board, or on a “neighboring” board. Traditionally, SERDES communication speed has doubled with every major technology node: 28Gbps at 32nm, 56Gbps at 14/16nm, and 112G at 7nm and beyond. The advantage of these fast and highly complex SERDES interfaces



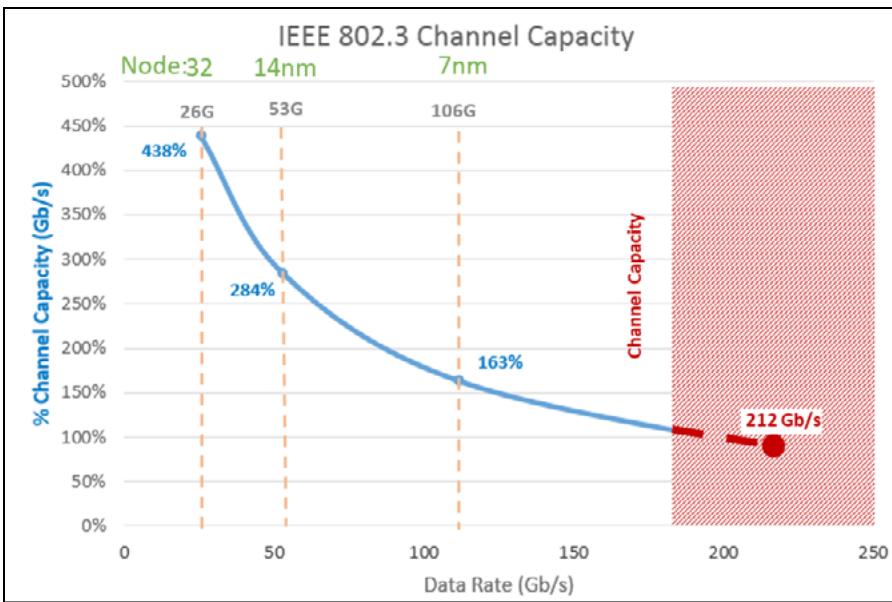
**Figure 3:** Reach of Meg6 (inches) vs. data rate

is the few signal pins (i.e., ball grid arrays [BGAs]) needed to transfer large amounts of data compared to the many (>1,000) slow (~2Gbps) parallel signals that may be used in 2.5D or other on-module configurations.

From a product perspective, networking processors require double the bandwidth from one generation to the next generation. This seems to be a perfect match for the SERDES roadmap, where signal speed also doubles from one node to the next. Looking under the hood of additional changes driven by high-speed SERDES, however, you also find:

- Insertion loss of a SERDES signal is a fairly linear function of the signal speed – i.e., all other things equal, SERDES at twice the frequency will only be able to communicate approximately half the distance of the previous generation (**Figure 3**). This will drive either costly repeaters on the board, or other novel solutions that are less affected by frequency increase and insertion loss.
- Isolation requirements (how many ground BGAs are needed for shielding around each SERDES communication link) increase by 10-15% when signal speed is doubled. That also means that packages sizes will have to grow by 10-15% in area to provide the extra space for these isolation BGAs.

The above two bullets are cost-adders, and “inconveniences,” but the primary problem comes in when we look at the roadmap for increased electrical data rates: The industry experts agree that at 112Gbps we will reach an end to the traditional SERDES scaling that can be routed on



**Figure 4:** Shannon's Limit for long-reach interconnect.

a board. Information theory, as described by Shannon's Limit (**Figure 4**), predicts the end of doubling of the SERDES speed with the same integration scheme. The only other way to double SERDES bandwidth in conventional technology would be doubling the number of SERDES lanes – also roughly doubling the area of the package. In addition to the substantial substrate cost increase (a 3rd power exponential function), card assemblers (who are already uncomfortable with the current 65-75mm modules) would have to create new 2nd level attach techniques. Overall, this does not appear as a good path.

Optical integration is the only light at the end of the tunnel that could enable the needed continuation of bandwidth growth for networking products. The challenge will be to devise a modular electrical-to-optical conversion right on the processor module, and to connect optical fibers directly to the module. This will require the networking ASIC to be co-packaged with several optical chips (and likely some other logic support chips as well), again a step function increase in package complexity.

**Technology scaling has become incredibly expensive.** While the total cost of creating a 14nm chip is estimated to be around \$80M, the expected total cost for a 7nm chip is around \$300M — a 3 to 4x cost increase. And the same 3 to 4x cost increase is expected again when moving from 7nm to 3nm, where designs are expected to reach \$1B and beyond. This dramatic cost increase will drive partitioning and reuse,

where only the portion of a chip is in the next node that really must have the newest technology, whereas all other functionality will be integrated in prior node silicon in the same module.

Summarizing the driving forces for these high-end networking applications:

1. Memory components are moving inside the package to satisfy memory bandwidth access.
2. Scaling of SERDES speed for long reach communication will hit the bandwidth wall at around 112Gbps, and the signal connections will need to be replaced with lower loss technologies – most likely optical connections on the module.
3. Technology scaling is becoming exceedingly expensive, which very few companies will be able to afford (and only for the content that absolutely must be in the next node). Most other applications will move to a mix-and-match approach where different technologies (optimized for a particular task) are integrated into one module.

None of these drivers are compatible with the conservative single-chip module (SCM) packaging technology traditionally used in that application space. In many ways, memory requirements and HBM integration have opened the minds of architects to “think outside the box” of monolithic integration. This new and seemingly limitless

thinking is leading to architectures that would have resulted in vigorous head shaking just a few years ago.

If we accept the conclusion that many of the traditional single-chip modules will get replaced by more “insane” levels of on-module integration with more and more content, then the next big question is: how do these different chips in a module communicate with each other? What will be the interface of choice between them?

Many chip IP providers have recognized this challenge, and have started creating custom short-reach interfaces targeted for on-module communication. Because the different chips that get integrated into the same package must speak the same language (yet may come from different sources), these interfaces will require standardization. None of them, however, have found wider acceptance at this point. Let’s take a look at the critical attributes, and visit some of the approaches with the understanding that the goal is to communicate over a short distance from one chip to another chip within the same module. Key attributes are therefore:

**Bandwidth efficiency.** Many MCM use-cases demand excessive amounts of data to be moved between chips. The communication interfaces enabling this must be on the edge of the chips. There exists a limited amount of chip-edge (or “beachfront”) available for these interfaces. The most critical parameter for these interfaces is, therefore, the “chip edge bandwidth efficiency,” i.e., how much data can be communicated per mm of chip edge.

**Power efficiency.** The challenge is actually more about power-out than power-in. With ever-increasing power density of high-performance networking chips, it becomes increasingly more difficult to remove the heat from a module. Communication interfaces typically use a sizable 30% of the chip’s power in a networking SCM. Adding more interfaces and additional chips in the module further increases the already tight thermal budget.

The two primary interface types are serial and parallel. Serial interfaces generally run at significantly higher speed per signal (up to 112Gbps), but are more complex, introduce additional latency, and often consume more power. Conversely, parallel interfaces are simpler, generally more power efficient, but run considerably slower, necessitating a significantly greater number of signal interconnects.

The best example of a parallel interface is the HBM: over 1,000 signal wires running at 2Gbps enable 2Tbps of bandwidth, but drive the need for a silicon interposer to enable the signal count.

Other approaches for interface options are somewhat in-between a traditional SERDES and a parallel interface (we can call them “weird serial” for now). These approaches include fast I/O with equalization built into the signaling scheme, single-ended serial interfaces, etc. There are currently at least five similar but competing nonstandard interfaces proposed from different original equipment manufacturers (OEMs) and IP providers. Unfortunately, none of these are really interoperable with each other.

Aiming to influence the direction of interface standardization, alliances (e.g., USR Alliance) have formed, proposing different approaches while striving to emerge with the industry-standard solution. All options have pros and cons, and none have yet found widespread adoption, but they all share the need to be custom-tailored with specific packaging technologies.

Looking forward, all of the package integration plays described so far are based on 2-dimensional side-by-side integration of chips (even if we call them 2.1D, 2.3D, or 2.5D). While the trace lengths of a couple of millimeters between chips sounds short, there is significant opportunity to further reduce I/O power when considering true 3D integration. Current expectations suggest a 90-95% reduction in interface power for 3D integration compared to 2-dimensional integration. This is due to:

- Lower load capacitance of the ~50 $\mu\text{m}$  long TSV compared to an ~2mm long signal trace;
- Lower I/O drive strength; and
- Elimination of any need for equalization or termination.

In addition to this tremendous power reduction, the small size and density of the TSVs enable higher signal density between chips, and therefore also orders of magnitude greater bandwidth.

## Summary

The approach of creating discrete modules for specific purposes is ending and will be replaced by more complex

packaging integration. The best solution will be the one offering the greatest bandwidth and the lowest power per transferred bit. While we will inevitably encounter even more outlandish proposals along the way, the ultimate solution will be 3D integration.

## Biographies

Wolfgang Sauter received his MS in Mechanical Engineering at The Technical U. of Munich and his PhD in Mechanical

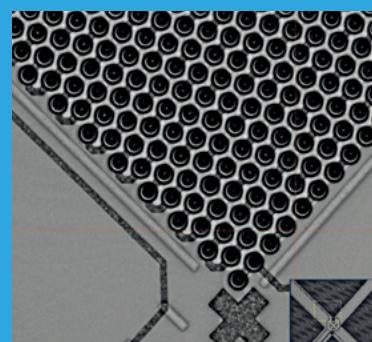
Engineering at the U. of Vermont. He is a Distinguished Member of Technical Staff at Avera Semi, a wholly owned subsidiary of GLOBALFOUNDRIES; Wolfgang.Sauter@globalfoundries.com

Mark Kuemerle received his MS from Case Western Reserve U. He is a Fellow for Integrated Systems Architecture at Avera Semi, a wholly owned subsidiary of GLOBALFOUNDRIES.



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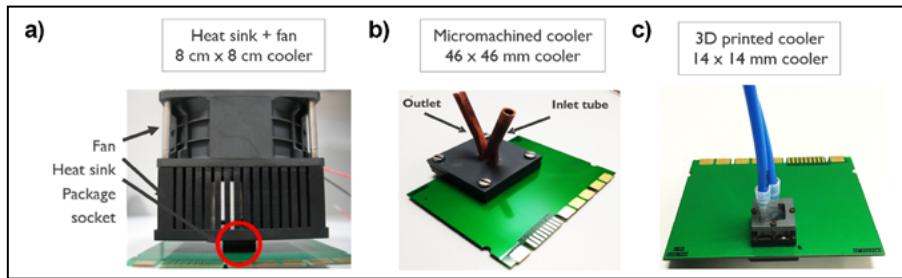
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# A cold shower for chips

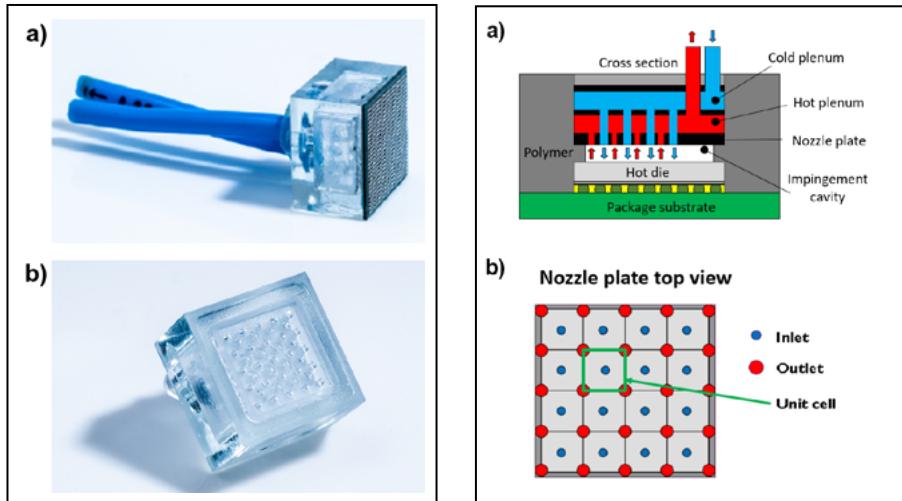
By Herman Oprins, Tiwei Wei, Vladimir Cherman, Eric Beyne [imec]

**C**ooling the electronics in large data centers comes with a heavy price tag. It is estimated that almost half of the electricity bill for such centers is dedicated to powering the ventilators for air cooling. Moreover, with increasing power-intensive applications and server densities, air cooling capacity is quickly reaching its limits and server rooms are running out of space for the large fans. Liquid coolants are gaining in importance as a more economically viable alternative to meet future cooling and footprint demands. In order to cool down 100W, a fan and heat sink combination of several 100cm<sup>3</sup> is needed, compared to a liquid cooling unit that is a factor of 1000 times smaller (**Figure 1**). Because the cooler has similar dimensions to the chip package, it can also be placed in close proximity to the heat source, which allows for packing more chips in a rack, thereby increasing compute density.

Many large data centers are now making the jump from air to liquid cooling. While the transition already means a significant improvement in cooling efficiency, there is still a lot to gain in the specific design of the cooler. The most common method to achieve liquid cooling is through the use of “cold plates.” These metal plates with flow paths guide liquids and are directly glued onto the chip. Drawbacks of this technique are the presence of the thermal interface material (TIM), creating a fixed thermal resistance, and the formation of a temperature gradient across the chip surface. Especially the layer of glue presents a real thermal bottleneck for the heat removal that cannot be addressed by further optimization of the cooler itself. Liquid jet impingement cooling might be a solution. By opening up the backside of the chip and allowing direct contact between the liquid coolant and chip (**Figure 2**), the TIM thermal resistance is avoided. Moreover, vertical impingement ensures that all liquid that hits the chip surface has the same inlet temperature.



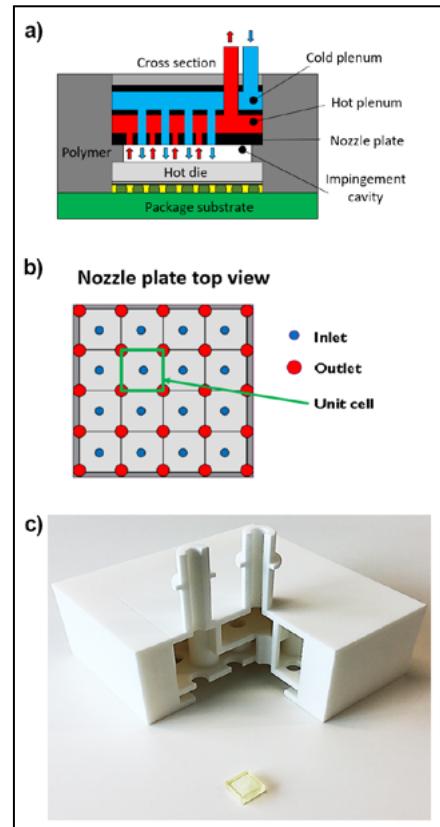
**Figure 1:** a) (left) Air cooling installations have a larger footprint than liquid alternatives; b) (middle) Micro-machined liquid coolers and especially c) (right) the current 3D-printed liquid coolers can be up to an order of magnitude smaller.



**Figure 2:** a) (top) The liquid jet impingement cooler is attached to the chip; b) (bottom) The nozzle array sprays cooling fluid directly onto the open backside of the chip.

## Liquid economy

Imec’s jet impingement cooler directly cools the backside of high-performance chips or chip stacks, but is fabricated using low-cost polymer fabrication techniques. The key part of the system is an array of nozzles that acts as a “showerhead” for each chip (**Figure 3**). The nozzle array is made up of the distributed inlets and outlets on the nozzle plate. The inlet tubes in the inlet plenum feed the liquid into the individual inlet nozzles, while the outlet tubes in the layer above collect the outflow. The interaction between inlet and outlet flows happens in the cavity region where the fluid is in contact with the chip.



**Figure 3:** a) (top) Cross section of the 3D-printed cooler; b) (middle) Top view of the nozzle plate with distribution of NxN inlets and outlets; and c) (bottom) 3D-printed model of the internal structures.

Impingement cooling solutions have already been successfully implemented for large (30-50cm) modules for power electronics that generate kilowatts. For the integration to chip or

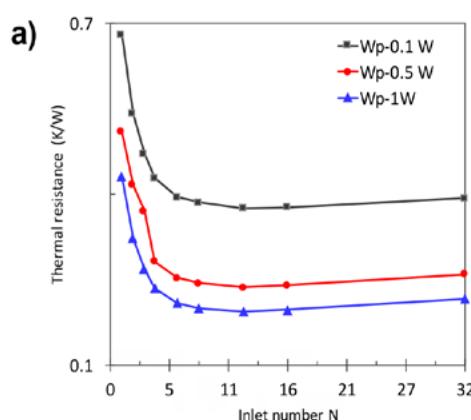
package level, many bare die cooling solutions have been proposed, mainly based on expensive Si processing techniques. Imec presents a low-cost but highly efficient alternative based on 3D-printing techniques. While this technique cannot attain the resolution of Si nozzles, this might not be necessary. It is true that thermal performance of smaller apertures is higher, the need for a higher pump pressure to guide the cooling fluid through the nozzles, makes the overall yield limited. Moreover, imec's simulations and measurements demonstrate that a similar performance can be achieved with mm-size nozzles at reduced costs.

### How many showerheads to cool a chip?

With a unit cell model imec researchers assessed the optimal number of nozzles, nozzle pitch and diameter for an 8x8mm<sup>2</sup> test chip. A part of the nozzle array with one inlet shared by 4 outlets is considered a unit cell. The simulations show that the more nozzles are introduced, the more the temperature decreases and the more uniform the temperature profile. And the more nozzles you need, the smaller they become for a given chip area. A higher number of small diameter nozzles can indeed achieve a better thermal performance – or decrease in thermal resistance – but comes at the expense of the required pump power. Similarly, increasing the flow rate can result in a further increase in thermal performance, but again requires a higher pressure. Taking into account this tradeoff between thermal performance in terms of thermal resistance and pump power, the simulations show that it becomes less energy efficient to increase the number of nozzles beyond an 8 by 8 array of inlet nozzles on the chip surface (for a fixed 200μm cavity height) or in other words, 1 nozzle per mm<sup>2</sup> (**Figure 4a**). Moreover, for a 1mm<sup>2</sup> unit cell the nozzle diameter at the saturated performance is then on the order of several hundreds of μms.

### A cooler material

The choice of the number of nozzles and the nozzle diameter impacts the required fabrication technology, with finer nozzle diameters requiring more expensive processing options. For the 8x8mm<sup>2</sup> test chip and accompanying

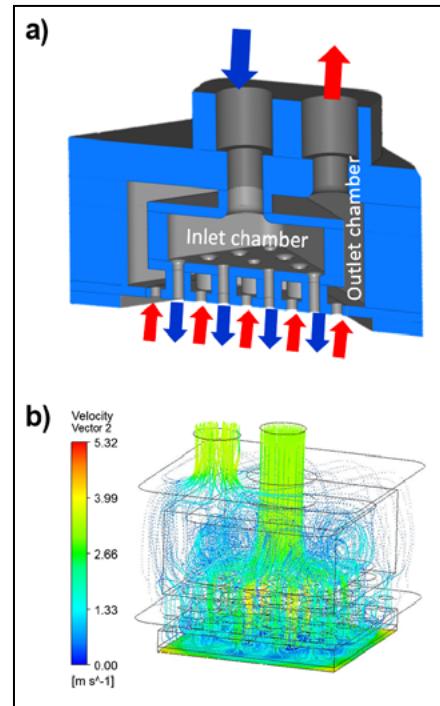


N×N	Inlet diameter	Fabrication technology
1	2.4 mm	Mechanical machining process
2×2	1.2 mm	
4×4	600 μm	Injection molding / 3D Printing
6×6	400 μm	
8×8	300 μm	Silicon processing
16×16	150 μm	
32×32	75 μm	Silicon processing
64×64	38 μm	

**Figure 4:** a) For a constant pumping power (Wp) thermal performance saturates beyond an 8x8 nozzle array; b) The resulting nozzle diameters for this size of nozzle array are in the fabrication possibilities of 3D-printing.

nozzle diameters, 3D-printing is a viable option (**Figure 4b**). Recent advancements in the technique made it possible to print structures with diameters ranging from 100μm to 1mm. Silicon processing has the advantage that it can be used to fabricate small diameter holes below 10μm with deep reactive ion etching (DRIE) technology. However, the cost of silicon processing is higher than the other fabrication methods. Besides, the simulations demonstrated that further downscaling of the nozzle diameter is not necessary due to the saturation in thermal performance.

Polymer fabrication may be cheaper than Si processing techniques, but does it meet the same performance standards? After all, polymers have a much lower thermal conductivity compared to Si, resulting in a higher thermal resistance for thermal conduction. Therefore, good thermal conductors such as Cu or Al are typically used for heat sinks as opposed to insulators, such as polymers. To study the impact of the cooler material on the chip temperature, imec researchers used a model of the full cooler that shows the thermal and hydraulic interaction of the different nozzles and the impact of the thermal conductivity of the cooler material (**Figure 5**). The results demonstrate that a polymer cooler has the same performance as a Si or Cu cooler, because the heat removal is in this case dominated by forced convection in the coolant. This opens opportunities for the use of polymer-based low-cost fabrication options.



**Figure 5:** a) (top) Model of the full cooler showing b) (bottom) the flow field of the coolant.

### The power of printing

Aside from the price tag, 3D-printing offers several advantages for the fabrication of a polymer liquid jet impingement cooler. Firstly, the cooler can be printed as a single piece, while, for example, mechanical machining still requires gluing separate parts. Secondly, the technique allows for the fabrication of complex internal structures. This is especially interesting when creating the intricate combination of inlets and outlets to guide the flow in the cavity. Finally, because of the

versatility of 3D-printing, the design can be modified at any moment to accommodate the chip. This ensures that the location of the nozzles coincides with the hottest sites on the chip. Whenever a chip with a different layout needs cooling, the design can be easily adapted and the cooler reprinted.

At the same time, 3D-printing also poses specific design challenges. There are, first, restrictions on nozzle diameters and other small features such as the cavity height. Printing techniques like digital light processing or stereolithography leave excess liquid resin after curing of the polymer that needs to be removed from the internal cavities. Therefore, resin removal places constraints on nozzle diameters and plenum thickness. A second, concomitant challenge is the difficulty to check if internal structures are free from resin, because the cooler is printed as one part. For this application, imec demonstrated that the scanning acoustic microscopy technique (SAM) can be used to check for potentially blocked resin inside the nozzles. Finally, nozzle side walls should be sufficiently strong to prevent the wall from collapsing, which could result in a “liquid short-circuit” between the inlet and outlet flow. All structures should therefore be self-supporting.

## The cooler put to the test

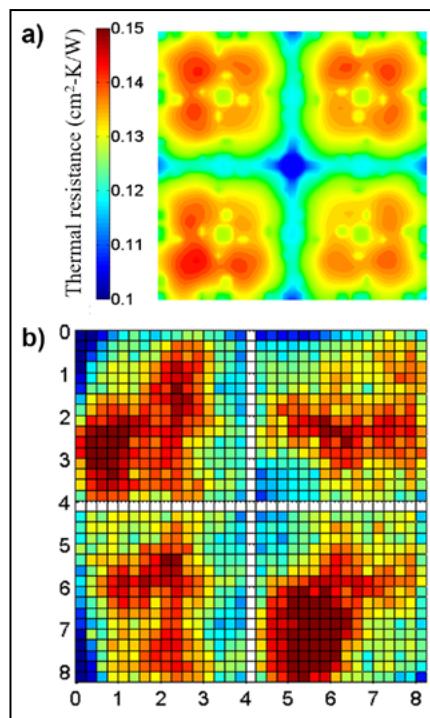
To test the design experimentally, imec fabricated an impingement cooler for an  $8 \times 8 \text{ mm}^2$  test chip. This test chip contains a number of heaters and sensors, making it possible to create a power dissipation pattern and measure the temperature in more than 1000 points over the entire chip surface. It was used to locally measure the temperature effect at the inlets and outlets and evaluate the quality of the cooler. Furthermore, the chip allows for an assessment of the ideal number of nozzles. For this, 3x3 up to 8x8 nozzle arrays were printed, resulting in nozzle diameters ranging from 300 to 800  $\mu\text{m}$ .

The best thermal performance was noted for the cooler with the highest number of nozzles (8x8), while the 3x3 nozzle array performed worse. Moreover, compared to a single-jet cooler with 1 inlet for the same chip, a multi-jet impingement cooler has a

lower thermal resistance and a better temperature uniformity for the same flow rate. All printed nozzles are within 5 to 10% of the nominal design diameters. Systematic deviations – either smaller or larger – can be compensated for in the design. Finally, the comparison between the measured temperature map and simulation results with fabrication parameters show good agreement ([Figure 6](#)).

## How cool is the chip cooler?

To put the cooler into perspective, it was compared to published data of other impingement coolers in terms of thermal resistance and pump power. For this, coolers fabricated in different materials were considered: Si, ceramic, metal and plastic. The imec cooler displays a very good thermal performance of  $0.13 \text{ cm}^2 \text{ K/W}$  for the 8x8 nozzle array at a 1000 ml/minute flow rate and a 0.3 bar pressure drop between the inlet and the outlet of the cooler. In other words, with this cooler, the chip will only heat up  $13^\circ\text{C}$  for each  $100 \text{ W/cm}^2$ , the typical power density for a standard processor, where the limit is around  $100^\circ\text{C}$ . With this performance, cooling of  $500 \text{ W/cm}^2$  would be feasible, making it one of the best cooler performances in literature.



**Figure 6:** a) (top) Model and measurement of the  $8 \times 8 \text{ mm}^2$  test chip thermal resistance for a b) (bottom)  $4 \times 4$  array impingement cooler with  $600 \text{ ml/min}$  flow rate.

Only Si-based coolers with  $\mu\text{-pitch}$  nozzles outperform the imec cooler. However, those coolers need up to five times more pump power and are considerably more expensive. At the end of the day, the price tag is an important benchmarking criterium. Making the choice for a certain fabrication technique or material is based on the goal to reach as much cooling power per pump power. But it also determines the price of the cooler, which makes energy costs for data centers enormous.

## Summary

This benchmarking study clearly shows that it is not necessary to aggressively scale down nozzle diameters to a few tens of microns, but that very good thermal performance can also be achieved with nozzles in the range of a few hundreds of micrometers. At these sizes, cheaper polymer fabrication technologies, such as 3D-printing, can be used. Moreover, the simulations indicate that the thermal conductivity of the cooler material has no impact on thermal performance of the impingement cooler. Therefore, despite being made out of insulating materials, the polymer coolers achieve similar cooling performance as coolers in materials with good thermal conductivity. This makes the 3D-printed liquid jet impingement cooler a very cost-effective alternative to more expensive coolers for data centers to use.

## Biographies

Herman Oprins received his MSc and PhD degrees in Mechanical Engineering from KU Leuven, Belgium. He is a Senior Researcher at imec; email Herman.Oprins@imec.be

Tiwei Wei received his MSc degree in Optoelectronic Engineering from Chongqing U., China. He is a PhD candidate at KU Leuven and imec.

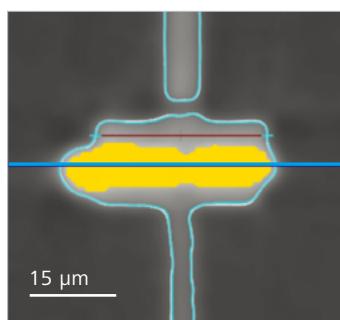
Vladimir Cherman received his MSc and PhD degrees in Electronic Engineering from Saint-Petersburg Electrotechnical U., St. Petersburg, Russia. He is a Senior Researcher at imec.

Eric Beyne received his MSc degree in Electrical Engineering and PhD degree in Applied Sciences from KU Leuven, Belgium. He is a Fellow and Program Director at imec.

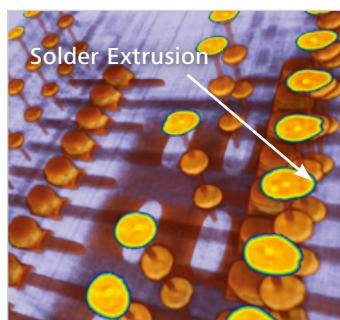
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# Air and liquid cooling solutions advance to meet thermal needs of ICs

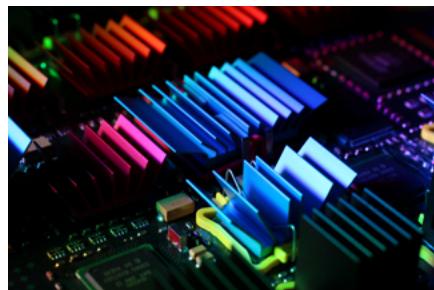
By Josh Perry *[Advanced Thermal Solutions, Inc.]*

Integrated circuits (ICs) have revolutionized electronics since the first one was designed by Texas Instruments in 1958 and they are now used in everyday electronics such as computers, mobile phones, and home appliances. Over the decades, as semiconductor technology has advanced, ICs have become smaller, faster, and more powerful with billions of transistors in a space no larger than a fingernail. Despite enhancements in fabrication techniques and advanced materials, one thing has remained constant throughout the years: thermal management is critical to ensure maximum performance over the full lifetime of the chip, to avoid errors, and to optimize mean time between failures (MTBF).

Heat is a menace for electronics, irrespective of the market sector. It doesn't matter what the final product is, heat must be managed to ensure proper performance. To maintain operation, the heat must flow out of a semiconductor at such a rate as to ensure acceptable junction temperatures. This heat flow encounters resistance as it moves from the junction throughout the device package, much like electrons face resistance when flowing through a wire.

In thermodynamic terms, the resistance described above is known as conduction resistance and consists of several parts. From the junction, heat can flow toward the case of the component, where a heat sink may be located. This is referred to as  $\hat{I}_{JC}$ , or junction to case thermal resistance. Heat can also flow away from the top surface of the component and into the board. This is known as junction to board resistance, or  $\hat{I}_{JB}$ . Because of the multiple heat transfer paths within a component, a single resistance cannot be used to accurately calculate the junction temperature. The thermal resistance from junction to ambient must be broken down further into a network of resistances to improve the accuracy of junction temperature prediction.

As board layouts become denser, there is a need to design optimized thermal solutions that use the least amount of space possible. Simply put, there is no margin to allow for over-designed heat sinks with tight component spacing. When there is more than one component, the situation becomes much more complex than with just a single component on the board. There is conduction coupling between components through the printed circuit board (PCB), and radiation and convective coupling between the components and adjacent cards (**Figure 1**).



**Figure 1:** Heat sinks dissipate thermal energy from ICs through convection, conduction, and radiation heat transfer.

Numerous solutions have been designed through the years to deal with excessive heat from increasingly powerful chips, but air cooling remains the standard because of cost and ease of implementation. Liquid cooling solutions are gaining in popularity as heat dissipation requirements exceed the capability of air to manage and there are new techniques, such as direct-to-chip cooling, which are being researched, but only infrequently implemented.

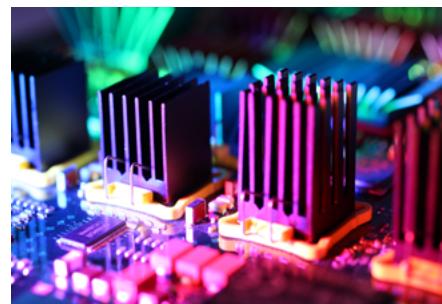
## Air cooling

Although liquid cooling has been gaining momentum, air cooling is still the first solution for cooling high-powered chips. A heat sink is a passive heat exchanger, typically composed of

copper or aluminum and consisting of a base and fins that extend outward, which have been essential to the thermal management of integrated circuits. Conduction, convection, and radiation heat transfer are all at work when using a heat sink. The heat spreads into the fins and the flow of air causes a change of enthalpy across the heat sink surface to remove the heat.

Temperature distribution and air distribution in any electronic system are temporal and spatial. Even between cards in a telecom chassis you will see a significant temperature gradient from the top to the bottom. It is important to remember that when heat is generated it goes in every direction, including into the board upon which the device is sitting. Because heat is going in every direction, air management must also be considered. Heat will be carried by the airflow to other devices, which will impact their junction temperatures.

Different heat sink geometries produce different heat transfer rates. Standard geometries include pin fin or straight-fin designs, while more intricate spread fin or wavy fin arrays increase the surface area of the heat sink and improve its thermal performance (**Figure 2**). Engineers will also need to optimize spreading resistance from the component to the heat sink, and in many cases this can be solved by increasing the thickness of the base.

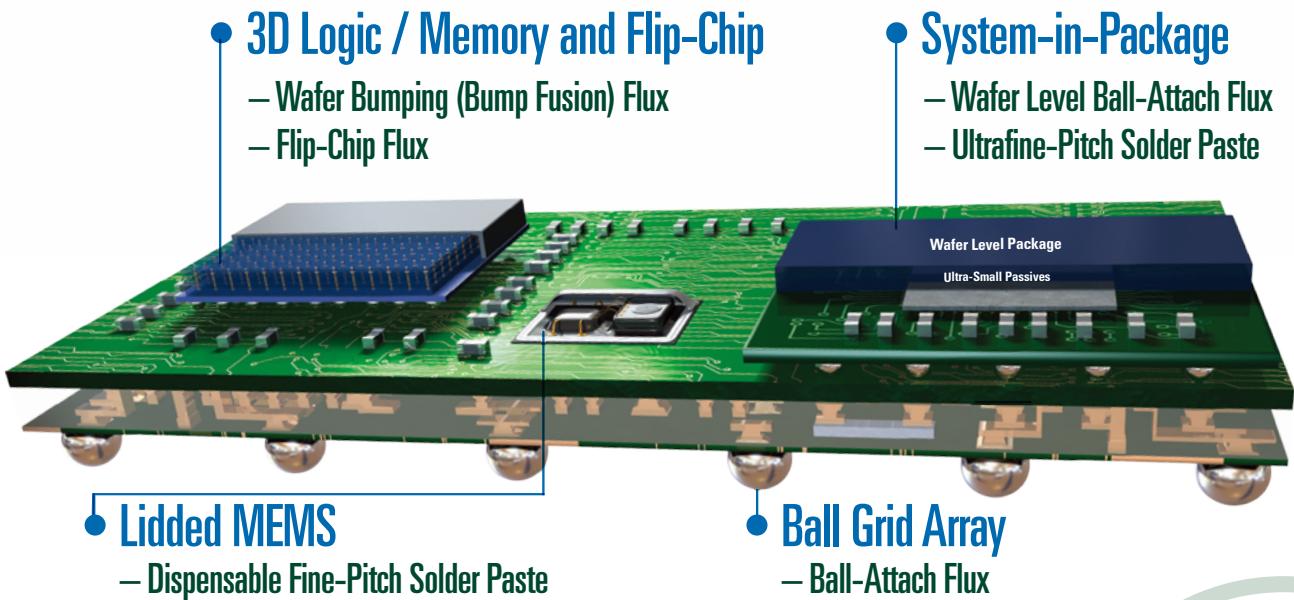


**Figure 2:** Pin fin heat sinks are a common air cooling solution in systems with high or ambiguous airflow.

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To improve the performance of heat sinks, fans or blowers can be added to a system. Through the years, fan designs have improved. Fan blades have been streamlined to produce great flow rate with less noise and fans have become more power efficient to meet the desires of customers trying to use less resources and save costs.

New materials are constantly being developed to improve the effect of air cooling. Graphene/graphite and diamond are two options that increase the heat transfer capabilities of a heat sink but are limited by issues of manufacturability and cost. In addition, engineers are exploring new thermal interface materials to improve the connection between the heat sink and the chip, which will increase heat transfer.

Not only are the components themselves getting higher powered, but increased demand for functionality in ever-smaller packages has meant that these components are increasingly being squeezed into tighter areas. Engineers have turned to heat pipes or vapor chambers as tools to transfer heat away from components. Heat pipes alone will not remove the heat, but

rather simply move it from one place to another, they can, however, be attached to a heat sink assembly that will remove the heat to the ambient. The small form factor of heat pipes make them increasingly popular in telecommunications, mobile, and Internet of Things (IoT) applications where space is at a premium and a heat sink may not fit on top of a chip.

### Liquid cooling

There has been talk for years about how liquid cooling is the future of electronics thermal management. While air cooling retains its supremacy, the future is now moving to liquid cooling. Many engineers have designed liquid solutions for removing excess heat from ICs and other components. Typically, a liquid loop contains a cold plate (usually aluminum or copper) located on top of the component to pull heat away from the chip and transfer it to a fluid and a heat exchanger that transfers the heat from one fluid to another (either air or liquid) before the fluid flows back across the chip.

Water transfers heat much better than air, so liquid cooling provides higher thermal performance than a heat sink, but it also requires a pump to keep the fluid circulating, which increases the energy costs of the system, and can be bulky and difficult to implement at the chip level. There are challenges to liquid cooling, but cold plates can keep junction temperatures within the operating range while dissipating several hundred W/cm<sup>2</sup>.

Liquid is increasingly common in electronics as new materials are used in chip packaging, such as silicon carbide (SiC) and gallium nitride (GaN), which can withstand higher power densities and higher temperatures. But the higher heat loads and the desire for smaller packaging mean passive, air cooling techniques are unlikely to accommodate the thermal management needs of the system.

Researchers have also designed on-chip cooling solutions, immersion cooling solutions, and liquid cooling of three-dimensional chip stacks that can remove even greater heat fluxes. Boiling and jet impingement (spray) cooling solutions that were originally designed for larger systems are also being integrated for thermal management at the chip level.

Nanofluids (or engineered fluids) are another important development in IC liquid cooling. The nanoparticles dispersed in a base fluid are typically metal or metal oxide particles with a size range of 1-100nm. Researchers were able to demonstrate as much as a 20% enhancement in heat transfer performance of the single-phase, liquid-cooled system when nanoparticles were introduced.

### Summary

At the chip level, designers need to factor in the package type and materials, power dissipation fluctuations, power dissipation from adjacent components, spacing between components, and the thermal resistance of critical components to design an optimal thermal management solution. Engineers continue to use air cooling solutions as a cost-effective means for dissipating enough heat to keep IC junction temperatures at proper operating levels. Heat sinks (along with fans or blowers) provide the necessary cooling for the majority of chips, but as semiconductor technology continues to develop and chips become denser and more powerful, then liquid solutions will be required.

Advanced materials are creating new packaging techniques to mitigate the effects of heat at the packaging level and there are techniques, such as microfluidics, that hold promise for the future of IC cooling.

### Biography

**Josh Perry** is a Marketing Communications Specialist at Advanced Thermal Solutions, Inc.; email [jperry@qats.com](mailto:jperry@qats.com).



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# Advanced eWLB solutions for 77GHz ADAS mmWave applications

By Dian Wang, Fazhi An [Calterah Semiconductor Technology (Shanghai) Co., Ltd.]  
Seung Wook Yoon [STATS ChipPAC Pte Ltd. JCET Group]

**S**emiconductor packaging can have a significant impact on the overall device cost and performance. In terms of the performance, size and scalability, traditional packaging technologies are reaching their limits with respect to the severe challenges related to emerging applications. Over the next 10 years, the automotive integrated circuit (IC) market is forecasted to outgrow the rest of the IC market by a factor of two [1]. Currently, 8,000 electronic components are used in the Audi A8 and over 2,000 electronic parts are used per automobile on average with 80% of innovations in automotive technology coming from semiconductors [2].

In terms of performance, power consumption, integration and reliability at a required cost, current and future demands of automotive semiconductors are met by developing advanced silicon process technology, innovative packaging solutions based on chip and package co-design, low-cost materials, reliable interconnect technologies, and advanced assembly and test manufacturing systems.

## Emerging WLCSP market of mmWave applications

Market trends as experienced by end applications drive the emergence and evolution of any package technology. Currently, the primary automotive packaging solution is leaded or laminate wire bonding, which account for more than 80% of the total assembly market.

The smallest possible package size is the wafer-level chip-scale package (WLCSP) because the final package is no larger than the required circuit area. Since its introduction, WLCSP has experienced significant growth on account of its small form factor, lower cost, and high-performance requirements of mobile and portable applications.

WLCSP and 77GHz radar sensors with fan-out wafer-level packaging (FOWLP)

are already well adopted in the automotive market for cabin or infotainment and automotive driver assistant system (ADAS) safety [3,4]. The range of applications continues to expand with the ultimately larger wave in the development of next-generation automotive capabilities, i.e., electric vehicles (EV) and automated vehicles (AV). The car radar market is expected to grow 28% annually (2015-2022) and reach more than \$200M in packaging and assembly.

## eWLB/FOWLP for 77GHz mmWave & automotive radar applications

In today's vehicle safety systems, radar is used in conjunction with cameras, ultrasound and other sensors to obtain information about a vehicle's surroundings. As shown in **Table 1**, a radar sensor has more advantages over other ADAS sensors. It can easily operate in cloudy, rainy weather conditions, and at night. It supports a longer operating distance too.

	Radar	Lidar	Ultrasonic	Camera
Short Distance < 2m				
Long Distance 200-250m				
Angle Measurement	Medium	High	Low	Low
Direct Velocity Measurement	Medium	High	Low	Medium
Working in Rain	Medium	High	Low	Medium
Working in Snow/Fog	Medium	High	Low	Medium
Working under dust	Medium	High	Low	Medium
Working without sensor exposed	Medium	High	Low	Medium
Cost	Medium	High	Low	Low

**Table 1:** Comparison of various ADAS solutions.

With Si-based front-end technologies showing improved performance, wireless systems at millimeter wave (mmWave) frequencies are becoming more and more important [4-6]. Adaptive cruise control (ACC) radar systems at 77GHz [7, 8], point-to-point radio links at 60GHz, or high-resolution radio imaging at 94 and

140GHz [9] are just a few examples of the applications observed for upcoming markets. The impact of packaging on the overall electrical performance of the IC becomes increasingly important with frequencies increasing beyond 10GHz. Therefore, for the crucial development of commercial mmWave applications, the availability of high-performance packages for monolithic microwave integrated circuits (MMIC) is crucial.

Traditionally, many of these systems used frequencies in the 24GHz band. For automotive, both a narrow band (NB) and an ultra-wide band (UWB) are currently available. Due to spectrum regulations and standards developed by the European Telecommunications Standards Institute (ETSI) and Federal Communications Commission (FCC), the use of the UWB band will be phased out by the year 2022 (the "sunset date") in both Europe and the U.S. In phasing out the 24GHz UWB, the regulating authorities have opened up frequencies for automotive radar in the 77GHz band. Radar sensors serve short-, mid- and long-range radar (SRR, MRR, LRR) with the bandwidth available from 77-81GHz providing up to 4GHz of sweep bandwidth [10,11].

A very promising solution for mmWave packaging is the embedded wafer-level ball-grid array (eWLB) platform [12,13]. It is based on an embedded device technology with fan-out redistribution. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. The length of the redistribution lines is within the range of the die size. eWLB has the ability to attain minimum interconnection length and excellent electrical

performance. eWLB can achieve the minimum interconnection length and excellent electrical performance up to mmWave frequencies. The conversion gain and the noise figure of the mixer affect the performance of the overall system. Therefore, a high-transmission performance of the mmWave signal is very important in the design of a package.

With the push toward autonomous driving and automated vehicles, the

research and development programs for sensors enabling the above mentioned technologies have gone into high gear over the last several years. SRR, MRR and LRR sensors are essential components for the overall sensors needed for the complete implementation of automated vehicles. Many packages in these segments use advanced packaging options such as fan-out eWLB, with lower parasitics at 77GHz [14].

For radio frequency (RF) and high-frequency devices, eWLB showed less parasitic electrical interference, therefore, significantly improving overall device electrical performance. In one example, a 77GHz SiGe mixer packaged with eWLB achieved excellent high-frequency electrical performance due to the small contact dimensions and short signal pathways or interconnection length, which decreased parasitic effects [15,16].

The sections below demonstrate the advantages of the eWLB packaging solution for the mmWave device or high-frequency applications as compared to substrate or laminate-based packaging, such as flip chip or wire bonding.

**Interconnection length.** eWLB enables integration where the distance has to be as short as possible (loss increases with distance) to minimize loss (assuming both technologies have the same material loss).

**Conductance loss.** Plated Cu used in organic substrate materials has large surface roughness because of the process used to improve adhesion and plating process control. eWLB uses a thin-film fab process for the seed layer and a well-controlled Cu plating to achieve a smooth Cu RDL surface, which is more effective for skin effect in high-frequency ranges (i.e., at 100GHz, Cu skin depth is ~0.2mm).

**Dielectric loss.** Organic substrate materials have high losses in the mmWave range. Furthermore, heterogeneous material sets bring complexity in terms of electrical behaviors. eWLB uses molding compound and low-loss dielectric materials that enable the achievement of less dielectric loss.

**Design flexibility.** eWLB provides more design flexibility for less routing interference with fine line width (LW) and line spacing (LS) capability (less than 10/10 $\mu$ m LW/LS).

One key element for the change from a rather complex and expensive solution to an easy-to-use and, therefore, inexpensive and affordable product is the use of standard surface mount device (SMD) packaging technology. The eWLB package is SMD attached, thereby simplifying the upstream assembly process and has already been proven in a few mmWave applications.



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Items	Specification
PKG size	6.6x6.6mm
Die Size	3x3mm
Ball Pitch	0.5mm
Ball Dia	0.3mm
IO No.	111
UBM	No
Cu RDL No.	1 layer
Die Thickness	0.4mm
PKG Thickness	0.8mm

**Table 2:** Device specifications for a single-die eWLB device.

Items	Specification
PKG size	6.8x9.8mm
No. of Die/Die Size	2-die / 2.7x2.8mm
Ball Pitch	0.5mm
Ball Dia	0.3mm
IO No.	128
UBM	No
Cu RDL No.	1 layer
Die Thickness	0.4mm
PKG Thickness	0.8mm

**Table 3:** Device specifications of a two-die eWLB device.

Test	Q100 Test Condition	Test Conditions	Pass
PC Preconditioning	JEDEC J-STD-020	MSL124 h bake at 125° C Soak 85C 85 %RH 168 hrs Reflow simulation (3times) with lead free profile Tmax=260 C Pre and Post test SAT	✓
HAST Highly Accelerated Temperature Humidity Stress Test	JESD22-A110	110°C/85%RH for 264 hours	✓
UHAST Unbiased Highly Accelerated Temperature Humidity Stress Test	JESD22-A102	110°C/85%RH for 264 hours	✓
TC Temperature Cycle	JESD22-A104	Grade 1: -65°C to 150°C for 500 cycles	✓
HTSL High Temperature Storage Life	JESD22-A103	Grade 1: +150°C Ta for 1000 hours	✓
HTOL High Temperature Operating Life	JESD22-A108	Grade 1: +125°C Ta for 1000 hours.	✓
ELFR Early Life Failure Rate	AEC Q100-008	48 hours at 105° C	✓

**Table 4:** Package-level reliability results of eWLB devices with advanced dielectric materials (ADM).

## 77GHZ ADAS eWLB development

The sections below describe the development steps needed for 77GHz ADAS eWLB development.

**Test vehicle specification.** As a mechanical test vehicle, an eWLB package was designed in 6.6x6.6mm (single-die configuration) and 6.8x9.8mm (two-die configuration) package sizes utilizing low-temperature curable advanced dielectric materials (ADM), which provide robust package reliability [17].

Two test devices were designed and fabricated with CMOS millimeter IC technology and assembled in a single RDL layer, 0.5mm ball pitch (without under-bump metallization [UBM]) standard eWLB structure using ADM. The specification details of each test vehicle are shown in **Tables 2** and **3**.

As seen in **Table 5**, eWLB devices consume less power and reduce Rx noise compared to flip-chip packaged devices. These electrical performance advantages in the mmWave range are enabled by the shorter interconnection lengths and unique material set of the eWLB technology.

The RLC parasitic values for eWLB and flip-chip devices were extracted by computer simulation using the commercial 2D electromagnetic field solver. The model of the chip interconnected to the package can be built as a series inductance from the interaction of signal and ground currents and a shunt capacitance corresponding to the coupling effect between signal and ground interconnects.

The simulation results showed that an eWLB packaged device can have less of a parasitic effect. Compared with C4 bumps, it has a 70% reduction in inductance and a 30% reduction in capacitance. This illustrates that the loss suffered with eWLB packaging is lower than that of a flip-chip chip-scale package (fcCSP) on account of shorter interconnection lengths in eWLB packaged devices.

The signal integrity simulation work was carried out with functional

devices to investigate package-level performance in real applications. In 3D simulations, a few critical pins were selected and studied, such as clock and VDD, as well data pins as shown in **Figure 2**. For signal integrity studies with specific data pins, eWLB showed more than 10-20dB improved cross-talk as compared to flip-chip due to its thinner Cu RDL (3-10μm) and overall shorter interconnection lengths.

## Summary

Thanks to its unique material properties and thin-film RDL with an encapsulated structure, eWLB technology is an important wafer-level packaging solution capable of meeting the challenging high-frequency electrical requirements of future mmWave applications. In this study, single-die and 2-die eWLB reliability was researched at both the component level, as well as at the temperature cycling on

Calterah		Another CMOS Vendor	
	TV1	TV2	-
<b>Process</b>		CMOS	CMOS
<b>Packaging Technology</b>	eWLB	fcCSP	
<b>No. of RF Chips</b>	1	2	1
<b>No. of TX Channels</b>	2	4	3
<b>No. of RX Channels</b>	4	8	4
<b>TX Output Power</b>	12dBm	12dBm	12dBm
<b>RX Noise Figure</b>	12dB	15dB	
<b>Power Consumption</b>	0.65W	1.2W	2.1W
<b>Package Size</b>	6.65 x 6.65 mm	6.82 x 9.82 mm	10.4 x 10.4 mm
<b>Automotive Grade</b>	AEC-Q100		AEC-Q100

**Table 5:** Performance comparison of eWLB and fcCSP 77GHz radar devices.

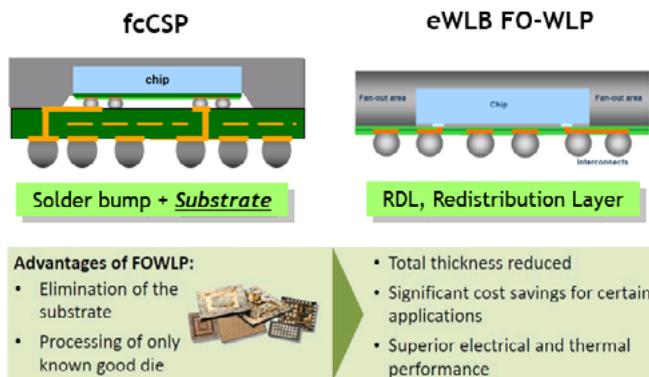


Figure 1: Comparison of fcCSP and eWLB structures, and eWLB advantages.

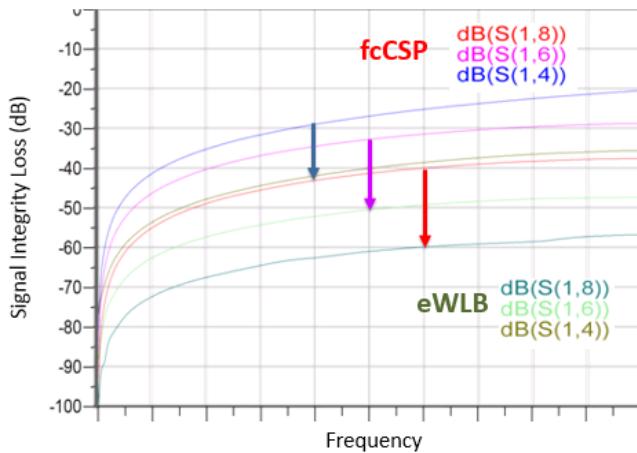


Figure 2: Plot of signal integrity/cross-talk vs. frequency study results of fcCSP and eWLB.

board (TCoB) level with comprehensive design-of-experiments (DOE) studies. Both eWLB configurations passed the AEC-Q100 Grade-1 package-level reliability testing performed.

Furthermore, factors such as superior high-frequency electrical performance in the mmWave range and the ability to enable heterogeneous integration such as: 1) the integration of passives like inductors/resistors/capacitors into the various thin-film layers; 2) active/passive devices into the mold compound or encapsulation; 3) achieve 3D vertical interconnections for new 3D system-in-package (SiP) and 2.5D/3D packaging solutions; and 4) differentiate eWLB from other packaging technologies. eWLB technology provides a more holistic performance relevant to an increasingly broad range of applications including automotive, 5G and mmWave applications, either with antenna on the package (AoP) or antenna in the package (AiP).

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## Biographies

Dian Wang received a PhD from City U. of Hong Kong and is a mmWave Scientist and Acting Product Director at Calterah Semiconductor Technology (Shanghai) Co., Ltd.

Fazhi An received an MS degree in Integrated Circuit Engineering from Fudan U. and is a Mixed-signal IC Design Engineer at Calterah Semiconductor Technology (Shanghai) Co., Ltd.

**Contact author:** Seung Wook Yoon received a PhD from KAIST, Korea, and is Director of Group Technology Strategy at STATS ChipPAC Pte Ltd. JCET Group; email [Seungwook.yoon@statschippac.com](mailto:Seungwook.yoon@statschippac.com)

# Package assembly design kits bring value to semiconductor designs

By Ruben Fuentes, August Miller, Jonathan Micksch [Amkor Technology, Inc.]

**T**oday's state-of-the-art packaging designs allow semiconductor companies and their customers to implement the latest technologies and deliver the "wow-factor" with an ever-increasing number of features and options in space-constrained form factors. Other system constraints include: time to market, design cycle time, accuracy, productivity and more.

To simplify the design of the newest advanced packages, such as high-density fan-out (HDFo) and to address all these other constraints, Amkor has introduced the SmartPackage™ Package Assembly Design Kit (PADK). This article will discuss the need and value of such design kits.

## The value of design kits

Semiconductor and integrated circuit (IC) designers have used process design kits (PDKs) for decades to achieve design for manufacturability (DfM). These foundry-specific PDKs are used with electronic design automation (EDA) tools in the chip design process. These checks are known by IC designers as layout vs. schematic (LVS) and layout vs. layout (LVL) – terms that are not used in the packaging world.

For outsourced semiconductor assembly and test suppliers (OSATS), package designs have relied on verification methods such as

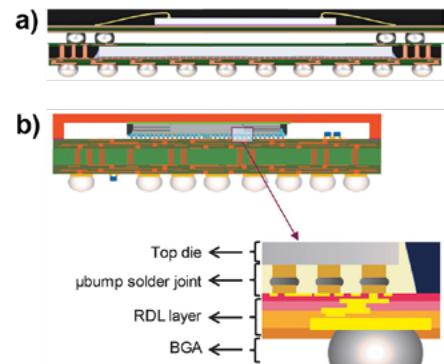
design rule checks (DRC) in computer-aided design (CAD) software and other EDA verification methods such as computer-aided manufacturing (CAM) checks. The combination of these checks ensures that each package design meets the intended manufacturing and assembly requirements.

## Adding packaging to the PDK methodology

As die and package integration complexity continues to increase with 2.5D and 3D structures, so does the need to integrate a die- and package-level verification process – basically, it is the integration of the PDK in IC design and DRC and CAM checks in advanced packaging. An example of this advanced package complexity with redistribution layers (RDLs), vias, interposers, and more is shown in **Figure 1**.

The newest advanced packaging designs, such as high-density fan-out, are at the intersection of the IC design world and the packaging design world. Because PDKs have been used in IC design for many years, they provide an established approach for advanced packages as well. Taking tools that were used exclusively for IC design and applying them to package design creates a bridge between the two domains.

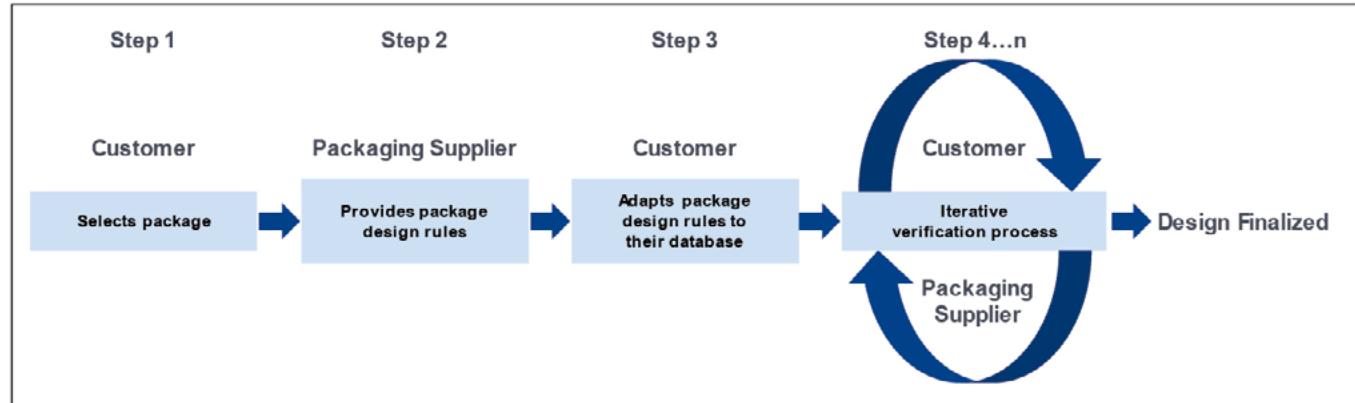
Gerber data is the de facto standard used for exchanging data in the printed circuit board



**Figure 1:** HDO package-on-package (PoP) structures showing a) tall copper pillars on both the right- and left-hand sides; and b) an HDO cross section.

industry and is the typical packaging design export for artwork generation. In contrast, the de facto industry standard for IC designs export is GDSII for data exchange of ICs and IC layouts. For HDO packaging, where the final layers are actually semiconductor-type processes, the GDSII data is essential and a natural extension for design data transfer and provides the best of both worlds.

The existing package design approach is shown in **Figure 2**. Once the user selects a specific package, the packaging supplier provides the design rules. Each customer has their own design database setup where they adapt the package design rules to their specific database



**Figure 2:** The traditional package verification process.

configuration. The number of iterations and length of time to resolve these rules have always been an issue in the traditional package verification process. For today's HDO package designs, this approach no longer works.

To fill the void between die design and package design, Amkor's SmartPackage PADK brings together design, manufacturing, and assembly for HDO packages. Although IC

designers are aware of the process and advantages of PDKs to conduct LVL/LVS verification, they have limited knowledge of package design and package design tool DRC/CAM verification processes. While PADKs offer similar advantages to PDKs, there are some distinct differences in how they are implemented. One of the critical, and often forgotten or neglected, aspects of the traditional process is that packaging

engineers are normally not completely familiar with the IC design process. The same is also true in that IC designers are normally not completely familiar with the package design process. This has created the "perfect storm" as HDO is at the intersection of the IC design world and the packaging design world.

#### Getting packaging details right

SmartPackage PADKs are designed to ensure that the customer's HDO design meets Amkor's design and assembly requirements throughout the design phase. With this tool, there is no guessing whether the proper design rules have been followed. From 3D interconnect, 3D alignment, feature size and routing, the PADK provides an easy to use method to gain greater control and ensure a complete and swift design verification in one pass. SmartPackage PADK verification examples include:

- Pin alignment (die to package);
- Feature size design rule validation;
- Die and component placement design rule validation; and
- Netlist connectivity.

To utilize the SmartPackage PADK, customers are required to use the Amkor Start Point database. This database has all the layer structures, layer classes and subclasses, pad stacks, and essentially all the design rules a customer needs to get started on their design. In the IC world, if the foundry does not provide the database, the IC design house must establish it – which is a long and tedious process. For packaging, Amkor has invested time and effort to develop a Start Point database for customers.

For the new PADK approach, users do not have to be familiar with the previous package design process. The new approach makes it easy to obtain the knowledge to implement the new methodology in a very easy to use, straightforward manner. The goal is to get the design attribute outputs from whatever EDA tool they currently use into Mentor's Calibre™ system. Once inside of Calibre, Mentor has plenty of high-density advanced packaging (HDAP) tools to ensure a complete and trustworthy verification. The next section provides more details on this partnership and the tools made available to Amkor's PADK users.

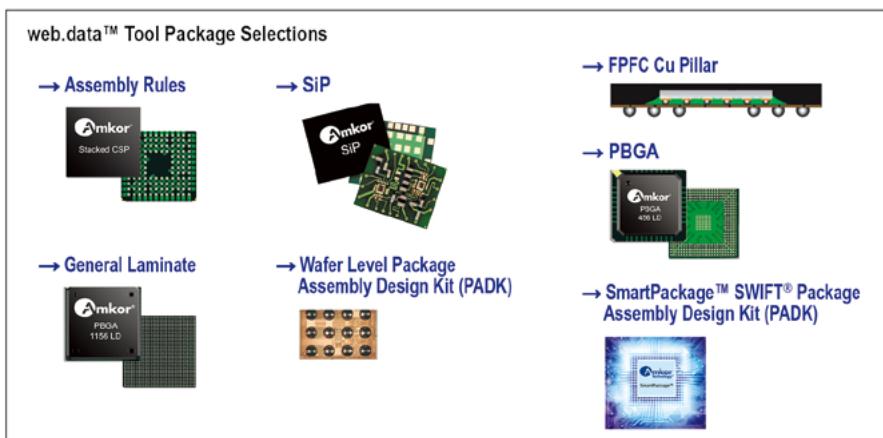
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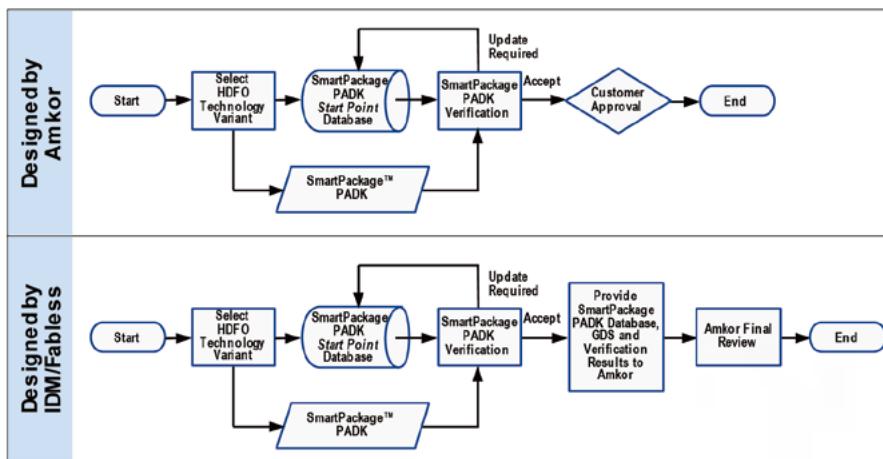
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**Figure 3:** User accessible documents in the SmartPackage PADK.



**Figure 4:** The PADK package verification process.

Once designed in the package design software, the customer exports the manufacturing outputs that are conditioned by the Start Point database and the outputs are verified in Calibre. Beyond traditional packaging items like trace/space and via sizes, the PADK will also check component spacing and perform many assembly and manufacturing checks, thereby building on the strengths of the package design software and making it a much more powerful instrument than just a traditional package design checking software tool.

For a new user to access the Amkor PADK, the user must request access via the Amkor Account Team. When a PADK is revised, customers that have access to the PADK will receive an update notification. After access is approved, the user sees a list of documents available to them as shown in **Figure 3**. By selecting the desired PADK, the user is presented with a nondisclosure agreement (NDA). Once the NDA is

accepted, the user can download the PADK. The SmartPackage PADK contains: 1) Design rules document; 2) Calibre rule deck; 3) Required configuration and instructional information; and 4) Start Point design database.

As shown in **Figure 4**, the Start Point database is a package design database that has been developed for customers to use on their HDFO designs. It allows them to “get up and running” after simply inputting a few minor details. The process is not quite the same as the traditional PDK or the traditional packaging approach, so awareness of these differences is important.

In traditional IC designs, designers have very little discretion. On the other hand, with laminate package design tools, designers have a lot of discretion. They are able to manipulate the design rules. The PADK is a process that can be used “on the fly” to bring the customer in-line with packaging assembly processes and prevent them from straying from approved rules.

## PADK and Mentor’s HDAP design process and tools

In 2018, Amkor and Mentor jointly announced the industry’s first partnership to support Mentor’s high-density advanced packaging (HDAP) design process and tools. Amkor’s SmartPackage PADK takes advantage of Mentor’s HDAP design process and industry-leading tools.

## Results from PADKs

One of the important user benefits of the PADK is that when it detects an error, the error is flagged as a design error. The PADK identifies the design rule, so the designer can refer to the SmartPackage design rules and see the violation or value discrepancy. This straightforward, intuitive process is receiving considerable interest from users and potential users. Surprisingly, they usually have all the tools – but this is an aspect of which they have not previously taken advantage. So, it takes training, knowledge transfer, and establishing trust in the packaging-level partnership to take this next step.

Some of the most commonly encountered verification issues that the PADK tool highlights include:

1. Component placement/floor planning issues;
2. Die-to-die spacing;
3. Capacitor-to-die spacing;
4. Feature-to-feature spacing; and
5. Feature size deviation.

**Figure 5** shows the type of error a user might encounter.

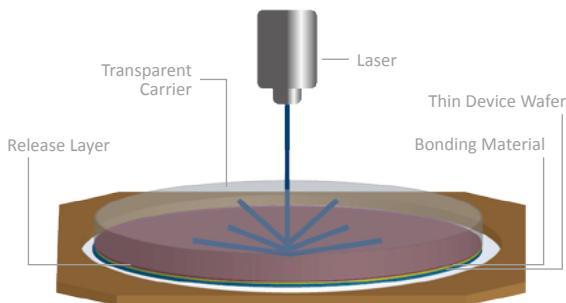
Using the new PADK, users have already demonstrated that an extreme cycle time reduction for HDFO packages is possible. A major time reduction occurs by reducing the iteration cycles between the user and the package supplier as shown in **Figure 2**. This reduction can be from days or even weeks, to only a few minutes. The process allows users to get to the desired state in their design, run their check, fix the errors and get back to designing again before they get too far into the design process only to realize they were headed in the wrong direction.

Because users can perform the verification in real-time in their facility, when the design is sent to Amkor, it will be easily accepted and can efficiently progress towards production.

# Creating Safe Environments

## Laser Release System

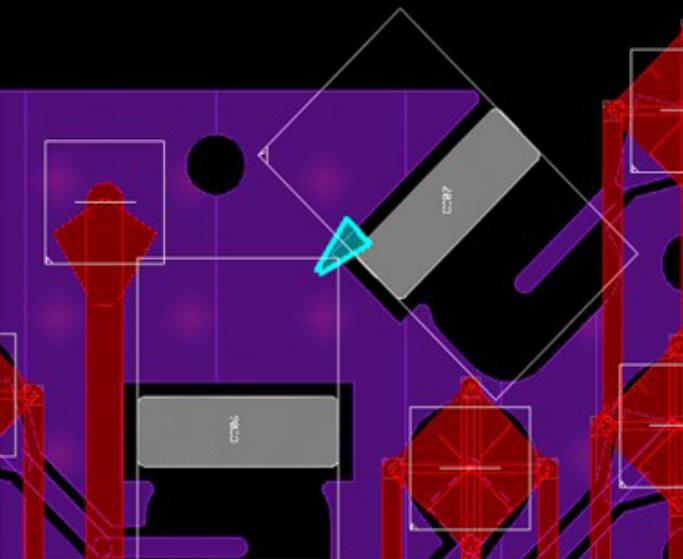
In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



### Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with: 308 nm 343 nm 355 nm



**Figure 5:** Example of a design rule check violation for component spacing.

By identifying and correcting the errors themselves, users have found the new process to be much more flexible than the old way because it allows them to: 1) prioritize revisions, 2) realize more of the goals they wanted to achieve in the design, and 3) better understand the intuition/methodology behind the rules. This educational process also helps them in future designs to avoid and resolve problems even faster.

### Towards faster time to market and more

IC designs tend to be very static, so the rules must be followed without deviation. In the packaging world, the situation is quite different because there are many different ways to achieve the same goals by modifying different rules and compensating for changes in other locations. To avoid problems from this “too flexible,” laissez-faire approach, the SmartPackage PADK moves toward the IC design methodology to stay within more stringent requirements for multi-layer packages.

For users, the PADK methodology leverages existing design tool capabilities by utilizing the investment they have already made and provides enhancements to simplify and speed up the design verification process for packaging. The results are early, rapid and accurate verification of advanced packages to significantly increase productivity, reduce cycle times and limit the number of design iterations.

### Acknowledgement

SmartPackage is a trademark of Amkor Technology, Inc.  
Calibre is a trademark of Mentor.

### Biographies

Ruben Fuentes is VP of Worldwide Design at Amkor Technology, Inc.; email [ruben.fuentes@amkor.com](mailto:ruben.fuentes@amkor.com)

August Miller is Director of Design at Amkor Technology, Inc.

Jonathan Micksch is Manager II of Design at Amkor Technology, Inc.

# INDUSTRY NEWS



## The fan-out panel option: where is the sweet spot?

Fan-out wafer-level packaging (FOWLP) has expanded to many applications in a variety of formats and structures. The FOWLP market can be divided into three segments: high-density round carrier, standard-density round carrier, and large-area panel. With continued price pressure for integrated circuit (IC) package assembly, FOWLP is no exception. This drive for a lower cost assembly method has driven the development of large-area panel processing. There are many challenges to panel-level fan-out production. Many of these challenges are being addressed in consortia activities. But where does the panel fit and what types of packages make sense for large-area panel production? This was one of the topics discussed in the panel session that concluded IWLP 2018 held in October in San Jose, California.

The panel discussion, entitled "What is the Sweet Spot for Large Area (Panel) Packaging?" was moderated by Jan Vardaman of TechSearch International



and Tanja Braun of Fraunhofer IZM. Panel members included Richard Bae from Samsung Electro-Mechanics (SEMCO), Tim Olson of Deca Technologies, Markus Leitgeb of AT&S, Thomas DeBonis of Intel, and John Hunt of ASE.

The panel opened with a discussion on the difference between the embedded die and FOWLP. AT&S indicated that all of its products are on panel. ASE considers fan out (FO) to be a form of embedded



die and offers its a-EASI using embedded power devices, SESUB, from its joint venture with TDK with embedded die in a laminate substrate, fan-out chip on substrate (FOCoS), and the Deca process joint venture with redistribution layer (RDL) for M-Series, as all examples of FO. Deca believes that design rules pushed close together are considered fan-out and larger body size devices need the panel approach to reduce cost. SEMCO pointed out that embedded die and fan-out panel-level packaging (FOPLP) are different technologies.

## Where do the companies stand?

Below is a summary of the various companies' positions on the panel topics.

SEMCO believes the definition of embedded die vs. FOPLP is determined by the use of a RDL. If RDL is used, then it is considered FO. The company started production of embedded passives and activities in 2010. For example, Galaxy Watch uses FO with the panel process. The application processor is placed next

to the PMIC, which is in the bottom package, using SEMCO's FOPLP process. Backside RDL on package thereby enables SEMCO to stack a standard memory, creating a package-on-package (PoP). In this example, RDL is used instead of packages such as molded core embedded package (MCeP) and substrate-like PCB (SLP). Intel started embedding capacitors and inductors a long time ago and noted that the use of RDL is what allows the package technology to be called FO. The difference is the L/S requirement: an L/S >15/15 could be considered embedded die, while a finer pitch of <15/15 would be described as FO.



The panel also responded to the question regarding major applications for panel FO (FO in general). Deca believes there are three classes of FO applications: 1) Single-die package, which is happening today: e.g., Infineon's eWLB is an early example still in volume production; 2) Multi-die system-in-package (SiP), and there are several such multi-die products. 3) Heterogeneous integration, greatest of all, has to use sub-1µm features. SEMCO noted that future 2020 DDR5 and GDDR6 power integrity and signal integrity will be driving new packages. Meanwhile, the memory package will need to deal with more power. Future applications include application processor plus memory.

According to AT&S, the RF market is a good candidate for panel FO, as well as multi-die packages and large body sizes. ASE noted that its first products with its M-Series FOWLP on a 300mm line will be PMIC and Audio CODEC, followed by RF. ASE has 300mm FOCoS



for 2µm feature RDL. The next versions of FOCoS will be for high-bandwidth memory (HBM) and logic.

For its part, Intel noted that it builds and sells final product. With larger products, they lose more space around the edge of

the die—such as when large product is within a SiP. It makes sense to integrate a big chip into a larger size panel.

The panel did not agree on an optimal panel size. Intel favors 510 x 515mm, others say 600mm x 600mm. ASE and Deca prefer 600mm x 600mm, but they did note that there is no reason to go to a panel option until 2020 when there is sufficient demand. It was noted that it is possible to cut the panel in four quarters and use 300mm tools. Meanwhile, SEMCO is looking at artificial intelligence (AI), servers, edge computing, etc., for panel applications. Edge computing may need large packages around >30mm, 50mm, or even 75mm.

The panel members agreed that yield is critical and that panel processes must have the same process yields as the round FOWLP process (i.e., 99.5% and above). One issue mentioned by ASE is that many panel tools are for PCB operations and designed for operation in a Class 10,000 clean room. The FO process on panel requires class 100 designed equipment. Handling is a concern because panels cannot be handled manually. SEMCO is in mass production with high yield.

For the last question—How many panel lines are needed and what packages will move into production next?—stay tuned for more answers during next year's IWLPC to be held again in San Jose, October 22-24, 2019.

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## Making TVs better – it's all about the package

By Cody Peterson *[Rohinni LLC]*

**T**oday's TVs and displays are dominated by liquid-crystal display (LCD) light-emitting diode (LED) technology, with the only existing competitor being organic LED (OLED) displays. All the major television and display companies are selling a vast amount of LCD-LED televisions.

Configuration of the LEDs in LED TVs can vary, as they can be in groups behind the panel or along the edge. The reality is that existing LED solutions face a number of prevailing challenges and disadvantages, and the way in which they are configured in a display has a major impact on performance. For example, most displays today mount LEDs at the edge of the display for backlighting, which enables the display to be thinner. However, because this is essentially a solid light plate, the liquid crystals aren't able to completely block the light within areas to produce images, which, in turn, washes out colors and turns blacks to gray. Next, when packaged LEDs are mounted behind the LCD to produce light, other negative effects result. The TVs become thicker because packaged LEDs are thick, and because packaged LEDs are so expensive, display makers can't afford to put thousands of them behind the TV. This allows slightly better blacks because these LEDs can be turned off in large zones within the TV.

Moving forward, OLED televisions have reached the consumer. With a dazzling, sleek display, OLED technology has proven to be a breakthrough for TVs. The organic films are located between semiconductors equipped with an electrical current. Extremely slim OLEDs illuminate themselves, allowing each pixel to be controlled to define an image. The ability to control displays at a single pixel level allows for the possibility of "total black." In this process, as different OLEDs are being switched on and off individually,

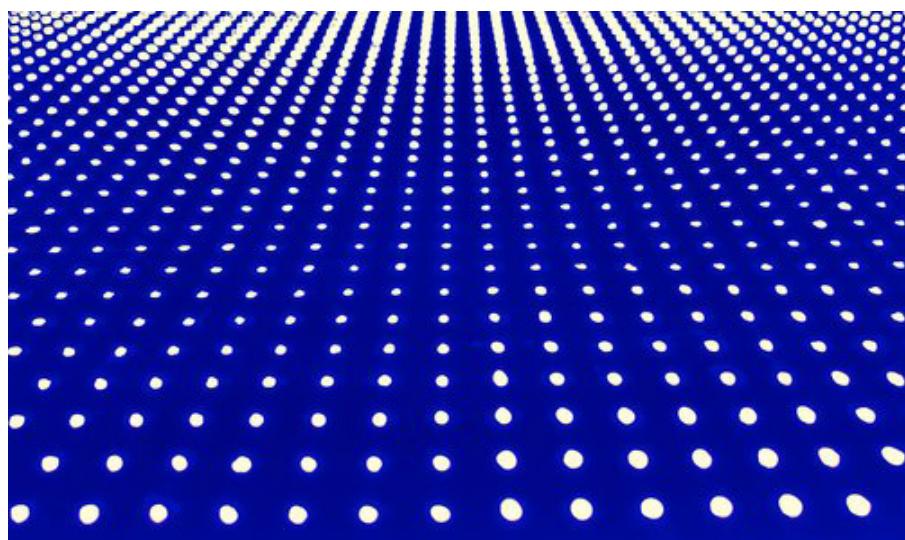
less power is used to generate a higher level of brightness.

These high-end televisions have their own drawbacks, as well – most notably, lack of brightness. Go into any electronics store, and you'll almost always see an OLED TV displaying a demo that contains small bright vivid images with a large amount of black areas. This highlights its advantages and hides its disadvantages. The brightness in OLED displays is basically throttled. You can have small areas that are extremely bright, but when you try to produce a large bright area (e.g., an explosion or a sunny day), that same amount of light is diffused over the entire surface. OLED makers play games with their specs that make it look as if they are as bright as LEDs, but they really aren't. There's a reason you don't see OLED spotlights – the fundamental technology just isn't capable of really high brightness.

A cutting-edge new technology is now stepping into the limelight, as microLEDs and miniLEDs are growing in popularity. MicroLED "packages" are essentially package-less—a fraction of the size of

the LEDs in average LCD displays. The microLED package is constructed of the substrate, electrode, microLED, and a thin film or glass. With an extremely thin LED package, the possibilities of slimming down consumer electronics and televisions are endless. MicroLEDs are paving the way to slimmer electronics against their LED/LCD and OLED counterparts.

Because the high-level technology is much smaller and thinner, and with the elimination of the expensive packaging, an enormous quantity of LEDs can be placed in a single display. For example, this means it's now possible to place more than 50,000 LEDs instead of today's highest performing displays, which utilize only up to 300-500 LEDs, at most. Moreover, the pitch between these microLEDs can be microns apart. MicroLEDs are not composed of an organic compound, so you don't have to worry about burn-in – a persistent problem with archaic plasma TVs and current OLED displays. Because they are capable of being applied to a variety of materials, it is possible to apply microLEDs to a variety of surfaces,



**Figure 1:** This microLED array illustration provides an example of what is possible using Rohinni's placement approach.



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including flexible substrates and curved displays. Also, microLEDs consume far less power because they run at a more optimal point on the efficiency curve, resulting in even longer life. Positive characteristics of this display are countless. For example, jaw-dropping differences in brightness compared to OLED, “true blacks” and LED control at a near pixel level, and improved high dynamic range (HDR) reproduction. There is one major issue, however: the manufacturing process for microLED displays has proven to be challenging and strenuous. Mass transfer of the LEDs is difficult due to a plethora of technological challenges associated with typical approaches, including equipment precision, first-pass transfer yield, time required, technology and equipment needed, methods of inspection, reworking failed/missing die, and the cost of processing.

Difficulties in the process of mass transfer of microLEDs are the primary reason for the absence of the technology in products currently on the market. To address this challenge, Rohinni has simplified the entire process and developed a complete solution to the issues facing mass transfer and product development. By revolutionizing the entire approach, fine-tuning equipment, mastering causes of die failure, thorough internal inspections, and managing costs of sample production, we were able to leap over the mass-production hurdle. Reinventing the pick-and-place process and holding incoming materials and robotics to a much higher standard has enabled achievement of placement speeds up to 10x faster and more accurate than any we believe currently exist. We have also developed a roadmap to realize placement of thousands of devices per second with the necessary placement accuracies to achieve Six Sigma yields.

Analysts looking at microLED mass production assess feasibility of true mass production based on Six Sigma. The current belief is that the yield of successful LEDs on a printed circuit board (PCB) is Four Sigma or greater. According to analysts, achieving commercialization with this level of success is feasible, with expenses in processing and repair. To reach a standard of “mature” commercialized products, the processing success must reach a level of Five Sigma

or greater. The transfer technology, assembly, high-quality materials, chip technology, and all other associated processes and materials are pushing the lighting industry to a new level.

The new approach described above has the potential to make traditional LED packaging (lamp-LED, SMD-LED, etc.) nearly obsolete, enabling new design possibilities sought out by several mass tech markets. The company’s manufacturing processes and equipment are well developed in their ability to precisely transfer microLEDs and semiconductors. Rapidly placing semiconductors with an extremely high first-pass yield will enable the lighting and other industries to realize significant changes and to bring new products to market more quickly.

Solving the manufacturing issue at a reduced cost of production in the microLED paradigm will challenge other incumbent technologies as well. This new process exceeds the brightness in current

lighting applications, conserves energy, and reduces deficiencies that currently exist in OLEDs and traditional LCD-LED displays. Pioneering product development using the technology is moving forward in other industries. Rohinni and keyboard maker Kaja jointly created Luumii, which produces thin, power-efficient keyboard backlighting. We have also just recently created a new joint venture with major automotive supplier Magna International that will bring lighting innovation to the global mobility market. Potential applications for this new approach to microLED abound – limited no longer by packaging, but only by the imagination.

## Biography

Cody Peterson has founded two successful startup companies, holds 60 patents, received multiple innovation awards, and is currently the founder and Chief Visionary Officer at Rohinni LLC; email [press@rohinni.com](mailto:press@rohinni.com)



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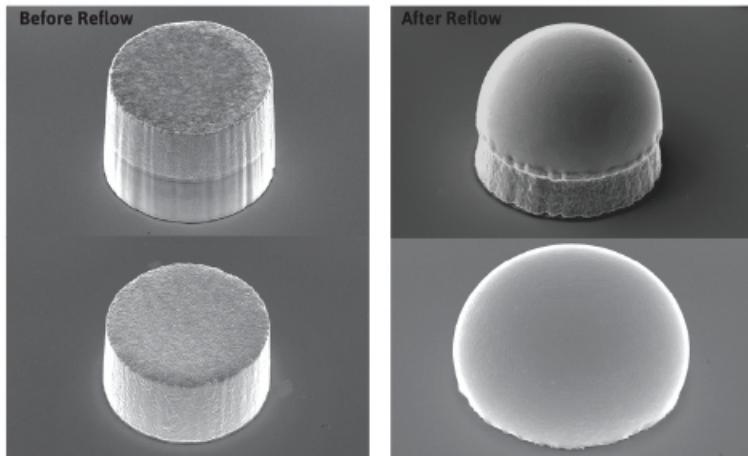
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