

# ChipScale

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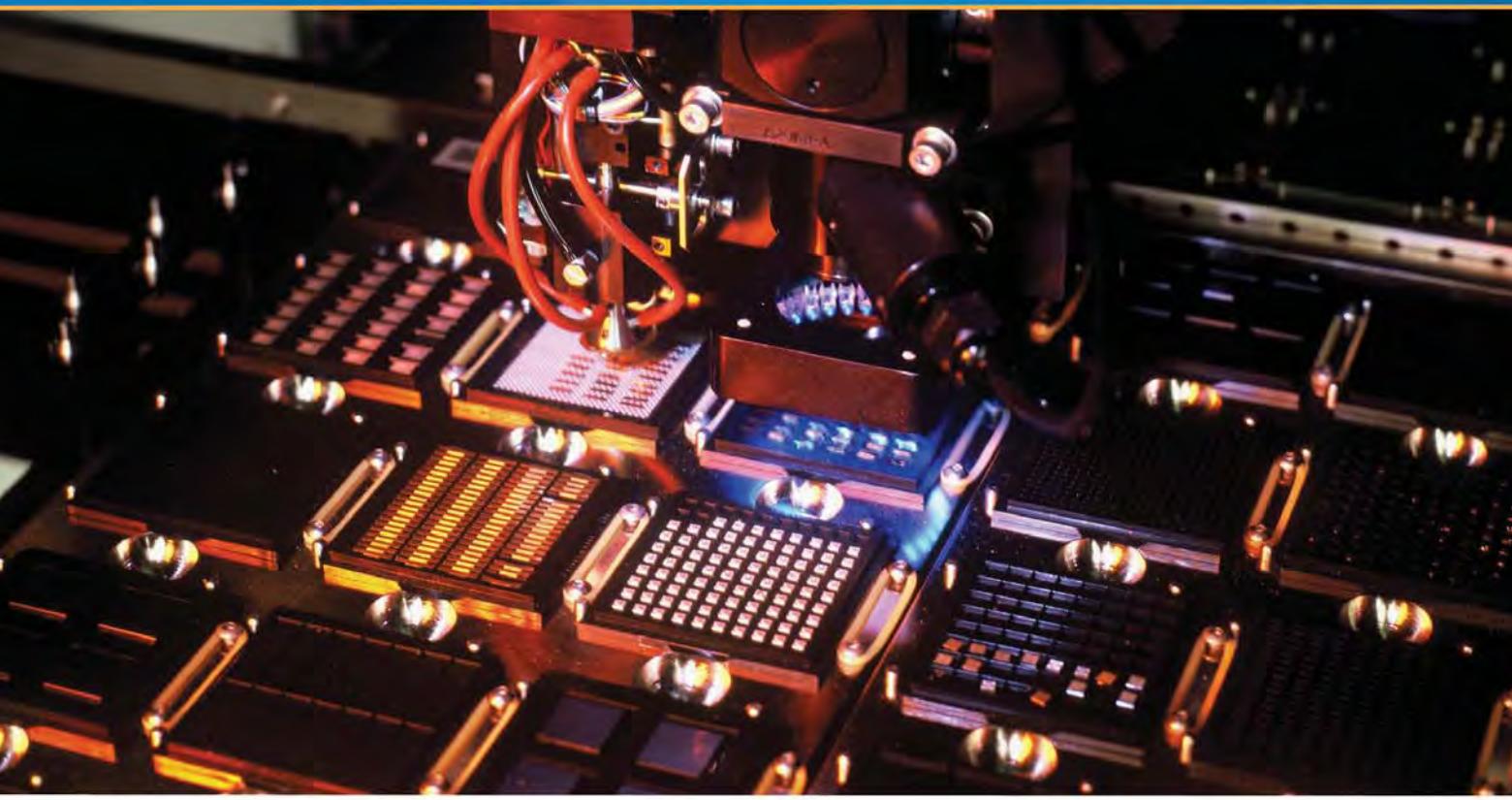
REVIEW®

*The International Magazine for the Semiconductor Packaging Industry*

Volume 15, Number 5

September - October 2011

- The Interconnect Challenge
- TSV Interposers & 3D IC Integration
- Advancements in Medical Electronics
- Design-for-Test for 2.5D & 3DICs
- X-Ray Inspection for Counterfeit ICs
- International Directory of Defect Inspection Systems



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Sept-Oct 2011  
Volume 15, Number 5



Sept Oct's cover image depicts this issue's content on xray inspection with the international directory of defect inspection systems. Bill Cardoso provides a cutting edge view of the technology behind Creative Electron in the article "X-Ray Inspection Techniques to Identify Counterfeit Electronic Components"

## Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging  
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,  
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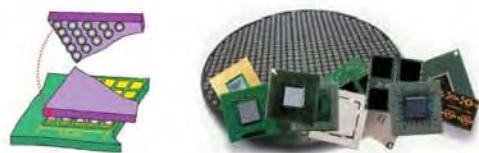
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6	H	
7	Rite Track	
8	Plasma-Therm	
9	Shinkawa	
10	HANMI Semiconductor	

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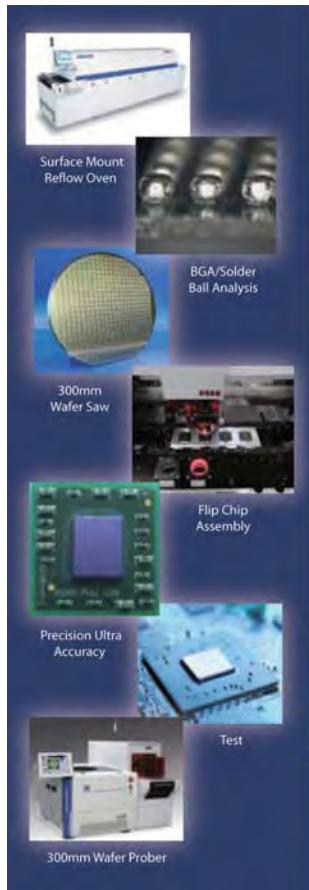
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# FROM THE PUBLISHER



## Recipe for Success

**W**e've always known we were on to something here at *Chip Scale Review*, what with devoting our coverage to semiconductor device packaging; but there's something very satisfying about seeing the rest of the industry come to the realization that packaging is a vital value-add rather than just a necessary evil, and therefore worthy of its own publication. And if the number of attendees, participants, sponsors and exhibitors registered for the 2011 International Wafer Level Packaging Conference is any indication, this message has finally been heard industry-wide, loud and clear. Position your company in the direction of next-generation advanced packaging and you can't go wrong.

At SEMICON West, I heard the term "contemporary packaging" used to refer to legacy IC packages technologies such as wire bond, QFNs and flip chip packages. These technologies currently satisfy 70% of the market because they fill the bill for low-cost, low-risk IC packages. But that appears to be changing as the growing smart phone, tablet and cloud computing market intensify the need for higher performance packages, even at an initially higher risk.

Srinivasa Sundararajan, packaging technology analyst for Oppenheimer, suggests that the technologies for manufacturing contemporary packages will soon be considered commodity techniques and while they'll likely retain a 50% market share, the highest margins will be realized by the tools, materials, and processes that serve the advanced packaging segment (WLP, SiP, and 3D), which he predicts is likely to grow at 20% CAGR. He says these companies or vendors should see growth through 2015 at least, because these advanced packaging technologies are enabling in nature, and without them, smart phones and tablets requiring small sizes and form factors wouldn't be possible.

As Tien Wu of ASE so succinctly put it during his keynote address at SEMICON West, it's time to explore the new dynamics of the semiconductor business. He said industry veterans look at the industry and wonder, why are we still here, and what can we do? How can we move forward? For the younger generation, the opportunity is ripe for diving into change; but where to begin? More than Moore has created an economic advantage for the back-end. The front-end sees this and wants a piece of that pie as well.

I take this all in, and wonder what it means for *Chip Scale Review*? We've focused on test, assembly and packaging since our beginnings; anticipating the time when it would be the most exciting place to play. But how do we keep our legacy readers and advertisers engaged, while also keeping our content cutting edge, and opening up opportunities for new readers and advertisers? Pleasing all palates requires a delicate balance of the key ingredients, and as our team has been putting together our 2012 Editorial Calendar, we think we've come up with a recipe that will appeal to everyone. Innovations in assembly, test, inspection, etc. of contemporary packages will always be a staple ingredient, accompanied by a healthy dollop of WLP, SiP, and 3D integration, and with the usual smattering of MEMS, and LED packaging for added spice. Bon Appetit!

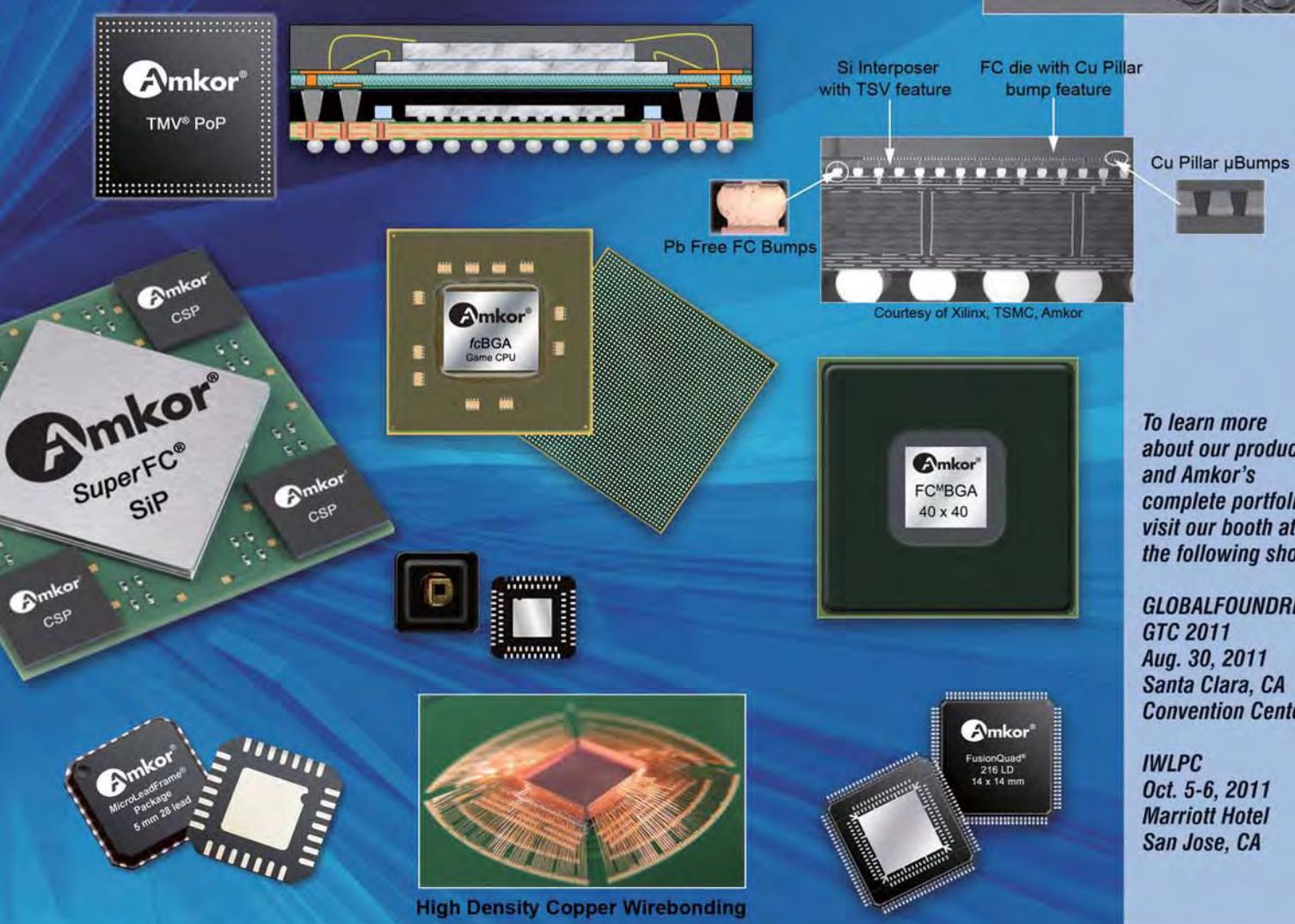
*Kim Newman*

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Image courtesy of Sematech

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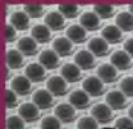


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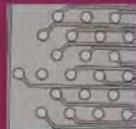


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# GUEST EDITORIAL

## Automobiles Remain a Hotbed for Semiconductor Market

By Brian Matas, [IC Insights]

In the classic 1964 movie Goldfinger, "Q" briefs James Bond, the suave agent 007, on the operation of his new specialized automobile:



*"You'll be using this Aston Martin DB5 with modifications. Now, pay attention please. Windscreen: bulletproof, as are the side and rear windows. Revolving number plates, naturally, valid in all countries...."*

*"Anything else?"*

*"You see this arm here? Now open the top and inside are your defense mechanism controls: smoke screen, oil slick, rear bulletproof screen, and left and right front-wing machine guns. Now this one I'm particularly keen about. You see the gear lever here? Now if you take the top off, you'll find a little red button. Whatever you do, don't touch it."*

*"Why not?"*

*"Because you'll release this section of the roof and engage and fire the passenger ejector seat."*

*"Ejector seat? You're joking."*

*"I never joke about my work, 007."*

At one time or another, many of us probably wanted to be James Bond and drive exotic automobiles with all sorts of gadgets and electronic wizardry. But, the fact is, today's "specialized" vehicles are equipped with enough sophisticated and practical electronic systems to make "Q" and the 1960s-era James Bond envious.

Without a doubt, the automobile market continues to be a hotbed for electronic systems and the advanced

semiconductors that power them. Consumer preferences for comfort and convenience along with government mandated safety and environmental regulations have caused automakers to increase the number and quality of electronics onboard new cars, which in turn, has resulted in a jump in semiconductor content. Factors contributing to this phenomenon include:

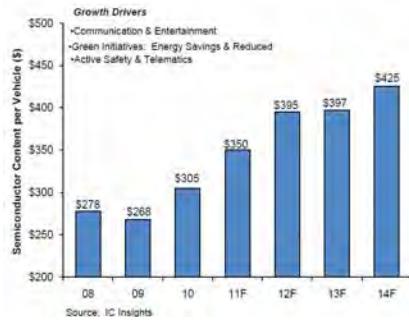
- **Comfort/Convenience**—Connectivity and onboard telematics are essential selling points for new-car shoppers who want to smoothly transition content from their media devices to their cars, home, or office. Bluetooth technology is now commonplace in cars, and Wi-Fi and center-stack displays that replicate the driver's smartphone screen, as well as onboard charging pads for phones and portable electronics will soon be standard.

- **Performance—Electronics** are used to optimize fuel consumption and engine performance, and improve vehicle traction control and stability. Electronics systems are typically cheaper, safer, and more reliable alternatives to hydraulic- and mechanical-based systems, resulting in fewer vehicle recalls, fewer hits on warranty, and ultimately, greater profit for automakers.

- **Ergonomics/Safety**—Airbags, anti-roll systems, lane departure and collision avoidance, automatic parallel parking, drowsy drivers detection, and emergency-calling systems are now marketing tools. Meanwhile, interiors are the next great frontier for design innovation. Comfortable seating; creative, functional, and tastefully

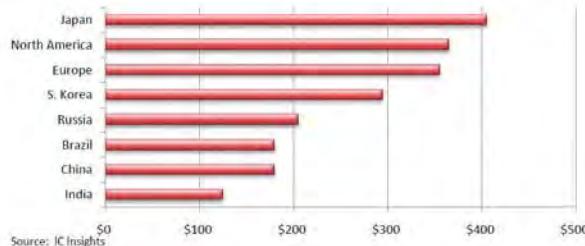
designed dashboards; and specific mood settings through lighting and aromas are being tested and will likely be another area where electronics and semiconductor content will be applied.

IC Insights believes the "trickle-down effect" of technology in cars is happening faster than originally expected. Sophisticated electronic systems, which were the exclusive domain of luxury-class vehicles a few years ago, have become more commonplace in mid-range and lower-priced automobiles. This has caused IC Insights to raise its forecast for average semiconductor content per automobile to \$350 for 2011, a 15% increase from the \$305 average in 2010 (see **Figure 1**). Semiconductor content per vehicle is



**Figure 1.** Average semiconductor content in automobiles from 2008 and forecasted to 2014 expected to average 9% annual growth through 2014, increasing to \$425 per vehicle at the end of the forecast period. The total automotive semiconductor market is forecast to increase 12% in 2011 as new car shipments are forecast to increase now that factories in Japan and supply chains throughout the world have mostly recovered from the devastating earthquake in Japan earlier this year.

Semiconductor content per vehicle varies based on factors such as the make and model of the car and the region of



**Figure 2.** 2011 Average Semiconductor Content per Car based on region in the world where it is sold. In 2011, the average semiconductor content per car is forecast to range from a high of \$405 in Japan to approximately \$350 in North America and Europe, to approximately \$150 in the BRIC (Brazil, Russia, India, China) region, as seen in **Figure 2**.

Automotive Applications-Specific Analog products (32%), Automotive Special Purpose Logic devices (13%), and 32-bit MCUs (14%) are forecast to be among the fastest-growing IC products in 2011. Analog products are used to gauge input functions like speed measurement and engine monitoring. Output functions such as power windows, adjusting power seats, controlling fuel injections, and ignition timing require D-A converters controllers and power IC drivers.

Mixed-signal logic ICs (analog and digital functions on the same chip) are used in tire pressure monitoring systems (TPMSs) and electronic stability control (ESC) systems—two of the latest safety systems that will be required for new cars sold in Japan, North America, and Europe. In Europe, tire-pressure systems will be required on all new cars sold after November 1, 2011, and stability control systems will be required on all new cars sold in the U.S. starting in 2012. These mandated systems will boost the need for various sensors, analog, and mixed-signal devices that will be needed to interpret the information for the driver.

In the important automotive market segment, 32-bit processing in MCUs is driven by the advent of “intelligent” car designs and increases in sophisticated, real-time sensor functions for government-mandated safety and crash-

avoidance systems. In the next few years, complex 32-bit MCUs are expected to account for over 25% of the processing power in vehicles. MCUs with 32-bit processing cores are typically found in driver information systems, enhanced safety features, and engine control units that optimize real-time performance.

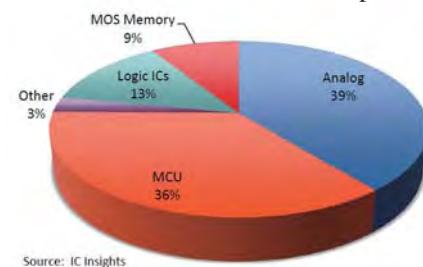
Overall, the use of microcontrollers in cars is also expected to substantially increase as more drivers turn to electric and hybrid-electric vehicles (HEVs). Hybrid vehicles use 32-bit MCUs to monitor the need to switch between gasoline engines and electric motors in HEVs. This often requires complex software and 32-bit processing as well as large amounts of on-chip memory and more I/O functions. More than a dozen MCUs are used to supervise electrical-power boosting and battery-storage systems inside electric and hybrid vehicles.

In today’s models of high-end cars, up to 100 microcontrollers (8-, 16-, and 32-bit devices) are used throughout the vehicle. This is more than six times the number of MCUs used in luxury automobiles in the 1990s. A growing number of luxury automobiles and high-end sports utility vehicles (SUVs) are offering automated “self-parking” options, which use dozens of sensors, controllers, and actuators that exist in other automotive systems (such as antilock brakes, electronic steering, and collision avoidance). In the case of Toyota’s Lexus LS460 sedan, the car’s Advanced Parking Guidance Computer communicates with 45 to 60 other microcontrollers and embedded computer systems attached to a 1Mb/s control area network (CAN) bus. Ford offers an ultrasonic sensor-based Active Park Assist option in its Lincoln MKS sedans and MKT luxury “crossover” utility vehicles as well as the Escape SUV series. BMW, Volkswagen,

and others are also designing park-assist and self-park features into their vehicles. Meanwhile, a growing number of automakers are hoping to expand on concepts used in early self-parking options, advanced cruise controls, and collision-avoidance systems to develop “smart” autonomous (driverless) vehicles over the next 10 years.

Analog ICs and microcontrollers are forecast to account for the bulk of the automotive IC market in 2011, with logic and memory ICs accounting for most of the remaining dollars (**Figure 3**).

The convergence of on-board technologies that help navigate, calculate, and communicate important



**Figure 3.** 2011 Automotive IC Market by Device Type (Fest, \$18.6B)

information to the driver will be a key factor in consumers’ decision to purchase a new car. Consumers have come to expect certain safety features, are more aware of the impact of their car on the environment, and have become dependent on being always connected to their social networks and the Internet. More often, consumers will reject products—including the cars they drive—that do not match or enable their lifestyle.

With the help of sophisticated electronics, automobiles have become more efficient, cleaner burning, and packed with more safety systems than ever before. This will keep the automotive IC market an active and vibrant market for semiconductors for the foreseeable future. 

*Brian Matas, VP, Market Research, IC Insights, can be reached at bmatas@icinsights.com*

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# INDUSTRY NEWS

## NEXX Systems Celebrates 10 Years of Yankee Ingenuity

By Francoise von Trapp, Sr. Technical Editor

**A**ugust marked the 10th Anniversary of NEXX Systems, manufacturers of semiconductor equipment designed expressly for wafer level packaging processing (WLP). The company, headquartered in Billerica MA, celebrated the milestone with a company-wide barbecue that honored founder and former CEO Dick Post, and was attended by local dignitaries, friends and family of Post, suppliers, customers, and collaborative partners.



Friends, colleagues, suppliers and customers gather to celebrate NEXX's 10th Anniversary

Rezwan Lateef, VP of Business Development, and Tom Walsh, CEO each addressed the guests, talking about the company's accomplishments and future goals, and presenting Post with the gift of a star named after him to acknowledge his vision and continued guidance.

Also a founding member of the company, Lateef recalled the day the company was first established with 20 original employees, to the global organization it has now become with 142 full time employees, 36 based outside the US, and 140 systems installed at 40 companies. According to Walsh, the recent opening of the China office was part of a continuing strategy to building local infrastructure globally, hiring direct sales personnel, and service and process engineers. Walsh explained that this is particularly important in Asia and NEXX has already opened offices



Dick Post, NEXX founder, and Arthur Kiegler, CTO, talk about the early days

in Taiwan and Singapore. He said the office in China posed a particular challenge and should be considered a major accomplishment navigating all the government regulations. In addition to addressing the company's accomplishments, various speakers reminisced about working alongside Dick Post, and acknowledging his vision for this company, including Arthur Kiegler, CTO and inventor of the company's flagship, Stratus electroplating system.

Post himself humbly credited the company's success thus far to the hiring of "smart people". "You have to find the people who can do more than you can do. Every hire must raise the average," he noted. One of those hires was his own successor. Walsh joined the company in 2009, hand-picked by Post to take the company to its next phase of growth. "It's hard to find someone who can take over and pretty seamlessly run this thing on up to the next level. I guarantee you I can't do what he's doing. He gets to have the thrill of a Wall Street adventure," he said.

### What's Next for NEXX

Walsh says he's seen NEXX grow from a company focused on developing a process to one that is more customer-driven in terms of emphasis, although its entrepreneurial

spirit remains the foundation of what it is today.

Robert Jackson, who joined NEXX as VP and general manager of electrodeposition systems 10 months ago, concurs with Walsh on NEXX's next steps, and Walsh's capability to guide them there. "What brought me to NEXX was the opportunity to work with Tom Walsh again, move into an area of semiconductor plating with an emerging company in the packaging space," he explained. "In the semiconductor industry, the packaging space is growing much faster than the front-end, and the chance to take an emerging technology and go through the process again within a growth industry was a really exciting opportunity."

### Targeting the Wafer Level Market

What differentiates NEXX most from its competitors, notes Walsh, is that its products are designed specifically for the wafer level packaging environment Jackson speaks of. Both the Stratus ECD and Apollo PVD systems have unique architectures designed for flexibility and high productivity.

Walsh says that older wire bond packages are transitioning to flip chip technologies, and that the wireless explosion over the next 5-10 years will result in a huge growth rates on those products.

Commenting on packaging technologies in general, Srinivas Sundararajan, packaging technology analyst for Oppenheimer, says advanced packaging is one of the few areas of technology that is likely to grow at 20% plus CAGR, notes Sundararajan. "Companies or vendors that specialize in tools that deal with next-generation advanced packaging markets are likely to see growth through 2015 at least",



Rezwan Lateef, presents Post with the certificate for his star, while Tom Walsh, CEO gives the star's coordinates

he said, emphasizing that advanced packaging technologies are “enabling” in nature. His viewpoint is that without the enabling technologies, devices such as smart phones and tablets that require small sizes and form factors just would not be possible or conveniently sized or priced.

### **Collaboration with SEMATECH**

Walsh also recognizes the importance of R&D. “As CEO, I realize that R&D is what fuels our engine. It is fundamental to our strategy which is why we invest 17% of gross sales annual to continued R&D,” he stated, adding that since NEXX is still small, it’s necessary to reach out and develop collaborative efforts both in joint development projects with leading customers, and with leading advanced packaging research centers, such as they have with IBM and SEMATECH.

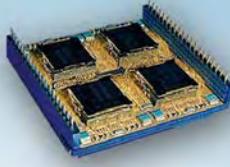
NEXX Systems collaborates with SEMATECH on innovative electrodeposition technology in the area of advanced wafer-level packaging items. According to Sitaram Arkalgud, director of SEMATECH’s 3D program, the collaboration with NEXX has involved developing cost-effective through silicon via plating solutions for member companies. He explained that each member company has considerable input during all aspects of the tool selection, evaluation and process development phases, and that the resulting technology is transferred back to those participating members – in this case, those in the 3D program. He says that the unique, modular

architecture of the Stratus was an important factor in the tool selection, since it provides SEMATECH with considerable flexibility, as well as permitting high throughput and a low cost-of-ownership in high volume manufacturing.

Walsh is excited about NEXX’s next

10 years and says the industry should expect to see some exciting new product introductions in 2012. His intention is to continue exacting on the vision Post had when he started NEXX, and to build on what began with “good old-fashioned Yankee ingenuity, smart people, and hard work.”

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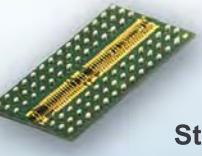
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## NANIUM and Georgia Tech Collaborate on Chip-last Commercialization

NANIUM, Europe's largest outsource semiconductor assembly and test (OSAT) provider, has become a Supply Chain Member of the 3D Systems Packaging Research Center at the Georgia Institute of Technology (GT PRC) Embedded MEMS, Actives and Passives (EMAP) Industry Research Consortium. As such, NANIUM will serve as package integrator for the new technology.

The agreement is the foundation of the partnership, and the co-operation between the GT PRC and NANIUM is an example of the increase in global industry collaborations for GT PRC, providing a path for commercialization of System-on-Package (SOP) based technologies.

The incorporation of the EMAP Chip-Last embedding advancements will allow the extension of NANIUM's fan-out technology portfolio to SiP solutions for new applications and markets, including Interposers.

## GLOBALFOUNDRIES and Amkor to Collaborate on Advanced Assembly and Test Solutions

GLOBALFOUNDRIES and Amkor Technology, Inc. have entered into a strategic partnership to co-develop and commercialize integrated fab-bump-probe-assembly-test solutions. Through the partnership, Amkor would become a founding member of GLOBALFOUNDRIES' Global Alliance for Advanced Assembly Solutions, designed to accelerate innovation in semiconductor interconnect, assembly and packaging technologies.

By joining forces, the companies say they plan to extend the ecosystem to address growing market needs, while bolstering their ability to deliver end-to-end solutions for customers at advanced technology nodes. Additionally, the companies have amended an existing license agreement to expand their lead-

free wafer bump licensing relationship.

As the industry moves aggressively to more advanced technology nodes, innovation in interconnect, assembly and packaging solutions is becoming increasingly important. Supply chain management has become a critical topic. The partnership between GLOBALFOUNDRIES and Amkor is expected to enable the supply chain to better meet these diverse requirements and deliver robust and reliable solutions to mutual customers.

## Assembleon Enters the Semiconductor Market

Assembleon, tool manufacturer for the surface mount industry, has entered the semiconductor back-end market with the launch of its A-Series Hybrid, a single tool used for high speed, high accurate die placement and bonding. High parallel placement technology targets System-in-Package (SiP) and Multi Chip Module (MCM) manufacturing as well as flip chip bonding.

According to Patrick Huberts, program manager for the A-Series Hybrid, different pieces of equipment are currently used in the industry to place chips and known good dies (KGD) for manufacturing SiP, MCM and high performance flip chip modules. Assembleon's solution puts all the processes on a single machine, for reduced production and investment costs, explains Huberts.

Tool features include programmable force control, a fluxer dip station and high accuracy cameras. The tool can reportedly bond flip chips at a repeatability of 10µm while placing at a record speed of 2,500 components per hour (cph) per single placement head. Die bonding speeds are 3,500cph per head at 25µm. The company claims that this first-of-its kind tool achieves 99.99% yields, avoids the risk of cracked components, and eliminates waste, rework and defective end products.

## NxGen Electronics Names Tri Le President

NxGen Electronics, provider of microelectronic packaging solutions and product innovations, has appointed Tri Le as president. Tri has managed engineering and operations teams at NxGen for the past 6 years, promoting a customer focused

strategy within the company, leading NxGen to engage in collaborative affiliations with customers to create and commercialize NxGen's IP.

"Tri has expertise in building and leading teams through complex development programs that require coordination of marketing and business development, and (the electrical, mechanical and software) engineering services we offer", said Chairman and CEO, Art Fillmore.

Prior to joining NxGen, Tri served as an Optoelectronic Packaging engineer at Peregrine Semiconductor, a startup company specializing in RF CMOS solutions. He also previously held technical positions at TRW (now Northrop Grumman). Tri holds a Bachelor in Engineering and an Executive MBA from Anderson School of Management at UCLA specializing in Entrepreneurship.

## Dennis P. McGuirk Named President and CEO of SEMI

SEMI has appointed Dennis "Denny" P. McGuirk as president and CEO, effective November 14, 2011. McGuirk succeeds Stanley T. Myers, who led SEMI for the past 15 years and has served on its board of



# The Interconnect Challenge

By Scott Jewler, [\[Powertech Technology, Inc.\]](#)

**T**hose of us in the semiconductor industry, as well as the rest of the world's population as a whole have come to expect nearly magical increases in the computing, communication, and entertainment capability of the electronic devices we use at short and regular intervals. Powered by the practical application of Moore's law and the endless imagination of engineers, designers, and product managers, in one generation we've seen the novelty of a personal computer booting up on an eight inch operating disk and running a user-written Fortran program transformed into ubiquitous mobile phones, smart phones, tablets and other computing devices that touch the lives of over a quarter of the population of the planet in a meaningful way.

Those of us working in packaging and assembly can take some pride in our contribution to this incredible pace of advancement. Technologies such as plastic encapsulation, surface mount technology, area array packaging, 'chip scale' packaging, die and packaging stacking and related technologies all helped enable silicon functionality into smaller end products.

In terms of first-level interconnect between devices, however, the contribution of back-end technology has been less transformative. We developed aluminum, then gold, then copper wire bonding technology. We developed solder bump flip chip and transferred it to mainstream high volume nearly 30 years later.

## Mapping the Industry

As we look towards mapping the future needs of the electronics industry, and how interconnect must evolve to enable the industry to continue delivering the level of innovation now expected by the market, some guiding assumptions are clear. Planer scaling of transistors, the fundamental driver

of the last 50 years of semiconductor advancement, is getting more expensive both in terms of fabrication and design costs. Practically, this means fewer high-volume device types will be able to take advantage of smaller fabrication geometries. With multiple low-power processing cores, the next generation of high-performance logic devices will no doubt be able to calculate, process, and manage incredible amounts of data. This puts the next generations of incredible user experiences tantalizingly close at hand. The challenge for interconnect technology is how to get all these data and signals out of these super chips and turn them into something we analog humans can use to communicate, calculate, or entertain ourselves. This is the interconnect challenge.

## The Interconnect Technologies

Several new interconnect technologies are gradually entering the market to address these challenges. Disruptive to the existing infrastructure and semiconductor packaging supply chain, many conflicting points of view and predictions about the future of these new interconnection technologies are seen in trade media, conferences, and commercial discussions.

Copper pillar bumping is the first of this next generation of interconnect technologies to reach high volume manufacturing (HVM) ([Figure 1](#)). Although limited now to a few CPU and application processor applications,

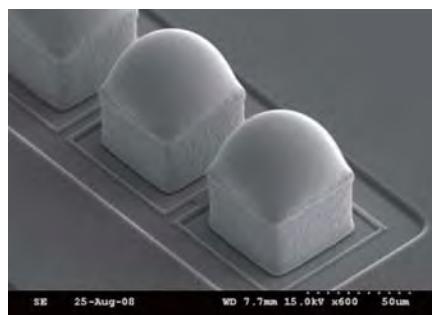


Figure 1. Copper Pillar Bump

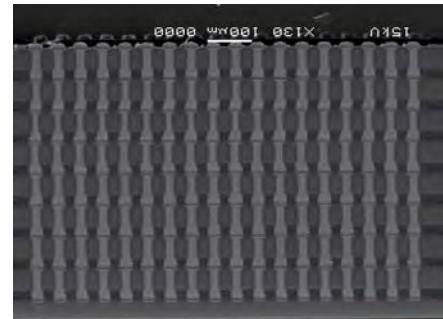


Figure 2. Through Silicon Vias  
copper pillars are a critical technology for higher interconnect densities and faster data communications speeds.

Through silicon via (TSV) is the next interconnect technology to move to volume production ([Figure 2](#)). Used in image sensors today to provide efficient interconnect between sensor and driver, TSV as an interconnect technology that is still generating more papers and articles than live applications. Like the ball grid array (BGA) in the late '90's, this situation could change in a short period of time.

Micro bumps using copper pillars and TSV are key enablers for another emerging new interconnect technology, silicon interposer integration. Silicon interposers (sometimes inscrutably referred to as 2.5D), enable fine-pitch high-speed connections between independent chips ([Figure 3](#)). They can also be used to fan out high density connections from the scale and pitch of a chip to the geometry that can be cost effectively managed at board level assembly.

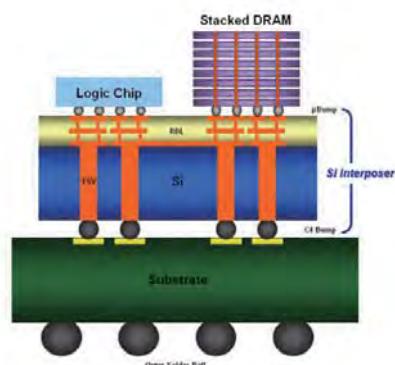


Figure 3. Silicon Interposer

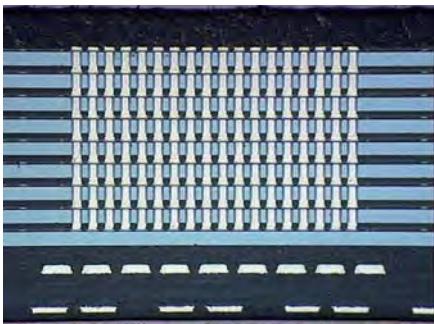


Figure 4. 3DIC

The emerging technology being most hotly debated is stacking of active die using TSV and micro bump interconnect technology (**Figure 4**). Widely referred to as 3DIC (a name that has created significant confusion with other vertical technologies including FinFET transistors, stacked transistors, conventional stacked IC's with wirebond and flip chip interconnect, and stacked packages with solder interconnect), stacking of active devices using TSV interconnect offers the possibility of incredibly dense functional integration while generating a host of technical and commercial concerns and debate.

### Micro Interconnect with Copper Pillar Bumps

In addition to improved thermal and electrical performance, copper pillar bumps provide higher standoff and better coplanarity than solder bumps as pad pitches decrease. These attributes in turn allow for substrates with smaller capture pads, freeing up routing channels and reducing substrate fabrication costs.

Design and package selection for a host of new products are taking advantage of these features to improve performance while reducing costs over prior solutions. In logic ICs, both perimeter and area array design using copper pillars can offer advantages. With current capabilities of bumping and flip chip bonding supporting bump pitches down to 40 to 50 $\mu\text{m}$ , perimeter pad layouts can access the electrical performance and space savings of flip chip over conventional wire bond without driving up substrate costs significantly. Area array designs from around 90 to 150 $\mu\text{m}$  can similarly utilize copper pillars instead of

traditional solder bumps to achieve higher assembly yields with lower cost substrates. Graphic and DDR3 DRAM are beginning to convert to this technology as well. By optimizing designs around substrate manufacturing capability and chip placement flip chip equipment accuracy; improved electrical performance over wire bonding can be achieved without significantly impacting manufacturing cost.

Controlled standoff, fine pitch, and excellent thermal and electrical performance make copper pillars the interconnect technology of choice for the emerging micro interconnect requirements for active and passive device stacking combined with TSV.

### Through Silicon Via

With market applications currently limited primarily to CMOS image sensors, TSV certainly qualifies as the most talked about and potentially transformative new interconnect technology in the industry. Numerous methodologies to form, insulate, and metalize vias through silicon are being developed and demonstrated. Slowly but surely questions about via geometry, keep-out zones, cost, and reliability are being answered.

TSVs can be formed in silicon substrates with only passive metal interconnect creating silicon interposers. They can also be created in active integrated circuit devices to create very short and electrically efficient interconnect between devices stacked vertically.

In via-middle technology, vias are generally formed in the front-end fab middle-of-line or contact metallization process. These vias are later exposed through back-side wafer thinning in what is typically thought of as back-end or assembly middle-of-line. The vias must be exposed without contaminating the surrounding silicon area with copper. Once exposed, they must be prepared to accept bumps for interconnect to other devices or interposers.

In via-last technology, full thickness wafers are typically shipped from the front end wafer fab. After front side bumping and attachment to a support

system, the wafers are thinned and vias formed from the backside. Similar to the via-middle process, the exposed vias are then bumped to prepare for interconnect to other devices or interposers.

### Silicon Interposers

Silicon interposers typically included multiple layers of metal routing, TSVs, and top and bottom side bumping. They have multiple uses including fanning out ball pitch of high-pin-count smaller devices to match substrate manufacturing technology and providing high-speed interconnect between processors and memory or other logic chips for network and computing applications.

Although there are some potential applications for Si interposers with greater than 10 $\mu\text{m}$  metal line widths, the majority of new applications appear to require 2-3 layers of 2-3 $\mu\text{m}$  lines in a non-organic insulator. To complete an interposer, TSV and top and bottom side bumping must also be completed.

For this reason the silicon interposer supply chain is still emerging. The metallization process is commonly found in wafer fabs however most of these facilities do not provide via-last or bumping capability. OSAT bumping houses may have the bumping or even TSV formation capability, but probably lack the fine-pitch Cu damascene processes required to create multiple layers of fine-pitch metallization.

Although a few exceptions may exist, the initial production of Si interposers will likely be most economical through collaboration between front-end and back-end service providers.

### 3DIC

Stacking ICs using wirebond or a combination of FC and wirebond has been widely practised for over 10 years. In today's most common communication and computing devices, stacks of 4 – 8 die with individual die thicknesses of less than 50 $\mu\text{m}$  are in very wide usage. Die sorting and assembly technology advancements have enabled these memory stacks to yield finished parts at extremely high yield, making them not only excellent performing but cost-

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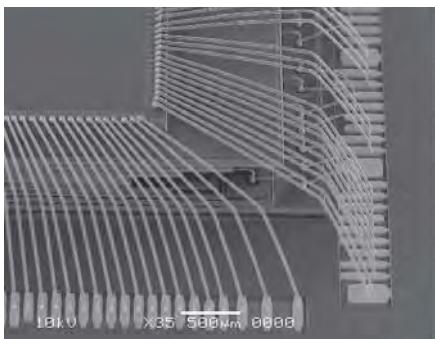


Figure 5. Common 9 die stack memory



Figure 6. Groundbreaking and construction of PTI's new 750,000 Sq Ft. Copper Bump and TSV Facility in Hsinchu

effective solutions.

Many arguments against 3DICs are overcome by taking as an example a homogeneous stack of memory IC similar to **Figure 5**. Using probable good die (PGD), thin die handling, cumulative yield loss, and the supply chain model are similar between wire bond and 3DIC solutions.

The big questions are cost and yield of the TSV interconnect technology. When considering TSV cost, it's helpful to recognize that unlike traditional package assembly, where material costs that are fully variable with volume constitute over 50% of the total assembly cost, in TSV, fixed assets in the form of PVD, DRIE, ECD, and other tools will form the major

portion of cost. Given that, the path to low cost-of-ownership on these types of tools is higher throughput; the key to driving cost of TSV will be volume. Small players testing the waters will not be competitive with those who invest in volume manufacturing.

## Conclusions

While packaging has delivered many innovative solutions to improve silicon function density over the years, the cost of continuing the path of Moore's Law creates new and compelling challenges. Among them, core packaging technologies have seen limited advances in first-level interconnect technology.

Copper pillar bumps, TSV, silicon interposers, and 3D IC technologies are entering the market and will be critical to meet the future needs of the industry. Memory devices will be among the first device types to take advantage of these new interconnect technologies. With high volumes and fast ramp cycles, these applications will be able to quickly drive scale and manufacturing efficiency leading to competitive costs and yields. Other applications will surely follow. ☀

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# Automated Design-for-Test for 2.5D and 3D SICs

By Erik Jan Marinissen, Mario Konijnenburg, [IMEC], Sergej Deutsch, Brion Keller, Vivek Chickermane, Subhasish Mukherjee, [Cadence Design Systems], Sandeep K. Goel, [TSMC]

**W**ith the advent of 2.5D and 3D stacked ICs (SICs) based on through silicon vias (TSVs), it is imperative to prepare for testing such products for manufacturing defects. The main test challenges for SICs are related to test flows, test contents, and test access.

## Test Flows

SICs offer many stages to perform manufacturing test than conventional chips, which typically are only subject to one wafer test ('e-sort') and one packaged test ('final test'). For SICs, we distinguish:

- Pre-bond test: before stacking, on either original thick wafers and/or on thinned-down wafers.
- Mid-bond test: during the stacking process, i.e., when a partial stack is formed.
- Post-bond test: when the stack is complete.
- Final test: after packaging the complete stack.

The challenge is to optimize the test flow as an integral part of the overall manufacturing flow to keep production costs as low as possible. This requires cost modeling of parameters such as wafer cost, die size, die yield, stacking process (D2W or W2W), stacking yield, test coverage, test cost, and package cost. Modeling results show that more testing will increase the test cost, but typically reduce the overall production costs.<sup>1</sup> Also, a cost-optimal test flow typically evolves over time, as production processes mature and yields increase, which in return requires flexible adaptation of the test flow.

## Test Contents

The dies being stacked are built with regular process technologies, suffer from all conventional (CMOS, DRAM) defects, and hence require all well-known tests: stuck-at faults,

transition faults, delay faults, very-low voltage tests, leakage currents, etc. 3D processing steps, such as wafer thinning, effect device performance, but so far no fault effects are identified that are not already covered by conventional test suites. The only structures that require our attention with respect to test pattern generation are the new TSV-based interconnects. The possibilities for testing TSVs prior to stacking are limited, and at that stage the actual interconnect (typically in the form of micro-bumps on top of the TSVs) has not been formed yet. Hence, the TSV-based interconnects are best tested as part of a mid- or post-bond test. They require a dedicated interconnect fault model and corresponding automatic test pattern generation (ATPG) engine.

## Test Access

SICs present various challenges related to test access, such as the ability to pump in test stimuli and pump out test responses from the die-/stack-under-test. For performing pre-bond tests, all non-bottom dies of the stack only have "TSV I/Os"; these small micro-bumps come in pitches much smaller and array sizes much larger than what can be handled by today's conventional probe technology. The probe industry is working hard to enable probing on fine-pitch micro-bumps, with JEDEC's upcoming Wide I/O Specification (JEDEC 42.6) for stacked mobile DRAMs as a first major target.<sup>2</sup> However, until this fine-pitch probe technology is proven mature, chip makers are putting additional dedicated probe pads on their non-bottom dies to enable pre-bond testing.

Another challenge is posed by stack-internal test access. After stacking, test access from the test equipment (either through probing or, after packaging, via a test socket)

is through the external I/Os of the SIC product, which are located in the bottom of the package; these signals must travel through the bottom die. Design-for-test (DfT) circuitry is required in all the dies comprising the stack to propagate test instructions and data up and down through the stack. Testing the TSV-based interconnects between two adjacent dies requires DfT that provides controllability and observability on both ends of the interconnect. To get test data higher up in the stack, DfT in the dies below it needs to propagate test stimuli coming from the test equipment upward in the stack, and, vice versa, test responses downward.

## 3D-DfT Architecture

IMEC has developed a 3D-DfT architecture that meets the above requirements.<sup>3,4</sup> It enables a modular test approach, in which dies, their embedded IP cores (if any), and TSV-based interconnect layers can be tested as stand-alone units. This modular test approach allows for test contents to be tailored to the manufacturing processes of various dies and provides yield monitoring and first-order diagnosis per module. Furthermore, it enables flexible

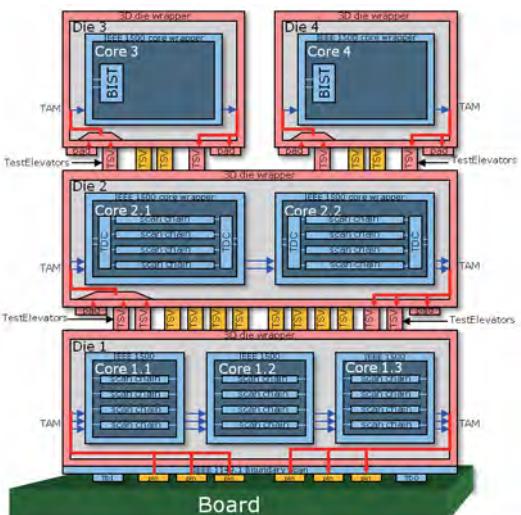
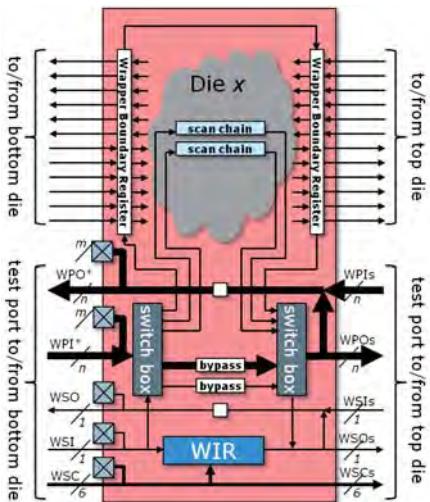


Figure 1. Overview of the 3D-DfT architecture based on die-level wrappers



**Figure 2.** Schematic implementation of the 3D-DfT die wrapper inclusion, exclusion, and various module test scheduling to support multiple test flows and their cost-improved updates as manufacturing yields mature over time.

The main component of the 3D-DfT architecture is a die-level wrapper. The wrapper adds specific 3D-DfT, on top of the existing conventional DfT in the die itself (**Figure 1**). The 3D-DfT wrapper builds on and extends well-known DfT standards such as IEEE Std 1149.1 (for board-level interconnect testing) and IEEE Std 1500 (for embedded IP cores). Each wrapper has a well-specified test interface at its bottom side, consisting of a serial interface for test instructions and test data, and an optional parallel interface (of scalable width) for (high bandwidth) test data. On the top side of the die, a mirror-copy of that test interface exists for each other die that will be stacked directly on top of it. In other words, for a top die, no such top test interface will exist; for a middle die in a single-tower stack, exactly one such top test interface will exist; and for a base die in a multi-tower stack, multiple top test interfaces will exist, one for each tower.

Serial (one-bit) and Parallel (n-bit) Test Access Mechanisms (TAMs) comprise the test interfaces. The Serial TAM handles both test mode instructions and serialized test data. The optional Parallel TAM carries parallel test data. In a typical use scenario, semiconductor manufacturers that perform pre-bond, mid-bond, post-bond, and/or final

tests will use the Serial TAM for test instructions and the Parallel TAM for test data, as it provides higher test throughput and hence shorter test times. Once the SIC is soldered onto a board, board-level interconnect testing and in-chip debug will typically use the Serial TAM, which is then connected to the IEEE Std 1149.1 (“JTAG”) TAP pins.

The stacked dies’ Serial and Parallel TAMs are daisy-chained up in the stack and back down again. Every die can be instructed to be in either a TestTurn or TestElevator mode; the TestTurn mode directs the TAM downward from this die on, while the TestElevator mode continues to involve the next-higher die in the TAM. This allows the test

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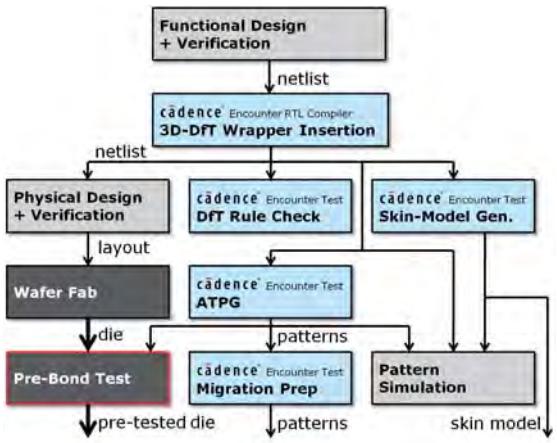


Figure 3. EDA tool flow for die makers



Figure 5. Screen shot from our EDA tool set

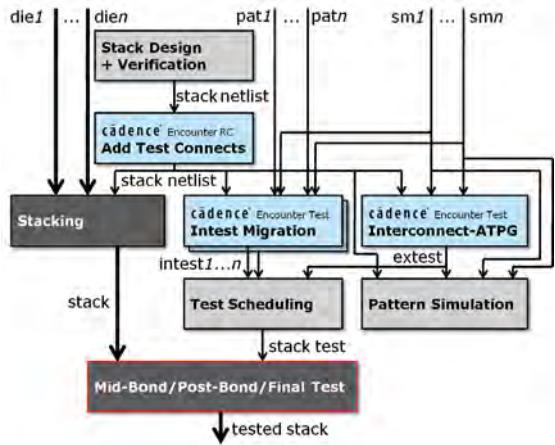


Figure 4. EDA tool flow for stack makers

engineer to flexibly configure his/her test access path in the stack. Each die can be instructed to be in one of three test modes: Intest, Extest, or Bypass. In Intest mode, the die's internals are tested, and its internal DfT infrastructure is included in the TAM. In Extest mode, the die's external connections are tested, i.e., the TSV-based interconnects to another die. In Bypass mode, the die is not testing at all, but simply propagates the TAM data, typically to and from another die-under-test.

If a probe solution is available for micro-bumps, these I/Os can be used for pre-bond testing. This depends on the actual diameter, pitch, and array size of the micro-bumps and the match (or mis-match) to the available probe technology. If pre-bond probing on micro-bumps is impossible, the 3D-DfT architecture provides the option to equip the die with additional dedicated probe pads. A dedicated mode of operation enables test access via these pre-bond

probe pads. As dedicated probe pads bring significant additional area costs, chip designers might want to restrict their number to be less than the number of TSV-based I/Os. This 3D-DfT architecture is prepared to handle different widths for the Parallel TAM for pre-bond and post-bond cases, specifically to allow the trade-off between test bandwidth and corresponding test time on one hand, and cost of additional pre-bond probe pads on the other hand.

A Wrapper Instruction Register (WIR) controls the test mode of a die. Upon reset, this WIR brings the die into its safe functional mode of operation. The WIRs of the various stacked dies are daisy-chained and can be programmed by the test engineer by shifting in instructions via the Serial TAM. This gives the test engineer the flexibility to include, exclude, or re-order tests at will at every stage of the test flow. For example, in a stack of three dies, it would be possible to test all dies sequentially, followed by a simultaneous test of all inter-die interconnects: Die 1; Die 2; Die 3; Intc 1-2 || Intc 2-3. Alternatively, it would also be possible to test Dies 1 and 2 simultaneously, followed by the first interconnect level, Die 3, and then the second interconnect level: Die 1||Die 2; Intc 1-2; Die 3; Intc 2-3.

**Figure 2** shows a schematic implementation of a 3D-DfT wrapper

for a die in the middle of a stack. It has functional and test ports toward the next-lower die shown on the left, and functional and test ports toward the next-higher die shown on the right. It has a Wrapper Serial Control (WSC), a Serial TAM (consisting of Wrapper Serial In (WSI) and Wrapper Serial Out (WSO)), and a n-bit wide Parallel TAM (consisting of Wrapper Parallel In (WPI) and Wrapper Parallel Out (WPO), shown as fat lines). Also clearly visible in **Figure 2** are the mirrored test interface at the top side of the die, and the (optional) additional probe pads for pre-bond testing.

## EDA Tool Support

Cadence Design Systems has worked with IMEC to implement and support the described 3D-DfT architecture with their design automation tools. This led to two tool flows. The first tool flow is for die makers, the second one for stack makers that use the dies as building-block components; these flows are shown in **Figures 3** and **4** respectively. The light-blue boxes show the specific solutions for DfT insertion and test generation. The gray boxes represent the other steps in the flow; light-gray boxes denote other (non-test) EDA steps, dark-gray boxes represent physical operations. The end result of each flow is the ability to perform a test.

The flow for die makers starts with the functional design (and verification) of the die in question. A 3D-DfT wrapper is added to this die design with dedicated scripts for the synthesis tool

Encounter RTL Compiler.<sup>5</sup> The user needs to specify whether or not this is a bottom die that needs to implement IEEE Std 1149.1, the various (optional) instructions and corresponding op-codes that he/she wants to have implemented in the WIR, and the widths of pre-bond and post-bond Parallel TAMs. After a DfT rule check, the die can move on to physical design (layout) and wafer manufacturing. A next step would be automatic test pattern generation (ATPG) with Encounter test. Several sets of test patterns can be generated: for verification of the DfT (through pattern simulation), for pre-bond testing by the die maker, and for die Intest by the stack maker. In case the die maker does not want to disclose the full design details of the die with the stack maker, Encounter Test is able to generate a so-called 'skin model'; this is an abstract version of the die design, which includes all that is necessary for testing this die as part of an SIC, but excludes internal design IP. The skin model allows the stack maker to generate his/her own interconnect (Extest) patterns, but for testing the die itself, he/she will depend on 'migrateable patterns', which can be prepared by Encounter test. In case the die maker does not mind disclosing the full design details of the die to the stack maker, migrateable Intest patterns and skin model are not required and the full netlist of the die suffices; However, because the skin model contains just the logic necessary to run the external boundary scan interface, it allows for a much smaller gate-count model for the SIC.

The outputs of the various dies that presumably go through the die maker flow become the inputs in the stack maker flow. In **Figure 4**, it is assumed that the various die makers want to hide their design details from the stack maker. Hence, for each die in the stack, the stack maker gets the physical die, migrateable Intest patterns for that die, and an abstract skin model for the die. The first action for the stack maker is to do the functional stack design (and verification), i.e., setting the order and configuration of the dies in the stack. In practice, this will typically be done even before the various die makers start

their efforts. The synthesis tool has the ability to automatically interconnect the (Serial and Parallel) test ports of various dies in the stack. The resulting stack netlist is complemented by either the full netlist or the skin model of each die. This combination is used in Encounter

Test for both Intest migration and interconnect-ATPG. Intest migration takes the Intest test patterns as delivered by the die maker, and translates them from a test defined at the die I/Os to a test defined at the SIC I/Os. This translation takes into account the test

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data transportation through Elevator modes of dies lower in the stack and the corresponding required instruction settings for that. This procedure is repeated for the Intests of all dies in the stack. Interconnect-ATPG generates Extest test patterns that cover faults specific to the TSV-based interconnects between the various dies in the stack. These patterns can be simulated for verification purposes. The various tests need to be put in a test schedule and applied to the SIC which is made up of the stacked physical dies.

## Results

A test chip design from TSMC was one of the first vehicles on which the tool flow was demonstrated. The circuit in 65nm CMOS technology was small and I/O rich. The die design was extended with a 3D-DfT wrapper, and, assuming it was the bottom of a die stack, also IEEE Std 1149.1 hardware. The correct operation of this test chip design was verified through design rule checking and pattern simulation. The gate area DfT overhead for this design was 8.4% for plain scan insertion and

JTAG circuitry, and an additional 1.1% for the 3D-DfT wrapper. Note that the relative 3D-DfT area will scale down further for larger, more realistically-sized designs. In addition to these gate area costs, there are area costs for JTAG pads and pre-bond probe pads.

The first hardware demonstrator prototype of the 3D-DfT architecture is currently being developed.

2.5D- and 3D-SICs might contain dies from various die makers. For testing SICs with dies from heterogeneous sources, it is important that the DfT infrastructure in the various dies is compatible. This will require standardization of the DfT, such that compliant dies contain a feature set that guarantees a minimum set of interoperable DfT structures. Specifically toward this goal, the IEEE 3D-Test Working Group is developing the P1838 standard, and our 3D-DfT architecture has been proposed to this Working Group.<sup>6</sup>

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*Erik Jan Marinissen, Principal Scientist at IMEC can be reached at mariniss@imec.be*

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# TSV Interposers: The Most Cost-Effective Integrator for 3D IC Integration

By John H. Lau, [Electronic & Optoelectronic Research Labs, ITRI]

**3**D integration consists of 3D IC packaging, 3D IC integration and 3D Si integration. It is the presence of through silicon via (TSV) — or lack thereof — that separates 3D IC packaging from 3D IC/Si integrations, since the latter two use TSV but 3D IC packaging does not. TSV 3D integration involves stacking thin chips with microbumps while 3D Si integration refers to thin wafer stacking without bumps (i.e., bumpless). In 3D IC integration the TSVs can be made by using either via first, middle, or last methods, while for 3D Si integration the TSVs can be made before bonding if Cu-to-Cu method is used or after bonding if  $\text{SiO}_2$ -to- $\text{SiO}_2$  method is used. The TSV diameter for 3D Si integration is  $\leq 1\mu\text{m}$ , but is much larger for 3D IC integration e.g.,  $\geq 5\mu\text{m}$ . Via filling material for 3D IC integration is usually copper and is fabricated by electroplating, while for 3D Si integration is either tungsten or copper by physical vapor disposition (PVD).

In the next 10 years, high volume products with 3D Si integration, will exist in niche applications. But ultimately 3D Si integration is the right way to go and compete with Moore's law. In the mean time, 3D IC integration offers a compelling and cost effective stepping stone and more.

## Memory-Chip Stacking

Basically, there are two groups of 3D IC integration; one is memory chip stacking and the other uses interposers (active and passive). Unfortunately, due to cost issue and competing technologies, e.g., Au/Cu wire bonding, memory-chip stacking is not in volume production today.

## Active Interposers

TSVs can be used as active interposers

such as logics and microprocessors. For example, Samsung has proposed a wide I/O DRAM in which the master chip is the active interposer. However, due to the high device density and complexity of the circuits on the CPU and logic chips, finding places/spaces to "drill" holes (TSVs) either by via-middle or via-last processes are very difficult. Additionally, the CPU (or logic chip) and memory chip sizes and number of pin-outs may differ. Forcing them to attach reduces design freedom and could compromise functionality. Thus, for active interposers, we have to wait for the ecosystem and EDA, except for some companies with both memory and logic technologies/capabilities and niche applications such as CMOS image sensor (CIS), 3D MEMS, and 3D LEDs.

## Passive Interposers

The biggest issue with 3D IC integration using active interposers for system houses is the "business model". Companies buy the chips from different sources and want them to be "bullet-proof" before they are shipped to the OSATs. Forcing two chips from different sources together into "one chip" is not acceptable to the system houses because if something wrong, they don't know who is responsible for finding the root causes and fixing the problem so they can quickly ship their products again.

Using a passive interposer to integrate a few "bullet-proof" chips together is what the system houses prefer. Thus, passive interposer

becomes the most effective and low cost 3D IC integrator, as it eliminates the need to fabricate TSVs into active dies. Additionally, there is no need to thin and metalize the active dies. Furthermore, there's no need to temporary bond and subsequently debond a supporting wafer to the active wafers. In this scenario, the passive interposer is the workhorse of our 3D IC integration SiP before the 3D Si integration time comes.

## Passive Interposers Used as Substrates (2.5D Integration)

There are two kinds of passive interposers; one is 2.5D IC integration (Moore's Law chips on the interposer's top side) and the other is 3D IC integration (Moore's law chips on both sides of the interposer).

**Figure 1** shows ITRI's test vehicle for the study of its electrical, thermal, and mechanical performances. The interposer (with  $15\mu\text{m}$  vias) supports four memory chips (with  $10\mu\text{m}$  vias) stacked, one thermal chip, and one mechanical chip. It is over-molded

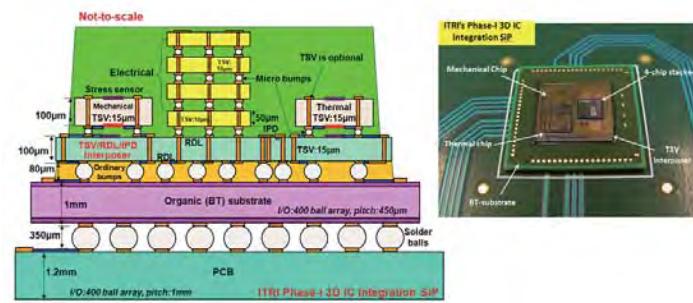
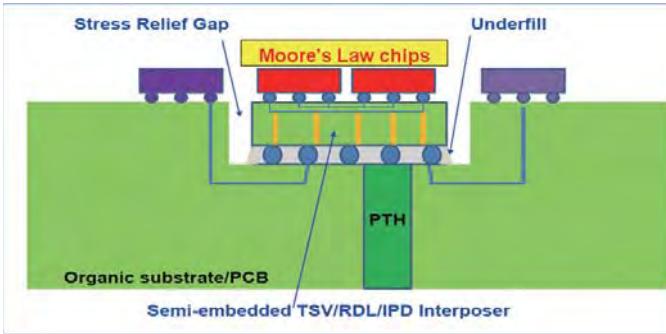


Figure 1. TSV interposers used as substrates: ITRI's Phase-I 3D IC integration test vehicle. Updated from [IEEE/ICEP (2011)]

for pick-and-place purpose as well as to protect the chips from harsh environments. There are RDLs and stress sensors on the interposer's top and bottom sides. Also, integrated passive devices (IPDs) are fabricated through the thickness ( $100\mu\text{m}$ ) of the interposer ( $12.3\text{mm} \times 12.2\text{mm}$ ).



**Figure 2.** Semi-EMBEDDED TSV interposer with stress relief gap. Note: underfill between the chips and TSV interposer and the chips and organic substrate/PCB is necessary

This test vehicle can be degenerated to the case of: wide I/O DRAM if there are not mechanical and thermal chips and the interposer is an ASIC; wide I/O memory if there is not the memory-chip stacking nor the TSVs in the mechanical/thermal chips and the interposer is either an ASIC or microprocessor; and wide I/O interface if there is not the memory-chip stacking and there are not any TSVs in the thermal/mechanical chips. Thus, the enabling technologies developed with this test vehicle can have very broad applications.

**Figure 2** shows a semi-embedded TSV interposer with a stress relief gap. The design is low profile and free to use of any Moore's law chip without TSVs, which results in a short design cycle with low manufacturing cost. Additionally, RDLs allow chips to talk to each other at short distance. Many TSVs can be used for power and ground. This design is very reliable because the stress relief gap reduces the thermal expansion mismatch between the embedded interposer ( $6 - 8 \times 10^{-6}/^{\circ}\text{C}$ ) and the organic substrate/PCB ( $15 - 18.5 \times 10^{-6}/^{\circ}\text{C}$ ).

### Passive Interposers Used as Stress Relief (Reliability) Buffers for Moore's Law Chips

A Moore's Law chip can be attached on a Cu-filled TSV interposer and then on a BT-substrate, or it can be attached on the BT-substrate directly. The Cu-filled TSV interposer acts like a stress relief (reliability) buffer and reduces the stress (from 250MPa to 125MPa) acting at the Cu-low- $k$  pads

of the Moore's law chip. This is more important for smaller feature size chips because the allowable stress on their Cu-low- $k$  pads is smaller. This is because the coefficient of thermal expansion (CTE) of the Si chip

is  $2.5 \times 10^{-6}/^{\circ}\text{C}$ , of the BT-substrate is  $15 \times 10^{-6}/^{\circ}\text{C}$ , and of the Cu is  $17.5 \times 10^{-6}/^{\circ}\text{C}$ . The effective CTE of the Cu-filled TSV interposer, depending on the number of vias, is  $8 - 10 \times 10^{-6}/^{\circ}\text{C}$ . Thus, with the Cu-filled TSV interposer, the thermal expansion mismatch between the Moore's Law chip and the interposer is smaller than that between the chip and the BT-substrate. If an underfill is added between the chip and the interposer, the stress acting at the Cu-low- $k$  pads of the chip is further reduced to 42MPa [IEEE Trans. on Advanced Packaging (2009) and Trans. on CPMT (2011)].

### Passive Interposers Used as Carriers

A 3D module has been designed that consists of two stacks assembled one over other with three chips [IEEE Trans. on CPMT (2010)]. The module size is  $12\text{mm} \times 12\text{mm}$  and  $1.3\text{mm}$  thickness. The silicon carrier is  $12\text{mm} \times 12\text{mm} \times 0.2\text{mm}$  with 168 peripherally populated vias. The bottom carrier (Carrier 1) is assembled with a  $5\text{mm} \times 5\text{mm}$  flip chip. The top carrier (Carrier 2) is assembled with a  $5\text{mm} \times 5\text{mm}$  flip chip and two stacked  $3\text{mm} \times 6\text{mm}$  wire bonded chips. Carrier 2 is over-molded to protect the wire-bond chips. The silicon carriers have been fabricated with two metal layers with  $\text{SiO}_2$  as dielectric/passivation layer. Electrical connections through the carrier are formed by TSVs.

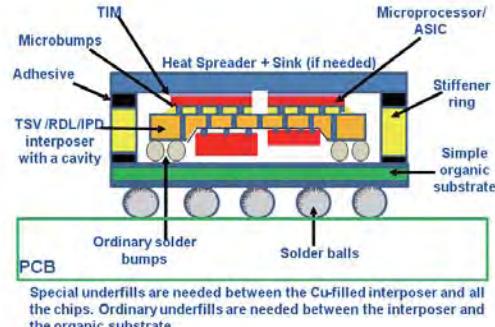
Carrier 1 is mounted on a FR4 PCB using SAC305 of  $250\mu\text{m}$  diameter. Carrier 1 assembly is underfilled and cured at  $165^{\circ}\text{C}$  for 3 hours.

### Passive Interposers for 3D Integration

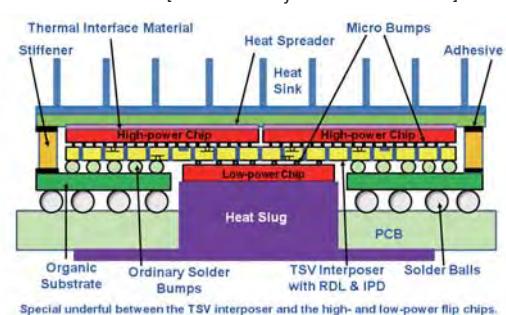
Most passive interposers reported in literature are 2.5D IC integration SiPs, i.e., the interposer supports chips only on its top surface. In this study, a few low-cost and thermal enhanced 3D IC integration SiPs with a passive TSV interposer are presented. There are no TSVs in any of the Moore's Law chips.

### Design Philosophy

The present design philosophy addresses the 3D IC integration with a passive TSV interposer with RDLs and/or IPDs for all kinds of Moore's Law chips for small form factor, high pin-count, high performance, low power, wide bandwidth, and eventually/potentially



**Figure 3.** TSV interposer supporting high-power chips on its top side and low-power chips at its bottom side with a cavity. Modified from [Invited Plenary talk at IWLPIC 2011]



**Figure 4.** Passive TSV interposer with RDL and IPD supporting high-power chips on its top-side and low-power chips at its bottom-side. The heat of the high-power chips is dissipated from their back-side through a TIM and heat spreader + sink if necessary. The heat of the low-power chips is dissipated from their back-side through a TIM and a heat slug + spreader if necessary. The organic substrate is with a cavity.

low-cost applications. To achieve this, the design uses chip-to-chip interconnections through a passive TSV interposer in a 3D IC integration SiP format to:

- Provide vertical (as well as horizontal) electrical feed through interconnections.
- Arrange power, ground, and signal distributions.
- Perform redistributions (to fan out high pin-out and ultra fine-pitch circuitries).
- Provide decoupling (to enhance the electrical performance).
- Connect to the next level of interconnects.
- Construct a cost-effective thermal management system

For example, 3D IC integration SiP (wide I/O memory) can be redesigned with a TSV/RDL/IPD passive interposer as shown in **Figure 3** (the cavity is optional). In this case, no new EDA is needed, there are no TSVs in the chips, the heat from the high power chips can be removed from its back side, and the solder joint reliability is not an issue. The outlook (package) of this proposed 3D IC integration SiP is very attractive to integrated device manufacturers (IDMs), original equipment manufacturers (OEMs), and electronics manufacturing services (EMS) because it is a standard PBGA package and has been used by the electronic industry for more than 15 years.

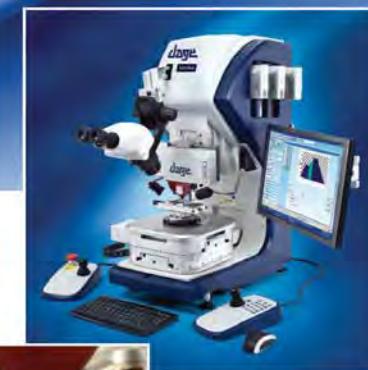
The 3D IC integration SiP as shown in **Figure 4** features a silicon interposer with high-density TSVs, RDLs, and IPDs that connect various Moore's chips with pads that have different pitches, sizes, and locations. A simple, organic substrate with a cavity and with standard (in size and pitch) solder balls for PCB assembly supports the passive interposer. All the high-power chips such as the micro-processor unit (MPU), graphic processor unit (GPU), application specific IC (ASIC), digital signal processor (DSP), micro-controller unit (MCU), radio frequency (RF), and high-power memory chips are on top of the TSV interposer in a flip-chip format so that the backside of these chips can be attached to a heat spreader

via a thermal interface material (TIM). In this example, most of the heat from the high-power chips can be dissipated through the heat spreader (with a heat sink if it is necessary). All low-power chips, e.g., MEMS, OMEMS, CMOS image sensors, and memory are at the bottom-side of the interposer. The back-side of the low-power chips is attached

to a heat slug/spreader. A ring-stiffener connecting the organic substrate and the heat spreader provides adequate standoff for 3D IC integration with the passive interposer and to support the heat spreader with or without the heat sink. Underfill encapsulants are needed between the TSV interposer and the high- and low-power flip chips, and

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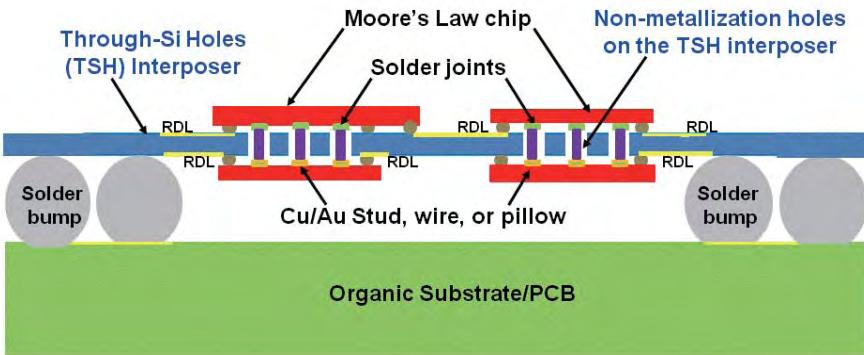
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**Figure 5.** A very low-cost through-silicon holes (TSHs) interposer for 3D IC integration

between the TSV interposer and the organic substrate. However, underfill is not needed between the 3D IC integration SiP and the PCB.

The outlook (package) of this proposed 3D IC integration SiP has been used by the electronic industry for more than 15 years. It's not only effective in thermal management, but its solder joints are very reliable. Therefore, in conjunction with the proper design of the high-power and low-power chips above/below the passive TSV/RDL/IPD interposer inside the package, a cost-effective, 3D IC integration SiP that displays high electrical and thermal performance can be achieved and manufactured.

**Figure 5** shows a very low-cost passive interposer involving a piece of silicon with holes made by either deep reactive ion etch (DRIE) or laser. These holes are not metallized and thus it is called through-Si hole (TSH) interposer. It can be used to support Moore's Law chips on its top-side and bottom-side, and let the signals of Moore's Law chips on the top-side transmit to the Moore's Law chips on the bottom-side (or vice versa) through the Cu/Au wires, studs, or pillows. The TSH interposer's RDL (redistribution layers) can let the Moore's Law chips communicate to each other on the top-side and/or the bottom-side of the TSH interposer.

**Figure 6** shows a low-cost (with bare chips) and high (optical, electrical, thermal, and mechanical) performance optoelectronic system embedded into a PCB or an organic laminated substrate. This system consists of a rigid PCB (or a substrate) with an embedded optical polymer waveguide, vertical cavity

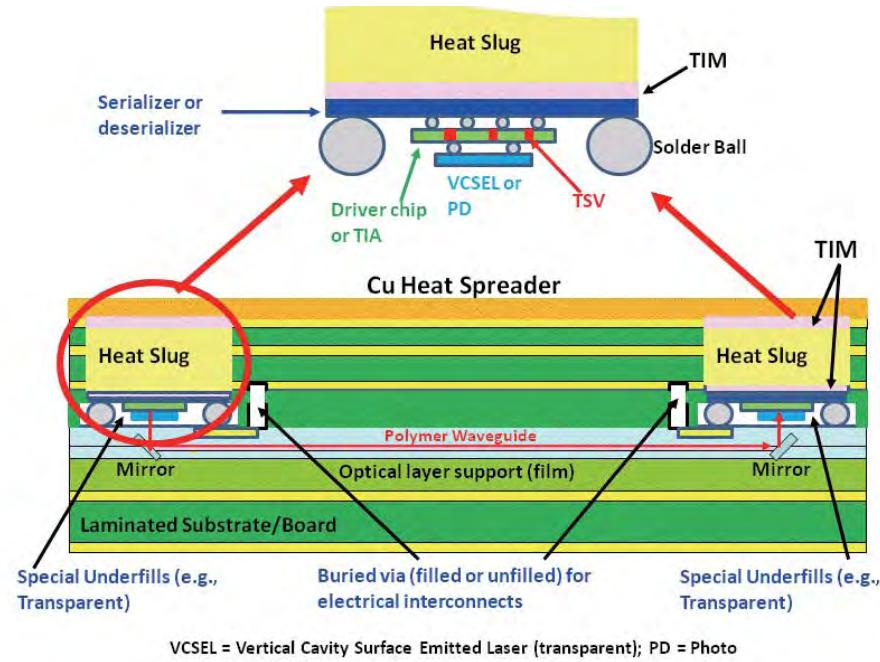
surface emitted laser (VCSEL), driver chip, serializer, photo-diode detector, trans-impedance amplifier (TIA), and deserializer. The bare VCSEL, driver chip, and serializer chip are 3D stacked and then attached on one end of the embedded optical polymer waveguide in the PCB. Similarly, the bare photo-diode detector, TIA chip, and deserializer chip are 3D stacked and then attached on the other end of the embedded optical polymer waveguide in PCB. The back-side of the driver or serializer and the TIA or deserializer chips is attached to a heat slug with or w/o a spreader. This structure offers low-profile optoelectronic packaging for chip-to-chip optical interconnects. Optical, thermal management and

mechanical performances have been demonstrated by simulations based on optic theory, heat-transfer theory, and continuum mechanics.

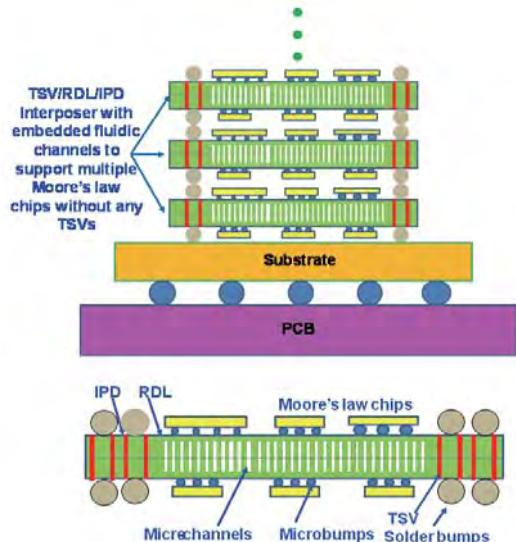
## Passive Interposers used for Thermal Management

The 3D IC integration SiP shown in **Figures 3, 4, 5, and 6** cannot be stacked into 3D because of the heat spreader and heat sink. Also, there may not be the luxury to separate all the high-power chips (on top) from the low-power chips (at the bottom) of the interposer. **Figures 7 and 8** show a new 3D IC integration SiP design that can be stacked with chips randomly arranged on top or bottom of the interposer.

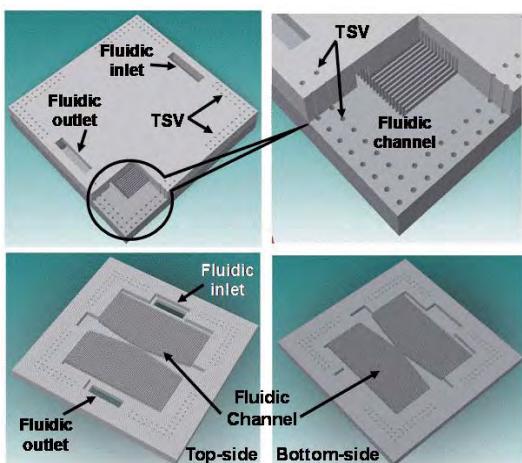
The basic unit consists of the TSV/RDL/IPD interposer with embedded fluidic channels. This interposer is fabricated by bonding two silicon wafers together, and an optimized liquid cooling channel structure is embedded in between the chips. Silicon is chosen as interposer material because it is a suitable material for the integration of both electrical and fluidic structures in the same substrate with micro fabrication process. The difference between these two chips is that the



**Figure 6.** Embedded 3D hybrid IC integration for opto-electronic interconnects. Updated from [ASME Trans. J. of Electronic Packaging (2011)]



**Figure 7.** 3D IC integration SiP consists of a series of TSV/RDL/IPD interposers with embedded fluidic channels to support multiple Moore's law chips on its top and bottom sides. Updated from [Keynote given at IEEE/EDAPS 2010]



**Figure 8.** Interposer with TSVs for electrical feed through and fluidic microchannels for thermal management. Updated from [Advanced MEMS Packaging, McGraw-Hill, 2010]

bottom Si chip does not have any outlets. TSVs can be designed along the periphery of the interposer. After W2W bonding, electrical interconnection through the carrier is made by the TSV with on-wall metallization (in this case, the copper filling may not be necessary). The fluidic channels are connected out through the inlet and outlet. There are sealing rings (the solder is Au20Sn and the UBM is TiCuNiAu) around both the fluidic path and the individual TSV to isolate the fluid from the electrical interconnection (**Figures 7 and 8**).

## Summary and Recommendations

In the next 10 years, most TSVs

will be fabricated on passive interposers. They are not only a stepping stone for 3D IC integration, they will be here for a very long time like the solder-bumped flip chip technology.

Passive interposer technology is the most cost-effective 3D IC integrator because it can serve as both substrates and carriers. Also, the passive interposer acts like a stress relief (reliability) buffer, which reduces the stress acting on the Cu-low-k pads of Moore's law chips. This advantage becomes more pronounced when the feature size (technology node) is getting smaller and so does the allowable stress of the chip pads. Furthermore, they can manage almost all thermal problems of 3D ICs.

3D Si integration is the right way to go to compete with Moore's law. However, it is still a long way off. Hopefully by 2020 at least the memory-chip stacking (bumpless) could be manufactured by W2W bonding at lower costs and higher throughputs by using the 3D Si integration. 15 years from now, the heterogeneous structures such as the wide I/O DRAM could be manufactured at high volume with the 3D Si integration technology by (bumpless) C2W bonding. These processes will likely be performed by semiconductor foundries. The packaging assembly and test houses will handle the routine tasks such as dicing, packaging, and testing.

## Acknowledgements

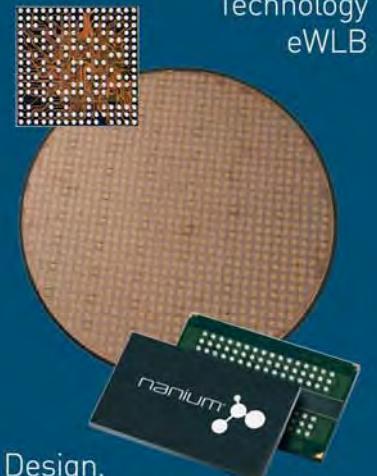
The author would like to thank Dr. Ian Yi-Jen Chan, Vice President and Director of Electronics & Optoelectronics Research Laboratory for his strong support on this project. He also would like to thank the useful contributions from the 3D IC Integration Task Force members.

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# Big Market Player Makes a Big Move

By François von Trapp, Sr. Technical Editor

**R**elocating any company is not an easy task, nor one that is taken lightly. When it involves dividing operations into two new locations for various purposes, it's an even bigger deal. So when SUSS MicroTec completed the simultaneous



Figure 1. Sunny skies ahead for the SUSS MicroTec team, outside their new west coast digs

relocation of its bonder manufacturing division from Waterbury VT to Sternenfels, Germany, and its North American headquarters from Waterbury to Sunnyvale CA, Chip Scale Review thought it would be a good idea to pay a visit to the new NA headquarters, and learn more about the motivation behind the move, how it all came about, and how things are shaking out so far. So in late July, François von Trapp, Sr. technical editor, and Kim Newman, publisher, visited SUSS MicroTec for



Figure 2. Wilfried Bair, General Manager, SUSS MicroTec, talks about the advantages of moving to Sunnyvale

the grand tour. We met with Wilfried Bair, general manager; Andrew Romano, applications manager; and Stefan Lutter,



Figure 3. Andrew Romano, Applications Manager, gives us a window tour before suiting up for the cleanroom

product manager for the bonder division, (who was visiting from Germany); and Gayathri Jampa, application engineer.

While Vermont may look and feel a lot like home (aka SUSS MicroTec's world headquarters in Garching, Germany), the reality is it's 3000 miles away from the bulk of the company's manufacturing and a logistical nightmare for potential customers in this global market. Other than the scenery and great skiing that reminded company founder, Karl Suss, of Bavaria, there aren't many advantages to being there, especially with the continued globalization of this industry.

The opportunity to make the move presented itself when SUSS MicroTec bought Hamatech's mask cleaning operation in Sternenfels, Germany in 2010. The motivation to buy the company is the synergy with SUSS MicroTec's mask aligner technologies and the EUV mask cleaning technologies, which can be leveraged across a variety of platforms. The now available large manufacturing space that came along with the purchase was a bonus, and allowed for a new home for manufacturing resist coaters and the bonding tool product line, explained Bair.

At the same time, North American headquarters were relocated to Sunnyvale, providing better access for tool demos to prospective customers, as well as to be able to serve existing development customers working on prototypes and low volume



Figure 4. SUSS MicroTec's SB6/8E is part of the company's semi-automatic bonding line and is, according to Romano, a workhorse for manufacturing manufacturing in Silicon Valley, as well as production customers in Korea, Taiwan and China. The new applications lab is now well suited to support process development and characterization of 200 and 300mm 3D TSV temporary bonding and debonding, as well as permanent bonding processes. Additionally, the lab will also support development of MEMS, LED, and wafer level packaging (WLP) processes. According to Bair, LEDs has been a particularly active market for them, with a significant part of the current demos being in the LED space.

The timing for all of this couldn't have been better. Bair explained that with the company's focus on 3D TSV processes, it was critical to get settled in the new location before the market ramps to production. The 3D market will take off in 2012-2013 timeframe," predicts Bair, "We'll be ready for the ramp to capacity."

## 450 Readiness

With 450mm seemingly imminent, it seemed apropos to question Bair about the company's position on 450. With a focus on automated tools for HVM, Bair says the company is following developments in the 450 space closely, and reviewing specs. He believes that there are selective technologies suited



**Figure 5.** Romano shows of the DB12S, a debonding module central to the room temperature bonding processes



**Figure 6.** Lance Mistler (left) and Randy Fitzgerald (right) at the CB 300 bonder

to the increased wafer size, such as Cu bonding, which requires lower temperatures. There is motivation at SUSS MicroTec to make the low temperature temporary bond and debond tools 450mm capable.

Bair also noted that moving to 450mm is a bigger technology challenge in the front-end than in the back end. But once the front-end moves to 450mm, there will have to be back-end equipment that can handle 450mm wafers. So the whole transition is dictated by what happens up front. Suffice it to say that when 450mm hits volume manufacturing SUSS MicroTec will be ready for them.

## The Grand Tour

After briefing us on the state of the move, Bair put us in the capable hands of Andrew Romano, for an explanation of the company's development work with research partners as well as a tour



**Figure 7.** Applications engineer, Gayathri Jampana and Romano pose with the XBC300 automated bonding system

of the applications and demo lab, which is outfitted to support 3DIC, MEMS and LED processes. He explained the different work taking place.

Demos happen two ways, explained Romano. Potential customers send wafers, SUSS MicroTec engineers perform the processes according to customer specs and recipes, and send the wafers back for evaluation. Alternatively, customers send their assignees to SUSS MicroTec along with the wafers to participate in the demos.

Revenue generating projects are also taking place in the applications lab, thanks, in part, to several joint development projects (JDPs) that are currently underway. One of these is the recently announced project with Tanaka Precious Metals to jointly develop sub-micron gold particle pattern transfer and bonding technologies. The transferred pattern of gold particles helps to absorb wafer surface roughness, reportedly making it possible to achieve metal-metal bonding on a wafer level at 200°C while also enabling high temperature resistance, high reliability hermetic seals and electrical connections. Target applications include assembly and packaging processes for MEMS, LEDs and WLP.

Inside the applications lab, Romano guided us by the tools that have been installed so far. These include a manual 200mm dual cleaning system for surface preparation of wafers for fusion bonds; a pattern lithography tool that Romano said was the workhorse for MEMS; a spin coater, and various manual and



**Figure 8.** Kim Newman, publisher, CSR; Jampana, and Francoise von Trapp, Sr. Technical Editor, CSR – bonding as SEMI Sisters

automated bonding tools and clusters that run the gamut of bonding processes such as temporary bond and debond, adhesive, thermocompression and fusion bonds.

Applications engineer, Gayathri Jampana, enthusiastically showed off her "charge," the XBC300 bonding cluster. Jampana is SUSS MicroTec's newest hire in the Sunnyvale location, and her job is to further develop fusion bonding processes on this tool. She explained fusion bonding, which involves the spontaneous adhesion of two substrates – in this case silicon wafers – placed in direct contact. This room temperature process can be performed with or without dielectric layers following a wet chemical or plasma activation step. Jampana has been working with dry activation plasma, which she says is a more effective process than wet, and depends upon van der Waals forces. Advantages of this process is that it is a low force bond, (critical when dealing with ultra-thin wafers) and requires low temperatures to achieve (also critical for 3D TSV stacking.) It is expected that room temperature (RT) processes will be the way to go.

## A Final Note

So far, Bair says the move has been a success and the company is ready to grow right along with its target markets. Already considered a market leader in lithography tools for WLP, Bair says the company is in the top three position for MEMS, compound semiconductors and LEDs as well. One thing is certain, in this new location, clear skies are always ahead. 

# Electronic Medicine: The Next Disruptive Medical Technology

By François Berger and Ali Bouamrani, [CEA-Leti, CLINATEC]

**M**edical history is paved with disruptive progresses often supported by innovative technologies associated with conceptual tools. Anatomo-clinical medicine is still prevailing in current medical procedures. It emerged from the idea that symptoms can specify the location of the pathological process. Autopsy and microscopy were disruptive technologies that provided a window for defining diseases.

The electronic race toward more miniaturized systems following Moore's law and stimulated by the exponential dissemination of electronics tools was a fantastic trigger for technology improvement. Semiconductor technology provided innovative materials such as modified silicon, nanoporous silicon and, more recently, graphene. This favored the development of extensive miniaturization and integration at the nanolevel. Photonics benefited from the inorganic light-emitting diodes (LEDs). Similarly, energy and radiofrequency communication devices were fully optimized.

The classical understanding of electronic for medicine is primarily in the "e-medicine" field. However, electronics are already an essential tool in medicine. Radiologic imaging devices, lab-on-chips as well as many medical devices are built around semiconductor technologies. Our vision is that electronics are not only instrumental tools for medicine, but a more basic trigger that could contribute to reinvent classical anatomo-clinical medicine defining, in association with molecular and cellular medicine, a new electronics medicine potentially dramatically disruptive as well. To succeed, we need to anticipate major but mandatory modifications of the technology, medical and industrial organizations. Developing new strategies to accelerate the translation at the patient's bedside of technological breakthrough and making it safer is a priority.

There are a number of emerging fields in medicine that could benefit and be developed in synergy with electronics technologies. Real disruptive applications can participate to re-invent medicine in pathological fields still confronted with therapeutical inefficacy, death and handicap.

## E-Medicine

E-medicine involves the implementation of

informatics tools and mobile communication devices moving the highly centralized medical organization to a decentralized organization with point-of-care networks. E-medicine is a very important field of development, but it is still not fully accepted and disseminated. The main issue is that medico-economical evaluation was very low in contrast with major investments needed in practices modifications. Only a disruptive impact, which means major benefit for the patient and the medical care system, will really support e-medicine growth. Several opportunities are available, benefiting from the miniaturization and integration of electronics technologies.

Highly miniaturized MEMS sensors can be integrated on the surface of the body, providing new medical examination and monitoring modalities. Movement, pressure, temperature as well as biologic information can be investigated and monitored with minor modifications of a patient's every day life. The power of informatics algorithms could identify complex profiles to monitor diseases progression and response to therapy. It was recently demonstrated that physical therapy can impact the progression of some neurodegenerative diseases. These sensors could be employed also to implement physical therapy at home using "medical-wii-like" devices associating disease monitoring and therapy.

## Personalized Neurostimulation and Physical Modulation

Classical electrostimulation therapies use technologies that are similar to heart pace makers. Electronics give us the opportunity to develop second-generation devices, solving the issue of energy constraints that requires surgery for the battery renewal. Miniaturized batteries, the use of body energy, or cell metabolism are alternatives to improve the energy dependency of implanted devices. Multiplexed neurostimulation may also provide the opportunity for adaptability to the individual neuroanatomy. Complex multiple neurostimulation devices will be indispensable for that. Adapting neurostimulation parameters to brain conductivity and excitotoxicity is the last perspective: a close-loop-monitoring device should permit this optimization linking neurostimulation parameters to the brain electrophysiology. At the end, development of an autonomous internally regulated 3D multiplex



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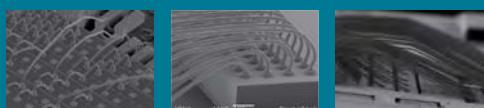
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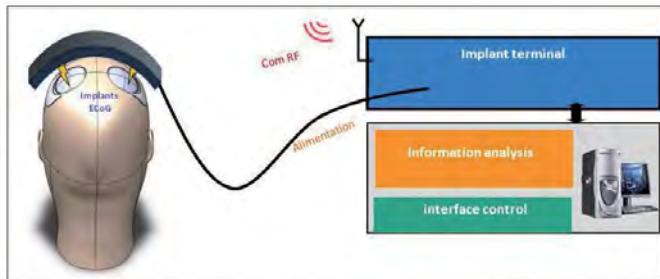
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**Figure 1.** The brain-computer interface concept in response to major handicap such as tetraplegia

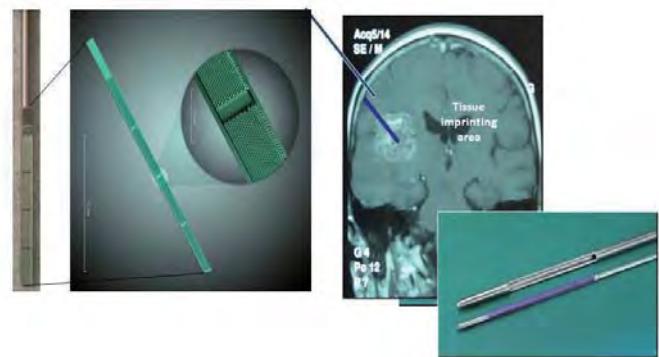
neurostimulation device may dramatically enhance therapeutical efficacy and quality of life in neurostimulated patients. Emerging physical modalities such as optical or magnetic stimulations will also benefit directly from electronics.

### Brain Computer Interface (BCI) Technologies

Spinal cord traumatic injury can destroy the communication between the brain encephalic command and the motor behavior, resulting in a major handicap named tetraplegia. BCI strategy is to directly record the brain neuronal activity emitted by the patient and to translate it into physical action. The challenge is to develop complex algorithms that can interpret the complexity of the patient's command using the brain electrophysiologic information locally activated. Depending on the number of degrees of liberty that will be extracted, more complex devices will be controlled from a computer mouse to an exoskeleton giving back motor autonomy to the patient. Intracortical device has been developed and already tested in tetraplegic human patients (**Figure 1**)

### The Brain-Biomarker-Interface Concept.

Exploration of non-tumoral brain pathologies is commonly considered as impossible because of potential deleterious side effects related to tissue removal. However, DBS provides the opportunity to access previously unexplorable brain areas contacted with functional neurosurgery micro-invasive tools. Silicon is an extraordinarily useful material that can be chemically modified and micronanostructured. A specific microstructuration and chemical modification was developed that improves the bioharvesting of biological materials in contact with the non-lesional devices introduced within the brain (**Figure 2**). As done in criminal medicine, brain pathology traces are recovered without any lesion providing a unique opportunity to decipher brain pathologies. The perspective is to move neurodegenerative and potentially psychiatric diseases in the field of personalized therapy as it is being done in oncology. New materials have been developed to optimize biological capture at the interface with pathologies such as nanoporous silicon.



**Figure 2.** silicon as a key material for innovative bioharvesting in the brain.

### Local Drug Delivery

Systemic therapies have difficulties reaching the brain because of the blood-brain-barrier. They also induce many side effects because of their systemic diffusion through the entire body. Delivering treatment locally and precisely at the pathological site has been investigated for many years. However, existing devices result in local leakages, inducing side effects and inefficacy. The use of miniaturized, locally controlled devices fabricated with new materials and employing electro-driving forces may solve these major difficulties.

### “Electronics drugs”

Nanoelectronics supports nanofabrication processes, reaching the size of the molecular actors of diseases. Recent technologies have been developed using conventional non-expensive nanofabrication strategies originating from electronics, such as imprints nanofabrication or photolithography to design nano-objects used for therapy. Applications are emerging using these devices as contrast agent for radiology, but also as carriers for drug delivery or gene therapy. Moreover, these nanofabricated structures could also interfere directly with the molecular pathways governing the pathological processes independently or after activation by external physical triggers such as magnetic stimulation. A new world is emerging where the traditional tools from the pharmaceutical industry will be renovated by electronics fabrication processes.

### Multifunctional Smart Theranostic Devices.

The ideal devices will integrate several properties associating continuous monitoring of brain activity, therapeutical actions using both physical therapy, local or systemic delivery and close loop regulation.

### Prerequisites for Success

Innovative technologies need to be evaluated prior to human application to anticipate potential toxicology. Cell culture but also animal tests are mandatory. A widely debated issue is the novelty of

these nanofabricated devices and new materials and our capacity to predict their safety. Specific tests and methodologies need to be implemented. Classical toxicology involves mainly histological analysis and hepatic, renal or hematologic investigations. The mechanisms of nanotube toxicology have been attributed to an immunological reaction, adding the dosage of multiplexed cytokines and cell-inflamatory tests to the standard tests done for classical drugs. Whole-genome explorations, now easily performed using DNA-chip technologies, offer the opportunity to investigate widely potential non-anticipated cell toxicology events. Moreover, relevant animal models need to be used, especially big animal models, such as pigs or primates, which have immune reactions that are much closer to humans.

Classical clinical validation of new drugs follows a 4 phase trial strategy that includes tests for potential side effects and defining more efficient doses without side effects; testing efficacy of the drug in a limited number of patients; and comparing the efficacy of the new drug to the existing medical reference in a large number of patients. Time to the market for a new drug is more than 10 years. Medical devices are evaluated even more rigorously for their technological robustness than for their clinical impact. European regulation recently called for clinical trials to prove efficacy and inoccuity in brain-implanted devices, moving medical devices regulation closer to the drug regulation.

The efficacy of conventional drug development is being questioned because of the decreasing ability to deliver new active drugs, due to cost and severe side effects found even after regulatory approval. To solve these problems a new methodology is emerging, involving early phase trials to explore, in a small number of patients, both side effects and technological proof of concept. To predict and monitor both the optimal putative efficacy and potential side effects, a multimodal strategy is employed using multimodal

imaging and biological investigations. This provides a powerful approach to know at the early stage and rapidly if the strategy is really efficient or toxic saving time for patients and accelerating access to the market.

### **Medico-Economic Evaluation: A New Business Model for Electronics.**

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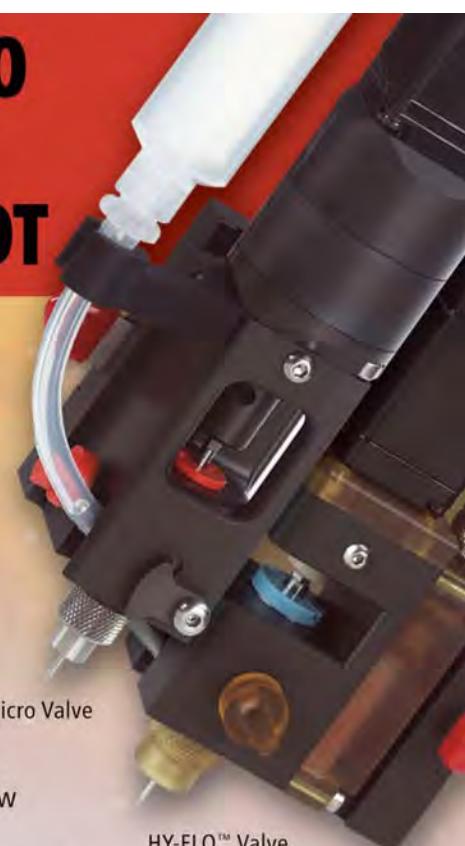
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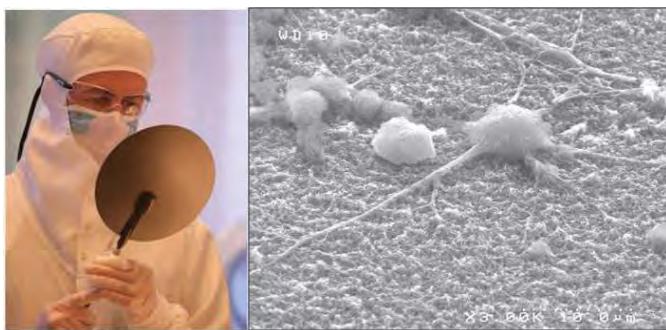
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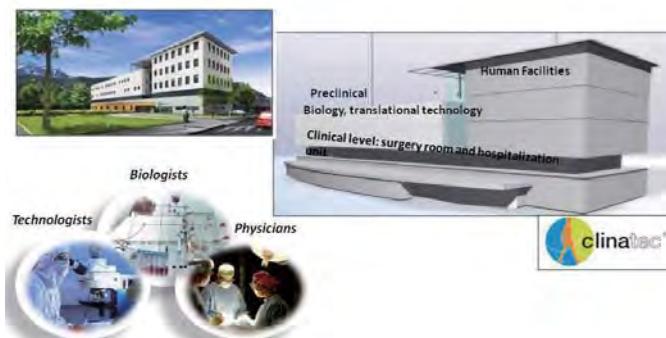
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**Figure 3.** Illustration of a neuronal stem cell grown on carbon nanotubes-coated silicon.



**Figure 4.** CLINATEC a preclinical and clinical research center : multidisciplinarity, direct integration to the LETI-CEA MINATEC campus and multimodal investigations toward accelerated and safer translation at the bedside of micronano and electronics technologies

and mobile phone business models, which means "high volumes at low price" with a small individual benefit. The Moore's Law race and industrial competition imposed development of more sophisticated fabrication units in the semiconductor industry. In the medical area, too many drugs or medical devices are developed with a low medical benefit but an elevated economical cost. The limits of the big pharmaceutical companies classical blockbuster strategy have been reached. Is it rational to spend millions of dollars or euros and more than 10 years to deliver drugs that statistically offer an increased survival of one or two weeks with sometime severe side effects and a high cost for the social security system? Its critical to not follow the same medico-economical scheme to develop electronic medicine for health. It seems that on both electronics and pharmaceutical sides the business models have to be re-invented. The poor translation of e-medicine was explained by a poor demonstration of the benefit. The price of the product will be directly connected to efficacy. To reach the market, innovative products will have to be really efficient. To prove that, medico-economical studies will be mandatory to convince private or public social security system. An efficient association between pharmaceutical and electronics companies must be developed.

Anticipating ethics and societal acceptance is mandatory. Recent studies on the social perception of nanotechnology demonstrated that citizens are not aware of what nanotechnologies are, and are

alarmed by the possible non-motivated dissemination of technologies with potential deleterious side effects. Side effects are unacceptable for non-medical applications. Development of adequate research to eliminate unknown toxicology is highly requested. For medical applications, society has a good understanding of the risk/benefit balance that is one of the first ethical bases for the practice of medical innovation. This means that new technologies tested in human patients will need to be investigated in patients presenting a prognostic outside of the potency of classical accepted medical strategies. The second main ethical principle is informed consent. This means that patients and their family need to be fully informed of the new biomedical strategy. To do that, we initiated a research work with human sciences researchers testing the understanding of the technology and building with both the experts and the patients a relevant informed consent for the early phase trial. At least, a fundamental ethical issue is the status of the human body integrating autonomous electronics as well as the indispensable discrimination between real medical applications and human enhancement.

### The Clinatec Example

A strong medical, societal, industrial and economical need is emerging to accelerate the translation of micronanotechnology innovation at the bedside, keeping and enhancing the essential patient's safety. The Grenoble example is both highly specific and paradigmatic considering the combination of high-level research in the field of medical technology and the exponential development of the electronics and micronanotechnology research center, LETI. Moreover, LETI was extended by the creation of MINATEC campus. The health investment was also major in LETI by the implementation of a department in charge of health technology development as well as by the building of a nanobiology research center combining biological research laboratories and technologists. To finalize this, a new global campus "GIANT" will be achieved in 2015, connecting all these technology entities with the city, bringing students, habitations, sport complex and public transportation, to provide a unique integration between technology, education, industry and the citizens. Connection with the patients and physicians was clearly missing. The decision was made to implement a preclinical and clinical development center in the same location where technology is created. Additionally, there will be a direct functional connection established with the university hospital, which will allow for direct early and continuous communication and synergy with the technology developers. The examples illustrated in this paper clearly demonstrated that the best innovations will

be obtained from technologies which to date did not communicate with medicine.

In CLINATEC, a multidisciplinary preclinical and clinical platform has been implemented devoted to biocompatibility and proof-of-concept demonstration. A complete workflow of investigations for clinical proof of concept in the field of medical devices was implemented. One crucial issue is the anticipation of the need for multimodal endpoints in the preclinical investigations to be able to translate them in the clinical trial. The combination of molecular, clinical, histological, and multimodal-imaging endpoints is a guarantee for enhanced preclinical biocompatibility investigation as well as for the early detection of toxicology in the first tested patients. We also integrated a specific “translational technology” unit, involved in packaging, clinical integration and final design of the prototypes.

Biocompatibility will be explored first at the cell level using the cell culture facility. A surgery room will be available, compatible with large animal surgery. The implementation of multimodal investigations will include magnetic resonance imaging, SPECT, Magneto-encephalography, electrophysiology, and photonic explorations as well as a behavior platform. The human platform will be able to translate the preclinical endpoints previously developed and to monitor efficacy and potential side effects of new technologies implanted for the first time in patients. A neurosurgery room will be available and a small 6 beds hospitalization unit. Multimodality is a key objective including the possibility to perform in the same patient MEG, MRI, SPECT or photonic as well as molecular investigations. Implementing this multimodal approach in the surgery room was a challenge warranting many technological developments.

### Conclusion

A major opportunity is emerging in the association between electronics and medicine. It already defined new medical applications and a potential new exponential market for electronics industry. Micronanotechnologies, electronics and industrial procedures not

connected to medicine could be a new inspiration source for medicine. Real breakthrough innovations have been already translated at the bedside, suggesting that electronics medicine could be the next medical revolution. However, crucial prerequisites will have to be addressed for both medical and economical success. 

*François Berger, MD-PhD, director CLINATEC, may be contacted at francois.berger@cea.fr*

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# X-Ray Inspection Techniques to Identify Counterfeit Electronic Components

By Bill Cardoso, Ph.D., [Creative Electron, Inc.]

*“As long as people have been in the business of inventing, others have been in the business of faking their inventions.”<sup>1</sup>*

The success of a global economy relies on the free flow of information and products across multiple geographical boundaries. In a networked society, markets transcend political borders to reach every corner of the globe. With such connectivity come serious challenges to protect one's homeland from foreign and domestic threats. The influx of counterfeit electronic components in the supply chain is an ever-increasing threat to the industry's economy. The latest report issued by the US Department of Commerce states that the number of counterfeit incidents almost tripled between 2005 and 2008.<sup>2</sup> The US is especially vulnerable to the threat of counterfeit electronic components. The task of controlling the influx of products into our 327 ports, with over 10M containers and almost 31M entries every year, is daunting. Moreover, the focus of our homeland security officials is in counterterrorism, border security, readiness against natural disasters, immigration, and cybersecurity. As a result, the more than 50,000 people employed by the Department of Homeland Security are busy looking for different threats to the homeland, and despite recent efforts, the search for counterfeit components is not always on the top of their list.<sup>3</sup> Therefore, it became the responsibility of the microelectronics industry to assure that the supply chain is free of counterfeit electronic components.

The recent escalation of electronic parts counterfeiting on the world stage comes in tandem with a sharp increase in the technical sophistication of this criminal enterprise. This escalation has also increased the demand for

counterfeit detection techniques at each and every point in the supply chain. The resulting paradigm shift has led to a higher aggregated value of the distribution chain. As a result, a suite of inspection techniques has replaced the once appropriate and sufficient visual attribute analysis practiced a decade ago. This article discusses the positives and pitfalls of a powerful inspection technique, and the overall strategy for using it in the identification of counterfeited parts.

Radiography is one of several tools needed in the arsenal against counterfeit components. Among the other techniques include visual inspection, resistance to solvent immersion, decapsulation, X-ray fluorescence (XRF), and electrical testing. None of these techniques alone can tell you that a part is authentic. However, together they create a “line of defense” that can tell you if a component is a suspect counterfeit. In order of effectiveness, the recommendation is to begin with visual inspection, then X-ray, decapsulation, XRF, and if needed, electrical testing.

Other advanced techniques have been explored by Bhanu Sood and include ultrasound, scanning electron microscopy, thermogravimetric analysis, differential scanning calorimetry, and thermo-mechanical analysis.<sup>4</sup> Although not routinely used in the detection of counterfeit components, these advanced techniques have shown to be useful in challenging cases of component authenticity determination.

## Radiography for Counterfeit Detection

Radiography (or X-ray inspection) is a ubiquitous technique to all recent and upcoming counterfeit detection

standards, including IDEA 1010B, CCAP 101, AS5553, AS6081, and AS6171. X-ray inspection gives you the unique ability to “see” what is inside an electronic component without damaging it. To illustrate how X-ray images represent an electronic component, Figure 1a shows a simplified side view diagram of a typical plastic molded part. The top view X-ray of a real plastic molded component is shown in Figure 1b. The dark regions in the X-ray image represent dense areas in the component. Conversely, the light areas represent light areas in the field of view. For this reason the area around the component is represented in white. The X-rays traveling through the different density areas of the component under inspection cast a shadow onto the camera. Thus this X-ray imaging technique is also known as a shadowgram.

A common technique used to identify counterfeit components using X-rays is to utilize an exemplar as a basis of comparison. The

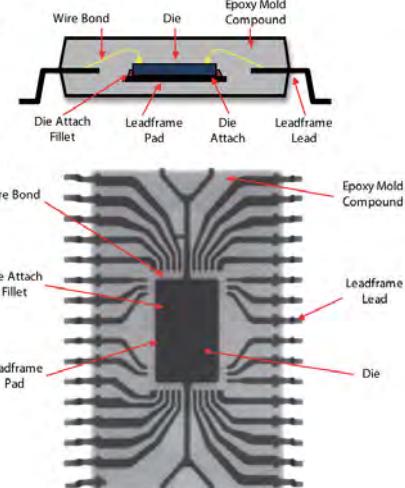


Figure 1a. Cross section (side view) diagram and 1b top view X-ray image of epoxy mold compound encapsulated electronic component

exemplar samples can be obtained in different ways. The usual method includes the comparison to components in previous lots that were obtained from trusted suppliers. In the event that such prior information is not available, the part can be compared to another one currently in use. In this case, it is often necessary to X-ray the printed circuit board with the assembled component. Both options, if available, must be used carefully, as manufacturers can change the leadframe structure, die size, and wire bonding schemes without notice. Therefore, it is imperative for the user to seek more information on the part before judging it a counterfeit suspect.

The major challenge in the determination of a counterfeit component is the usual lack of an exemplar that can be used as a basis of comparison. The most common strategy used in this case to assess the authenticity of an electronic component is to perform the comparison within parts of the same lot (**Figure 2**). This in-lot comparison is powerful because all parts within the lot must be identical. However, often time counterfeitors remark different parts (that do not have identical X-ray images) to fulfill an order. Even if you do have an exemplar available, it is also common to find counterfeit components mixed with good parts. That is the counterfeitors' attempt to circumvent detection by customers doing tests of just a few parts in the lot. For this reason it is imperative to test all parts to assure homogeneity within a lot. Until not long ago testing thousands of components was cost prohibitive. However, recent breakthroughs in the automation of radiography inspection have made it possible to inspect of thousands of parts in trays, tubes, or reels.

## What Are You Looking For?

When looking for counterfeits, the most common things you may find inside the components are:

- **Inconsistent die size** – because the die is a thin piece of silicon, a top view X-ray image will likely not show the die. However, the die-attach fillet (**Figure 1**) is dense enough to appear in a top view X-ray image. As a result, you can determine the die size by measuring the boundaries created by the die-attach fillet. Since counterfeitors often remark different parts to pass as genuine, it is almost inevitable they will mix different components with different die sizes.

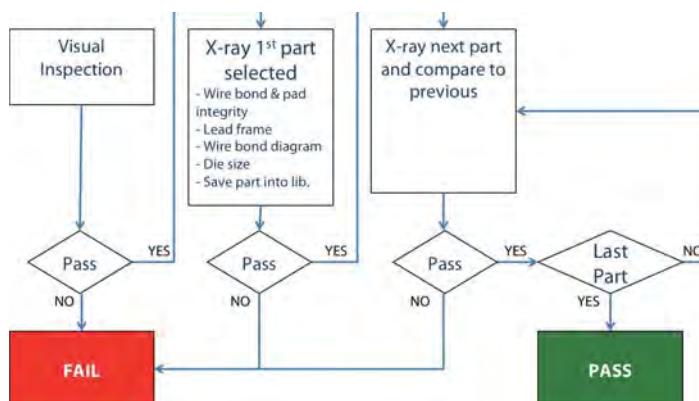
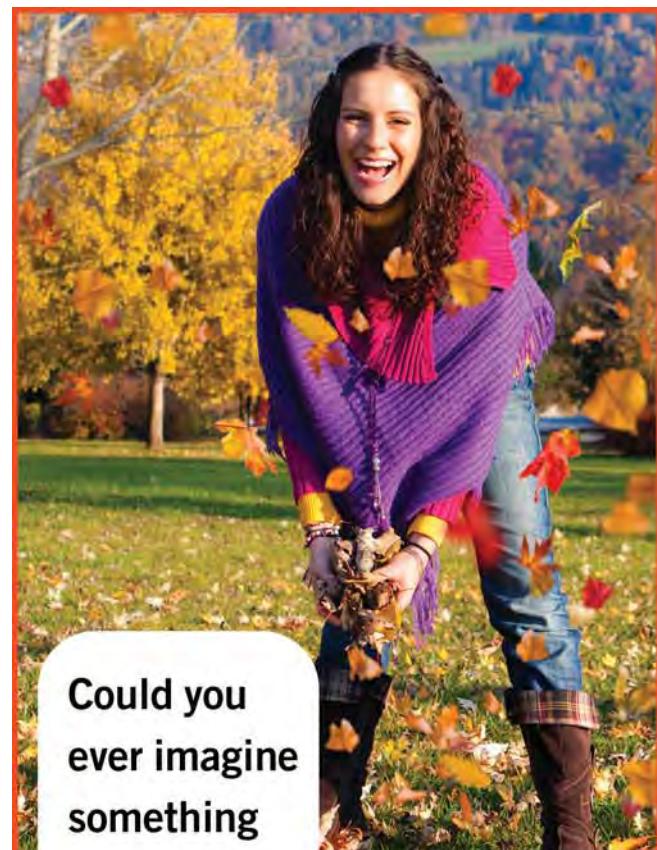


Figure 2. Flow chart diagram on X-ray inspection for component counterfeit detection



**Could you  
ever imagine  
something  
so small  
making  
such a big  
difference?**

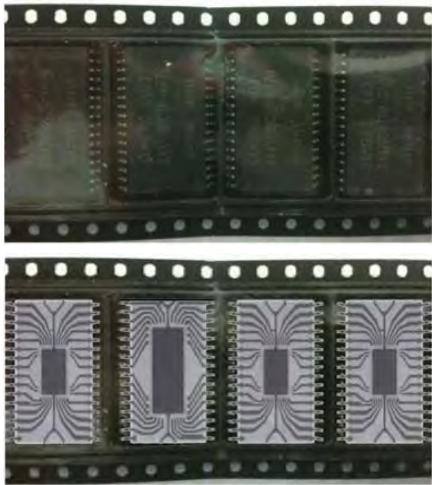


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**Figure 3a.** Photo of a section of the reel, all components show identical part number, date code, and part number, **b)** overlaid X-ray image onto photo showing mixed components

Another technique to verify the size of the die is to take a side view X-ray image of the part. In this case the through density of the die is enough to appear in the X-ray image.

- **Inconsistent leadframe** – Similarly to the previous case, counterfeiters often mix parts with different leadframes in the same lot.
- **Broken or missing wire bonds** – A broken wire bond may be a result of extreme mechanical or thermal stress applied to the part. Similarly, the absence of wire bonds is the sign of a suspect lot of parts. It is very important to note that some parts are packaged with aluminum wire bonds. Since Al is a low-density material, these wire bonds will not show in an X-ray image, whereas gold and copper wire bonds will. In this case, it's important to use decapsulation to confirm that they are not Al wire bonds.
- **Incorrect wire-bonding diagram** – Even if the parts have the same leadframe and die size, the wire-bonding diagram must remain consistent.
- **Missing die** – Although die directly visible, it is important to verify the presence of wire bonds and the die-attach fillet. Examples of empty packages being sold as functioning parts

have been found.

- **Inconsistent die attach voiding** – The mature semiconductor manufacturing process leads to consistent parts. The presence of large variations in the die attach voiding may be a reason to

**Figure 3** shows the X-ray image of a section of a reel of Samsung K6X1008C2D CMOS SRAM with mixed leadframes and die sizes. This is a clear example of a reel where good and bad parts have been mixed together in an attempt to deceive a user doing sample testing of the lot.

### Special Cases

It is critical to be careful assessing the authenticity of an electronic component based on the aforementioned criteria. In some cases, legitimate components with the same part number will have different internal structures. It is necessary, however, that the lot number and/or date code must be different. The following three examples illustrate how good components can end up with different internal structures as seen by the X-ray inspection. In these examples it is assumed the parts analyzed with the X-ray inspection have different lot numbers and/or date codes. Otherwise they should be deemed highly suspect.

- **Different Leadframe Structure:** Market globalization led to the distributed manufacturing of electronic components. Therefore, it is common for original component manufacturers (OCM) to fabricate the same part number in their domestic and international facilities. It is entirely possible that these different locations procure different leadframes due to relationships to their suppliers. It is also possible for a manufacturing plant to change leadframes at a certain point in time based on design and/or supplier changes.

- **Different Die Size:** “Die shrink” is a term often used in the semiconductor industry to refer to the continuous miniaturization of integrated circuits. According to Moore’s Law, the number of transistors in an integrated circuit

doubles every two years.<sup>5</sup> This means that the same circuit can be implemented in a fraction of the size of the previous generation of semiconductors. Thus, die shrink is a natural consequence of the electronics industry evolution. Therefore, it is possible to find legitimate components with different lot numbers, date codes, and die sizes. The wire bonding diagram of these parts is usually the same, but not necessarily always identical.

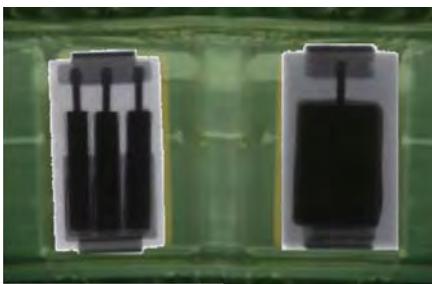
- **Different Wire Bonding Diagram:**

As a consequence of die shrink, the power and signal characteristics of different generations of the same component can change. For example, it is possible that the earlier generation of a part needed more power to bias larger transistors. Thus, the multiple wire bonds needed to carry the necessary current to bias an earlier version of the die may not be necessary for the lower power later versions of the same circuit.

The determination of a component’s authenticity should not be done lightly. If the X-ray inspection shows that parts have different die sizes and/or leadframe structures and the same date code and/or lot number, you can discard them as highly suspect. However, if the date codes and lot numbers are different, it does not mean they are authentic. Rather, this situation requires more research to verify the authenticity of the parts under scrutiny. Organizations that provide the community with invaluable knowledge on counterfeit components include ERAI ([www.erai.com](http://www.erai.com)), IDEA ([www.idofea.org](http://www.idofea.org)), and CTI ([www.cti-us.com](http://www.cti-us.com)).

### Passive Components

Recent shortages of passive components, namely capacitors, inductors, and resistors led to a substantial increase of their market value. A higher market value is a larger incentive for counterfeiters to enter the market. Passive components, especially surface mount devices, are particularly easy to counterfeit. Low tolerance parts



**Figure 4.** X-ray images of tantalum capacitors overlaid onto photograph of reel of parts

can be substituted by a lower cost part with the same value. For example, a 1% 47nF capacitor can be replaced by a lower cost 20% 47nF capacitor. Furthermore, these parts often do not have markings or any other types of mechanical differentiators. In some cases, however, radiography can be very useful. **Figure 4** shows the X-ray image of a reel of tantalum low EST capacitors. In this example the X-ray image of the individual capacitors was overlaid on top of the optical image of the same parts. The inconsistency of the X-ray images, despite the identical markings on the top of the parts, clearly shows the presence of counterfeited parts.

### The Need for Speed

The recent trend towards 100% component inspection organically led to the development of automated systems that can inspect large numbers of parts in a short period of time. Fast and efficient X-ray inspection is needed to balance the economics of companies that need to verify the authenticity of thousands of parts per day. The automation efforts are described here in two fronts: hardware and software.

### Reel-to-Reel and Conveyor Belt Systems

Electronic components are packaged



**Figure 5.** TruView Touch: X-ray inspection with embedded Reel-to-Reel TURBO and Conveyor Belt systems

in reels, tubes, and trays of parts. For this reason the system shown in **Figure 5** is equipped with a reel-to-reel system that automatically feeds the reel of components through the X-ray system to automatically inspect every part in the tape. Similarly, the conveyor belt system feeds trays and tubes of components so that the X-ray image of every part can be taken. An embedded parts counter is included to allow the user to identify

the suspect parts and recover them from the reel after the X-ray inspection is completed.

### SMART

The Standalone Multiple Anomaly Recognition Technique (SMART) is a software tool originally designed to assist operators in the detection of contraband in cargo containers in the operating real world environment. This



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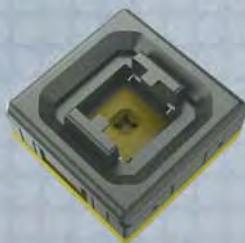


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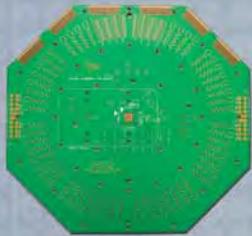


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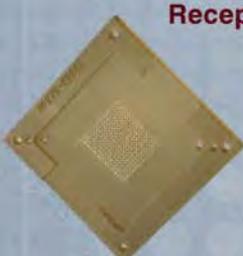


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anomaly recognition technique relies on the use of sub-band decomposition of the radiographic image to establish the parameters in the consistent content region(s) of the



component that provide a baseline for anomaly detection. Based on this information, SMART scans the consistent image region (or the entire component) for anomalies. These anomalies are detected by SMART as deviations in the energy content in the sub-band decomposition of the image. SMART measures deviations from the most common shape in the image using a frequency decomposition approach. Thus, SMART intrinsically filters the images in the frequency domain.

## The Inspection Outcome: Breaking the Counterfeit Components Economics

It is well known that counterfeiters operate a lucrative criminal enterprise. The following two real life examples attempt to put numbers to assess the scale of this illegal industry. The reports shown describe the total amount of parts inspected within each lot, the total inspection time using a TruView 180-3 HD equipped with a Reel-to-Reel TURBO system. The monetary value indicated quantifies the potential loss when selling or buying such parts.\*

### Kemet Tantalum Low ESR Capacitors

Total number of parts inspected: 2,149

Inspection time: 15 minutes

Cost per part: \$6.44

Total potential loss: \$13,840

### Samsung K6X1008C2D CMOS SRAM

Total number of parts inspected: 3,000

Inspection time: 19 minutes

Cost per part: \$31.52

Total potential loss: \$94,560

\*The cost per part included in this analysis reflects the prices quoted to the author by different distributors at the time this paper was being written. EP

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- [5] Gordon Moore, co-founder of Intel Corporation, [www.intel.com](http://www.intel.com)

Bill Cardoso, Ph.D., President Creative Electron, Inc. may be contacted at [bcardoso@creativeelectron.com](mailto:bcardoso@creativeelectron.com)

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Sonoscan Inc. 2149 E. Pratt Blvd. Elk Grove Village, IL 60007 Tel: +1-847-437-6400 www.sonoscan.com			3D PR MP - 610 mm WFR, PKG, SUB, PCB
SUSS MicroTec Inc. 228 Suss Drive Waterbury Center, VT 05677 Tel: +1-802-244-5181 www.suss.com	(X,Y,Z) - CM PR, NP MP - 300 mm WFR (BONDED)		
Takaoka Electric Manufacturing Co., Ltd. 8-1, Akashi-cho, Chuo-ku Tokyo 104-0044, Japan Tel: +81-3-6371-5000 www.takaoka.co.jp	2D, 3D PR MP - 300 mm WFR, SUB		
Teradyne, Assembly Test Division 700 Riverpark Drive North Reading, MA 01864 Tel: +1-978-370-2700 www.teradyne.com/atd		2D, 3D PR, NP MP - 450+ mm PKG, SUB, PCB	
Test Research 7F No 45 Dexing W Road, Shilin District Taipei City 11158 Taiwan Tel: +886-2-2832-8918 www.tri.com.tw	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Tohken Co., Ltd. Odakyu-Daiichi Seimei Bldg. 10F 2-7-1 Nishi Shinjuku, Shinjuku-ku Tokyo 163-0710, Japan Tel: +81-3-5325-4315 www.tohken.co.jp		2D, 3D PR MP - 400 mm WFR, PKG, SUB, PCB	
Topcon 3D Inspection Laboratories Inc. 19501 Clark Graham, Suite 300 Baie d'Urfé, Quebec, Canada H9X 3T1 Tel: +1-514-695-0112 www.topcon3d.ca	2D, 3D PR MP - 300 mm WFR, PKG		
Toray Engineering Co., Ltd. Nihonbashi Muromachi Bldg. 3-16, Nihonbashi-Hongokucho 3-chome, Chuo-ku Tokyo 103-0021, Japan Tel: +81-3-3241-1541 www.toray-eng.com	3D PR MP - 300 mm WFR		

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COMPANY HEADQUARTERS	OPTICAL INSPECTION	X-RAY INSPECTION	ACOUSTIC INSPECTION
Company Street Address City, State, Country Telephone Website	2D - 2 Dimension ( X,Y ) 3D - 3 Dimension ( X,Y,Z ) PR - Programmable NP - Non-Programmable MP - Max Product Size CM - Contact Manufacturer	2D - 2 Dimension ( X,Y ) 3D - 3 Dimension ( X,Y,Z ) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer	2D - 2 Dimension ( X,Y ) 3D - 3 Dimension ( X,Y,Z ) PR - Programmable NP - Non Programmable MP - Max Product Size CM - Contact Manufacturer
	Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board	Product Type Applications WFR - Wafer PKG - Package SDP - Solder Paste SUB - Substrate PCB - PC Board
Ultrasonic Sciences Ltd. Unit 4, Springlakes Ind. Estate, Deadbrook Lane Aldershot, Hampshire, UK, GU12 4UH England Tel: +44-1252-350550 <a href="http://www.ultrasonic-sciences.co.uk">www.ultrasonic-sciences.co.uk</a>			3D PR MP - 630 mm WFR, PKG, SUB, PCB
VI Technology Espace Gavanière, Rue de Rochepleine Saint-Egrève 38120, France Tel: +33-4-7675-8565 <a href="http://www.vitechnology.com">www.vitechnology.com</a>	2D, 3D PR MP - 600+ mm SDP, PKG, SUB, PCB		
View Micro Metrology 1711 W. 17th Street. Tempe, AZ 85281 Tel: +1-480-295-3150 <a href="http://www.viewmm.com">www.viewmm.com</a>	2D, 3D PR, NP MP - 300+ mm SDP, PKG, SUB, PCB		
Viscom Inc. 1775 Breckinridge Parkway, Ste. 500 Duluth, GA 30096 Tel: +1-678-966-9835 <a href="http://www.viscom.com">www.viscom.com</a>	2D, 3D PR, NP MP - 500+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
ViTrox Technologies Sdn. Bhd. No. 85-A, Lintang Bayan Lepas 11 Bayan Lepas Industrial Park, Phase 4 11900 Bayan Lepas, Penang, Malaysia Tel: +60-4-646-6227 <a href="http://www.vitrox.com">www.vitrox.com</a>	2D, 3D PR, NP MP - 762 mm SDP, PKG, SUB, PCB	3D PR MP - 609 mm WFR, PKG, SUB, PCB	
VJ Electronix Inc. 234 Taylor Street Littleton, MA 01460 Tel: +1-978-486-4777 <a href="http://www.vjt.com">www.vjt.com</a>		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Xradia Inc. 5052 Commercial Circle Concord, CA 94520 Tel: +1-925-288-1228 <a href="http://www.xradia.com">www.xradia.com</a>		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
YXLON Int'l Inc. (COMET Group ) 3400 Gilcrest Road Akron, OH 44260 Tel: +1-330-798-4800 <a href="http://www.yxlon.com">www.yxlon.com</a>		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Zygo Corporation Laurel Brook Road Middlefield, CT 06455 Tel: +1-860-347-8506 <a href="http://www.zygo.com">www.zygo.com</a>	2D, 3D PR, NP MP - CM SDP, PKG, SUB, PCB		



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## Europe's OSAT Takes the Stage

By Chip Scale Review Staff



Armando Tavares

There's been an ongoing effort in the European semiconductor market to maintain a full supply chain within the EU especially when it comes to 3D integration and packaging, which is expected to require full collaboration across the ecosystem. As many of the top outsourced semiconductor assembly and test services (OSATS) are headquartered outside of Europe, fulfilling that goal has been a bit of a challenge. In June, at the CEA Leti Annual Review in Grenoble, Mark Scannell, Program Manager at CEA Leti, commented that middle of the line processes for 3D integration has yet to be identified. "Why not in Europe?" he queried. "There's a packaging house right here in Portugal." He was referring to NANIUM, a now independent company, formerly part of Qimonda. Chip Scale Review decided to interview the President of Executive Board of NANIUM, Mr. Armando Tavares, to find out more about this company, its mission, goals, and technology roadmap in next-generation advanced packaging markets.

**CSR:** While NANIUM has been in existence since 1996, it's maintained a relatively quiet presence in the global semiconductor industry. Could you explain a little bit about how it started?

**Tavares:** NANIUM was established in February 2010 as an independent company under the ownership of the two largest privately owned Portuguese banks and the Portuguese state (Figure 1).



Figure 1. NANIUM Facilities in Vila do Conde, Portugal

However, the company already has 15 years' experience in the demanding semiconductor market. We began working for large IDMs in 1996 as Siemens Semiconductors. The site followed the spinoff of the group into Infineon Technologies (1999) and subsequently into Qimonda (2006). We have clean-room area of 20.600 m<sup>2</sup> (222.000 ft<sup>2</sup>) for development, manufacturing and labs. Until early 2009, the company was running high volume production assembly and test of memory components. Consequent to the Qimonda insolvency in Germany, we adopted a new approach to the market and restructured our activities. Currently, we have around 450 employees and we are leading-edge in fan-out wafer level packaging (WLP) technologies.

**CSR:** Since NANIUM became independent, how has its strategic alignment and overall mindset changed with regards to restructuring?

**Tavares:** NANIUM performed an exhaustive study of the market to identify opportunities, the right business offer as well as business model under the boundary conditions of

being located in Europe. In response to market demands and based on our key strengths, our mainstream became WLP. We also extended our capabilities in producing more complex leadframe and substrate-based components. The new products are typically less commodity, inherently lower and midsize volume but higher value. In addition to production itself, we also entered intensively in engineering services, providing package design and development, test program development, fast quality prototyping and lab services to our customers. In summary, we are in the transition phase from a high volume memory packaging and test facility to becoming an OSAT with a wide package and service portfolio.

**CSR:** How successful has this transition been so far? Who are the customers of NANIUM?

**Tavares:** I would say that we are on the right path. The extension of our service portfolio to engineering, prototyping, small, medium and high-volume manufacturing is bringing us different types of customers, large IDMs, small and mid-size enterprises, fabless companies, design houses, IP companies, either already established in the market or startups. NANIUM is not only a service provider. We add value to our customer e.g. through business partnerships and joint developments, for example with INTEL and Tessera Technologies / Invensas.

One market trend we foresee is the increasing demand in WLP for single die and system-in-package (SiP) applications. With our 12"



Figure 2. NANIUM's WLP production Line

WLP capability and volume capacity, we are well prepared to strategically position ourselves in this market (**Figure 2**). We have a continuously increasing worldwide customer base including those in France, Germany, Israel, Russia, US, Japan, China and Taiwan. We have requests for products with higher complexity, requiring a system approach and co-design capabilities, innovation and creativity. Dealing with complexity is one of our strengths, which we are continuously developing.

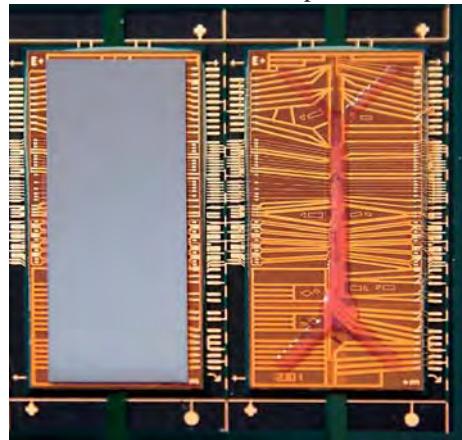
**CSR: Has NANIUM been affected by Portugal's current financial situation?**

**Tavares:** The current situation is for sure a huge challenge for our country. But it is at the same time an opportunity for the companies in Portugal, in particular those exporting their products and services. NANIUM is exporting almost 100% of its services; this is beneficial for our company and for the country, since it contributes to strengthen our economy. Each crisis requires special efforts and deep commitment to overcome. We are used to work globally, and we know it is always necessary to strive for competitiveness and sustainability in business. Our company is prepared for this challenge.

**CSR: As one of the few OSATS in Europe, how does NANIUM remain cost competitive with the major OSATS located in Asia and the US?**

**Tavares:** With competitive labor costs, Portugal's geographic location assures a good proximity to customers based in Europe and USA both in terms of flying time as well as time zone. Also being within EU, Portugal has highly efficient customs with short cycle-times, in addition to political stability and a high degree of intellectual protection. The site itself is strategically positioned, close to an international airport and to a deep sea-harbor, and with quick access to the country's main highways. Its facilities allow for secure environments to be set-up and customized for leading edge products according to the client's needs. Furthermore, NANIUM has a sound IT communications infrastructure, which can provide remote access/ interface

applications by customers to equipment in-house. A differentiating factor making us competitive is also our focus on wafer level packaging and more complex packages and system solutions, as SiP and multichip



**Figure 3.** SDRAM chips with RDL and spacer for multichip package

packages (MCP) like stacked die packages (**Figure 3**).

**CSR: Europe offers a rich environment for collaborative research and development in the semiconductor market, including assembly, packaging and test. How does NANIUM participate in this?**

**Tavares:** NANIUM is in discussion with most of the major European institutes in the field of semiconductor research like Fraunhofer in Germany, CEA Leti in France and Imec in Belgium. Locally, we have co-operation protocols with the major Portuguese universities. With them we run joint development projects and help develop their students to become our potential future experts.

And we are active not only in Europe. We just signed a membership agreement with 3D Systems Packaging Research Center of the Georgia Institute of Technology (Georgia Tech) joining forces to enable Chip-Last embedding commercialization. In addition, we are active members of several associations like SEMI, ESIA and just recently Silicon Saxony.

In addition, we have a strong focus on collaborations with notable customers from all over the world to develop new technologies for their products, for instance the development framework with INTEL next generation fan-out WLP (eWLB).

**CSR: What would you say is NANIUM's position with regards to Mark Scannell's suggestion that NANIUM take on the middle of the line processes for 2.5D, 3D integration, and heterogeneous packaging?**

**Tavares:** NANIUM is serving the "More than Moore" domain of heterogeneous integration of different functionalities in packages with increasing pin count but at the same time decreasing form factor, SiP on package level and in near future also on wafer level. Our technology roadmap does currently not foresee in-house 3D through silicon via (TSV) and manufacturing of 2.5D interposer. However, we support our customer also in these fields through partnerships with companies specialized in TSV manufacturing.

As one of the providers of fan-out WLP (Wafer Level Packaging) solutions for single die and SiP (System-in-Package), NANIUM currently utilizes chip-first embedding in a reconstituted wafer approach. This technology is already qualified and in volume production for 12" reconstituted wafer. It allows an alternative offering to TSV. The so-called through package vias (TPV) is a good solution for many applications. The customer does not need to design TSV in his product, saves chip area, keeps more design flexibility and can use the same chip in different packages.

Another 3D integration technology NANIUM is working on together with 3D Systems Packaging Research Center of Georgia Institute of Technology is chip embedding in substrate. The incorporation of the embedded MEMS, actives and passives (EMAP) chip-last embedding

advancements will allow the extension of NANIUM's fan-out technology portfolio to SiP solutions for new applications and markets, including interposers. This is expanding NANIUM offerings, which can benefit from chip-last over chip-first approaches.

**CSR:** *NANIUM's legacy core competency is in DRAM assembly, packaging and test. Does the company intend to enter the 3D TSV race to build Wide I/O DRAM on Logic?*



Figure 4. Component Assembly Lines

**Tavares:** We are still running packaging and test for memory products (Figure 4). Our company is use to work on the more complex and diversified SDRAM products like those for graphics high speed solutions, game consoles as well as consumer and mobile products. Our expertise in package design,

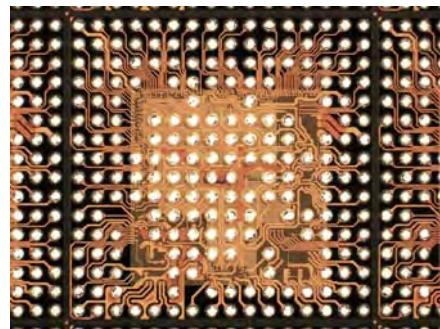
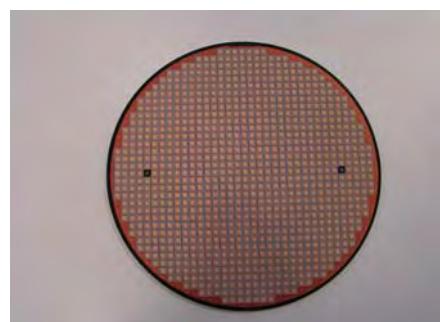


Figure 5. NANIUM 12" eWLB Wafer and final Component before singulation

package development, test program development, product engineering and high quality production at high yield and competitive price in this business area is still requested in the market.

We are running several projects with leading memory design and IP houses as well as manufacturers to create

(continued on page 56)

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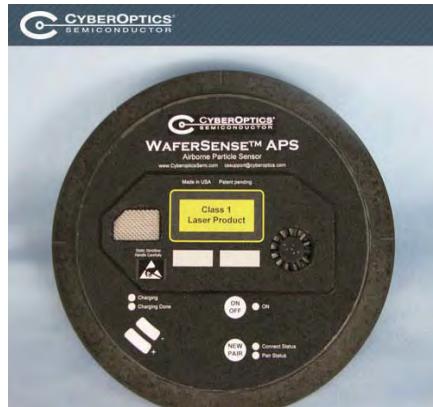
The XD7600NT100HP from Nordson DAGE is said to offer groundbreaking 100nm (0.1μm) feature recognition for finite analysis of the most challenging inspection applications. The XD7600NT100HP combines the digital acquisition technology of the Nordson DAGE XiDAT 3.0 imaging system with Nordson DAGE's ImageWizard software. Dual monitor



configuration allows operators to view the X-ray image on a 24" widescreen LCD monitor while at the same time providing the location of faults on a highly detailed, full screen display of the X-ray navigation map of the sample on the second LCD display. The system is available with a proprietary high-power NT tube that retains sub-micron feature recognition at full power. The XD7600NT100HP can be equipped with computerized tomography (CT) option providing 3D modeling and volumetric measurement of solder joints, ideally suited for analytical investigation of solder interconnections for critical applications such as stacked die, MEMS, package-in-package and package-on-package. [[www.nordsondage.com](http://www.nordsondage.com)]

## Airborne Particle Sensor

The Airborne Particle Sensor (APS) from CyberOptics is part of the WaferSense family of semiconductor sensors. It validates and analyzes wafer contamination in real time and moves through semiconductor process equipment to monitor airborne particles, reporting information in real-time to allow engineers to efficiently



validate wafer contamination. Positioned to reduce and/or replace handheld and bench-top particle counters, the APS can identify particles under actual varying wafer conditions in tool and report data in real-time to validate and analyze particle contamination. Available in 200mm and 300mm form factors, the APS can go deep inside a tool without the need for partitioning required by monitor wafers to isolate the source of the particle contamination. [[www.cyberopticssemi.com](http://www.cyberopticssemi.com)]

## Automated Optical Inspection

The high speed FX SL AOI inspection system for populated printed circuit boards, from Nordson YESTECH offers accelerated throughput at over twice the inspection speed of previous generation systems without sacrificing defect coverage and extremely low false failure rate. The FX SL saves valuable inspection time, reportedly delivering high speed automated inspection of solder and lead defects, component presence and



position, correct part, polarity and through-hole parts. This AOI system features YESTECH's Advanced Fusion Lighting™ and 5 megapixel image processing technology, including color inspection, normalized correlation and rule-based algorithms. The full inspection program can be completed in less than one hour, including solder inspection. The system is well suited for both high-volume or high mix manufacturing environments. It utilizes a standard package library to simplify training and insure program portability across manufacturing lines. [[www.nordsonyestech.com](http://www.nordsonyestech.com)]

## 3D Imaging and Analysis

The Versa 3D™ DualBeam™ system, from FEI company, provides high-resolution, three-dimensional (3D) imaging and analysis on a wide range of sample types. The Versa 3D's configurable platform allows customers to adapt the system's capabilities to their specific requirements. Low vacuum electron imaging capabilities allows the system to accommodate contaminating or out gassing samples that are incompatible with high vacuum operation. Low vacuum also provides the ability to compensate for charge build up in non conductive samples



even at the high currents required for analysis techniques, such as energy dispersive (x-ray) spectroscopy (EDS) and electron backscatter diffraction (EBSD). New features, such as FEI's SmartSCAN™ and Drift Corrected

Frame Integration (DCFI), facilitate electron beam imaging of sample types with a range of different properties. Advanced backscattered electron, as well as secondary electron and ion detectors, collect a wide variety

of topographic, elemental and compositional information "from every angle." The Versa 3D addresses the diverse needs in materials research, life sciences, electronics and geosciences. [\[www.fei.com\]](http://www.fei.com)

(continued from Page 14)

directors since 1986. Myers announced his plans to retire in April and the SEMI International Board of Directors subsequently initiated a globally comprehensive search process.

"The markets and customers our membership serves are at very exciting points in their evolution. Finding the right individual — one who embodies the characteristics of leadership, integrity and a dedication to member service that were so apparent in Stan — as well as the proven ability to lead the evolution

of SEMI to its next stage, has been the major goal of the Executive Committee of SEMI with the support of the entire International Board of Directors. We are pleased to announce the appointment of Denny McGuirk to this role," said SEMI Board Chairman and ATMI Chairman, president and CEO Doug Neugold.

McGuirk served for 12 years as the president and chief executive officer of IPC – Association Connecting Electronics Industries, a global trade association, based in Bannockburn,

Ill. Previous to IPC, McGuirk was executive director of the National Fluid Power Association and also served in various positions with the National Rifle Association of America. He also served for 24 years in the United States Air Force, attaining the rank of Colonel.

McGuirk graduated from the United States Air Force Academy in 1969 with a Bachelor of Science in Western European Affairs. He Holds a Master degree in Public Administration from the University of Colorado.

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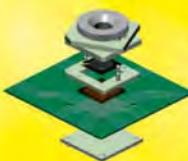
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packaging solutions for higher memory density and higher speed using mature conventional assembly technologies. This avoids the need of still very expensive 3D TSV and 2.5D interposer application for these products.

**CSR: Looking forward, what is on NANIUM's technology roadmap? What is the company's overall mission?**

**Tavares:** The company's overall mission can be summarized in three words: NANIUM goes OSAT. We strive for excellence and want to assure sustainable success. Our technology roadmap is characterized by the technology diversification from a pure memory

assembly and test volume backend to an OSAT with a much wider technology offering and service portfolio.

Our main focus is clearly on WLP (fan-out and fan-in). In fan-out WLP we are working with 12" wafer size, which is challenging for many process steps, but the efforts pay back in reduced cost per component (Figure 5). A comprehensive development program is in place to develop additional features for this technology. Most of them are initiated by customer requests.

Second priority was set on substrate based complex SiP solutions like multichip packages, stacked die, and

side-by-side die solutions or even combination of both and several types of hybrid assembly. Integration of more functionality on less space is key in this area. Special solutions for improved electrical and thermal performance are mandatory to achieve this target.

Our aim is to provide high quality services and add value to our customers and shareholders, while continuing to be cost competitive. With our highly qualified, competent and motivated team and state-of-the-art facilities and equipment, we are ready to provide services beyond the client's expectations. 

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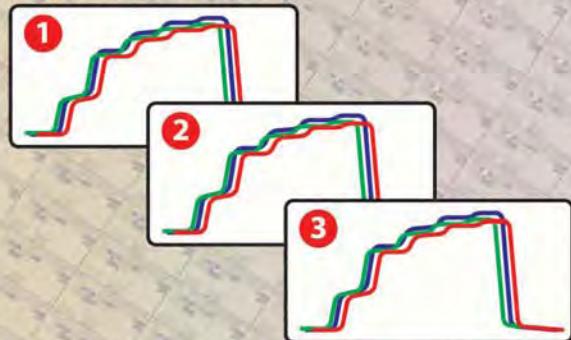
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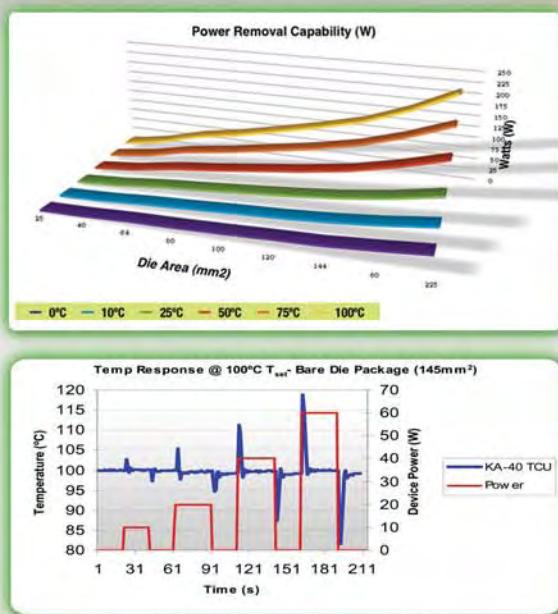
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