

ChipScale Review®

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Volume 21, Number 1

The Future of Semiconductor Packaging

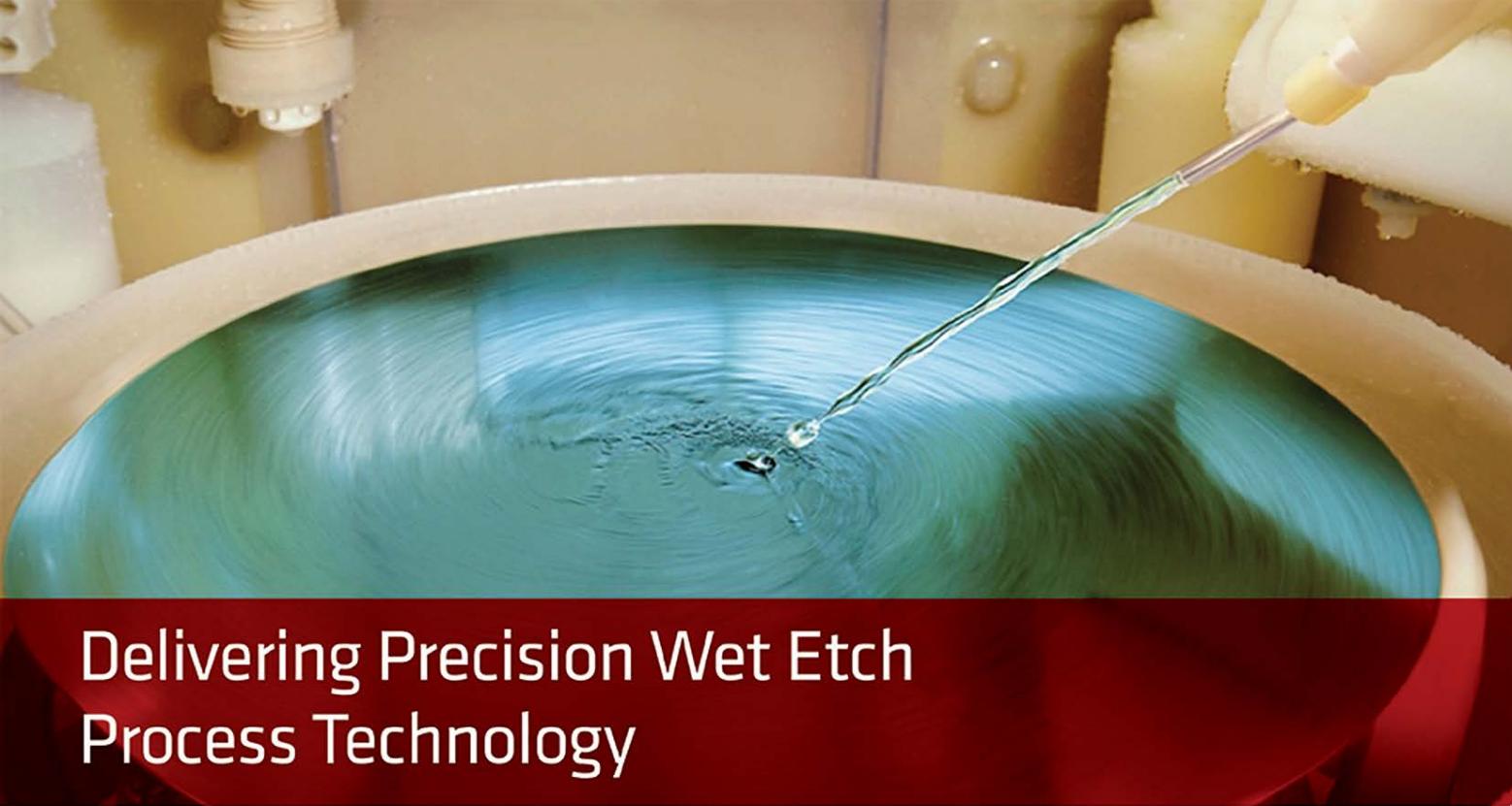
January • February 2017

Future of packaging with silicon photonics

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- Cu pillars for 3D stacking
- FOWLP technology trends
- High frequency test sockets
- Electronic assembly reliability
- Electroplating for packaging applications
- Package integration drives RF test complexity
- Using feed-forward metrology to improve stepper throughput





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The cover shows two different optoelectronic interconnection methods developed to enable photon and electron conversion at the level of the microelectronic (logic) chip. Parallelized optical fibers (front) and lithographically-defined compliant polymer waveguides (behind) carry data in optical form to/from the IC. The flip-chip bumps on each die form the electrical connections to the package substrate. As optoelectronic conversion moves closer to the chip, improved data transfer speeds, bandwidth and power efficiencies are expected.

Cover image courtesy of IBM Corporation

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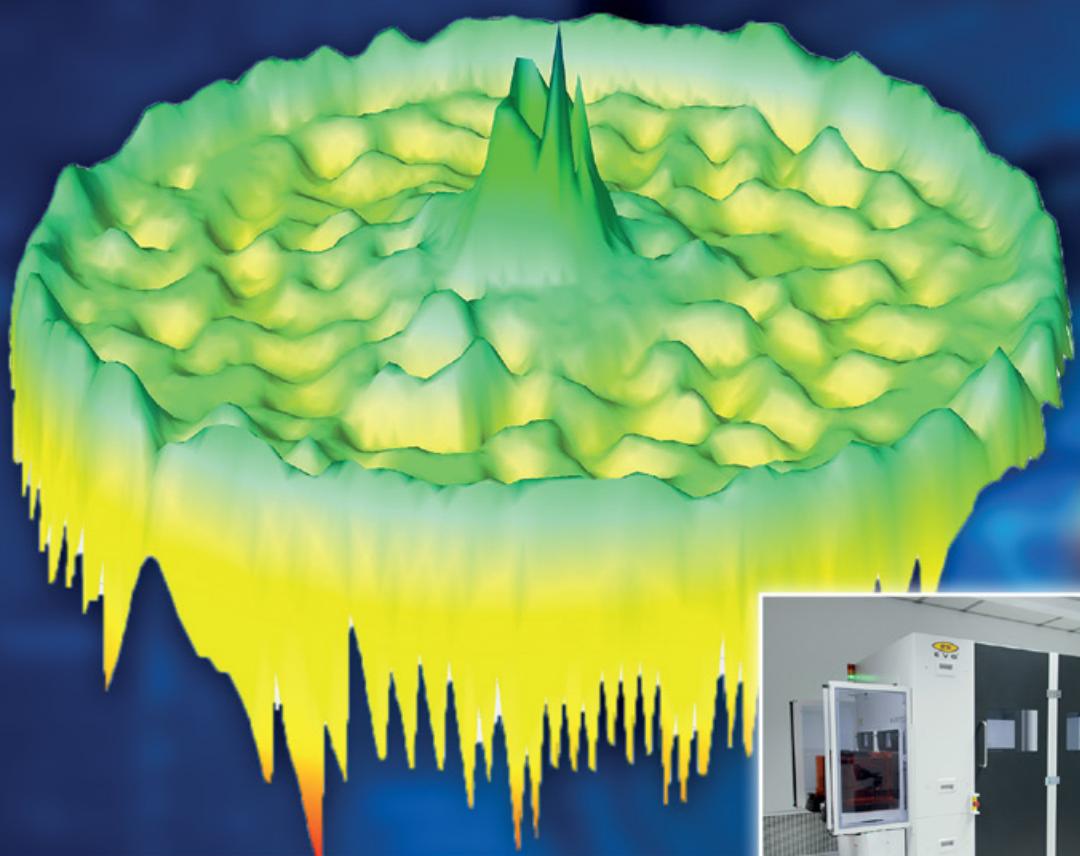
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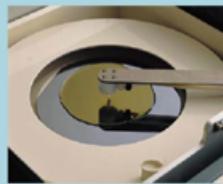
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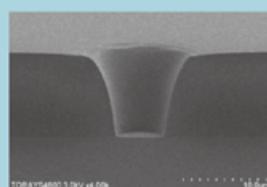
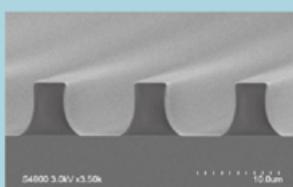
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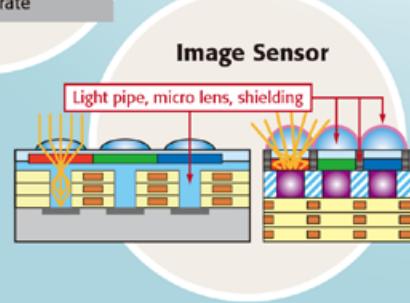
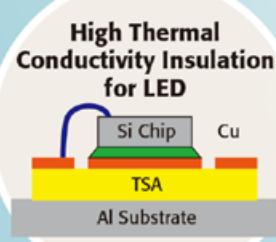
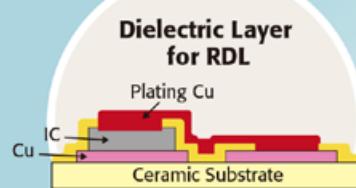
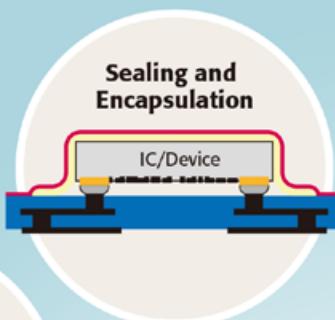
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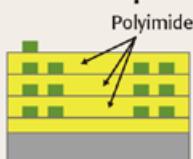
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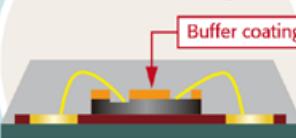
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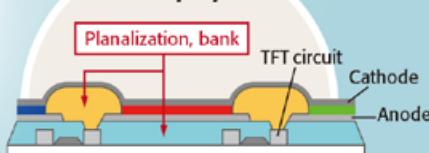
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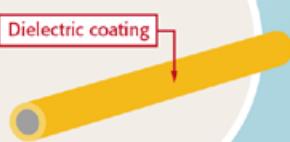
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Technology and economic considerations for panel-level fan-out packaging

By Choon Lee, Tom Bondur, Manish Ranjan *[Lam Research]*

The era of “More than Moore” has extended to the packaging world. Packaging plays a critical role in improving electrical and thermal performance and power consumption. Recently developed packaging technologies such as high-density wafer-level fan-out (WLFO) have gained increased attention as a way to meet performance and form factor requirements in the semiconductor market. To ensure broad adoption for this packaging technology, several foundry and outsourced semiconductor assembly and test (OSAT) companies are considering the use of larger panel size substrates. This article will discuss some of the cost motivation and performance challenges associated with the use of panel substrates for fan-out wafer-level packaging.

Today, packaging is enabling advances in consumer electronics such as smartphones by enabling more transistors on a smaller area. For example, in the iPhone 7, the Apple applications processor has around 150% more transistors even though the chip has increased by only 20%. For reference, the chip has approximately 3.3 billion transistors in a chip with an area of 125mm².

This latest generation of applications processors is manufactured using a technology called “integrated fan-out,” which is based on high-density WLFO. Several key building blocks for this packaging technology include multiple redistribution layers and mega pillars to support the package-on-package (PoP) structure. Packaging innovations include the use of mega pillars with 200μm diameter and 200μm height instead of a through-mold via (TMV) for a typical PoP structure. Furthermore, the top-level memory package height was reduced using a side-by-side arrangement of LPDDR4 memories (instead of conventional memory die stacking), and the impressive

introduction of 0.3mm ball pitch for the first time in memory history. Lastly, this technology introduction eliminated the use of flip-chip substrates, thereby enabling a reduction in overall package height. At the 2016 ICEP conference in Sapporo, Japan, Google demonstrated the advantages associated with the combination of application processor and memory in a planar layout to boost memory performance and reduce power usage. It is evident that the use of packaging technology for enabling next-generation system-level performance is gaining increased focus from several top-tier semiconductor device and fabless suppliers.

Form factor drives WLFO

In applications requiring advanced silicon node technology, the chips will generally shrink, which, in turn, pushes the package transformation from fan-in wafer-level chip-scale package (WLCSP) to WLFO to accommodate the routing of higher pin counts. In analog products for mobile applications, conventional lead frame and/or polymer-based packages have often been converted to WLCSP or WLFO on account of form factor and manufacturing cost considerations. Today, there are a variety of companies, including Xiaomi, IMC, Qualcomm, and PMIC, commercializing WLFO packaging. These companies are producing a variety of packaging sizes from 3mm to 15mm to meet device packaging requirements. Typical package sizes for WLFO range from 3mm x 3mm to 10mm x 10mm for low- to mid-range devices, while package size for leading-edge semiconductor chips can exceed 15 x 15mm.

Why is this conversion happening? Popular smartphones are constrained to a certain size, but battery capacity, and consequently battery size, are getting bigger. This means that the remaining motherboard area allotted for chips has

remained unchanged, yet consumers are demanding more novel smartphone functionality. Disruptive packaging technologies are critical to saving space and meeting consumer demand for higher performing devices.

Beyond smartphones, wafer-level fan-out packaging is being used in the automotive market to help enable active safety systems such as blind spot detection and radar modules. NXP, Freescale and Infineon have demonstrated their products and/or prototypes in the market for advanced driver assistance systems (ADAS), all using a 10mm package size or smaller.

Cost benefit drives PLFO

The primary motivation for panel-level packaging schemes such as panel-level fan-out (PLFO) is more die in a larger area format for cost advantages. In contrast to the 300mm diameter wafers used in WLP, the conventional panel sizes in panel-level fan-out are large—approximately 3 times larger than wafers, which creates huge opportunities for economy of scale. In the case of substrate packages, assembly houses are working with the substrate suppliers who run the panels as starting format and supply strips singulated from the panels to the assembly houses. Strips are used because much of the manufacturing infrastructure developed for conventional packaging handle strips of various sizes. For example, wire bonders and flip-chip bonders can handle a maximum of 100x300mm strip size. As well known in the packaging industry, the material contribution of the substrate comprises approximately 30% to 60+% of the entire packaging cost, therefore reducing substrate cost plays a large role in reducing overall cost. That is why OSATS and integrated device manufacturing (IDM) packaging groups are keenly taking a look at the bigger panel processing.

Table 1 shows the total numbers of units the panel and the wafer can produce per each package size. As seen in **Figure 1**, one single-batch processing for a panel can produce almost 3 times as many units as for a wafer, from which one can make a natural guess of cost saving. How much exact savings can be achieved using the panel over the wafer is still in discussion [1].

Approaches for panel-level fan-out manufacturing

Panel-level fan-out manufacturing can be categorized in two different types. One uses the current infrastructure of substrate manufacturing, which is based on a printed circuit board (PCB) approach. This approach involves adding extra equipment such as pick-and-place, panel mold tools, grinder, and others. The second type is a thin-film approach [2, 3]. It involves modifying wafer processing tools to accommodate rectangular panels rather than circular wafers. For example, the manufacturer would define new tool configurations for lithography, sputtering, plating, imaging, and etching equipment for rectangular panels [4]. One advantage of the former approach is that it makes use of a currently installed line, which minimizes the capital investment. However, it has process technology limitations for meeting fine-pitch and feature requirements. The second type has an advantage of having wafer processing equivalent accuracy and technology, but its disadvantage is the capex investment and technology immaturity of applying wafer (circle) processing to panel (rectangular) processing. Both approaches have common challenges, which can result in yield loss during the various manufacturing processes.

Despite the complexities mentioned, there is a simple comparison of panel versus wafer capacity analysis as shown in **Table 2**. As the table shows, panel-based solutions could produce nearly three times the number of package units, making a compelling case for panel-based solutions. To meet the demand scenario shown in **Table 2**, a capex investment of ~\$200M will be needed for panel fan-out equipment, while a capex investment of ~\$400M will be needed for the capacity of WLFO. The market price for a 7x7mm

package is conservatively around 20+ cents, which, in turn, results in the revenue of \$280M. Hence, there is potential opportunity to make a profitable return on investment in a short time period.

It should be mentioned that the process risk factors are not considered in this calculation. However panel-level processing can possibly build upon the infrastructure developed during the last decade for fan-out technology. TSMC's InFO, for example, demonstrates a monumental milestone for a new paradigm of packaging technology in terms of getting rid of substrate, proximate system integration of chip-to-packaging and "real" fab-like backend manufacturing infrastructure.

Summary

From the cost standpoint, panel-level fan-out (PLFO) is a viable concept and feasible. Even though it is currently in the development stage, thin-film based PLFO will probably enter volume production during the next few years. Due to technical challenges, it may be initially applicable to products requiring only a single redistribution layer. Once the equipment infrastructure matures, panel-level fan-out processing may be extended to applications that require multi-layer redistribution. In the foreseeable future, WLFO will be extended to multi-die applications using finer line and space capability to support further integration of packaging. We are seeing the embryonic era of the fan-out market, which can hopefully be another driving force in leading mobile, as well as automotive and computing markets.

References

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Packaging size (mm)	# of packaging per wafer (units)	# of packaging per panel (units)
5 x 5	2,500	6,752
7 x 7	1,268	3,528
10 x 10	612	1,652

Table 1: Comparison of the total number of units that can be processed by panel-level processing or wafer-level processing.



Figure 1: Area comparison of a wafer vs. a panel.

	Wafer-Based Solution	Panel-Based Solution
Package Units Per Panel or Wafer	1,268	3,528
Yearly Number of Panels or Wafers	1.1 M wafers / year	400k panels / year
Required Panels or Wafers Per Month	92K wafers / month	33k panels / month

Table 2: Needed capacity of panel vs. wafer processing assuming 1.48 units/year for a 7x7mm package.

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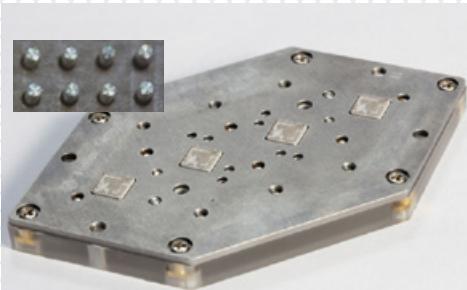
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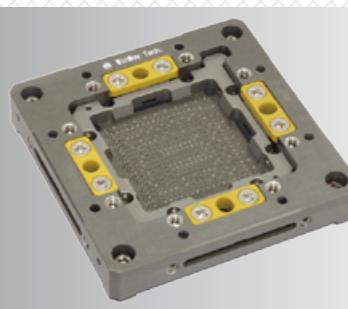
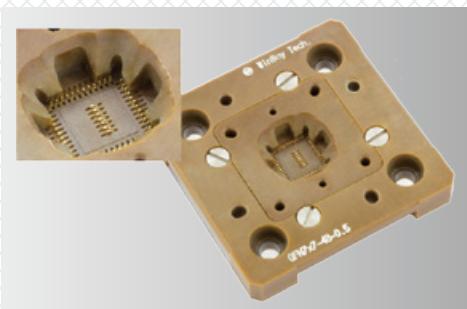
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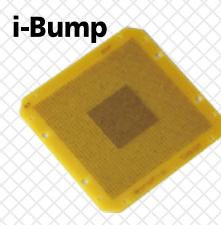
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GUEST EDITORIAL



Data center O/Ils could pave the way for the photonic-in-package era

By Eric Mounier, Thibault Buisson [Yole Développement]

Today, every photonics event worldwide has a session or workshop dedicated to silicon photonics (SiPh). The topic has been increasing in popularity for years, and people talking about it have been either skeptical or enthusiastic. For optics veterans who were involved in fiber-optic telecom activities in the 2000s and thus are cautious about such things, SiPh could represent either a rebirth of optical technologies to cope with the coming bandwidth bottleneck, or another game of smoke and mirrors, with business expectations far beyond the real market need. We have been tracking SiPh for years and this year, Yole Développement (Yole) published the third edition of its silicon photonics market and applications report [1].

Silicon photonics: at the tipping point

SiPh has been under development for years to overcome technical challenges (something in which Intel is well versed), and there are still only a few products on the market. But today, this technology is being pushed hard by large webcom companies like Facebook and Microsoft. Indeed, if we look at investments from the top 5 cloud providers (GOOGL, FB, AAPL, AMZN and MSFT) and compare them to the top 5 service providers (T, VZ, S, TMUS and CTL), it is likely that total investments from the former will exceed investments from the latter two or three years from now, to the tune of more than US\$50 billion

a year [2]. Driven by exponential data growth, both industries are investing, but cloud providers are becoming a threat to “traditional” service providers. Large webcoms are progressively taking control of the game in the photonics industry—not only in data centers but also in metro, and possibly for the long haul.

Where does that leave SiPh?

The answer is quite simple: silicon photonics is a short-term answer to interconnect bottlenecks in data centers. But that's not all: it is also a promising technology platform for other applications, such as medical applications and sensors. As the technology matures, it will open up

possibilities for applications that for years have been perceived as “blue sky research,” for example, quantum computing.

SiPh offers all the advantages of silicon technology, including low costs, higher integration, more embedded functionalities and higher interconnect density, but lower power consumption and better reliability compared with legacy optics. At a recent OFC event, Facebook created a lot of buzz by requiring a “\$1/GB” target for future data centers; a simple calculation shows we are at \$5/GB today. But what is the current status of the technology? Back in 2000, during the fiber-optics telecom bubble disaster, Bookham was the first to commercialize SiPh components,

The photonics supply chain is 20 - 30 years behind the IC supply chain*

(Source: Silicon Photonics for Data Centers & Other Applications 2016 report, Yole Développement, October 2016)

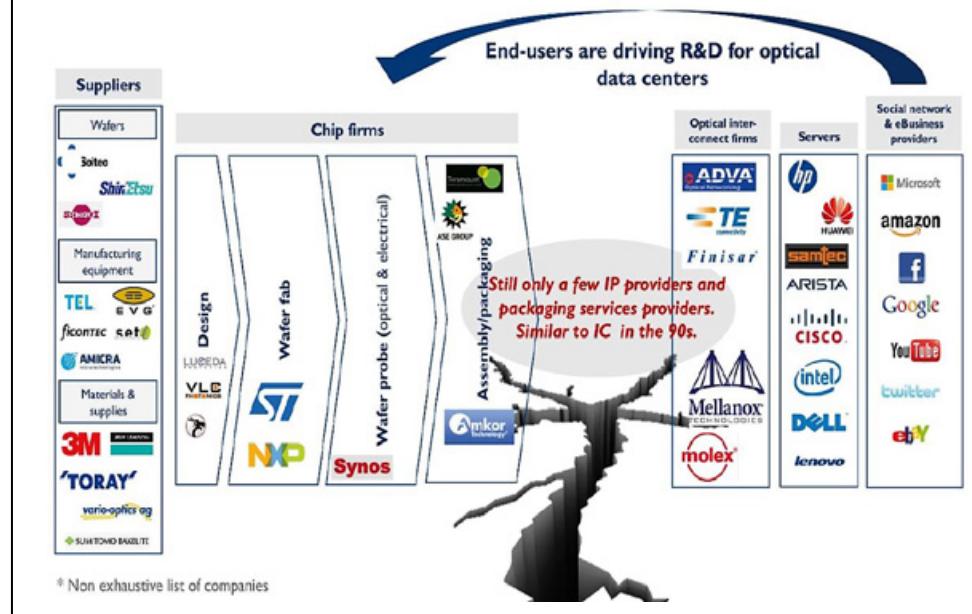


Figure 1: The photonics supply chain is 20-30 years behind the IC supply chain. SOURCE: [4]

including arrayed waveguide grating (AWG), and transceivers [3]. Then in 2006, variable optical attenuators (VOA) were commercialized by Kotura, which has since been acquired by Mellanox.

Today, the number of companies shipping SiPh products has increased with Luxtera, Kotura/Mellanox, Cisco/Lightwire, Intel, Acacia and STMicroelectronics. We are also seeing new startups and more and more products reaching the market, mostly for 100GB, but soon for 400GB. The rise of startups in the field is also a very encouraging sign of growing investments from the venture capital (VC) community—and we all know how tough a domain photonics is for any startup.

According to our research, today's chip market value is small: estimates were less than US\$40 million in 2015. But analysts believe it holds great promise, with a market value of US\$1.5 billion in 2025 for chips, and more than US\$6 billion in 2025 for transceivers [3].

The horizon, however, is not so clear, as there are still challenges to overcome:

- Laser source integration and competition with vertical cavity surface emitting lasers (VCSELs) (actually SiPh's best bet in the 500m–2km range);
- The photonics supply chain has yet to be formed, with possible opportunities for outsourced semiconductor assembly and test suppliers (OSATS) and the emergence of SiPh foundries (**Figure 1**); and
- As always in optics: packaging and assembly.

Compared to semiconductors, where packaging accounts for 10% of the final die cost, packaging and assembly is generally 80-90% for a photonic die [4]. Fiber alignment, thermal management and non-standardization mostly account for the large percentage.

Though SiPh has the advantage of an integrated circuit's (IC) infrastructure, function integration, low manufacturing cost and high density, packaging still contributes to a large portion of the cost.

Will the game end here?

First off, SiPh uses silicon as the medium for optical signals, allowing much faster digital signaling than is currently possible with traditional electron-based semiconductor devices. It is a disruptive technology meant to achieve a new breed of monolithic optoelectronic devices for a potentially low-cost Si process, with the ultimate goal of delivering optical connectivity everywhere, from the network level to chip-to-chip. As SiPh evolves and chips become more sophisticated, Yole expects to see the technology used more often in processing tasks, such as for interconnecting multiple cores in processor chips to boost access to shared cache and buses. As more and more bandwidth will be required in data centers (representing 75% of total data flow), the technology will be necessary for 100GB and 400GB.

Secondly, silicon photonics is a mix of several technical blocks: optical, IC for processing, MEMS for packaging, copper pillars, through-silicon vias (TSVs) and more. Advanced packaging developments, such as interposers, copper pillars and TSVs (used as light guides and no longer as electrical interconnects), could be the solution to more integrated chips. In terms of fiber connections, there is also a clear need for technology to move to mass production at a low cost. New technologies for interconnects with integrated optics could be a viable solution. Laser integration also needs to be considered; some companies (including Kaiam, Luxtera and Kotura/Mellanox) have developed very clever laser assembly solutions that will be beneficial in the short term. Other solutions using epi bonding (from Leti, Intel and Aurion) are also viable solutions for the future.

Yole's analysts believe that the growing need for optical interconnects for data centers will pave the way for new developments to achieve lower cost and higher integration. This in turn will accelerate mass-volume production. Innovative approaches will come from developments in the

field of advanced packaging, such as interposers. This could solve the current challenges surrounding heterogeneous integration.

On the business side, Yole sees opportunities for the photonics supply chain to consolidate—the way the IC supply chain has today. In particular, OSATS could play a key role by offering dedicated photonics application services, for example, small packaging houses.

In the end, new packaging and assembly developments will allow more functionalities to be integrated into a single package, similar to what we are seeing in the industry with the system-in-package (SiP) trend. Are we seeing the rise of the photonic-in-package era? Yole's analysts think so!

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Biographies

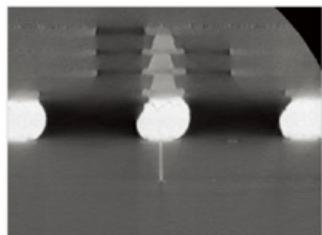
As Sr. Technology & Market Analyst of the MEMS & Sensors team at Yole Développement, Eric Mounier performs numerous technical and market analyses focused on MEMS and sensors, visible and IR imagers, semiconductors, printed electronics and photonics, including silicon photonics; Email: mounier@yole.fr

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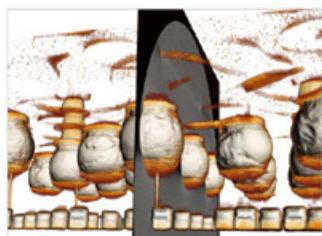
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The future of packaging with silicon photonics

By Deborah Patterson [Patterson Group, LLC]; Isabel De Sousa, Louis-Marie Achard [IBM Canada, Ltd.]

I

t has been almost a decade since the introduction of the iPhone, a device that so successfully blended sleek hardware with an intuitive user interface that it effectively jump-started a global shift in the way we now communicate, socialize, manage our lives and fundamentally interact. Today, smartphones and countless other devices allow us to capture, create and communicate enormous amounts of content. The explosion in data, storage and information distribution is driving extraordinary growth in internet traffic and cloud services. The sidebar entitled, “Trends driving data center growth,” provides an appreciation for the incredible increase in data generation and its continued growth through 2020.

To process and manage the unabated growth in data traffic, silicon photonics will be used to define new data center architectures. This article discusses the impact that silicon photonics will have on data center technology trends, and on the next-generation microelectronic packaging developments that address optical-to-electrical interconnection as photon and electron conversion moves to the level of the package and microelectronic (logic) chip.

Data center dynamics

The large-scale restructuring of data centers is one of the most dynamic transformations taking place in information technology. The need to re-architect the data center is being propelled by the staggering surge in shared and stored data along with an increasing demand to effectively interpret the tremendous amounts of content being generated. In addition to the huge growth in data traffic, the infrastructure supporting the Internet of Everything (IoE) will emphasize real-time responsiveness between people and/or objects. The next wave in data processing and data traffic management will require the ability to support cloud computing, cognitive computing and big data analysis along with the necessary speed and capacity to deliver a timely response.

Optics have traditionally been

employed to transmit data over long distances because light can carry considerably more information content (bits) at faster speeds. Optical transmission becomes more energy efficient as compared to electronic alternatives when the transmission length and bandwidth increase. As the need for higher data transfer speeds at greater baud rate and lower power levels intensifies, the trend is for optics to move closer to the die. Optoelectronic interconnect is now being designed to interface directly to the processor, application specific integrated circuit (ASIC) or field programmable gate array (FPGA) to support switching, transceiver, signal conditioning, and multiplexer/demultiplexer (Mux/Demux) applications.

Figure 1 shows a forecast for silicon photonics adoption through 2025 with data centers dominating initial growth. Silicon photonics are also being developed to support applications as diverse as high-performance computing and optical sensors.

The data center need for speed and capacity. **Figure 2** illustrates forecasted data center traffic by 2019. One of the more notable trends is that almost three-quarters of all data center traffic will originate from within the data center. The recognition of this statistic, compounded by the enormous increase in data traffic, has significantly altered the approach to data center design. Besides upgrading optical

cabling, links and other interconnections, the legacy data center, comprised of many off-the-shelf components, is in the process of a complete overhaul that is leading to significant growth and change in how transmit, receive, and switching functions are handled, especially in terms of next-generation Ethernet speeds. In addition, as 5G ramps, high-speed interconnect between data centers and small cells will also come into play. These roadmaps will fuel multi-fiber waveguide-to-chip interconnect solutions, laser development, and the application of advanced multi-chip packaging within the segment.

The high-end or “Hyperscale” data center is massive in both size and scalability. It provides a single compute architecture made up of small individual servers and

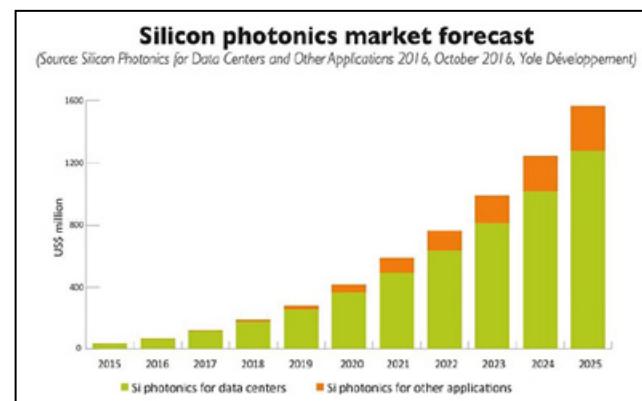


Figure 1: Silicon photonics growth rates will initially be dominated by applications within the data center. SOURCE: Yole Développement, Oct. 2016

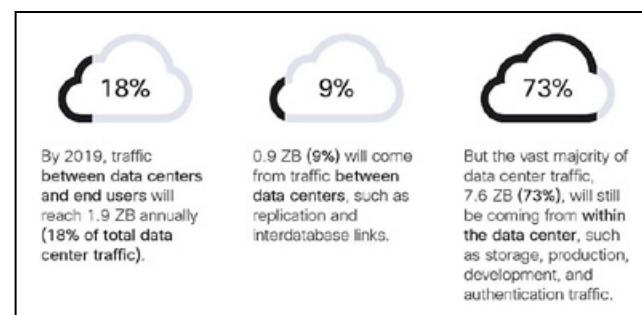


Figure 2: Data center traffic and bit rates show remarkable growth. The vast majority of data center traffic will reside within the data center. SOURCE: Cisco Global Cloud Index, 2014–2019

peripheral functions such as memory, power management, and networking, all woven together through layers of redundant systems. Hyperscale data centers are represented by companies such as Amazon, Microsoft, Google, and Web 2.0 companies like Facebook. They can house over a hundred thousand to a million servers.

Conversely, alternative data center architectures are also under consideration. An example is the build-out of many small data centers linked together through heterogeneous networks. No matter which approach, moving the enormous volume of data within and between data centers will continue to require increased speed and bandwidth with lower latencies and greater power efficiencies. Silicon photonics is positioned to address these fundamental conditions.

Servers will be reconfigured to support higher speeds along with new componenrty at 10 gigabit Ethernet (GbE), 25, 40, 100 and 400GbE. Meanwhile, new standards such as 1TbE will eventually be introduced. **Figure 3** illustrates typical data center connections, nomenclature, Ethernet speeds and link distances.

Because each data center server generation lasts 3-5 years and the infrastructure (buildings) typically lasts 3-5 generations, the technology choices incorporated now will become the legacy infrastructure over the next 10-25 years. Therefore, determining which technologies deliver maximum flexibility, capacity and reduction in total system cost-of-ownership is non-trivial and leading-edge development emphasizing concurrent semiconductor and package design is receiving greater visibility.

Optoelectronic integration of transceivers and switches

Because optics can transport more data at significantly lower power than electronic transmission, the intent is to drive optoelectronic conversion as close to the chip and microelectronic packaging level as possible. The data remains in optical form – leveraging high optical densities – until it enters the package and interfaces with the silicon photonic die. At this point, the data is converted from photonic to electronic format to undergo computation, storage, redirection, etc., by conventional logic ICs. Running electrical and optical pathways side-by-side on a micrometer scale is the eventual objective.

Data centers are being “disaggregated”

so that compute, storage, memory, networking and power conditioning/distribution can be reorganized and redistributed systemically. Signal routing efficiencies, better thermal management, and densification of connections brought forth by well-designed package integration is expected to improve system upgradability, flexibility, and reliability while lowering cost. Silicon photonics will be especially useful in enabling the high communication bandwidth requirements of disaggregated systems.

Transceivers represent the initial high-volume application for silicon photonics as optics migrate as close as possible to the origin of the data. Outside the data center, optical transceivers are used in transport, enterprise, carrier routing and switching markets. Within the data center, transceivers are located with each server and attached to the edge of the board. This arrangement contributes to extra distance between the optical components and the processor. The IBM research team in Yorktown, NY has proposed advanced packaging designs where the silicon photonic die can be integrated directly into the processor module, bypassing today's standard transceiver housings. Integrating the transceiver functions within the silicon photonic die or processor module is an area of concentrated activity.

Ethernet switches, on the other hand, currently rely on electronic interconnect but are another targeted area of silicon photonic interest. This is because data center

architecture is undergoing a fundamental shift away from traditional three-tiered designs to route information. Power consumption and latency have increased as data traffic volumes have surged. This is due to too many “hops” or handoffs when routing data between source and destination (controlled by routers and switches). “Leaf-spine” network architecture is replacing the older tiered approach. The leaf-spine network is controlled by ASIC switches.

A “leaf” is typically the top-of-rack (ToR) switch that links to all servers within a common tower or rack (shown in **Figure 3**). The next layer of switches is represented by the “spine.” The spine is a higher capacity switch (40 or 100 gigabyte per link) that connects to leaf switches (across the server racks), to other spine switches, and to the next level of “Core” switches. This is known as a “flat architecture” and it is implemented through high-capacity ASIC switches. The largest ASICs currently offer 32 x 100GbE ports. ASIC switch capacity and port count dictate the size of the leaf-spine network, e.g., the number of servers that can be linked together. Higher speed ports drive lower bandwidth costs per Gb/s and higher capacity switches drive the total number of links (minimizing the number of data hops, associated latency, and power consumption).

In addition to the electrical domain switching described above, there is significant interest in on-chip switching of the full optical content of fibers

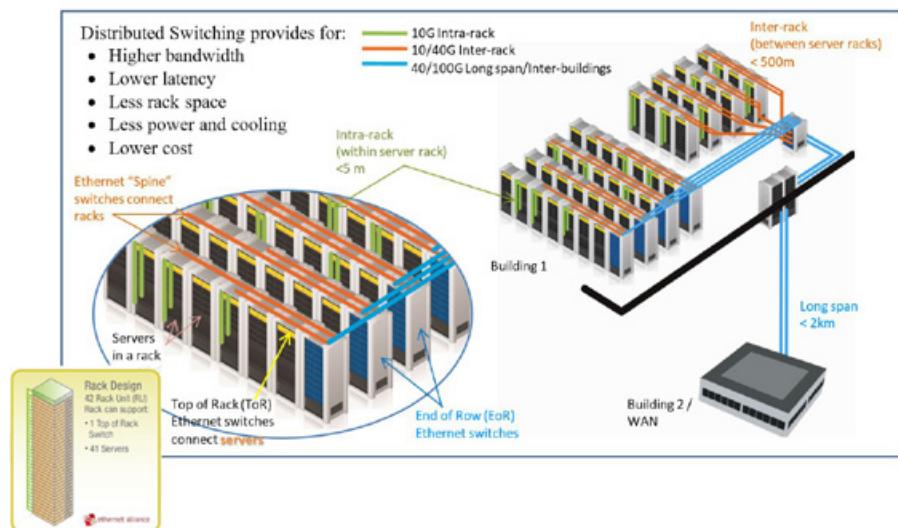


Figure 3: Illustration showing data center connections. The shorter server-to-server connections within the server rack typically require <5m (green) of routing, longer connections between the server racks may require up to 500m (orange), and long span connections within a building or between buildings can measure up to 2km (blue). SOURCE: Image courtesy of Finisar, Patterson Group, LLC, IBM, Ethernet Alliance

Trends driving data center growth

The following information is taken from the 2015 Cisco Global Cloud Index [1] and the Cisco Visual Networking Index: Global Mobile Data Traffic Forecast [2] to provide the reader with an appreciation of what is driving today's explosion in data traffic.

The growth in mobile users has had a phenomenal impact on data traffic. The average smartphone user in 2015 consumed more data in less than a minute than a mobile user in 2000 did in an entire month [3]. Mobile video, which represented 55% of data traffic in 2015, is projected to grow to 75% by 2020. The video forecast becomes even more significant when one realizes that the bit rates required for streaming high-definition and ultra-high definition (4K) video are 2x and 9x faster than standard definition video, further driving the need for both capacity and speed. And this does not even include game changers such as virtual, augmented and mixed reality technologies. In addition to the changes in volume and density of video content, there will be a massive migration of stored data to the cloud. Today, almost three-quarters of stored data on client devices still reside on PCs with integrated hard drives. The expectation is that a majority (51%) of stored data will be associated with non-PC devices with always-on wireless connectivity and no hard drives, propelling consumer cloud storage requirements to 1.6GB per month by 2019. Cloud users will store data (which is archival and may or may not require bandwidth) and will pull/push data from/to the cloud (which requires bandwidth).

Data centers manage both cloud traffic and data center traffic. Cloud computing represents a subset of all data center traffic that exists within and between data centers and end users. Cisco's Global Cloud Index forecasts global cloud traffic to quadruple between 2014 and the end of 2019, from 2.1 to 8.6 zettabytes (ZB). Global data center traffic is projected to grow from 3.4 to 10.4ZB (where a zettabyte is equal to a trillion gigabytes). **Figure S1-1** illustrates the concept of 10.4ZB.

The global forecast of devices and connections track to a 10% CAGR. In comparison, they outpace the CAGRs of the global population (1.1%) and the Internet user rate (6.5%). But that's not all. The Internet of Everything (IoE), described by Cisco as the connection of people, processes,

data and things, may drive data center and cloud traffic growth to over 500ZB annually by 2019 - almost 50 times that of data center traffic alone (10.4ZB). It is assumed that IoE content and applications will increasingly be stored, managed and propagated through the data center, along with a substantial increase in big data analytics that will continue to mature into indispensable tools of strategic and tactical decision making. Future 5G build-out will drive speed and capacity requirements closer to the user with significant reduction in latency (>100x faster than 3G and roughly twice as fast as 4G),

opening the door to interacting in real-time with your environment and people in ways that are only just being imagined.

Figure S1-2 highlights a few examples of the huge increases in devices, their impact on overall Internet and data center traffic and speeds, and the almost four-fold increase in cloud management over the current five-year period. Although the forecast start dates vary from 2014-2016, the story remains consistent. Between the growth of wireless and mobile traffic (which will account for two-thirds of total IP traffic by 2020), social media activity, the progression of video volumes and densities, the ramp of imaging such as embedded vision, virtual/augmented/mixed reality and 3D video, the continued migration to cloud storage, the propagation of sensors feeding the Internet of Everything, and the evolution of big data analytics and cognitive computing, it is clear that the need for speed and capacity growth will continue unabated for a long time to come.



Figure S1-1: Chart illustrating the concept of 10.4ZB. SOURCE: Cisco Global Cloud Index, 2014–2019

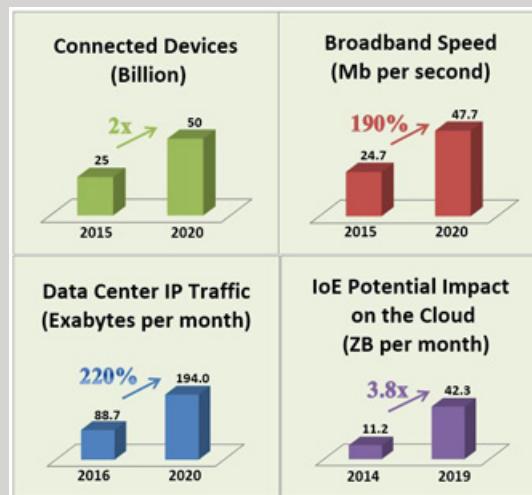
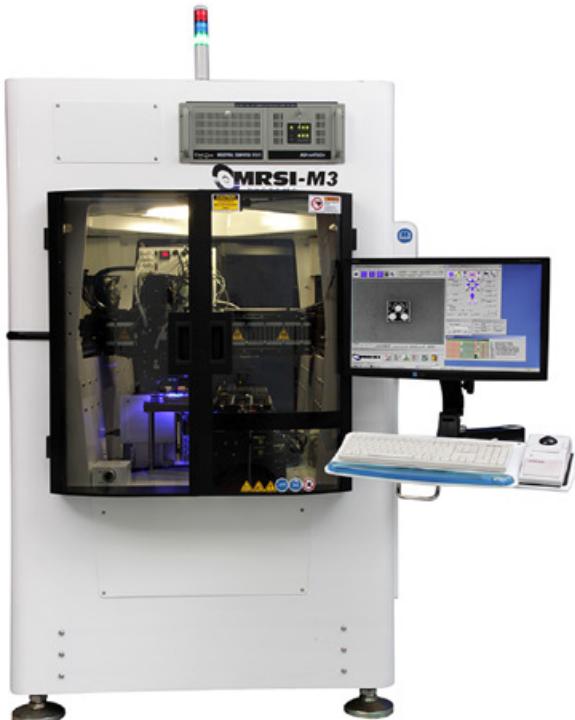


Figure S1-2: Connected devices and their impact on cloud and data center traffic. SOURCE: Data courtesy of Cisco GCI, VNI and IoT White Papers



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without conversion into the electrical domain. Such a fiber optic switching matrix can route tens to hundreds of fibers in, acting as a hub to transmit high-bandwidth optical data while working in tandem with its electronic counterpart.

Advanced packaging with silicon photonic die

In today's data centers, pre-packaged transceivers and other optical modules include discrete, large-pitch components. These traditional "gold boxes" and off-the-shelf components are too expensive for downstream data center proliferation; however, adoption of silicon photonics has the promise of meeting aggressive price targets. Price targets at 100GbE are found between \$1-\$5 per gigabit for single-mode fiber as compared to \$2 per gigabit for multi-mode fiber [1]. It is generally recognized, however, that \$1-\$2 per gigabit for single-mode fiber is necessary in order to achieve widespread impact in datacom (for example, through the enablement of new architectures). It is also understood that silicon photonics and its packaging will need to leverage the know-how, best manufacturing practices, and massive scalability developed for high-volume CMOS manufacturing and microelectronic assembly. This will bring down cost enough to fuel high-volume integration, which in turn, will contribute to driving costs down along traditional semiconductor growth and cost trajectories. Silicon photonics is projected to offer cost-efficient optical interconnects (I/Os), allow for a reduction in components, and reduce assembly and test steps to decrease manufacturing costs while increasing throughput.

Currently, assembly, test, fiber and laser connections – everything except for the silicon chip(s) – are adding prohibitive cost and slowing down deployment. Much of this is due to low-volume fiber-to-die assembly practices and the impact on overall test and manufacturing flows. In order for the cost of silicon photonic assembly and test to meet end-product, design-for-manufacturing cost targets, clever and disruptive packaging approaches that also address the optical I/O (fiber- or waveguide-to-die) and laser-to-die interconnections are required.

A tale of two supply chains

When assembling a silicon photonic package, two specialized providers are typically employed: the semiconductor assembly and test service (SATS) provider

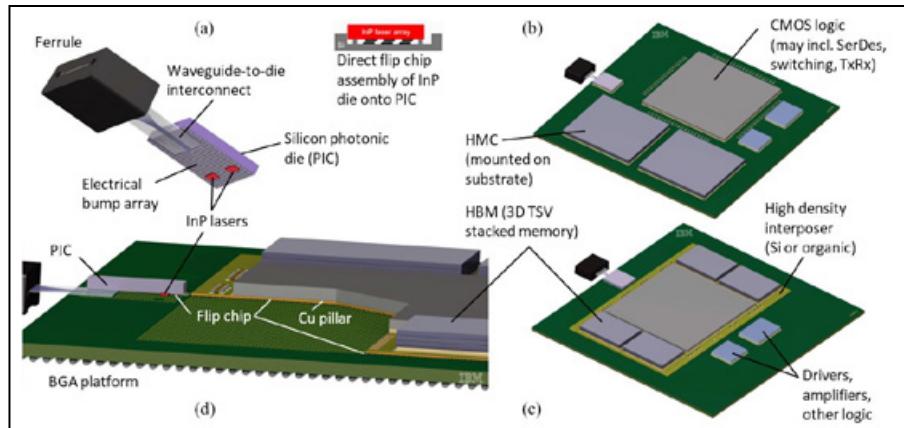


Figure 4: Silicon photonic MCM illustrating (clockwise) a) a photonic integrated circuit (PIC) with flip-chip mounted laser die and edge-coupled waveguide; b) logic, HMC and PIC mounted directly to a BGA substrate; c) logic and HBM mounted on a high-density interposer with copper pillar micro-bumps that enable high-speed connectivity; d) cut-away revealing copper pillar, flip-chip, BGA and optoelectronic interconnections. SOURCE: Image courtesy of IBM Corporation

and the optics contract manufacturer. The core competencies of the SATS and fiber optic assembler are quite different and typically do not overlap. The SATS provider specializes in the assembly and test of the electrical (digital and analog) ICs, passive components and electrical interconnect at the substrate or interposer level, whereas the optics contract manufacturer specializes in interconnecting the photonic IC (PIC) to the optical fibers. The optics contract manufacturer manages fiber and laser alignment at sub-micron levels and also provides specialized optical testing at the package and die level. The end customer/OEM must therefore oversee two separate assembly and test process flows as well as define the build and test plans. It is no surprise that assembly and test strategies may include "known good" multi-chip platforms designed within the optoelectronic module.

Optoelectronic multi-chip modules (MCMs) can contain processors, ASICs, FPGAs, memory, passive components and other functional elements plus the PIC. Certain operations can be integrated on the photonic chip [2] while others will be combined in-package (MCM/SiP). Logic and optical functions can include transmitters, receivers, multiplexers/demultiplexers, modulators, splitters, photodetectors, resonators, optical isolators and polarization controls. Non-optical CMOS amplifiers, drivers, or serializer/deserializer (SerDes) functions may also be located within the module. **Figure 4** illustrates various advanced packaging technologies that can be used to integrate silicon photonic (also known

as "nanophotonic") digital and analog componentry within an optoelectronic package. These modules often require high-density interconnect and a combination of advanced packaging techniques.

Figure 4a shows a next-generation silicon photonic die designed to accommodate a waveguide array that will transport the photons into the die where efficient coupling can take place. The die also contains an array of flip-chip bumps to support electrical signals. In this illustration, laser die are attached to the silicon photonic chip through self-aligning flip-chip bumps that provide a low profile and closely coupled chip-to-laser interconnection. Lasers can also be accommodated off-chip through flip-chip or wire bond attachment.

Figure 4b shows a ball grid array (BGA) substrate with a central logic die such as an ASIC, two hybrid memory cubes (HMC) and associated CMOS devices. A typical HMC is represented by a packaged 4-8 die DRAM stack supported by a controller chip and using 3D TSVs for vertical chip-to-chip connectivity. The packaged HMC has a standard BGA pitch (e.g., 650µm) and is mounted on the substrate along with the other components and PIC. These modules use flip-chip and/or wire bonding for I/O interconnection.

An alternative design is illustrated in **Figures 4c and 4d**. In this case, the logic die and high-bandwidth memory (HBM) stacks are mounted directly onto a high-density interposer to closely link the logic, memory and PIC. It is desirable to have the PIC closely coupled to the logic die using either approach (b or c) to promote power efficiencies. The interposer can be

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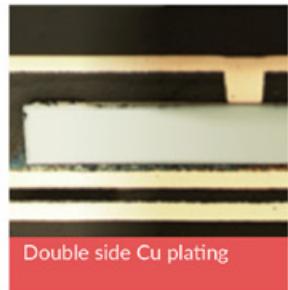
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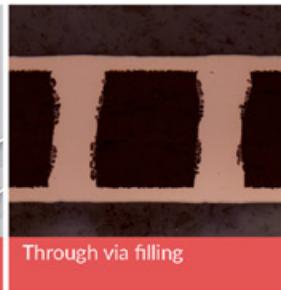
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inorganic (Si) or it can be a high-density organic laminate material. When used as an interposer, these organic high-density interconnect (HDI) materials are sometimes referred to as “2.1D” to differentiate them from 2.5D silicon interposer structures. HDI substrates support dense wireability and flip-chip interconnect at a lower cost than silicon interposers because they are not manufactured in the foundry. With multiple layers, 10 μ m vias, and 2/2 μ m or 3/3 μ m line and space routability, HDI materials can present a cost-effective alternative to 2.5D approaches. In the case of HBM, where a 55 μ m bump pitch is used, HDI material presents a viable option. Populated interposers can also be tested before assembly with the PIC and BGA substrate. Substrates and/or interposers may also contain embedded components, low-loss integrated waveguides, or embedded fiber connectivity.

These complex modules are often larger in area, integrate many material types, and must address significant thermal dissipation and signal integrity considerations. Packaging know-how must not be underestimated and deep experience in electrical and thermal modeling, materials characterization, component choice, vetted design rules, comprehensive test, and design for manufacture is essential. In addition, providers need to address package-level reliability testing in consideration of the photonic components, including features such as fiber strain relief [3].

Signal integrity and thermal dissipation pathways are crucial. For example, to support SerDes operation at 28GHz, the silicon photonic die and SerDes interface – integrated into the logic die and placed in close proximity to the PIC – must be optimized. The optical elements need to be calibrated and balanced against the electrical interface as well. Optical systems reduce/eliminate the need for signal conditioning and amplification steps that would be required for systems with long electrical traces. It is also important to mitigate hot spots on the ICs and the thermal drift that some optical components experience.

Silicon photonics programs at their most effective are designed with a system-level integration mindset. Therefore, concurrent package design for the PIC and the electrical and thermal elements within the module are considered together. Development must include a) silicon photonic die design, b) parallel waveguide

interconnect technology, c) chip-to-waveguide (fiber) assembly processes, d) overall thermal management, and e) final integration between the logic components and photonic IC using various assembly techniques. The build strategy will depend on the type of advanced packaging employed (and at what level higher density flows are designed into the module), the test complexity, yields for both the optical and electrical process flows, and overall cost tradeoffs. A provider that offers assembly of the electrical/thermal elements plus integration of next-generation chip-to-fiber interconnects would be a welcome addition to the packaging landscape.

Demonstrating silicon photonic “firsts”

IBM has been developing CMOS integrated silicon photonic die and packaging approaches for close to fifteen years. **Figure 5a** shows a photograph of the first CMOS integrated coarse wavelength multiplexed silicon photonics chip. This silicon photonics reference design, demonstrated in 2015, is capable of transmitting and receiving 4 wavelength channels – each operating at 25Gb/s. The chip combines both mixed signal electronic circuits and optical capability on a single die. The die was manufactured through the former IBM Microelectronics Division, now a part of GLOBALFOUNDRIES, whose monolithically integrated silicon photonics technology (called CMOS9WG) was used. It is derived from their 90nm CMOS process, a mature technology node that can facilitate commercialization. The design was simulated and fully verified with a process design kit (PDK) integrated with industry-standard CMOS

design tools. The die contains modulators, germanium photodetectors, and ultra-compact wavelength division multiplexers (WDM). **Figure 5b** shows the die with an array of 100 μ m Pb-free flip-chip bumps on a 200 μ m pitch. The flip-chip interconnects keep electrical I/O loss to a minimum. **Figure 5c** identifies the transmitter and receiver elements along with their eye diagrams, showing a clean, high-quality response.

In this design (**Figure 5**), the lasers are manufactured separately and connected off-chip with the optical signals coming into the die through the top four laser ports. The chip contains four receive and four transmit channels, each capable of transmitting data at 25Gb/s via independent wavelengths. The four carrier signals (λ) are bundled into 100Gb/s fiber ports through wavelength multiplexing. An extension of this design would allow for up to twelve such fiber ports when using a standard 12-fiber connector, thereby enabling 600Gb/s bi-directional data rates from a single optical transceiver. The intention of the program was to push 100Gb/s data speeds over a range of up to 2 kilometers (1.24 miles) as required by large data center environments [4].

Note that the die in **Figure 5** is designed with only two optical I/Os representing a single input fiber and output fiber. Currently, duplex fiber connections represent the lowest cost and most widely used approach. One fiber in and one out have been sufficient to support current bandwidth needs. Because of the low I/O count, active optical alignment is often employed and involves assembly in a manual or partially automated fashion using specialized tooling. The result is a lower throughput, limited

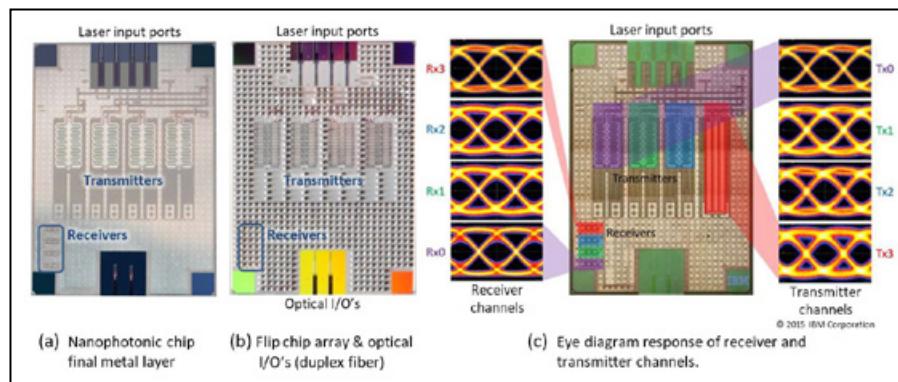


Figure 5: An IBM silicon (nanophotonic) wavelength division multiplexed 4 x 25Gb/s reference design (die) supporting both electrical and optical circuits. Two optical I/Os are seen at the bottom of the die. These connect to optical fibers, one in and one out. SOURCE: Images courtesy of IBM Corporation

scalability, and higher cost process as compared to electrical interconnect and manufacturing operations.

Delivering chip-to-fiber assembly know-how to the semiconductor market is a crucial differentiator required to feed turn-key optoelectronic assembly solutions. IBM's silicon photonics program embraces a disruptive approach that leverages existing high-throughput microelectronic tools and techniques to assemble cost-efficient and scalable single-mode optical inputs and outputs that can be deployed in high volume.

Multi-waveguide to chip interconnect

To keep up with data traffic growth, both software and hardware strategies are utilized. Among these are the migration from the duplex fiber connections described in the previous section to multi-fiber or multi-waveguide interconnects (ideally leveraging industry standard 12-fiber connectors). The following sections identify data rate trends, techniques and trade-offs utilized to support these trends, a 12-fiber interconnection approach demonstrating the feasibility of automating fiber-to-chip assembly, and a next-generation multi-waveguide polymer structure created through lithographic patterning for high-throughput assembly.

Riding the wave of data rate progression. In order to carry greater amounts of optical data, the optical port density and optical bandwidth per port must increase, along with higher manufacturing throughput and scalability. Technology development to intercept downstream requirements is being pursued now. The bit rates (speeds) are trending as follows:

- Within the server rack (intra-rack): 10GbE → 25GbE → 40GbE → 100GbE → 400GbE (finalizing standardization);
- Between server racks (inter-rack): 40GbE → 100GbE → 400GbE (finalizing standardization); and
- Within the data center or between buildings (inter-data center or “long haul”): 100GbE → 400GbE → 1TbE/1.6TbE (standardization remains to be determined).

Figure 6 highlights the unabated rise in data center revenue as broken down by data rate through 100GbE.

400GbE bit rates are now being

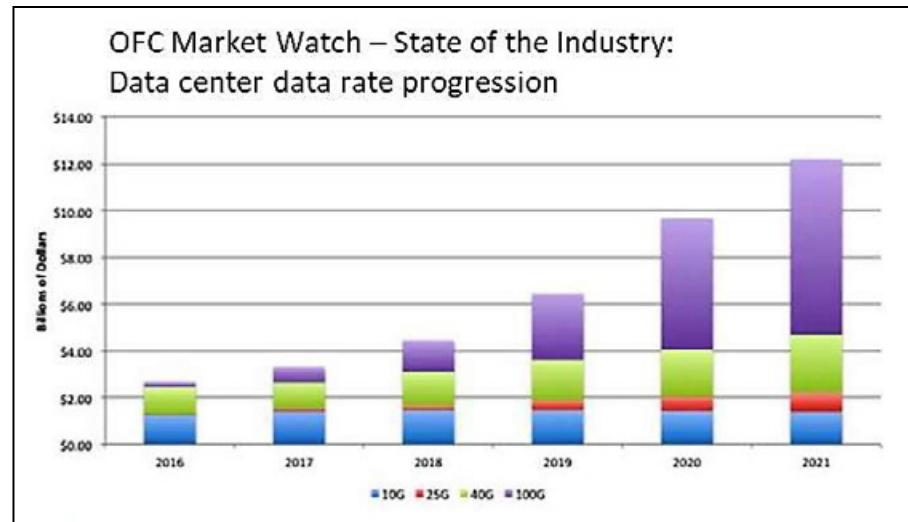


Figure 6: a) Data centers remain a dynamic multi-billion dollar market feeding a progression of high-speed data rates.
SOURCE: Data Center Optics, Discerning Analytics presentation, OSA Industry Development Association, OFC May 2016

standardized for 2018 introduction and it's not just for long haul distances. It will also be used at distances below 100 meters to manage intra- and inter-rack data traffic. The sidebar entitled, “Techniques to extend data rates,” describes various ways to mix and match technologies using next-generation 400Gb/s Ethernet as an example. The number of data lanes (fibers) into and out of the die depends on the application. A single one in/one out port count is used today for fiber links in excess of 500 meters while up to eight (4 transmit/4 receive) fiber connections are used for 100-500 meter core applications such as Parallel Single Mode 4 (PSM-4) in support of 100Gb/s (standard) and 400Gb/s Ethernet (proposed) [5]. Emerging applications such as communication hubs and on-chip fiber switches [6] can require port counts of tens of fibers per chip. 2016 saw a significant shift toward 100GbE components. The development and introduction of complex packaging and optical interconnects to lower 100GbE costs and support next-generation 400GbE is timely.

Adding more chip-to-fiber connections can substantially expand bandwidth and capacity by providing a platform upon which the techniques listed in **Table S2-1** (sidebar) can be deployed. This leap in data will carry forward for several generations to support 100GbE → 400GbE → 1TbE+ roadmap progression. Aggressive cost goals (<\$1 per attachment [7]) must be met to justify mass adoption.

Therefore, practical, high-volume chip-to-fiber assembly techniques are an area of current concentration.

Bridging legacy infrastructure with next-generation electronics. The 12x1 mechanical transfer (MT) interface is a single-mode fiber standard that has been handed down from the telecom industry. Single-mode fiber has been employed because of its high efficiency in guiding light over long distances with very low loss. Single-mode fiber is preferred over multi-mode fiber and is becoming a de facto standard within several areas of next-generation data center designs.

An automated, self-aligned 12-fiber connection to a silicon photonic die is examined below. The program leverages semiconductor assembly, tools, and process flow experience. The 12 optical I/O solution is attractive because of the vast deployment of 12-fiber connectors, making it the lowest cost for parallel optical connections per fiber port. This type of connector is used in PSM-4 transceivers for 100Gb/s and is planned for 400Gb/s and beyond. Multiple 12-fiber connectors are anticipated to fulfill the optical I/O needs of communication hubs and on-chip fiber switches. Multiple wavelengths may be used in each fiber for CWDM, creating a large requirement on both the optical bandwidth per fiber connection as well as the number of fiber connections.

Figure 7a shows a 12 I/O silicon photonics demonstration die with a flip-chip array providing the electrical connections. The die supports two

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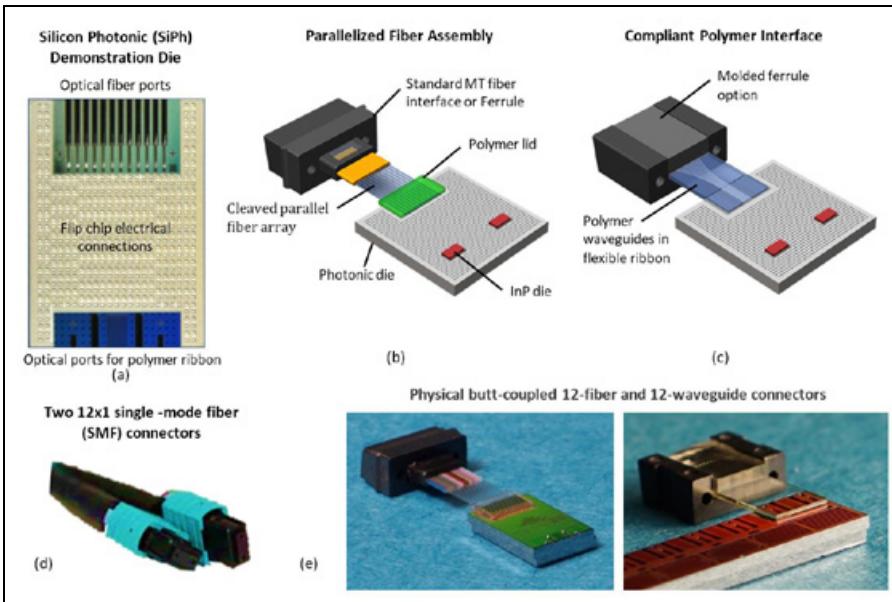


Figure 7: a) IBM silicon photonic die; b) schematic representations of the parallelized fiber and c) compliant polymer ribbon assemblies; d) an industry standard 12x1 single-mode fiber connector; e) photos of the parallelized fiber and compliant polymer structures. SOURCE: Images courtesy of IBM Corporation

next-generation photonic-to-electronic interconnect approaches: twelve fiber inputs or “V-grooves” can be seen on the top area of the die (green) and finer waveguide inputs are clustered on the bottom center of the die (blue). The V-groove represents the physical structure where the light is “butt coupled” – that is, where the fibers terminate into on-chip metamaterial optical mode converters. The finer waveguide inputs correspond to adiabatic optical coupling from a polymer waveguide interface to the chip.

The first approach is called the “parallelized fiber assembly” because a fiber optic ribbon emerging from the MT interface (also referred to as a “ferrule”) is assembled at once to a photonic chip; this is depicted in **Figure 7b**. The design was specifically developed to utilize high-volume pick-and-place equipment (vacuum pick-tip) that can handle the fiber stub.

The second approach illustrated in **Figure 7c** employs a “compliant polymer” interface. In this design, a polymer ribbon with lithographically defined waveguides and self-alignment structures acts as an intermediary between the chip and the standard fiber connector. The polymer ribbon contains finely spaced embedded waveguides that align to both the ferrule and die. The design results in improved thermo-mechanical reliability as compared to rigid connections such as the direct fiber-to-chip attachment (where fiber pistoning or other chip-package interactions can be an issue).

Both approaches offer flip-chip or wire bond electrical connections and support direct, self-aligning InP laser attach to the silicon photonic die. The technology direction depends upon the application. The parallelized fiber approach employs standard components with known reliability and excellent optical fiber transparency. The compliant polymer shows much promise in terms of structural reliability, is reflowable, and is compatible with high-volume manufacturing to support more and varied waveguide pathways. **Figure 7d** shows an industry standard 12x1 single-mode fiber connector that would attach to the other end of the MT fiber interface and **Figure 7e** shows the physical assemblies with 12x1 arrays of optical I/Os.

Automating optical microelectronic assembly. CMOS logic and optical transmit and receive functions need to be closely integrated. Many of today’s chip-to-fiber attachments use vertical diffractive grating couplers as they are typically the easiest coupling scheme to integrate on a wafer. These are defined by the active alignment of fiber(s) that attach at a semi-vertical angle to the face of the photonic die. However, diffractive grating couplers suffer from limited spectral bandwidth, which is generally insufficient for CWDM applications. In addition, they exhibit unattractive coupling efficiency from fiber-to-chip where the two polarizations of light present in the fiber need to be considered. Finally, they emit light almost

vertically from the plane of the chip, which complicates or even negates flip-chip electrical connection and impacts thermal management strategies. With these considerations, in-plane coupling techniques and adiabatic mode converters were pursued instead. These are inherently tolerant to fabrication imperfections, polarization of light and spectral bandwidth.

Two major challenges to mating single-mode optical fibers to silicon photonic waveguides are alignment accuracy and fiber mode conversion [8]:

1. Alignment tolerances between the optical fiber(s) and waveguide couplers embedded within the silicon photonic die should not exceed $1\text{-}2\mu\text{m}$ on-chip for acceptable coupling efficiency. (For comparison, $\pm 10\mu\text{m}$ placement accuracy is suitable for solder bumps used for electric connections.)
2. There is a large mismatch in energy confinement between an optical fiber and a silicon photonic waveguide. The energy is distributed over a $\sim 10\mu\text{m}$ spot in the fiber while it forms a sub-micron spot in a typical silicon photonic waveguide. This creates the equivalent of a large impedance mismatch that must be addressed with a suitable optical mode converter, which is analogous to an impedance matching circuit.

Precise self-alignment features are crucial to maximizing assembly tolerances and must be designed into any automated photonic assembly process that seeks to utilize standard electronic manufacturing equipment. Self-alignment structures are designed within the silicon photonic die and optical components (ferrule) to meet the $1\text{-}2\mu\text{m}$ on-chip photonic alignment requirement. Self-alignment techniques must also work within the speeds and tolerance limitations of today’s production equipment.

Pick-and-place handling of fiber components in a microelectronic manufacturing process is particularly challenging. Not only are optical fibers typically handled with specialized tools instead of standard vacuum pick-tips, but the placement accuracy of standard equipment is normally on the order of $\pm 10\mu\text{m}$ (almost an order of magnitude larger than single-mode optics requirements). In addition, high-speed pick-and-place equipment does

not offer the 3D spatial movement required for chip-to-fiber alignment. Equipment is designed to engage the die in-plane. Pressure sensitive movement is only possible in the downward direction after lateral positioning. This means, for example, that you can pick up a parallelized fiber array and lay it down in the V-grooves of the photonic die, but not be able to push the fiber array inward to butt into the waveguide coupler. To counteract this limitation in movement, a platform was designed to transfer a portion of the vertical pick-and-place movement into a horizontal force that successfully butts each fiber termination within the V-groove of its on-chip waveguide coupler [9,10]. The self-alignment features designed into the components and adaptive tooling demonstrated that high-throughput pick-and-place equipment could be applied to photonic fiber assembly, paving the way for large-scale automation and scalability in complexity, yield and manufacturing volume.

The graphic progression in **Figure 8a** shows how vertical force from the pick-and-place equipment is converted to the horizontal force needed to slide the fibers properly into the die. **Figure 8b** shows a 12-fiber planar array assembled onto the silicon photonic die with self-alignment providing $\sim 1\mu\text{m}$ on-chip final alignment accuracy. **Figure 8c** demonstrates how well the fibers fit into the V-grooves on the silicon photonic chip. **Figure 8d** computes the fiber core-to-waveguide coupler misalignment for 10,000 random structural tolerance combinations to demonstrate the manufacturability of the fiber self-alignment. The results show a 3σ misalignment below $\pm 1.3\mu\text{m}$ demonstrating tolerances well within required placement accuracies [11].

Compliant polymer ribbon: an elegant approach. Another waveguide-to-chip interconnect method is currently under development. In this approach, a flexible polymer ribbon replaces the cleaved fiber array. The design mechanically decouples the chip's optical interface from the fiber connector by substituting a mechanically compliant polymer ribbon. The ribbon contains an array of mechanical self-alignment structures and polymer waveguides that transmit light from the fiber to the die. This offers several advantages over other known approaches [12]:

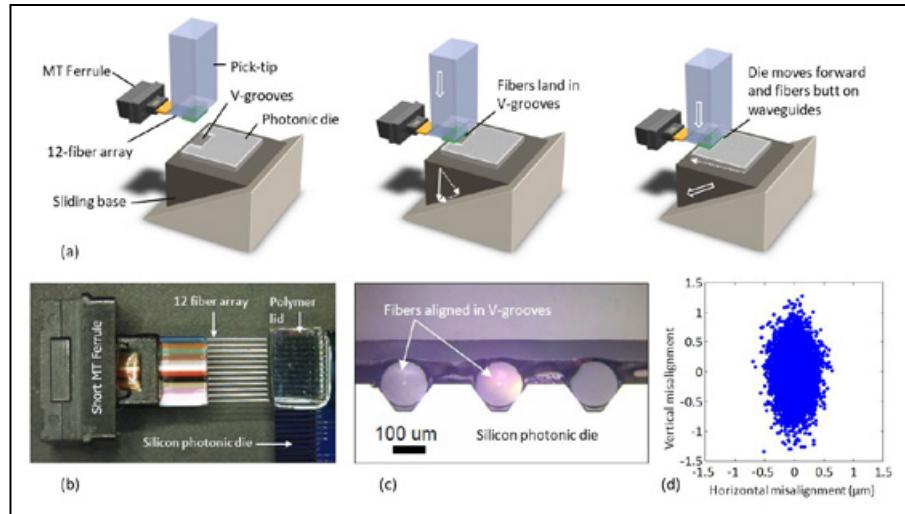


Figure 8: Demonstration of self-alignment of parallelized fiber assembly: a) trigonometric transfer of vertical to horizontal force, pushing the die forward to mate with the fibers; b) top down photograph of a 12-fiber ribbon array attached to a silicon photonic die; c) cross-sectional micrograph showing a close-up of three fibers settled into their corresponding V-grooves within the die; d) Monte Carlo analysis demonstrates manufacturability of fiber self-alignment with a 3σ misalignment below $\pm 1.3\mu\text{m}$. SOURCE: Images courtesy of IBM Corporation

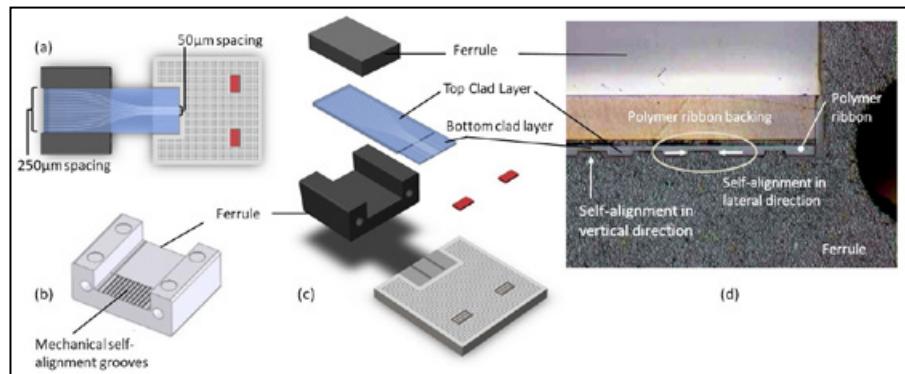


Figure 9: a) Top down view of compliant polymer ribbon aligned with ferrule (no lid) and silicon photonic die; b) ferrule with self-alignment guides for polymer ribbon; c) exploded view of assembly showing two-piece molded ferrule; d) cross section of polymer ribbon aligned to grooves in the molded ferrule. SOURCE: Images courtesy of IBM Corporation

- Cycling strains within the package are separated from the die by the compliancy of the polymer material, improving long-term reliability.
- The material and design supports large optical bandwidth. As compared to diffractive couplers where a 1dB bandwidth of a two-polarization vertical coupler has been reported at $\sim 30\text{nm}$ [13], the polymer ribbon demonstrated a 0.8dB penalty over a 100nm bandwidth and all polarizations [14].
- Integrated waveguides are lithographically patterned within a three-layer polymer stack. Lithography provides for significant flexibility in design to optimize

optical mode conversion efficiencies, define self-alignment structures or create other features of interest such as pitch conversions, bent die interfaces or port shuffles.

Figure 9a illustrates a 12-waveguide array, although the number of patterned waveguides can vary. At the fiber connector side, the waveguide spacing is designed at a 250 μm standard fiber connector pitch and tapers down to a 50 μm pitch at the photonic chip interface. The polymer waveguide is 8 μm wide at the chip interface where it mates with the silicon waveguide tapers. As in the parallelized fiber approach, the far end of the polymer interface is compatible with a standard 12x1 MT fiber interface.



At the MT fiber connection point, a custom molded U-shaped ferrule (**Figure 9b**) is used to allow for the alignment and connection to standard metal pins. Ferrule-to-polymer self-alignment structures are used on both the polymer ribbon and the ferrule. **Figure 9d** shows the ferrule's trapezoidal alignment ridges that promote vertical and lateral self-alignment of the polymer ribbon. Rectangular ridges are also patterned on the polymer ribbon to fit into trapezoidal grooves on the silicon die for self-alignment. Each of these features and process steps ensures final alignment accuracy within 1-2 μ m. When used hand-in-hand with position-tolerant optical coupling approaches, high-throughput assembly with low optical coupling-loss can be achieved.

The ferrule and polymer ribbon are assembled first. Because corresponding self-alignment structures are defined on both components, accurate alignment with low-accuracy, high-throughput assembly equipment is achievable. Like the parallelized fiber, the sub-assembly (ferrule and polymer ribbon) is pick-and-placed onto the silicon photonic die where a UV curable transparent epoxy adhesive is dispensed and then cured once the polymer ribbon is properly self-aligned. Material properties, application, dispense location and quantity, etc., are examined to properly control the bond-line for optimal performance.

The compliant polymer interface has been demonstrated to successfully butt-couple standard single-mode optical fibers to mode-matched polymer waveguides, and adiabatically couple the energy into on-chip silicon photonic waveguides. The results yield wide bandwidth with encouraging peak performance. They also reinforce the objective of adopting high-volume manufacturing processes to chip-to-waveguide assembly.

Summary

In today's data centers, distance dictates the use of copper, single-mode fiber or multi-mode fiber transmission. Silicon photonics enables bandwidths and power efficiencies (energy/bit) that conventional electronic cables cannot compete against. Tomorrow's high-volume data center demands will incorporate advanced packaging techniques that synchronously integrate

both electronic and photonic features. Because silicon photonics is a CMOS-compatible process, adopting the microelectronics industry's high-volume manufacturing processes and best practices is realistic. The convergence of two key assembly competencies, advanced multi-chip packaging and chip-to-waveguide interconnect, will contribute to the dynamic growth of this exciting market segment.

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Techniques to extend data rates

Data centers have historically been built using off-the-shelf components. As data center hardware matured, architecture evolved to take advantage of technology improvements at a measured pace. However, the unprecedented data explosion has accelerated data center redesign and is reshaping many technology roadmaps that support this segment.

To ensure higher bandwidth and rapid data delivery across the electrical interface, four general approaches are considered when evaluating system-level trades-offs such as overall efficiency, cost, and return on investment. These are speed (increasing symbols [1] per second or baud rate), modulation, lane count (number of fibers), and transmission technology (often distance dependent). The divergent needs of each end application guarantee that architecture will remain flexible. A granular segmentation in the Ethernet switch market, for example, will provide the data center with customized options it lacked in the past. **Table S2-1** describes various ways to mix and match technologies in support of next-generation 400GbE data rates.

The techniques listed in **Table S2-1** will allow for considerable variation. This is necessary because legacy technology at speeds $\leq 10\text{GbE}$ still represent a significant portion of data center infrastructure. In addition, new usage models in certain IoT/IoE,

industrial and automotive segments will leverage slower speeds. This said, there is much excitement and focus on facilitating faster data speeds. The IEEE Ethernet Task Force passed new Ethernet standards for 25GbE and 400GbE with 50GbE and 200GbE under consideration. These multiples will feed today's 100GbE and ultra-fast 400GbE infrastructure upgrades.

The general trend is that sophisticated techniques such as PAM-4 modulation, single-mode fiber (SMF) and wavelength multiplexing are becoming the de facto standard at shorter and shorter distances. For example, in the data center environment, SMF has traditionally carried signals over long distances such as 500 meters (inter-rack) to 2km (intra-data center) to 10+km (between data centers). SMF is now employed at 100 meters and is migrating to distances as short as 20 meters in order to provide downstream flexibility for data center upgrades. In fact, Microsoft announced that it will employ SMF at distances of 20 meters and greater. This is an evolutionary departure from traditional multi-mode fiber (MMF) interconnection that supports today's vertical cavity surface emitting lasers (VCSEL).

Trade-offs such as fiber cost become a more dominant factor as the number of links needed at shorter distance increases. Fiber can cost as much as \$200-\$300 for large switches. Because there are so many more short links (eg.,

transceivers, switches) incorporated into data centers, the overall capacity cost of fiber becomes significant and its rollout will, therefore, be planned to include subsequent upgrade costs as data center design continues to respond to increased capacity demands.

Reference

1. Data is sent in “symbols” where a symbol represents a specific state of frequency, amplitude and phase. A symbol can be single or multiple bits of data. In digital communications, the symbol rate is also known as the baud rate.

Feature	Technique	Getting to 400 GbE data rates
Speed	Increase baud rate (data symbols [1] per second) with forward error correction	Baud rate on each lane (fiber) is increased when transitioning from 10GbE to 25GbE or 50GbE per lane
Modulation	Using more bits for each transmission symbol	PAM-4 (used for 50GbE) transmits 2 bits of information per symbol versus NRZ with 1 bit per symbol
Lane Count	Increase copper traces and/or optical fibers	8 lanes at 50GbE (PAM-4) or 16 lanes at 25GbE (NRZ) both produce 400 GbE data rates
Transmission Technology	Tradeoff - copper traces versus optical fibers	Optical fiber can carry signals much farther than copper traces
	Tradeoff - Single Mode Fiber (SMF) versus Multi-Mode Fiber (MMF)	SMF requires more precise transceivers but can carry data over longer distances than MMF
	Tradeoff – number of wavelengths (λ) versus number of optical fibers	8λ at 50GbE on a SMF with PAM-4 modulation will enable 400GbE over a single fiber at distances of 10+km

Table S2-1: Rising data rates leverage current infrastructure while providing a platform for new technology.

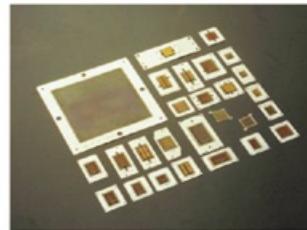
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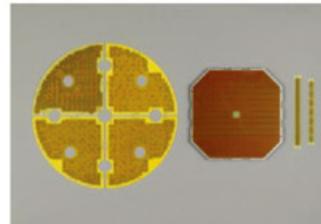
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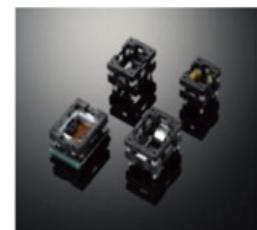
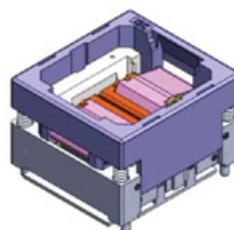
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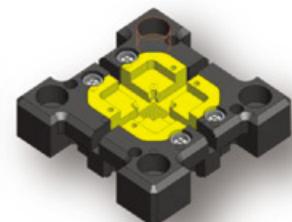
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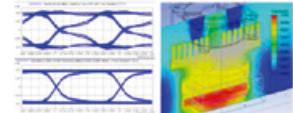
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Electrodeposition of Ø50 × 50µm Cu pillars for 3D stacking applications

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In this work, we demonstrate defect-free plating of Ø50 × 50µm Cu pillars on 300mm wafers, for 3D stacking applications. We also demonstrate the capability to control and tune within-wafer (WIW) and within-die (WID) uniformity of Cu pillar heights to given application requirements. Furthermore, by adjusting the concentration of plating additives, we are able to modify the shape and morphology of electroplated Cu pillars.

Introduction

Electrochemically deposited pillars/bumps are an integral part of 3D technology [1,2]. Electrodeposition offers the capability to fabricate complex structures at high throughput and lower cost than other deposition techniques. However, it is not immune to challenges such as tighter specifications for within-wafer and within-die pillar/bump height uniformity, or achieving specific structure shape and morphology, which present themselves with downscaling. For example, within-die uniformity (or coplanarity) is of special interest because of the fact that variations in pillar height within a die might have serious consequences on post-plating processing steps such as die-to-die and die-to-wafer stacking.

In order to meet the specifications for successful application of pillars/bumps in 3D technology, an electrochemist has a number of means to do so. These could involve, for example, substrate-surface pretreatments, modifying bath composition, various mass transport control methods, various current deposition waveforms, controlling the bath temperature, specific tool setup, etc.

A typical Cu plating bath for fabrication of Cu interconnects for applications in microelectronics industry could contain a basic makeup with a source of Cu ions and a supporting electrolyte, and a number of organic additives. The additives are often

designated as suppressors, accelerators, levelers, and grain refiners, according to their role in the electrodeposition process. Type, amount, ratio to other components, and their interactions during the plating process could have a profound influence on the properties of the plated Cu. The maximum temperature of the plating bath in a typical production tool is limited to about 60°C. This does not seem like much, but the variation in temperature of only several degrees could have a significant effect on the quality of the deposit.

In this paper, we report on wafer-level plating of Ø50 × 50µm Cu pillars. We examine the role of the surface pretreatment, bath composition, plating parameters, and tool setup in controlling the within-wafer (WIW) and within-die (WID) uniformity of Cu-pillar heights. Plated Cu pillars are characterized using optical microscopy (OM), scanning electron microscopy (SEM), focused ion beam (FIB), laser scanning microscopy (LSM), and other physical/chemical characterization techniques. Based on the acquired measurements and the observed trends, we optimize the experimental parameters to match application requirements.

Experimental

All wafer-level plating experiments were performed using an AMAT Raider electroplating tool with segmented anodes, enabling additional adjustment of the deposition current distribution. Copper plating chemistries from CUPUR® U Series (BASF's copper plating series for wafer-level packaging (WLP) applications) including Virgin makeup solutions (VMS, basic aqueous Cu bath with source of Cu ions, supporting electrolyte, and inorganic components), and all the additives, accelerator, suppressor, and leveler, are provided by

BASF SE (Ludwigshafen, Germany). Screening of useful concentration ranges of various bath components under different deposition conditions was performed on a coupon-level in a lab-bench plating tool at BASF laboratories, and was used as a starting point in wafer-level studies.

Cu pillars were plated on 300mm wafers with cylindrical openings 50µm in diameter and 60µm deep, as shown schematically in Figure 1. In all of our experiments, the 150nm Cu seed and the 30nm TiW barrier layer, fabricated using physical vapor deposition (PVD), were used as a substrate.

The Cu pillars are defined in a 60µm thick positive tone I-line layer by exposure on an Ultratech AP300 wafer stepper. Prior to plating, the diameter of the resist openings was measured simultaneously across the whole wafer using a Falcon 630 Plus tool (Camtek Ltd), with critical dimensions allowed to deviate ±2µm. The variations/non-uniformity of the diameter of the openings have direct impact on the wafer-level height uniformity of the plated Cu pillars, making this quality control step a must.

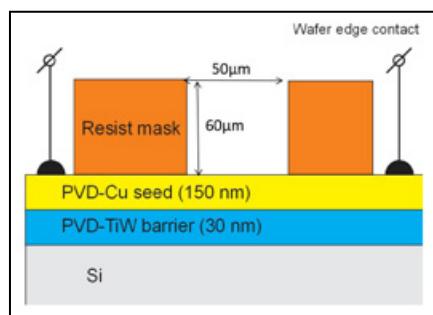


Figure 1: Schematic representation of the substrate, showing the dimensions of the opening in the photoresist, and barrier/seed (TiW/Cu) layer thickness (not drawn to scale).

Our goal was to fabricate Cu pillars $43\mu\text{m}$ high with a standard deviation $\pm 5\mu\text{m}$ (3σ), but requiring economical/practical plating times, i.e., with plating rates as high as possible without affecting WIW and WID uniformity. Post-plating, photoresist was stripped from the wafer and the height of all Cu-pillars on a 300mm wafer was measured simultaneously using the Falcon 630 Plus tool. The examples of the graphical output of the Cu pillar height measurements across the whole wafer and within a single die are given in **Figure 2**. For easier quantitative analysis and comparison between different wafers, and studies of the effects of various experimental parameters data is plotted using both tool metrology software, and other standard analysis software packages (e.g., Origin).

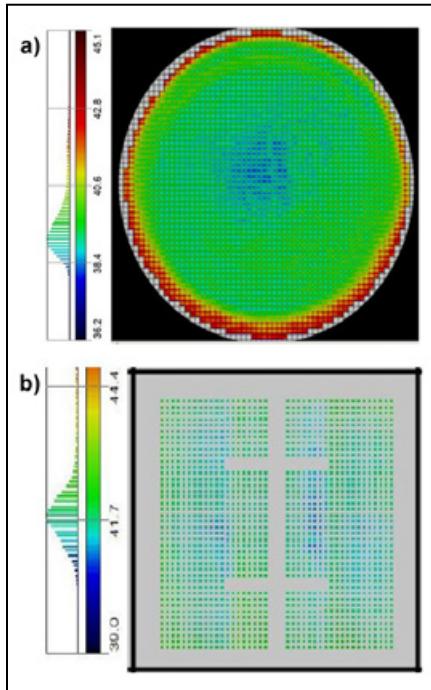


Figure 2: Graphical output of the full wafer a) and a single die b) Cu pillar height measurements. In both a and b), the height of each Cu pillar is measured and displayed. Color scale legends with corresponding height and values are placed next to the plots.

SEM and FIB tools were used to characterize the morphology and grain structure of individual Cu pillars. The shape of the top surface of a Cu pillar was also examined using a LSM/optical profiler. The concentration of additives in the plating bath was monitored using the cyclic voltammetry stripping (CVS) technique.

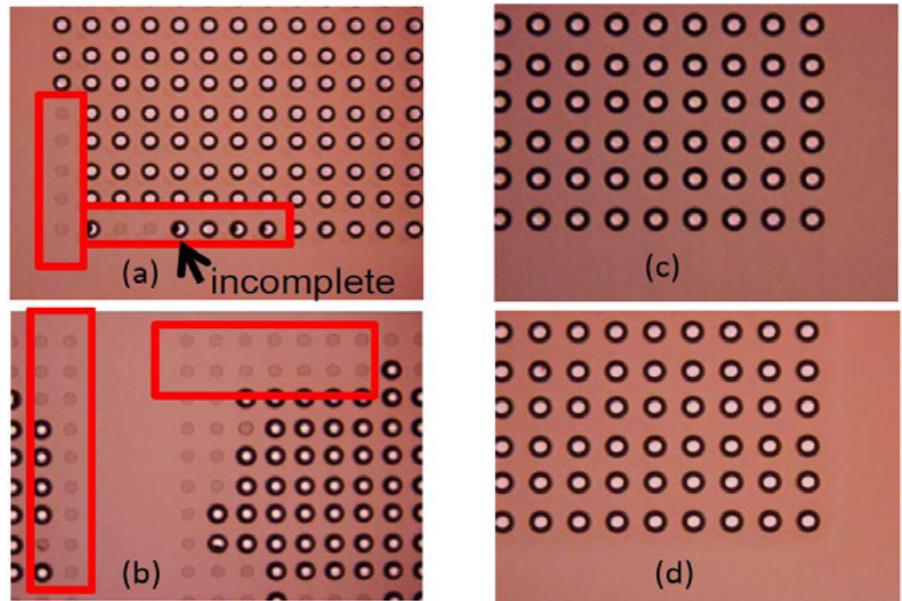


Figure 3: a) and b): Optical microscopy images of plated Cu pillars with no descum step applied; c) 3 months old descum; and d) descum performed just prior to plating.

Results and discussion

Cu seed surface pretreatment. Preliminary wafer-level tests showed a large number of defects, pillars missing, or simply not being plated in some areas on the die/wafer (**Figures 3a** and **3b**). Suspecting that post-lithography residues on the Cu seed surface blocked deposition, prior to plating we implemented a descum, which is a plasma surface pretreatment step. After implementation of the descum step, no missing bumps were observed during optical microscopy inspection (**Figure 3c** and **3d**). It made no difference whether descum was performed three months before (**Figure 3c**), or on the same day of the plating experiment (**Figure 3d**), suggesting that parts of the wafer indeed suffered from the resist residues, and not from seed quality deterioration with time. Consequently, descum became a mandatory processing step in all following experiments.

WIW and WID Cu pillar height uniformity. Defining a useful processing window for a given plating bath, structures to be fabricated, and a plating tool, is often a cumbersome trial-and-error effort, and reporting on it is beyond the scope of this paper. What we would like to focus on is the interplay between plating rate and WIW and WID Cu pillar height uniformity. Our goal is to optimize plating parameters in such a way that a good wafer-scale uniformity and coplanarity are obtained at a plating speed

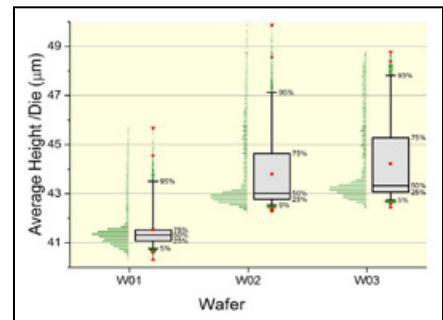


Figure 4: Cu pillar average-height-per-die distributions for W01, W02, and W03, plated at 0.86, 2.58 and $3.44\mu\text{m}/\text{min}$ rates, respectively.

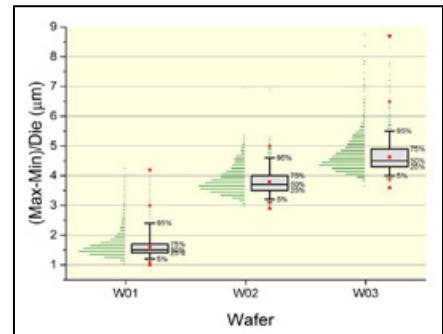


Figure 5: Maximum height difference for each die on wafers W01, W02, and W03, plated at 0.86, 2.58 and $3.44\mu\text{m}/\text{min}$ rates, respectively.

considered fast enough for the production line in the microelectronics industry. Plating at a low rate of approximately $0.86\mu\text{m}/\text{min}$ resulted in the best uniformity and coplanarity (the lowest maximum height difference within die, W01 in **Figure 4, 5**,

and 6b) on wafer scale. Targeting maximum height differences (within die) below 1 μm for the given system, requires plating time in excess of 1 hour, which could be considered too long by many in the field. By increasing the plating rate to 2.58 $\mu\text{m}/\text{min}$ (W02) and 3.44 $\mu\text{m}/\text{min}$ (W03), we reduced the plating time to 16.67 min and 12.5 min, respectively. However, this reduction in plating time is accompanied with deterioration in height uniformity and especially in coplanarity (**Figures 4, 5, and 6**). How does one correct for such an increase in non-uniformity within die? Hardware improvements are a possibility, but they are likely to be complex and economically impractical. For example, one could optimize the design of the counter electrode (anode) according to the characteristics of the mask used to define the photoresist pattern, to get the most uniform distribution of pillar heights within a die. However, to be an economically viable option, the same mask would have to be used for a very long time, or be easily

adjustable to the new pattern designs. So the best option is to continue optimizing plating baths, i.e., adjusting the ratios of the organic additives already used in the plating, or synthesizing new ones for high-speed/high-WID uniformity. It is still likely that plating at lower plating rates would lead to better local uniformity, and one should consider accepting the drawback of longer plating times when extremely stringent WID uniformity specifications are set.

The shape of Cu pillars. The shape and symmetry of Cu pillar (i.e., the top surface that is in contact with electrolyte during plating) can be affected by plating bath composition, deposition current density, and forced convection/flow pattern [3-7]. We have explored the effect of bath composition and deposition current density on the shape of Cu pillars, while we have not modified the flow rate or the pattern in the plating tool. To make it easier to quantify our results, we have defined “shape-describing” variables and assigned ranges of values to different pillar shape characteristics. These conventions are summarized in **Figure 7** and **Table 1**.

Similar to results already published in the literature [3-5], we found that the asymmetry in the shape of pillars could be removed by adjusting the concentration (ratios) of organic additives in the plating bath. Of the three organic additives in the plating bath – accelerator, suppressor, and leveler – the pillar shape was most sensitive to variations in concentration of the suppressor. There were also minimum amounts of accelerator and leveler required to remove the asymmetry, and bath composition was first optimized to get reproducibly symmetrical Cu pillars.

The effects of suppressor and deposition current density on Cu pillar shape are summarized in **Figures 8** and **9**. By varying the suppressor concentration, while keeping all other parameters and the concentration of other bath components constant, we were able to manipulate the Cu pillars’ shapes (**Figures 8a** and **9a**). By increasing the amount of suppressor in the plating bath we were able to change the shape from domed to recessed. The parameter H2 changed from 7.5% to -2.8% for a plating rate of 1.53 $\mu\text{m}/\text{min}$. When the same set of experiments was repeated at the increased plating rate of 3.44 $\mu\text{m}/\text{min}$ (**Figure 9b**), H2 increased when compared to corresponding experiments at lower deposition rates. An increase in deposition current density – for the given bath composition – promoted a dome shape, or a slightly reduced recess. It is noteworthy that defect-free Cu pillars (**Figure 8**) were plated for all the conditions presented, and that one could tailor the shape of the structure without worrying over reliability issues (i.e., voiding within feature with change in profile of a Cu pillar).

Plating rate enhancement

In all the experiments described in the previous paragraphs, galvanostatic deposition was used, i.e., the deposition

Shape	Parameter
Dome	$H_1 \geq 7\%$
Flat	$0\% \leq H_2 < 7\%$
Recess	$H_2 < 0\%$
Symmetric	$H_1 < 7\%$
Asymmetric	$H_1 \geq 7\%$

Table 1: Variables and corresponding values describing the shape of the Cu pillar’s top surface.

current was constant during the entire plating process. In practice, two additional steps could have been applied at the very beginning of the plating process: during introduction of the wafer into the plating cell (so called “hot entry”), and the initial strike step. However, their role is in facilitating the defect-free plating during the main step, and the duration of both is negligible in comparison with the “deposition” galvanostatic step.

The maximum deposition current (and thus the pillar growth rate) is ultimately determined by the mass (Cu^{2+} ion) transport limitations at the bottom of the opening in the photoresist. These limitations become less severe with

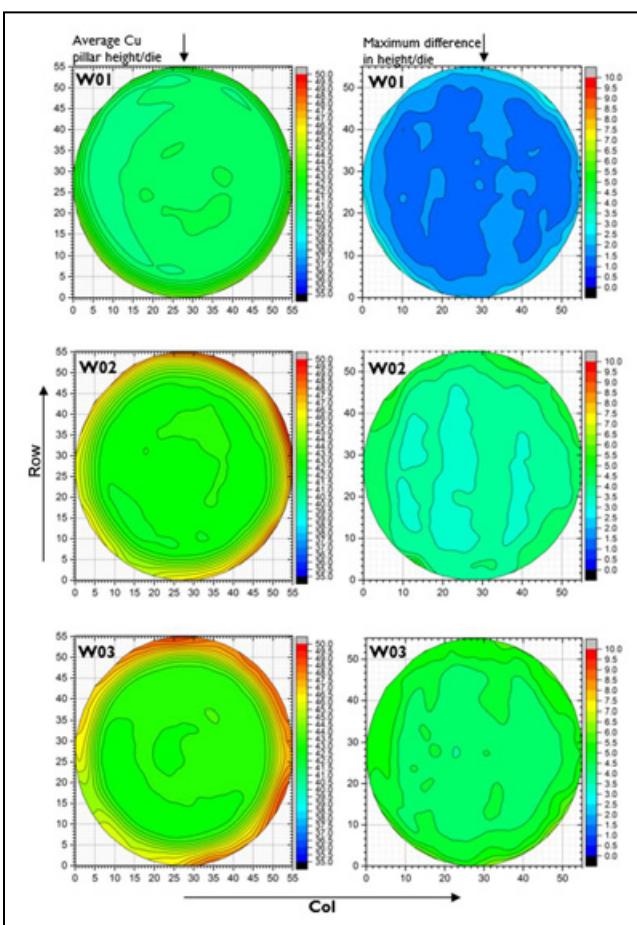


Figure 6: Contour plots of average Cu pillar height/die and maximum difference in height within-die for wafers W01, W02, and W03, plated at 0.86, 2.58 and 3.44 $\mu\text{m}/\text{min}$ rates, respectively.

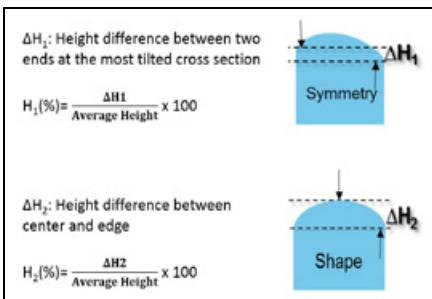


Figure 7: Definition of variables used to describe the Cu pillar shape (top surface):

ΔH_1 : The height difference between two ends at the most tilted cross section.

$$H_1(\%) = \times 100$$

ΔH_2 : Height difference between center and edge.

$$H_2(\%) = \times 100$$

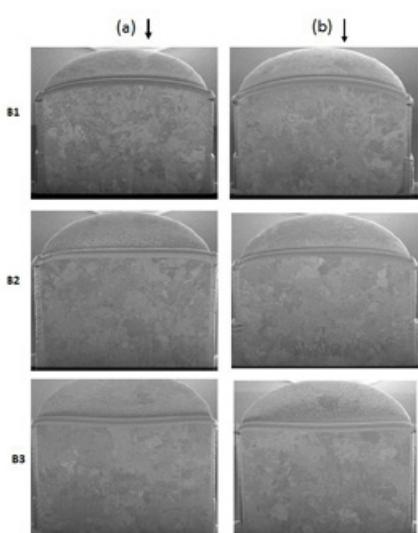


Figure 8: FIB cross-section images of the Cu pillars deposited on 300mm wafers at plating rates of a) 1.53 $\mu\text{m}/\text{min}$, and b) 3.44 $\mu\text{m}/\text{min}$. The suppressor concentration has been increased going from $\text{RC}^*/5$ in B1, RC in B2, to $6\times\text{RC}$ in B3, while all the other parameters were unchanged. No defects were detected. NOTE: RC^* = Recommended concentration.

time, with the pillar's growth and the depth of the opening becomes shallower. Obviously, the reduction in plating time can be achieved by increasing the deposition current gradually, in accordance with the evolution of the geometry of the opening. The introduction of multiple current steps could be done through a trial-and-error approach, or by using analytical and computational models [8]. More current steps would allow finer control of the plating process, and therefore even faster fabrication of pillars. However, one has to optimize both input current, and the duration of each step, which becomes

challenging when there is a large increase in the number of steps.

Another variable that could affect the deposition rate is temperature [9,10]. And while the increase in temperature has an effect on so many different parameters, including solubility, reaction kinetics, mass transport, etc., one should not forget that it could have a detrimental influence on the functioning of the organic additives in the plating bath. In

our experiments we have used a typical production temperature.

An example of the effects of multi-step current waveforms and different bath temperatures on plating rate (time), uniformity of Cu pillar heights, and coplanarity is given in **Table 2**, and **Figures 10** and **11**. Wafer W09 is plated using a stable and reproducible baseline two-step process that takes about 12.5 minutes (plating speed of 3.4 $\mu\text{m}/\text{min}$)

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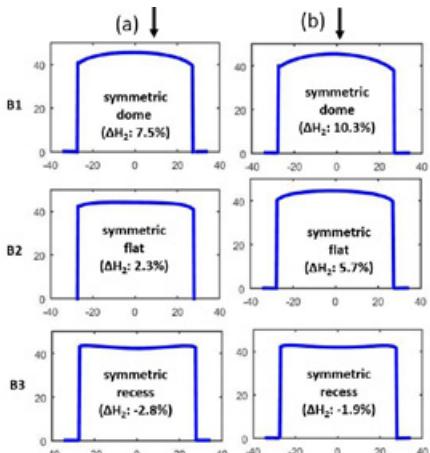


Figure 9: The effect of organic additive concentration and deposition current density on the shape of Cu pillars. The plots show LSM profile scans of the Cu pillars deposited on 300mm wafers at a plating rate of a) 1.53 $\mu\text{m}/\text{min}$, and b) 3.44 $\mu\text{m}/\text{min}$. The suppressor concentration has been increased from $\text{RC}^*/5$ in B1, RC in B2, to $6 \times \text{RC}$ in B3, while all the other parameters have been kept constant.

min), with the plating bath temperature maintained at 25°C. By increasing the number of current steps to four, while keeping all other parameters identical (W10), the plating rate increases to 4.0 $\mu\text{m}/\text{min}$, and plating time is reduced by 1.6 minutes (13%). The pillar height distribution and coplanarity are only slightly broader. Current steps were better optimized in the test with wafer W12, in which the plating bath temperature was maintained at 35°C. The plating speed of 5 $\mu\text{m}/\text{min}$ was achieved, plating time reduced by 3.9 minutes (31%), and all that with just a slight broadening in the pillar height uniformity and coplanarity distribution profiles. We believe that with further optimization of current steps, their duration, and bath temperature the plating time could be reduced even further.

Summary

We have explored the effects of various experimental parameters on wafer-level electrochemical deposition of Cu pillars. By optimizing deposition current density, current distribution, bath composition, temperature, and surface pretreatments, etc., we were able to demonstrate the ability to tailor the Cu pillar height, within-wafer (WIW) and within-die (WID) pillar height uniformity, and Cu pillar shape, according to the application specifications.

Ideally, one would want to have an economical process taking a very short time to finish and leading to defect-

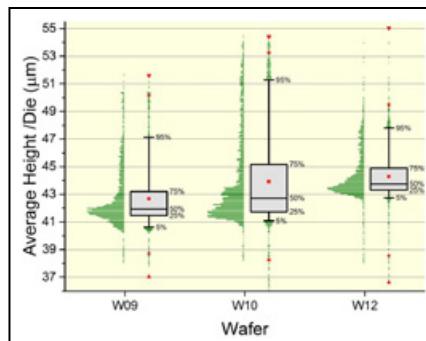


Figure 10: Distribution of averaged-per-die Cu pillar heights for wafers plated using multi-step current waveform and different bath temperatures. The corresponding legend is also displayed in **Table 2**.

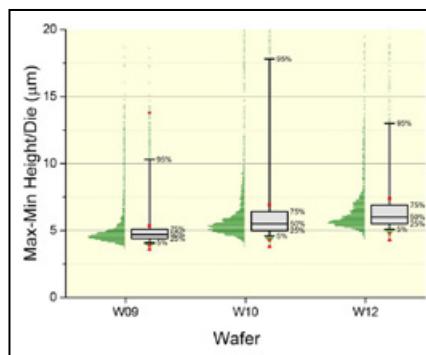


Figure 11: Coplanarity (defined as a difference between maximum and minimum pillar height within a die) for wafers plated using a multi-step current waveform and different bath temperatures. The corresponding legend is also displayed in **Table 2**.

Wafer ID	Waveform	Temp. (°C)	Plating Speed ($\mu\text{m}/\text{min}$)	Plating Time (min)
W09	2-step	25	3.4	12.5
W10	4-step	25	4.0	10.9
W12	4-step	35	5.0	8.6

Table 2: Waveforms and temperature used for plating Cu pillars on wafers W09-W12, and plating speed and time achieved. Corresponding average per die height uniformity and coplanarity are plotted in **Figures 10** and **11**, respectively.

free pillars, with near perfect WIW and WID uniformity. By looking into new cell designs, development of new plating baths, and experimental and optimization methodology, we continuously strive to match these closely-coupled, but somewhat antagonistic requirements.

For the system described in this paper, we fabricated defect-free Ø50 μm and (43 \pm 5) μm (3 σ) high Cu pillars, and manipulated its shape and morphology with relative ease. At the time of reporting, the champion (i.e., the fastest) process was about 8.6 minutes long with an

average height of 43.5 \pm 3 μm , a 2% WIW uniformity, and a 9% WID uniformity.

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Surface insulation resistance of no-clean flux residues under various surface mount components

By Bruno Tolla, Denis Jean, Kyle Loomis, Yanrong Shi [\[Kester\]](#)

No-clean fluxes present great benefits for the electronic assembly industry, but the activity of the unwashed process residues must be tightly controlled in order to meet high reliability standards. The pervasive miniaturization trends of the industry, coupled with the intricacy of the new component architectures, has profoundly affected the nature and the reactivity of the flux residues. A series of customized surface insulation resistance (SIR) experiments under various surface mount components demonstrate the dramatic impact of the partial activation and restricted outgassing of the fluxes on the reliability of the final assembly. Mainstream no-clean pastes and liquid fluxes, which are qualified under all the standard SIR and ECM reliability tests, present SIR values several decades lower than the 100Ω limit mandated by IPC J-STD-004B when tested with quad-flat no-leads (QFNs) packages. Different surface mount components (e.g., passive, quad flat package [QFP], ball grid array [BGA]) can be more or less forgiving depending on the induced heat gradients and resistance to outgassing. From this perspective, we demonstrate how a thorough examination of the interplay between assembly architecture, processing conditions and flux formulation is the necessary condition for the design of reliable fluxes mitigating the risks of in-field failures of the final assembly. This study forms the background for the proposal of new reliability testing standards for the electronic assembly industry.

Introduction

The electronic assembly industry is perpetually evolving to satisfy the ever-increasing needs for performance, efficiency, versatility, and system integration in robust and cost-effective packages. From the big data revolution

to energy efficiency problematics, from consumer to industrial applications, these driving forces result in growing system complexities. From an assembly process perspective, interconnect densities are constantly increasing, while form factors, stand-off heights, and component layouts at various scales are always more challenging. These trends, associated with the needs for mobility and end-use in challenging environments, greatly increase the sensitivity of modern electronics to in-field failures. Meanwhile, there has been little progress in the definition of reliability qualification protocols for these assemblies. The certification standards do not reflect the current design trends and the industry as a whole is calling for more predictive tests. Because of the component and architecture complexity, and the great variety of assembly materials and processes, it is of paramount importance to design model testing vehicles and protocols allowing the study of specific reliability failure modes. This paper represents such an attempt by focusing on the dramatic influence of surface mount components on reliability failures from assembly materials (solder pastes and fluxes). The design of testing boards involving multiple component types in various configurations allows a methodical study of the interaction of materials, components and assembly processes. It also allows us to analyze the multiple chemical mechanisms at play during the assembly process, which will ultimately drive the reliability of the electronic device during its operating life. It therefore contributes to a fundamental understanding of the in-field failure of complex electronic architectures, which is a necessary condition for the design and adequate testing of robust products.

Experimental

The equipment and procedures used during our investigations are regrouped in this section. The specifics of our testing methodology (temperature, voltage gradients, humidity levels, exposure time, component characteristics) have a critical influence on the outcome of the test, as will be discussed in the following section.

Temperature calibration study. Local temperature conditions experienced by the assembly materials (flux and solder pastes) were recorded by means of a Mole thermal profiler, whose thermocouples were placed in the interconnecting area between a standard IPC-B-24 SIR board and conventional quad flat packages (QFP208). The assemblies were subjected to various reflow profiles using a Speedline Electrovert OmniExcel 7-zone oven.

Surface insulation resistance (SIR). All tests were executed according to the joint industry standard IPC J-STD-004B, under test method IPC-TM-650 §2.6.3.7, involving SIR monitoring over a period of 7 days of an IPC-B-24 board exposed to a moist environment (40°C , 90% RH) under a constant bias of 12.5VDC. This board is made of bare copper on an FR-4 epoxy laminate. It consists of four comb patterns formed by interdigitated Cu traces (width: 0.4mm, spacing: 0.5mm). A Vitronics Delta3 industrial-scale wave soldering machine was used for the application of pattern-up/pattern-down soldering profiles. All other flux preconditioning and reflow protocols were carried-out in the 7-zone oven described above.

SIR assessments under BGA components. The standard IPC-B-24 board was customized by replacing the interdigitated connector pattern

with a daisy-chained pad structure (**Figure 1**). This architecture enables the measurement of the surface insulation resistance of laminate sections located between the interconnections underneath the BGAs.

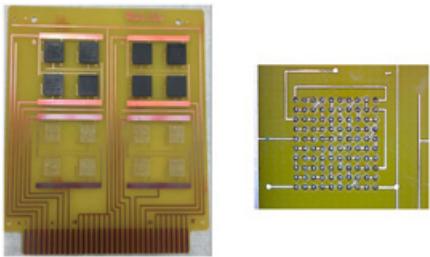


Figure 1: A custom-designed SIR board under BGAs.

Solder paste was stencil-printed on the pads in a Speedline MPM Momentum printer equipped with a 4mil laser-cut stainless steel stencil. BGA100 components were then positioned with a Juki KE-1080LN pick-and-place system. The assembly was reflowed under air in the 7-zone reflow oven, using a conventional IPC LF242C reflow profile. It was then subjected to the same environmental conditions (T, RH, voltage bias) and duration as the standardized SIR tests described above.

SIR assessments under QFN components and resistors. The second board showcases a more radical departure from the conventional designs used in reliability assessment (**Figure 2**). This test vehicle was developed to be more representative of current trends in the electronic assembly industry, while providing a challenging environment to discriminate the reliability of chemical fluxes and solder pastes in realistic application conditions. It features a series of resistors of various dimensions (2512, 1210, 0805) and a matching board pattern, where additional interdigitated traces were placed in the central body area to serve as local sensors for biasing and SIR measurements (**Figure 2.1**). In a similar fashion, two quad flat no-leads packages (QFN44, QFN100) are connected to a pattern featuring an additional sensor loop in the channel between the thermal pad and the perimeter I/Os (**Figure 2.2**). This sensor enables SIR data collection

across the channel (loop-to-thermal pad and loop-to-I/Os biasing).

Various no-clean solder pastes were used to assemble these test boards. A 5mil laser-cut stainless steel stencil was used in conjunction with the Momentum printer to transfer the paste on the regular pad structures of all components. The sensors traces under the resistors were also stencil-printed to ensure enough flux was deposited in this area. The assemblies were then reflowed in air using a conventional profile. Their SIR was monitored over a period of 7 days under a moist environment (85°C, 85% RH) considered as challenging conditions for these no clean pastes, based on an earlier study [1]. An 8VDC bias was applied to achieve the desired voltage gradients under the components, as will be discussed in the following section.

Results and discussion

The following set of experiments aimed to methodically assess and deconvolute the various failure modes associated with the use of surface mount components from a chemical reliability perspective. Starting in an open environment, we describe the mechanisms of interaction between materials, components and assembly process. We then use custom-designed populated boards of increasing complexities to test for reliability in real-life conditions while controlling each environmental variable.

Partial activation effects. One fundamental impact of the board components is their disturbance of the thermal transfer in the interconnection area. This region consists of a shallow layer of flux and solder intercalated between the devices and the epoxy laminate. These materials have radically different heat transfer coefficients,

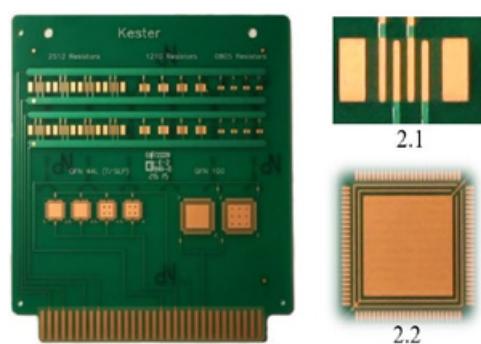


Figure 2: A custom-designed SIR board under passives/QFNs.

and tend to “shadow” the convective transfer of heat from the reflow oven to the interconnection. We quantified this effect in real application conditions by executing the temperature calibration study described in the experimental section, under the various reflow profiles reported in **Figure 3**.

Both the baseline conditions (labeled FR4) acquired on unpopulated IPC-B24 SIR boards and the local temperatures collected under the QFP208 components (QFP) are represented. One can visualize the heat gradients by comparing curves of the same color. These temperature drops between bare and populated boards vary in function of the reflow profile: long profiles provide more time for the temperature under the components to equilibrate, while temperature gradients as high as 40°C can be experienced on short profiles, regardless of the peak temperature. These heat heterogeneities could be dramatic enough to drop the temperature below liquidus for some profiles (green curve), resulting in non-reflowed solder under the QFP components. It is therefore likely for fluxes located under massive components to experience thermal conditions differing significantly from the original profile. In these conditions, the energy transferred to the flux by the reflow oven is much lower than expected. Therefore, the physical state of the flux residue differs from the one obtained in equilibrated conditions as described by the IPC standards. This so-called “partially activated state” can have drastic effects on the reliability of the final assembly, as demonstrated in the following series of experiments. Four fluxes were reflowed in various conditions on IPC-B24 boards prior to being submitted to the standard SIR testing protocol (**Figure 4**).

The conventional fluxes (represented by Flux D) are extremely sensitive

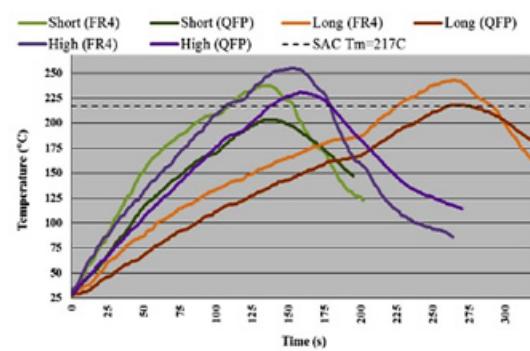
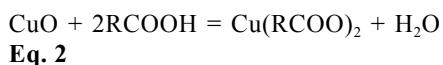
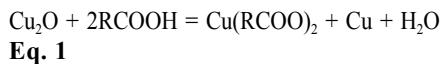


Figure 3: Reflow profiles for temperature calibration.

to the activation conditions: these fluxes need to be soldered pattern-down (where the scrubbing action of the wave removes the majority of the residues) to pass the IPC standard. It is interesting to note that partial activation (modeled by condition #2) actually degrades the reliability of the final assembly compared to the unheated state (condition #1). More advanced fluxes were developed to guarantee a better process window, two of them (fluxes A and B) being highly reliable under all activation conditions.

These effects are modeled by the chemical reactions describing the fluxing process of Cu substrates by halogen-free activator packages [2-4]:



The fluxing residues are made of organometallic compounds, as represented in **Equations 1-2**, combined

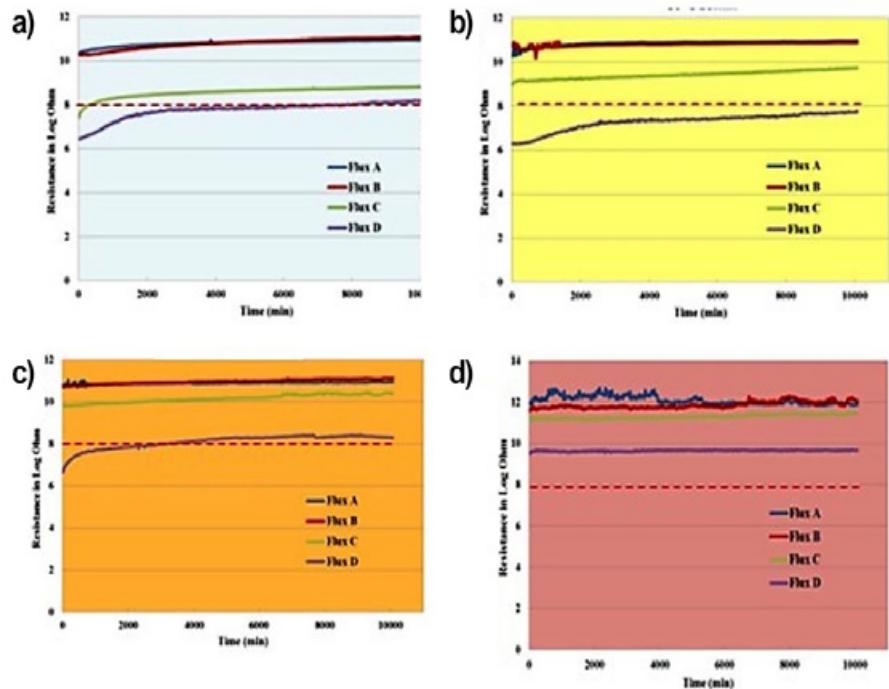


Figure 4: SIR studies under various activation conditions: a) Flux dried at room temperature/24h; b) Flux preheated at 80°C/10min; c) Flux wave soldered pattern-up (120°C preheat + 200°C/5s); and d) Flux wave soldered pattern-down.

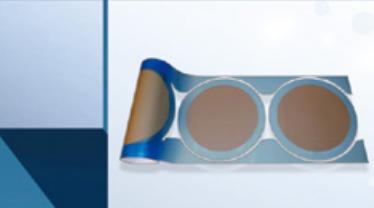


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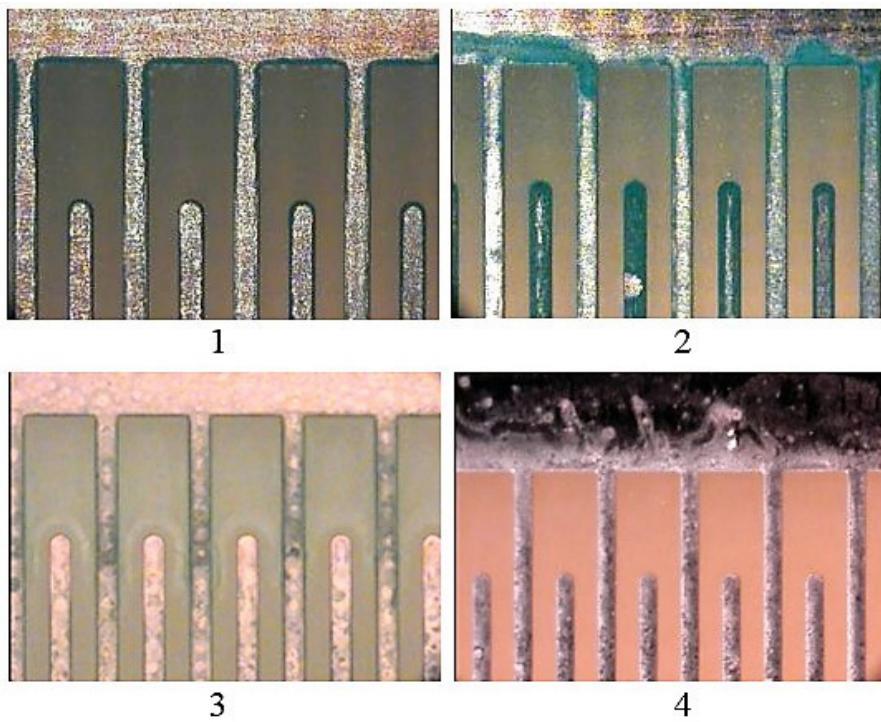


Figure 5: Microscopic analysis of residue from flux D after reflow on a IPC-B24 board under the four conditions of **Figure 4**.

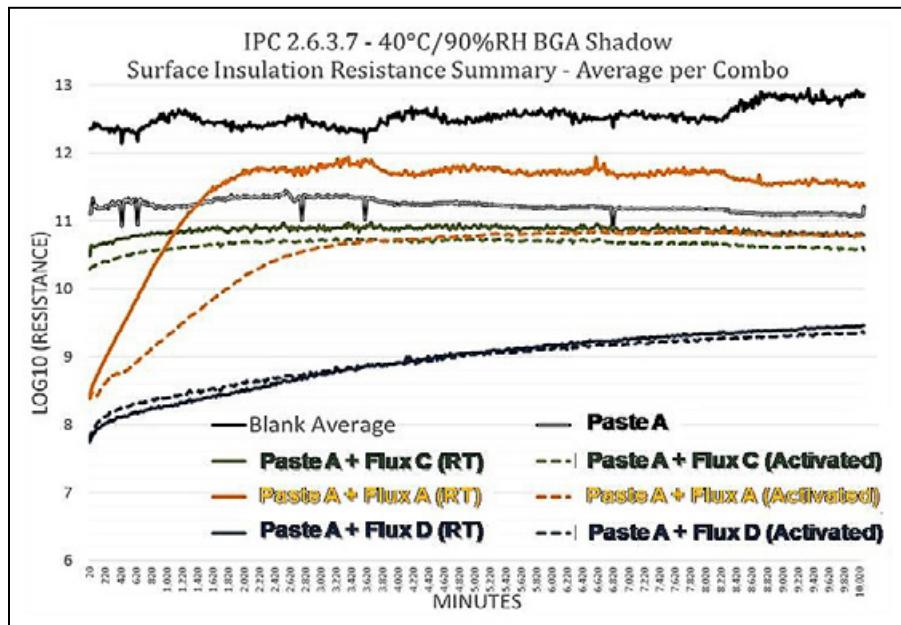


Figure 6: SIR study under BGA components. Various fluxes and activation conditions are plotted.

with unreacted activators, as well as their dehydration and decomposition products resulting from reactions/**Equations 3 and 4**:



All these chemical equilibria will be impacted by the actual temperature conditions experienced by the flux. Therefore, the nature and physical characteristics of the residues produced by the reflow process will strongly depend on the heat gradients described in our experiment. As an example, **Figure 5** visualizes the evolution of Flux D under

the various activation conditions. The change in coloration of the residue, as well as the evolving amounts found on the board, constitute a visual representation of the chemical processes described by **Equations 1-4**.

The second fundamental impact of a deviation from the calibrated reflow profile is not captured in these equations. The flux formulations generally contain a complex set of solvents, and a change in the reflow conditions will affect their respective evaporation rates. Consequently, flux residues can contain significant amounts of solvents when local thermal gradients result from the placement of large components acting as thermal sinks. Area array components with large form factors, low stand-off and a dense I/O pattern can produce the same effects by compromising the solvent outgassing channels. These residual solvents will mediate the electrochemical processes responsible for all reliability failure modes. Their impact is a function of the solvent polarity and moisture sensitivity. For a discussion around these mechanisms, the authors refer the readers to their recent communication on the topic [5].

Reliability assessments under BGA components

The concepts described earlier were applied to real-life application conditions. In a first set of experiments, we studied the influence of ball grid array components on the activation level of flux residues. These components were selected to discriminate the heat "shadowing" impacts (thermal gradients), from the solvent-trapping effects. The relatively open interconnection structure (0.8mm pitch, 0.34mm space) and high stand-off (0.36mm initial) of the BGA100 test vehicle do not put significant restrictions to solvents venting off from the flux. The equipment setup and experimental protocol are described in the experimental section.

Various solder pastes were screened with this method. We reported in **Figure 6** the results obtained with the most reliable one as a baseline (Paste A). This paste was designed to minimize the electrochemical activity of its residues in moist environments. These flux residues are essentially inert under all reflow and activation conditions, as demonstrated by a minimal drop of the SIR values under BGAs over the whole duration of the test. The specific impact of pastes on reliability will be described in the next series of experiments. The assembly was then contacted with various fluxes to focus

the discussion on the contribution of chemical packages to the reliability under components.

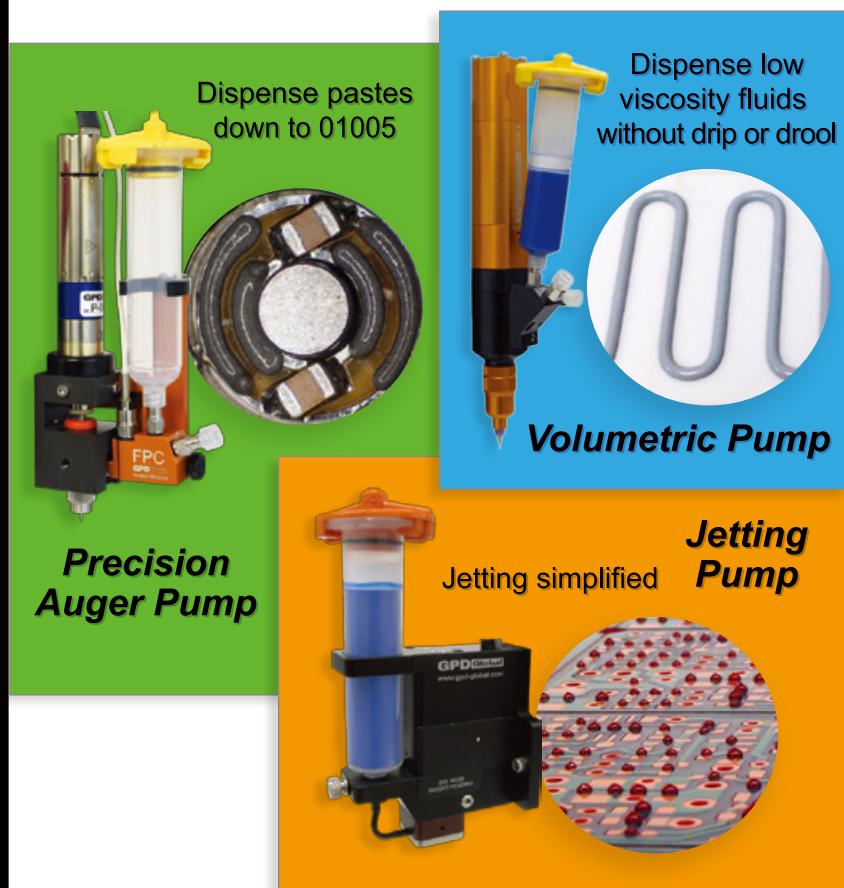
The colored lines in **Figure 6** represent the impact of three different flux formulations added in large excess to the assembled device. These fluxes were either dried for 12h in ambient conditions (solid lines) or partially activated (dotted lines). Partial activation corresponds to condition #2 of the previous set of experiments (10min preheat at 80°C). Under these BGA components, the conventional Flux D remains significantly less reliable than the more advanced fluxes A and C, with drops in SIR values averaging two decades (i.e., a factor 100 in linear scale). Under this experimental setup, the impact of partial activation was only seen with Flux A, which still presents high SIR values, however. One can also observe that Flux D presents a better performance than in the previous series of experiments executed on conventional IPC-B-24 boards. This is attributed to the significantly larger pad spacing for the BGA100 components compared to conventional IPC-B-24 boards, resulting in a 60% decrease of the voltage gradient across conductors (for an identical voltage bias of 12.5V). As reported in an earlier communication [5], voltage gradients are a critical factor of electrochemical failures, therefore the nominal voltage bias should systematically be normalized for data analysis.

Reliability assessments under various components

Following these observations, a more elaborate board was designed, where various voltage gradients and component complexities were tested. The experiment intended to represent mainstream applications; the selected components are currently used in high-volumes in our industry. The custom-designed board described in the experimental section uses capacitors and QFNs with various pitches, resulting in voltage gradients ranging from 16 to 45V/mm and 27 to 57V/mm, respectively. The current IPC standard for SIR calls for a value of 25V/mm (down from 100V/mm in the older version). The resistors represent low-complexity components, from which solvents can easily vent off. We assessed the voltage gradients' effects specifically on these simple and open structures. The QFNs represent a more complex architecture, with a greater thermal mass creating the temperature gradients discussed earlier. In addition, the small clearance underneath these components and the tortuosity of the outgassing channels makes this architecture very prone to trap solvents and decomposition products. The large amounts of solder paste deposited on the thermal pads at the center of the structure, amplify the phenomenon. For these reasons, the QFNs represent ideal test vehicles to assess the impact of the multiple

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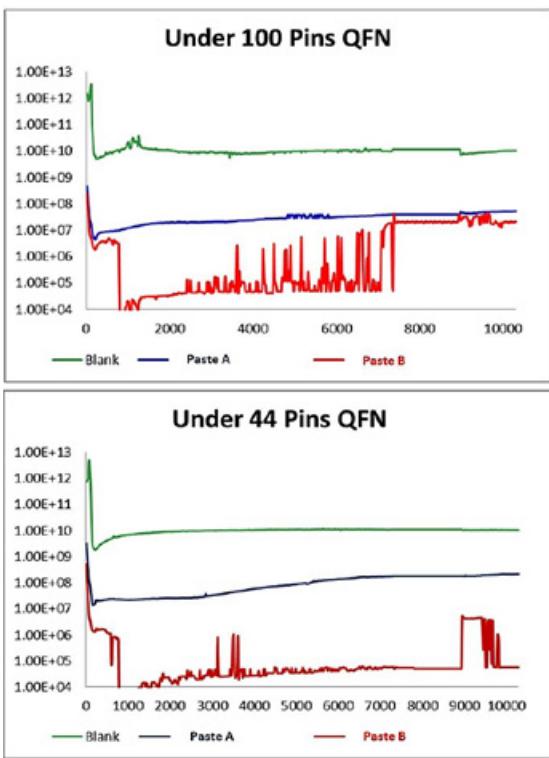


Figure 7: Reliability performance of two commercial pastes under QFN components.

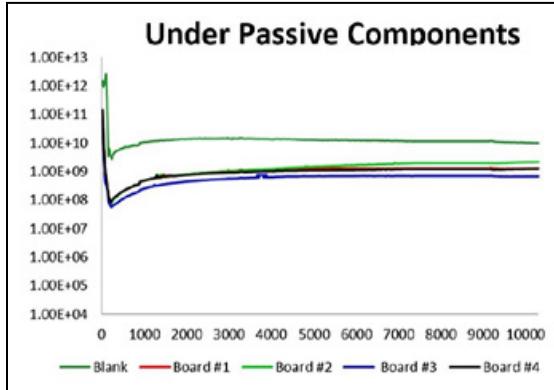


Figure 8: Reliability performance of two commercial pastes under passive components.

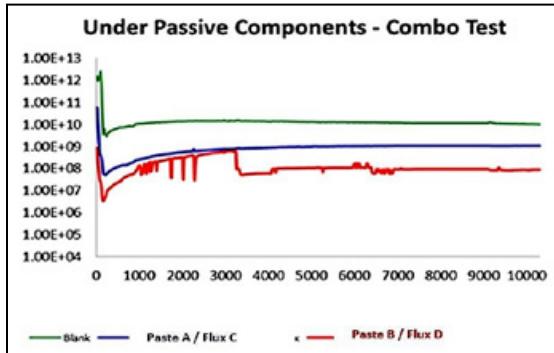


Figure 9: Reliability performance of the pastes/flux "combo" under passive components.

component-driven reliability failure mechanisms described earlier.

Indeed, this new test vehicle is capable of discriminating solder pastes very efficiently as demonstrated in **Figure 7**. The two commercial pastes reported here present radically different reliability levels under both QFN components. The application of Paste B results in a SIR drop of more than four decades, while the other paste maintains a rather standard performance level under these components. The combination of a greater thermal mass and the resistance to outgassing make these QFNs a challenging environment for Paste B. Meanwhile, the chemical package used in Paste A turns into reliable residues under the same conditions.

In contrast, the voltage gradient effects assessed under the resistors were minor (e.g., less than one decade) compared to the major SIR drops observed for some pastes under QFNs. Moreover,

these two pastes behave similarly and acceptably under the passives (**Figure 8**)—a direct demonstration of the critical impact of the component characteristics on the reliability of the final assembly. This also highlights the limitations of the industry standards using unpopulated boards: both pastes are classified as ROL0 under IPC-J-STD 004B.

In an effort to discriminate the heat gradient effects from the resistance to outgassing, we dispensed an additional amount of fluxes onto the components, following the conventional SMT assembly process of passives and QFNs with solder paste. The fluxes migrated underneath the components because of their low surface tension, and the assembly was subsequently dried at room temperature. The area under the resistors was saturated with unheated residues, which had plenty of clearance to outgas the volatile portion of the solvents. This "combo" configuration didn't change the outcome of the test significantly, as observed in **Figure 9**. Similar results were obtained under the QFN components, the performance of Paste A remaining at the same level (**Figure 10**).

These results indicate that the reliability failure mechanisms at play under surface mount components are complex and convoluted. The dramatic variation in the

reliability performance of Paste A, when tested under various devices, results from a complex process associating multiple mechanisms, from physical solvent outgassing to fluxing and decomposition reactions, and affected by local temperature gradients and component architectures.

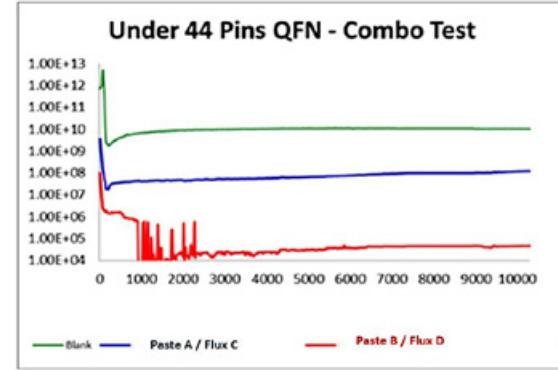
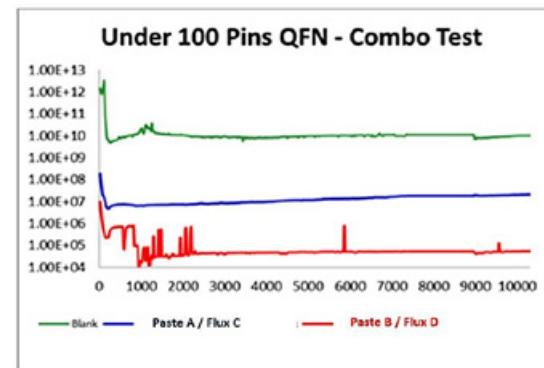


Figure 10: Reliability performance of the pastes/flux "combo" under QFN components.

Summary

This study demonstrates the strong interaction between solder materials and components in determining the reliability of an electronic assembly. The multiple mechanisms at play were described, and their dramatic impact

was assessed through the comparison of simple and open structures (capacitors, BGAs) with more complex architectures (QFNs). The latter creates a challenging environment for some commercial pastes that dramatically fail reliability tests while performing honorably under current industry standards. On the other hand, it is demonstrated that solder material suppliers are able to design robust formulas performing reliably under various environmental conditions and with a large set of components.

We showed that complex lead-less devices like QFNs create specific issues on account of their greater thermal mass, low stand-off, and the tortuosity of their outgassing channels. This architecture is prone to trap solvents and decomposition products, and it creates thermal gradients that alter the complex chemical processes at play during reflow. While these processes were studied in detail, it is difficult to discriminate their impact. Regardless, the general differences observed between open architectures (BGAs, capacitors, open conditions) and QFNs indicate that the outgassing effects are prevalent. A specific design of experiments is required for demonstration.

These results highlight the importance of the design of representative qualification protocols for electronic assemblies, in terms of architecture and end-usage environment (T, RH, voltage gradients). This requirement becomes critical when low stand-off components are to be used—a common trend of today's electronics industry. Consequently, there is a need to update the testing and qualification standards, and we certainly hope the customized boards presented here will participate in this reflection.

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*The Evolution of
Interconnect Innovation*

Fan-out packaging: a key enabler for optimal performance in mobile devices

By Cassandra Melvin, Roger Massey [Atotech Deutschland GmbH]

As technology becomes more advanced and innovative, smartphones are increasingly thinner and are adopting larger, higher definition displays, while providing higher speed connections with better overall power efficiency. All just to satisfy our never ending demand for faster, higher tech devices, with maximum battery life [1]. Advanced packaging technologies, and in particular fan-out wafer-level packaging (FOWLP), enable manufacturers to deliver these features by overcoming key processing challenges using packaging innovation.

The emergence of FOWLP has been directly linked to satisfying the changing requirements for consumer electronics, and particularly those of mobile devices. This article will explore the drivers behind fan-out packaging, the key processing challenges, and the requirements at the application level. It will also discuss why fan-out is the ideal packaging technology for future generation mobile devices, and will present a turnkey electroplating solution for manufacture within both the current wafer, and the much anticipated larger panel format.

Smarter mobile phones require innovative approaches to both IC manufacturing and packaging. Moore's law has been pushed to its limit and is being surpassed by a new momentum for "More than Moore." This new approach to advancing technology requires packaging solutions to push technical boundaries and enable increased integration and performance, with fan-out packaging being considered as an ideal technology to achieve this.

What is fan-out packaging?

A fan-out package can be defined as IC packaging wherein the interconnections are fanned out of the chip area and therefore bumping is not dependent on the die surface [2]. Another distinguishable feature is that fan-out packages use an epoxy mold compound to fully embed the dies, rather than placing them upon a substrate or interposer as in other packaging types.

There are a variety of fan-out packaging types, with varying levels of integration and architecture complexity.

While the FOWLP process sequence varies from one manufacturer and packaging variant to the next, the baseline processes are generally comparable. An adhesive material is applied to a carrier wafer and one or multiple die are then placed face down onto the adhesive layer. This is followed by a wafer-level over-molding, which essentially embeds the die(s) into the molding layer. Debonding is next in the process, during which the carrier wafer is removed from the newly reconstituted over-molded wafer, thus exposing the active area of the die. Redistribution layer (RDL) formation is next, which occurs across the increased area of the over-mold, followed by soldering, and finally die singulation [2].

For current and next-generation mobile devices, ultra-thin and high-density packages are needed. Fan-in package types known as wafer-level chip-scale packages (WLCSP) had previously been the preferred technology for smartphones (Figure 1), as the package offers a relatively small

form factor and footprint. The downside, however, is that WLCSP tends to have limited I/O count (approximately 200) and a minimum package profile of 0.6mm [3]. When dealing with a pitch shrink, CSP suffers processing challenges as the area available for I/O layout is limited to the die surface. Fan-out packaging, however, does not have this limitation as the technique allows for the redistribution of I/Os beyond the die surface and onto the over-mold which, in turn supports a thinner package down to 0.4mm [3]. The benefits of a higher I/O density and thinner package will be discussed in the next section.

Fan-out: key drivers

Key drivers for the industry to pursue fan-out packaging technologies are discussed in the following sections.

Better performance. Mobile devices, and particularly smartphones, have become ubiquitous in our daily lives. Smartphones are no longer considered to be phones, but rather pocketable, personal computers; it's been reported that nearly 80% of smartphone owners reach for their phone within the first

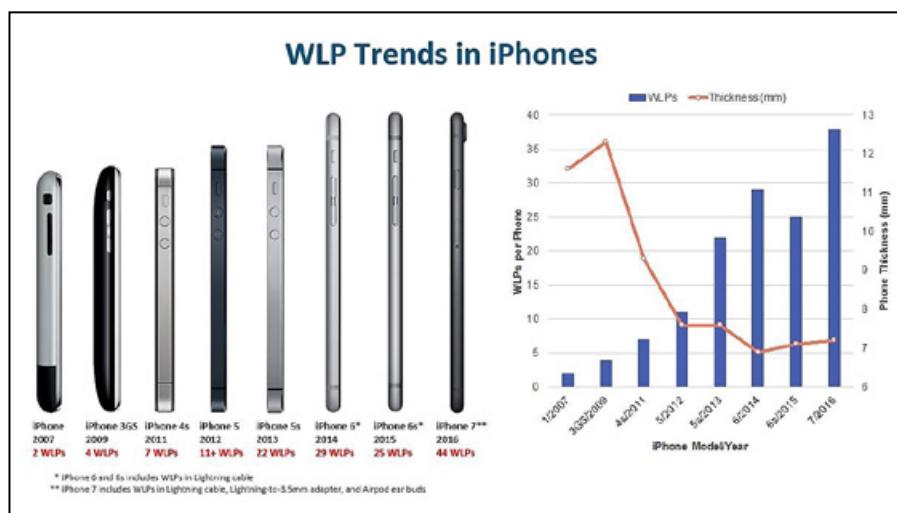


Figure 1: The image shows the decreasing thickness of handsets and the increasing number of wafer-level chip-scale packages (WLCSP), a fan-in technology. Some of these CSPs may be replaced or integrated into FOWLP for future generations of mobile devices. SOURCE: TechSearch International

fifteen minutes of being awake, and spend an average of 132 minutes communicating on their smartphone throughout the day (**Figure 2**) [4]. To support such a high level of activity, a smartphone must be robust and offer best in class performance.

For microprocessors, best in class performance refers to optimized reliability, including both thermal and electrical performance. Product or component

Additionally, more physical connections to the printed circuit board (PCB) enable better heat flow, which is critical for thermal performance. Power dissipation is necessary to effectively remove the heat generated by the IC when in use, as overheating due to poor power dissipation leads to IC malfunction and/or destruction. This is particularly critical in mobile devices where heat management is an issue.

achieve this using fan-out packaging.

Both heterogeneous and homogeneous integration are achieved by embedding more ICs and passives within the same package and also by utilizing more complex packaging architectures. One example is the multi-chip package, wherein multiple dies of various functionalities are embedded into a mold compound within the same package. Another way to achieve more integration and functionality is to use a package-on-package, such as TSMC's reputable InFO package (DRAM on APE) which is used in the latest iPhone models [6]. There are numerous other fan-out packaging technologies that employ 2D, 2.5D, or 3D architectures in order to maximize integration; i.e., system-in-package (SiP), multi-chip module (MCM), and stacked dies, among others.

Smaller form factor. The aforementioned drivers – performance and functionality – are directly correlated to another key driver: smaller form factor. Manufacturers are tasked with building next-generation smartphones, with better performance and more functionality than their mobile predecessors, while not compromising the sleek and slim design that consumers so fervently demand. Therefore, next-generation smartphones require denser packages, which are made possible by transistor scaling (Moore's Law) or advanced integration using innovative packaging technologies.

Through implementation of die embedding, in combination with the fine-feature processes possible with wafer processing, FOWLP minimizes the number of RDLs required to form a high-density package while not suffering from excessive cost penalties. As the RDL can be formed across the whole over-mold area, it is possible to eliminate the need for an IC substrate or interposer altogether, which decreases the form factor considerably over traditional packaging techniques.

With integration, and specifically, by embedding multiple die within the same package and with use of innovative packaging architectures, form factor can be reduced even further. According to C. C. Wei, co-CEO at TSMC, InFO technology enables a twenty percent reduction in package thickness [5]. Meanwhile, Yole Développement has estimated that the form factor reduction provided by fan-out packaging is at least 40% compared with standard flip-chip packaging [3]. Flip-chip, currently the more prevalent packaging technology in high-volume production, requires an IC substrate that results in a

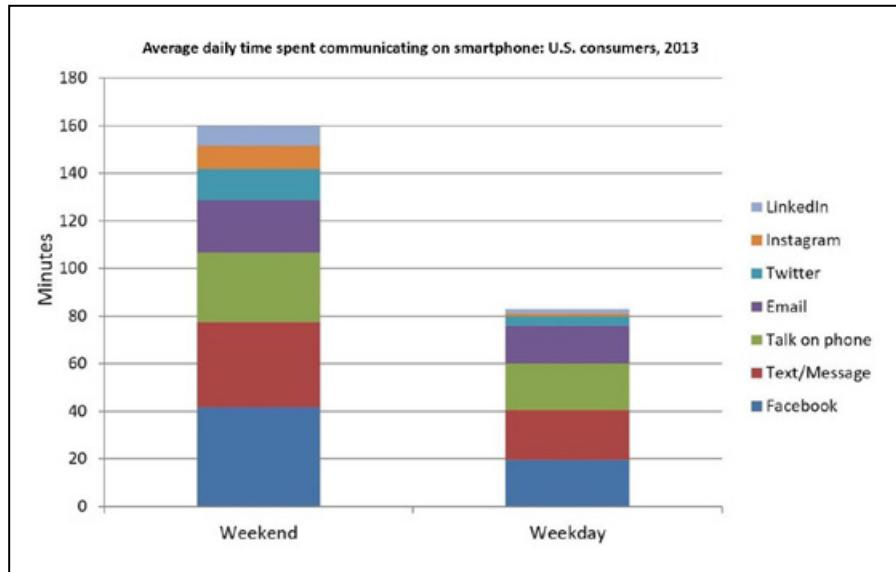


Figure 2: The diagram shows the average daily time spent communicating on smartphones according to [4].

reliability performance ultimately determines the lifetime of the device, as well as its ability to perform multiple tasks quickly, concurrently, and consistently over an extended period of time. As such, one key measure of any package is electrical performance. Where multiple die are embedded in a single FOWLP, when compared to other packaging techniques, the overall electrical path is shorter, resulting in faster signal transmission and improved electrical performance. This provides a considerable technical advantage and positions FOWLP as an ideal technology for high-speed, high-performance devices.

Higher I/O density. Redistribution layers serve as a rerouting of the I/O layout and enable a higher I/O count. A high I/O density generally begets better electrical performance, as more outputs results in faster electrical signals between die and minimizes the risk posed by electrical shorts. A higher I/O density also enables the package to perform more operations in parallel. Therefore, a high I/O count allows for more complex, high-speed die to be packaged.

As previously mentioned, in FOWLP the bumping is not dependent on the die surface and therefore a higher I/O density can be achieved by fanning out the electrical interconnections with the implementation of more RDLs. In the most advanced fan-out packages, up to four RDLs may be used for the purpose of maximizing I/O density, which in turn facilitates improved electrical and thermal performance, including power dissipation. In the case of TSMC's InFO, a 10% improvement in power dissipation is achieved using fan-out packaging [5].

More functionality. Smarter phones deliver more functions for the user, through greater memory storage, more sophisticated cameras, faster WiFi®, touch screens, voice recognition, high-performance CPUs, longer battery life, and motion sensors that are essential for mobile gaming. The trend, however, is towards thin phones, which poses a challenge for IC and packaging manufacturers: how to fit more functionality into slim smartphones? The answer is integration, and there are various ways to

larger form factor and footprint than that of FOWLP. The use of a multilayer substrate in flip-chip packages also contributes significantly to the overall manufacturing costs when compared to FOWLP, which uses a low-cost mold material.

The technical benefits of FOWLP are numerous, substantiated, and increasingly difficult to ignore: 1) better reliability performance by means of embedding and more RDLs; 2) more functionality and higher levels of integration through multi-chip embedding and complex architectures; 3) form factor reduction via innovative architectures; and 4) substrateless embedding technologies for reduced manufacturing costs. For these reasons, the semiconductor industry will witness the substantial and widespread adoption of FOWLP technologies in the coming years.

Fan-out: exponential growth

Frequently described as a disruptive technology, fan-out will change the packaging landscape with further adoption by outsourced semiconductor assembly and test suppliers (OSATS), integrated device manufacturers (IDMs), and foundries alike. Fan-out packaging, while having recently gained momentum with the entrance of TSMC's InFO, is not a new technology, however. Embedded wafer-level ball grid array (eWLB) is a type of fan-out packaging that has been in production at Infineon for nearly a decade [7]. Variations of Infineon's second-generation eWLB technology have been co-developed, qualified, and/or licensed by companies such as STMicroelectronics, STATS ChipPAC [8], NANUM S.A., and ASE [2]. Other types of fan-out packages are being produced in low volume at Nepes and Deca Technologies [2].

TSMC's entry with its innovative InFO technology has, and will continue to have, a far reaching and lasting impact on the fan-out market. If Apple continues to use InFO PoP technology in future generation iPhones, surely there will be followers.

In absolute numbers, the expected growth in fan-out technologies will be exponential, going from \$244M in 2015 to \$492M in 2016, and sprouting up to \$891M in 2017 [2]. According to [2], the forecast for 2021 is a remarkable \$1.3B with substantial growth in both the eWLB and PoP market segments. Market reports by JMS [1], TechSearch International [9], and Prismark [6] similarly forecast substantial growth for fan-out packaging.

Fan-out: key challenges

The technical advantages and the forecasted market growth, position fan-out as the preferred advanced packaging technology for next-generation mobile devices. However, there are several process challenges associated with fan-out packaging: warpage, die shift, yield, and the transition to panel-based manufacturing [2].

Warpage is a critical processing challenge for fan-out based technologies. When thinner packages are used, in addition to heterogeneous materials and more Cu layers (RDLs), wafer bowing occurs after processing. Wafer bowing is a result of unequal stress distribution over the wafer and influences yield. To overcome this, manufacturers must optimize their process sequence and fan-out design [10].

Die shift is another process challenge and is a result of the slight movement of the die, after placement on the carrier wafer and during the over-molding process. Die shift is a challenge for wafer-based technologies, however, with the desired migration to panel formats, die shift becomes even more critical, as the equipment to handle the consistent and accurate die positioning on a large square format are simply not yet proven. Die shift impacts yield, which is one of the primary concerns for both wafer- and panel-based fan-out packaging.

Qualcomm has stated that a 300mm wafer produces approximately 616 packages, compared to 1,911 from an 18 x 24 inch panel (10 x 10mm package size) [3]. Therefore, a transition to panel-based fan-out packaging would enable significant cost savings for manufacturers, but only if the infrastructure is available and capable. Unfortunately, existing panel-based PCB equipment is not prepared to successfully address the requirements for miniaturization, RDL pitch down to 2 x 2 μ m, as the tools are not designed for such fine dimensions. This is one of the many reasons why a direct transfer is not currently possible onto standard PCB equipment. Equipment manufacturers and material suppliers are also not currently able to offer solutions for overcoming panel warpage and die shift. Finally, standardization is also a challenge, as PCB manufacturers utilize a wide array of panel sizes.

Fan-out: Cu plating application requirements

The following sections discuss requirements for Cu plating applications relative to fan-out packaging technologies.

Requirements for RDL. Trends for next-generation mobile devices – thinner smartphones with more functionality – require miniaturization at all levels. For advanced packaging technologies, miniaturization involves decreasing the RDL pitch down to 2 x 2 μ m and below. Redistribution layers are essential to fan-out technologies, as it is with more RDLs that I/O density is increased. Successful formation and plating of such fine features pose a challenge for both suppliers and manufacturers, with the plating challenge being the simultaneous plating of fine lines and spaces (2 x 2 μ m), large Cu pads (up to 300 μ m), and in some cases also microvias (example: 5 x 10 μ m) with a deposition rate that optimizes throughput.

Requirements for Cu pillar. Cu pillars are needed for certain types of fan-out packaging such as package-on-package (PoP), in various dimensions including both standard pillar in the range of 40 x 50 μ m and tall pillar in the range of 200 x 50 μ m. The standard performance requirements – high-throughput, high-yield, and optimal reliability performance – can be met with an optimized Cu pillar process that enables uniform and pure Cu deposition using high-speed plating. High-speed plating will result in a higher throughput, however it also increases the risk of voiding in the intermetallic phase of Cu and SnAg (**Figure 3**) and influences uniformity, both of which impact the electrical performance and yield. The purity of the deposit, and specifically the presence of organic co-deposition, also influences the voiding performance. Therefore, a good Cu pillar process should enable high-speed plating of pure and uniform Cu. This can be achieved with the right organic additives and high-speed plating equipment that collectively reduce the occurrence of organic co-deposition and optimize uniformity.

When electroplating tall Cu pillars, the situation becomes more complex, as high aspect ratio structures are more difficult to plate in a timely manner. Structures with a 1:1 aspect ratio (AR)

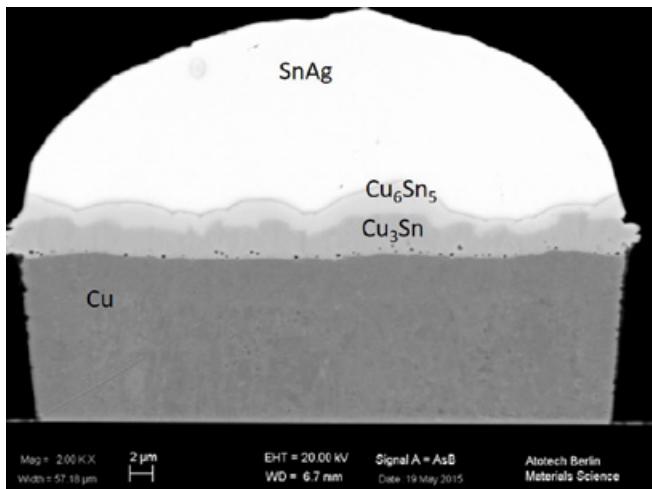


Figure 3: The image shows void formation in the intermetallic phase between Cu and SnAg. The voids appear as small black spots.

are efficiently plated with primarily convection-controlled plating, however structures with ARs up to 4:1 involve a different plating mechanism (**Figure 4**).

During plating of high AR structures, mass transfer via diffusion occurs at the pillar base, while fluid exchange via convection takes place at the top of the

pillar structure. As the diffusion layer thickness increases, the limiting current density decreases, making it more difficult to achieve a rapid deposition speed at the bottom of a high AR structure. Therefore, for fast plating of high AR structures, the diffusion layer thickness should be controlled.

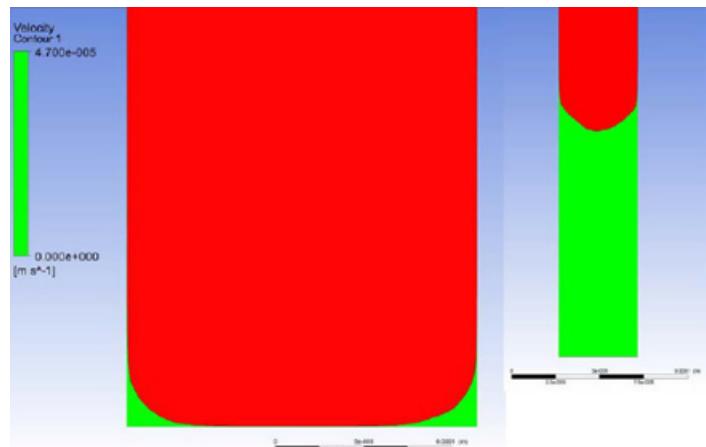


Figure 4: The diagram illustrates the prevalence of diffusion speed (green), in comparison to convection (red), for high aspect ratio (HAR) pillars. The approximate ARs are 1:1 (left) and 4:1 (right).

For plating low AR (1:1) structures, convection supports fast plating, and therefore the electroplating equipment has the primary role of facilitating deposition. Electroplating equipment with systems and features that enable optimum and direct electrolyte flow and programmable agitation enable high-current density



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plating, and when coupled with the right organic additives and reverse pulse plating capability, will support optimized uniformity and limit organic co-deposition, to produce a pure Cu deposit.

Electrolyte flow, agitation, and the additives, however, have limited influence on diffusion-controlled mass transfer or its limiting current density. Plating beyond 90% of the limited current density will result in dendrite formations in the Cu grains, as shown in **Figure 5**. Excessive dendrite



Figure 5: An example of dendrite formations in a Cu deposit.

growth hinders soldering, causes shorts between Cu RDL lines when plating RDLs, and negatively impacts reliability. Therefore, for high-speed plating of high AR pillars, the limiting current density must be increased. To increase the absolute value of the current density in the bottom of the pillar structure, where diffusion occurs, certain process parameters may be modified. Temperature and the Cu content of the electrolyte should be increased, and acid concentration must be optimized.

In summary, the applicable current density that can be applied for defect-free plating of high AR pillars is lower than that for plating structures with dimensions similar to standard pillars ($40 \times 50\mu\text{m}$), resulting in a longer plating time and consequently lower throughput. To achieve defect-free and high-speed plating of tall Cu pillars, the right organic additives and high-speed plating equipment are needed, as well as a process that optimizes temperature, the Cu electrolyte content, and the acid concentration.

A turnkey solution for Cu plating in fan-out packaging

Atotech offers a turnkey plating solution (chemistry and equipment) that

satisfies all aforementioned requirements for RDLs and both standard and tall Cu pillars. In addition, we offer a chemistry-only Cu plating process for plating RDLs and pillars.

Spherolyte Cu process. Our Spherolyte process includes high-purity chemistries and organic additives for Cu plating. We have a specially designed Cu RDL and pillar plating process for use in a newly developed equipment (MultiPlate) for very high-speed plating, as well as standard electrochemical deposition (ECD) plating equipment. Both processes satisfy all aforementioned requirements for the Cu deposit while providing a high deposition rate [11].

MultiPlate. Our MultiPlate is an ECD plating tool for very fast deposition of Cu. It is equipped with technical features that enable optimal electrolyte flow, programmable agitation, and reverse pulse plating at very high-current densities. To date, plating results generated in this tool demonstrate a better performance, in terms of deposition rate, uniformity, and the purity of the Cu deposit, than industry standard Cu plating solutions. When plating very thick Cu, as in the case of tall Cu pillars, the advantage of very high-speed plating is even more substantial.

The technical benefits of MultiPlate's key features [12] include: 1) advanced fluid delivery; 2) segmented anodes that enable adjustable current distribution by segmentation for optimized uniformity; 3) free programmable agitation that allows for the precise movement of the substrate for optimized agitation and flow; and 4) pulse reverse plating that enables the control and stabilization of the Cu pillar plating performance with physical parameters, thereby eliminating the need for a leveling additive.

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Biography

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How process variables affect variation in voiding on bottom termination components

By Brook Sandy-Smith [Indium Corporation]

Voiding under bottom terminated components (BTCs) is a challenge for the electronics industry. Currently, common assemblies require a large number of quad flat no-leads (QFNs) devices, and these assemblies will often include several different types of BTCs. These components have flat terminations with a surface finish on the underside of the component, often with no exposed leads or solder joints. Typically, the center of the component has a large thermal ground pad with additional signal leads around the perimeter. Initial assembly testing will assure continuity on the signal leads, but in some cases this does not prevent field failures. These field failures can be attributed to poor thermal conductivity in the center solder joint leading to overheating and die cracking. Poor thermal conductivity results from discontinuity in the z-axis of the solder joint on account of voids in the solder joint.

Addressing the challenges

Inspecting BTCs can be challenging because there are concealed solder joints, requiring X-ray scans of the assemblies (**Figure 1**). X-ray imaging gives a 2-dimensional view of the component and designates lower density areas with lighter contrast. Software is then used to quantify the percentage of the area that shows voids, the size of the largest void, and total number of voids. It is also important to look at the images of perimeter solder joints as bridges can be detected and varying shapes can sometimes indicate variations in component coplanarity.

Optimizing an assembly process to minimize voiding will mean looking more closely at many aspects of the assembly. Minimum voiding is not easily achieved by changing one part of the process or simply switching solder materials. Many different assembly scenarios have been investigated when voiding has played a part in failures. The contributing factors are varied and are grouped into three types of factors: design,

process, and material. **Figure 2** shows some examples of variables critical to consider in efforts to optimize performance.

There are two main mechanisms that contribute to void formation: poor wetting and volatile entrapment. First, areas that do not allow the solder to wet well will cause inconsistency in solder joint formation and increase the probability for voiding. Poor wetting is often caused by deterioration of the surfaces of components and pads. Surface finishes protect copper pads from oxidation in contact with air. They also serve as a barrier to solder joint formation because the flux or metallurgy must make a bond despite the presence of the surface finish. In this way, surface finishes can vary greatly in their impact on voiding. Solder paste flux works to remove oxides and enhance wetting.

The second mechanism – volatile entrapment – is uniquely challenging with BTCs because of the large covered area and low standoff between the components and the board. During reflow, board and solder materials that contain volatile compounds will outgas. These gases freely escape around other components because they are not constrained by the tight spacings found in BTCs. Once liquidus is reached in reflow and the solder alloy melts to form the solder joint, any remaining entrapped gas can form bubbles. Many of these bubbles are pushed to escape by the surface tension of the liquid solder, but those that do not escape before the alloy solidifies will be present in the solder joint as voids.

While focused on

voiding, it is easy to lose sight of the most critical factor in assembling BTCs: standoff height. Component manufacturers recommend a certain amount of standoff provided by the solder joint. Component manufacturers recommend that the minimum acceptable standoff is around 50 microns. This is typically measured through destructive analysis such as cross-sectioning and using SEM imaging for measurement. Some X-ray machines are now also capable of topographical analysis that can detect height and coplanarity. If the solder joint is less than this minimum thickness, there will not be enough solder to bridge the gap for coefficient of thermal expansion (CTE) mismatches between the board and component. This can lead to additional functional failures, with

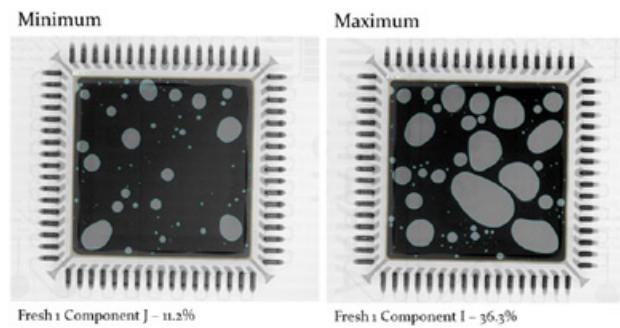


Figure 1: QFN voiding X-rays showing examples of minimum and maximum values with analysis.

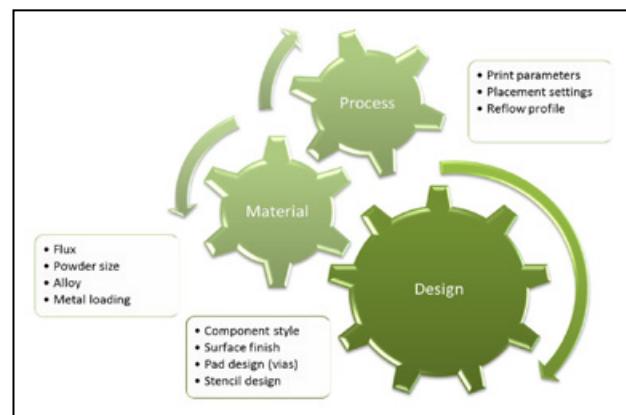


Figure 2: Diagram of assembly process variables.

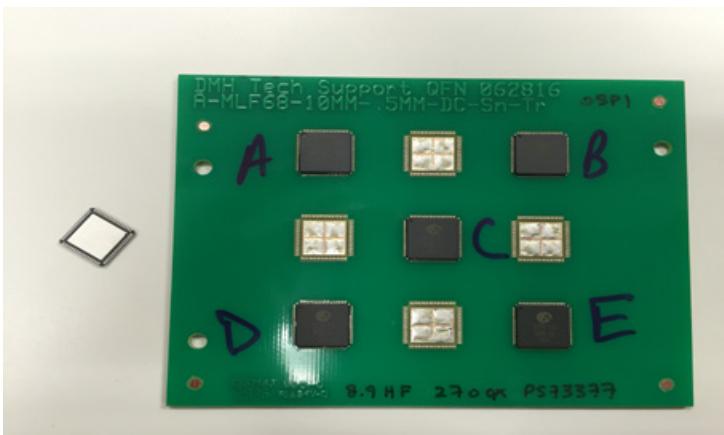


Figure 3: Test board design with QFNs and window-pane stencil design.

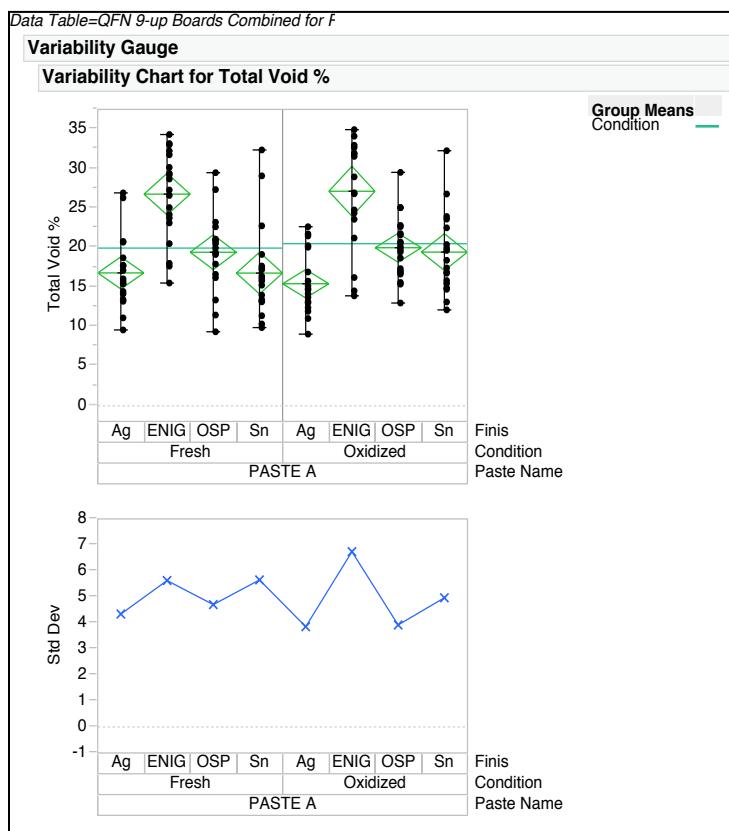


Figure 4: Results of surface finish comparison testing.

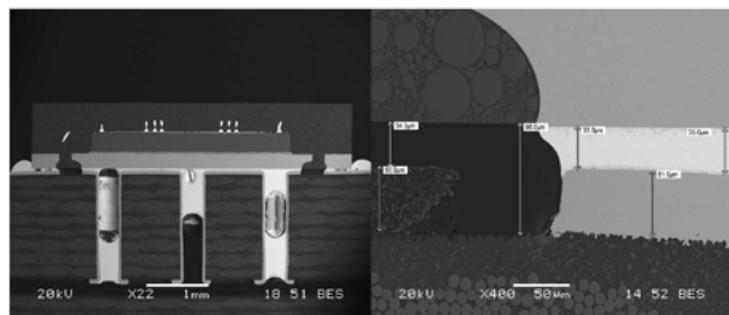


Figure 5: Example of worst case solder escaping into vias, thereby reducing standoff height.

only a tenuous link to voiding. Solder joints with sufficient standoff have shown acceptable performance in accelerated life testing with voiding up to 50% [1]. This does not take into account the thermal load required for the component to function optimally, but does demonstrate the robust nature of the solder joints associated with BTCs.

Case study of factors contributing to voiding

Factors contributing to voiding were evaluated in a case study. A summary of the results is presented below.

Surface finish and component cleanliness. Investigating the impact of surface finish on the boards and components is critical because it contributes greatly to the function of solder wetting and variations in voiding performance. In this case, we studied the voiding for one solder paste, one component design, and one board design, while varying surface finish and level of oxidation.

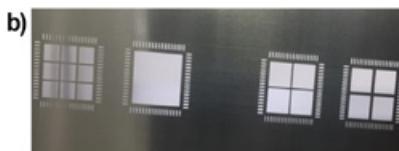
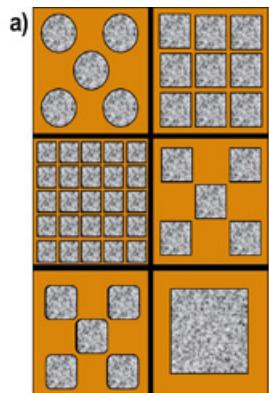
This design uses a commercially available dummy QFN with a tin finish. Because components are placed only on five locations in **Figure 3**, it is possible to see how the solder has wet to the central pad and perimeter pads. The stencil design is broken into quadrants to minimize component floating during liquidus and to form channels to encourage volatile escape. These boards were tested with four surface finishes: ENIG, OSP, immersion silver (Ag), and immersion tin (Sn). Some boards were also tested in an oxidized condition, achieved by sending the boards through the same reflow profile twice before printing the solder paste and reflowing again.

In **Figure 4**, there are mean lines in each box to show that the oxidation of the boards played little role in voiding differences (less than 1% difference compared to a spread of data around 30%). ENIG boards had increased variation. The diamond plots summarize the scatter of data points to show the mean and represent the variation. The ENIG finish corresponded with higher amounts of voiding, which is an unexpected result. Typically, the ENIG finish is chosen to be the best oxygen barrier.

Pad design and vias. The test board design used for material comparisons was designed with flat pads. Functional assemblies often include vias in the central pad. These vias aid in conducting heat from the component die. There are several different designs for thermal vias; typically they are plated through-holes, sometimes with a plug or barrier on top to discourage solder from wicking into the vias. When solder can flow into the vias, a considerable portion of the solder volume is displaced, leading to insufficient standoff height.

The cross-sectional images in **Figure 5** show a worst case example with open-plated vias. The standoff height is reduced to 35 microns and the solder on the perimeter solder joints has been squeezed out. The external bumps of solder form an interior corner at the edge which will contribute to crack propagation. Many industry leaders have developed solutions to this problem. The main focus is to keep solder away from open vias where vias cannot be plugged. Some of these new strategies, such as via-in-pad plated over (VIPPO) [2], balance via design with solder mask patterning and stencil design to ensure there is enough solder volume to maintain lower voiding and create a robust solder joint.

Stencil design. When discussing the need to have enough solder volume for a robust solder joint, it is necessary to consider stencil design. The first priority is to calculate the appropriate volume of solder paste on the perimeter solder joints. Too much solder here can contribute to bridging, while too little can increase the propensity for the component to tip. Perimeter pads should not extend very far past the edge of the component, especially if there are not plated leads along the edge. Next, the focus is sizing and



Pattern	Area Reduction	Theoretical	Alloy Volume % of
9 Thin Pane 4 mil	12.9%	0.4%	
9 Thin Pane 5 mil	12.9%	-19.7%	
9 Wide Pane 4 mil	24.9%	-13.5%	
Full Pad 4 mil	0.0%	-7.8%	
Full Pad 5 mil	0.0%	15.2%	
Quadrants Fine Pane 4 mil	6.6%	-13.9%	
Quadrants Fine Pane 5 mil	6.6%	7.6%	
Quadrants Wide Pane 4 mil	12.9%	-19.7%	
Quadrants Wide Pane 5 mil	12.9%	0.4%	

Figure 6: a) Recommended stencil designs from component manufacturer guidelines; b) Stencil design for test design and geometric values.

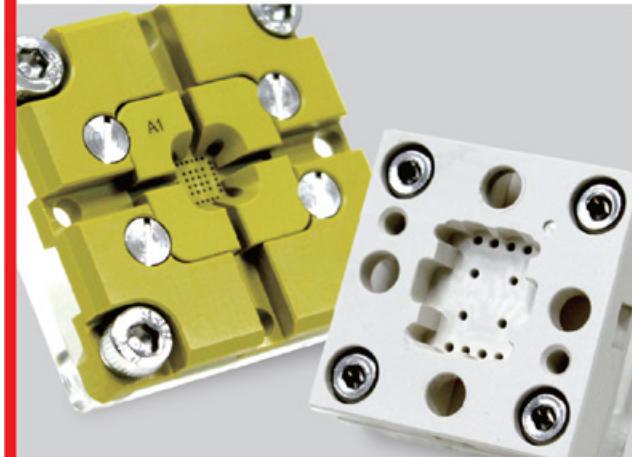
distributing solder deposits to fill the central pad. It is most common to print several deposits on this pad for two reasons: to minimize lifting or floating of the component due to the surface tension of molten solder and, secondly, to keep solder from flowing into vias.

Component manufacturers often recommend designs as illustrated in **Figure 6**, which suggest area coverage between 37% and 81%. Considering that area reduction geometrically, it seems logical that voids would emerge as the volume of solder is less than the theoretical space to be filled. Continuing on this path of logic that solder paste volume should be adjusted to assure sufficient solder alloy to fill the expected volume of the solder joint for appropriate standoff, stencil designs were chosen to vary area coverage and resulting solder alloy volume. These stencil designs were tested with a 4 mil foil as well as a 5 mil foil to give an apples-to-apples comparison of a clear 25% increase in solder paste volume. The table in **Figure 6** shows calculations for each stencil design. This assumes a 50 micron standoff for the full pad as theoretical volume.

Figure 7 compares the results of two solder pastes: one is optimized for low voiding and the other is a legacy benchmark material. Paste A clearly shows less voiding overall and less variation. The different stencil designs do not have a large impact on the overall voiding percent. Comparing the stencil thickness, it seems the 4 mil designs have slightly more variation. Paste G shows a higher average and more variation overall. The full pad design yields a slightly lower average, but there is little difference between designs. The 5 mil stencil seems to have more variation, but also some very low values. Discussion of these results has led to two hypotheses: component cleanliness plays a significant role in the incidence of high values, and/or another factor such as placement height contributes significantly in the case of pastes with a propensity for void formation. This second hypothesis reinforces the importance of standoff height, not only after reflow, but also after placement. It should also be noted that these results would likely show greater differentiation if the board design included vias or solder mask patterning to match the stencil designs [3].

Material selection. Solder paste is comprised of powder with a given alloy composition and flux. The ratio of metal to flux, typically expressed as metal loading by weight, can affect voiding. Higher metal loadings can be favorable because the thicker paste maintains more standoff height during preheat. Decreasing powder sizes can pose a challenge due to increased surface area of oxidation. In addition, some solder alloys intrinsically have different voiding performances because of differences in wetting characteristics, surface tension, and oxidation resistance. On the other hand, there are several aspects of flux that can contribute to voiding under BTCS: how strongly the flux prevents oxidation and promotes wetting, and how the flux volatiles evolve during reflow. Solder pastes specifically designed to reduce voiding often achieve this with trade-offs in other areas of performance, such as stability or printing performance.

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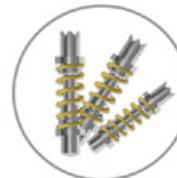
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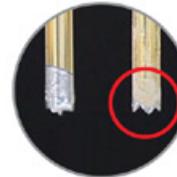
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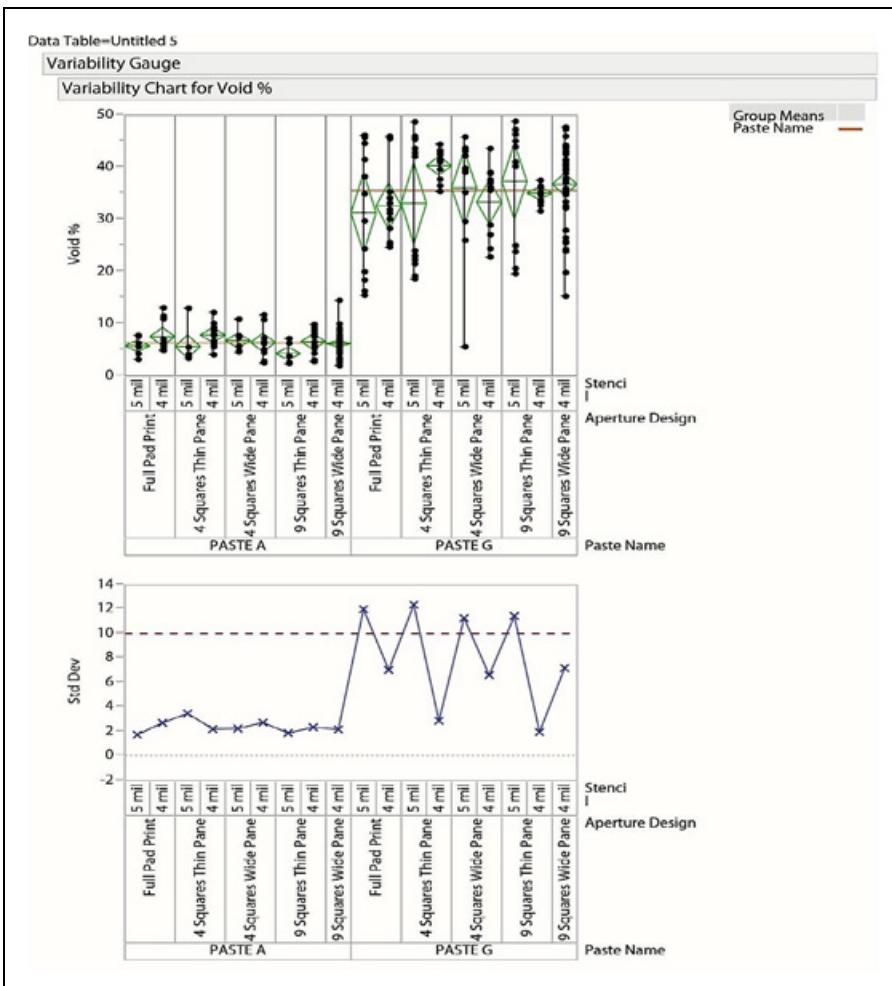


Figure 7: Results from the stencil design investigation.

Referring again to **Figure 7**, this is a typical material comparison. All process and design factors should be kept constant aside from solder paste selection. Often the comparison is conducted at more than one reflow profile to allow for process preferences, or in this case, different stencil designs. The difference between Pastes A and G is quite pronounced; typically, one material will not show such a dramatic improvement.

Addition of solid solder preforms. In many cases, especially for designs with open vias, it might not be possible to stencil print enough solder paste to supply the solder volume needed. Solid solder preforms can be used to add solder volume without adding flux volatiles. There are two prevailing strategies here: use a preform that is thin and flat with dimensions slightly smaller than the central thermal pad and place into paste [4], or use a preform in a standard size similar to a 0402 component, which will tilt the component temporarily, but coalesce completely during reflow [5].

Reflow profiling. Reflow profile optimization is often a first go-to solution

because of its ease of modification. Different materials may have different unique preferences, but there are some trends that impact voiding performance [6]:

- If the preheat is too quick, there is not enough time for volatiles to evolve and escape before the solder is molten;
- If the preheat is too quick, the paste can slump, reducing the standoff and preventing the escape of volatiles;
- If the profile is generally too short, volatiles will be more easily entrapped;
- Low peak temperature tends to require more time for complete solder wetting;
- Excessive peak temperature or profile length results in oxidation on surfaces, increasing the potential for voiding; and
- Reflow in nitrogen leads to lowest voiding results.

Investigations have often shown that voiding can be minimized with a longer or hotter profile. However, these investigations are typically conducted with a focus only on BTCs. It is important to always consider

the full assembly when profiling. For production assemblies, the process window will be limited by several factors: component maximum temperatures, oxidation resistance on large components, avoiding graping on small components, etc. When creating an optimal profile for voiding on a production assembly, profiling to minimize voiding must be tempered with attention to the other challenging parts on the assembly.

Summary

Voiding under BTCs is a complex challenge. The results shown here were collected from studies designed to investigate the impact of different variables independently. When approaching process optimization on a production assembly, the best solution will come from considering each one of these factors and how variations in those factors has affected variations in the assembly process. The most common cause of a voiding investigation is a sudden increase in the incidence of voiding. Sometimes design parameters change and cannot be modified — then we look to modify process or material variables to bring voiding levels back into range. No matter the cause for investigation, many factors may be at play in exacerbating voiding in BTC assemblies.

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Evolution of impedance-controlled coaxial test sockets and IM material application

By Jiachun Zhou (Frank), Dexian Liu, Nhon Huynh, Kevin DeFord [Smiths Connectors, Smiths Group]

As the speed or frequency of semiconductor integrated circuit (IC) chips increases continuously, the test socket and contactor industry has been driven to develop new technology solutions for testing IC packages at higher frequency. Many advanced sockets and contactors have been developed during the last decade to address the requirements from high-speed IC chip makers. Generally, there are two basic approaches for high-speed IC test sockets, one with shorter contactors in order to reduce the socket's electric transmission path, and another with an impedance-controlled coaxial structure to match the impedance of contactors to tested IC chips and test boards. For example, the spring probe, one of the primary contact technologies used in IC chip testing, has become increasingly shorter, with the working length reduced from more than 6mm down to ~2.5mm over the last 15 years. On account of the mechanical limitations in spring probe size reduction, impedance controlled sockets with coaxial structures have become another valuable solution for testing high-speed IC chips with success. This paper will introduce the basics of coaxial structures and impedance matching, evolution of coaxial test sockets, and the application of IM (insulated metal) material in this structure.

Technical challenges in test socket applications

It is well known that signal discontinuity in transmission lines and interconnects (or contacts in test sockets) can affect the signal integrity (SI) performance when testing high-speed IC chips. This discontinuity is mainly caused by mechanical features in the interconnect that may result in impedance change vs. the IC chip. To achieve the best SI performance in IC chip testing, it is required to maintain constant impedance within the test socket, such as 50Ω , which matches that of the IC chip's impedance. However, because of the limitations of mechanical features, it is hard to control

the impedance of traditional plastics used in test sockets. One common approach to maintain constant impedance or achieve controlled-impedance is a coaxial structure that has been widely applied in transmission lines and some interconnects. Application of coaxial structure in IC chip test sockets began about 15 years ago. Since then, various coaxial structures have been developed in the test socket industry.

The basic theory of coaxial structure for controlled-impedance can be expressed as the formula below and [Figure 1](#):

$$Z_0 = \frac{138}{\sqrt{\epsilon_r}} \log_{10} \frac{D}{d}$$

Where,

Z_0 : Impedance;

ϵ_r : Relative dielectric constant

D: Dielectric layer outside diameter (or grounded metal body cavity internal diameter); and

d: Conductor or contactor diameter.

Following the formula, the impedance of the coaxial structure is affected mainly by signal conductor (or spring probe as an example) diameter and the dielectric constant of the dielectric material between the spring probe and grounded metal. [Figure 1](#) shows air as the dielectric medium—notice its low dielectric constant ($\epsilon_r = 1.0$). Most coaxial transmission cables use composite insulation material with higher dielectric constants ($\epsilon_r \sim 2.0$). If using a lower dielectric constant, the thickness of the dielectric layer

can be thinner to accommodate a larger metal conductor diameter for better current capacity. The grounded metal body cavity inner diameter (ID) (equal to the cavity internal diameter) is mostly determined by the distance between two probes, or pitch, in the IC device package. Using spring probes as an example, in order to have more stable performance and improve manufacturing feasibility, a larger diameter "d" is expected. With a fixed impedance, such as 50Ω , and a pitch of 0.8mm, the signal pin diameter is 0.3mm in air ($\epsilon_r = 1.0$). If a higher dielectric constant material is used, such as $\epsilon_r = 2$, the signal probe diameter "d" will be 0.22mm to achieve a 50Ω impedance. Therefore, selecting an interface dielectric material with a small dielectric constant is always preferred in an impedance-controlled coaxial structure.

Theoretically, the impedance-controlled test socket structure should follow [Figure 1](#), and have a spring probe with a diameter of "d" surrounded with dielectric material (air or insulation material) and grounded metal shield with a diameter of "D." The correlation between "d" and "D" must be represented as in the formula to achieve the required impedance. This ideal impedance-controlled structure is feasible and widely used in long signal transmission wires. But it is not possible to apply this ideal structure in package test sockets on account of a couple of challenges:

- 1) How to hold the signal pin in the center of the socket's cavity while retaining its position, without movement, over thousands of compression cycles in an IC chip test environment; and
- 2) How to insulate the power pins from a metal body, avoiding electric shortage, while maintaining mechanical stability.

Because the impedance-controlled test socket concept with coaxial structure was proposed many years ago, much development effort has been spent to solve

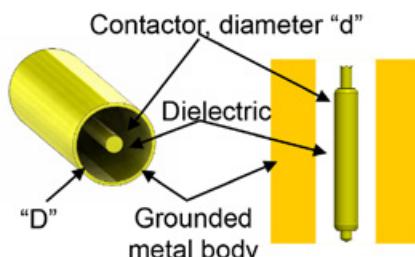


Figure 1: An ideal coaxial structure.

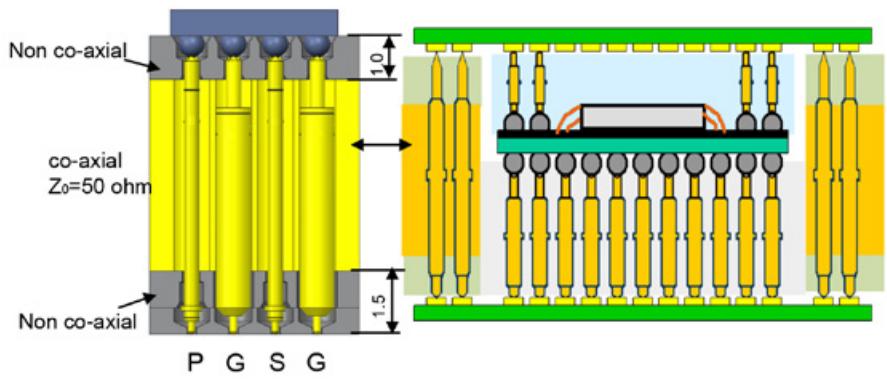


Figure 2: A sandwich coaxial structure and its application (P – power, S – signal; G - ground).

these challenges. Although various concepts have been proposed, only a few are applied in high-volume testing environments today including those that will be introduced here.

Evolution of the impedance-controlled socket with coaxial structures

A sandwich coaxial socket structure is the most commonly used impedance-controlled design. As shown in **Figure 2**, the sandwich coaxial socket has three layers: top and bottom layers made of high-strength insulating composite materials, and a middle layer consisting of a metal body. The middle layer has a coaxial pattern structure for signal pins to have impedance-controlled functions. The top and bottom layers retain the signal and power pins providing mechanical stability. The dielectric layer in the signal pin cavity is air, which has a dielectric constant of ~ 1.0 , the minimum achievable dielectric constant. Following the impedance calculation formula, the signal probe diameter “d” is usually very small, in the range of $0.20\text{--}0.3\text{mm}$ for a pitch in the range of $0.6\text{--}1.0\text{mm}$. One advantage of the sandwich coaxial structure is its well-grounded metal layer. Usually, a thicker middle metal layer can be used for better constant impedance. This sandwich coaxial socket structure is commonly used in package-on-package (PoP) device testing as the return path from an upper fan-out printed circuit board (PCB) to the bottom test board (shown in **Figure 2b**).

Obviously, the major weakness of the sandwich coaxial socket described above is the non-coaxial structure in the top and bottom plastic composite layers. As shown in the impedance distribution of the sandwich coaxial socket in **Figure 3**, the middle metal coaxial layer has a well-controlled 50Ω impedance, while the top and bottom layers have unmatched impedances. The actual

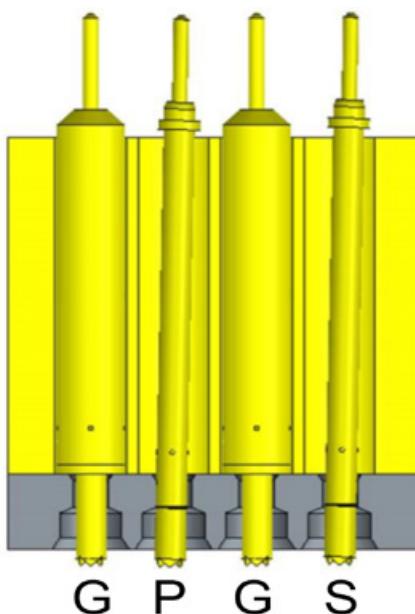


Figure 4: Signal (S)/power (P) pins status in assembly or maintenance.

impedances of the top and bottom layers may be predicted by SI simulation during socket design and are determined by a variety of factors including the composite materials selected, pin structure, and cavity dimensions.

Another weakness of the sandwich coaxial socket is poor manufacturing and maintenance feasibility on account of difficulties in retaining the spring probe's position. As shown in **Figure 4**, when the socket is placed upside down for assembly or maintenance, the signal and power pins are captured in the top layer cavity with limited thickness, which may cause the probe to move at an angle. The random tilting of signal probes in cavities affects socket assembly and probe replacement in the field. Increasing top layer thickness is one solution, but it will affect the signal integrity performance of the whole socket.

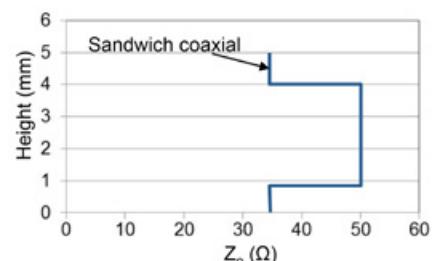


Figure 3: Z distribution in a sandwich coaxial (example).

Because of the challenges inherent in the sandwich coaxial socket, development efforts turned again to a full impedance-controlled coaxial structure. One solution to this challenge was developed by Smiths Connectors in the form of a patented socket material technology (IM, or insulated metal) and structure marketed under the trade name, DaVinci. This impedance-controlled coaxial socket features a metal body that is insulated on all surfaces, including top, bottom, and all signal and power pin cavities. DaVinci socket components are shown in **Figure 5**. A proprietary manufacturing process has been applied to generate a thin insulation layer on metal base components. This insulation layer ensures signal and power probes do not make contact with the grounded metal base material, while the ground probes are well-grounded by contacting metal cavity surfaces that are without an insulation layer. IM socket material is inherently very strong, which minimizes socket deflection generated by

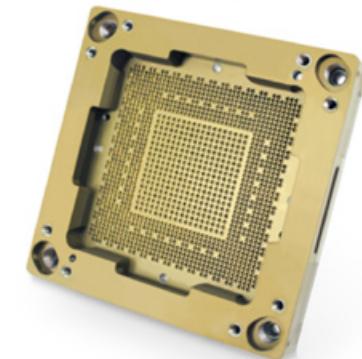
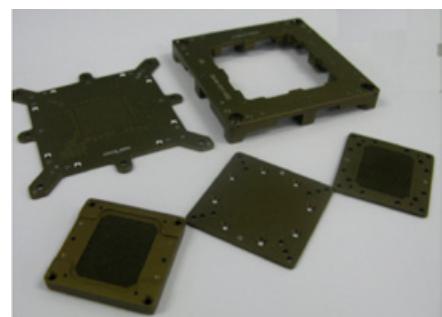


Figure 5: Insulated metal socket and components.

spring probe preload force when mounted on a test board. For example, plastic composite socket materials have a maximum deflection of $\sim 50\mu\text{m}$ in a 0.8mm pitch, 1750 pin count design. Using IM material in the same socket structure results in a maximum deflection of only $\sim 9\mu\text{m}$, significantly less than composite plastics. Most plastic composite materials will shrink or expand with humidity variation, but IM socket material eliminates this concern and provides dimensional stability.

While IM socket material eliminates the risk of signal and power pins shorting to a grounded metal base, the DaVinci socket structure also incorporates signal pin retention features. As shown in [Figure 6](#), a specific feature is added in the signal pin cavities to hold the signal pins. This allows

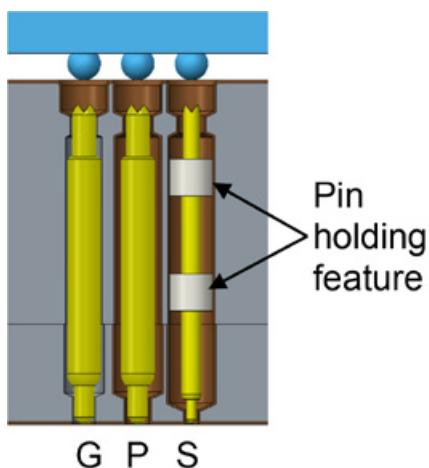


Figure 6: DaVinci socket structure.

the pins to align with package pads on the top side and test board pads on the bottom side. Precise alignment of signal pins within the cavity ensures that the probes maintain reliable contact through thousands of cycles in high-volume device testing environments, especially at high- and low-temperature testing. A plastic composite material with a low dielectric constant is used for the retention rings to minimize

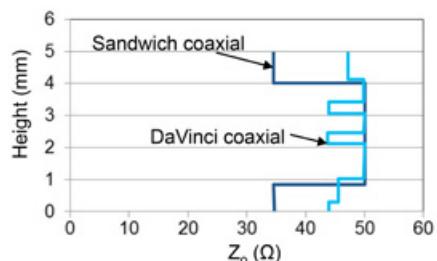


Figure 7: Impedance distribution comparison (reference only, varies with actual dimensions).

impedance differences between the ring and air gap sections.

Performance comparison of coaxial sockets

A coaxial structure is typically incorporated in the design of an IC device test socket to optimize the signal integrity performance at high frequency through controlled impedance matching of the IC chip and test board. Generally, the

impedance of an IC chip is 50Ω for single-ended and 100Ω for a differential pair of pads. The impedance distributions along the signal pin transmission sections is one indicator of coaxial structure SI performance. Consistent impedance around the required specification, such as 50Ω , is vital. [Figure 7](#) compares DaVinci socket impedance distribution with that of a sandwich coaxial socket. The sandwich socket has low impedances in nearly half of the signal



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transmission path. The DaVinci socket has more consistent impedance distribution with only two points demonstrating slight impedance changes. These impedance variations in DaVinci can affect SI, but are controlled in the acceptable range of socket SI performance in IC testing. Performing this impedance distribution calculation ensures optimization of the coaxial structure. As mentioned above, selection of dielectric materials, probe dimensions and structure of probe retention features were optimized in the design stage, resulting in a more uniform impedance distribution while avoiding dramatic impedance fluctuations along the signal transmission path.

To verify SI performance of coaxial test sockets, extensive studies, including SI simulation and measurements, have been performed. One measurement uses a typical signal and ground pin pattern, shown in **Figure 8**, and an Agilent E8363B network analyzer with a 40GHz measurement range. It is well known that one approach for better test socket SI performance is to use short

contactors or spring probes. To identify the SI performance improvement of a coaxial structure socket, a short probe with an electric transmission length of 2.8mm is selected as a comparison. The insertion loss (IL) and return loss (RL), as major SI performance parameters, are presented in **Figure 9**, identifying short probe, sandwich coaxial socket, and DaVinci coaxial structures. The SI performance summary of these curves is listed in **Table 1**. As shown

	IL, -1.0dB	RL, -10dB
DaVinci	>40GHz	>40GHz
2.15mm length pin	27GHz	27GHz
Conventional coaxial	19GHz	18GHz

Table 1: SI performance comparison.

in these curves, the DaVinci socket has the best SI performance among the three tested sockets with bandwidths of >40GHz at -1dB in IL and -10dB in RL. The short pin has better SI performance than the sandwich coaxial socket. However, the short pin socket SI performance is largely affected by socket material, pin maps, and pin structures, which cause many variations. One major limitation of the short pin is its low compliance, as minimal as 0.3mm, which may not be enough to cover total tolerances in package thickness and flatness in large packages.

Because of the limitations of coaxial structures, small diameter signal pins must

Summary

For many years, developing optimal coaxial structures applied in IC package testing has been a major focus for many engineers working in this industry. Because of mechanical limitations and challenges, only sandwich coaxial sockets have been widely applied in high-volume IC package testing environments. The DaVinci socket utilizing IM material and a proprietary pin holding structure has several advantages:

1. Excellent signal integrity with over 40GHz bandwidth at -1dB (IL) and -10dB (RL).
2. Very rigid and high-strength metal material that minimizes deflection from preload, especially in high pin count packages (>2000 pins).
3. Reliable and stable signal pin performance over 500K compressive cycles on account of the solid dielectric pin holding feature inside the signal pin cavity.
4. A reliable insulated surface layer on the socket body and cavity holes that eliminates any electric shorting in applications.
5. Stable socket dimensions that remove concern about shrinking or expansion with humidity variations.

Extensive research has been performed to optimize coaxial socket structure with these patented technologies. Products incorporating the solutions presented in this paper have been extensively used in IC package test houses and have shown significant advantages to users.

Biography

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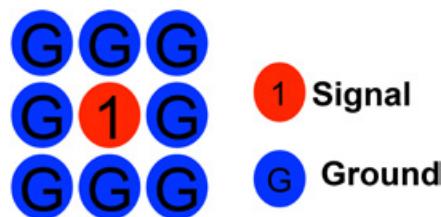


Figure 8: Pattern of SI measurement.

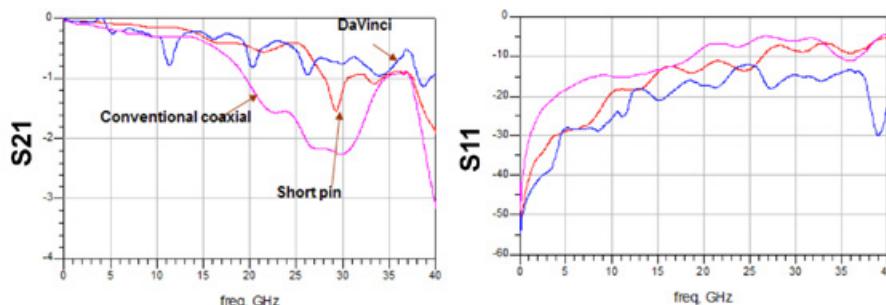


Figure 9: SI performance comparison: short pin and coaxial socket structures.

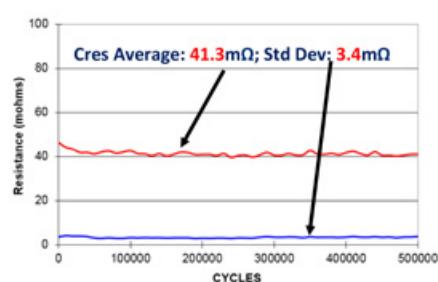


Figure 10: Signal pin 500K cycling test results.

be used in the test socket. There can be concern in using a small signal pin relative to its contact reliability over thousands of compressive cycles. **Figure 10** illustrates the performance of a signal pin with diameter of ~0.25mm tested over 500K cycles. The average contact resistance over 500K cycles is <60mohm with standard deviation of <16mohm. This is within the performance specification for signal pin performance in an IC package testing environment.

Advances and applications of gold electroplating for wafer-level packaging

By Therese Souza, Lynne Michaelson [Technic Inc.]

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Over the years, thick gold films have been applied to wafers to utilize gold's unique electrical and mechanical properties. This paper will review the current state-of-the-art application of gold plating onto wafers, substrates, and wafer-level packages by electroplating. We will also examine new developments in formulations of cyanide (CN) free chemistries that offer improved ease of use, neutral pH, higher stability, and are free of heavy metal additives.

Gold plating applications

Gold plating is used in many industries to take advantage of gold's electrical, thermal, and mechanical properties. For example, in the semiconductor industry, gold plating is used for a variety of bonding applications due to gold's corrosion resistance and mechanical properties. In the microelectromechanical sensor (MEMS) industry, gold compression bonding is used where low temperatures ($<200^{\circ}\text{C}$) are required. Tall gold pillars are plated on liquid crystal display (LCD) drivers and bonded to printed wiring boards (PWBs) using thermal compression bonding. In flip-chip and chip-scale packaging applications, the under bump metal (UBM) stack has gold as a final surface finish. In addition to bonding applications, the electrical and thermal properties of gold make it useful for backside and via plating on power amplifiers that are used in cell phone applications. The majority of these semiconductor applications require soft, pure gold. This paper will discuss the development of a cyanide-free, acidic gold plating bath that is compatible with photoresist and is more stable than the existing commercially available alkaline cyanide-free plating baths.

Electroplating bath compatibility

Compatibility of photoresist with the gold electroplating bath is one of the most important issues when discussing gold electroplating in the semiconductor industry.

The cyanide-based baths can be formulated to be alkaline ($\text{pH}>8.5$), acidic buffered baths (pH between 1.8–6), and neutral, buffered baths (pH between 6 and 8.5) [1]. Even over a wide pH range, these baths attack photoresist because free cyanide is produced [1]. Non-cyanide plating baths can be formulated to be compatible with photoresists they are not, however, as stable as the cyanide-based plating baths. **Table 1** compares the stability constant of the gold cyanide complex to the most commonly used non-cyanide gold complex: gold sulfite. The gold sulfite complex is much less stable than the cyanide complex when comparing their stability constants, gold sulfite ($K=10^{10}$) vs. gold cyanide ($K=10^{39}$) [1]. In addition, the gold sulfite complex is most stable at an alkaline pH . Because most photoresists tend to be soluble in alkaline solutions, sulfite gold plating baths are generally formulated to have a pH between 8 and 10 in order to minimize the dissolution of the photoresist. A neutral to acidic pH is most desirable for resist compatibility; this condition, however, is not as stable for the gold sulfite complex.

A combination of proprietary stabilizers and heavy metal additives have been used to formulate sulfite gold plating baths that have decent stability while being compatible with resists [2]. However, most of these plating baths are still alkaline (pH of 8–10) and contain hazardous heavy metal additives that start to negate the health and safety benefits of the sulfite gold plating bath versus the cyanide gold plating bath.

In addition to better resist compatibility and less health and safety issues, the sulfite gold plating bath has a few other advantages over the cyanide-based baths. Sulfite gold plating baths are known to have better throwing power than cyanide-based baths [3]. This benefit enables good step coverage and uniform plating for semiconductor applications

requiring via and backside plating. In addition, low stress, specifically compressive stress, is required for many gold plating applications in the semiconductor industry. The sulfite gold bath can be formulated to have low stress [1]. Finally, pure gold deposits with lower surface roughness and high electrical conductivity are often required [2]. A properly formulated sulfite gold plating bath can produce a gold deposit that meets the above requirements [2].

Morrisey [4] developed a sulfite gold bath stable to a pH of 4.5 using polyamines and aromatic nitro compounds as additives. Although this plating bath worked well in small installations, there were some consistency issues that prevented this bath from

Gold Complex	Equation	Stability Constant
Cyanide	$\text{Au}^+ + 2\text{CN}^- \rightarrow [\text{Au}(\text{CN})_2]^-$	$K = 10^{39}$
Sulfite	$\text{Au}^+ + 2\text{SO}_3^{2-} \rightarrow [\text{Au}(\text{SO}_3)_2]^{3-}$	$K = 10^{10}$

Table 1: Stability constants for selected gold complexes [1].

being used in high-volume manufacturing. Further study of Morrisey's bath resulted in a reformulation of this sulfite gold plating bath. A proprietary stabilizer was discovered that enables the bath to have excellent stability and to be operated at an acidic pH . Successful operation of this acid sulfite gold plating bath across four different manufacturing toolsets, as well as numerous wet benches and research plating tools, demonstrates the versatility of this chemistry. The following paper will discuss the operation and performance of this acid sulfite gold plating bath.

Electrolyte operation

In the semiconductor industry, it is critical that the gold plating bath is compatible with photoresist because many of the parts are plated through a mask. As shown in **Figure 1**, resist dissolution typically occurs at an alkaline pH of 10 or higher. In addition, cyanide-based gold plating baths are not

compatible with resist. Therefore, a non-cyanide gold plating bath with near neutral to an acidic pH is desired for plating on parts with photoresist. To the best of our knowledge, all of the commercially available sulfite gold baths have either an alkaline pH or utilize heavy metal additives such as thallium and arsenic. Although sulfite gold baths with a pH ~8 appear to be compatible with resist, there is still some resist degradation on account of localized areas that may have a pH higher than 8. This resist degradation may not be severe enough to affect the feature shape, but it will contaminate the plating bath and reduce the overall lifetime of the bath [3].

In order to increase the compatibility of the gold plating bath with photoresist, an acidic sulfite gold bath has been formulated with a proprietary stabilizer that improves the stability and performance of the bath. The operating parameters for this acid sulfite gold bath are shown in **Table 2**. This bath can be operated from pH 6.3-6.9 with an optimum of 6.6. As shown in **Figure 1**, this pH range is lower than other commercially available sulfite gold baths. In addition, this bath does not require any heavy metal additives for grain refining. Although sulfite gold plating baths

are less toxic than cyanide based gold baths, the addition of these heavy metal stabilizers introduces health and safety concerns as well as waste disposal issues. This acid sulfite gold bath does not have heavy metal additives so the bath is less toxic.

The proprietary stabilizer used in the formulation described in **Table 2** not only enables operation of the plating bath at an acidic pH, but also ensures that the bath has a longer lifetime than other commercially available sulfite gold baths. This acid sulfite gold bath was installed at a customer site and run for 1.5 times longer than the competitor's bath, which is typically run in production. At the time that the acid sulfite gold bath was dumped, it was still fully operational based on the step coverage analysis of the gold plated within the vias. Typical alkaline sulfite gold baths degrade with operation and the step coverage of gold plating inside the

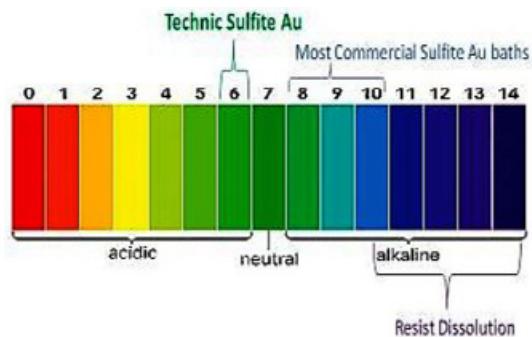


Figure 1: Comparison of pH range for sulfite gold plating baths. The new acid sulfite gold bath operates at a pH range of 6.3-6.9.

Parameter	Range	Optimum
Gold Metal	7.6 – 12.3 g/l	8.2 g/l
Buffer	400-520 ml/l	460 ml/l
Sol'n Conductivity	150-300 ml/l	225 ml/l
Stabilizer	25-40 ml/l	30 ml/l
pH	6.3-6.9	6.6
Specific Gravity	>10° Be	>10° Be
Temperature	45-65 °C	50-60 °C
Current Density	0.1 – 0.8 ASD	User selects
Deposition Rate	12 µm / hour @ 0.3 ASD	

Table 2: Operating parameters for acid sulfite gold bath.

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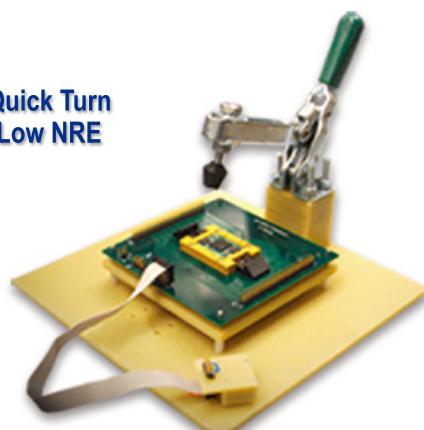
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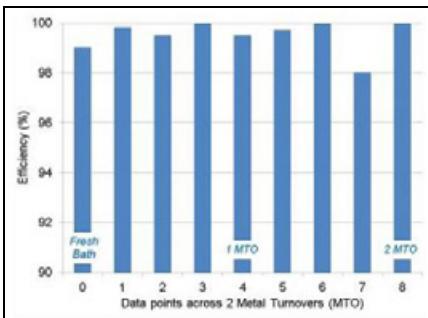


Figure 2: Efficiency of the acid sulfite gold plating bath over the duration of two metal turnovers.

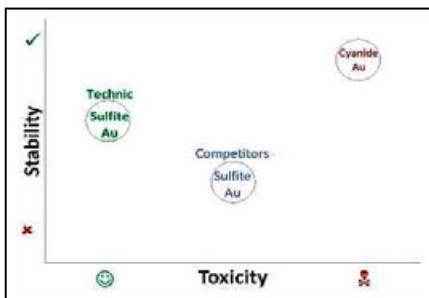


Figure 3: Schematic illustrating the stability and toxicity for various gold plating bath formulations. The acid sulfite gold bath has good stability and is less toxic than the other plating baths.

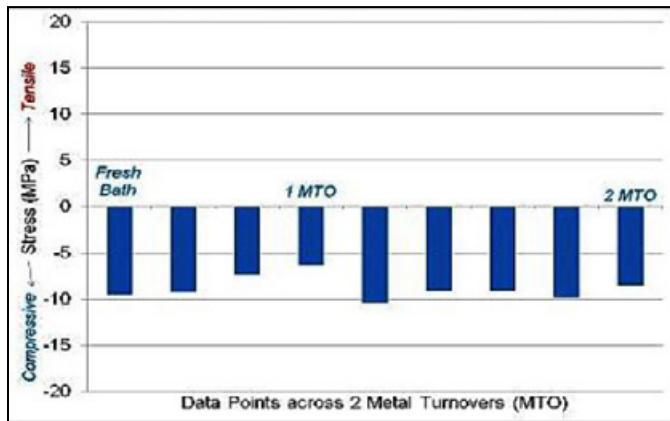


Figure 4: Low compressive stress observed for the acid sulfite gold bath over 2 MTOs.

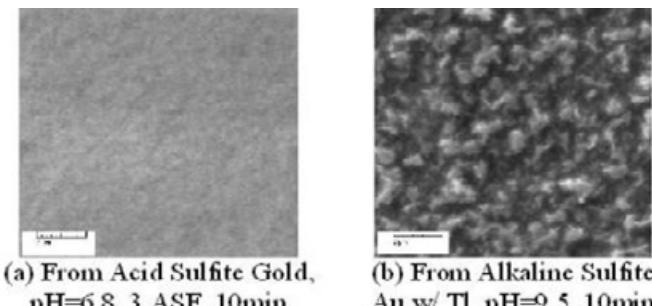


Figure 5: Top down SEM images comparing gold film plated from a) acid sulfite gold vs. b) alkaline sulfite gold bath w/thallium (Tl).

via declines. A standard alkaline gold bath is dumped after 2-3 metal turnovers (MTO). **Figure 2** shows that the efficiency of the acid sulfite gold plating bath is maintained between 98-100% over 2 MTOs. Internal studies indicate that the bath can operate normally over 5 MTOs. Further studies are required to determine how long this bath can be used in production.

Although sulfite gold baths are not as stable as cyanide-based gold baths, this acid sulfite gold bath appears to be more stable than other commercially available non-cyanide gold baths. In addition, because this bath does not use any heavy metal additives, it is considered less toxic than both the cyanide-based baths and the sulfite gold baths with thallium and/or arsenic. This comparison is shown schematically in **Figure 3**.

Deposit properties

Gold deposits produced from this acid sulfite gold bath meet the desired properties for the semiconductor industry and are shown in **Table 3**. Many sulfite gold users desire a low compressive stress for the as-plated gold deposit. Stress measurements can vary depending on the technique that is used to measure the stress. Two different techniques have been used to evaluate the stress of the gold deposits from the acid sulfite gold chemistry.

The stress results shown in **Table 3** come from customer evaluations of the deposit stress on polished wafers. These measurements are from tools utilizing wafer curvature to measure the stress of the deposit. **Figure 4** summarizes the results of a stress study performed

using stress tabs from the Deposit Stress Analyzer System from Specialty Testing & Development Co. The stress of the gold deposit was measured over two metal turnovers. As can be seen in **Figure 4**, the stress is uniform over the duration of this study measuring between 5-10MPa compressive. Again, this demonstrates the stability of the acid sulfite gold plating bath.

Roughness is another important property for the gold deposit. Typically, heavy metal additives such as arsenic and thallium are used in commercially available sulfite gold baths in order to produce the desired fine grain deposit [1,2]. As discussed previously, these additives increase the toxicity of the plating bath. The newly formulated acid sulfite gold chemistry does not contain these heavy metal additives. This bath still produces a smooth, fine-grained deposit even without these additives as shown in the top down scanning electron microscope (SEM) images in **Figure 5**. The image in **Figure 5b** is from a commercially available alkaline gold bath with thallium as a grain refiner. It is apparent that the gold deposit from the acid bath in **Figure 5a** is smoother than that from the alkaline gold bath (**Figure 5b**). Therefore, the acid sulfite gold bath is more stable and less toxic than the competitor's sulfite gold bath while providing a deposit with a smoother morphology and lower roughness.

Plating applications

Different plating applications are discussed below.

Pattern plating: thick gold (5-10 microns). As shown in **Table 3**, excellent within-wafer uniformity is achieved for thin plated gold that is approximately 1 micron thick. However, many applications require thicker gold plating of 5 to 10 microns. These applications frequently require that the gold be plated through a mask. An example of through-mask plating can be seen in **Figure 6**. In this application, a photoresist was deposited over a sputtered gold seed layer. The wafer with the photoresist is then immersed in the acid sulfite gold plating bath. The gold is plated to

PARAMETER	ACHIEVED
Stress	0 +/- 30 MPa
Hardness	70 – 80 Knoop
WIW	2.4% 1-sigma 49pt Contour (~1 µm thk) 2.0% 81 pt Diameter (~1 µm thk)
Ra	7.5 nm avg
Purity	99.99%

Table 3: Gold deposit properties from acid sulfite gold.

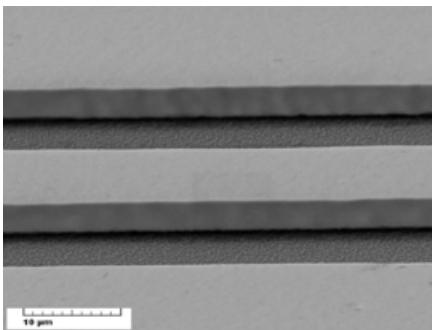


Figure 6: Tilt (60°) SEM image showing gold lines plated through resist using the acid sulfite gold bath.

a thickness of approximately 7 microns. After plating, the resist is removed from the wafer. The gold-plated pattern is shown in **Figure 6**. The edges of the gold-plated pattern are sharp and the morphology of the plated gold is smooth. There is no observation of under-plating and the feature shape looks good—demonstrating excellent compatibility of this plating bath with photoresist.

In another pattern plating application – square and rectangular isolated features of various sizes – are plated as shown in **Figure 7**. Initial plating of these features resulted in poor within- feature uniformity. **Figure 8** shows the contact profilometer scan that was taken across the width of the rectangular feature. This rectangular feature has high points at the edges of the feature, which have been termed “bat ears.”

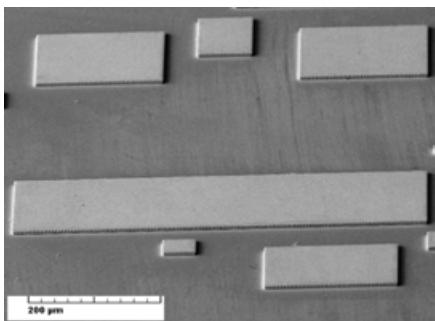


Figure 7: Tilt (65°) SEM image of various features plated using acid sulfite gold. Average gold thickness across all features is $9.18 \pm 0.14\mu\text{m}$.

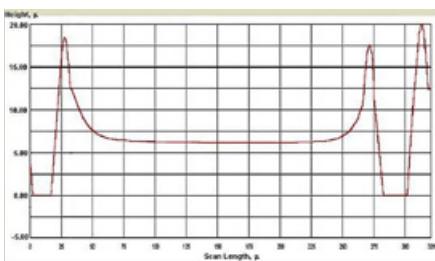


Figure 8: Contact profilometer scan of a rectangular feature showing “bat ears,” i.e., poor within-feature uniformity.

After further optimization of the plating bath, the “bat ears” were eliminated and the within-feature uniformity improved. **Figure 9** is a contact profilometer scan across the rectangular shape showing square corners and no “bat ears.” **Figure 10** is a higher magnification SEM image showing this rectangular feature with very square corners.

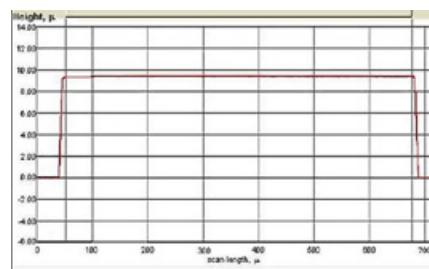


Figure 9: Contact profilometer scan of a rectangular feature in **Figure 10**. Improved square corners: no “bat ears!”

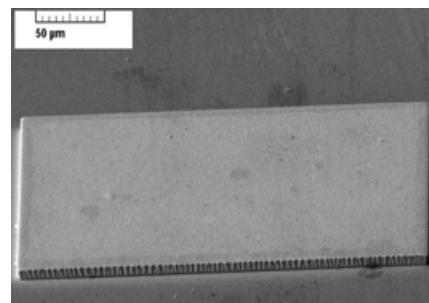


Figure 10: Tilt (65°) SEM image of a feature plated with the improved acid sulfite gold plating bath.

In order to look at the co-planarity of these various features across the wafer, the step height of the small and large rectangular shapes shown in **Figure 7** were measured at five locations across the diameter of the wafer using the contact profilometer. The target thickness for this application is 9 microns. The results are shown in **Table 4**. There is no statistical difference in thickness between the large and small features. In addition, the range of all these measurements is $0.44\mu\text{m}$ demonstrating excellent within-wafer uniformity even over various size features.

Feature	Au Thickness (5 sites across wafer)
Small	9.12 ± 0.14
Large	9.23 ± 0.13

Table 4: Summary of gold thickness measurements across both the small and large rectangular features shown in **Figure 7**.

Pattern plating: very thick gold (30+ microns). Typically, cyanide-based gold plating baths are used when thick gold

plating of 30+ microns is required because cyanide-based baths have a faster plating rate than sulfite-based bath. However, in certain applications with strict health and safety requirements, cyanide-based plating solutions cannot be used. Therefore, the newly developed acid sulfite gold plating bath was tested on wafers requiring 30+ microns of plated gold. The plating rate was about 12 microns/hour. The initial test showed very poor uniformity across the plated feature as shown in **Figure 11a**. The edges of the patterned feature are plated higher than the center. **Figure 11b** shows the contact profilometer scan across this feature demonstrating the “bat ears” previously discussed. Although this poor within-feature uniformity is unacceptable, there is no evidence of under-plating indicating excellent resist compatibility even after 2+ hours in the plating solution.

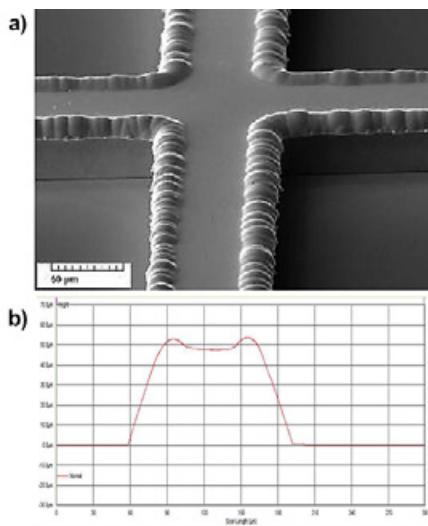


Figure 11: a) Tilt (65°) SEM image showing the initial attempt at pattern plating a 30+ micron thick gold deposit; b) Contact profilometer scan across the feature in a).

In order to improve the poor feature uniformity shown in **Figure 11a**, the acid sulfite gold plating bath was studied to determine which bath components were impacting the within-feature uniformity. After some modification of the bath chemistry, a 30+ micron gold deposit was achieved with sharp corners and excellent within-feature uniformity as can be seen in **Figure 12a**. The contact profilometer scan in **Figure 12b** shows the corners of the feature are square and the “bat ears” are gone. These results open up a new application space for gold sulfite plating baths.

Via plating. Sulfite gold plating baths are known to have better throwing power than cyanide gold baths [3]. This property, along with good resist compatibility, makes this type of bath ideal for backside and via plating of power amplifiers for GaAs devices. This

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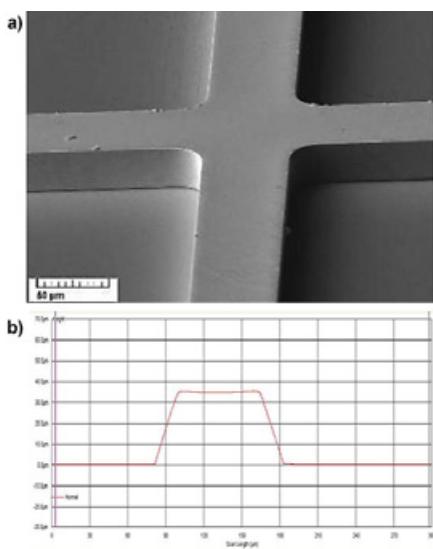


Figure 12: Excellent feature shape with the optimized acid sulfite gold bath: gold thickness is 30+ microns. a) Tilt (65°) SEM Image; b) Contact profilometer scan.

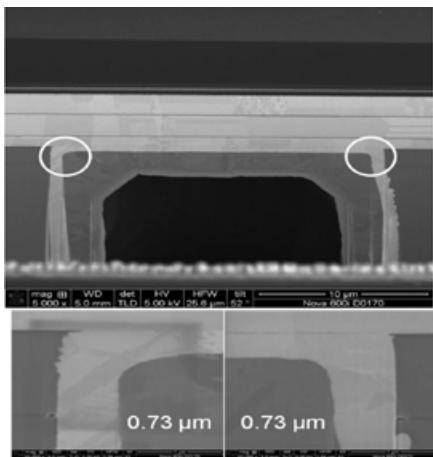


Figure 13: Excellent step coverage of gold in vias plated with the newly formulated acid sulfite gold bath.

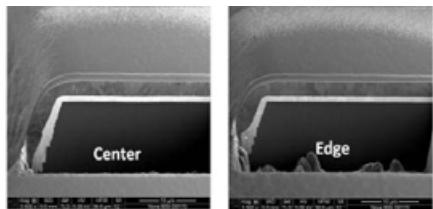


Figure 14: Cross section SEM image illustrating uniform plating across the wafer, center and edge.

	Alkaline pH Bath	Acidic pH Bath
Front	15.9 μm	11.8 μm
Back	5.3 μm	11.3 μm
Total	21.2 μm	23.1 μm

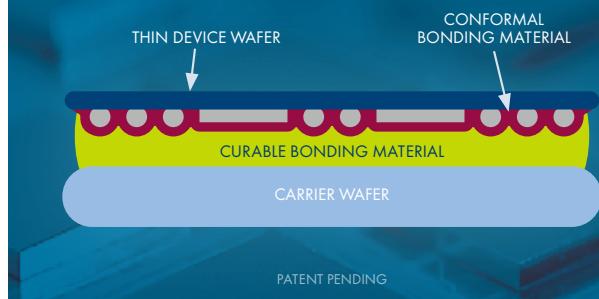
Table 5: Comparison of throwing power for the alkaline bath vs. the acidic bath. The acidic bath plates the same thickness on front and back. **Table 5** lists

newly formulated acid sulfite gold plating bath has demonstrated excellent step coverage for via plating as shown in **Figure 13**. The circled corner areas in the top picture in **Figure 13** are enlarged in the lower images to show the uniform gold plated layer in the corners of the vias. The amount of gold plated in the vias far exceeds the customer's minimum requirement.

In addition to uniform plating within the via, it is also critical for the plating to be uniform across the wafer. **Figure 14** compares plating at the center and the edge of the wafer. The backside gold plating is uniform across the wafer and achieves the target thickness of 1 micron.

Throwing power for uniform plating. The newly formulated acid sulfite gold plating bath has also demonstrated better throwing power than the commercially available alkaline sulfite gold bath. An experiment was conducted in which two beakers were set side by side, one beaker was filled with the acid sulfite gold bath and the other beaker with an alkaline sulfite gold bath. The part to be plated was double-sided but only the front side of the part faced an anode—the backside was not facing an anode. Plating was performed in each beaker at the same time and the result was filmed. The acid sulfite gold beaker showed that the backside of the part started to plate immediately on account of the high throw of this bath. The alkaline gold bath took much longer before gold plating started on the backside of this part. **Table 5** lists

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the resulting gold thickness on the front and backside of the part from each plating bath. The alkaline pH bath has a large discrepancy between the gold thickness on the front versus the backside of the parts. The frontside is three times thicker than the backside. Whereas, the part plated with the acid sulfite gold chemistry has the same thickness on the front and back of the part even though the backside was not facing an anode or controlled by a separate power supply.

Summary

The versatility and unique features of a newly formulated acid sulfite gold plating bath have been discussed. A proprietary stabilizer enables this bath to operate at an acidic pH, whereas, the competitive sulfite gold baths operate at an alkaline pH. The acidic pH plating bath is more compatible with photoresist than the alkaline pH baths. Gold deposited from this plating bath is smooth with low roughness even though the bath does not contain any heavy metal grain refiners. This bath is non-toxic and does not require any complicated waste treatment because the bath is free of harmful components such as cyanide, thallium, and arsenic. The unique chemistry of this bath enables excellent step coverage and

bath efficiency over two metal turnovers. In addition, the stress of the gold deposit is very low at 5-10MPa compressive. This acid sulfite gold plating bath can be used for a wide range of applications.

As discussed, pattern plating ranging from 5 to 30+ microns of gold has been demonstrated. In addition, the excellent throwing power of this bath has been demonstrated by uniform gold plating across the backside and in vias. Also, this bath has been successfully operated on four production plating tools, numerous research tools, and various wet benches demonstrating the versatility of this chemistry. This plating bath is commercially available as Elevate® Gold 7990. Future research on this plating bath will include additional studies to understand the performance of this chemistry over 5 MTOs.

Acknowledgements

The authors wish to thank the research team at Technic including Scott Bateson and Tom Tyson for their work on this project and Bob Foreman, General Manager, 1 Zone, LLC, for his valuable contributions to this paper.

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Biographies

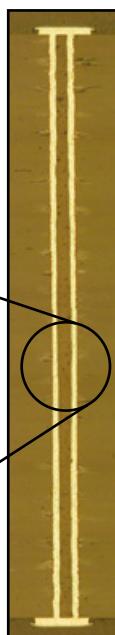
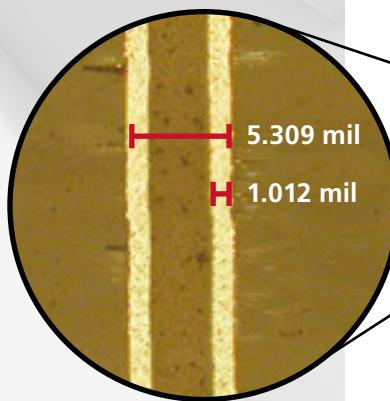
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FOWLP: comparison and highlights of the latest technology trends

By Romain Fraux *[System Plus Consulting]*

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To highlight the last implementations of fan-out wafer-level packaging (FOWLP), this work will address technological and cost reviews with comparison of several actual FOWLPs. With photos taken from physical analyses, we will describe and compare the design and manufacturing construction of FOWLP integrated in recent automotive radar applications from Bosch (Infineon radar chips with embedded wafer-level BGA [eWLB] technology) and Continental (NXP radar chips with redistributed chip packaging [RCP] technology). We will also discuss the latest introduction of Qualcomm FOWLP into smartphones and will show why that company is going to provide more products with fan-out packages by comparing the cost structure with fan-in WLP. Finally, the latest evolutions of package-on-package (PoP) for application processor and memory are highlighted based on teardown analyses of the flagship smartphones. Pictures of packages cross sections from Samsung, Qualcomm and Apple will be presented, and we will describe and compare their choices in terms of supply chain and technologies.

Introduction

FOWLP is currently the fastest-growing advanced packaging technology, and it will continue growing towards a \$2.4B market by 2020 [1]. Fan-out is gaining in popularity, and many applications (e.g., telecom, automotive, and medical) are starting to implement it. As shown in **Figure 1**, 2016 is a turning point for the FOWLP market since Apple and TSMC changed the game and may create a trend of acceptance of fan-out packages. The market will actually be split into two types: 1) The “core” market of fan-out, including single-die applications such as baseband, power management, RF transceivers, etc. This is the main pool for FOWLP solutions and will keep growing; 2) The “high-density” market of fan-out, started by Apple APE, that will include larger I/O count applications such as processors, memories, etc. This market is more uncertain and will require new integration solutions and high-performing fan-out packages, but has a very high potential.

Mobile customers have high expectations of miniaturization and higher integration while keeping costs low. FOWLP has proven its ability to reach these targets. Its small form factor and low-cost capabilities shown in the first wave of acceptance, referred to as the “core” market, are now enhanced with high-integration ability of the new fan-out architectures shown in **Figure 2**. These architectures are expected to spread driven by the “high-density” fan-out market. The main example of wider integration that is available is that of TSMC’s fan-out package-on-package (PoP) for Apple.

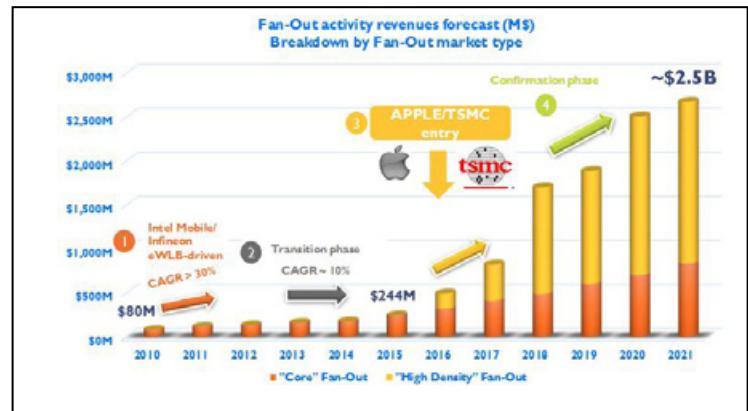


Figure 1: FOWLP activity market forecast [1].

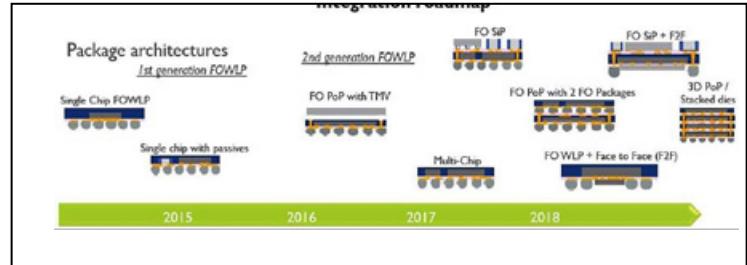


Figure 2: Volume production roadmap for FOWLP [1].

FOWLP for radar applications

A key market for FOWLPs is automotive applications—and it is now widespread. In June 2016, Infineon announced that it had shipped a total of 20 million radar chips [2]. They were the first to introduce FOWLP in 2012 for the packaging of radar chips, which enabled radar systems to become more affordable. Indeed, traditional radar systems are mounted in chip-on-board (COB) using wire bonding to connect the chip with the substrate, which is not standard for a surface mount technology (SMT) assembly line. FOWLP offers the possibility of using a standard solder reflow assembly and also features low transmission losses from chip-to-package and board [3].

Key players for FOWLP in automotive radar applications are Infineon with eWLB package and NXP with its RCP. Both are integrated in automotive 77GHz radar for advanced driver assistance systems (ADAS). Infineon, through the eWLB platform, has been largely adopted by Bosch in long-range radars (LLR) and mid-range radars (MMR), and NXP is mainly integrated in the Continental Industrial Sensors' long-range advanced radar sensor (ARS).

The NXP chipset in Continental radar consists of three components, each packaged with FOWLP: a 3-channel receiver (77GHz), a 2-channel transmitter (77GHz) and a 4-channel voltage control oscillator (VCO) (38.5GHz). On the other hand, Infineon's chipset solution only uses two components: the 38GHz VCO being integrated with the transmitter die. As shown in [Figure 3](#), the Infineon and NXP components share the same 6mm x 6mm package footprint; and die areas for both solutions represent only 25% of the packages' area.

[Figure 4](#) highlights the package structure with SEM pictures of cross sections. Infineon and NXP dies have almost the same thickness, but the molding is not subjected to the grinding process for the RCP package. Infineon uses an extra step to thin the epoxy until the silicon die and adds a protective layer on the package. For the RCP

package, a ground plane corresponding to an additional copper structure helps to limit the die shift and provides electromagnetic (EM) shielding as well as more rigidity to the package.

The supply chain used by Infineon and NXP for FOWLP is different. Both players have internally developed their packaging platform – the eWLB for Infineon and the RCP for NXP – but only Infineon choose to keep the manufacturing internally. Although the eWLB process has been licensed to other outsourced semiconductor assembly and test (OSAT) players, the packaging of radar chips is still made by Infineon in Germany on 200mm (8-inch) wafers. On the other hand, NXP prefers to rely on NEPES, a South Korean OSAT specialized in wafer-level packaging and using 300mm (12-inch) production lines. We calculated that this choice to subcontract to a 300mm producer relies on a 20% lower packaging cost.

FOWLP for consumer applications

FOWLP could find many potential applications in mobile phones. Applications such as baseband, power management, RF transceivers, and audio codec are all looking to this platform for potential performances and cost saving reasons.

The first FOWLP component we observed in 2009 was an Infineon baseband chip found in a LG feature phone. Since that time, we found other components using this technology. The Samsung Galaxy S7, which was released in March 2016, contains an audio codec chip using a FOWLP. This audio codec is particularly interesting because it is present only in versions of the Samsung Galaxy S7 and S7 Edge featuring the Qualcomm Snapdragon 820 processor,

which has been mostly observed in the U.S. Therefore, as shown in [Figure 5](#), two players supply Samsung for the audio codec in the Galaxy S7 and S7 Edge: Qualcomm with the WCD9335 in versions featuring the Qualcomm Snapdragon 820, and Cirrus Logic with the CS47L91 in versions using the Samsung Exynos 8890 processor.

The audio codec supplied by Cirrus is packaged with a traditional fan-in WLP (FIWLP) compared to a FOWLP for Qualcomm. In term of silicon usage, the Qualcomm solution, which also uses an additional A/V processor from DSP Group, consumes 40% less silicon area compared to the Cirrus solution.

The FOWLP technology used for the Qualcomm audio codec is the eWLB, licensed by Intel/Infineon to several outsourced semiconductor assembly and test suppliers (OSATS) including ASE, NANUM S.A., and STATS ChipPAC. To show the real interest in going from a FIWLP to a FOWLP, we calculated the cost to produce the Qualcomm actual chip and compared it to the cost it could have been if it had been packaged with a FIWLP. The fan-out area of the Qualcomm chip is very low compared to radar chips because the die represents 80% of the package area. The molding area all around the die is then very limited as shown in [Figure 6](#).

In the case of a FIWLP, the die size is then 100% of the package area. By using the same wafer front-end process (CMOS 40nm), we calculated that an increase of 25% (from 80% to 100%) of the die size drive to a die cost increase of 20%. On the other hand, the cost of the packaging is lower for FIWLP. We calculated that FOWLP steps are close to 50% more expensive compared to FIWLP. But packaging cost is much less expensive compared to CMOS front-end cost. For our component manufactured with a CMOS 40nm process, the packaging cost represents less than 15% of the total cost. So at the end, the FOWLP solution with a 50% cost increase for the packaging and a 20% cost decrease for the front-end is 10% less expensive compared to the FIWLP solution. Of course the results would have been very different if the technology node used for the CMOS was larger and therefore less expensive. In this case, the cost increase of the FOWLP steps would have driven a higher component cost.

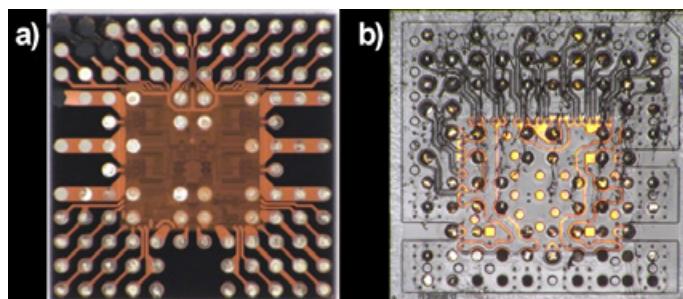


Figure 3: a) (left) Infineon RRN7745P; b) (right) NXP MR2001RVK.

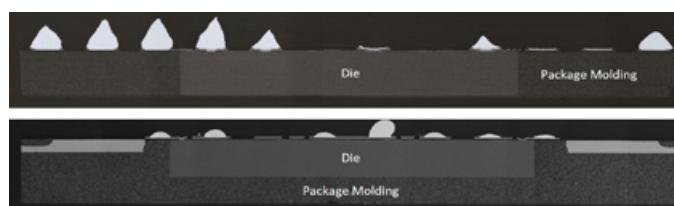


Figure 4: a) (top) Infineon eWLB cross section; b) (bottom) NXP RCP cross section.

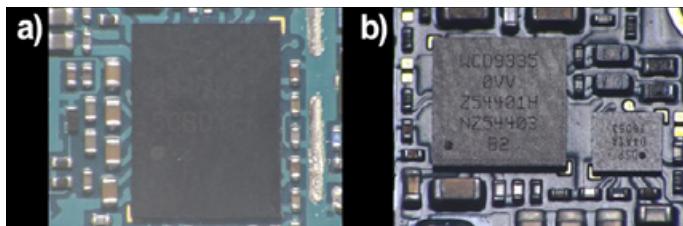


Figure 5: a) (left) Cirrus CS47L91; b) (right) Qualcomm WCD9335 and DSP Group D4A1A.

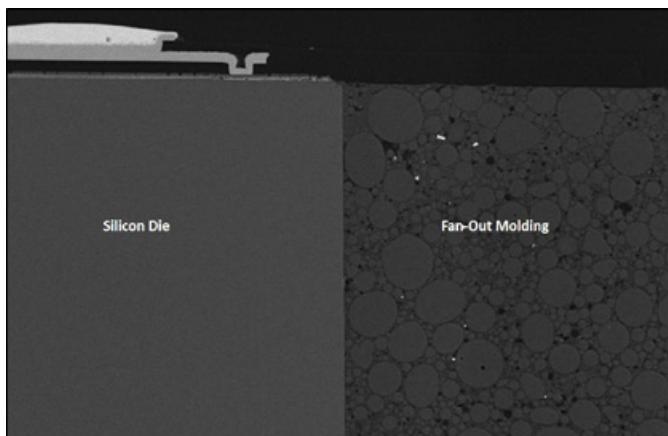


Figure 6: Qualcomm WCD9335 cross section.

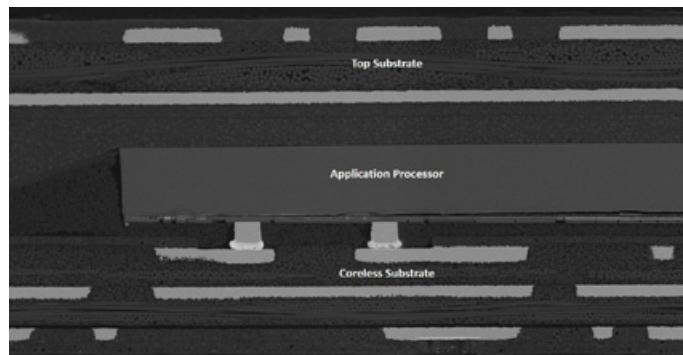
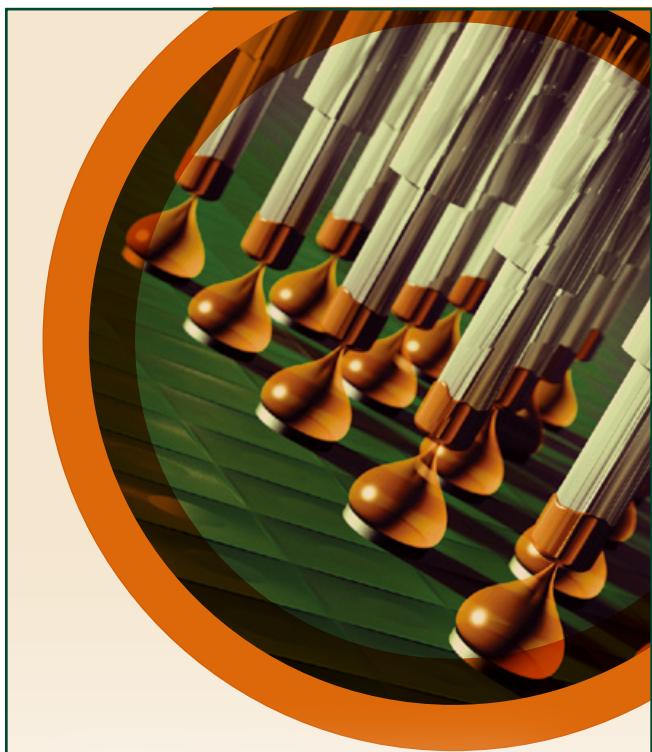


Figure 7: Qualcomm Snapdragon 820 cross section.

Package-on-package for application processors

Package-on-package (PoP) is used massively in smartphones and tablets to stack the application processor (AP) with the dynamic random access memory (DRAM). Among the years, the main challenges have been to reduce the package thickness and to offer higher levels of integration. The through-molded via (TMV) technology developed by Amkor Technology has become the most predominant solution offering the best compromise [4]. But new PoP technologies have entered the market in order to provide a better level of integration and a lower package thickness. An example is the technology used by Qualcomm to package its latest high-end Snapdragon processors as shown in **Figure 7**. The Qualcomm Snapdragon 820 uses an embedded die packaging approach with Shinko's technology, using copper core solder balls to replace the TMV technology. This platform is called molded core embedded package (MCEP) and includes copper pillar flip-chip of the processor to a core-less substrate with embedded trace



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substrate technology. Thanks to this MCeP process, Qualcomm is able to offer a very thin packaging of the application processor (less than 0.5mm) and a better integration of the top memory package.

More recently, a breakthrough has been made by Apple for the A10 processor in the iPhone 7 by introducing the first wafer-level package-on-package (WLPoP). The technology is TSMC's integrated fan-out PoP (inFO-PoP).

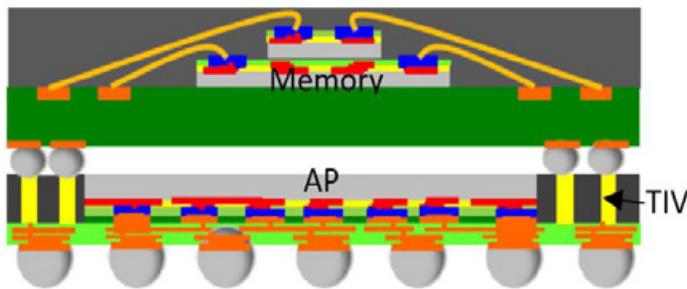


Figure 8: TSMC inFO-PoP structure [5].

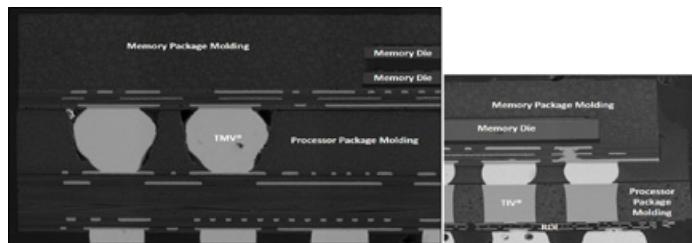


Figure 9: a) (left) Samsung Exynos 8 PoP cross section; b) (right) Apple A10 PoP cross section.

Apple and TSMC offers a considerable thickness reduction of 30% compared to traditional PoP with TMVs as shown in **Figure 9**. In addition to providing a lower thickness, another advantage of this technology is to be built at the wafer level and then to remove some expensive steps linked to the flip-chip process (flux cleaning, underfill) and to the use of a laminate substrate. When the process becomes completely mature, it will definitively lead to an important cost reduction.

Summary

Even though FOWLP has been in production for more than six years, the technology is just beginning to be implemented in high volume. The examples presented highlight the fact that FOWLP could lead to cost reductions under several conditions:

- As a replacement to chip-on-board integration for radar chipsets;
- In combination with advanced CMOS technology nodes for single-die consumer applications such as baseband, power management, RF transceivers, or audio codec; and
- In 3D-PoP configurations for the stacking at the wafer-level of the application processor with the memory.

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Biography

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Improving stepper throughput with feed-forward metrology of die placement error

By Tom Swarbrick, Keith Best / Rudolph Technologies, Inc.]

Fan-in wafer-level packages, such as flip chips, arrange I/O contacts over the surface of the die. The number of contacts is limited by the size of the die. Fan-out packaging processes allow chip manufacturers to increase the I/O count by artificially extending the die surface. In fan-out processes the die are embedded in an epoxy molding compound with more space between die than on the original wafer. The reconstituted substrate may mimic the shape of a wafer, allowing subsequent processing in equipment designed to handle wafers, or it may be a larger rectangular panel, conferring benefits from certain economies of scale in subsequent processing. After reconstituting the wafer/panel, the fan-out process uses thin film techniques to create redistribution layers that extend beyond the edges of the die and onto the adjacent molding compound. Finally, solder balls on contact pads atop the redistribution layer provide reliable connections to a mating printed circuit board. The additional spacing between die extends the surface area available for contacts and permits an arbitrarily large number of contacts per die.

A major challenge in fan-out processing lines is the inaccuracy of die placement on the reconstituted wafer/panel. Die placement error can occur in the initial placement and during the reconstitution process, and die can also shift in subsequent processing steps. Accurate information about the location of the die is required to ensure that the interconnects formed in the redistribution layer connect with the I/O contacts of the die. Manufacturers have addressed die placement error by using a photolithography system to measure the position of each die and realign each exposure, i.e., die-by-

die alignment. Although effective, the alignment process is time consuming and can amount to as much as two-thirds of the overall exposure cycle. Eliminating die-by-die alignment in the exposure tool can dramatically increase its throughput, with commensurate reductions in the cost-of-ownership of lithography systems.

Here we describe an experiment designed to demonstrate efficacy of feed-forward measurements in achieving accurate overlay in an advanced packaging lithography tool (JetStep® Series, Rudolph Technologies).

Measurement capability

Lithography processes generally require overlay accuracy of 25% of the feature size (critical dimension, CD). Redistribution layer (RDL) interconnect features are currently in the 5 to 15 micrometer range, although, they are expected to continue to shrink down to the 2 micrometer range in the foreseeable future. Inspection and metrology systems use optical imagery and image analysis

techniques to detect feature locations and measure distances between features (Figure 1). To establish the accuracy of this measurement tool we evaluated a test pattern on a stepper reticle generated by electron beam lithography – a technique capable of creating patterns with nanometer scale accuracy, well beyond the requirements of RDL overlay. The reticle comprised several arrays of

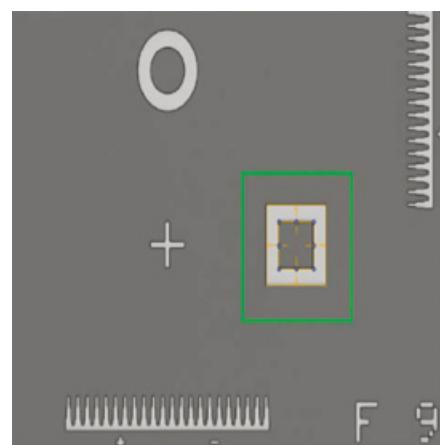


Figure 1: NSX® Series optical microscope image of one of the cells in the array in Figure 2.

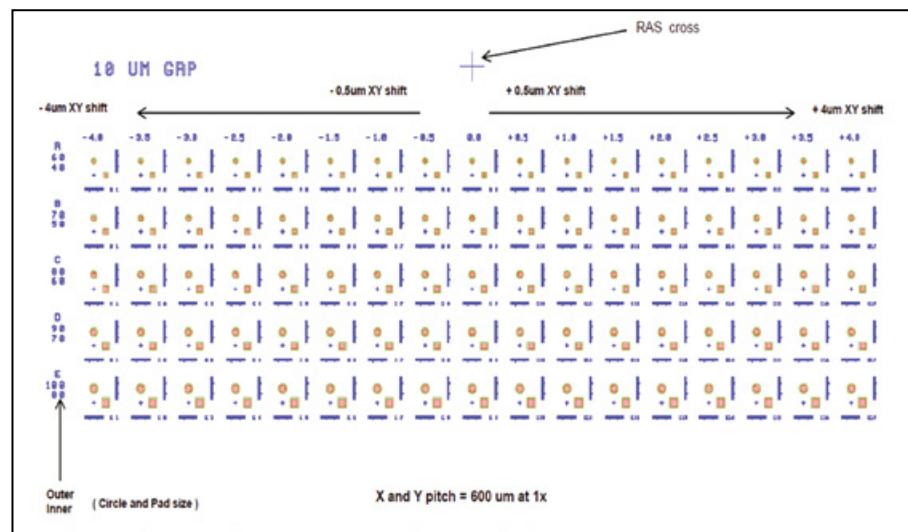


Figure 2: One of several box-in-box and circle-in-circle arrays from the test reticle.

specifically designed test features (box-in-box and circle-in-circle test patterns and alignment verniers) covering a range of sizes and offsets (**Figure 2**). The results demonstrated a measurement accuracy of better than $0.1\mu\text{m}$ (**Figure 3**).

Overlay accuracy

Testing overlay accuracy with feed-forward die placement error information proceeded in two phases. Phase one consists of three steps. In the first step we define layer one containing a set of alignment targets with and without various X/Y offsets on a 300mm silicon wafer (**Figure 4**). Six targets spaced widely across the wafer surface, serve to define the reference frame of the wafer. Nine pairs of targets, arranged in a 3×3 matrix, mimic embedded die with a range of placement errors. Each pair has a known X/Y offset and rotation (**Figure 4**).

In step two we measure the placement errors of the target pairs with reference to the six targets that define the global wafer position. These measured offsets are fed forward to the stepper and used in step two to compensate for placement errors defined by the layer one alignment mark pairs. The feed-forward compensations, a set of full-field patterns, are exposed to create layer two. If the method is successful, the pattern defined in layer two should be properly positioned with respect to the appropriate layer one target pair.

In phase two we create a third layer using the same feed-forward method as performed on the layer one alignment mark pairs. The layer three pattern is shifted to the right 1mm to interlock optical verniers in the pattern. The overlay error between layer two (feed forward) and layer three (feed forward), as measured by the optical verniers, provides the accuracy measurements of the feed-forward technique (**Figure 5**).

Discussion

The test results demonstrate an overlay accuracy of less than $1\mu\text{m}$, fully capable for most RDL layers in fan-out packaging processes. The method requires recognizable features on the reconstituted wafer/panel that can be used to register its position and establish a global reference frame for the individual field measurements. In some fan-out processes, these may already exist as a result of the embedding process. If not,

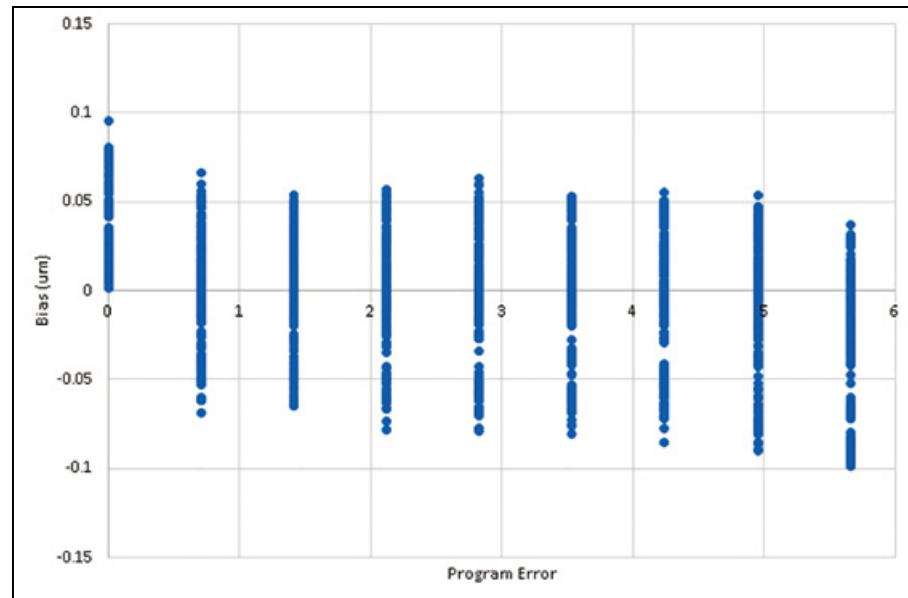


Figure 3: A bias/linearity chart plotting the magnitude of the error (Euclidean distance) for various program errors. Measurement errors are less than $0.1\mu\text{m}$ in all cases.

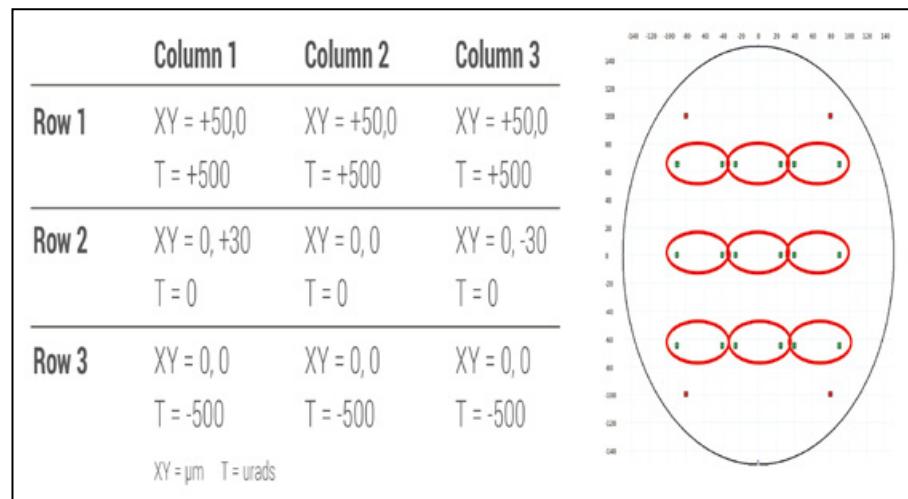


Figure 4: Layer one contains six targets (shown in red – four visible at the outer corners and two located between the circled target pairs in the middle row – obscured by the red circles) that define the wafer frame of reference and nine pairs (circled in red) in a 3×3 matrix that mimic the rotated and offset placement of individual die. The table on the left specifies the die placement errors of the target pairs.

steps can be taken to incorporate them into the process flow.

Large exposure fields are desirable to reduce the number of exposure cycles per panel/wafer. If multiple die are present in a large exposure field, each die may have slightly different placement errors. It may be possible to achieve acceptable overlay errors by computing an average or best fit correction for the full field based on the individual errors. It may also be possible to feed back the measured placement errors to the die placement tool to improve placement accuracy and

reduce individual placement variability. The challenges presented by multiple die in an exposure field exist regardless of the choice to use die-by-die or feed-forward alignment. The more die present in the field the greater the throughput benefit derived from avoiding die-by-die alignment. Ultimately, manufacturers must balance the throughput benefit of feed-forward corrections against any negative impact on overlay accuracy and process yield caused by multiple die in a single exposure field.

Summary

We have described a method to use feed-forward measurements of die placement errors to achieve the overlay accuracy necessary for RDL layer depositions. We have determined that the measurement capability of an optical inspection and metrology system is sufficiently accurate to provide the needed information. We have demonstrated sub-micrometer overlay accuracy between a layer deposited using the feed-forward method and one deposited with die-by-die alignment. Eliminating the requirement for die-by-die alignment, which may account for two thirds of the lithography cycle time, can dramatically improve stepper throughput and reduce photolithography costs.

Biographies

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Keith Best received his BS degree from the U. of Greenwich, and is the Director of Lithography Applications Engineering at Rudolph Technologies.

X	-0.45	X	-0.50	X	-0.60	X	-0.70	X	-0.65	X	-0.65
Y	-0.70	Y	-0.60	Y	-0.70	Y	-0.55	Y	-0.65	Y	-0.60
Mean	-0.35	-0.49				X	-0.50			X	-0.60
Min	-0.70	-0.70				Y	-0.60			Y	-0.60
Max	-0.15	-0.30				X	-0.35	X	-0.50	X	-0.60
STDEV	0.15	0.12				Y	-0.60	Y	-0.50	Y	-0.70
MN+3SIG	0.81	0.84				X	-0.20	X	-0.15	X	-0.40
						Y	-0.35	Y	-0.30	Y	-0.40
						X	-0.30	X	-0.30	X	-0.40
						Y	-0.45	Y	-0.40	Y	-0.40
						X	-0.20	X	-0.20	X	-0.35
						Y	-0.50	Y	-0.50	Y	-0.50
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						X	-0.30	X	-0.30	X	-0.35
						Y	-0.60	Y	-0.60	Y	-0.65
						X	-0.25	X	-0.20	X	-0.30
						Y	-0.30	Y	-0.40	Y	-0.50
						X	-0.30	X	-0.30	X	-0.35
						Y	-0.40	Y	-0.50	Y	-0.50
						X	-0.25	X	-0.25	X	-0.35
						Y	-0.65	Y	-0.65	Y	-0.65
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						Y	-0.50	Y	-0.65	Y	-0.45
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Package integration driving RF test complexity and requirements

By Judy Davies *[Advantest]*

High-performance wireless mobile products allow us to perform myriad connected tasks every day – from holding virtual meetings to watching streaming content to navigating through city traffic. All of these products are connected through a variety of wireless standards. These include Long Term Evolution (LTE), LTE-Advanced and LTE-A Pro smartphone standards, as well as LTE-M, Wireless Local Area Network (WLAN), Global Positioning System (GPS), ZigBee® and Bluetooth®. This glut of standards creates technological complexities, as these wireless technologies – many of which are enabling the Internet of Things (IoT) – have requirements and performance criteria that differ depending on the application in which they’re being used.

Devices built on the Third-Generation (3G) and Fourth-Generation (4G) LTE broadband standards, which cover most current frequencies, are being fully tested and characterized before they are packaged, assembled and shipped. Testing these RF-based system-on-chip (SoC) devices and RF transceivers for these applications creates unique challenges, as does test of analog baseband transceivers, with their various types of function blocks – transmit digital-to-analog converters (DACs), receive analog-to-digital converters (ADCs), audio DACs and audio ADCs, to name a few.

Looming on the horizon is the new Fifth-Generation (5G) standard. It promises to bring new levels of speed and capacity, with lower latency and greater flexibility than LTE, but its new encoding technologies and chip structures will require new production, packaging and test technologies. In fact, the expected needs of next-generation wireless networks are shaping the next-generation of RF test equipment.

Another factor is the proliferation of advanced packaging methodologies – e.g., fan-out wafer-level packaging (FOWLP), multi-chip packages (MCPs), through-silicon vias (TSVs), embedded passives and actives, and systems-in-package (SIPs), to name a few. These packages – all of which are competing for further dominance – are impacting how the industry goes about wafer sort, final test,

packaging test, burn-in and other steps required to go from basic wafer fab to end product.

Packaging integration essential

Practically speaking, in terms of packaging for RF transceivers, as well as for RF chips in general, every RF device still comprises a large number of passive components, such as capacitors and inductors, which allows it to be useable as an end product. Packaging integration is thus essential to turning an RF piece of silicon into a device that can easily talk to the antenna in the RF space. Three key aspects come into play in this regard:

1. Embedded passive devices – essential to making useful RF end products based on RF chips – embedded passives are a key element that outsourced semiconductor and test suppliers (OSATS) bring to the party.
2. Multiple standards – every mobile phone today utilizes a variety of standards, so implementing an RF set that can deal with various standards is critical. These multipurpose devices switch mode depending on the user’s location, increasing their complexity and contributing to their test challenges.
3. Multiple antennas – instead of a single antenna, multiple antennas are increasingly being employed within a wireless product. This is essential to ensuring that the device will work no matter how it is held by the user.

Turning all of these components into a decent RF package is an art. Ultimately, flexibility and scalability of automated test equipment (ATE) is a fundamental requirement in order to test these devices thoroughly – this includes both early die sort and final test once the peripherals and passives are attached within the integrated package. Test of advanced packages also requires more standardized ways of connecting everything together, but which approach will dominate is still being determined.

Regardless of the package technique employed, more rigorous functional test and

more robust compliance test are essential for the end-product requirement – this is where precision, capability and bandwidth of new equipment come into play. Combining a tester-per-pin architecture with massive parallelism is one approach to ensuring the high performance and high utilization chipmakers need to get their products to market more quickly, and at a lower test cost.

Learning from the past

A great deal of discussion is underway regarding how packaging impacts the way test cards are developed. There is a parallel here to what happened 10-15 years ago with respect to printed circuit boards (PCBs). Virtually every electronics company in the world created its own PCBs, put its own components onto the board, and put them into the electronic products that were purchased from store shelves. Board test was big business back then. That business has now changed and the chain has consolidated into subcontract manufacturing of PCB assemblies by a handful of very large players, with a few small ones hanging on.

Similarly, a significant change is coming with respect to package integration – there will be more and more integration as well as more into a single piece of silicon, creating smaller and smaller PCBs – or, in some cases, no board at all. As this industry shift continues to play out, the line between chip and package is blurring – particularly with more intelligence being put into the package. There’s also increasing competition for business between PCB load and assembly houses and OSATS, particularly with more complex integration schemes. What customers will choose depends on whether they need one-stop shopping, which the OSATS say they can do, or if there is still a board aspect involved for which they’d prefer to tap the capabilities of the more traditional PCB load/assembly providers.

Regardless of how this shakes out, we know from these past shifts in the PCB space that integration at the package level will take time to shake out. And the complexity will grow even more, increasing the pressure on the test sector to deliver methodologies that will allow

manufacturers to alleviate their time to market and cost pressures.

Parallelism, coverage lower costs

Signal transmission and reception in 5G systems – including techniques such as the aforementioned multiple antennas within a single housing – will also impact the requirements of future test equipment. The fundamental test requirements for 5G are further complicated by the anticipated billions of IoT devices with different types of sensors using low-power wireless links to connect to the internet. These sensors are expected to be located literally everywhere, allowing us to access, interact with and control our environment whether at home, in our cars, or at work.

Current RF testing solutions, which typically require multiple cards plus a separate calibration kit, have employed a fan-out architecture in which subsystem resources are shared. This means that devices with multiple frequency paths are actually tested in serial within the device, rather than in true parallel mission mode testing. It also means that only one RF standard can be tested at a time per site.

One new solution is Advantest's V93000 channel card called Wave Scale RF that condenses four independent RF subsystems into one integrated card with a high degree of parallelism – up to 192 ports for parallel testing of multiple RF device types – by omitting shared resources (Figure 1). This removes the limitations placed on test speedup, reducing test times by 50% or more, and enabling device parallelism of 16, 32 or even higher, which cuts the per-device to a mere fraction of that associated with existing approaches.

These cards, together with complementary Advantest V93000 Wave Scale MX (for mixed-signal) cards, can simultaneously test multiple standards or multiple paths within each RF device, achieving in-site parallelism as well as high multi-site efficiency. Devices can be tested up to three times faster than with other approaches – significantly reducing the cost-of-test. This is a key requirement for OEMs and fabless semiconductor companies that need to get volume RF-enabled devices to market as quickly as possible.

The new card is optimized for analog IQ baseband applications and testing of high-speed DACs and ADCs. As with Wave Scale RF, Wave Scale MX omits shared resources, delivering parallel, independent operation of all 32 instruments controlled by a hardware sequencer. This is essential for leading semiconductor and telecommunications chip

providers, who must deal with a 10x reduction from what they sell into cell phones to what they can charge in the industrial area. The challenge in this environment is that the functionality, from a security perspective, has to be as safe as a phone line, while ensuring that the data is directed into the right channel and properly authorized – i.e., the security requirement is as high, or even higher, as it is for phone line communication.

One of the biggest concerns about the IoT is the security aspect – under these conditions, silicon providers are going to be under some tremendous pressures to guarantee that whatever they deliver adheres to industry reference standards. Whether these standards will be as stringent as those adopted within the automotive and aerospace industries remains to be seen, but they will most certainly need to be stronger than consumer grade.

The requirements noted above serve as further evidence that devices will need to be qualified and tested rigorously and robustly, with manufacturers also needing to ensure long-term device reliability (again, based on user demand), so the pressure on delivering high-quality devices at the lowest possible investment cost will continue to escalate. This proliferation requires a breakthrough in methodology and serves as further justification of the need for advanced, appropriate equipment

that can fully take advantage of these changes in the RF device landscape.

Biography

Judy Davies is VP of Global Marketing Communications at Advantest; email mktgcomms@advantest.com

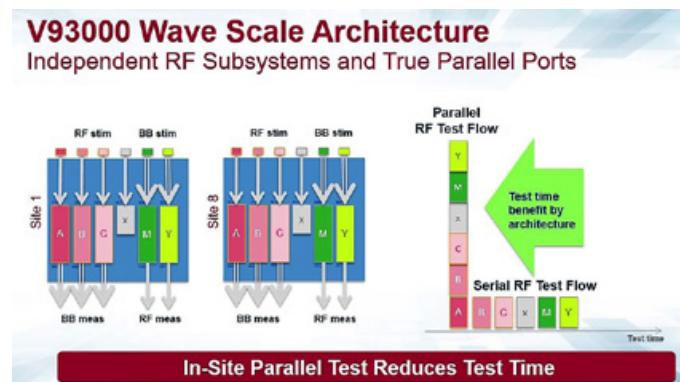


Figure 1: V93000 Wave Scale architecture. SOURCE: Advantest



The benefits of cross-licensing for IC packaging

By Kevin Roe [Intellectual Property Attorney] and Phil Marcoux [PPM Associates]

TSMC is reported to be spending over \$1B on advanced IC packaging development. Intel, the third largest R&D investor, plans to devote a sizable allocation of its R&D dollars to advanced IC packaging [1]. Likewise, Samsung is expected to make a sizable IC packaging investment (**Figure 1**). In addition to their internal development, these companies do not rely solely on in-house generated patents for creation and protection of their products and processes.

Creating and defending intellectual property for anything, not just IC packaging, have become very dicey, expensive and complex business requirements. Until the late 1990s,

much of the semiconductor segment of the electronics industry sought to share intellectual property using what are called “cross licensing” agreements to help advance both the success of the corporation and the industry. This strategy wasn’t implemented because of the benevolence of the industry leaders, but more often out of the realization that key technology developments were expensive to discover, develop and protect.

Starting in the mid-1990s a number of parties and companies discovered that they could gain more commercial value by independently licensing their IP rather than enter into cross license agreements. In some cases, their licensing tactics resulted in several very expensive and bitter litigations. By mid-2000, several large companies banded together to seek changes to the patent system to reduce their exposure to litigation. In response revisions to the

U.S. patent system were made via the America Invents Act that was signed into law in 2011 [4]. These resulting revisions to patent ownership, put into practice by the U.S. federal courts and the U.S. Patent Office, were seen by many as protection against meritless patent harassment (Non-Practicing Entities, i.e., parties that don’t actually use the patents they seek to enforce). However, one unfortunate consequence of this legislation actually supported and resulted in the demonization of individual inventors and their patents in the U.S. One of the most onerous and less understood revisions is the expanded rights of accused infringers and third parties to file re-examination requests against any patent and to wage ongoing appeals. This anti-inventor legal bias will have extremely negative consequences for the U.S.

Many companies are continuing to look for ways to reduce their legal costs and exposure even further. As a result of the changes in patent treatment, cross-licensing agreements are now returning as an attractive and viable way to indirectly monetize corporate patents. For example, even in the IC packaging business arena, companies known as outsourced semiconductor assembly and test suppliers (OSATS)

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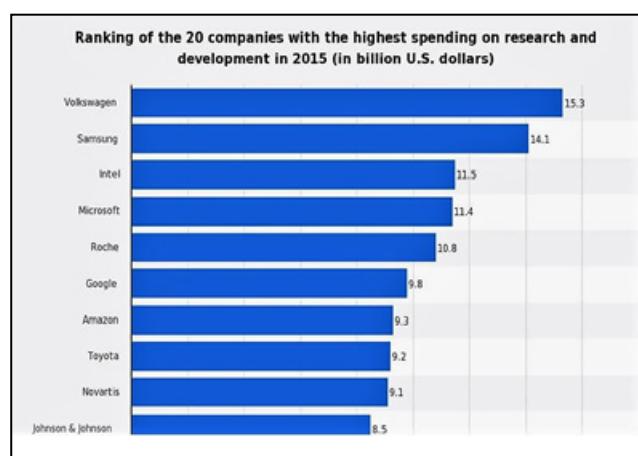


Figure 1: Ranking of the top 20 R&D investing companies in 2015 [2].

are said to be investigating such arrangements, which is a new twist to their traditional mode of business.

Cross-licensing of patents allows the parties to the agreement to exploit and commercialize products using what's protected by the patents. Sometimes the parties contribute money, and sometimes other IP as payment for entering the agreement. Another arrangement is to join a consortia. There are a number of consortia devoted to advanced IC packaging and a number of new ones are emerging. Some of the better known international IC packaging consortia include imec (Belgium), Leti (France), Fraunhofer IZM (Germany), NCAP (China), and A*Star IME (Singapore). Some industry analysts feel that the U.S. lags in IC packaging consortia efforts, but there are a few IC packaging consortia, including Georgia Tech PRC, AIM Photonics (NY), and NextFlex (CA).

Crafting a cross-license agreement has many potential pitfalls, the least of which could be running afoul of anti-trust laws. Therefore, the parties are advised to have expert legal help. Having a thorough understanding of what each party can potentially gain and potentially lose in the agreement is also advised to avoid having the agreement fail to meet each party's expectations. Consortia patent licensing agreements have an additional set of issues and will be discussed in more detail in a later article to be published here. Cross-licensing of patents between companies and other organizations offers at least eight major advantages:

Avoidance of expensive litigation. Litigation typically ranges in costs from \$40,000 to reach a summary judgment in a U.S. federal district court to as much as \$2,000,000 for a full-scale trial. Filing appeals to the U.S. Court of Appeals for the Federal Circuit or the U.S. Supreme Court can typically cost from \$50,000 to \$500,000 for each court.

Avoidance of enormous time investments. Litigation cases can last months to several years consuming critical technical staff in support of litigation defense or offense. Avoidance of risking your company's

future on rulings that could potentially be biased or made by judges with little technical education or practical work experience in technology. Sometimes, such rulings are made without even a basic understanding of which audience a patent is actually written, or what purpose a patent is supposed to serve.

Avoidance of negative publicity, which can be devastating to employee morale and customer relations;

Gaining access to new technology more quickly than by internal efforts (frequently leap-frogging several years of development and debugging);

Gaining access to new technology without large cash outlays for internal efforts (which can literally range from several millions to billions of dollars);

Gaining access to new technology developed from fresh, external viewpoints without internal limitations in imagination (yes, even engineering and research staff can be herded and

stampeded over the cliff by group-think); and

Gaining access to new technology that potentially has already been debugged and vindicated by successful commercial products (debugging internally developed new technology, can take several years, but market windows of opportunity can sometimes only last months).

History records a number of cross-license patent agreements in the semiconductor sector that resulted in huge benefits to both the participants and the industry. Some notables include: Intel and NVIDIA for chipsets [6]; Microsoft and JVC in 2008, which cleared infringement challenges to Linux [7]; and possibly one of the more significant agreements being those between Intel and AMD that ended years of bitter legal battles and opened production of critical microprocessors to others [8]. Beyond the packaging

The advertisement features a teal background with white and light blue geometric shapes. At the top left is the SEMI logo. The main title "ISS EUROPE" is prominently displayed in large white letters, with "INDUSTRY STRATEGY SYMPOSIUM" in smaller letters above it. Below the title is the subtitle "EUROPE LEADING THE NEXT WAVE OF INNOVATION". To the right, a circular graphic contains the text "5-7 MAR 2017 MUNICH GERMANY". At the bottom, a white bar contains the text "REGISTER NOW AT: WWW.SEMI.ORG/ISSEUROPE".

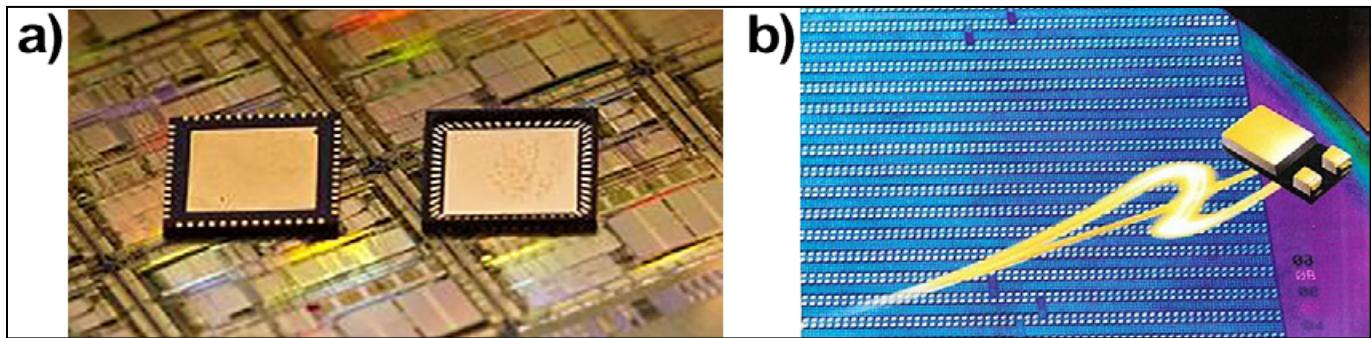


Figure 2: A few examples of cross-licensing used in IC packaging; a) (left) QFN packaging and b) (right) WLP. SOURCES: Promex Industries and Motorola

industry, possibly five of the most influential examples of innovations that came about because of cross-licensing agreements and that resulted in large benefits for society are DVDs (1998), MPEGs (1997), RFIDs (2005), sewing machines (1856), airplanes (1917), and DVDs (1998).

Specific to IC packaging there are a few examples of cross-license agreements including those for joint packaging development and manufacture by Unisem and ASAT (for QFN and related lead-less packaging), Amkor and UTAC (for QFN and MLF packaging), and Motorola and ChipScale, Inc. (for wafer-level packaging) (**Figure 2**).

There are a number of ways to structure additional elements of cooperation into cross-licensing agreements for the benefit of the parties to the agreements. Grant backs, patent pooling, joint defense, and “freedom to operate” pools are examples of such benefits. Although it should be noted that the legal liabilities should be capped in cost (especially by smaller companies) so that these costs will not exceed the fundamental economic value of the technology gained from the agreements.

Cross-licensing agreements are re-emerging as a vital element for any business. Semiconductor packaging developers and users will have much to gain forming such agreements as wafer-based and other advanced IC packaging methods and multi-chip manufacturing methods become the norm for electronic products. Such agreements will replace the maturing

individual packaging and surface mount technology (SMT) assembly methods. Cross-licensing agreements can cover the sharing of new technology for IC system packaging design: for example – improved I/O signal conduction, improved power and ground supplies, and/or improved heat dissipation), quick prototype fabrication, large-scale manufacturing, functional testing (e.g., testing at full speed or testing at a greater or a reduced speed), and/or reliability testing (e.g., test fixtures for highly accelerated stress testing (HAST), radiation testing, vibration testing, or other types of reliability testing.

Acknowledgment

The above article is not intended as legal advice. Readers with specific legal concerns should consult an attorney experienced in intellectual property issues and litigation for advice.

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Biographies

Kevin Roe received his JD from Santa Clara U. Law School, a PhD in Electrical Engineering from the U. of California, Davis, and an MS in Electrical Engineering from Stanford U. He is an intellectual property attorney in Saratoga, CA; email kevin.roe@att.net

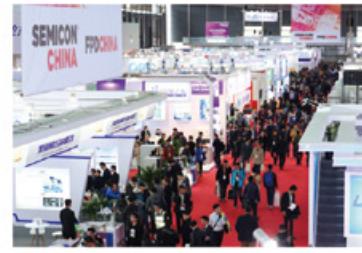
Phil Marcoux received his MSEM (MSEE/MBA equiv.) from Santa Clara U., a BSEE from the U. of Florida, and is a past Associate Professor in the Graduate School of Engineering at Santa Clara U. He has been named Father of SMT (in the U.S.) by the IPC in 2007. He is Managing Director at PPM Associates; email oneppm@ymail.com; website www.oneppm3d.com



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Harsh Environment Pkg
Pkg for Medical Applications
Thermal/Mech Simulation
Reliability of Interconnects

HIGHLIGHTS

- 41 technical sessions including:
 - 5 interactive presentation sessions, including one featuring student presenters
- 18 CEU-approved Professional Development Courses
- Technology Corner Exhibits, featuring more than 100 industry-leading vendors
- 6 special invited sessions
- Several evening receptions
- 3 conference luncheons
- Multiple opportunities for networking
- Great location

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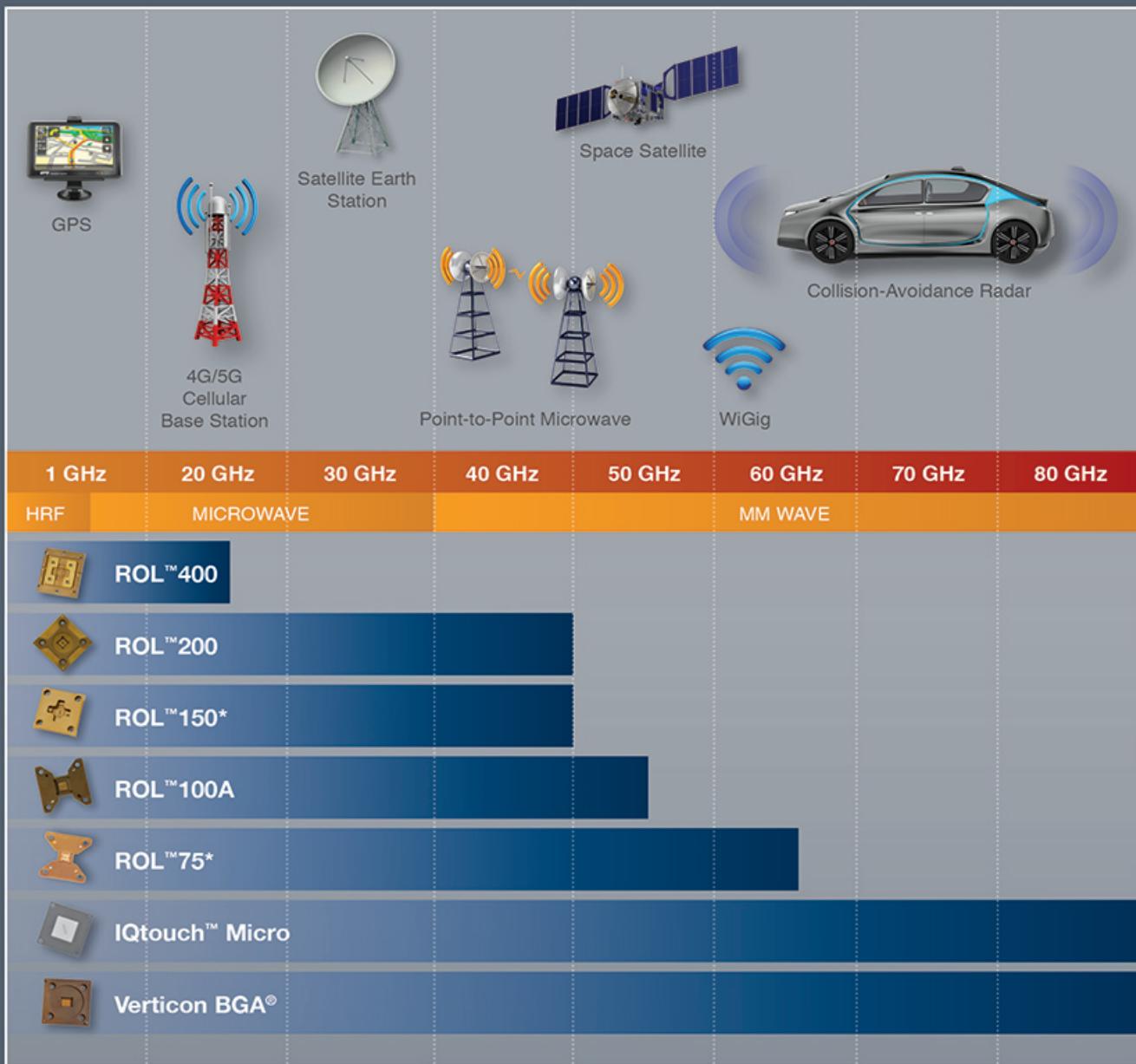
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March April 2017

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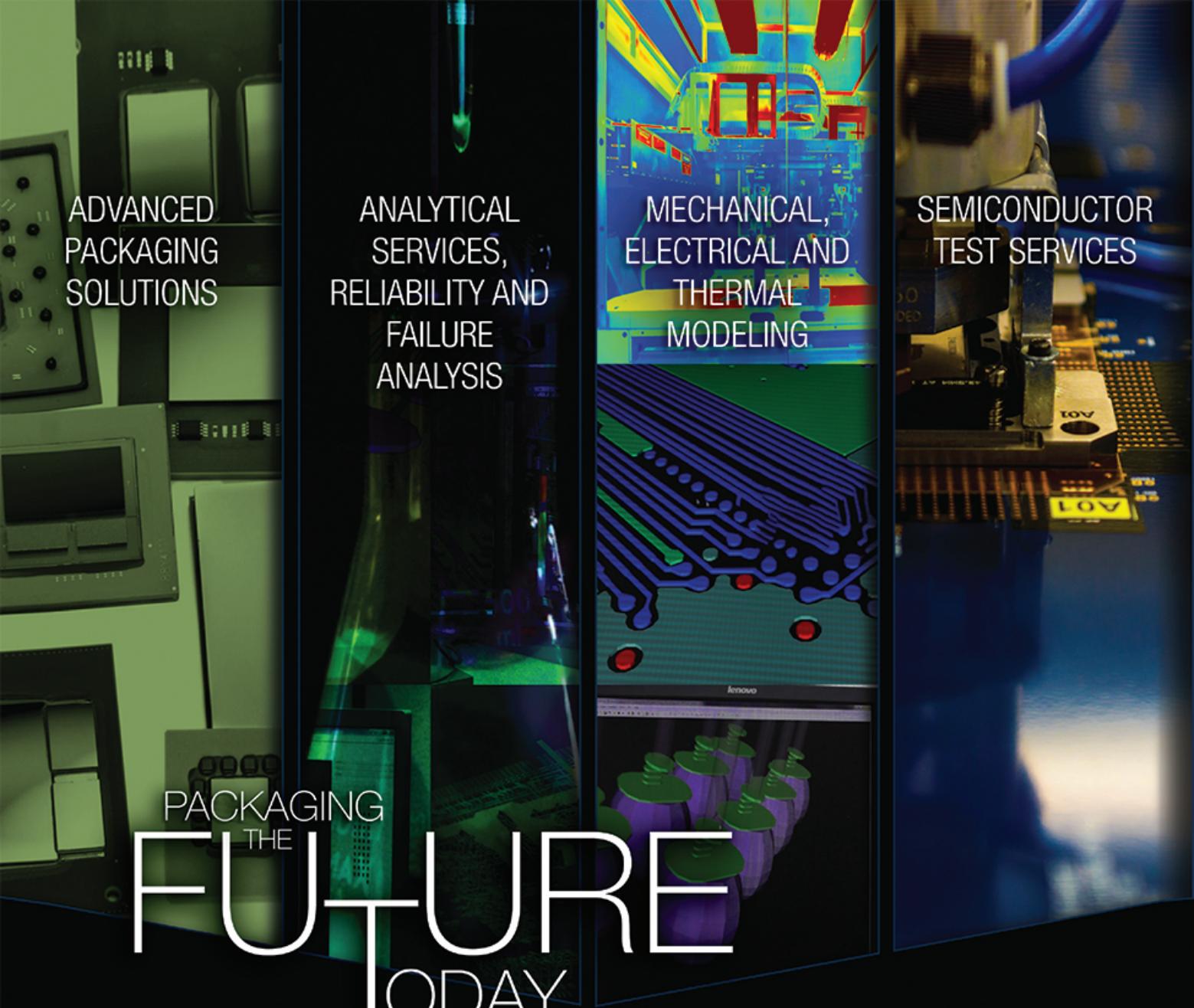
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