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The Future of Semiconductor Packaging

Volume 23, Number 5

September • October 2019

Ultra-thin Si die integration

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An illustration of the latest development towards the integration of ultra-thin silicon bare dies within a flexible film. ChipInFlex is a generic wafer-level process for manufacturing a flexible label that integrates silicon components. Working on a silicon carrier helps achieve a high resolution of integration. The process described is the first to offer flip-chip silicon dies interconnection within a flexible film and collective thinning.

Photo courtesy of CEA-Leti

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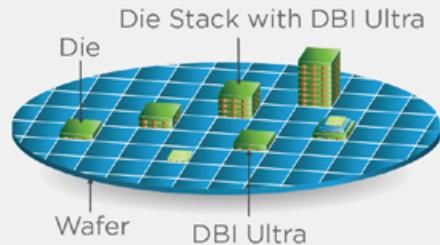
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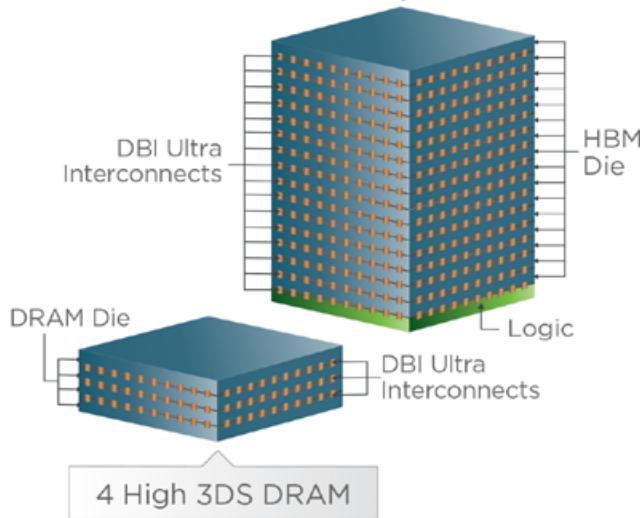


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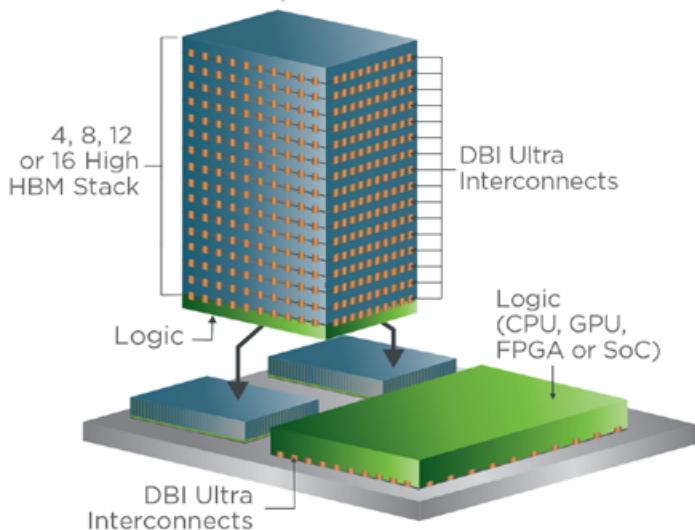
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EXECUTIVE VIEWPOINT



R&D challenges associated with emerging technology platforms

Chip Scale Review (CSR) asked UTAC's President & CEO, W. John Nelson, PhD, to respond to questions that provide insights into the challenges associated with its research and development (R&D) focus on several technology platforms

CSR: The company is focusing its R&D on several packaging technology platforms that you believe are poised for the most growth: lead-less, power devices, microelectromechanical systems (MEMS), wafer-level chip-scale packaging (WLCSP), image sensors, and system-in-package (SiP). What are the primary drivers for these technologies and how will you be able to work on 6 different platforms without losing focus? Is there a lot of cross-over potential for the R&D that will have to be done?

UTAC: Lead-less package technology remains one of our strong growth areas driven by some of the growing product

segments such as analog and power products. We have seen, and expect to see, significant growth in these segments driven by Internet of Things (IoT), cloud computing, and automotive markets, for example (**Figure 1**). We not only have intellectual property (IP) in the core quad flat no-leads (QFN) technology, but also own IP for automotive-grade sidesolderable QFNs and a grid array QFN product called GQFN. We are positioning the company to be a key packaging solution provider for the 5G market starting in 2020. We are also developing flip-chip molded interconnect substrate (MIS) technology.

Our focus on MEMS has paid significant dividends in the last five years. We went

from providing simple MEMS oscillators, to being one of the leading outsourced semiconductor and test (OSAT) providers for complex inertial sensors for leading MEMS integrated device manufacturers (IDMs) in the world. We are developing more complicated sensor packaging such as oil-level sensors for automotive applications. We hope to enjoy the growth of MEMS driven by its increasing adoption in various markets such as mobile, automotive and IoT.

We continue to work on advanced WLCSP solutions in Singapore, which includes advanced technology, such as plasma dicing. Additionally, we are getting ready to address the next wave of growth for fan-out WLCSP in handset applications.

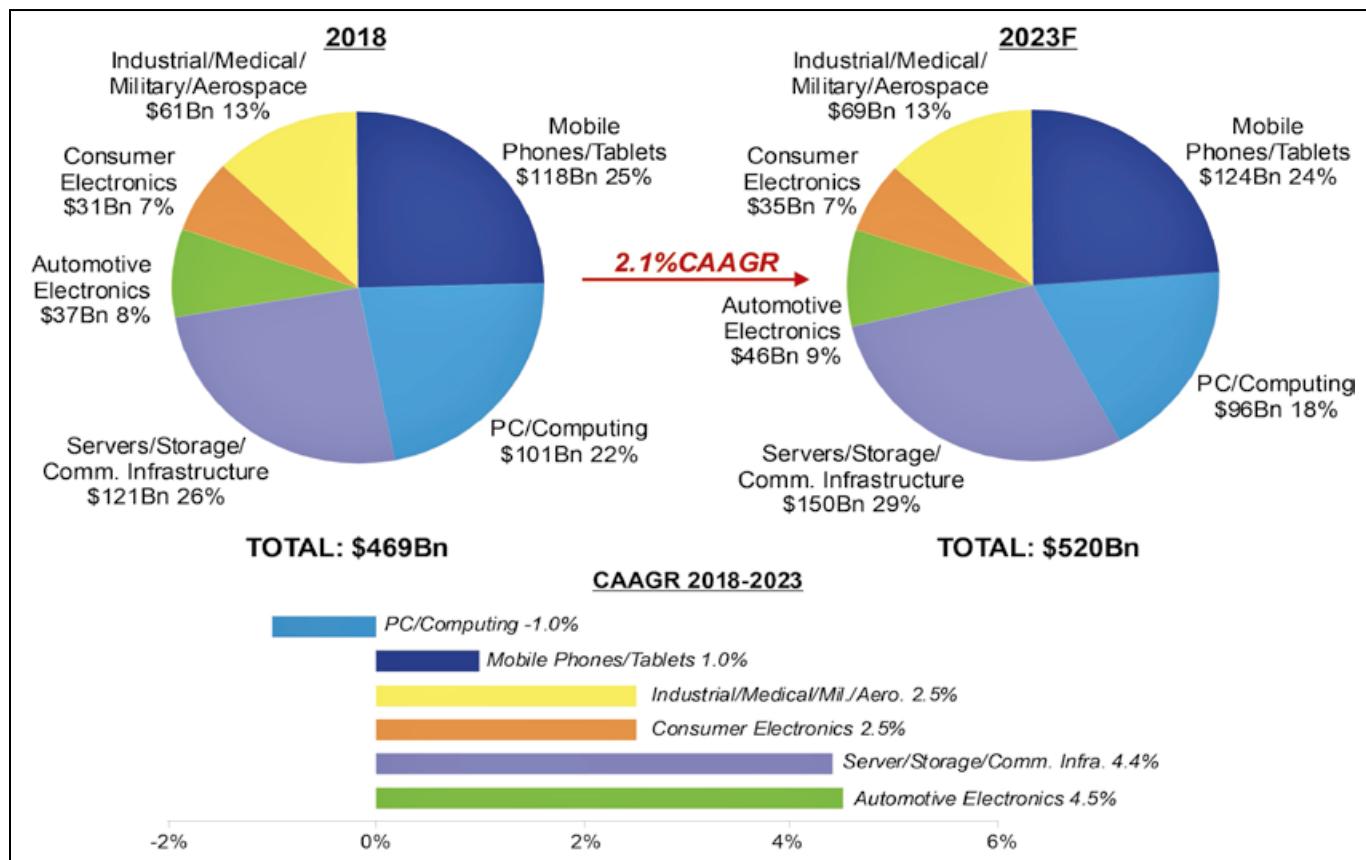


Figure 1: Drivers of the semiconductor market. SOURCE: Prismark

We have been providing industrial and automotive image sensors to IDMs in Japan. Image sensors are one of our growth platforms driven by its ubiquitous adoption in security, traffic, industrial and automotive applications. In that line, yes, we are working on low-cost, high-quality image sensor packaging solutions.

I just returned from visiting our IDM customers and I definitely sense that directionally, the IDMs are going towards providing more and more system-level solutions. While our SiP center of excellence is in our Dongguan factory, we are now proliferating our capability into our Thailand facility to address the growth in lead-less SiP package solutions.

We have dedicated engineers for each of these development products, but yes, there is a lot of knowledge that gets shared. We use a rigorous Phase-gate development process and I have also established a project management discipline to ensure quick identification of roadblocks. This process has worked greatly towards our success of first-time qualifications. So, while it may sound like we are working on quite a few items, the team is actually very focused on particular growth product and package families for specific customers.

CSR: The company scheduled full qualification of new packaging technology to achieve higher I/O in a small foot print with improved reliability by 1Q19. Did the company meet this goal, and what were the results?

UTAC: We have been a leading supplier of WLCSP back-end assembly and test services for over ten years in our USG1 factory in Singapore. Because we do not provide the front-end services of redistribution through ball drop, we are able to have foundry and other OSATS as customers. FOWLP demand was outpacing supply, so we collaborated with a third party to develop a robust back end of line assembly and test service for key customers. This particular technology provides improved interconnect density and board-level reliability vs. standard fan-in wafer-level packages, so is an attractive package for many applications including mobile and automotive. Our development requirements were met in Q1, which now allows us to support FOWLP services in our Singapore facility.

CSR: The company has scheduled sidewall WLP development and new dicing technology for completion by the end of 2Q19. What is the status on these projects and what were the technical challenges you had to overcome?

UTAC: We already had a qualified sidewall WLP back in 2017 and ready for production. We are currently engaged with customers for 1-side, 5- and 6-sided sidewall protection. For 1-side protection we are currently running engineering builds in USG1; our processes are fully qualified. For 5- and 6-sided protection we are engaged with an alpha customer. The technology has been ready for some time and now, development is focused on our ability to scale and reduce cost.

For new dicing technology such as plasma dicing, we are collaborating with an alpha customer and the equipment supplier for qualification with consigned equipment installed at USG1. We have completed qualification builds for several 200 and 300mm wafers with different devices. 200mm-based devices have all passed the customer's reliability tests without any failures. 300mm-based devices have passed time-0 tests and are now undergoing reliability tests. The development and factory team are gearing up the equipment for production readiness for our alpha customer and we are on schedule for the development.

CSR: What are the technical challenges you are facing as you make progress in the mixed-signal and RF test and probe segments? How vital are these market segments to future growth?

UTAC: These challenges are, in some ways, more of a commercial and economic nature. More specifically, in the area of testers, there is a range of solutions from lower cost, more niche and less fungible systems that satisfy some of the customer base, to the other end of the range with higher cost, more flexible systems that can satisfy a broader range of customers. This always requires careful investment considerations to satisfy the customer base in terms of cost. We continue to provide capabilities across all the mainstream testers and are making strategic plays into the niche testers.

In the area of wafer probe, there is an increasing trend to tri-temperature automotive probe and thin-wafer probe. In terms of final test handlers, there's also increased demand for automotive tri-temperature and increasing complexity with respect to multi-mode sensor and actuator handlers (e.g., 9 DoF gyro, magnetometer and accelerometers). The latter area does need more attention from equipment suppliers. We are positioned to help customers lower their cost of test with various types of high-parallelism strip test.

CSR: Are there other challenges the tester/probe industry faces that require an industry-wide approach (e.g., standards, roadmap consensus, etc.) that you believe need more attention by industry leaders?

UTAC: As described earlier, there are two ends of the tester solution range, from niche to flexible. This continues to foster healthy competition among the two largest suppliers that own 75% of the market and the niche players in the other 25%. In the handler space, more effort is needed in the challenging area of multi-mode sensors and actuators to offer cost effective solutions. In the film frame probe area, more attention is needed to facilitate hot temperatures, which is highly dependent on the film (tape) suppliers.

Biography

W. John Nelson, PhD, is President & CEO of UTAC, Singapore. He joined UTAC in October 2012 with more than 30 years of experience in the semiconductor industry. From 2007 to 2012, he was the EVP and COO of ON Semiconductor. He has a BS degree with honors and a PhD in Physics from the U. of Ulster, Northern Ireland. Media inquiries, please contact Carol Chiang, email: carol_chiangsm@utacgroup.com Tel: +65 67142220

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Integrating ultra-thin Si dies within a flexible label

By Jean-Charles Souriau [CEA-Leti]

Recent developments in the integration of ultra-thin silicon dies within a flexible film lead to a new paradigm. Indeed, thanks to the thinness and flexibility of devices, it is conceivable that functions can be added around any object without changing its aspect [1-5]. Currently, only electronic tracks between components are flexible in the major flexible electronic products on the market. This is due to the fact that the silicon components are already packaged or are too thick. In order to get fully-flexible devices, silicon dies have to be thinned to less than 100 μm . Three formats can be processed to build flexible electronic systems: ribbon, panel or wafer. The first two formats are well-adapted for large devices, are low cost, and allow high throughput. Patterning resolution in these formats is only fair, however. Working with silicon wafers helps achieve high resolution of integration. Silicon wafers are well-suited for flexible fan-out packaging, which helps build a heterogeneous, flexible system that combines a panel substrate, including a printed device and interconnection network with a silicon electronic die integrated within a small flexible label.

New process development

One challenge is to offer a process compatible with bare dies. A new technology called ChipInFlex proposes the integration of ultra-thin silicon dies within a flexible label made on a wafer carrier in the manufacturing microelectronic line [6]. It was chosen for the electrical interconnection gold stud bumps because it enables the hybridization

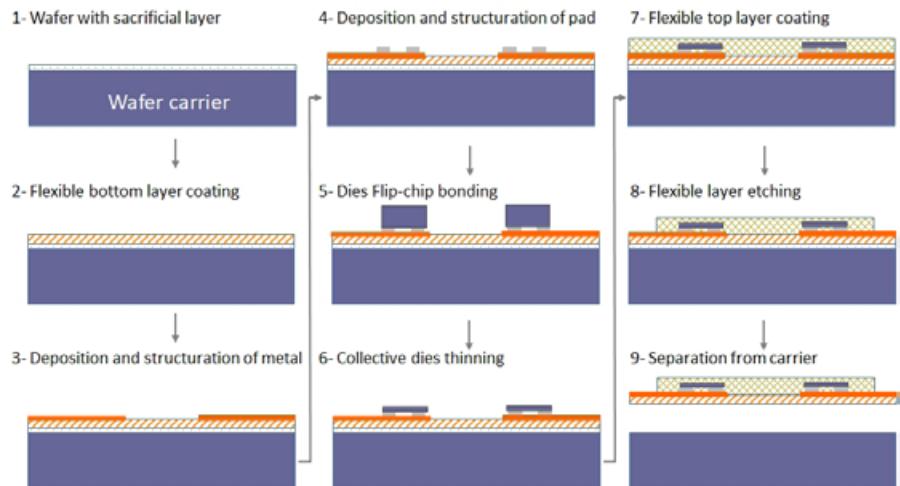


Figure 2: Wafer-level process flow of silicon dies' encapsulation.

by thermocompression at low temperature ($<150^\circ\text{C}$) and it is compatible with the polymer (Figure 1). Indeed, the use of solder bump, such as SnAgCu, was not conceivable. Moreover, stud bumps also can be made on bare dies. The choice of the flexible material in which to integrate silicon dies is critical. In the ChipInFlex study, we tested the commercialized photosensitive siloxane polymer SiNR, which is available in spin-on or dry film, and has low stress and a low-cure temperature. The manufacturing process experiment is detailed in Figure 2.

The carrier is a 200mm silicon wafer, which was treated to get a temporary adhesion layer. A SiNR film 30 μm or 80 μm thick was deposited by spin coating or laminating. The electrical network

was made of $\text{WN}_{50\text{nm}}/\text{Au}_{200\text{nm}}$ metallic. A 50 μm -thick coating of silver glue was deposited on pads by serigraphy. Dies were aligned and attached on the wafer using a DATACON flip-chip tool. The equipment system enables dispensing dots of polymer glue and then aligns and mounts the components under a combination of heat and pressure. In this study, the Epo-Tek E505 glue was used because of its useful viscosity properties as a function of temperature. Stud bumps can easily go through the glue and contact gold pads on the substrate. The bonding was performed in two steps. All dies were attached with the flip-chip tool and then collectively bonded using an EVG thermocompression bonder. Collective thinning, including coarse and fine grinding, was performed

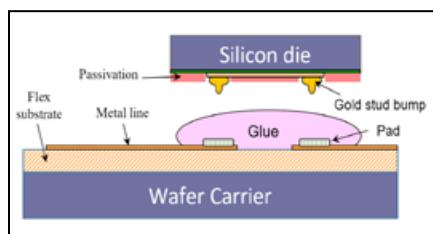


Figure 1: Flip chip Interconnection using gold stud bump.

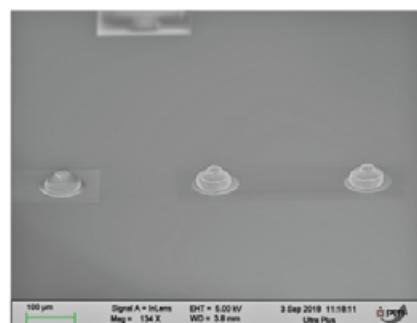
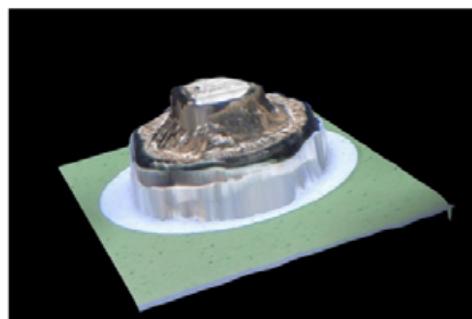


Figure 2: Gold stud bumps on a test vehicle.



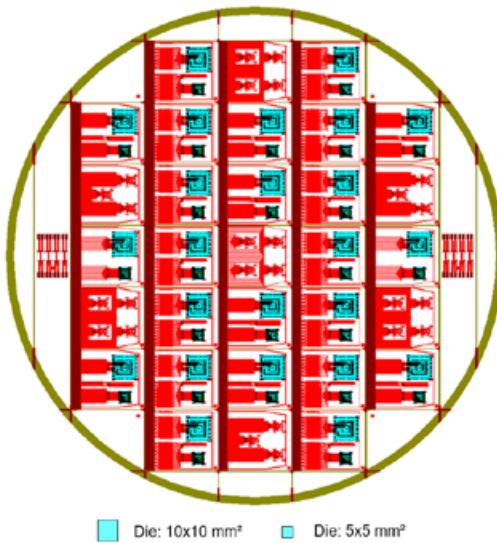


Figure 4: 200mm test vehicle wafer with 24 labels including large and small dies.

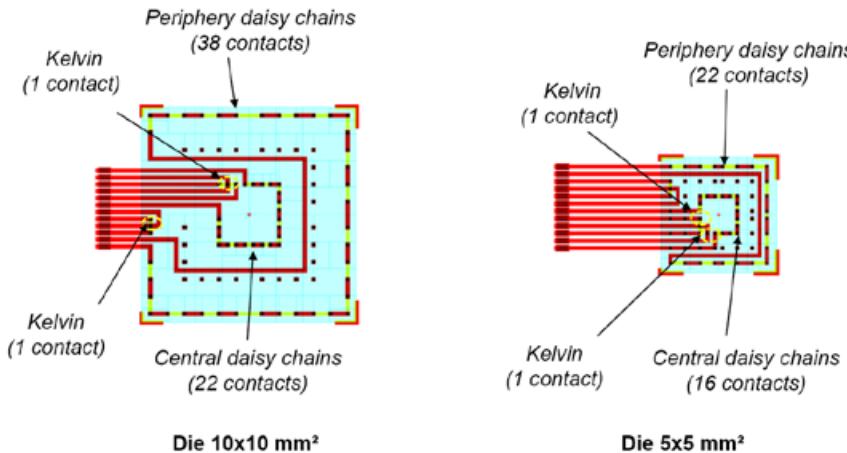


Figure 5: Layout overview of a four-point Kelvin pattern and daisy chains in silicon dies.

to reduce the die thickness to $\sim 40\mu\text{m}$. An additional $80\mu\text{m}$ -thick SINR layer was laminated under vacuum to encapsulate dies and the polymer was opened locally to reach metal lines and allow external connection. Finally, flexible labels were diced by laser and taken from the wafer carrier.

Results on electrical test vehicle

A silicon test vehicle was designed to mimic bare dies. Two sizes of chips were designed, $5 \times 5\text{mm}^2$ and $10 \times 10\text{mm}^2$, respectively. The test vehicle included $0.6\mu\text{m}$ -thick AlSi lines and passivation layers of SiO_2 ($0.5\mu\text{m}$ thick), and SiN ($0.6\mu\text{m}$ thick), respectively. Gold stud

bumps were formed on pads using standard ball-bumping equipment. The stud bumps were approximately $70\mu\text{m}$ in diameter and $30\mu\text{m}$ in height (Figure 3).

The wafer included 24 $30 \times 25\text{mm}^2$ labels and each one could receive one large and one small die (Figure 4). The test vehicle was designed to test the resistance of a single contact between the die and the flexible substrate thanks to a four-point Kelvin pattern. In addition, the continuity of daisy-chain structures, located at the periphery and at the center of the dies, could be measured (Figure 5). These patterns include from 16 to 38 contacts according to the size of dies and position.

Three wafers were fully populated and electrically characterized. Wafers 1 and 2 included a bottom polymer layer $80\mu\text{m}$ thick. Wafer 3 included a bottom polymer layer $30\mu\text{m}$ thick. For comparison, a fourth wafer without bottom polymer was populated only with small dies. Electrical tests were performed during the manufacturing process after the main steps, flip-chip bonding, backside thinning and final encapsulation (Figure 6). More than 90% of the Kelvin structure was functional. Global average values of Kelvin patterns are presented in Figure 7 and details for each location are shown in Table 1.

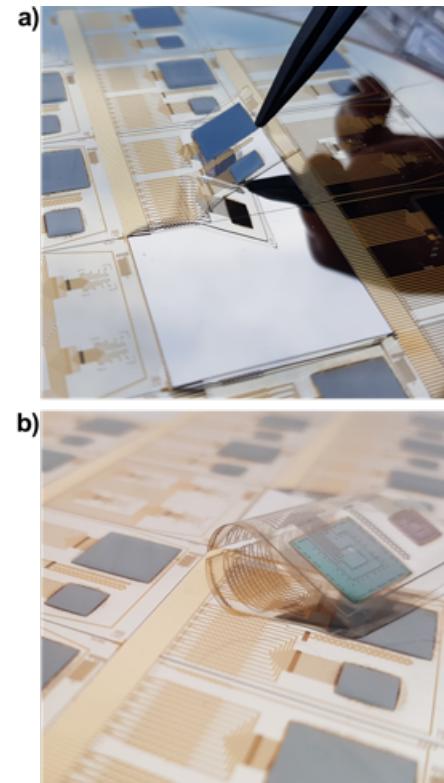


Figure 6: Label including silicon dies flip-chip bonded and thinned down to $40\mu\text{m}$.

Table 1: Average resistance (in mOhm) of Kelvin patterns.

		Large dies		Small dies	
		Peripheral	Central	Peripheral	Central
Wafer 1	After bonding	11	14	14	11
	After thinning	11	15	15	11
	After coating	15	15	15	12
Wafer 2	After bonding	9	10	11	13
	After thinning	9	10	11	13
	After coating	11	11	12	13
Wafer 3	After bonding	6	9	7	9
	After thinning	6	9	7	9
	After coating	8	10	8	8

The final average resistance of a single contact was found to be from 12 to 14mOhms for wafers with an 80 μ m-thick bottom polymer, 9mOhms for the wafer with a 30 μ m-thick bottom polymer and 3mOhm for the wafer with no bottom polymer. The presence of a bottom polymer layer helped absorb the force on the stud bump during the thermocompression process and probably

reduced the resistance value of the contact. No differences were observed between the center and the periphery of dies. **Figure 8** shows the mapping of a central four-point Kelvin pattern measured on a small die on the periphery after final coating. The continuity of all the daisy chains was tested and the functionality rates are presented in **Table 2** after each step.

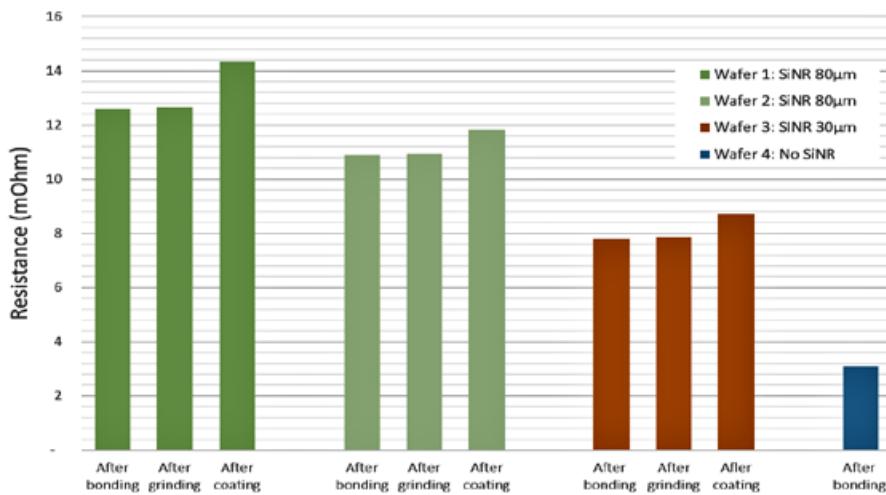


Figure 7: Global average resistance of Kelvin patterns measured after main steps of the process.

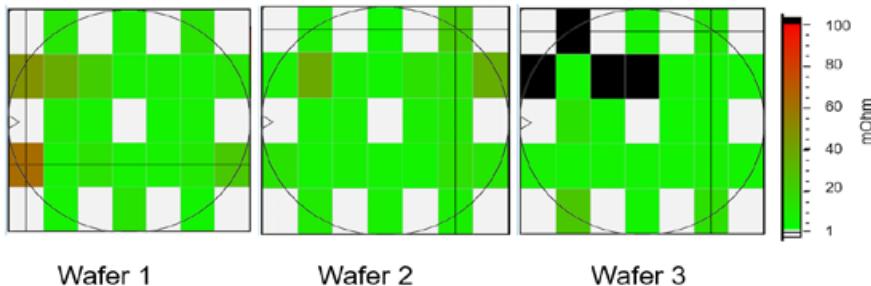


Figure 8: Resistance value mapping of a central four-point Kelvin pattern measured on small die in the periphery after final coating.

		Large dies		Small dies	
		Peripheral	Central	Peripheral	Central
Wafer 1	After bonding	87.5	100	87.5	100
	After thinning	87.5	100	87.5	100
	After coating	83.3	100	91.7	100
Wafer 2	After bonding	95.8	100	100	100
	After thinning	95.8	100	100	100
	After coating	91.7	100	100	100
Wafer 3	After bonding	100	100	100	100
	After thinning	100	100	100	100
	After coating	83	75	88	83

Table 2: Percentage of functional daisy chain after the main steps of the process.

	Line		Large die		Small die	
	Straight	Zigzag	Periph. daisy chains	Central daisy chains	Periph. daisy chains	Central daisy chains
Cal. value	56	51	67	39	59	43
Label n 1	62	50	65	40	53	41
Label n 2	58	45	68	39	53	39

Table 3: Resistance (in Ohm) measured of test patterns and compared with calculated values.

First, it can be noted that more than 87.5% of daisy chains were functional after bonding, which is a very good result for a new development. Moreover, the percentages of valid central daisy chains are excellent—100% for the three wafers. The most remarkable result from this study is that no failures occurred after thinning. It can be observed that yields are slightly reduced after coating, and few daisy chains failed. However, more data are needed to draw conclusions.

Two flexible labels were diced using a laser and removed from the wafer carrier. A printed circuit board (PCB) was designed and manufactured to facilitate electrical characterization. A ZIF connector was used to interconnect the label on the

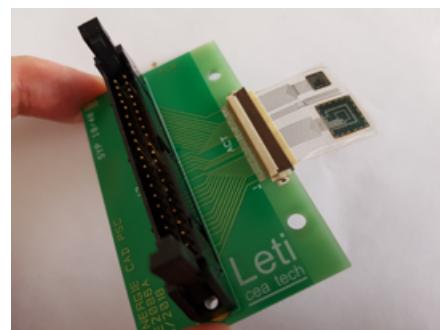


Figure 9: Printed circuit board to interconnect the label using a ZIF connector.

PCB (**Figure 9**). Six test patterns were measured. The first two patterns were just electrical tracks on the polymer without contact with the silicon die. The goal was to ensure that metal lines were not damaged by removing the label from the carrier. Peripheral and central daisy chain patterns of large and small dies were measured. Electrical results are summarized in **Table 3** and compared with calculated values.

It has to be pointed out that all central daisy chains in the study were functional. Moreover, measurements closely agree with calculated values. More tests are ongoing on new labels to confirm these results.

Summary

With ChipInFlex, a new paradigm was introduced for integrating ultra-thin silicon bare dies within a flexible label made on the wafer carrier. ChipInFlex is a generic wafer-level process for manufacturing flexible labels and integrates silicon components. This process is the first to offer flip-chip silicon dies interconnected within a flexible film. The electrical interconnection is achieved with gold stud bumps made

on bare dies. ChipInFlex is also the first packaging solution that can perform collective thinning on the wafer. The process has been successfully validated on an electrical test vehicle. A first step towards a complete electronic system in a flexible label has been made. CEA-Leti's packaging team is currently developing a demonstrator, with applications ranging from sensors to radio frequency identification (RFID) dies.

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Biography

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Embedded silicon fan-out solution for 40GHz mmWave chip packaging

By Li Ma, Linyu Li, Fan Yang, Daquan Yu, Zhiyi Xiao [Huatian Technology (Kunshan) Electronics Co., Ltd.] and Tong Tian, Jia bao Niu [StorMicro Technologies Co., Ltd.]

Recently, the development of millimeter-wave (mmWave) wireless communication has been fast driven by commercial applications, such as short-range high-data rate wireless communication, passive imaging and automotive radars. The requirements for these systems are usually high performance, compact size, high level of integration, and most importantly, low manufacturing cost. Fan-out wafer-level packaging (FOWLP) has emerged as a successful technology to meet the above-mentioned requirements for mmWave applications.

FOWLP for mmWave applications

FOWLP has evolved as one of the most versatile packaging technologies in recent years and already accounts for a market value of over 1 billion USD due to its unique advantages and wide applications. FOWLP can undoubtedly meet the market demands for miniaturized package size, higher performance and integration density, lower power consumption, and lower manufacturing cost. The embedded and fan-out package can provide higher I/O numbers and eliminates the use of substrates to gain cost advantages. The technology also has good electrical performance and heterogeneous integration capabilities, which has gained significant attention in recent years [1,2]. FOWLP volumes have largely been driven by mobile and consumer applications (RF, baseband, connectivity, near-field communication [NFC], power management integrated circuits [PMIC], audio codec, microcontrollers [MCU], etc.) and are now moving to 4G communication, mmWave, automotive, MEMS/sensor and Internet of Things (IoT) applications.

Many different types of embedded and fan-out packages have been developed and reported for mmWave. Infineon Technologies first developed an embedded device technology based on a molded reconfigured wafer, known as embedded wafer-level ball grid array (eWLB), which is a classic fan-out

packaging for mmWave applications [3,4,5]. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. eWLB has the ability to attain minimum interconnection length and excellent electrical performance, but there are some limitations because of its adoption of molding materials. The STATS ChipPAC team has used eWLB technology to develop the 77GHz automotive radar, which enables superior performance and Grade 1 automotive reliability [6].

Researchers from imec developed a 77GHz automotive radar RF front-end EMWLP (embedded molding wafer-level package) module with through-silicon vias (TSVs) as the vertical interconnection [7]. The bare transceiver die and the pre-fabricated TSV chip are reconfigured to form a molded wafer through the compression molding process. The measurement results match the simulation results very well. Christopher Beck, et al., reported on a highly integrated 60GHz radar transceiver for industrial sensor applications [8].

Advantages of embedded silicon fan-out technology

Embedded silicon fan-out (eSiFO[®]) technology was developed, improved and matured by Huatian Technology. This package can be viewed as a silicon-based fan-out structure that provides more area for wiring flexibility and BGA connections, and also is similar to standard WLP.

The biggest difference between an eSiFO[®] package and a typical eWLB package in structure is that there is no epoxy molding compound in the fan-out area, which is replaced by the silicon carrier. The eSiFO[®] package also addresses the cost reduction challenge by eliminating the use of expensive wafer-level molding equipment and materials in the process flow. A production yield of over 99% has been reported in 2017 for a single-die product with one layer RDL

[9], which demonstrated the feasibility of eSiFO[®] in high-volume manufacturing.

The manufacturing process used for eSiFO[®] is a simple chip-first/face-up mature wafer-level process. Regarding its performance, eSiFO[®] has the following advantages:

- Good electrical performance. It enables short electrical paths from the die out to the package and uses high-resistance silicon because a silicon carrier can further improve electrical performance for low-loss millimeter wave transmission [10].
- Good thermal performance. Because the thermal conductivity of silicon is much higher than that of the molding compound used in the typical eWLB package, eSiFO[®] has a relatively lower thermal resistance and its temperature profile is more uniform [11].
- Multi-chip integration capability. Different dimensions of cavities for different chips can be achieved through a one-step etching process, so it is easy for eSiFO[®] technology to implement multi-chip integration.
- 3D system integration capability. eSiFO[®] is compatible with the standard TSV technology to form a 3D vertically-stacked structure [12].

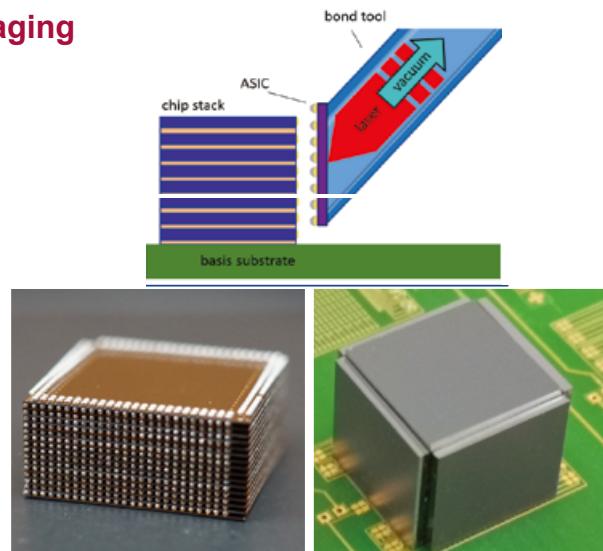
40GHz mmWave chip packaging using eSiFO[®]

An eSiFO[®] package for 40GHz mmWave applications was designed into a 5.0×5.0mm package size with a single 1.85×1.22mm embedded die. In order to improve the sensing performance and block the signal, the shielding regions were strategically made. More than 80% of the area was covered by a metal layer. A number of approaches were applied to reduce the internal stress, such as the thin shielding layer, and the stress release openings. Altogether, 86 balls of 200μm height were fabricated on the first RDL. To interconnect the chips and I/Os

New Advanced Bonding Technologies

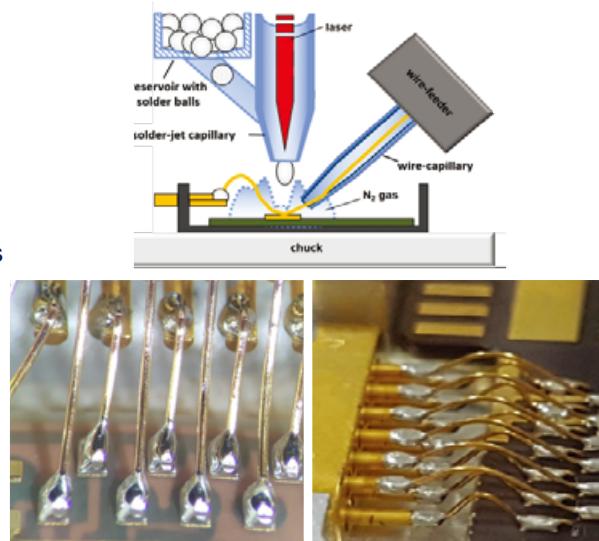
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to the periphery of the reconstructed chip, one RDL layer is designed and produced. The minimum L/S is 20 μ m/20 μ m, which requires high accuracy lithography technology.

Process flow. The manufacturing flow is shown in **Figure 1**. First, the silicon wafers containing the shielding layer and silicon cavities were formed. Second, the thinned known good dies (KGDs) from device wafers were embedded into the cavities. The narrow trenches between the chips and sidewalls of the cavities were filled through a vacuum film lamination process. Meanwhile, the pads of the embedded die were opened using a lithography process. In order to improve the performance of the device, the thickness of the dry film is increased compared to the common eSiFO®. At this point, a new wafer is reconstructed with no significant differences from the ones by a standard WLP process. The following process flow is similar with the WLP processes, such as the RDL formation and ball drop. The difficulties for the product were how to open the pads of the embedded die in the RDL process and how to ensure the continuity of the seed layer in the opening hole (30 μ m) of the thick first-passivation layer, which has a high aspect ratio (\geq 1.5:1).

In this project, a 12-inch blank wafer was used as the carrier wafer. The metal layer (Cu) is used for a shielding cap so that the signal cannot transmit to the silicon and be reduced. The 1 μ m Cu layer was deposited by physical vapor deposition (PVD) rather than the Cu plating process because the thickness is enough according to the electromagnetic simulation results. Additionally, the thick Cu may cause stress and wafer warpage. Then the cavities were formed by lithography and the wet-etch metal process. In order to decrease the stress of the large-area metal layer, the scribe lines were opened.

The cavity formation has two steps, including oxide etch and silicon etch processes. To avoid the tilt and cracking of die during the pick and place process, a smooth bottom surface without any salient point is critical for this product. After process optimization, we found that having no oxide and no photoresist (PR) residual are essential to enable a smooth bottom surface after the oxide etch process. Therefore, two effective measures should be carried out, including the oxygen plasma process after lithography and the oxide etch process with extra oxide etch cycles. The cavities were formed using the Bosch process. The specification of the cavities is 104 μ m with a TTV of \pm 7 μ m.

Because die attach has a huge influence on the pad exposure and final yield, it is a significant process needed for 40GHz mmWave chip packaging that uses eSiFO® technology. We used a dedicated die attach tool from ASM, called NUCLEUS, for the attachment; the tool has a high accuracy of \pm 5 μ m. **Figure 2** shows the image after attachment. The die shift and rotation of die attach is below 5 μ m, which meets the design requirement.

The formation of the first passivation layer is another essential step in the 40GHz mmWave chip packaging process flow. In this production, we used a vacuum lamination process with the photo-patterable dry film. The narrow trenches between the dies and sidewalls of the cavities are completely filled, as shown in **Figure 3c**. The dry film material has a big influence on the warpage and the electrical performance. After development process optimization, the pads of the embedded chip are opened completely, as shown in **Figure 3**. As a result, the pads were well connected with the RDL.

After the first passivation process is formation of the RDL. The RDL formation includes three main processes: 1) seed layer formation, 2) patterning lithography, and 3) Cu layer plating. A thick seed layer with a 0.3 μ m metal Ti layer and a 0.5 μ m metal Cu layer were deposited by PVD in order to ensure that the seed layer in the high-aspect ratio hole maintained continuity. The development of patterning lithography is

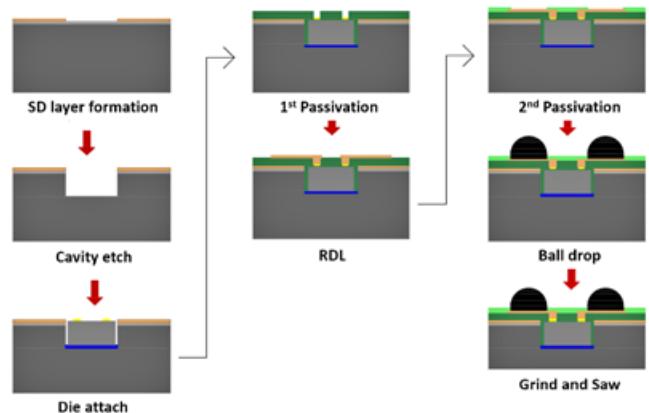


Figure 1: The process flow of 40GHz mmWave chip packaging.

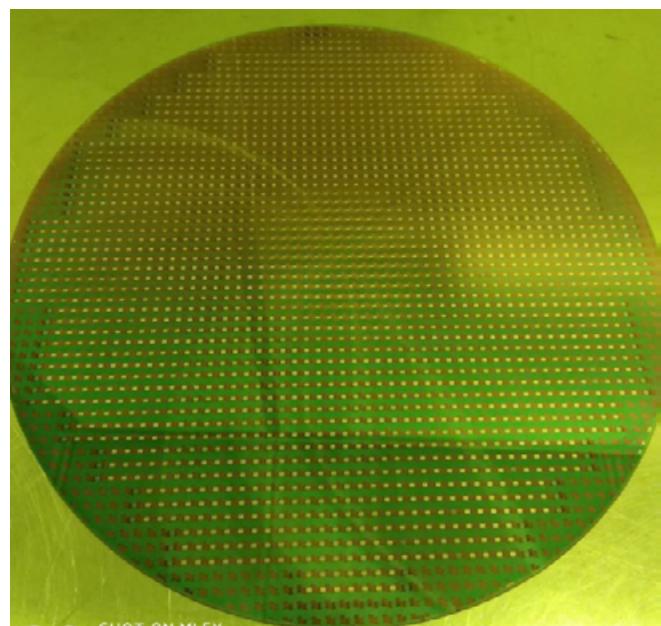


Figure 2: The whole wafer image after the die attach process.

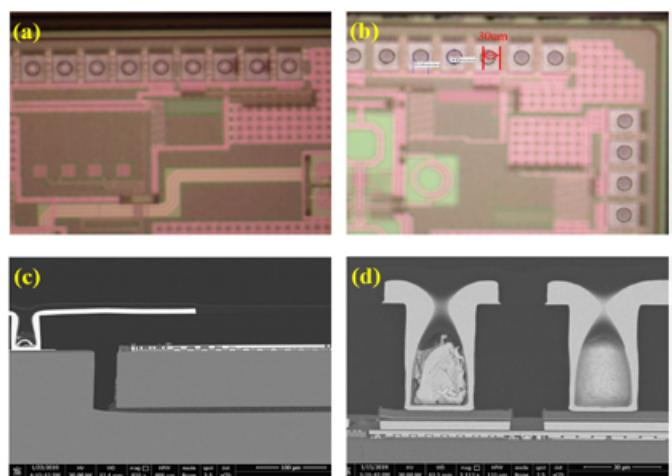


Figure 3: a) The optical microscopy image after the first passivation process; b) The optical microscopy image with CD dimension; c) the cross-sectional SEM image of the filled trench filling and the first passivation layer; and d) the SEM image of the first RDL metal connecting the pads on the embedded chip.

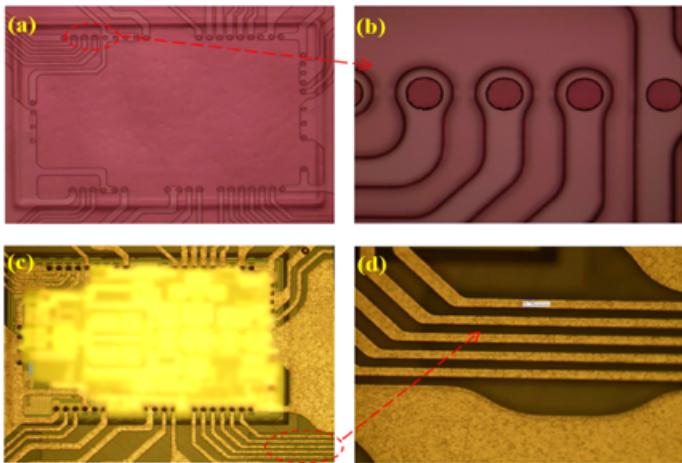


Figure 4: Images of the RDL1 fabrication process: a) the RDL patterns; b) the enlarged view of lithography patterns; c) the overview of the Cu layer; and d) the minimum line width of the Cu layer.

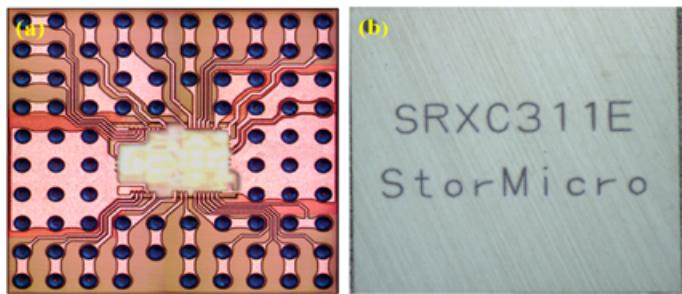


Figure 5: a) The front side of a single die; b) The back side view of a single die.

a key step in this product because the aspect ratio is close to 2:1. After lithography process optimization, a suitable photoresist is crucial for such a high-aspect ratio hole. As shown in [Figure 4a](#) and [Figure 4b](#), no photoresist residues in the opening area can be found. Finally, the plating Cu process increased the lead thickness to 10 μm to ensure a low resistance circuit. The lead minimum L/S is 20 μm /20 μm , which should be controlled within $\pm 3\mu\text{m}$.

Following the first passivation process, the second passivation is done whereby the ball drop layers, and the grind and saw processes are built-up using the standard WLP processes. The polymer passivation layers were made to be 10 μm thick by the lithography process. The ball diameter is 250 μm , while the ball height is 200 μm . The final package size is 5000 X 5000 μm , and the final package thickness is 600 μm , as shown in [Figure 5](#). After intensive optimization work, the yield of the 40G mmWave product exceeded 98%.

Measurements and results. The chip is a type of a micrometer wavelength transceiver that operates in the Ka band—its sweeping frequency is 2GHz. The receiving and transmitting performance are strongly affected by packaging. The return loss and transmit power of the chip are close to the simulated values, as shown in [Table 1](#) and [Figure 6](#).

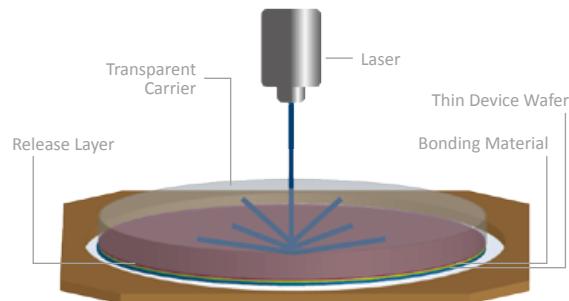
Item	simulated value	actual value
Return loss	-20dB	-15dB
Transmit power	10dBm	9.3dBm

Table 1: Comparison between simulated and actual values.

Creating Safe Environments

Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with: 308 nm 343 nm 355 nm

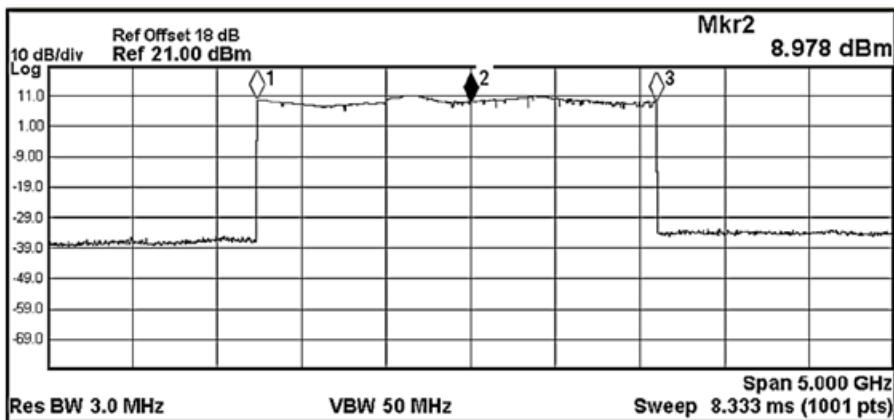


Figure 6: The test properties of the 40G mmWave product.

With respect to the sweep frequency and power consumption, the chip has obvious superiority. Its applications include intelligent traffic systems, security systems and unmanned aerial vehicles.

Summary

A mmWave (40GHz) package based on eSiFO® technology has been successfully demonstrated and discussed in this article. Among the attributes of the technology are its metal shielding layer and a thick polyimide (PI) layer on the surface of the die that provides excellent electrical performance. Compared to other wafer-level fan-out technologies, eSiFO® is a manufacturing friendly technology, because a wafer that uses it does not differ significantly from a standard silicon wafer. In combination with its elimination of the wafer-level molding process and materials, eSiFO® is also a highly cost-competitive technology. All these advantages make an attractive choice for various applications.

Acknowledgement

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Biographies

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The rising adoption of advanced substrates: IC substrate, SLP and embedded die

By Mario Ibrahim [*Yole Développement*]

In this period, with the semiconductor market facing a slowdown and competition becoming rough, substrate manufacturers are looking to differentiate themselves from each other. Moreover, the requirements of the existing markets are pushing industries that previously assumed a passive role regarding innovation, like substrate manufacturing, to become more involved.

In the last few years, the market backed the development of advanced technology to better answer the demands of the mega trends, such as automotive, 5G, artificial intelligence (AI) and others. This resulted in a profitable business as advanced packaging platforms became the perfect solution for size reduction, while increasing performance and integration. Driven by this success story, substrate makers are keen on reproducing this phenomenon within their own businesses.

Let us not overly dramatize the substrate makers' situation. They are still profitable, but are willing to be even more so while reducing their risk. Non-advanced substrate manufacturing still represents the major portion of the activities and revenue of the so-called printed circuit board (PCB) houses. The innovation in the number of stacked layers is continuing within the conventional board business. The differentiating factor in this industry, however, is coming from somewhere else, and it is from what we at Yole Développement (Yole) call "advanced substrate" activities. We focus on three major platforms and technologies within the advanced substrate category (others exist, but are not discussed here):

- Advanced integrated circuit (IC) substrate: this serves as the interconnection between an IC chip and a board (intermediate layer), including flip-chip chip-scale package (FCCSP) and flip-chip ball grid array (FCBGA) substrates;

- Substrate-like PCB (SLP): this serves as an advanced board onto which chips are mounted; and
- Embedded die (ED): this serves as a stacking technology whereby dies are embedded into a board, substrate or mold.

If we combine the revenue of the above three platforms, they will represent more than \$11B by 2024 exhibiting a CAGR₂₀₁₈₋₂₀₂₄ of more than 13%. This is much higher than the forecast 4% growth for the conventional PCB market over the same forecast period [1]. That growth illustrates the interest the players and countries have in going deeper and further into developing such advanced technologies. This also implies efforts to improve manufacturing processes. We observe a push from major players such as ZD Tech and AT&S to switch from a subtractive process to a modified semi-additive process (mSAP), or a semi-additive process (SAP). This action will enable reduced line/space (L/S) dimensions and thereby provide more flexibility on the footprint, together with more integration. With the coming of the 5G, AI, vehicle autonomy and electrification markets – without forgetting mobile – the advanced substrate platforms have interesting prospects ahead.

Business opportunities for advanced IC substrates

Starting in 2018, Huawei and ZTE have been going all-out to strengthen their capabilities for the upcoming 5G era by placing orders with supply chain partners earlier. AMD, NVIDIA and Intel are also stepping up to capture new business opportunities for high-performance computing (HPC) application chipsets. Outsourced semiconductor assembly and test suppliers (OSATS) are projecting increased demands for

FCBGA adoption in AI processors for automotive applications. At the end of 2018, the market was unable to meet the demand for FCBGA due to overwhelming demands from 5G base stations and HPC.

It seems that the FCBGA supply chain was not expecting such a strong new demand from 5G players. As a result, the average selling price (ASP) of advanced IC substrates for FCBGA applications rose, which pushed players like Kinsus and Unimicron to further boost their production capacity in order to meet the demand. AT&S, the Austrian substrate manufacturer, announced very recently the expansion of its IC substrates business for HPC by investing nearly \$1B in a new plant in Chongqing, and capacity expansion at the Leoben plant [2].

Currently, the majority of the demands are coming from Huawei's 5G activities. So, in order to reduce their risk, advanced IC substrate manufacturers are developing a broad customer portfolio to prevent relying on a single major player. Some manufacturers have had their products pass validations by Nokia and Ericsson as part of their efforts to enter 5G markets in Europe and the U.S.

The demand for FCCSP substrates, which is mainly driven by the smartphone market, is continuing to grow, even if it is slowing down on account of the sluggish outlook for smartphones. Nevertheless, a switch from wire bond into FCCSP with Cu pillar bumping is ongoing for PC/laptop dynamic random access memory (DRAM) and server double data rate (DDR) DRAM. Samsung has already migrated to this substrate type, while it is still a work in progress for SK Hynix and Micron, which are expected to start soon. In addition, some 5G RF chips and power amplifiers are also shifting to FCCSP.

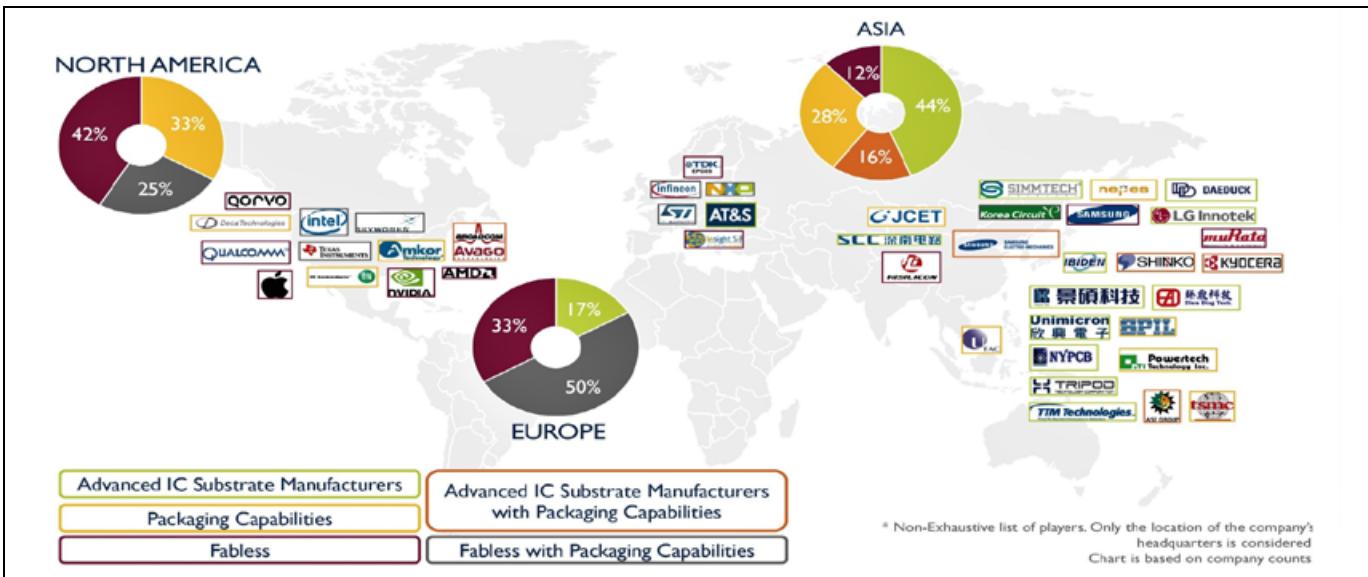


Figure 1: Supply chain of advanced IC substrate players: geographical analysis. SOURCE: [1]

From a technology point of view, the roadmap for advanced IC substrates is heading toward L/S values of around 5/5µm, higher I/O counts (>>3000) and lower ball and bump pitches. To go to even lower L/S values, fan-out technology will be required to reach L/S<2/2µm, but with a lower functionality density as compared to advanced IC substrates.

The total revenue for advanced IC substrates is almost evenly shared between FCCSP and FCBGA. When it comes to the produced volumes, FCCSP numbers are much higher than those for FCBGA. That implies that the ASP for FCBGA is much higher than for FCCSP due to bigger, more complex and higher performing substrates and packages. Generally, the FCCSP substrate and package covers applications with lower I/O counts and smaller package sizes, while FCBGA covers applications with higher I/O counts and larger package sizes.

The advanced IC substrate market is dominated by Asian countries and players (**Figure 1**). Samsung Electro-Mechanics is the leading supplier with a 12% share of the market, followed by Unimicron and Simmtech, each with 9%. The combined revenue of Taiwanese and South Korean companies accounts for more than 65% of the total advanced IC substrate market, with Japan completing the podium (based on 2017 revenue) [1].

SLP market continues its rise

This second advanced substrate platform can be considered as an

improvement of the high-end HDI PCB. The major difference between SLP and high-end high-density interconnector (HDI) PCB is the use of mSAP (and probably SAP in the future) combined with subtractive layers for SLP, instead of subtractive for HDI.

SLP technology was first introduced to the market by Apple in its iPhone X back in 2017, allowing the company to add a second battery by reducing the surface occupied by the board. Samsung used it in its Galaxy S9 in 2018. It was then still unclear if this technology was going to take off as its usage was linked to some specific smartphones and only two players, with rumors that Apple was dropping it. However, at the end of 2018, positive signals were given by players like Meiko, ZD Tech, Unimicron and Compeq with the expansion of their SLP

production capacities to meet orders from Apple, Samsung and Huawei. Huawei will, most likely, be the third player adopting this technology in its Mate 30 smartphone later in 2019. The novelty brought by Huawei is application diversification because of its willingness to also use SLP for its smartwatches and tablets (**Figure 2**). During the coming five years, more and more players will have mSAP capabilities and will step into SLP production.

Based on the discussion above, the SLP market will continue its increase showing a CAGR₂₀₁₈₋₂₀₂₄ of 17% and exceeding the \$2B revenue milestone by 2022. Until 2020, 100% of the revenue will come from the smartphone market. Starting from 2020, the revenue will arise from smartwatches and tablets, in addition to smartphones. By 2024 it is expected that

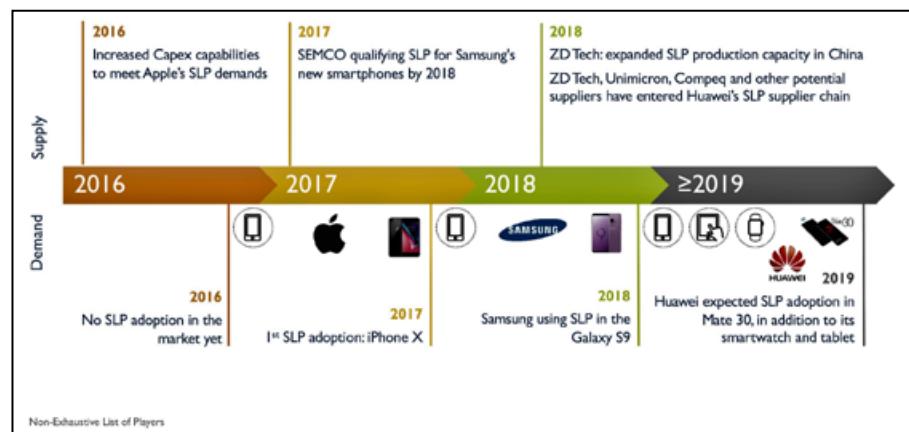


Figure 2: Substrate-like PCB (SLP) evolution achieving new milestones with progressive adoptions. SOURCE: [1]

15% of the total number of smartphones sold will have SLP, constituting 83% of the total SLP revenue [1].

As for today, SLP technology is still improving. The players are finally reaching production maturity allowing them to turn operations into profits. The mSAP technology evolution for the coming few years will focus on reducing the line/space dimensions from around $25/25\mu\text{m}$ in 2019, to $20/20\mu\text{m}$ and less. At the same time, SEMCO is working on slim and ultra-fine (with higher layer count) SLP technologies based on improvements of its HDI PCB technology by the use of mSAP and SAP processes.

Besides companies from Taiwan, South Korea and Japan, China is acquiring mSAP capabilities internally by the way of Chinese companies' investments, as well as by technology transfer from foreign companies. Vietnam is considered as an emerging country that will also benefit from the technology transfer of SLP production lines toward its lands. Despite still being labelled as a low-end substrate manufacturing country, this will change in the near future as a knowledgeable workforce is starting to emerge. Yole expects SLP to evolve into an oligopoly market with few key SLP manufacturers engaged in this business.

Embedded die: huge investments and growing interest

Historically, the first ED patent was granted to General Electric back in 1968. The first product using ED was commercialized in 2010. The technology is able to embed one or more dies, actives and passives.

The production started with technology based on a single passive embedded die. The manufacturers experimented with the easiest type of embedding and reached yields above 98% for this kind of technology. The future is more toward the use of advanced processes such as mSAP instead of subtractive in order to reach lower L/S values, thereby allowing higher integration and especially embedding complex active dies with higher I/O counts. Some players are developing substrates embedding >>30 dies, active(s) and passives.

Besides the interest in integration of die(s), ED technology is known for its good thermal management with the possibility of having a double-sided cooling system. One of its most promising applications is power

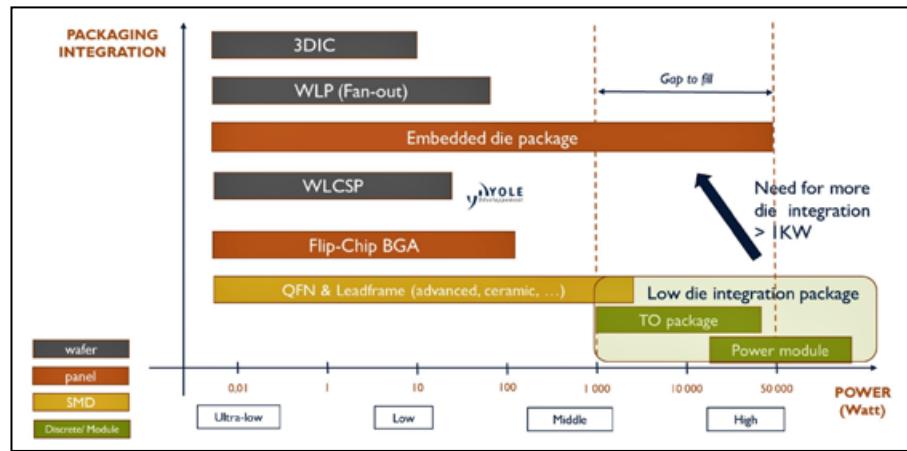


Figure 3: Opportunity(ies) for embedded die(s) technology: high-integration solution for low/mid power applications. SOURCE: [1]

modules (**Figure 3**). ED is compatible with power devices <50kW. Besides the mobile phone market, the emergence of vehicle electrification and the need for more efficient telecom infrastructure for 5G will facilitate ED in terms of finding gaps in technology needs that can be filled in these three markets. Recently, Infineon and Schweizer announced the development of a new technology used in a 48V starter generator in the mild hybrid (i.e., power-assist) cars based on Schweizer's smart P² Pack ED technology embedding a power MOSFET [3].

What is different from the previous advanced substrate platforms is that ED technology development is not exclusive to substrate manufacturers. It requires either a turnkey solution from a substrate manufacturer (ACCESS Semiconductor), OSATS (ASE), or a partnership between a substrate manufacturer, an integrated device manufacturer (IDM), and an OSAT.

Even though this technology is not yet very well known on the market, and to anticipate the forthcoming demand, huge investments are being made by players like Schweizer and ACCESS Semiconductor in new factories based in China. In 2018, the ED market was relatively small, accounting for only \$21M. The growth of this market is expected to exceed 49% CAGR₂₀₁₈₋₂₀₂₄, making it the fastest-growing advanced substrate platform compared to the other two. By 2024, the market is expected to reach \$231M, mainly driven by automotive, telecom and infrastructure markets. Mobile will still be an important source of revenue for ED, but will no longer drive its expansion.

As this technology is still in its infancy, there are still plenty of different ED technologies from various players trying to break ground. This platform will require some consolidation in the future. Which technology and which company will

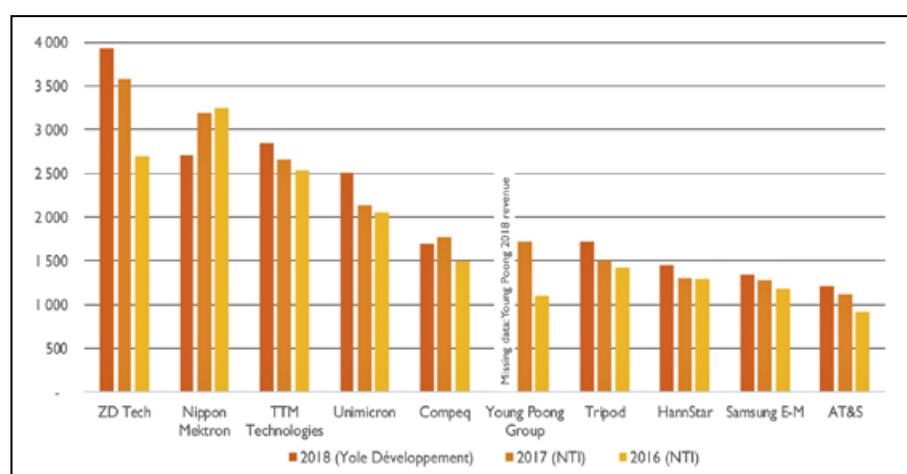
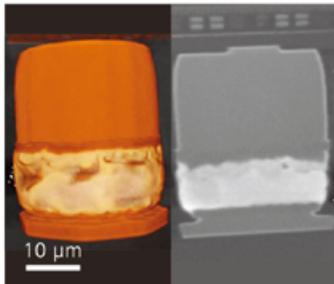


Figure 4: Top 10 substrate makers: revenue (M\$) comparison including 2018 numbers. SOURCE: [1]

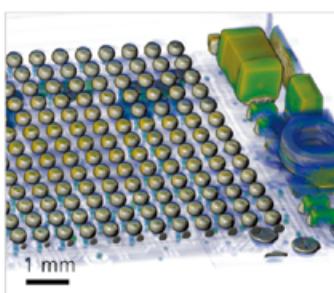
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DRAM interconnect within a 10 mm x 7 mm x 1 mm package containing 4-die stack, 0.8 $\mu\text{m}/\text{voxel}$, showing solder extrusions; imaged by Xradia 620 Versa.



3D image (left); virtual cross section (right) of 25 μm diameter Cu-pillar microbump.



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Seeing beyond

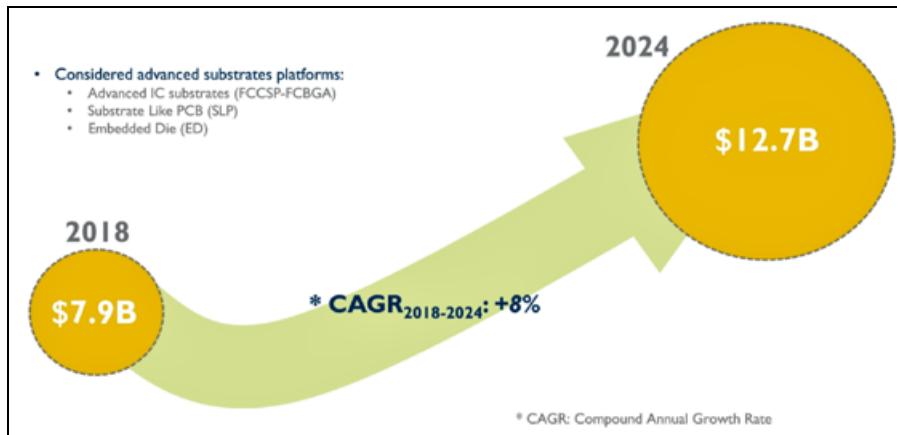


Figure 5: Global advanced substrates revenue forecast. SOURCE: [1]

have “THE” ED technology is difficult to predict and will depend on the application. R&D will progress, and more players will enter production in the coming 2-3 years.

2019: a difficult year for substrate makers?

Talking about substrate manufacturers globally, this industry is heavily dominated by Asia. It records 91% of the \$58B revenue (based on Top 116 companies’ revenue from NTI 2017). Four main countries control this business, led by Taiwan (33%), and followed by Japan (22%), China (21%) and South Korea (13%). China is regulating and consolidating its substrate manufacturing industry. This will result in small companies either shutting down, or being acquired by other Chinese companies with the potential to form large Chinese substrate manufacturing groups. It will not be a shock if in 2020 we see China clinching the runner up position from Japan. Despite this potential ranking reshuffle, Japan, Taiwan and South Korea will still be at the heart of the innovation.

If we take a closer look at the top 10 substrate manufacturers ranked by 2018 revenue (**Figure 4**), we will see that all of them have revenue >\$1B. Only two non-Asian companies (AT&S, Austria and TTM, USA) figure in this ranking and this situation remains the same even in the top 20. The leader in 2018, for the second year

in a row, is undoubtedly ZD Tech with its revenue closing in on the \$4B mark (\$486M net income) and outpacing, even more, its runner up compared to 2017. TTM will jump into the second position overtaking Nippon Mektron, which may be challenged in the future by Unimicron, the current number four. Nippon Mektron is the only company in the top 10 relying on one type of activity: the flexible and rigid-flexible PCB. The company is therefore more exposed to market fluctuation and seems to be affected by stagnation in the mobile phone market.

Ranking the companies by their revenue and net income does not show the same standing. In terms of net income, the best company is by far ZD tech, followed by TTM, Tripod and AT&S. The YoY growth of the top 10 companies fluctuates greatly from one company to another. This fluctuation is linked to the products, technologies and customer portfolio that each company has. The more diverse they are, the less risk to which they are exposed. The year 2019 will be difficult for substrate makers because of the global semiconductor market slow down, so the 2019 rankings may be affected by this decline.

Summary

Substrate manufacturing is following the trends of the advanced packaging industry, which, in turn, is driven by

megatrends. Substrate makers understood the need to innovate and are putting efforts into the development of advanced substrate platforms. The demands of the market trends and the need to differentiate are driving this movement. Advanced IC substrate, a well-established advanced substrate platform, will continue its growth primarily on account of FCCSP, but driven by extensive adoption of FCBGA in HPC/AI and 5G. SLP, with the potential adoption by Huawei and application diversification, will gain more traction. ED, despite its infancy, seems to be boosted by the lack of alternative solutions for power devices requiring better thermal management and more integration.

Who will be the first big player to massively adopt this technology and where? How will the substrate manufacturers perform during the difficult year of 2019? Will their standing be affected? Will advanced substrates reach the same level of fame as the advanced packaging platforms? Will they overtake them? Plenty of relevant questions will be answered in the coming 2-5 years. Yole is deeply involved in the domain and will pursue investigating the answers to these questions as it follows the rising adoption of advanced substrate technologies.

Acknowledgement

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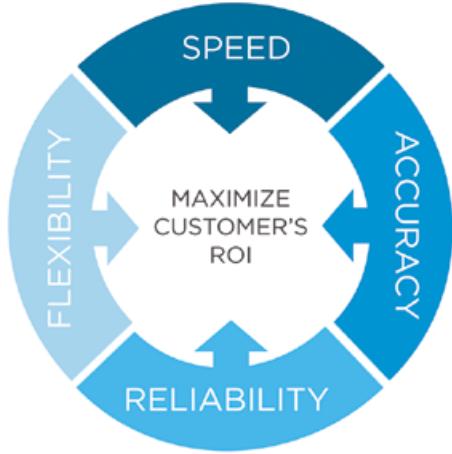
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Biography

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YOUR STANDARD IN PRECISION AUTOMATION

Inkjet printing: gaining competitive advantage

By Luca Gautero, Simon Donkers, Wouter Brok [Meyer Burger]

The semiconductor industry is giving attention to inkjet printing to gain benefits from its features. Inkjet business presents a less capex intensive alternative for patterning when compared to, for example, a lithographic step. Moreover, on the operational expenses side, materials are efficiently used. Especially, back-end-of-line (BEOL) and integrated circuit (IC) packaging profit from the digital patterning of encapsulations (permanent or temporary), or by using interconnects with appropriate types of materials (see the sidebar, "Background," for additional discussion).

Inkjet printing offers a contactless, direct application of functional materials to substrates with topology. The height of features can span up to hundreds of micrometers. This additive process allows the creation of precisely controlled patterns on a scale in the tens of micrometers. Equipment manufacturers are either specializing in servicing a single application with inkjet printing technology (e.g., ceramic tiles industry), or providing a versatile and adaptable platform targeting many different applications.

The versatile and adaptable platform approach combines modules, carefully selected or designed, to enhance the desired inkjet capabilities. Thanks to this matching effort, the technology reaches a broad application range. Consequently, inkjet tools are commonly not standardized for specific application requirements. This situation is especially relevant for the semiconductor industry, where inkjet equipment manufacturers and early adopters are transferring existing manufacturing processes to this additive technology. The key elements to create a success story with inkjet printing are the application, its corresponding functional ink, and the printer.

Equipment characteristics

Inkjet positions itself as a digital technology for lines/spaces (L/S) in the 50/50 μm region. This range is of interest for packaging technology like flip chip, which holds most of

the manufacturing worldwide [1,2]. To achieve such a result with three sigma confidence, all the error components need to be in control. A skillful identification of these components is crucial in a design for quality. A coarse division of the error components identifies them as printhead, ink and motion. Printhead and ink related errors are normally evaluated together as drop placement error. This can be managed by selecting a suitable printhead and a jetting ink formulation. These choices, however, are limited by process needs related to the application. The drop placement error alone can contribute up to 20 μm (3sigma). Motion is then divided in accuracy and precision. These latter numbers are normally given by the equipment manufacturer, which are driven by equipment design.

For multi-layer prints it is important to accurately position each print pass relative to already existing structures. The approach of the graphical market is to control the error budget by printing registration marks in the sideline of pages and between prints. Visible offsets between color channels are then corrected as they appear on the printed result. This implies that the first products in each batch are scrapped for alignment, and that an area within each print needs to be reserved for registration marks.

In stark contrast, a first-time-right design is chosen for functional applications. An

accurate and precise motion system is combined with a camera-based alignment system. This system ensures repeatable performance already at the first print. High-resolution encoders are used in the motion axis to ensure high repeatability. Encoders are only one part of the solution; the other part, an accurate machine base, ensures the straightness and perpendicularity of the axis. As part of the calibration, a proper mapping, which highlights differences between the motion encoders and absolute print locations, is made. These inspections, reoccurring at every tool produced, ensure and allow for continuous control and improvement.

A tool is typically designed around the incoming substrates. The graphical market has optimized for sheet-to-sheet or roll-to-roll (R2R) printing. Therefore, according to constraints introduced by these two types of substrate, graphical printers are optimized for low cost of ownership and fast throughput. For the functional printing market, each type of substrate and ink brings its own particular design constraints. The optimal way to deal with these constraints is to adapt the machine to them. Equipment modularity is therefore a key design specification. **Figure 1** shows three examples of machine design concepts, to illustrate various possibilities.

For the semiconductor industry, two distinct machine designs are developed. The

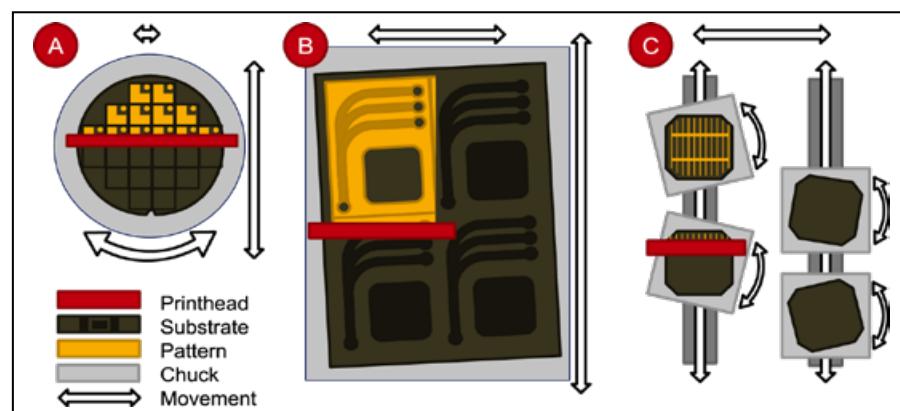
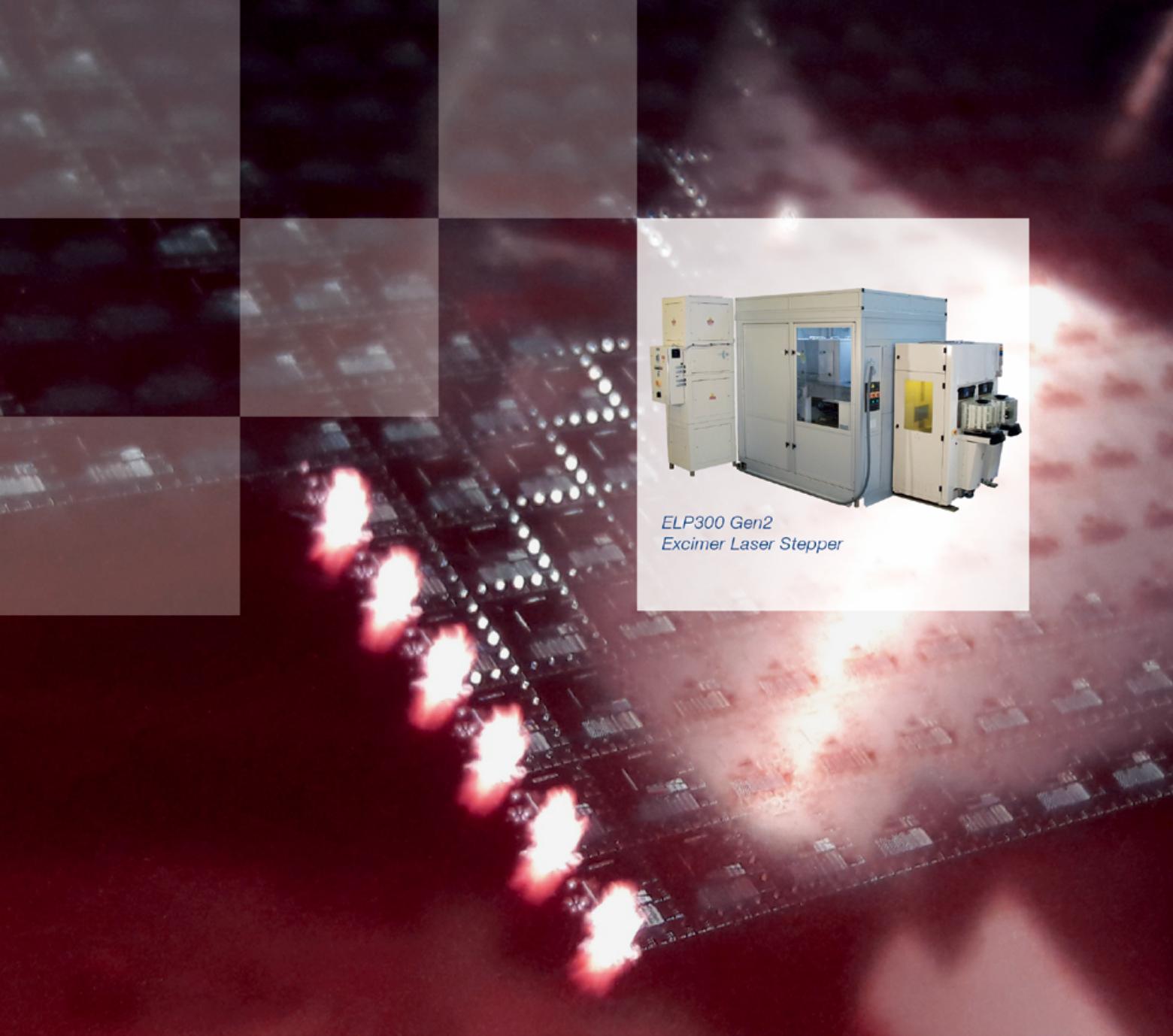


Figure 1: Overview of different printer designs: a) Silicon wafer design, having a round rotatable chuck offers maximum flexibility and process control; b) A large substrate design: rather than mechanically aligning substrates, the print image is digitally rotated; c) A dual-lane, dual-chuck design. While the left lane is printing, the right lane is exchanging substrates and aligning.



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wafers. This laser processing system is a technology enabler for wafer-level packaging, including direct material patterning of non photo-definable resist, removing seed layers for redistribution layers (RDLs) and UBMAs, as well as laser debonding for thin wafer handling.

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first relates to the silicon wafer shape: e.g., the machine presents a single round substrate carrier (**Figure 1a**). As mentioned above, camera(s) and the motion platform ensure an accurate print position. Throughput can be increased with multiple printheads, reaching up to the width of the substrate. By design, the assembly allows for easy maintenance of each printhead and the calibration of its position, to enable control of the error budget.

The second semiconductor-inspired design, which relates to lead frames and panels, presents a chuck and a moving printhead assembly (**Figures 1b** and **1c**).

Figure 1b, which shows how the chuck design follows the substrate specifications, holds a single substrate or carrier of substrates. This configuration is preferable for high-mix/low-volumes (HMLV). Compensation for inaccuracies on account of small board deformations due to previous processing can be accomplished for each substrate. The optical inspection system quantifies deformations and dynamically modifies the print image to match the unique shape; such an approach boosts yield (**Figure 2**). **Figure 1b** is an ideal implementation for printing a solder mask onto large PCBs where the deformations are common.

Now consider instead a low-mix/high-volume (LMHV) situation, in which incoming substrates are less prone to deformation and the speed given by the parallel performance of design C (see **Figure 1c**) provides high throughput. In **Figure 1**, the motion system offers correctly aligned substrates to the printing system. During this printing action, the alignment of the upcoming substrates is performed. **Figure 1c** is an ideal production machine, for example, in the photovoltaics market. There, throughputs higher than one thousand substrates per hour are essential. Although speed is key in this design, fragile substrates need to be handled delicately. These contradicting design constraints are fully satisfied by the two print lanes with multiple substrates each.

Synergies emerge by deliberately designing a printer around the requirements for the process. As a pragmatic example, inspection per substrate is designed into the machine to detect any print defects. These print defects can then trigger either maintenance, manual or automatic, or, when redundancy is designed into the system, an automatic change of printing strategy. If these actions are taken, later prints will therefore not be affected. Another design leverages

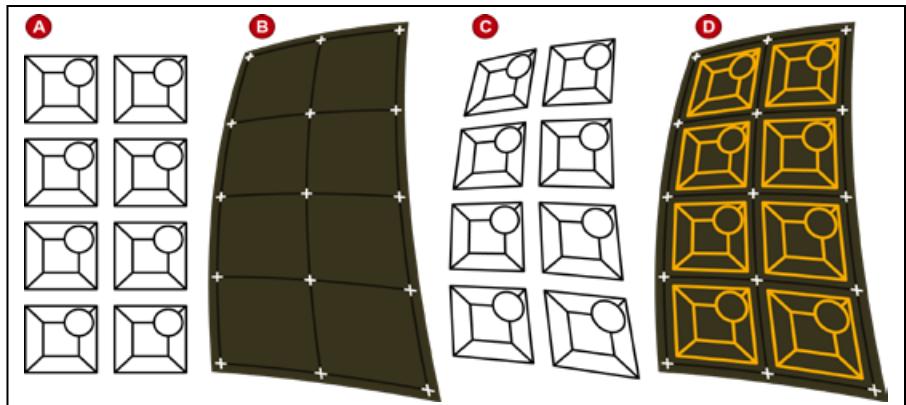


Figure 2: Overview of substrate compensation: a) A theoretical print image, b) Schematic deformation of a substrate with fiducials; c) Modified print image; and d) Final print result.

the wait time of the substrate exchange to inspect the printhead performance. These two designs provide control on quality before and after each print. This assures that no print defects will be created.

Controls on printhead variation

Within the graphical market, printheads and inks are developed simultaneously over the years to assure an optimal print quality. For functional applications, obtaining an optimal end result is a shared responsibility among three players: material suppliers, equipment manufacturers, and device makers. Inks are tailor-made by material suppliers upon desired functional and jetting process requirements. Equipment is designed to accommodate substrates and offer large process windows for ink jetting. The device maker is the process owner, therefore central in the specification of both inks and equipment. The focal point of attention of these three players is the physical printhead. A printhead is integrated into the equipment and will drive the dispatch of material according to the manufacturing requirements.

Current state of the art printheads offer extensive control over the nozzle

actuation waveform. This greater freedom comes with a larger process window to investigate for good printhead settings. Optimal performances of printing, which means a decrease in the drop placement error, are obtained by matching and optimizing ink to printing parameters such as pressure, temperature, and nozzle actuation waveform. When experiments and quality controls of the droplets, as they exit nozzles, are performed by a camera system with dedicated image recognition software (called a “drop watch”), the influence of any parameter become appreciable in a quantified, reproducible manner.

Figure 3 shows two examples of recorded droplet formation. Both of these examples show a collection of images recorded at a fixed time after jetting, while a single parameter of the nozzle actuation waveform has been varied. **Figure 3a** shows the harmonic behavior of the liquid in the nozzle chamber. This shows that with a fixed incoming voltage, a big difference in drop speed is a consequence of the pulse duration. Once the pulse duration is fixed, the pulse voltage offers fine control over the exact shape and speed

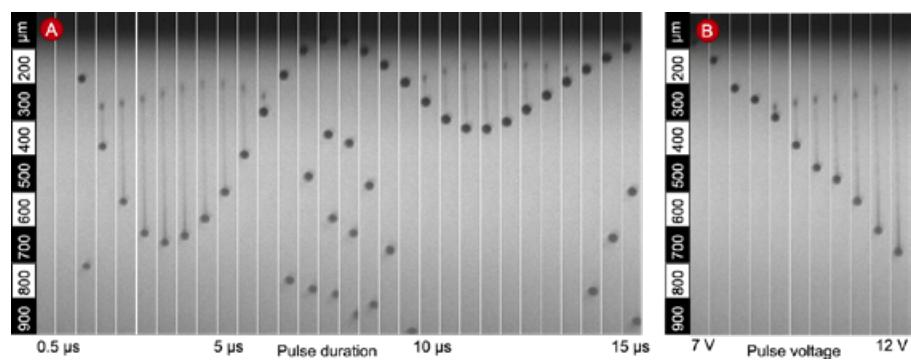


Figure 3: Advanced drop analysis overview of the influence of pulse duration and voltage on the jetting formation. The vertical scale represents the distance from the nozzle plate.

of the droplet (**Figure 3b**). Aside from these two examples, a drop watch also allows the quantification of the process boundaries. They explore compatible jetting frequencies, investigate jetting uniformity, and inquire the time reliability of drop formation. With this information, the design of the machine, together with the process window, is made robust.

Drop watchers detect and quantify variation of the printhead. Variation of speed and angle among nozzles of a printhead, even within specification, can result in erratic performances. This knowledge helps to drive print strategies. These new inkjet strategies are achieved with comprehensive simulators (**Figures 4a** and **4b**). These tools allow users to zoom into their print strategy down to the single drop level. When and which nozzle printed a drop is clearly displayed. With this detailed information, various strategies can quickly be sketched, reviewed and printed to find their effect.

The stepping of the printhead is a parameter in print strategies. In a multi-pass print, where the desired resolution (dot per inch, or DPI) is higher than the native printhead resolution (nozzle per inch, or NPI) and the stepping is one, the printhead passes over the substrate once, moves one pixel, and repeats

(**Figure 4c**). Instead, a better approach is given by higher stepping numbers: the printhead shifts a few millimeters during passes, and an entirely different set of nozzles prints next to each droplet, thereby mitigating the printhead variations without throughput impact (**Figure 4d**).

Another print strategy could send the printhead over the same area multiple times to dispatch ink. In other words, multiple nozzles would be involved in printing that area (**Figure 4e**). The benefit is additional redundancy. Furthermore, the additional drying time offers more control over the layer formation. This strategy, in combination with the variable stepping, creates a much more diffuse drop placement pattern (**Figure 4f**).

Digital revolution in action

One of the advantages of inkjet printing is its digital nature, which makes each product unique, even in LMHV situations. Compensation for substrate rotation (**Figure 1b**) has already been presented. When multiple fiducials are available, digital correction can go much further as shown in **Figure 2**. This maintains a tight drop placement relative to the substrates, even if the substrate has significant deformations.

Another benefit of inkjet printing is the high repeatability of material volume control. Inkjet printing repeatedly prints the same volume of active material on each substrate or specific location thanks to its digital nature. Active printed layers are accurately calibrated with the exact quantity of material needed. It is therefore a wise choice to create the active material on sensors, or to reach an extremely precise thickness for optical applications, with an inkjet tool.

Productivity enhancements

Material suppliers are continuously developing their inks to improve the performance and reliability. Also, printheads have ever more advanced designs, and are better equipped with features for higher stability. Still, drop watch features, as described earlier, are used in production environments. They quickly scan all nozzles' drops for basic properties, such as speed and angle, which results in a performance map of the entire printhead. This can easily be used as an automated trigger to run preventive maintenance and prevent the occurrence of print defects.

Several printheads are available with ink recirculation possibilities. When ink is

circulating, better temperature control and continuous ink change are achieved even when the printer is idle. Furthermore, any build-up of agglomerates or air bubbles is immediately removed to prevent nozzle clogging [3].

A well-known phrasal idiom for printheads is: “a working nozzle is a happy nozzle.” Production printers have an automated jetting sequence (jetting guard) to act during long inactive intervals. Ink flows, in the range of microliter/day, are enough to ensure that the printer functions reliably. With this guard set, the system is always ready to run production.

Drop behavior on a substrate's surface

Functional inkjet printing is typically applied on impermeable substrates. Any printed volume will therefore be found on the substrate surface. Printing parameters will affect the way the drop is landing. After landing, the material will flow. The final extension of the solidified material on the surface depends on the curing process, solvent evaporation or simple solidification due to temperature decrease [4]. These effects are intertwined with timing of drop placement, which is controlled by print strategy and machine design.

Referring to the above discussion, a particular example considers inks with low viscosity at room temperature and low surface energy. These deliver planar features, but conflict with precise pattern formation (**Figure 5b**). Advanced printing optimization

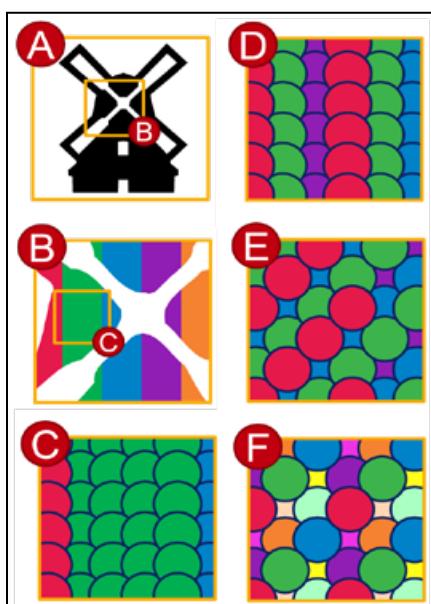


Figure 4: Print strategy variations for a printing task that requires four passes. Droplets are colored by the nozzle firing them. a) Print image; b) Simulator overview of a detail of 4a; c) A zoom-in view of 4b showing each individual droplet. Drops highlighted per nozzle with different colors; d) Alternative stepping print strategy compared to 4c; e) Alternative multi-pass print strategy compared to 4c; f) Combining 4d and 4e.

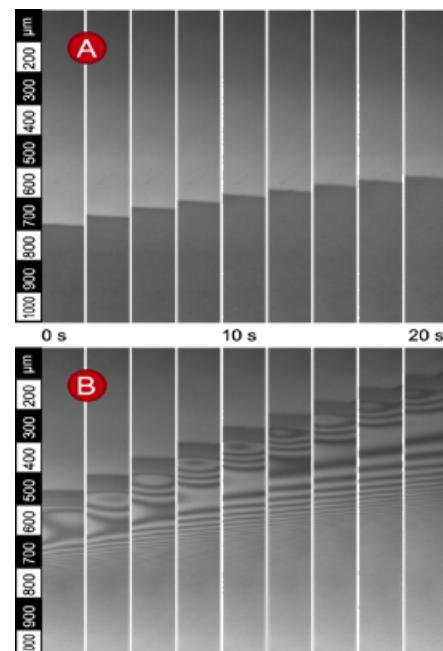


Figure 5: Overview of lateral edge movement for two levels of ink viscosity (5a and 5b) in time without applying any active solidification method.

routines coupled with off-line characterization will identify the conditions for acceptable solidification methods. Solidification methods are indeed a balanced combination of ink design, environmental control (temperature, humidity, etc.) and active curing (UV, IR, etc.).

Summary

Functional inkjet printing can reliably support applications with high accuracy and excellent process controls for the semiconductor industry. Suitable equipment and ink materials are commercially available and they are defining additive manufacturing innovation. Equipment manufacturers, material and printhead suppliers, as well as application owners, work together to leverage the unique benefits of inkjet printing. It is essential to apply the tools, strategies and methods detailed here to minimize the time to market.

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Background

The suitability of inkjet printing for the semiconductor manufacturing [S1] is best described by typical examples: dielectric inks offer passivation, isolation and protections; common applications are encapsulation, stress buffer on silicon dies, buffer rings, wafer edge protection and containment structures with high aspect ratio, like dams or fillings. Hot melts offer temporary masking for etching or plating of conductors. On lead frame substrates, isolation patterns for routed quad flat no leads (QFN) packages, solder mask, and roughening are typical examples of inkjet patterning. Conductive inks produce interconnects, antennas and passive components. Adhesive formulations enable wafer bonding and die attach. Print results are shown in **Figure S1** for: solder flux (**Figures S1a** and **S1b**), BGA solder ball encapsulation (**Figure S1c**), solder mask on routed QFN (**Figure S1d**), 3D-printed dams (100 µm walls, 500 µm height) (**Figure S1e**), and printed adhesive patterns (**Figure S1f**) illustrate the capabilities of inkjet technology.

Sidebar reference

- S1. “Inkjet-based additive manufacturing addresses challenges in semiconductor packaging,” *Chip Scale Review*, Vol. 21, No. 2, http://www.chipscalereview.com/issue/1704/ChipScale_Mar_Apr_2017.pdf

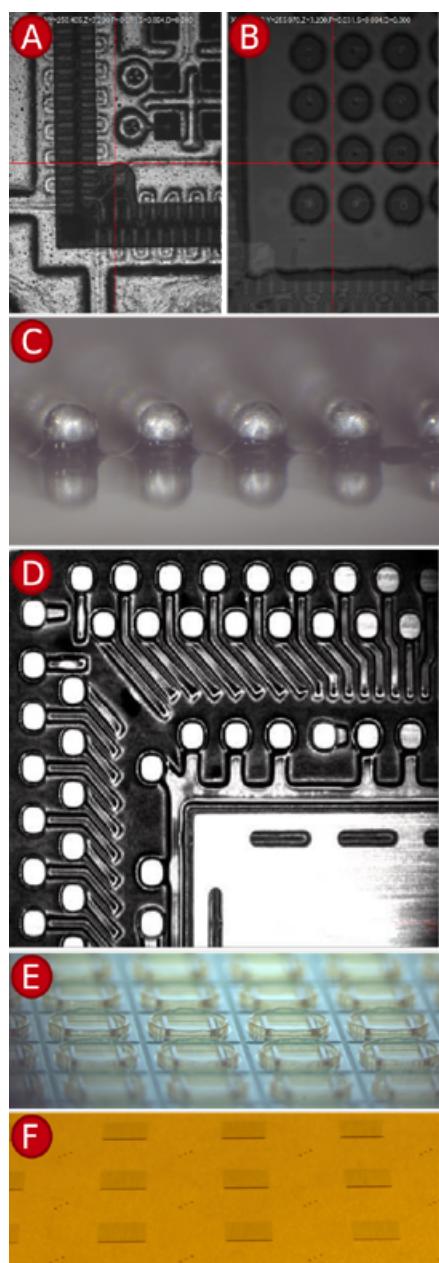


Figure S1: Typical print results for several applications.



Biographies

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Innovation in inspection and metrology for new manufacturing technologies

By Scott Jewler [SVXR, Inc.]

In 1984, KLA introduced the 2020 Wafer Inspector. With this innovation, the wafer fabrication industry began the transition from the manual optical inspection of the time to today's artificial intelligence-powered fab-wide process control with feedback and feedforward loops. Automatic inspection and metrology have since become cornerstones of wafer manufacturing with as many as three out of ten process steps dedicated to inline monitoring.

In semiconductor packaging, automated optical inspection has been widely deployed. However, because critical interconnect features are frequently optically obstructed, this technique is unable to provide feedback on the performance of core processes such as flip-chip bonding. As interconnect density continues to increase, and as increasingly complex and multi-layered assembly technologies are widely adopted, and as market tolerance of process escapes and field failures diminishes, it has become clear that transmissive inspection and metrology of semiconductor assembly processes is needed to increase yields, lower costs, and eliminate escapes.

Acoustic microscopy, micro-focus X-ray, magnetic resonance, and infrared (IR) technologies are all finding their ways into packaging factories. While each technology serves a useful purpose, none offer the combination of speed, sensitivity, and resolution needed for inline continuous process monitoring.

A newly developed high-resolution automatic X-ray inspection (HR-AXI) technology overcomes these limitations. Combined with advanced artificial intelligence algorithms, 100% inline inspection and metrology of critical optically obstructed features can now be accomplished.

Why use HR-AXI for advanced packaging?

Interconnect density in advanced packaging is increasing at a rapid pace. 2.5D packages with hundreds of thousands of solder joints are shipping in volume. Complex system-in-package (SiP) modules now include integrated shielding, multiple active components, finely spaced passive components, and double-sided surface mount technology.

At the same time the interconnect density has been increasing, the market has grown much more unforgiving of quality escapes and field failures. Social media brings unrelenting attention to new technology and blockbuster product releases and rapidly amplifies reports of any issues in performance or reliability. A small quantity of field failures can redistribute billions of dollars of market share.

Meanwhile, electronic devices take on more and more responsibility for human safety. Assisted and autonomous driving depend on device reliability. While redundancy can reduce the risk of functional failure, the cost of recalls and repairs only increases with additional devices.

How does HR-AXI add value?

Ultimately, value determines if an inspection or metrology step will be added to the manufacturing process flow or not. How does HR-AXI add value? HR-AXI increases process tool utilization. Typically, a sample is prepared after a maintenance event or shift change and moved to the lab for analysis. Depending on the process and event, the process tool may idle while the quality of the set-up sample is confirmed. This confirmation may be done by conventional X-ray or cross sectioning, but either way, the production capacity of the idled tool is lost while waiting for the quality check to be performed. HR-AXI eliminates the need for offline process set up checks by

monitoring product quality immediately and continuously on the production floor.

HR-AXI also improves cycle time. Manufacturing cycle time drives agility and efficiency in manufacturing. Shorter cycle times mean less inventory carrying cost, better responsiveness to demand signal changes, and improved absorption of overhead. By continuously monitoring product quality at key process steps, lots move more quickly through the manufacturing line. Cycle time can be optimized and savings captured.

Furthermore, HR-AXI improves product quality and reliability. Statistical process control (SPC) is effective at minimizing variation due to common causes of variation. Unfortunately, not all causes of variation are common. Special or assignable causes also exist and these are not typically exposed by conventional SPC techniques. As advanced packaging process requirements get more restrictive, it is also common to find cases where process capability is marginal to, or incapable of meeting, the design specification. A marginal process may be in control, but still produce an unacceptable number of defective products.

Flip-chip contact non wets (CNW) (**Figure 1**) are a particular concern. Frequently occurring randomly, these defects are very difficult to detect with conventional techniques. Because they often have assignable causes, SPC is

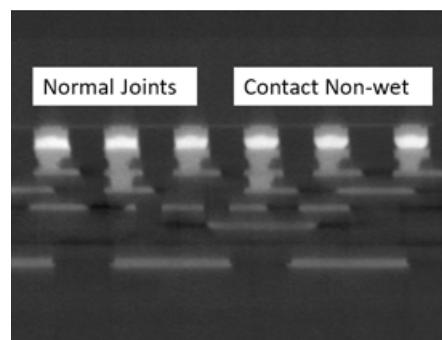
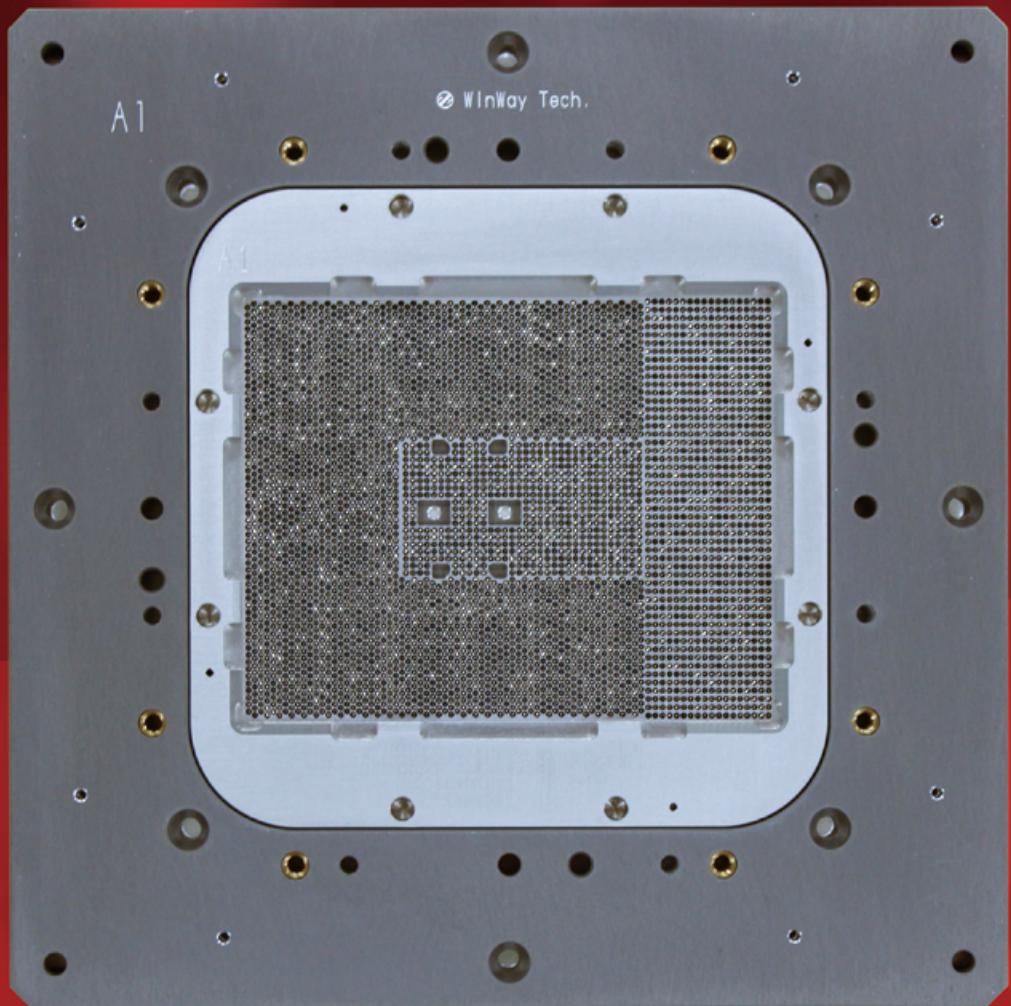


Figure 1: Normal joint vs. contact non wet.



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not an effective control strategy. CNWs are particularly problematic as they are typically undetected by electrical test. Affected units can make it into end products where they become infant mortality failures.

Elements of an effective HR-AXI system

There are three critical elements of an HR-AXI system. The first is the measurement instrument. Transmissive X-ray systems typically consist of an X-ray source, a sample manipulator, and an X-ray detector. To achieve high-resolution and high-speed measurements, a new type of X-ray instrument was developed.

Traditional high-resolution X-ray inspection systems typically utilize a point projection source. To achieve resolution of say $1\mu\text{m}$, the maximum spot size of the source must also be maintained at $1\mu\text{m}$ or below. This limits the power that the source can produce. Also, $1\mu\text{m}$ spot size sources are typically limited to about 10W. To achieve high resolution, the sample under test is typically moved into close proximity of the source. The detector can be up to a meter away.

In HR-AXI, the structure and function of the X-ray instrument is modified. A high powered 1000W source is used to dramatically reduce the imaging time. A new, high-resolution detector is introduced. The combination of a high-power source and high-resolution detector enables inspection and metrology of advanced packaging interconnect at the throughput needed to enable inline 100% monitoring.

While this new HR-AXI configuration offers much higher throughput than conventional point projection high-resolution X-ray systems, the introduction of higher flux and a low noise detection system also significantly increases the dynamic range and signal-to-noise (SNR) ratio of acquired images.

The human eye can differentiate between millions of color hues, but only 50 or so shades of gray. Traditional high-resolution point projection X-ray systems were designed for human interpretation so dynamic range or gray scale has not been an area of focus. When moving to automatic computer detection, this additional dynamic range provides a significant advantage over lower dynamic range point projection X-ray systems.

While beam hardening makes the relationship somewhat nonlinear, generally the more material thickness through which an X-ray beam transmits, the more of it is absorbed. A high dynamic range detector is sensitive to small changes in absorption resulting from differences in material thickness. Advanced computer vision analytics supplemented with machine learning and artificial intelligence (AI) can use these very localized absorption measurements to find defect signatures in massive data sets. To enable HR-AXI, a high-speed and high-resolution X-ray instrument with wide dynamic range is foundational.

While it may seem intuitive that using an X-ray source with 100 times more power would cause an increase in damage to sensitive ICs due to affects of ionizing radiation, the opposite is true. The dose seen by the device is a function of source power, exposure time, the square of the distance from the source to the sample, and the area of exposure. The higher source power is more than offset by the shorter exposures time and greater distance between the source and sample resulting in a 75% or greater decrease in the dose seen by the device. Sensitive dynamic random access memory (DRAM) devices can be imaged using HR-AXI without the detrimental effects seen from conventional point projection X-ray systems. **Table 1** shows details of dose calculations.

Dose	α	(Dose Rate or Power) \times Exposure time	Distance 2 \times Exposed Area
Power	1000W	10W	100X
Distance from Source	3.5X	X	12X reduction in dose
Exposure time	Y	30Y	30X reduction in dose
Dose	Z	\sim 4Z	X200 dose is about $\frac{1}{4}$ of typical FA Xray dose

Table 1: X-ray dose calculation.

Data analytics

Inline 100% inspection and metrology require rapid scanning of production parts and the simultaneous judgement of whether or not parts meet the relevant specifications. The development of automatic inspection and metrology algorithms requires a number of complex operations.

In the X200 deployment, a 30 mega-pixel sensor is utilized to image a 12X18mm field of view in a step-and-repeat scanning pattern. Each image can include tens of thousands of solder joints. The images must be digitally aligned to a pattern and the individual solder joints uniquely identified. Because subsequent analysis is on a per solder joint level, a database of solder joints is created and augmented through the analysis process.

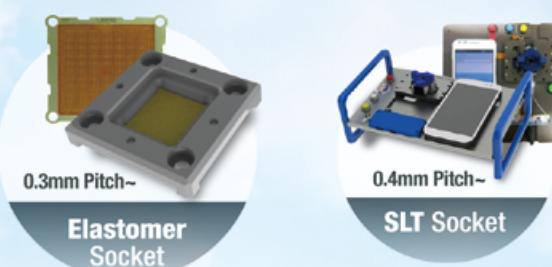
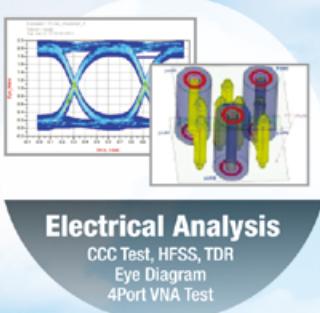
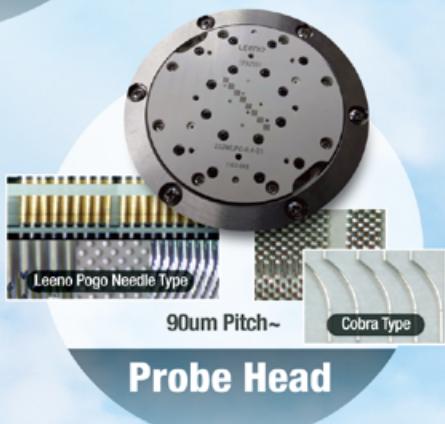
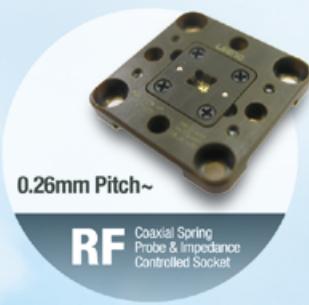
For inspection, individual solder joints are compared to a model of a normal solder joint and variation in the test solder joint from this normal structure is characterized. Various techniques utilizing computer vision and machine learning are used to generate reference models and to determine how a test joint differs from the model. Solder joints that differ sufficiently from the normal model are further classified by comparing these to know defect types and their attributes. In this way, subtle differences such as those between a normal contact and a contact non wet can be identified at high speed under continuous inspection operations.

One of the biggest challenges in advanced packaging HR-AXI is the treatment of noise in the signal. IC packages are complex structures. In transmissive X-ray imaging, any element of the package that absorbs X-rays will produce a pattern on the image. So, while high atomic number materials such as tin and silver absorb more X-rays than lower atomic number copper, substrate copper features such as vias, traces, and via pads also appear in X-ray images and can be considered noise for the desired analysis. Because these copper features are typically fabricated to a looser tolerance than die features, such as solder bumps, these copper features can move around relative to the solder joint features of interest making their treatment in analysis problematic.

Analysis techniques must interpret variation in solder joint features without being confused by potentially overlapping copper features. Parametric tuning of algorithm attributes is used to optimize defect detection while minimizing the occurrence of any false positives related to background noise.

In **Figure 2a**, a 2D representation of a solder joint model is shown. While the actual features space models have many more variables, the model shown

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is illustrative of how a solder joint can be characterized in feature space. In **Figure 2b**, representative test unit solder joints are plotted over the training

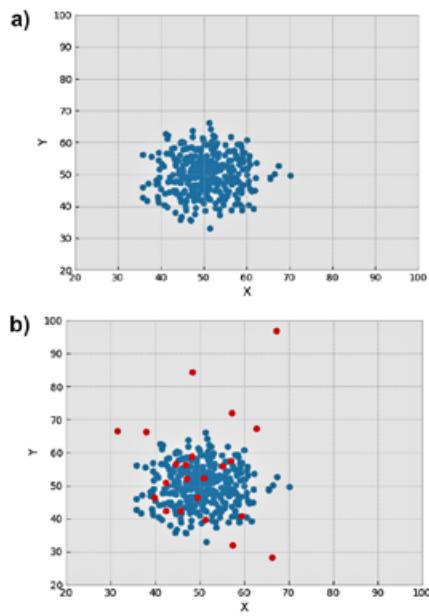


Figure 2: a) 2D representation of the training model;
b) Test unit features compared to the training model.

model. In these images, the difference between inlier or normal solder joints, and outlier or abnormal solder joints, can be seen. Using similar features, the outliers can be further grouped or classified using defect labels and models as shown in **Figure 3**.

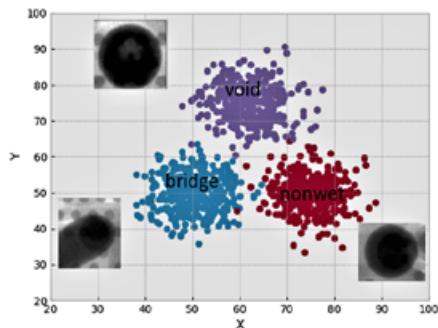


Figure 3: Training model with overlay of test results.

Data visualization and communication

When working with large data sets such as those collected during HR-AXI inspection, the ability to communicate information in a way that can be quickly and accurately interpreted by human operators and engineers is critical. Defectivity levels can be superimposed onto a visualization of the customers' manufacturing strip or wafer substrate. Patch images of individual defects can be accessed directly from the results database where these are augmented by color enhancements that highlight the variation between the modeled joint as identified by the algorithm.

Because solder joint inspection data is tracked on a per joint basis for each unit, strip, wafer, and lot processed through the tool, a rich data set is available for further integration into a fab-wide manufacturing control system. In the future, this data can be seamlessly integrated with additional inspection and metrology steps (for example bumped wafers, bare substrates, and additional bonding steps) to enable manufacturers to precisely map variation and its impact on product quality throughout the line.

Figure 4 shows a strip map with the number of defective solder joints labeled for each individual unit. **Figure 4** shows a wafer map with voids exceeding a specific area ratio marked with the color representing the relative void size.

For visualizing a specific failed solder joint, **Figure 4** shows an example from the integrated review tool. Unit, lot, and

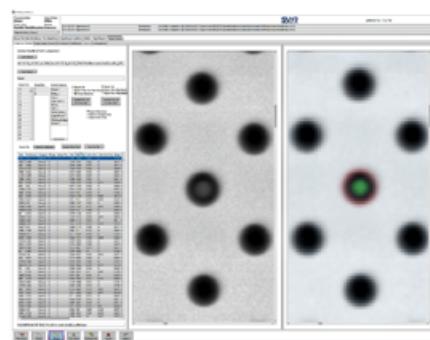


Figure 4: Inline review tool.

run information is shown in the top left corner of the screen and can be sorted by the user to drill down to a specific defect. A patch image of the defect under review is displayed together with a colorized version to assist the user in understanding why the algorithm classified the defect in the way that it did. The defect shown in the image is a void. The colorized image highlights in green the area of the solder joint where there was less absorption of x-rays than anticipated by the model highlights in red where solder exists and absorption was higher than anticipated by the model. While the void itself is detectable in the patch image, it's not obvious without the colorized image that the solder joint with the void is actually larger in size than the model as well, probably due to conservation of mass.

Other defect types such as CNWs, also form distinct patterns in how they vary from nominal models. While this type of defect is often difficult to discern in the patch images, the colorized comparison to the model allows users to understand the specific variations that the algorithms have identified and used for classification.

Summary

Assembly of advanced package structures is becoming increasingly difficult with more and more tightly spaced interconnects. At the same time, the market's tolerance for non-conforming semiconductor products is rapidly diminishing.

Traditional statistical process control (SPC) techniques are proving insufficient at detecting variation with assignable causes. Holding production while samples move to a lab for analysis forces lost productivity and longer cycle times.

The time has come for manufacturers of advanced IC packages to adopt fully-automated inline transmissive inspection and metrology solutions. Doing so not only improves outgoing product quality, it drives down costs by increasing proactive attention to process changes, reducing time to discovery of misprocessed devices, and eliminating lost productivity and cycle time waiting for slow offline set-up checks.

Biography

Scott Jewler is Co-founder and COO at SVXR, Inc., San Jose, CA. He is a veteran of the semiconductor packaging industry having previously held management positions at Amkor Technology, STATS ChipPAC, and Powertech Technology. Scott has seven granted patents and numerous prior publications. Email scottjewler@svxr.com



Overview and outlook for heterogeneous integrations

By John H. Lau [Unimicron Technology Corporation]

Heterogeneous integration [1] is defined as using packaging technology to integrate dissimilar chips, photonic devices, or components (either side by side, stacked, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance. In general, heterogeneous integration can be classified as heterogeneous integration on organic substrates, on silicon substrates, on fan-out RDL (redistribution-layer) substrates, and on ceramic substrates. In this study, examples of these types of heterogeneous integration are given. Also, the applications of heterogeneous integration to package-on-package (PoP), CMOS image sensor (CIS), microelectromechanical systems (MEMS), and a vertical cavity surface emitted laser/photodiode (VCSEL/PD) detector are presented. Finally, the trends in heterogeneous integration are discussed.

Heterogeneous integration on organic substrates

Today, the most common applications of heterogeneous integration are on organic substrates, or the so-called SiPs. The assembly methods are usually surface mount technology (SMT) including solder-bumped flip chips with mass reflow and wire bonding chips on board. In general, these assembly methods are for low-end to middle-end applications, such as smartwatches, automobiles, smartphones, and many consumer products. **Figure 1** shows an example of heterogeneous integration on a printed circuit board (PCB). It can be seen that the heterogeneous integration of four chips and four capacitors are by the fan-out wafer-level packaging method [2,3]. The package size is 10mm x 10mm and has two RDLs. Sixty of

these samples without underfill went through the thermal cycling test—the failure locations and failure modes are shown in **Figure 1** (at 814 cycles). It can be seen that the failure locations are at the solder joints under the chip corners with the longest distance to neutral point (DNP) and the failure mode is the cracking of the solder joint between the package and the bulk solder.

Another example is the latest Apple iPhone XS and XS Max (**Figure 2**). The rear SiP (A) is a single-sided assembly that consists of the baseband chipset, a power management IC (PMIC), etc. The large SiP (B) on top is a two-sided assembly that consists of the A12 chipset, flash memory, etc. The small SiP (C) on top is also a two-sided assembly that consists of the RF front-end modules (FEMs).

All the PCBs are substrate-like PCB. Heterogeneous integration on organic substrates for high-performance applications have been proposed by Shinko with its integrated thin-film high-density organic package (i-THOP) substrate [4,5] as shown in **Figure 3**. It can be seen that thin-film layers are built on top of the build-up layers. The metal thickness, line width and spacing of the

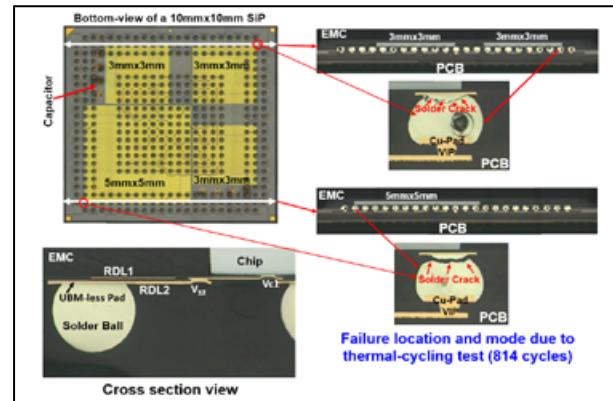


Figure 1: Heterogeneous integration of four chips on a PCB.

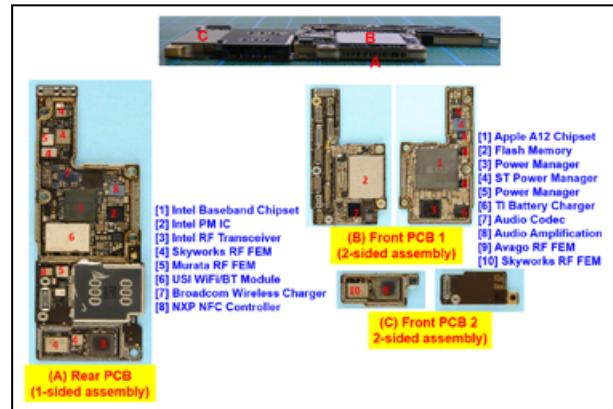


Figure 2: Apple's XS and XS Max iPhones. There are three SiPs supported by a substrate-like PCB.

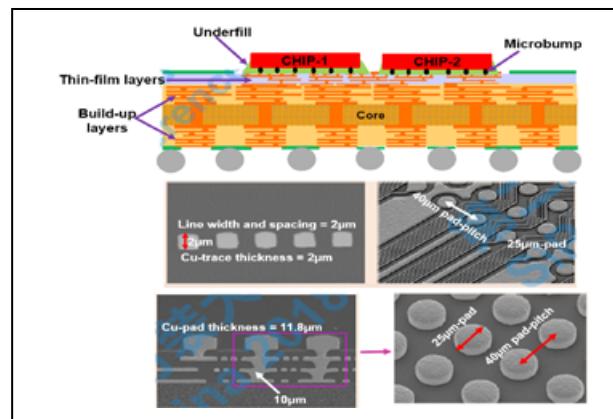


Figure 3: Shinko's i-THOP organic substrate (thin-film layers on top of build-up layers) for heterogeneous integration. Metal line width and spacing as well as thickness = 2µm; diameter and thickness of the Cu pads are, respectively 25µm and 11.82µm, and are on a 40µm pitch.

RDLs can be as small as $2\mu\text{m}$. The thin-film Cu RDLs are vertically connected through a $10\mu\text{m}$ via. The surface Cu pad-pitch is $40\mu\text{m}$ and the Cu pad-diameter is $25\mu\text{m}$ with a height of 10 - $12\mu\text{m}$.

Heterogeneous integration on silicon substrates

In this study, three different kinds of silicon substrates for heterogeneous integration applications are considered, namely, active or passive through-silicon via (TSV) interposers, TSV-less interposers such as bridges, and silicon optical bench.

Heterogeneous integration on TSV interposers. TSV interposers have been used for the lateral communications between chips, and the vertical interconnections between chips, and the next level of interconnect, such as package substrates. Since CEA-Leti [6], Xilinx/TSMC's chip-on-wafer-on-substrate (CoWoS) [7] and NVIDIA/TSMC's CoWoS-2 [8] are the most well-known examples of passive TSV interposers (no devices). **Figure 4** shows some active TSV interposers, such as those proposed by Intel. **Figure 4a** shows the FOVEROS technology (announced in December 2018). It can be seen that the TSV interposer is with CMOS devices (an active interposer), just like a chip, and is face-to-face thermal compression bonded with the chiplet/system-on-chip (SoC). It is expected to launch in the latter part of 2019 with Lakefield. **Figures 4b** and **4c** show another new technology, announced in July 2019, by Intel called omni-directional interconnect (ODI). For ODI Type 1 (**Figure 4b**), the active TSV interposers (chips) are underneath the big chip such as an SoC, and are face-to-face thermal compression bonded with the SoC. For ODI Type 2, the active TSV interposer (bridge, i.e., chip) is underneath and connecting the chiplets/SoCs. ODI Type 3 is a special case of Type 2, in which the active interposer (or the base logic chip) is connecting the SoCs/chiplets. Intel also announced the management data input/output (MDIO) for die-to-die interface, which is used to replace the current advanced interface bus (AIB). All these heterogeneous integrations on TSV interposers are for extreme high performance, and the

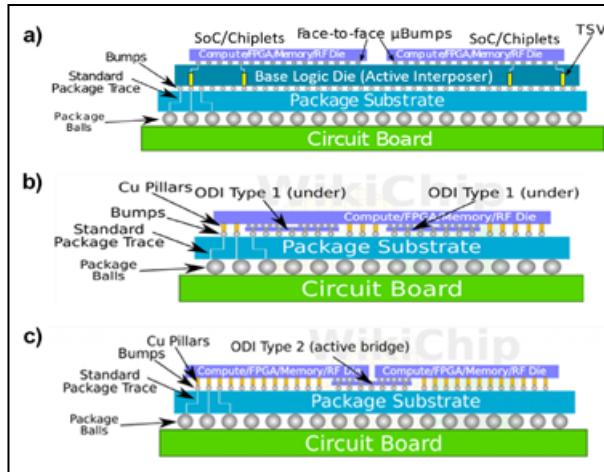


Figure 4: a) Intel's FOVEROS technology with active interposer; b) Intel's ODI technology – Type 1; and c) Intel's ODI technology – Type 2.

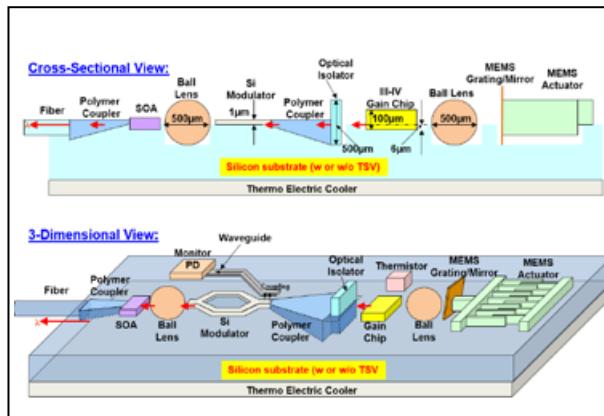


Figure 5: IME's MEMS-based tunable laser source with Si-modulator.

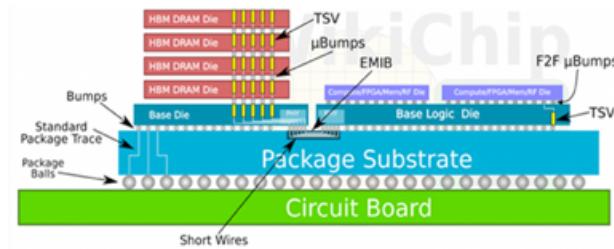


Figure 6: Intel's co-EMIB (a combination of EMIB and FOVEROS) to perform horizontal (EMIB) as well as vertical (FOVEROS) interconnections.

active TSV interposers are for even higher performance.

Heterogeneous integration on a silicon optical bench. In 2007, IME proposed a MEMS-based tunable laser source with Si-modulator, polymer couplers, and a III-IV gain chip on a silicon optical bench, which is cooled by a thermoelectric cooler as shown schematically in **Figure 5**. The key features of the MEMS actuator are: driving voltage = 30V @ $30\mu\text{m}$

displacement, resonant frequency = 2.559kHz , crosstalk $<-60\text{dB}$, polarization dependent loss $<0.1\text{dB}$, wavelength-dependent loss $<0.05\text{dB}$, rising time = $75.6\mu\text{s}$, falling time = $63.4\mu\text{m}$, and reliability $>1\times 10^7$ times. The key features of the Si-modulator are: total length = $3500\mu\text{m}$, splitter = $30\mu\text{m}$, combiner = $30\mu\text{m}$, modulator length $\sim 3440\mu\text{m}$, cross section $\sim 0.4\mu\text{m} \times 0.35\mu\text{m}$, designed maximum frequency $>20\text{GHz}$, and designed propagation loss $<20\text{dB/cm}$.

Heterogeneous integration on TSV-less interposers. TSV-less interposers such as embedded multi-die interconnect bridge (EMIB) [9] have been used by Intel for its notebook and field-programmable gate array (FPGA) products. For the notebook, the silicon bridge provides the lateral communications between the graphic processor unit (GPU) and the high-bandwidth memory (HBM). The vertical interconnections between the HBM/GPU/CPU (central processor unit) and the PCB are through the build-up organic package substrate. In July 2019, along with the ODI technology, Intel also announced the co-EMIB

technology. It is a combination of EMIB and FOVEROS as shown in **Figure 6**. It can be seen that the co-EMIB can do horizontal (EMIB) as well as vertical (FOVEROS) interconnections.

Heterogeneous integration on fan-out RDL-substrates

After STATS ChipPAC's FOFC-eWLB [10], ASE's FOCoS [11], and Samsung's Si-less RDL interposer [12], TSMC came out with its own solution (**Figure 7**). The figure

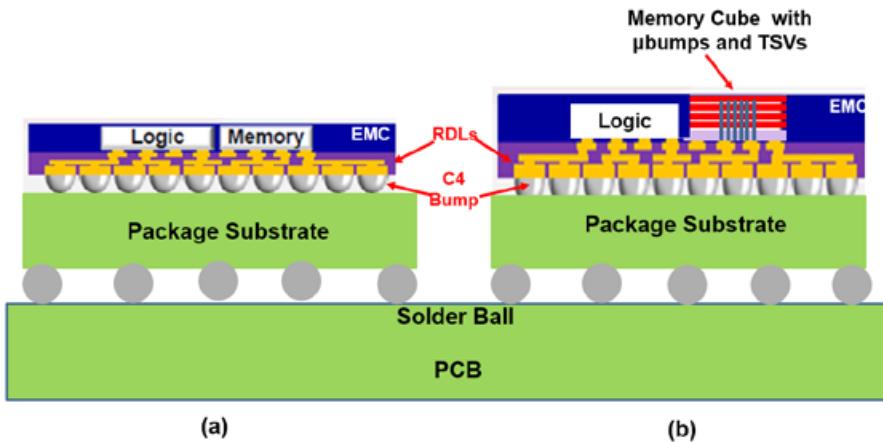


Figure 7: a) TSMC's integrated fan-out on substrate (InFO_oS); and b) TSMC's Integrated fan-out with memory on substrate (InFO_MS).

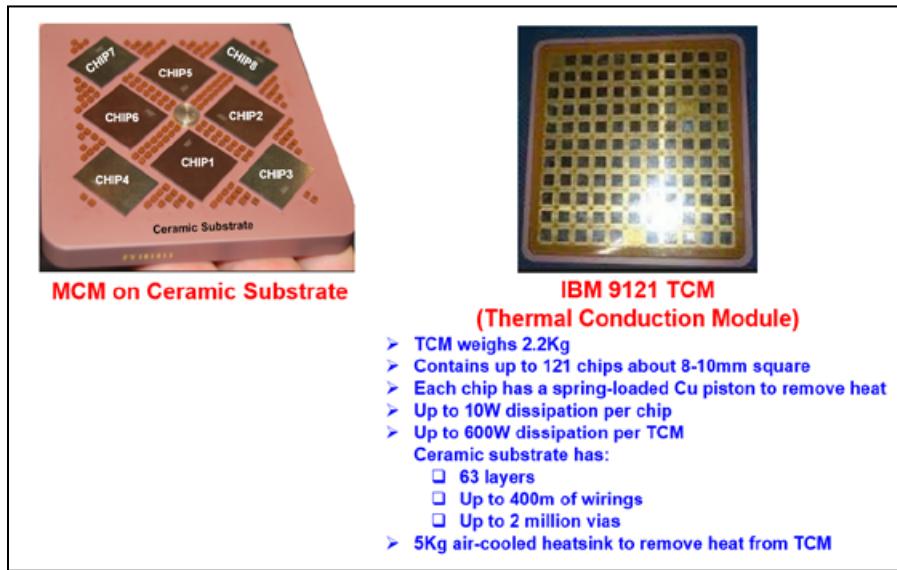


Figure 8: Heterogeneous integrations on ceramic substrates.

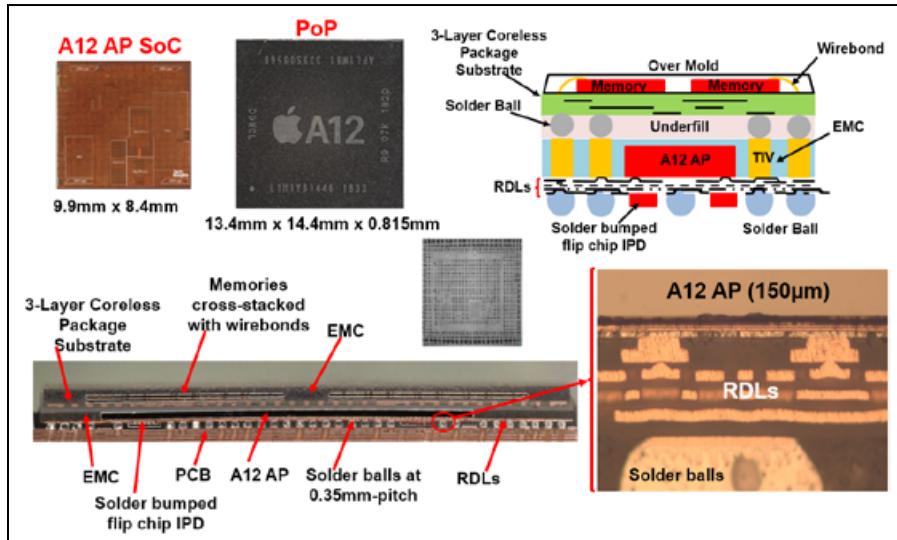


Figure 9: Heterogeneous integration of TSMC/Apple's PoP.

schematically illustrates TSMC's future fan-out RDL-substrates for heterogeneous integrations [13]. **Figure 7a** also shows the integrated fan-out on substrate (InFO_oS) for heterogeneous integration, which eliminates the micro bumps, underfill, and TSV interposer with the RDLs. **Figure 7b** shows the integrated fan-out with memory on substrate (InFO_MS), which is meant for higher performance applications.

Heterogeneous integration on ceramic-substrates

Figure 5a schematically shows an example of heterogeneous integration on ceramic-substrates. IBM's thermal conduction module (TCM) is the most well-known. For example, the TCM from an IBM 9121 mainframe processor contains up to 121 chips (8 to 10mm square) and the ceramic substrate is 63 layers, up to 400mm of wiring, and up to 2 million vias, **Figure 5b**.

Application of heterogeneous integration

The applications of heterogeneous integration to PoP, CIS, MEMS, and a VCSEL/PD detector are briefly mentioned in this section.

PoP for smartphones. **Figure 9** shows the schematic and images of the PoP for the application processor (AP) chip set in the iPhone shipped by Apple since October 2018. The PoP, which is a heterogeneous integration of the AP (A12) and the mobile DRAMs, is fabricated using TSMC's InFO-WLP technology. Basically, the PoP platform used for all the APs (A10, A11, and A12) is very similar. However, because TSMC used 7nm process technology to fabricate the A12, the chip dimensions are slightly smaller than that of A11 even though more functions, such as artificial intelligence, are included. In order to have a better electrical performance, there are a few integrated passive devices (IPDs), which are solder bumped flip chips at the bottom of the fan-out package as shown in **Figure 9**. There are three RDLs and the minimum metal line width and spacing are 8μm. The pitch of the solder balls of the package is 0.35mm.

CIS/processor with Cu-Cu hybrid bonding. The heterogeneous integration of the backside illuminated CIS (BI-CIS) chip and the processor chip with TSVs was in production by Sony from 2011 to 2015. In 2016, Sony was the first to

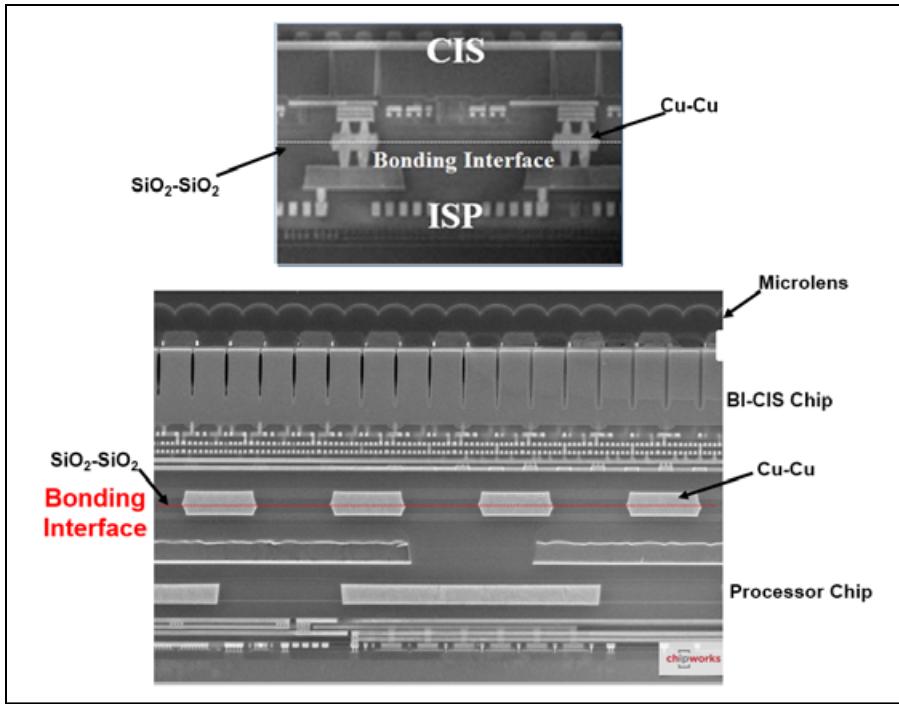


Figure 10: Heterogeneous integration of CIS and ASIC.

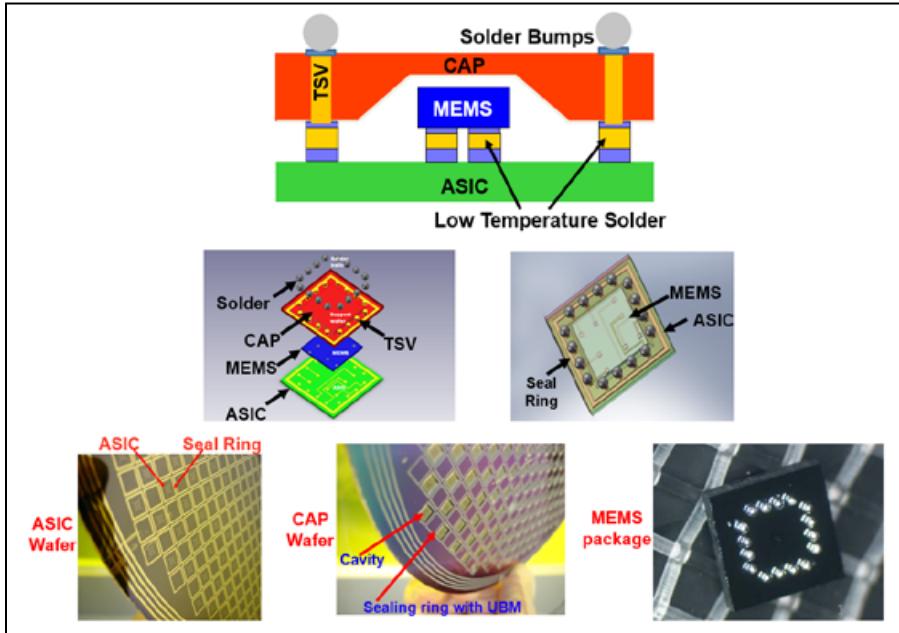


Figure 11: Heterogeneous integration of MEMS and ASIC.

use Cu-Cu direct hybrid bonding (which bonds the metal pads and dielectric layer on both sides of the wafers at the same time) in high-volume manufacturing. With this development, the TSVs were gone! Sony produced the IMX260 BI-CIS for the Samsung Galaxy S7, which shipped in 2016. Electrical test results [14] showed that their robust Cu-Cu direct hybrid bonding achieved remarkable

connectivity and reliability. The performance of the image sensor was also excellent. A cross section of the IMX260 BI-CIS is shown in **Figure 10**.

MEMS/ASIC with low-temperature bonding. **Figure 11** shows the heterogeneous integration of a MEMS and ASIC by IME [15]. The MEMS device (chip) is first bonded onto the ASIC wafer and then the ASIC wafer

with the MEMS devices is wafer-to-wafer bonded to the cap wafer with TSVs. Most current chip-to-wafer and wafer-to-wafer bonding methods use temperatures higher than 300°C. During bonding, however, the MEMS devices are already released (by way of free-standing microstructures, e.g., membranes, beams, and cantilevers), and low-temperature bonding is desired to reduce damage to the microstructure owing to the thermal-expansion mismatch of the bonding structure (less bow). With proper design of the bonding pads and under bump metallization (UBM), and selections of solder materials, 180°C or lower bonding temperatures are possible. During/after bonding, the solders will have reacted within themselves and the UBM, and become an intermetallic compound (IMC) with a melting point much higher than that of the solders. This feature is a welcome one by 3D MEMS and IC heterogeneous integration. For example, after the bonding of a MEMS device with an ASIC wafer with a low melting solder, all the bonding (solder interconnect) areas become the IMC with a very high re-melting temperature. When a cap wafer is bonded to the ASIC wafer (already bonded with the MEMS device), the interconnect between the ASIC and the MEMS devices will not be reflowed. Furthermore, when the whole 3D MEMS and IC heterogeneous integration module is attached to the PCB with surface mount technology (SMT) lead-free soldering (250°C), the solder interconnects between the ASIC and MEMS, and the cap and ASIC, will not be reflowed.

Embedded VCSEL/PD with polymer waveguide. The heterogeneous integration of a VCSEL and a PD detector is shown in this section. **Figure 12** shows a single-

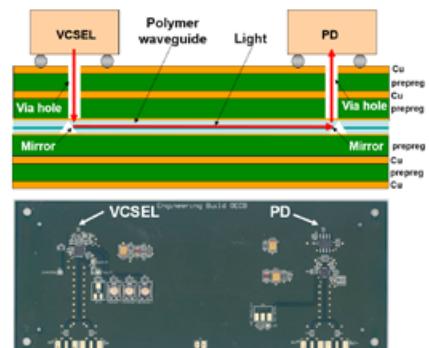


Figure 12: Heterogeneous integration of VCSEL and PD.

channel opto-electrical circuit board (OECB) with an embedded waveguide using a traditional PCB manufacturing process by IME and Unimicron [16]. The OECB is made up of four electrical layers and one optical layer embedded below a 60 μ m thick organic substrate. Two optical vias with 100 μ m diameter are formed to guide the optical beam from the VCSEL to the 45° mirror coupler. Likewise, the optical beam exiting the waveguide is diverted from the 45° mirror coupler through the optical via and received by the photodetector. A 10cm-long embedded polymer waveguide consists of a 70 μ m \times 70 μ m core and a 15 μ m-thick top and bottom cladding. Two 45° mirror couplers are formed at both corners of the waveguide by using a 90° diamond dicing blade. These mirrors convert the optical beam emitted from the VCSEL in the vertical path to the planar direction and into the waveguide. An embedded hybrid 3D heterogeneous integration of optoelectronic interconnects has been proposed [17], in which the VCSEL is flip-chip bumped onto the VCSEL driver chip with TSVs, which is flip-chip solder bumped onto the serializer chip.

Trends in heterogeneous integrations

The semiconductor industry has identified five main growth engines (applications), namely: 1) mobile, 2) high-performance computing (HPC), 3) automotive (especially self-driving cars), 4) Internet of Things (IoTs), and 5) big data (especially for cloud computing and edge computing). The system-technology drivers such as 1) 5G, 2) artificial intelligence (AI), and 3) machine learning (ML) are boosting the growths of these five semiconductor applications.

Packaging technologists are using various packaging methods such as wire bonding, flip chip, build-up substrate, PoP, wafer-level chip-scale package (WLCSP), FOWLP and panel-level packaging (PLP), 2.5D/3D IC integration, HBM, MCM/SiP/heterogeneous integration/chiplets, and bridges to house (package) the semiconductor devices for the five main applications listed above. Because of the drive of 5G, AI, and ML, in general, the semiconductors' density increases, pad-pitch decreases, and chip size increases.

All these provide challenges (opportunities) to packaging technologists.

One of the packaging technologies is heterogeneous integration. For the next few years, we will see more of a higher level of heterogeneous integrations, whether it is for time to market, performance, form factor, power consumption, signal integrity, and/or cost.

How to select different types of heterogeneous integrations? It depends on the applications. The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations. For example, with respect to semiconductors driven by AI for HPC applications, the metal line width and spacing of the RDLs of the heterogeneous integrations must be ultrafine (<2 μ m or down to sub-micron). In this case, the silicon substrate, such as the TSV-interposer is needed. On the other hand, semiconductors driven by 5G for mobile applications, the metal line width and spacing of the RDLs of the

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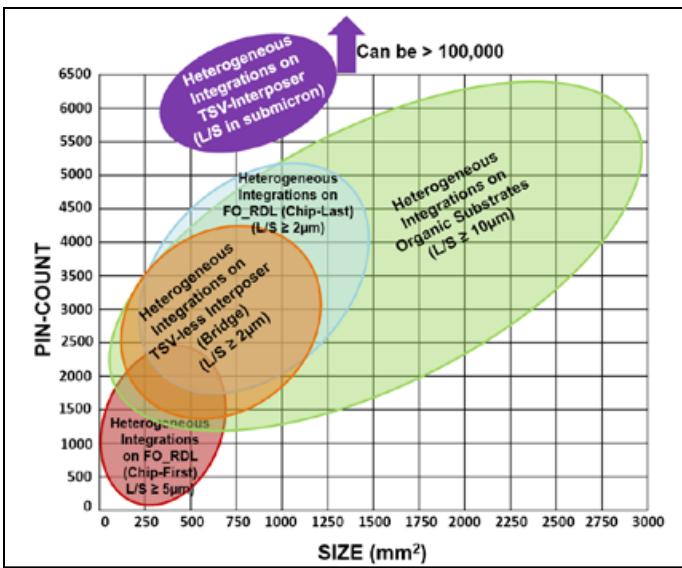


Figure 13: Heterogeneous integration on various substrates with different size, pin-count, and metal line width and spacing.

heterogeneous integrations are in the 10 μm range. In this case, a build-up organic substrate for the RF chip and antenna-in-package (AiP) is adequate, but on a fan-out substrate is even better on account of there being less transmission loss [18].

Figure 13 shows the application ranges (size, pin count, and metal line width and spacing (L/S) of RDLs) for heterogeneous integrations on various substrates. It can be seen that: 1) the heterogeneous integrations on silicon substrates (TSV-interposers) can have the largest number of pin counts ($>100,000$), smallest metal L/S (sub-micron), but the largest substrate size is = 1200mm 2 today; 2) the heterogeneous integrations on silicon substrates (TSV-less interposers such as bridges) can have pin counts of 4000, very small L/S ($\geq 2\mu\text{m}$), and the substrate size being $\leq 1200\text{mm}^2$; 3) the heterogeneous integrations on fan-out (chip-first) substrates can have pin counts of 2500, metal L/S ($\geq 5\mu\text{m}$), and the substrate size $\leq 625\text{mm}^2$; 4) the heterogeneous integrations on fan-out (chip-last) substrates can have pin counts of ≥ 5000 , L/S ($\geq 2\mu\text{m}$), and the substrate size $\leq 1400\text{mm}^2$; and 5) the heterogeneous integrations on organic substrates can have pin counts up to 6000, metal L/S ($\geq 10\mu\text{m}$), and the substrate size can be as large as 3000mm 2 .

Summary

Some important results and recommendations are summarized as follows:

- Heterogeneous integration has been defined and classified.
- Examples of heterogeneous integrations on organic substrates, silicon substrates, fan-out RDL substrates, and ceramic substrates have been provided.
- The applications of heterogeneous integration to PoP, CIS, MEMS, VCSEL, etc., have also been briefly mentioned.
- The selection of various heterogeneous integration schemes depends on the applications. The most important selection criterion is the metal line width and spacing of the RDLs for the substrates being used in the various

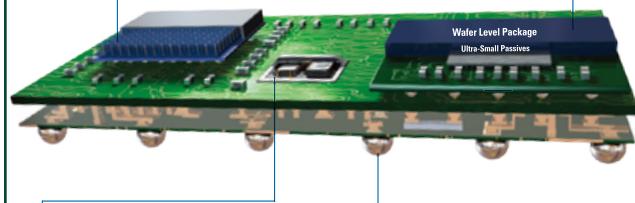
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- heterogeneous integrations.
 - 75% of the heterogeneous integrations will be on organic substrates (actually, most are SiPs). They are in very high-volume consumer products such as automobiles, smartwatches and smartphones. 25% of the heterogeneous integrations will be on other substrates such as silicon, fan-out RDLs, and ceramic and they will be used in small-volume products, such as HPC.
 - In order to promote the various kinds of heterogeneous integration/chiplet schemes, standards are necessary! The Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS) is heading in the right direction.
 - Electronic design automation (EDA) tools for automating system partitioning and design are desperately needed for complex heterogeneous integration systems.
 - For the next few years, we will see more of a higher level of heterogeneous integration, whether it is for time to market, performance, form factor, power consumption, signal integrity, and/or cost.
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Biography

John H. Lau is Executive Assistant to the Chairman at Unimicron Technology Corporation, Taoyuan City, Taiwan (ROC). He has more than 38 years of R&D and manufacturing experience in semiconductor packaging, 480 peer-reviewed papers, 30 issued and pending US patents, and 20 textbooks. He is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. He earned a PhD degree from the U. of Illinois at Urbana-Champaign. Email John_Lau@unimicron.com

Burn-in: when, for how long, and at what level?

By Ephraim Suhir *[ERS Co.]*

It is shown that the bathtub curve (BTC) based time-derivative of the failure rate at the BTC initial moment of time can be considered as a suitable criterion of whether burn-in testing (BIT) for a packaged IC device should be, or does not have to be conducted. It is shown also that this criterion is, in effect, the variance of the random statistical failure rate (SFR) of the mass-produced components that the manufacturer of the product of interest received from numerous vendors, whose commitments to reliability were unknown, and therefore the random SFR of these components might vary significantly, from zero to infinity. Based on the general formula for the non-random SFR of a product comprised of such components, the solution for the case of normally distributed random SFR of the constituent components was obtained. This information enables answering the “to burn-in or not to burn-in” question in electronics manufacturing.

If BIT is decided upon, the Boltzmann-Arrhenius-Zhurkov (BAZ) model can be employed for the assessment of its required duration and level. Our analyses shed light on the role and significance of important factors that affect the testing time and stress level: 1) the random SFR of mass-produced components of which the product of interest is comprised; 2) the way to assess, from the highly focused and highly cost-effective failure-oriented-accelerated-testing (FOAT), the activation energy of the “freak” population; 3) the role of the applied stressor(s); and, most importantly, 4) the probabilities of the “freak” failures depending on the duration of the BIT effort, and a way to assess these probabilities as functions of the duration and level of the BIT, and the variance of the random SFR of the mass-produced components of which the product of interest is comprised.

These factors should be considered when there is an intent to quantify and, eventually, to optimize the BIT procedure. Future work should include experimental verifications of the suggested concepts, methodologies and predictions.

Background

BIT (see, e.g., [1–3]) is an accepted practice for detecting and eliminating early failures in newly fabricated electronic products prior to shipping the “healthy” ones that survived BIT to the customer(s). BIT can be based on temperature cycling, elevated temperatures, voltage, current, humidity, random vibrations, etc., and/or, because the principle of superposition does not work in reliability engineering, on the appropriate combination of these stressors. BIT is a costly undertaking: early failures are avoided and the infant mortality portion (IMP) of the BTC is supposedly eliminated at the expense of the reduced yield. But what is even worse, the elevated BIT stresses might not only eliminate “freaks,” but could cause permanent damage to the main population of the “healthy” products. BIT should, therefore, be well understood, thoroughly planned, and carefully executed.

It is unclear, however, whether BIT is always needed, nor to what extent are the current BIT practices adequate and effective. Highly accelerated life testing (HALT) [4], which is the procedure of choice currently employed as a BIT vehicle, is a “black box” that tries “to kill many birds with one stone” and is unable to provide any trustworthy information on what it does. It also remains unclear what could possibly be done to develop an insight into what is actually happening during, and as a result of, the HALT-based BIT and how to effectively eliminate “freaks,” while minimizing the testing time, reducing its cost and avoiding damaging the sound devices. When HALT is relied upon to do the job, it is not even easy to determine whether there exists a decreasing failure rate with time. There is, therefore, an obvious incentive to develop ways, in which the BIT process could be better understood, trustworthy quantified, effectively monitored and possibly optimized. Accordingly, in this analysis some important BIT aspects are addressed for a

packaged electronic product comprised of numerous mass-produced components [5].

We intend to shed some quantitative light on the BIT process, and, since nothing is perfect (the difference between a highly reliable process or a product and an insufficiently reliable one is “merely” in the levels of their never-zero probability of failure), such a quantification should be done on a probabilistic basis. Particularly, a suitable criterion should be developed to answer the fundamental “to burn-in or not to burn-in” question [6], and if BIT is decided upon, a way to quantify its outcome should be found. This could be done using the BAZ model [7]. This model has been recently employed as an effective constitutive equation in the probabilistic design for reliability (PDFR) [8] for packaged IC devices, when there is an intent to evaluate the probability of failure and the corresponding lifetime of a packaged electronic or an optical product. The model was suggested by Zhurkov [7] in the kinetic theory of the strength of solids as a generalization of Arrhenius’ theory of chemical reactions [9] and Boltzmann’s thermodynamic theory of gases [10].

Analysis

A major question that needs to be asked is, “Is burn-in always needed?” The following two sections discuss two mutually complementary and independent analyses: 1) The analysis of the configuration of the IMP of a BTC obtained for a more or less well established manufacturing technology of interest; and 2) The analysis of the role of the random SFR of the mass-produced components of which the product of interest is comprised as far as the effect of this SFR on the nonrandom initial SFR of the product is concerned.

Prediction based on the analysis of the BTC configuration. The desirable steady-state portion of the BTC commences at the end of BIT as a result of the interaction of two major irreversible time-dependent processes: the “favorable”

statistical process that results in a decreasing failure rate with time, and the “unfavorable” physics-of-failure-related process resulting in an increasing failure rate. The first process dominates at the IMP of the BTC and is considered here. The IMP of a typical BTC, the “reliability passport” of a mass-produced electronic product, can be approximated as:

$$\lambda(t) = \lambda_0 + (\lambda_1 - \lambda_0) \left(1 - \frac{t}{t_1}\right)^{n_1}, \quad 0 \leq t \leq t_1.$$

Here, λ_0 is the BTC’s steady-state minimum, λ_1 is its initial (highest) value at the beginning of the IMP, t_1 is the duration of the IMP, the exponent n_1 is $n_1 = \frac{\beta_1}{1-\beta_1}$, and β_1 is the measure of “fullness” of the BTC’s IMP. This “fullness” is defined as the ratio of the area below the BTC to the area $(\lambda_1 - \lambda_0)t_1$ of the corresponding rectangular. The exponent n_1 changes from zero to one, when the fullness β_1 changes from zero to 0.5. The time derivative of the failure rate at the initial moment of time ($t = 0$) is $\lambda'(0) = -\frac{\lambda_1 - \lambda_0}{t_1} \frac{\beta_1}{1-\beta_1}$. If this derivative

is zero or nearly zero, this means that the IMP of the BTC is parallel to the time axis (so that there is, in effect, no IMP at all), that no BIT is needed to eliminate this portion, and “not to burn-in” is the answer to our basic question: the initial value λ_1 of the BTC is not different from its steady-state λ_0 value. What is less obvious is that the same result takes place for $\frac{\beta_1}{t_1} = 0$.

This means that although BIT is needed, the testing could be short and low level, because there are not too many “freaks” in the population and because, although these “freaks” exist, they are characterized by very low probabilities of non-failure, so that the planned BIT process could be a next-to-an-instantaneous one. The maximum value of the fullness β_1 is $\beta_1 = 0.5$. This corresponds to the case when the IMP of the BTC is a straight line connecting the initial, λ_1 , and the steady-state, λ_0 , BTC values. The derivative $\lambda'(0)$ is $\lambda'(0) = \frac{d\lambda(t)}{dt} = -\frac{\lambda_1 - \lambda_0}{t_1}$ in this case, and this seems to be the case, when the BIT is mostly needed.

Prediction based on the analysis of the random SFR process. The non-random time t dependent SFR

$$\lambda_{SR}(t) = \frac{\int_{\lambda_0}^{\infty} \exp(-\lambda t) f(\lambda) d\lambda}{\int_{\lambda_0}^{\infty} \exp(-\lambda t) f(\lambda) d\lambda}$$

can be obtained from the probability density distribution function $f(\lambda)$ for the random SFR λ [5]. When this failure rate is normally distributed, i.e., when

$$f(\lambda) = \frac{1}{\sqrt{2\pi D}} \exp\left(-\frac{(\lambda - \bar{\lambda})^2}{2D}\right),$$

the above formula yields:

$$\lambda_{SR}(t) = \sqrt{2D} \varphi[\tau(t)].$$

The “time function” $\varphi[\tau(t)]$ depends on the dimensionless “physical” (effective) time

$$\tau = t \sqrt{\frac{D}{2}} - s, \quad \text{where the } s = \frac{\bar{\lambda}}{\sqrt{2D}}$$

known in the probabilistic reliability theory as the safety factor, can be interpreted as a measure of the degree of uncertainty of the random SFR. The time derivative $\lambda'_{SR}(t)$ is expressed as

$$\lambda'_{SR}(t) = \sqrt{2D} \frac{d\varphi[\tau(t)]}{dt} = \sqrt{2D} \frac{d\varphi}{d\tau} \frac{d\tau}{dt} = D\varphi'(\tau).$$

It can be shown that the derivative $\varphi'(\tau)$ at the initial moment of time ($t = 0$) is equal to -1.0 , so that

$$\lambda'_{SR}(0) = \lambda'_1 = -D.$$

This result explains the physical meaning of this derivative: it is the variance (with a “minus” sign, of course) of the random SFR of the constituent mass-produced components.

Duration of BIT

If it is decided to conduct BIT, then one has to determine its duration and level. The BAZ model suggests a simple, easy-to-use, highly flexible and physically meaningful way to evaluate the probability of failure of a material or a device after the given time in testing or operation at the given temperature and under the given stress or stressors. Using this model, the probability of non-failure during the BIT can be sought as

$$P = \exp\left[-\gamma_i D I_* t \exp\left(-\frac{U_0 - \gamma_o \sigma}{kT}\right)\right].$$

Here D is the variance of the random SFR of the mass-produced components, I is the measured/monitored signal (e.g., leakage current, whose agreed-upon high value I_* is considered as an indication of failure; or an elevated electrical resistance, particularly suitable for solder joint interconnections), t is time, σ is the “external” stress, U_0 is the activation energy (unlike in the original BAZ model, this energy may or may not be affected by the level of the external stress), T is the absolute temperature,

γ_o is the stress sensitivity factor and γ_i is the time sensitivity factor. The above distribution makes physical sense. Indeed, the probability, P , of non-failure decreases with an increase in the variance D , in the time t , in the level I_* of the leakage current at failure, and in the temperature T , and increases with an increase in the level of the activation energy U_0 .

The time derivative of the probability P is $\frac{dP}{dt} = -\frac{H(P)}{t}$, where $H(P) = -P \ln P$

is the entropy of the distribution. This explains the reliability physics underlying this distribution: the probability of non-failure is proportional to the entropy of its distribution and is inversely proportional to the time of testing or operation. The entropy $H(P) = -P \ln P$ is zero for $P = 0$ and for $P = 1$, and reaches its maximum $H_{\max} = e^{-1}$ for $P = e^{-1}$. The maxima of the entropy and the probability of non-failure take place at the moment of time

$$t = \frac{1}{\gamma_i D I_*} \exp\left(\frac{U_0 - \gamma_o \sigma}{kT}\right),$$

and it is this time that is accepted in the BAZ model as the mean time to failure (MTTF).

There are three unknowns in the above expressions: the product $\rho = \gamma_i D$; the stress-sensitivity factor, γ_o , and the activation energy U_0 . These unknowns could be determined from a two-step FOAT. At the first step, testing should be carried out for two temperatures, T_1 and T_2 , but for the same effective activation energy, $U = U_0 - \gamma_o \sigma$. Then the relationships

$$P_{1,2} = \exp\left[-\rho I_* t_{1,2} \exp\left(-\frac{U_0 - \gamma_o \sigma}{kT_{1,2}}\right)\right]$$

for the measured probabilities of non-failure can be obtained. Here, $t_{1,2}$ are the corresponding times, and I_* is the leakage current at failure. Because the numerator $U = U_0 - \gamma_o \sigma$ in these relationships is kept the same, the amount $\rho = \gamma_i D$ can be found as

$$\rho = \exp\left[\frac{1}{\theta - 1} \left(\frac{n_2^{\theta}}{n_1}\right)\right],$$

$$\text{where } n_{1,2} = -\frac{\ln P_{1,2}}{I_* t_{1,2}} \quad \text{and} \quad \theta = \frac{T_2}{T_1}.$$

The second step of testing, aimed at the evaluation of the stress sensitivity factor γ_o , should be conducted at two stress levels, σ_1 and σ_2 , (such as, say, temperatures or voltages). If the stresses σ_1 and σ_2 are thermal stresses determined for the temperatures T_1 and T_2 they could be evaluated using a suitable stress model. Then $\gamma_o = k \frac{T_1 \ln n_1 - T_2 \ln n_2 + (T_2 - T_1) \ln \rho}{\sigma_1 - \sigma_2}$.

If, however, the external stress is not a thermal stress, then the temperatures at the second step test should preferably be kept the same. Then the ρ value will not affect the factor, γ_σ , which could be found as

$$\gamma_\sigma = \frac{kT}{\sigma_1 - \sigma_2} \ln\left(\frac{n_1}{n_2}\right),$$

where T is the testing temperature. Finally, after the product ρ and the factor γ_σ are determined, the activation energy U_0 can be determined as

$$U_0 = -kT_1 \ln\left(\frac{n_1}{\rho}\right) + \gamma_\sigma \sigma_1 = -kT_2 \ln\left(\frac{n_2}{\rho}\right) + \gamma_\sigma \sigma_2.$$

The probability of non-failure dependent random time-to-failure (TTF) can be obviously determined as $TTF = MTTF(-\ln P)$, where the MTTF has been defined above.

As an example, the following data were obtained at the first step testing:

1. After $t_1=14h$ of testing at the temperature of $T_1 = 60^\circ C = 333 K$, 90% of the devices reached the critical level of the leakage current of $I_s=3.5\mu A$ and, hence, failed, so that the recorded probability of non-failure is $P_1=0.1$; the applied stress is elevated voltage $\sigma_1=380V$;
2. After $t_2=28h$ of testing at the temperature of $T_2 = 85^\circ C = 358 K$, 95% of the samples failed, so that the recorded probability of non-failure is $P_2=0.05$. The applied external stress is still elevated voltage of the level $\sigma_1=380V$.

$$n_1 = -\frac{\ln P_1}{I_s t_1} = -\frac{\ln 0.1}{3.5 \times 14} = 4.6991 \times 10^{-2} \mu A^{-1} h^{-1};$$

$$n_2 = -\frac{\ln P_2}{I_s t_2} = -\frac{\ln 0.05}{3.5 \times 28} = 3.0569 \times 10^{-2} \mu A^{-1} h^{-1};$$

$$\text{Then } \theta = \frac{T_2}{T_1} = \frac{358}{333} = 1.0751, \text{ and}$$

$$\rho = \exp\left[\frac{1}{\theta - 1} \left(\frac{n_2^0}{n_1} \right)\right] = \exp\left[\frac{1}{0.0751} \left(\frac{0.030569^{1.0751}}{0.046991} \right)\right] = 785.3197 \mu A^{-1} h^{-1}.$$

At the second step of testing, one can use, without conducting additional tests, the above information from the first step, its duration and outcome. Let us assume that testing at the second step has shown that after $t_2=36h$ of testing at the same temperature of $T_1 = 60^\circ C = 333 K$, 98% of the tested samples failed, so that the predicted probability of non-failure is $P_2=0.02$. If the stress σ_2 is elevated voltage $\sigma_2=220V$, then

$$n_2 = -\frac{\ln P_2}{I_s t_2} = -\frac{\ln 0.02}{3.5 \times 36} = 3.1048 \times 10^{-2} \mu A^{-1} h^{-1},$$

and the formula for the stress sensitivity factor γ_σ yields:

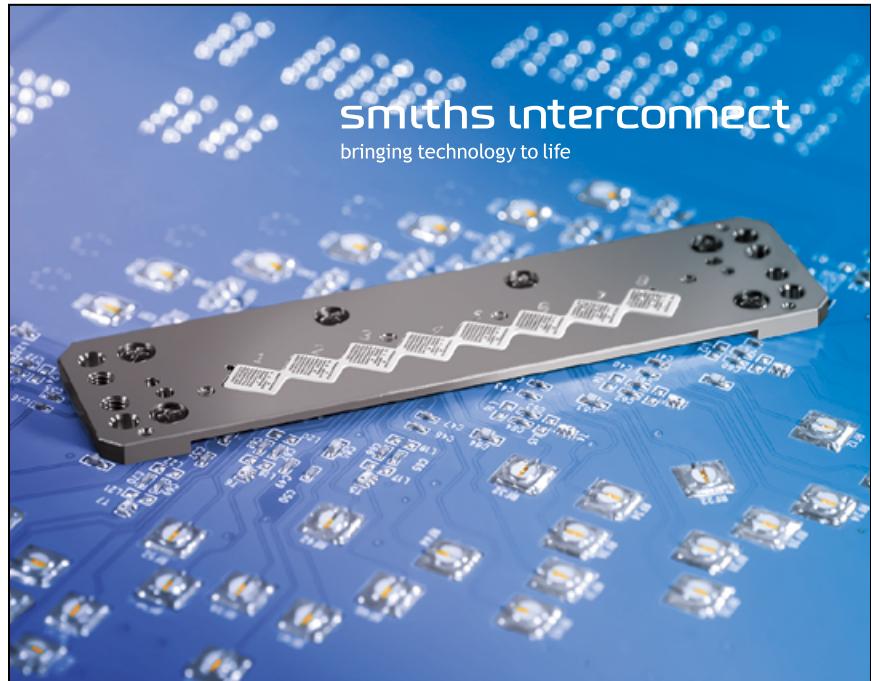
$$\gamma_\sigma = kT \frac{\ln\left(\frac{n_1}{n_2}\right)}{\sigma_1 - \sigma_2} = 8.61733 \times 10^{-5} \times 333 \frac{\ln\left(\frac{4.6991 \times 10^{-2}}{3.1048 \times 10^{-2}}\right)}{380 - 220} = 4326 \times 10^{-5} eV \times V^{-1}.$$

Then

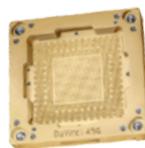
$$U_0 = -kT \ln\left(\frac{n_1}{\rho}\right) + \gamma_\sigma \sigma_1 = -8.61733 \times 10^{-5} \times 333 \ln\left(\frac{4.6991 \times 10^{-2}}{785.3197}\right) + 7.4326 \times 10^{-5} \times 380 = 0.2790 + 0.0282 = 0.3072 eV$$

or, to make sure that there was no calculation error,

$$U_0 = -kT \ln\left(\frac{n_2}{\rho}\right) + \gamma_\sigma \sigma_2 = -8.61733 \times 10^{-5} \times 333 \ln\left(\frac{3.1048 \times 10^{-2}}{785.3197}\right) + 7.4326 \times 10^{-5} \times 220 = 0.2909 + 0.0164 = 0.3072 eV.$$



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No wonder that these values are considerably lower than the activation energies of “healthy” products. Many manufacturers feel (“rule of thumb”) that the level of 0.7eV can be used as an appropriate tentative number for the activation energy of “healthy” electronic products. In this connection it should be indicated that when the BIT process is monitored and the activation energy U_0 is being continuously calculated based on the number of the failed devices, the BIT process should be terminated, when the calculations, based on the FOAT data, indicate that the energy U_0 starts to increase. The calculated data show also that this energy slightly increases with an increase in the level of loading. This increase is, however, only about 5-8%. The MTTF is

$$t = \frac{1}{\rho I_*} \exp\left(\frac{U_0 - \gamma_\sigma \sigma}{kT}\right) = \frac{1}{785.3197x3.5} \exp\left(\frac{0.3072 - 7.4326 \times 10^{-5}}{8.61733 \times 10^{-5} x 333}\right) = 16.1835h,$$

and the TTF is $t = MTTF \times (\ln P)$. The calculated BIT-related TTF for different probabilities of non-failures are shown in **Table 1**.

P	0.0050	0.0075	0.0100	0.0500
TTF, h	85.7453	79.1835	74.5278	48.4814

Table 1: TTF vs. probability of non-failure.

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Clearly, the probabilities of non-failure for successful BITs should be low enough. It is clear also that the BIT process should be terminated when the calculated probabilities of non-failure and the activation energy U_0 start rapidly increasing: this means that testing is “invading” the “healthy” products domain.

Summary

Although our analysis does not suggest any straightforward and complete way of how to optimize BIT, it nonetheless sheds useful and insightful light on the significance of some important

factors that affect the BIT’s required time and level for a product comprised of mass-produced components. Future work should include experimental verification of the suggested concepts and criteria.

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Biography

Ephraim Suhir is on the faculty of the Portland State U., Portland, OR, and is also CEO of ERS Co., Los Altos, CA, USA. He has authored 400+ publications, presented numerous keynote and invited talks worldwide, and received many professional awards, including 1996 Bell Labs DMTS Award, 2004 ASME Worcester Read Warner Medal (he is the third “Russian American,” after S. Timoshenko and I. Sikorsky, who received this prestigious award) and 2019 IEEE EPS Field award for seminal contributions to mechanical reliability engineering. Email suhire@aol.com; www.ERSuhir.com

Extreme cooling solution for power electronics and next-generation optoelectronic sensors

By Philippe Soussan *[imec]*

Bringing more and more miniaturized and high-performance components together in increasingly smaller packages is a major trend in the manufacturing of electronic products. This evolution is well-known in the microelectronics industry, where 3D integration technologies are increasingly used to generate compact high-performance computing systems, as one way to further extend Moore's Law. The trend is also emerging in a variety of related application domains that are more driven by system constraints, including, for example, the smart factory and smart mobility. Here, smart robot solutions – self-guided by sensors and actuators – are equipped with compact high-performance microsystems. These systems typically implement the latest generation of power electronics, able to work at high frequencies and to withstand high temperatures.

The downside of the evolution described above is a dramatic increase in the system's heat generation—negatively impacting its performance and reliability. Today's air-cooling solutions are inadequate to remove the excess heat in small form factors. This situation calls for innovative technologies able to remove the large amounts of heat from the small system area.

With respect to smart factory robots or autonomous vehicles, the requirements for heat removal from, as an example, power devices, are challenging to meet. Heat sinks must be robust, low cost and have a high cooling performance—capable of reaching heat dissipation levels of 500W/cm^2 and beyond. In case a liquid is used for heat removal, no leakage of the liquid towards the system can be tolerated. Moreover, the space for implementing any liquid-containing

cooling system is very limited, and the cooling system may not limit the robot's mobility.

Why choose a microfluidics heat sink?

Through the years, a variety of cooling solutions, including air-cooled heat sinks, two-phase refrigeration and jet impingement systems, have been explored. All of these systems come with their own advantages and drawbacks. Among the various approaches, the use of microchannel structures turned out to be very effective as heat sinks. These microchannels serve as flow passages for a cooling liquid (such as water), which in general is more effective in removing heat compared to air. This greater effectiveness is due to the liquid's higher thermal conductivity and specific heat capacity. By pumping the liquid into small, parallel, high-aspect-ratio microchannel structures, the convective heat transfer surface area and the heat transfer coefficient is further increased, enabling a high heat flux removal.

Microchannel arrays have already been extensively studied since their first introduction in the early 1980s. Although using microchannels to cool electronics is attractive, their use and cost-effective implementation remained challenging until now. The cost issue can be resolved by using silicon (Si)-based fabrication processes – with Si being a high thermal conductive solid. Si-based technology allows the fabrication of high-quality and low-cost devices, with a high yield and large volume, by leveraging massively parallel production processes.

In order to increase the heat transfer performance of the microchannels, varying channel dimensions and structures in different configurations have been explored. In many cases,

a tradeoff had to be made between a decreasing overall thermal resistance and an increasing pressure drop along the channels, which is known to negatively affect the heat transfer performance.

Tuning the channel dimensions

A team of researchers at imec has developed a Si-based microchannel heat sink that can be fabricated separately and then interfaced to the backside of a target heat-dissipating chip. The team's major objective was to minimize the system's total thermal resistance by optimizing the heat sink's channel width and height for a given flow rate and pressure drop, and by finding an optimized process for bonding the two chips.

Optimized dimensions for continuous straight channels were obtained from both analytical and numerical calculations, and validated experimentally. Following the analytical study, the total thermal resistance can be described as the sum of the conduction resistance, the convective resistance, the caloric resistance, and the contact resistance. The convective resistance, which accounts for the ability to transfer the heat from the solid heat sink surfaces to the liquid, largely depends on the channel dimensions. The contact resistance accounts for the interface thermal resistance between the two Si pieces and can be minimized by optimizing the bonding process.

Once the optimized microchannel geometry and bonding parameters are found for a given flow and pressure drop, 3D thermal and fluidic simulations are performed to predict the fluidic performance and thermal behavior of the heat sink. By using the approach described above, the design and fabrication of the microfluidic heat sink can be tailored to any external system constraints, such as space or liquid supply.

Key ingredient: high-aspect ratio microstructures

The above approach was applied for developing an optimized Si-based microfluidic heat sink assuming a maximal water flow rate of 150mL/min and a maximal pressure drop of 2.5bar (**Figure 1**). Analytical calculations revealed an optimal channel width of about 20-30 μ m for a channel height between 150 and 250 μ m (**Figure 2**). Based on these results, microstructures with a 30 μ m channel width and a target channel depth of 250 μ m were designed.

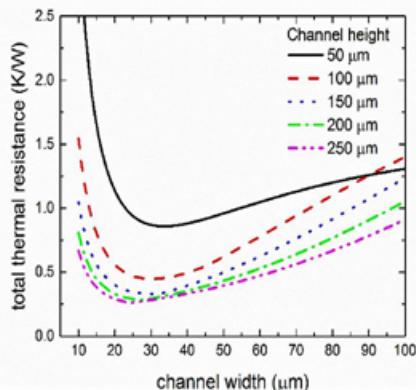


Figure 2: Analytical calculation of the total thermal resistance considering different channel dimensions, assuming a flow rate of 150mL/min and a maximal pressure drop of 2.5bar.

Microchannel heat sinks with the dimensions noted above were subsequently fabricated using advanced CMOS-compatible Si fabrication processes. In particular, the deep reactive-ion etch (DRIE) process was used to fabricate microchannels with a challenging high aspect ratio – key components of the micro-cooler (**Figure 3**).

The heat sink can be interfaced to the backside of any heat-dissipating chip using fusion bonding and thermocompression bonding (**Figure 4**). In this study, a 5x5mm² thermal test chip that was able to generate a high heat flux and to sense the temperature variation via tungsten (W) resistors was used. By using an optimized copper/tin-gold (Cu/Sn-Au) interface, a very low thermal contact resistance was achieved between both parts.

Robust, fully-sealed channels were obtained in a so-called “closed channel” configuration. The team also studied an alternative configuration, called “open channel.” In this configuration,

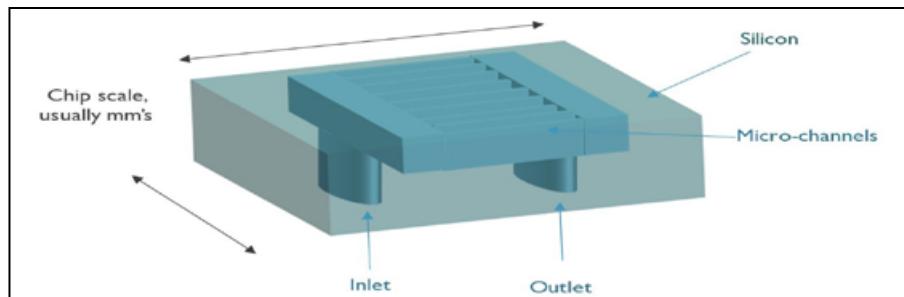


Figure 1: Schematic view of the micro-cooler.

an even lower thermal resistance can be expected. But the sealing of the channels entirely relies on the bonding process between the two Si pieces, which is a more challenging approach. Alternatively, the channel wafer can be directly bonded at full wafer scale for even less thermal resistance.

Cooling results: a power dissipation of 600W/cm² (and beyond)

Imec’s compact heat sink assembled to the thermal test chip achieves a total thermal resistance as low as 0.34K/W at less than 2W pump power. It enables a high heat flux removal far beyond any conventional air-based heatsink. This makes it possible to dissipate power of more than 600W/cm² while keeping the component temperature below 100°C. The cooling chip typically contains 67 parallel channels, implemented in a small form factor on the order of a few tens of mm².

Cooling the next generation of applications

The cooling performance of the cooling chip and the tailored approach to the chip design make the proposed solution particularly appealing for any application that is dealing with high-performance thermal management of wide band gap optoelectronics materials, and with the cooling of read and drive circuitry. This covers in a non-exhaustive way the following applications:

- Radio-frequency/microwave modules for the next generation of telecom systems with high-performance directive antennas. Such modules typically rely on the integration of a heat-generating power amplifier to be able to deliver a strong burst to the antennas. Current solutions remain very bulky.

- Next generation of power electronics modules based on GaN or Si. These are typically used for engine, drive train and electric motor management of cars, robots, and in the uprising generation of electric vehicles.
- Novel integrated sensors for light detection and ranging (LIDAR) applications, spectrometry relying on the III-V integration with CMOS and photonics technologies. Current systems that are based on free space optics are not scalable by nature. An effective cooling solution will be needed especially for the laser integration.
- Temperature management of specialty microelectromechanical systems (MEMS) products for lab-on-chip applications. These systems typically have a drive and read IC connected to a MEMS (fluidic) device. Such microsystems are seeing major adoption in the biomedical field where the chip temperature needs to remain cold in order to avoid destroying a large variety of (bio)chemical agents.

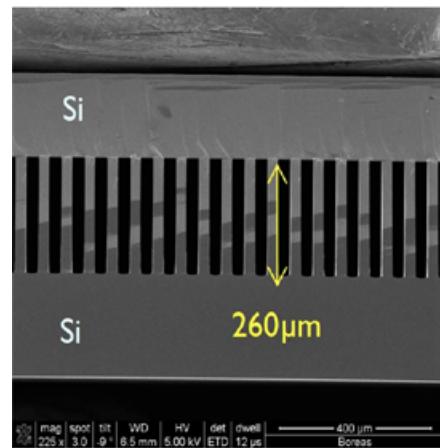


Figure 3: Scanning electron micrograph (SEM) of the high-aspect ratio microchannels.

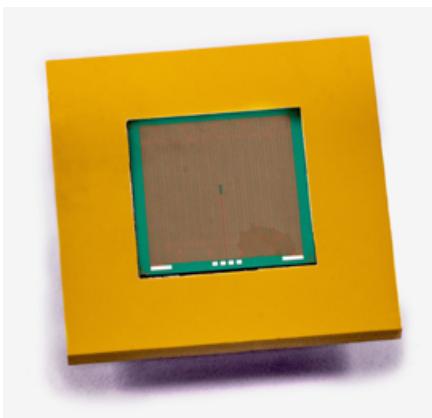


Figure 4: Photograph of imec's Si-based microfluidic heat sink.

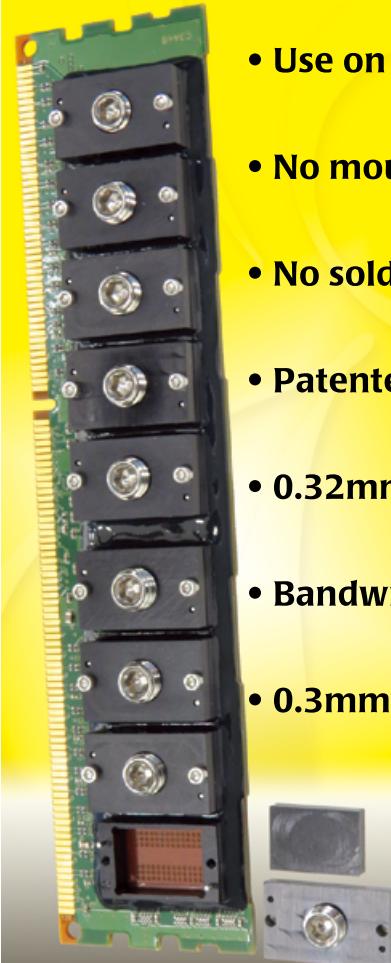
Summary

Imec has proposed a miniature Si-based microfluidics heat sink demonstrating thermal power dissipation of over 600W/cm^2 . The thermal performance of the fabricated devices compares favorably to microelectronics coolers presented in literature. At the heart of the device are small, parallel high-aspect ratio microchannel structures, fabricated with CMOS-compatible fabrication processes, thereby ensuring low-cost final devices. An important asset of the proposed solution is the ability to accurately predict and optimize the fluidic performance and thermal behavior prior to chip design and fabrication. This allows the solution to be easily tuned according to the requirements and restrictions imposed by the application, in terms of, for example, available space or liquid supply.

The new cooling approach can potentially meet the heat challenge that faces the new generation of power electronics, sensors and high-performing devices in a variety of systems. The proposed solution is expected to enable applications beyond the microelectronics industry.

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Biography

Philippe Soussan is a Program Director within the sense & actuate unit of imec, Leuven, Belgium. His field of expertise covers the interaction between processes and material properties, as well as wafer-scale technology integration in the field of multi-physics devices, this comprises: 3D interconnects, micro-fluidics and lately, integrated photonics. Philippe has authored or coauthored more than 130 publications and owns more than 15 patents. Email Philippe.Soussan@imec.be

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GUEST EDITORIAL



Why should we have industry standards?

By Cristina Chu [*Energetiq Technology, Inc.*]

Why should we have industry standards? Consider that the development of standards requires a company to invest the time of their key technology leaders. In this process, a team of volunteer members share market knowledge, leveling the playing field, making fair competition possible and establishing a vector for the market that captures the voice of the customer. In this article, I investigate the market conditions provoking the development of the panel-level packaging standard SEMI 3D20—an effort in which I participated starting with its kick-off in July 2017. The standard was published in its first version in July 2019.

Market conditions

In September 2016, TSMC made semiconductor industry history with the announcement of shipments of the Apple A10 application processor for the iPhone 7. TSMC disrupted the electronics market by demonstrating how a billion-dollar investment in advanced packaging technology could deliver performance improvements and a thinner solution than standard packaging technology for a new semiconductor node. By 2017, TSMC exceeded 50% market share in fan-out technologies and doubled the total available market size. It introduced a capacity of 100,000 wafers per month for its InFO packages, a high-density fan-out wafer-level packaging (FOWLP) solution, and demonstrated that fan out could be a growing and sustainable market. Previously, the market was focused on the standard density FOWLP solutions.

IBS shows how the cost of designing a single chip at an advanced node has become increasingly expensive throughout time, growing from \$50M at 28nm, to \$57M at 22nm, to almost \$100M at 16nm (**Figure 1**). Manufacturers are no longer

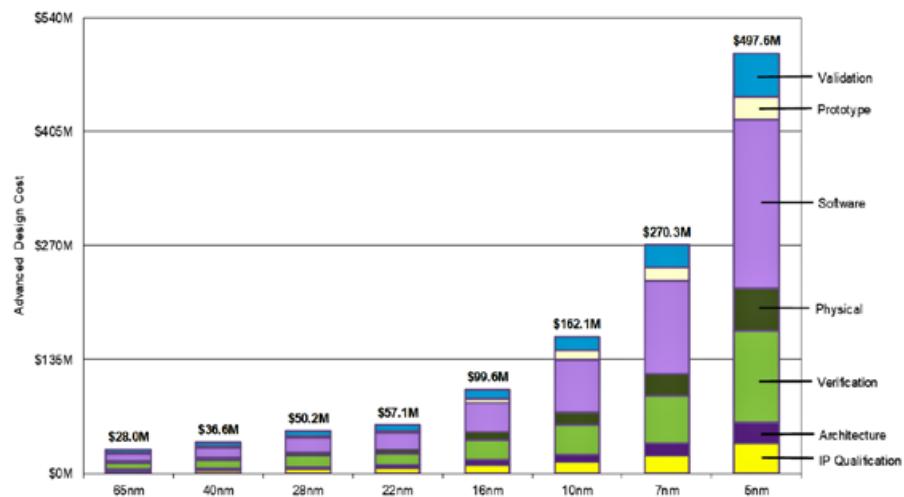


Figure 1: IC design costs escalate. SOURCE: IBS, Inc., August 2019

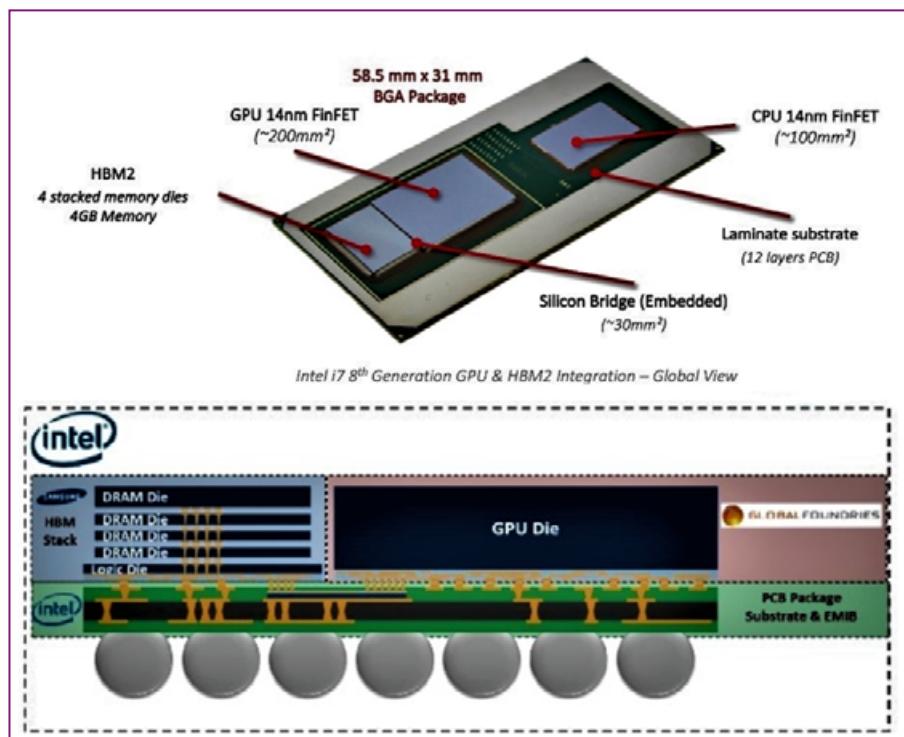


Figure 2: Intel i7 8th generation CPU, GPU and HBM memory on a single package using Intel's embedded multi-die interconnect bridge (EMIB). SOURCES: Intel Core i7-8809G with EMIB report; System Plus Consulting, 2018; Substrate Giants Awakening Yole Développement, 2019 www.i-micronews.com

investing in more advanced nodes as a matter of course. In August 2018, GLOBALFOUNDRIES announced that it would put its 7nm node investments on hold. At more advanced nodes, fewer customers can afford designing everything onto a single die. GLOBALFOUNDRIES shifted its investments towards innovations at existing geometries, extending its current node capabilities.

the nodes and the Chinese government is investing in SMIC to do so as well.”

Heterogeneous packaging, such as shown in System Plus Consulting’s tear down of the Intel Core i7-8809G (see Figure 2), can capitalize on integrating chips made at various nodes, so that investments are targeted where performance is compulsory. Customers can choose to design a 28nm stacked memory and connect it to a 14nm processor on a silicon interposer, or even a

markets traditionally served by outsourced semiconductor assembly and test suppliers (OSATS) and wafer-level packaging houses. This is clearly visible in the graphic representation Yole Développement has made of the spaces in which substrate suppliers and OSATS are working, most notably with respect to redistribution layer (RDL) line/space (L/S) dimensions between 1μm and 20μm (see Figure 3).

Since TSMC demonstrated that advanced packaging innovations could be implemented at a fraction of the cost of front-end design developments with significant benefits in both performance and cost savings, the fabless players and integrated device manufacturers (IDMs) are diving further into all aspects of BEOL design, including advanced packaging design. The result has been that the OSATS and substrate suppliers are battling it out against the backdrop of heterogeneous packaging at wafer- and panel-scales as the supply chain is squeezed and wafer-level precision begins to be demanded on PCB substrates, as well as at the wafer level (Figure 4).

The increased rise in global consolidations has made standards indispensable. There are fewer semiconductor end customers and fewer suppliers. SEMI member companies often face a dilemma: acquire their peers, or be acquired. Concurrently, suppliers have fewer potential customers. Suppliers who don’t thoroughly understand market requirements and dilute their investments in custom solutions will simply be unable to maintain the gross margins necessary to sustain profitability.

Interdependence between end customers and suppliers has become greater. Some end customers acquire key suppliers in order to secure their mindshare and ensure their ability to drive the supplier’s strategic development. One example is the U.S. smartphone chipmaker Qualcomm Technologies, Inc., joint venture with TDK Epcos Corporation, which was initially held under the name RF360 Holdings. Qualcomm depended heavily on RF360 to supply the RF filters that Qualcomm needed to enable 4G and 5G technologies. By acquiring RF360 in its entirety, Qualcomm could focus the groups’ work on developing products that supported Qualcomm, rather than Qualcomm’s competitors. Moreover, the acquisition would allow the company

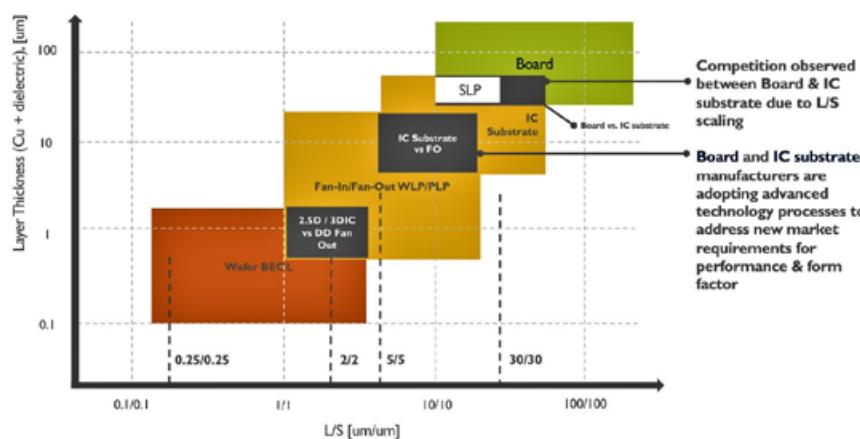


Figure 3: Substrates' landscape. SOURCES: Status of the Advanced Substrates report, Yole Développement, 2019; Substrate Giants Awakening Yole Développement, 2019 www.i-micronews.com

Like TSMC, GLOBALFOUNDRIES also seems to see advanced packaging as an opportunity to improve performance and differentiate its products and services at a fraction of the cost of introducing a new node. Jan Vardaman, of TechSearch International, Inc., discussed the strategic opportunities that advanced packaging provides end customers at SEMI’s Marketing Symposium at SEMICON West (San Francisco, CA, 2019): “As the industry moves to the next silicon nodes ($\leq 7\text{nm}$, etc.) on-package integration is needed to achieve the economic advantages that were previously met with silicon scaling.” Vardaman further noted that TSMC’s investment in packaging was related to its ability to capitalize on foundry business. Though silicon scaling becomes less affordable, a select few push forward in conjunction with packaging opportunities. Moreover, in his article, “Big Trouble at 3 nm,” *Semiconductor Engineering* Editor, Mark LaPedus explains that, “Samsung and TSMC will continue to pursue IC scaling at 5nm and 3nm and beyond, while Intel continues moving down

printed circuit board (PCB) package. Today, the challenges in advanced packaging are that there are too many options rather than not enough. When there are too many options, wasted development efforts can dilute the adoption of cost-effective new technologies. This is where it is critical for the SEMI trade association and the leading manufacturers to work together to direct the industry to more aggressively develop standards so that the industry makes a holistic decision, across the entire supply chain, to develop their products most efficiently. A company that participates in standards definition gains the market understanding that makes possible confident and informed decision making to deliver more competitive products to market.

Advanced packaging makes it possible to innovate at the chip, package and PCB level. End customers have seen that innovation that takes place further towards the back end of the line (BEOL) can be significantly more cost effective than node scaling. As a result, PCB substrate suppliers are now pushing the limits of their capabilities and entering the

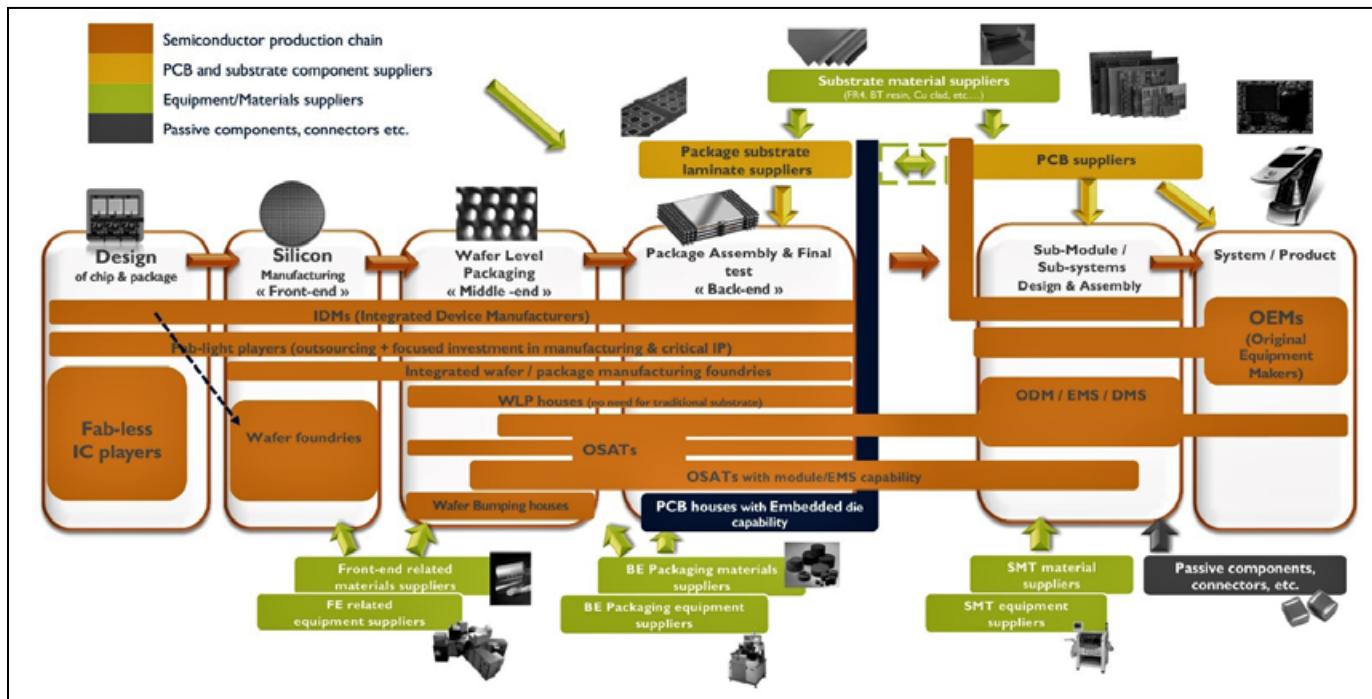


Figure 4: Semiconductor supply chain – 2020. SOURCES: Status of the Advanced Packaging Industry report, Yole Développement, 2019; Status of the Advanced Packaging Industry Yole Développement, 2018 www.i-micronews.com

to diversify beyond smartphones to other industries that required interconnectivity, such as automotive and robotics.

Another example of vertical integration can pertain to acquisitions intended to minimize risk of access to materials in high demand and/or short supply. The semiconductor power market holds enormous potential to supply clean energy and increased efficiency across several applications, from electric batteries in automotive to industrial solar inverters. However, the supply constraints can affect the abilities of the players in these industry segments to deliver new technologies. In order to offset these risks, Swiss STMicroelectronics invested in Norstel, a Swedish supplier of silicon carbide substrates. The semiconductor automotive and industrial market leader's (i.e., STMicroelectronics), investment will help secure ST's competitive advantages in a growing market in which prices may skyrocket in response to a material shortage.

Standards definition process

In the case of the SEMI 3D20 standard, the industry desperately needed consensus on the dimensions of panel processing at a minimum for

the technology to enter true volume production. When we kicked off the standard, Richard Allen from the National Institute of Standards and Technology (NIST) and I did a survey to see the range of different panel sizes under consideration. We had the benefit of participation and knowledge from experienced players in panel processing, such as Tanja

Braun, PhD, who had already done a similar survey a few years earlier and was actively driving panel processing for research purposes at Fraunhofer IZM in Berlin. In **Table 1**, Vardaman captured the different sized substrate dimensions under consideration in 2019 in TechSearch's "Flip Chip and WLP Report: Market Forecasts and Technology Analysis."

Company	Chip First or Last	Process	Panel Size (mm x mm)	Production Status
ASE (one layer coreless ETS)	Chip-last	Face-down	510 x 410	Production
ASE and Deca Technologies	Chip-first	Face-up	600 x 600	Development
China Wafer Level CSP	Chip-first	Face-down	300 x 300	Production
Nepes (nPLP)	Chip-first	Face-down	600 x 600, to 650 x 650	Production demonstrated
PTI (ePLP®)	Chip-first, and chip-last	Face-down	510 x 515	Qualified
Samsung/SEMCO (FOPLP)	Chip-first	Face-down	Three sizes, inc. 415 x 510 and up to 600 x 600	Production
Unimicron (based on touch panel display line)	Chip-last	Face-down	370 x 470; 510 x 515	Development

Table 1: FOWLP panel activities. SOURCE: TechSearch International, Inc.

We also had the infrastructure of SEMI standards and sponsorship from SEMI employees James Amano, Senior Director of International Standards, as well as extensive support from Senior Coordinator of International Standards, Laura Nguyen. For months, we gathered a long list of potential characteristics we could add to the standard. We hoped to drive a single size, but consensus among the task force was not possible. Instead, we settled for two sizes in the interest of narrowing down from more than five potential choices. We decided to keep these characteristics separate from the requirements of the standard because consensus would take too long and delay the most critical parameters that were higher priority. Now, this growing laundry list of additional parameters has become a source from which to pull the highest priority requirements into the specification. Some of these

parameters include initial panel thickness, final panel thickness, maximum panel mass, initial panel material, maximum panel warpage, in addition to ID marking, orientation and corner conditions.

Collaboration has been extensive across a global team. There are related standards, such as those being developed for FOUP and Loadports, and many more. Sometimes parameters are high priority because a sister standard requires definition from our substrate standard in order to make progress.

Some companies, however, don't want to make the investment. These companies may not contribute at all to the standards because they are apprehensive about sharing market know how. Other companies may make minimal investments, sending someone with limited knowledge of the topic, who will report back to the team what's going on, but won't make significant technical contributions to the standard. These companies will not have the opportunity to shape the direction in which the market will go and will not benefit from the chance to be first to market.

On the other hand, when companies send their best leaders, the company has the potential to lead the industry and determine the direction in which the technology will develop. For example, Intel's participation in the standards development process was critical—Stefan Radloff, Technologist, provided valuable guidance, such as the dimensional direction and phases of the standard. The return on investment can be significant. It takes more than just sending the best leaders to represent the industry in standards — it's also imperative that contributors are objective. Standards are not only about what is beneficial to a single player. These leaders must have the capability of understanding what is beneficial for the industry at large, not only for the company they represent. Some end customers would prefer to leave standards as wide open as possible, so they have the freedom to develop a broad range of process solutions without having to limit themselves in any way. This situation, however, is not beneficial to the industry. It promotes waste, forces suppliers to build custom solutions and limits the ability of smaller suppliers to grow because they can't survive to compete effectively with larger players.

A standard in and of itself does not limit competitiveness. If anything, a standard allows the industry to focus on bringing the innovations of suppliers to serve end customers' goals with minimal risk. Suppliers can accelerate their delivery of solutions that will serve their customers needs because they are not wasting their efforts bringing product developments to market that will never align with industry requirements. Creating standards that strive to benefit the whole industry gives end users an array of suppliers from which to choose and also gives suppliers the ability to invest more efficiently and compete more successfully for opportunities by bringing solutions to market that will meet industry requirements.

Biography

Cristina Chu is VP of Product Marketing at Energetiq Technology, Inc., Wilmington, MA, USA. Energetiq products deliver high brightness laser-driven light sources for a range of applications including etch, metrology and EUV lithography equipment. Chu has held leadership positions in the SEMI Standards Program and worked in advanced packaging equipment sales and marketing at ASMPT, TEL and NEXX. Chu has a Master in Architecture from Harvard University and a BA as a Senior Fellow from Dartmouth College. Email cchu@energetiq.com

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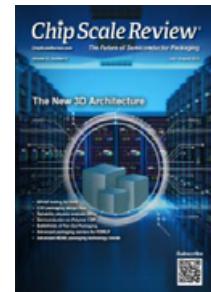
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Choon Heung Lee, Ph.D.
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The semiconductor industry and market is experiencing many changes that differ from the past. Changes in the last 5 years include many concentrated M&As and an inflection point that is occurring with connectivity to everything and everywhere. In terms of packaging technology, fundamental processes and materials linking most advanced packaging technologies have been well established. On the other hand, specific advanced technologies require an unprecedented level of scale in CAPEX investment and proper expertise in engineering and operations. In this talk, I will map these changes and share the challenges facing OSATs. I will present my view on how OSATs can adjust to these changes and move in the best direction.

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Wednesday, October 23, 2019 | 8:15am
Slowdown: When Did it Start... What Drove it... When Will the Recovery Come



VLSIresearch

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By early 2018, it was clear to VLSIresearch that the end of the boom was near and that 2019 would be bad. Many of its indicators had been raising red flags since late 2017. This alarm was reflected each week in VLSI's Weather Reports, which were seen by the thousands who subscribe to SemiWEEK, plus more in its other reports. Still growth would stay positive while the industry partied through 2018. However, while positive, growth was clearly slowing. In this presentation, we'll show the data that revealed a clear growth peak around December of 2017, and how it started a steady decline that continued through 2018. By January of 2018, it was clear the party was over, even though no other major market research firm would forecast a negative year until it was well under way.

As the year has progressed, key pressure fronts for an industry recovery reached the outer cyclical boundaries and started to reverse course. The question is, when will we be back in a growth cycle? Will it be a "V" or "Canoe" shape? The presentation will highlight the factors that will likely determine the future course.

Some of the questions to be addressed in the presentation include:

- What are the pressure and strategic inflection points?
- What's different about the cycle today?
- The effect of a slowing in Moore's Law

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Wednesday, October 23, 2019 | 4:00pm
A Borderless Future for Electronic Interconnect



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Tim Olson
 Founder & CTO

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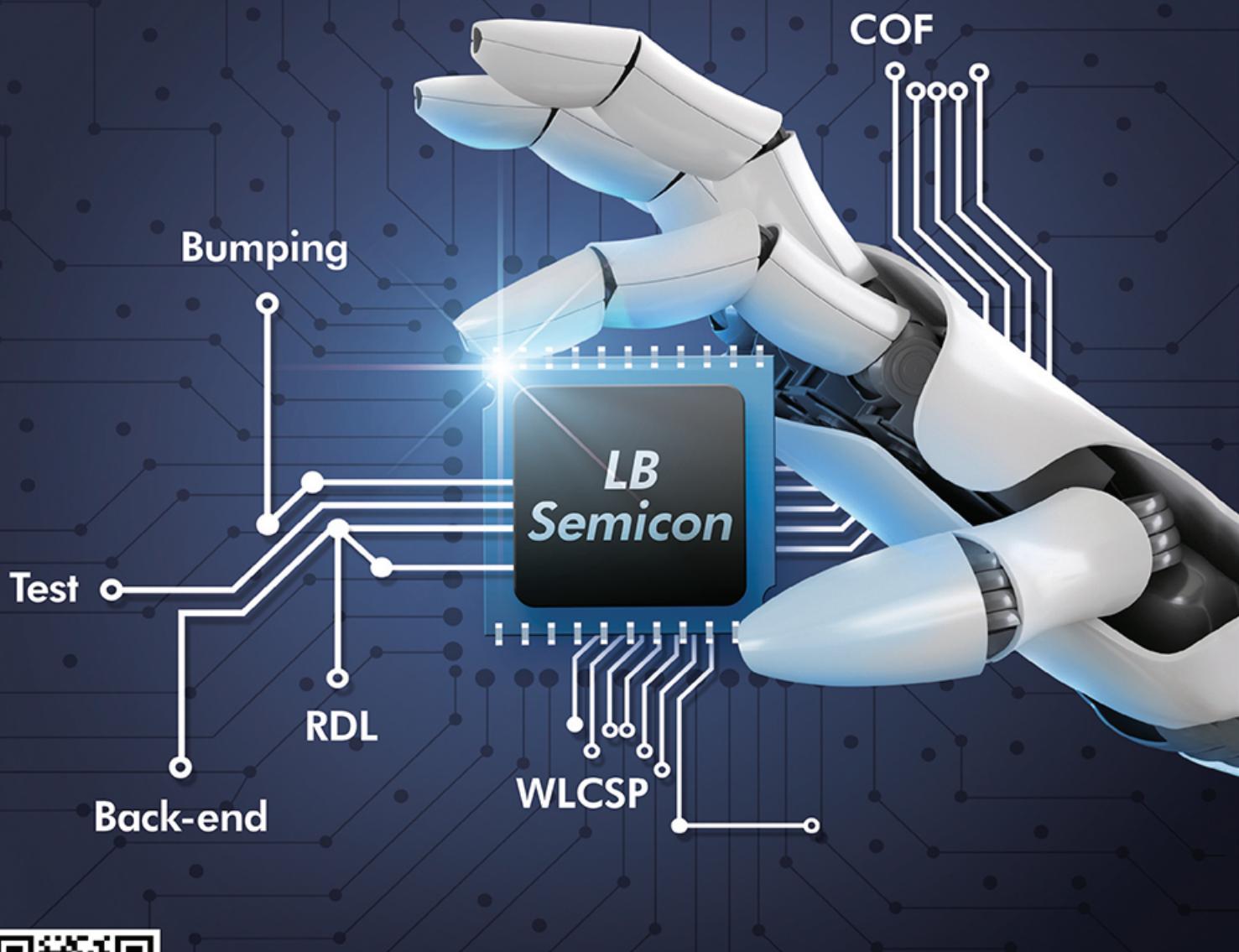
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