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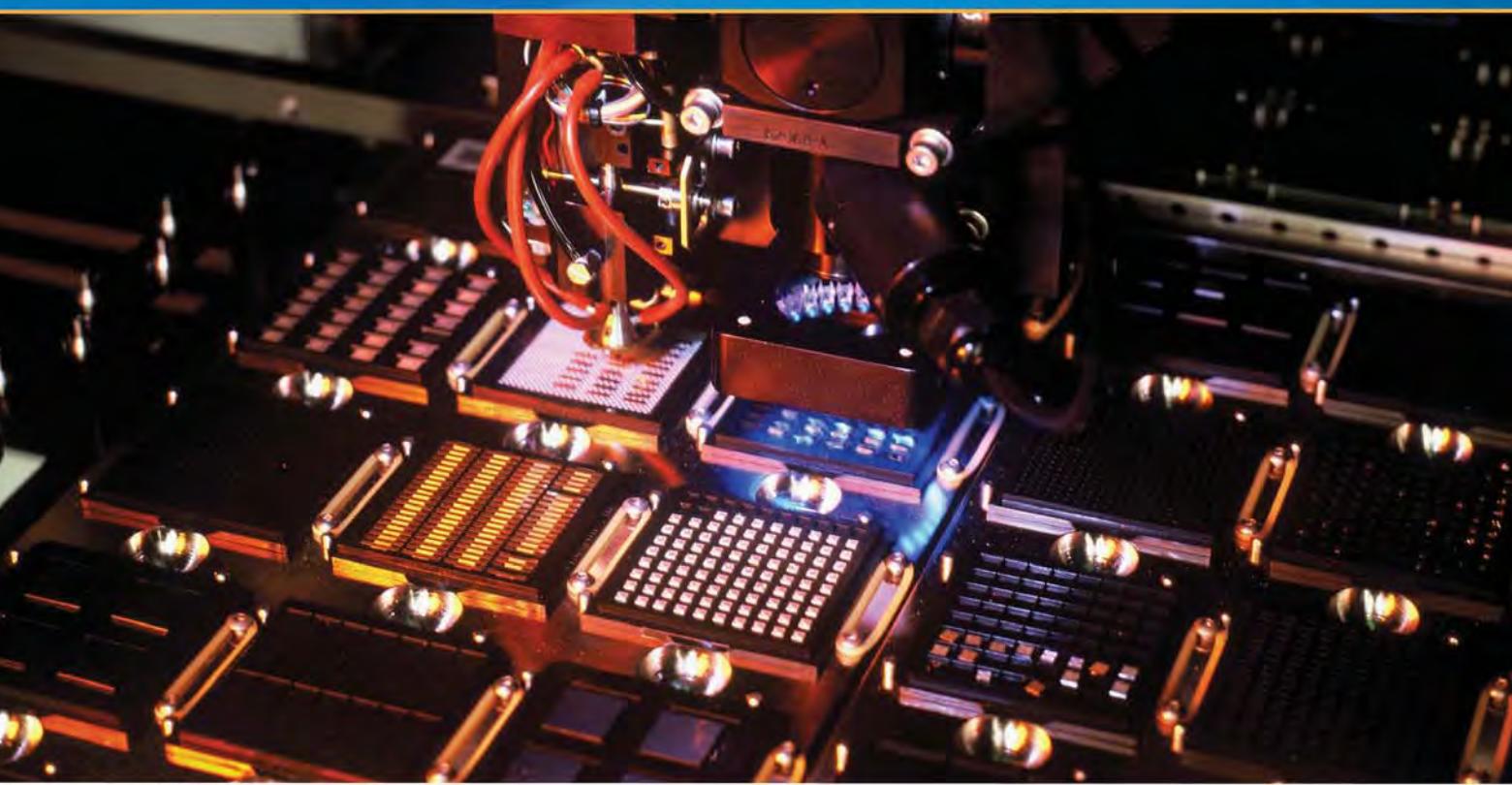
*The International Magazine for the Semiconductor Packaging Industry*

Volume 14, Number 5

September-October 2010



- Aerosol Jet Interconnect
- Flip Chip Die Bonding for 3D ICs
- WLCSP Drop Test Reliability and Design
- The Ever Changing Photovoltaic Landscape
- International Directory of Wafer Scribing and Dicing Systems



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# CONTENTS

Sept-Oct 2010

Volume 14, Number 5



This edition's cover features an inside view of SET's FC300 Automated High Force Die / Flip Chip Bonder for automated handling of chips and substrates up to 100 mm from waffle packs. With  $\pm 0.5 \mu\text{m}$  post bond accuracy and 20 microradians leveling, the SET FC300 offers the latest evolutions in bonding techniques. The article "Flip Chip Die Bonding for 3D IC Integration" explores some of the new challenges, advantages, and options.

Courtesy of Smart Equipment Technology SAS,  
Saint Jeoire - France.

## Chip Scale REVIEW

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging  
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,  
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

### FEATURE ARTICLES

<b>Flip Chip Die Bonding for 3D IC Integration</b>	<b>14</b>
Keith A. Cooper, Michael D. Stead <i>SET-North America</i> , Gilbert Lecarpentier, Jean-Stephane Mottet, <i>SET-SAS</i>	
<b>Jetting Your Way to Fine-pitch 3D Interconnects</b>	<b>18</b>
Mike O'Reilly, <i>Optomec, Inc.</i> , Jeff Leal, <i>Vertical Circuits Inc.</i>	
<b>Drop Test Reliability and Design of Wafer-Level Chip Scale Packages</b>	<b>22</b>
Yong Liu, Stephen Martin, <i>Fairchild Semiconductor Corp.</i> , Luke England, <i>Micron Technology</i>	
<b>3D IC Integration with TSV Interposers for High Performance Applications</b>	<b>26</b>
John H. Lau, <i>ITRI</i> , and Y. S. Chan and S. W. Ricky <i>Hong Kong University of Science and Technology</i>	
<b>Wafer Scribing &amp; Dicing ... Which Method? Equipment?</b>	<b>30</b>
Gil Olachea, <i>Az Tech Direct, LLC</i>	

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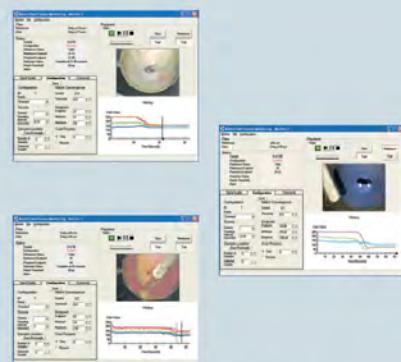
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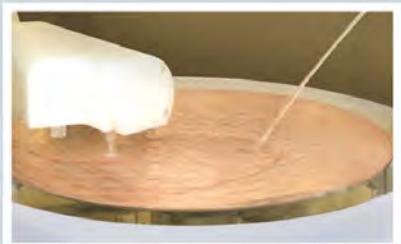


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**FEATURE ARTICLES**

- The Ever Changing PV Landscape** An overview of worldwide PV production, new technologies and market demand. **36**  
 Bob Klenke, *ITM Marketing*

**DEPARTMENTS**

<b>From the Publisher</b>	<b>Forecasting ... We all do it! Year End 2010 and Forecasting into 2011...</b>	<b>6</b>
Kim Newman, <i>Chip Scale Review</i>		
<b>Editor's Outlook 1 + 1 = 3</b>		<b>8</b>
Ron Edgar, Technical Editor, <i>Chip Scale Review</i>		
<b>Industry News</b>		<b>10</b>
<b>2010 International Directory of Wafer Scribing and Dicing Systems</b>		<b>32</b>
Ron Molnar <i>Az Tech Direct</i>		
<b>Emerging Trends A Good Place to Place Your Bets (in ICs)</b>		<b>41</b>
Sandra Winkler, Senior Analyst <i>New Venture Research</i>		
<b>What's New!</b>		<b>42</b>
<b>Market Forecast</b> Walker's September Forecast: Recovery, Boom, Growth, What's Next?		<b>44</b>
Françoise von Trapp, Contributing Editor, <i>3D InCites Group, LLC</i>		
<b>Product Showcase</b>		<b>47</b>
<b>Advertiser Index, Advertising Sales, Calendar</b>		<b>48</b>

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# FROM THE PUBLISHER



## Forecasting ... We all do it! Year End 2010 and Forecasting into 2011...

**P**ositive and optimistic industry trends were evident at SEMICON West 2010, with these trends visible as well in our July/August issue of Chip Scale Review (CSR). Both the editorial content and corporate advertising were expanded in the issue, as progressive companies took action to capitalize on the upturn and promote their products, services, and new technologies. SEMICON West 2010 and corporate 3rd Quarter, 2010 financial reports are history. Let's look to the future.

This is the time of year when industry experts and amateurs alike look back and then forward attempting to forecast the 2011 industry trends. Forecast information, regardless of its in-house or industry source, drives all levels of corporate resource planning, capital equipment procurement, and marketing budgets. Following the significant 2009 industry downturn and somewhat amazing 2010 upturn, forecasts are exhibiting much broader variability than in recent years. This wide range of forecast estimates may actually lead to "corporate indecision" regarding the 2011 outlook and slow down the positive industry momentum.

Decisions for 2011 will be critical, and although CSR isn't in the business of professional forecasting, nor is my phone ringing off the hook with execs soliciting my advice, I'm happy to share my perspective of the industry with you based on my discussions with a significant number of industry professionals. One thing is certain – corporate productivity is at or near a record level in 2010! Companies have increased their sales and bottom lines by doing more with fewer people. They have been slow to resume hiring in 2010 following their 2008 and 2009 reductions in staff. A major decision facing many companies is whether to increase staffing or continue to "stretch" their resources further in 2011.

Global economics, inventory levels, buying trends, and many other important factors influence the forecast accuracy of future performance. Market forecasting may not be one of your job responsibilities, however, I venture to say it enters into many of your daily decisions. Let me give you a few data points to help you with some of your decision-making: (1) Both MEPTEC and SMTA report increased advance registration for their Medical Electronics Symposium in September, (2) SMTA and CSR staff both see increased attendee and exhibitor registrations for their International Wafer-Level Packaging Conference (IWLPC) in October, and (3) exceptional editorial content and comprehensive supplier directories in CSR continue to attract new advertisers.

I appreciate that you have taken the time to read this letter, as it offers me the opportunity to convey my personal take on the health of our industry. There's still one more quarter remaining before we "close the books" on 2010. Information to review! Meetings to attend! Decisions to make! Give me a call if you can use my insight (advice at no charge) as we all strive to make our numbers and await the final accounting reports on our sales and earnings figures for the year.

I look forward to meeting many of you at the upcoming IWLPC event in Santa Clara, CA where we can discuss each other's views of the industry forecasts. We have one more issue to publish before year end, so I'd appreciate any comments and feedback you have regarding the publication. 

*Kim Newman*  
Publisher

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# EDITOR'S OUTLOOK



## 1 + 1 = 3

By Ron Edgar [[redgar@chipscalereview.com](mailto:redgar@chipscalereview.com)]

I admit it — I've finally lost my marbles! How can one plus one equal three? According to the rules of arithmetic, that is just not possible. How can the result be greater than the sum of the parts? New math? Fuzzy logic? Or just plain wrong? None of the above, and here's why.

The simple truth is, sometimes we have to break the rules. Suppose I want to build a better mousetrap. I disappear into my lab and a long time later I emerge with a new device. But no one can mass-produce the materials, the device is too costly to build, and someone else has already made something better. But if I had got together with some like-minded people, we could have cooperated on the design. After basic agreement on the device, we could each use our specialties to develop a piece of the device. We could agree on standards to make the device and, in the end, we produce a product that is well made, can be manufactured cost effectively, and fills a major need. So cooperation plus standardization = well made, cost effective, and wide appeal; or  $1 + 1 = 3$ .

An interesting example comes in a 2008 article by Professor Ruth Taplin of the London School of Economics where she is the Director of the Centre for Japanese and East Asian Studies. Her article, *The Taiwan Model for Patenting Nanotechnology*, discusses how the Taiwanese government is pouring money into basic research on next-generation IC memory. "This funding will be shared between the basic research supervisor National Science Council (NSC), including the Nano Device Laboratory

(NDL) and the Industrial Technology Research Institute (ITRI)." She goes on to say, "ITRI's research funding will be focused on industrialization of technology. The institute is developing nanotechnology platforms to produce high standard results through cooperation between related industries, academics and research centres." Again,  $1 + 1 = 3$ .

The costs associated with cutting-edge technology development is astronomic. Frequently this cost is much more than any single company can afford. Also, the range of skills required is so diverse that it is unlikely to live under one roof. The cost effective answer? Cooperation and standardization.

Industry organizations such as IPC and JEDEC are the core of global standardization. IPC "is a Global trade association dedicated to the competitive excellence and financial success of its 2,700 member companies which represent all facets of the electronic interconnect industry, including design, printed circuit board manufacturing, and electronics assembly. IPC is an ANSI-accredited standards developer (which brings us to ANSI, another huge source of standardization). JEDEC, Joint Electron Devices Engineering Council, now known as JEDEC Solid State Technology Association, is an independent semiconductor engineering trade organization and standardization body with over 300 members, including some of the world's largest companies. It is associated with Electronic Industries Alliance (EIA) another trade organization that represents all areas of the electronics industry in the USA. The Global

Semiconductor Alliance (GSA)'s stated mission is "to accelerate the growth and increase the return on invested capital of the global semiconductor industry by fostering a more effective fabless ecosystem through collaboration, integration and innovation."

The cooperation, standardization, and communication fostered by these and other industry groups are the nuts and bolts that hold together a substantial portion of our industry. They ensure that a wafer made in one place can be processed in another. They ensure that components made all over the world can be brought together and successfully assembled into a product. They ensure that different products can "talk" to each other.

One might think that sharing ideas is bad for the bottom line. Quite the opposite. Industry cooperation and standardization has led to better products, lower cost, faster time to market, and better ROI. True, your special piece of IP that differentiates your product and allows you to compete is critical, but for the most part, the bulk of all products are built with standard parts to standard specifications. Truly, the result is greater than the sum of the parts;  $1 + 1 = 3$ .

International Wafer-Level Packaging Conference (IW LPC) is almost with us (October 11-14, 2010, Santa Clara Marriott Hotel, Santa Clara, CA, USA. IW LPC is jointly sponsored by SMTA and this magazine and "explores cutting edge topics in wafer-level packaging and IC/MEMS/MOEMS packaging, including 3D/Stacked/CSP/SiP/SoP and mixed technology packages." In his message,

Andrew Strandjord of Pac Tech USA, Conference General Chair, says, "The objective of the IWLPC is to provide a unique venue that brings together scientists, engineers, academia, manufacturing, and business people from around the world to present and debate some of the latest and hottest packaging technologies." Be sure to go to [www.iwlpc.com](http://www.iwlpc.com) for more information on how to attend and what is offered in the many presentation sessions. IWLPC has become one of the premier venues in our industry and a unique opportunity to rub shoulders with the movers and shakers from the thinkers and imagineers (thank you Disney) to the companies that make the dreams come true.

This edition we have another directory for you. Our previous offerings have proven hugely popular and useful and we hope you find this likewise. Ron Molnar, Az Tech Direct, has prepared our *2010 International Directory of Wafer Scribing and Dicing Systems*.

We have a fine set of articles this edition. *Jetting Your Way to Fine-pitch 3D Interconnects* is a fascinating look at the current state of TSV, wire-bond, and, yes, aerosol jet printing. Check it out! This is really interesting stuff from Mike O'Reilly of Optomec, Inc., and Jeff Leal of Vertical Circuits, Inc. A studious review of *Flip-Chip Die Bonding for 3D IC Integration* with focus on "technically effective and manufacturable processes" is presented by Keith Cooper and Michael Stead of SET-North America and Gilbert Lecarpentier and Jean-Stephane Mottet of SET-SAS. There is a lot of good detail in this article and well worth wading through. A collaborative article between Yong Liu and Stephen Martin of Fairchild Semiconductor and Luke England of Micron explores the *DropTest Reliability and Design of Wafer-Level Chip-Scale Packages*. The results of this study are presented showing corroboration between the modeling and the actual drop tests. Our business article, written by long-time friend and contributor Bob Klenke of ITM Marketing looks at *The Ever*

*Changing Photovoltaic Landscape* and is an overview of the worldwide PV production, new technologies, and market demand. Sandra Winkler, in her regular column, *Emerging Trends*, is looking for *A Good Place to Place Your Bets (in ICs)*.

We have our regular columns, *What's New* and an expanded *Industry News*. We hope everyone finds something interesting and useful in this edition. 'Till we meet again. Oh, don't forget,  $1 + 1 = 3$ .<sup>SP</sup>



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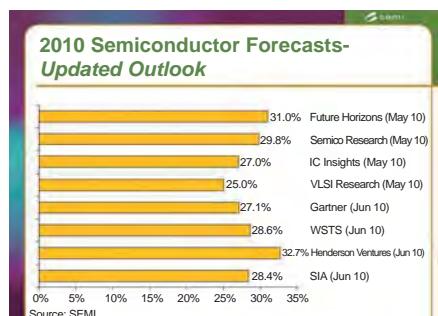


# INDUSTRY NEWS

## From SEMICON West: A Positive Outlook

"This is an exciting time as the industry begins its recovery," noted SEMI's Jonathan Davis in his opening remarks at SEMICON West's annual press conference in July. "I want to savor this moment, I don't know how many times I'll get to stand up here and say the market is going to double this year."

Stan Myers, president and CEO of SEMI offered equally encouraging news, noting that the latest versions of semiconductor forecaster reports indicate an average expected growth rate of 38.7% (**Figure 1**). Offering as a reference point, the January 2010 forecast of 14.9% growth, Myers said the recent predictions are "fairly impressive" and expect to see bigger numbers moving forward. "Growth has been consistently positive since April of 2009," said Myers, "demand for semiconductors has clearly recovered from recent market declines."



2010 Semiconductor Forecast outlooks as of July, 2010. (Source: SEMI)

Myers cited market drivers such as ongoing recovery in economy, (although concerns with debt, unemployment and economic growth in the second half of 2010 remain), the electronics market growth, improved fab utilization and firm average selling prices. He also pointed to 11 months of book-to-bill ratio being above parity as another positive indicator. Japan is experiencing similar growth in the semiconductor equipment market. "Recovery is active in all major semiconductor manufacturing markets; the difference is to what degree," said Myers.

Amidst all the celebrating, Myers did express some concern about investment

in innovation, which he says is needed for continued growth. His concern is that there isn't enough investment to maintain innovative approaches, although North America continues to invest in advanced technologies, and in Europe, a reported \$5B per year will be spent on semiconductor equipment and materials in both 2010 and 2011.

With regard to SEMICON West itself, event organizers reported an increase in just about everything over 2009. The final combined attendance (visitors and exhibitors) for SEMICON West and Intersolar North America grew 17% to 29,423, with verified visitors rising 9% to 19,423. Visitor interest between the shows was 68% for both SEMICON West and Intersolar, 16% for SEMICON-only, and 16% for Intersolar-only. Technical sessions at the TechSITE, TechXPOT, and Extreme Electronics show floor stages, as well as main stage keynotes and executive panel sessions were reported to be standing-room only. Additionally, the premiere of Virtual SEMICON West online companion event reportedly attracted nearly 700 "virtual" attendees as of August 24, most of whom were not able to attend the live show.

## SEMI Reorganizes, Makes Management Changes

In August, SEMI announced a reorganization into three dedicated business units for IC manufacturing, photovoltaic (PV), and Emerging and Adjacent Markets. As part of this, Karen Savala succeeds Jonathan Davis as president of SEMI North America, and Davis will assume the new position, president of the Semiconductor IC Business Unit.

The reorganization is the result of a year-long review and analysis by SEMI's board of directors to achieve better accountability and improved member service in the primary market areas of semiconductor ICs, PV solar, and related markets such as high-brightness LEDs, MEMS/MST, and printed and flexible electronics. The three new business units

will be responsible for developing and delivering member services on a global basis through SEMI regional offices based in China, Europe, India, Japan, Korea, North America, Russia, Taiwan and Singapore.

"While all these areas share a common process technology base and need for effective supply chain collaboration, these changes are intended to enable more responsive and specialized products, services and leadership in the multiple industries that SEMI members now serve," said Stanley Myers, president and CEO of SEMI.

In addition to Davis and Savala's changing roles, Tom Morrow will direct the activities of the Emerging and Adjacent Markets Business Unit, in addition to his duties as V.P. of Global Expositions and chief marketing officer. Dan Martin will continue to lead the PV Group, now recognized as a dedicated SEMI business unit, assisted by Bettina Weiss who will take on new global responsibilities as executive director, PV Group.

## SEMICON Europa 2010 to focus on Nano Innovations

SEMI's lineup of keynote speakers and program highlights for SEMICON Europa 2010, October 19-21, Dresden, Germany will feature all European fabs including GLOBALFOUNDRIES, Infineon, Intel, STMicroelectronics and X-Fab, as well as leading R&D organizations in SEMICON Science Park. Key market segments to be addressed include: semiconductor front-and back-end, MEMS/MST, secondary equipment and advanced packaging.

"SEMICON Europa offers a wide range of programs that address Europe's manufacturing issues and opportunities," said Heinz Kundert, president of SEMI Europe. "This year's event continues the transformation of SEMICON into a manufacturing communication platform through programs put together by committees of industry experts."

In addition to the events' technology conferences, courses, free technology and

standardization sessions, executive and networking events, this year SEMI has expanded co-location opportunities to include the Plastics Electronics Conference, covering topics such as organic electronics, displays, organic photovoltaics, and lighting; The 12th European Manufacturing Test Conference (EMTC); the Advanced Packaging Conference; and the International MEMS/MST Industry Forum.

For more detailed information about keynote speaker addresses, technical programs and short courses, or to register to attend the exposition, please visit [www.semiconeuropia.org](http://www.semiconeuropia.org).

## SEMATECH Completes 300mm Line for Via-Mid 3D ICS



As part of its work in 3D IC integration, SEMATECH's 3D Interconnect program announced that its 300mm 3D IC pilot line is complete and operating at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex. Dedicated to via-mid 3D applications, this development and exploratory platform reportedly includes all processes and test vehicles necessary to demonstrate the viability of via-mid technology in conjunction with advanced CMOS.

Based on  $5 \times 50\mu\text{m}$  TSVs, the processes include TSV formation and metallization, wafer and die alignment, bonding, thinning, and the necessary metrology for these integration sequences. Supported by the conventional CMOS processing capabilities of CNSE, SEMATECH researchers are working jointly with chipmakers, equipment and materials suppliers, and universities on device interactions for fabrication at the 65nm node for planar and future scaling to 30nm for planar and non-planar CMOS technologies.

"Our program provides our members with access to complete 300mm R&D

capability in 3D, allowing them to evaluate tools, process modules and even integration sequences in a realistic setting," explained said Sitaram Arkalgud director of 3D Interconnect at SEMATECH,

adding that the organization plays a strategic role, working with the industry to drive manufacturability and forge consensus on technology options, standards, and cost modeling.

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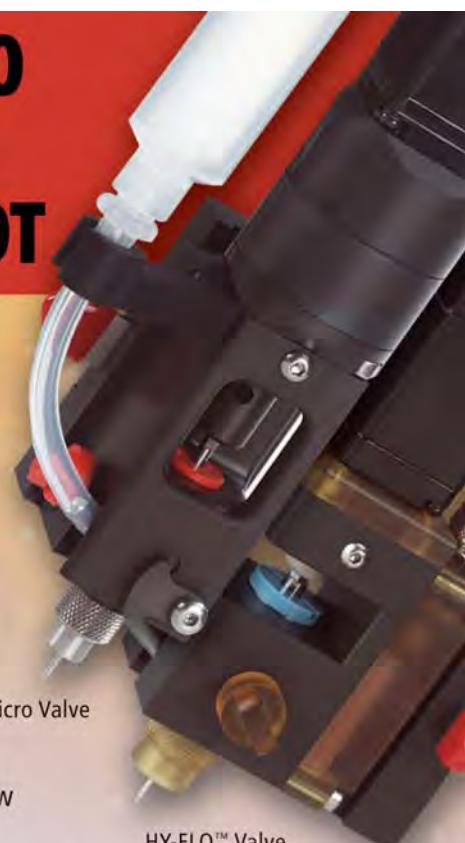
**Feasibility Testing** and  
process verification based on years  
of product engineering, material flow  
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According to Richard Brilla, vice president of strategy, alliances and consortia at CNSE, the integration of this 3D IC pilot line enhances the research and development capabilities at the UAlbany NanoCollege. "This marks another critical step forward in accelerating advanced manufacturing for innovative nanoelectronics technologies," he said.

### **Kulicke & Soffa CEO, Scott Kulicke Retires, Bruno Guilmart Takes the Helm**

Effective September 30, 2010, Scott Kulicke, officially hands over the reins of Kulicke & Soffa (K&S) to Bruno Guilmart, who was elected president and CEO of the company in the wake of the announcement of Kulicke's planned retirement. Kulicke will also retire from the Company's Board of Directors and the Board has elected Guilmart to fill his seat. MacDonell Roehm, an independent director, will remain non-executive Chairman of the Board of Directors.



Bruno Guilmart



Scott Kulicke

Late last year, Kulicke, CEO since 1979, announced his intention to retire no later than June. "Leaving will be difficult. Besides the host of ongoing projects and programs that will make K&S an even better company, I'll miss the talented and dedicated team of K&S employees around the world who have made the company so successful," said Kulicke, in a statement to the press. "The Board conducted a comprehensive search for my successor, considering many strong candidates, both internal and external. Bruno is a great choice. Given his industry experience, his drive and his technology expertise, I am confident in his ability to lead K&S into the future."

According to Roehm, Guilmart has a strong industry track record as CEO,

leading companies in the USA and Asia including Lattice Semiconductor, Unisem Group, and Advanced Interconnect Technologies. "He is uniquely positioned to build on Scott's legacy and extend K&S's leadership position in our industry," he said, adding that he's observed K&S's evolution under Kulicke's leadership over the past 25 years. "The industry in general and K&S in particular will miss Scott's knowledge base and wisdom," said Roehm. "We wish him well during his retirement."

Kulicke will stay with K&S in an advisory capacity to ensure a smooth management transition. Guilmart will reside in Singapore, the center of the K&S' global operations. Other headquarter functions will migrate to Singapore in fiscal 2011.

### **Heraeus Doubles PV Staff; Introduces Pastes Targeting PV**

In response to recent success of its front and back side silver pastes for crystalline Si solar cells, Heraeus has recently taken measures to further increase its presence in the photovoltaics market. Over the past few months, the company has announced capacity expansion at its Photovoltaic (PV) business unit, and more recently doubled its technology staff at the US facility in West Conshohocken, PA. In addition, the PV business unit introduced a new line of front side silver pastes, the SOL9400 Series that reportedly offer improved performance over the company's current product offering.

"The new staff has excellent knowledge of material science, and solid experience in the PV industry. They brought not only new energy but also new ideas to the team. These important additions to our staff will help us expand our product portfolio and grow our technology advantage in the PV paste market," said Dr. Weiming Zhang, VP of technology for Photovoltaic Business Unit. He said the initial feedback from key customers for the SOL9400 has been positive, and that they are particularly impressed with its improved efficiency and faster throughput than its predecessor.

"We continue to innovate, develop new products and customize them for specific

production requirements. As the global solar market continues its rapid growth we believe solar manufacturers will increasingly turn to Heraeus," said Andy London, Global Business Unit Leader for Heraeus PV.

### **DB Design Announces Management Buy-Out**

The management team of Fremont CA based DB Design, supplier of test hardware and interface products, announced it has purchased the company from WELLS-CTI, Inc. The acquisition will reportedly allow the company to focus on its unique market while servicing new and existing customers. Rennie Bowers will focus on operations and engineering, and Mark Stenholm will take charge of sales, marketing and product development.

"We are very excited about the opportunity to bring our vision to DB Design as the new leadership team," notes Stenholm. "After working at DB since the very early days, Rennie and I believe that we can enhance our customer satisfaction while continuing to explore new markets." Adds Bowers: "Purchasing DB Design ensures our continued quality and world-class service."

Serving a broad customer base that includes top semiconductor manufacturers, DB Design specializes in innovative test interface solutions including change kits, stiffeners, docking systems and manipulators. The company will continue its operations in Silicon Valley.

"WELLS-CTI has decided to focus on our core, high growth areas including advanced thermal management," said Matt Bergeron WELLS-CTI CEO. "We wish the new DB team the best of luck and look forward to working with them on future projects."

### **Rudolph Expands Presence in Semiconductor Process Control**

In a move to expand its presence in semiconductor process control, Rudolph Technologies, Inc. has acquired selected assets and IP of the Yield Dynamics software business from MKS Instruments, related to yield management software used by semiconductor manufacturers and

fabless semiconductor suppliers. As part of the acquisition, approximately 35 engineering and applications personnel, most of whom are based in Tianjin, China, will join Rudolph's Data Analysis and Review Business Unit.

As processes become more challenging, manufacturers are becoming more dependent on data management systems to deliver process information analysis designed to automate decision-making and optimize yield. The Yield Dynamics package reportedly includes Genesis? Enterprise software, a fabwide yield management solution that combines parametric and yield optimization in a unified platform with data mining and workflow development across all data sources.

"The products and technology include patented analytical techniques for yield improvement that are complementary to our existing yield management and process control portfolio," stated Mike Plisinski, Rudolph's vice president and general manager, Data Analysis and Review Business Unit. "In addition to the technology, we welcome the China personnel to our growing applications and product development team."

## BITS Workshop 2011: Call for Papers



Planning for the Twelfth Annual Burn-in & Test Socket Workshop (BiTS) is well underway. Organizers of the event, scheduled to take place March 6-9, 2011, at the Hilton Phoenix East in Mesa, AZ, are seeking presentation and poster proposals on a broad range of Test & Burn-in topics to build a strong technical program. Some topic ideas include techniques and technologies that address electrical and mechanical challenges, PCB design and manufacturing challenges, advanced packaging technologies and test process and operational challenges. For a full list of suggested topics visit [www.bitsworkshop.org](http://www.bitsworkshop.org).

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# Flip Chip Die Bonding for 3D IC Integration

By Keith A. Cooper, Michael D. Stead [SET-North America] and Gilbert Lecarpentier, Jean-Stephane Mottet [SET-SAS, ]

**3**D integration has emerged as a prime route to providing higher electrical functionality within smaller spaces. A key attraction for this methodology is shorter interconnection paths by means of chip stacking, creating new types of vertical interconnects that provide direct circuit paths from one chip to another.<sup>1</sup> These direct connections provide higher operating speeds with reduced power consumption and lower overall costs than competing methods. According to market research firm, Yole Développement, 3D integration using through-silicon vias (TSVs) is expected to provide a major growth opportunity for the semiconductor industry (**Figure 1**).

Of course, 3D integration has created a new set of challenges, though many of its core elements and processing steps are based on established front-end unit processes such as lithography, etching, depositions, and the use of various materials and combinations. This article explores solutions in two particular areas: the removal of oxides prior to metal-metal bonding, and the proposal of a collective hybrid bonding method to optimize accuracy and throughput between chip-level or wafer-level bonding methodologies.

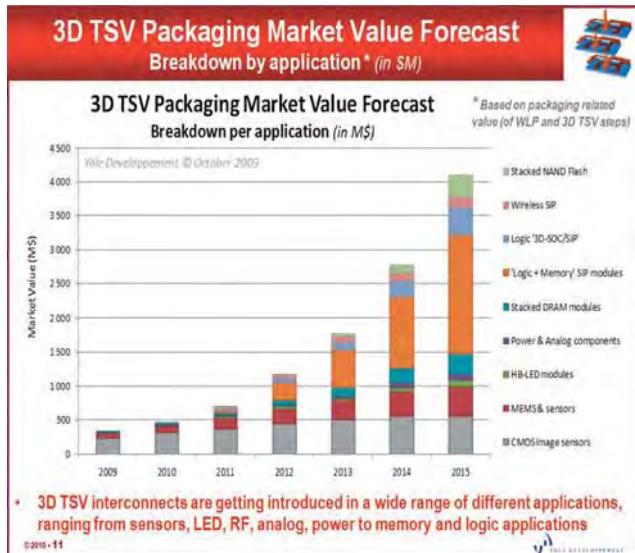


Figure 1. TSV market forecast histogram (courtesy of Yole Développement),

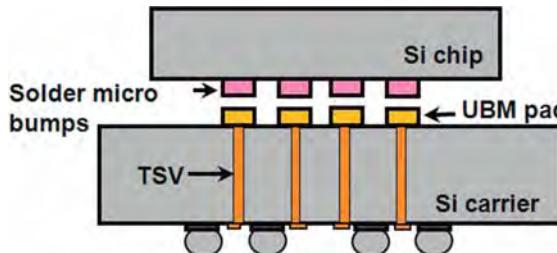


Figure 2. Schematic drawing of 3D stacking of the Si chip/Si carrier with TSV (not to scale). (courtesy of A. Yu of IME Singapore)

## Oxide removal prior to bonding

After TSVs are etched, they are filled with a conductive material such as copper or one of its alloys. After the dielectric and metal patterns have been formed, substrates are thinned to some fraction of their original thickness, then the substrates are bonded together to form one electrical entity.

Many papers have cited the advantages of Cu-based systems, which include ease and familiarity of processing, mechanical and electrical integrity, and scalability.<sup>2-6</sup> For these and other reasons, Cu has become a major focus as an interconnect material for 3D integration. A representative TSV structure for 3D chip stacking is shown in **Figure 2**.

To vertically join circuits, the exposed

Cu surfaces are bonded together using either die-to-die (D2D), die-to-wafer (D2W), or wafer-to-wafer (W2W) bonding. Regardless of the method used, the Cu surfaces are likely to have oxides present that compromise results of thermocompression bonding.

Metal surface oxidation is a persistent problem in device bonding. Because oxides generally adhere poorly to other metals

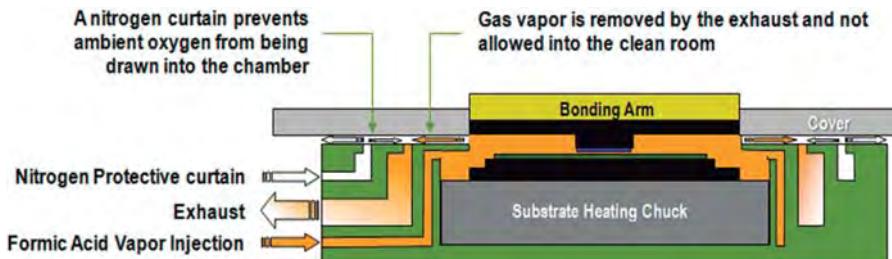
or oxides, the bonding force must penetrate the oxide, literally breaking through it to achieve metal-to-metal cohesion. Not only does this increase the required bonding force, but the presence of oxides may also raise the electrical resistance of the joint. Even after the device has been bonded, existing oxides may

provide a convenient site for further oxidation, leading to reliability and performance problems.<sup>4</sup> For this reason, high-quality and reliable bonding benefits from a controlled environment to either prevent oxide formation during the bonding sequence or to remove previously formed oxides. The requirements for an oxide removal process include:

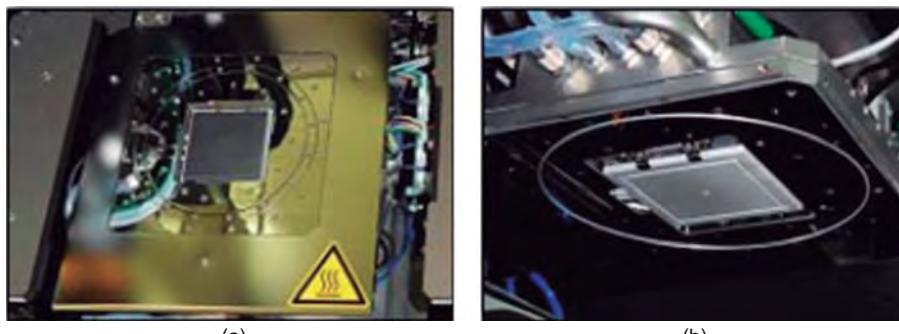
- Fast, effective removal of oxides
- Inert to other surfaces
- Minimal or non-existent residue
- EHS compliant
- Sufficient duration of effect
- Cost-effective

Historical methods for removing or inhibiting oxides include mechanical scrubbing during the bonding process, using an acid dip prior to bonding, or using oxide-reducing flux. Though these methods have worked for larger feature sizes, they can create misalignments, add processing steps, or in the case of flux, can lead to reliability or performance problems if flux residues are not completely removed.

However, a novel oxide removal method exists involving a local confinement chamber built into the bonding tool that uses reducing gasses, such as forming gas or formic acid vapor, to safely reduce the oxides immediately prior to bonding. The confinement chamber is created by using a non-contact virtual seal between the bonding head and the substrate chuck, ensuring gas collection and preventing oxygen intrusion. This setup enables gas confinement for D2D or D2W bonding



**Figure 3.** Schematic of local confinement chamber for D2D bonding



**Figure 4.** Photos of the confinement hardware looking down at the bonding chuck (a) or up at the bonding head (b)

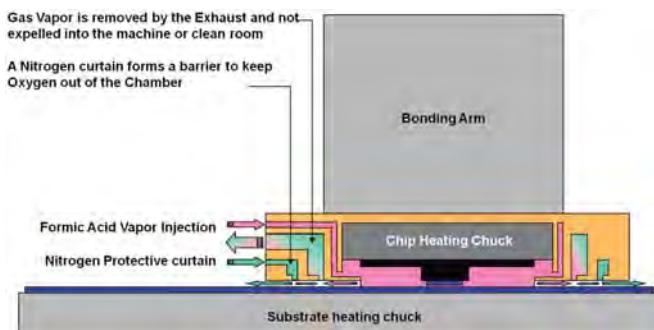
under controlled atmosphere while preserving the alignment of the device with respect to its substrate.

The process gas is injected through horizontal nozzles aimed at the device being bonded (**Figure 3**). An exhaust ring removes the process gas from the micro-chamber and sends it into the gas exhaust line, keeping the gas out of the machine and the clean room. A nitrogen curtain is formed around the exhaust, ensuring that ambient air is not entrained into the micro-chamber by the Venturi effect, while a cover attached to the bond head creates the confined micro-chamber (**Figure 4**). This configuration operates with either inert gasses to prevent oxide formation on bonding surfaces during the bonding sequence, or with reducing gasses such as forming gas to remove and prevent oxides.

**Figure 5** shows a second confinement chamber configuration that is suited for

D2W bonding. Similar to the D2D version, hardware for this design provides the oxide reduction capability to the chip and only to selected areas of the wafer being populated. When the chip has been aligned to its bonding site, the bonding arm lowers the chip very close to, but not yet in contact with the wafer. In this position, the chamber hardware on the arm forms a virtual seal to the wafer. A small gap between chamber and the wafer surface is maintained to avoid possible contamination or misalignment between chip and wafer.

To qualify the confinement chamber's performance, a chip with copper test patterns was heated in a test apparatus to 350 °C for 30 seconds while formic acid vapor flowed into the chamber at 8 SLPM (**Figure 6**). All oxides were presumably removed and the copper surface was highly reflective.



**Figure 5.** Schematic of local confinement chamber for D2W bonding

Next, formic acid vapor flow was terminated, and the copper surfaces oxidized rapidly at 350 °C with ambient air, producing a mottled appearance in less than 5 seconds. Following this, the formic acid vapor was reinstated and the copper returned to its reflective state within a few seconds, indicating that oxide removal was effective and rapid. Quantitative tests with electrical and/or bonding data are ongoing and are positive, showing effective removal of oxides at 250–350 °C. **Figure 7** indicates the testing of the copper coupon as described.

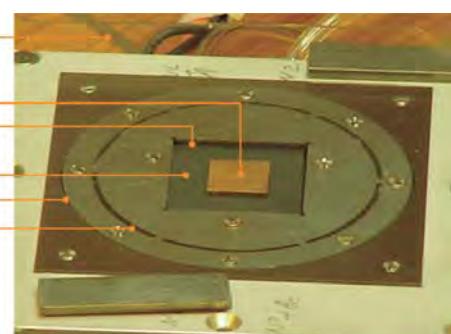
The confinement chambers have been implemented in either configuration on SET device bonders. Materials and applications explored and qualified include Cu-Cu for 3D integration, AuSn for optoelectronics, and In for infrared focal plane arrays. This setup may use any inert or reducing gas, but formic acid vapor is in favor over forming gas due to safety concerns and process efficacy.

### Collective hybrid bonding

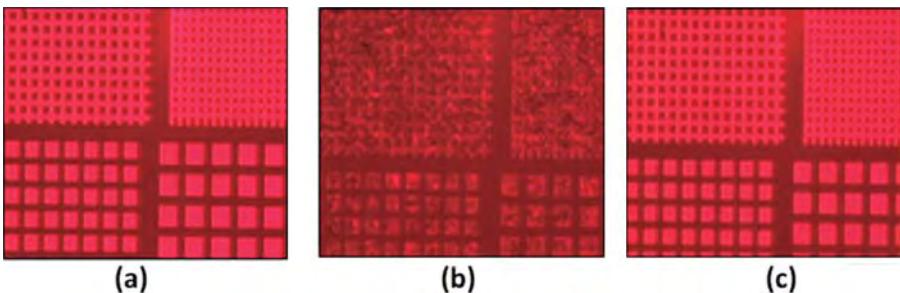
When considering which of the three methodologies (D2D, D2W or W2W) to use, many issues must be weighed and considered, including:

- CTE mismatch between materials
- Die size
- Yield and use of known-good-die (KGD)
- Overall cost

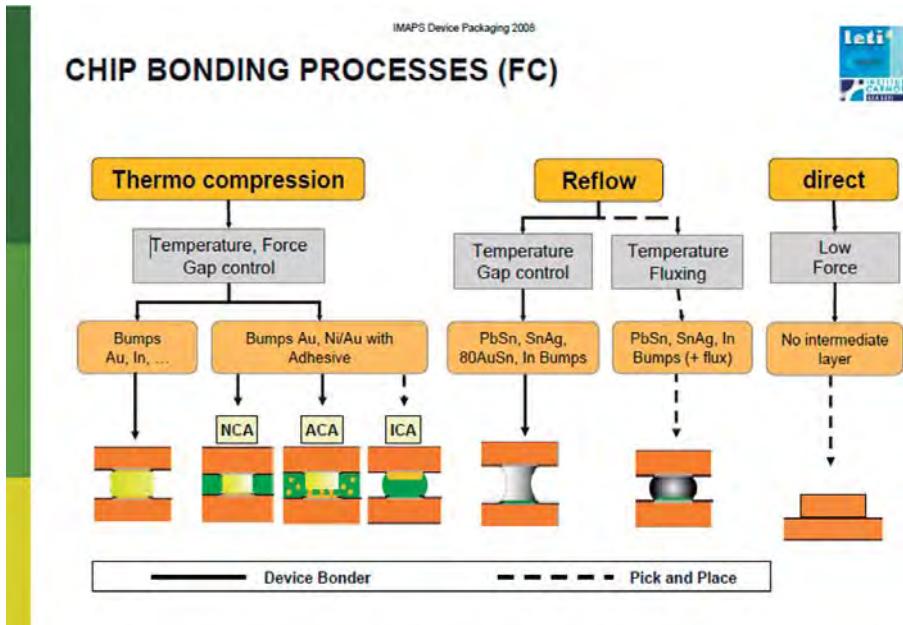
D2D bonding effectively addresses the issues of CTE mismatch between substrate types, the potential mismatch in die size between device types, and also offers the advantage of bonding only good die. It has been in use for many years for high-performance chips such as infrared imaging devices. Because of the high resolution imaging requirements, these



**Figure 6.** Test apparatus for formic acid chamber



**Figure 7.** Copper patterns on test chip (a) after 30 seconds of formic acid vapor, (b) after a few seconds of atmospheric ambient, and (c) after formic acid flow is reinstated, showing the rapid reduction of the oxides



**Figure 8.** Matrix of chip bonding processes

imaging devices have extremely high bump counts (> 10 million), necessitating the use of very precise and often time-consuming bonding processes. Though D2D will continue to play a role in certain markets, it is a slow and therefore expensive methodology that will likely be relegated to low-volume applications.

Developed and used extensively for MEMS processes where a cap wafer was required, W2W bonding has also been in use for some time. More recently, it has been applied to 3D integration due to its inherent high throughput and process simplicity. But since 3D integration is specifically intended to bond various device types of widely different sizes and materials, W2W bonding may be attractive only when joining smaller, higher-yielding devices, and where die and wafers are equally sized.

D2W bonding is a promising assembly strategy that may capture the best of the

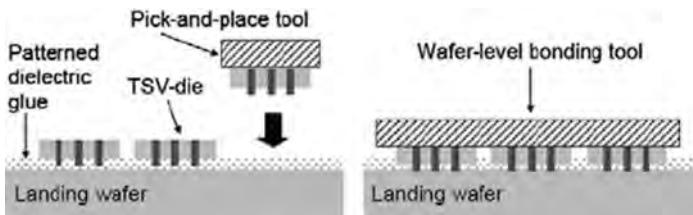
two previous methodologies, but long bonding processes can also limit its cost-effectiveness. It offers high yield due to using only KGD, high flexibility allowing heterogeneous integration, and high accuracy placement potential by means of the flip chip device bonding technique. This method might suffer from potentially lower throughput since each die is aligned and bonded or placed individually. However, this drawback is offset by the benefit of bonding only KGD to known-good bonding sites of the wafer, increasing the final yield and accurate placement of the die. This is particularly important for 3D integration where alignment and bonding of multiple dies must be performed with high precision.

thermocompression of copper and other metals, thermosonic bonding, and adhesive and fusion bonding, (Figure 8). The roadmap for 3D integration calls for increasing density of TSVs and related elements, necessitating ever-tighter alignment and control, and driving a move toward D2W bonding.<sup>7-8</sup>

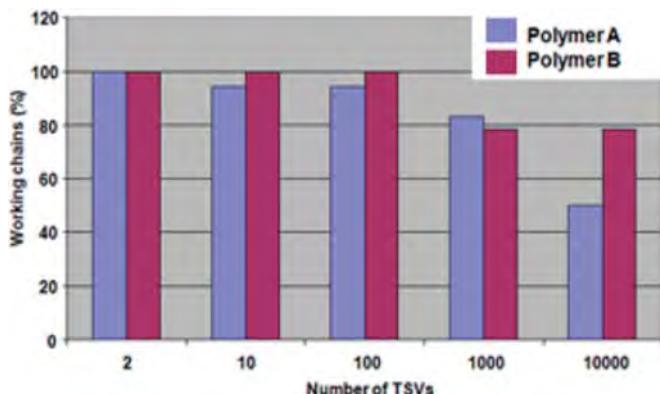
A new method has been developed, in which singulated die are initially bonded or tacked to a wafer in D2W fashion, then the bonding process is completed in a wafer bonder tool. Intended to address the issues of CTE mismatch and bonding KGD of various sizes, yet with the cost effectiveness and throughput of a W2W scheme, this method has been referred to as collective hybrid bonding (Figure 9).

In one application of this collective hybrid bonding strategy, a patterned dielectric adhesive was used to populate a wafer in D2W fashion.<sup>9</sup> The author notes the inherent flexibility of D2W for 3D integration, particularly for heterogeneous integration, as it allows varying die sizes and is compatible with the selection of KGD. Following the D2W placement step, the populated wafer was further bonded in a two-step process in a wafer bonder wherein reflow of the polymer pulled the Cu TSVs into mechanical and electrical contact with the Cu landing pads. For this process, 2 different polymers were used; electrical results are shown in Figure 10 and indicate yields of 80% for daisy chains up to 1000 TSVs in length.

In another study, test die with Cu-Cu and Cu-Sn TSV's of 10 $\mu$ m and 40 $\mu$ m pitch, respectively, were tacked with high accuracy onto a 300mm landing wafer using a similar polymer. After tacking, final bonding was performed in a wafer bonder. Electrical test structures indicated all sites aligned to within about 1.5 $\mu$ m, with maximum die rotation of 0.03 degrees observed.



**Figure 9.** In collective hybrid bonding, accurate placement of TSV die is followed by gang bonding of all dice to complete the bonding process. (Courtesy of Anne Jourdain IMEC)



**Figure 10.** Electrical yield on 1000 TSV daisy chain structures with collective hybrid bonding method. (Courtesy of Anne Jourdain, IMEC)

## Conclusions

Two key areas of 3D integration were discussed, namely the removal of metal oxides prior to bonding, and the use of collective hybrid bonding to optimize accuracy and throughput. Solutions have been integrated using a flip chip bonder platform, with a view toward creating technically effective and manufacturable processes. Hardware and methodology have been successfully installed and implemented at customer sites, with plans in place to apply and optimize these

"Three Dimensional Interconnects with High Aspect Ratio TSV's and Fine Pitch Solder Microbumps," Proc. of 59th ECTC, 2009.  
 3. Rahul Agarwal, et al., "High Density Cu-Sn TLP Bonding for 3D Integration, Proceedings of 59th ECTC, 2009.  
 4. John Lannon Jr., et al. "High Density Cu-Cu Interconnect Bonding for 3D Integration" Proc. of 59th ECTC, May 2009.  
 5. Bart Swinnen, et al., "3D Integration by Cu-Cu Thermo-compression Bonding of Extremely Thinned Bulk-Si Die

solutions in new and existing product lines. <sup>8</sup>

Containing 10µm Pitch Through-Si Vias," Proc. International Electron Devices Meeting, Dec 2006, pp. 1-4.

6. Pierric Gueguen, et al. "3D Vertical interconnects by Copper Direct Bonding", MRS fall (2008).

7. Gilbert Lecarpentier, et al., "Wafer Level Packaging Chip to Wafer approach using Flux Less Soldering and featuring Hermetic Seal Capability", 4th Annual IMAPS Conference on Device Packaging, Scottsdale, Arizona, March 2008.

8. Leo DiCioccio, et al., "An Innovative Die to Wafer 3D Integration Scheme: Die to Wafer Oxide or Copper Direct Bonding with planarized oxide Inter-Die Filling", Proceedings of IEEE International Conference on 3D Systems Integration, October 2009.

9. Anne Jourdain, et al., "Electrically Yielding Hybrid Bonding for 3D Stacking of IC's", Proc. of 49th ECTC, 2009

10. Gilbert Lecarpentier, et al., "Die-to-Wafer bonding of thin dies using a 2-Step approach; High Accuracy Placement, then Gang Bonding", Proc. of IMAPS Device Packaging Conference, 2010

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# Jetting Your Way to Fine-pitch 3D Interconnects

By Mike O'Reilly [Optomec, Inc.] and Jeff Leal [Vertical Circuits Inc.]

**A**n insatiable consumer appetite for instant access to exponential functionality at reduced cost is powering the smart phone and intelligent tablet device markets. The question is: why? Goldman Sachs uses the 5C's to describe the attraction of these devices: consumption, content, connected, constant-on and commerce. While they were referring to the Apple iPad, the 5C's can be applied to the continuous push by "smart" device manufacturers to meet consumers' ongoing thirst for instant access to electronic content regardless of how it is supplied. These smart devices are finding their way into a wide range of markets such as automotive (smart cars); appliances (catch the latest episode of Food Network right on your refrigerator); search the web, check out a book from the library, watch that latest on-demand movie while downloading the latest exercise video — all controlled through a Wii multi-media console.

So how do manufacturers deliver a compelling product that fits within increasingly smaller packages and supports streaming audio, video, fast search/download, and touch screen commerce, all at attractive prices? Is through silicon via (TSV) the only packaging solution?

Challenges abound with the TSV approach, although the majority can be solved with time and money. The most challenging obstacles are 3D infrastructure and the associated supply chain to enable broad adoption of 3D ICs. 3D TSV interconnects have many possible implementation scenarios ranging from when in the process flow (first, middle, or last) the via is formed, to which process is used in its creation (e.g. front, or back-side). Another key challenge is I/O standardization between memory and application layers. Lastly, as package complexity

increases, thermal management may become a troublesome issue. Yes, TSV holds lots of promise, but the fact remains: manufacturing challenges are yet to be fully addressed.

Can wire-bond solutions continue to meet system-in-package (SiP) scaling demands? While wire bonding attempts to address growing interconnect density challenges — the overall diameter of the bonding wire is  $<35\mu\text{m}$  and equipment placement accuracy is improving — the sheer number of interconnects between memory stacked 8-16 chips high present both performance and manufacturing challenges. Issues, such as signal integrity, become real show stoppers as customers push performance goals of these devices. The challenge is exacerbated when stacking sophisticated multi-chip packages that integrate processors. While wire-bond technology remains viable for the majority of today's semiconductor interconnect applications, it may be reaching an inflection point as 3D packaging demands push the functionality envelope.

Is there another way to meet these advanced packaging challenges without having to completely reinvent manufacturing processes and technologies?

Replacing traditional wire bonds with fully printed conformal interconnects using evolutionary packaging steps may be the answer to these complex issues. A proprietary aerosol jet technology has been used in a variety of printing applications ranging from crystalline silicon solar wafers and next-generation touch screen displays, to fully printed transistors. The ability of this technology to print a variety of materials onto a wide array of substrates at feature sizes as small as

$10\mu\text{m}$  makes it a logical choice for addressing fine-pitch semiconductor packaging requirements.

## Aerosol Jet Process - How it Works

Aerosol jet<sup>1</sup> printing begins with atomization of an ink, which can be heated up to  $80^\circ\text{C}$ , producing droplets on the order of one to two microns in diameter. The atomized droplets are entrained in a gas stream and delivered to the print head, which also can be heated to  $80^\circ\text{C}$ . Here, an annular flow of clean gas is introduced around the aerosol stream to focus the droplets into a tightly collimated beam of material that also serves to eliminate nozzle clogging. The combined gas streams exit the print head through a converging nozzle that compresses the aerosol stream to a diameter as small as  $10\mu\text{m}$ . The jet of droplets exits the print head at high velocity ( $\sim 50 \text{ m/s}$ ) and impinges upon the substrate. Electrical interconnects are formed by moving the print head, equipped with a mechanical stop/start shutter, relative to the substrate. All printing occurs without the use of vacuum or pressure chambers and at room temperature.

The high velocity of the jet enables a relatively large separation between the print head and the substrate, typically 2-5mm (**Figure 1**). The droplets remain tightly focused over this distance, resulting in the ability to print conformal patterns over three dimensional

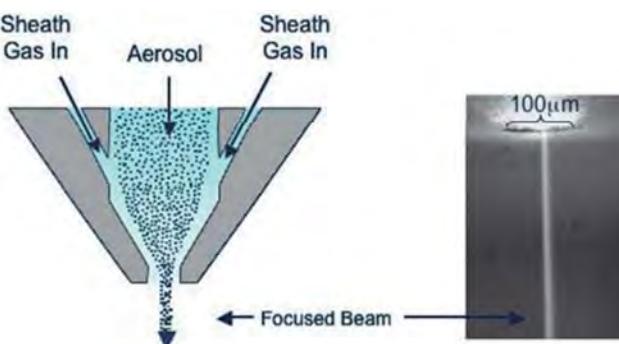


Figure 1. Aerosol jet print head

substrates such as stacked die. Despite the high velocity, the printing process is gentle; substrate damage does not occur and there is generally no splatter or overspray from the droplets.

Once patterning is complete, the printed ink typically requires post-treatment to attain final electrical and mechanical properties. Post-treatment is driven more by the specific ink and substrate combination than by the printing process.

The atomization step is very flexible compared to inkjet. Particulate suspensions are easily atomized, although as a general rule, suspended particles should be on the order of  $0.5\mu\text{m}$  or less. Ink viscosity may be in the range of 1-1000 cP, although it may be necessary to optimize the viscosity for a particular application. The materials used to construct the printing system hardware are generally not susceptible to degradation by the ink solvents, allowing a wide range of solvent vehicles to be used in the process.

## Direct Write of Interconnects

The relatively large working distance (the distance from the print tip to the substrate) of the aerosol jet print head enables conformal printing along stacked dies of 2mm or less in total height without having to adjust Z-height positioning. Typical interconnects are  $25\text{-}30\mu\text{m}$  wide by  $>5\mu\text{m}$  in height. Total length of the interconnects are typically 1.5mm long with throughput for a single nozzle reaching up to 5,000 interconnects per hour (Figure 2). The aerosol jet print head is highly scalable,

supporting 2, 3, 5, or more nozzles at a time, enabling projected throughputs of  $>20,000$  or more interconnects per hour. The print head can handle extended print runtimes of twelve hours or more before ink refill is required. An automated ink refill system that will extend ink runtime to twenty-four hours or more is under development.

## Automation Integration

The aerosol jet print engine has been integrated into an electronics automation supplier's production proven platform (Figure 3). The automation platform accommodates the print engine including the atomizer and print head, heater, shutter, and process controls. Additionally, the automation platform is equipped with auto-fiducial synching; shutter cleaning station; motion control with  $\pm 5\mu\text{m}$  of accuracy; heated platen to  $150^\circ\text{C}$ ; auto board load and unload; and GUI driven interface with on board system diagnostics. The platform is highly scalable and capable of supporting evolving semiconductor packaging form factors.

## A Working Process

This novel solution is suited for printing fine featured interconnects and other materials meeting demanding manufacturing specifications. However, printing is only one step in the manufacturing of fully functioning SiP's using the vertical interconnect pillar (VIP) process.<sup>2</sup> In addition to industry standard package manufacturing steps, five additional steps

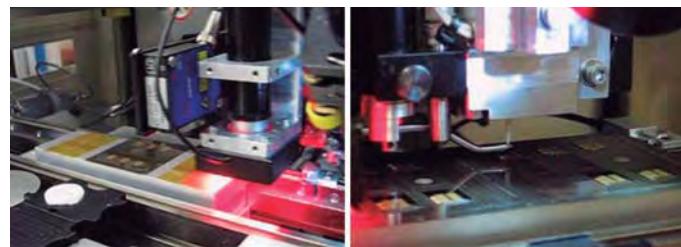


Figure 3. Integrated aerosol jet print solution

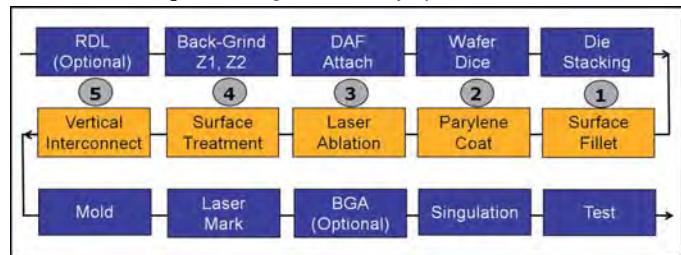


Figure 4. Vertical interconnect pillar (ViP) process

(Figure 4) that fully enable the implementation of fine-pitch vertical interconnect printing are necessary and include surface fillet, parylene coating, laser ablation, surface treatment, and fine-pitch vertical interconnect.

Typical print inks tend to flow downhill regardless of their viscosity. The surface fillet (Figure 4) is used to create a gentle sloped surface on the stacked die, typically creating  $45\text{-}60^\circ$  inclines, which prevent the material from free flow at steep angles. The parylene coating is applied to the entire stack and then an excimer laser is used to open specific pads on the dies and substrate where an electrical connection is required. A surface treatment is used to clean away ablated material and change the surface tension to enable printing of fine-pitch vertical interconnects without shorting between parallel lines on the stacked die over 3D topology.

Using inks that meet both mechanical and electrical requirements is key to the fine-pitch interconnect process. These

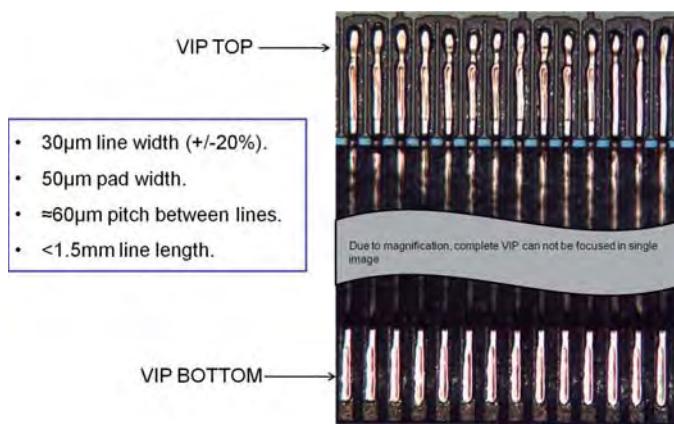


Figure 2. Vertical interconnect package

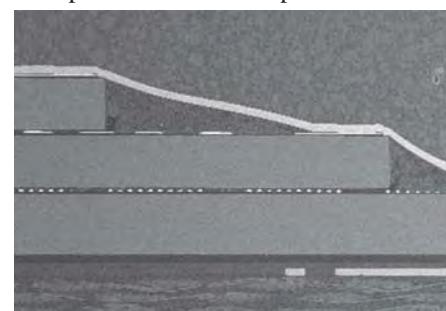


Figure 5. Aerosol jet printed interconnect

inks must be capable of extended 8+ hour production runs without any changes in output rates or electrical characteristics. They need to stack properly without overspray or satellites, maintaining mechanical dimensions throughout the course of a manufacturing shift. As direct-write printed electronic applications continue to grow, a new class of nanoparticle electrically conductive materials (inks)

has found its way into the market, fully meeting manufacturing specifications.

As interconnects are printed from board connectors along the die stack, they come into contact with the laser ablated (exposed) pads and create electrical connections. A single printed interconnect may connect with openings on several die, thereby creating a more compact electrical connection and efficient circuit (**Figure 5**).

With wire bond, interconnects extend from one pad to another, requiring the need for multiple physical wires to create a complete pad-to-pad circuit. As package densities increase the number of wire-bond connections increase, creating the potential for cross talk and/or signal integrity challenges within SiP packages. This may force a vendor to slow the operational efficiency of the circuit and limit full device functionality.

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### Validating the process

The steps in the ViP process have been optimized over the past twelve months. Each process step has been fully analyzed and optimized for SiP packages. Actual boards filled with functioning SiP's have gone through the proprietary process steps, including the aerosol jet fine line interconnect print step with printed conformal interconnects of 25-30 $\mu\text{m}$  wide by >  $\mu\text{m}$  high, and fully functioning parts have been manufactured.

Any product that will be commercially sold needs to pass industry standard reliability testing (**Figure 6**). Complete product qualification tests are underway that will re-validate the process and product by Q3 of 2010. Pilot production sites are due online before the end of 2010, with full, high-volume production systems available by Q1 2011.

### Expanding Capabilities

Fine line printing for SiP technology is just at the beginning of its life cycle. When direct write ViP technology was introduced more than two years ago, the minimum line width was 100 $\mu\text{m}$ , with a pitch of 200 $\mu\text{m}$ . With the introduction of the aerosol jet technology, line widths of 25-30 $\mu\text{m}$  are being achieved with pitches of < 65 $\mu\text{m}$ . With further refinement of the technology, line widths as small as 10-15 $\mu\text{m}$  at 25 $\mu\text{m}$  pitch are expected to be possible.

Aerosol jet technology also has the added benefit of printing a wide array of materials. Investigation is underway for utilizing the process to print a dielectric material coating to selectively insulate pads. The benefit of this

	VCI DRAM (BGA) Pass Server Level Reliability	VCI FLASH (μSD)	VCI FLASH (LGA)	VCI SiP (BGA)
<b>Moisture Resist Test:</b>	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C
<b>Biased-HAST:</b>	Bias 3.6V, 130°C, 85% RH, 144 hours	Bias 3.6V, 130°C, 85% RH, 96 hours	Bias 3.6V, 130°C, 85% RH, 96 hours	Bias 3.6V, 130°C, 85% RH, 96 hours
<b>Autoclave/PCT:</b>	Unbiased, 121°C, 2atm, 100%RH, 96 hours	NO	Unbiased, 121°C, 2atm, 100%RH, 96 hours	Unbiased, 121°C, 2atm, 100%RH, 96 hours
<b>High Temp Storage:</b>	150°C, 1000 hours	150°C, 1000 hours	150°C, 1000 hours	150°C, 1000 hours
<b>Temp Cycle:</b>	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)
<b>Card Tests: (DBT/Insert/Salt)</b>	N/A	SDI Spec.	N/A	N/A

Figure 6. VCI reliability test criteria

approach is further reduction in process and equipment costs. Other areas, such as surface fillet printing and printing redistribution layers (RDLs) with this process are also being explored.

### Viable Interconnect Alternative

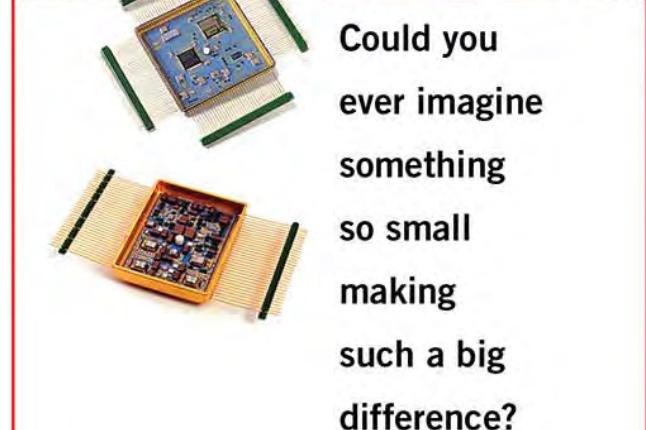
Wire-bond solutions will not just fade away and TSV is emerging as the solution for the most complex packaging challenges. However there is the middle ground where 3D printed interconnects can provide real cost and functional benefits for the production of multi-chip stacked die in SiP applications. Aerosol jet's fine line printing capabilities enable significant pitch reductions, thereby increasing interconnect densities and affording greater semiconductor packaging functionality at a fraction of the cost of TSV technology. With its ability to use off-the-shelf materials and print in normal atmospheric conditions, equipment and maintenance costs are greatly reduced. This multi-function platform is clearly poised to enable high density interconnect solutions for a range of advanced 3D semiconductor packaging applications. 

### References

1. Aerosol Jet is a trademark of Optomec, Inc.
2. Vertical Interconnect Pillar process is a trademark of Vertical Circuits, Inc.

For questions concerning the Aerosol Jet print solution, email the company at [requestinfo@optomec.com](mailto:requestinfo@optomec.com)

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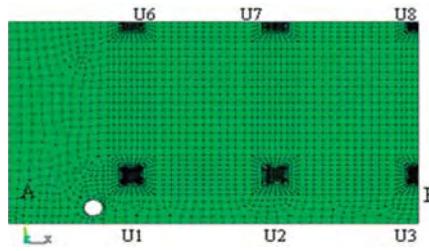
# Drop Test Reliability and Design of Wafer-Level Chip-Scale Packages

By Yong Liu, Stephen Martin [Fairchild Semiconductor Corp], and Luke England [Micron Technology]

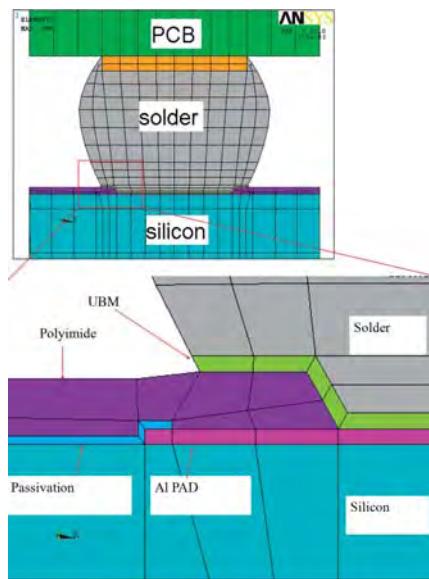
The trends in next generation wafer-level chip-scale packages (WLCSPs) are toward thinner and finer pitches with microbumps. The mechanical shock resulting from mishandling during transportation or customer usage may cause WLCSP package solder joint failures.<sup>1</sup> Since the board-level drop test is a key qualification test for portable electronic products, it is becoming a topic of great interest for many researchers.<sup>2-4</sup> Most of the drop test and modeling works focus on the failure modes of solder joints. The impact of other aspects of WLCSP design has not yet been fully investigated. This comprehensive study, with modeling and testing, investigates the WLCSP design and its drop test reliability. The results of varying WLCSP design parameters such as under-bump metallization (UBM) geometry, polyimide side wall angle and thickness, metal stack thickness, and solder joint height are documented.

## WLCSP Drop Test and Model Set Up

The drop test set up is based on JEDEC standard JESD22-B111.<sup>5</sup> The board, with a dimension of 132 x 77 x 1.0mm, accommodates 15 components of the same type in a three-row-by-five-column format. Due to the symmetry, a quarter finite element model (66 x 38.5 x 1mm) of a JEDEC board with WLCSP chips is selected. **Figure 2** shows a finite element model of the lower left quarter of the test board with six components (U1, U2, U3, U6, U7, U8) that are numbered according to the JEDEC standard. The line AB in **Figure 1a** is defined across the board at a distance of 1mm from the edges of components U1, U2, and U3. There are six corner points on the PCB defined 1mm below each of the six packages.



**Figure 1a.** Finite element model of quarter PCB with chip units (U1, U2, U3, U6, U7, U8)



**Figure 1b.** Finite element model of the cross section

and 1mm distance left from each of the six packages.

**Figure 1b** shows the finite element model of the cross section of the corner joint for a WLCSP structure. The basic setting includes a 2.7 $\mu$ m thick aluminum pad, 2 $\mu$ m thick UBM with 0.5 $\mu$ m Au and 0.2 $\mu$ m Cu, and a 0.9 $\mu$ m thick passivation that covers 5 $\mu$ m of the edge of the aluminum pad. A 10 $\mu$ m thick polyimide layer is above the passivation and the aluminum pad. There is a 200 $\mu$ m diameter via open in the polyimide layer;

its side wall angle (between its slope and the bottom surface) is 60 degrees. The UBM connects to the aluminum pad through the via. The solder is placed on the UBM and connects to the copper post on the PCB board.

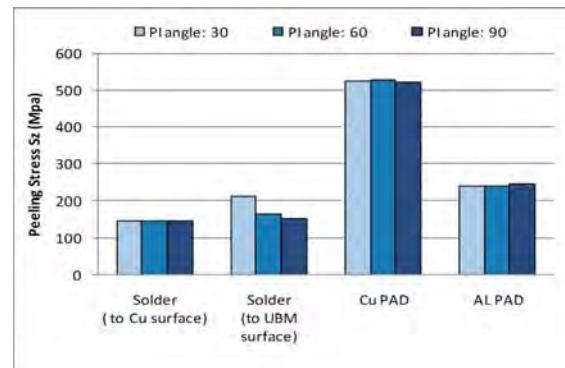
**Table 1** defines the elastic modulus, Poisson ratio, and density of each material. The silicon, passivation, polyimide, PCB, and UBM are considered as linear elastic materials, while the solder ball, aluminum pad, and PCB copper pad are considered as having non-linear material properties.

	Modulus (Gpa)	Poisson Ratio	Density (g/cm <sup>3</sup> )
Silicon	131	0.278	2.33
Solder	26.38	0.4	7.5
Passivation	314	0.33	2.99
Polyimide	3.5	0.35	1.47
PCB	Ex=Ey=25.42 Gxz=Gyz=4.91 Gxy=11.45	Nuxy=0.11 Nuxz=Nuyz=0.39	1.92
Cu PAD	117	0.33	8.94
Al PAD	68.9	0.33	2.7
UBM	196	0.304	9.7

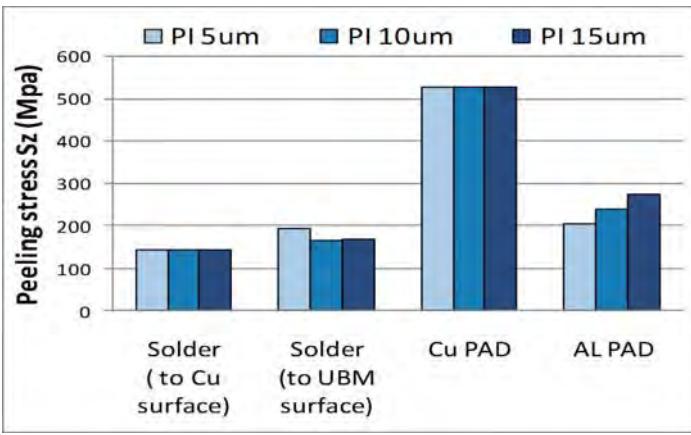
**Table 1.** Elastic modulus, Poisson ratio, and density of each material

	Yield stress (Mpa)	$\gamma$	$m$
Solder (SAC405)	41.85	0.00011	0.0953

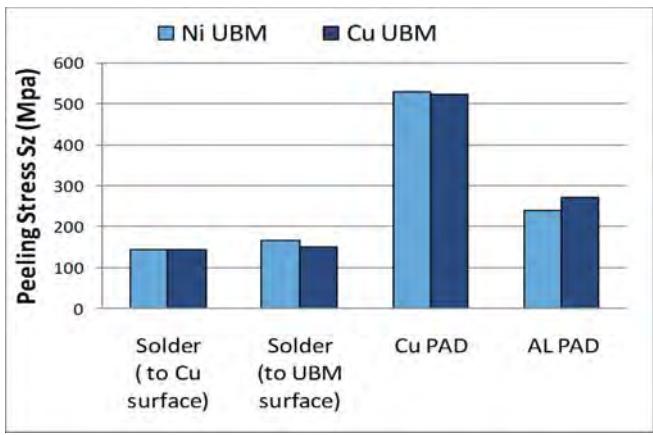
**Table 2.** Rate-dependent Peirce model of solder SAC405



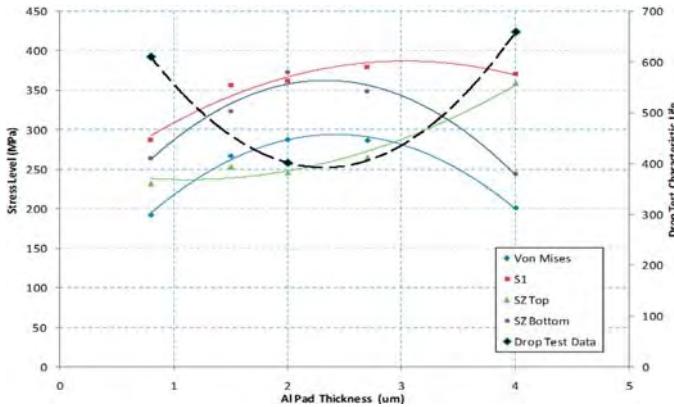
**Figure 2.** Comparison of maximum peeling stress at U1 with different polyimide side wall angles



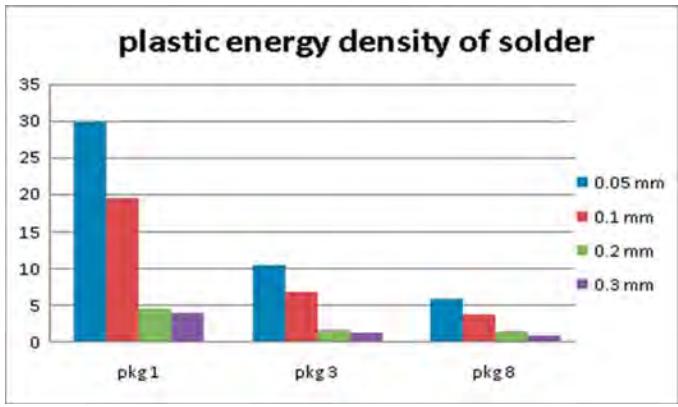
**Figure 3.** Comparison of maximum peeling stress at U1 for different polyimide thicknesses



**Figure 4.** Comparison of maximum peeling stress at U1 with two different UBM designs



**Figure 5.** PI stress versus Al pad thickness



**Figure 6.** Plastic energy density of solder joint (MPa)

**Table 2** gives the non-linear properties for solder SAC405 and is considered as a rate-dependent Peirce model. The data was obtained through the Hopkinson dynamic material high speed impact test.

### Impact of Polyimide Side Wall Angle

The polyimide layer connects both the aluminum pad and UBM (**Figure 1b**). **Figure 2** shows the maximum peeling stress comparison of the solder, copper pad, and aluminum pad with different polyimide side wall angles at location U1.

The stresses in the copper pad, aluminum pad and solder interface connected to the copper pad show that there is no significant difference with different polyimide side wall angles. However, there is an impact on the solder joint interface that adheres to the UBM.

### Impact of Polyimide Thickness

The polyimide thickness is selected to be 5 $\mu$ m, 10 $\mu$ m, and 15 $\mu$ m respectively.

**Figure 3** shows the peeling stress for the solder, copper pad, and aluminum pad with different polyimide thickness at location U1.

The peeling stress on the aluminum pad increases as the polyimide thickness increases from 5 $\mu$ m to 15 $\mu$ m. The solder stress at the interface with the UBM decreases as the polyimide thickness increases from 5 $\mu$ m to 10 $\mu$ m. However, after 10 $\mu$ m there is no significant difference.

### Impact of the UBM Structure

A copper UBM structure is designed to compare with the existing 2 $\mu$ m nickel standard UBM having 0.5 $\mu$ m Au and 0.2 $\mu$ m Cu. The thickness of the copper UBM is 8 $\mu$ m. **Figure 4** shows the peeling stress comparison for the solder joint, copper pad, and aluminum pad with copper UBM and with the standard UBM of the package at location U1. From **Figure 4** it can be seen that the peeling stress on the solder joint interface attached to the standard UBM

is greater than that attached to the copper UBM. However, the peeling stress on the Al pad with copper UBM is greater than the standard UBM.

### Impact of Aluminum Pad Thickness

Different aluminum pad thicknesses (0.8 $\mu$ m, 2 $\mu$ m, 2.7 $\mu$ m, 4 $\mu$ m) are simulated.

**Figure 5** gives the polyimide stresses versus the Al pad thickness and its correlation with the drop test life (black dotted line). There is an optimal Al thickness from both modeling and drop test results.

### Impact of Solder Joint Height

Different solder joint heights (50 $\mu$ m, 100 $\mu$ m, 200 $\mu$ m, 300 $\mu$ m) are considered.

**Figure 6** gives the trends of solder joint plastic energy density with different heights.

In all three package locations, higher solder joints result in less plastic energy density. This indicates that a higher solder joint can help to improve the

	Unit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
No via in pad	PCB 1										301					465
Via in pad	PCB 2										785					476
	PCB 3															986
	PCB 4															476
	PCB 1															368
	PCB 2															825
	PCB 3															224
	PCB 4															493
																582
																598

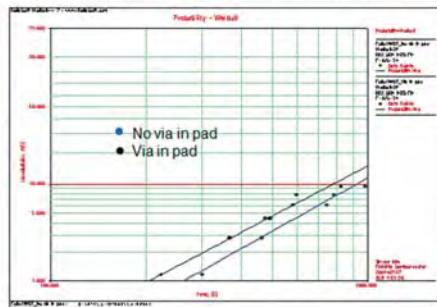


Figure 7. Drop test result

WLCSP drop test dynamic plastic energy performance.

### Drop Test

The drop test condition is 1500g with half sine wave in 0.5ms. Drop count is 1000. A total of 90 units are investigated and mounted on eight JEDEC PCBs in two groups, one with vias and the other

without vias under the copper pads. The drop test results are shown in **Figure 7** and **Figure 8**. From **Figure 7** it can be seen that most of the drop failures appear at the corner locations U5, U11, and U15. **Figure 8** shows the copper pad/crack which occurs at the interface of the solder and copper at the PCB. The test results correlate with the simulation result that

the maximum first principal strain appears at the location of U1 which has the same behavior as U5, U11, and U15 due to the model's symmetry. **Figure 9** gives the first principal strain curves at the interface of the copper pad, solder, and PCB with the package locations U1, U3, and U8. The failure rank is U1>U3>U8. When the dynamic first

PCB1, unit15, the corner bump

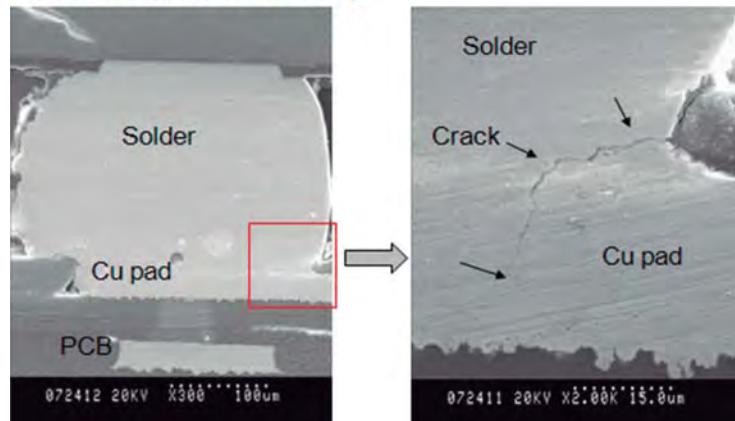


Figure 8. Drop test failure mode

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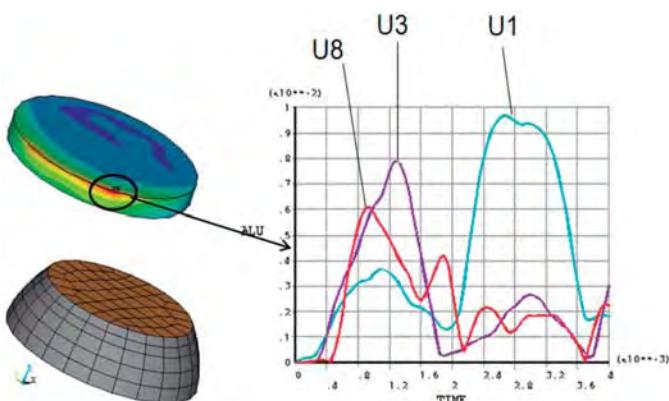
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**Figure 9.** First principal strains of the copper pad at the interface of the solder, copper pad, and PCB for package locations U1, U3, and U8

principal strain reaches the failure strain, the copper pad/trace will break/crack.

### Conclusion

This WLCSP design variable modeling and test study investigate the dynamic behavior of WLCSPs subjected to drop impact by varying the following design parameters: polyimide side wall angle and thickness, UBM geometry, aluminum metal stack thickness, and solder joint

height. Both the drop test and modeling results show that the corner joints of each WLCSP chip (U1, U5, U11, U15) near the PCB screw holes fail first as compared to the chips at other locations. Next to fail are the corner solder joints of chip locations U3 and U13, followed by the U8 chip (center) and the rest of the chips. The failure mode is shown to be cracking at the interface between SAC405 solder and the copper pad/trace, as well as cracking of the copper trace. The test results correlated with the simulation for the failure modes and the PI stress trends with different Al pad thickness. In addition, the solder joint height can significantly improve the drop test dynamic plastic energy performance of WLCSPs.

### Acknowledgments

The authors wish to thank the support of Fairchild Semiconductor and especially the Package Development Group in South Portland, ME, and Bucheon, Korea. ☺

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# 3D IC Integration with TSV Interposers for High-Performance Applications

By John H. Lau, [Electronics & Optoelectronics Labs (EOL), Industrial Technology Research Institute (ITRI)], and Y. S. Chan and S. W. Ricky [Hong Kong University of Science and Technology]

**M**oore's law has been the most powerful driver for the development of the microelectronics industry. This law emphasizes lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through system-on-chip (SoC). On the other hand, the integration of all these functions can be achieved through 3D IC integration system-in-package (SiP), (Figure 1).<sup>1-8</sup>

As Moore predicted in 1965, silicon chips are getting larger while incorporating a higher pin-count and finer pad-pitch.<sup>3-7</sup> Unfortunately, conventional substrates with build-up layers made by organic materials, such as bismaleimide triazine (BT), are facing great challenges in supporting this. To address these issues, silicon interposers with high-density through silicon vias (TSVs), redistribution layers (RDLs), and integrated passive devices (IPDs) have emerged as a viable solution to provide high wiring density redistribution and interconnection.<sup>1-5</sup>

TSVs are the heart of 3D ICs, and in addition to being used for stacking memory chips, they can be used in a passive interposer to support ultra-fine

pitch, high pin-count, high-power, and high-density IC chips; and in active interposers such as logic, microprocessors, and high-bandwidth memories.<sup>3-7</sup> For example, Figure 2a shows a conventional face-down plastic ball grid array (PBGA) package, in which the chip is supported by a high-density BT-substrate with build-up layers connected through microvias.<sup>9</sup> As the chip gets bigger and its pitch gets smaller, the BT substrate can no longer support it.<sup>9</sup> Hence, an intermediate substrate is needed (e.g., the passive TSV/RDL/IPD interposer) to redistribute the array of fine-pitch pads on the chip to fewer and relatively larger pitch pads on a simpler and thinner BT substrate without any build-up layers (Figure 2b) to achieve a smaller footprint with better performance. The packaging system in Figure 1b is called the 2.5D IC integration SiP.

Figure 3 demonstrates the ultimate goal of a high-power, high pin-count, and fine-pitch CPU and memory chips stacked together to address the memory bandwidth challenge. In this case, the CPU acts like an active TSV interposer. However, due to the very high device

density and the complexity of the circuits on the CPU and memory, finding places/spaces to "drill" holes (TSVs) is very difficult, as shown in Figure 4. Besides the tiny devices such as transistors (which cannot be seen in this SEM image), there are many tiny vias ( $\leq 0.1\mu\text{m}$ ) on a chip. They are connected to devices (e.g., 4 tiny vias for each transistor) to build the first metal (M1) layer. Today for many chips, the number of these tiny vias already exceeds the world population of over 7 billion. One of the core competences and major businesses of foundries is to make these tiny vias. They are not the same TSV for 3D IC integration.

Additionally, the CPU and memory chip sizes and number of pin-outs may differ. Forcing them to attach reduces design freedom and could compromise functionality. Longer routings may be needed in the TSV CPU and memory chip, which affects performance. Most importantly, the required TSV manufacturing yield is too high (>99.99%) for the TSV CPU to bear additional costs due to yield loss.<sup>10</sup> Thus, a passive TSV interposer connecting the CPU and memory in certain 3D

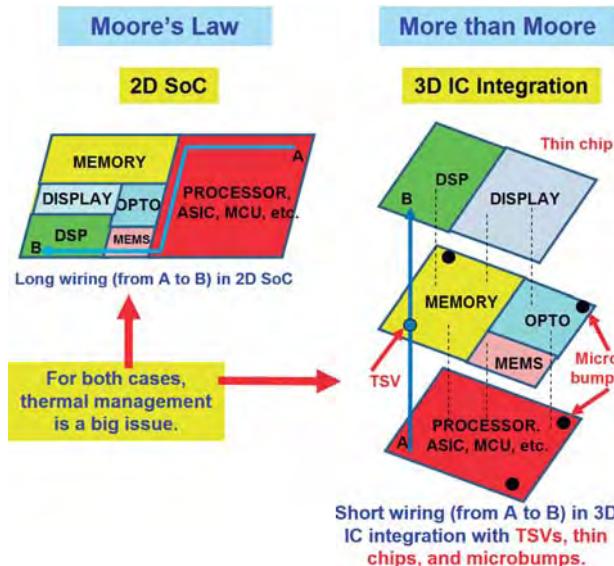


Figure 1. Moore's law vs. more-than-Moore

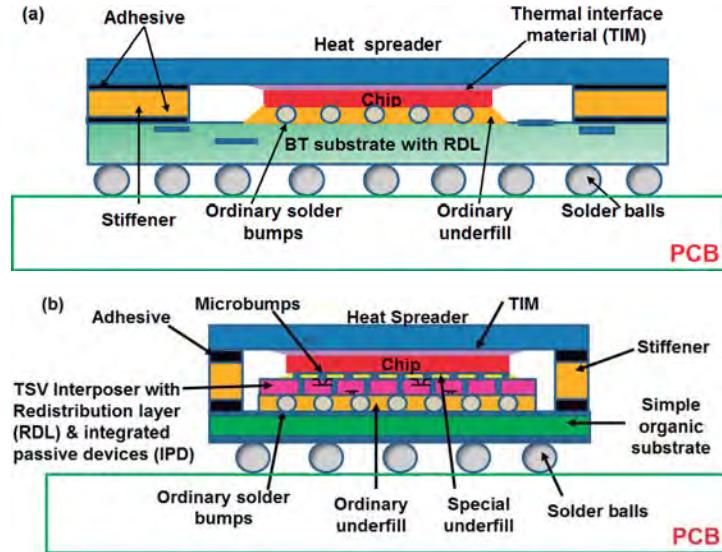
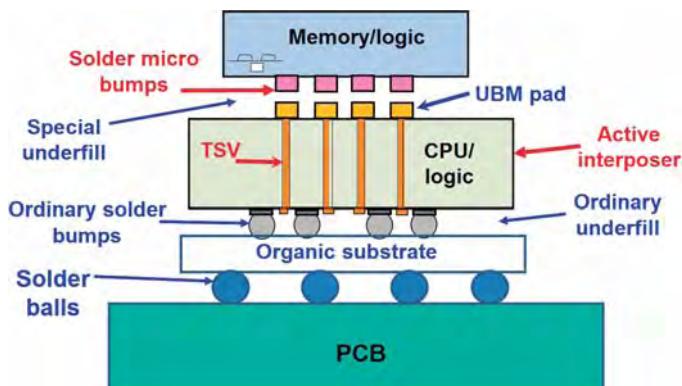


Figure 2. (a) Conventional face-down PBGA. (b) Face-down PBGA with a passive TSV interposer (2.5D IC integration)



**Figure 3.** CPU/logic as an active TSV interposer to support a memory/logic (3D IC integration)

configurations could be effective in resolving these issues.

Thermal management is critical to 3D IC integration because 3D circuits increase total power generated per unit surface area; chips in the 3D stack may overheat if proper and adequate cooling is not provided; the space between the 3D stack may be too small for cooling channels; and thin chips may create extreme conditions for on-chip hot spots. Thus, low-cost and effective thermal management solutions are desperately needed for widespread use of 3D IC integration SiPs.<sup>11,12</sup>

## Design Philosophy

This design addresses the electronic packaging of 3D IC integration with a passive TSV interposer for high-power, high-performance, high pin-count, ultra fine-pitch, small real estate, and low-cost applications. To achieve this, the design uses chip-to-chip interconnections through a passive TSV interposer in a 3D IC integration SiP format with excellent thermal management. Rather than “digging holes” (TSVs) on active

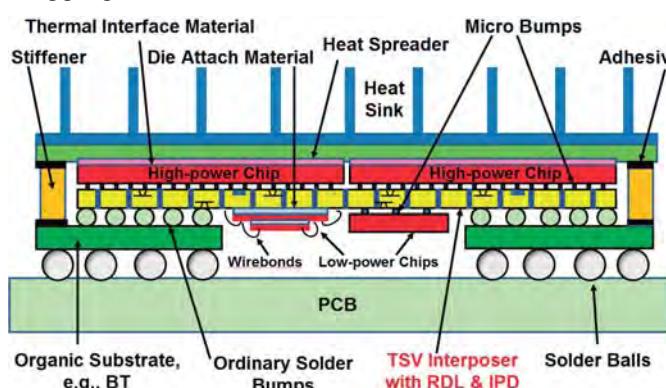
(devices) chips, existing dies with a passive TSV interposer are used to:

- Provide vertical electrical feed through interconnections.
- Perform redistributions (to fan out high pin-out and ultra fine-pitch circuitries).
- Provide decoupling (to enhance the electrical performance).
- Connect to the next level of interconnects (e.g., the package substrate with fewer pin-outs and coarse pitches).
- Construct a cost-effective thermal management system (e.g., heat spreader/sink).

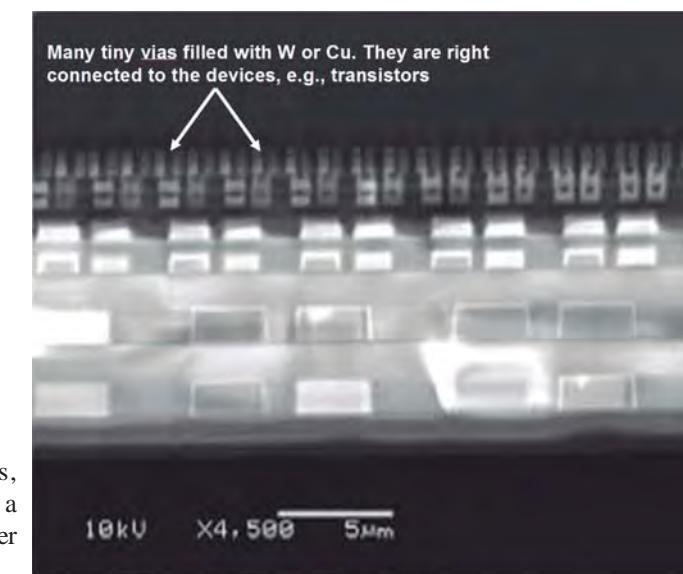
Why not dig holes on the active chips now? Besides the technology issues mentioned earlier, electronic design automation (EDA) tools for 3D IC, are not ready. Because the ecosystem (e.g., infrastructures and standards) of 3D IC does not yet exist, this area cannot be worked on seriously and with full-force.

## The New Design

This 3D IC integration SiP (**Figure 5**)



**Figure 5.** Thermal-enhanced and cost-effective 3D IC integration SiP (without TSVs on active chips) supported by a passive TSV interposer with RDL and IPD

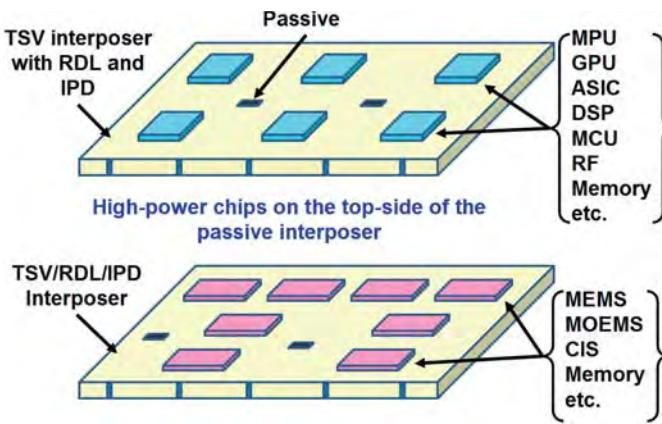


65nm Cu/low-k Chip by GlobalFoundries (2006) to show the tiny vias.

**Figure 4.** Vias (not TSVs for 3D IC integration) in a chip

All the high-power chips — such as the micro-processor unit (MPU), graphic processor unit (GPU), application specific IC (ASIC), digital signal processor (DSP), micro-controller unit (MCU), radio frequency (RF), and high-power memory chips, (**Figure 6**) — are on top of the TSV interposer in a flip-chip format so that the backside of these chips can be attached to a heat spreader via a thermal interface material (TIM). In this case, most of the heat from the high-power chips can be dissipated through the heat spreader (with a heat sink if it is necessary). All low-power chips — MEMS, OMEMS, CMOS image sensors, and memory chips (**Figure 6**) — are at the bottom-side of the interposer with either flip-chip or wire-bond formats or both. A ring-stiffener connecting the organic substrate and the heat spreader provides adequate standoff for 3D IC integration with the passive interposer and to support the heat spreader with or without the heat sink. Underfill encapsulants are needed between the TSV interposer and the high- and low-power flip chips, and between the TSV interposer and the BT substrate. However, underfill is not needed between the 3D IC integration SiP and the PCB. For wire bonding chips, encapsulants may be needed.

This proposed 3D IC integration SiP is very attractive to integrated device manufacturers (IDMs), original equipment manufacturers (OEMs), and electronics



**Figure 6.** The passive TSV interposer with RDL and IPD supporting high-power chips on the top and low-power chips at its bottom

manufacturing services (EMS) because it is a standard face-down PBGA package and has been used by the electronic industry for more than 15 years.<sup>13</sup> It's not only effective in thermal management, but its solder joints are very reliable.<sup>14, 15</sup> Therefore, in conjunction with the proper design of the high-power and low-power chips above/below the passive TSV/RDL/IPD interposer inside the package, a cost-effective, 3D IC integration SiP that displays high electrical and thermal performance can be achieved and manufactured.

The thickness of the proposed TSV/RDL/IPD passive interposer should be  $\leq 200\mu\text{m}$ , the thinner the better. Thus thin-wafer handling methods are required for the passivation, metallization and/or wafer bumping processes. Fortunately, by using the passive interposer, thin-wafer handling is not necessary for the TSV-less high- and low-power chips.

### A 3D IC Integration SiP Design Example

**Figures 7 and 8** show a design example for detailed analysis of a 3D IC integration SiP that consists of 4 identical high-power chips (e.g., microprocessors) uniformly distributed on the top-side of a TSV/RDL/IPD interposer and 16 identical low-power chips (e.g., memories) uniformly distributed at the bottom-side. (This design can be degenerated for the case shown in **Figure 3**.) The dimensions of the high-power chips are  $10\text{mm} \times 10\text{mm} \times 200\mu\text{m}$ , the low-power chips are  $5\text{mm} \times 5\text{mm} \times 200\mu\text{m}$ , and the interposer's dimensions are  $35\text{mm} \times 35\text{mm} \times 200\mu\text{m}$ . There are 1600 identical TSVs with  $20\mu\text{m}$  diameter and  $850\mu\text{m}$

pitch. The backsides of the high-power chips are attached to a heat spreader through a  $100\mu\text{m}$  TIM. An aluminum heat sink with 21 uniformly distributed fins is attached to the back of the heat spreader. Special underfill is used between the TSV interposer and the high- and low-power flip chips. Ordinary underfill is used between the TSV

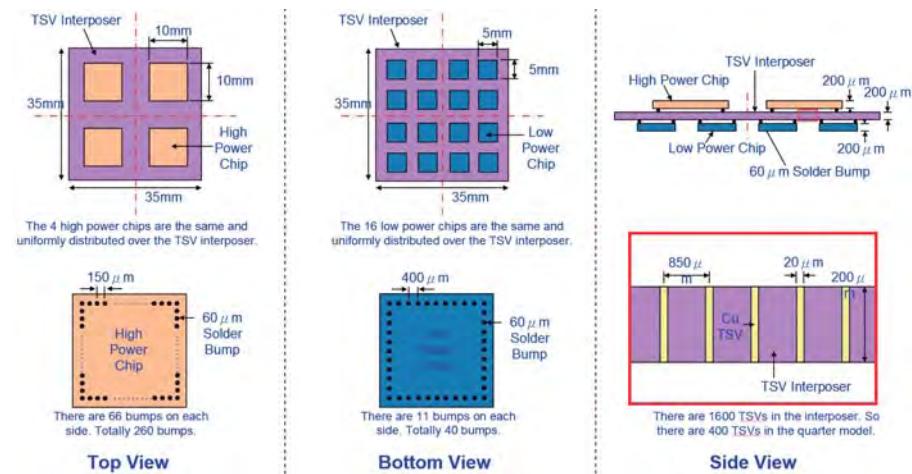
interposer and the organic substrate. Encapsulant is needed for the wirebonding memory stack.

The 3D IC integration SiP mentioned in **Figure 8** is attached (with ordinary solder bumps) to a BT-substrate ( $44\text{mm} \times 44\text{mm} \times 0.8\text{mm}$  with a cavity of  $33\text{mm} \times 33\text{mm} \times 0.8\text{mm}$ .) The substrate is also connected to the heat spreader with the heat sink through an aluminum ring-stiffener as shown in **Figure 8**. Then, the substrate is lead-free (SnAgCu) soldered on a FR-4 PCB ( $50\text{mm} \times 50\text{mm} \times 2.5\text{mm}$ ). Nonlinear finite element modeling and analyses of the temperature distributions and creep strain energy density per temperature cycle have been reported and shows that with proper selection of the heat sink and underfills, the micro-bumps and solder joints are reliable for most of the operation conditions.<sup>16</sup>

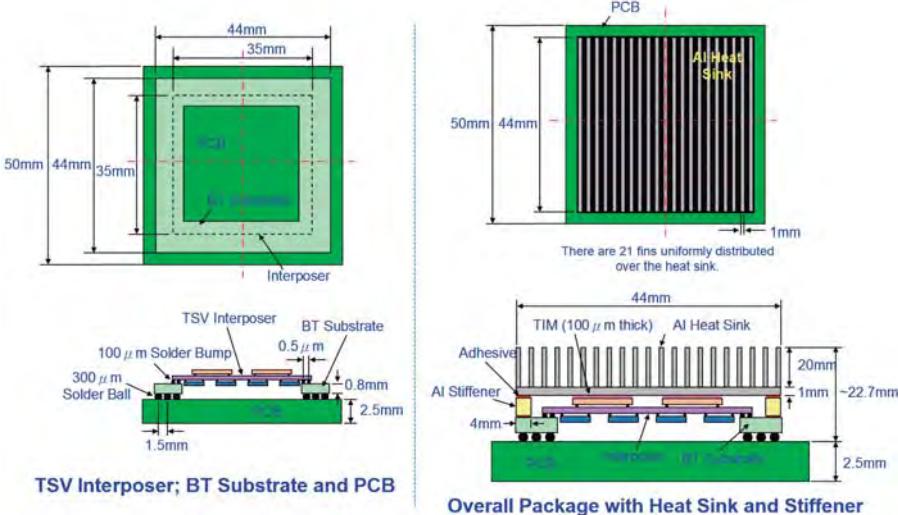
### Summary and Recommendations

A generic, low-cost and thermal-enhanced 3D IC integration SiP has been proposed for high performance applications. Also, a special design has been provided for demonstration. Here is a summary of the important results and some recommendations.

- (1) The TSV/RDL/IPD passive interposer, which supports the high-power chips on top and low-power chips at its bottom, is the gut and workhorse of the current design.
- (2) With the passive interposer, it is not necessary to 'dig' holes on the active chips. In fact, try to avoid making TSVs in the active chips.
- (3) Using a passive interposer allows for flexible coupling of available and/or necessary chips, enhances functionality, and shortens routing.
- (4) Current TSV manufacturing yield loss makes it cost prohibitive to put TSVs in active chips. Using a passive interposer is a cost-effective alternative.
- (5) Wafer thinning and thin-wafer handling costs (for the interposer) are lower because these are not needed for the active chips and thus adds no additional cost due to yield loss.
- (6) With the current designs, all the chips are bare; the packaging cost for individual chips is eliminated.
- (7) More than 90% of heat from the 3D IC integration SiP is dissipated from the back-side of high-power chips using a TIM and heat spreader/sink.
- (8) The appearance and footprint of current 3D IC integration SiP designs are



**Figure 7.** Dimensions of the passive TSV interposer with 4 high-power flip chips on its top and 16 low-power flip chips at its bottom (the gist of the 3D IC integration SiP)



**Figure 8.** Overall dimensions of the 3D IC integration SiP with heat spreader and sink

very attractive to IDMs, OEMs, and EMS because they are standard packages.

(9) Underfills between the copper-filled TSV interposer and the high- and low-power chips are recommended to reduce creep damage of the lead-free micro-bump joints and prolong their lives.

(10) The industry should build an ecosystem incorporating standards and infrastructure for 3D IC integration so that EDA vendors can create the software for design, simulation, analysis and verification, manufacturing preparation, and test of 3D IC integration SiP.

(11) IC integration SiP.

(12) A roadmap for heterogeneous 3D IC integration that integrates passive and active interposers (not including memory stacks) has been established. (**Figure 9**).

## Acknowledgement

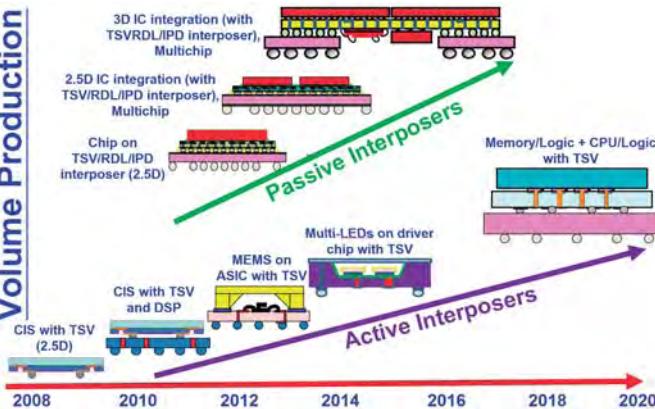
The author (JL) would like to thank HKUST for the fund: DAG08/09.EG12. He also would like to thank Dr. Ian Yi-Jen Chan of Electronics

& Optoelectronics Labs of ITRI for his strong support.

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## Volume Production





# Wafer Scribing & Dicing... Which Method? Equipment?

By Gil Olachea [Az Tech Direct, LLC, [golachea@aztechdirect.com](mailto:golachea@aztechdirect.com)]

**O**kay, what's your preferred method for singulating wafers into die? Sawing? Laser cutting? Laser or mechanical scribing and breaking? Do you really care? If you're an OEM, does it matter? If you're in the assembling/packaging end of the business, is this your issue? Ever see a flow chart or generic process spec on how and what happens with the wafer when it is received by the packaging foundry? Most of these documents simply state wafers are to be singulated ... some documents will split-out wafer taping, however they don't precisely identify sawing, scribe/break, laser or another dicing process to be employed.

Now, let's re-think the question, "... does it really matter what singulation process is chosen?" If you produce III-V semiconductors, MEMS, RFID's, ultra-thin (25-50um) wafers, small die (<1x1mm<sup>2</sup>) you now do care! Why? Because conventional sawing or

scribing may introduce other issues relative to the yield, cost, performance or reliability of the semiconductor devices downstream.

This article will introduce you to the International Directory of Wafer Scribing and Dicing Systems ... a comprehensive supplier listing of fully or semi-automated equipment used in singulating wafers into individual die, or in some cases singulating individual I.C. packages from molded package arrays.

The greatest market for semiconductor singulation equipment is in die preparation for package assembly. Industry estimates fluctuate between 70 to 80% in favor of wafer singulation vs. package singulation, so let's focus on wafer singulation. "DISCO's market split is about 70% in semiconductors and the remaining balance in other markets, including medical, automotive, hi-brightness LEDs, and MEMS," shares Devin Martin of DISCO Hi-Tec America.

The majority of wafer singulation is performed by way of sawing. For many years this has been a stable, reliable and low-cost process. It continues to address wafer advances of decreasing wafer thickness, denser dice, complex metal interconnects, new dielectrics, back-metal systems, and so-forth. Improvements in saw blades and saw hardware/software continue to marvel us in their ability to keep pace with semi advancements.

I attempted to obtain roadmaps for where the market is proceeding in saw, scribe, laser; it was virtually impossible. Even the internal maps are

imprecise. Since the semi market is so diverse, the equipment guys have a difficult time keeping pace.

"Consider the current challenges in dicing: 300mm wafers, low-k dielectrics, copper interconnect, Gallium-anything (III-V materials), sensors, MEMS, sub-30μm street-width, back metals, CSP with very dense bump fields, 3-D, thinner wafers, and so-on," states Henry DeJonge, ALSI's Director of North American Sales. "Now couple these issues with the ever-present demand on the engineering talent required to stay ahead of the tech-curve of process-related improvements needed to deliver a clean die. It keeps me VERY busy!"

After-all ... there've been no 'revolutionary' developments that have shifted the manner in which wafers are



DISCO's Model DFL7161 fully auto-matic ablation laser saw. (source: DISCO Hi-Tec America)



ALSI's Model ICA1204 multi-beam, fully automatic, laser grooving system integrates cleaning/coating stations, accepts 300mm wafers and offers a single-pass cutting process. (source: ALSI)

singulated into die. What's that, you say? "What about laser? That's revolutionary!" I'll argue the move to laser technology is *evolutionary* — a use of another method to accomplish the same outcome.

Laser technology is a paradigm shift from the conventional dicing processes and equipment — predominantly saw/blade or scribe/break. A tremendous investment already exists with these conventional forms of singulating die from wafers. Most packaging foundries are very hesitant in replacing good equipment with long service lives remaining. Squinting-eyed CFO's carefully watch the profit line and ROI (return-on-investment) to assure capital dollars are properly placed and redeemed. Advances in dicing saw equipment and consumables continue to keep pace with the demand for narrower

street widths, which reduces the wafer fab cost per die by yielding more dice per wafer, but more importantly extends the life of the capital investment in the conventional saw equipment.

So, selecting a laser dicing technology would require additional or incremental capital. The other side of this view and fueling the laser choice are semi advancements challenging conventional singulation processes. These are low-*k* dielectrics, narrowing streets, exotic semi materials, and thinner wafers (<50um) to name a few. However, few laser solutions offer the throughput efficiency of a single-pass cut. Most solutions utilize a laser for a first-pass shallow cut/scribe followed by either a conventional saw cut or breaking. This will reduce productivity causing that squinty-eyed CFO to become even more critical and disjointed.

Additionally, lasers have introduced a few issues of their own ... the ablation laser process leaves Si 'slag' on the die walls thereby causing the die to 'hinge'. Furthermore, the heat generated by the laser (some are low power beam and/or water-cooled) can cause brittleness near the cut.

A couple of interesting technologies to keep watch on are:

1. "stealth" laser - a sub-surface cut using a laser to avoid disturbing sensitive patterns or metals in the streets;
2. multi-beam lasers — enabling single-pass cutting (a few exist today);
3. Plasma etching — very pricey, being staged to address the 450mm wafer evolution.

So, what's the answer? ... establish your requirements, contact the suppliers in the following Directory, and carefully assess your options! ☺

The advertisement features a collection of semiconductor test equipment arranged on a light-colored surface with a subtle grid pattern. The items include:

- A black rectangular socket with a gold-plated rectangular pin grid array (RPGA) package inserted.
- A black rectangular socket with a gold-plated square pin grid array (QPGA) package inserted.
- A black rectangular socket with a gold-plated circular pin grid array (CPGA) package inserted.
- A black rectangular socket with a gold-plated rectangular chip carrier (CC) package inserted.
- A black rectangular socket with a gold-plated rectangular chip carrier (CC) package inserted.
- A green printed circuit board (PCB) with a gold-plated rectangular chip carrier (CC) package inserted.
- A circular green PCB with a central gold-plated circular area and several smaller pads around it.
- A black rectangular socket with a gold-plated rectangular chip carrier (CC) package inserted.
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Advanced Dicing Technologies Ltd. Advanced Technology Center Haifa 31095, Israel Tel: +972-4-854-5222 www.adt-co.com		Method: Saw Automation: LU, WA, CD WD: 300 mm FR: 700 mm/s Models (3)	
Advanced Laser Separation International N.V. Platinawerf 20-G 6641 TL Beuningen (Gld), The Netherlands Tel: +31-24-678-2888 www.alsi-international.com			Method: Laser Automation: LU, WA, CD WD: 300 mm FR: 500 mm/s Models (3)
Aremco Products, Inc. P.O. Box 517, 707-B Executive Blvd. Valley Cottage, NY 10989 Tel: +1-845-268-0039 www.aremco.com		Method: Saw Automation: WA WD: 150 mm FR: CM Models (2)	
Disco Corporation 13-11 Omori-kita, 2-chome, Ota-ku Tokyo 143-8580, Japan Tel: +81-3-4590-1100 www.disco.co.jp	Method: Laser Automation: LU, WA WD: 300 mm FR: 1,000 mm/s Models (2)	Method: Saw Automation: LU, WA, CD WD: 300 mm FR: 1,000 mm/s Models (14)	Method: Laser Automation: LU, WA, CD WD: 300 mm FR: 1,000 mm/s Models (1)
Dynatex International 5577 Skylane Blvd. Santa Rosa, CA 95403 Tel: +1-707-542-4227 www.dynatex.com	Method: Mechanical Automation: CM WD: 200 mm FR: 100 mm/s Models (1)		
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EO Technics Co., Ltd. 864-4 Kwanyang 2 Dong Dongan-ku, Anyang, Korea Tel: +82-31-422-2501 www.eotechnics.com			Method: Laser Automation: CM WD: CM FR: CM Models (1)
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Micro Processing Technology, Inc. (MPT) 936 Dewing Avenue, Suite B Lafayette, CA 94549 Tel: +1-925-299-8940 www.microptech.com	Method: Mechanical Automation: CM WD: 200 mm FR: 1,000 mm/s Models (1)		
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Shibuya Kogyo Co., Ltd. Ko-58 Mameda-Honmachi, Kanazawa Ishikawa 920-8681, Japan Tel: +81-76-262-1200 www.shibuya.co.jp			Method: Laser/Water Automation: CM WD: CM FR: CM Models (1)
Synova SA Chemin de la Dent d'Oche CH-1024 Ecublens, Switzerland Tel: +41-21-694-3500 www.synova.ch		Method: Saw + Laser/Water Automation: LU, WA, CD WD: 300 mm FR: 600 mm/s Models (1)	Method: Laser/Water Automation: LU, WA, CD WD: 300 mm FR: 1,000 mm/s Models (4)
Thermocarbon Inc. 391 Melody Lane Casselberry, FL 32707 Tel: +1-407-834-7800 www.dicing.com		Method: Saw Automation: CM WD: CM FR: CM Models (1)	
Tokyo Seimitsu Co., Ltd. 2968-2 Ishikawa-machi, Hachioji-shi Tokyo 192-8515, Japan Tel: +81-42-642-1701 www.accrettech.jp	Method: Laser Automation: CM WD: 200 mm FR: 300 mm/s Models (2)	Method: Saw Automation: CD, CM WD: 300 mm FR: 1,000 mm/s Models (6)	

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# The Ever Changing PV Landscape

## An overview of worldwide PV production, new technologies and market demand.

By Bob Klenke [ITM Marketing]

**A**s the classic expression goes nothing is more constant than change. This could well define the dynamics that have impacted the photovoltaic (PV) industry during the past several years. Changes in production capacity, implementation of new technologies, and supply chain partnerships, as well as alterations in market demand, have all had a profound effect on the worldwide solar industry.

A common issue driving the upward growth of the PV industry is the need to meet increasing worldwide demand for energy, especially from developing countries and emerging markets such as Brazil, China, India and Russia. For example, China brings one coal-fired electric generating plant online per week to meet its growing energy demand due to ever increasing volumes of manufacturing. It is interesting to note that China will surpass the United States as the world's largest energy consumer measured in quadrillion BTUs per year. China's booming economy combined with an improved standard of living means their insatiable appetite for energy will exceed even that of the land of gas guzzling SUV's by 2015.

Alternative energy sources including nuclear, hydroelectric and biomass have been successfully implemented but have reached a plateau in long-term application due to regulatory concerns and/or supply limitations. Electricity generated by solar power, solar thermal heating and wind generated electricity present the greatest alternatives in terms

of fulfilling the dominant worldwide energy requirements.

Historically, the principal market driver for PV growth has been geopolitical factors such as the early adoption of incentives by Japan in the mid 1990's followed by widespread feed-in-tariff (FIT) programs in Germany, Spain, Greece and other European countries. Rollbacks in some of these FIT programs could shift PV demand to other regions of the world. At the same time, the Asia solar market experienced a significant growth 'spurt' beginning in the 2005-2006 time period lead primarily by China's efforts to 'green' their negative image as one of the world's leading polluters due to their reliance on aforementioned coal-fired electric generation.

### Production Capacity

For the past several years the worldwide solar industry operated under the premise that they could sell whatever they produced. This belief changed drastically at the end of 2008 because of the global economic downturn. The dramatic increase in domestic Chinese solar production combined with the 2008-2009 global economic contraction created a short-term overcapacity of polysilicon on the order of 2.5-3 times 'normal' demand, resulting in downward

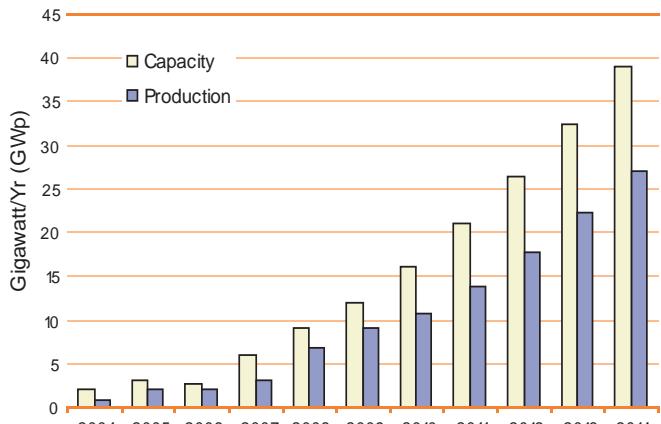


Figure 1. Projected worldwide photovoltaic capacity and production levels  
(Source: European Photovoltaic Industry Association)

pricing that is expected to last through the end of 2011. This oversupply condition also applies to the solar cell market, which is almost 3 times 'normal' demand, and could potentially last until 2012 when demand is expected to slowly approximate supply needs. For all these reasons, the current worldwide solar utilization rate of production vs. capacity is at an approximately 66% level (Figure 1).

This production-to-capacity utilization rate is expected to increase to approximately 75% beginning in 2012 and remain there through 2014. Additionally, this dramatic change in the market environment has resulted in approximately a 30-50% drop in the average selling price (ASP) of solar panels since mid-2008 with pricing expected to remain low until demand catches up with supply.

### Supply Chain Implications

In 2008, China was the preeminent world leader in production, producing

26% of all solar cells followed by Germany and Japan at 18% each, and the United States with 15%. Taiwan accounted for 13% of all global production, while the rest of Europe accounted for 7% with the remaining 3% scattered across the rest of the world.

Despite the projected return in demand forecasted for 2010, the 2008-2009 price erosion continues to constrict PV earnings. Some estimates persist that the recent decrease in PV pricing represents a permanent ratcheting down of price structures that could transform the PV industry into a more competitive marketplace with this collapse in demand likely to shift market share among the world's leading solar producers (**Table 1**).

This shift in market share was most evident when Germany's largest solar manufacturer, Q-Cells was directly affected by the Spanish government's decision that it could no longer afford

2009 Rank	2008 Rank	Company	Headquarters	2009 Revenue (\$M)	2009 Growth (%)	Market Share (%)
1	1	Intel Corporation	USA	\$32,410	-4.0%	14.1%
2	2	Samsung Electronics	South Korea	\$17,496	+3.5%	7.6%
3	3	Toshiba Semiconductors	Japan	\$10,319	-6.9%	4.5%
4	4	Texas Instruments	USA	\$9,617	-12.6%	4.2%
5	5	STMicroelectronics	France	\$8,510	-17.6%	3.7%
6	8	Qualcomm	USA	\$6,409	-1.0%	2.8%
7	9	Hynix	South Korea	\$6,246	+37%	2.7%
8	12	AMD	USA	\$5,207	-4.6%	2.3%
9	6	Renesas Technology	Japan	\$5,153	-26.6%	2.2%
10	7	Sony	Japan	\$4,468	-35.7%	1.9%
11	10	Infineon Technologies	Germany	\$4,456	-25.2%	1.9%
12	11	NEC Semiconductors	Japan	\$4,384	-24.8%	1.9%
13	16	Micron Technology	USA	\$4,293	-3.2%	1.9%
14	14	Broadcom	USA	\$4,278	-7.9%	1.9%
15	19	Elpida Memory	Japan	\$3948	+97%	1.7%
Subtotal top 15				\$127,194	-10.4%	55.3%
Others				\$102,723	-14.2%	44.7%
Total market				\$229,917	-11.7%	100.0%

**Table 2.** Top 15 semiconductor manufacturing companies 2009 revenue (Source: Gartner Dataquest)

2009 Rank	2008 Rank	Company	Headquarters	2009 Production (MW)	2009 Growth (%)	Market Share (%)
1	3	First Solar	USA	1,100 MW	+54.2%	12.1%
2	2	Suntech	China	704 MW	+24.7%	7.8%
3	4	Sharp	Japan	595 MW	+20.5%	6.6%
4	1	Q-Cells	Germany	586 MW	-3.4%	6.5%
5	7	Yingli	China	525 MW	+46.5%	5.8%
6	5	JA Solar	China	520 MW	+42.3%	5.7%
7	6	Kyocera	Japan	400 MW	+27.5%	4.4%
8	11	Trina Solar	China	399 MW	+47.3%	4.4%
9	9	SunPower	Philippines	397 MW	+40.3%	4.3%
10	12	Gintech	Taiwan	368 MW	+51.1%	4.0%
11	8	Motech	Taiwan	296 MW	+8.7%	3.2%
12	13	Ningbo Solar	China	260 MW	+32.6%	2.8%
13	10	Sanyo	Japan	260 MW	+17.3%	2.8%
14	15	E-Ton Solar	Taiwan	220 MW	+55.9%	2.4%
15	14	Schott Solar	Germany	218MW	+36.7%	2.3%
Subtotal top 15				6,848MW	+34.6%	75.1%
Others				2,282MW	+21.3%	24.9%
Total market				9,130 MW	+29.2%	100.0%

**Table 1.** Top 15 photovoltaic manufacturing companies 2009 production volume (Source: Photon International)Photovoltaic Industry Association)

to subsidize 500 megawatts (MW) of solar power installations in 2009. The resulting impact was immediate layoffs and cutbacks in European-based manufacturing plants with a corresponding shift by Q-Cells to a new factory in Malaysia in an effort to reduce manufacturing costs.

Even with these shifts in market share, the top 15 PV manufacturers control approximately 75% of the total available market with this higher market concentration equating to lower price competition. Contrast this with the semiconductor market where the top 15 semiconductor manufacturers control only 55% of the total available market resulting in increased price competition among suppliers (**Table 2**).

There are also distinct differences between the PV and semiconductor industries' manufacturing value chains. Whether carried out by integrated device manufacturers (IDM) or semiconductor assembly and test service (SATS) providers, typical

semiconductor manufacturing processes consisting of wafer fabrication, packaging assembly and test generally represents about 95% of the total value chain. In contrast PV manufacturing processes that generally encompass polysilicon wafer production, wafer fabrication, cell fabrication and module assembly account for less than 53% of the total PV value chain. The remaining 47% entails PV system assembly consisting of cables, chargers, mounting systems, tracking systems and integrated building solutions.

## Market Drivers

The cost of electrical power generated using solar technology is a complicated function of the PV system cost, the cost of grid purchased power, the average hours of available sunshine, and capital costs. In almost all geographic locations PV power generation is not yet competitive with grid purchased power. PV systems are on a long-term price experience curve based on a declining 7% compound annual growth rate (CAGR) where increases in module efficiency, capacity expansion and reduction in manufacturing materials and process costs will result in long-term parity with grid purchased power.

Traditionally, the majority of PV applications have been distributed on-grid installations due mainly to government incentives and regulations. Residential applications, including non-distributed off-grid and other consumer type applications, are expected to increase as economics reach closer to grid parity pricing. Since attaining parity with grid purchased power is the ‘silver bullet’ for economic justification of residential-based PV installations, which are generally excluded from major government stimulus plans, it should be noted that country-to-country cost variation has a significant impact upon non-commercial solar applications. For example, the average 2009 residential price of grid purchased electrical power in the United States

Base Technology	Share	Sub-Category Technology	Share
Single and Multicrystalline silicon (Si)	71%	Single and Multicrystalline silicon (Si)	71%
Non-Standard Crystalline silicon (Si)	10%	Hetero-junction with intrinsic (HIT)	4%
“		Inverted metamorphic multi-junction (IMM)	3%
“		String ribbon/edge-defined film (SR/EFG)	2%
“		Organic photovoltaics (OPV)	1%
Thin Film	19%	Cadmium telluride (CdTe)	11%
“		Amorphous silicon (a-Si)	6%
“		Copper indium gallium selenide (CIGS)	2%

**Table 3.** 2009 photovoltaic cell technology production share by type (Source: Yano Research Institute)

was \$0.1165/kilowatt hour, which is significantly lower than countries with regulated cost structures such as Germany and other European countries where grid purchased power is approximately the equivalent of \$0.20-0.25/kilowatt hour. Obviously these higher cost countries help the economic justification of residential-based PV installations which are often aided by highly popular geopolitical-based incentive programs.

## New Technologies

Various emerging technologies are under development to increase conversion efficiency and/or lower material and manufacturing costs. Examples of these are multi-junction monolithic cells and organic-based cells. Multi-junction monolithic cells exhibit a high conversion efficiency of 25-40% compared to polysilicon-based cells at 18%. Organic-based cells are significantly less efficient at 6-10% but exhibit greatly reduced material cost.

When all crystalline-based cell technologies are considered, approximately 81% of all PV cells manufactured worldwide are based on silicon wafers. While thin film technologies currently comprise only 19% of total PV, they retain the fastest growth rate due to the ability to reduce material costs as well as increase economy-of-scale with advanced factory automation techniques.

Previous estimates that thin film technology including various competing technologies such as cadmium telluride (CdTe), amorphous silicon (a-Si) and copper indium gallium selenide (CIGS) would grow from a historic rate of 10% to 25-30% of total PV production has not proven to hold true. Advances in technology notwithstanding, the widespread conversion to thin film technology has been slowed by the short-term oversupply of polysilicon which has depressed the pricing of crystalline-based PV cells and therefore made the conversation to thin film less financially attractive (**Table 3**).

It has been expressed that a ‘wild west mentality’ exists within the PV industry. To this extent, industry standards and production guidelines are being developed to address tabbing, stringing and glass-to-foil lamination to ensure solar cell product reliability. The IPC’s Solar Standards Committee has standards under development in seven key areas. Principle among these is E-12 that will set acceptance standards for the lamination of glass-to-foil solar modules and E-14 providing standards for the tabbing and stringing of silicon solar cells.

## Energy Consumption Patterns

Per capita energy consumption on a global basis is the result of a complex set of factors including supply availability, government policy and

market pressures. The consumption of oil, natural gas and biomass as well as electricity generated from coal, nuclear power and hydroelectric sources vary widely. Electricity generated by solar and wind power represents the fastest growing segment of the world's total energy portfolio.

Solar farms for example, also referred to as solar power plants, are becoming abundant in many countries around the world as a direct result of government planning as well as direct or indirect funding. Many utility companies across Europe and the United States are becoming increasingly interested in procuring PV power generating systems as one of the leading technologies for near-term renewable energy sources. Approximately 75% of German utilities currently use PV as part of their energy resource portfolio and close to 50% of US-based utility companies have PV resources in place or plan to implement them within the next five years.

## Market Demand

Due primarily to current incentive programs, Germany and Spain are the leading consumers of PV modules followed by Japan and the United States. Besides the indication that solar consumption is not a direct product of population density or gross domestic product (GDP), the graph below reinforces the expansion opportunity

for increases in solar consumption in countries such as Brazil, China, India and Russia (**Figure 2**). The growth of PV installations in 2010 will be led by a re-energized German market that has from a sluggish first-half of 2009. But this continued growth could stall if FIT programs are scaled back. Indications persist that this trend might continue as potential cuts in FIT programs could affect Germany and Italy in combination with budget concerns in Greece and Spain resulting in a shift of PV demand to other regions of the world.

By 2014, China is expected to be the world's largest PV market, surpassing both the United States and Germany, estimated to be the second and third largest markets by that timeframe. China will become a dominant force in both the supply of solar cells and PV modules as well as leading the demand for PV systems with utility scale solar power plants spearheading the country's PV market growth.

Recently China undertook a significant electrification program for rural communities inland from coastal population centers to offset the growing trend in urbanization. In lieu of reliance on sluggish, unprofitable, state-owned firms managed by the communist China central planning system to accomplish this undertaking, an ambitious program of regional solar power plants were, and still are, being constructed. Despite

China being the world largest importer of aluminum and copper on an unprecedented global scale as well as the leading recycler of scrap metal, the scarcity of copper and aluminum created a shortage of electrical transmission line capability thereby increasing the 'regionalization'

of China's solar industry.

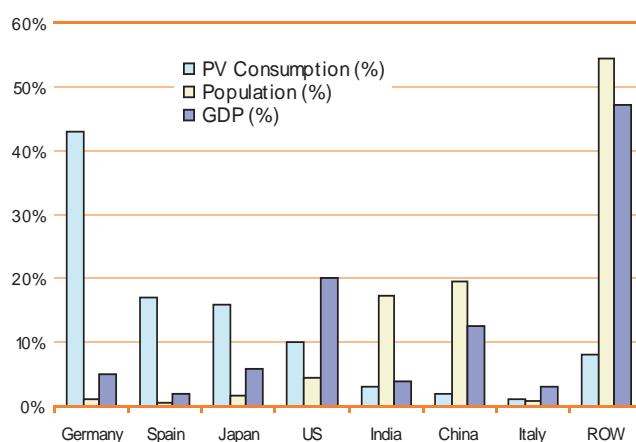
## Future Outlook

In addition to traditional crystalline cells and thin film technology, other technologies are emerging on the PV scene. Organic PVs (OPV) and dye-sensitized solar cells (DSC) are coming to the forefront. DSCs show particular promise since they generate electricity through sensitizer-added nanoporous semiconductor electrodes that convert light energy into electrical energy with low material cost and significantly do not require the use of silicon-based materials.

While not as dramatic as the downturn in 2008-2009, it is projected that quarterly PV shipments will look similar in 2010 with demand remaining slow through the first half of 2011 and then rebounding to previous high growth levels beginning in the second half of 2011. Additions in capacity planned by several leading and cost competitive PV manufacturers could potentially result in a risk of oversupply therefore driving down PV price points.

Equally dramatic will be the shift in market demand to alternative regions of the world other than today's dominant PV consumers where countries totaling 12% of the world's population account for 95% of total PV consumption. Developed PV markets such as Germany, Spain, Japan, Italy and the United States will be surpassed by developing countries and emerging markets including Brazil, China, India and Russia. A fitting example of this trend is the fact that the world's largest solar power plant is being constructed by a US-based PV supplier — in Inner Mongolia.

Bob Klenke is the managing director of ITM Marketing, a full service market research and technical marketing firm and is a staff member of ITM Consulting. [\[bob\\_klenke@itmconsulting.org\]](mailto:[bob_klenke@itmconsulting.org])



**Figure 2.** Photovoltaic consumption versus population and GDP (Source: Navigant Consulting, CIA World Factbook)



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# EMERGING TRENDS



## A Good Place to Place Your Bets (in ICs)

By Sandra Winkler, Senior Analyst [New Venture Research, [www.newventureresearch.com](http://www.newventureresearch.com)]

The semiconductor industry took a beating in early 2009, but sprang back sooner than many to end the year in better shape than initially anticipated. Small, handheld, always connected devices sold well even in the depths of the recession. Items priced under \$300, even \$400, still sold. Smart phones were all the rage. PCs shrank to the smaller, more portable notebooks, which, in turn, shrank even further to the netbook. E-readers and other handheld consumer items gained market acceptance. We do love our gadgets.

Going into the future, what would be good markets for a semiconductor company to be in? Areas that offer one or more of the following:

- High product volumes
- High, or reasonable, growth potential
- High volume of ICs per individual product

There are many ICs that fit within these categories:

- MPUs
- Standard cell / PLD
- DRAM
- Flash
- Analog — communications
- Analog — voltage regulators
- Special purpose logic chips of all types, including consumer, computer, communications, and automotive

### Package Solutions

With so many products being wireless, baseband products will continue to be in demand. They are being included in stacked options such as package-on-package (PoP) in increasing numbers. Memory, included in this list, is also being placed in both die stack and PoP options in large numbers. Even PLDs can be found in stacked solutions. And logic devices have been included in PoP solutions from the inception of package-on-package.

Many companies are looking at through-silicon vias (TSVs) as an interconnection method for devices within stacked packages, and as a way to increase performance, improve signal integrity, and reduce parasitics. Elpida Memory is an early adopter of this technology and has a number of memory products in production, as have several other memory companies. IBM is planning on moving the SRAM off the MPU and connecting it in a stack with TSVs. QUALCOMM is taking a serious look at this technology. PLD companies are reviewing this technology to place their devices in a homogeneous stack.

Most stacked package options are fitting within the FBGA outline, although QFN options are gaining acceptance.

QFN as a package solution has been gaining in popularity for some time, extremely popular for analog and simple logic chips, of which there are many. Coming onto the market is a new twist for this package, and that is to have inner leads on the leadframe to create a perimeter array pattern on the leads, thus allowing this package solution to reach into higher I/O counts. This would allow it to compete with low-cost FBGA packages, to provide an even lower cost option, as leadframes are less expensive than substrates.

The same goes for WLPs, giving the package a new twist to reach into higher I/O counts by creating the overmold WLP, in which the backside is coated with overmold to create a larger surface on the face in which to place the electrical traces.

Not that there is a shortage of a need for packages in the low I/O ranges. Indeed, most analog and simple logic chips are of low I/O, and they are plentiful. SO and SOT solutions are still in demand, especially for voltage regulators, which are in all electronic devices.

What is being conveyed here is that both older and newer forms of packages are in demand, and new twists are giving new life to existing package solutions. Being diversified is a safe bet.<sup>SR</sup>

# WHAT'S NEW!

## X-ray Inspection System

Nordson DAGE announced that it will showcase its XD7600NT100HP X-ray inspection system at this year's SMTA International Electronics Exhibition and Conference, Oct. 26 - 27th in Orlando, Florida. The XD7600NT100HP offers 100 nm (0.1 $\mu$ m) feature recognition for finite analysis of challenging inspection applications. Due to its 2.0M pixel digital imaging system, oblique angle viewing of up to 70° around any point of a 16" x 18" (407 x 458mm) inspection area is possible without compromising magnification.

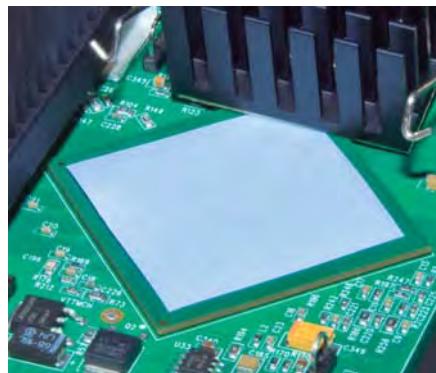


The XD7600NT100HP combines digital acquisition technology of the XiDAT 3.0 imaging system with the company's proprietary ImageWizard software, and is configured with dual monitors. This allows operators to view X-ray images on one 24" widescreen LCD monitor while simultaneously providing the fault locations in a detailed X-ray navigation map on the second LCD display. The system is available with a high-power NT tube that is able to retain sub-micron feature recognition at full power.

Additionally, the system can be equipped with computerized tomography (CT) option providing 3D modeling and volumetric measurement of solder joints suited for analysis of solder interconnections for critical applications such as stacked die, MEMS, package-in-package (PiP) and package-on-package (PoP). [[www.nordsondage.com](http://www.nordsondage.com)]

## Thermal Interface Pads

Keratherm U 90 and U 80 silicone-free thermal interface materials (TIMs) from MH&W International provide high thermal conductivity where contamination threats



prevent the use of silicone-based thermal pads. U 90 is a ceramic-filled polyurethane film that has a thermal conductivity of 6.0 W/mK and thermal impedance of 0.05 K in²/W. U 80 is the lower cost version, also silicone-free, which provides 1.8 W/mK of thermal conductivity and 0.11 K in²/W of thermal impedance.

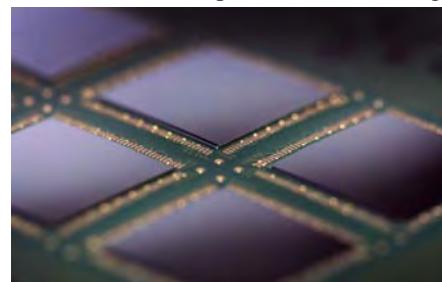
Both TIMs are available with a light tack adhesive to keep them in place during assembly or pre-attached to heat sinks. The light tack adhesive can be compared with adhesives used on repositionable notes. The TIM pads won't be damaged when removed from mounting surfaces, which is a common problem when stronger adhesives are used. Typical applications these TIMs include medical devices, laser equipment, LED lighting, solar energy, disk drives and automotive electronics. [[www.mhw.intl.com](http://www.mhw.intl.com)]

## Wafer Backside Coating for Stacked Packages

With the introduction of Ablestik WBC-8901UV, Henkel extends its wafer backside coating (WBC) portfolio to stacked die packages, addressing the demanding requirements of multiple die stack applications for the memory market segment, including packages such as TSOPs, MCPs and FMCs (Flash Memory Cards).

Applied via a spray coating method following the wafer thinning process, Ablestik WBC-8901UV is precisely deposited across the back of the silicon wafer following which the material is B-staged using a UV irradiation process. After this step, dicing tape is laminated to the wafer, backgrinding tape is removed, and the wafer is diced in preparation for die pick-up and placement.

The unique formulation of the WBC offers an alternative to current film-based solutions for stacked die packages, with a reported 30-50% total cost of ownership. Additionally, process flexibility is affected because it allows for packaging specialists to adjust die attach thickness based on specific manufacturing



requirements and use their dicing tape-of-choice, rather than be limited by the pre-determined thickness of film materials that incorporate dicing tape. Henkel reports it is currently partnering with spray technology and backgrinding equipment manufacturers to deliver an integrated, in-line process solution for this unique WBC advance. [[www.henkel.com/electronics](http://www.henkel.com/electronics)]

## Fine Pitch Bump Adapters

As part of the Correct-A-Chip series, Aries Electronics' Fine Pitch Bump Adapters were developed to allow higher pitch devices to be used on smaller pitch boards. The adapter tops have landing pads that can be designed to accept any device on any pitch and settle into fine-pitch footprints including thin-shrink small outline packages (TSSOP) and quad flat packages (QFP) with pitches down to 0.40mm. In addition, the adapter bottom has raised connection pads up to 0.010" (0.25 mm) that provide easy mounting of the adapter to the target board.

Reclaimed adapter board space allows for manufacturers to add components to the design at minimal cost. Additionally, the Fine Pitch Bump Adapters allow for BGA device integration in boards with smaller pitches that previously could not be used together.

Fine Pitch Bump Adapters are available in panelized form, as an adapter only, or as a turn-key solution with devices mounted. The boards are 0.062"

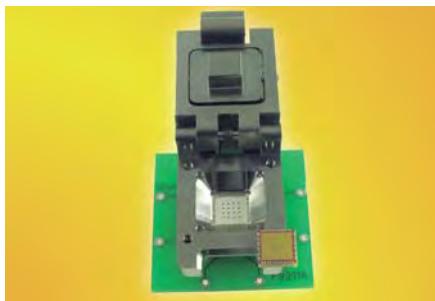


(1.57mm) thick FR4 or Rogers 370 HR, with 1oz. copper traces on both sides. The non-solder mask defined (NSMD) pads are finished with electroless nickel immersion gold (ENIG). The apparatus can operate up to 221°F (105°C) for FR4 and 266°F (130°C) for lead-free. The new adapters are available in tape and reel for high speed SMT assembly and can be manufactured for RoHS compliance. [\[www.arieselec.com\]](http://www.arieselec.com)

### Stamped Spring Pin Socket

Ironwood Electronics introduces the CBT-QFN-7002, a stamped spring pin socket that addresses high performance requirements for testing UART serial to parallel data converters. The contactor is a stamped spring pin with 26g actuation force per ball and cycle life of 500,000 insertions. The self-inductance of the contactor is 0.88 nH, insertion loss < 1 dB at 15.7 GHz and capacitance 0.097pF. The current capacity of each contactor is 4 amps at 80°C temperature rise. Socket temperature range is -55 to +180°C.

The socket also features a low profile snap lid and has a wave spring with swivel compression plate for vertical force without distorting device position. The CBT-QFN-7002 is specifically configured to test 7 x 7mm, 0.5mm pitch, QFN packages that have 48 positions with center ground pad. The socket is mounted using supplied hardware on the target PCB with



no soldering, and is said to require the smallest footprint in the industry. This allows inductors, resistors and decoupling capacitors to be placed very close to the device for impedance tuning. This socket can be used for quick device screening and data conversion functional test applications that have the most stringent requirements. [\[www.ironwoodelectronics.com\]](http://www.ironwoodelectronics.com)

### Low Current Land Grid Array Fuse

AVX Corporation has expanded its Accu-Guard Low Current Series with the addition of a low-current, UL E141069 approved, RoHS compliant 0402 fuse. This miniature fuse utilizes thin film and land grid array (LGA) technology to provide an accurate 125mA current rating in a small package. The thin-film technology allows for precise control of the component electrical and physical characteristics that is not possible with standard fuse technologies, forcing end-device manufacturers to choose between size and current rating.



Reportedly the lowest current fuse available today, it is suited for use in handheld devices like cell phones, PDAs, two-way radios, and video and digital cameras, in addition to hard disk drives (HDD), LCD screens, computer instrumentation, battery chargers and rechargeable battery packs. [\[www.avx.com\]](http://www.avx.com)

### BGA Clamshell Sockets

E-Tec Interconnect's "economy" ClamShell sockets for BGA, LGA & QFN chips feature a locking system that allows for controlled distribution of locking forces with 1 or 3 locking pegs depending on pincount.

The sockets feature an open top retainer for improved heat dissipation and access to die. Pressdown forces can be pre-set with a stopper screw and re-



adjusted manually, and the easy open/close method requires no screws or tools.

The small body size makes these sockets ideal for use on high-density PCBs, requiring little board space. They are available in SMT, thru-hole and solderless compression type for either low or high pin count configurations; with raised SMT pins to lift socket above components on board; and with probe pin and elastomer sockets. [\[www.e-tec.com\]](http://www.e-tec.com)

### Worldwide IC Packaging Market Report

Now available from New Venture Research, The Worldwide IC Packaging Market, 2010 Edition, offers an in-depth look at the worldwide integrated circuit (IC) packaging market.

Individual IC device market forecasts are provided for units, revenue, and ASP, from 2008 through 2014. The package solutions for each of these markets are then forecast, broken down into I/O ranges. In a separate chapter, package types are rolled up to deliver an overall worldwide forecast divided into 12 different package families plus bare die solutions. Additionally, forecasts for die mounted using direct chip attach (DCA) methods were developed.

This report is intended to aid companies associated with the IC packaging market in forecasting demand for their own products. [\[www.newventureresearch.com\]](http://www.newventureresearch.com)

# MARKET FORECAST

## Walker's September Forecast: Recovery, Boom, Growth, What's Next?

By Françoise von Trapp, Contributing Editor [[3D InCites](#)]

**W**hile macroeconomics continues to improve, questions still pop up about the strength of this recovery. At MEPTEC's annual September Forecast Luncheon, Sept. 9, 2010 at Dobson Ranch Inn in Mesa AZ, Gartner Dataquest's Jim Walker offered both explanation on the recovery thus far, while offering his predictions and reasoning for what's to come in the next few years.

### Economy at a Glance

Giving a broad view of the world economy, Walker explained that while India, China, and Southeast Asia are seeing strong growth, the US and Europe are still lagging, putting a drag on worldwide growth. As China's middle class continues to grow, the country has become the largest buyer of consumer electronics while in the US and Europe consumer spending and sentiment is stalling as concern continues around unemployment, the real estate market, consumer and commercial debt.

Basically, we're dealing with a mixed bag resulting in confused signals within the industry. On one hand, Walker noted, current market data indicates strength, while on the other announcements and anecdotes are cause for concern. It appears that the industry is approaching a revenue peak, the question is, notes Walker, will the inevitable slowdown cause a revenue adjustment?

### Market Overview

Summarizing the overall semiconductor device and applications market, Walker predicts revenue is still poised to hit record highs in 2010 reaching 31.5% growth driven by the PC, cell phone and LED markets, although he doesn't rule out a downturn scenario. While the PC supply chain is expected to experience a correction, DRAM will be the fastest growing device type in 2010. There will also be a "modest chip correction" in the second half of 2010 as semiconductor growth aligns with system growth.

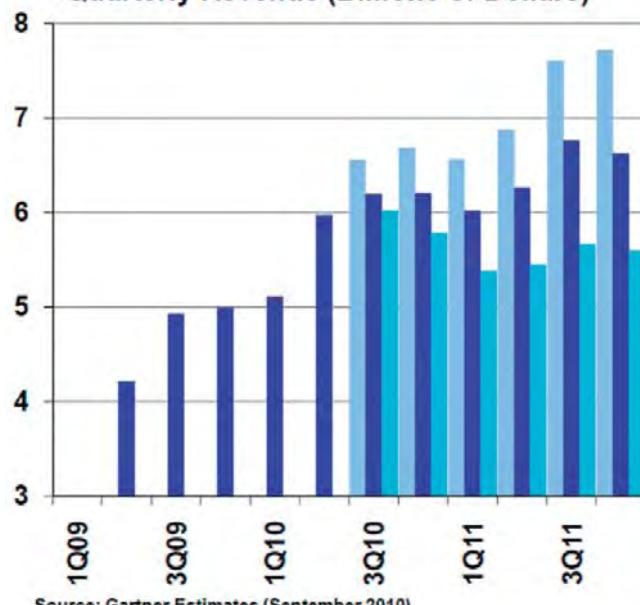
Walker says there's strong growth across the board in capital spending, with mostly foundries spending on capacity buys. According to Gartner data, the top 5 capital spenders in 2010 are Samsung, TSMC, Intel, Global-Foundries and Hynix. And for the first time ever, two packaging companies, ASE and SPIL, made the top 20. "It's a milestone, in my opinion, that the packaging guys are starting to spend on capex," said Walker, saying that it's due largely to the transition from gold to copper wire bonding.

### Growth in Packaging

After 3 years of market declines, Walker says that the back-end equipment market is expected to surge with better than 130% growth. He says growth for advanced package tooling will be solid, and memory ATE and copper wire bonders will be top performers. However, 2011 could be impacted by uncertainty of market conditions. Q4 2010 will provide clues to strength of 2011.

Technology buys and foundry and memory capacity buys are what's driving equipment spending. Walker predicts that while fab growth will continue, it will begin to slow down in

Quarterly Revenue (Billions of Dollars)



Source: Gartner Estimates (September 2010)

Figure 1. SATS Market quarterly revenue scenarios

2011 and 2012 due to ordering in 2010. Memory will experience an over-investment through 2012 and will drive a 2013 downcycle. Walker suggests that key questions to pay attention to moving forward: Is the current surge in chip demand sustainable in the near term? Will chip manufacturers respond to any kind of negative economic news with capex pushouts? Which chip manufacturers will be able to invest, and which will go fabless/asset “lite”?

“The packaging value of the industry is going up because we are the enabler of Moore’s Law,” noted Walker. “Most of the integration in a cell phone, because time-to-market is so short, is via packaging.” He added that design wins of SOC-type products have gone down, and with that the value of the back-end can increase in a five year period. Front-end equipment manufacturers are seeing this opportunity to serve the back-end needs in wafer-level packaging and TSV. “Value-add appears to be growing in the back-end,” he said.

However he doesn’t see that the TSV market has driven equipment buys for companies like TSMC or Elpida, regardless of their announcements of outfitting 300mm TSV lines. “Elpida announced they’d begin production on TSV in June 2010, but I still haven’t seen anything on that yet.” He said, adding that it will be the middle of next year before we see any TSV production, and that will be in pilot lines only. Walker expects there won’t be any measurable volume of TSV devices for several years.

Addressing the outsourced semiconductor assembly and test (OSAT) market, based on quarterly revenue forecast scenarios, Walker predicts an expansion of 37% this year and eventually will have 50% of the packaging and test market (**Figure 1**).

SATS vendors are focusing on advanced packaging and copper bonding capacity; the latter because of the increase price of gold. Memory assembly and test capacity is being expanded.

The top 5 SATS vendors are currently ASE, Amkor, SPIL, STATS ChipPAC, and Powertech Technologies. “The one that has grown the fastest over the past 5-10 years is Powertech Technology,” says Walker. He said the company only

handles memory package and test, and has weathered the storm using financial acumen, understanding the market, and having a guaranteed customer to supply through the downturn. He noted that ASE has taken market share from SPIL, most likely because SPIL didn’t invest in copper wire bonders and ASE was aggressive. “They’re all experiencing nice growth in the marketplace,” he said, thanks to good strategies and good relationships with their customers.<sup>8</sup>

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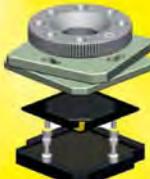
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SMTA International  
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<http://smta.org/smtai/index.cfm>

### October 28-29, 2010

KGD Workshop  
Santa Clara, CA USA  
[http://www.semi.org/en/eventstradeshow/ctr\\_028107](http://www.semi.org/en/eventstradeshow/ctr_028107)

### October 31, 2010 November 4, 2010

IMAPS  
Raleigh, NC USA  
<http://www.imaps.org/imaps2010/index.htm>

### November 2-4, 2010

ITC – International Test Conference  
Austin, TX USA  
<http://www.itctestweek.org/>

### November 10, 2010

MEPTEC Q4 Semiconductor Roadmaps:  
Santa Clara, CA USA  
<http://meptec.org/meptecroadmaps20.html>

### December 1-2, 2010

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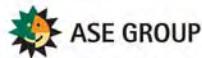
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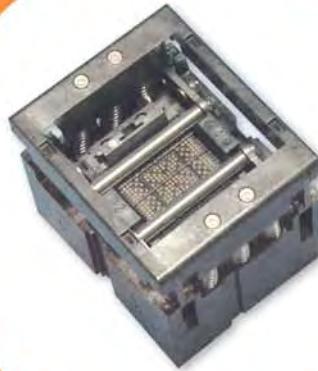
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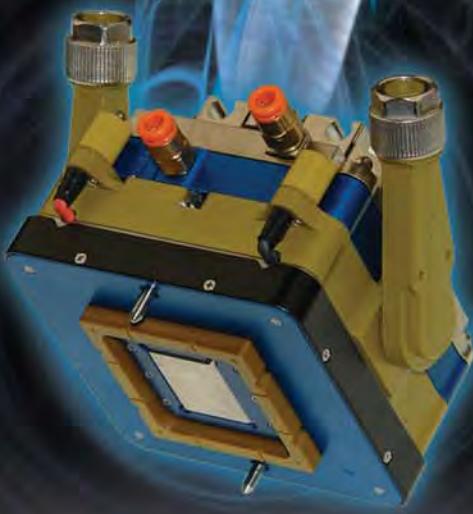


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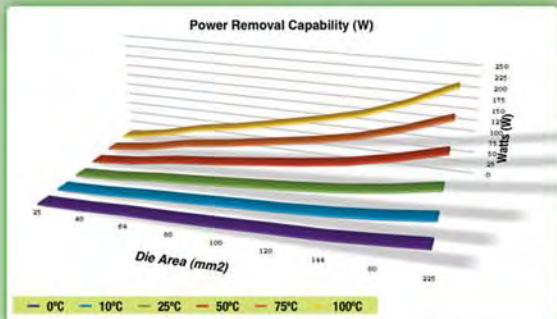
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