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The Future of Semiconductor Packaging

Volume 19, Number 4

July • August 2015

Thermocompression bonding

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- Wafer-level packaging
- Glass-based interposers
- Cu-pillar flip-chip assembly
- High-temperature electronics
- Integration of polymer optical waveguides
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- Addressing the challenges of custom and standard MEMS products





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Package size continues to shrink while the demand for increased performance and reduced power dominate the market. The preferred solution is one that extends advances in IC technology beyond the fab to include 2.5D and 3D assembly. New high-UPH processes using thermocompression bonding (TCB) enables this next-generation of cost-effective high-performance computing and graphics products.

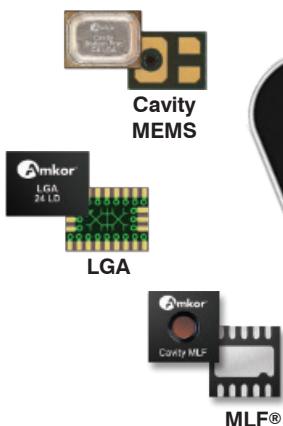
Photo courtesy of Kulicke & Soffa.

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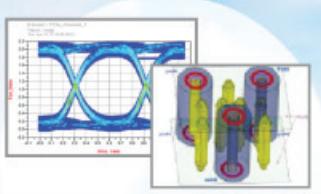
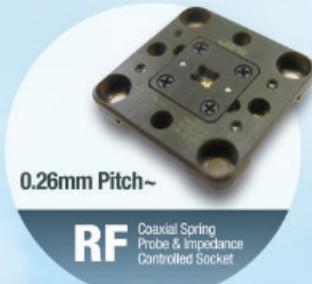
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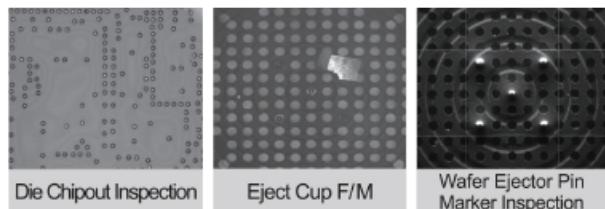



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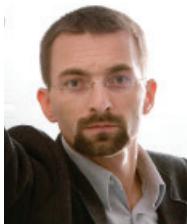
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Addressing the challenges of custom and standard MEMS products

By Vincent Gaff *[Trionics Microsystems]*

With a well-established presence in the electronics industry, from niche markets with high added-value to high-volume consumer applications, MEMS devices are at the heart of product innovation. But many new opportunities have yet to be explored, with new hurdles that the MEMS value chain needs to lower by reinventing its model.

The MEMS ecosystem has always gathered itself around one common objective: bring value to match the industry expectations and better compete with other promising technologies. Today, growing markets such as aeronautics and security, medical, consumer electronics, the Internet of Things (IoT), and automotive require more and more innovation to deliver custom products in line with the high level of expectations of very specific applications. In this context, some criteria are obviously emerging such as these key success factors for future applications:

- **People:** engineers must integrate a broad range of high-level skills (simulation and design, manufacturing, packaging, test and calibration, etc.) through an educational level in line with the expectations of the ecosystem (**Figure 1**). Once built and structured, these experienced teams are able to keep up with the fast transitions of the targeted markets, thereby acting as a strong leverage to meet customer requirements.
- **Technology expertise:** a complete and proven portfolio of technology blocks (acquired through R&D programs and various customer projects) is needed to better understand and implement the



Figure 1: A complete portfolio of equipment and MEMS process steps combined with high-level skills from experienced engineering teams are able to fulfill an extensive range of development and custom process manufacturing requirements through a close support to customers.

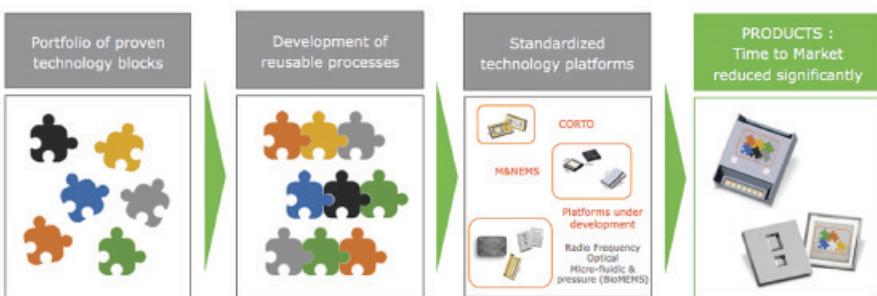


Figure 2: Expertise in the design and manufacturing of innovative nano and microsystems leads to a library of reusable technology blocks and standardized platforms enabling an industrialization of the technological approach.

requirements for current and future applications (**Figures 2 and 3**). Coupled with tailored processes (wafer-level packaging [WLP] solutions with integrated vacuum, through-silicon vias [TSVs], etc.), the combination is then tailored for an extensive range of manufacturing and research developments.

- **Manufacturing flexibility:** from custom products for niche markets with high-added value up to hyper volumes for consumer applications, agility is a must-have to execute customer projects within the right timeline. The strategic approach to address key regions of the world must be defined by integrating a strong support in order to offer a local source of supply with responsive, proactive and knowledgeable technical support.
- **Collaboration:** each of the relationships built over the years

within the ecosystem must be based on a collaborative approach. Beyond competitive and intellectual property topics that remain sensitive to handle, there is still plenty of room for all kinds of players (research institutes, startups, customers, and even competition) to understand final uses and future needs for product co-developments, thus accelerating the innovation cycle through an improved roadmap.

Taken together, it is easy to notice that the criteria listed above constitute a powerful leverage to improve the innovation phase and help the MEMS value chain follow fast market and technology transitions. Developing a brand new custom MEMS device, however, presents several hurdles: 1) It requires investments of several millions of dollars; 2) It needs a

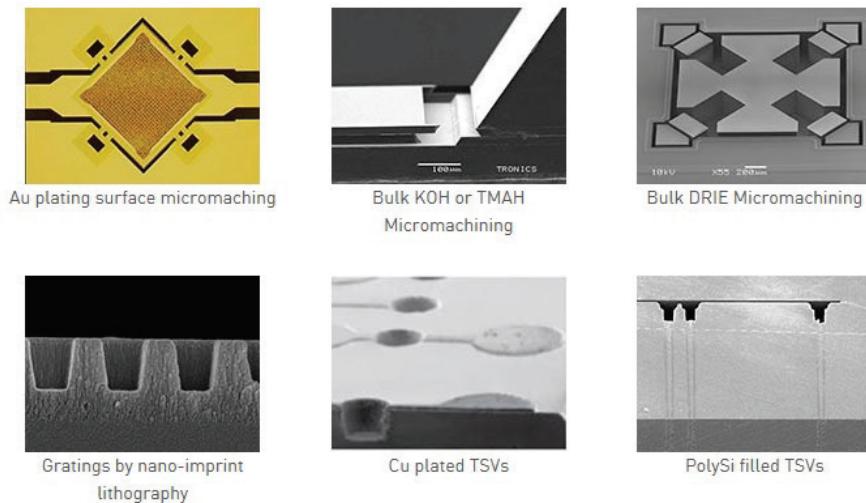


Figure 3: Specialized processes for custom devices are developed and industrialized, including surface and bulk micromachining technologies, as well as thin- and thick-films processes.

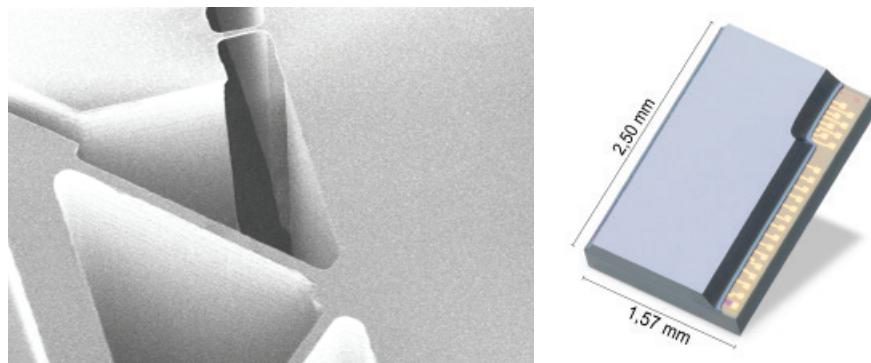


Figure 4: Combining a large portfolio of proven technology blocks with reusable processes, the standardized technology platform approach has enabled us to achieve 6DOF demonstrators that are currently the smallest combo sensors of the industry on the same, single die (less than 4mm²).

schedule of 1-3 years to set up specific manufacturing technologies; and 3) It has product performance improvement and qualification phases that are often laborious to achieve and can take from 2-5 years depending on the product performance requirements.

To overcome the issues listed above, it is necessary to anticipate them as much as possible and build products on standardized and validated technology platforms (**Figure 4**). Conceived with fixed technology features (e.g., anti-stiction, long-term proven hermeticity, compatibility with standard assembly flows, etc.) and proven and characterized functionalities on a first test vehicle (e.g., multi-axis inertial product, micro-mirror, single RF switch,

etc.) this approach can be used for a greater variety of products.

The key is to focus innovation on design, which must rely on proven design kits – in accordance with technological design rules that enable good production yields from the first pieces of silicon – so the targeted specifications can be better reached. Such a model has one main advantage beyond all the others: to serve multiple products, multiple applications, and multiple user environments, with a lower cost-of-ownership, a shorter development time, and higher production yields.

Once these platforms are established and controlled, and the industrialization phase done on a first pilot product, the following ones can be developed

more quickly by focusing on product integration, performance improvements and qualification cycles. Indeed, in that case all the process development and technology platform qualification work has already been done in the previous steps. Customers can quickly get first functional prototypes and directly address and focus their development on the electronics, the packaging, and the integration. Moreover, customers can be supported with design kits for the development of their prototypes/products in a similar way to the semiconductor fabless approach. The business model is thereby reinvented, representing a viable solution for the MEMS industry to lower the hurdles of current and future applications.

Beyond the advantages noted, there is a long way to go for the standardized technology platform approach before it can address all the requirements of custom MEMS devices, and thus overcome the challenges of cost, performance and integration. MEMS is still an emerging industry and some of these platforms are under development (e.g., for RF switch circuits, optical mirrors, etc.), while some others already exist (e.g., pressure sensors, inertial sensors: accelerometers and gyros). Whatever the level of maturity, each one of them will remain limited to a certain product family (one platform for inertial MEMS, a different one for RF MEMS switch circuits, another one for optical micro-mirrors, etc.). Work is currently in progress at some major industry players aiming to keep pace with innovation for future applications in growing markets, such as optical systems, RF devices, and BioMEMS.

Biography

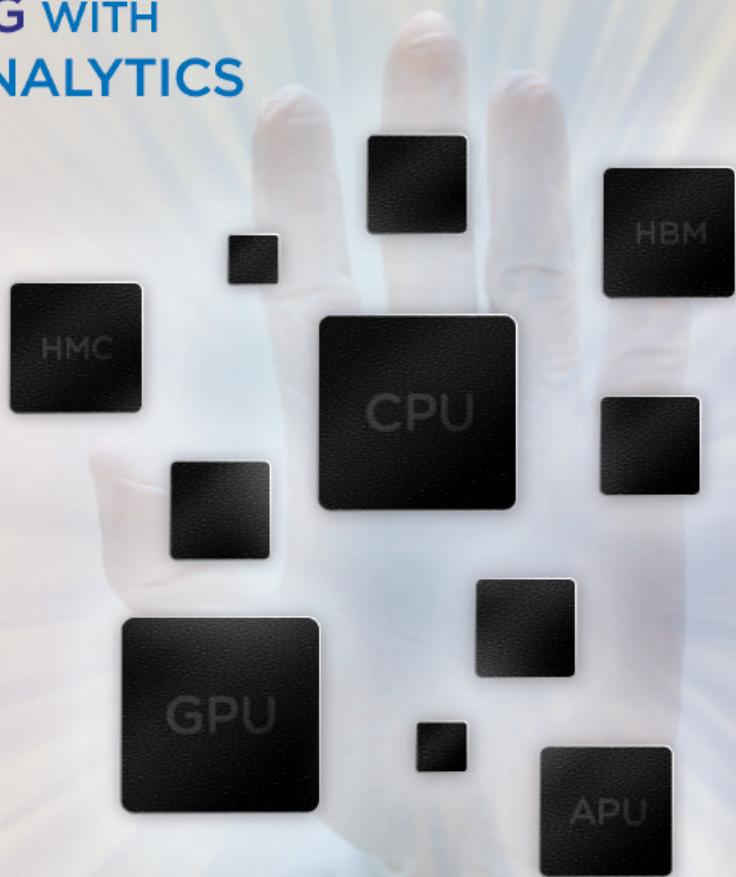
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GUEST EDITORIAL



Europe - a growing hub for advanced packaging

By António Barny [[NANIUM, S.A.](#)]

On June 18-19, 2015, major European players in the field of semiconductor packaging, assembly and test met at NANIUM in Portugal to showcase their capabilities, discuss the current state of advanced packaging, their projections for the future, what they believe will be needed to strengthen this industry in Europe, and how to better work together throughout the complete semiconductor supply chain.

The continuous need for miniaturized system integration that allows for higher performance at less space and lower cost at the package and module levels serves the "More-than-Moore" domain. The present times are marked by a game-changing environment both in terms of the concepts of what is made, and the ways in which the industry makes it.

There is a tremendous rise of applications seen in the field of wearables, the internet of things/everything (IoT/IoE), and smart cities. Additionally, further system integration for fast mobile connectivity devices and integrating die-partitioned large system-on-chip (SoC) into new system-in-package (SiP) solutions with SoC-like performance are increasing. To implement these applications fast and efficiently, collaborative work in joint projects and consortia together with institutes, academic, suppliers, service providers and customers seems to be the most promising way. New business models enforcing co-design and co-development along the complete supply chain from the very beginning of the development project are needed to meet the first-time-right and time-to-market needs, as well as to be competitive.

This changing atmosphere certainly represents a big opportunity for Europe to benefit from the knowledge and know-how it has been gathering throughout

the years in all the areas of the supply chain. Furthermore, some reinforcement of manufacturing in Europe is needed to close the "valley of death" between new development and its manufacturability in high-volume manufacturing lines. To address and discuss this topic with European decision makers was also an objective of the meetings.

The "SEMI Packaging Tech Seminar," organized by SEMI, the international association for Semiconductor Equipment and Materials suppliers, had 180 attendees and focused on the most recent industry and market developments. It showcased the capabilities in Europe and international trends in terms of advanced packaging manufacturing. The day after, approximately 60 participants gathered together for the European Semiconductor Packaging, Assembly and Test (ESPAT) Industry Interest Group, to discuss the next steps on working more closely together in Europe to get prepared for the upcoming challenges with respect to the international competitive situation facing the industry. The team decided to become a SEMI ESPAT Special Interest Group (SIG) within SEMI. The objectives of the group were summarized, and the charter and by-laws were discussed and approved. For more information, please refer to: <http://espap.weebly.com>

The events took place at the headquarters of Europe's largest outsourced semiconductor, assembly, and test (OSAT) supplier, NANIUM, S.A., located in Porto in the north of Portugal. Throughout the event, what became clear was the competence and advanced packaging and test know-how available all over Europe in applications as diverse as MEMS, sensors, mobile, automotive, industrial, health and healthcare, aerospace, and security.

Indeed, nowadays Europe puts forward a very competent offering in

advanced packaging, both where it comes to research close to the industry needs, equipment and material supplier activities, and advanced packaging and test services provided by the OSATs and test houses. All participating companies agreed that this current situation provides a strong basis to tackle the booming opportunities expected in the near term.

Over the past few years, we have witnessed European companies' increasing importance in niche markets. On the other hand, today's advanced packaging is less dependent on the Asian supply chain because the focus is not so much on conventional packaging technologies, such as wirebond and flip-chip interconnect-based packages using leadframe and organic substrate as interposers and packaging less complex single-die solutions. Rather, it is focused on smart system integration for more demanding applications in terms of performance, security and reliability, as well as the customer's demand for close cooperation with the highly educated and experienced engineering teams of the partners.

Europe's message is clear: It relies not only on the big IDMs (Infineon, Bosch, NXP, STMicroelectronics, austriamicrosystems), but also on its OSATs and test houses, small or large (e.g., NANIUM, First Sensor Microelectronic Packaging, Sencio, GS Nanotech, e2v, Rood Microtec, Presto Engineering), and R&D centers distributed all over Europe (e.g., CEA-Leti, Fraunhofer, imec).

Biography

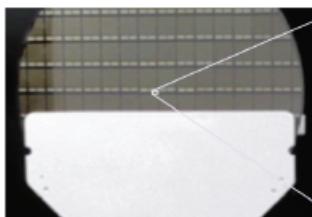
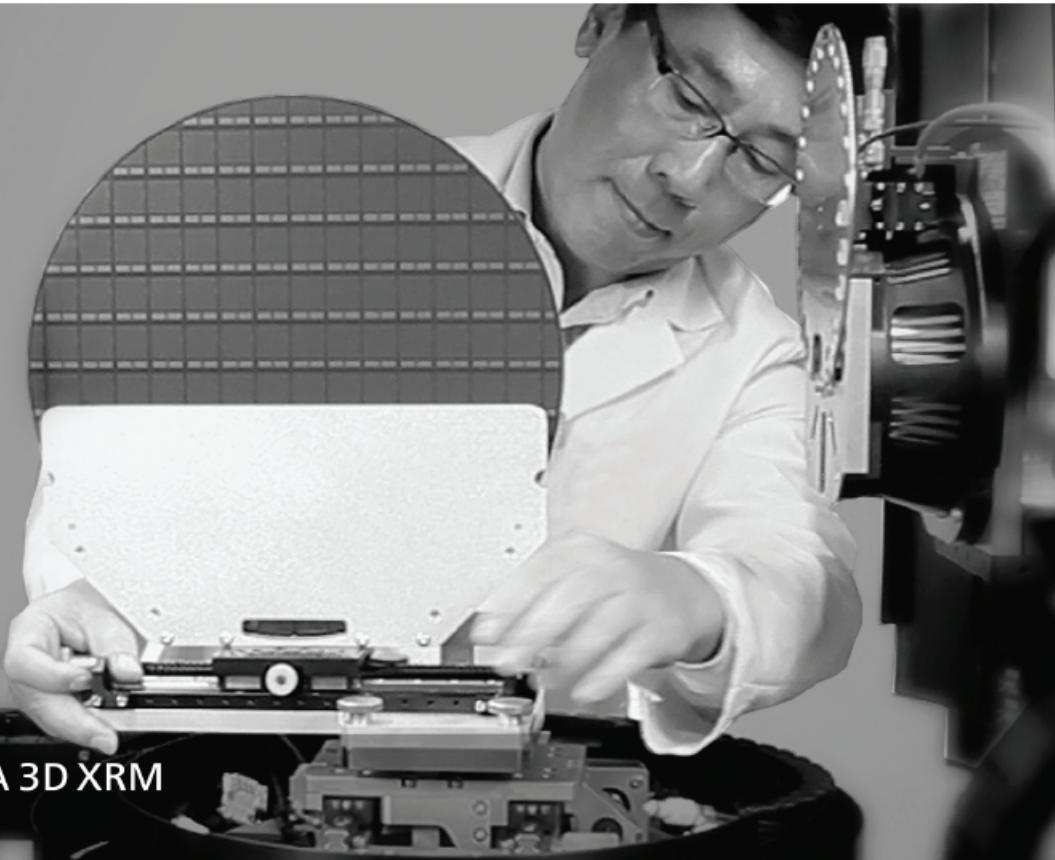
António Barny received a university degree in Computer & Electronics Engineering, and a Master's degree in Entrepreneurship and Innovation. He is a Business Development Manager at NANIUM, S.A.; email antonio.barny@nanium.com

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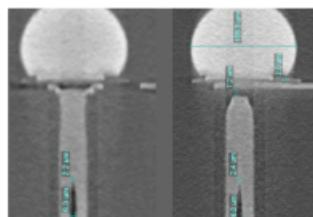
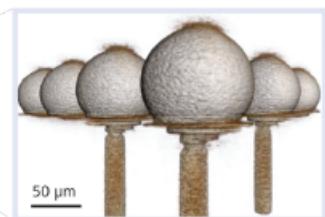
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INDUSTRY NEWS



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High-density fan-out: evolution or revolution

Rama Alapati

*Director, Package Architecture & Customer Technology (PACT)
GLOBALFOUNDRIES*

Continued form factor and I/O density scaling pressures have necessitated innovation in wafer-level packaging technologies, including high-density fan-out at leading edge Si nodes. A thorough analysis of the end applications reveal clear I/O density envelopes for multi-die fan-out packages. Industry solutions today are highly fragmented, enabling disruption in the application space. Silicon foundries entry into the fan-out space also clearly highlights opportunities for value capture in this expanding package format. For traditional players in this field, “collaborative competition” enables a new way of connecting with the foundries and business models, and also ensures this new paradigm is possible and viable.



2.5D/3D IC - examining low-cost alternatives

Sitaram Arkalgud, PhD

*VP, 3D Portfolio & Technologies
Invensas Corporation*

Keynote Address - Day 2: Wednesday, October 14, 2015

2.5D and 3D products have entered the semiconductor market, albeit at the higher end of performance and pricing. The penetration has been slow, primarily due to the high cost of Si interposer technology, and, consequently, new TSV-less technologies have recently been proposed. This presentation will examine the market dynamics, the segments where TSV based products have made significant inroads, and where alternative technologies could have an impact.



Panel Discussion: Tuesday, October 13, 2015

Fan-out WLP panel processing: will it happen and what will it be?

Moderator: E. Jan Vardaman [TechSearch International]

*Panel Members: Tim Olson [Deca Technologies],
Beth Keser [Qualcomm], Bill Chen [ASE],
Curtis Zwenger [Amkor], Jose Campos [NANIUM]*

With the demand for thin-package handling devices with increasing I/O counts, a number of companies have selected fan-out wafer-level packages (FO-WLPs) to meet their needs. The drive to reduce cost has resulted in the investigation of larger scale panel processing for FO-WLPs. The idea is that processing in a larger panel would provide a lower cost structure than a wafer format. A number of new processes are being considered and will be discussed. This panel discussion will also examine some of the issues in large-panel processing, such as die placement accuracy and speed, molding materials and processes, warpage, and material requirements.

Panel Discussion: Wednesday, October 14, 2015



Interposers, 3D TSVs, and alternatives: what are the options and where do they fit?

Moderator: Françoise von Trapp [3D InCites]

Panel Members: Aric Shorey [Corning Glass], Thibault Brisson [Yole Développement], Hughes Metras [CEA-Leti], Mike Kelly [Amkor Technology]

After years of development and speculation, TSV-based silicon interposer and 3D IC devices are finally being implemented in production volumes in devices destined for high-end computing applications, where the cost/performance benefits are justified. In parallel, many companies have elected to invest in alternative approaches to Si and TSVs to come up with more cost-sensitive solutions to meet the high-density requirements of next-generation mobile products. With the plethora of device types differentiated only by process flows and materials used, it's difficult to differentiate between these options and where they are best suited. This interactive panel will attempt to sort out the confusion. With the aid of a Kahoot quiz, we will test the audience's understanding of available options (there will be right and wrong answers this time, and a prize to the winner) and panelists will fill in the blanks with details on their understanding of the requirements, and which device suits which application.

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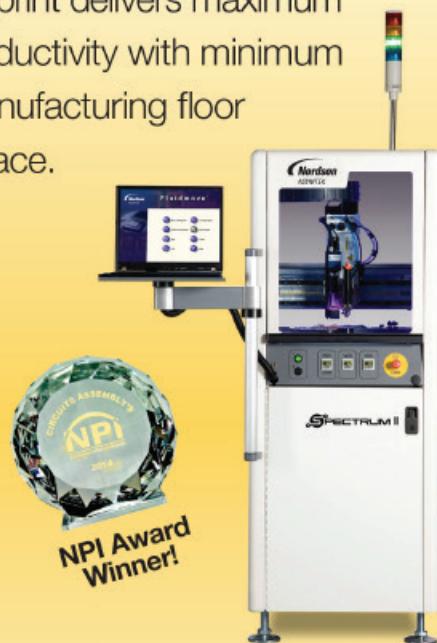
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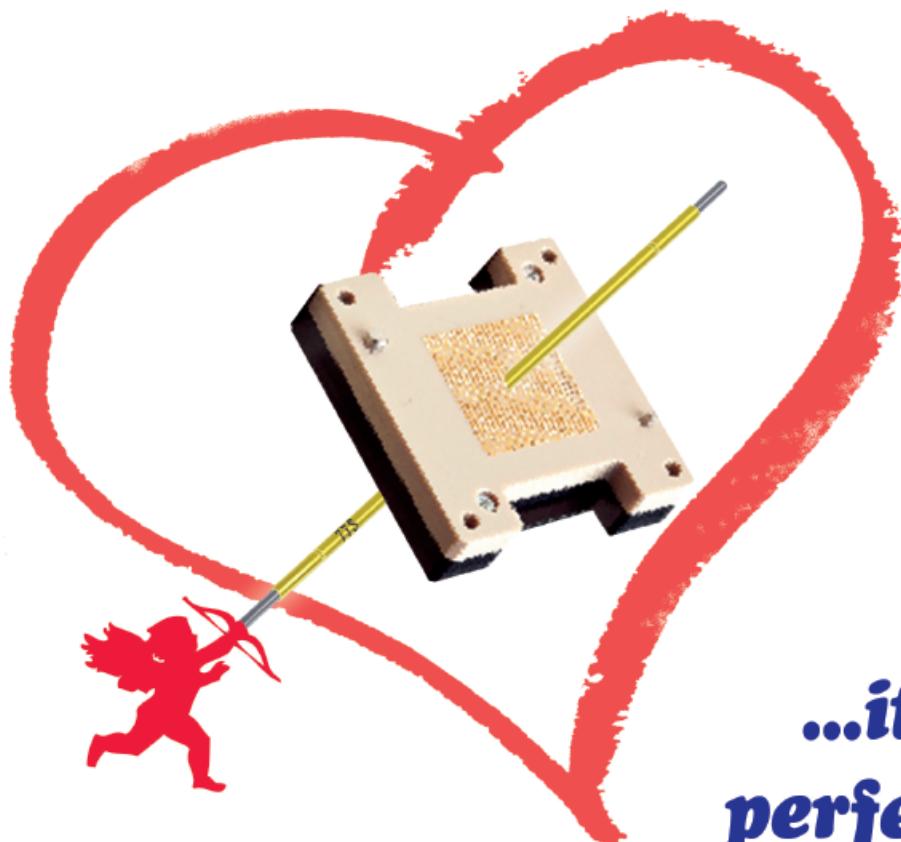
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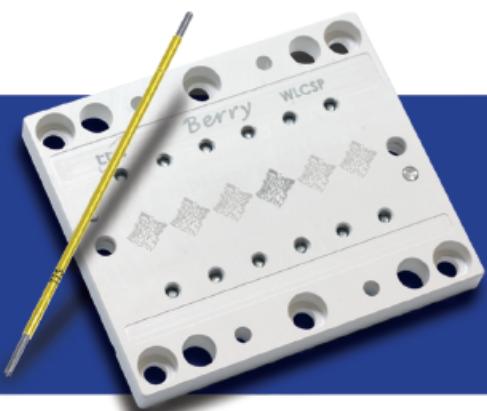


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IRT Nanoelec, Leti's partners demo 3D stacking in scalable SoCs

By Debra Vogler, Sr. Technical Editor

In advance of SEMICON West, IRT Nanoelec in conjunction with CEA-Leti and its partners, STMicroelectronics and Mentor Graphics, announced the realization of a 3D chip called “3DNoC” to demonstrate the use of 3D stacking technology in scalable, complex digital systems-on-chip (SoCs).

According to the news release, the 3DNoC chip is based on a 2D die that can be used in a stand-alone applicative mode, and also in a 3D stack with several dice, to multiply the processing performance of the system. The project’s complete demonstration platform shows both the simulated and measured thermal effects in the 3D chip using a new Mentor Graphics® Calibre® thermal-analysis prototype.

“The technology developed for this realization can be easily used and transferred to address mixed-technology applications, such as imagers and RF transceivers, or complex digital processing, such as high-performance computing and programmable devices,” said Severine Cheramy, IRT 3D program director. “In parallel with these results, we are working on developments that address more fine-pitch 3D technology than those used in the 3DNoC demonstrator and solutions for thermal dissipation, temporary bonding, and stress issues.”

Chip Scale Review asked Cheramy to comment on some of the developments alluded to in the above text quote: “This first work releases rough partitioning (core level),” Cheramy told CSR. “In order to get finer partitioning (logic block or gates), very low-pitch interconnections chip-to-chip (C2C) will be required.” Specifically, Cheramy noted that Leti is working on fine-pitch copper pillar ($20\mu\text{m}$) and Cu-Cu direct bonding (pitch $<10\mu\text{m}$). “Additionally, for high-performance applications, we are also working on a stress solution for a very large interposer, such as the kind used with high-aspect ratio TSVs and a stress buffer layer.”

Describing the differences between traditional 2D SoC and a 3D system, Cheramy told CSR that the network-on-chip (NoC) structure is already used for 2D SoC devices. “The principle is to decouple the information into packets in the x- and y-directions so this can be naturally extended to the third dimension by decoupling the information also in the z-direction (see Figure 1 for an illustration). Figure 2 illustrates the granularity scale difference between parallel 3D and sequential 3D structures.

Tech Brief Dept continued on page 61

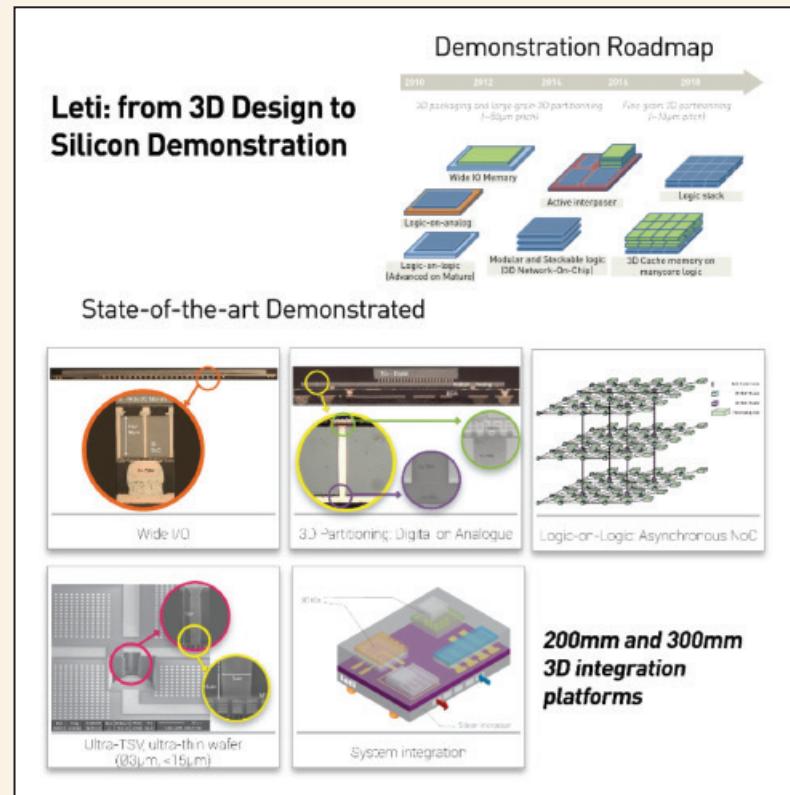


Figure 1: From 3D design to silicon demonstration. SOURCE: Leti

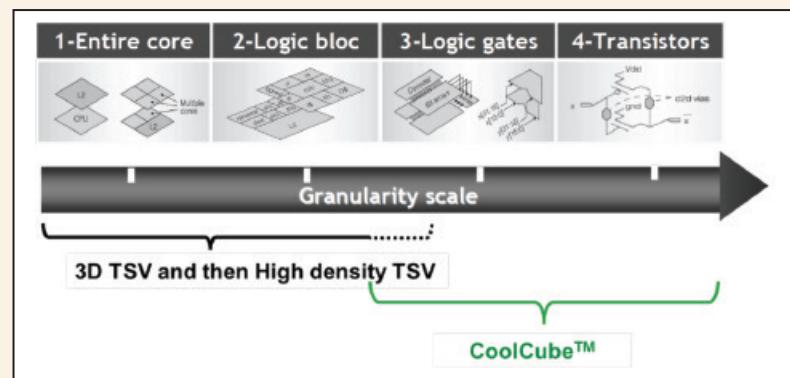


Figure 2: Granularity scale illustration showing the difference between parallel 3D and sequential 3D structures. SOURCE: Leti

Glass-based interposer and board-level packaging

By Lars Brusberg, Henning Schröder [Fraunhofer Institute for Reliability and Microintegration (IZM)]

Glass as a substrate material for interposer application has many benefits compared to conventional packaging materials like silicon, ceramic or polymer-based laminates because of its excellent dielectric and transparent properties. Furthermore, the integration potential of glass is superior because of its dimensional stability under thermal load and its coefficient of thermal expansion (CTE) matching to that of silicon ICs. A small pitch size of conductor traces, small-scale through-vias, and high alignment accuracy, are the key requirements that will be achieved from glass-based packaging. Glass has several advantages in comparison with other materials used for this purpose, such as silicon and polymer materials, which have been used as interposer materials [1-3]. Large glass panel fabrication has grown tremendously in size, driven by its success and widespread use in the display industry. Despite being very thin, panels, as well as the machinery to handle and structure them, are getting ever larger and more economical in size. There also has been a lot of progress on glass composition and surface strengthening of glass to increase its robustness, e.g., for touch displays. Thin glass can also be structured to facilitate in-plane optical waveguides, e.g., by ion-exchange techniques. In this manner, optical signal distribution can be embedded in panel size electro-optical circuit boards (EOCB) [4]. The specific dielectric properties of glass provide a high integration potential by combining electrical and optical functionalities in one single substrate.

CO₂-laser drilling of TGVs for glass interposers

Planar and vertical electrical interconnects in interposers are realized using conductor traces and through-glass vias (TGVs). Much focus is therefore placed on thin-film processing for 2D

interconnects on the glass surface and TGV technologies for interconnecting the top and bottom of the substrate. TGV technologies are based on drilling and filling approaches as studied in previous work by using the CO₂-laser technique [5]. Very fast CO₂-laser drilling of holes and thermal post-treatments for reducing mechanical stress are very promising for fast processing and high reliability. Holes with a diameter smaller than 100μm in different glasses with thicknesses between 145 and 500μm have been achieved by CO₂-laser drilling as shown in **Figure 1**. The holes have been metallized by sputtering a seed

30μm or below is available. In order to process the large glass substrates, resist coating and metallization by sputtering are essential and can be realized. Spray coating and dip coating are common technologies and sputter machines can handle large substrate sizes with sufficient homogeneity.

In recent years, a great deal of laser processing technology has been developed and introduced into mass production. For instance, maskless lithography using laser direct imaging (LDI) technology avoids high mask costs with the highest process accuracies and flexibilities. For glass cutting, a CO₂ laser process in combination with cold jetting to thermomechanically scribe and mechanically break the glass achieves a high optical end-face quality. Thin glass used in these large panels cannot only be used for a small glass interposer, but also as a dielectric layer sandwiched into a stack of common PCB materials. Because of the increasing requirements in thermal and mechanical stability in printed circuit boards (PCBs), it is promising to laminate thin glass foils instead of conventionally organic materials for PCB fabrication. Without any further processing, the thin glass sheet reduces the CTE of the base material and the PCB.

For drilling the glass panels, we selected a solid-state laser (Nd:YVO₄) with an optical output power of 20W in combination with an optical galvo scanning system for cylindrical TGV drilling. The laser beam is focused on the glass panel backside and starts drilling from there by moving the laser beam focus position continuously up to the glass surface. The system was chosen because drilling and free-form cutting can be realized easily in the same machine. The smallest via diameter of 0.5mm in glass can be achieved with such a system. Another benefit of the selected laser system is the resulting cylindrical TGV shape, which is excellent for polymer

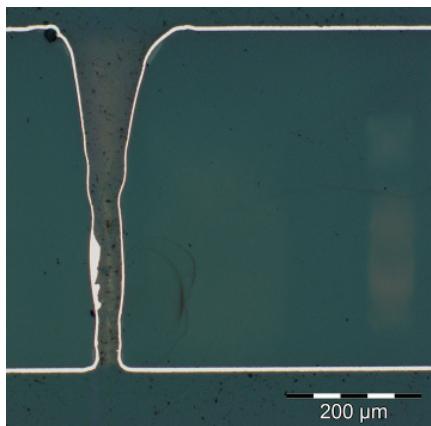


Figure 1: Cross section shows a metallized CO₂-laser drilled through-glass via in 500μm thin glass (glass panel-level processing).

layer and galvanic copper plating. The CO₂-laser drilling in combination with copper metallization has high potential for TGV forming in glass substrates for interposer applications.

The growing display industry produces glass panels having a size of 2.4m x 2.8m, to which standard subsequent finishing processes like thin-film deposition, lithographic processing, stacking, and cutting have been upscaled. Also, thin glass for roll-to-roll fabrication with a thickness of only

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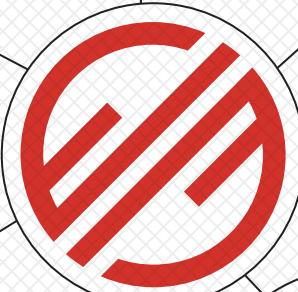


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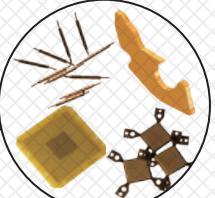


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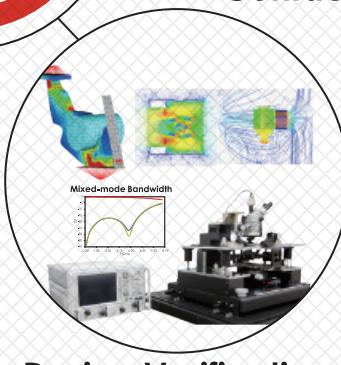
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plugging and mechanical drilling afterwards. Drilled TGVs are completely filled with an epoxy resin-based plugging material. Afterwards, a fast mechanical drilling with standard PCB equipment can be applied very efficiently. Because the drilling diameter is 300 μ m smaller than the diameter of the cylindrical TGVs, there is no impact on the glass that could result in cracks [6]. Thin-film metallization by sputtering a seed layer on glass, and Cu-plating on both sides of a 145 μ m thin glass has been successfully studied as shown in Figure 2 [7].

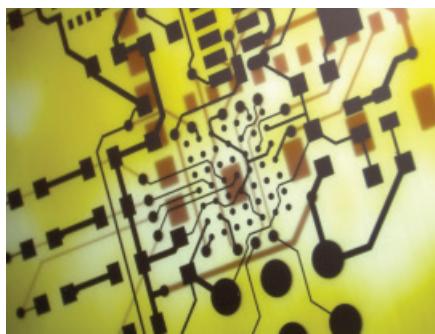


Figure 2: Cu-wiring on both surfaces of a 145 μ m thin glass was accomplished using sputtering technology [7].

Electro-optical transceiver packages

Thin glass is an excellent material for an integration of waveguides and lenses as elements for guiding and changing properties for optical beams within the package [8]. The substrate itself, therefore, serves as a micro-optical system. The most crucial issue today is mirror integration. Until now, there has been no technology ready to be transferred into commercial processes that is able to form planar mirror surfaces within thin glass with the required alignment precision, defined angle, and optical quality. However, a glass interposer was demonstrated with assembled components (a lensed VCSEL array, photodiode array, laser driver and transimpedance amplifier [TIA]) on the top side and an attached glass lid with integrated waveguides and end-face polished mirror on the bottom side. The transceiver operates with 40Gbps and has a low power consumption of 592mW [9]. The transceiver is mounted on a PCB and optically interconnected by the glass waveguide lid to a fiber array connector (MT) placed on the edge of the board as shown in Figure 3.

Depending on the integration level and overall size in packaging, one has to distinguish between interposer- and panel-

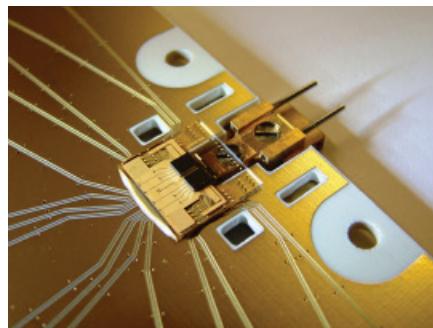


Figure 3: Glass interposer with assembled components mounted on a printed circuit board [9].

level approaches. To be compatible with silicon photonic and telecom fiber networks, the optical waveguides are designed to be operated at wavelengths of 1310nm or 1550nm. For data communication by means of active optical cables or optical backplanes being used in data centers, a “classical” transmission wavelength is 850nm, which can also be used in the glass layers.

Board-level photonic integration

Thin glass panels can also be used for integration as a center optical layer in an EOCB sandwiched into a stack of common PCB materials (Figure 4). EOCBs have been fabricated with planar multimode waveguides within thin glass foils based on a two-step thermal ion exchange process. Novel lamination techniques were developed to allow glass waveguide panels to be reliably integrated into a conventional electronic multi-layer PCB. In addition, a complete suite of optical connector technologies were



Figure 4: Multilayer EOCB with 1301 electrical through-glass vias (TGVs), two embedded thin glass layers, planar integrated gradient-index multi-mode glass waveguides and four mid-board optical coupling interfaces [6].

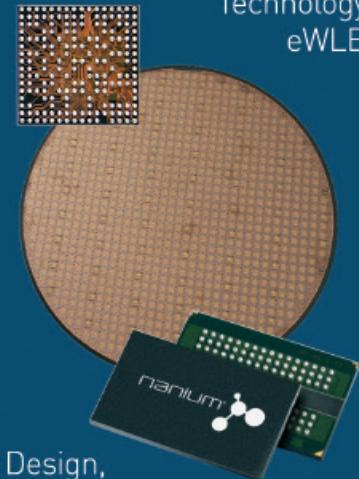
developed to enable fiber-to-board, board-to-board and chip-to-board connectivity. A fully integrated connection platform comprising a 281 x 233mm² multi-layer electro-optical



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backplane with integrated planar glass waveguides, a pluggable connector system, and slots for five pluggable test cards are demonstrated [10] as shown in **Figure 5**. Both on-card and externally generated 850nm and 1310nm optical test data were conveyed through the connector and waveguide system and characterized for in-system and system-to-system optical connectivity at data rates up to 32Gb/s per optical channel exhibiting bit error rates of less than 10^{-12} .

Because of its optical transparency and low loss waveguide performance in the telecom wavelength range, it seems straightforward to propose the possibility



Figure 5: Optical backplane demonstrator platform with an embedded multi-mode glass waveguide layer [10].

of an EOCD made from thin glass layers as a packaging and interconnection platform for silicon photonics board-level packaging. Ongoing work for single-mode fabrication in glass, fiber-to-waveguide coupling, and waveguide-to-chip coupling presents very promising results [11,12]. Glass-based interposers and board-level packaging can be merged technologically with inherent optical integration capability in the multi-mode and single-mode waveguide domain.

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Biographies

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Henning Schröder received his MSc degree in Applied Physics from the U. of Magdeburg, Germany, and his PhD degree at the Technical U. of Berlin. He is a Group Manager in the Optical Interconnection Technologies Group (Dept. System Integration & Interconnection Technologies) at the Fraunhofer Institute for Reliability and Microintegration (IZM).

This work was the recipient of the Outstanding Interactive Presentation award at ECTC 2014. The Optoelectronics Packaging subcommittee solicits papers on all topics pertaining to the design, development, and technology of packaging silicon photonics; optical interconnects; parallel optical transceivers; single-mode or multi-core connectors; optical waveguide coupling; optical chip-scale, heterogeneous, and microsystem integration; and 3D photonics. Submission deadline for 2016 ECTC is August 13, 2015. For more information, please visit www.ectc.net

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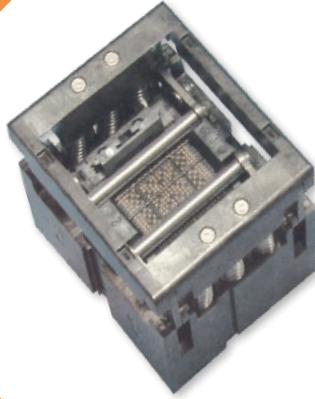
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Ultra-low residue semiconductor-grade fluxes for Cu-pillar flip-chip assembly

By Maria Durham, Hyoryoon Jo, SzePei Lim, Jason Chou, Andy C. Mackie [Indium Corporation]

It is no surprise that increasing the functionality of mobile devices necessitates increased semiconductor device density in ever-shrinking packages. The last edition of the International Technology Roadmap for Semiconductors (ITRS) [1] showed that flip-chip I/O pitches, cost per I/O, die thickness, and overall package thickness will all reduce significantly in the remainder of the millennium (Figure 1). This puts a major burden on assembly materials and processes as they must function together to enable the manufacture of powerful, high-yield, yet increasingly flimsy packages, all of which must be done without significantly impacting final device reliability. In an effort to identify the appropriate materials and process parameters for the emerging copper-pillar flip-chip, several functionality tests were conducted on ultra-low residue (ULR) no-clean fluxes.

Flip-chip assembly using flux

Flip-chip assembly onto substrates has traditionally been carried out by either spraying the flux onto the substrate, or dipping the solder bumps into flux, and occasionally may involve both processes (Figure 2).

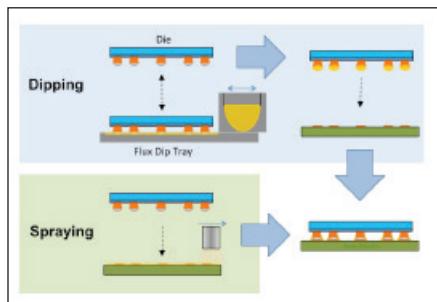


Figure 2: Flip-chip flux application methods.

Traditionally, the flux remaining after reflow ("residue") has been cleaned away using water or an aqueous-based solvent system. The residue of water-soluble fluxes are, by their very nature, a humectant and, if left behind, may give rise to current

Single Chip Package Technology Requirements for Mobile Devices						
	Year of Mass production =	2014	2016	2018	2020	Units
Transistor (T1)	MPU 1/2 Physical Gate Length after etch	18	15	13	11	nm
Wafer	Die thickness - Extremely thin packages (minimum)	10	5	5	5	microns
	Cost per I/O for OSAT production (minimum cost)	0.36	0.34	0.32	0.3	(USD\$/pin/100)
	Chip Area	100	100	100	100	mm ²
Mobile Device Packages	Package pin count (maximum)	207 - 1100	218 - 1150	252 - 1150	278-1150	number of I/O
	Package profile or thickness (minimum)	0.22 - 0.40	0.20 - 0.35	0.19 - 0.35	0.19 - 0.35	mm
	Junction temperature - T _j (maximum)	105	105	105	105	degC
	Operating temperature - ambient (maximum)	45	45	45	45	degC

Figure 1: Flip-chip package changes from 2014-2020. SOURCE: 2014 ITRS

leakage between adjacent I/Os – quantified as surface insulation resistance (SIR) – or as metallic dendrites, which grow due to a process called electrochemical migration [2]. However, the combination of large die, finer pitch, and reduced clearance (die-to-substrate distance) has increased the complexity for ensuring adequate cleaning [3], often necessitating either a longer cleaning process, or multiple cleaning cycles.

No-clean flip-chip fluxes

No-clean flip-chip fluxes traditionally have a residue level of 50-60%, whereas ULR no-clean fluxes have residues of <5%. Several characteristics have been tested to show their criticality to the functionality of the copper-pillar flip-chip application.

Flux residue levels. After reflow, fluxes leave behind a certain amount of residue. ULR (ultra-low residue) no-clean fluxes are designed to provide the same degree of functionality as both standard (high-residue) no-clean fluxes and water-soluble types, and yet the flux residue is almost undetectable. Although there is no standard terminology, ultra-low flux residue may be said to comprise less than 5% by weight of the initial flux. ULR fluxes allow the free flow of capillary underfill/molded underfill (CUF/MUF) into the gap between the bottom of the die and the substrate, minimizing the risk of underfill void formation. If the residue chemistry is compatible with the underfills, then delamination during subsequent thermal cycling and other stress testing is avoided.

Flux promotes good solderability between two surfaces. It does this by reacting with metal oxides or forming a salt or metal complex that dissolves in the flux residues away from the solder joint, leaving a clean metal surface. The negative free energy of formation of tin-(Sn) based intermetallics drives the formation of a strong bond between the cooled solder and the underlying metal.

Poor solderability leads to weak joints and possibly voiding. On the other hand, excessive solderability may, in certain instances, lead to bridging. For logic devices operating at high frequency, even bridging between adjacent contacts on the same trace (that is, contacts at the same potential) may give rise to parasitic capacitance and, hence, unequal R/C delays on different contacts. The flux activity (a measure of its reaction speed and capacity to remove oxide films) must, therefore, be optimized to promote good wetting without causing excessive bridging. This latter is a characteristic issue seen with the high activity levels associated with water-soluble fluxes.

Characteristics of ULR fluxes. Flip-chip fluxes have many characteristics that are critical to their functionality. Just some of the key factors are rheology, residue level, solderability, the ability to retain die in place during reflow, and compatibility of the final residue with MUF and CUF.

Rheology. The rheology of the flux is important to many aspects critical to correct flux functionality, such as the flux depth in the dip tray (as opposed to the engineered tray depth), the ability to remove die from the flux dip tray,

consistent dipping (or dispensing or printing) performance, the ability to hold the die in place before reflow (so-called MDR, or movement during reflow), flux bridging between adjacent I/Os, and the ability to inspect the flux on the die bottom after dipping (often associated with flux bridging).

Viscosity is only one of the rheological characteristics of a flux, and only for a Newtonian material is the viscosity constant with varying shear stress or shear rate. Most dipping fluxes are non-Newtonian; therefore, the use of a single-point viscosity measurement, although common, is not recommended for complete rheological characterization, but may be used as shorthand for many different rheological parameters.

Rheology also plays a critical role for very fine-pitch ($\leq 60\mu\text{m}$) copper-pillar-bearing die, where surface tension is starting to be important:

- If the viscosity is too low, flux may wick up to the bump/copper-pillar and contaminate the die surface.
- If viscosity is too high, it may lead to bridging (Figure 3) between adjacent I/Os. Also, if the tack (extensional viscosity) is too high, it may even make it impossible to remove the device from the tray – a major problem with smaller die.

For standard mass-reflow processes, it is important for the flux to be able to keep the die in place during reflow or to minimize die-skew, also referred to as MDR. This is not simply related to the room-temperature viscosity, but is a complex function of both the low shear rate rheology, as the flux loses mass during

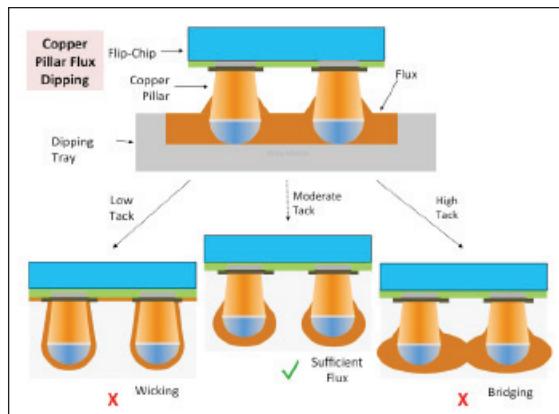


Figure 3: Flux rheology for fine-pitch dipping.

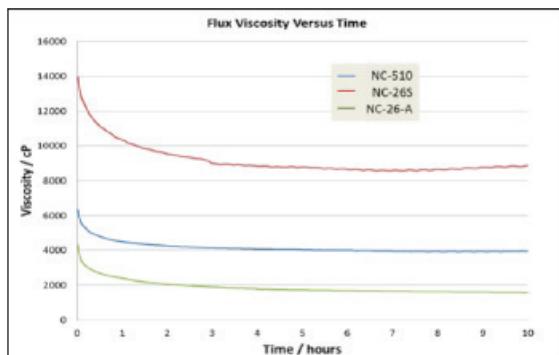


Figure 4: Flux stability shown by viscosity vs. time.

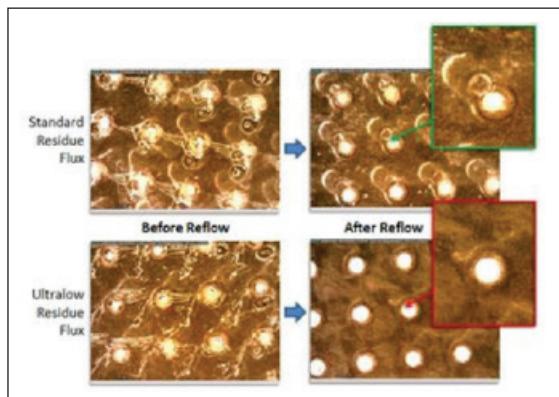


Figure 5: Visual comparison of flux residue types.

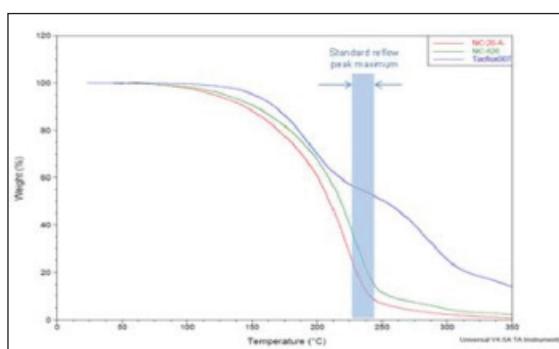


Figure 6: Thermogravimetric analysis results.

reflow and the flux activity as the temperature rises. A test method (the MDR test) was therefore developed and designed to quantify the movement of a component on flux during the reflow process.

Experiment and discussion

The following sections outline the tests conducted to determine the suitability for use in emerging copper-pillar flip-chip applications at the sub-100 μm pitch level.

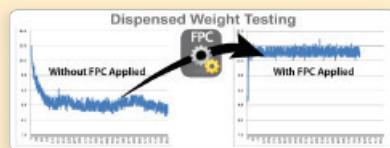
Rheology. A cone and plate viscometer measured the viscosity of the flux as a function of time at 25°C. The results for several ULR no-clean fluxes are shown in **Figure 4**. The data clearly indicates that the three ULR no-clean fluxes have a consistent viscosity over a period of 10 hours, which is just slightly longer than a typical work shift. After each shift, the user commonly cleans the flux tray and replenishes it with fresh flux to ensure consistency. The rheology (viscosity or tack) of a flux can be fine-tuned to suit the specific application, package configuration, and equipment capability.

Residue level. As a simple visual indication, a ULR no-clean flux was compared to a standard flux residue before and after reflow. **Figure 5** shows the change in appearance. Note the dramatic change in the residue level for the ULR flux. In addition to visual inspection, thermogravimetric analysis (TGA) was used to characterize the amount of flux residue after a simulated long reflow, using a ramp rate of 10°C/min and under a nitrogen flow. As shown in **Figure 6**, the two ULR no-clean fluxes (NC-26S and NC-26-A) and the standard residue flux (TACFlux007) exhibit significantly different flux residue levels.

From **Figure 5**, there is little or no flux visible after reflow, whereas with the standard residue flux, there is still some flux present; **Figure 6** confirms this. At a standard reflow peak temperature range of 235–250°C the ULR no-clean fluxes have less than 10% residue, as compared to about 50% for the standard residue flux. Note that the TGA data is unrepresentative of real reflow as the exposed surface area is much smaller in TGA than for most real flip-chip applications. In reality, the flip-chip fluxes will have lower residue levels than shown here.

MDR and solderability. Specimen preparation for both the solderability and the MDR (movement during reflow) tests is done by printing flux onto a metallized coupon using a stencil. SAC305 solder spheres are placed onto the flux using a standard, automated

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pick-and-place machine with tape and reel spheres. The metallized coupon with the printed flux and spheres is then reflowed at <100ppm O₂ using a standard flip-chip reflow profile.

Solderability (spread test). After reflow, the solder height is measured automatically and the solder spread ratio (%) is calculated using the below equation:

$$S = ((D-H)/H) \times 100 \quad (1)$$

Where: S = Spread factor

D = Initial sphere diameter

H = Post-reflow solder height

The results of the solderability test are shown in **Figure 7**.

Typically, the standard residue no-clean flux and water-soluble flux would be expected to have better wetting; however, as shown in **Figure 7**, the flux wetting behavior of the two ULR fluxes NC-26-A and NC-26S is close to the WS-575-A water-soluble flux. Users have found this to be the optimum activation level for wetting without excessive or insufficient flux.

Movement during reflow (MDR). The ability for the flux to hold the die in place during reflow was studied by using a proprietary MDR test. This uses the same test setup as the solderability test, but data analysis is based on the sum of the squares of the Dx and Dy for each final solder spread (sphere) center (**Figure 7**) after reflow. The results are shown in **Figure 8**.

Remember that the lower the MDR number (the least movement), the greater the ability to eliminate skewing. **Figure 8** shows that TACFlux007 has the least movement during reflow, which is typical for a standard residue flux. However, a standard flux will leave a lot of residue – typically up to 60%w/w of the initial flux – partially filling the area under the chip and making it impossible to get a void-free underfill. Two of the ULR no-clean fluxes, NC-26-A and NC-26S, show a comparable MDR to the water-soluble flux WS-575-A, which is acceptable for most applications.

Note that, although the MDR test shows the NC-26-A and NC-26S to be equivalent, customer data confirms that the higher residue and higher viscosity material, NC-26S, is better able to maintain the large die in place during reflow, and also shows significantly reduced capillary action (wicking) during the dipping and reflow processes.

Compatibility with MUF/CFU.

Several different test methods have been developed and tested by the global Indium Corporation technical team to demonstrate the compatibility of the flux residues and the results have been reported elsewhere [5].

In this paper, the simple interfacial shear strength between a sample of reflowed flux and the cured CUF or MUF allows an easy comparison of the compatibility between the two. Compatibility is a strong function of the residue quantity, and is also related to the interdiffusion and chemical interactions between the flux residue and the underfill. The degree of compatibility can be varied by applying different materials. For each shear strength measurement, one combination of flux and three underfill samples were tested.

For sample preparation, a 65μm layer of flux is applied onto the substrate. This substrate is then reflowed under a typical lead-free reflow profile using a standard nitrogen-purged reflow oven at (<100ppm O₂). Underfill is then applied and a silicon die placed on the underfill. The whole assembly is then cured as recommended in the product data sheet associated with the specific CUF or MUF underfill. The results of the shear strength test are shown in **Figure 9**.

The data indicates that the two ULR fluxes, NC-26-A and NC-26S, are close but have slightly lower shear strength when compared to the no flux samples, which is to be expected because there is no flux present. Both fluxes show good compatibility and correlation with these underfills.

Future challenges

Several challenges in flip-chip assembly remain, such as the generally accepted movement from standard mass reflow (MR) type processes to thermocompression bonding (TCB) at around the 40-60μm pitch node [5]. This dramatic change in processes is driven by the coplanarity and solderability

issues caused by the adoption of coreless substrates and embedded traces [6]. The adoption of TCB itself faces the challenge of insufficient throughput (in terms of UPH) and fluxes are currently being optimized in collaboration with industry partners to meet these evolving process needs.

The increasing criticality of underfill compatibility is also a matter of concern, and the development of so-called “near zero residue” (NZR) fluxes, less than 2% by weight of the initial flux, will be a major part of Indium Corporation’s roadmapping for future flip-chip fluxes.

Summary

Simple test methods, such as those from the IPC (that is, tests outside the auspices of system-level tests like those

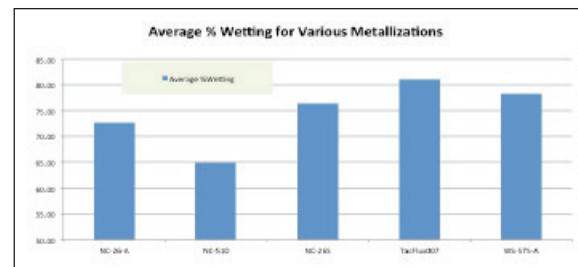


Figure 7: Results of the solderability test.

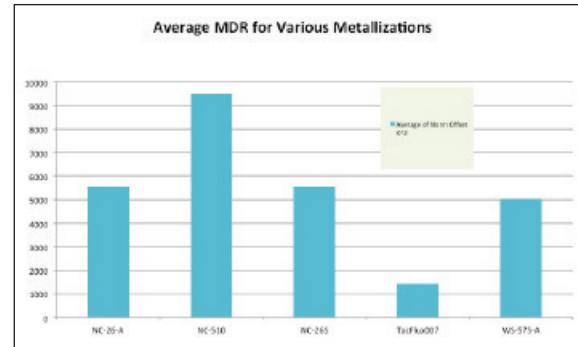


Figure 8: Results of the MDR test.

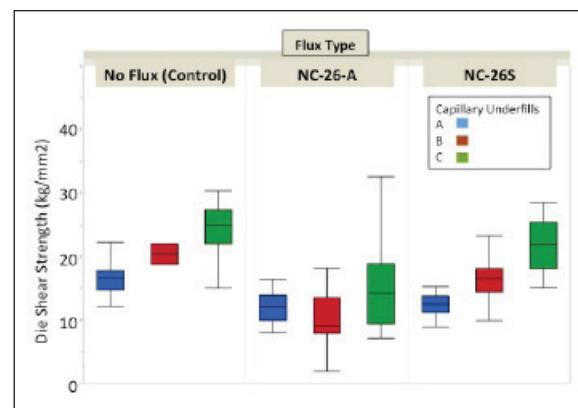


Figure 9: Results of the underfill shear strength test.

from JEDEC [7]) are largely inadequate to quantify the critical-to-functionality parameters of ULR no-clean fluxes [8]. The authors have, therefore, worked together to develop a suite of test methods and produce associated data to give users confidence that the materials are suitable for use in emerging copper-pillar flip-chip applications at the sub-100µm pitch level.

The successful implementation of these commercially available ULR flip-chip fluxes at customer sites in China, Taiwan, and Korea underlines their utility in the high-volume and high-yield assembly processes demanded by outsourced semiconductor and test providers (OSATs) and original design manufacturers (ODMs) packaging flip-chip die for the coming generations of portable electronic devices.

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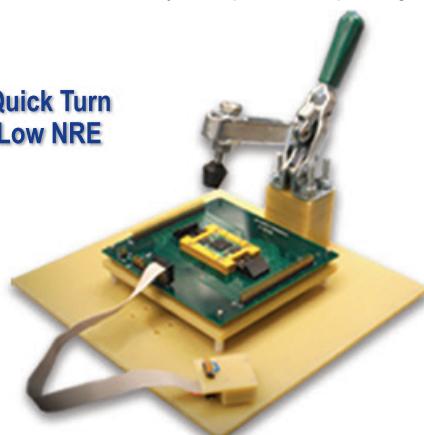


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Polyimide and polybenzoxazole technology for wafer-level packaging

By Chad Roberts [HD Microsystems]

Wafer-level packaging (WLP) has been instrumental in enabling low cost, high-volume chip-scale packaging leading to integrated and functionally advanced mobile devices. Polyimide (PI) and polybenzoxazole (PBO) materials have been critical to microelectronics packaging providing exceptional mechanical, thermal and dielectric properties that enable WLP designs and improve the reliability of today's advanced packaging solutions. Both PI and PBO chemistries offer flexible formulations of both positive and negative photosensitive versions for complex packaging architectures. PI and PBO chemistries deliver unique properties in WLP applications for redistribution layers, solder bump stress buffers, wafer bonding and passivation layers. Recent packaging trends have pushed for low-temperature cure PI/PBO chemistries while balancing properties of coefficient of thermal expansion (CTE), Young's modulus and improved copper adhesion. In this paper, the chemistry, processing, applications and recent trends of polyimides, polybenzoxazoles and the respective precursor liquid formulations will be reviewed with a focus on wafer-level packaging.

Background

Smartphones, cameras, tablets, and other mobile devices continue to push boundaries of integrated circuits (IC) and packaging designs to accommodate smaller form factors and increasing reliability demands. Wafer-level chip-scale packaging (WLCSP) is a key enabling technology for mobile devices. Wafer-level packaging provides low-cost, high-volume, semi-hermetic packaging, and WLCSP may be defined as IC packaging that occupies no more than 20% more surface area relative to the original die allowing for testing and packaging of an entire wafer prior to dicing, rather than individual die [1, 2]. This compact packaging minimizes

chip-to-PCB inductance and enhances thermal conductance. Cost savings, in terms of materials utilization and real estate efficiency, is often touted as the major driver for wafer-level packaging [1]. However, as WLP-based chip designs become more efficient with reduced interconnects and enhanced signal propagation, Moore's law of consumer electronics is steadily maintained through the use of WLCSP. In essence, year-over-year, consumers have been able to purchase greater and greater computing power in the form of more compact, highly functional mobile devices with each year's model offering enhanced and innovative capabilities, functionality, durability and reliability.

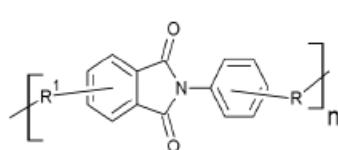
Using the flip-chip approach to bypass bulky molded lead frame designs, WLP designs routinely include processes to fan-out interconnects such as ball grid arrays that have redistribution layers and that may require polymer underfill. In addition, WLP designs may include other 3D integration technology such as through-silicon vias (TSVs) and wafer-to-wafer (W2W) bonding allowing for stacked, shortened signal paths and lower power dissipation [1, 3, 4]. Polymeric materials are well established for protection and passivation of ICs and printed circuit boards (PCBs), and PI and PBO materials are recognized as the dielectric material of choice as a result of excellent thermal and chemical stability, relatively low stress levels, and excellent mechanical properties. Toward the end of the 20th century, photodefinable polyimide and PBO formulations were developed [5, 6], and

their commercialization has enabled WLCSP by reducing the number of steps and enhancing the resolution for redistribution layers (RDLs), fan-out, stacked architectures and other advanced packaging techniques [6, 7]. In recent years, WLCSP has led to an evolution of polyimide and PBO structures, compositions and formulations enabling thicker films, low-temperature cure, copper compatibility, low-stress coatings and bonding adhesives [8-10].

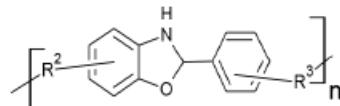
Technology and chemistry of polyimides and PBO

To truly understand the unique value of PI and PBO materials in microelectronic packaging, one must first start with related polymer synthesis and technology of the structure/properties relationship for designing film properties and photo-activated chemical transformations enabling either positive or negative image development.

Synthesis of polyimides (PI) and polybenzoxazoles (PBO). An orientation to the chemistry involved for liquid polyimide packaging materials is provided in this section. For an extensive review of PI synthesis and related chemistry, Liaw's recent publication provides an in-depth discussion [11]. PIs and PBOs cover a broad range of chemistry, structures and properties, but in general, PI and PBO refer to polymeric structures comprising alternating aromatic and heterocyclic structures as depicted in **Figure 1**. Although alternate synthetic pathways have been documented, aromatic dianhydrides in combination with aromatic diamines are routinely reacted



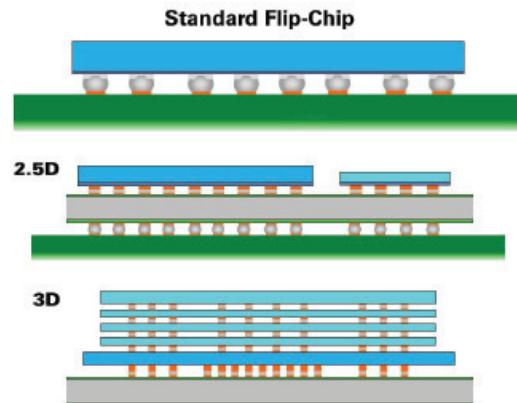
Polyimide (PI)



Polybenzoxazole (PBO)

Figure 1: General synthesis of polyimide and polybenzoxazole.

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forming poly(amic acid) (PAA) and the respective PI, which is then produced upon further heating. In contrast, PBO materials may be synthesized via a poly(hydroxyl amide) intermediate from the reaction of a diamino-dihydroxybenzene and an aromatic diacid chloride.

Properties of PI and PBO materials are dictated by the morphology and chemical structure. Because of the high oxidation state of these compounds, these polymers possess considerable resistance to thermal oxidation and chemical attack. Depending on functionality and configuration of the R groups (R , R^1 , R^2 , and R^3), polyimides and PBOs may be very rigid with high tensile strength, high modulus and T_g in excess of 400°C such as in the case where R groups are strictly, simple phenyl and biphenyl rings leading to highly linear, rigid polymer chains without any kinks or bulky groups. Thus, the in-plane orientation of these polymer chains results in exceptionally low coefficient of thermal expansion (CTE) [11].

Based on their unique combination of thermo-oxidative stability, superb electrical properties, and excellent solvent resistance, polyimides have found a strong-hold as passivation layers in microelectronics applications [11]. Charge transfer complexes and electron polarization result from strong inter-chain interactions of rigid polyimides leading to significant color in films and coatings, low CTE, insolubility in common solvents, and excellent chemical resistance. Fortunately, polyimides are typically derived via a soluble PAA or ester($R^4 = \text{alkyl}$) precursors as shown in Figure 1, and R, R^1 , R^2 and R^3 groups such as ethers, methylene, sulfones, isopropylene, and hexafluoro isopropylene may be incorporated from monomer composition, and such dianhydrides, diamines diaminodihydroxy benzenes or diacid chlorides may be selected to enhance adhesion, transparency, contrast, residual stress, thicker film formability and low-temperature cure [11].

Photosensitive polyimides. In the early days of polyimide photolithography, polyimide micro-patterns were formed by either wet etching or dry etching films using conventional photoresists as masks. In this day and age, photosensitive polyimide (PSPI) formulations have not only reduced manufacturing cost, but also enabled improved contrast and greater resolution with fewer process steps [11]. Figure 2 illustrates this modern photolithographic process utilizing PSPI formulation rather than a combination of convention photoresist and a polyimide precursor solution (not shown). PSPI may be defined as polyimide precursors with photosensitive reagents incorporated in the polymer structure and/or formulation chemistry, and such reagents undergo photo-chemical transformations including de-

Process Step	PSPI – Negative Tone	PSPI – Positive Tone
Apply PI Precursor	Yellow	Yellow
SoftBake	Yellow	Yellow
Expose	↓↓↓ ↓↓↓	↓↓↓ ↓↓↓
Develop	Yellow	Yellow
Cure	Yellow	Yellow

Figure 2: Graphic comparison of the process flow for negative and positive tone PSPIs.

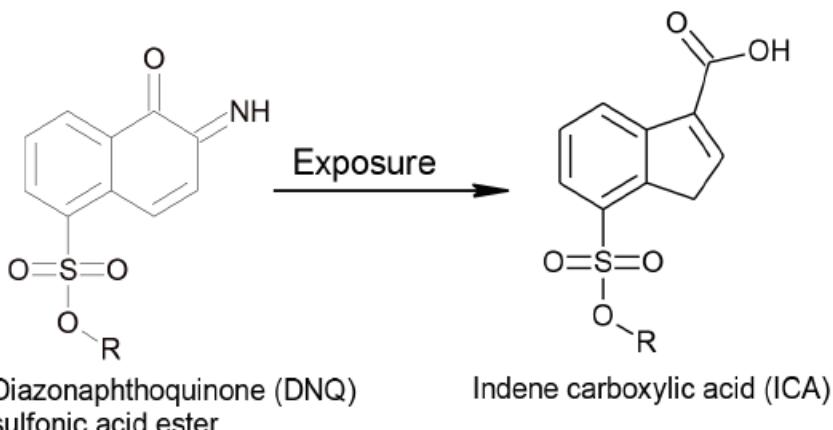


Figure 3: Wolff rearrangement of DNQ to an alkali-soluble ICA group.

protection, polarity changes, chain scission, cross-linking, and imidization. Photosensitive polyimides formulations are not typically based on soluble polyimides or PBO, but rather, these formulations are based on soluble poly(hydroxyl amides), PAA or poly(amid ester) precursors along with cross-linkers, photo-generated acids/bases, and photosensitive compounds [8, 11, 12]. These changes in polymer structure and formulation chemistry may lead to more soluble regions in the coating leaving a developed image with the same pattern as the exposure mask, and thus, this material is considered a positive tone PSPI. Conversely, exposed regions of a negative tone PSPI will become insoluble in the development fluid leading to a negative image relative to the original mask.

For photosensitive materials, the material properties and performance may be divided into the image formation process and final film properties. Key image formation parameters include exposure sensitivity, contrast, resolution, development process, shelf life and final cure procedure, and pertinent film properties include thermal/dimensional stability, electrical properties, adhesion, purity, and water/chemical resistance [12]. Resolution may be dictated by the equipment, but the PSPI formulation will determine the ability to balance film retention and development of imaged regions of the PSPI coating. Sensitivity is dependent on the influence of the light transmittance of the polymer coating at the exposure wavelength whereas contrast may be thought of as a function of the cross-linking reaction rate and cross-link density that derives from the reaction for a negative PSPI or the rate of deprotection or solubility enhancement for a positive PSPI [8, 12, 13]. Additional image formation parameters and film properties will be discussed in more detail in the following sections.

Negative tone photo-sensitive polyimides. Based on their inherent chemistry and insolubility, most polyimides are traditionally processed as PAA or the corresponding poly(amic ester) precursor solutions, and negative tone photo-resists may be synthesized by direct modification of these precursor structures or respective monomers starting materials. Photo cross-linkable functional groups are incorporated via attachment of acrylic groups through esterification or ionic bonding with tertiary amine containing acrylates; and the negative PSPI formulation would usually include a free-radical photo-initiator, which is activated upon exposure. Then, the initiator polymerizes the pendant acrylic functionalities along with other formulated acrylic monomers [8, 11]. Therefore, exposed areas become insoluble, and unexposed regions are washed away with the development process. Once the negative pattern is generated, a high-temperature cure cycle of 350°C or greater is required for polyimide ring closure, de-polymerization of acrylics and photo-package burn out. However, recent developments with chemical amplification techniques have enabled PSPI and PSPBO (photosensitive polybenzoxazoles) to cure and reach optimum properties well below 300°C [14].

Positive functioning photo-sensitive polyimides and PBO. For positive acting PSPI, the base resin is typically poly(α -hydroxyl-amide) or a hydroxyl containing polyimide used in combination with a photosensitive, solubility enhancer [12-13]. As depicted in **Figure 3**, diazonaphthoquinone (DNQ) undergoes a Wolff rearrangement to form a ketene that reacts with ambient water to form indene carboxylic acid (ICA). In the unexposed areas, the DNQ derivatives are designed to act as a solubility inhibitor for the poly(α -hydroxyl-amide) or a hydroxyl pendant

polyimide, whereas the ICA enhances the dissolution of the base resin in the exposed regions. In contrast to free-radical, photo-initiators in negative acting PSPI, the contrasting effect of DNQ/ICA is essentially limited to the depth of light penetration in the PSPI and PBO coating, whereas free-radicals in negative tone PSPI propagate deep into the coating beyond the photo-initiation activation limit [11].

Cure temperature, especially over 300°C, and thick-film patterning of PSPI can be a packaging design limitation, and these areas have been the subject of significant research in recent years [10, 11, 13]. Transparency of the base resin and the formulated coating, therefore, is critical in order to maintain good contrast and depth of penetration for thick-film development; so fluorinated diamines, dianhydrides and other monomers for optically transparent PI and PBO are preferred for positive tone PSPI [13]. In addition, positive-tone, low-temperature cure PDPI have been the subject of several recent investigations. For example, in 2014, Matsukawa, et al., disclosed a low-temperature cure process using epoxy cross-linking to cure a photo-patterned, pre-cyclized soluble polyimide [10].

Film properties. PSPI or PBO materials are selected based on the mechanical and electrical performance criteria for the end-use application, and compatibility with user cure and other process conditions. Pertinent film properties and test data for PI and PBO films can vary significantly in terms of thermal stability, solvent resistance or mechanical performance, and the impact of cure temperature can be substantial. A final cure is required to convert the PI or PBO precursors into the final polyimide or PBO structure and to volatilize photo-package components and residual solvents from the films. With a nitrogen purge, final cure with stepwise heating and a one-hour hold at temperatures in excess of 300°C are often required, although recent technology advancements using techniques like chemical amplification have allowed for final cure temperatures approaching 200°C [12-14]. However, in a production environment, a rapid curing process such as infrared (IR) heating, variable frequency microwave or a combination of hot plate and convective heating may be preferred. The curing temperature should be at least 10°C above subsequent processing temperatures to ensure mechanical integrity and prevent out-gassing from the film.

As an example, film properties of HD-4100 PSPI and HD-8820 PSPBO are summarized in **Table 1** as a function of cure temperature. Note that each film was cured for one hour in a nitrogen-flushed

Item	Unit	HD-4100 Series						HD-8820		
Type	—	Solvent-Negative PI						AQ-Positive PBO		
Cure conditions	°C / 1 hr	250	275	300	320	350	375	250	280	320
Tensile strength	MPa	169	157	184	165	190	200	112	133	170
Elongation	%	49	45	54	30	50	45	10	95	100
Young's Modulus	GPa	3	3.2	2.9	3	3.4	3.5	2.6	2.5	2.3
Tg value (TMA)	°C	210	216	227	260	290	325	244	257	300
CTE	ppm	218	142	138	60	50	35	60	71	67
Weight loss temp. (1%)	°C	293	307	306	305	365	430	338	382	403
Weight loss temp. (5%)	°C	319	340	332	330	410	480	448	477	488
Residual stress	MPa				29	32	35		35.7	40.4
Dielectric Constant	-						3.2			3

Table 1: Comparison of HD4100 and HD8820 properties as a function of cure temperature.

convection oven, and low-temperature-cured film properties may be compensated for by longer cure duration or alternate heating methods. For the solvent-negative HD-4100 PI and the HD-8820 aqueous-positive PBO materials, the thermal stability and mechanical integrity are most strongly impacted by final cure the

temperature. In addition, the HD-8820 PBO exhibited a significant reduction in tensile strength and elongation especially at the 250°C cure, whereas no significant change in the CTE was observed. The observed changes in T_g, CTE and weight loss temperature are a direct result of the level of cyclization to polyimide and degree

of photo-package “burn-out” previously discussed. At cure temperatures greater than 350°C, or in the presence of oxygen at even lower temperatures, more complex structures rather than simple benzenimide or benzoxazole heterocycle may be formed because of side-reactions leading to branching and potential cross-linking [11].

Polyimide and PBO packaging materials

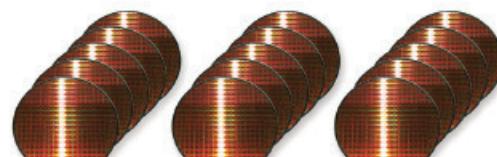
In the previous sections, an overview of the synthesis, materials properties, and chemistry of photosensitive components was presented, especially in the context of designing PI/PBO structure and photosensitive formulation for optimum balance of film properties and image development. Next, specific examples of WLCSP and related advanced packaging designs will be reviewed with a focus on the utility of PI and PBO materials.

Packaging designs with PI and PBO. Evolving packaging designs have spurred on the development of passivation layers with demands for low stress, contrast at thicker layers, low-temperature cure and high-temperature adhesives. Examples

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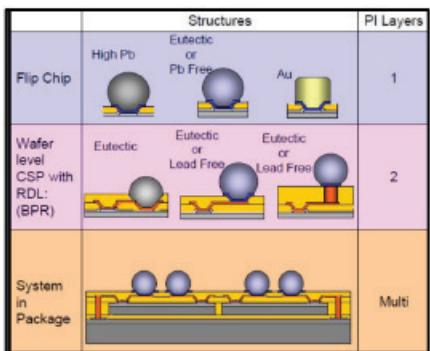


Figure 4: Flip-chip, WLCSP, and SiP examples of packaging structures with typical PI/PBO layers.

Item	Unit	HD-4100	HD-8820	HD-8930	HD-8940
Tone	-	Negative	Positive	Positive	Positive
Sensitivity (i-line@5um cure)	mJ/cm ²	300	300	210	230
Developer	-	Solvent	TAMH (aq)	TAMH (aq)	TAMH (aq)
Cure condition	DegC/1hr	350-390	300-350	200-250	200-250
Thickness	μm	4 - 11	3 - 10	4 - 10	5 - 10
Tensile strength	MPa	200	170	170	170
Elongation	%	45	100	80	100
Young's Modulus	GPa	3.5	2.3	1.8	2.2
Tg	DegC	325	300	240	230
CTE	ppm/C	35	60	80	60
Weight loss (5%)	DegC	480	490	310	310
Residual stress	MPa	34	37	25	25
Dielectric constant	-	3.2	2.9	3.1	2.9
Dissipation Factor	-	0.010	0.009	0.010	0.009
Break down voltage	kW/mm	250	470	330	420
Volume Resistivity	Ω * cm	2.4 × 10 ¹⁶	3 × 10 ¹⁶	3 × 10 ¹⁶	3 × 10 ¹⁶
Moisture absorption	%	1.5	<1.0	<1.5	<1.5

Table 2: Comparison of high-temperature cure PI and PBO (HD4100 and HD8820) and low-temperature cure PBO formulations (HD8930 and HD8940).

of packaging structures incorporating polyimide and PBO layers/sections are depicted in **Figures 4** and **5** where light orange regions, as opposed to the copper color, are PI/PBO. For all the depicted designs, a passivation layer such as PI or PBO is needed for protection of the die from surface damage during handling and molding, adhesion enhancement between the die and mold compound, and most importantly, stress reduction at the die surface from thermal cycling, which is especially important for low-k interlayer dielectrics [1, 3]. System-in-package (SiP) design requires thick layer passivation with elasticity and low stress. For WLCSP and fan-out embedded wafer-level ball grid array (FO-eWLB) structures, adhesion at UBM and RDL metals is critical, and TSV and related processes require permanent or temporary, high-temperature bonding adhesives. The next section will focus on high-temperature adhesive for WLP, and then applications for low-temperature cure stress-buffering PSPI and PSPBO will be reviewed.

High-temp bonding adhesives for W2W bonding/3D architectures. New Interfaces and adhesion issues have emerged as designs have moved to include multi-chip packages (MCP) and system-in-packages (SiP). Therefore, adhesion

properties of PSPI and PBO materials will be more and more critical for future requirements [15]. In 2010, the suitability of HD-3007 (non-photodefinition PI) and HD-7010 (PSPI) for wafer-to-wafer bonding was reported, based on the excellent adhesion, thermal stability, and bonding process compatibility. Clean removal of HD-3007 temporary adhesive from patterned HD-4004 with EKC865 cleaner was demonstrated, whereas patterned HD-7010 forms a permanent adhesive bond while maintaining the imaged passivation layer between the wafers [16]. Zoschke, et al., evaluated the suitability of HD-3007 polyimide for temporary wafer bonding for 3D WLP applications such as wafer thinning and backside processing for TSV fabrication. The wafer-to-wafer bond remained intact despite multiple processes such as back-grinding, chemical mechanical polishing (CMP), physical vapor deposition (PVD), spin coating, electroplating, lithography, and sub-300°C cure cycles. In comparing laser-induced and solvent-based wafer debonding, superior performance of laser processing was demonstrated with debonding times less than 1 minute per wafer [17]. Commercially available W2W bonding adhesives were recently reviewed by Ishida and Lutter [18].

Low-temperature cure PSPI/PBO stress buffer. For mobile devices, stress from temperature cycling (T-cycling) and mechanical shock is a key issue [19], and in addition, recent packaging

designs include temperature sensitive components such as MEMS [15]. As a result, several investigations have been directed at minimizing or buffering the stress from mechanical shock and T-cycling. For example, in 2010, Töpper, et al., systematically compared 30 different packaging materials in terms of curing/shrinkage, planarization, copper compatibility, and T-cycling reliability. After evaluating a range of packaging chemistries including PI, PBO, BCB, silicones, acrylates, epoxy/novolaks, and polynorbornene, the Fraunhofer IZM group concluded that reliability of under bump metallization (UBM) with solder ball on polymer (BOP) is the key advantage for polyimide materials. Because of the breath of PI structures and cure temperature effects, however, modeling and device design must use actual CTE, elongation-to-break, and tensile strength data [9].

While mobile devices are only one driver for low-temperature cure [2], another important driver is wafer warpage, especially in light of designs with wafer thinning down to 30μm. In addition, a number of recent WLP designs emphasize the need for a low-temperature cure, photo-definable stress buffering dielectric with excellent adhesion at multiple interfaces. For example, in reviewing several WLCSP designs, Liu et al., points out reliability benefits with 1) solder bumps having polymer collar or other BOP approaches for local stress relief, 2) warpage reduction based on

over-molding and passivation layer balance, and 3) polymer buffer layers in panel-based packaging for improved solder joint reliability [2].

In related investigations, WLCSP designs have also been modeled with the goal of eliminating solder joint failure, and the junction of solder, Cu UBM, and polyimide was identified as the typical failure site. In a similar study, Xu, et al., at Qualcomm, fabricated and tested several designs with a focus on UBM, RDL and solder ball type, T-cycle and drop shock testing, which led to design recommendations of thicker RDL and Cu-based UBM [19]. Lastly, Rogers, et al., recently described a fully-molded FO-WLP technology. Requiring stress buffering passivation layers with low-temperature cure and excellent adhesion, advantages of this technology include a more continuous, stronger die/mold interface, reduced delamination, and improved board-level reliability.

Low-temperature cure (200-250°C), photo-definable PBO materials have been recently commercialized, and the properties of these PSPBO formulations are compared with high-temperature cured (above 300°C) PSPI and PSPBO in **Table 2**. Compared to the standard, 320°C cured HD-8820 PBO, the low-temperature cure, HD-8930 and HD-8940, PBOs offer comparable tensile strength, elongation, modulus, CTE with reduced residual stress and minimal loss in T_g and thermal stability. Both HD-8930 and HD-8940 are formulated for copper compatibility. Of the two PSPBOs, HD-8930 PSPBO has superior chemical resistance, whereas HD-8940 is more optimized for adhesion to copper.

Summary

PI and PBO materials require unique synthesis and chemistry to yield valued material properties, and the photosensitive chemistries are especially distinct in that a combination of acrylic cross-linkers or a photo-activated dissolution inhibitor/enhancer may be used. In addition, WLP, fan-out, W2W bonding for TSVs, and other 2.5/3D architectures require unique demands of RDL passivation, stress-buffering layers and high elongation and tensile strength for reliability, along with requirements of high-temperature adhesives. PSPI and PSPBO chemistries have to meet the challenges of low-temperature cure, low stress, copper compatibility and improved adhesion. As new packaging design and processing techniques emerge, new

formulations and chemistries for PSPI/PBO materials will be developed to meet challenges such as low viscosity or high-contrast, thick passivation layers with the optimum balance of ability to relieve local stress, adhesion, and chemical resistance.

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Biography

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3D high-density channel integration of a polymer optical waveguide using the Mosquito method

By Takaaki Ishigure, Daisuke Saganuma, Kazutomo Soma [Keio University]

Over the past decade, fiber optics has become not just a technology dedicated for telecommunication networks, but has also been applied to inter-rack wirings for high-performance computers and servers in data centers. In the community of optoelectronics, it is well known that a super computer – ASC purple developed at IBM in 2005 – was the first to install multi-mode fiber (MMF) links. Triggered by this machine, MMF links have been deployed widely in several high-performance computers (HPCs) mainly connecting their internal racks, because fiber-optic links have the potential to contribute not only to increasing the data processing speed, but also to maintaining the low-power dissipation of the whole computing system. Since then, optoelectronics technologies have been gradually penetrating into racks: fibers come closer to the chips on the board. For on-board wiring, optical printed circuit boards (OPCBs) on which multi-mode polymer optical waveguides are incorporated, have been regarded as a promising component, and many papers have already been published [1-4]. Over the past decades, OPCB links have aimed to transmit a data rate up to 10Gbps/ch. However, because of technical advances in electrical counterparts, optical channels are now required to transmit at least 25Gbps. In addition, a key advantage of optics should be the ability to support high-bandwidth density wiring. However, almost all the previous demonstrations utilizing multi-mode polymer waveguides did not necessarily satisfy the requirements, particularly when the core of the waveguides has a conventional step-index (SI) structure.

In order to realize high-bandwidth-density OPCB links, we have proposed the formation of graded-index (GI) circular cores in polymer optical waveguides, by which optical characteristics such as low propagation loss, low coupling loss with GI multimode fibers (MMFs), and low inter-channel crosstalk are realized. Because the photolithography process based on UV-exposure via a photomask has been a representative

fabrication methodology, it is difficult to form GI circular cores in polymeric films. To address this issue, recently, we developed a very simple fabrication methodology for GI circular core polymer waveguides and named it “the Mosquito method” [3]. Here, we discuss the potential of the Mosquito method: it is capable of forming 50 μm diameter GI circular cores with not only a straight parallel alignment, but also complicated circuit patterns with curved core alignments. Furthermore, the Mosquito method allows three-dimensional wiring. After specifying how the core diameter and pitch could be reduced, we investigate three-dimensional channel alignments.

Using photolithography, 2-D polymer waveguide arrays can be fabricated, but several 2-D arrays need to be stacked to realize 3-D alignment, which should be a very complicated procedure. Even if a 3-D aligned waveguide is fabricated using this method, it would be difficult to draw cores that straddle the layers. Meanwhile, the Mosquito method has a large advantage in forming three-dimensional waveguides, because it resembles popular 3-D printing technologies. This article includes the review of a conference paper presented at ECTC 2014, which received the outstanding session paper award [4].

The Mosquito method

For on-board interconnect applications, the waveguides need to be connected with MMFs with a 50 μm diameter GI circular core. In order to connect the waveguides with a GI-MMF with low connection loss, the same structure as the GI-MMF – a GI-circular core in polymer waveguides – is ideal. Therefore, we have focused on how to form a GI circular core in polymers. Then, we developed a new methodology: the Mosquito method [5, 6]. The method is a very simple fabrication technique

that utilizes a microdispenser (Figure 1). First, a monomer for the cladding (low-refractive index) is coated on a substrate. Then, a viscous monomer for the core (high-refractive index) is dispensed from a thin needle of a syringe that is connected to a dispenser. In the Mosquito method, the needle tip remains inserted into the liquid state cladding monomer while dispensing the core monomer. The needle scans horizontally within the cladding monomer, resulting in the formation of a waveguide structure. Parallel arrays of circular cores are fabricated by repetitive parallel scans of a single needle (Figure 1).

For the waveguide material, we use silicone resins supplied by ADEKA Corp. (FX-W712 and FX-W713 for the core and the cladding, respectively). Because these two monomers are miscible, after the core monomer is dispensed, the two monomers diffuse slightly into each other to form a concentration distribution. After dispensing multiple cores, both the cores and cladding are exposed to a UV LED for curing. As the obtained polymer is a three-dimensionally cross-linked copolymer, the fabricated waveguides have a high durability (up to 250°C).

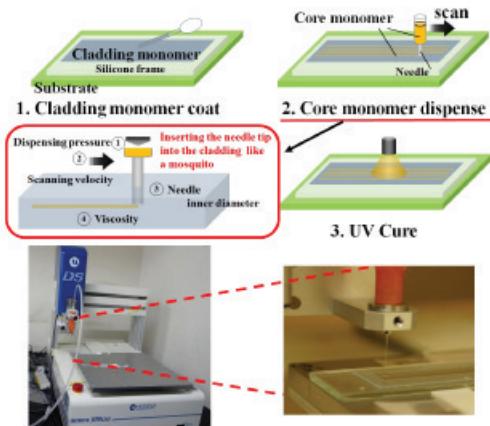


Figure 1: Fabrication process of polymer waveguides using the Mosquito method. Photo (left): desktop robot with a syringe; (right): needle dispensing core into cladding.

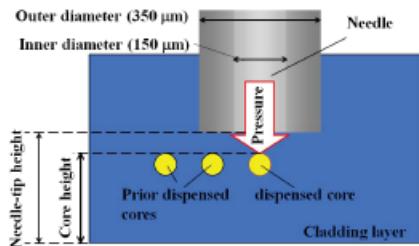


Figure 2: Height of dispensed cores in the cladding.

Parallel waveguide

We already succeeded in fabricating a parallel waveguide with a 40 μm core diameter and a 125 μm pitch [5] using the Mosquito method. As mentioned above, multiple scans of a single needle are required for a parallel core alignment. Here, the outer radius of the needle is wider than 125 μm . However, an inter-channel pitch narrower than the outer needle radius is realized. In our previous investigations [6], we found that the dispensed core monomer sank slightly in the cladding monomer probably due to the dispensing pressure, as illustrated in **Figure 2**. Therefore, the repetitive needle scanning shows little influence on the parallel



Figure 3: Cross section of a waveguide with 40 μm cores and a 62.5 μm pitch.

core alignment even if the pitch is narrower than the needle's outer radius.

So, in this paper, we focus on how we can decrease the inter-channel pitch. First, we fabricate a waveguide with a 40 μm core and 62.5 μm pitch. A cross section of the fabricated waveguide is shown in **Figure 3**. The pitch of this waveguide is measured to be $61.7 \pm 3.4\mu\text{m}$, which is the average value for twelve channels. From **Figure 3**, we confirm a high pitch uniformity even for a pitch as narrow as 62.5 μm . Meanwhile, a pitch smaller than 62.5 μm should be possible if the core diameter is smaller than 40 μm . **Figure 4** shows a cross section of a waveguide with a 40 μm pitch where the core diameter is set to be 25 μm .

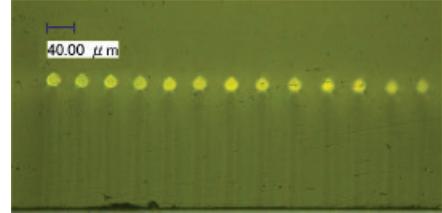


Figure 4: Cross section of a waveguide with 25 μm cores and a 40 μm pitch.

In this case, the pitches for the first 6 cores from the left edge look slightly narrower than the pitches for the rest of the cores. Therefore, the minimum pitch size could be approximately 50 μm when the same needle (and the same monomers) are used.

Three-dimensional wiring

Because the needle tip is inserted into the cladding, if the needle scans vertically as well as horizontally, three-dimensional waveguides can be formed. Therefore, to form 3-D waveguides, the needle tip needs to scan in an appropriate range of height from the substrate surface, specifically at the bottom of the cladding.

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When we use a cladding with a $380\mu\text{m}$ thickness, we found that the height of the needle should be within 120 to $240\mu\text{m}$ in order to form the cores with a high degree of circularity [6]. Applying this result, we designed three-dimensional waveguides: multi-layered structures and a fan-in/out structure.

Multi-layered structure. First, for investigating the possibility to form a multi-layered structure, a 1-channel and 5-layer polymer waveguide is fabricated as shown in **Figure 5a**, by repeating the horizontal needle scan with a different height from the substrate surface with a $125\mu\text{m}$ step. **Figure 5b** is a cross section of a fabricated 1-channel 5-layer waveguide. It is confirmed that the cores on the higher layers are aligned very accurately.

Then, 12-channel and 2-layer waveguides are fabricated [7]. **Figure 6** is a cross section of a fabricated two-layer polymer waveguide. The pitches in the top and bottom layers are controlled

to be $127.5 \pm 1.8\mu\text{m}$ and $127.2 \pm 2.7\mu\text{m}$, respectively. It is found that the horizontal pitch error is remarkably small, while the vertical position accuracy is not highly controlled. This could be because when the needle scans for the top layer cores, the dispensed core monomer pushed the cladding monomer, thus disturbing the alignment of the bottom layer cores.

Fan-in/out structure. A fan-out structure is formed in a 10cm long waveguide as shown in **Figure 7**. In this waveguide, on edge (a), the 7 cores are hexagonally stacked with a $40\mu\text{m}$ pitch, which is the same core alignment as a multi-mode multi-core fiber (MM-MCF) [8], while a 1-D alignment with a $250\mu\text{m}$ pitch is realized on edge (b), as designed. Here, the core alignment on edge (a) is a design feature: a 3-layer alignment (2-3-2) of 7 cores is rotated counter-clockwise with an angle of 15° on the center core (channel 4), as shown in **Figure 7**. This rotated design allows easy vertical core alignment conversion because all the cores have different vertical positions.

The total length of the fan-in/out waveguide is 10cm , where the core alignments at both ends remain within the 2cm long region, while the 6cm long middle part is allotted for the pitch conversion. In order to distinguish the effect on the loss between vertical and horizontal core bending, the pitch is converted only horizontally in the 5cm long region, followed by only vertical conversion in the rest of the middle part.

The surface plan and cross sections on edges (a) and (b) of a fabricated fan-in/out waveguide are shown in **Figure 8**. The numbers from 1 to 7 indicated in **Figure 8** are the channel numbers drawn by the needle in order. The designed fan-out device in **Figure 7** was fabricated successfully utilizing the Mosquito method. The minimum and maximum insertion losses among the 7 cores in this waveguide, however, were as high as 5.26 and 11.22dB , respectively, at 850nm [9]. So, in this paper, we present a new design as shown in **Figure 9b**: the lengths for the pitch conversion in the horizontal and vertical directions are 4cm and 2cm , respectively. The 2cm long straight parts at two edges in **Figure 9a** are removed for the design in **Figure 9b** to achieve compact fan-in/out with low insertion loss.

The measured insertion loss of each channel in fabricated fan-in/out

waveguides (A) and (B) is shown in **Figure 10**. For these loss measurements, 1m long $25\mu\text{m}\varnothing$ GI-MMFs are used for launch and detection probes, and these probes are actively aligned in butt-coupling to each core. A vertical-cavity surface-emitting laser (VCSEL) emitting at a wavelength of 850nm is used for the light source.

From the results (**Figure 10**) for designs (A) and (B), a remarkable loss reduction is confirmed only by increasing the length for the vertical core bending. In addition, it is also found that the straight regions at both edges affect the insertion loss particularly in channel 1 and channel 2, which are dispensed prior to the other 5 cores. Because the inter-core pitch on edge (a) is as small as $40\mu\text{m}$, the needle scan for dispensing the channels 3 to 7 could cause an alignment deviation in channel 1 and channel 2, resulting in an excess micro-bending loss. From **Figure 10**, the average insertion losses of waveguide (B) was calculated to

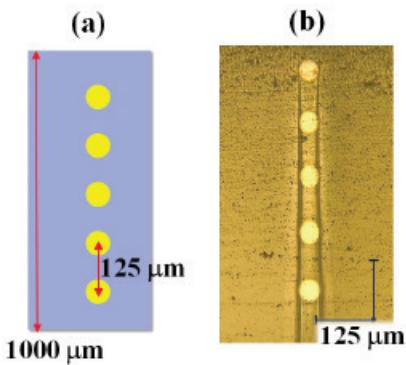


Figure 5: Cross sections of a) designed and b) fabricated 1-ch. 5-layer polymer waveguide.

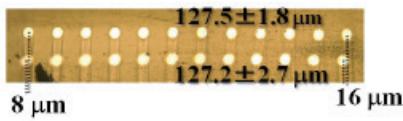


Figure 6: Cross section of a two-layered waveguide.

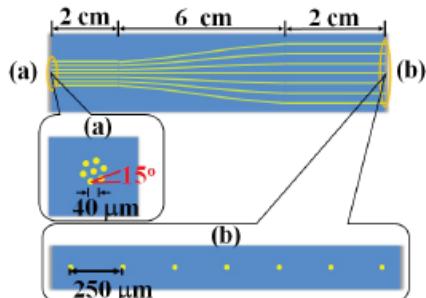


Figure 7: Design of a fan-in/out waveguide.

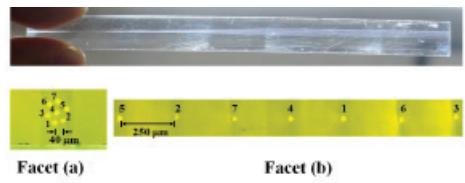


Figure 8: Surface plan and cross sections of a fan-out waveguide.

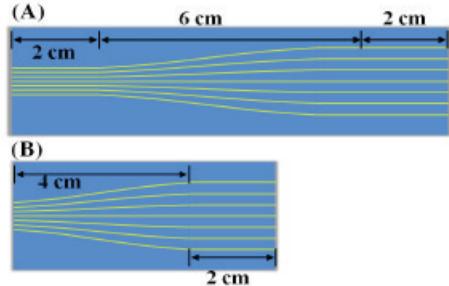


Figure 9: Compact design of a fan-in/out waveguide (B) compared with the original design (A).

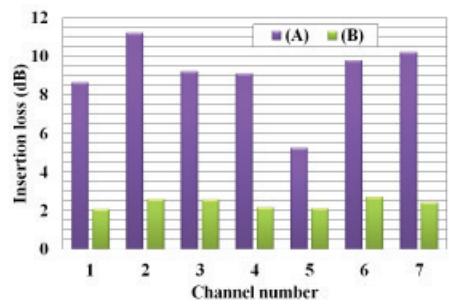


Figure 10: Comparison of insertion losses in obtained fan-in/out waveguides.

be 2.39dB, which is a marked reduction compared to the original design.

Summary

By optimizing the dispensing and needle scan conditions, we succeeded in fabricating GI-circular core waveguides. For high-density wiring, the inter-channel pitch is decreased to 40 μ m, despite the needle outer diameter being larger than 300 μ m. Such a narrow pitch alignment is possible because the dispensed core from the needle sinks slightly into the cladding; repetitive needle scans show little effect on the core shape and alignment.

The needle scans in both the horizontal and the vertical directions in the Mosquito method, make it possible to create three-dimensional waveguide circuits: multi-layered parallel waveguides and a 3-D core alignment conversion for a 7-core MM-MCF. The Mosquito method, which is very similar to a 3-D printing technology, would be a promising way to create polymer optical components, not only for high-bandwidth density on-board optical interconnects, but also for a wide variety of optical applications.

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This work was the recipient of the Outstanding Session Paper award at ECTC 2014. The Optoelectronics Packaging subcommittee solicits papers on all topics pertaining to the design, development, and technology of packaging silicon photonics; optical interconnects; parallel optical transceivers; single-mode or multi-core connectors; optical waveguide coupling; optical chip-scale, heterogeneous, and microsystem integration; and 3D photonics. Submission deadline for 2016 ECTC is August 13, 2015. For more information, please visit www.ectc.net

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The transition of thermocompression bonding to HVM

By Tom Strothmann *[Kulicke & Soffa]*

High-volume use of thermocompression bonding (TCB) in semiconductor assembly processes has recently started and the known benefits of the technology, such as reduced form factor and higher speed with reduced power, are now being realized. The production status of TCB has changed since the process is ramping for the production of stacked memory products. Both the hybrid memory cube (HMC) and high-bandwidth memory (HBM) are using TCB in the assembly process.

The adoption of TCB assembly processes can be attributed to three significant factors. The first factor is cost, wherein the known technical benefits of the technology can be achieved with a competitive cost structure. The second factor is process control. Current TCB equipment has implemented exceptional process control capability to ensure any process deviation is detected quickly and product risk is controlled. The third factor is data integration, where the equipment uses full data logging capability and traceability for all die back to the silicon source wafer. Recent advances in TCB equipment offer solutions for all of these factors for both chip-to-substrate (C2S) and chip-to-wafer (C2W) bonders.

Fundamental requirements and state-of-the-art

Thermocompression assembly enables next-generation fine-pitch, 2.5D and 3D assembly technologies using fine-pitch Cu pillar interconnects with typical pitches of 40 μm and pillar heights of 30 μm . High-accuracy placement is required to ensure high yield, with placement accuracy of $\pm 2\mu\text{m}$ typically required. Memory products are driving the commercial volume in the technology, using TSV technology and thin die stacks

ranging from 4 to 16 layers in height. The thickness of the die with through-silicon vias (TSVs) can be 50 μm or less, so equipment must be designed to handle and bond thin die without inducing mechanical damage. Accurate control of force before and during the bonding process is critical as is the capability to switch the recipe between force and position mode during the process. Force is particularly critical for bonding with non-conductive paste (NCP) or non-conductive film (NCF) underfill because forces upwards of 300N may be required during these bonding processes. The last fundamental and most critical requirement is high units per hour (UPH) for the process. The cost of TCB must be competitive with alternative assembly technologies and this can only be achieved if the throughput and yield of the process is high. Actual process time will vary based on the process selected, but a UPH of >1000 is generally considered to be the threshold for cost-effective production. The fundamental equipment requirements are summarized in **Table 1**.

Attribute	Specification/Requirement
Die Thickness	$\geq 35\mu\text{m}$
Accuracy	$\pm 2\mu\text{m}$ (3s), $\pm 20\text{ mdeg}$ (3s) post bond $\pm 1\mu\text{m}$ (3s), $\pm 10\text{ mdeg}$ (3s) glass die
Planarity	2 μm /10mm
Force	0.5 to 300N (500N required in future)
Force Accuracy	1% (or 0.25N in low force applications)
Z Height Resolution	$\pm 1\mu\text{m}$ (with temperature compensation)
Temperature Ramp	200°C/s (heat ramp), 100°C/s (cooling rate)
Sprint UPH	3000 UPH
Metrology	Die crack detection, Post bond inspection, Contamination inspection

Table 1: TCB equipment specification requirements.

TCB demand and memory market attributes

TCB volume is driven by the memory market because stacked DRAM die with TSVs have extremely short routing length between the die, resulting in substantially better performance and reduced power consumption. DDR4,

Wide I/O 2, HMC, and HBM can all be assembled using the technology and the choice of memory architecture is heavily dependent on the application. Lower silicon cost for DDR4 probably makes it the best for cost-sensitive mobile markets including tablets and low-end smartphones. Wide I/O 2 provides better heat dissipation, power, and bandwidth than DDR4 with higher cost, and is probably the best choice for high-end smartphones. Designs using HBM and HMC have better bandwidth with reduced power, but are more expensive. HBM memory may be the best choice for high-end computer graphics processing, which is less constrained by cost. Both AMD and Nvidia have also announced the use of HBM in their next-generation graphics modules. HBM products are typically assembled with interposers to enable very high-density routing to the HBM stack, creating a demand for chip-to-wafer (C2W) TC bonders. High-performance computing (HPC) or networking routers are best matched to the HMC. Intel recently announced that its Xenon Phi processor "Knights Landing" will use the Micron HMC stacked DRAM. Because of the interface design and reduced requirement for routing density, HMC can be assembled on laminate with chip-to-substrate (C2S) TC bonders. HBM and HMC currently drive the highest demand for TCB.

Demand for TC bonding beyond memory will likely be driven by assembly of advanced node products at 14nm and below. TCB reduces the stress on the Cu pillars because the local reflow characteristic of the technology causes less expansion mismatch between the die and the substrate during assembly. **Figure 1** is representative of a TCB stacked memory structure using thin TSV memory die.

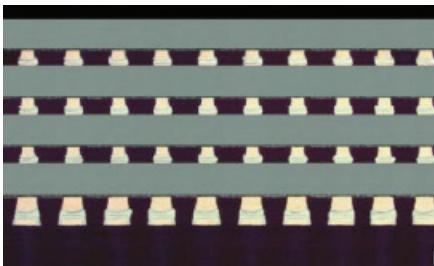


Figure 1: 50µm thick top die stack using 30µm bondline thickness.

TC bonding processes and cost

Processes used for TCB today can be grouped into two main categories: processes that use a pre-applied underfill, and those that apply underfill after the bonding process. Underfills applied prior to bonding can be in the form of a non-conductive paste (NCP) applied to the target surface, or a non-conductive film that is applied to the wafer prior to dicing (NCF). In both cases, the underfill must not only create a void-free bond, but also provide flux to remove oxides at the solder interface. If underfill is not applied before the bonding process, it is typically done as a capillary underfill (CUF) after the bonding process. The die is underfilled in much the same way as in standard flip-chip processes, however, the underfill process is more challenging because of the narrower bondline of a typical thermocompression bonded device. The four potential processes are described with key attributes in **Table 2**. Both HMC and HBM can be assembled with a TC CUF process; however, there is a trend toward NCF to achieve greater process stability as die stack height increases. The advantages and disadvantages of each of these processes are outlined in **Table 2**.

Factors affecting throughput

There are several machine factors that affect throughput that need to be optimized for each type of process run on a TC bonder. The relative allocation for the various factors is shown graphically in **Figure 2** and compared for the various processes.

TC bonding with NCP. TC-NCP is the most established of the thermocompression bonding processes. It has seen intermittent high volume for several years, although typically with low UPH. The non-conductive paste is dispensed onto the substrate prior to bonding and distributed uniformly with pressure during the bonding process. The NCP is partially cured during the bonding process, protecting the solder joints from the stress that develops between the die and the substrate during cooling.

The process avoids the need for capillary underfill after the bonding process and presents a device ready for over-molding.

High-quality, void-free TC-NCP processing with greater than 1100 UPH has been demonstrated on advanced dual-head TC bonders. Examining the allocation of time to each of the process steps in **Figure 2** and the summary in **Table 3**, it can be seen that two-thirds of the cycle is consumed by the actual bonding process, whereas only one-third of the time is spent transporting the die, aligning it, and waiting for the bond head to cool an acceptable die transfer temperature. Substantial improvements in throughput will be difficult to achieve without reducing the actual bonding process time, although it is expected that a UPH of >1400 is possible. The process time can only be reduced further through collaboration. The materials suppliers must provide materials with improved flow properties and faster curing rates while the tool vendor must provide machines with enhanced process control, advanced process features, and the in-depth process understanding to enable the use of the advanced materials.

One disadvantage of NCP is the risk of contaminating the bonding tool. As the NCP flows under the die, it must completely fill in the bondline space and any excess will squeeze out to form a fillet. For thick die, the volume contained in the fillet is large and can accommodate variability in the dispense volume or the bondline thickness. Die with a thickness less than 100µm do not have adequate volume in the fillet to account for

normal variation in dispense volume and bondline thickness, so there is a potential for the fillet height to exceed the die thickness and contaminate the bond tool. While TC-NCP is an excellent choice for die above a thickness of 100µm, it is not realistic for very thin die or for die stacking.

TCB with NCF. NCF has some of the same advantages as non-conductive paste in that it eliminates the need for capillary underfill and reduces the stress on the copper pillars during the bonding process. NCF has the additional advantage that it is already uniformly distributed on the die, so it is easier to achieve a uniform and void-free underfill. Because less material flow is required and thickness control is very good, the chance of having excess underfill flow out and contaminate the bonding tool is reduced; this makes underfill film a very attractive solution for thin die and stacked die and has resulted in the use of NCF in memory products.

NCF is used in volume production today although the development of new NCF materials is on-going. Development

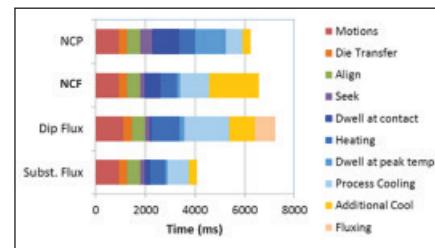


Figure 2: The relative allocation for the various factors is shown graphically.

	Process	Advantages				Disadvantages			
		Paste	Film	Dip Flux	Substrate Flux				
No Pre-applied Underfill	Paste	<ul style="list-style-type: none"> Low stress Die is underfilled during TCB Mature process UPH ≥ 1100 				<ul style="list-style-type: none"> Large potential for tool contamination with thin die Void-free underfill requires slower process Longer bond times to ensure curing High force required for high bump counts 			
	Film	<ul style="list-style-type: none"> Low stress Die is underfilled during TCB Less chance for tool contamination than paste UPH ≥ 1100 				<ul style="list-style-type: none"> Some chance of tool contamination for thin die Void-free underfill requires slower process Large temperature changes each cycle (slower) High force required for high bump counts Films still under development 			
	Dip Flux	<ul style="list-style-type: none"> No chance of tool contamination Very short bonding process times Low forces even for high bump counts UPH ≥ 1000 				<ul style="list-style-type: none"> Requires post-bond CUF (difficult for large die) More stress on bonds before CUF Requires cooling to <100C at dip fluxing station 			
	Substrate Flux	<ul style="list-style-type: none"> Very fast – very small bond head temp changes per cycle UPH ≥ 1500 				<ul style="list-style-type: none"> May require flux cleaning Requires post-bond CUF – difficult for large die More stress on bonds before CUF Fluxing processes still under development 			

Table 2: TCB process comparison.

	NCP	NCF	Dip Flux	Substrate Flux
Bonding	66%	42%	47%	48%
Additional cooling	5%	31%	14%	8%
Die handling & align	29%	27%	39%	44%
Cycle time	6.3	6.6	7.2	4.1

Table 3: Cycle-time allocation between bonding processes.

of the films is challenging because of the diverse requirements placed on them. The film must be stable during the die pick operation, become nearly liquid without curing during the temperature ramp, and cure very quickly at a temperature below the melting point of the solder. It should also contain a high percentage of filler particles to reduce the expansion coefficient, yet still have some transparency to ensure alignment marks are not obscured.

Underfill films have been developed that meet the requirements listed above, but all require that the probe tool of the bonder go through a large temperature excursion. Many films become sticky above 80°C thereby limiting the die transfer temperature. Analysis of the cycle time components in **Figure 2** and **Table 3** shows that nearly half of the process time is consumed by cooling, despite a cooling rate of 100°C/s. The most effective UPH improvement

will come from improved cooling speed because 50% faster cooling improves UPH by 15%. Current NCF formulations are expected to limit the UPH to about 1400, so a higher UPH will require reformulation to enable a higher transfer temperature. This work is on-going but collaboration between equipment and materials suppliers is the key to improved throughput and overall cost reduction.

TCB with dip flux and CUF. The TCB-CUF process dips the die into flux prior to placement and TCB. A key advantage is the absence of any pre-applied underfill, which eliminates the possibility of bond tool contamination. It is for this reason that it is extensively used for die under 100µm thickness and for stacking of very thin die. There are, however, significant disadvantages to this process. The process requires a challenging capillary underfill operation into very narrow bondlines and there is no stress relief for the solder joints until this underfill is completed. Throughput is low because the flux dip, die transport, alignment and seek, must all be done below about 100°C to avoid evaporation of the flux and premature flux activation. The resulting temperature excursion within a bonding cycle is similar to the case of bonding with underfill film, however, there is the added step of flux dipping with the associated throughput penalty.

The most significant throughput improvements can come from speeding up the dip flux process itself and from higher cooling rates. Implementation of these items and a number of smaller improvements can bring the dip flux process to a UPH of about 1200 for a dual head machine, however, going beyond 1200 UPH with a dip flux process will be challenging without changes in the flux itself to allow dipping at higher temperature.

TCB with substrate flux and CUF. Thermocompression bonding using substrate flux has the potential to provide a very high-throughput process, but it is not applicable to stacked die. Substrate fluxing substantially reduces the required temperature cycle in the process because the bond head is only handling bare die and can remain at fairly high temperatures throughout the bonding cycle. A transfer temperature of 150°C has been demonstrated, and it is expected that temperatures of 200°C might be possible. The temperature excursion of the bond head is then only about 100°C. The process eliminates the chance for tool contamination.

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with underfill and so it should be useful for thin die-to-substrate bonding. As with dip fluxing, capillary underfill is required and may be challenging.

Much of the current efforts in substrate fluxing are aimed at finding a good method of applying the flux. Too much flux may require added bonding times to boil it off, or make it difficult to clean before the underfill process. Insufficient flux may not fully remove oxides at the solder interface. Accurate control of flux volume will be critical to ensure this process achieves the highest UPH.

The current baseline process already provides a UPH of 1600 and has the potential for UPH near 2000. Although methods of flux application still need to be optimized and questions about flux residue remain, this process has the potential to be the fastest of all the TC processes.

TCB cost vs. alternative technologies

A rigorous analysis of TC bonding must look at the total packaging cost as well as the overall cost-benefit of the technology. While TCB enables higher I/O counts and finer

pitch interconnects through better control of the stress and warpage, the actual bonding process is only a small contribution to the overall assembly cost. The TC bonding process flow enables savings through the elimination of other process steps and their associated operating costs. **Table 4** summarizes the assembly process flows for a baseline C2 process (i.e., a process using mass reflow as in standard FC or C4, but with Cu pillar die) and various TC processes with different fluxing and underfill technologies. Capillary underfill is still the dominant process, being used for more than 80% of devices[1,2]. Alternatives are emerging to address issues of CUF with tighter bump pitches and reduced bump height. Pre-applied underfills like non-conductive paste (NCP) or non-conductive film (NCF) are used in about 5% of cases [1] and avoid the need for CUF, as shown in **Table 4**. NCP and NCF processes add material cost relative to CUF but allow for finer pitches and stacked die applications. The selected die bond and

underfill process affects the assembly process flow, so all steps need to be considered for cost analysis.

A cost analysis and comparison was performed using the SavanSys Solutions flip-chip cost model [3] for the processes in **Table 4**. SavanSys offers an activity-based cost modeling approach, i.e., the total packaging cost is determined by analyzing the required time, the amount of labor, material cost, tooling cost, equipment depreciation, and yield loss for each process step (see for example ref. [4]).

An application processor unit (APU) such as may be found in high-end mobile devices was used for the model: 15 x 15mm Pop design package (bottom die only), 28nm process node, C2 mass reflow process with CUF, and a 1-2-1 substrate design.

Table 4 shows an overview of die, substrate, assembly and total packaging

	Die	Subst.	Assembly	Die Bonding	Total
C2 - CUF	\$11.96	\$0.58	\$5.10	\$0.77	\$17.64
TC - CUF	\$11.96	\$0.58	\$5.14	\$0.84	\$17.67
TC - NCP	\$11.96	\$0.58	\$5.34	\$1.24	\$17.88

Table 4: Packaging cost comparison of C2 mass reflow vs. TCB.

LC-2 Burn-In Value Menu

8-slot • single zone



32-slot • multiple temperature zone



64-slot • production oven



Nutrition Facts

Serving Size:
Choose the Size You Need
Servings Per Container: 1

	Amount Per Serving	100% Daily Value*
Total I/O	up to 256 channels per BIB.	
Total Power	up to 500 Amps of DUT current available per BiB, up to 10 individually programmable power supplies, up to 150 Volt power supply outputs.	
Total Flexibility	up to 8M vector memory depth with scan capability per BiB, individual temperature control up to 50 Watts, compatible with many BiB sizes.	

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cost for the reference device using a C2 reflow process relative to TC-CUF and TC-NCP processes for the same device. Throughput for TC bonding is set at 1000 UPH whereas 2500 UPH was assumed for C2 reflow. Die and substrate cost are estimated at \$11.96 and \$0.575, respectively. The assembly cost ranges from \$5.10 for the reference device to \$5.14 and \$5.30 when using TC-CUF and TC-NCP. The cost that each process step adds is divided into labor, material, capital, tooling, yield loss and indirect cost portions. The resultant die bond process step accounts for 15-23% of the assembly cost and the increase in assembly cost for the use of TCB is less than 5%.

Process control

The second factor enabling HVM use of TCB is process control. The TC bonded assembly process is complex and requires extensive process control measures. Assembly yield excursions in the process dramatically add to the cost of the process and are unacceptable given the high cost of known good die used in the assembly operation. This is particularly true in a stacked-die process where an error in bonding one die can result in the loss of the entire stack at significant cost to the customer. Characteristics such as temperature uniformity, z-position compensation, and well-controlled accuracy at high force must be inherently stable and optimized through machine design. There are, however, several key process characteristics that must be monitored and controlled throughout a bonding process. The bonding process can have as many as 10 individual steps controlling temperature ramps, z-position, force, and vacuum release.

With requirements for multiple parameter tracking, limits for process control and statistical trend analysis on primary and secondary parameters, the process controls for TC bonding are closer to those required in a front-end fab process than a typical assembly process. The shift in process control strategy represents a paradigm shift for process control for a reflow process. Process parameters such as temperature, force, Z-position, and placement accuracy must be carefully controlled during the bonding process, but it is also useful to monitor secondary process parameters such as time-to-solder melt. This means the machine must not only have limits set on key parameters, but also the ability to compute secondary parameters and analyze trend data in real time. Typical process control parameters are shown in **Table 5**.

The importance of secondary parameters can be demonstrated with the example of solder melt detection and process control for the time to melt parameter. Time-to-melt is not a direct parameter like temperature, force or position. It is a calculated parameter derived from measuring the time elapsed from the point of contact of the die to the target surface to the point where the solder melts. Solder melt can be determined by carefully monitoring the Z-position while applying low force during the temperature ramp. A shift in Z-position indicates the solder has melted. A stable process will have a predictable time-to-melt where control limits can be established. Time-to-melt can be considered a macro parameter for the process because it is one that does not look at a specific characteristic, but rather the overall health of the process. A change in the time-to-melt can be an indicator of bond head heater performance change over time, degradation in the thermal interface to the bond head or changes in planarity. Time-to-melt is also a very useful parameter to look at for validation of the portability of the process between bond heads and multiple tools.

Advanced metrology is a key enabler for effective process control and innovation in metrology is required for any successful TC process. These tools should also include inspection for damaged die after pick, post-bond placement accuracy verification, checks for place tool contamination and in-line measurement of underfill dispense volume.

Data logging and communication

The third factor enabling HVM use of TCB is data integration. Although the equipment can operate as a stand-alone system, it must use full data logging capability, including die traceability and the capability to support host communication to import and export yield maps. The machine should also have the capability of feeding real time data into the host MES regarding machine status and WIP. The most effective implementation of the TC process utilizes a systems approach wherein the machine operation accounts for upstream process variation while providing a data stream for downstream processes. This data integration into the customer network is a critical component to support yield enhancement programs. Advanced process control systems are used to integrate the TC bonding equipment into the factory process flow. The metrology used in the TC bonder enables real time metrics for inline process control and fault detection and software design enables data feed for fault detection and classification (FDC) and run-to-run (R2R) control to provide fast reaction times and short control loops. The diagram shown in **Figure 3** represents the fundamental concept for incorporation of a TC bonder into a factory APC system. The basic requirements for data logging and host communication are shown in **Table 6**.

Parameter	Comment
Placer temperature	Selected bond step
Force	Min, max, average at defined bond step
Z-Position	Selected bond step, multiple steps possible
Maximum Temperature	During the bonding cycle
Temperature at Vacuum Release	Placer temperature during release of the die after bond
Stage Temperature	Sampled at selected bond step
Post Bond Accuracy (X)	Measured value after bonding
Post Bond Accuracy (Y)	Measured value after bonding
Time to Melt	Secondary calculated factor

Table 5: Typical process control parameters for TCB.

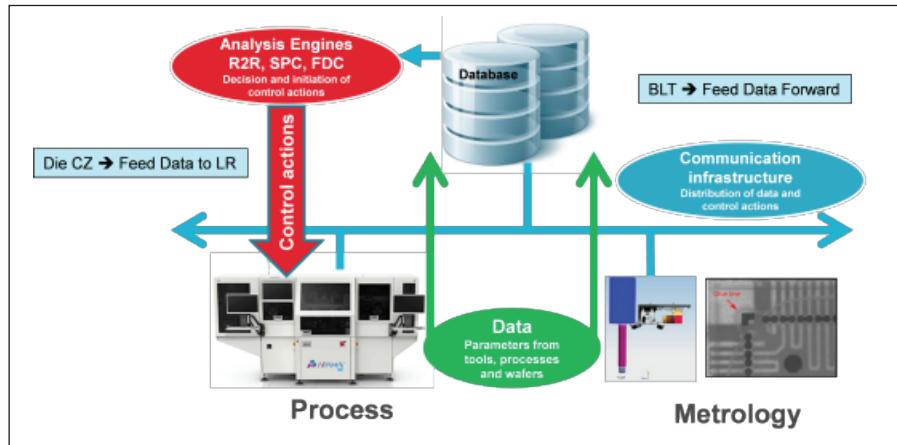


Figure 3: TCB incorporation into advanced process control.

Typical Host Communication Requirements (SECS/GEM)		Material Identification Tracking
Wafer maps imported (pick good based on map)		Source Wafer ID
Wafer maps exported (bonded die traceable to source wafer)		Source Wafer Position ID
Status of production work in process		Target Wafer ID (C2W)
Process data logged for each die bonded		Target Wafer Position ID (C2W)
Plot of key parameters for a single die		Layer position
Plot of key parameters over multiple die		Bond position
Process monitoring and intervention by host		X, Y position on substrate (C2S)
Process out of control notification to host		Strip ID (C2S)
Store raw data in a network file system		
Import process control parameters from host		

Table 6: Typical communication requirements.

Summary

Thermocompression bonding has reached an inflection point where the high-performance attributes of the technology have been enabled by the reduced unit cost of the process. Advanced TC bonders are now used to produce high-end stacked memory packages at a competitive cost. The state-of-the-art TC bonder enables high UPH and high yield on a variety of assembly processes through optimized machine design and rigorous process control capability. TC bonding also enables higher I/O counts and finer pitch interconnections than traditional interconnect methods through better control of the stress and warpage between devices and the substrate. This capability will be critical for the next-generation advanced node

products using increased I/O count and fragile dielectric layers. Although cost has previously been considered a barrier to the implementation of TC bonding processes, an analysis of the total cost of competitive processes shows the incremental assembly cost adder for TC bonding is actually rather small in a high-UPH TC bonder. The hurdle to widespread adoption of the TC bonding will more likely be the initial capital expenditure associated with buying new equipment when depreciated infrastructure already exists for mass reflow processes. Adoption of the technology will therefore be driven by technical need and market forces. Once the infrastructure is established, the cost is directly proportional to throughput and throughputs of more than 1000 UPH have been demonstrated and reasonable roadmaps exist for extending throughput to more than 1500 UPH. Collaboration between assembly,

equipment and materials engineers will be the key to achieving these substantial improvements and additional cost reduction for the TC process.

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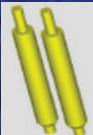
Biography

Tom Strothmann received his BA from the U. of Kansas and is a Director of the Advanced Packaging LR Business Line at Kulicke & Soffa; email tstrothmann@kns.com



Ultra Low Inductance enables High Speed Testing

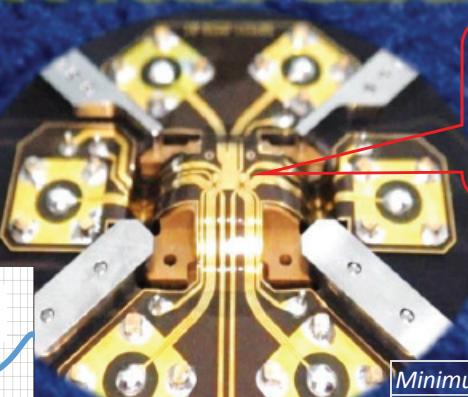
YPX Probe Card

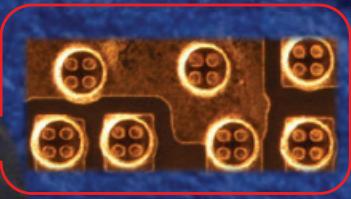


Pogo-pin



YPX





Graph showing Inductance (nH) vs Frequency (GHz) for Pogo-pin and YPX:

Inductance @ 1GHz	Pogo-pin: 1.12nH	YPX: 0.08nH
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Minimum Pitch	200um
Stroke	100um
Contact force/pin	0.049N(5gf)~
Trace L/S	20/20um
Insertion Loss	-3dB@20GHz
Return Loss	-15dB@20GHz

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COMPANY HEADQUARTERS Street Address City, State, Zip Country Telephone Fax Website	BONDING TOOLS	WHAT ELSE THEY MAKE
DIE-BONDERS		
Amicra Microtechnologies GmbH Wernerwerkstr. 4 D-93049 Regensburg Germany Tel: +49- 941-208209 0 Fax: +49- 941-208209 9 www.amicra.com	Die Bonders, Flip Chip Bonders	Wafer Inking Systems , Multi Bin Laser Diode Test systems
ASM Pacific Technology Limited 12/F Watson Centre 16 Kung Yip Street Kwai Chung Hong Kong Telephone: 852 2619 2000 Fax: 852 2619 2118/9 www.asmpacific.com	Die Bonders, Flip Chip Bonders	Various others
BE Semiconductor Industries N.V. P.O. Box 90 6920 AB Duiven Ratio 6 6921 RW Duiven The Netherlands Telephone: +31 26 319 4500 Fax: +31 26 319 4550 www.besi.com	Die Bonders, Flip Chip Bonders (Datacon)	Meco (plating systems), Fico (molding / trimming), ESEC
Finetech GmbH & Co. KG Wolfener Straße 32/34, Haus L 12681 Berlin Germany Telephone: +49 30 93 66 81 303 Fax: +49 30 93 66 81 144 www.finetech.de	Die Bonders, Flip Chip Bonders (offline)	SMT/BGA rework, Laser bar-bonder, VCSEL, Photodiodes, Chip-on-glass, RFID
Geringer Halbleitertechnik GmbH & Co. KG Liebigstraße 1 93092 Barbing Germany Tel.: +49 9401 9110 50 Fax.: +49 9401 9110 51 www.geringer.de	Die Bonders, Flip Chip Bonders	Standard multi chip die bonders (single head and double head) for eutectic process and epoxy, incl. flip-chip, as well as lamination systems, remounters and test handlers and taping systems
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COMPANY HEADQUARTERS	BONDING TOOLS	WHAT ELSE THEY MAKE
Street Address City, State, Zip Country Telephone Fax Website		
Hybond Inc. 330 State Place Escondido, CA 92029 USA Telephone: 760-746-7105 Fax: 760-746-1408 www.hybond.com	Eutectic Die Bonders (offline/manual)	Wire bonders / Peg and bar lead diode bonders
MRSI Systems 101 Billerica Ave – Building #3 North Billerica, MA 01862 Telephone: 978.667.9449 Fax: 978.667.6109 www.mrsisystems.com 	Die Bonders, Flip Chip Bonders (TCB), Thermosonic Bonding	Eutectic Die Bonder, Epoxy Dispensers
Orion Systems Integration Pte Ltd 2 Woodlands Spectrum #03-10 Woodlands Sector 1 Singapore 738068 Telephone: +65 91845082 Fax: +65 68630832 www.orionsi.com	Flip Chip Bonders	
Palomar Technologies, Inc. 2728 Loker Ave. West Carlsbad, CA 92010 USA Telephone: 760-931-3600 Fax: 760-931-5191 www.palomartechologies.com	Die Bonders	Ball Bonders, stud bumpers, manual Die Bonders
Panasonic Factory Solutions Company of America 1701 Golf Road Suite 3-1200 Rolling Meadows, IL 60008 Tel: 847.637.9600 Fax: 847.637.9700 www.panasonicfa.com/content/microelectronics-equipment	Die Bonders	Wire Bonders, other
Protec Co. Ltd 43, Namdongseo-ro 330beon-gil, Namdong-gu, Incheon, Korea 405-846 Telephone: +82-32-822-9171 Fax: +82-32-8229188 protec21.co.kr/eng/index.php	Epoxy Die Bonder, Eutectic Die Bonder, Hybrid Die Bonder	Flip Chip attach, Lid attach system
Semiconductor Equipment Corp. 5154 Goldman Avenue Moorpark, California 93021 Telephone: 805.529.2293 Fax: 805.529.2193 www.semicorp.com	Flip Chip Bonder	Pick & Place Systems, Cleaning Systems for: FOUPS, SMIF Pods, Cassettes, FOSBS & EUV Pods
SET Corporation SA Smart Equipment Technology 131, impasse Barteudet 74490 Saint Jeoire France Telephone: +33 (0)450 35 83 92 Fax: +33 (0)450 35 88 01 www.set-sas.fr/en	Die Bonders, Flip Chip Bonders	Large device bonders and nano-imprint

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High-temperature electronics and applications

By David Shaddock, Liang Yin [GE Global Research]

High-temperature electronics is an emerging technology that has been enabled by the growing number of components available that operate reliably at higher temperature. High temperature is defined in this document as an operating temperature greater than 175°C. Research on high-temperature electronics has been ongoing for over 40 years, largely driven by oil and gas applications to drill deeper wells in search of new energy sources. However, until about the last 10 years, the selection of devices and components to make a useful circuit has been limited. Over the last 10 years, there has been an increase in offerings for semiconductors, capacitors, resistors, and other components that are enabling applications. Packaging suppliers addressing high-temperature applications have also emerged, but a standard packaging process for high temperature is lacking, largely due to a limited understanding of materials, structures, and processes needed to provide the application reliability requirements.

A quantitative accelerated reliability test (QALT) [1] method using physics of failure (PoF) models to define the reliability test is a useful method for determining lifetime at high temperature. The PoF models define the relevant application stresses (temperature, electrical, chemical, and mechanical) to apply during the test. Properties of electronics materials and component failure rates are typically not defined for temperatures above 125–150°C making modeling and reliability predictions difficult. If data is available, it takes the form of a qualification test at use temperature for short times as demonstration of operation, but seldom for more than 1000 to 2000 hours, and often without an electrical bias. Applying electrical stress is difficult because the electrical test connections must be as reliable as the device being tested. This situation is improving with more

understanding of fixtures and leveraging burn-in test equipment. The authors have reported on high-temperature fixtures for surface mount component and other device testing at high temperature with electrical biases.

Elevated temperature increases mechanical stresses because of coefficient of thermal expansion (CTE) mismatches, accelerates corrosion processes, and degrades electrical properties. Conductors become more resistive and insulators become more conductive. High-temperature environments also reduce mechanical strength, increase creep, or even cause material phase changes or decomposition in electronic materials. Additionally, dielectric leakage in semiconductor devices, capacitors and insulators increases with temperature. Mobility, mean-free-path, and saturation velocity in semiconductors decreases. The challenge in designing high-temperature electronics is to select materials and structures to minimize these failure modes, not unlike any electronics, but a change is necessary in selection of materials used for normal temperature electronics.

Applications

High-temperature electronics has applications anywhere there is a high-temperature environment or high power and there is limited capability to keep the electronics cool using thermal management techniques. This situation may arise because of limited space, availability of a heat sink, or weight limitations. An approach that has been used for electronics in high-temperature environments is to put the electronics in a vacuum dewar with phase change materials to delay the time the electronics reaches high temperature. This approach adds weight, and volume, and usable life time is limited.

The oil and gas industry has been the main driver for high-temperature electronics. The motivation is to drill deeper for reservoirs. The deeper a

well is drilled the hotter it gets with no cooling path. The oil and gas industry uses electronics to navigate a drill bit while monitoring the surroundings for temperature, pressure, flow and radiation to identify promising energy sources. Once the well is established, the well temperature, pressure, and flow are monitored. There continues to be a need for instrumentation to operate at 200°C for lifetimes of ~1000 hours for drilling and logging, while production applications are ~40,000 hours.

High-temperature electronics has been identified for applications in geothermal energy extraction where the temperature can exceed 300°C. Enhanced geothermal systems (EGS) have the potential to generate 100GW of energy in the United States over the next 50 years, emits no greenhouse gases, and provides a 24-hour a day base load source to the electrical grid [2]. EGS uses cracks in hot rocks in the earth to create channels for water injected from the surface to be circulated and heated for generation of steam to generate electricity. Instrumentation is needed to operate at 300°C or higher depending on the location. GE, under contract from the Department of Energy, fabricated a temperature-to-frequency converter that operates at 300°C using silicon carbide (SiC) devices and high-temperature packaging materials [3].

High-temperature electronics has application in aircraft engines. Temperatures in excess of 200°C in on-engine applications require lifetimes of tens of thousands of hours. The distributed control system in an aircraft engine would replace centralized control of sensors and actuators by the full authority digital engine control (FADEC) located on the fan with smart sensors and actuators in hot zones connected on a communication bus located throughout the engine [4]. Each system element individually connects to the network with real-time communication for control and monitoring.

Distributed control reduces the amount of computations the FADEC needs to do and helps reduce its cooling requirement. Fuel cooling is approaching limits as more heat is transferred into it and the added weight required to maintain unusable fuel tanks used for cooling it is prohibited. Uncooled electronics reduces the need for cooling and its associated weight. There is also improved fuel economy associated with weight saving on account of the reduced cabling needed to connect each element to the FADEC. The design enables the use of replaceable components across platforms and provides mitigation to obsolescence.

High-temperature electronics have applications in automotive engine controls, sensors, and hybrid power modules for electric vehicles. The motivation is higher power for electric vehicle drives and reducing or eliminating the weight and size of thermal management to improve efficiency. A focus area is using SiC power devices to replace silicon devices because of their inherently higher reliability, efficiency, frequency, and operating temperature to enable more compact systems with higher power density [5-6].

High-temperature electronics is needed for space exploration for Venus (482°C) and Jupiter (230°C) missions [7]. Venus and Earth are similar in size and density but have very different environments. NASA has interest in understanding how they followed different paths, how the greenhouse effect works, how geologically active the planet is, and if there were ever oceans or was habitable. Venus has a sulfuric acid atmosphere in the clouds and on the surface it is 462°C with 92 bar pressure. The longest surviving Venus mission is Venera 13 in 1987 that lasted 127 minutes. The electronics was in a pressure vessel with phase change material [8]. NASA and Ohio Aerospace Institute have recently demonstrated SiC junction field effect transistor (JFET) electronics and packaging operating at 500°C for over 10,000 hours [9].

Semiconductor devices

Semiconductor devices are the heart of electronics sensor and control products. High-temperature operation requires a change in the fabrication process and junction structure to reduce leakage. Increased temperature operation increases leakage current, decreases forward voltage drop on P-N junctions, increases gain on bipolar junction transistors, and decreases threshold voltage on MOS devices [10]. Semiconductor devices are limited in temperature by electromigration, corrosion, and increased diffusion. Leakage current increases in junctions caused by thermal generation of carriers that disrupts bipolarity. An illustration of this is shown in **Figure 1**. Semiconductor devices have lightly doped regions where the carrier concentrations are on the order of 10^{14} cm^{-3} to 10^{17} cm^{-3} . Intrinsic carrier concentrations above this would disrupt bipolarity.

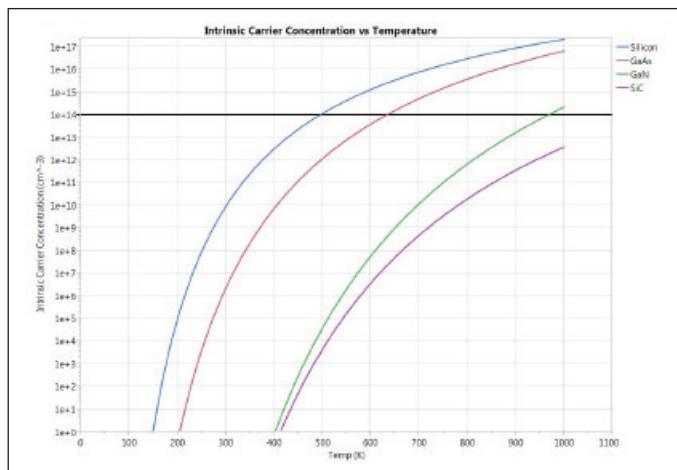
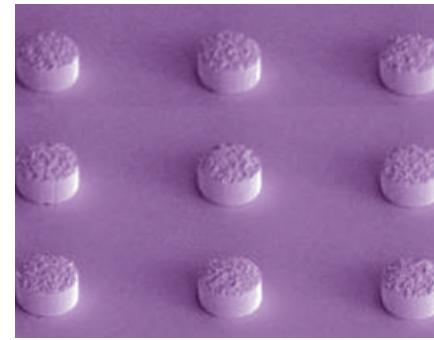


Figure 1: Intrinsic carrier concentration of semiconductor materials.

Silicon semiconductor devices are typically not specified for use over 125°C but can be used at higher temperature for shorter lifetimes. Screening has been used for silicon semiconductors for 175°C operation. Metal oxide semiconductor (MOS) devices are preferred over bipolar devices for high temperature because they are majority carrier devices. Improvement in high-temperature operation has been reported on low impurity silicon metal oxide semiconductor field-effect transistors (MOSFETs) with higher junction doping levels and decreased channel width-to-length aspect ratio. A zero temperature coefficient (ZTC) point exists where the drain current will not change with temperature. This can be used to reduce temperature sensitivity of a circuit. Another



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method to reduce leakage, that is not common, is dielectric isolation wherein the junctions are formed within SiO_2 wells to isolate them from the bulk silicon. Texas Instruments and Silicon Space Technology provides silicon devices up to 220°C through proprietary modifications to their processes to reduce leakage current.

Silicon device temperature is extended to beyond 250°C to 375°C by using silicon-on-insulator (SOI) technology [11]. Devices using this structure are commercially available and specified for 200–230°C [12]. SOI devices reduce leakage by forming the MOSFET on the top layer of the wafer over a SiO_2 layer to insulate the junction from the bulk silicon, which is more than 99.9% of the wafer and is the source of parasitic effects. The number of component types available is limited but growing. The cost of SOI devices is about 10 times that of silicon devices.

Wide band gap semiconductor devices provide very high-temperature capability because the wider band gap reduces the concentration of thermally induced carriers. However, this technology is less mature than SOI. SiC components are limited to diodes and transistors such as JFET and MOSFET. The reliability of a gate oxide in SiC is a challenge so structures such as JFETs have been used in demonstrations. However, JFETs are normally on devices and difficult to scale to more complicated circuits than a MOSFET. Silicon carbide (SiC) has made great strides because of reductions in crystal defects and improvements in oxide quality. SiC has an advantage in power devices because of its high breakdown voltage, lower switching losses, and high thermal conductivity as well as high-temperature capability. General Electric has SiC MOSFETs that are rated for 200°C junction temperature. General Electric leveraged its success in MOSFET fabrication to demonstrate the first high-temperature SiC operational amplifier and other analog and digital circuits operating at 300°C for the US Department of Energy.

Packaging

Packaging for high temperature requires a careful consideration of the material systems to ensure service life and reliability in its environment. **Figure 2** provides an illustration of issues with normal temperature electronics packaging used at high temperature. Plastic packaging fails at high

temperature because of thermal stress when operating above the glass transition temperature (T_g). Corrosion and loss of electrical insulation could occur because of the decomposition of brominated flame retardants above 200°C. Thermal strain increases and requires more closely matched thermal expansion coefficients and low modulus materials. The latter being a challenge because polymers increase modulus over time. Processing conditions can also affect reliability. The assembly technologies presented in literature include studies of the reliability of technologies that leverage existing infrastructure for manufacturing and sourcing materials. The studies find success and limitation of materials that provide a foundation to build upon to achieve long lifetimes. Many publications do not present reliability for any significant time period and are commonly reports of successful operation at high temperature.

Research on high-temperature packaging has largely been with ceramic multi-chip modules (MCM) and less on high-temperature printed circuit board (HTPCB) technologies. The temperature range has commonly been greater than 300°C, but some are in the 200-300°C range. Ceramic MCM assembly processes are compatible with surface mount assembly and have high potential for reliable life at high temperature because of the nature of the material and close

CTE match between semiconductors and ceramics. They are also more expensive. HTPCB assembly processes are compatible with mixed technology (through-hole and surface mount) assembly and high-volume infrastructure. Not all components are compatible with ceramic hybrids that require surface mounting components. Those who have applications, such as power conversion that need high-value capacitors, resistors or magnetics, find the components are only offered in through-hole packages with mechanically compliant leads.

Wire bonding to die with matching wire and pad metals has been shown to be reliable at high temperature by avoiding detrimental intermetallic formation such as Kirkendall voids. Gold wire bonded to gold pads has been shown to be reliable above 300°C. The gold anneals over time making it very pliable thereby causing shorting in vibration environments. Aluminum wire to aluminum pads has been shown to be reliable above 250°C. High lead solders are used in oil and gas applications such as HMP (Pb93.5Sn5Ag1.5) and Pb85 (Pb85Sb10Sn5). Studies of other solders using transient liquid phase (TLP) and sintered silver are in progress to assess their reliability. An off-eutectic AuSn solder has demonstrated reliability above 300°C in high-temperature storage and thermal cycling. This method uses diffusion of gold surfaces to raise the melting point of AuSn eutectic solder above 500°C.

Why current packaging won't work

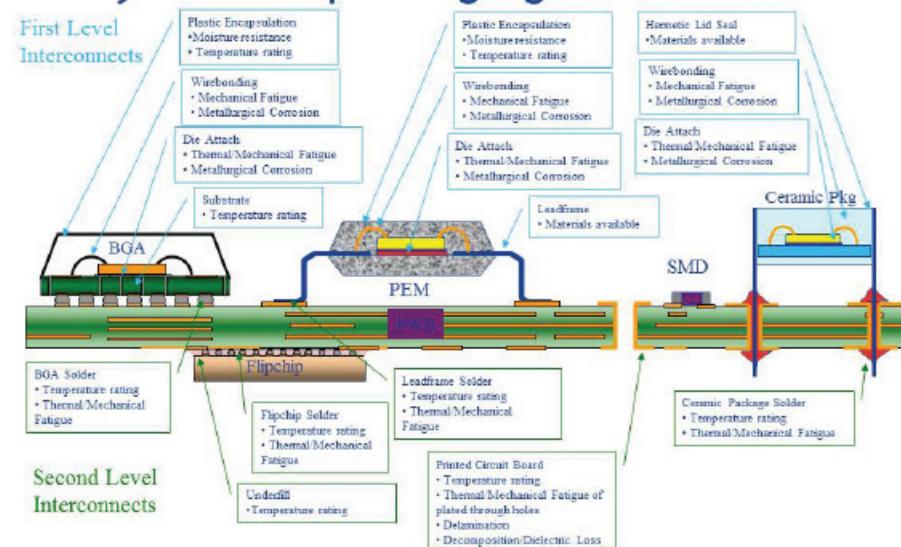


Figure 2: Why current packaging won't work.

Ceramic substrates are the choice for temperatures above 250°C because of the high-temperature nature of the materials. Although ceramic substrates are fabricated from high-temperature materials and processes, reliability at high temperature is not a given. Ceramic substrates use alumina for thick-film hybrids with gold or silver conductors, low-temperature co-fired ceramic (LTCC) with gold or silver conductors, and high-temperature co-fired ceramic (HTCC) with tungsten conductors. Selection of the thick film is important. Studies have found that some thick films may lose adhesion after high-temperature aging; additionally, the dielectric may contain contaminants such as sodium that cause reduction in insulation resistance and adhesion [13]. LTCC and HTCC provide multilayers needed for high routing density. LTCC has a lower CTE than alumina to better match silicon and SiC [14] and provides reliable high-density circuitry. Aluminum nitride substrates have a better CTE match, but thick films exhibit poor conductor adhesion. Thin-film AlN substrates were demonstrated with stable adhesion at 310°C but the process is much more complex.

HTPCB laminates will degrade at high temperature because of decomposition, peel strength loss, insulation resistance degradation, and via failure in thermal cycling. An illustration of decomposition is shown in **Figure 3**; it shows three polyimide (P1, P2, P3) and one hydrocarbon ceramic (NP1) laminate after aging at 200°C for 1000 hours. The polyimide laminates decompose to the point where the laminate reduces to glass weave and conductors with little dielectric remaining. The hydrocarbon ceramic has a higher temperature rating and was reduced to a similar condition after 6000 hours but failed in surface insulation resistance testing because of its brominated flame retardant. The performance of laminates with longer lifetimes is presented by the authors [15].

Summary

High-temperature electronics will become more main stream because application needs already exist. This technology will require the industry to extend the testing range of materials beyond current specifications, reduce cost, and extend reliability models to higher temperature. There is active research in identifying reliable packaging materials (substrates, solders, interconnects) and devices (SOI, SiC, GaN) to support the growth of this technology area and devise cost-effective solutions. It is expected that there will be more high-temperature electronics products on the market with the first commercial applications in the energy exploration industry.

After 1000 hours Isothermal Aging

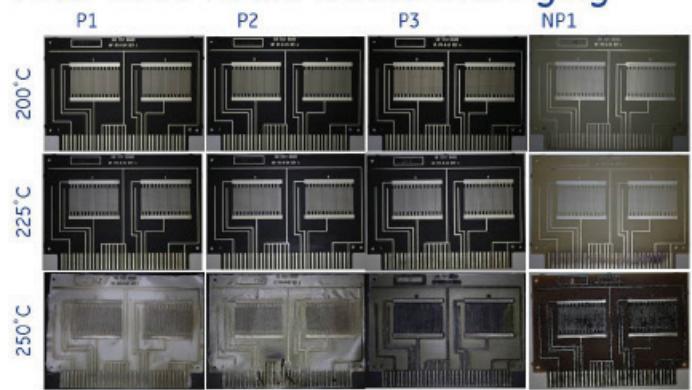
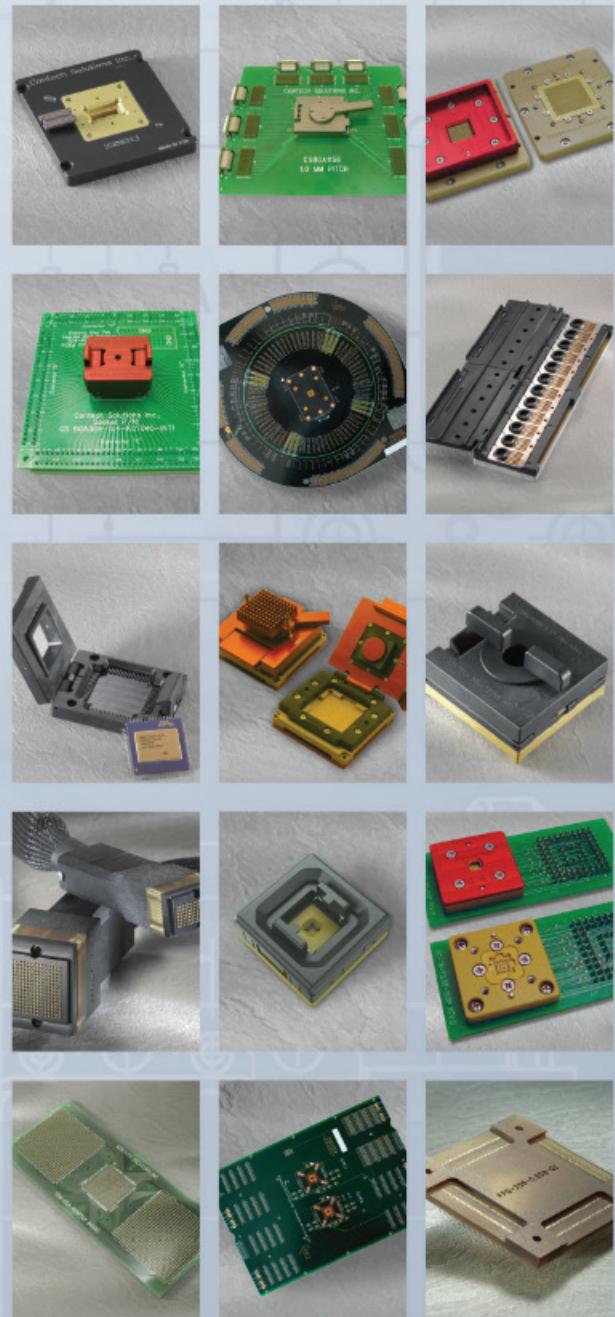


Figure 3: High-temperature laminates after 1000h at 200°C aging in air.

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Biography

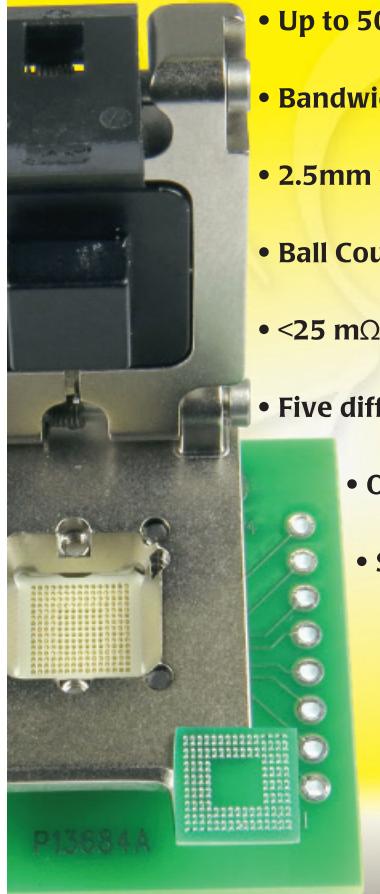
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Optical inspection technologies for 3D packaging

By Arun A. Aiyer, Tianheng Wang, Helen Simson [Frontier Semiconductor, Inc. (FSM)]

In the realm of 2.5D/3D packaging, a high-throughput/production-ready metrology tool with a single high-performance sensor that addresses multiple measurement needs throughout the process flow, i.e., from front-end-of-line (FEOL) to back-end-of-line (BEOL), can be very valuable in terms of yield improvement, cost-of-ownership reduction, and tool utilization. FEOL metrology related to through-silicon via (TSV) creation and BEOL metrology related to remaining Si thickness (RST) and Cu reveal are addressed by our Virtual Interface Technology (VIT). Substrate thicknesses ranging from a few microns to several millimeters, TSV depth and profile, RST and Cu nail height, can be measured by a single sensor. This technology provides tool-to-tool compatibility at different measurement points along a die stacking process line.

All commercially viable packaging that uses chip stacking and/or die stacking requires that conductors such as Cu nail, or Cu pillar, or solder bumps, be placed on the chip or die I/Os to act as the interconnection. Measuring co-planarity of these μ Features is important in enhancing device yield. Miniaturization in 3D packaging along with demand for higher density I/Os are challenging inspection and metrology approaches to higher measurement capability and throughput. Therefore, a high-throughput, production-ready metrology tool with a high-performance sensor that can measure C4 bumps to Cu reveal height and capable of 100% height inspection, will be very valuable in terms of yield improvement.

Measurement of surface topography in MEMS wafers and measurement of z-dimension of high-aspect ratio features in semiconductor wafers can be accomplished with scanning white light interferometry (SWLI). Additionally, it is quite effective in measuring surface roughness of optically smooth surfaces with a resolution \sim 1nm or better. Other applications include measuring machined surfaces, micro-fluidic devices, optics and fibers, ceramics, glass, paper, thin films, and polymers.

Measuring with VIT

VIT is a Fourier domain technique that utilizes temporal phase shear of the measurement beam for thickness measurement

of thick substrates. The unique sensor configuration enables creation of non-physical interfaces that enhance a tool's measurement capabilities in terms of measurement range, accuracy and repeatability. One example of how this technology is used in thick substrate measurement is demonstrated with the help of **Figures 1-5**. The sample can be illuminated from either side.

In non-VIT mode, spectral fringe frequency increases with sample thickness. For thicker substrates, fringe crowding similar to that seen in **Figure 2** occurs. Measurement in VIT mode, however, leads to low-frequency fringes for the same sample (**Figure 4**). Preventing fringe crowding enables better fringe sampling, which in turn avoids aliasing error, thereby improving measurement accuracy and repeatability. The latter two are the result of improved signal/noise ratio (S/N) in the fast Fourier transform (FFT) spectrum as can be seen from the signal amplitudes in **Figures 3 and 5**.

Sample under 1.3μ illumination

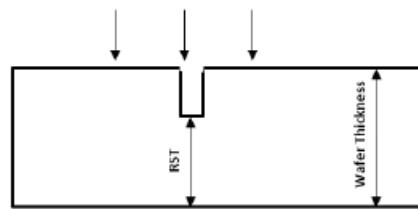


Figure 1: Schematic of a TSV sample under illumination.

When VIT is enabled, signal pairs are used in determining wafer thickness and thickness under the TSV or RST. Referring to **Figure 5**, wafer thickness is obtained by adding optical path difference (OPD) corresponding to peaks B and D, and the RST is determined by adding OPDs at peaks A and D. These peaks are 5x or more stronger than amplitudes of the signals (seen inside the red box in **Figure 5**) obtained without VIT. Stronger signals improve measurement accuracy and repeatability. Thickness and RST mapping of a 300mm

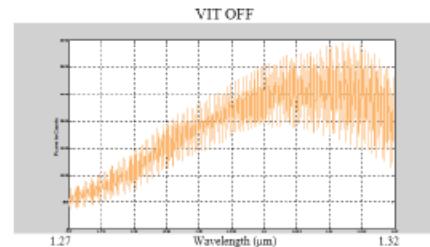


Figure 2: Wavelength spectrum corresponding to a sample shown in **Figure 1**

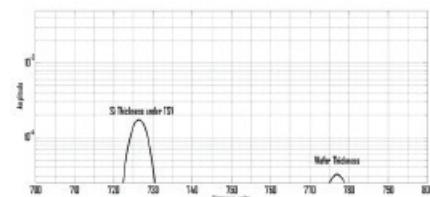


Figure 3: Thickness spectrum corresponding to the wavelength spectrum.

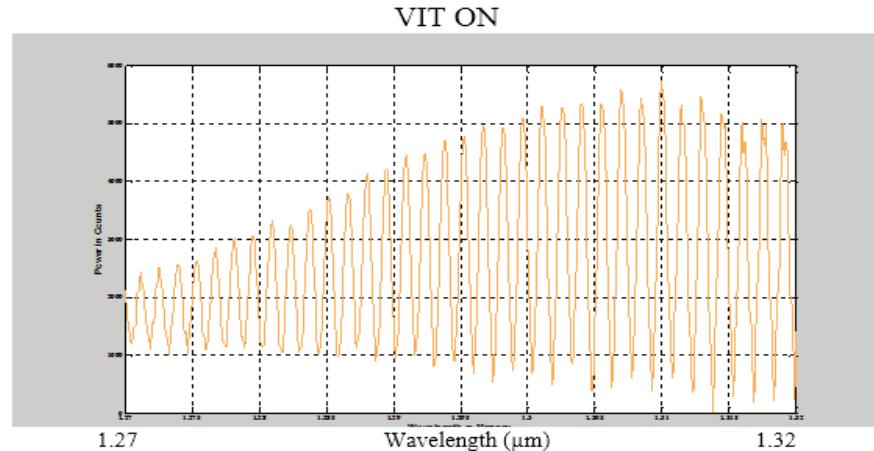


Figure 4: Wavelength spectrum corresponding to a sample shown in **Figure 1** with VIT mode turned "on."

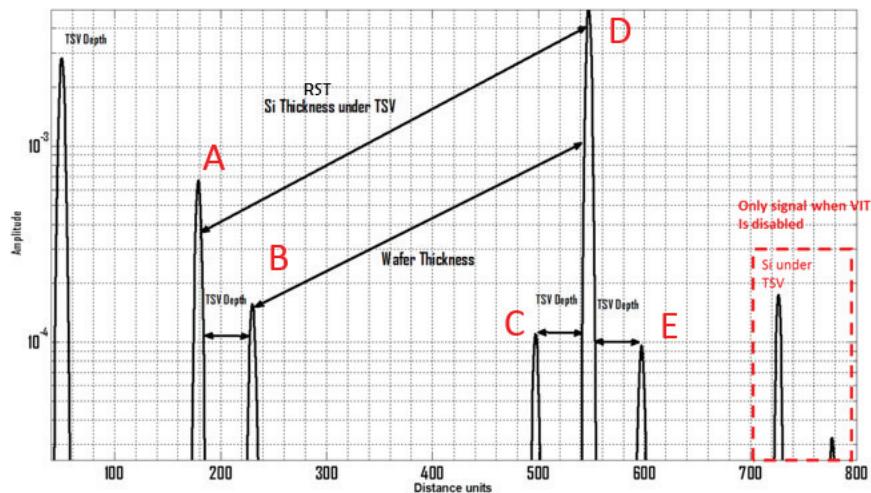


Figure 5: Thickness spectrum with VIT that facilitates simultaneous measurement of thickness, depth, and via profile.

wafer is shown in **Figures 6 and 7**. The 1σ standard deviation achieved by this technique is approximately in the nanometer range and is 5x to 10x better than what is achieved in non-VIT mode. In **Figures 6 and 7**, wafer thickness and RST measured in a 300mm wafer are mapped out. Such maps are useful in visualizing process variations that may exist across the processed substrate.

The parameters to be measured are depth, top CD (TCD), bottom CD (BCD), and side wall angle (SWA).

Depth. The VIT-enabled thickness spectrum is displayed in **Figure 5**. This signal signature is typical from a sample like that shown in **Figure 1**. Peaks A, B, C, D and E appear only when VIT is enabled. It is important to note that the separation between peaks A/B, C/D, and D/E is the same as the TSV depth value, which is independently given by the first peak in the spectrum. VIT, therefore, has

a self-checking mechanism built into it when measuring via depth. Via depth obtained from a TSV sample with dimensions $\sim 12\mu\text{m} \times 70\mu\text{m}$ has been mapped out in **Figure 8**. These measurements were made with repeatability and reproducibility on the order of nanometers.

TSV bottom CD. Peak D in **Figure 5** results from virtual interfaces, while peaks C and E are from the coherent interaction of virtual interface with the interface defined by via bottom. Knowing the areas under these peaks, “optical” bottom CD (BCD) is calculated using the expression:

$$\text{BCD} \propto 2 * A_D^{1/2} x (\text{PSD}_C / \text{PSD}_D)^{1/4}$$

Where A_D is an area proportional to the measurement beam spot, and PSD_C and PSD_D , respectively, are the areas under peak C and peak D. Therefore, this is not a model-based approach.

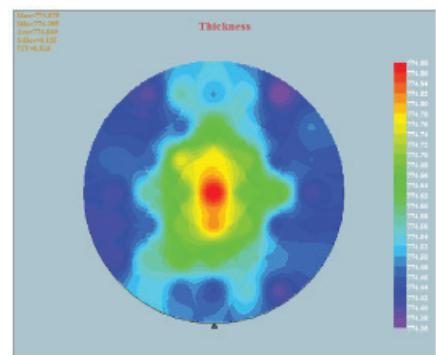


Figure 6: Thickness map of a 300mm wafer ($\text{TTV}=0.515\mu\text{m}$).

We used the above approach to measure BCDs of a $5 \times 50\mu\text{m}$ via farm. The result of 49-point measurement is shown in the chart in **Figure 9**. **Figure 10** shows the TCD of some of the vias in the farm, and **Figure 11** gives the infrared (IR) image of the bottom of a few of these vias. The average BCD calculated in VIT mode is $4.47\mu\text{m}$, and that estimated from the NIR image is $4.38\mu\text{m}$. Knowing top and bottom CDs, the sidewall angle (SWA) can be determined. VIT can be engineered to measure TSV parameters either from the wafer front side and/or back side. Therefore, a bottom probe may be used for profile measurement even if the via is filled.

Measuring with 3DI

3DI is an imaging technique that captures phase shift introduced by μ Features such as μ Bumps, C4 bumps, Cu pillars, redistribution layer (RDL) bumps, etc., in the measurement beam. Use of a source-sensor configuration enables creation of a phase map of the features, from which their height information can be deduced. Additionally, this technique allows all features in the field of view to

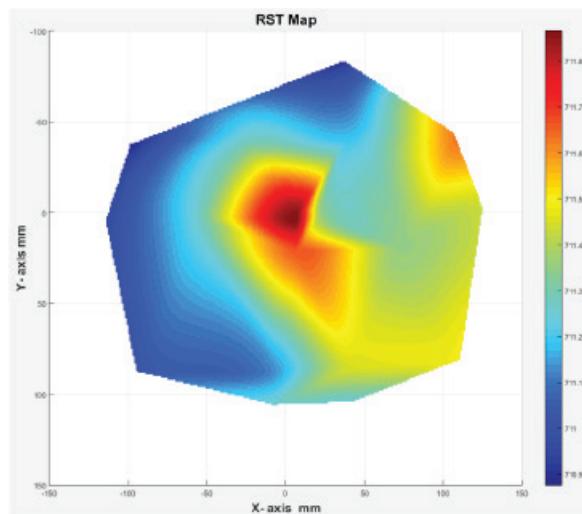


Figure 7: RST map from a 300mm wafer. (Avg. RST=711.28 μm , TTV ~1.0).

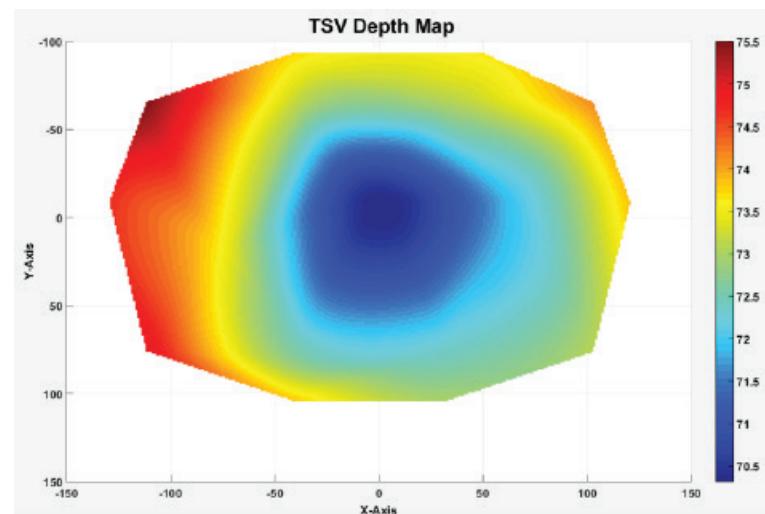


Figure 8: TSV depth map across a 300mm wafer.



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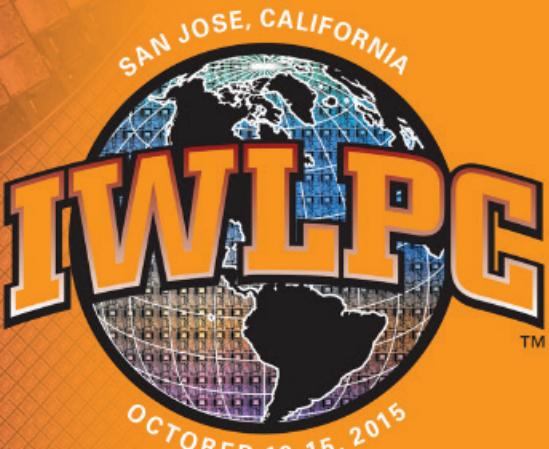
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EVENT SCHEDULE

Tuesday, October 13 – Wednesday, October 14

Exhibition, Panel Discussion and Technical Presentations on 3D, WLP and MEMS

Thursday, October 15

Professional Tutorials

T1: Introduction to Fan-Out Wafer-Level Packaging

T2: 3D IC Integration and 3D IC Packaging

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Tuesday, October 13



Keynote Breakfast Address
High Density Fan-Out: Evolution or Revolution

Rama Alapati, *GLOBALFOUNDRIES*



Panel Discussion
Fan-Out WLP Panel Processing: Will it happen and What will it be?
Moderator: Jan Vardaman, *TechSearch International*

Exhibitor Reception

Join us in the Bayshore Ballroom for the Exhibitor Reception where over 60 exhibitors will showcase the latest products and technologies offered by leading companies in the semiconductor packaging industry. This evening reception offers attendees numerous opportunities for networking and discussion with colleagues.

Wednesday, October 14



Keynote Address
2.5D/3D IC – Examining Low Cost Alternatives

Sitaram Arkalgud, Ph.D., *Invensas Corporation*



Panel Discussion
Interposers, 3D TSVs and Alternatives: What are the Options and Where do They Fit?

Moderator: Françoise von Trapp, *3DInCites*

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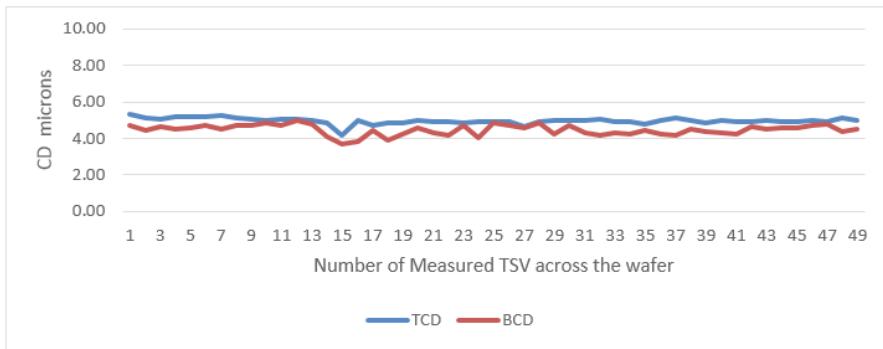
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	TCD μm	BCD μm	SWA deg.
Av	5.09	4.47	89.72

Figure 9: Top and bottom CDs of 5x50 μm TSVs in a 300mm wafer. TCD measurement via imaging and BCD measurement via VIT mode.

be measured simultaneously, thus enabling massively parallel measurement of all individual features imaged by the sensor.

Figure 12 shows, in schematic format, some of the features that are measured. **Figure 13** compares the three different tools based on three different technologies that we offer for 3D inspection of these μ Features. Of the three, the 3D inspector offers the shortest measurement time, which enables 100% inspection of every wafer at an industry-acceptable throughput rate. **Figure 14** gives an example of 3DI's ability to measure Cu nails after Cu reveal, while in **Figure 15**, its capability to do both 3DI and 2DI is shown.

Scanning white light interferometer

Scanning white light interferometry (SWLI) is a versatile interference microscopy technology that provides a non-contact, 3-D method of measuring surface topography and roughness. Illumination from a white light beam passes through a microscope objective lens to the sample surface. The objective lens is coupled with a beam splitter so some of the light is reflected from a reference mirror. The light reflecting back from the surface recombines with the reference beam. The recombined beams create bright and dark bands called fringes, which make up the interferogram. Fringes represent the object's topography. By scanning the object or the objective in the z-direction, several interferograms are captured by the CCD camera, which are analyzed to recreate the sample surface.

In **Figure 17**, topography of a feature in a product wafer as measured by FSM's SWLI is shown. This low aspect ratio feature is 25 μm in diameter and 5 μm deep. The various parameters that characterize roughness of a Si wafer, obtained by employing phase shifting feature in WLI, are given in **Table 1**. These numbers pertain to a scan line that spans

across the FoV of the instrument. Profile along this scan line is given in **Figure 18**.

SWLI is used for measuring height of flat μ Bumps similar to those shown in **Figure 19**. Height measured by white light correlates well to those measured with 3DI and VIT. This can be seen in the chart in **Figure 20**. The corresponding data is given in **Table 2**.

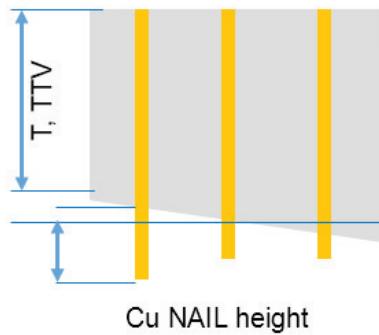


Figure 12: Array of μ Features to be measured.

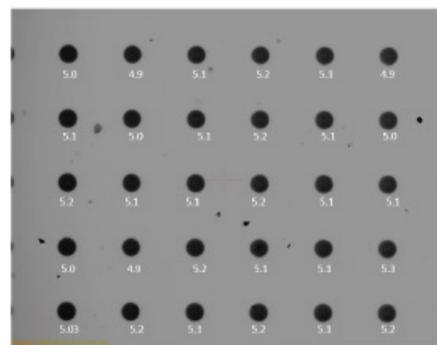


Figure 10: Top CDs from a 5x50 μm TSV farm.

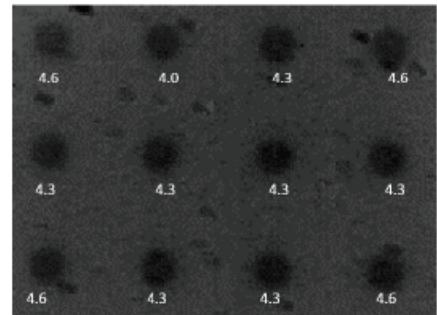
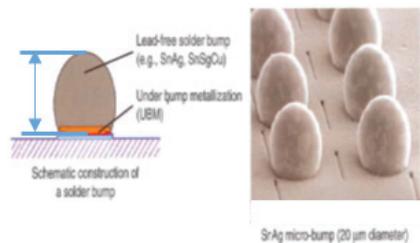


Figure 11: NIR image of 5x50 μm TSV bottom.
(Resolution: 0.3 $\mu\text{m}/\text{pixel}.$)



Bump height

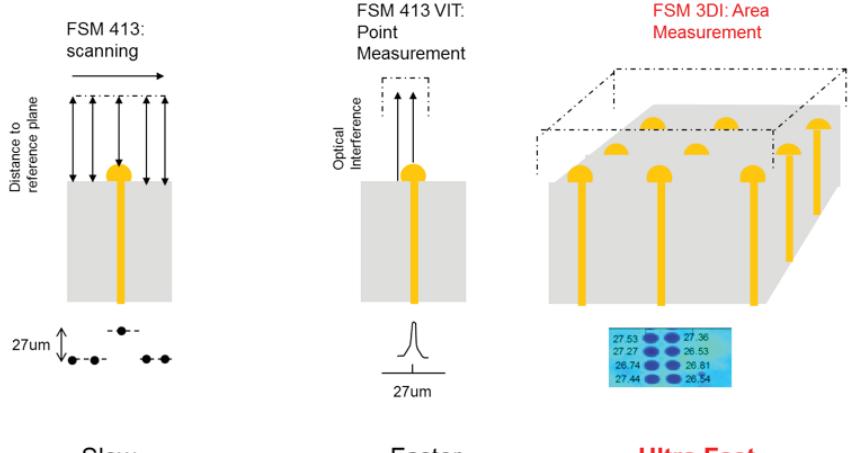


Figure 13: Schematic representation of three different techniques available for measuring μ Features used in 3D packaging.

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9/3 (Thu) Exposition: 10:00-17:00

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| 08:30 – 17:00 | eMDC Forum |
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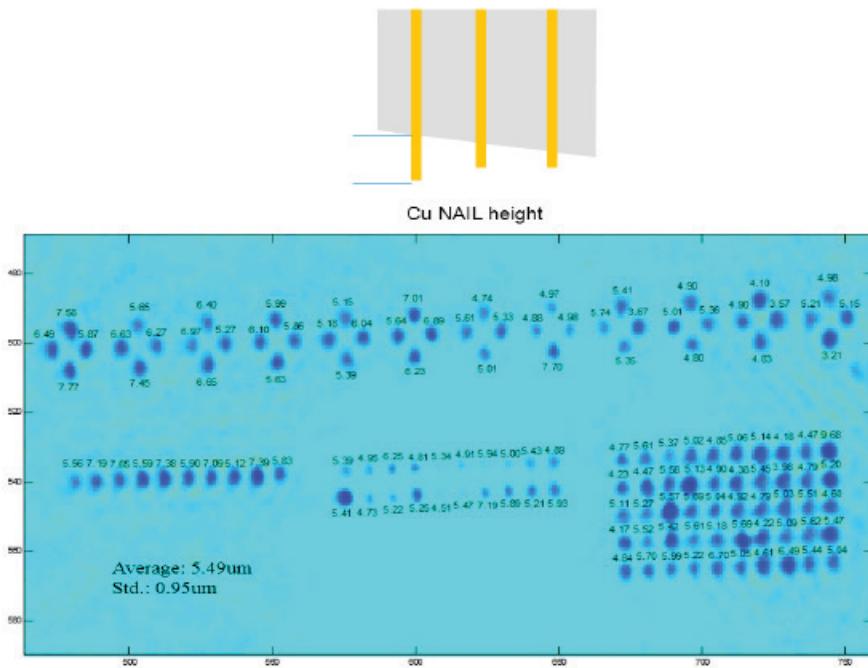


Figure 14: An example of massively parallel 3DI of Cu nails after Cu reveal.

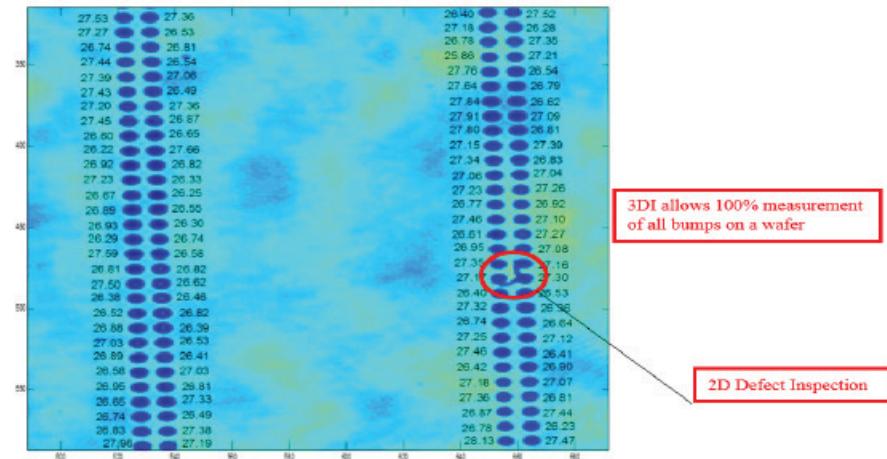


Figure 15: An example of massively parallel 3DI and 2D inspection of μBumps.

Summary

The tool based on VIT has a depth/thickness measurement range spanning a few microns to a few millimeters. This makes the tool capable of monitoring several FEOL and BEOL processes in 3D packaging applications. These include TSV depth and profile measurements, bonded wafer stacks measurement, RST and thinned Si wafer measurements, after-reveal Cu nail co-planarity measurement, and C4 bumps, μBumps and Cu pillar height measurements. In Si, the measurement range spans from 4µm to 5mm. This new tool provides tool-to-tool compatibility at different measurement points along a die stacking process line. Measurement

repeatability shows that the tool is robust and is ideal for production environment. These factors in turn minimize cost incurred in Operations & Service training and lessens spare parts inventory. Consequently, tool downtime is reduced leading to better cost-of-ownership. The tool based on 3DI technology allows for 100% 3D inspection of Cu nails, C4 bumps, μBumps and Cu pillars at a throughput acceptable to industry.

FSM's microscope-based white light optical profiler is used in applications such as surface topography measurement, surface roughness measurement, step-height measurement, and more. High spatial resolution and z-resolution achieved

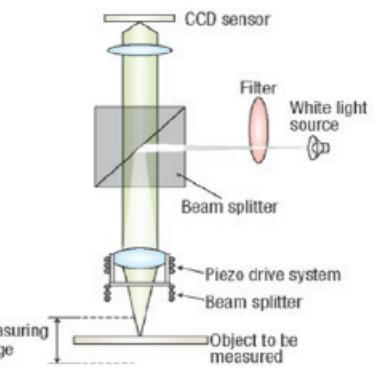


Figure 16: Vertical scanning white light interferometer.

Ra	0.0021 µm
Rq	0.0026 µm
Rv	-0.0065 µm
Rp	0.0091 µm
Rt	0.0155 µm

Table 1: Various parameters that characterize the roughness of a Si wafer, obtained using the phase shifting feature in WLI.

Definitions: Ra=average roughness; Rq=RMS roughness; Rv=max valley depth; Rp=max peak height; Rt=max height of the profile.

Bumps	3DI	WLI	VIT
1	11.88	11.6	11.73
2	11.64	11.05	10.63
3	11.6	11.21	12.01
4	11.36	11.21	11.81
5	11.19	11.13	10.88
Average	11.534	11.240	11.412
Range	0.690	0.550	1.380
St.Dev	0.266	0.212	0.615

Table 2: Data in this table corresponds to the measurements shown in Figure 20.

with WLI is well-suited for roughness measurement of smoother surfaces.

Acknowledgements

The authors would like to acknowledge the support given by Ann Koo during the development of these tools and Nikos Jaeger for providing some of the schematics used in the article.

Biographies

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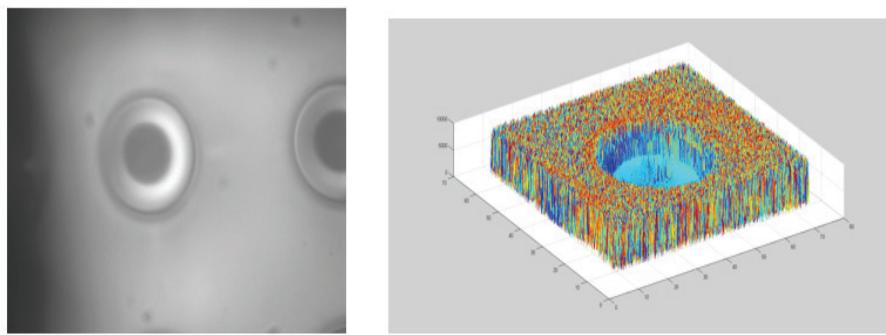


Figure 17: Surface topography measurement using a scanning white light interferometer.

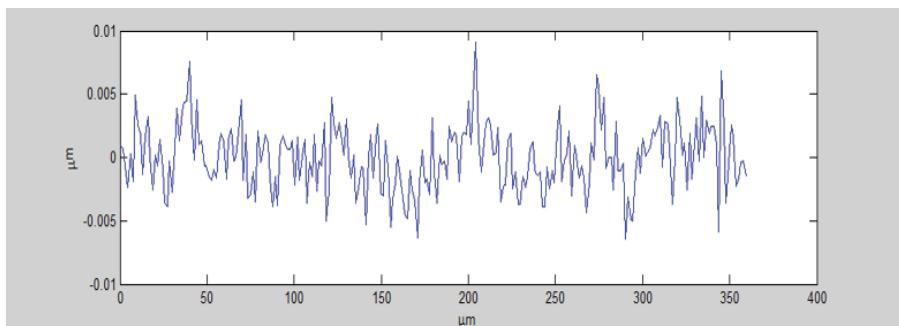


Figure 18: Surface roughness of a polished Si wafer measured by the WLI.

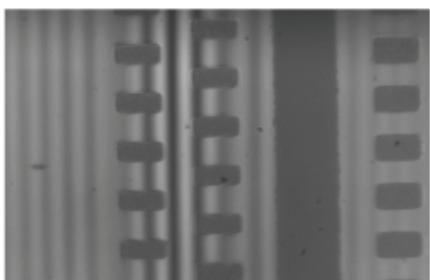


Figure 19: White light interferogram taken during a flat µBump (rectangular features in the figure) height measurement.

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Helen Simson received her PhD in Applied Optics (Physics) from the Indian Institute of Technology (IIT) Madras, India and is an Optical Engineer at Frontier Semiconductor.

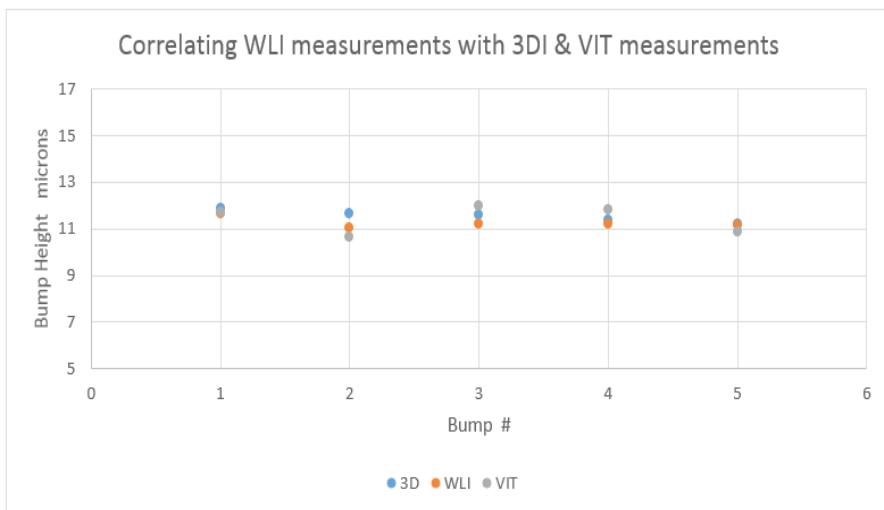


Figure 20: Measuring µBumps using WLI. The data correlates to 3DI and VIT measurements.

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The business of wafer-level packaging polymers

By Chris Blatt, Lita Shon-Roy [Techcet Group, LLC]

Wafer-level packaging (WLP) is one of the fastest growing segments of the semiconductor materials industry, driven by mobile applications with the ever-increasing need for more performance in a smaller package. Although mainstream WLP is often considered mature by many, over the last few years, many of the suppliers and OEMs primarily focused on front end processes, have started to make significant investments in the packaging market segment, i.e., equipment and materials.

Throughout the years, the chip fabs have been pushing for lower costs while enhancing performance. Typically, this has resulted in roughly a 30% reduction in cost for each technology node as they chased Moore's Law. The chip fabs continue to be focused on minimizing costs, however, much of the inefficiencies originally associated with front end processes have been removed over the past two decades. Now, cost reductions are much more difficult to achieve, especially in light of new materials that are being introduced for sub-22nm nodes. Therefore, the percentage of the total cost that packaging now represents is significant and needs to be addressed in order to continue with the desired cost targets. As a result, packaging is being looked at for further improvements in efficiencies and cost reduction. The target is achieving more benefits from increasing connections per square inch while reducing cost per I/O. Packaging is viewed as the "last frontier" for cost savings.

The various WLP schemes include flip-chip wafer bumping, fan-in wafer-level chip-scale packaging (WLCSP), fan-out WLP, 2.5D interposer packaging, 3DIC/TSV (through-hole silicon via) and integrated passive devices. Of all these technologies, the 2.5D and 3D schemes tend to be more complicated and expensive to put into practice. In particular, 3DIC/TSV is by far the more elaborate and expensive, and has not gained much traction in the marketplace. At present, the flip-chip packaging scheme is by far the most popular among the group, but limited in I/O due to its dependency on an interposer. By minimizing the dependency on an interposer, and instead using a polymer passivation layer,

process steps are removed, thereby simplifying manufacturing and reducing the overall cost, i.e., fan-in WLCSP. Going one step further, multiple layers of polymer can be used to "fan-out" the interconnections between the chip and the outside world. The end result is a significant increase in I/O. Flip-chip wafer-bumping and Fan-in and Fan-out WLP packaging schemes are shown in **Figure 1**.

The main driver for fan-out WLP is lower cost I/O. In **Figure 1**, polymers surround the chip and reside between all active interconnections. Flip-chip packaging has been used for decades and is now common place. This technology enabled the use of chip-on-board technology allowing multiple chips to be housed in a single package. The limitation to this design is that the connections through the interposer must be vertical, which tends to limit the ability to spread out the connections from the chip to the outside world without using multiple layers of interposers. In addition, the processing required to make the connections through the interposer requires etching or laser drilling through-holes — a notoriously slow processes.

WLP fan-in and fan-out schemes allow for lower cost per square inch by minimizing the need for the interposer AND enabling the use of more I/O per square centimeter. Both the fan-in and fan-out technologies use passivating polymer below the chip to enable connections to the board. Only the fan-out WLP uses multiple layers of polymer to spread out the connections, as shown in **Figure 1**. This lessens the need to go 2.5 or 3D, which would require the use of multiple interposers to spread out connections, and simplifies the processing, lowering the overall process cost.

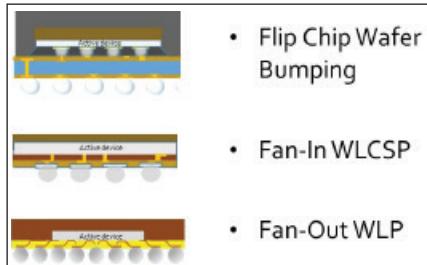


Figure 1: The three most popular WLP packaging methods.

WLP fan-out: enabling a cost-effective solution

So, "Why doesn't everyone use fan-out technology today (**Figure 2**)?" The answer lies in the material properties of the polymers currently on the market. Fan-out technology involves photo-activated polymer materials that are used as passivating layers in between metal interconnects. The process is similar to traditional print and exposure methods combined with metal sputtered deposition. The curing temperature of the polymers needs to be well below the melting point of the epoxy molding compound, ideally <200°C, to prevent reliability problems.

By using multiple polymer passivating layers, the pads on chips can be connected in a fan-out fashion such that the I/O count can be easily increased by 25% or more. The cost per I/O can be greatly reduced given the higher density of solder ball connections that can be made per square centimeter of packaging area.

In the WLP fan-out scheme, the epoxy used in the epoxy molding compound (EMC), traditionally used for supporting the chip is unstable at temperatures above 220°C, i.e., $T_{melt} = 220\text{-}250^\circ\text{C}$. Unfortunately, the curing temperature of most polyimides desired for passivation are well above 300°C. This mismatch has stimulated a wave of development in working toward lowering the overall curing temperature of passivating polymers in hopes of finding one that will be process-compatible.

In general, polyimides have many ideal properties including good coefficient of thermal expansion (CTE), minimal shrink, and high elongation for wafer-level packaging application. As a result, much of the development work is being focused on lowering the overall curing temperatures while trying to maintain and improve upon the other important properties of polyimide or other industry standard polymers (**Table 1**).

Companies such as Dow Chemical, JSR, HD Microsystems, TOK, and Sumitomo are all hoping to gain market share by introducing the winning polymer for WLP fan-out applications. The main motivation

Low-temperature curing	<200°C
High elongation	50-70%
Low cost	\$1/gram
Inherent low D _f material	<0.005
Low water absorption (reliability of the final device)	<0.1%

Table 1: Ideal polymer properties for WLP fan-out.

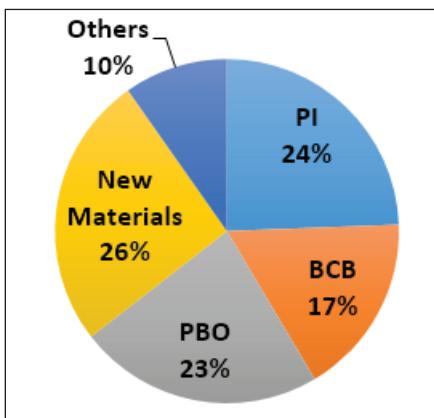


Figure 2: WLP polymer materials market 2020: ~\$300M.

The variety of polymers within each classification (polyimides, PBOs, BCOs, epoxies, resins, and siloxanes) is enormous. While many of these materials offer low-temperature versions, <250°C, the tradeoffs for lower temperature are not usually tolerated, i.e., stress cracking, material adhesion issues, excessive water absorption, CTE mismatch, loss factor, change in material properties due to environmental factors like heat and humidity, etc. In addition, other process considerations have to be taken into account. For example, using tetramethyl ammonium hydroxide (TMAH) as the developer is a desired method over other more expensive solutions; and the polymer materials need to be “ready to use” and not require the customer to mix or add activators.

The only certainties about the future of packaging is that packages will be expected to have more I/O per square centimeter at a lower average price per I/O than today. In order to accomplish these goals, new materials, or modifications to existing polyimides, PBOs and BCOs will be needed. The materials market for WLP polymers is expected to grow 15% to 20% annually over the next several years, generating a market for new materials that may total more than \$80M by 2020.

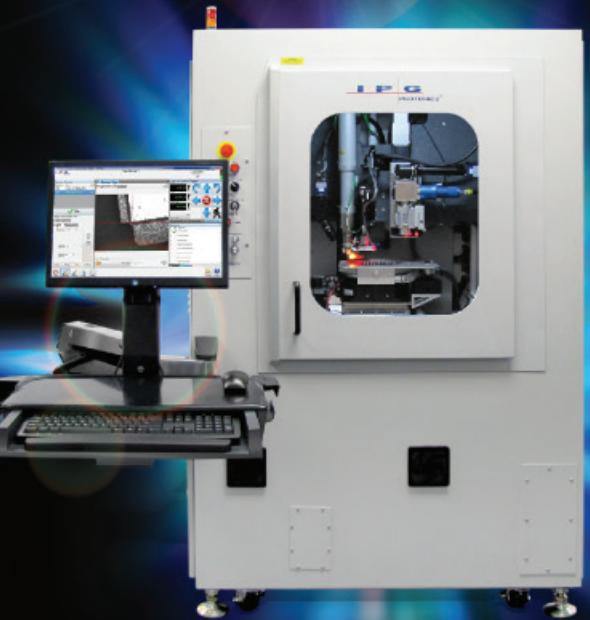
Biographies

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for these companies is the promise of a fast growing market expected to more than double in the next 5 years: ~\$120M in 2015 to ~\$300M by 2020 (Figure 2). This represents polymer and epoxies for all WLP areas, of which new materials is estimated to be approximately 26% of total revenues. At present, polyimide has the majority of the market, but has lost some ground to polybenzoxazole (PBO) and benzocyclobutene (BCO). These polymer classes offer slightly lower curing temperatures, but are more expensive.

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Nordson ASYMTEK launches a programmable tilt + rotate dispenser

By Debra Vogler, Sr. Technical Editor

Nordson ASYMTEK recently announced a new Programmable Tilt + Rotate 5-Axis Fluid Dispenser that enables a jet to dispense using 5 axes of automated control instead of only 3 axes. The company noted that additional X and Y tilt modes enable dispensing from a vertical position and at varying tilt angles along all four sides of a device, and up the side of a substrate or component. This capability is particularly important for 3D packaging applications.

According to the company, for 3D IC applications, applying fluid for capillary underfill of stacked die using conventional vertical dispensing necessitates building up fluid to reach the top of the stack. If there are variations in the height of the stack, the defined fluid volume might end up short of the top layer or overflow the top. The programmable tilt + rotate feature enables the user to determine the height of the die stack's top layer and then dispense fluid along all four sides of the stack just below the top surface. The company also said that dispensing from the top down can further reduce the amount of excess fluid required with conventional vertical dispensing, thereby reducing the total wet-out distance around the die stack. "When stacking fluid from the bottom up, you need to add additional fluid to get the height profile," said Garrett Wong, Product Manager at Nordson ASYMTEK. "As such, fluid tends to flow out and underfill in the lower levels of the stack, as well as to the "tongue" away from the die stack (shown in the left image of **Figure 1**). As this fluid flows out while dispensing, it reduces the overall height of the fluid stack, and therefore can result in more fluid being required to create the target fluid height to reach and flow out to the top of the stack." Wong also told *Chip Scale Review* that, by dispensing to the side of the stack at the target dispense height, the user does not need to stack up as much fluid to reach the top of the die stack and get sufficient underfill to that layer (refer to the image on the right in **Figure 1**). The company noted that using the tilt mode, the jet dispenses up to $\pm 30^\circ$ with 1° resolution in either the X or Y axis.

According to Wong, wet dispense accuracy is calibrated at the different tilt angles and dispense gap heights, thereby calibrating out the error/inconsistency at the various positions. "Calibrations are performed in all four directions, as well as in the vertical orientations," Wong told *CSR* (see **Figure 2**). "Up to 10 sets of calibrations can be stored and used with each process program, allowing for multiple dispense gaps and tilt angles to be automatically actuated through for different parts and geometries on a single substrate."

CSR asked Wong to discuss the technical challenges that had to be addressed to develop solutions to ensure dispensing accuracy. He noted three significant challenges. The first was maintaining

the target dispense area for 300mm wafers when factoring in spatial constraints of the platform and motion system. "This was resolved through minimizing the structural design of the system and using the rotational arm to pivot our jet valve to achieve the tilt dispensing in the two axes, as well as intelligently positioning the mounting of the system components to avoid interferences and moving the syringe from a direct mount on the valve to a remote mount in front of the camera," explained Wong.

The second challenge that had to be addressed was achieving the required dispense accuracy and understanding the sources of error. "We resolved this challenge by reducing the mass of the bracket solution to minimize inertia, as well as implementing software controls and calibrations to remove the sources of wet dispense accuracy errors," said Wong. "Building the system to work with the DispenseJet® DJ-9500 gave us a solid base for achieving target accuracy and precision."

The last major technical challenge the company tackled was using software automation of the tilt and rotate functions to achieve target cycle times, as well as to ensure safe operation for avoiding damage to the dispenser or substrate parts. Additionally, because of the moving components that are a part of the system, it was also vital to ensure safe operation for the user. The company resolved these issues in the design of both the tilt and rotate mechanisms to allow for maximizing rotational velocities. "Additional controls in the software and hardware limit the system from achieving velocities that could then injure an operator in the event that a user bypasses the door safety system and inserts a hand into the system while it is running," Wong told *CSR*. "Commanding the tilt and rotate functions to only actuate at the safe Z height further ensures that the system will avoid damage to either the substrate parts or the dispenser."



Figure 1: Illustration of underfill flow-out for a 3D die stack.

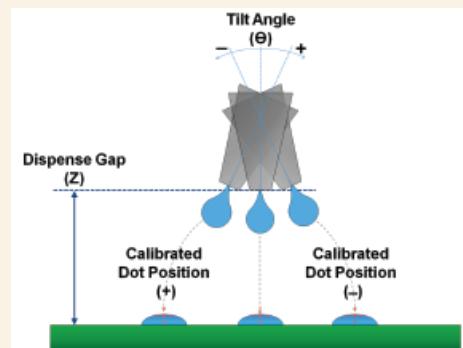


Figure 2: Illustration of how wet dispense accuracy is calibrated at different tilt angles and dispense gap heights.

EVG targeting vacuum encapsulation/bonding needed for next-gen MEMS

EV Group is targeting vacuum encapsulation and bonding processes needed for next-generation MEMS to meet the growing demand for devices that service applications for the Internet of Things (IoT) and wearable sensors. Vacuum sealing of MEMS devices is driven by three primary issues: 1) Reducing power consumption caused by parasitic drag on resonators (e.g., gyroscope applications); 2) Reducing convection heat transfer (e.g., microbolometers, temperature-controlled devices; and 3) Preventing corrosion or other types of interaction with O₂ or H₂O (e.g., parts with exposed Al or AlN).

Thomas Uhrmann, Director of Business Development at EVG, outlined the trending requirements for vacuum sealing/bonding of MEMS devices at SEMICON West 2015 (7/14-16, San Francisco, CA). Among the bonding requirements he noted are 1) CMOS-compatibility (e.g., temperature limits of MEMS sensors and CMOS processes, contamination limitations, and material



Thomas Uhrmann,
Director of Business
Development,
EV Group

Wafer Bonding Processes: Main Features

	Anodic	Glas Frit	TLP	Eutectic	Metal TC
Bonding temperature	350°C – 450°C	350°C – 450°C	180°C – 300°C	300°C – 450°C	100°C – 400°C
Re-melting temperature	na	Same as bonding	Higher than bonding	Same as bonding	na
Bond cycle time	5 – 20 min	20 – 30 min	30 – 50 min	30 – 50 min	15 – 90 min
Line width	>20 µm	200 µm – 500 µm	>30µm	>30 µm	>30 µm
Tolerance to topography	0	1 – 1.5 µm	1 µm	1 µm	0
Vacuum range	Low - Medium	Low - Medium	Medium - High	Medium-High	Medium-High
Getters compatibility	Yes	Yes	Yes	Yes	Yes
Leak rate	Low	Low	Very low	Very low	Low

Table 1: Wafer bonding processes: main features. SOURCE: EVG; from MEMS TechXPOT, SEMICON West 2015

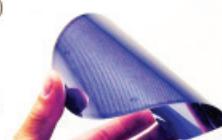
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compatibility), 2) Stress management (e.g., bow and warp management; high-temp processing), 3) Long-term stability of vacuum inside the devices (e.g., getters and high-vacuum bake outs are competing); and 4) Direct vacuum measurement (e.g., optimizing testing schemes for high-vacuum MEMS devices, testing integration into the process flow, and wafer-level testing).

Markus Wimplinger, Director of Business Unit Technology Development and IP at EVG, told *Chip Scale Review*, that high-vacuum levels are driving the need for metal-based bonding schemes and it is becoming more important to integrate MEMS into CMOS devices. Such integration can require electrical connections, hence the need for a CMOS-compatible metal bond. "At the moment, the metal of choice is AlGe," Wimplinger told *CSR*. "AlGe eutectic bonding is quite a delicate process where a lot of process knowledge is needed to get high yields and reasonable throughputs." Wimplinger also noted that there are inherent issues when dealing with Al, such as oxide management. "There is also interest in using pure Al, but so far that hasn't been possible because of oxide management issues."

In his presentation, Uhrmann summarized the bonding challenges by noting that integrated combination sensors with different vacuum requirements are challenging the wafer bonding process. "Combining the right bonding process with the right integration scheme is key," said Uhrmann. Additionally, "Low-temperature thermocompression bonding will play an increasing role for future high-performance MEMS devices."

CORRECTIONS

MAY - JUNE 2015 ISSUE

- Page 22, figure 3 caption in part reads Tessaron it should be correctly spelled as Tezzaron.
- Page 61, the author, Prashant Aji photograph was incorrectly furnished and is correctly identified now.





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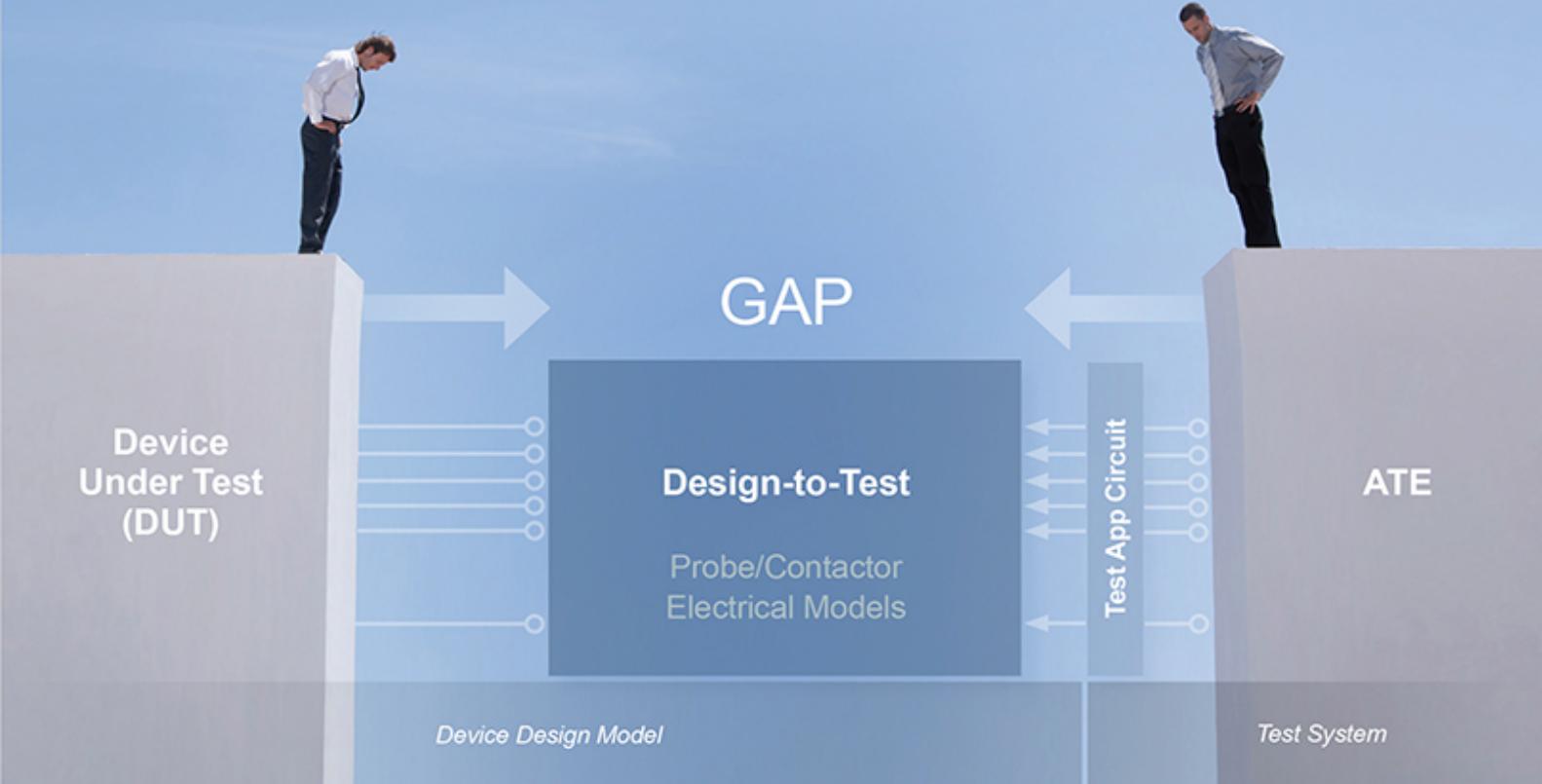
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