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R E V I E W

The International Magazine for the Semiconductor Packaging Industry

Volume 18, Number 4

July • August 2014

Solder alloy trends and technologies in semiconductor packaging and assembly

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- Scalable approaches for 2.5D IC assembly
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As present-day technologies and legislative demands evolve, so does the versatility of soldering materials and processes. Indium Corporation's Dr. Ning-Cheng Lee, VP of Technology, and Dr. Andy C. Mackie, Senior Product Manager, review images of a copper pillar/microbump formed using one of the company's bump-fusion fluxes. These fluxes transform rough, oxidized, plated microbumps into shiny, low-oxide, coplanar hemispheres.

Cover image courtesy of Indium Corporation

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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

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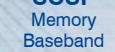
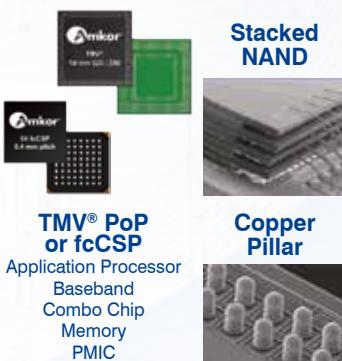
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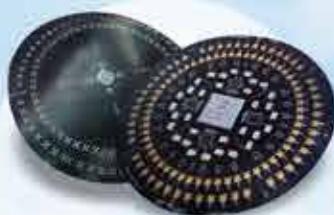
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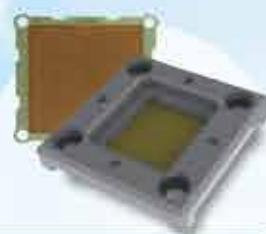
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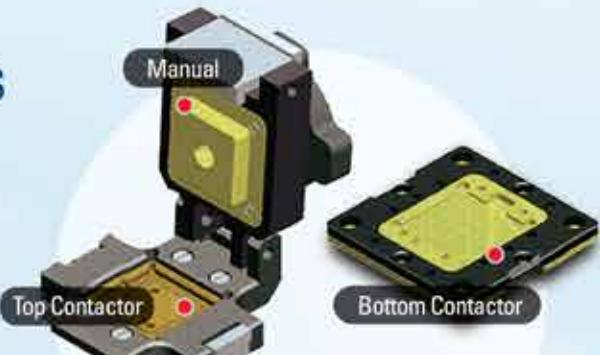
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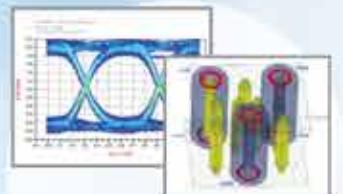
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knewman@chipscalereview.com
Lawrence Michaels Managing Director/Editor
lkm@chipscalereview.com
Debra Vogler Senior Technical Editor
dvogler@chipscalereview.com

CONTRIBUTING EDITORS

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Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER

Welcome to the July/August edition! This year marks Indium's 80th year anniversary in the electronics industry and we wish to extend the company our sincere congratulations. Check out the feature article in this issue.

Yole Développement's senior analyst, Phil Garrou, provides an insightful guest editorial on the impact of warpage on microelectronic packaging. And the latest advances in burn-in and test are published alongside the international user-buyer directory of socket manufacturers. We continue our series focused on R&D Institutes with inputs from Professor Klaus-Dieter Lang of the Fraunhofer Institute for Reliability and Microintegration IZM.

CSR extends a warm welcome to Roger Grace as a member of the magazine's contributing staff. Roger brings a wealth of knowledge that is focused in the MEMS sector. Looking ahead, be sure to pick up the Sept/Oct edition of CSR in which Roger will provide his latest MEMS Commercialization Report Card.

Registration is open for the International Wafer-Level Packaging Conference (Nov. 11-13, San Jose, CA). Boost your company's visibility with a sponsorship and reserve your booth today to ensure networking during exhibiting hours. The Industry News section announces the sponsors and keynote address. Go to www.iwlpc.com today!

Kim Newman

Publisher

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Warpage in microelectronic packaging: a closer look

By Philip Garrou [Yole Développement]

Warpage is a significant issue in surface mount technology (SMT) assembly. It is present in all packaging scenarios from the least sophisticated molded lead frame packages to state-of-the art 3DIC stacked silicon packages. Control of warpage is necessary to achieve yield and reliability especially in today's advanced packages. The continued drive for miniaturization, especially with respect to component height, is exacerbating warpage as it has reduced the thickness of layers that were serving to maintain stiffness and flatness of the components.

Today's advanced electronic packages are made from a variety of materials, including various metals and polymers used in PCBs, solder masks, die attach, over molding, etc. These different materials have coefficients of thermal expansion (CTEs) that can vary from silicon at ~3ppm to silicones at >100ppm. Each material expands to a different degree when heated and cooled.

Polymeric materials are especially problematic. When polymeric materials are cured, they generate a stress-free state at their cure temperature. When subsequently cooled, thermo-mechanically induced stress, and therefore warpage, occurs. In addition, polymer layers shrink during curing, which creates further stresses and warpage.

Laminate substrates

PCB laminates used as substrates for ball grid arrays (BGAs), chip-scale packages (CSPs), package-on-package (PoP) structures, and 2.5/3DICs are a mixture of a rigid reinforcement like a fiberglass weave and a thermoset polymer such as BT (bismalimide-triazine) with copper traces and vias, and a solder-resist coating.

Amkor has reported on the variation in substrates' warpage from different vendors [1]. Substrates sourced from different suppliers, or by different processes from the same supplier, have different degrees of substrate warpage because of different residual stresses.

Warpage

Different materials and package configurations have various challenges with respect to warpage. Several are outlined in the sections below.

Warpage in thin core coreless substrates. To achieve thinner, higher density substrates, especially for today's mobile applications, there has been a move to thin core and coreless substrates (**Figure 1**). Coreless substrates consist of only build-up layers and Cu conductor layers without a stiff core.

Because the core is usually the source of stiffness, thinning (or removal) of the core, as expected, causes major warpage issues. Thinner core substrates show higher warpage at reflow temperature [2] (**Figure 2**).

Shinko has suggested that lowering the CTE and increasing the modulus of the base resin and solder resist will help resist warpage. In addition, a stiffener layer may be required to reduce warpage in coreless substrates [3].

Warpage from underfilling. Underfills are used to protect solder balls by compensating for the thermal expansion differences between the flip-chip (FC) die and a substrate. However, underfilling leads to assembly warpage after cool-down because of underfill shrinkage [4].

Warpage during molding. Epoxy molding compounds (EMCs) are used both in low end lead frame encapsulated packages, as well

as advanced packages such as overmolded BGAs, CSPs, FOWLPs, stacked packages, and 2.5/3DIC stacks.

EMCs are viscoelastic materials that show a time-dependent stress response called "stress relaxation." If such stresses are not "annealed out," warpage can actually increase with time as the stresses relax. Therefore, all EMC suppliers recommend a "post-mold cure," which is an annealing process, where the component/substrate is slowly ramped to just below T_g and cooled back down slowly. This process allows for relaxation of these stresses and reduction in overall warpage.

Warpage in advanced packaging technologies. Various solder joint defects can occur during SMT reflow soldering because of excessive BGA component and/or board warpage [5] (**Figure 3**).

BGAs. Standard flip-chip BGA (FCBGA) packages show warpage because of underfill and single-sided molding. AMD has reported on the effect of BGA warpage on the thermal performance of microprocessor packages. The company uses a thermal lid to minimize the effects of warpage [6] (**Figure 4**).

Fan-out wafer-level packaging (FOWLP). FOWLP, such as embedded wafer-level ball grid array (eWLB), is currently being commercialized by ASE, STATS ChipPAC and Nanium. Die are embedded in a polymeric (EMC) wafer, known as a reconstituted wafer, using wafer-level molding. Thin-film redistribution processes are then used to fan-out

Cored vs Coreless Substrates

(Source: 3D Glass & Silicon Interposers report, Sept. 2012)

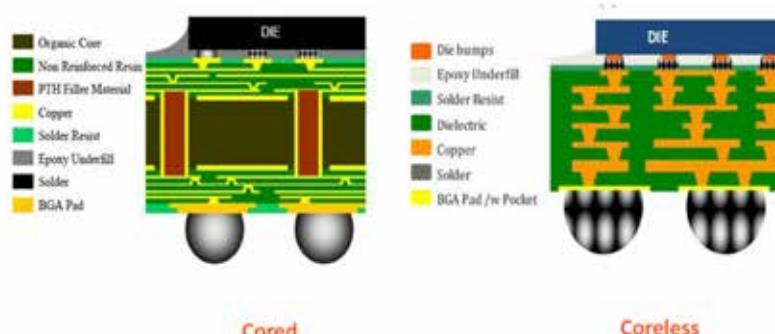
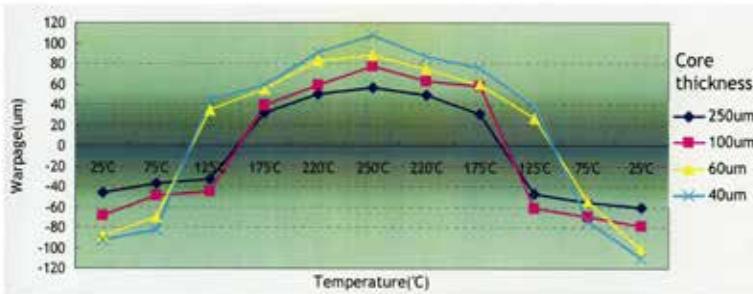


Figure 1: Cored vs. coreless substrates. SOURCE: "3D glass and silicon interposers" report, Sept. 2012.

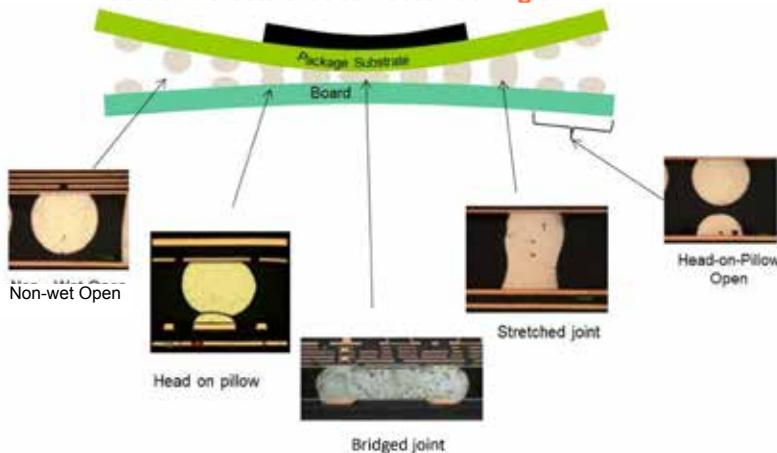
Warpage at reflow temperature for different core thickness substrates *



* K. Lee, "Mobile Platform Packaging Challenges," iNEMI workshop, Nagoya JP, 2009

Figure 2: Warpage at reflow temperature for different core thickness substrates. SOURCE: K. Lee, "Mobile platform packaging challenges," iNEMI workshop, Nagoya, Japan 2009.

Solder Defects that can occur during SMT *



* K Von Dreel, "fcBGA Package Warpage," HDP Users group Sept 13 2013

Figure 3: Solder defects that can occur during SMT. SOURCE: K. Von Dreel, "FCBGA package warpage," HDP Users Group, Sept. 13, 2013.

the interconnections past the x,y dimensions of the die, prior to package separation.

Warpage magnitude and direction must be well understood and controlled for each FOWLP process. The reconstructed wafer EMC should show little shrinkage and have high modulus and low CTE. Overall package warpage is sensitive to the die/EMC thicknesses ratio, die/package ratio, redistribution layer (RDL) thickness, etc. With a proper design, warpage reportedly can be controlled within 0.5mm [7]. Nanium has detailed the warpage during processing of a 300mm eWLB wafer [8].

Package-on-package (PoP). Package-on-package (PoP) technology consists of two or more fine-pitch components stacked on top of one another (**Figure 5**). The bottom package is typically a high-performance logic device and the top package is typically memory.

Bottom package: 1) Has land pads on the perimeter of the top surface to allow for top package attach; and 2) Requires thin die and a mold cap to allow for top package clearance.

Top package: 1) Based on conventional stacked die BGA, but larger ball size and thinner mold body; and 2) Ball pitch and size are constrained by the need to clear the bottom package.

Nokia has reported more than 90% of the defects in PoP assembly are due to package warpage [9]. Additionally, STATS ChipPAC, Spansion and Freescale have detailed a shadow moire study aimed at minimizing warpage on a 15 x 15mm PoP module. Nine die attach materials, 6 mold compounds (EMC), and two substrate materials were examined for their impact on package warpage [10].

2.5/3D ICs

Leading edge packaging is moving towards

2.5/3D structures with through-silicon via (TSV) interconnection. For 3DICs, chips are stacked on top of one another, whereas for 2.5D, chips sit next to one another on a high-density silicon interposer.

Large interposers create assembly issues due to warpage. Thin silicon interposers (i.e., 100µm thick) containing fine-line interconnect (<1µm) for die attach on the top side, and organic or inorganic RDL on the bottom side, for attaching to BGA substrates, result in an unbalanced structure that will show warpage dependent on the materials properties of the front and back side materials [11] (**Figure 6**). The stacking sequence also shows significant impact on overall assembly due to warpage issues [12].

Modeling of warpage

Finite element modeling (FEM) is used to predict process-induced warpage of substrates and PWBs. In 2006, Infineon compared four modeling methods used to predict substrate package warpage [13].

Warpage being addressed by industry users groups

The HDP Users Group (<http://hdpug.org/>) has a program focused on FCBGA warpage. Their goal is to establish a limit for dynamic package warpage that can be mitigated during board assembly without impacting solder joint quality.

iNEMI (<http://www.inemi.org/>) has a program called "Warpage Characteristics of Organic Packages," led by Intel, Flextronics, and Alcatel; the organization also has a program called "Package Qualification Criteria to Ensure Acceptable Warpage Performance at 2nd Level Assembly," led by Intel and Cisco.

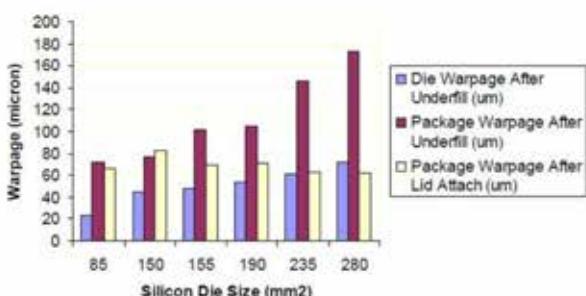
Summary

Warpage is reportedly the #1 issue in advanced component assembly today.

FCBGA packages have warpage issues both for the bumped chip, and the substrate to which it is mounted. Commercial substrate consistency is reportedly poor in terms of lot-to-lot variations. Warped substrates and components cause poor bump attachment (i.e., opens and shorts). This is the same for CSP and FOWLP packages and is exacerbated for PoP structures. Warpage has also become the number one assembly issue for fine-pitch 3D IC technology where the stacking sequence impacts the warpage significantly.

While the major assembly houses use

Warpage of Microprocessor Packages as a function of die size, underfilling and lid attach *



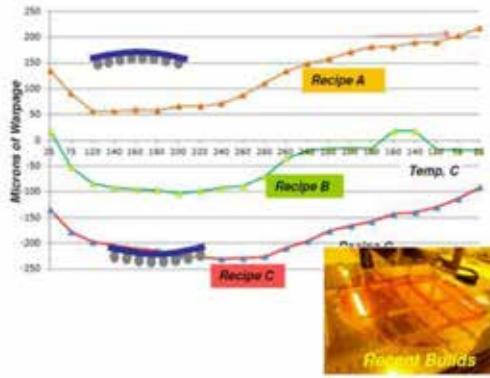
* 2007, R. Master et. al., "Effects of Organic Package Warpage on Microprocessor Thermal Performance," ECTC, p. 748

Figure 4: Warpage of microprocessor packages as a function of die size, underfilling, and lid attach. SOURCE: R. Master, et al., "Effects of organic package warpage on microprocessor thermal performance," p. 748, ECTC 2007.



Figure 5: Typical package-on-package (PoP). SOURCE: "3D glass and silicon interposers" report, Sept. 2012, slide #229 ("Emerging evolutions of PoP for the 3D stacking of memory module on logic").

Variation in Interposer Warpage Due to Differing Front and Backside Processes *



Inorganic and Organic Passivation

- Warpage tuning across several fabs

Considerations:

- Film stresses for incoming wafer
- Interposer thickness
- BS RDL or not

* M. Kelly et. al., "Assembly Challenges for 2.5D Packages," IMAPS Device Packaging Conf., Scottsdale, 2013

Figure 6: Variation in interposer warpage due to differing front and backside processes. SOURCE: M. Kelly, et al., "Assembly challenges for 2.5D packages," IMAPS Device Packaging Conf., Scottsdale, AZ 2013.

FEA modeling to predict warpage, and use techniques such as shadow moire to measure warpage during prototype runs, most still view warpage as somewhat of an "art" requiring extensive data bases of known structures.

The industry must control package warpage to continue to move forward.

Biography

Philip Garrou received his PhD in Chemistry from Indiana U. In 2004 he retired from Dow Chemical as Global Director of Technology and Business Development for its Electronics Business Unit. He has served as President of IEEE CPMT (2004-2005) and IMAPS (1998) and is currently a Sr. Analyst for Yole Développement; email garrou@yole.fr

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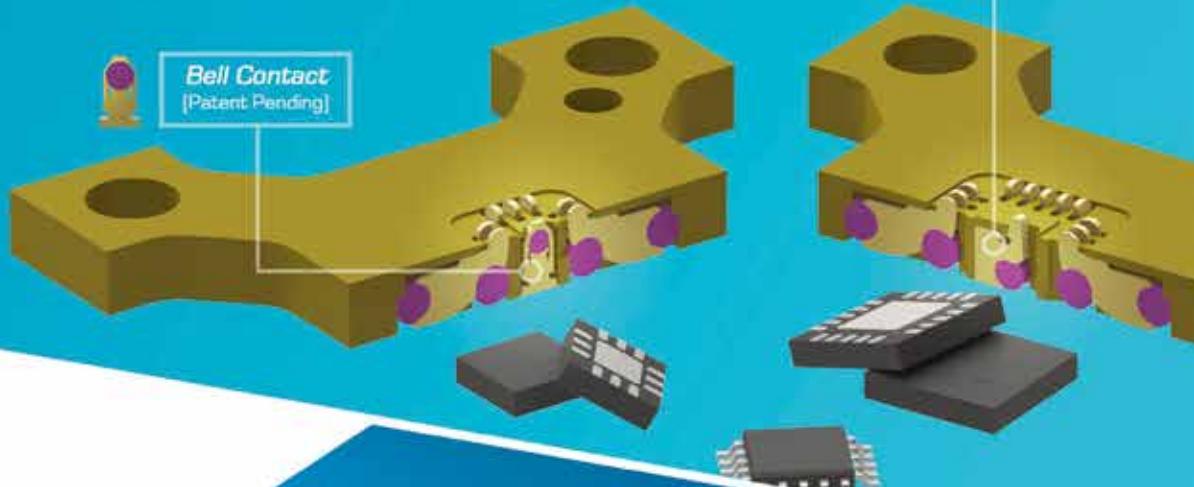
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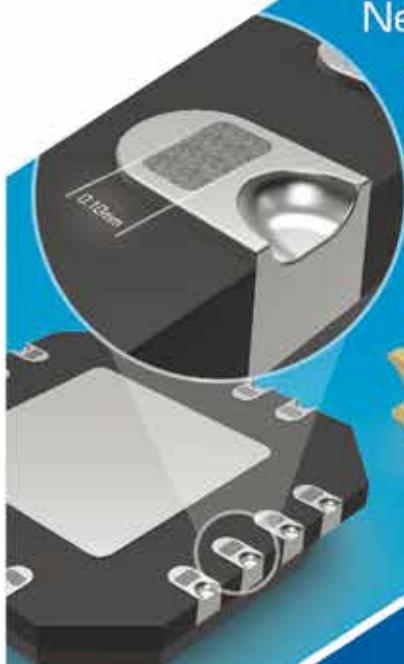
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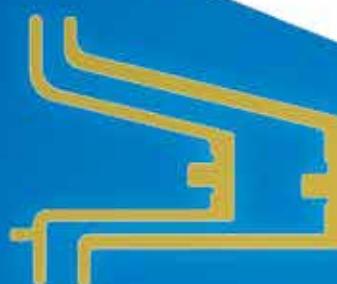
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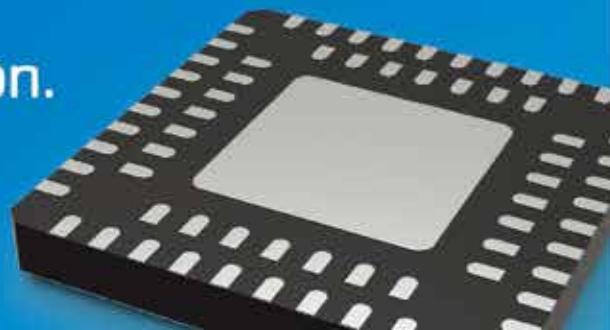
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INDUSTRY NEWS

International Wafer-Level Packaging Conference (IWLPC) Keynote Announced



Living Connected Through Trillions of Sensors



Dr. Janusz Bryzek, Chair, TSensors Summit will present at the 11th annual IWLPC the coming wave of sensor-based products.

We are witnessing the emergence of the largest economic tide in the history of humans: the Internet of Everything (IoT), including eHealth. The magnitude of this global tide is estimated at \$19 trillion by 2020, exceeding the size of today's US economy.

The foundation of this global tide is sensors. Sensor use in the mobile market grew to 10 billion units/year today, up from 10 million in 2007 (iPhone introduction). The Abundance movement (a movement aiming at the elimination of major global problems, e.g., hunger and lack of medical care) forecasts the demand for sensors to grow to 45 trillion units in two decades. The TSensors (Trillion Sensors) Initiative has emerged, aiming at acceleration of new sensor commercialization to support the needs of the Abundance movement.

Sensors are starting to invade every aspect of our lives, generating massive amounts of data (i.e., "big data"). Consumer products already are using about 100 different types of sensors. Sensor-derived data moving through the Cloud, Fog and Swarm networks is expected to reach a BrontoByte (1027), thereby enabling analytics on an unprecedented scale, and enabling prediction of our needs through machine learning algorithms running on quantum computers.

Sensors are one of the eight exponential technologies enabling the growth of goods and services faster than growth of demand for them. Exponential technologies enable exponential organizations (ExOs) that are expected to demonstrate sales growth of a billion dollars in one to three years. New ExOs are expected to replace 40% of the Fortune 500 companies in the coming decade, in a manner similar to the replacement of Kodak with Instagram in 2012.

This presentation will discuss these issues in more detail and present an amazing showcase of available sensor-based products.

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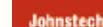
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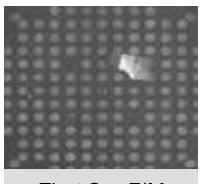
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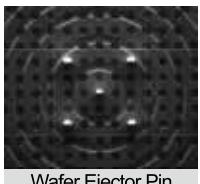
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SECTION		FLIP CHIP BONDER-A110	FLIP CHIP BONDER-S100
PRODUCTIVITY	UPH	15,000 (Based on Dry Run)	
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	CHIP ROTATION(θ)	$\pm 0.1^\circ$ @ 3σ	
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)	
FOOTPRINT	DIMENSION (Wx Dx H)	1,600mm x 1,200mm x 1,500mm	
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INDUSTRY NEWS



2014 ECTC
continues its
tradition of
excellence

The 64th annual Electronic Components and Technology Conference (ECTC) sponsored by IEEE/CPMT convened at the Swan and Dolphin Hotel on May 27–31, 2014. By all measures, the event, considered by many to be the premier international conference on IC packaging, components, and microelectronic systems technology, was a success.



Program Chair, Alan Huffman, RTI International and Wolfgang Sauter, IBM, 63rd ECTC General Chair, with ECTC Keynote Speaker, Dr. Peter Bocko, CTO of Corning Glass Technologies (center).

There were many broken records at this years ECTC, including the highest attendance ever in Orlando: 1,170 attendees from 33 different countries; 18 professional development courses (PDC) attended by more than 400 participants; 101 Technology Corner exhibitors including 21 new exhibitors; and an overall increase of corporate sponsors.



Ms. Ruth Zhou, Marketing Manager, World Scientific Publishing Co., Inc. held a reception in honor of Prof. Avram Bar-Cohen, who received the 2014 IEEE Components, Packaging and Manufacturing Technology Award.

The conference consisted of 369 technical papers, presented in 36 oral and 5 interactive presentation sessions, including a student poster session. This year, the ECTC abstract acceptance rate was 61%, with submission divided between universities (45%), corporations (44%) and institutes (11%).

The number of papers accepted from China continues to increase year-to-year. China was third in papers presented at the ECTC following United States and Japan.

While 3D still dominated in the number of sessions, other alternate packaging structures, such as PoP and PiP, also had a good representation of papers. Finally,

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Bill Moody receives congratulations from Wolfgang Sautter, IBM, 64th ECTC General Chair, on his retirement from organizing the Technology Corner for many years.

the interconnection issues, such as chip-package interactions and solder and RDL wiring electromigration attracted many attendees.

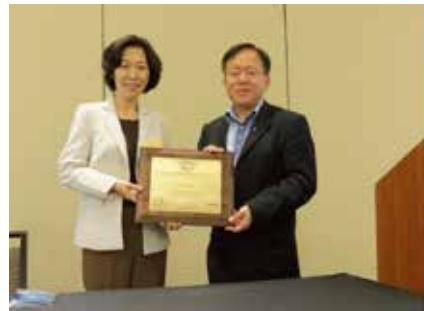
ECTC: day-by-day

Starting on Tuesday, the ECTC offered a packed program to all attendees. Tuesday is the education day with



This year's ECTC Gala sponsors were: Amkor, DOW Electronic Materials, Nanium, SPTS, Applied Materials, and Micron.

the courses, three special sessions on Technology and Application Trends in the Field of Flexible Electronics chaired by Karlheinz Bock of Fraunhofer EMFT, Wireless power transfer system session chaired by Manos Tentzeris of the Georgia Institute of Technology and Craig Gaw of Freescale, and Emerging Technologies and Market Trends of



Jie Xue of Cisco and current CPMT President presents a plaque in recognition to Ricky Lee of Hong Kong University of Science & Technology for serving as the CPMT Society President from 2012-2013.

Silicon Photonics chaired by Jie Xue of Cisco Systems and Ricky Lee of Hong Kong University of Science & Technology. Additionally, ITSR and i-Nemi had their ground rules and technology meeting. Two social functions, the ECTC Student reception hosted by Valerie Oberson of IBM,

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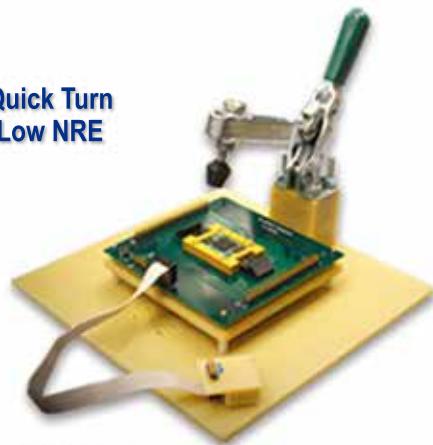
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Xongxia Lu, Technical Program Manager at Intel, attends one of the 36 oral presentation sessions.

and the ECTC speakers reception, complemented a full technical day.

On Wednesday, in addition to the oral and interactive sessions, the technology corner opened its door. At lunch the ECTC Keynote Speaker, Dr. Peter Bocko, CTO of Corning Glass Technologie, covered the extensive uses of glass technology today, from electronics application to art. ASE was the luncheon sponsor. Nancy Stoffel of GE Global Research chaired the panel session on the contribution and influence of packaging on system integration and performance. The technology corner's vendors sponsored the night reception.



Enjoying the Speakers Reception are (standing): Prof. Mark Poliks, University of Binghamton, and Prof. Robert Kao, National Taiwan University; and (sitting): Babak Arfaei, Universal Corp., and Eric Perfecto, IBM, ECTC Publicity Chair.

On Thursday, the main conference continued, and at lunch, the CPMT society gave out the society's major awards. This year, the IEEE CPMT Award recipient went to Avi Bar-Cohen of the University of Maryland. At night, following the ECTC Gala Reception, the CPMT seminar co-chaired by Kishio Yokouchi of Fujitsu Interconnect Technologies Ltd., and Venky Sundaram

of the Georgia Institute of Technology, covered the latest advances in organic interposers.

Finally, on Friday, the oral presentations continued, and the interactive presentations showcased the students' papers. Finally, the ECTC raffle was held at the Program Chair Luncheon, sponsored by NCAP China.

Mark your calendar for the 65th ECTC

Planning is already underway for the 65th ECTC, which will be held May 26-29, 2015, at the Sheraton Hotel & Marina in San Diego, CA. The first call-for-papers has been issued and abstracts must be received by October 14, 2014. For more information visit www.ectc.net.

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Solder alloy trends and technologies in semiconductor packaging and assembly

By Andy C. Mackie, Ning-Cheng Lee [Indium Corporation]

As far as anyone can tell, solder as a joining material has been around since pre-Roman times [1]. Its continued use, through present day and beyond, is a testament to the continued utility of this set of materials. Solder as a versatile electronics joining material is continually adapting to the demands of technology, legislation, and the widely varying needs of its myriad applications. Solder appears in several areas in electronics packaging: for standard semiconductor devices, it may appear in flip-chip joints; as solder in wafer-level chip-scale packages (WLCSP) and ball-grid arrays (BGAs) (**Figure 1**). For power devices, solder may appear as the die-attach material in wire-bonded packages, or by forming all of the interconnects in a clip-bonded package (**Figure 2**). **Figure 3** shows the evolution in flip-chip solder bump geometry and materials over the last 25 years.

Although wire bonding or conductive adhesives are also used as a means of direct electrical interconnect in the semiconductor industry, soldering is by far the most favored approach in semiconductor packaging for high I/O and ultra-fine pitch applications. This is mainly due to the uniformity of the bonding material even at micron sizes, tolerance of the surface to be bonded, physical properties of the joint, bonding process windows, and quality and reliability of joints formed with soldering technology that unceasingly meet the challenges of advancing new designs. Consequently, it is important to understand the nature, options, and limitations of certain solders, and their associated soldering processes, in order to maximize their benefit in semiconductor assembly operations.

Basics of the solder process

The goal in forming any electrical interconnect is to form a strong,

reliable, and electrically and thermally conductive joint. The formation of the solder joint is enabled by two factors: the complete melting of the solder at a temperature below the thermal budget of the in-process device, and the wetting and spreading of solder onto surfaces. The frequently used term "solderability" is a way of describing how quickly and evenly the solder spreads onto a surface. Strong, low-voiding solder joints always result from good wetting. Solderability is a very loose term as it combines elements from both kinetics and thermodynamics. The main driving force for good solderability is thermodynamic: that is, the negative-free energy of formation of an intermetallic, which is created when liquid solder contacts many solid metal surfaces, favoring the contact of the liquid metal with the metal surface. In most applications, the solder joints formed in the chip packaging process have to survive several subsequent reflow and possible rework cycles during the final system-level assembly process, even before the assembly has seen use.

Depending on the application, the solder joint then has to survive over the lifetime of the final assembly. The

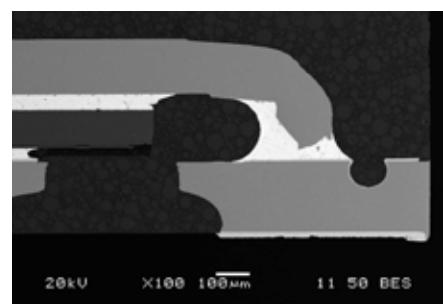


Figure 2: Use of solder as the die-attach material in the formation of interconnects in a clip-bonded package.

Figure 1: Applications of solder in electronics packaging.

reliability requirements for a packaged die inside a portable device mostly only require device survival during thermal cycling up to 90°C and a certain amount of mechanical shock, although flip-chip packages are always underfilled, reducing the effects of instantaneous stresses on the solder joints. Contrast this relatively benign need with those requirements for the solder used in “under-the-hood” automotive electronics where high operating temperatures, high current density, shock, thermal cycling, vibration, and the possibility of exposure to high humidity and salinity all combine to make this one of the most demanding applications for electronics today.

Different forms of solder

Many methods have been used to apply the solder, requiring it to be available in a variety of forms, one of which is molten solder, discussed below.

Molten solder. Molten solder has been directly jetted onto wafers for wafer bumping, although the process is typically too slow for general usage. Molten solder has also been printed directly onto under-bump metallization (UBM) in IBM’s C4-NP process [2]. Another method of applying molten solder directly (in this case to a substrate) is as a solid wire, melted immediately prior to use in a “soft-solder” die-attach application for larger power die (typically those contained in a TO220 and larger package), where solder paste often cannot deliver the low voiding and tilt control needed.

For most applications, solder is usually applied in one of several solid-alloy forms before a melting (“reflow”) process, described as follows:

Solder paste. Solder paste is comprised of solder powder of a specific diameter range with a flux carrier vehicle and has the advantage of tremendous flexibility of usage. Typically, a viscous, pseudoplastic, thixotropic material, solder paste can be adapted for printing, dispensing, dipping, pin-transfer or even jetting. In standard flip-chip applications, it has usually been printed onto wafers or substrates, then reflowed and cleaned to form bumps, although occasionally

it is applied to solder balls on a wafer-level chip-scale packaging (WLCSP) assembly, or via pin-transfer to a lead frame, using a dipping process. Wafer bumping for finer pitch (<185µm) standard bumps and for copper pillar applications on the die surface has mostly been converted to plating. Concerns about print consistency and substrate co-planarity with the newer reduced layer-count/low coefficient of

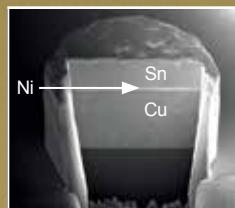
thermal expansion (CTE) substrates have led substrate manufacturers to move away from type 6 and 7 solder pastes for solder-on-pad (SOP) formation, and move toward the use of reflowed solder spheres. The potential of further solder powder miniaturization for these applications also appears to be low because of increasing solder volume consistency issues for ultrafine-pitch printing.

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SEM picture of copper pillar plated with 4 µm/min



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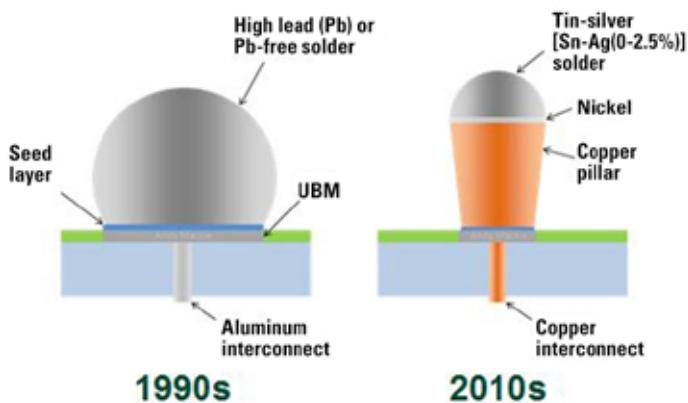


Figure 3: The evolution in flip-chip solder bump geometry and materials in the last 25 years.

Low metal-loading solder paste may be used in a variety of ball-attach (BGA/WLCSP) operations in place of flux, which sometimes cannot retain the solder sphere in place, leading to the “missing ball” phenomenon.

Solder preforms and solder spheres. Solder preforms and solder spheres are available in a variety of shapes and sizes (**Figure 4**), and can provide near-net-shape processing to allow some degree of control of such critical variables as bond line thickness and die tilt in die-attach. They may also be used as a means of simply adding volume to a solder paste joint.

Preforms may be used either with a separate flux medium, purchased with a conformal flux coating already applied, or applied “dry” without any flux. In this last case, a reactive reducing atmosphere, such as formic acid or forming gas, is used for reflow. Flux acts as both a means of removing oxides and holding the die, preform, and substrate metallization in alignment. If no flux is applied, an external fixture of some kind (usually spring-loaded) must physically restrain the die from moving. Preforms have the advantage over solder paste of having inherently lower surface area, and hence lower oxide levels, so may give much lower voiding.

Alloy types

Besides the reliability and similar needs of the final joint, other critical factors that determine the proper solder alloy include cost, environmental

compliance, subsequent exposure to heat (such as subsequent reflow or rework processes), and simple pragmatics of the desired reflow equipment or process. The concept of “thermal budget” is typically applied to semiconductor devices and may also govern

assembly processes, as it combines constraints of maximum time and temperature exposure driven by the exigencies of Arrhenius-based diffusion kinetics.

Pb-containing solders

Pb-containing solders such as Sn/Pb37 (the alloy referred to in semiconductor assembly as “eutectic”) have mostly been eliminated because of environmental considerations. The remaining usage occurs in both standard surface mount technology (SMT) processes for more reliability-conscious markets, such as medical and military, and in semiconductor assembly where high-Pb content solders are almost exclusively used in die-attach applications for higher junction temperature devices.

High-content Pb solders are well known to give good reliability at higher temperatures, which led to their adoption in the latter half of the 20th century as die-attach materials for applications, such as automotive device packaging, where Pb/Sn5/Ag2.5 and Pb/Sn2/Ag2.5 are the predominant alloys.

Pb-free high melting point materials and solders

The search for an alternative to high Pb-containing solders that meet

RoHS and similar legislation has been ongoing for many years, with many alternative approaches, such as BiAgX® solder paste technology, sintered nano material, and transient liquid phase (TLP) materials under consideration.

Solders. It is interesting to note that although the trend toward elimination of Pb in power semiconductor devices may have initially been for real or perceived environmental benefits, more pressing concerns have emerged. These are twofold: the need for increased reliability at higher die junction temperatures ($T_j > 150^\circ\text{C}$, especially for the higher current densities associated with gallium nitride and silicon carbide die), and new failure modes associated with electrical reliability in thinner die. The thinning of logic and memory devices is well known, but it is interesting to note that many power semiconductor die are also thinning down, in some instances to 60 or even 50 μm thickness, to reduce the die contribution to RDS_{ON}.

BiAgX® technology is based on a mixed solder paste system, which uses a combination of a high tin-containing solder as an initial wetting medium suitable for surfaces like bare copper, copper/OSP (organic solderability preservative), electroless nickel immersion gold (ENIG), and electroless nickel/electroless palladium/immersion gold (ENEPIG). When subjected to a standard high-temperature reflow profile, the high-tin solder melts and



Figure 4: Solder preforms and solder spheres are available in a variety of shapes and sizes.

then reacts with the nickel or copper surface to form an intermetallic, leaving a high Bi-containing BiAg solder joint that will not re-melt until over 260°C.

Gold-containing solders, most commonly Au/Sn20 (melting point 280°C), are used in very high current density applications for their reliability and high thermal and electrical conductivities. Even very small joints will completely and elastically deform without creep, leading to their use in areas such as electrical interconnects in wafer-probe cards. Au/Sn20 also has the highest tensile strength of any solder, making it ideal for very demanding, smaller die usage, but unsuited for die larger than around 2mm square, as it may physically break the die. It is also becoming an increasingly suitable material for applications where the die may attain 300°C or so in operation due to the high melting point. In this case, Au/Ge12 (356°C) may be a suitable alloy. It is interesting to note that when Au/Sn20 solders onto high gold-content

surfaces, voiding can usually be reduced by decreasing the initial gold content of the solder.

Transient liquid phase (TLP) soldering. TLP soldering involves the use of a solder alloy or low melting metal in conjunction with at least one other metal to which the molten solder wets to form an intermetallic compound (IMC). The “transient” part of these classes of solder materials comes from the need for the final joint to have no free solder alloy left, as it has completely converted to an IMC. A composite preform [3] has been developed that uses a thin layer of solder on a highly-compliant silver layer that is reflowed, then converted to an IMC, and is designed to be used as a die-attach material for very high temperature (T_j) applications such as IGBT modules, where vacuum soldering is commonly used.

Sintering materials. Sintering materials such as nano silver are not usually solders, but often touch on the

same application areas. Dispensed or printed paste-like nano materials cannot have a volumetric metal loading higher than 50%, as the material becomes too high in viscosity to be easily applied using standard techniques. For this reason, sintering materials initially have an open metallic network that is inherently fragile, and typically, unless high temperature and/or high pressure post-processing is used for densification, their usage is limited. Cost (of both materials and new capital equipment) is also a significant barrier to adoption as a Pb-free material.

Low melting point solders

Some packaged devices, such as ultrasonically-bonded plastic-capped MEMS packages, have a thermal budget that constrains the choices for assembly solder alloy to those with a maximum processing temperature of less than 200°C. With such device types, even the processing of “eutectic” solder (melting point 183°C) may be sufficient



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to drive a need for a peak temperature above 200°C. Due to their naturally high malleability, indium-containing solders have been used in these types of applications for many years. Pure indium (In100) solder bumps are used in ultrafine pitch detector array applications where the low melting point of the solder allows the formation of a strong compliant joint without exceeding the thermal budget of the device. Such devices are often of less than 20µm pitch, with over 50,000 I/Os.

Packaged LED devices are also sometimes manufactured in final assembly with SnBi or SnBiAg solders to reduce the thermal budget on the LED die and increase their useful lifetimes.

High-Sn solders

High tin-containing (Sn) solders usually melt between 217°C and 231°C (the melting point of pure Sn) and are most commonly used for standard SMT assemblies since their adoption early in the 21st century. These so-called “SAC” (SnAgCu) solders are typically used in BGA, micro-BGA and wafer-level CSP applications, and have been used for larger pitch flip-chip bumps and SOP (solder-on-pad).

The solder micro-bumps on copper pillars for most applications are formed of below-eutectic SnAg, and the low compliance of the final joint is starting to drive a need for the use of indium-containing solders [4].

Modified or doped alloy solders

Since the adoption of SAC alloys for SMT, and as spheres for WLCSP and BGA manufacture, there has been a lot of concern about both their cost and long-term reliability relative to eutectic solders. For this reason, a variety of high-content Sn solders has been developed that incorporates low percentage to less than 1% by weight of one or more elements that do not typically appear in solders. **Figure 5** illustrates the small number of elements that are suitable for usage in these applications.

Some of the additive elements that have been adopted or reported in the industry: 1) Bi and In stiffen the solder through the solution hardening

mechanism; they also lower the melting temperature of alloys. 2) Sb also stiffens the solder through solution hardening, but raises the melting temperature of solder. 3) Zn stabilizes both SnAg₃ and Cu₆Sn₅ IMC networks in the solder microstructure. It impedes the formation of large SnAg₃ platelets, and slows down the electromigration process. 4) Ni and Co suppress the growth of IMC, resulting in a refined grain size. The fine IMC particles dispersed at the grain boundary effectively harden the solder.

Among the impurity (trace addition fraction of 1%) elements, alloying elements with hexagonal close-packed (hcp) structures, such as Co, Zn, Ti, and Mg, enhance heterogeneous nucleation of β-Sn phases in Sn-rich solders, and are effective in reducing the undercooling of solder joints.

Mn exhibits the hcp structure as well, reducing the undercooling. The addition of Mn significantly suppresses IMC growth, resulting in stabilized, fine IMC particles and a very thin IMC layer at the solder joint interface. The fine IMC particles stabilize the solder microstructure (**Figure 6**), improving the solder’s thermal fatigue

properties, while the thin IMC layer results in a significantly improved drop test performance, as demonstrated by Indium Corporation’s SACm™ alloy technology.

For semiconductor packaging applications, these alloys are usually used in the form of solder spheres, which are soldered to BGA or WLCSP packages. The finished package is subsequently soldered to a substrate using a solder paste or epoxy flux.

Nano solders

Solder pastes comprised of nano solder particles (<100nm diameter) were perceived to have the potential to reduce the solder reflow temperature, yet enable the creation of a finished joint with typical solder melting temperature. This implied that it could potentially reduce operating costs and enable a high reliability device of special application to semiconductor packaging. However, it was found that although the solder did start melting at a lower temperature, the reflow peak temperature could not be reduced. The high cost of nano solder particles was another significant barrier to adoption.

Periodic Table of Solder Elements

Elemental Group Number																	
1	2	IIIa	IIIb	IV	V	VI	VII	VIII	IX	X	XI	XII	3	4	5	6	
Li	Be												B	C			
Na	Mg												Al	Si	P	S	
K	Ca	Sc		Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	
Rb	Sr	Y		Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	
Cs	Ba	La	Ce	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi		
Fr	Ra																

Omits gaseous and highly radioactive elements

Key:	Used at % levels in solders
	May be added in small quantities
X _y	Highly toxic
X _y	Highly reactive with oxygen/moisture
X _y	Expensive
X _y	No known use in solder

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Figure 5: Elements suitable for use in solders.

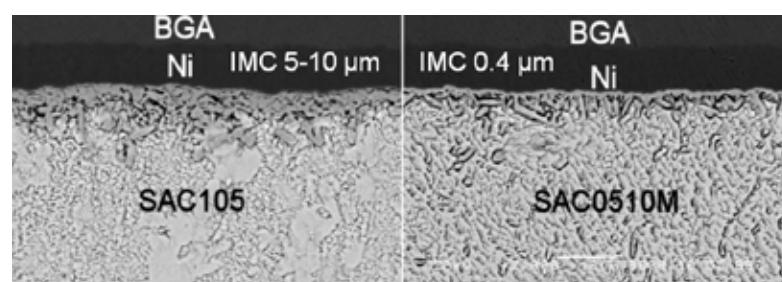


Figure 6: Fine IMC particles stabilize the solder microstructure.

Nano particles as an additive to conventional solder paste do show potential for enabling solder joints with higher reliability. For instance, nano aluminum (Al) particles were reported to improve the microstructure and fatigue life of SAC solder joints in quad flat package (QFP) devices, which has been attributed to the dislocation restricting of particles. However, the seemingly inevitable voiding associated with poorly-wetted nano particles remains a challenge.

Summary

Solder as an electrical and thermal joining material has a long history behind it, but as the needs of electronics joining processes and legislative demands flourish and change, it is clear that solder also has a bright future in a variety of evolving forms as a highly flexible and durable interconnect material for many future semiconductor assembly interconnects.

Biographies

Andy C. Mackie received his PhD in Physical Chemistry from the U. of Nottingham, UK, and a Master's of Science (MSc) in Colloid and Interface Science from the U. of Bristol, UK. He is a Senior Product Manager at Indium Corporation; email amackie@indium.com

Ning-Cheng Lee received his PhD in Polymer Science on structure-property relationships from the U. of Akron, and a bachelor's degree in chemistry from the National Taiwan U. He is Vice President of Technology at Indium Corporation; email nclee@indium.com

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Scalable approaches for 2.5D IC assembly

By Charles G. Woychik, Liang Wang, Sitaram Arkalgud, Guilian Gao, Andrew Cao, Hong Shen, Laura Mirkarimi, Eric Tosaya
[Invensas Corporation]

The ability to stack die using through-silicon vias (TSVs) offers many performance enhancements that have been discussed previously [1, 2]. Earlier silicon interposer (Si-ITP) designs used thick interposers in order to provide rigidity and flatness for handling and subsequent assembly of finer pitched die on the top surface. One problem in this approach is that the thicker interposers require larger diameter TSVs that consume increased silicon area and produce higher stress while also taking longer to plate. The alternative of smaller diameter TSVs results in high aspect ratios that make it harder to fill. Therefore, using thinner interposers having smaller diameter TSVs is the strategic direction we believe the industry should take.

In order to achieve this goal of smaller TSV diameters along with thinner interposers, however, a major obstacle to overcome is processing the backside of a thin Si-ITP wafer supported by a handling wafer. A particularly significant problem in this process is the removal of the completed thin wafer from the handling wafer without damaging the thin wafer and the complete removal of adhesive residues [3, 4]. Overcoming these challenges continues to be a serious problem in developing an acceptable process for high-volume manufacturing and is expected to get worse as wafer thicknesses scale down with increasing stacked layers.

In this paper, we will discuss our experience with processing three major assembly flows for a common type of 2.5D application, as schematically illustrated in **Figure 1**. In this figure, two micro-bumped dies (MBDs) are attached to a Si-ITP, which is then

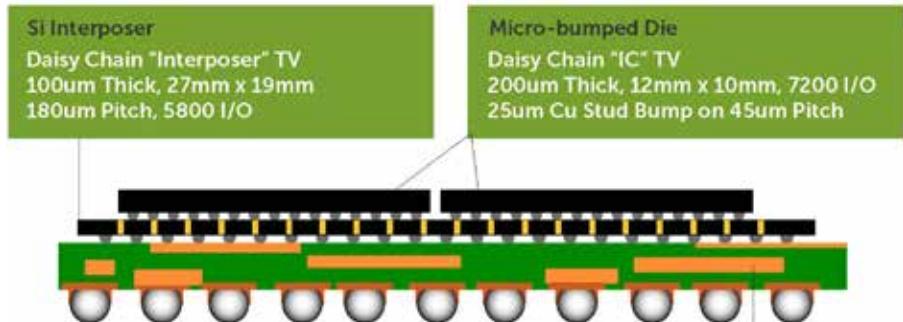


Figure 1: 3-4-3 build-up substrate.

attached to a standard build-up substrate. We will discuss the rationale for each approach and present the advantages and disadvantages of each.

Test vehicle design

In this evaluation, each MBD is 10mm x 12mm in size and 0.600mm thick, as shown in **Figure 1**.

For the MBD, a Sn-2.5Ag alloy solder capped Cu pillar type of interconnection was used with a 45 μ m pitch. The Cu pillar had a 25 μ m diameter and a 20 μ m height with a 12.5 μ m height half-sphere solder cap on the tip. The Si-ITP was 19mm x 27mm in size and 0.100mm thick, with 20 μ m diameter x 100 μ m depth Cu-filled TSVs. A standard redistribution layer (RDL) was used on the top surface and a low temperature polyimide RDL was used on the backside of the Si-ITP. The topside

Assembly Flow Exploration at Invensas

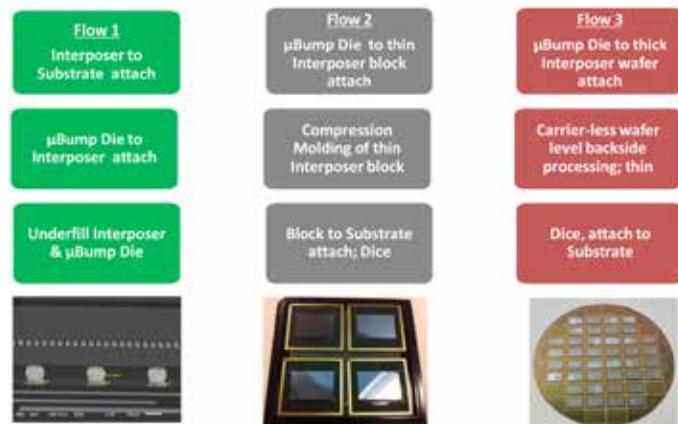


Figure 2: Assembly flow exploration at Invensas.

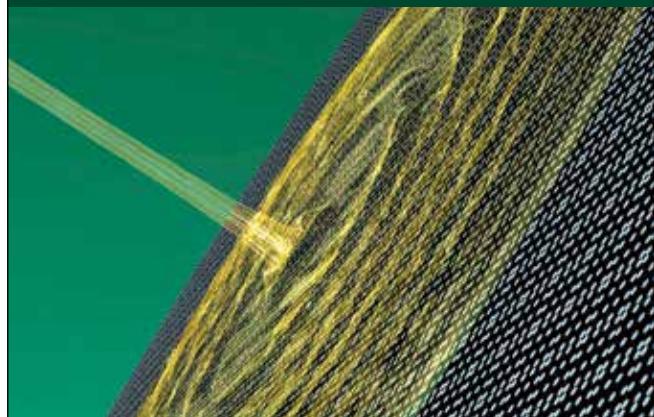
was electroless nickel/immersion gold (ENIG) plated and the backside was bumped using a standard Pb-free solder alloy. The substrate was a 3-4-3 build-up type of construction.

Evaluation of assembly flows

The three assembly flows are presented and the rationale for using each method is discussed in this section. The use of a thick cored substrate for assembly of the interposer was found to show a dramatic decrease in overall warpage of the assembly for all

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methods evaluated. **Figure 2** shows three different assembly flows. In process flow 1, the interposer is first attached to the substrate and then the MBDs are attached in the last step on the interposer. In process flow 2, the MBDs are first attached to the Si-ITP and then this assembly is attached to the substrate. In flow 3, the MBDs are first attached to a thick unrevealed wafer and then molded on the top surface, thinned, and the TSVs revealed. Solder balls are attached on the backside of the wafer and dice, then attached to the substrate. The process details are discussed below.

Process flow 1. As shown in **Figure 3**, a singulated fully-processed Si-ITP (topside ENIG and backside Pb-free solder bumps) is first attached to the substrate using an in situ thermal (IST) bond tool, as shown in step 1 of **Figure 3**. After cool down to room temperature, the assembly bowed as illustrated in step 2 of **Figure 3**. Next, the two MBDs are attached to the topside of the Si-ITP using the IST tool. This is a very important step because the preheat of the interposer/substrate assembly needs to be such to ensure that

Assembly Flow 1 – Substrate First Approach

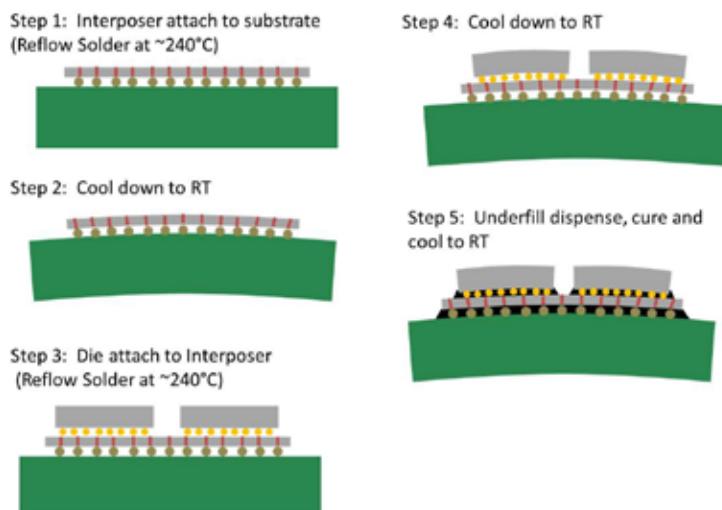


Figure 3: Assembly flow 1: substrate first approach.

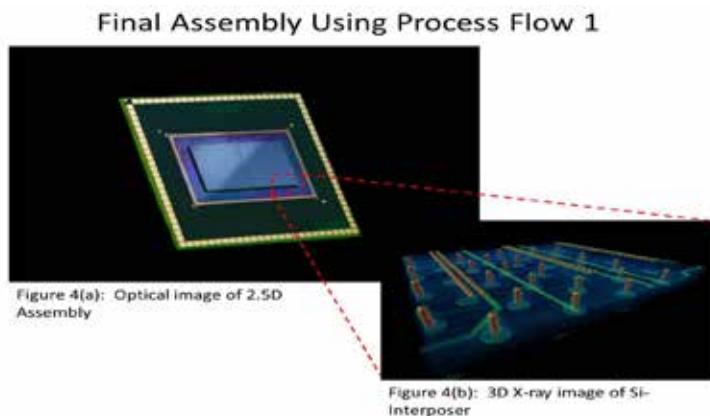


Figure 4: Final assembly using process flow 1.

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the Si-ITP is sufficiently flat for the IST bonding of the two MBDs as shown in step 3. Upon cool down to room temperature (RT), the assembly bows as shown in step 4. The underfill materials for both the interposer and the MBDs are dispensed and cured. The final structure after assembly is shown in step 5 after cool down to RT. The final assembly is shown in **Figure 4a**. **Figure 4b** shows a 3D X-ray image of a section of this assembly outlined by the dotted red lines.

The second step of bonding the two MBDs to the interposer is the critical step. Here the use of an IST bond tool requires that preheat of the interposer attached to the substrate needs to be at a temperature that ensures that the interposer remains flat during a Pb-free solder reflow of the MBD. A desirable feature of using this method is that one can use the substrate as a support for the fragile interposer and MBDs during assembly, which can be done using an outside semiconductor assembly and test (OSAT) type of assembly methodology. A major challenge in this approach, however, is that the coefficient of thermal expansion (CTE) mismatch between the different levels of packaging results in warpage, which needs to be addressed by careful thermal profiles in the IST bond tool during the two stages of assembly.

Process flow 2. A completed Si-ITP wafer is processed using a temporary handle wafer approach that was described in the previous section. The first new step in this approach is to dice out an array of 2x4 Si-ITP die from the wafer, called a block. This Si-ITP block then becomes the foundation on which the 3D assembly is built. In step 1 of **Figure 5**, the block is held in place using a vacuum chuck to ensure flatness. The individual MBDs are attached to the block using the IST bond tool. In step 2, an underfill material is dispensed for each of the MBDs and then the entire block is cured. The experimental data reveals that the amount of warpage after underfill is not significant.

In Step 3, the MBDs attached to the interposer block are compression molded to provide rigidity and flatness

for subsequent processing. Here the molding provides the necessary rigidity to be able to handle the thin interposer block. After cool down to RT, the molded block warps about 40 μm without solder balls attached to the backside.

In Step 4 of **Figure 5**, the molded block is then bumped with Pb-free solder balls using solder jetting and singulated into bumped interposer assemblies. The jetting process is able to accommodate the warpage in block assembly.

Finally, in Step 5, the bumped molded interposer assembly can be attached to the substrate using conventional flip-chip attach methods.

A major driving factor in developing this approach is to use the overmold to provide support and flatness to handle the thin silicon interposer along with the fragile MBDs during the assembly process. Also, in this assembly method, better assembly

yield of the MBDs can be achieved due to the fact that one is attaching a thick flat MBD to a flat thin Si-interposer, which is firmly held in place with a vacuum chuck.

Process flow 3. This approach is a dramatic change from the previous two methods. Here a thick, not thinned, Si-ITP wafer with TSVs is used; the MBDs are also not thinned. By using thick singulated die and a thick unrevealed

wafer, one can ensure complete flatness of both the interposer and the MBDs during assembly. As a result of the very fine-pitch MBDs and the high number of interconnects, flatness is of primary importance in order to achieve a high assembly yield.

In step 1 of **Figure 6**, the thick MBDs are attached to a thick unrevealed interposer wafer having TSVs using the IST bonding tool. A benefit of this method is that one can achieve Si-Si flatness, which is ideal for achieving high solder joint assembly yield of the MBDs to the interposer wafer. In step 2, a special capillary underfill capable of flowing under a large die having a small standoff was dispensed on all the dies on the wafer and cured. After this step, the amount of warpage was very small.

In step 3, the MBDs are thinned and a permanent handle wafer structure is attached to provide further rigidity and support. Then the wafer is thinned,

Assembly Flow 2: Substrate Last

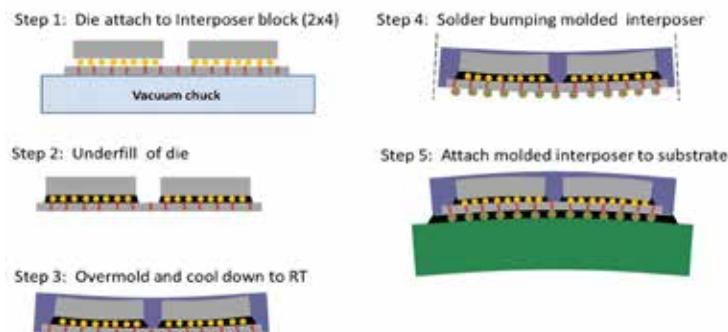


Figure 5: Assembly flow 2: substrate last.

Assembly Flow 3: Permanent Carrier

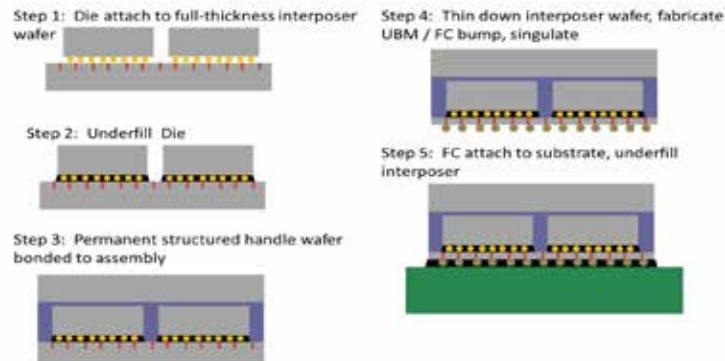


Figure 6: Assembly flow 2: permanent carrier.

TSVs are revealed, and backside under bump metallization (UBM)/solder bumps are deposited, and diced as shown in step 4. The combination of a low CTE handle wafer, MBDs, and Si-ITP make for a low CTE element that can then be attached to the substrate using conventional flip-chip assembly methods. The resulting structure is shown in step 5.

This approach provides an ideal flatness condition for high assembly yield, especially for the micro-bumped die. As cited earlier, an IST bond tool can be used for the die attach, however, this approach is conducive to a mass reflow soldering process. As a result of the thick unrevealed wafer, after the underfill material is dispensed and then cured, there is little warpage.

There are a number of features that make this approach (process flow #3) desirable. First, the thick unrevealed wafer is extremely flat and can easily accommodate a high-density array of MBDs to achieve a high assembly yield. In addition, the handle wafer can provide rigidity and flatness to the Si-layer stack assembly such that during backside grind and TSV reveal, one can maintain the extremely tight flatness control for the TSV reveal. Finally, the stack consisting of handle wafer, MBDs and thin Si-ITP is rigid and flat so it can be easily handled without damaging the thin interposer or jeopardizing the integrity of the micro-bump interconnects.

Discussion

Process flows 1 and 2 show the logical flow for assembly from an OSAT perspective. The process responsibilities and the optimum process flow between the frontend (fab) with the backend (OSAT) is still to be determined [5]. Much of the earlier work on 3D IC assembly of a Si-ITP focused on these two types of approaches. A particularly important issue for both of these flows is the need to use a handle wafer to process the interposer wafer so that it can be effectively removed without causing any damage to the wafer or leaving any type of residue that can affect subsequent processing.

We have evaluated numerous handle wafer materials and bond and debond methods and have determined that consistently achieving high yield is the major technical hurdle to deliver a viable process for HVM. This finding is consistent with others doing similar work [6].

Even if the issue of yield with bond/debond using a handle wafer were

resolved, the handling and maintaining flatness during assembly are still major problems. From this work we have found it to be very difficult to handle thin Si-substrates, whether in wafer form or singulated die. This is a major detractor to achieving high assembly yield. Therefore, a new approach needed to be developed. This is where the process flow 3 leverages a wafer-

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level process flow to provide the best flatness in order to be able to achieve a high assembly yield for the micro-bumped die. The pitch of the micro-bumps will continue to decrease and this will drive the need for Si wafer-level flatness in order to be able to achieve high die assembly yield.

Additionally, process flow 3 does not require any handling of thin die, blocks or wafers. By proper engineering, one can achieve a high density Si-module that is solder bumped as shown in step 4 of process flow 3 in **Figure 6**. This subassembly can then be soldered to the substrate using ordinary flip-chip assembly methods. **Table 1** compares three key attributes that will enable a high-volume assembly process: 1) The need for temporary bond/debond of a handle wafer, 2) thin wafer/die handling, and 3) overall warpage control. As can be seen from this table, flow 3 offers the lowest risk 3D IC packaging solution to achieve a high-yield assembly process.

To make 3D IC a reality, one needs to address the basic packaging issues in order to achieve high yield and a reliable package structure. These are basic packaging concepts that are decades old, but nevertheless still apply to this next-generation of packaging challenges. Basically, the semiconductor fabs have been successful in leveraging wafer-level processes to develop a robust TSV technology. However, the assembly packaging issues outlined in this paper continue to be major roadblocks to achieving a low cost stacking process with TSVs. Low cost

can only be achieved by developing a high-throughput assembly process that does not break thin die and can provide robust assembly yield of the interconnects.

Acknowledgements

The authors would like to acknowledge the help and support of the engineering team at Invensas. Special mention should be given to Ellis Chau, Scott McGrath, Roseann Alatorre, Grant Villavicencio, Bong-Sub Lee, Hala Shaba, Gabe Guevara, and Ron Zhang.

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Biographies

Charles G. Woychik received his PhD in Materials Science and Engineering from Carnegie Mellon U. and is the Senior Director of 3D Portfolio and Market Analysis at Invensas Corporation; email cwoychik@invensas.com

Liang Wang received his PhD in Electrical Engineering from the U. of Texas, MS and BS in Physics from Nanjing U., and is Lead R&D Engineer at Invensas Corporation.

Sitaram Arkalgud received his PhD and MS in Materials Engineering from Rensselaer Polytechnic Institute, BS in Metallurgical Engineering from Karnataka Regional Engineering College, and is Vice President of 3D Portfolio & Technologies at Invensas Corporation.

Guilian Gao received her PhD in Materials Science from the U. of Cambridge, MS in Corrosion and Protection from the U. of Manchester, BS in Materials Science and Engineering from Beihang U., and is a Principal Engineer at Invensas Corporation.

Andrew Cao received his PhD, MS, and BS in Mechanical Engineering from UC Berkeley and is a TSV Process Engineer at Invensas Corporation.

Hong Shen received his PhD in Electrochemistry from the U. of Cincinnati and is a Sr. Processing Engineer at Invensas Corporation.

Laura Mirkarimi received her PhD in Materials Science and Engineering from Northwestern U., BS in Ceramic Engineering from Penn State U., and is VP of Design Analysis and Reliability Engineering at Invensas Corporation.

Eric Tosaya received his MS and BS degrees in Ceramic Engineering from the U. of Washington, and is VP of Memory & MEMS Portfolios & Technologies at Invensas Corporation.

Key Attributes	Flow 1	Flow 2	Flow 3	Comments
Temporary Bond/Debond	Interposer to substrate attach	Microbump die to thin Interposer block attach	Microbump die to thick interposer wafer attach	Additional cost, temperature restrictions, yield, defectivity
	Microbump die to interposer attach	Compression molding of thin interposer block	Carrier-less wafer level backside processing; thin	
	Underfill interposer and microbump die	Block to substrate attach; Dice	Dice, attach to substrate	
Thin wafer/die handling	Yes	Yes	No	Yield, defectivity
Warpage Control				

Table 1: Comparison of three key attributes among process flows 1-3 that enable a high-volume assembly process.

Cost-effective lithography for large area interposers

Warren Flack, Manish Ranjan [*Ultratech, Inc.*]

During the last several years, device manufacturers and foundry customers are paying increased attention to packaging technologies. This shift is driven by the fact that innovative packaging solutions can potentially provide a cost-effective solution for meeting next-generation performance requirements. One such technology that has gained attention is the silicon interposer solution. Customers are now evaluating large area silicon interposer solutions that may exceed the maximum imaging field of step-and-repeat lithography tools. This article discusses the lithographic process used to create a large area interposer on a stepper by the combination of multiple subfield exposures. Overlay metrology structures are used to confirm the relative placement of the subfields to construct the interposer. Routing lines from 1.5 to 4.0 μm in width are evaluated to measure critical dimension (CD) control where the lines cross the subfield boundaries. CD metrology at the bottom and top of the photoresist is performed using a top down CD-SEM (scanning electron microscope) tool. Finally, large area test interposers are patterned using two subfields on a 1X stepper and processed through a Cu electroplating module for detailed characterization.

Introduction

Over the past few decades, IC technology has used shrinking gate dimensions to increase gate switching speed and decreased operating voltage to reduce power consumption. As the demand for improved form factor and superior battery life accelerates, the semiconductor manufacturing supply chain is taking a closer look at back-

end-of-line (BEOL) manufacturing technology. Innovative IC packaging solutions are being developed to meet the needs for consumer electronics. Furthermore, IC packaging now is widely seen as a method to prolong Moore's law [1]. Many companies are evaluating the use of silicon interposers with through-silicon vias (TSVs) to address requirements for higher performance and smaller form factor packages.

Key advantages of silicon interposers include high routing line density, superior electrical and thermal performance, lower power requirements than equivalent single-chip packages through combination of multiple chips on one substrate, and the possibility of integrating passives into the substrate [2,3]. The individual device die can provide numerous functions including memory, logic, analog and MEMS (micro-electromechanical systems). To achieve high bandwidth between individual die on the interposer requires fine pitch routing lines. For advanced wide I/O applications, it is anticipated that interconnect line widths of less than 2 μm will be needed.

A step-and-repeat (stepper) lithography system provides the necessary patterning capability for high-resolution devices with zero printable defects. However, for some designs the interposer area can exceed the maximum stepper field size.

Large interposer fabrication

The need for patterning large area devices with stepper lithography is not new. Superchips from the very high-speed integrated circuit (VHSIC) program were constructed using macrocells [4]. Each macrocell was

a self-contained integrated circuit placed in a single stepper field and only interconnect layout rules were used at crossing field boundaries [5, 6]. A more recent demand for large area devices is for infrared focal plane arrays used for aerospace applications [7]. The image sensor pixels are contained within a stepper field and only interconnect routing is allowed to cross stepper field boundaries similar to superchips.

Because interposers are designed to interconnect single chip devices, the field stitching considerations are similar to focal plane arrays and superchips. A large area interposer can be fabricated by splitting the interposer design into multiple sections where each section is smaller than the maximum field size of the step-and-repeat lithography system.

Figure 1 shows a 50 by 50mm interposer split into a top half (purple) and a bottom half (pink). This two subfield approach works for a lithography system with a field size greater than 50 by 25mm.

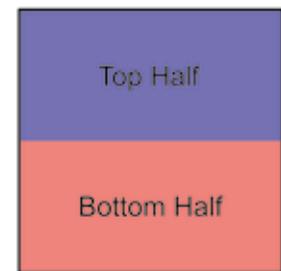


Figure 1: The large area interposer design is split into top and bottom halves for stepper lithography layout.

The reticle for the lithography system is then fabricated for each section of the interposer. **Figure 2** shows the layout for a 1x reticle that supports placing multiple fields on one plate. The top half of the interposer (purple) is field 1 on the reticle and the bottom half of the interposer (pink) is field 2 on the reticle. This reticle can now be used on

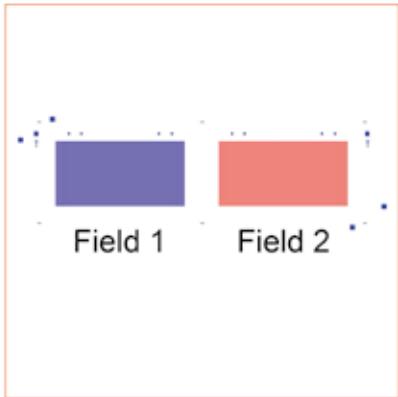


Figure 2: 1X reticle layout for an interposer split into two fields. The reticle size is 150 by 150mm.

the lithography stepper to image the full interposer on the wafer by alternating the patterning of rows of field 1 (purple) and field 2 (pink) as shown in **Figure 3**. The interposer routing lines that cross the boundary of the top half and bottom half of the interposer are stitched by allowing a small amount of Y overlap between the two fields. This same approach can be used to fabricate even larger area interposers by having additional reticle fields stitched in both the X and Y direction.

Experimental methods

Exposures are performed on an Ultratech AP300 advanced packaging stepper with a 0.16 NA Wynne-Dyson lens [8]. This catadioptric optical system design permits the use of broadband illumination from a mercury arc lamp, and the system used in this study has a capability to select i-line, g-line or ghi-line wavelengths. The large area

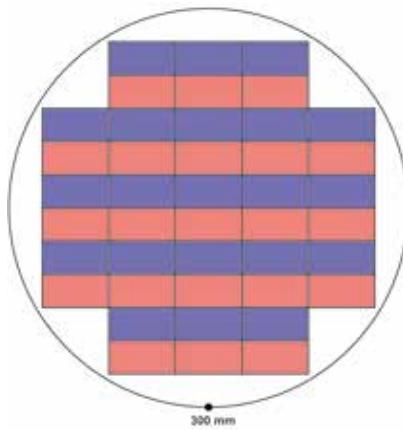


Figure 3: 300mm wafer layout with 21 interposers. The interposer size for this case is 50 by 50mm.

interposer evaluated for this study is 44.0 by 44.0mm with interconnect lines covering the whole chip area. Because the exposure field of the 1X stepper used in this study is 44x26.7mm, the interposer design is split in two fields each with a size of 44 by 22mm similar to **Figures 1** and **2**. The reticle set was designed to include test structures that provide evaluation of overlay and CD performance at the field boundaries. For this case, only a Y stitch is required.

Multiple test structures were created to evaluate reticle field stitching performance. **Figure 4** shows a line

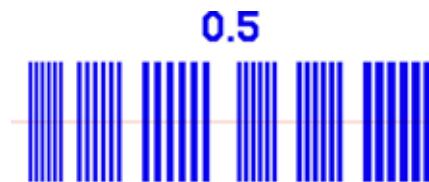


Figure 4: CD performance features with varying pitches. The red line indicates the stitch between field 1 and field 2. The 0.5 above the structure indicates the Y overlap in microns.

integrity structure with six sets of line and space patterns with varying CD and pitch. The patterns above the red stitch line are on reticle field one and the patterns below the red stitch line are on reticle field two. The CD of the test structures vary from 1.5 μ m line and space on the left side to as large as 4.0 μ m line and 2.0 μ m space on the right. The 0.5 in blue above the pattern indicates that the top and bottom half have a stitch overlap in Y of +0.5 μ m between the fields. Additional line integrity structures were created with field stitch overlaps varying from as small as -0.5 μ m to as large as +10.0 μ m.

An electrical test structure was created to evaluate the field stitch performance of electroplated Cu lines. **Figure 5** shows a serpentine/comb four point probe structure. The pattern above the red stitch line is on reticle field one and the pattern below the red stitch line is on reticle field two. The test structures range from 1.5 μ m line and space to 3.0 μ m line and space. The field overlap in Y was +0.5 μ m.

The lithographic process was then evaluated on Cu seed 200mm wafers

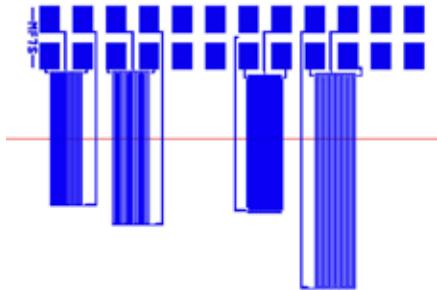


Figure 5: Serpentine/comb structure. The red line indicates the stitch between field 1 and field 2.

using actual device process conditions. The Cu interconnect lines are fabricated using a semi-additive electroplating technique as shown in **Figure 6**. In this technique, a Cu seed layer consisting of 30nm TiW and 50nm of Cu is deposited onto the wafer, which acts as the current distributing layer during the electroplating process (**Figure 6a**). Next, a 3.5 μ m-thick positive photoresist is coated on the wafer and the area to be electroplated is opened to the Cu seed via the lithography process (**Figure 6b**). The resist is descummed and then 2.5 μ m of Cu is electroplated onto the wafer (**Figure 6c**). The photoresist is then stripped off of the wafer (**Figure 6d**). The Cu seed is wet etched followed by wet etch of the TiW to create the final structure (**Figure 6e**).

This study employed a chemically-amplified positive resist that is based on a phenolic polymer. This resist can produce vertical sidewalls with minimal footing on Cu substrates, and is capable of resolving submicron

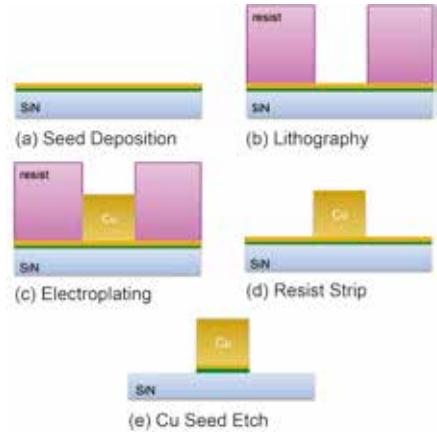


Figure 6: Wafer process flow to fabricate Cu interconnect lines using a semi-additive electroplating technique: a) seed deposition, b) lithography, c) electroplating, d) resist strip, and e) Cu seed etch.

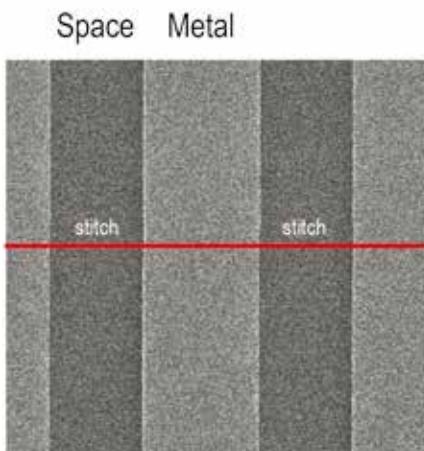


Figure 7: Stitched, plated metal lines at 3 μm pitch. The field Y overlap is 0.5 μm . The red line is the field stitch location.

patterns in 3.5 μm thick resist using i-line lithography. The resist was optimized to produce a 1.5 μm line and space pitch on Cu seed wafers. The exposure latitude of 1.5 μm lines and spaces measured on a 0.16 NA stepper was 18% with a $\pm 10\%$ CD criterion. For this study, the resist was exposed at i-line using a nominal exposure dose of 140mJ/cm².

The 1X stepper offers multiple alignment options, and for this study both blindstep and zero layer alignment were evaluated. Blindstep uses the XY stage encoder along with a previously calibrated transform to accurately print a multiple field array. The zero layer technique requires a dedicated array of field alignment targets to be printed on the wafer. These targets are used to align and stitch two adjacent reticle fields together to optimize overlay. Overlay metrology was performed using

microscope measurements and the self-metrology feature on the 1X stepper.

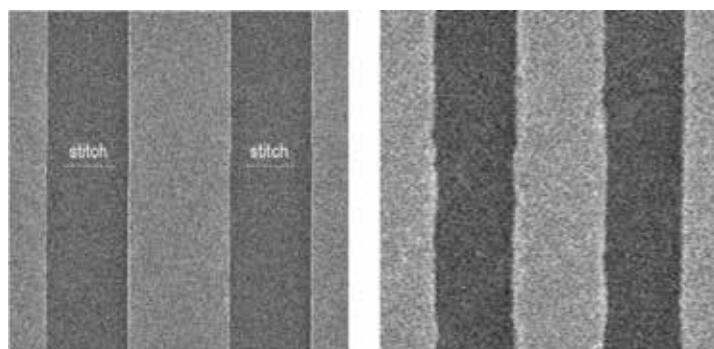
Results

Sample interposer structures were stitched together using two lithography fields. The resist line at the stitch area was evaluated for different pitches and overlaps. **Figure 7** shows a top down SEM image of stitched dense plated lines with 3 μm pitch. The plated lines form within the spaces of the resist pattern. This view shows an optimized stitch with a 0.5 μm Y overlap and the actual stitch location is difficult to discern. A red horizontal line is added to the stitch location. Based on these experimental results, a 0.5 μm Y overlap is used in the rest of this study.

The steps following resist development also influence the shape and size of the Cu lines. Both descum and the seed removal steps need to be optimized for effective control of CD. Descum is essential for uniform plating results because it reduces the surface tension of the photoresist to allow proper wetting to the Cu seed. However, this process consumes photoresist and the CD of the resist opening increases as a result.

The seed etch can also have a large impact on the shape and size of the Cu lines. During wet etching of the Cu seed, the electroplated structures are also etched with a reduction of CD as a result as shown in **Figure 8**. To reduce this effect, the Cu seed thickness needs to be as thin

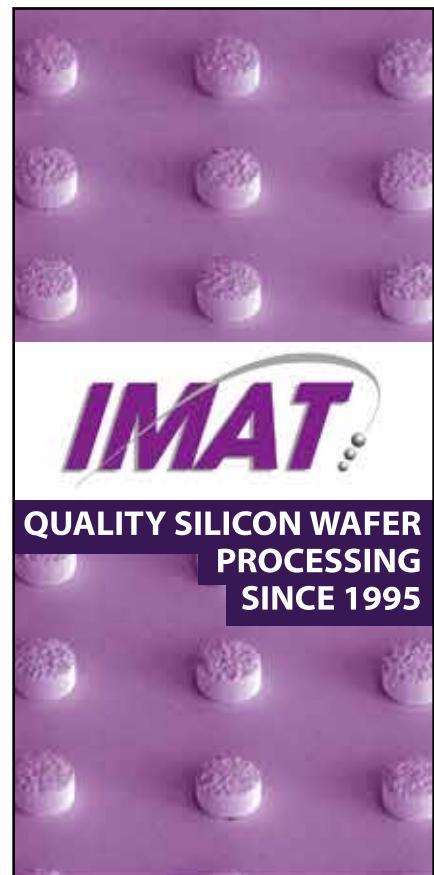
as possible in order to minimize the etching time. **Figure 9** shows a top down view of a Cu electroplated serpentine/comb structure with a 3 μm pitch. Visual inspection reveals no



(a) Before Cu seed etch

(b) After Cu seed etch

Figure 8: Top down view of Cu plated metal lines a) before Cu seed etch, and b) after seed etch. Both cases are for 3 μm pitch, line and space pattern.



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Figure 9: Cu electroplated serpentine/comb structure with a 3 μ m pitch. Visual inspection reveals no line breaks or shorts in the structure.

line breaks or shorts in any of the serpentine/comb structures.

Summary

Extending device performance increasingly relies on advancements in back-end technologies such as the use of very large interposer designs with aggressive interconnect density requirements. A stepper system provides the necessary patterning capability

for high-resolution devices with zero printable defects. To produce large area interposers, however, requires stitching of stepper subfields.

This study experimentally investigated patterning copper lines with lateral dimensions as small as 1.5 μ m line/space in a vertically stitched 44 by 44mm device. An optimized stitch was obtained using a 0.5 μ m Y overlap and the actual stitch location is difficult to discern.

This work demonstrates that stitching of subfields for interposer interconnects can be achieved by leveraging existing stepper lithography and process technologies.

Acknowledgment

Elements of this article appeared in the paper Large Area Interposer Lithography originally published at the 64th Electronic Components Technology Conference and is copyrighted by the IEEE.

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Biographies

Warren Flack received his BS and MS degrees in Chemical Engineering from the Georgia Institute of Technology and his PhD in Chemical Engineering from the U. of California at Berkeley and is the Senior Director of Global Applications at Ultratech, Inc.; email wflack@ultratech.com

Manish Ranjan received his MS degree in Industrial Engineering from the State U. of New York at Binghamton. He also received an MBA from The Wharton School of Business in Philadelphia and is the Vice President of Product Marketing for the Advanced Packaging and HBLED market segment at Ultratech, Inc.

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3D inspection challenges of copper pillar bumps

By Russ Dudley [Rudolph Technologies, Inc.]

Market demand for more functionality in smaller devices continues to drive rapid development and deployment of three-dimensional (3D) integration technologies that interconnect vertically stacked chips. These approaches often require hundreds of thousands of connections per die. Copper (Cu) pillar micro bumps have been widely adopted to form these connections because their small size and pitch can provide the required interconnect density. Inspecting these bumps throughout the process is critical because failure after chip-to-chip or chip-to-wafer bonding is very costly. C4 bumps have been the enabling interconnect technology in flip-chip wafers for some time. More recently, many manufacturers have moved to pillar bumps, typically copper, which are usually surmounted by a solder cap. The use of pillar bumps is growing rapidly. They offer small pitch flexibility, higher I/O counts, better standoff and improved heat dissipation. Typical pillar bumps in today's production are as small as 30 μm high and 20-30 μm in diameter, with 10 μm and 5 μm diameters in development. This article describes the use of a configurable platform to meet the 2D and 3D metrology and inspection requirements of Cu pillar bump processes in advanced packaging applications. The ability to configure sensors allows engineers to optimize system performance for the differing requirements of process development, ramp and high-volume production. The use of a common platform minimizes the training and support burden across the process.

Successful micro bump inspection and metrology must meet a number of challenging requirements. The system must provide sub-micron precision in measurements of height, coplanarity, position, diameter and volume. The sensor must also be able to handle finely pitched bump arrays where the space between bumps is typically equal to bump diameter.

In addition to measuring the bumps themselves, the system must be capable of measuring the thickness of layered materials surrounding the bumps at various stages in the bump fabrication process. Inspection capabilities must include the ability to detect bump defects, including missing bumps, bridged bumps and misshapen bumps. With manufacturers' roadmaps indicating more than 100,000 bumps per die and more than 60 million bumps per wafer, the measurement system must be able to process and store large amounts of data quickly and effectively. Finally, the system must provide both 2D and 3D inspection capabilities while striking an acceptable balance between precision and throughput.

Bump Inspection and metrology requirements

Bumping processes are a critical component of most 3D integration (3DI) schemes. Bumps provide the vertical reach required to make connections through the adhesive that bonds stacked chips together. A wafer with through-silicon vias (TSVs) may have Cu pillar bumps on one side and Cu nails (copper protrusion) on the backside. 3DI bumping processes are largely extensions of processes long used for solder bumps and flip-chips. Compared to flip-chip bumps, 3DI bumps are smaller, more closely spaced and far

more numerous. Pillar bumps incorporate a lithographically-defined base, the pillar, which is usually composed of copper, typically with a solder cap on top.

As shown in **Figure 1**, bump metrology requirements include thickness measurements of a polymer layer as well as step height measurements for the Cu pillar to the polymer layer and wafer surface. The conventional approach to thickness measurements is a spectroscopic sensor such as a reflectometer. These sensors can differentiate thin layers because the resolution is only dependent on the spectral width of the source, and is independent of the objective lens and spot size. A reflectometer, however, cannot measure step height to an opaque material such as metal. Several conventional methods exist for non-contact measurement of step heights, such as various confocal sensors, triangulation sensors and scanning white light interferometry. These sensors typically have difficulty differentiating between reflections from the top and bottom surfaces of a layer, that is, layer thickness. This limitation stems from the depth of focus of the objective, which in turn depends on the numerical aperture (NA) of the objective. Thus, in contrast to the reflectometer, sensor performance is highly dependent on the objective lens.

The single platform described here (NSX 320 System) includes 3D metrology performed using a proprietary

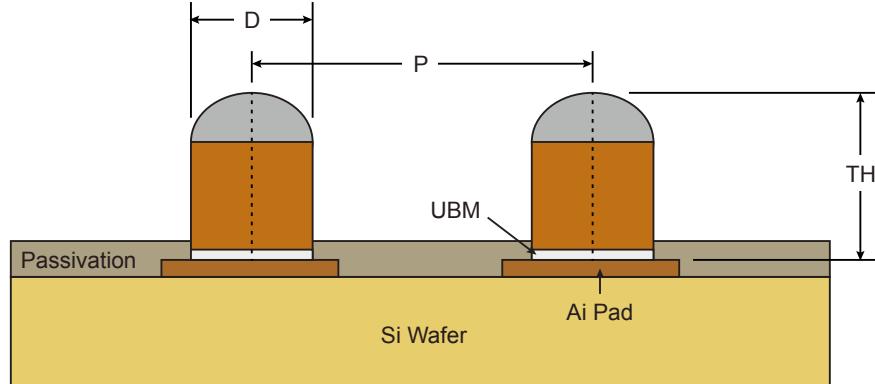


Figure 1: Cross section view of a Cu pillar highlighting critical metrology requirements.

interferometric sensor technology that can measure the height of the post and the thickness of the surrounding polymer at the same time to optimize the measurement performance and system throughput. The new sensor technology combines traits of reflectometry and interferometry to provide a complete solution for both direct thickness measurements of transparent layers, as well as step height measurements. In both cases, multiple layer interfaces can be resolved to avoid the confusion created when measuring step height from a metal to a transparent layer. The platform also provides the ability to inspect for surface defects, irregular posts, missing posts, and a variety of other inspections performed on bumped wafers or substrates.

Single platform inspection and metrology

Traditionally, systems designed for metrology have significant differences from systems designed for inspection, which preclude common use of a shared design approach. For example, metrology systems typically require greater vibration isolation than inspection systems, especially if the

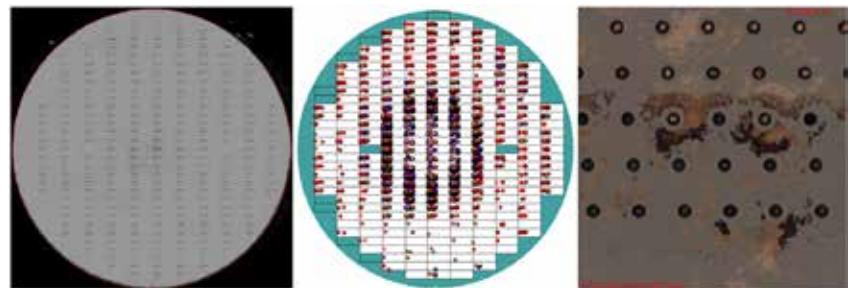


Figure 2: High-speed inspection results provide wafer defect map and images for review.

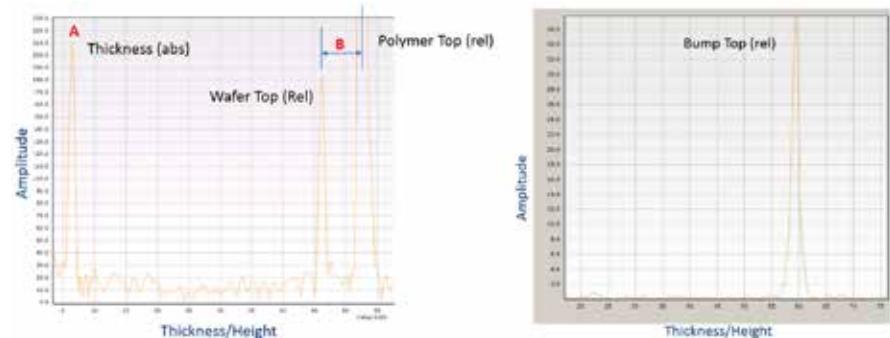
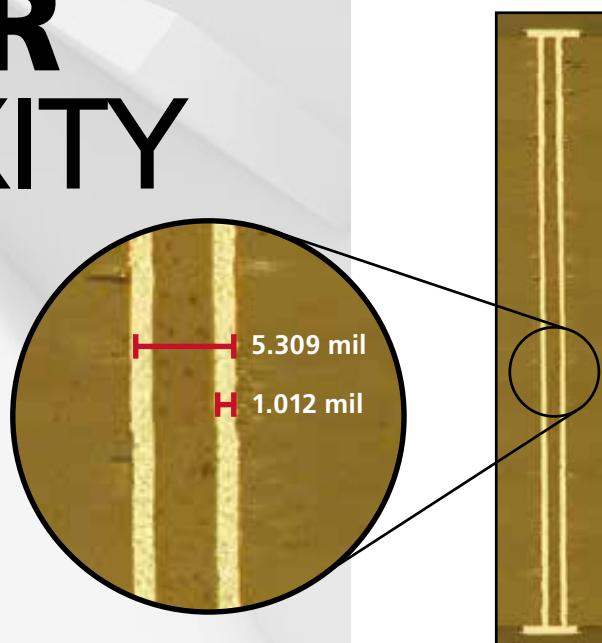


Figure 3: When the sensor is measuring the polymer area (left), several measurement peaks are produced, corresponding to the thickness of the polymer A, and B, the distance to the upper and lower surfaces of the polymer. On the opaque bump there is only a single peak (right).

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metrology includes interferometry. As another example, inspection systems require high speed stages and optics because they must be able to cover the full wafer, whereas metrology systems are usually used in a sampling mode that measures only a limited number of die.

Inspection and metrology systems, however, do share many requirements, and the common components tend to be the most expensive. Both require wafer handling robotics, factory interface software, clean room compatibility and, when access to both front and backside is needed, a wafer inversion module. Sharing one set of these expensive components and adding the capabilities required to accommodate both inspection and metrology can deliver significant economic advantage.

The single platform used in this work is a well-established, fully-automated platform with a wafer chuck, high-speed calibrated x-y table and a clean room compatible enclosure. The measurement table is mechanically isolated from vibration and a large bridge and vertical z-stage can accommodate several optical sensors. The platform is equally capable of sample measurement and high-speed, full-wafer inspection as highlighted in **Figure 2**.

The specialized high-speed optics and the 3D optical sensors are mounted side-by-side. The spatial offset between the objective lenses for each is calibrated so that any point in the microscope's field of view can be moved under any of the 3D sensors with a positioning accuracy of approximately a micrometer.

The platform is available in standard configurations for use in various advanced packaging and 3DI applications, including a basic wafer-level packaging configuration, an advanced wafer-level packaging configuration, and a TSV configuration.

Cu pillar measurements

The height of the Cu pillar bump above the wafer surface and above the surface of the surrounding polyimide film are critical measurements. The interferometric sensor is capable of making these measurements simultaneously. The sensor measures the thickness of the transparent film and the distance from the objective to the top of the bump along with the top and bottom of the adjacent transparent film. The distance measurements thus permit the calculation of the step height where the film meets the bump.

Figures 3 and **4** illustrate measurements of Cu pillar height and polymer layer thickness.

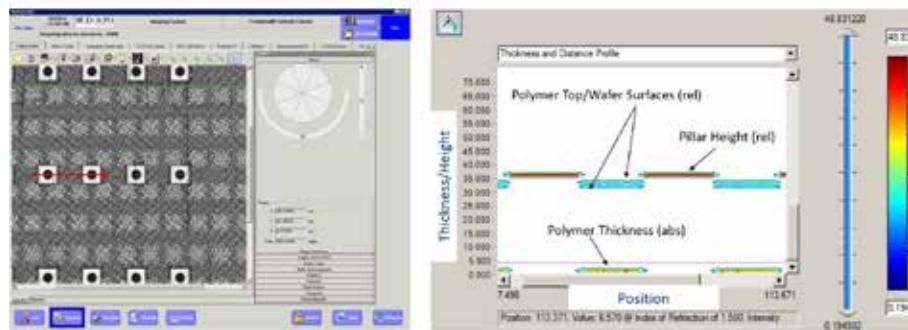


Figure 4: The image on the left shows the location of the line scanned. The plot on the right shows the calculated values for thickness and height along that line.

Loc	Run										STD	3 STD
	1	2	3	4	5	6	7	8	9	10		
1	37.504	37.540	37.551	37.545	37.544	37.558	37.543	37.555	37.539	37.537	0.015	0.045
2	37.055	37.038	37.108	37.058	37.092	37.045	37.073	37.060	37.115	37.044	0.027	0.082
3	36.626	36.594	36.575	36.574	36.569	36.547	36.596	36.618	36.641	36.602	0.029	0.087
4	36.753	36.705	36.726	36.707	36.735	36.784	36.702	36.712	36.725	36.728	0.025	0.076
5	37.758	37.786	37.764	37.782	37.807	37.786	37.730	37.790	37.812	37.816	0.026	0.079
6	36.587	36.620	36.621	36.604	36.566	36.641	36.572	36.623	36.598	36.608	0.024	0.071
7	36.752	36.736	36.758	36.723	36.748	36.752	36.731	36.780	36.719	36.717	0.020	0.060
8	36.905	36.919	36.914	36.926	36.937	36.962	36.937	36.947	36.945	36.910	0.018	0.055
9	37.388	37.374	37.375	37.405	37.332	37.352	37.369	37.388	37.357	37.345	0.022	0.066
10	37.518	37.536	37.502	37.494	37.502	37.475	37.515	37.490	37.502	37.527	0.018	0.055

Table 1: Bump height repeatability.

Loc	Run										STD	3 STD
	1	2	3	4	5	6	7	8	9	10		
1	10.462	10.475	10.468	10.471	10.472	10.468	10.468	10.470	10.469	10.475	0.004	0.012
2	10.448	10.443	10.445	10.445	10.440	10.446	10.445	10.448	10.448	10.444	0.003	0.008
3	10.451	10.450	10.449	10.446	10.447	10.449	10.452	10.449	10.447	10.444	0.002	0.007
4	10.445	10.447	10.446	10.445	10.443	10.444	10.446	10.446	10.450	10.448	0.002	0.006
5	10.497	10.499	10.492	10.498	10.495	10.496	10.486	10.491	10.489	10.492	0.004	0.012
6	10.471	10.471	10.465	10.472	10.477	10.469	10.467	10.468	10.460	10.473	0.005	0.014
7	10.467	10.477	10.473	10.476	10.474	10.475	10.477	10.468	10.469	10.467	0.004	0.012
8	10.467	10.466	10.473	10.470	10.469	10.474	10.470	10.475	10.472	10.471	0.003	0.009
9	10.431	10.426	10.434	10.425	10.426	10.436	10.435	10.436	10.435	10.432	0.005	0.014
10	10.458	10.446	10.451	10.449	10.447	10.453	10.450	10.449	10.450	10.453	0.003	0.010

Table 2: Polymer thickness repeatability.

The plots in **Figure 3** show peaks derived from the interferometric data at a single point on the polymer layer (left) and on the bump (right), with thickness/height on the x-axis and signal amplitude on the y-axis. Three peaks are visible in the left plot. Peak A is a direct measurement of the layer thickness.

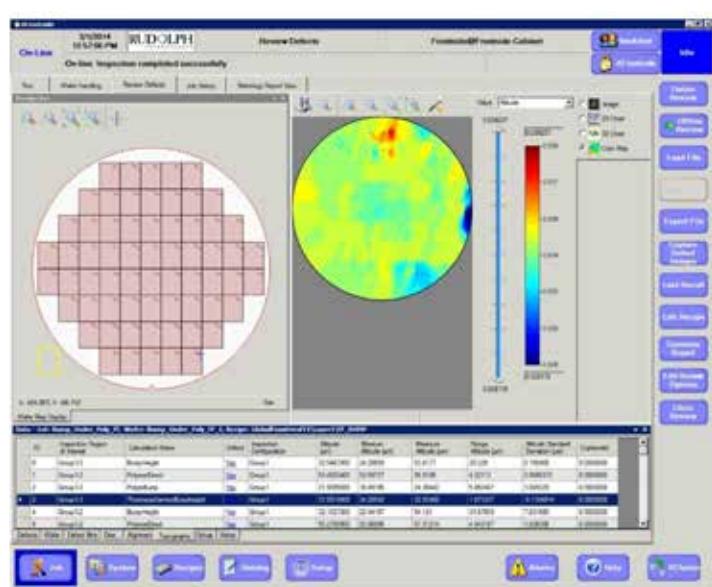


Figure 5: Full wafer plot of bump height.

(approximately 7 μm). The two peaks to the right, separated by distance B, indicate the distance from the objective to the top and bottom of the layer. Note that A = B. The plot on the right shows the single peak acquired when the top of the opaque bump is measured. The image on the left side of **Figure 4** shows the location of a scan over bumps. The plot on the right shows the corresponding derived measurements, with thickness/height on the y-axis and location on the x-axis. The measurement system includes software to automatically interpret the measurement peaks to produce the desired results. **Figure 4** is a graphical representation of the final result after software interpretation.

To qualify the performance and prove the utility of the measurements produced by the interferometric sensor, we evaluated the repeatability of the polymer thickness and Cu pillar height measurements. The results are shown in **Tables 1** and **2**.

Figure 5 shows bump height data plotted for the full wafer. With appropriate sensors the system is capable of plotting full wafer maps for shape, bow, warp, total thickness variation (TTV), residual Si thickness, adhesive layer thickness, and more.

Summary

The system used for the work described builds on a well-established platform to combine fast, full wafer defect inspection with accurate 2D/3D metrology. In the case of Cu pillar bumps, it provides simultaneous measurement of bump height and polyimide thickness. Thickness and distance measurements are made through a single optical system at exactly the same position with no confusion by multiple film surfaces. Flexible setup with comprehensive recipes for all aspects of local and full wafer measurements makes the system easy to use. All data may be passed in Rudolph Results Files (RRF) to yield management software for defect classification, trend analysis and root cause identification.

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Biographies

Russ Dudley is a graduate of DeVry Institute of Technology, and attended the AEA Stanford Executive Business Program; he is the Manager of 3D Business Development at Rudolph Technologies, Inc.; email Russ.dudley@rudolphtech.com

Reza Asgari received his post graduate degree in Mechanical Engineering, with emphasis on computer vision systems, from Louisiana State U. and is a Product Manager at Rudolph Technologies, Inc.



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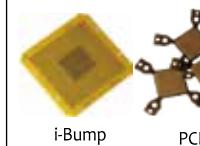
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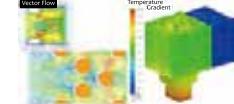
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MARKET UPDATE



Keeping pace with the packaging evolution

By Fred Taber [BiTS Workshop]

I'm a 'test guy.' I've been one my entire career. In earlier times I was all about test systems and test programs, while these days, most of my colleagues know me from my more recent work on test consumables or "personalization" tooling for wafer test, package test and burn-in, such as wafer probes and test and burn-in sockets. For the past 15 years, I've also been the General Chairman of the Burn-in & Test Strategies Workshop (BiTS). Indeed, a career in test offers no shortage of directions to pursue, or from which to switch back and forth.

This past March saw the 15th anniversary of the BiTS Workshop – a milestone that was a fitting time for another career switch. Beginning with BiTS 2015, Ira Feldman, of Feldman Engineering Corp., will take over the BiTS helm. Under Ira's leadership, BiTS will be in great hands to embark on the next 15 years.

Aside from managing the straight-ahead routine of dealing with the multitude of day-to-day details leading up to each year's event, more so, those 15 years with BiTS taught me much about test and burn-in of packaged ICs. In that sense, it encouraged reflection about industry events and their technical program content to assure that BiTS offered what attendees wanted and needed to help them in their day-to-day jobs.

Similar to the many directions one can take with a career in test, when seeking to build test skills through industry events, there's an abundance of test-related conferences and workshops from which to choose. By my rough count, just those events sponsored by the Test Technology Technical Council of the IEEE's Computer Society, number over 30. Plus, along with BiTS, there are others outside of that sphere; among them are the privately sponsored Silicon Valley Test Workshop (SVTest) and the Semiconductor Wafer Test Workshop (SWTW), sponsored by the IEEE's Components, Packaging and

Manufacturing Technology (CPMT) Society. Complementing the technical program, some events include exhibits of products and services.

Though all are called 'test' conferences or workshops, 'test' encompasses such a broad range of intensely focused disciplines that no one event can possibly capture all of them in its technical program. Among that group of test conferences/workshops are a few large events that attempt to cover a broad spectrum of test topics, yet perhaps there will be one or two papers on a niche topic of interest and, commensurately, a few suitable exhibitors. That is hardly sufficient to justify the expense of attending (or exhibiting at) a broad-based event if you are involved in certain specific test niches. In the other direction, narrowing the topic niche too much, not only attracts a smaller base of authors, attendees and exhibitors, but it weakens the technical program by leaving little room for associated subjects.

Striking the right balance, 'test' niches are best served by topic-centric events that incorporate other sphere of influence topics, like the BiTS Workshop does (of course you knew I'd say that!), among others.

Those who are familiar with BiTS know that sockets for package test and burn-in are the legacy topic focus; in fact the original name of the event was Burn-in & Test Socket Workshop. It remains a core topic today, yet with the rapidly growing market adoption of advanced packaging technologies such as wafer-level packaging (WLP) and others, traditional methods of burn-in and test have been challenged. To reflect the objective to continue bringing attendees the latest burn-in and test strategies for next-generation advanced packages (such as wafer-level chip-scale packaging, or WLCSP, and fan-out wafer-level packaging, or WLP), BiTS was rebranded the 'Burn-in & Test Strategies Workshop' in 2011. This was more than a name change. It demonstrated undertaking greater coverage of those

sphere of influence topic areas noted earlier. This meant more coverage of advanced packaging trends and tooling, plus some basic test and burn-in methodology subjects, among others.

The BiTS 2014 program incorporated the core topic plus sphere of influence approach with three renowned speakers (Keynote Speaker: Simon McElrea of Invensas, Distinguished Speaker: Brandon Prior of Prismark Partners and Honored Speaker: E. Jan Vardaman of TechSearch International) who addressed advanced packaging trends in each of their talks. Also featured were two 'Test 101' tutorials taught by leading test experts (Peter Ehlig and Jeffrey Roehr of Texas Instruments) and a sold-out EXPO that featured more than 50 exhibitors representing products and services from up and down the package test and burn-in supply chain.

One example of BiTS covering trends in test and burn-in tooling for advanced packaging is electrical contacting of WLP for final testing. WLP includes WLCSP, and fan-out wafer-level packaging (FOWLP).

For the BiTS Workshop, addressing test tooling for advanced packaging technologies, such as WLCSP and FOWLP, may appear to stray from its traditional topic track of socketing for final test and burn-in of conventional packaged electronics, because the final testing is performed at the wafer-level on a prober, not on a traditional singulated package. Yet, as the details unfold, the fit for this topic in the BiTS program, both as a core and a sphere of influence topic, becomes apparent: keeping pace with wafer (final) test of these advanced packaging technologies requires the very same contacting technologies employed by sockets (and regularly discussed at BiTS), but repackaged to appear as a wafer probe and built on a probe card to integrate into the prober.

Final testing of WLCSP is performed on die within an actual silicon wafer where the electrical contacts (interconnects) are

within the chip perimeter. For FOWLP, final testing is done on an artificial wafer (or other format) where singulated die are reconstituted and additional electrical contacts are formulated outside of the chip perimeter, thus achieving a greater number of interconnects.

This testing is done at the wafer level using conventional test systems and wafer probers. No different than the usual wafer probing process. What's unique from conventional wafer probing, is that the 'probe card' utilizes electrical contacts that are common in package test and burn-in: spring pins. **Figure 1** is an example of a Kelvin spring pin.

With conventional wafers, less rigorous wafer testing sorts good die from bad die on a wafer; the good die are packaged and then, using sockets, a more thorough package test and reliability screening is performed. With WLP, the chip is already packaged, so the more thorough package test programs and reliability screening are applied at the wafer level, then the individual die are singulated, ready for further assembly.

Traditional wafer probing employs any of a number of wafer probe technologies to contact the chip I/Os. There are many

impressive wafer probe contact technologies on the market—everything from traditional cantilever probes to variations of vertical probes. Likewise, fabrication techniques range from wire-forming and bending, to MEMS semiconductor processes. Wafer probes may simply contact a single die, to handling very high parallelism by contacting every chip on a 300mm wafer.

Nonetheless, wafer-level packages (WLP) have contacting demands that make these wafer probe technologies unsuitable for use in WLP testing. While

spring pins, a primary socket contact technology, already proven for traditional package test, offers a virtual ready-made solution at the interconnect-to-interconnect pitch (300µm to 400µm) required. Spring pin attributes include: 1) Greater compliance to handle larger interconnect height variations (shortest interconnect height to tallest interconnect height); 2) High electrical performance to perform the gamut of functional and parametric tests; 3) Higher force wipe on harder solder balls assures low contact resistance; 4) Kelvin contacting for better power management; and 5) Multi-device under test (DUT) – up to 16 die in parallel; and 5) Multi-device under test (DUT) – up to 16 die in parallel, contacting up to 2000 interconnects.

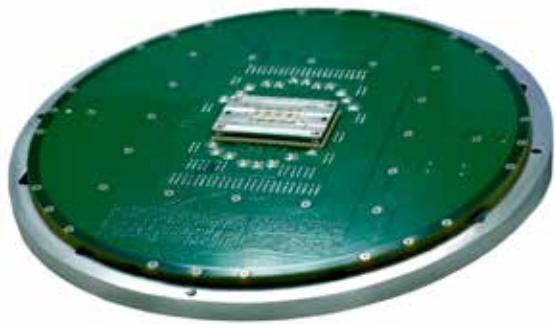
Additionally, spring pins typically offer a lower cost solution, easier maintenance and a shorter lead-time. Space transformers are frequently unnecessary. A spring pin-based probe head mounted on a probe card printed circuit board (PCB) results in a probe card that smoothly integrates into the wafer test infrastructure. Unlike a socket, the housing that contains the spring pins is simplified with the elimination of an alignment feature: to align the spring pins to the die's interconnects, the prober's pin to pad alignment feature is used (the vision system on probers now recognize the crown and other tip profiles on the spring pins). For online cleaning, the regular cleaning station on the prober is used. Offline, standard probe metrology tooling can be utilized to perform required measurements; tip positional adjustments are unnecessary with spring pins.

As illustrated with WLCSP and FOWLP, the BiTS Workshop is committed to keeping pace with the packaging evolution by continuing to bring what's NOW & NEXT to its attendees. Visit the BiTS Workshop website at www.bitsworkshop.org for more information about BiTS and a robust archive of 15 years' worth of presentations, including a Premium archive (presentations with synchronized audio) for BiTS 2013 and 2014.

The BiTS 2015 calendar has the Call for Presentations opening in August; Exhibitor registration begins in August, while attendee



Figure 1: 0.3mm Kelvin spring pin.
SOURCE: Multitest



A WLCSP probe card. SOURCE: Smiths Connectors | Interconnect Devices, Inc.



High pin count Multi-DUT (x4) WLCSP probe head. SOURCE: Smiths Connectors | Interconnect Devices, Inc.



Low pin count Multi-DUT (x4) WLCSP probe head. SOURCE: Multitest

registration will start in December. Save the date: BiTS 2015 is March 15-18, 2015.

Biography

Fred Taber received his BSEE from Southeastern Massachusetts U. (now the U. of Massachusetts – Dartmouth) and was a Senior Engineering Manager in the Worldwide Test organization at IBM. He is also a founder of the BiTS Workshop and has served as its General Chairman since its founding in 2000 through BiTS 2014; email taber@bitsworkshop.org

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Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to +260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to +125°C FQ < 30 GHz CF & CR = CM
Andon Electronics Corporation 4 Court Drive Lincoln, RI 02865 Tel: +1-401-333-0388 www.andonelect.com	P	BA, LA, SM, TH	CP > 1.0 mm CL & FQ = CM OT = -65°C to +240°C CF = CM CR < 1.0 A
AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 4 Merrill Industrial Drive Hampton Beach, NH 03842 Tel: +1-603-926-2517 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
Aries Electronics, Inc. 2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to 155°C CL, FQ, CF & CR = CM
BeCe Pte. Ltd. Block 1, Yishun Street 23, # 01-09 Singapore 768441 Tel: +65-6257-2930 www.bece.com.sg	T	BA, LA	CP = CM CL = CM OT = CM FQ = CM CF = CM CR = CM
Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
C2WIDE Co.,Ltd Rm705,84,GaSanDigital 1Ro, GeumCheonGu Seoul, Korea(153797) Tel: +822-364-1878 www.c2wide.com	B, D, P, T	BA, LA	CP = 0.4/0.5/0.65/0.8/1.0mm CL = 300,000 OT = -55° to 130°C FQ > -0.63dB@20GHz CF = 25~35g CR = 3A Continous
Cascade Microtech, Inc. 2430 NW 206th Avenue Beaverton, OR 97006 Tel: +1-503-601-1000 www.cascademicrotech.com	D, P, T	BA, LA, SM	P > (0.35 - 0.8) mm CL > (50 - 300,000)x OT = -45°C to +175°C FQ < (9.4 - 40.0) GHz CF < (15 - 55) g CR < (1.0 - 4.0) A

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Centipede Systems Inc. 41 Daggett Drive San Jose, CA 95134 Tel: +1-408-321-8201 www.centipedesystems.com	T	BA, LA, SM	CP > 0.3 mm CL > 500,000x OT < +160°C FQ = CM CF = CM CR < 2.0 A @ 150°C	
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com		B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A
Custom Interconnects 2055 S. Raritan Street, Unit A Denver, CO 80223 Tel: +1-303-934-6600 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz CF = CM CR < 5.0 A	
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com		B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Enplas Tesco, Inc. 765 N. Mary Avenue Sunnyvale, CA 94085 Tel: +1-408-749-8124 www.enplas-ets.com	B, D, T	BA, LA, SM	CP > 0.4 mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14 - 35) g CR < (0.5 - 1.0) A	
Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3 mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30 GHz @ -1dB CF < (15 - 40) g CR < (0.5 - 1.0) A	
E-tec Interconnect Ltd. Industrial Zone C Forel (Lavaux) CH-1072, Switzerland		D, P	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (100 - 10,000)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40 g CR < (0.5 - 3.0) A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4 mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40 GHz @ CM CF < (10 - 12) g CR = CM	
Gold Technologies, Inc. 2360-F Qume Drive San Jose, CA 95131 Tel: +1-408-321-9568 www.goldtec.com	B, D, T	CM	CP > (0.4 - 0.5) mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6 - 16.0) GHz @ -1dB CF & CR = CM	
High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > (0.5 - 0.8) mm CL > (50k - 250k)x FQ < (4.4 - 10) GHz @ -1dB CF < (30 - 50) g OT & CR = CM	
High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5 mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0 A	

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HSIO Technologies, LLC. 13300 67th Avenue North Maple Grove, MN 55311 Tel: 763-447-6260 www.hsiotech.com	D, P, T	BA, BD, LA, SM	CP = ≥ 0.3 mm CL = Product Dependant OT = -55° to 155°C FQ > 15-40GHz @ -1dB CF = Product Dependant CR = 2-4A
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	P	BA, LA	CP > 0.8 mm CR < 10 A CL, OT, FQ, CF = CM
Ironwood Electronics 11351 Rupp Drive Burnsville, MN 55337 Tel: +1-952-229-8200 www.ironwoodelectronics.com	 B, D, T	BA, LA, SM	CP > (0.25 - 0.4) mm CL > (2k - 500k)x OT = -70°C to +200°C FQ < (6 - 40) GHz @ -1dB CF < 50 g CR < (2.0 - 8.0) A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	 D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (300k - 1,000k)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A
Leeno Industrial Inc. 10 105 beon-gil MieumSandan-ro Gangseo-gu, Busan, Korea 408-313-2964(US)/82-51-792-5641 www.leeno.com	 B, D, P, T, CM	BA, BD, LA, SF, TH	CP > 0.1 mm CL = >200K OT = -55C ~ 150C FQ = 6ghz >-50ghz@ -1db CF = 6g - 50g CR = <3.0A @0.4p
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25 - 0.4) mm CL = CM OT = CM FQ = CM CF = CM CR = CM
M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjco.jp	B, D, T	BA, SM	CP > 0.2 mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM
Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25 - 50) g CR < (1.0 - 3.0) A

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Modus Test LLC P.O. Box 56708 Atlanta, GA 31156 Tel: +1-678-765-7775 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3 mm CL > 1,000,000x OT = +200°C Max. FQ < 20 GHz @ CM CF < 35 g CR < 5.0 A
Multitest Electronic Systems 4444 Centerville Road, Suite 105 Saint Paul, MN, 55127-3700 Tel: 1-651 407 7726 www.multitest.com	D, T	BA, LA, SM	CP > (0.25 - 0.5) mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5 - 40) GHz @ CM CF < (26 - 55) g CR < (1.8 - 4.6) A
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong,Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0 - 12.4) GHz @ -1dB CF < (7 - 15) g CR < (0.5 - 1.0) A
Paricon Technologies Corporation 421 Currant Road Fall River, MA 02720 Tel: +1-508-676-6888 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1 - 0.4) mm CL > 1,000,000x OT < 150°C FQ < 40 GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtest.com	D, T	BA, LA, SM	CP > 0.4 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < 25 g CR < 3.5 A
Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
ProFab Technology Inc. 41817 Albrae Street Fremont, CA 94538 Tel: +1-925-600-0770 www.profabtechnology.com	D, T	BA, LA	CP > (0.26 - 0.45) mm CR < 7.0 A CL, OT, FQ & CF = CM
Protos Electronics 1040 Di Giulio Avenue, Ste. 100 Santa Clara, CA 95050 Tel: +1-408-492-9228 www.protoelectronics.com	D, T	BA, LA, SM	CP = CM CL > 300,000x OT = -55°C to +135°C FQ < 22.3 GHz @ -1dB CF < 20.8 g CR < 4.0 A
Qualmax, Inc. IT Castle, 1-dong, 1101-ho 550-1 Gasan-dong, Geumcheong-gu Seoul, Korea 153-768 Tel: +82-2-2082-6770 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5) mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0 - 4.0) A
R&D Altanova 3601 So. Clinton Avenue, South Plainfield, NJ 07080 Phone: 732-549-4554 Fax: 732-549-1388 www.rdaltonova.com	D, P, T	BA, BD, LA, SM	CP < 0.3 mm CL = 150,000x OT = -40° to 150°C FQ > 38GHz @ -1dB CF = 15g CR = 4A
Rika Denshi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40° to +160°C FQ < 36 GHz @ -1dB CF < (15 - 30) g CP & CR = CM

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Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0 A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35 mm OT = -55°C to +150°C FQ < (9 - 10) GHz @ CM CR < (1.0 - 15) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Avenue, Suite 100 San Jose, CA 95120 Tel: +1-408-269-2800 www.sanyu-usa.com	CM	CM	CP > 0.2 mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15 - 25) g CR < (4.0 - 5.0) A
Sensata Technologies, Inc. 529 Pleasant St, P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	 B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10 - 25) g CR < 1.0 A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3 - 0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5- 20) GHz @ CM CF & CR = CM
Smiths Connectors IDI 5101 Richland Avenue Kansas City, KS 66106 913-342-5544 www.smithsconnectors.com	 D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 250k - 1M OT - 40° to 150°C FQ < 25GHz @ -1db CF 8 – 85 grams CR 1.5 to 5 Amps
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3 Bayan Lepas, Penang 11900, Malaysia Tel: +60-4-646-6966 www.tts-grp.com	D, T	A, LA, SM, TH	CP > 0.2 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 20 GHz @ -1dB CF & CR = CM
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: +1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5 - 1.0) A
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com	D, T	SM	CP > 0.4 mm OT = -40°C to +150°C FQ < (6 - 8) GHz @ CM CL, CF & CR = CM

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WinWay Technology Co. Ltd. No. 68, Chuangyi S. Road, Second District of Nanzih Export Processing Zone, Nanzih Dist Kaohsiung City 81156, Taiwan Tel: +886-7-361-0999 www.winwayglobal.com	B, D, T	BA, BD, LA, SM	CCP > (0.2 - 0.4) mm CL > (50k - 500k)x OT = -50°C to +150°C FQ < (0.2 - 30) GHz @ -1dB CF < (10 - 41.3) g CR < (1.5 - 7.0) A
Yamaichi Electronics Co., Ltd. 3-28-7 Nakamagome, Ota-Ku Tokyo 143-8515, Japan Tel: +81-3-3778-6111 www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4 mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM

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Sapphire as a sensor platform

Syed Sajid Ahmad, Fred Haring, Greg Strommen, Kevin Mattson, Aaron Reinholtz
[Center for Nanoscale Science and Engineering at North Dakota State University]

Sapphire, with its unique properties, provides a robust and reliable platform for electronics and sensors with numerous advantages over other sensor platforms. Sapphire is not as brittle as silicon and thus provides a substrate for sensors for harsher environments where silicon-based electronics may be at risk of failure.

With required modifications in process, silicon-based sensors can also be manufactured on sapphire providing greater durability and, in some cases, a larger and expanded use environment and sensing range. Photosensitive devices and circuits can be implemented in the silicon-on-sapphire (SOS) technology as a direct translation of CMOS circuits [1]. Culurciello also explains SOS biosensor interfaces [1].

If there is a need to add a silicon-based component, the coefficient of thermal expansion (CTE) of sapphire is $\sim 7\text{-}8\text{ ppm}/^\circ\text{C}$, compared $2\text{-}3\text{ ppm}/^\circ\text{C}$ for silicon. This results in a reduced CTE mismatch between the chip, or in this case the substrate, and the solder interconnects, which results in longer lifetimes for the mounted chip.

Sapphire is an insulator and therefore provides numerous processing benefits. Through-vias for the densification of electronics can be made in sapphire with simpler processing steps and at a higher throughput requiring less expensive processing equipment. For additional densification, passives and support electronics can be located on the backside of the sapphire more easily and reliably. Sapphire is tough and nonconductive making it easier to make fluidic channels on it for sensing purposes as they will not require extra processing to insulate them electrically.

Sapphire is optically transparent (low absorption, transmission loss, and reflection, along with a wide transmission band) allowing the transmission and reception of return optical signals for sensing purposes. It also is well suited for manufacturing light sources on it along with sensors for optical signals. Sapphire provides full dielectric isolation (no substrate capacitance). “SOI manufactured processors require an average of 40-50% less power than CMOS ones [1].” It has high radiation hardness (a back gate is not needed). It has higher thermal conductivity than SiO_2 and therefore has no self-heating effect.

Via process for electronics densification on silicon is expensive and slow. The Center for Nanoscale Science and Engineering (CNSE) at North Dakota State University (NDSU) has

shown laser via capability in sapphire that can be used to interconnect electronics from one side of the sapphire to the other. The sapphire via also does not require extra processing to isolate it as is needed for silicon because silicon is semiconducting, whereas sapphire is an insulator.

Although electronics can be housed on both sides of organic and inorganic substrates, they are not yet developed for manufacturing thin-film devices on them, while sapphire has been used to create robust and reliable integrated electronic devices on it.

Silicon is a semiconductor, therefore, insulating steps are necessary when adding functionality to its backside. Sapphire, however, is an insulator, therefore, insulating steps are not necessary when adding functionality to its backside, which therefore provides

	Sapphire	Silicon
Conductivity	Insulator	Semiconductor
Through-via insulation	Does not require insulation of through-vias	Requires insulation of through-vias
Backside insulation	Circuitry on backside will not require insulation	Circuitry on backside will require insulation
Backside micromachining	Laser can be used for sapphire micromachining	Wet processes are necessary for the silicon, which are slow and hazardous
Laser-via cleaning	Laser vias are clean	Silicon’s crystal structure necessitates cleaning of laser-vias
Laser-via wall condition	Sapphire micromachining yields clean, even cuts	Crystal structure renders laser-cut features to be uneven after cleaning

Table 1: Sapphire vs. Silicon

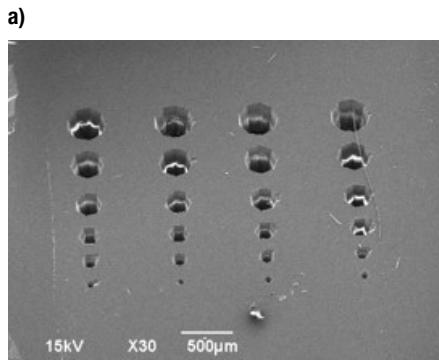


Figure 1: a) (left) Various size vias in sapphire; b) (right) Close-up

an incentive for the exploration of the use of the backside of the sapphire devices to add further functionality, or the addition of peripheral components to the backside of the device.

A comparison of sapphire vs. silicon is shown in **Table 1**. The insulating nature of sapphire provides a unique opportunity to provide electrical paths, embed components or form components in sapphire, without the need to use dielectric layers to isolate them from the die. The grooves may be used as micro-mixing or dispensing channels for use with nano-materials or liquids. Etching traces or trenches in sapphire leaves depressions that can be filled with conductive inks to make circuits or interconnects. Etching traces in sapphire also has the potential to be used as a heat removal system by running a fluid through the backside of the sapphire die. Etching features within the sapphire chip allows for components to be embedded within the die without increasing the volume of the device and uses space in the die that is normally wasted.

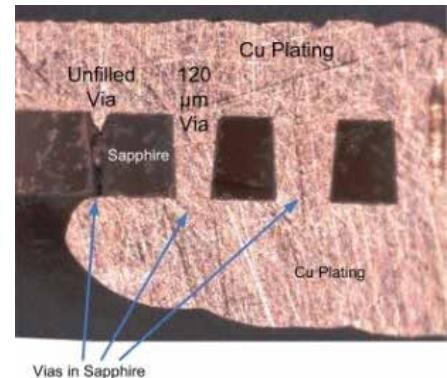
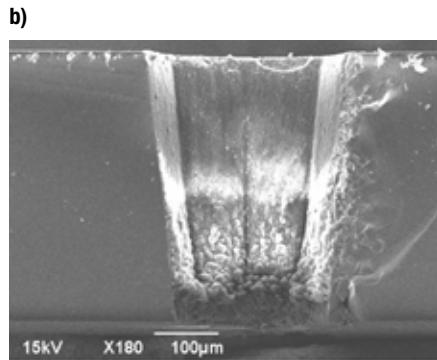


Figure 2: Sectional view of Cu-filled vias

Development work performed at CNSE/NDSU

Use of lasers for sapphire micromachining. Sapphire is difficult to machine because it is hard and brittle. Laser processing has the potential to quickly, delicately and accurately ablate sapphire into a variety of intricate structures. Laser patterning and via drilling on sapphire wafers and dice with various lasers at CNSE/NDSU has shown significant capabilities to make micro-features on and in the sapphire [2]. Laser-etching to pattern/micromachine was able to adequately form channels, pockets and through-vias. These channels were filled with conductive ink to produce conductive traces. Components could be placed in pockets and joined by filling the channels with conductive material. Through-vias could be used to join the features on the front and back together. Through-vias can also be used to join one chip to another chip or to a substrate. The next sections provide an overview of the work done by CNSE/NDSU.

Vias for chip and wafer-level interconnects. Through-via in silicon aids in the densification of electronics where size and weight matter. As part of the work done by CNSE/NDSU, through-vias in sapphire were formed with a laser. Sapphire through-vias were metallized and their continuity was confirmed (**Figures 1** and **2**).

Vias were successfully plated with Cu from 120 μm and up. The filling was complete as well as void-and inclusion-free. The left via (**Figure 2**) – 60 μm wide – was not filled in this instance. The via to its right has a 120 μm diameter at the opening on top. The sapphire was placed in a thermal cycle test with a high temperature of 100°C and a low temperature of 0°C, with a 10-minute dwell time. Optical observation did not show any damage after 72 cycles. A daisy chain was constructed on sapphire (**Figure 3**) to show the continuous front-to-back interconnect.

At CNSE, via formation has been studied using 8 different kind of lasers

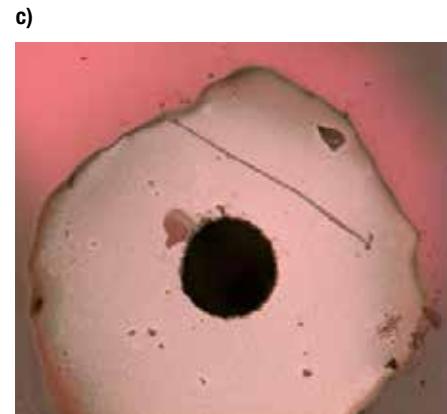
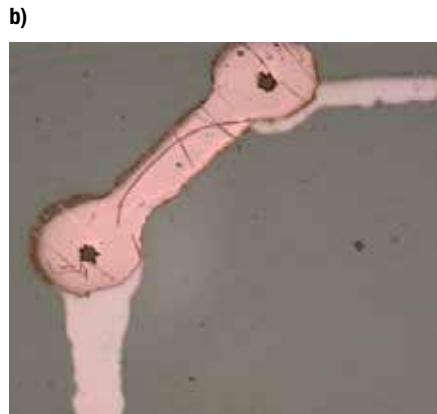
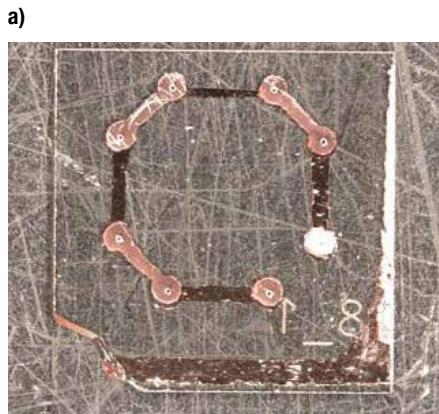


Figure 3: a) (left) The traces on the front of the sapphire are electrically connected to the traces on the back through plated vias in a daisy chain circuit. Traces zigzag from front to back; b) (middle) Close-up of a trace on the front connecting to two traces on the back of the sapphire; and c) (right) Close-up of the filled via.

(3 in-house and 5 external suppliers). Via sizes of approximately $40\mu\text{m}$ diameter and at an approximate 3° wall angle have been realized (**Figure 4**) [3].

Via filling has been demonstrated through a metal cold spray process developed at CNSE/NDSU and through-plating [4, 5]. A two sapphire chip stack has also been demonstrated in recent work and a three chip stack has also been studied (**Figure 5**).

Work at CNSE/NDSU also has shown that a thin layer of metal can be used to protect the surface of circuitry on sapphire to save it from the effects of heat and debris [6]. **Figure 6** shows the surface of the chip before and after the removal of the protective layer.

Constructing pockets, traces, and trenches. To reduce the size of circuits, the trace thickness, as well as the distances between the traces, must be minimized. The thinnest traces etched ranged from 14 to $18\mu\text{m}$ wide and 8 to $12\mu\text{m}$ deep. The closest traces were $30\mu\text{m}$ from center to center and had a $15\mu\text{m}$ wall between them (**Figure 7**).

Patterned grooves for circuitry and antenna formation. Backside patterning may be used for nano-imprinting of inks and other liquids. Traces, $45\mu\text{m}$ wide, were etched deep enough to result in thick conductive traces when filled with conductive ink (mill-and-fill process). Ink was squeegeed in and then cured (**Figure 8**). The vias at the center of the antenna conducted from the antenna to the other side of the $200\mu\text{m}$ R-plane sapphire.

Metal patterning for circuitry. A passive element was produced by applying a conductive layer and then etching it with laser to shape the desired conductive feature or electrical element or component. A $200\mu\text{m}$ R-plane sapphire was coated with a layer of copper by sputtering. The laser was used to isolate the traces by removing the copper and leaving only the patterned traces to form the element (**Figure 9**). The laser cleanly removed all of the unwanted copper and removed almost no sapphire leaving traces $40\mu\text{m}$ wide.

In recent work, formation of capacitors and inductors on the back of a sapphire device (**Figure 10**) has also been studied at CNSE/NDSU [7].

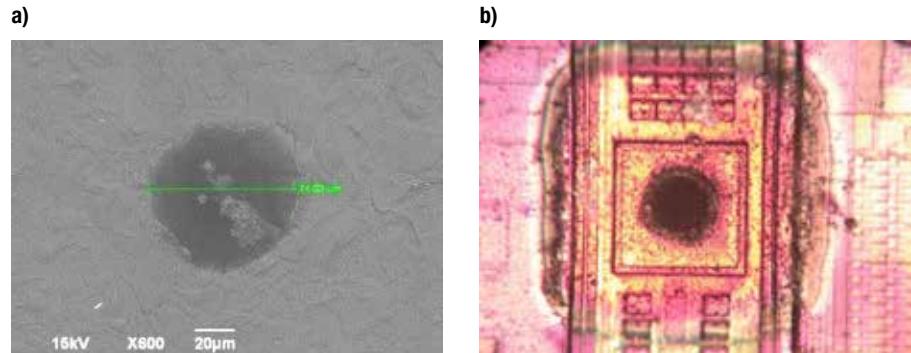


Figure 4: Vias in sapphire machined by laser services suppliers: a) (left) SEM of a representative via; b) (right) The halo around the via is showing the extent of a coating to protect the circuitry from heat and debris generated during the laser drilling of the via. The coating is removed later to obtain a clean via.

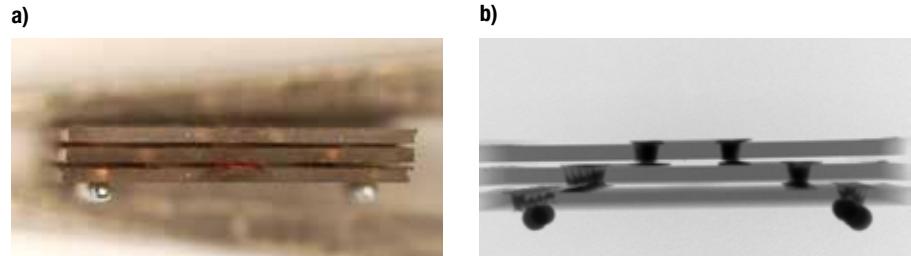


Figure 5: A three-sapphire chip stack: a) (left) Side (optical) view; b) (right) Tilted x-ray view.

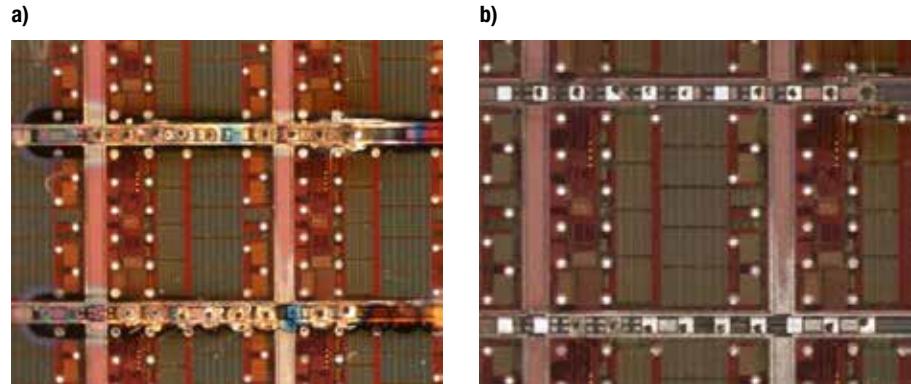


Figure 6: a) (left) Laser vias drilled after copper-sputter; and b) (right) after copper-etch to remove the protective layer of copper over pads.

Pocket or trench patterning for adding passive components to the back of dice or wafers. A simple circuit pattern was etched into the sapphire in an attempt to produce a circuit pattern with uniform depth and width control of traces as opposed to etching a pattern completely through the chip (**Figure 11**). Embedding components will lower the overall thickness of a circuit. So, instead of placing the component on top of the surface, the components are placed into pockets that are designed for a close fit. The circuit that connects these components can be produced multiple ways.

All of the techniques discussed above, or a combination thereof, may be applied to

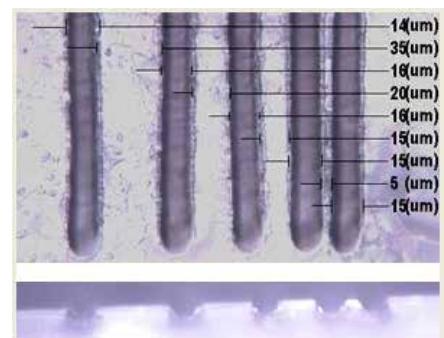


Figure 7: Photo showing grooves made in sapphire using a laser. The bottom portion of the photo shows the side view of the grooves in the surface of the sapphire.

3D chip or wafer assembly and packaging for electronics densification.

Technology development impacts

The developments discussed above pave the way for the manufacture of smaller and robust sensors to monitor and measure human, process and environment health. Use of sapphire for robust and densified sensors will help spawn new business, research and technology development opportunities. Several of these opportunities are described below.

The use of the transparency of sapphire provides the ability to place sensing light on one side of the sensor to sense an object on the other side. The "image sensors using SOS technology can be used as back-illuminated sensors without thinning process [8]." Furthermore, "Sapphire optical fiber interferometric sensors have been developed and demonstrated for the measurement of displacement, strain, ultrasonic waves and temperature [9]."

A sapphire-based sensor "excels in gasification, sulfur recovery, and other high-pressure, high-temperature processes that require the ability to survive in sulfuric and other toxic environments. High-temperature miniature Fabry-Perot sensor (MFPS) and ultra high-temperature Fabry-Perot sapphire temperature sensor technologies have been used in applications including medical diagnostics, coal-fired boilers, downhole oil and gas and advanced propulsion systems [10-12]."

Higher order mode rejected fiber Bragg gratings (FBGs) in sapphire crystal fiber using infrared (IR) femtosecond laser illumination have been fabricated for environmental sensing applications. Additionally, the response of nerve cell to inhibitor has been recorded by AlGaN FET. "AlGaN/GaN sensors on sapphire are transparent to visible light, which allows the implementation of additional optical techniques such as fluorescence measurements [13]."

Summary

The work presented and the developments outlined above encourage design and production of denser electronics and sensor systems for use everywhere. Sapphire provides a robust and reliable platform to provide highly

densified, miniaturized and compact electronic systems for use on earth and in space for applications in every sphere of life.

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The advertisement features the EV Group logo at the top left, consisting of a yellow oval with three horizontal lines inside, followed by the letters 'E V G' in a bold, black, sans-serif font with a registered trademark symbol. To the right of the logo is a dark grey bar with three white vertical rectangles containing the words 'invent', 'innovate', and 'implement'. Below the logo is the product name 'GEMINI®FB XT' in large, bold, black capital letters. Underneath it, the text 'BREAKTHROUGH FUSION WAFER BONDING SYSTEM' is written in a smaller, all-caps font. To the left of the main text block are three blue chevron bullet points. The first point says '3X Improvement in Wafer-to-Wafer Bond Alignment Accuracy'. The second point says 'XT Frame Platform for up to 50% Throughput Increase'. The third point says 'Enabling High-Volume Production of 3D Devices such as Stacked DRAM, Memory-on-Logic and Future CMOS Image Sensors'. Below this text block is a large photograph of the Gemini FB XT machine. It is a large, industrial-grade bonding system with a white frame and orange copper-colored bonding heads. To the right of the main machine is a smaller inset image showing a close-up of a wafer being processed inside the machine. At the bottom of the advertisement is a black call-to-action bar with the text 'GET IN TOUCH to discuss your manufacturing needs' and the website 'www.EVGroup.com'.

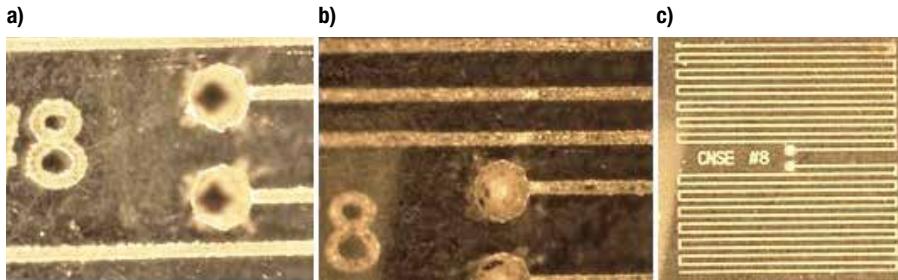


Figure 8: (left) Traces etched into sapphire; b) (middle) Etched traces filled with conductive ink; c) (right) Circuitry made with the mill-and-fill process.

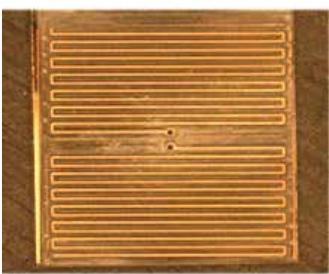


Figure 9: Element manufactured by isolating etch process on 200 μ m R-plane sapphire.

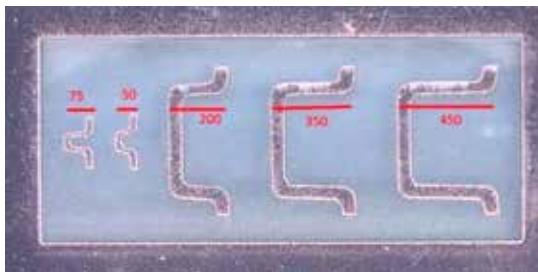


Figure 10: Micro-inductor patterns on sapphire.

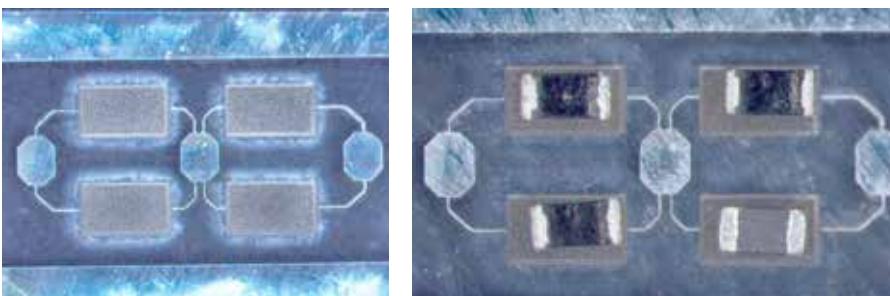


Figure 11: Circuit with embedded components made by insulating traces.

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Biographies

Syed Sajid Ahmad holds two masters degrees in Physics from the U. of the Punjab and Islamabad U. and is Manager of Engineering Services at the Center for Nanoscale Science and Engineering at North Dakota State University (CNSE/NDSU); email Syed.Ahmad@ndse.edu

Fred Haring received his Bachelors degree and as a fabrication technician has provided semiconductor chip packaging and assembly technical support at CNSE/NDSU for the last decade.

Greg Strommen is an engineering technician at CNSE/NDSU and has provided thin-film processing technical expertise to the industry for the last 23 years.

Kevin Mattson is a fabrication technician at CNSE/NDSU and has provided thin-film processing technical expertise for more than 17 years.

Aaron Reinholtz received a BS in Electrical and Electronics Engineering from North Dakota State U. and is the Associate Director for Electronics Technology at CNSE/NDSU.

Electronic Packaging and System Integration

Chip Scale Review staff surveys Fraunhofer Institute for Reliability and Microintegration IZM with Head of the Institute, Prof. Klaus-Dieter Lang

**Fraunhofer Institute
for Reliability and
Microintegration IZM
Gustav-Meyer-Allee 25
13355 Berlin
Germany
www.izm.fraunhofer.de**



Fraunhofer Institute for Reliability and Microintegration IZM Berlin, Germany, (top-right): Miniaturized RF modules for localization of sensor nodes by 24 GHz radar, (right-center) Clean room for microelectronics research, (right-bottom) Shape-adapted electronics by stretchable circuits on polyurethane.

Photographs, copyright Fraunhofer IZM

Backgrounder

Fraunhofer IZM was established in 1993 and has a current staff of 389 employees. Three independent Fraunhofer institutes have evolved out of Fraunhofer IZM. Over 350 researchers and developers work at the three sites in Berlin, Dresden and Oberpfaffenhofen, of which approximately 35% are involved in direct industry projects. Its customers are comprised equally of small- and large-sized companies.

Fraunhofer IZM is one of 67 Fraunhofer-Gesellschaft institutes and is the alliance's expert in electronic packaging. With its staff of 23,000 and research volume of 2 billion euros, Fraunhofer Gesellschaft is one of the world's leading research centers for applied biological and mechanical engineering research and development. Research of practical utility lies at the heart of all Fraunhofer Gesellschaft activities, and this is reflected by its 1.7 billion euro turnover through contract research, that is, direct contracting from industry or together with industry in national and international funding projects. Fraunhofer IZM closes the gap between wafer and application and is a member of the Fraunhofer Microelectronics alliance, representing the group's competency in packaging and smart system integration.

Mission Statement

Development demands and the market show two main trends helping to shape the ongoing development of system integration technologies:

First, an ongoing increase in the number of functions directly included in a system, which include electrical, optical, mechanical, biological and chemical processes, combined with the demand for higher reliability and longer system lifetime.

Second, increasingly seamless merging of products and electronics, which necessitates adapting electronics to predefined materials, forms and application environments. Only by these means can systems sensors and signal processing be implemented near to the point where signals are occurring. Heterointegration technology is used to develop customer-specific solutions that can also be manufactured cost-efficiently at medium lot sizes.

Chip Scale Review asks Prof. Klaus-Dieter Lang

■ Given the state of the semiconductor packaging industry – including all the technical and financial challenges associated with R&D for advances - what are the top one or two issues the industry must tackle over the next 18-24 months and why? Do you have proposed solutions for these challenges?

One of the biggest challenges facing today's semiconductor packaging industry is the sheer range of application areas and product types that rely on microelectronics in one form or another. This is, on the one hand, a sign of how powerfully and important packaging development has become over the years, and on the other hand, a consequence of industry reaching for every solution at its disposal to address pressing social, industrial and ecological issues. Population growth and aging are an example of the former, while the latter include technologies such as electromobility, public health, energy efficiency, and decentralized control of manufacturing processes. So, electronic packaging shifts more or less from a technological orientation to a functional orientation.

■ How will your organization participate in addressing the issues you raised in the first question?

At Fraunhofer IZM, we asked ourselves how we could support industry to implement sophisticated system integration solutions for

the above application environments. One main theme of our experience is that assembly and packaging have to become an integrated and emancipated part of a system's value chain. In response, our institute is currently completing a wide-ranging reorientation of our technology development focus: from the component to the system packaging, especially based on wafer-level and panel-level integration.

In this context, our main purpose is to develop new system integration solutions for large enterprises and SMEs assisting these target groups to implement these technologies into their products and production environments. In fact, Fraunhofer IZM's organizational and technical structure is tailored to the needs of material and equipment suppliers, technology providers, and end users. All branches of the institute (e.g., Berlin for SiP, or Dresden for 3D-WLP) are able to cover the complete assembly and packaging value chain – from system design to reliability assessment – making Fraunhofer IZM into a one-stop application development and consultation service for industrial and academic customers.

■ How is your organization's participation in standards activities and/or research consortia activities helping to meet the technology challenges that lie ahead in the next 2-5 years?

More broadly, Fraunhofer IZM addresses future key questions that arise in the issues noted above by conducting basic research projects. We also keep abreast of the latest developments throughout industry, and internationally by participating in EU and national collaborations with other research institutes (especially TU Berlin) and private industry. We then use this constantly improving know-how to support our partners from industry to implement new solutions to their daily packaging tasks. Second, we push cutting-edge technology by actively promoting and facilitating standardization as part of the above collaborative activities.

While our range of R&D expertise in modern assembly and packaging solutions is extremely broad, we have specialized our transfer lines in two integrated areas, which are organized in a Wafer-Level Integration Center and a Panel-Level Integration Center. In terms of wafer-level packaging (also 2,5D and 3D), our ASSID in Dresden has the capability for the complete processing of 300mm wafers. Apart from providing the latter technology and know-how for 200mm wafers, our Berlin branch also has the latest know-how in modern system integration solutions for panel-level packaging (up to 18" x 24" panels), including the embedding of passive and active components, particularly power semiconductors. A specific point of pride is our complete PCB production line for all-in-one manufacturing of PCBs in Berlin.

Miniaturization, multi-functionality, durability, reliability, cost-efficiency – these have been catchphrases since packaging technology was in its infancy. However, Fraunhofer IZM's strategic reorientation and infrastructure investment over the recent years specifically addresses what we consider to be the key upcoming issues in the assembly and packaging industry, largely deriving from the growing focus on functionality and application, as opposed to the system. At first, we urgently need to maintain the advancement of 3D system integration and system-in-package (SiP) development. Moreover, panel-level packaging will gain in importance. Here, we will need to be able to offer comprehensive technology development platforms and worldwide significant standards. Summing up, the shift from technology oriented packaging to system packaging considering the application environment will be essential in the future. Fraunhofer IZM currently makes, and extends, of course to the future, an important contribution to the competitiveness of our partners, because a flexible and advanced approach to electronic assembly and packaging is surely a key prerequisite for meeting the needs of tomorrow's industry and society.



Prof. Klaus-Dieter Lang: Prof. Lang studied Electrical Engineering from 1976 to 1981 at Humboldt University in Berlin. He received his MS Equivalent Diploma (Metallization Layers on GaAs) in 1981. During his employment at Humboldt University from 1981 to 1991 he worked in the research fields of microelectronic assembly, packaging and quality assurance. In 1985 and 1989 he got his two Doctor Degrees (Wire Bonding of Multilayers and Quality Assurance in Assembly Processes). In 1991 he joined the company SLV Hannover to build up a department for microelectronic and optic

components manufacturing.

In 1993 he became Section Manager for Chip Interconnections at Fraunhofer IZM (Institute for Reliability and Microintegration Berlin). From 1995 to 2000 he was the Director's personal assistant at Fraunhofer IZM, also responsible for Marketing and Public Relations.

From 2001 to 2005 he coordinated the Branch Lab "Microsystem Engineering" in Berlin-Adlershof and from 2003 to 2005 he headed the Department "Photonic and Power System Assembly." From 2006 to 2010 he was Deputy Director of Fraunhofer IZM. Since 2011 he is Director of the institute and responsible for the chair "Nano Interconnect Technologies" at Technical University Berlin.

Prof. Lang is a member of numerous scientific boards and conference committees. Examples are the SEMI Award Committee, the Scientific Advisory Board of EURIPIDES, the Executive Board of VDE-GMM and the scientific chair of the Conference "Technologies of Printed Circuit Boards" and "SMT/HYBRID/PACKAGING." He is a member of DVS, IEEE, IMAPS and he plays an active role in the international packaging community (e.g., German Chapter Chair IEEE-CPMT) as well as in the field of conference organization (e.g., Committee member SSI).

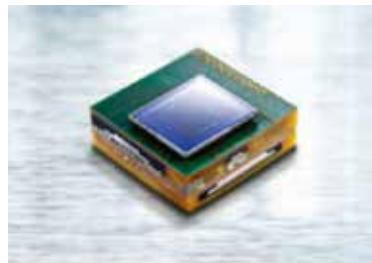
Prof. Lang has authored and co-authored 3 books and more than 130 publications in the fields of wire bonding, microelectronic packaging, microsystems technologies, chip on board, and others.

Recent significant technology development

A recent significant technology development is the modular sensor-kit with embedded components. Modular sensor systems provide a high degree of flexibility and variety. The selection of suitable sensors can be quickly set up to capture properties and to regulate or control desired parameters of an application-related system. The highlight of this sensor system is the interchangeability of complete sensor elements.

The foundation for the variety arises from individual modules with specific sensors that have the capability of pre-processing captured measurements. Each module transmits the data to the basic module using a standardized protocol (I²C). Moreover, sensor elements with high data rates (e.g., camera) are equipped with a USB connection to the basic module. All the data collected in the entire system is processed via a software application on the basic module. The results can be transmitted to a computer using a USB connection. Furthermore, the applications running on the basic module as well as on the computer can be programmed with the help of a graphical programming language.

Each module contains one or multiple sensors. Moreover, they are equipped with power conditioning, a microcontroller, and several passive components. The microcontrollers serve as interface to the overall system and perform the data pre-processing. All components are integrated into the circuit board using the PCB embedding technology. This method allows replacing individual or multiple modules, due to the even and identical top and bottom surface. The module selection, as well as the order is application oriented. For permanent usage they can be soldered or cemented. However, for temporary or variable usage requirements the modules can be stacked with specially designed connectors.



Camera module with embedded components

LC-2 Burn-In Value Menu

8-slot • single zone



32-slot • multiple temperature zone



64-slot • production oven



Nutrition Facts

Serving Size:
Choose the Size You Need
Servings Per Container: 1

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High-vacuum wafer bonding for hermetic sealing of novel MEMS devices

By Eric Pabo, Thorsten Matthias, Paul Lindner [EV Group]

Over the past decade, the MEMS market has enjoyed significant growth in terms of unit volume, while dollar value of total sales has grown rapidly despite substantial price erosion. As a result, we are now surrounded by MEMS devices in our daily life. There are accelerometers, gyroscopes, pressure sensors and microphones in our smart phones and tablets; our cars have pressure sensors, accelerometers, gyroscopes; our homes and offices have ink jet printers; and our workouts are being monitored by devices that measure our steps, time and location. Even more devices are coming that will incorporate novel MEMS devices, such as night vision cameras for our cars that use microbolometers as the sensor. This amazing growth has been enabled by the reduction of the cost, size and power consumption of MEMS, as well as improved application software to utilize the data generated by MEMS devices. Wafer-level packaging (WLP) by aligned wafer bonding of the MEMS devices has been an enabler of this phenomenal growth by contributing substantially to cost and device size reduction.

Packaging considerations for MEMS

Packaging and test have typically accounted for more than half the cost of a finished MEMS device. MEMS devices present substantial packaging challenges because of their moving parts, which are sensitive to stress, and that need to be protected from the environment, while at the same time also need to interact with the environment. Many MEMS devices required a hermetically sealed package that can keep water vapor out, to contain a controlled environment, or to maintain a vacuum environment. As the vacuum level inside the package increases, the density of

gas molecules decreases, which causes the atmospheric or parasitic drag on a moving part to decrease. For a gyroscope, as the drag decreases, the power required to drive the oscillation of the part decreases. This is important for portable battery powered devices such as cell phones. In a vibratory MEMS energy harvesting device, the parasitic drag of the residual gas in the package reduces the amount of energy that can be harvested. The sensitivity of some devices that detect IR radiation, such as microbolometers and thermopiles, is influenced by the heat transfer away from the sensing pixel, which is affected by the vacuum level inside the package. Also, absolute pressure sensors require a reference vacuum on one side of the sensing diaphragm.

Aligned wafer bonding

WLP by aligned wafer bonding has the advantage of sealing all MEMS devices on a wafer simultaneously. Depending on

die and wafer size, it is possible to seal up to 20,000 devices simultaneously. Anodic, glass frit, direct, metal and adhesive wafer bonding processes are all currently used in high-volume production (Figure 1). Of these processes, anodic, glass frit, and metal are used for vacuum encapsulation, with glass frit and metal bonding used for high-vacuum encapsulation. For a bonding process to be appropriate for vacuum encapsulation it needs to meet two criteria: 1) the material and process must not outgas significantly during the bonding process; and 2) the material must have very low permeability post-bond [1]. Adhesive bonding is not suitable for vacuum encapsulation because most adhesives outgas during curing and the adhesive materials are permeable after curing. Anodic bonding, glass frit, and direct bonding outgas at a limited level during the bonding process. The outgassing of glass frit can be further reduced by optimizing the preprocessing of the glass frit. For lower levels of vacuum

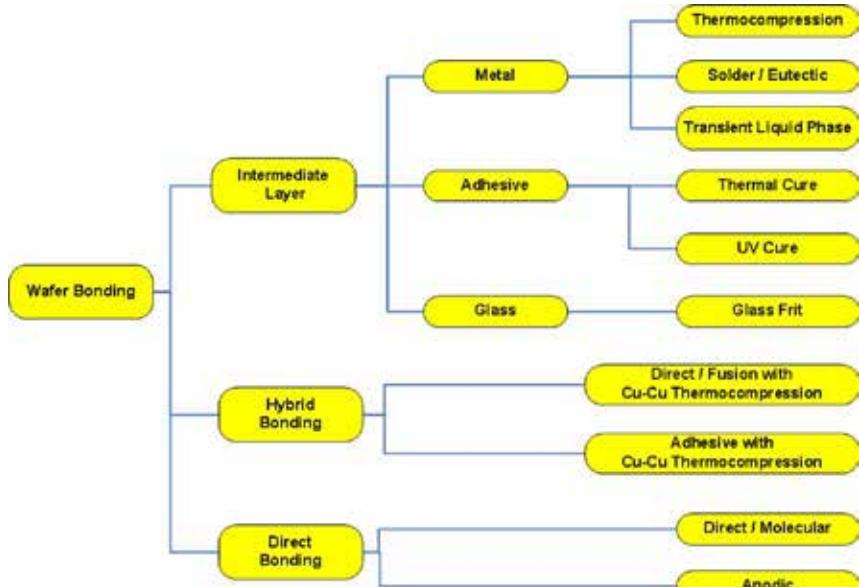


Figure 1: Wafer bonding process family tree.

encapsulation, this outgassing may be acceptable, or it can be handled with the addition of a getter [2]. Metal bonding typically has no, or very low, outgassing and extremely low permeability post-bond, which makes it ideal for vacuum encapsulation.

Glass frit was originally developed for the sealing of vacuum tubes and, along with metal bonding, has very low permeability post-bond. Glass frit is currently used in high-volume manufacturing (HVM) applications for vacuum encapsulation, but most manufacturers are planning to change to metal bonds. The change is because glass frit bond lines are very wide (~250 μm) as a result of the screen printing process used to apply the glass frit. As the MEMS die size shrinks, an ever increasing percentage of the wafer area is taken up by the bond line. In some cases, over 66% of the wafer area is consumed by the bond line [3].

Metal-based wafer bonding is typically divided into two process groups: 1) one where some or all of the metal is liquefied; and 2) one where none of the bond metal is liquefied. The liquid metal bonding processes themselves fall into two types: solder bonding and transient liquid phase (TLP) bonding. In solder bonding, which is sometimes referred to as eutectic bonding, the solder solidifies at a specific temperature or temperature range. This temperature does not change regardless of how many times the solder joint is heated and cooled, and is therefore a reversible process. The thermal profile versus time for a solder, or eutectic bond, is shown in Figure 2.

A TLP bond does not remelt at the same temperature at which it was formed. This is accomplished by having two metals present in the bond interface prior to bonding (one metal with a high melting point and one with a low melting point). During the formation of the bond, the low-melting-point material is liquefied, flowed and then dissolved into the high-melting-point metal. The new alloy formed by the combination of the two metals has a higher melting point than the low-melting-point metal. As an example, Au and Sn can be used for TLP wafer bonding, where the process temperature required to form the bond joint is 200°C and the remelt temperature is greater than 278°C [4]. Cu and Sn have also been used for TLP, with a

formation temperature of 280°C and remelt temperature as high as the melting point of Cu₃Sn (676°C) [5].

While the low-process temperature and high-working temperature of a TLP bond are very attractive, the TLP bond also has special challenges. First, there must be enough of the low-melting-point metal present to allow for some ‘loss’ due to solid diffusion during the heating ramp and still have enough to form the solder joint. Second, the ratio of the two metals determines the final alloy that will be formed if the mixing goes to completion, while the alloy determines the mechanical characteristics of the joint. The thermal profile of the bonding recipes influences how much of the low-melting-point metal will be lost through solid diffusion into the high-melting-point metal during the heat up, and the hold time and temperature will determine whether the

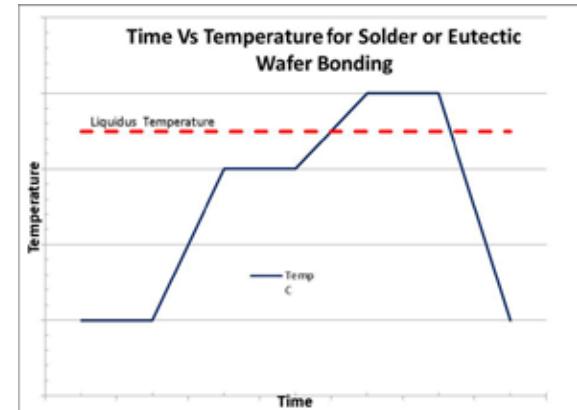


Figure 2: Temperature profile for eutectic metal vacuum bonding.

diffusion process goes to completion.

Both solder and TLP bonding can tolerate some roughness of the bonding metal on the incoming wafers and in some cases even sealing over topography.

In thermocompression bonding, which is also sometimes called metal diffusion bonding, the metal is never liquefied nor inelastically deformed. The physical phenomenon that creates the bonding joint is the diffusion of the metal atoms across




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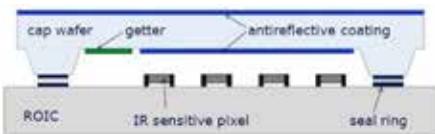


Figure 3: Schematic cross section of a microbolometer showing seal ring and getter.

the interface, which results in grain growth across the interface. The primary challenges of thermocompression bonding are the

requirements for the incoming wafers to be flat and the metal layers smooth and mostly free of oxides. Also, because this bond is formed by a diffusion process, the cycle time may be long when compared to a liquid metal bond.

Metal bonding is used in the majority of new designs for hermetic WLP and vacuum encapsulation. For these products to be successful, it is important to keep

in mind the surface finish requirements (smoothness) for incoming wafers, how the oxides will be managed (if not using noble metals), and how the metal ratios of the alloy will be controlled. It is also important to have a control plan that documents which input and output variables will be measured and how they will be measured.

Now that the sealing technology has been discussed, it is time to examine how the desired vacuum level will be achieved in the cavity, which will be sealed by the bonding process. It is important to understand the behavior of the bond chamber during pump down and then develop an understanding of what is happening to the vacuum level between the wafers and in the wafer cavities.

The typical high-vacuum bonder for production will have a roughing pump, a turbo pump and a control system (at least a cross over control system). When the pump down commences, the pressure in the bond chamber will drop rapidly to approximately 1×10^{-3} mbar as the ambient gas in the bond chamber is removed, after which the pressure drop slows. This slowing occurs for two reasons. The first is that the flow in the bond chambers transitions from a laminar flow (where the gas molecules primarily collide with each other) to a molecular flow (where the molecules primarily interact with the walls of the bond chamber). Second, the desorption of molecules from surfaces inside the bonder becomes significant, with the rate of desorption dependent on the temperature, among other variables. Most HVM bond chambers are currently limited to a vacuum level of approximately 5×10^{-6} mbar due to limitations on the allowable pumping time and because the chambers are not load locked.

If the vacuum level achieved was not sufficient, if the surfaces of the cavities outgas, or if extra assurance of the long-term vacuum in the cavity is needed, it is likely that a getter material will be needed. In very simple terms, the getter material absorbs gas molecules [6-7]. One key aspect of getter materials is that they must have a passive state—where they do not absorb gas molecules—to allow the transportation and handling of the getter material in ambient conditions;

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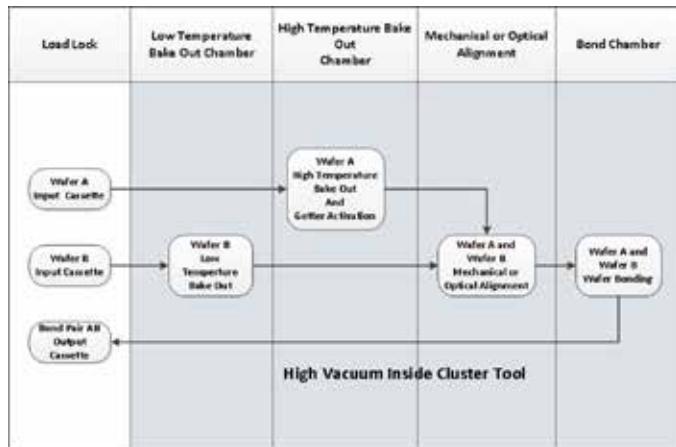


Figure 4: Temperature profile for solder bonding using vacuum encapsulation with getter.

otherwise they would become saturated and useless prior to wafer bonding. The process of changing the getter material to an active state is known as activation. It is very important that the getter not be activated prior to being in a high-vacuum environment. A schematic of a microbolometer that utilizes WLP with a getter for vacuum encapsulation is shown in **Figure 3**.

Wafer bonder requirements

Some MEMS devices have many challenging requirements for the bonding process for WLP. These include high-base vacuum, enhanced wafer bake out, different thermal history prior to bonding for the top and bottom wafer, getter activation, processing of the wafer surface in vacuum prior to wafer bonding, optical alignment in vacuum, and the ability to perform all the preceding steps without breaking vacuum.

Ideally, to meet these challenging requirements, the wafer bonder should be load locked so that the process chambers and handling module are kept pumped down at all times, except for during maintenance events. This allows for a better base vacuum and can decrease the process cycle time because the handling and process chambers are already at base pressure. This design also allows the wafers to be transferred by the robot between the various process modules without breaking vacuum. This is important because if a preprocessing module is used to remove surface oxide, the oxide will not reform while the wafer is being transferred to the bond chamber. In addition, the water and other gasses will not be readSORBED on the wafer surface while the wafers are being transferred from the bake out chambers to the bond chambers.

The addition of bake out chambers would improve the ability to remove adsorbed materials because in addition to being heated, they would be widely spaced to allow for the easy escape of desorbed molecules. Having multiple bake out chambers would allow for the top and bottom wafers to have different thermal histories prior to wafer bonding. This is particularly important for microbolometers that use vanadium oxide on the sensor's pixels and a getter in the final package, because the vanadium oxide should not be exposed to temperatures significantly above 200°C, and yet the getter should be activated at over 400°C.

A cluster tool configuration with multiple bond chambers would



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allow both the low-temperature bake out of the wafer with pixel arrays coated with vanadium oxide and the high-temperature bake out of the ‘non pixel’ wafer and activation of the getter material on this wafer prior to wafer bonding. After the bake out, both wafers could then be transferred to the aligner for alignment, and then to the bonding chamber. Getter activation could be done prior to wafer bonding because all handling is done under vacuum. This would allow the two wafers to have a different thermal history prior to wafer bonding. This means that the pixel wafer is never exposed to the temperature required for the getter activation. An example of a process flow that includes a low-temperature bake out, a high-temperature bake out, alignment, and bonding is shown in **Figure 4**. Having a chamber available for the removal of oxides from the wafer surface would also enable the formation of covalent bonds at near room temperature for certain materials.

Summary

Vacuum encapsulation of MEMS

devices by WLP is an enabling technology as it allows cost and size reduction, as well as ensuring long operation lifetimes. However, successful vacuum encapsulation of MEMS devices by WLP requires a thorough understanding of wafer bonding and vacuum technology, and the appropriate processing equipment.

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Biographies

Eric Pabo received his BS in mechanical engineering from Colorado State U. and is the Business Development Manager for MEMS at EV Group (EVG); email E.Pabo@EVGroup.com.

Thorsten Matthias received his doctorate from Vienna U. of Technology with a thesis in solid-state physics and is Director of Business Development at EVG.

Paul Lindner received his mechanical engineering degree from HTBLA Wels, Austria, and is Executive Technology Director at EVG.

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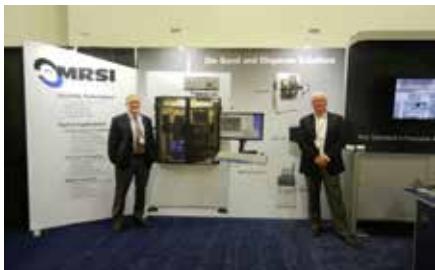
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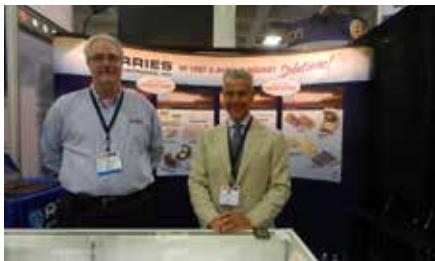
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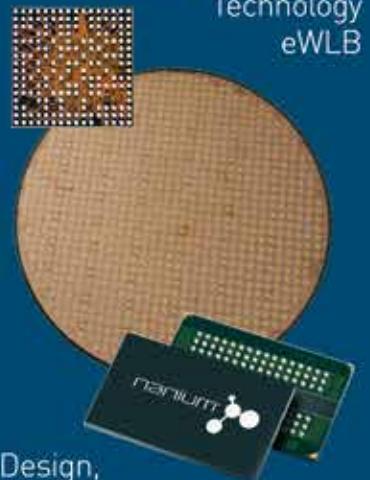


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