

Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 21, Number 3

May • June 2017

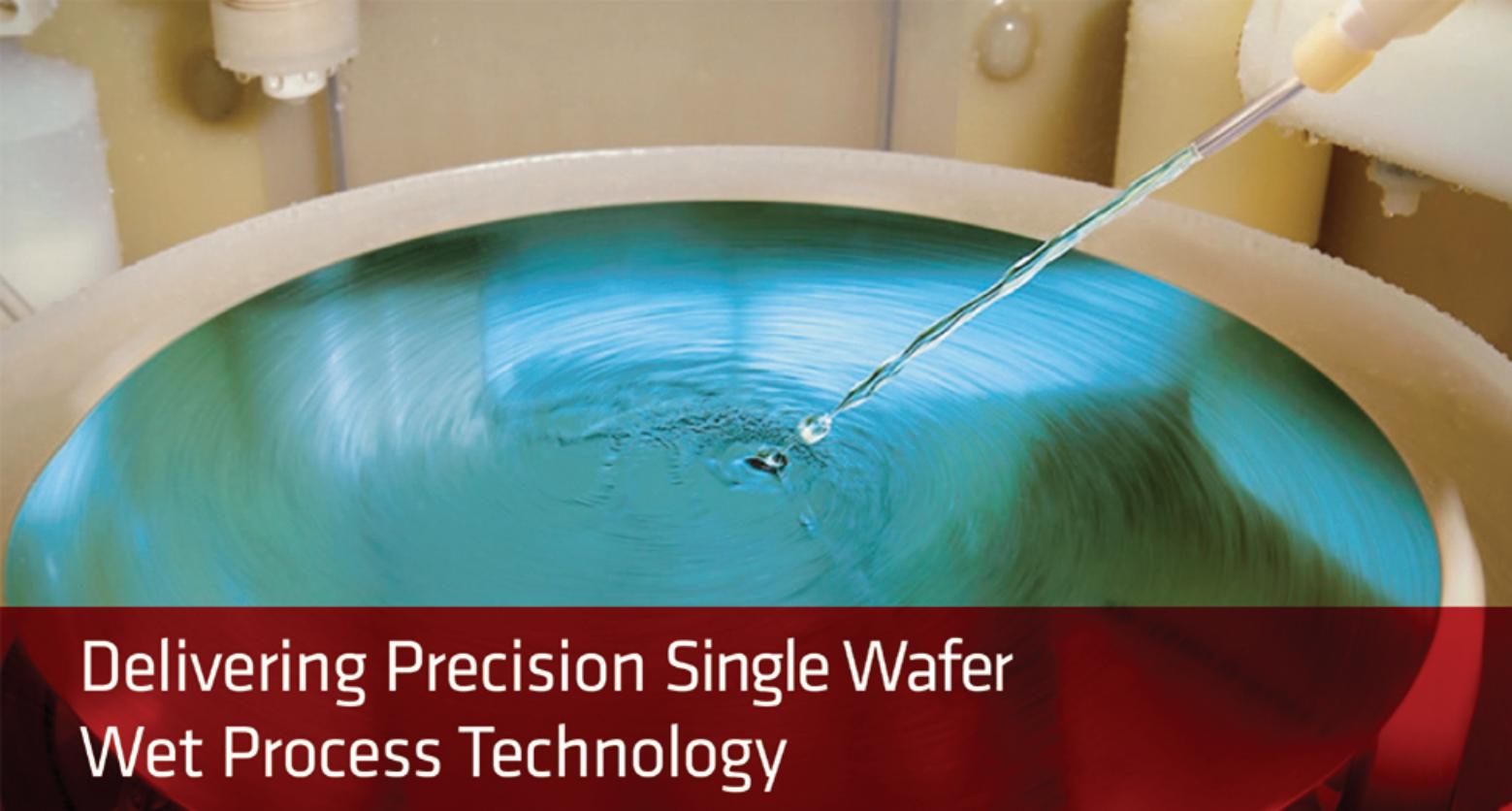


50 years: past, present & future

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- Failure analysis for 3D technology
- FOWLP for hi-performance RF SiPs
- Using glass for packaging & integration
- Impact of heterogeneous integration on business models
- Processing temporary bonding materials for fan-out applications





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The cover captures the essence of the 50 years of Leti R&D for solutions that encompass a wide variety of sectors, including sustainable transport systems, telecommunications, health, consumer electronics, energy, smart cities, defense and security, and space. Founded in 1967, Leti evolved into a global leader in micro- and nanotechnologies tailoring differentiating applicative solutions. Leti has formed partnerships with a multitude of global technology leaders that span a half-century of innovation.

Cover image courtesy of CEA-Leti

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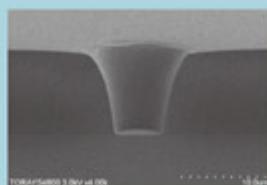
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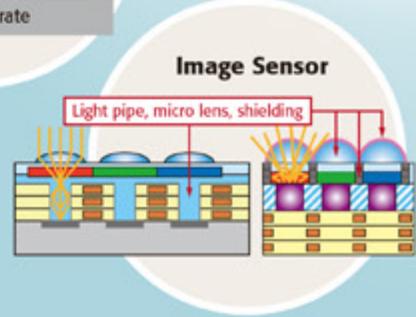
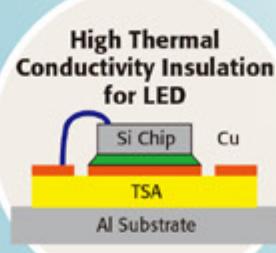
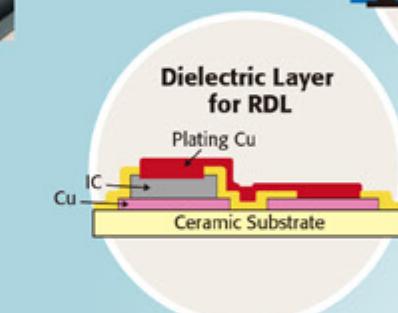
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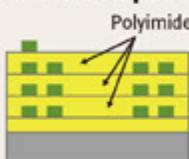
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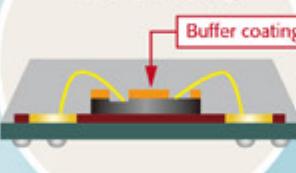
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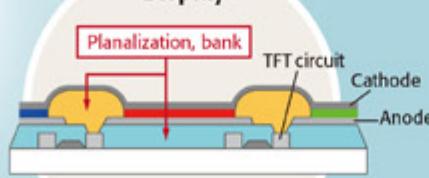
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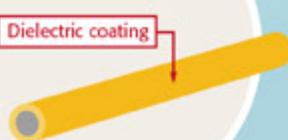
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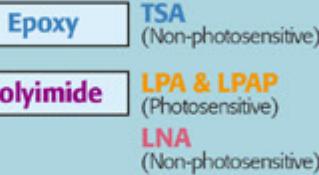
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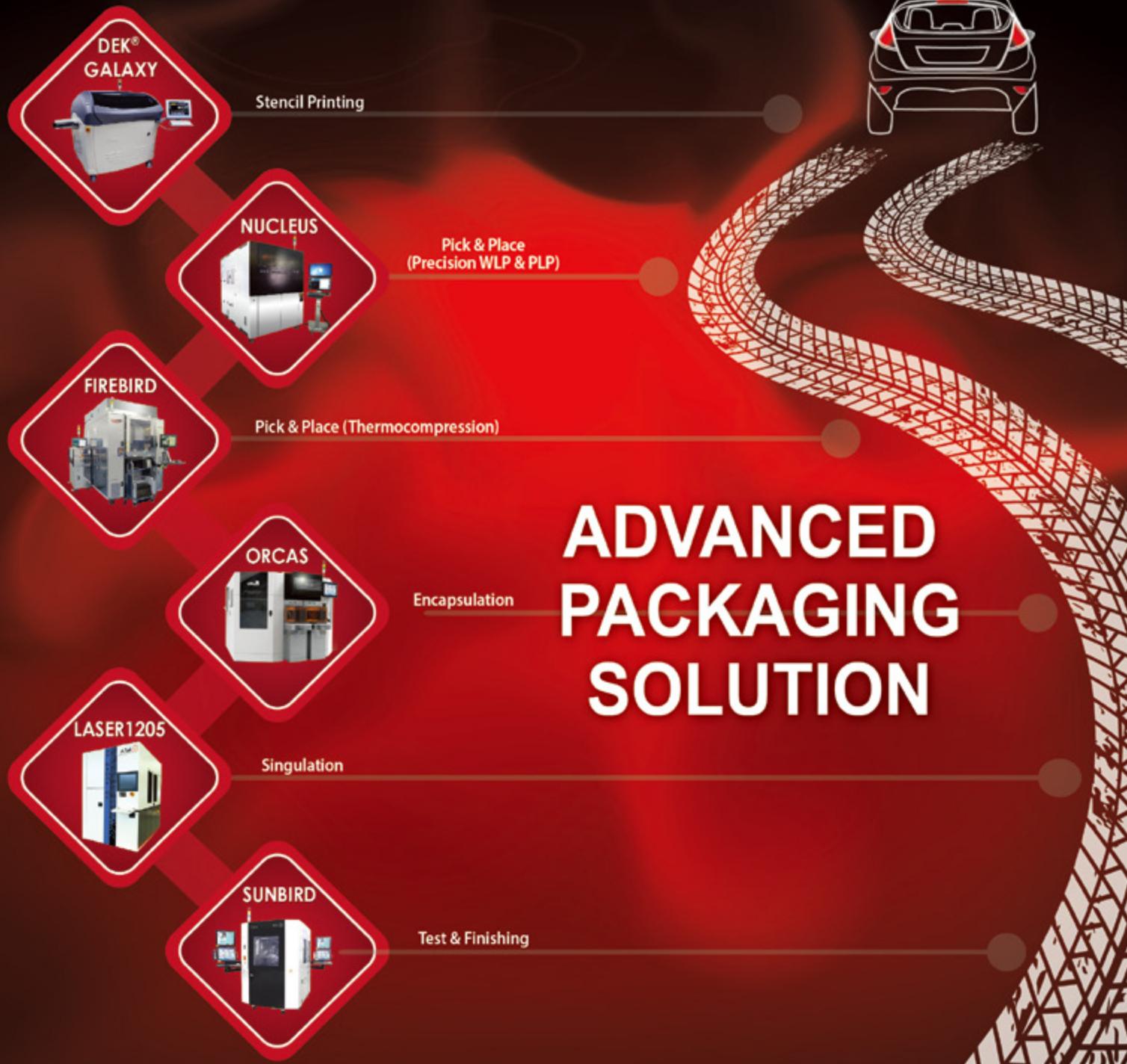
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Heterogeneous integration necessitates adaptable business models

By Jim Walker *[World Level Packaging Concepts]*

Maintaining a continuous revenue stream in cyclic markets is one of the major hurdles faced by outsourced semiconductor assembly and test (OSAT) service providers. Because there are over 150 companies in this market, many providers of commodity-type packages are challenged to gain (or even keep) market share while still improving their technical expertise. To grow and expand, many providers are now supplying ancillary functions to increase revenue and the perceived value of their companies. As manufacturing processes continue to converge with the development of wafer-level packaging (WLP) and system-in-package (SiP), competition is not now just other OSATS, but wafer foundries and electronics manufacturing services (EMS) as well. OSATS must morph their business models to remain competitive and retain their value added processes. This implies that a transition from a commodity-based supplier of standard semiconductor packaging services to a full-service, vertically-integrated total-solution supplier of outsourced electronic manufacturing services may be required.

Manufacturing convergence

OSATS provide manufacturing (packaging) services for designers and developers of semiconductor devices on a contract or "for hire" basis. The cost of building a packaging/assembly factory has escalated in recent times because the continued desire for smaller, faster, less costly packaging has caused the proliferation and complexity of new package types (now over 2500 variations).

Outsourced, state-of-the-art assembly facilities fall into three categories:

- Those of larger, technology-driven companies that have access to the

vast capital resources necessary to offer a wide spectrum of mature and leading-edge packages.

- Specialty market focused, such as those targeting memory or display driver packaging.
- Companies that are focused mainly on mature packages (such as PDIP, SOIC, PLCC and PQFP and transistors).

As packaging complexity evolves, it has necessitated an increase in the capital required. The larger companies, with their ability to reach a broad range of customers and large aggregated customer base, will continue to invest and potentially capture an ever-larger share of the semiconductor packaging market. The capital intensity requirements for the future have resulted, and will continue to result, in industry consolidation, as companies try to increase their share of the \$26 billion OSAT market that was produced in 2016.

As packaging technology evolves into heterogeneous integration, it continues to overlap, converge and intrude upon wafer manufacturing and board-level assembly. These forces cause competition among these manufacturing segments for value-added services. For packaging services companies, the continuing squeeze on margins and consolidation in the semiconductor industry has caused them to search for more profitable business models. These companies realize that to continue growing they can no longer operate just as an extension of an integrated device manufacturer (IDM) or original equipment manufacturer (OEM) packaging facility as has been the case for many years. They need to expand their focus from primarily providing just packaging and/or test services.

The OSAT companies are therefore seeking to move up (or down) the value

chain by providing new, higher-margin services, thus increasing their revenue and potential profitability. This trend has created new opportunities to adapt business models to new segments of the semiconductor industry, providing for heterogeneous integration solutions including WLP or SiP. Supplying these manufacturing solutions also increases the need for more complete design and supply chain management services.

The future growth in the electronic products industry will be driven by products that are, or eventually become, consumer products. Consumers demand products that are more tailored to their specific needs, as the functionality of electronic products has to be easy to customize. In this market, consumers care more about additional features besides the basic functionality of a product. Personal preferences become important purchasing criteria.

A differentiating factor for packaging providers is not just to provide the package, but also include the ability to design a system with the flexibility to enable customization. This differentiation is most noticeable at the final product or system level. However, the key to creating custom products is found further back in the supply chain, at the semiconductor level. And the differentiating factor at the semiconductor level is the semiconductor intellectual property (IP) included in the design of an integrated circuit (IC). It's the IP that provides most of the intrinsic value of an IC. Thus, a company that controls both the design of the IC for a final product and the design of the finished product itself can deliver additional value that will command higher margins.

In light of the above considerations, a more vertically integrated outsourcing service provider that controls both IC

and product design, would thus "own" the supply chain and the design chain, as opposed to just managing the supply chain. The benefit is greater control, flexibility and potentially higher profits. Controlling both the IP and manufacturing assets makes it easier to change a semiconductor design for use in a new product. In addition, a more vertically-integrated service provider can reduce costs and provide more value by eliminating the repeated markups found in other manufacturing models. In these models, higher-cost elements can be repeatedly bought and sold as they pass through the supply chain, with a markup being applied at each point. With a vertically-integrated service provider, there is just one markup before an item is sold to the final customer, thereby increasing the value of the service to the customer.

Using a vertically-integrated service provider would also provide time-to-market benefits. OEMs want to outsource their design and manufacturing to service providers that can meet their demands and provide the most cost-effective manufacturing model to satisfy those demands. They are seeking service providers that can deliver maximum value and increased flexibility. A vertically-integrated manufacturer must therefore be able to provide on-time delivery and have the available capacity and expertise to modify designs and increase production. Vertically-integrated manufacturers with appropriate geographic locations for each of the supply elements provide the benefit of local service on a global scale, reducing or eliminating shipping delays and associated transportation costs.

The vertically-integrated business model for providing outsourced services to electronic product manufacturers is emerging. For example, EMS company Foxconn has bought IC design, system design and software companies. It has also established wafer foundry and semiconductor packaging divisions. And, just recently, it has proposed acquiring semiconductor product companies, as witnessed by its current bid for Toshiba's memory products division. Foxconn has also made recent investments in regions like India, China and South America,

as it tries to gain more value-adding capabilities (design and software) in the emerging markets for the products it will be manufacturing.

Not to be outdone, a similar approach is being taken by OSAT companies. USI's acquisition by Advanced Semiconductor Engineering (ASE) within the past few years now allows ASE to offer EMS and printed circuit board assembly (PCBA) solutions to its customers. Similarly, Orient Semiconductor Engineering (OSE) and Hana Semiconductor have divisions offering EMS and PCBA solutions.

Finally, the last segment of the electronics manufacturing supply chain — the foundry (outsourced wafer fabrication) — is also pursuing the expanded services value chain. TSMC has begun to offer wafer-level packaging services to its customers, in direct competition to the OSAT companies.

So the vertically integrated model offers semiconductor and electronic manufacturing service providers many opportunities and much potential for growth. They will not be dependent on any one OEM program or product success in the marketplace on account of their varied customer base. By working with multiple OEMs, an EMS or OSAT, and perhaps even a foundry provider can operate its manufacturing assets at full capacity and function. A vertically-integrated manufacturer can provide OEMs with all the production capabilities with which they are comfortable and, at the same time, do so through an outsourcing model that is more financially and logically efficient.

It appears we are coming full circle in the electronics industry. The early years of the modern electronics industry in the 1950s (TVs, portable radios) brought products that were built start-to-finish, in-house (vertically integrated) by the OEMs of the day (RCA, Zenith, Philco). From the race to the moon in the 60s emerged the semiconductor industry itself as the driving OEM force, still vertically integrated (think TI, HP, and National Semiconductor calculators and LED watches). But rapid expansion into mainstream electronic products

became so pervasive that it became difficult, if not impossible, for an OEM or semiconductor company to be "all things to all people." The outsourcing business model therefore emerged, giving rise to the OSAT industry in the 70s and 80s, and the foundry industry by the early 90s. As product development and manufacturing costs became more obtrusive, further diversification of the semiconductor industry into "fabless" companies that outsourced all of their manufacturing requirements (wafer fabrication, packaging, and assembly) emerged. And as costs continued to escalate while product life cycles became shorter, the electronics industry transitioned further away from vertically-integrated companies (IDMs and OEMs) to that of companies based upon outsourcing manufacturing and other "non-core competencies."

So, there you have it. OEMs disappeared, replaced by original design manufacturers (ODMs). ODMs were replaced by virtual ODMs. Now the virtual ODMs are virtual OEMs, while EMS, OSAT, and foundry morph into vertical electronic outsourced services companies, controlling the entire supply chain. Further down the road one could even see them offering their own internal brand (i.e., generic) name in the future (similar to grocery store house brands).

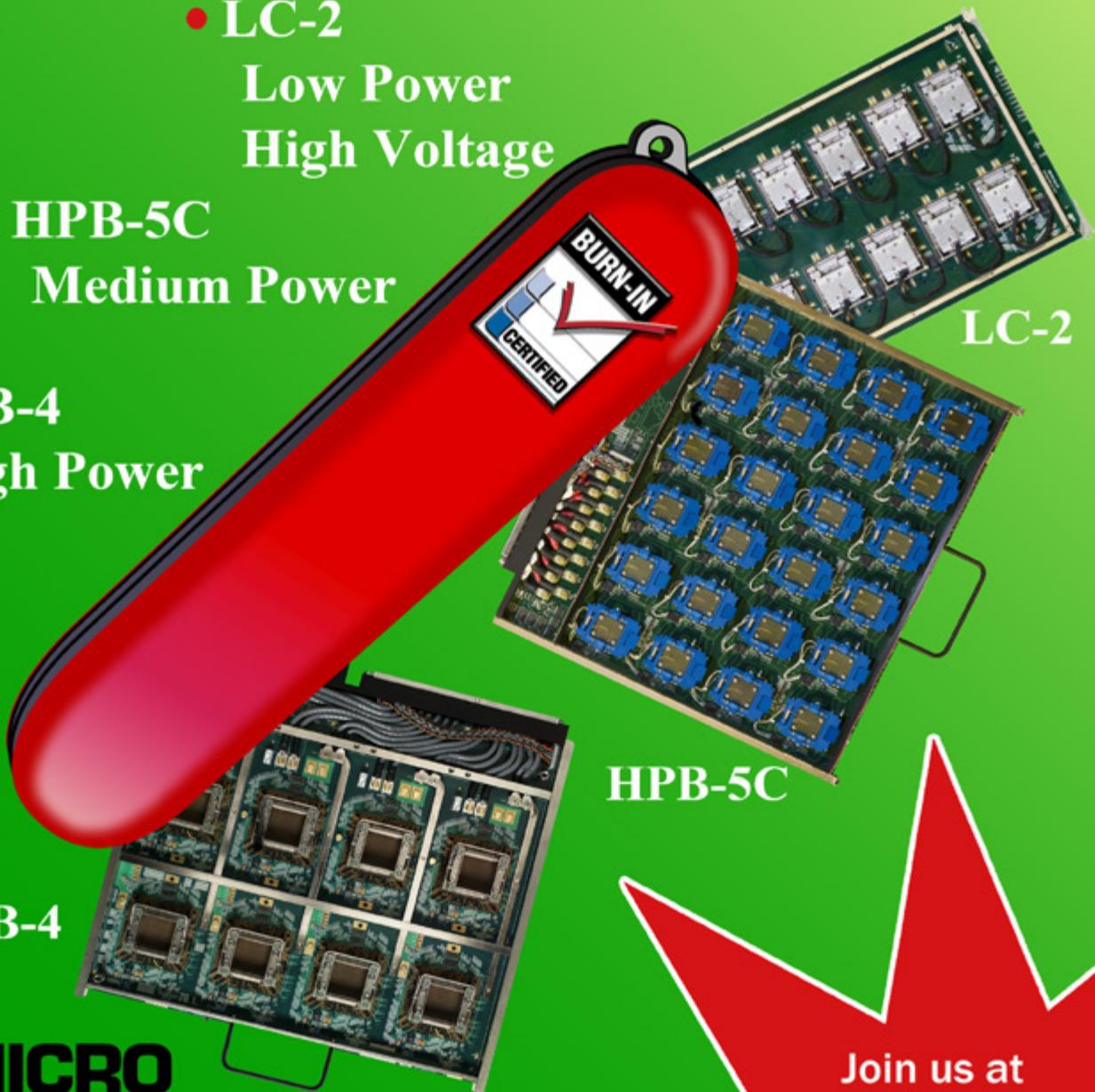
The shift to the vertically-integrated design/manufacturing outsourcing model is now under way. Electronic product manufacturers are recognizing the added benefits available from using this type of service provider with a vertically-integrated, outsourced business model.

Biography

Jim Walker received his BS in Chemistry from California State Polytechnic U., Pomona, with post-graduate studies at California State U., Los Angeles. He was co-founder of the Surface Mount Technology Association (SMTA) and recently retired as VP of Semiconductor Manufacturing Research for Gartner. Jim currently is President of World Level Packaging Concepts; email maseratijim@gmail.com

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50 years past, present and future

This year, Leti celebrates its 50th anniversary. CSR asked Leti's CEO, Marie Semeria, to discuss the high points and important milestones in its history.

Photo credit: Pierre JAYET/CEA

Leti, a CEA Tech research institute, is celebrating its 50th anniversary this year. Founded in 1967 as an electronics research division of the French Atomic Energy Commission, Leti evolved into a global leader in bridging the gap between basic research and commercial technologies by transferring its R&D results to industrial partners and startups.

With an annual budget of €315 million and a staff of 1,900 researchers, Leti works closely with its industrial partners on projects ranging from prototype development to pre-production. Solutions target a wide variety of sectors, including sustainable transport systems, telecommunications, health, consumer electronics, energy and environment, smart cities, defense and security and space.

Looking by turns into the past and the future, Leti CEO Marie Semeria offers a wide-ranging view of the history of microelectronics development and a forecast of the medium-term future.

Q. What milestone innovations have defined Leti's history?

A. Our researchers have been innovating for 50 years in multiple fields, including CMOS circuits, packaging and imagers, among other high-tech areas. A number of technologies pioneered by our team have enjoyed worldwide success. Silicon-on-insulator (SOI) is an outstanding example, which led to the founding of Soitec by two Leti researchers in 1992. SOI technologies developed jointly with STMicroelectronics and Soitec have established a prime platform for the Internet of Things (IoT) and the consumer market, which is becoming today's worldwide benchmark. We find these technologies in smartphone communication modules, positioning systems and cameras.

We are also a reference for infrared detectors, having initiated the creation of Sofradir, whose products are integrated into observation systems for security here on earth

and for tracking the cosmos. For 30 years, we have continuously extended our in-depth knowledge and skills in relation to MEMS, thereby placing it at the heart of the IoT. Among foundational patents, in addition to those pertaining to SOI and accelerometers, we can cite our patent on liquid crystal flat screens, which has clearly had a worldwide impact. This technology widens the reading field and is implemented in many monitors used in every walk of life. From the earliest days, we have worked on through-silicon vias (TSV) and on bonding methods in relation to packaging. Today, we possess a range of technologies and in-depth expertise in both 3D and 2.5D integration. Finally, each year, we launch between five and six start-up projects. Technologies recently developed by our startups, such as Aledia (LEDs), Wavelens (variable focus optical lenses on silicon) or Avalun (portable biological analyzers), are perhaps tomorrow's global standards.

Q. What are Leti's specific strengths?

A. We are an innovation institute. Our driving force is the development of technologies that can be industrialized and contribute to a country's competitiveness and to society's progress. Right from the start, the mission of the institute was to innovate and transfer its innovations to industry or to create startups to market them. This mission is founded on values transmitted from one generation of researchers to the next. Obtaining innovative, industrially usable results materializes our pioneering "spirit." Our collective motivation is embodied by teamwork, and includes working with our industrial or academic partners. Our agility is based on vigilance with regard to everything that happens outside the institute, on our dissatisfaction with the status quo, and on knowing how to accelerate or stop a project to start out on a more promising avenue of research. Another specific feature is our capacity for bringing together a wide variety of technologies: CMOS, sensors, communication systems,

packaging and 3D integration, power electronics, imagery, integrated circuits, and many more. Furthermore, we embrace a melting pot of technologies. This diversity is reflected in our 350 industrial partners ranging from equipment manufacturers and component makers to system designers; for example, we work with major groups such as Safran and Renault. In this respect, we are capable of building an entire project value chain in cooperation with a partner or partners. For example, in power electronics, our know-how extends a single chip to the entire vehicle. We also believe our overarching strength is the capacity to lead projects right through to pre-production stage in cooperation with manufacturing partners.

Q. What markets will drive technological development in the coming years?

A. We are a core player in developing the IoT and in making devices portable, reliable and secure. Technologies associated with IoT generate high performance in terms of data processing power and electricity consumption, while ensuring communication between devices and with the Cloud. 5G communication network infrastructure and full data-cycle security from sensor to service are two conditions governing the success of mass IoT deployment. SOI is the key technology in all these applications, as are 2.5D and 3D integration technologies. We have recently demonstrated integration of antennas and RF circuits with our silicon interposer technology. In parallel with miniaturization that allows computation capacity gains, integration of functions such as RF, onboard memories, sensors, packaging strategies and distributed logic architectures will be decisive in the new applications prompted by digitalization.

Automobiles represent just one of the high-stakes industrial sectors that have been transformed by electronics and digital technology. Advanced driver assistance systems, GaN power electronic components

and augmented reality systems are all examples of new Leti developments. The challenge in medical devices is to develop new diagnosis or therapeutic protocols that address chronic diseases such as respiratory insufficiency, diabetes, etc., by taking advantage of sensor and data processing technologies to promote care personalization. The IoT, automobile and connected health sectors are complemented by the data center, server and high-performance computing markets, in which Leti is active via an avant-garde roadmap combining photonics, 3D integration, interposer and new computation and memorization architectures.

Broadly speaking, we develop digital technologies and integrate them into the future products of our partner subject matter experts (SMEs), start-ups and major groups. High-tech and evolving conventional sectors are increasingly relying on technology to differentiate themselves and gaining competitive advantage. Our teams are catalysts for these transformations.

Q. What will be Leti's new R&D areas?

A. Artificial intelligence is a major area of research for us. Implementation of deep learning methods effectively assumes development of new circuit concepts combining computation and memorization functions (like brain neurons). 3D packaging technologies will play a key part in this evolution. Similarly, quantum computing technologies are mobilizing our teams to provide solutions to tomorrow's complex problems involving massive amounts of data. With our colleagues at Inac (a CEA-affiliated laboratory), we were the first organization in the world to demonstrate qubit technology based on silicon nano-threads, implementing a 300mm-compatible CMOS manufacturing process. These new intelligence paradigms require us to combine a system approach with a technological approach. In conjunction with partners IdEx Grenoblois at the Université Grenoble Alpes, we are preparing to underpin France's strong participation in the future Flagship Quantum, the European Union's major initiative on quantum technologies. Virtual and augmented reality are also key development areas for us on the cutting edge of localization, visualization and security technologies. Finally, cybersecurity represents one of the technological issues critical to large-scale deployment of the IoT. Security of all connected devices,

hard-ware, communications and data must be ensured to develop such services. We are contributing to the hardware and onboard software elements. In the majority of the sectors in which we will work, whether it be the IoT, the car or connected medicine, our 2.5D and 3D packaging technologies will be used to combine logic circuits, memories and photonics to create high-performance, low-energy consuming systems enriched with communication, memorization and security functions.

Q. What resources will you allocate to these projects?

A. Facilities that allow us to continue our technological advances are essential. This year, our clean rooms will be fully equipped. There are only two or three similar installations worldwide. Low-temperature epitaxy equipment, operated in partnership with Applied Materials, enables deposition of films just a few atoms thick based on a "cold" process that is compatible with the back-end. This can be used to produce 3D monolithic circuits based on Leti's CoolCube™ technology, for example. In partnership with the Japanese company SCREEN Semiconductor Solutions, we will install laser annealing equipment, allowing us to activate doping agents in thin surface layers. We are also setting up a bonding process that ensures highly accurate alignment in conjunction with EVG. This is key packaging technology, in which one can position one chip on another or one device on another. Technological research requires an equipment platform at the cutting edge of the latest global standards. Another condition for accomplishing these ambitious projects is being able to build capacity, so we can initiate long-term research in advance of the industrial-need stage. Ten to fifteen years of research and pre-industrialization are required to reach production stage. Investigating new avenues with our academic partners and Ph.D students is indeed essential.

Q. What role do manufacturers play in paying for Leti's programs?

A. Industry participation is crucial in terms of not only our funding, but also our rationale and very reason for growth. We share this founding principle within CEA Tech and within the Instituts Carnot network. More and more manufacturers come in search of differentiating solutions that are frequently at the intersection of different fields of

expertise. External resources, therefore, underpin growth in our activity. Eighty-five percent of our 315M€ budget comes from external sources and the remaining 15% is ensured by subsidy provided by the CEA, our governing body. Corporate contracts constitute half of our external financing. The other half is provided by European or national cooperation projects. Thanks to our international visibility, we have signed partnership agreements with major stakeholders, including IBM, Intel, Applied Materials and others, and further agreements are in the pipeline. We have to work with global technology leaders and create start-ups to maintain our position at the cutting edge of innovation. This is absolutely essential because only world leaders are capable of funding the highly advanced technological research conducted by Leti. STMicroelectronics, Soitec and Sofradir, which were launched with or grew because of Leti innovations, are world leaders in their fields. We must develop technologies that will enable these companies and others to continue the competitive differentiation in the long term. Similarly, SMEs need to differentiate themselves, while controlling costs and winning export market share. For years, fabless was en vogue. Today, everyone is aware that it is important to design and produce components at home, in France and Europe, to generate wealth and jobs. The French semiconductor industry is strategic, and a prerequisite for our sovereignty. We realize that the semiconductor industry is not simply CMOS! It is also imagers, infrared detectors, power electronics, sensors, etc. European manufacturers are well placed in these growth sectors, which are founded on "More than Moore" technologies. While conserving its expertise in the most advanced computing technologies (More Moore), we support our industry partners in their More than Moore strategies and help to develop the technologies behind their future products. It is here that Leti holds a strong hand in France and Europe.

Q. How is Leti positioned on More than Moore and on packaging, specifically?

A. Packaging plays a central role in More than Moore. We have developed a range of expertise in 3D integration. CoolCube™ is our latest 3D integrated circuit technology. We also have complete command of 2.5D or 3D chip assembly for building possibly heterogeneous sub-systems (comprising different chip types). This curtails size,

interconnection distances and electrical losses. In 2.5D integration, we rely on the silicon interposer, which is suitable for very high-density interconnections and has the advantage of being compatible with microelectronic processes. Wafer-level-packaging fan-out technology is in full development at Leti. We also participate in the EuroPAT-MASIP project, which brings together 28 partners for the development of new packaging, assembly and testing solutions to improve the competitiveness of European industry.

Q. How did Grenoble (France) become a leading global center for micro- and nanotechnologies?

A. Grenoble concentrates world-class technological research, academic laboratories of established excellence, and a vigorous industrial fabric on its Minatec (Micro and Nanotechnologies) and Giant (Grenoble Innovation for Advanced New Technologies) campuses. This combination forms an ecosystem whose dynamism continues to thrive. The strength of Grenoble's ecosystem

is such that even corporate acquisitions by foreign stakeholders can be reflected by growth in local activity. A typical example of this phenomenon was Leti's start-up Movea (movement detection systems), bought by American company InvenSense, which was itself bought by Japanese group TDK. Each time, the buyer is attracted to the dynamism of Grenoble's ecosystem and expands its local activity. Grenoble is an expanding open ecosystem, which is attractive and rewarding to companies and all those who seek to create and develop future communication and intelligence technologies here.

Leti: developing solutions for manufacturers

Leti is one of three institutes in CEA Tech, a division of the Commissariat à l'Energie Atomique, CEA, a global, government research organization. At Leti's headquarters in Grenoble, France, 1,900 researchers develop micro and nanotechnologies for solutions and applications supporting multiple industries and sectors, from the Internet of Things (IoT) to high performance computing and autonomous vehicles. A hundred people in laboratories in Leti's campus focus on packaging, specifically developing innovative solutions for 3D microsystem integration.

Leti develops technologies that meet market needs from feasibility studies to proof of concept. Working closely with its 350 industrial partners (major international groups, subject matter experts and start-ups), Leti leads projects ranging from prototype development to pre-production. Developed solutions target a wide variety of sectors: sustainable transport systems, telecommunications, health, consumer electronics, energy and environment, smart cities, defense and security and space.

Leti has formed partnerships with world leaders of industry including IBM, Intel, Qualcomm, Applied Materials, Panasonic, Murata and many others.

Pioneering achievements

Silicon-on-insulator (SOI). Leti pioneered SOI technology and transferred it to Soitec in 1992. In 1997, Leti transferred MEMS-on-SOI technology to Tronics and, in 2011, it transferred fully-depleted silicon-on-insulator (FDSOI) technology to STMicroelectronics. FDSOI's first major application, a GPS circuit in a connected watch, was first marketed in October 2016. SOI technologies developed jointly with STMicroelectronics and Soitec have established a prime platform for the IoT.

Cutting-edge packaging technologies. Leti has developed interconnection and packaging, back-end, technologies in parallel with its R&D on the process front end component since the 1990s. Today, its know-how is implemented in 3D (fan-out wafer level)

Leti by the numbers

| |
|------------------------------------|
| 1967: founded in Grenoble (France) |
| CEO: Marie Semeria |
| 1,900 researchers |
| 91,500 sq. ft. of clean rooms |
| 315M€ annual budget |
| 350 industrial partners |
| 2,700 patents held |
| 700 publications per year |
| 60+ start-ups created |

and 2.5D (silicon interposer) packaging methods. The institute also develops chip-on-flex assembly methods for medical and textile applications. Photonics-on-silicon are part of Leti's key approaches to increasing interconnection flow rates.

A look back in time

Figure 1 shows the first transistor developed by Leti in the late 1960s. **Figure 2** shows Leti's Lab Ion Implantation experiments in the 1970s. **Figure 3** was taken in Leti's clean room today.

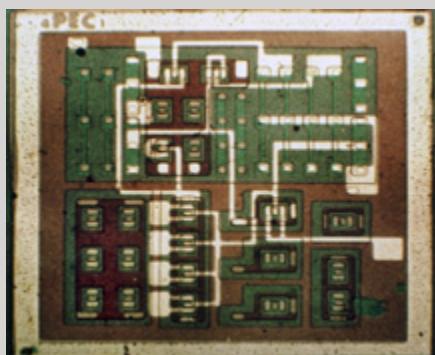


Figure 1: First Leti transistor.



Figure 2: Leti Lab ion implantation experiments in the 1970s.



Figure 3: Leti's clean room today. Photo credit: Pierre JAYET/CEA

Process challenges for temporary bonding materials in fan-out packaging

By Ramachandran K. Trichur, Tony D. Flaim [Brewer Science, Inc.]

The semiconductor industry has been experiencing steady growth since 2010, and the outlook continues to be positive for the industry with the application space for microelectronic devices opening up in high-performance computing, mobility, autonomous driving, wearable electronics, communications, connected devices, healthcare, and much more. Moore's law, which predicted the performance of devices until the recent past, is no longer able to predict performance just by scaling, and now performance is extended using advanced architectures in device packaging. Consequently, advanced packaging has progressively become a core technology to address the needs surrounding performance, cost, and form factor of electronic devices.

One of the recent developments in packaging technologies is fan-out wafer-level packaging (FOWLP). Although early forms of fan-out packaging technology have been commercially deployed for the last few years, outsourced semiconductor assembly and test services (OSATS) and foundries are now developing more advanced forms of fan-out technology for heterogeneous integration and system-in-package (SiP) applications. The advanced fan-out technology currently includes several variants and the final choice of technology used to package the devices is determined by the end application and various other factors including cost, performance, size, and time to market. A common thread in most of the advanced fan-out architectures is the use of temporary bonding and debonding (TBDB) technology as a fundamental element in the manufacturing of the devices.

The temporary bonding process consists of reversibly mounting a device wafer to a carrier substrate with a polymeric bonding material and a release layer. The bonding material and the carrier substrate mechanically support

the device wafer during thinning and subsequent backside processing. Primary design objectives of the bonding material and release layer are to withstand the high stresses created by thermal cycling, coefficient of thermal expansion (CTE) mismatch, mechanical grinding, vacuum processing, and a host of other factors, while remaining easily separable at the end of the process. The choice of the bonding material and the release layers are dependent on the target application and process requirements. Common release mechanisms used for debonding the wafers are mechanical, thermal, solvent and laser release. **Tables 1** and **2** show the various generations of temporary bonding materials and release layers offered by Brewer Science to support the advanced packaging market.

FOWLP technology

The manufacturing process for devices using FOWLP technology, in a broad sense, falls under two categories: chip-first fan-out processes, and redistribution layer (RDL)-first fan-out processes [1]. In both of these architectures, a carrier-assisted process is required for construction of the devices. The chip-first fan-out process utilizes a wafer reconstruction process in which known-good dies (KGD) from the original device wafer are picked and placed on a substrate and then over-molded with an epoxy molding compound and cured to

| Technology Generation | Bonding Material | Use Range | Targeted Applications |
|-----------------------|---|-----------------------------------|-----------------------------------|
| Commercial | GEN 1 WaferBOND® HT-1010 | Up to 200°C | 3-D IC, Compound semiconductors |
| | GEN 2 BrewerBOND® 220 | Up to 200°C | Compound semiconductors |
| | GEN 3 BrewerBOND® 305 | Up to 250°C | FOWLP, 3D-IC |
| Developmental | GEN 3+ Beta stage products | Multiple ranges < 275°C & < 350°C | FOWLP, 3D-IC, MEMS |
| | GEN 4 Experimental Products | 250°C – 400°C | FOWLP, die-wafer bonding, memory |
| Laminate Systems | Various compositions in dry film format | Multiple ranges | All applications including panels |

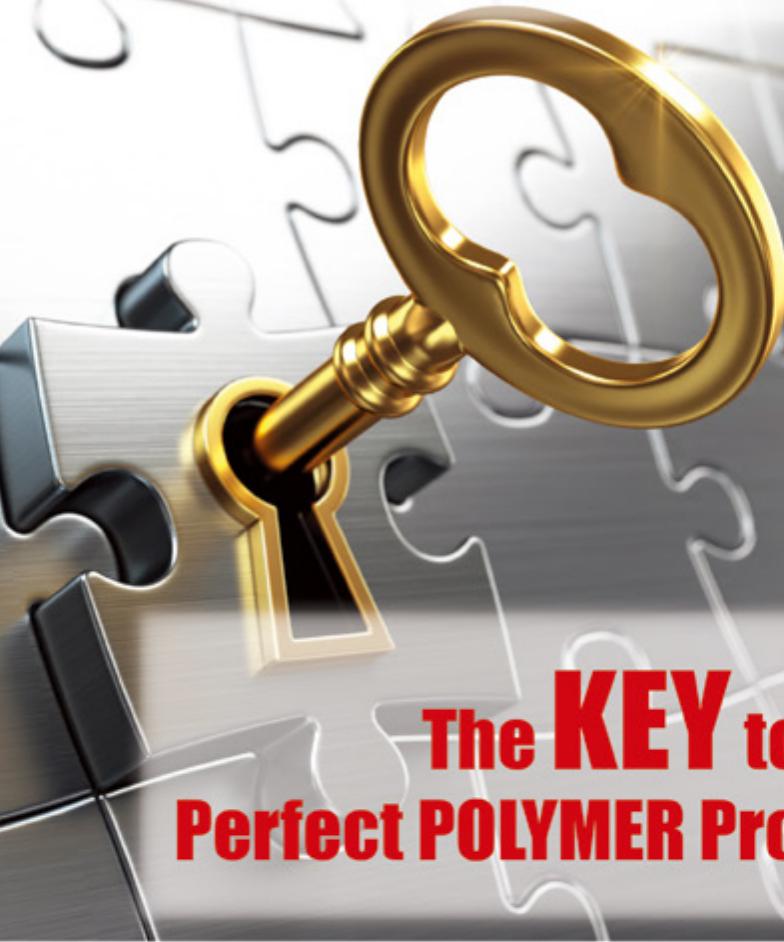
Table 1: Brewer Science temporary bonding material generations and target applications.

| Release Layer Materials | Material Type | Mode of Release | Targeted applications |
|-------------------------|---|-----------------|---|
| BrewerBOND® 510 and 510 | Ultrathin surface treatment | | Mechanical Release 3-D IC, Chip-first FO, compound semi |
| BrewerBOND® 701 | Very-high-temperature-stable, thin (150-nm) polymer coating | | Sensitive to 248-, 308-, and 355-nm laser systems 3-D IC, Fan-out |
| Experimental Products | High-temperature-stable, thin polymer coating | | Sensitive to 248-, 308-, and 355-nm laser systems RDL-First FO, 3-D IC |

Table 2: Brewer Science release layers and target applications.

create a heterogeneous and highly stressed substrate known as a reconstituted wafer. Subsequently, the reconstituted wafer is temporarily bonded to a carrier to flatten inherent bow before being further processed to fabricate RDLs on the wafer. In an RDL-first fan-out process, the RDL layers are built on top of the carrier wafer coated with a temporary bonding material, then the KGDs are placed on top of the known-good RDL layers followed by molding and mold-grinding processes. In both of these process flows, the wafer stack typically goes through metallization, photolithography processes, dielectric deposition, electroplating and other assembly processes. Literature points to multiple variations under these two broad categories, with die face-up, die face-down, RDL fine-line first, and RDL coarse-line first type architectures that add to the complexity and requirements of the materials and equipment supporting the process.

FOWLP Engineers

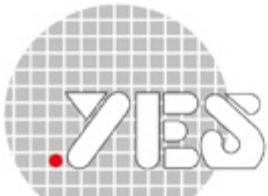


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Chip-first FOWLP. Figures 1 and 2 show general schematic process flows for a chip-first FOWLP process using either the die face-down or die face-up approach, respectively. The first step in both of these techniques is the fabrication of the reconstituted mold compound wafer as described previously. If the reconstituted wafers are thinner than 350 μm , these wafers exhibit severe bow due to large internal stresses, and a high-temperature-capable temporary bonding material is essential to support the reconstituted wafer through the process flow [2]. If the wafers are unsupported, it causes handling problems in equipment and registration errors during alignment for photolithography. Once the reconstituted wafer is bonded to a temporary carrier, the bow is greatly reduced or eliminated. Figure 3 shows an example of the bow in a mold-compound wafer before and after bonding to a temporary carrier wafer.

In the process flow depicted in Figure 1 for the die face-down approach, the reconstituted wafer is formed on the first carrier by over-molding the dies on a double-sided tape. Then the reconstituted wafer is transferred to a second carrier for subsequent RDL processing. The schematic in Figure 2 for the die face-up approach shows a single-carrier approach, where the reconstituted wafer is formed on the carrier coated with the high-temperature-capable temporary bonding material. Alternate process flows using a two-carrier approach are also viable.

Subsequently, the bonded stack consisting of the carrier wafer, temporary bonding material and the reconstituted wafer goes through RDL formation on top of the exposed die pads. Each layer of the RDL process involves seed layer deposition, photolithography, electroplating, photoresist removal, copper etching, polyimide or dielectric material coating, patterning and curing. For a multi-layer RDL formation, these process steps are repeated several times to fabricate the multiple RDL layers. During the RDL formation process, the temporary bonding material is exposed to temperatures of up to 250°C for several hours and the bond line is exposed to a variety of process chemicals including harsh acids, alkalis, and solvent chemistries.

The wafers are subsequently debonded and the device wafer is subjected to a solvent cleaning step to remove the temporary bonding material from the wafer surface. For debonding the carrier wafer, mechanical release and laser release are the preferred methods, although thermal slide debonding could be applicable in certain cases.

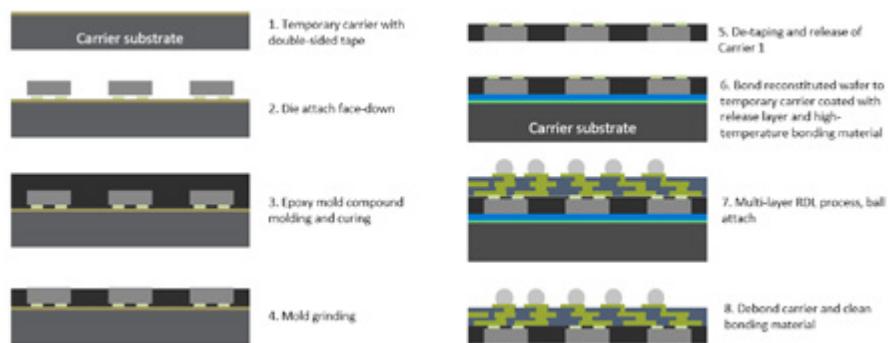


Figure 1: A general schematic process flow for a chip-first die face-down, fan-out process.

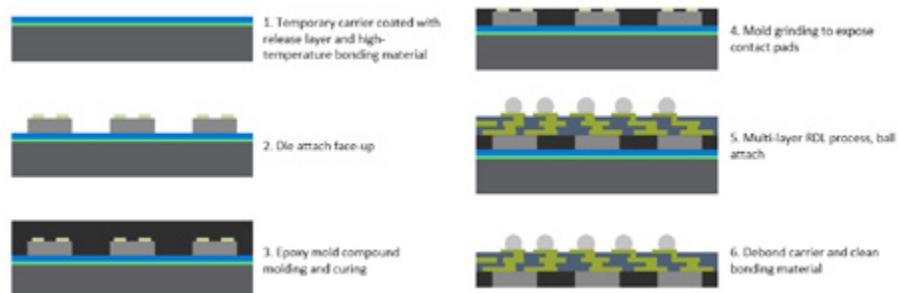


Figure 2: A general schematic process flow for a chip-first die face-up, fan-out process.



Figure 3: Bow experienced in a mold compound wafer before and after temporary bonding.

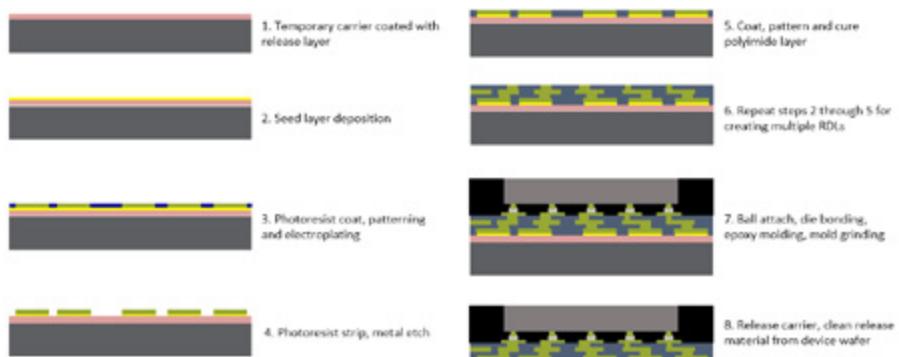


Figure 4: A general schematic process flow for a RDL-first fan-out process

RDL-First FOWLP. Figure 4 shows the schematic drawing of an RDL-first FOWLP process. Here, the processes for the RDL layer and the assembly processes for die attach are done on a temporary carrier coated with a sacrificial release layer. Typically, a glass carrier is coated with a release layer and then a series of process steps, as noted in the chip-first process, is completed for creating the RDL layer. These steps are repeated

multiple times to create a multi-layer RDL structure. After the RDL process is completed, the wafers go through assembly process steps involving die attach, molding and mold grinding, followed by carrier release. The preferred method for carrier release on a wafer level, for RDL-first type processes, uses a laser release mechanism.

In comparison to the chip-first process, the RDL-first process is harsher on the



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|--|---|
| <ul style="list-style-type: none"> • Si wafer bonding • Si wafer thinning • Plasma enhanced chemical vapor deposition (PECVD) • Photolithography • TSV etch • Oxidation • Seed layer deposition • Electroplating • Chemical mechanical polishing • Debonding | <ul style="list-style-type: none"> • Glass, ceramic or alternate carriers* • High-stress reconstituted wafer bonding* • Seed layer deposition • Photolithography • Electroplating • Polyimide or dielectric material coating (open face* and/or bonded state) • High-temperature curing for up to 10+ hours* • High-pressure molding and mold grinding* • Large area panel processing* |

Table 3: Comparison of standard backside process flows using TSV creation on silicon wafers and fan-out packaging. Processes with an asterisk (*) indicate a specialized process needed for fan-out devices.

sacrificial release layers because the full face of the release layer is open to process chemicals during the early steps of RDL formation. The release layer needs to have good adhesion to metal seed layers and/or polymer dielectric layers depending on the specific process flow. The release layer must also have good chemical resistance against photolithography chemicals, metal etch chemistries, and various other solvents in open-face testing. Moreover, the release layers need to withstand high-temperature processing during polyimide curing steps for extended periods and avoid flowing during high-temperature and high-pressure process die-attach processes and epoxy molding of the dies.

Material requirements for FOWLP

Table 3 provides a list of typical process steps for TSV creation on a silicon wafer as compared to processes used in fan-out packaging. The table also identifies the specific unit processes in a fan-out process flow that are challenging to the temporary bonding materials. Certain process steps in FOWLP processing are markedly different from process steps used during wafer thinning and the TSV creation process for silicon wafers. These process challenges are explained in the sub-sections below.

Internal stress and bow. The temporary bonding materials encounter highly stressed reconstituted wafers with bow and warpage of several millimeters along the wafer edge [2]. The residual internal stress and bow are due to the heterogeneous construction of the wafers with silicon and epoxy, as well as to the coefficient of thermal expansion (CTE) mismatch between the silicon dies ($2\text{-}3\text{ ppm}/^\circ\text{C}$) and epoxy mold

compound ($\sim 7\text{ ppm}/^\circ\text{C}$). The temporary bonding materials are required to have strong adhesion to the reconstituted wafer to maintain the flatness after bonding and the thermomechanical properties of the bonding material should assist in eliminating bow and warpage of the bonded stack during high-temperature downstream processes.

Exposure to process chemicals. In all of the silicon wafer processes involved in TSV creation, the first step is to bond the device wafer to the temporary carrier. In this instance, only the bond line of the temporary bonding material is exposed to process chemicals in the subsequent steps. However, in the case of RDL-first fan-out processes, the whole face of the sacrificial release layers may be exposed to the process chemicals used for photolithography, electroplating, metal etch, and others during the initial steps for RDL creation. So, the release layers used to support the RDL-first build-up processes need to withstand and support much harsher chemical exposure conditions without any impact to the process steps. For example, the release layers must not leach into or contaminate plating baths, must not be removed by photoresist strip chemicals, and must be compatible with organic layers similar to photoresists or polyimides that could be coated directly on top of the release layers.

Temperature cycles. In both chip-first and RDL-first fan-out processes, multi-level RDL stacks are created on the wafer while bonded to a temporary carrier. During the creation of RDLs, the polyimide layers are coated and patterned on the wafer. The polyimide layers undergo long curing steps for up to 3 hours at elevated temperatures of 230°C or more. So, if the device wafer has a 5-layer RDL structure, the temporary bonding material has

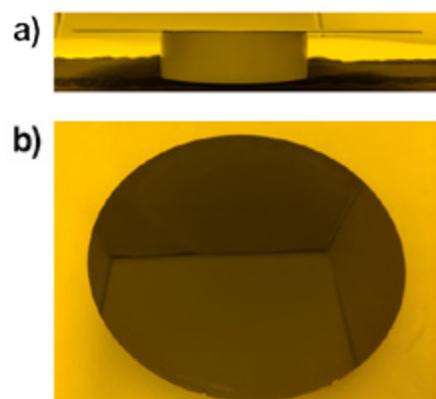


Figure 5: Image of a highly stressed mold-compound wafer bonded to a glass carrier using a developmental temporary bonding material after exposure to 250°C for 1 hour. a) Side view showing no bow after thermal treatment; b) A confocal scanning acoustic microscopy (CSAM) image showing no voiding or delamination.

to withstand 5 cycles of 230°C + temperatures for 3 hours. **Figure 5** shows the process survivability of our developmental temporary bonding material. The material was coated and bonded to a reconstituted wafer using a glass carrier and then subjected to heat treatment up to 250°C for 1 hour.

Mechanical stability at high temperatures. To realize a higher level of integration and performance in future devices, the technology roadmap for fan-out packaging is moving towards 2.5D, 3D fan-out system-in-package (SiP), and 3D package-on-package (PoP) architectures [3]. Process flows used to realize these device packages are much more complex than 2D fan-out architecture process flows described in previous sections. These advanced applications usually require RDL processes on both sides of the package where additional dies are attached on top to increase the levels of integration. This requires high accuracy for die placement in both levels to avoid alignment errors between dies, interconnects, and RDLs in the two levels, i.e., no movement in x, y, z, or θ direction in dies after attaching to the temporary carrier during processes involving high temperature and pressure. The RDL line-space (l/s) is targeted at $2\mu\text{m}$ for high-density fan-out, and any movement in the bonding material will cause the dies to move, resulting in poor alignment and device failure after completion of assembly, resulting in a yield hit.

Molding pressures. In RDL-first fan-out processes, the temporary bonding material coated on the carrier wafer is subjected to high pressures at elevated temperatures during the transfer molding process for packaging of the

die. The epoxy molding compound is transfer molded onto the dies at 100s of kN pressures, usually at an elevated temperature of ~150°C and subsequently cured at an elevated pressure. The temporary bonding material should not ooze out of the bond line during these processes and cause contamination. A high-temperature-compatible, mechanically stable bonding material is required to withstand the molding process.

Complex process flows using dual-side temporary bonding. The process flow for advanced 2.5D and 3D fan-out architectures could also involve a wafer flip process to create RDL layers on both sides of the wafer. For example, in a chip-first fan-out process, a temporary carrier is attached to the backside of the reconstituted wafer to form RDL layers on the frontside. Once all the RDL layers are completed on the frontside, another secondary carrier is attached on top of the RDLs and the first temporary carrier is debonded independently from the backside. The first temporary bonding material is cleaned from the backside and then RDL layers are built on the backside. Through-mold vias (TMV) and Cu-pillar interconnects are commonly used to connect the frontside RDL to the backside RDL, thereby interconnecting the packaged devices on both levels to the board.

Panel-level architectures. Industry roadmaps predict that fan-out architectures will quickly progress to be in high-volume manufacturing using a panel format to lower manufacturing costs and to support the demand for devices requiring a high level of integration for increased performance and smaller form factors. The materials used for temporary bonding and debonding will need to be compatible with coating methods, application processes, and tools involved in the panel assembly lines. Panels are not radially symmetrical and are very large compared to a 300mm silicon wafer, therefore spin coating processes used on the wafer side are not compatible, nor efficient for coating large panels. Therefore, design modifications are required in the formulation of temporary bonding materials to simplify the application process for panel formats. The bonding materials need to be applied either by using large-area liquid coating methods like spray coating, slot-die, or drawdown bar coating, or by offering a more suitable format of materials like laminate or dry film to be compatible with panel-level application processes.

Debonding processes. The debonding processes used for panel-level applications

are in their infancy. Laser debonding seems to be a preferred route for panel format, but the ecosystem for materials, tools and processes is still in development. In general, there is considerable opportunity for simplification and improvement of debonding processes for fan-out wafers and panels. Unlike silicon wafers, reconstituted wafers and panels are not brittle and are not prone to edge chipping or crack propagation, which are significant and common failure mechanisms seen in silicon wafer processing. Hence, during the development of TBDB technologies for silicon wafer processes, a great amount of engineering resources was spent on developing the materials, tools, and processes to minimize occurrence of cracks or chips on the wafer edges that can result in breakage and yield loss. Processes like edge trimming of device wafers, use of larger carriers, low-stress debonding, and engineering of specialized debonding fixtures were used to avoid damage to the device wafers. These specialized processes and tools have significant cost implications to the overall process. Reconstituted wafers and panels, on the other hand, are not brittle and may be more forgiving while handling during the downstream processes. Newer methods for debonding could be envisioned on the horizon that will ultimately simplify the debonding process and reduce the cost of the fan-out manufacturing processes.

From the above list of the challenges for TBDB materials used in fan-out architectures, it is abundantly clear that one product or one family of materials may not be suitable for all temporary bonding processes used in the advanced packaging applications. The materials used for silicon wafers for thinning and TSV processes face a different set of requirements compared to materials used for fan-out processes. The specific requirements in the fan-out process flow present multiple unique challenges to the temporary bonding materials used for fan-out packaging, thus requiring specialized engineering of the materials, tools, and processes.

Summary

We have identified the specific requirements pertaining to process temperatures, chemical compatibility, debonding method, substrate compatibility, substrate size, and other factors that guide the selection of a bonding material. A single type of temporary bonding material and release material is no longer enough to suit the variety of fan-out process flows that are being developed; rather, a portfolio of bonding

materials and release layers are needed to support all these evolving processes to provide a robust, high-yielding, cost-effective, and simple solution to the industry.

As the value and interest in FOWLP architectures continue to grow, processes are being developed and commercialized in both foundries and OSATS with temporary bonding and debonding technology used as the foundation for building the structures. Gradually, the line between traditional packaging houses and foundries is beginning to blur, especially when wafer-level processes are used for advanced packaging of devices for fan-out architectures. Because the end application space requiring devices with high performance and a high level of integration is continuing to expand, the opportunity for fan-out technology appears to grow at a strong pace. It implies that a significant portion of wafer-level fan-out manufacturing will be moving towards panel-level fan-out manufacturing for supporting the demand and to lower the manufacturing costs. While the ecosystem for panel-level fan-out is still in its early stages, more evolution can be seen in the coming years for materials, processes, and equipment technologies used for panel fan-out manufacturing.

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Biographies

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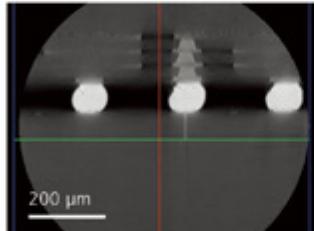
Tony D. Flaim received his PhD in Physical Chemistry from the U. of Missouri-Rolla and BA in Pre-Medicine from the U. of Missouri-Columbia and is the CTO at Brewer Science, Inc.

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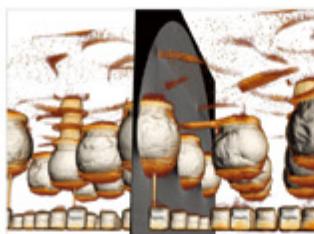
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Advances in failure analysis techniques for 3D technology

By Ingrid De Wolf, Kristof J.P. Jacobs [imec/KU Leuven]

Finding the location of failures in microelectronic chips, and understanding their root cause, is of high importance for the microelectronics industry. Failure analysis (FA) helps to optimize the product, prevent future failures, guarantee reliability, and reduce cost.

Failures in microelectronics are typically detected as “an electrical signal deviating from specifications.” To be able to understand the cause of a failure, one has to first localize it. In the FA domain, this is generally the most challenging task. There exist a large variety of techniques that can be used to localize failures, of which the most common ones include: X-ray imaging and scanning acoustic microscopy for package-level failures, photon emission microscopy and laser voltage probing for chip-level failures [1]. **Figure 1** shows a cartoon visualizing the difficult task a FA-engineer has to perform to select the optimal failure analysis technique.

Not only the “nanoturization” of active



Figure 1: Cartoon showing the difficulty of selecting the optimal failure analysis technique.

devices in the front-end-of-line (FEOL) and interconnections in the back-end-of-line (BEOL) raises concerns for failure analysis, but also the expansion into the third dimension. New structures such as micro-bumps, through-silicon vias (TSVs), thin chips, interposers, etc., add risks and failure mechanisms, and mechanical and thermal issues (e.g., chip package interaction) become much more important.

Failure analysis techniques

Although many of the commonly used failure analysis techniques remain applicable for 3D, there is a high demand for technique improvement and for new techniques to find failures in a stack of thinned chips, interconnected by TSVs, micro-bumps and Cu pillars. In the following sections, we first review the evolution and adaptation of two techniques that are commonly used in failure analysis: X-ray imaging and scanning acoustic microscopy (SAM). Next, we discuss some new evolutions of electro-optical (EO) and thermal-based techniques. Of course, there are many more systems that can be applied for 3D failure analysis [1-3].

X-ray imaging

X-ray imaging is traditionally used for package and board-level failure analysis. The well-established 2D and micro-computed tomography (μ CT) X-ray techniques rely on geometric magnification, whereby positioning the sample closer to the X-ray source results in a higher magnification. For tomography, the sample needs to rotate, limiting the resolution depending on the sample size. This is less of an issue for 2D imaging, but also one has to work under an oblique angle to image, for example, a TSV along its full length, which limits the magnification. This can partly be solved by tilting the detector instead of the sample. Other in-between solutions exist, where a rotating detector, tilted with respect to the source-sample axis, is used to capture 2D images and reproduce a 3D image of the sample (partial μ CT) [4]. The in-plane resolution is slightly less than what can be obtained in 3D- μ CT, but the depth resolution is generally very good, even at the wafer level, and the technique does not suffer from projection distortion. In any configuration, the X-ray imaging and μ CT remain very valuable for 3D technology.

A major advantage of X-ray imaging over cross-sectioning by mechanical or focused ion beam (FIB) means, and imaging in a scanning electron microscope (SEM), is that it is non-destructive and allows one to image a larger field of view, capturing many TSVs within one image. A limitation

remains the lower resolution compared to SEM, and the relatively long measurement time. For the limited resolution, there exist two main alternatives: X-ray imaging using synchrotron radiation and X-ray microscopy. The energetic X-rays at a synchrotron are focused using optical magnification, which currently allows one to get images with <30nm resolution. A major disadvantage

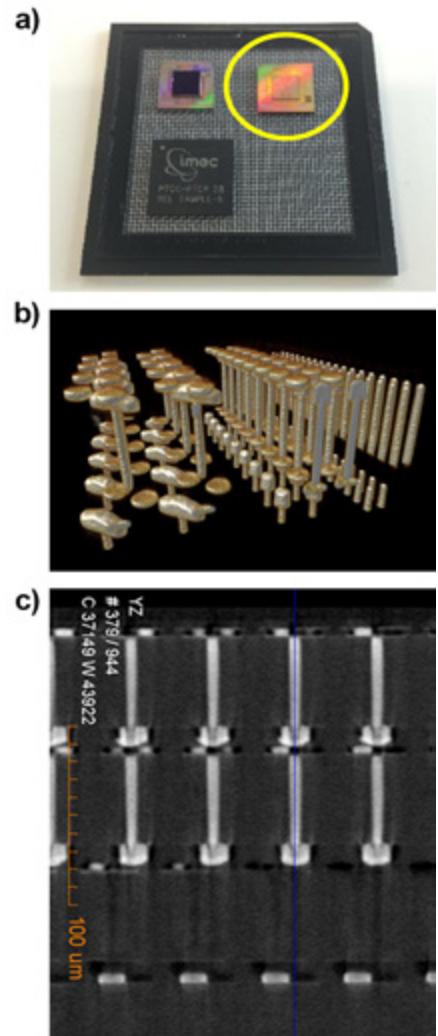


Figure 2: Nano X-ray microscopy images of a) a sample with stacked dies (yellow circle) showing very high detail results of TSVs, b) 3D image and c) a reconstructed 2D slice. Courtesy of Carl Zeiss X-ray Microscopy Inc.

is the requirement of a synchrotron source, making the technique less appropriate for failure analysis. A very interesting alternative is X-ray microscopy, which combines the best of both worlds: geometrical magnification and optical magnification in a lab system. Also in this system, the smaller the sample, the better the resolution. Very good results have been obtained on chip-sized and even 300mm wafer-sized samples [5]. **Figure 2** shows a high-resolution 3D image (0.3 μm /voxel) from a multilayer die-stack (sample encircled in yellow) obtained with such a system. For smaller samples, even 30nm resolution was demonstrated [6].

One concern remains the impact of X-rays on device performance. Dogan et al. [7], analyzed the impact of X-rays as a function of exposure time on the erase time of 150nm flash memory and 90nm and 45nm field-programmable gate arrays (FPGAs). The flash memories were clearly affected. They concluded that new technology devices seem to be less sensitive to the radiation but advised to test this premise for each new technology. X-ray tomography might be suitable for failure analysis, but one should remain cautious when using it to screen samples with active devices.

Scanning acoustic microscopy (SAM)

As in the case of conventional X-ray imaging, SAM is mostly used for package-level failure analysis. The principle is based on sending a sound pulse (MHz frequency range) from a transducer via an acoustic lens to the device and detecting the reflected waves from the different interfaces within the device. Water is used as a coupling medium to transmit the sound waves from the transducer into the sample. Because of the strong acoustic impedance mismatch between air and solid materials, SAM is extremely sensitive for the detection of voids and delaminations [1,2]. It is certainly of high interest for 3D FA to check the bonding interfaces for delamination. There is, however, one disadvantage: to obtain a larger penetration depth in a sample, such as a packaged 3D chip stack, one has to reduce the frequency that inevitably also reduces the spatial resolution of the measurement. The spatial resolution of conventional SAM systems that operate up to 300MHz is generally on the order of ~10 μm at best. Nevertheless, it has already been shown that 200MHz SAM images can provide indications of voids in TSVs that are smaller than 10 μm in size (**Figure 3**) [8].

A SAM operating at GHz frequencies has recently been developed (FhG IMWS and PVA TePla Analytical Systems) and promises

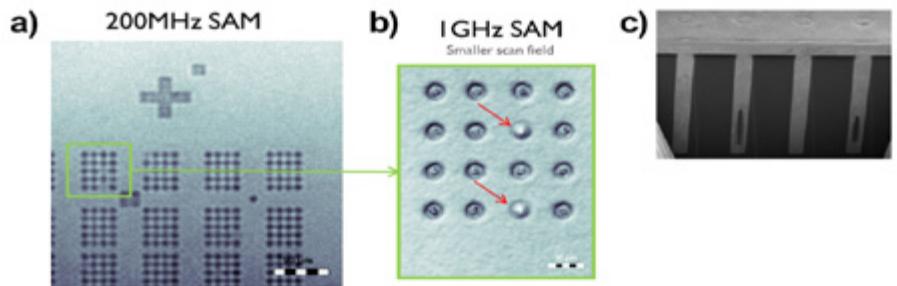


Figure 3: SAM images of 5x50mm TSVs: a) 200MHz SAM, b) GHzSAM, and c) FIB/SEM image confirming the presence of voids [10].

a resolution of 0.65 μm . This system uses an acoustic lens that is specifically designed to operate in the GHz frequency range and can focus sound waves to a micron-scale spot on the sample [9]. Because of the large aperture of the lens, not only longitudinal waves are transmitted into the sample, but also surface acoustic waves (Rayleigh) and shear waves. It was shown [2] that the Rayleigh waves, when reflecting from a vertical interface (e.g., TSV sidewall or crack) give raise to a fringe pattern that can provide useful information, not only on the presence of interfaces and cracks, but also on local stress. Because these high-frequency waves can only penetrate a few microns into the Si or Cu, GHz SAM is expected to be highly sensitive to sub-surface defects: for example voids near the top of the TSVs or delamination in the BEOL [10]. Research is ongoing at imec in collaboration with FhG CAM to address the exact depth and spatial resolution of such a system [10]. This system is very promising for via-last 3D technology, which is currently in development and uses chips thinned down to 15 μm and below.

An alternative method to investigate voids in TSVs is based on laser ultrasonics [11]. In this system, the TSVs are excited from the surface by a laser pulse and the back reflection of the laser-induced acoustic wave generated in the TSV is monitored with an optical interferometer. First tests have demonstrated that voids can be detected with this technique in TSVs.

Overall, acoustic methods allow the detection of voids, delaminations, and interface irregularities in samples, but have limitations either in resolution, or in penetration depth. Nevertheless, developments in this field are going fast and 3D-technology will remain to benefit from this for failure analysis purposes.

Magnetic field imaging

Magnetic field imaging systems measure the magnetic field associated with electrical current flow through conductors. As most

materials used in the microelectronics industry are transparent to magnetic fields, the technique lends itself to non-destructive sensing through stacked chips, metal layers and packaging materials, thereby perfectly addressing the failure analysis needs for 3D technology. There are three sensing options under investigation at this moment: magneto-optical, sensor based, and NV-diamond centers based sensing. In the first one, a magneto-optical (MO) sensor (a thin disk) is placed on the sample and is illuminated by polarized light from a scanning laser. For a current that flows underneath the sensor, the magnetic field in the sensor will induce a rotation in the polarization state of the reflected light. A limitation of this sensing option remains the limited sensitivity, as the distance to the current path should be smaller than 30 μm to detect a current of ~30mA. The resolution, as for all magnetic sensing, depends on the distance to the conductor [12].

The second option uses a superconducting quantum interference device (SQUID) or giant magnetoresistance (GMR) sensor on a scanning probe [13]. The SQUID typically has a larger sensitivity (~500nA) but requires a longer working distance that limits the spatial resolution to about 3 μm at best. A GMR sensor has a lower sensitivity (~10 μA) but a spatial resolution of ~250nm was demonstrated. The potential application of these sensor-based systems for failure analysis was clearly proven, showing that not only shorts in TSV daisy chains (**Figure 4a**) [14] but also opens (using an RF signal) can be detected [13]. It can even be applied to cross-sectioned samples (cross-sectioning stopped in Si before reaching the TSVs) to find the location of a leakage path between TSVs (**Figure 4b**).

The last option makes use of nitrogen-vacancy (NV) centers (point defects) in diamond [15]. These magnetic field sensors can have a higher sensitivity (photoluminescence) than the SQUID and they can provide information for both out-

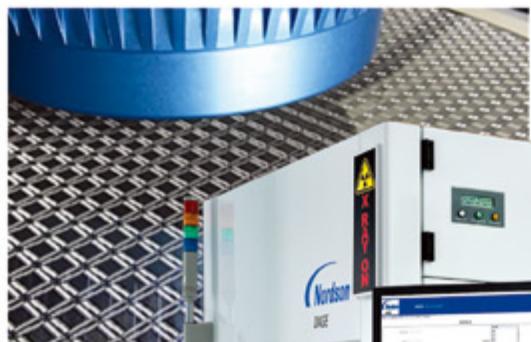
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and in-plane magnetic fields. This type of detector is currently not only of very high interest for FA of 3D systems, but also for other applications in nanotechnology.

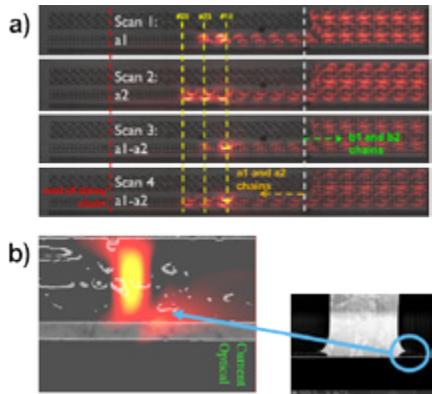


Figure 4: a) Current images from a 3-chip stack with $5 \times 50\mu\text{m}$ TSV interwoven daisy chains (a1 and a2) obtained from MFI in different connection schemes (scans) of the two chains. This allowed finding the TSV at the short location [14]. b) Current and optical overlay imaged obtained using MFI from a X-section, indicating a leak path at the bottom of a TSV. c) The failure at the notched bottom of the TSV is confirmed with SEM. Courtesy Neocera.

Electro-optical and thermal-based FA systems

Time domain reflectometry (TDR) is a well-known technique for failure detection—for example, printed circuit boards (PCBs). A low amplitude electrical pulse (to 25GHz) is generated into a conductive circuit and the reflected signal is measured as a function of time. Defects such as shorts, opens or cracks will cause a change in amplitude and phase of the reflected signal compared to a non-failed sample. However, the resolution of conventional TDR is insufficient for applications within 3D-stacked chips. A better resolution can be obtained with electro-optical THz-pulsed reflectivity (EOTPR) where the ultra-high frequency signals are generated optically. This technique also requires a functional reference sample, but alternatively a combination with modeling can also allow pinpointing the defect. Fault detection in a 3D-stack to within $20\mu\text{m}$ was demonstrated using this combination [16].

Two very similar EO-based FA-techniques are light- (LIVA) and thermally- (TIVA) induced voltage alteration [1]. In these techniques, a constant current is applied to the device and the voltage is monitored while scanning a laser beam across the region of interest. The light- or heat-induced resistance changes are measured. These techniques

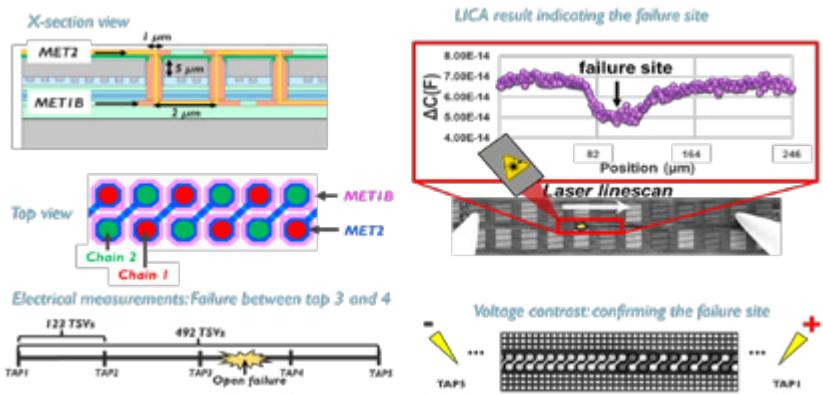


Figure 5: Application of LICA to find an open on a wafer-to-wafer stack with interwoven daisy chains of $1 \times 5\mu\text{m}$ TSVs, $2\mu\text{m}$ pitch (via last) and confirmation of the site using Voltage Contrast in the SEM [16].

mainly find applications in 2D FA. Imec recently [17] introduced another method for failure isolation in 3D TSV structures whereby the effect of the light on the TSV capacitance is measured. This light-induced capacitance alteration (LICA) technique can localize interconnection failures in TSV structures by using a scanning laser beam to selectively probe the interconnect capacitance of TSVs. A photo-induced change in TSV capacitance can only be detected electrically if the interconnect link containing the illuminated TSV is not interrupted (Figure 5). A requirement of such optical-based laser probing techniques is that the region of interest in the device should be accessible by a laser.

A 3D FA technique that offers a solution to the challenges discussed is lock-in thermography (LIT), developed by Altmann et al. [18]. It relies on the detection of thermal waves [18]. In this technique, the defect is stimulated electrically by a periodically pulsed (typically between 1 and 2kHz) supply voltage, and the position (X-Y localization) and phase (Z-localization) of the thermal response is detected by an infrared (IR) camera. This technique has been adopted by the industry as a tool for localization of resistive opens and electrical shorts in packaged 2D devices. Its application to 3D failure analysis was demonstrated, for example in [2,3,18]. Imec is currently exploring the application of other thermal methods for 3D FA.

Summary

The emergence of 3D-technology has increased the urge for the development of failure analysis techniques that allow the precise localization of a failure in stacked ICs and in new interconnect components such as TSVs and micro-bumps. Traditional FA techniques, such as X-ray imaging and scanning acoustic microscopy, have seen

very promising developments with regard to spatial resolution. Also, TDR has evolved into the more sensitive EOTPR. Existing laser simulation techniques have also triggered the invention of a new technique that can be applied to detect failures in TSV-chains: light-induced capacitance alteration (LICA). Lock-in thermography (LIT) found its applications not only for packaged chips, but also for FA of 3D stacked chips.

The positive evolution summarized above is largely a result of close collaboration between research institutes and the metrology industry, aiming to enable failure analysis of future technologies. Certainly, ongoing research on failure analysis methodology and techniques is required to keep pace with microelectronics technology development.

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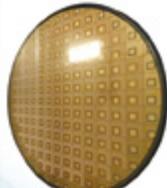
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Development of a FOWLP platform for high-performance and RF SiP applications

By Gaurav Sharma, Adam Beece [[GLOBALFOUNDRIES U.S. Inc.](#)]; Gao Shan [[GLOBALFOUNDRIES Singapore Pte Ltd.](#)]; Marcel Wieland [[GLOBALFOUNDRIES Germany](#)]

Advanced packaging is increasingly becoming an important enabler for next-generation IC product applications. Advanced packages provide unique value proposition combinations for different product segments. For example, in premium smartphones, small footprint area, low height and high application processor/memory bandwidth, all based on user acceptable battery life, are mandatory product requirements. Likewise, to meet the demanding performance specifications for networking, CPU and GPU consumer applications, advanced packaging solutions are needed that can enable leading silicon node die-partitioning ability and Tb/sec memory bandwidth. On the other hand, for the RF application space, the key differentiating product features are high-frequency RF performance and matching, passives integration, and power efficient designs. Furthermore, for 5G/mm wave RF applications, the package layout and design are much more sensitive than at lower frequencies. Minor changes in layout or parasitics can impact performance severely. Shorter wavelengths also necessitate the chip and the antenna be in close proximity and ideally designed as a “pair.” RF transitions from chip to antenna also need to be designed very carefully.

A fan-out wafer-level packaging (FOWLP) platform has the following advantages that make it a suitable advanced packaging technology for all of the above applications:

1. No packaging substrate or reduced substrate layer count enables smaller foot print area and profile thickness.
2. Wafer fab-like fabrication processes ensure increased I/O density, reduced interconnect length and parasitics, and excellent 2D and 3D interconnect process and quality control.
3. A low-loss mold compound-based packaging platform leads to good RF performance and close matching circuitry over a large frequency range.

Fan-out technology approaches

Over the last few years, fan-out packaging has emerged as a powerful WLP platform that can satisfy the myriad needs listed above. As depicted in [Figure 1](#), there are different fan-out packaging schemes that have been developed and exist in the industry today [1-4]. Traditional wafer-level fan-out (WLFO) is a die first and die face down process that has been in volume production for RF, Wi-Fi, PMIC, analog and low-end baseband types of applications [1]. Traditional WLFO, however, faces some inherent process and bill of material challenges that limit the technology from finding adoption in high-performance applications such as high-end baseband, networking processors, data center, etc. [3, 5].

Recently, a die-up fan-out process has been adopted for application processor and memory integration applications for smartphones. The die-first and die face-up approach utilizes a copper pillar for die interconnection to the fan-out redistribution layers (RDL) [4]. A wafer grinding process is employed on the molded wafer before the fan-out RDL fabrication process, which takes care of some of the inherent mold compound

topography issues associated with the traditional WLFO process, thereby ensuring a comparatively better control of the fan-out interconnect width/space/thickness. This approach, however, also has limitations of die yield loss because the known-good dies (KGD) are committed at the beginning of the fan-out assembly process. These die yield loss issues become economically

penalizing for expensive high-end product applications. Both traditional WLFO and die-up fan-out interconnects are based on metals and dielectrics schemes that are used in backend manufacturing. This limits the minimum achievable RDL linewidth and space to greater than $2\mu\text{m}/2\mu\text{m}$ [2]. Any further reduction in linewidth/space would necessitate fundamental material changes and switch to fab process-based interconnects.

The high-density fan-out (HD-FO) processes being developed in this work and elsewhere address the aforementioned weaknesses. As shown in the process flow in [Figure 1](#), the HD-FO RDLs are pre-fabricated on a silicon wafer in a process similar to silicon interposer. KGDs are then placed on silicon wafers with known-good and tested RDLs. Die placement is followed by wafer molding and bulk silicon removal, leaving only the original

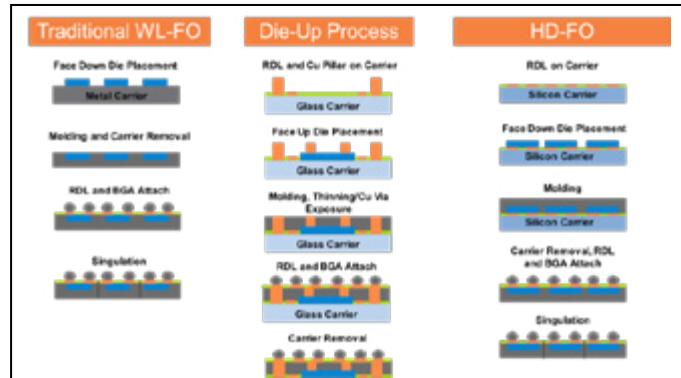


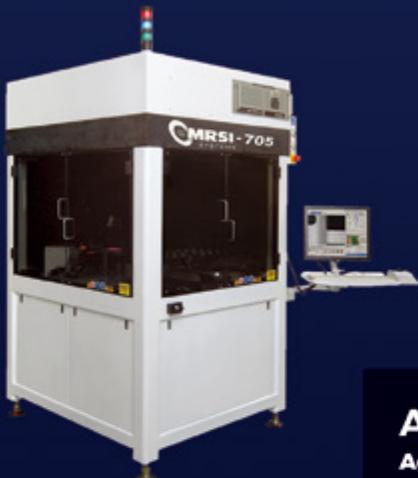
Figure 1: Overview of the different industry fan-out wafer-level packaging schemes and process flows.

die and RDL. Finally, fan-out RDL fabrication for substrate- and/or board-level interconnection are processed. This fan-out process flow ensures minimum KGD yield loss. Depending on the product application and associated package routing requirements, the RDL on the silicon wafer can be fabricated by either using a backend manufacturing process based on

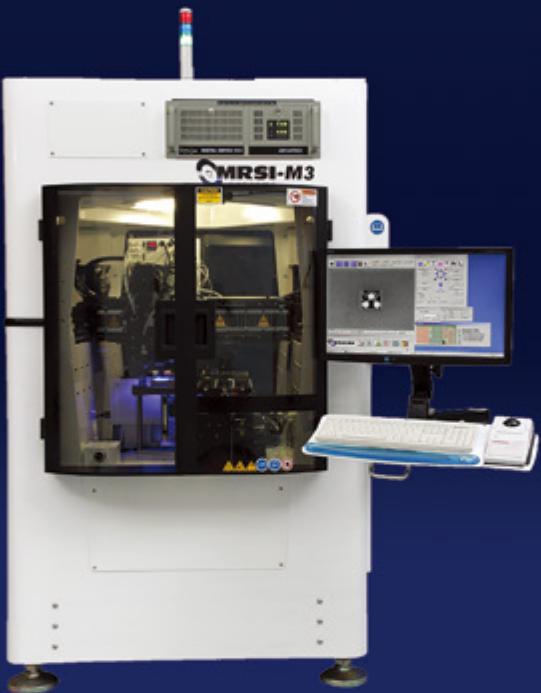
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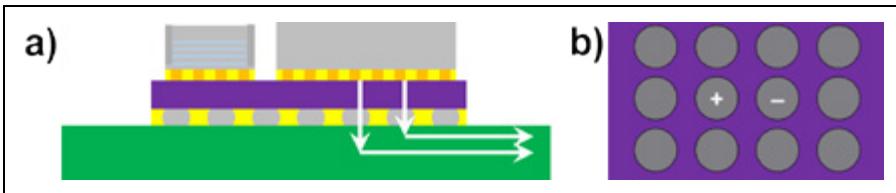


Figure 2: Schematic showing the vertical interconnect used for insertion loss simulation in a) cross section (left), and b) top down (right).

a complete organic interconnect, or a fab back-end-of-line- (BEOL) based inorganic interconnect scheme. Using the fab BEOL process enables RDL interconnect linewidth scalability down to $0.5\mu\text{m}/0.5\mu\text{m}$. Such sub-micron routing density will be needed for advanced high-performance applications like networking, CPU, and GPU that require die-to-die interconnection arising from either die partitioning or heterogeneous multi-chip integration on a fan-out platform.

Insertion loss comparison for 2.5D and HD-FO packages

To address the ever growing need of high-speed communication applications in wired, wireless infrastructure, data center high-speed interface IP such as SERDES, have to satisfy speed requirements of 28Gbps and beyond [6]. Quite significant work has already been done in this area using a 2.5D silicon interposer fabricated using a BEOL process [7-8]. However, the TSV faces performance limitations due to losses associated with silicon, longer interconnect path and the thin metallization dictated by the BEOL processes. There are a few studies published in literature that highlight electrical performance benefits of non-TSV packaging solutions like glass interposers [9], silicon-less interconnect technology, and non-TSV interposer (NTI) FOWLP over 2.5D silicon interposers [10].

One of the key high-performance product requirements is high-speed communication between the die and the package environment [6]. To simulate this product application scenario, vertical interconnect insertion loss modeling was carried out on the different package platforms: silicon interposer with either one or two TSVs per microbump and HD-FO with organic and inorganic interconnect layers.

Figure 2 shows the associated interconnect path and package

schematic. To isolate the inherent vertical interconnect insertion loss, no routing is assumed to be done on the package—BEOL is only used to connect the top die to the backside connection, and frontside microbump and backside controlled-collapse chip connection (C4) are not modeled. Only RDL, TSV (if required) and the backside pad are included in the interconnect path. A single differential pair is modeled, surrounded by eight ground structures.

As can be seen in **Figure 3**, HD-FO shows insertion loss that is an order of magnitude smaller than the TSV. Even up to frequencies as high as 60GHz, no significant insertion loss increase is visible for the HD-FO package interconnect. This is primarily due to no silicon losses that are associated with the interposer, a vastly shorter path without the TSV, no aluminum interconnect layer, and smaller pads. Earlier similar work on an electrical comparison between 2.5D interposer and NTI has shown that NTI also shows lower resistance than 2.5D [10]. Lower insertion and resistive losses will enable more power efficient and high-performance HD-FO package product designs. **Figure 4** shows comparisons of vertical interconnect insertion loss between HD-FO with two metal inorganic and organic interconnect layers. The inorganic interconnects perform slightly better on account of the reduced vertical interconnect length.

An emerging area for

advanced fan-out applications is multi-die packages with extremely high routing density requirements for advanced node die partitioning and heterogeneous die integration [6,11]. For such product applications that require high-speed die-to-die communication, lateral (die-to-die) insertion loss within the RDL is also extremely important. **Figure 5** shows the lateral interconnect insertion loss comparison between interposer and HD-FO with organic and inorganic interconnect layers. As expected, the

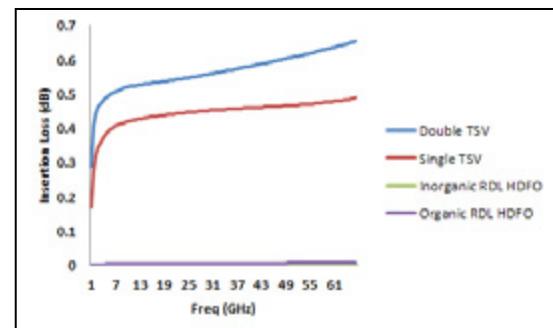


Figure 3: Vertical interconnect insertion loss comparison between TSV interposer and HD-FO. HD-FO shows orders of magnitude lower insertion loss for frequencies up to 60GHz.

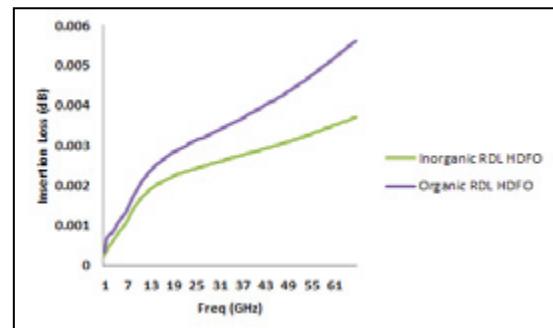


Figure 4: Vertical insertion loss comparison between inorganic and organic RDL HD-FO.

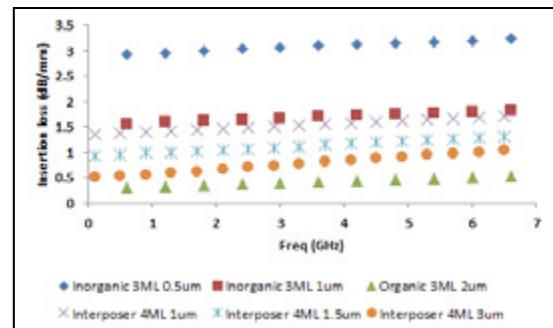


Figure 5: Lateral interconnect insertion loss comparison between single TSV interposer and organic, inorganic HD-FO. Different metal interconnect widths were evaluated for the same package type.

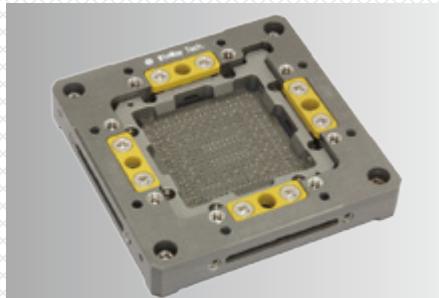
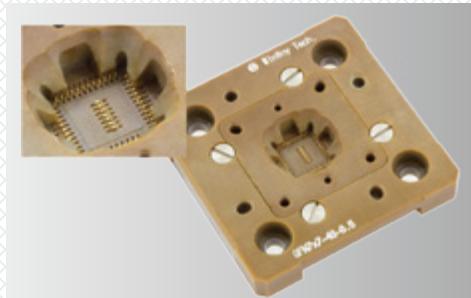
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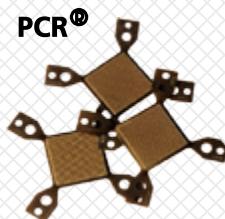
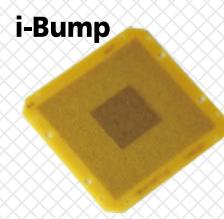
Plunger

Thermal Head

Manual Lid



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insertion loss decreases with increasing interconnect width for both inorganic interconnect HD-FO and interposer packages. For the same interconnect width of $1\text{ }\mu\text{m}$, the inorganic interconnect HD-FO and interposer show similar interconnect loss. This is expected because both the package interconnect schemes are based on the fab BEOL process.

Organic interconnect HD-FO with an interconnect linewidth of $2\text{ }\mu\text{m}$ outperforms interposer with a slightly higher linewidth of $3\text{ }\mu\text{m}$, partially due to thicker wire (lower resistance). An organic interconnect HD-FO loss of $<0.5\text{dB/mm}$ is acceptable for wide-bus communication, and is able to meet high-speed communication product requirements of maximum bandwidth density (Gbps/mm chip edge) [6]. It is also clear that a $0.5\text{ }\mu\text{m}$ width RDL needs to have low speeds and requires strong drivers. An increase in interconnect width and thickness will lead to a slightly coarse line/width space offering with the HD-FO schemes, yet in comparison to competing laminate-based packages, HD-FO will still provide more aggressive rules for advanced package designs [3]. It is clearly evident from the insertion loss studies that competing design requirements exist for optimizing the product's package routing and vertical and lateral interconnect insertion losses requirements. A comprehensive system-level analysis is required to further characterize and optimize package performance requirements for specific product applications [6].

Development of the fan-out package menu

As part of this work, an extensive fan-out package platform is being developed that spans multiple silicon process nodes: 180nm, 22FDX™, 14nm, and 7nm. Selection of appropriate fan-out technology, die/package size, with/without substrate combinations is being decided by package application requirements and product cost considerations. Following are the line/width and routing density capabilities for the different fan-out schemes being evaluated in this study: HD-FO (inorganic RDL) > HD-FO (organic RDL) > traditional WLFO.

Traditional WLFO is being developed for RF, Wi-Fi, PMIC, and analog IC types of applications that generally do not require high routing densities. The relatively small fan-out package sizes of less than $10\text{x}10\text{mm}$ can also be directly mounted on printed circuit boards and are still able to meet the product reliability requirements. No substrate requirement, as well as existing industry manufacturing capability, ensure cost-competitive packaging solutions for products that are primarily used in smartphones and hand-held electronics. HD-FO with organic and inorganic RDL and no substrate are being developed for smartphone application processor and baseband applications. Suitable package sizes of less than $\sim 15\text{mm} \times 15\text{mm}$ with minimum linewidth/space capability greater than $5\text{ }\mu\text{m}/5\text{ }\mu\text{m}$ are being developed. **Figure 6** shows the two such package configurations, a) side-by-side, b) side-by-side + package-on-package. Following are the specific package details: Tech node – 14nm, (a) Package size – $15\text{x}15\text{mm}$, Die size – $6\text{x}10\text{mm}$ (2 dies, side-

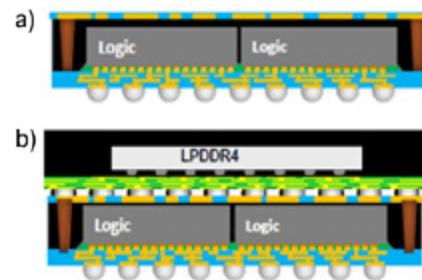


Figure 6: Fan-out packages under development
a) Side-by-side (SS); and b) Side-by-side and PoP (SS + PoP).

by-side), BGA pitch – 0.35mm (b) Bottom package is same as (a), top package has a die size of $10\text{x}10\text{mm}$ and a package size of $14\text{x}14\text{mm}$, with a BGA pitch of 0.35mm . Both package types have passed the package-level reliability tests shown in **Table 1** and are currently undergoing board-level reliability testing.

Successful chip package integration (CPI) is being ensured by incorporating different CPI macros and structures such as perimeter line, delamination sensor, under bump crack sensor, C4 corner/stitch, temperature humidity bias (THB) sensor, via serpentine/comb. These macros can detect and assess mechanical integrity for die seal (resistance/leakage), BEOL stack integrity under bump in corners, single/interconnect chain-based bump integrity, moisture penetration at die edges, damage in typical BEOL structures especially under die bond/bump pads (resistance, leakage).

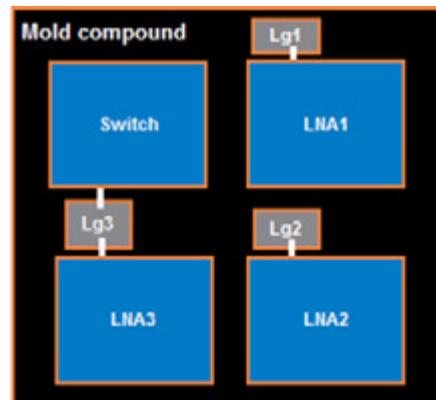


Figure 7: Fan-out modules with integrated switch/LNA/inductors for cellular phone FEM.

Package Level Test

| Environmental Stress | Conditions | Qualification Criteria | SS | SS + PoP |
|---|--|------------------------|------|----------|
| High Temperature Storage (HTS) | Unbiased, 150°C | No fail, 1000 hours | Pass | Pass |
| Pre-Conditioning (MSL3) | 125°C bake for 24hrs, MSL 1: $85^\circ\text{C}/85\%\text{RH}/168\text{hrs}$ 3x reflow 260°C | No fail | Pass | Pass |
| Temperature Cycling With Pre-conditioning | B-condition: -55°C to 125°C $D_t = 15\text{ min}, T_{t<1\text{ min}}$ | No fail 500x | Pass | Pass |
| Unbiased HAST With Pre-conditioning | $130^\circ\text{C}, 33.3\text{ psia}, 85\%\text{ RH}$ | No fail, 96 hours | Pass | Pass |

Board Level Test

| Environmental Stress | Conditions | Qualification Criteria | SS | SS + PoP |
|----------------------|--|------------------------|---------|----------|
| Drop Test (30x) | JESD22-B110/JESD22-B111 Condition B: 0.5 ms half-sine with peak acceleration of 1500 G | No fail, 30x | Ongoing | Ongoing |
| TCOB (1000x) | -40°C to 125°C Ramp = 15 min, Dwell = 15 min | No fail, 500x | Ongoing | Ongoing |

Table 1: Package-level and board-level reliability tests for fan-out packages. Both SS and SS + PoP package configurations have passed package-level reliability tests and are undergoing board-level reliability tests.

Fan-out based SiP for RF applications

Different fan-out package types are also being developed as system-in-package (SiP) platforms for sub-6GHz and mm-wave RF applications. **Figure 7** shows a proof-of-concept test vehicle that is under development for a LNA/switch/inductor module for 3G/4G RF front-end module applications for smartphones. For the LNA/switch fan-out module, the input inductors for the three LNAs are designed in the fan-out distribution layers. The specifications of inductance and Q_{peak} @ application frequency — depend on the cellular frequency band that the LNA are targeted to support.

Table 2 shows measured HD-FO inductor performance for different inductors. Inductor design parameters such as the number of turns, metal line, space, and thickness are varied to investigate their effect on inductance and Q factor. This is a ~3-4X improvement in measured Q factor for similar inductors designs on fan-out versus on CMOS [12-13]. The fabricated inductor designs use copper interconnect

| # of turns | L (nH)@6 GHz | Cu width/space/thickness (um) | Qmax |
|------------|--------------|-------------------------------|------|
| 4 | 3.7 | 15/15/15 | 52 |
| 3 | 1.3 | 15/15/15 | 44 |
| 2 | 0.8 | 15/15/15 | 44 |
| 3 | 1.6 | 15/15/5 | 38 |
| 3 | 1.6 | 15/10/15 | 52 |

Table 2: Measured HD-FO inductor performance.

width/space/thickness parameters that can be readily applied to high-volume backend manufacturing. The significant improvement in Q is a result of underlying mold compound material, which is a much less lossy substrate in comparison to a CMOS silicon substrate. For inductors fabricated on thick copper layers, a lower parasitic resistance also helps in improving the Q factor [14]. High-Q inductors can significantly improve the low-noise amplifier (LNA) and power amplifier (PA) designs by enabling better noise figures and power efficiencies. LNA is a crucial component of the front-end of the radio receiver circuit and the PA is an integral part of wireless communication circuitry [12,13].

Figure 8 shows a fan-out module with a co-packaged digital and RF chip with



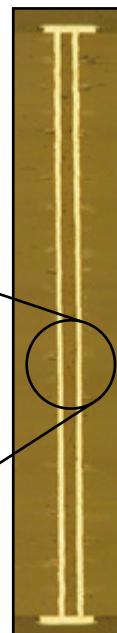
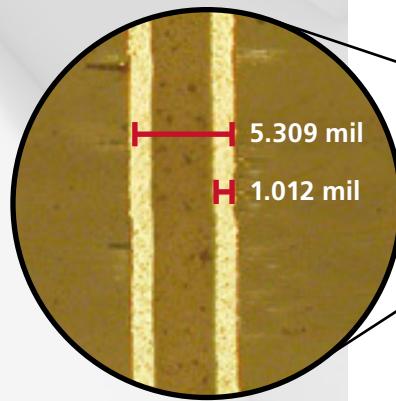
Figure 8: Fan-out module with digital chip/RF chip/antenna array integration for mm-wave applications.

integrated inductors, capacitors and an antenna for 60GHz Wigig system-on-chip (SoC) mm-wave applications. The target product applications at 60GHz are in-home wireless connections for HD virtual reality, local hot spots within 5G transport, and mobility applications such as car-to-car communication, driver assistance, in-car ultra-HD entertainment, and in-car infotainment. For mm-wave applications,

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one of the most important RF performance criteria is RF chip/antenna array integration and beam formation. **Figure 9** shows beam forming simulation results from a 4x4 patch antenna array with regular and depopulated configurations. The regular array shows a desired beam forming pattern. Following are the antenna array details:

- Rectangular patch antenna, application frequency = 60GHz, bandwidth = 9GHz, individual antenna gain = 6.3dBi, individual antenna radiation efficiency = 97%, substrate thickness = 500 μ m

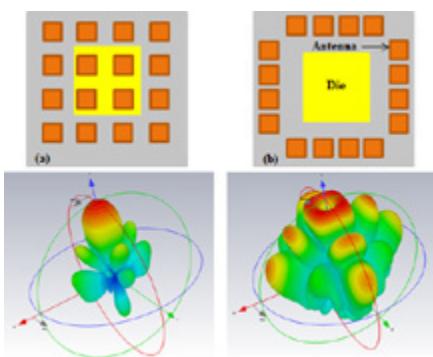


Figure 9: Beam forming simulation from antenna arrays a) regular 4x4, and b) depopulated 4x4.

Summary

HD-FO packages with inorganic and organic interconnects demonstrate vertical interconnect insertion loss that is an order of magnitude lower than for a TSV interposer. HD-FO with organic interconnect shows the least lateral interconnect loss in comparison to inorganic interconnect HD-FO and to a TSV interposer. However, it is evident that a complete silicon/package design optimization is needed to meet the competing package routing and vertical and lateral interconnect insertion loss requirements. Inductors on the HD-FO platform demonstrate a measured ~3X improvement in Q_{max} over similar CMOS-based inductors, which highlight the potential of HD-FO usage as a high-performance RF SiP platform. The copper interconnect parameters used in the HD-FO inductor design are also readily amenable for use in high-volume backend manufacturing. Early promising results on RF chip/antenna array beam forming architecture highlight the potential of fan-out modules for mm-wave applications.

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X2FBGA: a new wire bond CABGA package

By Yeonho Choi, Burt Barber *[Amkor Technology, Inc.]*

The wire bond ChipArray® ball grid array or CABGA package provides versatile solutions for a broad array of semiconductor products used in a variety of automotive, industrial, computing, networking, consumer and mobile applications. In addition to offering high performance and flexible signal routing capability for high I/O count devices, the CABGA family of small footprints and thin form factors make it a member of the so-called near-die size packaging category for single-die products in the semiconductor industry. Ever-expanding capabilities in mobile handsets have always required a continuous reduction in the form factors for all semiconductor components: both footprint and height.

The most recent CABGA achievement is the development of a maximum 0.4mm height fine-pitch ball grid array (FBGA), called X2FBGA (**Table 1**) to denote a double extremely thin FBGA form factor. X2FBGA's advantages offer it a potential position among the various near-die size packaging options available in the market, such as the quad flat no-leads (QFN) package, routable QFN package, flip-chip chip-scale packaging (fcCSP) and wafer-level packages. However, to overcome key challenges, specific actions had to be taken to make the assembly process feasible and bring solutions to market.

Identifying the challenges

Today, many packages can achieve a total seat profile less than 0.4mm including QFN, wafer-level packaging (WLP) side, fan-in WLP (also known as die size BGA or DSBGA) and fcCSP. The fan-in WLP height is determined by the wafer backgrind thickness during the backend process, so it is relatively easy to achieve. For QFN packages, mold cap tooling determines the body profile. With 0.25mm mold cap tooling, which has

been commonly used for several years, only the lead frame thickness needs to be included. The fcCSP uses exactly the same package outline platform as the wire bond CABGA and it enables more complicated interconnecting options and higher I/O count with high efficiency and superior electrical performance. The fcCSP has the option to expose the die backside on top of the package, so its thinness control is a relatively easy way to offer a maximum 0.4mm profile.

Compared to other packages, wire-bond CABGA has more challenges to

achieve a thin package profile. The added height of the CABGA solder ball bumps requires thinner die and ultra-low wire looping controls to fit all z-dimension stack-up elements within the thin mold cap space. The extremely-thin fine-pitched BGA (XFBGA) provides a maximum 0.47mm (or 0.50mm) height physical profile dimension, and, until recently, it has been the thinnest wire bond BGA achievable using traditional face-up die bond, wire connect and molding process technology combined with a commonly available thin 2-layer

| | LFBGA > 1.2 mm | TFBGA ≤ 1.2 mm | VFBGA ≤ 1.0 mm | WFBGA ≤ 0.80 mm | UFBGA ≤ 0.60/0.65 mm | XFBGA ≤ 0.47/0.50 mm | X2FBGA ≤ 0.40 mm |
|-----------------|--------------------|--------------------|--------------------|--------------------|-------------------------|-------------------------|-----------------------|
| | CA-HBGA | CA-HBGA CTBGA | CA-vFBGA CVBGA | CA-wLGA CA-wBGA | CA-uLGA CA-uBGA | CA-xFBGA CA-xLGA | CA-x2FBGA CA-x2LGA |
| Mold Cap | 0.70 mm 0.95 mm | 0.60 mm 0.53 mm | 0.45 mm 0.53 mm | 0.45 mm 0.35 mm | 0.35 mm 0.25 mm | 0.25 mm 0.20 mm | 0.1x mm |
| Substrate Layer | 2, 4 or 6 Layer | 2 or 4 Layer | 2 or 4 Layer | 2 or 4 Layer | 2 or 4 Layer | 2 Layer | 2 Layer |

Table 1: Amkor's ChipArray® BGA offerings: low-profile fine-pitch BGA (LFBGA), thin-profile fine-pitch BGA (TFBGA), very fine-pitch BGA (VFBGA), very very thin-profile fine-pitch BGA (WFBGA), ultra-fine BGA (UFBGA), extremely-thin fine-pitch BGA (XFBGA), and the newest X2FBGA.

| Wafer Level Package (Fan-in & Fan-out) | | | | | | | | | | | |
|--|-------------|-------------|--------------|-------------|-------------|-------------|-------------|-------------|--------------|-------------|------|
| Laminate TFBGA | | | | | | | | | | | |
| 1 Layer routable CSP, Additive | | | | | | | | | | | |
| 1 layer rt MILF (2 row IO + P*, 3rd exp pw bar*) Subtractive | | | | | | | | | | | |
| Max 4 row IO depth Assumed | | | | | | | | | | | |
| HVM max (& theoretical full array) | | | | | | | | | | | |
| Full array Bump Assumed | | | | | | | | | | | |
| Thickness per DPS Backgrind, 0.15° 0.4mm wafer + bump | | | | | | | | | | | |
| 2L Wire bond FBGA thickness in production | | | | | | | | | | | |
| 1L rt CSP rt MILF | | | | | | | | | | | |
| MLF/LGA | | | | | | | | | | | |
| Foot print | 0.5mm Pitch | 0.4mm Pitch | 0.35mm Pitch | 0.5mm Pitch | 0.5mm Pitch | 0.4mm Pitch | 0.5mm Pitch | 0.4mm Pitch | 0.35mm Pitch | 0.3mm Pitch | |
| 2x2 | 8 | 12 | 16 | NA | 14 | 16 | 15 | 16 | 14 | 16 | 25 |
| 3x3 | 16 | 20 | 24 | NA | 28 | 36 | 35 | 49 | 36 | 49 | 54 |
| 4x4 | 24 | 28 | 32 | NA | 44 | 52 | 64 | 80 | 64 | 81 | 121 |
| 5x5 | 32 | 40 | 44 | 44/52 | 60 | 72 | 81 | 112 | 81/112 | 148/144 | 192 |
| 6x6 | 40 | 48 | 56 | 56/58 | 76 | 88 | 112 | 140 | 121/121 | 155/156 | 264 |
| 7x7 | 48 | 60 | 58 | 76/84 | 88 + P | 112 + P | 144 | 192 | 169/169 | 211/209 | 400 |
| 8x8 | 56 | 68 | 80 | 84/100 | 104 + P | 128 + P | 176 | 240 | 225/225 | 308/301 | 484 |
| 9x9 | 64 | 76 | 92 | 110/116 | 120 + P | 152 + P | 268 | 272 | 265/280 | 383/404 | 625 |
| 10x10 | 72 | 88 | 104 | 114/112 | 134 + P | 168 + P | 240 | 320 | 346/361 | 454/576 | 784 |
| 11x11 | 80 | 100 | 112 | 112/114 | 152 + P | 152 + P | 272 | 352 | 416/441 | 485/529 | 1089 |
| 12x12 | 88 | 108 | 124 | 118/164 | 168 + P | 208 + P | 304 | 400 | 424/520 | 445/641 | |

Table 2: Near-die size packaging I/O density options and sweet spot analysis.

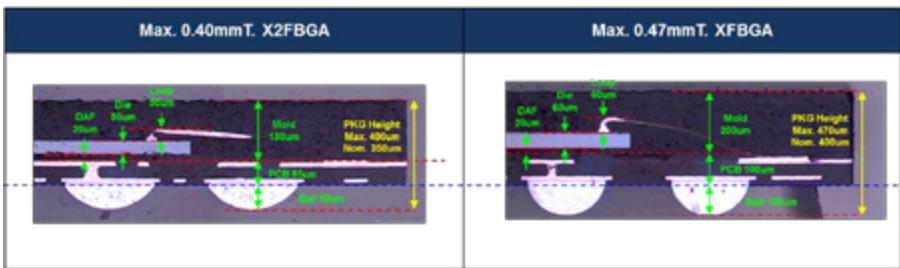


Figure 1: Cross-sectional comparison of the XFBGA and X2FBGA packages' construction.

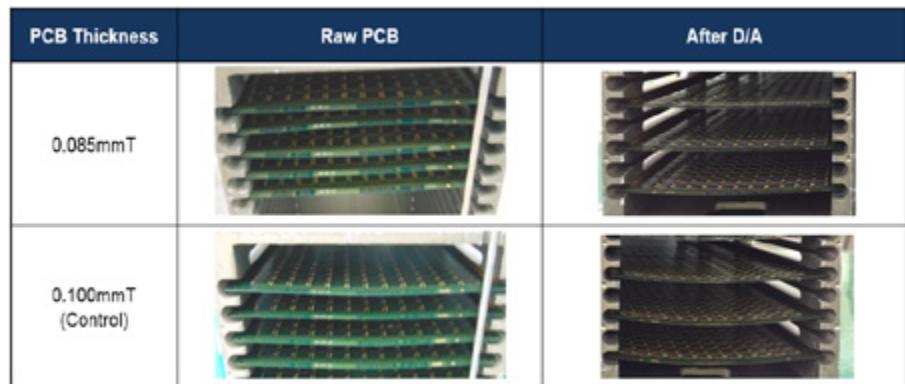


Figure 2: Substrate in the front-end-of-line (FEOL) process magazine, showing deflections and warpage management.



Figure 3: XFBGA picture after finishing the assembly.

laminate substrate. Based on XFBGA thickness reduction, CABGA's miniaturization capability, approaching the IC die size, has been improved by tighter control of the die edge to the bond ring and the tighter clearance control of the die-to-package body edge. This extended miniaturization capability is essential for the wire bond CABGA package to expand its applications in various market sectors, especially in mobile devices.

Table 2 shows packaging options with maximum I/O and maximum profile thickness capabilities. The 2~7mm body size range could be the sweet spot of the market opportunity that wire bond CABGA packages can contribute considering today's die size and I/O number trend. Taking these factors into account, wire bond CABGA packaging is expected to have significant acceptance and contribute

to further growth in this market with continued miniaturization in the near-die size packaging field. To achieve a near-term product, the maximum 0.40mm profile wire bond CABGA process capability was targeted. The main technical challenges in this development occur in four key areas: design, material, process and method.

Addressing the challenges

Designing the cross-sectional structure and its geometrical details, as well as setting control limits during substrate manufacturing and IC assembly processes, are the foundations for successfully building the X2FBGA. These areas establish the goals of each process and provide the targets to reach. To achieve the final maximum 0.40mm BGA height including tolerance limit, the nominal z-height dimension must be reduced; 0.35mm was set as a final

nominal dimension target to allow a +0.05mm tolerance specification limit. Compared to the existing XFBGA (see **Figure 1**), this required a 28% tightening of overall tolerance in addition to a 12.5% reduction of actual packaging material thickness. Mold tool design, substrate tolerance, and the associated design features to control bump ball height are all required to adjust, tighten and meet the target thickness reduction.

Material selection for mechanical property management is another challenge. The substrate core and solder mask material selection must be stiff enough to withstand and maintain the flatness of the substrate throughout the assembly process. Lower coefficient of thermal expansion (CTE) and ultra-thin (40µm) core material combined with a low-CTE solder mask is required to control the deflection and deformation of the raw PCB substrate and after-bake die attach (D/A) (see **Figure 2**).

The mold compound's physical properties were studied and chosen to prevent the molded strip warpage and maintain high quality and productivity during the backend of the assembly process. Wafer thinning and strength management, including sawing methods, are also important. The 50µm wafer thickness and die handling are performed to prepare for subsequent assembly processes. With this construction, the die top to mold cap leaves a z-space of only about 110µm. In addition to the ultra-low wire looping control during the wire bond process, the review and control procedure of the markable area on the body top surface must be considered during production planning to prevent potential interaction of the laser mark engraving depth with wires. **Figure 3** shows the end results.

A micro solder ball formation process with 80µm or less bump height has been in high-volume manufacturing for many years. Its production capabilities and market acceptance are well established for WFBGA and UFBGA packages. However, in some applications, customers specify a nominal 100µm bump height as the de facto application requirement. To prepare for and address such an application requirement, an additional 10-20µm of tooling reduction and

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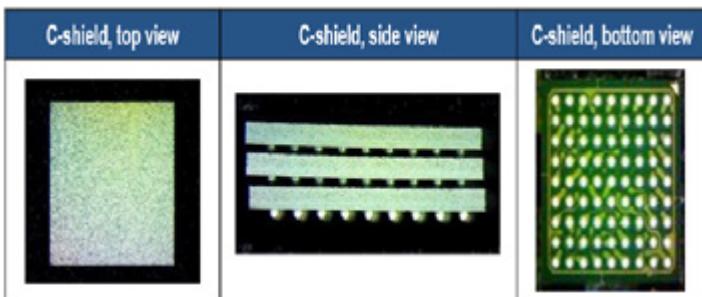


Figure 4: X2FBGA after conformal shielding.

adjustment in mold tool and die thickness have also been provided to allow additional bump space in the final package.

To certify its volume production readiness level, the X2FBGA package has been subjected to an internal qualification procedure and reliability tests. With all testing completed, the X2FBGA package passed all qualification requirements. Because this package targets mobile device applications, a conformal electromagnetic interference (EMI) shielding process is offered as an

option. The BGA form adds challenges in shield coating because the ball bumps require masking to prevent coating material contamination on the bottom side. As a result of targeted efforts in process development for a micro bump BGA conformal shield, we now offer a shield process up to a 100 μm bump height BGA (see **Figure 4**).

A new design option

By studying where and how the wire bond CABGA can provide advanced miniaturized packaging solutions, design, process, bill of material (BOM) and method advancements have been developed and implemented into Amkor's manufacturing processes to offer the X2FBGA package's capabilities. Ultra-

thin substrate design, sourcing, the right assembly material selection, tooling and process combinations are all available to support a variety of needs. We encourage users to consider the X2FBGA (with other advanced packaging options based on pros and cons) for their IC packaging needs and take advantage of its capabilities to satisfy existing and emerging design requirements.

Acknowledgement

ChipArray® is a registered trademark of Amkor Technology, Inc.

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Glass: a universal material class for semiconductor packaging and further integration

By Martin Letz, Matthias Jotz, Ruediger Sprengard [SCHOTT AG]

Glasses are a material class well-suited for semiconductor packaging and integration, as well as for operation at high frequencies and ultra-high data rates. Among several advantages, the high stiffness and heat resistance of glasses are beneficial. They can be produced with excellent homogeneity and good dielectric properties. Additionally, cost-efficient drilling processes are available, which are capable of serving as a basis for via metallization. The pristine surface of technical glass allows metallization of redistribution layers (RDLs) with line space well below 10 μm . The industrial supply chain, including handling support for structured and metallized glass sheets or wafers ready to be directly incorporated into semiconductor processes, is currently being built up.

Introduction

Silicon used in the electronics industry is a crystalline solid that is grown as large single crystals that show a periodic structure on an atomic length scale. In contrast, glasses are amorphous solids, which lack any crystalline order on the atomic scale. As true solid materials, especially oxide glasses, they combine stiffness, dimensional stability with low temperature coefficients, and high hydrolytic resistance. Oxide glasses can be produced with extremely high homogeneity. The widespread use of glasses in the optical industry shows that wave front shaping on fractions of the wavelength of visible light (400nm–800nm) is an industrial standard. A typical homogeneity of a glass is $\Delta\epsilon/\epsilon < 10^{-5}$ on length scales of 30cm and more, where ϵ is the dielectric constant or relative dielectric permittivity of the material. In practice, such homogeneity is measured using optic methods in the frequency range of several hundred terahertz that make use of the relation that the square of the refractive index equals the dielectric constant. The homogeneity of the dielectric

constant also holds for the GHz frequencies where electronic applications use glasses. Industrial manufacturing processes yield pristine glass surfaces with a roughness well below 1nm (root mean square [RMS]) and substrate thicknesses between 1mm and 30 μm .

The properties of glasses meet demand in the semiconductor industry, where higher miniaturization is a major trend. Besides reducing structure sizes, miniaturization means, besides reducing structure sizes, integration of different materials and devices, increasing density of I/O, higher data rates, and consequently, frequency components reaching well into the GHz range need to be transmitted. These packaging trends need substrate materials that: 1) Enable high mechanical capability through high stiffness and mechanical stability; 2) Allow economical via formation processes that are capable of forming several thousand holes per second for signal and thermal vias; 3) Have thermal expansion coefficients (CTEs) that are adapted to standard semiconductor materials like silicon and allow co-processing in extremely high process temperatures; 4) Allow defined metallization on smooth surfaces to reduce GHz loss; and 5) Have well-defined homogeneous material parameters at GHz frequencies that are incorporated into the most common RF field simulation software packages. In the current work we analyze how glass and glass interposers can meet these trends and needs in semiconductor packaging and integration.

The main drivers for further integration are wireless communication and

communication at extremely high data rates. Some of the applications are sensors, LiDar, and radar systems for automotive applications. They are operating at 77GHz and require safety relevant information with ever-increasing data quantities to be processed in real time. Wireless communication with the upcoming LTE5 standard increases the number of frequency bands, in combination with the need for more and higher quality filters, as well as high-power GHz applications. Massive multiple-in/multiple-out (MIMO) requests for reliable homogeneous materials for antenna arrays exhibit stable operation over a broad temperature range. In addition, graphic boards with ultra-high data rates exchanged between graphics processing units and graphics memory are a driver for higher integration with high-frequency capability well in the GHz range.

There is extensive development for glass as an interposer material in semiconductor packaging. In [1] interposers in ultra-thin glass are investigated, a general concept that was already described in [2–4].

Mechanical properties of glass substrates

The high Young's modulus of thin glasses leads to substrates with high stiffness and allows precise manufacturing and alignment of multiple layers in 2.5D and 3D integrated stacks. The transparency of glass enables optical alignment of different layers in combination with X-ray alignment of metallized layers. In (Table 1) we compare mechanical properties of different glasses.

| | D 263 eco | MEM | BOROFLOAT 33 | AF 32 | B 270 i | AS 87 eco |
|--------------------|-----------|--------|--------------|--------|---------|-----------|
| E-modulus | 72.9 GPa | 63 GPa | 64 GPa | 66 GPa | 71 GPa | 73.3 GPa |
| Knoop hardness | 590 | 480 | 480 | 555 | 542 | 500 (560) |
| Surface toughening | Good | | | | Good | Excellent |

Table 1: Comparison of the mechanical properties for different substrate glasses. For the glass AS 87 eco, the value in brackets is the Knoop hardness of the chemically strengthened material.

Structuring and via formation of glasses

Short pulse lasers allow structuring of glass [5] with an accuracy below 10 μm (**Figure 1**). Metallization with ample adhesion can be yielded on glasses after proper surface activation. Because glasses have limited thermal conductivity (see next section), additional vias are needed for thermal management.

Thermal properties of glasses

The excellent electrical insulation properties of glass lead to a low thermal conductivity, which is on the order of 1W/(m·K). The thermal resistance of glass in a package can be reduced by using ultra-thin glasses of thicknesses between 25 μm and 125 μm (**Table 2**). That is to say, the heat flux

that is generated within a chip package needs to be well designed for thermal management reasons. Therefore, metal vias will also play a major role in thermal management [6]. Additionally, glasses are available with CTEs that are either adapted to silicon or to other crystalline materials like lithium tantalate. Subsequently, semiconductor packages can be made by employing suitable glasses that are subjected to a minimum of mechanical stress while under thermal processing or under thermal stress. In particular, the management of temperature gradients within a package needs a careful adjustment of the thermal expansion of all materials involved.

Because metals are ductile materials, the opposite of brittle materials like silicon or glasses, a thin metallization of several microns in thickness can be made by copper, silver, or even aluminum even if their thermal expansion is much larger than glass or silicon. In case thicker metal structures are needed for thermal management, the thermal expansion of metals and metal alloys have to be selected in accordance with the packaging materials, as well as with the respective materials within active and passive devices.

Chemical properties

Most glasses are highly stable under chemical

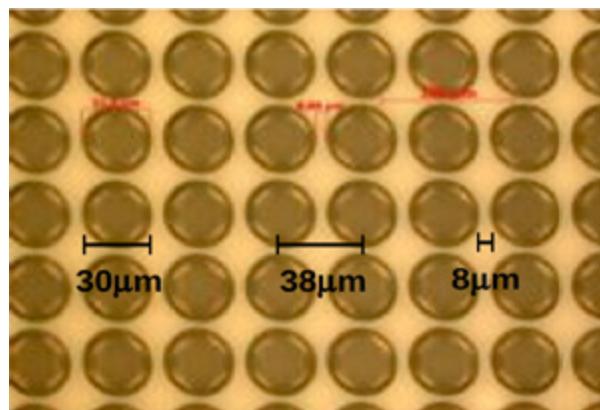


Figure 1: Example of a 50 μm thin AF32 glass, structured using short laser pulses with 30 μm holes with a 38 μm pitch.

attack, which is expressed in particular classes of chemical stability. However, etching with solutions like concentrated hydrofluoric acid is possible in most cases. A further property of glass is ion migration, which allows anodic bonding to silicon wafers for glasses like MEMpax, BOROFLOAT and D263eco.

Surface roughness and structured metallization

Pristine glass surfaces, also called fire-polished glass surfaces, can be made extremely smooth. RMS values for roughness below 1nm are possible directly yielded out of the manufacturing process. These values are hard and extremely expensive to reach by known polishing processes. Any ceramic material has a roughness that is multiple orders of magnitude larger than the roughness of fire polished glasses. The smooth surface becomes increasingly important as soon as electronic devices need to handle high-frequency components. Particularly on the boundary between a dielectric material and a metallization material, roughness leads to loss especially when high-electric field strength is concentrated near the interface between dielectric and metal. After proper surface activation, metallization on glass can achieve high mechanical stability that can even be improved by using a proper adhesion promoter.

Electric properties of glasses at GHz frequencies

A main reason for using glass in semiconductor packaging is its dielectric properties. Glasses are good dielectrics with low loss and small enough dielectric constants to handle parasitic capacitances and to allow for an accurate impedance matching in most of tomorrow's applications. The homogeneity of glasses especially leads to excellent results when field simulations are compared with real high-frequency structures. Depending on the details of an application, a glass with low dielectric loss (e.g., AF32) or with a low dielectric constant ϵ (sometimes represented as "k") is suitable. Here, MEMpax and BOROFLOAT are the substrate glasses with the lowest ϵ values (**Table 3**).

An increasing number of software companies for electrical field simulation incorporate the dielectric properties of SCHOTT substrate glasses into their material database. (Note: CST [7] already implemented the dielectric data of several glasses in its 2016 software release.)

Table 2: The thermal properties of selected glasses show that there are a number of glasses available that have CTE (20–300°C) values close to the CTE of silicon (3.4 ppm/K).

| | D 263 eco | MEMpax | BOROFLOAT | AF 32 | B 270 i | AS 87 eco |
|---|----------------------|---------------------|--------------------|---------------------|---------------------|-----------|
| Average coefficient of linear thermal expansion between 20 °C and 300 °C (CTE, α) | 7.2 ppm/K | 3.25 ppm/K | 3.25 ppm/K | 3.2 ppm/K | 9.4 ppm/K | 8.7 ppm/K |
| thermal conductivity λ | 1.08 W/m K at 100 °C | 1.12 W/m K at 90 °C | 1.2 W/m K at 90 °C | 1.16 W/m K at 89 °C | 1.02 W/m K at 90 °C | |

Table 3: The electrical properties of different substrate glasses are compared.

Summary

The material class of glasses offers numerous possibilities for integration in semiconductor processes. Well-defined dielectric properties allow accurate high-frequency design and laser-based processes can provide highly efficient structuring, via, and hole forming. Metallization is possible with excellent glass-to-metal interfaces that fulfill all necessary criteria in terms of mechanical stability, as well as criteria for electric boundary conditions. SCHOTT is actively supporting production of an industrial supply chain and develops its own processes for glass structuring. Handling concepts, which include frame mounting of structured glass, are also under development.

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Tackling the thermal challenge chip-scale packaging creates for high-power LEDs

By Giles Humpston [Cambridge Nanotherm]

While chip-scale packaging (CSP) has been around since the 1990s (and in production since the early 2000s), the LED industry has only adopted CSP approaches in earnest within the last few years.

Lumileds initially launched CSPs for mid-power blue backlighting applications in 2013, replacing mid-power plastic-leaded chip carrier (PLCC) LEDs. Lumileds subsequently developed a white flip-chip CSP high-power LED (HP-LED) for use in general lighting. Since then, other companies such as Nichia, Seoul Semi, and Samsung have introduced several HP-LED CSP products to the market, and things show no signs of slowing down. Market analysts at Yole Développement estimate CSPs will make up 34% of the HP-LED market by 2020.

The CSP difference

A chip-scale package in the LED industry (as in other industries) is a package that is no more than 1.2 times the size of the chip. At the simplest level, the use of chip-scale packaging involves reducing the size of a packaged LED by stripping out certain materials.

By way of background, the LED landscape can be divided into packaged and unpackaged LEDs. Packaged LEDs can be made into modules by printed circuit board (PCB) assembly lines using standard pick-and-place equipment. In the case of HP-LEDs, this packaging usually incorporates a ceramic submount to act as a heat spreader. Unpackaged bare die, by way of contrast, are used to make chip-on-board (CoB) LED devices and arrays. These can require specialized wire bonding equipment and the application of a phosphor before they are usable. While unpackaged flip-chips have enabled CoB LED manufacturers to place die closely together, they require high-precision pick-and-place machines in clean room facilities — not something most PCB assembly lines have.

CSP LEDs (while, technically, a “packaged” LED) effectively bridge this divide between “packaged” and “unpackaged” LEDs. By

metalizing the P and N junctions on the bottom of the bare die and then adding a phosphor onto the top, CSPs are “packaged” in the sense that they can be directly soldered onto a module PCB using standard pick-and-place equipment and made into a luminaire by adding a lens and a heat sink.

Benefits of CSP to LED designs

Using CSP, manufacturers can cut out several manufacturing steps and cut down on the materials used (such as ceramic submounts or PLCCs), thereby reducing costs. Additionally, with CSP LEDs, “level 2” module integrators not only get a cheaper product, but can also make LED modules using standard PCB assembly lines (PCBA) without the need for high-precision pick-and-place lines, wire bonding and other specialized infrastructure, which changes the dynamic within the industry. PCBA lines can now use more affordable CSP LEDs to build custom modules, whereas previously they were limited to more costly packaged LEDs. And as CSP LEDs are only a fraction larger than the die, and don’t need wire bonding, they can be placed much closer together. This means modules can be made more power dense than previously possible with packaged LEDs, coming close to bare die CoB performance.

Outlining the heat problem of CSP

While the benefits of CSP HP LEDs are compelling, however, the shift towards CSPs forces level 2 module and luminaire designers to face a more fundamental challenge: heat. HP-LEDs are on average only about 40% efficient, which means that 60% of the power put in comes out as heat. If this heat cannot escape into the surrounding atmosphere quickly enough, it can reduce the lifespan of the LED, affect the light quality, and cause color fluctuations.

Heat from an LED die cannot escape through atmospheric radiation because of the insulating encapsulant lens. Instead, the heat must conduct downwards through multiple materials before radiating out into the ambient atmosphere via a heat sink as indicated in **Figure 1**. The figure also illustrates that high-power packaged LEDs have traditionally featured a submount, typically some form of ceramic that’s not present in CSP LEDs. This is very effective at spreading the heat from the die before it hits the circuit layer, and then the module PCB, usually a metal-clad PCB (MCPCB). Here the heat conducts first through the MCPCB’s thermally conductive (but electrically insulating) dielectric layer, then through the remainder of the metal board to the heat sink. Moving from this traditional ceramic submount package to a CSP LED effectively removes the submount from

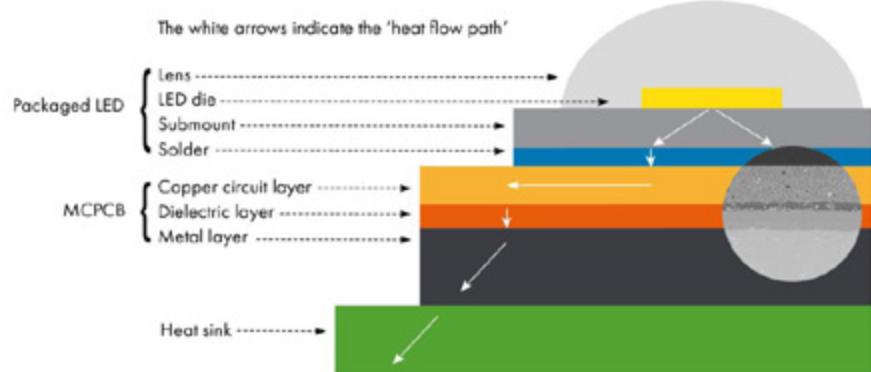


Figure 1: Heat flow path for a typical LED.

the thermal path. As a result, the heat will now hit the copper circuit of the MCPCB as a much more intense point source. It is therefore essential that the MCPCB can cope with this localization of heat.

Level 2 integrators need to develop a better understanding of the principles of thermal design to overcome the thermal issues that, in the case of CSPs, have suddenly become their problem with which to deal.

In determining how a thermal management solution can best deal with heat removal from such an intense heat source, it would be worth taking a moment to examine, in a little more detail, a couple of the key factors affecting the movement of heat through a thermal array.

Axial vs. radial conductivity in LED design

In most CSP LED board designs, efficiency of axial (z-axis) thermal conduction (i.e., down through the copper circuit and through the MCPCB) tends to play a more important role than radial (x/y axis) conduction (i.e., sideways through the copper circuit).

Consider a standard CSP LED soldered onto a copper circuit layer of around 50 μm thick and 35mm in diameter, which in turn sits on a dielectric, and then an aluminum heat spreader. Depending on the grade of the board, the thermal conductivity of the dielectric will typically range from around 3–10W/mK and between 10–50 μm in thickness, which means the axial thermal impedance will range between 0.16 and 0.01°C.cm²/W. For a slab of dielectric measuring 10mm on a side, every watt of heat flowing will not pass through instantly, but result in the calculated temperature difference (0.16 – 0.01°C) between the two faces.

In terms of radial thermal conductivity, copper is an excellent conductor of heat, with a thermal conductivity of almost 400W/mK. But at only 50 μm thick — half the thickness of a human hair — its ability to transport heat along its length is severely restricted. Taking a bar of copper 1mm wide by 50 μm thick by 5mm long, the thermal resistance from end to end is more than 250°C/W, which is huge compared to the axial thermal resistance. So when the copper disk is attached to a dielectric layer with very low thermal resistance, most of the heat will promptly disappear through the dielectric and down to the heat sink and none will get as far as the edge of the copper area.

In practice, to optimally cool CSP LEDs, a balance between the axial and radial conductivities is essential. If the copper

area is overly reduced, too much reliance is placed on axial conduction so the thermal resistance goes up. This means that close packing of CSP LEDs can result in thermal imbalance over the array area. Conversely, making the copper area excessively large has little benefit because of its high in-plane thermal resistance, which prevents the heat spreading any significant distance. A convenient rule of thumb is that for 35 μm -thick copper on a decent quality MCPCB, any copper further than 1.75mm from the

heat source (i.e., the heat source is on a 3.5mm diameter disc of copper) will not participate in cooling the LED.

Interface heat resistance across a thermal array

There are several other issues that affect the movement of heat, including the number of interfaces between the various materials that make up a CSP LED MCPCB stack—such as the LED package, solder joint,



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circuit board, thermal interface material, heat spreader, and many more. Each of these structures have vastly different dimensions, thermal conductivities and specific heat capacities, with various interface resistances between all the different layers. Of these, interface resistance is the most critical and the hardest one to model. The thermal resistance of a single interface can outweigh the thermal properties of the other materials in the structure and completely confuse any thermal calculations. The best technical solutions, therefore, seek to minimize interface resistance between elements in the board—the ideal method being the elimination of as many discrete layers as possible from the structure.

In addition, coatings and other layered constructions are particularly vulnerable to high interface resistance and the possibility the quality will erode over time. While homogeneous materials are the easiest to predict, if an assembly of different materials is necessary, the most robust and reliable approach to reducing the thermal resistance is to achieve bonding at the atomic level where possible between materials. Only a limited range of coating and deposition processes function on this premise.

Existing thermal management for CSP MCPCBs are not suitable

Bearing in mind principles such as those noted above, how does the industry currently try to remove heat from its designs, what is wrong with these approaches when it comes to CSP MCPCBs, and what better approach can be employed?

Almost all conventional MCPCBs follow the same basic format. They are manufactured from a sheet of metal (usually aluminum) covered with a thin ($30\mu\text{m}^+$) layer of copper for the wiring trace. This copper sheet is attached (and electrically isolated from the metal base) by a dielectric layer of epoxy resin filled with particles of thermally conductive ceramic to increase thermal performance. However, there is an upper limit to how much thermally conductive ceramic can be incorporated. Overload the epoxy with ceramic and the dielectric layer becomes friable and the adhesion to the metal substrate and copper wiring trace will be poor. This affects the ability of the product to be able to last several decades (50,000 hours) of active use.

While there are always new developments in these thermally conductive dielectrics, there is always a trade-off between performance and durability. This limits the performance of MCPCBs to a composite thermal conductivity of well under 100W/mK .

This thermal performance is perfectly acceptable for most LED module designs, but when it comes to CSP modules, particularly for power dense designs, they simply do not offer the required performance. Historically, there has only been one option available to manufacturers when the thermal performance of MCPCBs falls short of requirements, and that was to move to a wholly ceramic substrate such as aluminum nitride—a material that's as exceptionally high in thermal conductivity as it is in price.

Nanoceramic directly addresses the CSP heat problem

By taking the best elements of both ceramic and metal-clad PCBs, Cambridge Nanotherm has developed a product that addresses the heat challenge head on. This solution – nanoceramic – uses the primacy of axial conduction and low interface resistance to optimum effect.

For the dielectric layer for the MCPCB, a patented electro-chemical oxidation (ECO) process converts the surface of a sheet of aluminum to a layer of alumina (Al_2O_3) that is just tens of microns thick. While alumina is not a particularly efficient thermal conductor (around 7.3W/mK for the alumina created by the ECO process), the thinness of the layer means heat has an extremely short journey to make before hitting the aluminum base, so the thermal resistance of this layer is exceptionally low. This property, combined with the high dielectric strength of ECO alumina ($>50\text{V}/\mu\text{m}$) makes it an extremely effective dielectric option.

While in the case of Nanotherm's "LC" product for MCPCBs, the circuit layer is still attached by a layer of $3\text{--}5\mu\text{m}$ of epoxy, the ECO conversion process atomically bonds the alumina dielectric layer to the aluminum base from which it was formed. This helps to reduce and stabilize the thermal resistance of this interface and therefore the thermal resistance of the overall stack. The ECO process also makes the dielectric layer impressively robust — it is impossible to mechanically cleave the nanoceramic off the aluminum from which it was formed. This combination of a very thin dielectric layer with relatively high thermal conductivity, atomically bonded to the aluminum base results in an MCPCB that, while affordable, and machinable via traditional MCPCB processes, has an overall thermal conductivity of around 115W/mK . This sits within the comfort zone of many CSP HP LED applications, and marks a major improvement on existing MCPCB solutions.

By offering thermal performance that is tailored to the intense point flux requirements of CSP LEDs, along with drop-in manufacturability, MCPCBs with nanoceramic dielectrics are enabling CSP LED designers to continue to push the limits of their designs, creating smaller, brighter and more cost-effective light sources.

Biography

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Current and future applications for fan-out WLP/PLP glass carrier substrates

By Kazutaka Hayashi [AGC Asahi Glass]

Over the past few years, fan-out wafer-level packaging (FOWLP) and panel-level packaging (PLP) processes have grown increasingly popular with both semiconductor foundries and outsourced assembly and test companies (OSATS). The shift toward next-generation mobile, RF and automotive products has driven the need for thinner packages, fueling interest in moving from fan-in to fan-out package structures.

Fan-out technology is an enhancement of standard WLPs developed to provide a solution for semiconductor devices requiring a higher integration level and a greater number of external contacts. Its advantages include: 1) ultra-thin, lighter packages with higher input/output (I/O); 2) the ability to create heterogeneously combined solutions, i.e., system-in-package (SiP) and package-on-package (PoP), with reduced footprint and form factor; 3) lower power consumption; and 4) ultra-high processing speed – to name a few.

A key consideration in fan-out processes is the choice of carrier substrate, which can truly make or break the package. While several different materials can be used as the carrier, glass offers unique benefits that will contribute to further advancement and adoption of fan-out solutions.

Fan-out process

To grasp the importance of the carrier substrate, it's useful to understand the evolution of the fan-out process, as well as how it typically works today. FOWLP made its first appearance in 2006 with Infineon's introduction of its embedded wafer-level ball grid array (eWLB), which it subsequently licensed to most of the leading OSATS. However, recent market requirements for SiP solutions – particularly, miniaturized SiPs for mobile applications – have heightened

interest in implementing packages built using fan-out technology.

Industry experts such as analyst firm Yole Développement, which has tracked the evolution of FOWLP and FOPLP processes, cite 2016 as a turning point for fan-out technology. Apple's iPhone 7, launched last year, contains a chip built by TSMC using its proprietary integrated fan-out (InFO) technology, underscoring FOWLP's viability for volume production. In addition, Yole foresees significant growth in PLP, expecting it to reach a market value of US\$405 million by 2020. Products that may particularly benefit from fan-out panel packaging include such midrange communication devices as baseband processors, power management modules, and radio-frequency ICs (RFICs).

FOWLP combines multiple die from heterogeneous processes into a compact package. (Figure 1) illustrates the typical steps in the FOWLP process. In this particular approach (known as chips-last or RDL-first), the redistribution layer (RDL) is first created on a carrier substrate, and individual die are then placed and covered with a molding material. The entire package is exposed to ultraviolet (UV) irradiation to deform the molding layer, followed by removal/de-bonding of the carrier wafer, solder bump formation and, finally, singulation of the individual packages. The chips-last/RDL-first approach allows the use of only known good die and known good RDL, while eliminating through-silicon vias (TSVs) and removing the substrate lowers costs and package thickness,

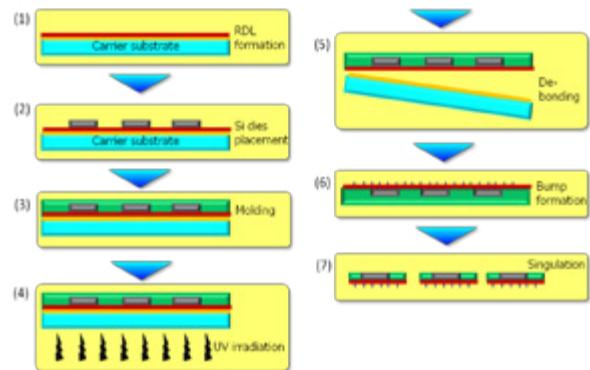


Figure 1: Schematic illustration of a typical FOWLP process (RDL-first).

and affords electrical advantages. The FOPLP process is similar, but entails the use of a square or rectangular package rather than a round one.

Fan-out challenges

The carrier substrate material selected is of vital importance, as a number of challenges have been identified regarding the manufacture of these advanced fan-out packages. These include the following:

CTE matching. To minimize warping after the molding step, the carrier's coefficient of thermal expansion (CTE) must be very close to that of the molding material, e.g., epoxy, resin, or glass composites with silica filler.

Strength. Breakage is a huge problem with respect to its impact on package cleanliness; it creates particulates that affect throughput and yield. The carrier substrate must therefore possess high tensile strength.

Heat resistance. Plastics deform at temperatures as low as 100-200°C, so a hardy material is a must to maintain structural integrity throughout the fan-out process.

Stiffness. If the package is slightly smaller than the panel or wafer, the substrate can bend when it's inserted,

| Requirement | Negative Effects | Glass | Si | Resin | Metal | Advantages of Glass |
|-----------------------|-----------------------------------|-------|---------------------------|-----------|---------|--|
| Stiffness | Gravitational sag | Good | Very Good | Poor | Good | 60-100 GPa in Young's modulus |
| | Warpage | | | | | Sufficiently high strength can be obtained by removal of surface flaws |
| Strength | Breakage of substrate | Good | Good | Poor | Good | Tg of typical substrate glass is >500 °C |
| Heat resistance | Deformation | Good | Good | Poor | Good | |
| CTE matching | Warpage | Good | Poor (only 1 type of CTE) | Poor | Poor | Fine adjustment can be performed in the range of 3-12 ppm/K |
| Chemical durability | Degradation by chemical treatment | Good | Good | Good | Average | Generally sufficient durability is obtained |
| Optical transmittance | UV de-bonding | Good | No transparency | Good/Poor | Poor | Approx. 300-350 nm |
| Scalability | Non-realization of panel size | Good | Up to 12" wafer | Good/Poor | Good | Glass shape: wafer and panel, panel dimension: Up to approx. 3m square |
| Flatness | Stable reconstructed wafer | Good | Good | Poor | Average | Flat glass sheet can be fabricated using float process, etc. |

Table 1: Glass provides numerous advantages as a fan-out carrier substrate (GPa = gigapascals; Tg = glass transition temperature).

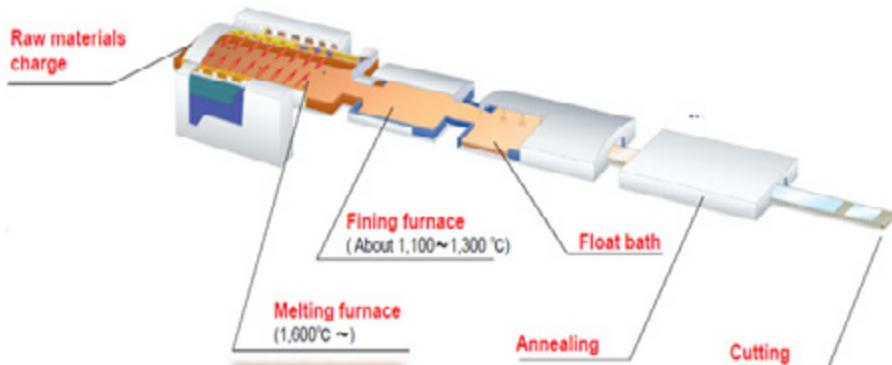


Figure 2: AGC's float process technology enables stable production of relatively thicker glass due to its horizontal configuration.

so the material must be hard enough to prevent bending.

Cost. Glass is much more cost-efficient – in part, because fewer techniques to mitigate its shortcomings are required than with other substrate materials.

Optical transmittance. As mentioned above, UV irradiation is used to deform the molding layer. This is a critical step, and requires a material that can effectively transmit the UV rays.

Flatness. Regardless of shape, the carrier must retain a stable, flat shape. This is difficult to achieve with some commonly used materials, such as resin or metal. This brings us to glass.

Why glass?

Glass offers significant advantages over other carrier substrate materials in all of the aforementioned areas. Its

advantages include high transparency, high stiffness, high heat resistance, and the ability to match CTE for a wide range of materials. (**Table 1**) offers a side-by-side comparison illustrating how glass fares compared to resin and metal.

Demand for substrates with a midrange CTE (~6ppm/K) is most common, but access to higher or lower CTE glass is highly valuable. When used properly, glass substrates can help suppress warpage caused by molding. However, the

reality is that it's not enough to suppress warpage simply by matching the CTE between the glass and resin-Si die composite because there will be some fluctuation of CTE caused by instability during the resin curing process. Thus, there are two key approaches for further suppressing warpage.

The first is to increase the Young's modulus (i.e., stiffness) of the glass. A measure of elasticity, equal to the ratio of the stress acting on a substance to the strain produced, the Young's modulus depends on the chemical composition and structure of the glass. Generally, glass with stronger interatomic bonds and higher bond density exhibits a higher Young's modulus. Experiments utilizing various elemental compounds have yielded new, stronger glass substrates with an optimal balance of stiffness and elasticity to meet manufacturers' requirements.

The second way to minimize warpage is to implement a thicker substrate, for which the main production methodology employed by AGC Asahi Glass (AGC) is well suited. Called the float process, it involves literally floating the molten glass on a bath of liquid tin, producing a perfectly flat surface on both sides (see **Figure 2**). To this end, AGC is focused on developing a high-elasticity glass substrate with CTE compatible to that of a resin-Si composite.

Range of glass substrates widens options

Because the CTE of the glass substrate needs to be matched to that of the molding resin and silicon composite, AGC has developed several types of glass for fan-out WLP/PLP,

| Property | units | New glass (Borosilicate) | Silica glass | Soda-lime glass |
|--------------------------------------|-------|--------------------------|--------------|-----------------|
| 0.5mm thickness Transmittance @254nm | % | >80% | 90% | <20% |
| CTE(25-300) | ppm/K | 5.2±0.2 (5-7) | 0.5 | 8-9 |
| Strain point | °C | 466 | 1120 | 511 |
| Softening point | °C | 710 | 1683 | 737 |
| Density | g/cm³ | 2.3 | 2.2 | 2.5 |

Table 2: New UV-C glass with high optical transmittance is being developed to offer improved performance in other areas as well (all data for reference only).

with a CTE ranging from 3 to 12ppm/K. Non-alkali glass is available with a CTE of up to 8ppm/K.

The choice of glass type typically depends on the application. Alkali ions have high mobility due to their low positive charge (+1), which means they can generate higher contamination if the alkali diffuses between the glass and RDL layer. If a user's application doesn't hinge on this issue, alkali glass is perfectly acceptable. Non-alkali glass is preferable for semiconductor fabrication, as it causes virtually no contamination from alkali ions. It has also been used widely for manufacturing thin-film transistor liquid crystal displays (TFT-LCDs).

Another next-generation glass substrate under development is a high-UV light transmittance glass substrate with CTE controllability that enables the de-bonding process to be applied using UV-C light (200-280nm). Currently, de-bonding is achieved by using UV-A light (315-380nm) to decompose the resin adjacent to the glass substrate. However, UV light with a lower wavelength can accelerate decomposition and lead to faster de-bonding, creating demand for a glass substrate with high-UV transmittance. While this applies to silica glass (SiO_2), it has a very low CTE (~0.6ppm/K). Soda-lime glass has wider availability than silica glass in general, but it has poor optical transmittance combined with a high CTE. (**Table 2**) exemplifies how the new glass will compare to these other alternatives.

Summary

It will be exciting to see how materials and device makers' roadmaps evolve as consumer requirements continue to place further pressure on the manufacturing process. One thing seems certain: demand for fan-out WLP and PLP solutions will only increase.

As fan-out packaging grows in popularity, a stable carrier substrate is increasingly needed that exhibits essential characteristics, including low warpage/breakage and high strength, stiffness, flatness and optical transmittance. Glass has been shown to exhibit all of these properties, making it far more desirable compared to such other common carrier substrate materials as glass and resin.

To meet a range of industry needs, AGC is making available a line of alkali and non-alkali glass substrates with a broad range of CTEs – in rectangular and square shapes, as well as traditional round wafers – with thicknesses ranging from 0.2mm to 2mm. The company also has an eye toward the future with the development of next-generation substrates: one combining high elasticity with high

thickness; and one seeking to enable UV-C rays to speed and facilitate de-bonding during the fan-out process.

Biography

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Recent advances and trends in advanced packaging

By John H. Lau [ASM Pacific Technology Ltd.]

Recent advances in flip-chip technology, fan-in wafer-level packaging, fan-out wafer-level packaging, 3D IC integration, embedded 3D hybrid integration, 2.5D IC integration, through-silicon via-less (TSV-less) interposers, and Cu-Cu hybrid bonding will be presented and discussed in this study. Emphasis is placed on the developments of these technologies in the past few years. The latest trends in semiconductor packaging will also be briefly mentioned.

Flip-chip technology

Recently, because of the requirements associated with higher functionalities of chips along with shrinking of their area, the number of pin-outs increases while pitch decreases. Also, because of the trend toward smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks and digital cameras) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and thinner package substrates lead to the necessity of using thermocompression bonding (TCB) for flip-chip assemblies. In this study, besides mass reflow, various TCB techniques are presented. Because wafer bumping is the mother of flip-chip technology, it will be briefly mentioned first. The C4 (controlled-collapse chip connection) bump was invented by IBM in the mid-1960s [1] and has been used extensively since then. Because of higher pin-count and tighter pitch, there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [2] and Cu-pillar with solder cap [3, 4] can be a solution. Their fabrication process (**Figure 1**) is basically the same as that of the C4 bumps except Cu electroplating is used instead of solder as shown in step #5 on the lower right-hand side of (**Figure 1**). It is followed by electroplating the solder cap and then reflowing the solder with flux. Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the

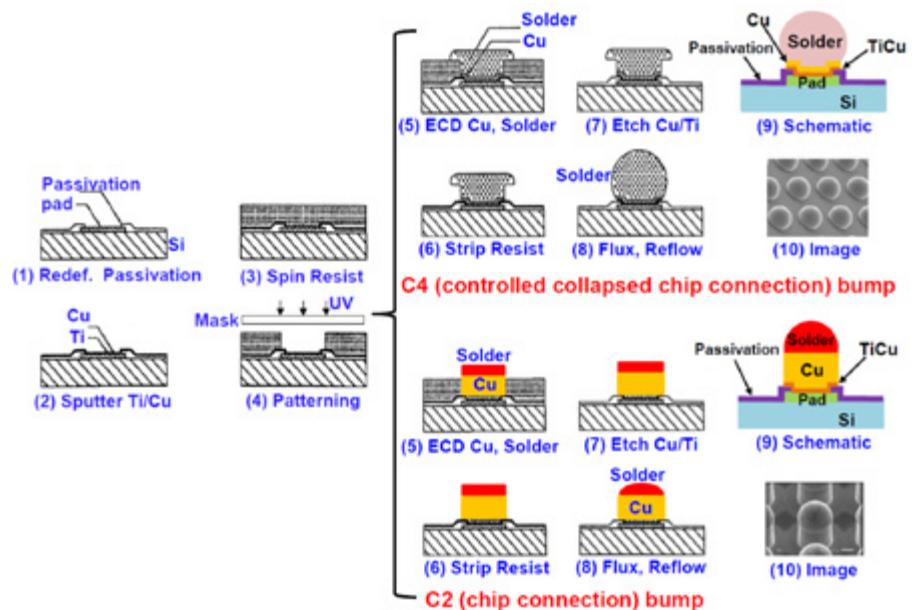


Figure 1: C4 and C2 wafer bumping processes.

self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity (W/m. K) and electrical resistivity ($\mu\Omega\text{m}$) of Cu (400 and 0.0172) are superior than those (55–60 and 0.12–0.14) of solder [5], as shown in (**Table 1**).

Basically, there are two groups of flip-chip assemblies: one is with an intermediate layer between the bonding pads, and the other is not, i.e., nothing! A flip-chip assembly with intermediate layers such as solder for mass reflow and Cu-pillar with solder cap for TCB are called indirect bonding, which is the focus of this section. Cu-to-Cu diffusion bonding, which has nothing between the bonding pads on the chip/wafer, is therefore, called direct bonding (which will be mentioned in the other section.)

Basically, there are four different flip-chip assemblies with intermediate layer (**Figure 2**), namely: a) mass reflow of chips with C4 or C2 bumps with capillary underfill (CUF); b) TCB with low-force of chips with C2 bumps with CUF; c) TCB with high-force of chips with C2 bumps with nonconductive

| Structure | Major Material | Thermal conductivity (W/m K) | Electrical resistivity ($\mu\Omega\text{m}$) | Pad pitch | Self alignment |
|-----------|----------------|------------------------------|--|-----------|----------------|
| C2 bump | Cu | 400 | 0.0172 | Smaller | Smaller |
| C4 bump | Solder | 55–60 | 0.12–0.14 | Larger | Larger |

Table 1: C4 vs. C2 bumps.

paste (NCP) underfill; and d) TCB with high-force of chips with C2 bumps with nonconductive film (NCF) underfill. Solder mass reflow (**Figure 2a**) of chips with C4 bumps have been used for flip-chip assembly for almost 50 years. (**Figure 3**) shows the cross section of an iPhone 6 Plus. It can be seen that the A9 application processor (AP) is housed in the bottom package of a package-on-

package (PoP) format and the C4 solder bumped flip chip is mass reflowed on a 2-2-2 organic build-up package substrate with underfill. The solder mass reflow of a chip with C2 bump is seldom used

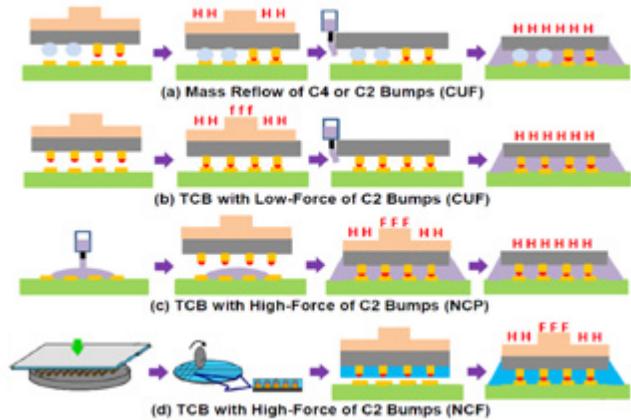


Figure 2: Various flip-chip assembly processes. a) Mass reflow of chips with C4 or C2 bumps with CUF; b) TCB with low-force of chips with C2 bumps with CUF; c) TCB with high-force of chips with C2 bumps with NCP; and d) TCB with high-force of chips with C2 bumps with NCF.

because its self-alignment characteristic is nowhere near the C4 bump.

In the past few years, TCB of chips with an intermediate layer such as C2 bumps has been attracting attention for high-density, thin-chip, thin-substrate, and ultra-fine pitch flip-chip assemblies. Basically, there are two methods, one is with low-bonding force and the other is with a high-bonding force. For the one with low bonding force, the assembly process is simple, as **Figure 2b** shows: 1) First, use the look-up and look-down camera to locate the position of the C2 bumps on the chip

and their corresponding pads on the substrate; 2) Apply flux on the solder cap or on the substrate or both; and 3) Pick-and-place the chip on the substrate and then apply temperature (H) to melt the solder and a low force (f) to hold the chip at a certain distance from the substrate. **Figure 4** shows a typical cross section of a flip-chip assembly with TCB with low force on the chip with C2 bumps [6].

High-bonding force TCB of the chips with C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate (**Figure 2c**) was first studied by Amkor [7] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone as shown in **Figure 5**. The NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

Fan-in wafer-level packaging

Fan-in wafer-level packaging (WLP) has been used extensively in most consumer products in the past 16 years. The packages made by the fan-in WLP method are called wafer-level chip-scale packages (WLCSP). The most advanced WLCSP is TSMC's UBM-free integration (UFI) WLCSP [8].

(Figure 6) shows the cross section of TSMC's UFI WLCSP. It can be seen that there is not an under bump metallurgy (UBM) at the end of the redistribution layer (RDL) for the solder bump. A polymer composite protection layer (PL) is introduced to secure the solder bumps. TSMC found that because of [8]: 1) The mechanical support of the PL, 2) The controlling of the maximum strain location, and 3) The material optimization, the UFI WLCSP solder joint is reliable (the characteristic life is more than 800 cycles and the thermal cycling takes place between the temperatures of -40 and +125°C, at one cycle per hour) even for a chip size up to 10.3mm x 10.3mm without underfill.

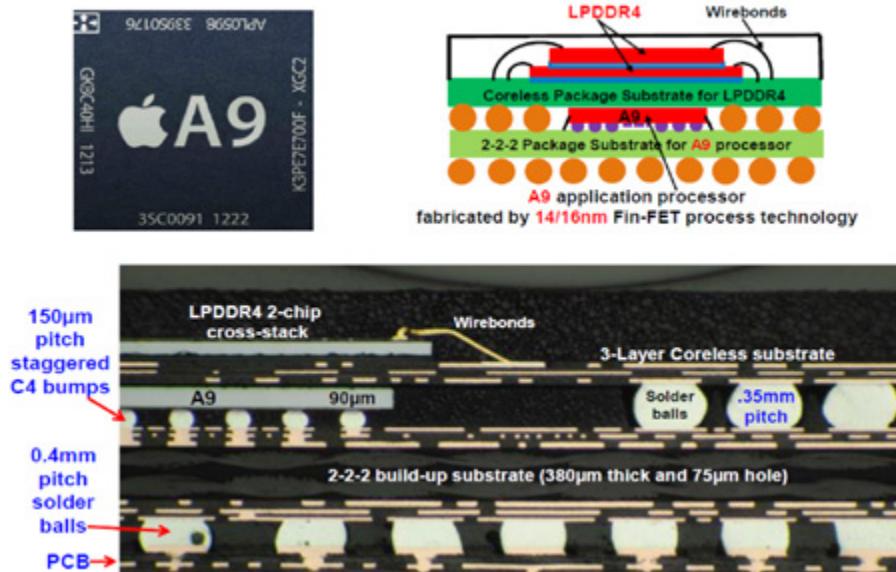


Figure 3: Cross section images of iPhone 6 A9-chipset packaging.

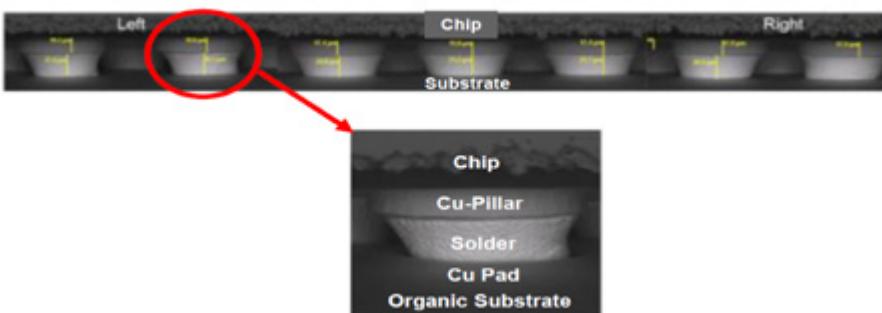


Figure 4: Cross section image of a flip-chip assembly with low-force TCB (CUF).

Fan-out wafer-level packaging

Flip-chip technology and fan-in WLP are facing stiff competition. Some of their market share will be taken away by the fan-out wafer/panel-level packaging (FOW/PLP or simply FOWLP) technology [9-11]. (**Figure 7**) shows the schematic and scanning electron microscope (SEM) images of the cross section of the PoP that houses the Apple A10 AP and mobile dynamic random access memories (DRAMs) of the iPhone

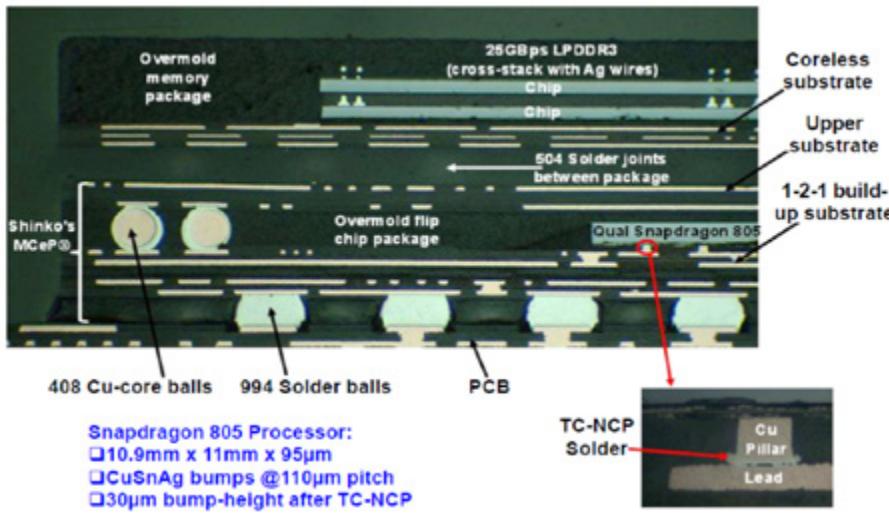


Figure 5: Cross section image of Qualcomm AP-chipset packaging with high-force TC-NCP.

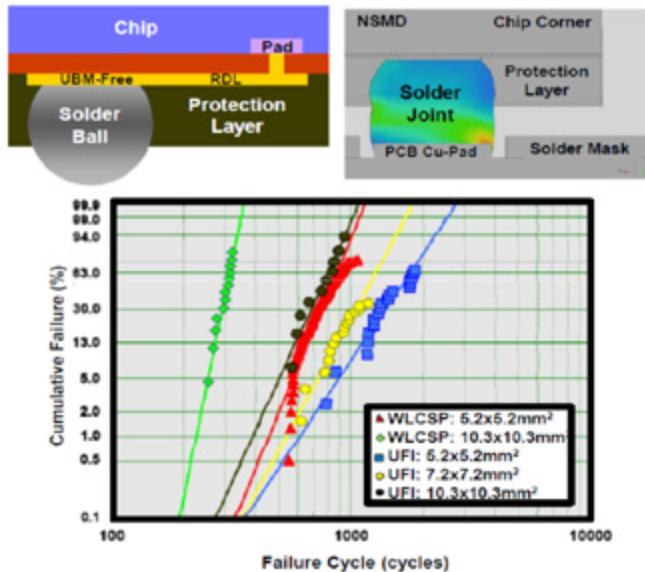


Figure 6: TSMC's UFI WLCSP with polymer composite protection layer.

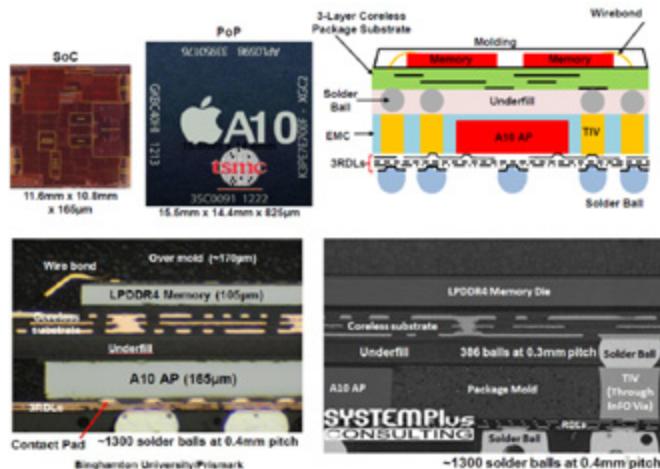


Figure 7: Cross section images of iPhone 7/7+ A10-chipset packaging.

baseband, power management integrated circuits (PMICs), radio-frequency (RF) switch/transceiver, audio codec, micro control unit (MCU), RF radar, connectivity ICs, etc., it can also be used for packaging high-performance and large ($>120\text{mm}^2$) system-on-chip (SoC) ICs, such as APs. Furthermore, with the popularity of system-in-package (SiP), fan-out (which can handle multiple dies and discrete components) will be used more because the fan-in WLCSP can only handle single die.

3D IC integration

Samsung mass-produced (August 2014) the industry's first through-silicon via (TSV)-based 64GB double data rate type 4 (DDR4) DRAM stack module (**Figure 8**). Each stack has 4 DRAMs, each DRAM die has 78 TSVs, and the DRAM stacks are on a printed circuit board (PCB). The module performs twice as fast as a module that uses wire bonding packaging technology, while consuming approximately half the power. The module is for environmentally friendly server applications. On November 26, 2015, Samsung started to produce the 128GB registered dual inline memory module (RDIMM).

(**Figure 9**) shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28nm process technology and is supported by four high-bandwidth memory (HBM) cubes manufactured by Hynix. Each HBM consists of four DRAMs with C2 bumps and a logic base with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28mm x 35mm), which is fabricated by UMC with a 64nm process technology. The final assembly of the TSV interposer (with C4 bumps) on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

This PoP is fabricated by TSMC with its integrated fan-out (InFO) WLP technology [9]. It can be seen from the bottom package that the wafer bumping, fluxing, flip-chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the A9 AP shown in **Figure 3**) have been eliminated and are replaced by the RDLs (for the A10 AP as shown in **Figure 7**). This results in a lower cost, higher performance, and lower profile package.

The points noted above are very significant because Apple and TSMC are the trendsetters. Once they used the technology (September 15, 2016), it became likely that many others will follow. Also, this means that FOWLP is not only for packaging

(**Figure 10**) shows Nvidia's Pascal 100 GPU, which shipped in the second-half of 2016. The GPU is built on TSMC's 16nm process technology and is supported by four HBM2 (16GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with C2 bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are on top of a TSV interposer (1200mm^2), which is fabricated by TSMC with a 64nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with C4 bumps.



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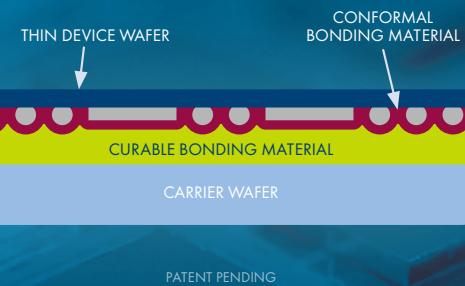
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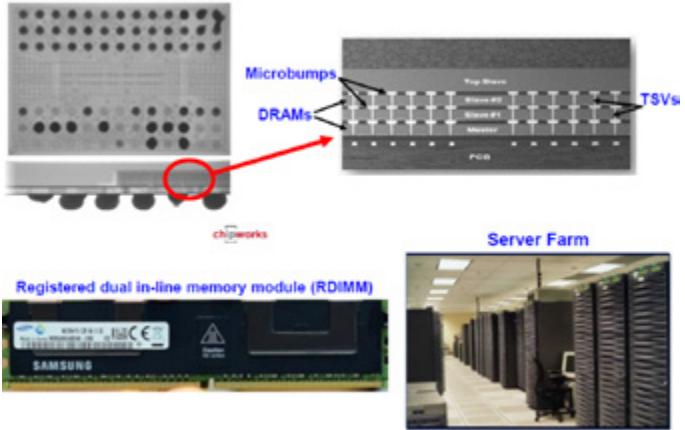


Figure 8: Samsung's DDR4 with TSV for servers.

Both Samsung and Hynix use the high-bonding force TCB of the C2 bumped DRAMs with NCF (after singulation from the NCF laminated C2 bumped wafer), as shown in (Figure 2d) to fabricate the 3D IC integration stack. This 3D memory cube is stacked one chip at a time and each chip takes ~10s for the underfill film to gel, the solder to melt and solidify, and the film to cure. Throughput is a problem, however.

In order to resolve this problem, Toray [12,13] proposed a collective bonding method, which is shown in (Figure 11). It can be seen that the C2 chip with NCF is pre-bond (bond force = 30N, temperature = 150°C, and time <1s) on a stage with temperature = 80°C. For post-bond (first step (3s): bond-force = 50N, temperature = 220–260°C, second step (7s): bond-force = 70N, temperature = 280°C) on a stage temperature = 80°C. Therefore, instead of using 40s in stacking up four chips by the conventional method, it only takes less than 14s by the collective TCB method. Some images of the cross section of the proposed collective bonding method are shown in (Figure 11). Reasonable good joints are achieved with optimized conditions.

(Figure 12) shows Intel's Knights Landing CPU with Micron's HMC (hybrid memory cube), which have been shipping to Intel's favorite customers since the second-half of 2016. It can be seen that the 72-core processor is supported by 8 multi-channel DRAMs (MCDRAM) based on Micron's HMC technology. Each HMC consists of 4 DRAMs and a logic controller (with TSVs), and each DRAM has >2000 TSVs with C2 bumps. The DRAM + logic controller stack is attached to an organic package substrate. Micron's current HMC assembly process is different from that of Samsung and Hynix. Instead of using high-force TCB-NCF (Figure 2d), Micron uses low-force TCB with CUF (Figure 2b). Again, just like Samsung and Hynix, Micron has to do it one DRAM at a time, so throughput is a problem.

Embedded 3D hybrid integration

Currently, a polymer-based waveguide is the most popular choice for optical interconnect packages due to its low cost, suitability for mass production, high thermal stability, and low optical loss [14-20]. The typical loss for the waveguide used in optical PCBs, depending on the fabrication process, materials, and its cross-sectional area, ranges from 0.6dB/cm to 0.05dB/cm. Depending on the fabrication process and materials, polymer properties can have a thermal stability of more than 260°C, which is adequate for a lead-free assembly process [21].

In order to make the package more compact, lower the package profile, enhance the performance, and lower the cost, the optical interconnect of a 3D hybrid IC integration SiP is embedded into an optical polymer waveguide PCB (or organic substrate) [19,20].

(Figure 13) shows a 3D hybrid optoelectronic system with electrical and photonics ICs for super-thin, super-light, high-performance, and low-cost applications [19,20]. The entire system consists of a PCB made of, e.g., FR (frame retardant)-4 material or a substrate made of, e.g., BT (bismaleimide-triazine) material with an embedded optical polymer waveguide, an embedded vertical cavity surface emitted laser (VCSEL), an embedded LD (laser driver), an embedded serializer, an embedded photodiode detector (PD), an embedded TIA (transimpedance amplifier), an embedded deserializer, and heat slugs with or without heat spreader. Two 45° mirror couplers are formed at both corners of the waveguide by using an excimer laser [16] or a 90° diamond dicing blade [17]. The bare VCSEL, LD, and serializer chips are stacked and then attached on one end of the embedded optical polymer waveguide in the PCB. It is noted that since the VCSEL is so close to the mirror of the optical polymer waveguide, an optical lens is optional. Similarly, the bare PD, TIA, and deserializer chips are stacked and then attached on the other end of the embedded optical polymer waveguide in the PCB. Both the 3D stacked hybrid chip sets are encapsulated by special underfills, e.g., transparent polymer.

As shown in (Figure 13), the VCSEL (with light emitting from the back-side of the chip) is flip-chip bumped with any materials on the LD chip with TSV, which is solder bumped flip chip on the serializer chip. Larger bumps with any materials are mounted (or bumped) on the serializer chip while it is in a wafer format.

After dicing the 3D hybrid IC chip set, it is placed in the cavity of the PCB (or substrate) on top of the embedded polymer waveguide. Special encapsulants, such as the transparent polymer, may be needed to protect the chip set. If it is needed, a heat slug or any conductive materials can be attached to the backside of the serializer chip by a thermal interface material (TIM). Again, if it is needed, a heat spreader can be

attached to the top side of the heat slug with a TIM.

Similarly, the PD chip is a solder bumped flip chip on the TIA chip with TSV, which is then solder bumped flip chip on the deserializer chip. The thermal management techniques are the same as those of the VCSEL chip set. In this case, underfills may be needed: 1) between the VCSEL chip and VCSEL driver chip; 2) the VCSEL driver chip and serializer chip; 3) the PD chip and TIA chip; and 4) the TIA chip and deserializer chip.

In many applications, the serializer and deserializer chips may not be needed or have to be placed outside the PCB. Also, when the heat dissipation of the driver and TIA chips is not very large, then the heat spreader may not be necessary. Furthermore, if the heat dissipation of the driver and TIA chips is very small, then the heat slug or conductive materials are not even needed. The optical, thermal, and mechanical analyses of this design have been shown in [19,20].

2.5D IC integration

In the past few years, because of the very high-density, high I/Os, and ultra-fine pitch requirements, such as the sliced field programmable gate array (FPGA), even a package substrate with twelve build-up layers (6-2-6) is not enough to support the chips (Figure 14a) and a TSV interposer (Figure 14b) is needed.

For example, the Xilinx/TSMC sliced FBG chip-on-wafer on substrate (CoWoS) [22], where the TSV interposer (also called 2.5D IC integration) has four top RDLs: three Cu damascene layers and one aluminum

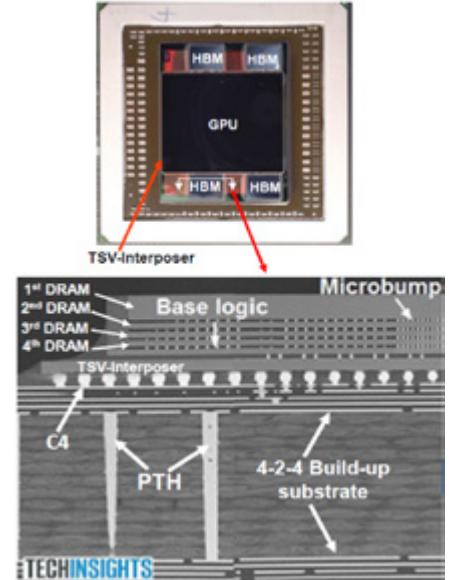


Figure 9: AMD's GPU with Hynix's HBM.

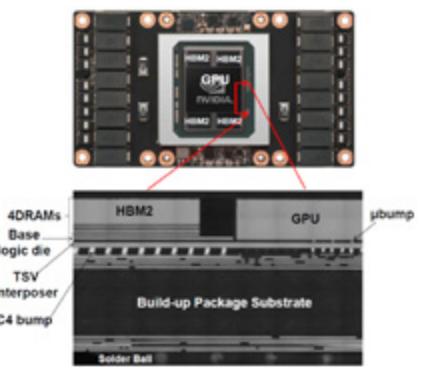


Figure 10: Nvidia's GPU with Samsung's HBM2.

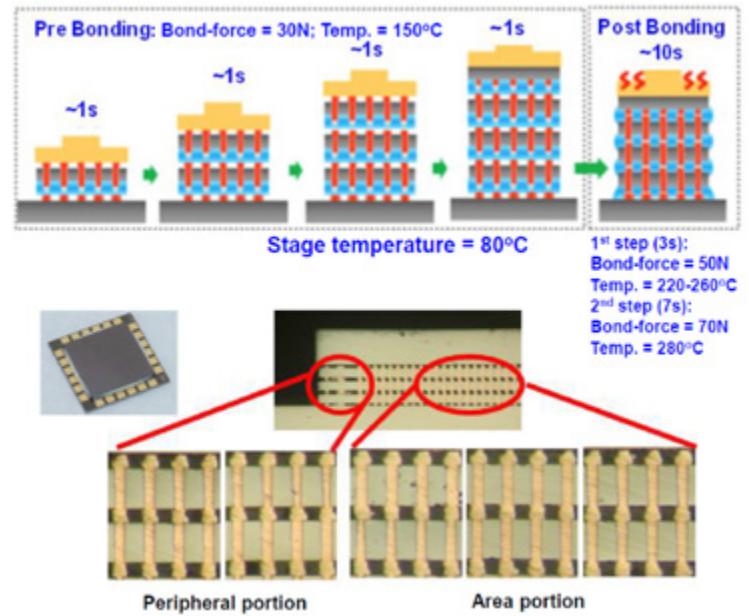


Figure 11: Toray's collective bonding method with TC-NCF for 3D IC integration.

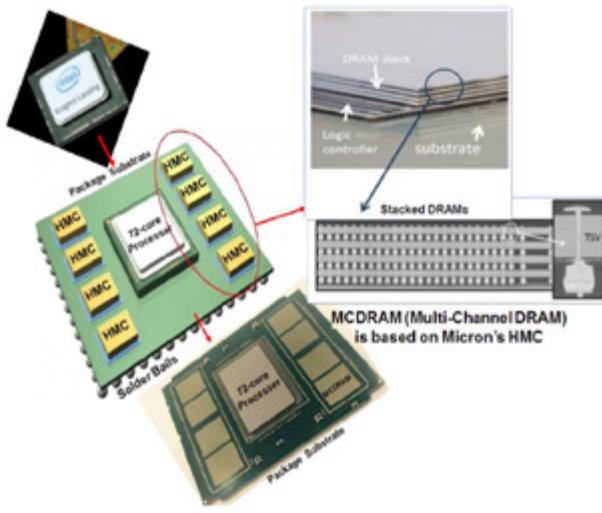


Figure 12: Intel's Knights Landing CPU with Micron's HMC.

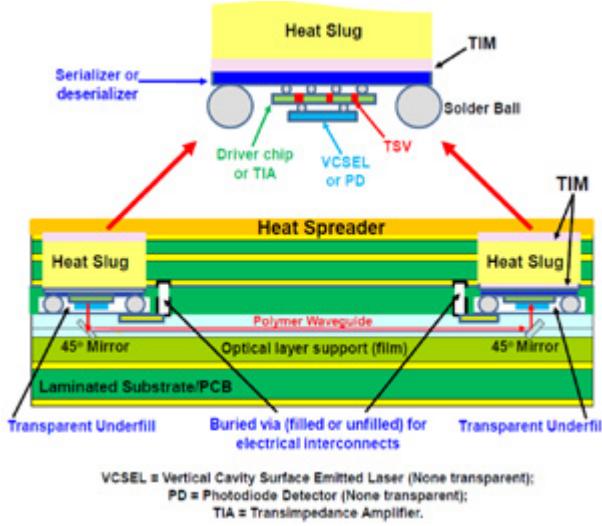


Figure 13: Embedded 3D hybrid integration in PCB/substrate.

layer. The 10,000+ lateral interconnections between the sliced FPGA chips are connected mainly by the 0.4 μm -pitch (minimum) RDLs of the interposer.

TSV-less interposers

So far, TSV-interposers are very expensive [23]. In order to lower the cost, enhance the electrical performance, and reduce the package profile, a TSV-less interposer (Figure 14c) has been developed in the past three years. For example, [24] detailed those proposed by Xilinx/SPIL, Amkor, ASE, Mediatek, Intel, ITRI, Shinko, Cisco/eSilicon, and Samsung. Recently, [25] disclosed that Intel is going to license AMD GPU technology. (Figure 15) shows, conceptually, the Intel/AMD/Hynix CPU/GPU/HBM heterogeneous integration

using Intel's TSV-less interposer: EMIB (embedded multi-die interconnect bridge) technology.

Cu-Cu direct hybrid bonding

Sony is the first to use Cu-Cu direct hybrid bonding (which bonds the metal pads and dielectric layer on both sides of the wafers at the same time) in high-volume manufacturing (HVM). Sony produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results [26] showed that their robust Cu-Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A cross section of the IMX260 BI-CIS is shown in (Figure 16). It can be seen that, unlike in [27] for Sony's ISX014 stacked camera sensor, the TSVs are gone and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu-Cu direct bonding.

The signals are coming from the package substrate with wire bonds to the edges of the processor chip.

The assembly process of Cu-Cu direct hybrid bonding starts off with surface cleaning, metal oxide removal, and activation of SiO₂ or SiN (by wet cleaning and plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a typical cleanroom atmosphere. The first thermal annealing (100–150°C) is designed to strengthen the bond between the SiO₂ or SiN surfaces of the wafers while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO₂ or SiN. Then, apply higher temperature and pressure (300°C, 25kN, 10⁻³Torr,

N₂atm) for 30 minutes to introduce the Cu diffusion at the interface and grain growth across the bond interface. The post-bond annealing is 300°C under N₂atm for 60 minutes. This process leads to the seamless bonds (Figure 16) formed for both Cu and SiO₂ or SiN at the same time.

Summary

Recent advances in, flip-chip technology, fan-in wafer-level packaging, fan-out wafer-level packaging, 3D IC integration, embedded 3D hybrid integration, 2.5D IC integration, TSV-less interposers, and Cu-Cu hybrid bonding have been briefly mentioned in this study. Some important results and recommendations are as follows:

- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps.
- C2 bumped chips are usually assembled by TCB with high force and NCP/NCF, while TCB with low-force on C2 bumped chips with CUF are sometimes used.
- The advantages of TCB are enabling higher pin counts, finer pitch, thinner chips, higher density, and thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- For most applications, in general, the maximum chip size of the conventional WLCSP is no more than 5mm x 5mm. With the help of the protection layer, the size of TSMC's UFI-WLCSP can be as large as 10.3mm x 10.3mm.
- Flip chip and WLCSP are facing stiff competition from FOWLP. Also, with the popularity of SiP, the fan-out wafer or panel-level SiP (WLSiP or PLSiP) will be used intensively.
- TSVs are meant for device-chip/wafer such as stacking DRAMs (3D IC integration).
- TSVs are too expensive for 2.5D IC integration (TSV interposer). In order to lower the cost, enhance the electrical performance, and lower the package substrate profile, more research and development should be done on TSV-less interposers.
- Polymer-based waveguide is the most popular choice for low-cost optical interconnect packages. In order to make the package more compact, lower the package profile, enhance the

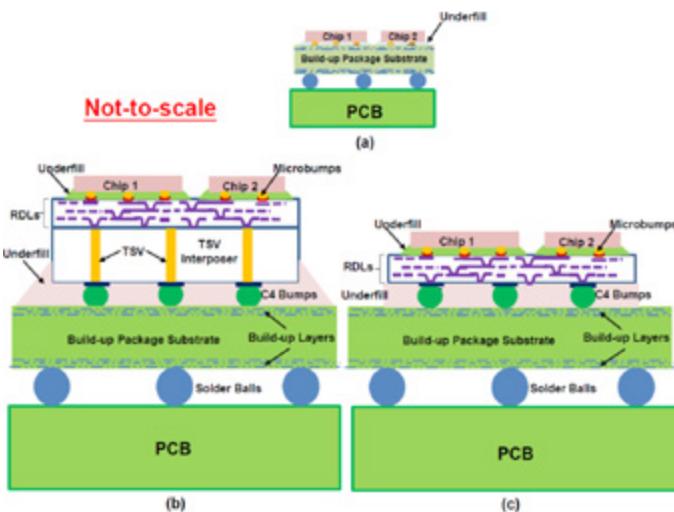


Figure 14: a) Build-up package substrate for flip chips; b) Build-up package substrate with TSV interposer for flip chips; and c) Build-up package substrate with TSV-less interposer for flip chips.

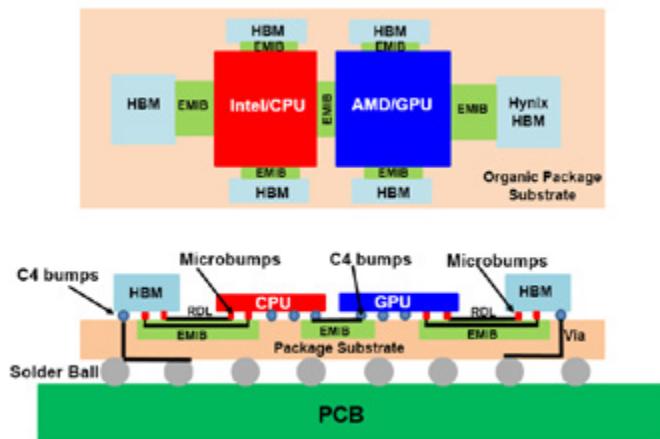


Figure 15: TSV-less interposer: Intel/AMD/Hynix CPU/GPU/HBM heterogeneous integration using Intel's EMIB technology.

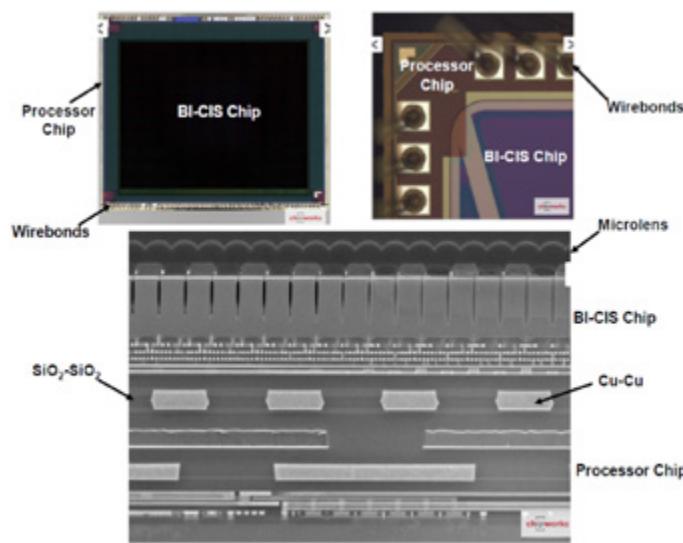
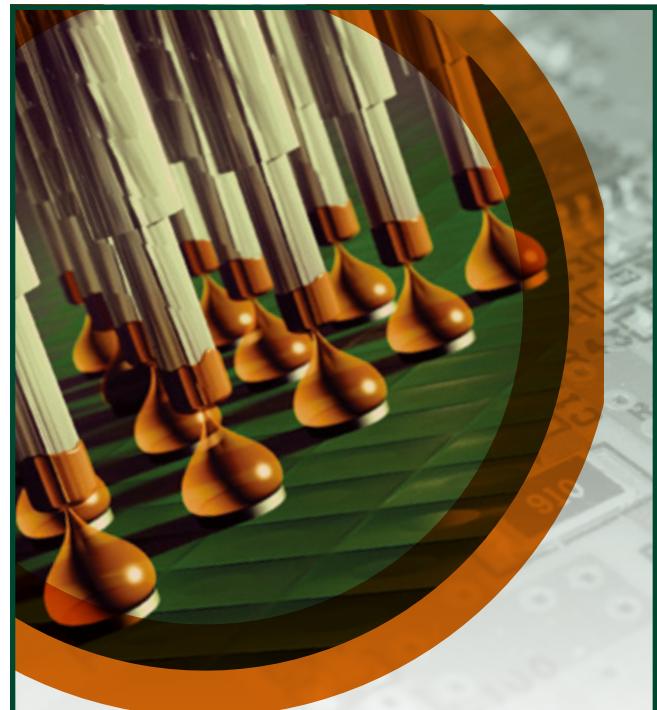


Figure 16: Cross section images of Sony's CIS by Cu-Cu hybrid bonding.



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- performance, and lower the cost, the polymer waveguide, photonics, and electrical ICs are 3D embedded into the PCB or substrate.
- In order to increase the throughput for 3D IC integration, Toray's collective TC-NCF bonding could be a solution.
 - Now that Sony has been in HVM with its BI-CIS with Cu-Cu hybrid bonding, in order to increase the throughput further for 3D IC integration, more research and development should be done on DRAM wafer stacking with Cu-Cu hybrid bonding.
- ### Acknowledgements
- The author would like to thank Chipworks, SYSTEMPlus Consulting, Prismark and Binghamton University for providing the teardown images.
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Biography

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Known-good die testing of complex digital ICs

By Dave Armstrong *[Advantest America, Inc.]*

Large, thin and high-power digital ICs pose a number of challenges to the test process necessary for achieving true known-good die (KGD). As these costly, fragile devices are destined for advanced 2.5D and 3D packaging solutions, advanced test capabilities and solutions must be implemented to reduce scrap assemblies and improve product margins. Producing a true KGD prior to assembly requires bringing final test and potentially system-level test content forward, executing it at the die level. This calls for an advanced thermal control (ATC) system, similar to what is traditionally used at final test, as well as fine-pitch probe alignment capability that exceeds the capability of leading-edge wafer probers. These are the two areas that we aim to address with our die-level handler. To understand the solutions it offers, it's important to look at the packaging landscape that gave rise to its development.

The assembly and packaging process is changing rapidly, with multi-chip assemblies becoming mainstream. When multiple devices are assembled together in one assembly (either 2.5D or 3D), the yield risk is driven by the lowest yielding device. Unfortunately, costly, high-yielding memory stacks may need to be scrapped because of undetected faults on other devices in the assembly.

Further complicating this situation is that high- and/or low-temperature testing is often needed to detect many of the marginal faults in a device. Traditional wafer probers lack a thermal control system responsive to on-die temperature variations. Other techniques (sticky tape, wafer frames, etc.) lack a viable thermal interface to the device under test (DUT), making thermal control very difficult, or more likely impossible.

The Advantest HA1000 die-level test system reduces the risks associated with 2.5D and 3D assembly, providing a way to handle, chuck, probe, and thermally control singulated thin die, die stacks, 2.5D assemblies, and even partially assembled 2.5D devices. The test system supports probing of pads, bumps, pillars, or even through-silicon vias (TSVs) with pitches down to 50 microns or smaller.

Today's KGD test challenges

The earlier KGD tests can be performed in a product test flow, the lower the test and yield costs, as well as the overall cost of goods sold. Today, both memory and logic performance testing and burn-in are being implemented as early as possible in the device test flow. This KGD testing of multi-die, 2.5 and 3D devices at the die level prevents more costly yield loss later at package-level test, as it identifies process problems earlier so they can be corrected to prevent assembling bad die on otherwise good assemblies. Without this step, yield cost will be higher in 3D chip manufacturing and 2.5D and 3D packaging, as well as for systems-in-package (SiPs) and multi-die devices.

Package-level testing usually runs high-performance tests prior to board and system assembly, driving up power and thermal control requirements. Additionally, package-level burn-in can increase this requirement by 1.5x to 2.5x and drives ATC requirements. As chips and systems become more integrated using 3D packaging technologies, this performance and reliability KGD testing will be required much earlier, at the wafer and die levels, before package assembly.

A pre-assembly die-level and/or partial-stack test insertion could provide a way to execute high-

power thermal tests. The HA1000's ATC, together with an extremely low thermal resistance, supports high-power scan tests, elevated voltage screens, dynamic voltage screens and other test techniques to perform die-level sorting prior to stacking. This increases the shipped products' quality level and screens for new reliability defects that may have been introduced during the thinning, bumping and sawing steps. On account of the reduced thermal mass, the ATC can also perform single-pass, multi-temperature testing by cycling temperatures several orders of magnitude faster than traditional wafer probe systems.

The value of adding a test step

While it is possible to use this type of prober to replace wafer probe itself, it's proving more valuable when additional test insertions are made into a traditional manufacturing flow. Adding a pre- or partial-assembly test step requires a financial analysis to confirm its return on investment (ROI). (Figure 1) indicates that the return on the test investment is 10% or more if the product yield is less than or equal to 93.3% (assuming the cost-of-test [COT] is a conservative 10%).

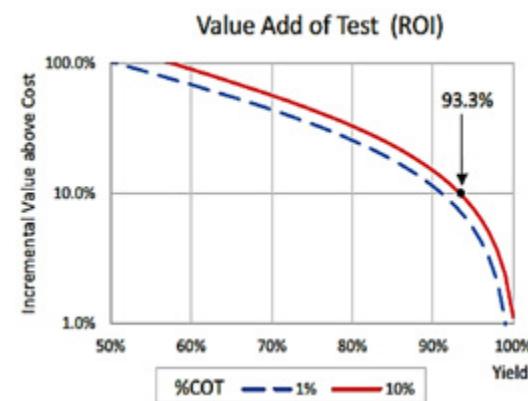


Figure 1: Single chip value of testing (ROI).

When considering the addition of a new test insertion prior to an assembly step involving the cost of additional chips, the same approach can be utilized to determine ROI. As shown in (Figure 2), if the additional chips (or interposer/package) are 3x the cost of the component being added, the ROI for additional testing prior to assembly is 10% or greater if the yield of the last device is less than or equal to 99.6%. Of course, a more realistic back-end yield would provide a significantly higher ROI.

A new approach: singulated die handling and testing

The Advantest HA1000 is a device-level handler for bare die stacks and partially assembled devices. The handler uses vision-based alignment and has the ability to probe a wide range of device sizes and thicknesses, and can support very high-pin-count probing. Depending on the size of the device and temperature setpoint, the test system can heat or cool parts of up to 300 watts. The die-level tester allows devices to be tested after wafer thinning, bumping and dicing. Testing devices in die form detects not only faults from the assembly process (chipping and cracking) but also untested faults, which are typically handled at final test, for a more complete KGD test.

Placing and probing thin die

Probably the most critical step for probing raw thinned devices is having a vision alignment system capable of positioning the probes appropriately on top of the fine-pitched device structures. For large and high-power thin die, an additional challenge is to apply enough probe force to ensure equal low contact resistance and thermal resistance across the entire die while not damaging the thin die.

The chuck must be carefully balanced to provide good surface area for thermal conduction. The HA1000 does this by using a monitored three-zone vacuum, ensuring that all corners of the die make solid thermal contact to the chuck. If suitable vacuum is not achieved in all three regions, an alarm sounds and

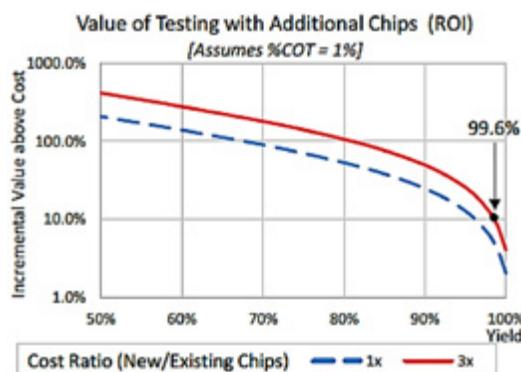


Figure 2: Single chip value of testing with additional chips (ROI).

the test stops. By using micro-channel technology, hot spots or temperature gradients are avoided.

Summary

The new die-level tester incorporates technology that enables final and/or

system-level testing to be conducted earlier in the manufacturing sequence. Performing this extended testing prior to assembly helps ensure that all the parts integrated into a 2.5D or 3D structure are high-yielding, highly reliable devices. Further, this additional test step reduces scrap assemblies and reduces product cost. As a result, the ROI for this additional test step is consistently quite high.

Biography

Dave Armstrong received simultaneous degrees in Electrical, Computer and Environmental Engineering from the U. of Michigan. He is the Director of Business Development at Advantest America, Inc.; email Dave.Armstrong@Advantest.com

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Auto radar probe test technologies for high-volume production

By Tim Cleary, Daniel Bock *[FormFactor]*

With multiple companies now developing single-chip radar solutions for vehicular and other motion-based technologies, autonomous vehicles (AV) are no longer a futuristic pipe dream, but are slowly becoming a reality as advanced driver assist systems (ADAS) pave the way for the eventuality of full AVs. In certain industrial sectors like mining and farming, AVs are already in use, albeit in restricted fashion and limited to private roads. By 2040, we can expect on-highway trucks to be the first to feature full AV technology on public roads. Automakers are expected to define their AV strategies in the next two to three years, but it won't likely be until the 2040s to 2050 that AVs will become the primary means of transport [1].

One of the biggest drivers for today's ADAS is the role they could play in reducing traffic fatalities. Numbers for 2013 show that fatalities dropped by 3.1% in 2013 models, which have more recent standard safety features—such as stability control and multiple airbags—than previous model years [2]. Furthermore, according to a recent study by The Boston Consulting Group, commissioned by the Motor & Equipment Manufacturers Association, currently available ADAS technologies could prevent some 9,900 fatalities and \$251 billion in socioeconomic losses in the U.S. each year [3].

Beyond passive safety systems, ADAS include adaptive cruise control and collision warning systems with automatic steering and braking intervention that rely on radar millimeter wave technology. In a collision warning system, a 77GHz transmitter emits signals reflected from objects ahead, at the side and to the rear of the vehicle, and are captured by multiple receivers integrated throughout the vehicle. The radar system can detect and track objects, triggering a warning to the driver of an imminent collision, and initiating electronic stability control intervention automatically (**Figure 1**) [4].

Historically, millimeter-wave testing of wafers was relegated to labs and low-

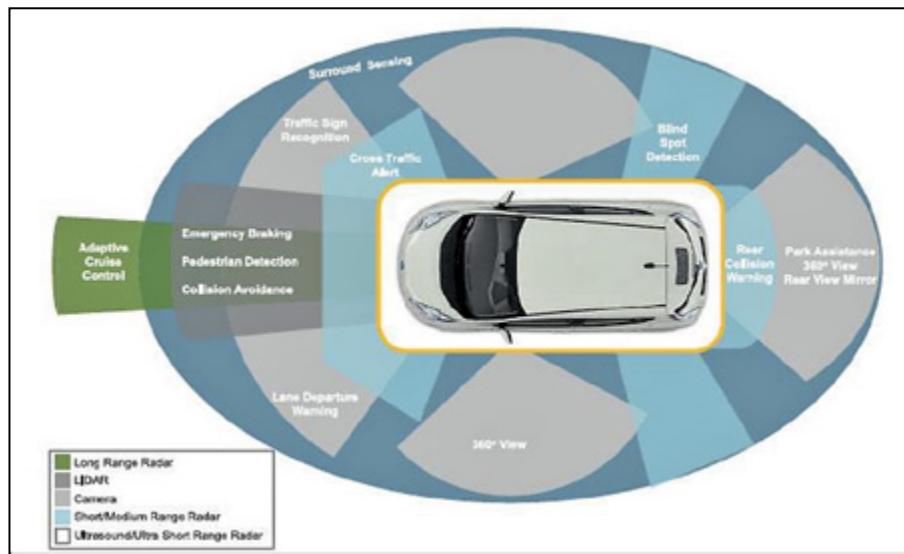


Figure 1: Vehicle safety technology sensor types include LIDAR for emergency braking, pedestrian detection and collision avoidance; and image sensors for camera technologies that provide 360° view, traffic sign recognition and traffic signal warning, park assist and rear view mirror.

volume production for defense, aerospace and other somewhat-exotic applications. However, with the coming of auto radar and high-speed data, this kind of testing is moving into high volume for the first time (**Figure 2**). This article provides what manufacturers—and in particular, what test engineers—need to know about changes in testing for millimeter-wave wafers used in auto radar and other E-band applications. It reviews some of the changes that will be required to support wafer testing in the 40GHz-81GHz range in high-volume manufacturing (HVM), and will talk about the advancements in probe card technology that enable multi-site production-level testing for auto radar chips.

For these technologies to be successful in reducing crashes and saving lives, it's critical that they function over the lifetime of the vehicle which can be upwards of 20 years. The radar and sensors are located on both the interior cabin and exterior of the vehicle, and can be subject to harsh

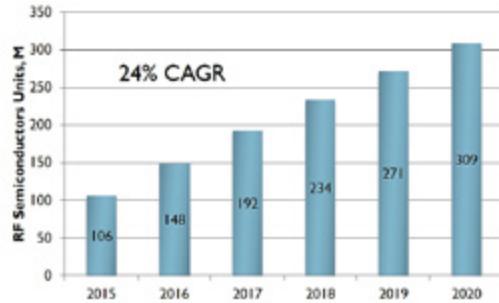


Figure 2: Estimated auto radar RF IC units. Image courtesy of Feldman Engineering.

conditions. Therefore, the government has issued a specific set of rules targeting auto safety, which in turn have impacted production testing requirements.

The Automotive Electronics Council (AEC) established AEC-Q-100, "Failure Mechanism Based Stress Test Qualifications for Integrated Circuits" to provide standardized test methodologies for reliable, high-quality electronic components. It includes testing to be performed at both the integrated circuit (IC) supplier and the packaging house. AEC-Q-100 grades are based on the ambient operating temperature

range, and range from 0-3, with Grade 0 at -40°C to 150°C, and Grade 3 at -40°C to 85°C. The ambient temperature for sensors and ICs used in ADAS varies depending on where in the automobile the sensor is mounted. They must meet at least a Grade 1, -40°C to 125°C, to meet the requirement [5].

While low-frequency testing technology is sufficient for millimeter-wave radar used in defense, aero and exotic applications, auto radar technology in high-volume production calls for a more enhanced way to test to accommodate the volumes of sensors and high-speed data. Test protocols need to handle multi-site calibration and testing with minimum crosstalk, and they must be accurate at frequencies of up to 81GHz. Essentially, testing needs to be designed specifically for multi-site production tests. Testing just became more costly for the manufacturer.

Requirements for production-level testing

Now that we've addressed the motivation and reasons for the industry's demand for higher-level testing, we need to look at what's required to ramp millimeter-wave radar test for automotive applications into volume production. The three pillars to achieve this include: multi-site testing; multi-site calibration; and automated probe card change-out.

Multi-site testing

Why is multi-site testing necessary? Once the volume of any chip has reached a certain threshold, there is significant cost pressure to move to testing multiple die in parallel using a multiple device under test (multi-DUT) approach. This approach requires investment in both the tester and the probe card. A half-step in this direction is to put in a switching matrix that keeps the tester resources to a minimum and eliminates the issue of die-to-die crosstalk. It takes longer than true multi-DUT testing, but it does reduce the step time and extend the life of the probe head. Full-on multi-DUT testing first requires a tester with sufficient resources. Several companies now offer this capability.

As production-level testing calls for multiple sites with 10+ RF channels, electrical isolation has become a challenge that needs to be considered, particularly when the chip is being tested at the wafer level. For example, if a die is designed with RF test channels on all four sides, it may be difficult to isolate two DUTs. In that case, it may be necessary to test the die one at a time, or two alternate die must be tested, skipping the one between them. Neither is desirable as it increases test time and test program complexity.

While the increased number of test channels increases capital cost, it's important to remember that the cost is spread over the lifetime of the test cell, and that this greater number allows for higher parallelism, assuming isolation can be addressed. This reduces total test time. The trick for test houses will be to keep all of this test capacity utilized as much as possible.

Multi-site calibration

The second pillar for production-level test is multi-site calibration. Measurement errors that might be considered insignificant at lower frequencies can become important at millimeter wavelengths. Using a simultaneous multi-site calibration during multi-DUT testing provides the highest electrical accuracy because all the DUT RF channels are in a known and controlled state.

RF calibration is used to move the measurement reference plane from the tester to the device in order to obtain the best device measurement and to remove the effects of the test fixture. This is done by measuring RF on a calibration substrate, like that shown in

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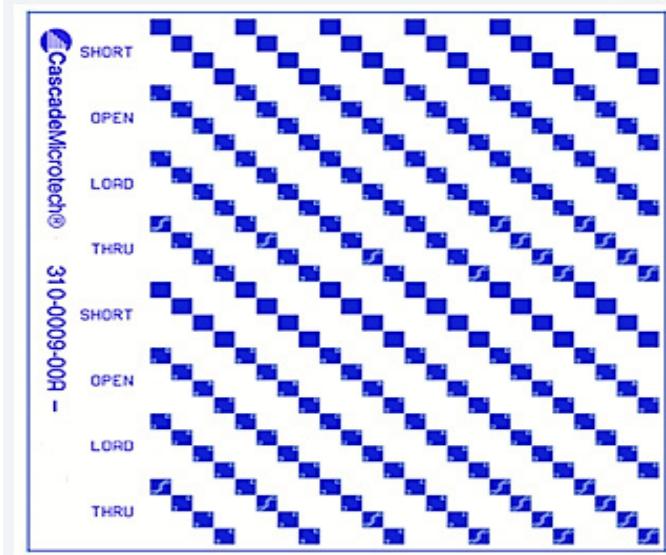


Figure 3: Example of a custom multi-DUT calibration substrate for SOLT.

| Calibration Method | Absolute Accuracy | Probe Card Support |
|--------------------|-------------------|---|
| SOLT | Fair | Fair (does not usually have straight thrus) |
| TRL | Best | Poor (unable to support variable-length thrus) |
| LRRM/LRRM | Good | Fair (does not usually have straight thrus) |
| SOLR | Good | Best (works best with bends in thrus) |
| SOL | Fair | Fair (works well with KGD tests) |
| SO | Low | Fair to Poor (depending upon RL) (easy to use) (does not require precise alignment) |

Table 1: Comparison of different RF calibration methods.

(Figure 3). The most accurate calibration substrate is also to make it mirror the multi-site layout of your probe card in order to properly measure the effects of the test fixture.

For RF calibration, there are a number of options that use some combination of RF standards. These usually include some combination of short, open, load and thru (**Table 1**). For lower frequencies, short-open-load-thru (SOLT) is a standard calibration technique. For highest accuracy, SOLT requires good definitions of all of the standards. It is possible to use short-open-load-reciprocal (SOLR) as an alternative. In contrast to SOLT, SOLR does not need a precise definition of the thru. This is useful when there are bends in the thru that make it harder to have a strict definition of the thru length.

As the frequencies get higher, an alternative model, multi-line reflect thru (mTRL) is used. mTRL was developed by NIST, and is considered to be the gold standard in RF calibration. However, it is difficult to use with probe cards because of

the fixed distance separation between the probe tips.

Cascade Microtech (a Form Factor company) developed line-reflect-reflect-match (LRRM), an algorithm that features more robust loss models, which compares favorably to mTRL. LRRM is more probe-card-compatible, because it only requires one thru (line) to be defined for it to calibrate. In some test layouts, it can still be difficult to define a good thru for calibration. In those cases, the 1-port SOL calibration method can be used. Although less accurate because of the lack of the thru, for production testing and known good die methods, it is (more than) adequate to use to determine if your device is good.

Automated probe card handling

The third pillar of production-level testing is automated probe card handling. Changing out the probe card from an RF test cell can be a labor-intensive task requiring a technician to unscrew all the cables connecting the probe card to the tester when a screw-on connector is used. This takes an hour or more and creates the risk of bending the cables in a way that would alter the RF performance or possibly damage the test setup. Implementing a probe station outfitted with blind mate connection capabilities automates the process by moving the stage in or out in the z-direction, mechanically aligning pins so that cables snap together “blindly” and are tightly held in place by pressure. Blind mating allows the RF connection between the probe card and the tester to take place without human intervention. This results in better repeatability and lowers overhead time for setup.

Blind mate connectors can be used for either coax or waveguide connectors (**Figure 4**). Coax types of connectors have a smaller connector that is easier to route, and can be better for design and setup as well as broadband performance. In contrast, the waveguide is narrow band with a larger connector. Because testers usually have waveguide outputs, staying in waveguide results in lower loss. However, some multi-DUT applications have 24 or more RF ports, and in those cases, coax is preferred, because it fits in tighter spaces.

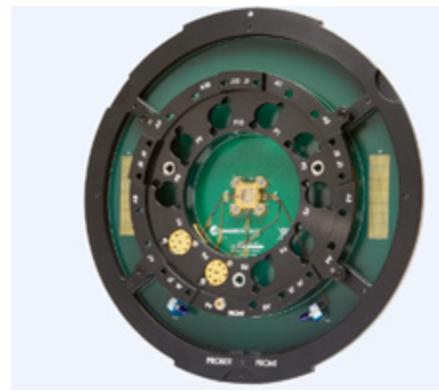


Figure 4: An example of a probe card with blind-mate connections for fast change out in the prober in a production environment. Photo courtesy of Cascade Microtech, a FormFactor company.

Cost-of-ownership for multi-site testing

As production volumes increase in this high-frequency market, companies are looking more closely at what the right choice is for them. With new consumer products at 80GHz+, they are starting to reach new conclusions.

Determining the cost-of-ownership (CoO) for a production-level millimeter-wave radar test cell can be broken down into three parts: the probe station, the tester, and the probe card. While the probe station is a fixed capital cost that isn't based on how many parallel die are being tested, it doesn't make sense to own more than needed to reach peak capacity. This is determined by how many dies are being tested and the required throughput during a product ramp. The tester is configured with expensive racks of electronics for high-speed signal measurements. It is critical to use those resources as optimally as possible if you are investing in the ability to test a large number of RF lines. The third expense is the probe card, which is considered a consumable product with a fixed lifetime based on some number of touchdowns. It makes no difference to the probe card lifetime how

many die are tested for any one touchdown.

For an x4 solution, the probe station becomes four times more efficient, the tester has a more expensive one-time cost, and the probe card will touch four times the number of die before it wears out. Alternatively, it's very costly to maintain extra tester resources and idle probe stations if the need for a particular design is small. Therefore, a variation on this model is to have a probe card set up for x4, but to only keep enough tester resources for one with a switch matrix so you can test each die one at a time. This helps the probe card touchdown life and keeps tester resources low, but it burdens the probe station with lower throughput due to longer test times.

Summary

Utilizing a multi-DUT test approach to lower costs is not a new concept. The memory market has long been masterful at getting the biggest bang out of every test touchdown, but there are specific advances required to apply that model to testing at millimeter-wave frequencies. Die isolation while under test becomes more critical, calibration strategies need to become more sensitive, and automating the test cell amid those heightened sensitivities requires advances in connecting technologies that adapt to the more rigorous electrical environment.

The promise of a safer and potentially much more efficient transportation future is alluring to say the least. It is timely that the test industry has anticipated these needs, and that leading-edge suppliers are now offering solutions that enable a cost-effective path forward. All of the requirements needed to enable cost-effective production volume testing reviewed here are now available from leading-edge companies that have worked within these frequency domains for years anticipating this opportunity to build a true production solution.

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Koh Young Singapore relocates office to Pasir Panjang, Singapore



Koh Young Technology has announced the relocation of its Koh Young Singapore office to Pasir Panjang, Singapore (Figure 1). The new office will serve as a sales, training, service and application support facility for Koh Young's 3D Solder Paste Inspection (SPI), Automated Optical Inspection (AOI) systems, and Smart Factory solutions.

"We have seen our growth accelerate in recent years in Southeast Asia since we opened our Singapore office in KA Place, in December 2013," said Peter (Jong Hoon) Shin, General Manager of Koh Young Singapore. "Our new office space is 20% larger than our previous office, and allows us to continue to enhance our ability to serve our customers at the highest levels." The company said that the new office provides more space for training, machine demonstrations and application support. Koh Young Singapore is now located at 108 Pasir Panjang Road, Golden Agri Plaza #03-13, Singapore 118535, Tel. +65 6634 2814.



Figure 1: The Koh Young Singapore office at Pasir Panjang, Singapore.

Yole addresses materials cost for power packaging



Yole Développement (Yole) released results of its evaluation of the power packaging materials market. According to Yole, power packaging materials represent the main part of power module cost. Its analysis shows that in 2016, almost 40% of the total cost is due to the cost of materials for packaging. "To understand the evolution of the power packaging market, it is now essential to look into details in the selection materials and design and evaluate each innovation," noted Mattin Grao Txapartegi, Technology & Market Analyst, Power Electronics at Yole Développement (Yole), part of Yole Group of Companies.

According to the analysis, the power module materials market will grow at 9.5% per year between 2016 and 2021, reaching almost US\$1.8 billion in 2021 (Figure 2).

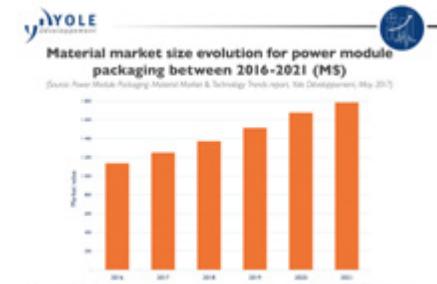


Figure 2: Material market size evolution for power module packaging between 2016-2021 (M\$).

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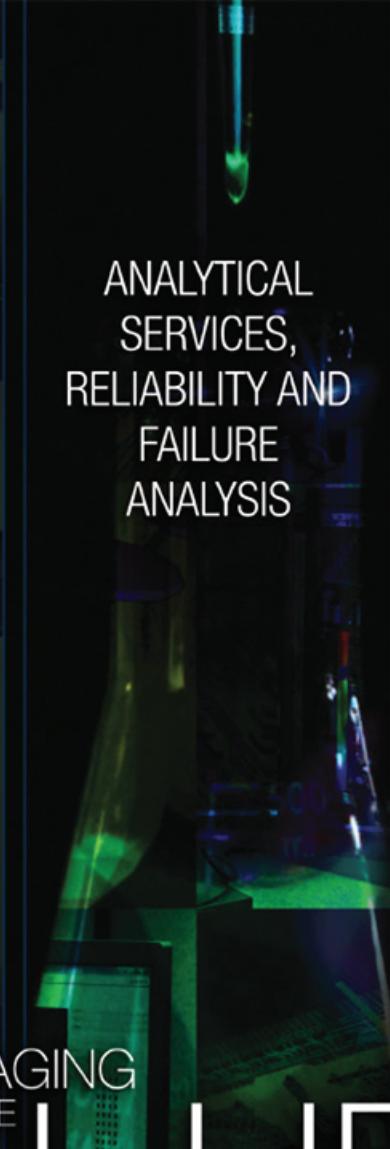
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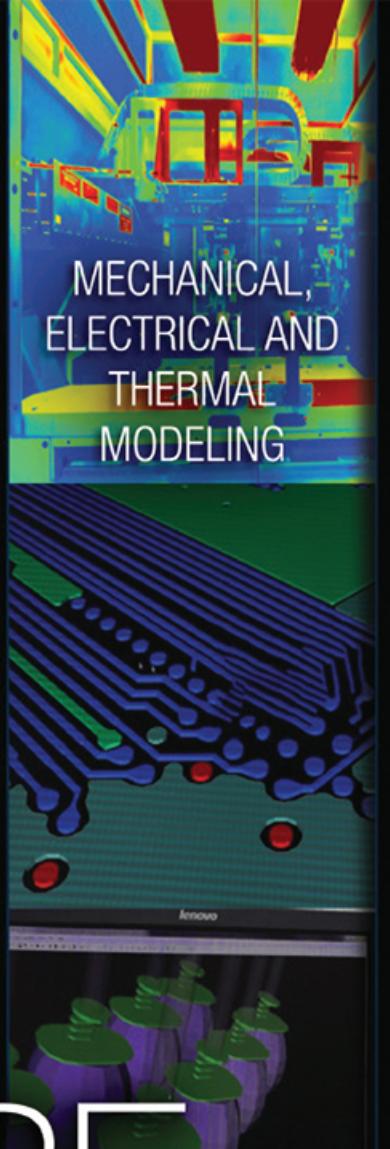
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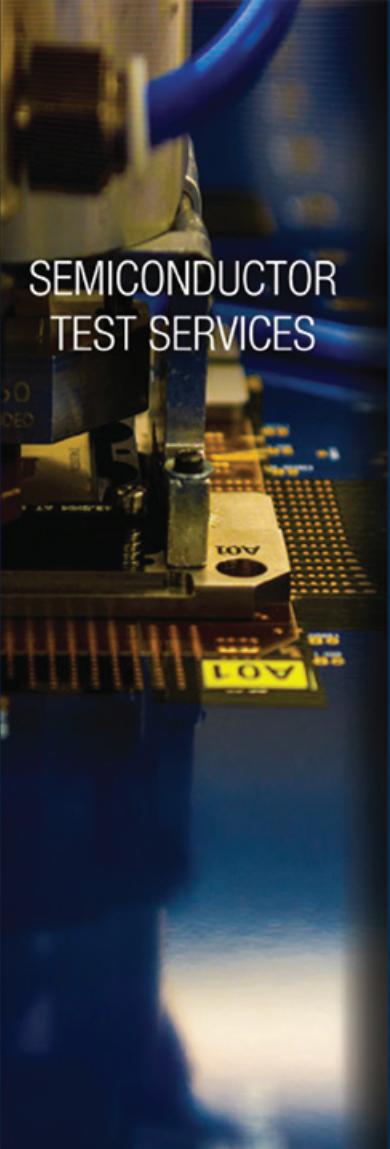
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