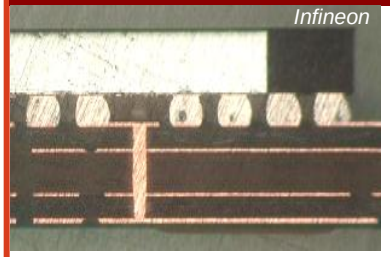
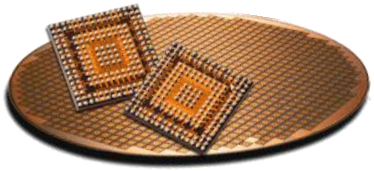
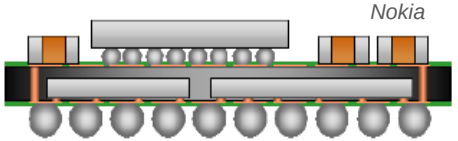
SAMPLE presentation

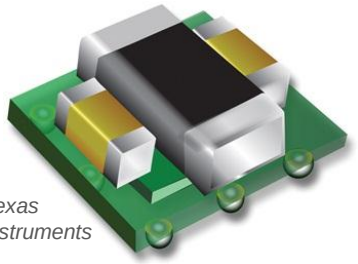
FOWLP & Embedded die Packages

Embedded wafer-level-package activity is expected to pick-up by 2015 above $200M overall driven by major wireless chip players worldwide


Infineon


STATs ChipPAC

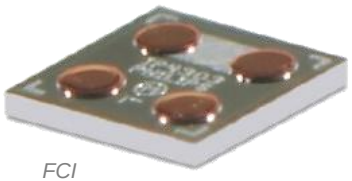

Nokia


Texas Instruments

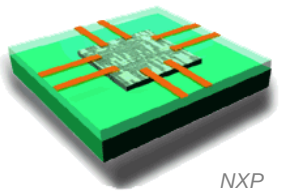

AT&S

YOLE Développement

Table of Content *(1/2)*



FCI



NXP

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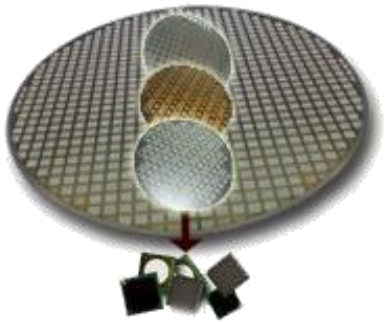
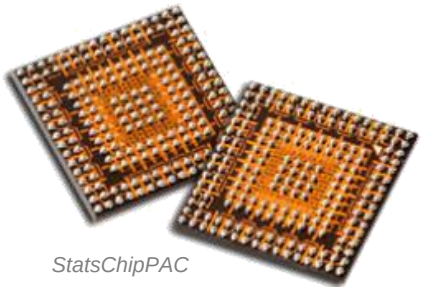




StatsChipPAC

Scope of the Report

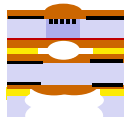
PANEL / Wafer-Scale-Packaging Platforms

Wafer-Level
Interface / Encapsulation

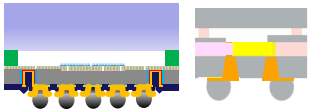
Wafer-Level
Electrical Redistribution

Flip-chip & Wafer-Level
Stacking / Integration

LED & Sensors
WLOptics

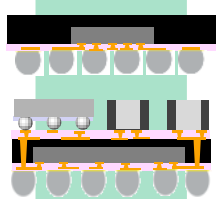


3D WLP
For MEMS & sensors
(also called 3D SiP sometimes)

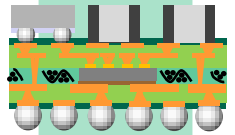


WL CSP
'Fan-in'

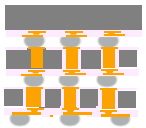
FOWLP
'Fan-out'



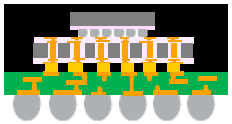
Embedded die
in PCB / laminate



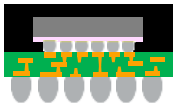
3D IC
& TSV



Glass / Silicon
2.5D
interposers



Flip-chip
wafer bumping
on BGA



→ **FOCUS of this report update**

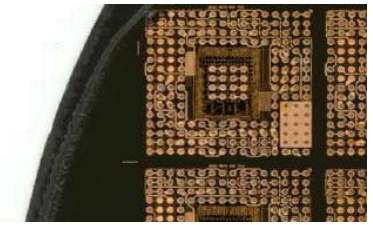
- **Wafer-level-packaging encompass multiple different technology platform flavors but leverage similar type of process manufacturing know-how**

Definitions

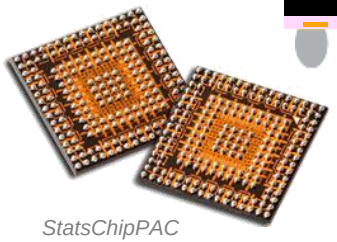
- **Embedded Packages refers to different concepts, IP, manufacturing infrastructures and related technologies. However, it is still possible to distinguish 2 main categories of embedded packages:**

Embedded Wafer-Level-Packages

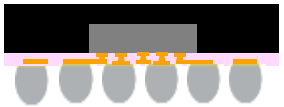
→ based on a **Molded Wafer** infrastructure



NANIUM



StatsChipPAC



Fan-Out WLP

FOWLP

WLFO

eWLB

Reconfigured wafers

FOWLP

"epoxy" molded wafers

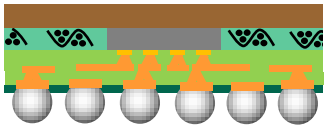
Chip first

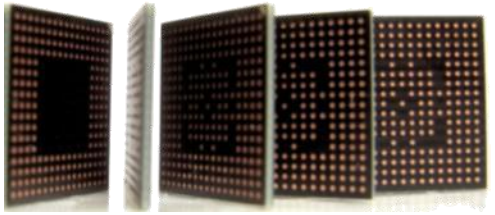
RCP

Wafer-Level Ball Grid Array

Fan-Out WLCSP

→ based on a **PCB / PWB** substrate infrastructure





Imbera

Embedded die

Chip embedding

Chip-in-polymer

UTCP

IMB

Embedded Active Module

Chip-in-foil

Embedded component

EAC – Embedded Active Component

iQFN

EOMIN

Hidden die

Embedded chip

iBGA

EMBIDS / EDC

ECP – Embedded Component Packaging

Objectives of the Report

- **This is the second report update on Embedded Wafer-Level-Packaging technologies and markets from Yole Developpement**

- **The objectives of this first report are the following:**
  - **Analyze both FOWLP and Embedded die package technologies**
  - **Key market drivers, benefits and challenges by application**
  - **Market trends & figures with detailed breakdown by application**
  - **Technology roadmap and description of the complete manufacturing tool-box for embedded wafer-level-packaging:**
    - **Key equipment: for 200mm / 300mm / Panel manufacturing**
    - **Specific material selection coming from both FE / BE / PCB / LCD areas**
  - **Analysis of several embedded package target prices for a few key applications**
  - **Supply chain perspectives, key players and emerging infrastructure for embedded wafer-level-packaging**
    - **Analysis of the rationales behind the different possibilities of FOWLP and embedded die package implementation (chip first / chip last, single die / multi-die / SiP / PoP module, etc …)**

Who should be Interested in this Report?

- **Integrated semiconductor Device Manufacturers and fabless IC companies**
  - Benchmark the industrialization status of embedded packaging technologies within the industry
  - Identify possible partnerships or second source packaging subcontractors for your forthcoming developments
- **Assembly and Test Service companies**
  - Get the list of the main companies interested in Embedded WLP
  - Screen possible new applications and technologies to support diversification strategy with embedded packaging platform
- **Equipment and Material suppliers**
  - Understand the differentiated value of your products and technologies in this emerging but fast growing market
  - Identify new business opportunities and prospects
- **Electronic module makers and Original Equipment Makers**
  - Evaluate the availability and benefits of using embedded package components in your end system
  - Monitor different embedded WLP suppliers to adjust your sourcing strategy
- **PCB and IC substrate manufacturers**
  - Monitor the evolution of IC packaging, assembly and test, especially linked to emerging chip embedding
  - PCB-based technologies, FOWLP, IPD and 3D interposers

Companies Cited in this Report

3D-Plus, ADL Engineering, ADTEC Engineering, Amkor, ams, Analog Devices, AT&S, Aptos, Asahi Glass, ASE, ASM, Atotech, Broadcom, Bosch, Camtek, Casio Micronics, CIRETEC, CMK, Compass Technology, CSR, Datacon, Daeduck, Denso, Dialog Semiconductor, Dow Corning, DuPont Electronics, Dyconex, Epic, Epcos TDK, EVGroup, Fico Molding, Flip-chip International, Fraunhofer-IZM, Freescale, Fujitsu, HD Microsystems, HEICO, SK Hynix, Ibiden, Imbera, IME, IMEC, Infineon, Invensas, IPDiA, ITRI, King Dragon International, KYEC, Leti, Lintec, LG Electronic, Micron, MicroChem, Mitsui, Murata, Nagase ChemteX, NANIUM, NEC Electronics, Nitto Denko, Nokia, NSC, NXP, OptoPac Oki Electric, ORC, Panasonic, PPT, Qualcomm, Renesas, Rohm & Hass, Rudolph technologies, Samsung, SEMCO, Shinko Electric, SPIL, STATS ChipPAC, ST-Ericsson, STMicroelectronics, SPTS, SMIC, Shin-Etsu, SÜSS Microtec, Taiyo Yuden, TDK, Tessera, Texas Instruments, tok, Tong Hsing, Toray chemical, Toray Engineering, Toshiba, Towa, Triquint, UMTC, Unimicron, Unovis, UTAC, Vertical Circuits, Wolfson Microelectronics, Yamada and more…

About the authors of this report

Jerome Baron

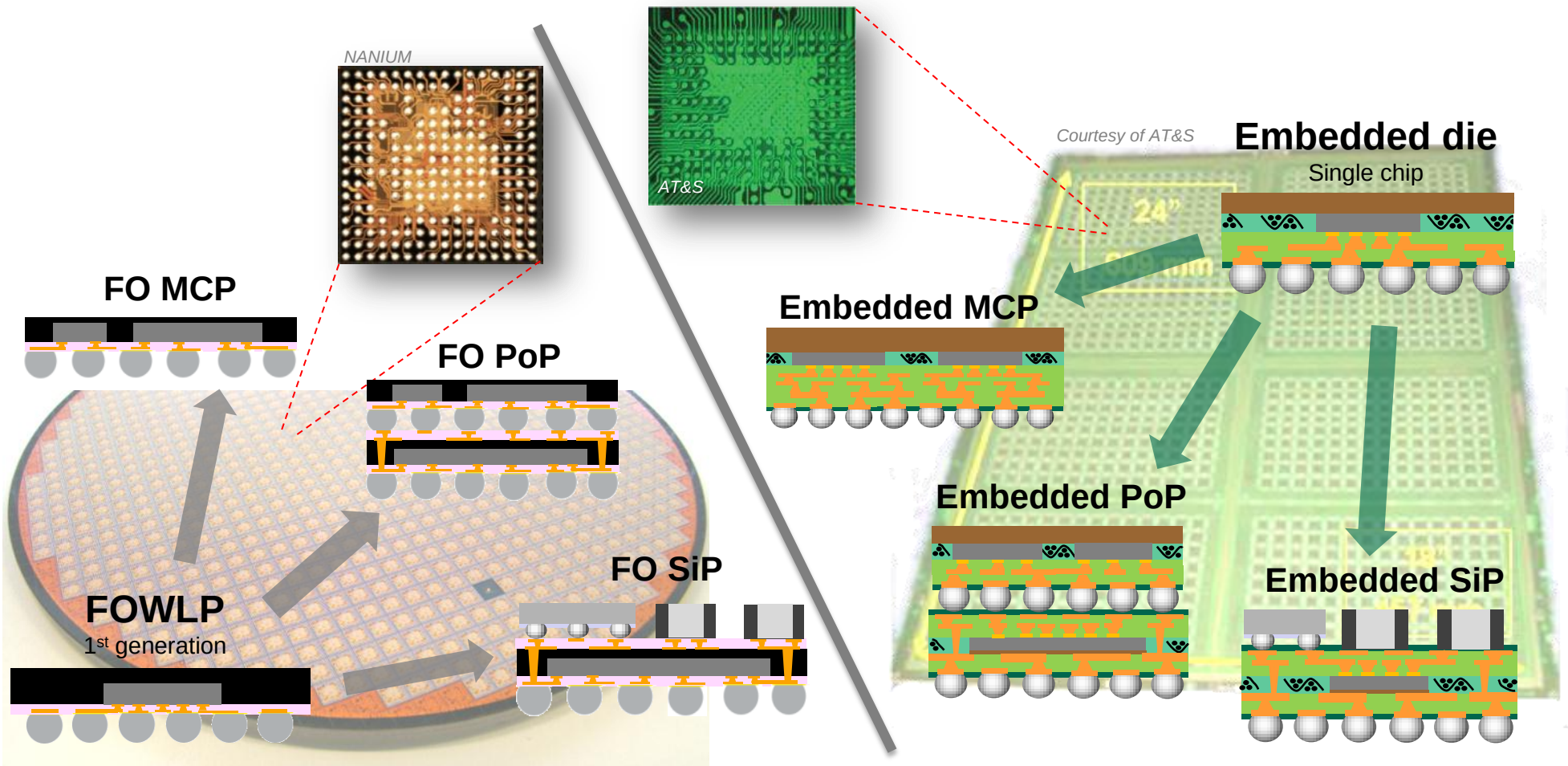
– Jerome is the business unit manager of the semiconductor packaging market research at Yole Developpement. He has been following the 3D packaging market evolution since its early beginnings at the device, equipment and material levels. He was granted a Master of Science degree from INSA-Lyon in France as well as a Master of Research from INL – Lyon Institute of Nanotechnology
Contact: *baron@yole.fr*

Lionel Cadix

– Lionel joined Yole after the completion of several projects linked to the characterization and modeling of high density TSV and 3DIC chip stacking in collaboration with CEA-Leti and STMicroelectronics during his PhD. He is author of several publications and 8 patents in the field of 3D Integration
Contact: *cadix@yole.fr*

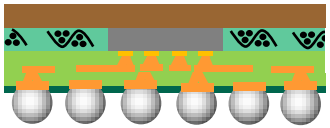
Concepts of FOWLP / Embedded di in package

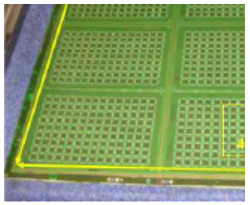
- **Two types of Embedded Wafer-level-packages are emerging**
  - **FOWLP is based on a reconfigured molded wafer infrastructure**
  - **Embedded die in package is based on a PCB type of Panel infrastructure**



Chip Embedding / Fan-Out WLP
Geometry definitions

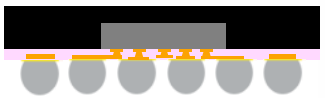
Chip embedding

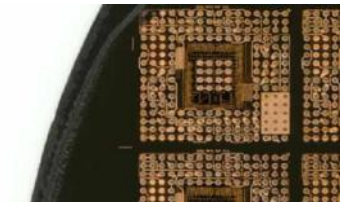




Courtesy of AT&S

FOWLP





Courtesy of NANIUM

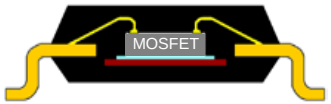
Line Spacing / Width (µm)

1st generation *(up to 2012)*	2nd generation *(2012-2014)*	3rd generation *(2014-2020)*
40/40	25/25	15/15
20/20	10/10	5/5

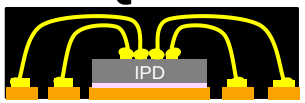
- **Shift in manufacturing technologies is expected**
  - **Geometries of the two emerging packaging technologies will shrink with time as to allow for higher routing density, highly integrated passive inductors and baluns, and integration of ICs with no prior RDL on the device wafer**
  - **There is a move (at least for fan-out WLP) from currently used mask aligners to front-end steppers to support this reduction of the feature sizes**

FOWLP / Embedded Die Packaging Roadmap

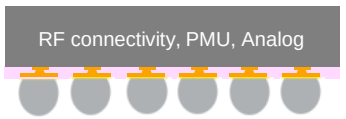
SOT / TSOP



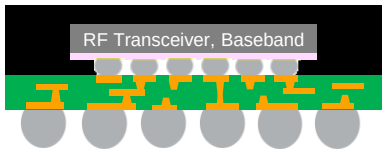
QFN



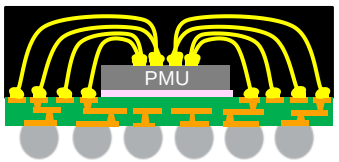
WL CSP



FC BGA

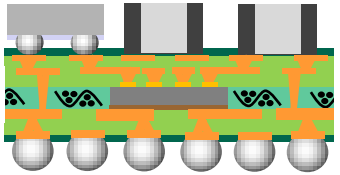


WB BGA



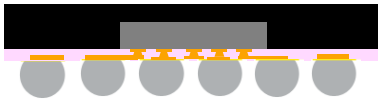
Embedded die

Micro-SiP module

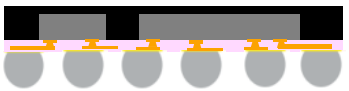


→ RFID, thin-film IPD, MOSFET, IGBT, DC-DC converters, IC drivers, MEMS & Sensors , RFEM…

FOWLP

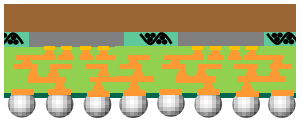


FO MCP



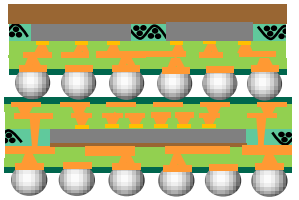
→ Digital Baseband SOC
→ RF Transceiver
→ NFC / Connectivity SOC
→ ASIC / DSP / FPGA
→ Specific Analog IC & Sensors

Embedded MCP



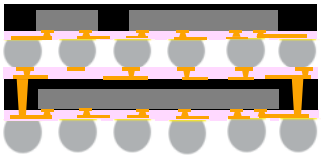
→ Power modules, IPD protection network modules Digital / Analog partitioning …

Embedded PoP



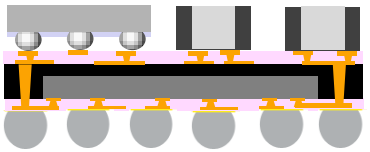
→ Digital + memory modules, Analog + Digital + memory modules, Sensor modules, Radio FEM module …

FO PoP



→ Digital + memory modules, Analog + Digital + memory modules, Sensor modules …

FO SiP



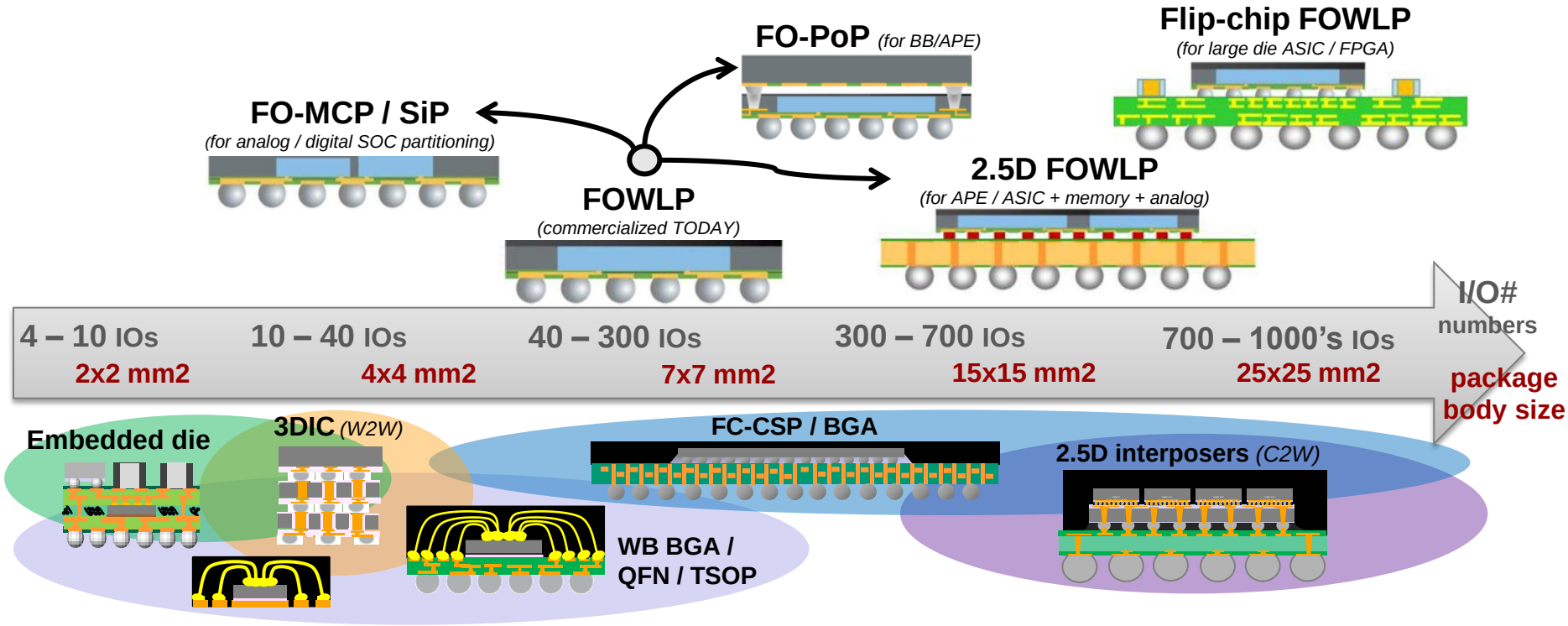
→ RF connectivity modules, Audio modules, Sensor modules, Radio modules …

MATURE tech
(2000 - 2010)

EMERGING tech
(2008 - 2014)

FUTURE tech
(> 2014 - 2018)

Narrow commercialization window
of present eWLB / FOWLP 1st generation technology

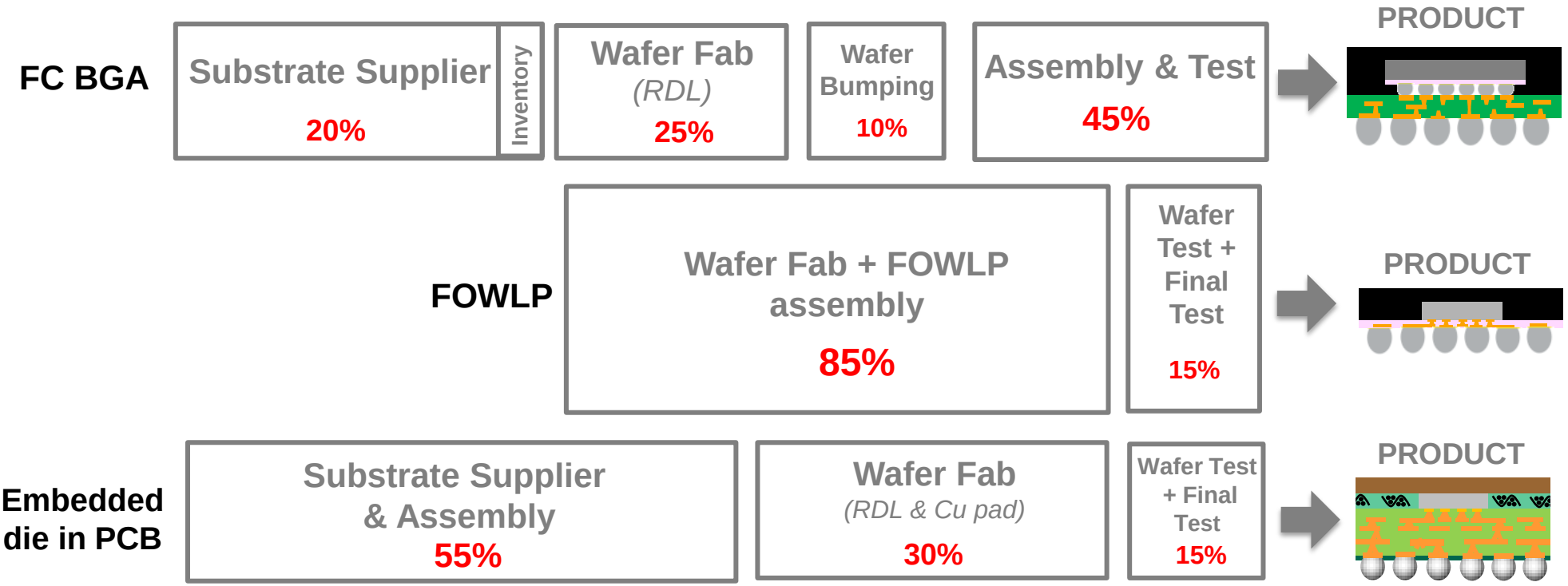


- **As of today (2012), the commercialization eWLB / FOWLP 1st generation technology is quite restricted to a quite narrow application window from 40-300 IO pin-counts, 4x4 to 7x7mm2 package body size**
  - **Package / devices below 4x4mm2 and 40 IOs: FOWLP will struggle to compete with Wire-bonded BGA/leadframe, Embedded die package and 3DIC wafer-to-wafer assembly platform → An extra niche to be found by developing FO-MCP / SiP platform here**
  - **Package / devices of more than 15x15mm²: flip-chip and 2.5D interposer are the best packaging solutions today → new flip-chip and 2.5D version of FOWLP technology will be adapted to compete on cost**
  - **Between 4x4mm2 and 15x15mm²: the solutions are not yet decided and the battle is hard between most every packaging technique → and this is where the biggest part of the IC packaging business is in volume!**

Packaging Value Chain Comparison*

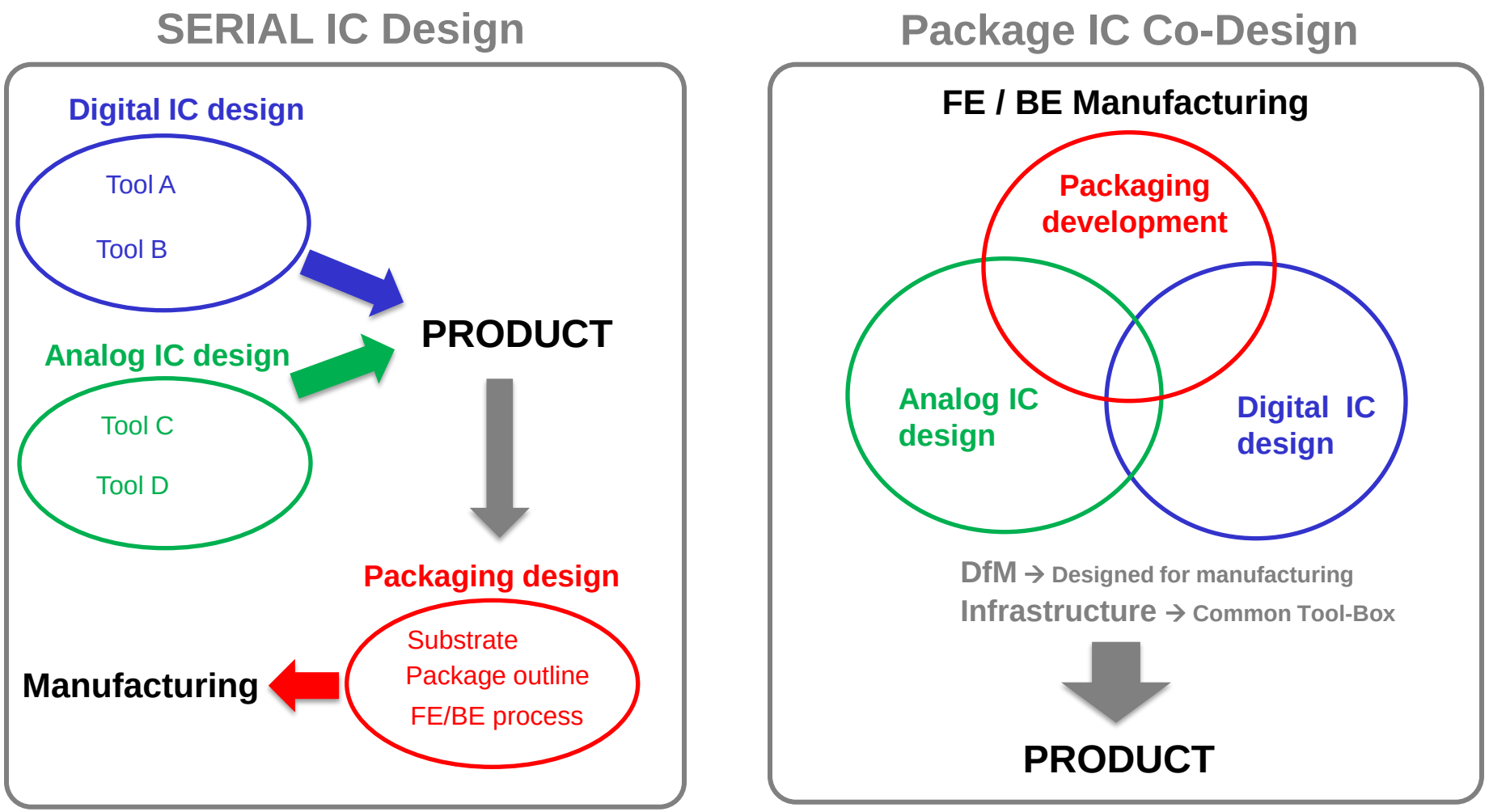
Comparison ratio of the packaging, assembly & test value

** Comparison scenario for the case of 64 I/Os, 0.4mm pitch IC*



- **New shift in the packaging, assembly & test value chains**
  - **FOWLP implies a simplification and consolidation of the packaging, assembly & test in a "Mid-end" type of infrastructure**
  - **Embedded die packaging opens the door to substrate suppliers to realize themselves the whole packaging, assembly and test on a Panel "PCB based" infrastructure**

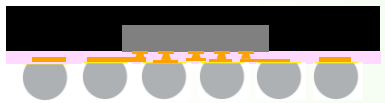
Package IC Co-Design is Necessary Before Embedded WLP

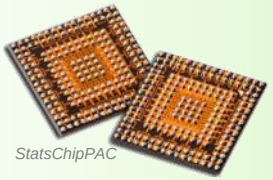


- **Package IC co-design drives to silicon die and process optimization, for e.g.**
  - **to avoid RDL at the IC wafer level before the embedded WLP process**
  - **RF chip package co-design is also necessary to integrate to take package parasitics into accounts**

Embedded Wafer-Level-Packages
Status of commercialization

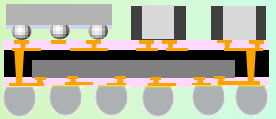
FOWLP
1st generation / single die





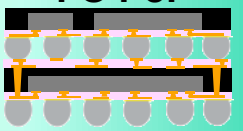
2nd generation FOWLP

FO SiP



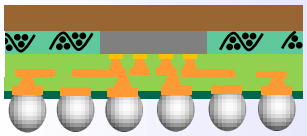
FO MCP

FO PoP



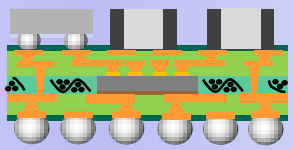
X Broadcom – ASIC
X Altera – FPGA
X STEricsson – RF Transceivers
X IFX / Intel Mobile – Wireless Baseband SOC
X Maxim IC – PMU
X SST – EEPROM memories
X Renesas – ASIC
X Toshiba – FPGA

Embedded die in package
(Single chip modules)



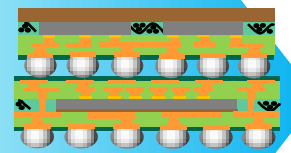
Embedded die SiP / PoP module packages

Embedded SiP



X TI – DC/DC converter
X Rohm – DC/DC converter

Embedded PoP



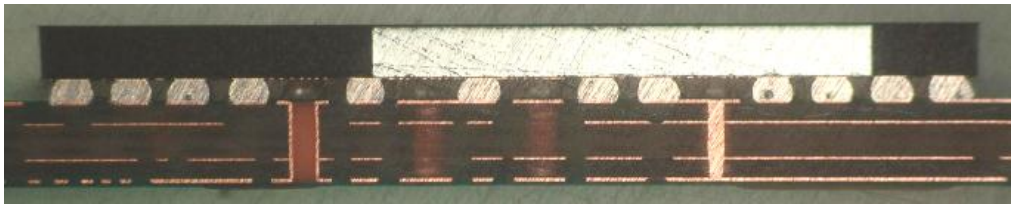
X ADI
X Infineon
X ams

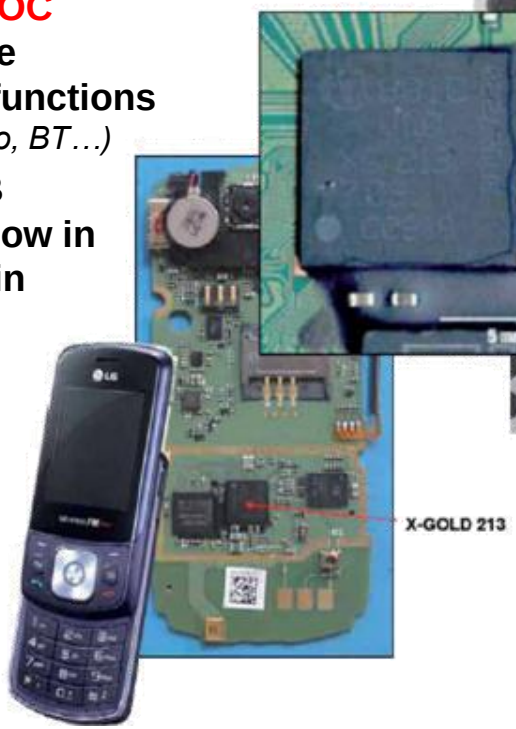
X Murata – Cellular terrestrial digital module
X Casio / CMK – Watch module
X NXP – RFID / IPD modules

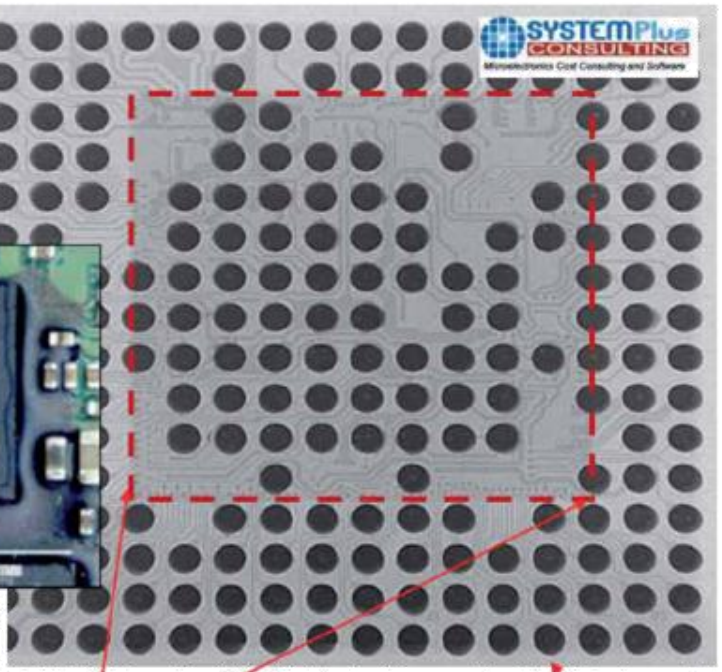
2006 2007 2008 2009 2010 2012 2014 2016 2018

First eWLB Package in High Volume Production!

- **First design win for eWLB**
  - Infineon (GE) was the first company to commercialize its own eWLB packaging technology in an LGE cell-phone in early 2009
  - ASE, StatsChipPAC have been qualified as subcontractors for eWLB manufacturing
  - Infineon's chip is a **wireless baseband SOC** with multiple integrated functions *(GPS, FM radio, BT…)*
  - Same eWLB product is now in production in some Nokia handsets since 2010

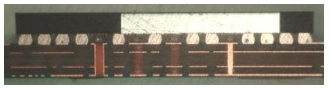






First eWLB package with Infineon's wireless Baseband SOC was found in an LG cell-phone *(Reverse Engineering pictures courtesy of SystemPlus Consulting and Binghamton University)*

Current end-products using eWLB / FOWLP



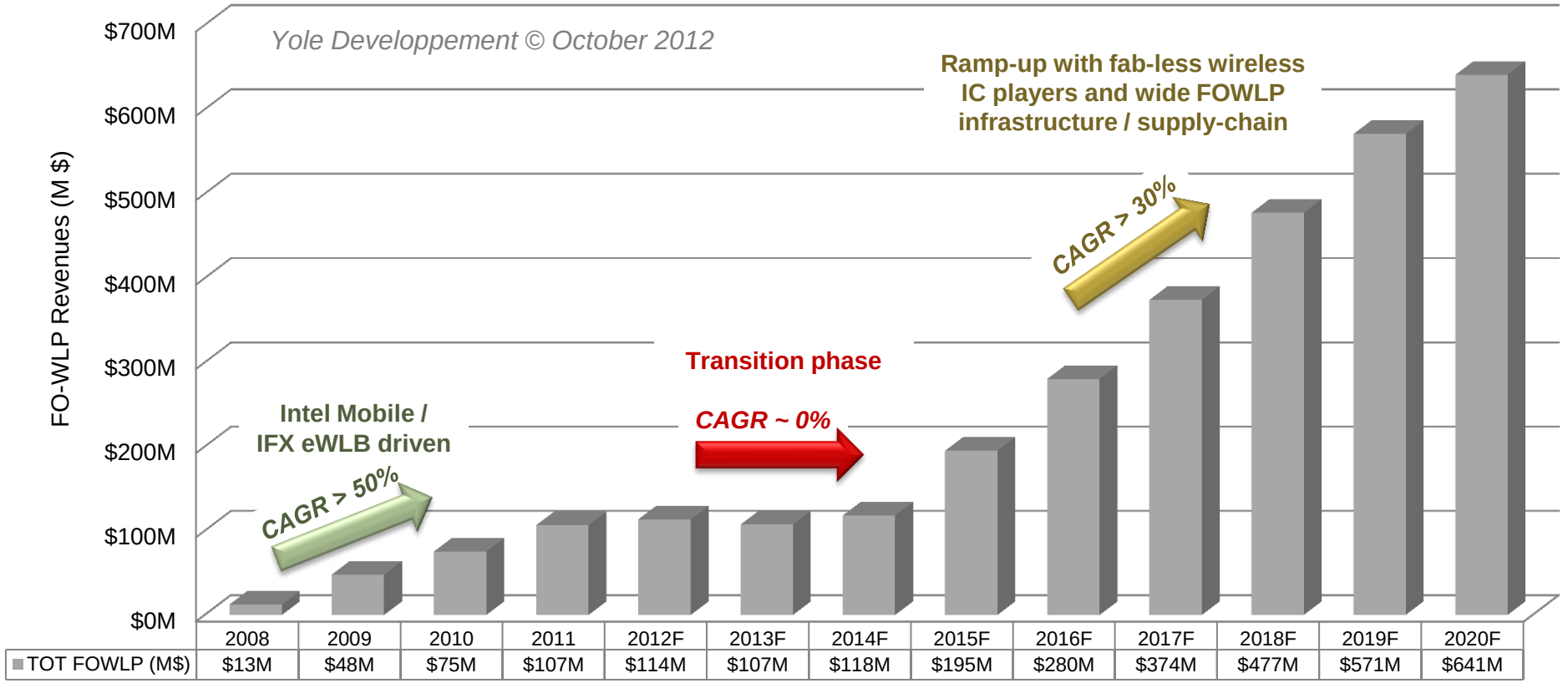
- **Mobile and wireless applications using FO-WLP packaging**
  - **LGE was the first OEM to integrate the eWLB to the wireless baseband in the following models**
    - PMB8810 phone, T310 phone, T300 phone, GD350 phone, GB220 phone, GB230 phone, GS170 phone, GU230 phones
  - **We can also find eWLB in Samsung cell phones (baseband modem)**
    - S3350 phone, Galaxy Tab tablet, Galaxy S phones
  - **Some Nokia's phones use eWLB for the baseband modem and RF tranceiver**
    - S30 series platform (2010 phone version), S40 series platform (2010 phone version), 1 smart-phone line (to be identified)

- **Extension of the technology platform to a wider field of application areas is in preparation**
  - **FO-WLP is expected to be integrated as well as some point in the automotive and medical applications**

FOWLP activity market evolution & forecast

FOWLP activity Revenues (M$)

Overall evolution since eWLB technology introduction



	2008	2009	2010	2011	2012F	2013F	2014F	2015F	2016F	2017F	2018F	2019F	2020F
TOT FOWLP (M$)	$13M	$48M	$75M	$107M	$114M	$107M	$118M	$195M	$280M	$374M	$477M	$571M	$641M

- **After growing fast since Infineon / Intel Mobile's push for eWLB technology commercialization, the FOWLP market activity reached the $100M market valuation last year**
  - **This young industry will probably need to wait for 2015 – 2016 time frame to reach the $250M market valuation as the technology to ramp-up in HVM, the demand moving from IDMs to fab-less wireless IC players (such as Qualcomm, Broadcom, Mediatek, etc…) and supported by a solid infrastructure and supply-chain of OSATs**

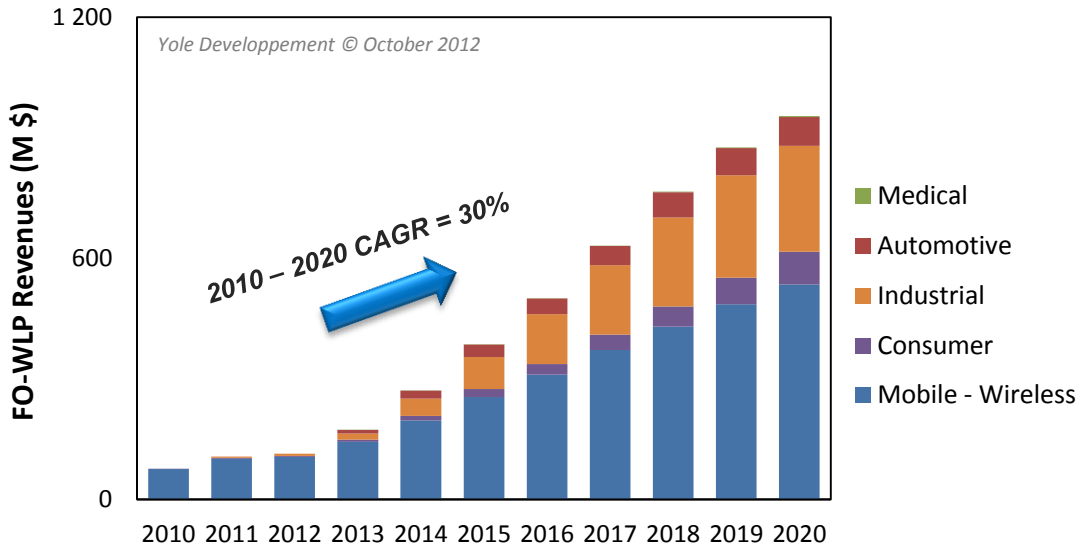
YOLE DÉVELOPPEMENT

Optimistic scenario *(1/2)*

- To bend the rules, we decided in this report to propose an alternative scenario for FOWLP market evolution
- Indeed, regarding the numerous rumors linked to this space, several feedbacks pushed us to propose an optimistic forecast model, making the market starting growing fast as soon as 2013
- This enthousiastic scenario would be linked to the following players' activity
  - Spreadtrum (CN)
  - Maxim (US)
  - ADL (TW)
  - Mediatek (TW)
- In this alternative model
  - A 30% penetration rate have been applied for FOWLP as soon as 2013, for existing products already using this platform
    - Digital Baseband Processor
    - APE/BB wireless SoC
  - Volume production for the other applications would start 1 year sooner than in our initial model (for RF tranceiver, PMU, ASIC, Touchscreen Controller, RF Connectivity devices)

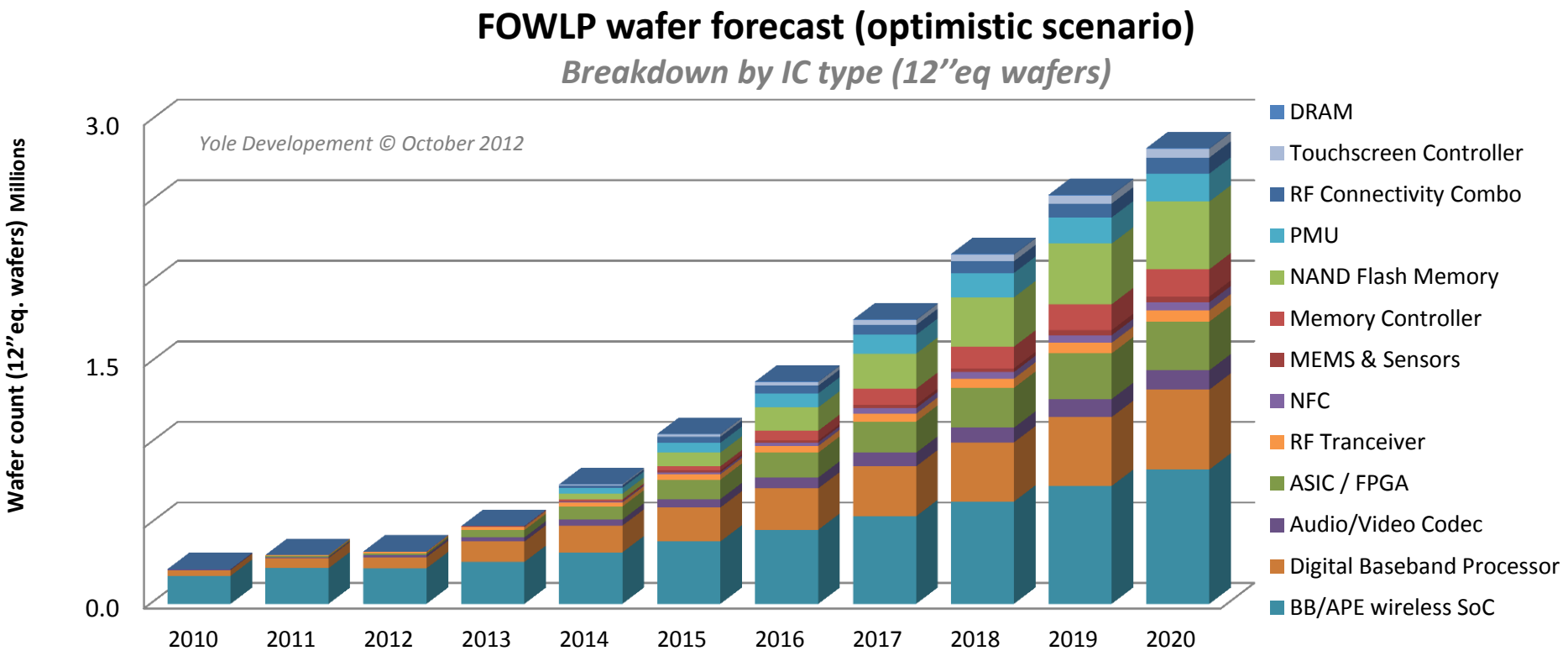
FOWLP Revenues (optimistic scenario)

Breakdown by application area (M$)



YOLE DÉVELOPPEMENT

Optimistic scenario *(2/2)*

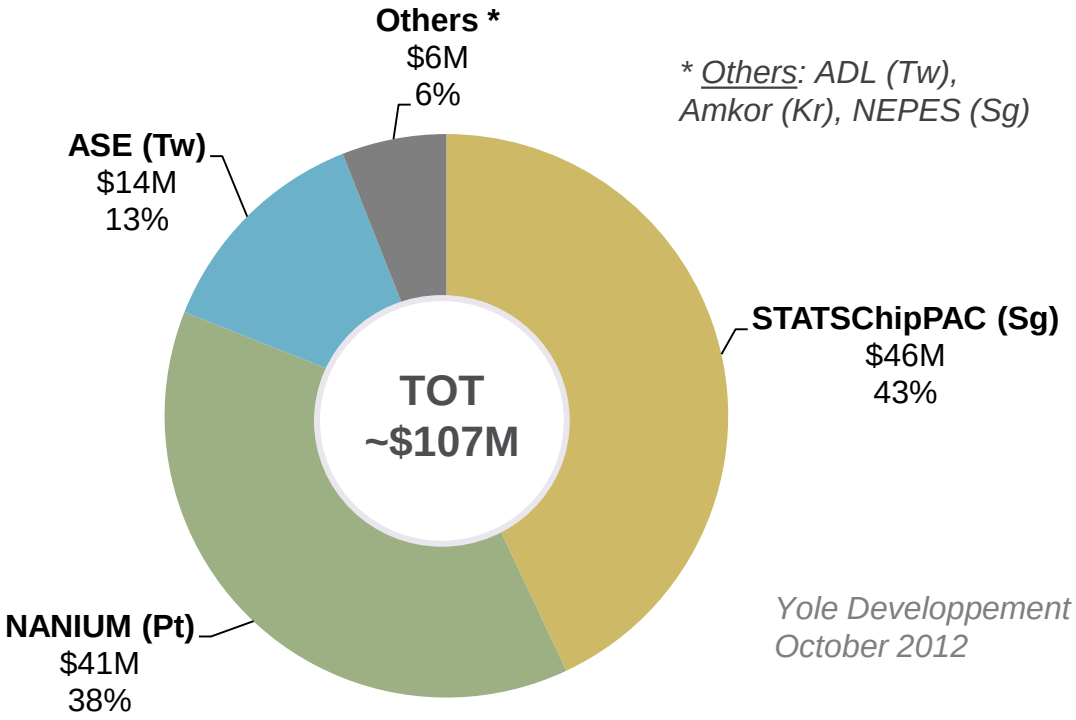


- **According to this model the market would grow at a 30% CAGR on the 2010-2020 time frame, leading to a ~ $1B market in 2020**
- **It would lead to nearly 500,000 wafers shipped in 2020 and more than 2.8 billion in 2020**
- **Now we just have to wait and see if the rumors come true and if the infrastructure of this young industry will be strong enough to support this fast growing evolution**

FOWLP 2011 revenues market shares (in M$)

FOWLP 2011 revenues market shares *(in M$)*

Breakdown between main players



** Others: ADL (Tw), Amkor (Kr), NEPES (Sg)*

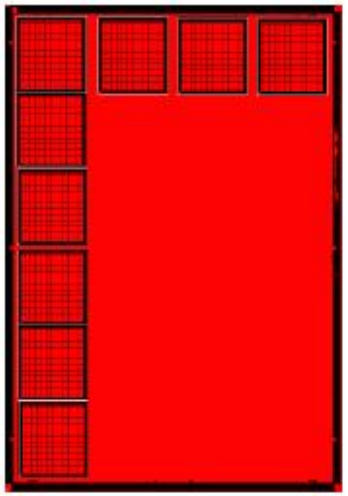
Yole Developpement © October 2012

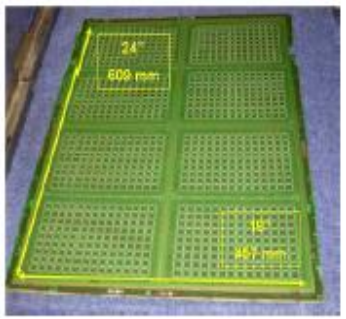
- **NANIUM (Pt) and STATschipPAC (Sg) shares more than 80% of the activity, mainly driven by Intel Mobile volume demand on eWLB production**
  - **ASE (Tw) is shutting down its 200mm eWLB line. Other OSATs have qualified other FOWLP technologies such as ADL (Tw), Amkor (Kr) and NEPES (Sg)**
  - **Additional packaging houses are coming on board as well such as TSMC (Tw), SPIL (Tw) and J-Devices (Jp)**

PANEL Infrastructure for Embedded Chip Packaging

- **Embedded die packaging technology will leverage an entirely new infrastructure based on large PANEL, low cost PCB manufacturing techniques!**
  - **Typically able to integrate more than 10,000 – 40,000 dies per panel!**

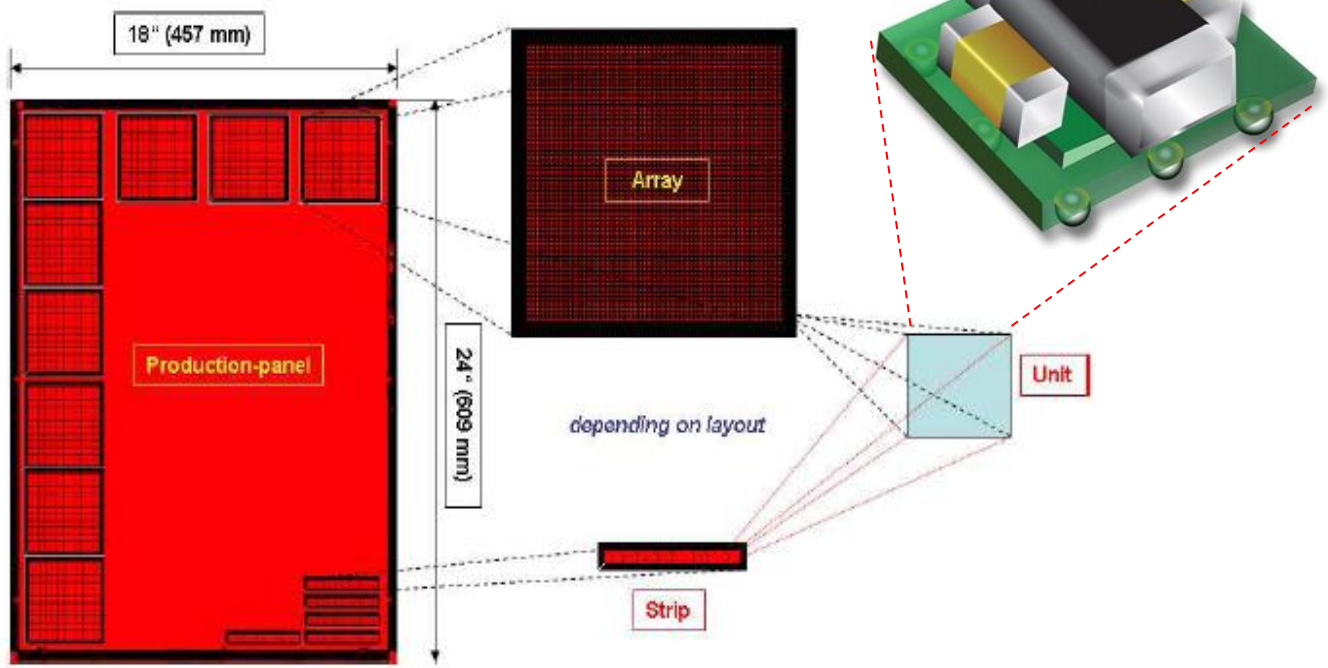
• Production format:
18" x 24" (457 x 609 mm)





Courtesy of AT&S

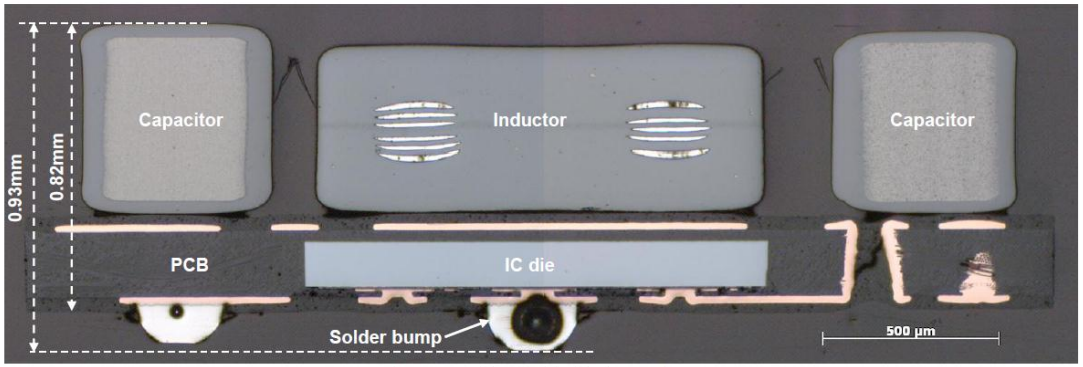
• Design relationship
Production panel – array / strip – unit



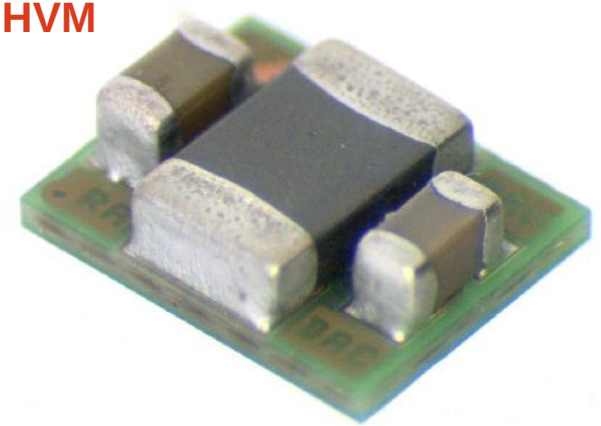
→ AT&S's first generation production is based on 18x24 sq. inch panels. 2nd gen on 21x24 sq. inch panels!

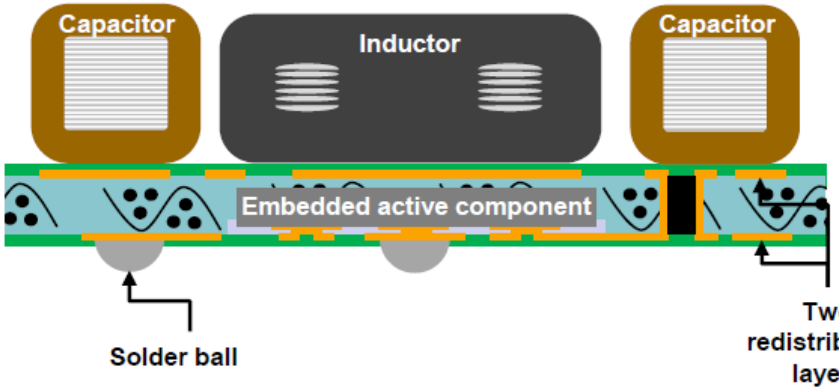
AT&S step into HVM for Embedded MicroSiP packages

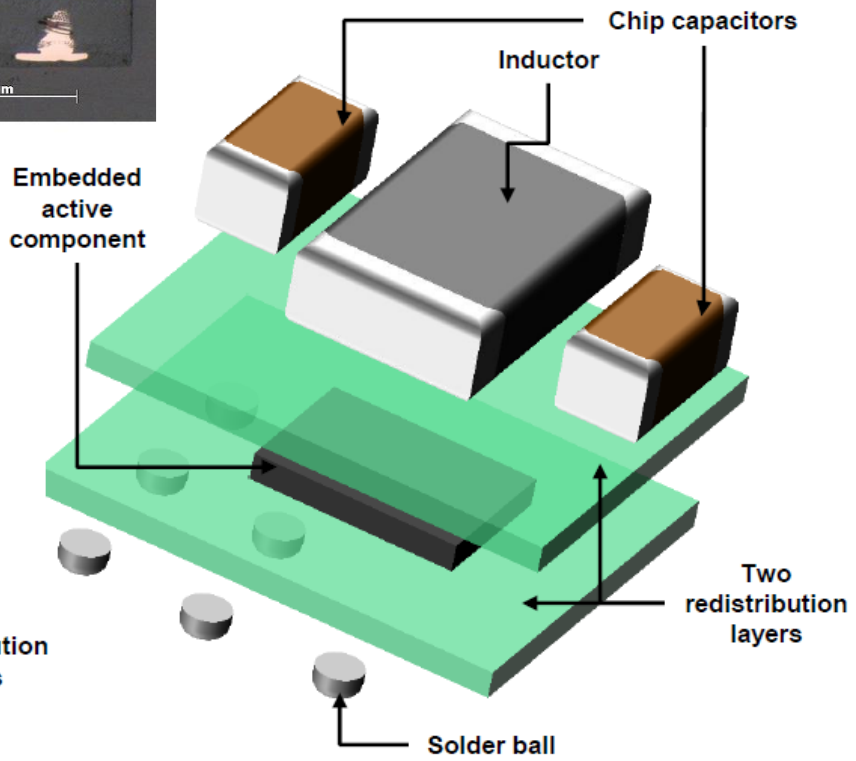
- **Texas Instruments (US) is the first customer to qualify into HVM the embedded die package line of AT&S**
  - **First application is a DC-DC converter MicroSiP™ module:**



Cross-section 2 – Optical overview





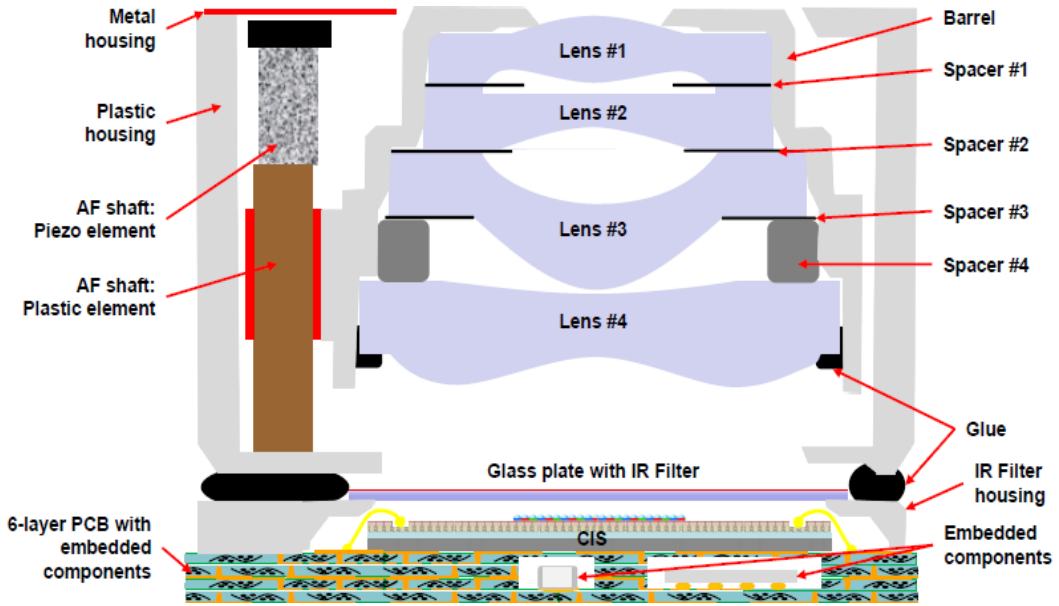


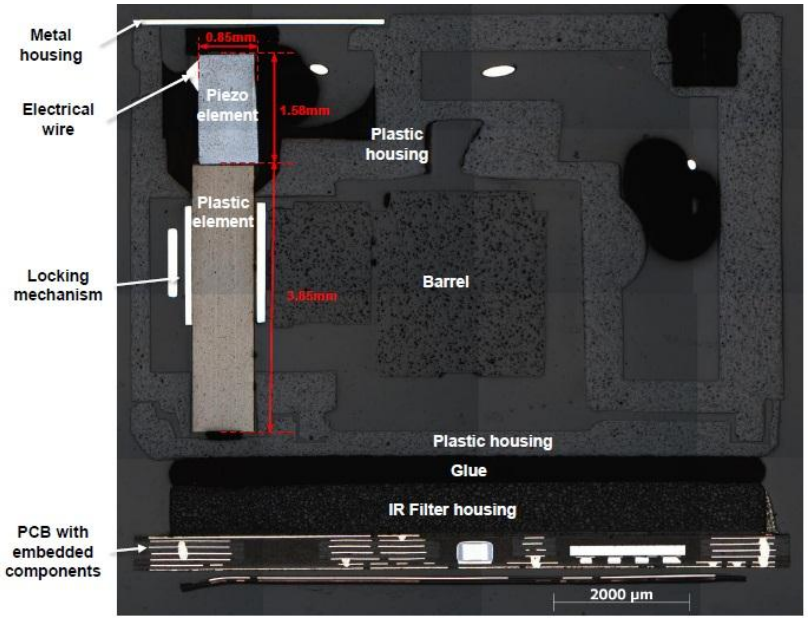
Teardowns courtesy of SystemPlus Consulting

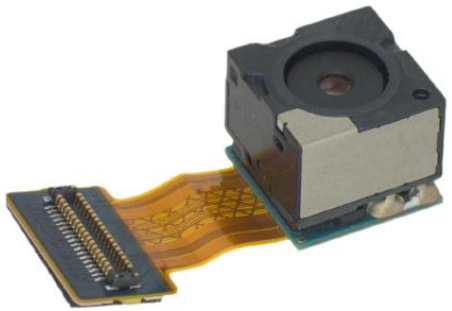
DNP's Embedded active & passive substrate in HVM

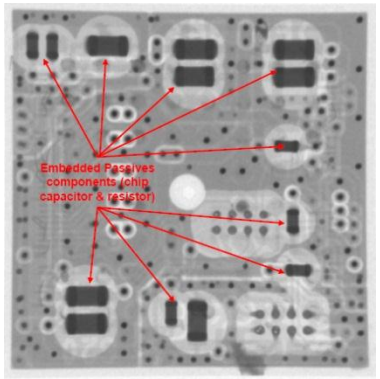
DNP

- **DNP (JP) is supplying Sony's camera module with embededded passive and active components in HVM since 2010 already**
  - **Auto-focus driver IC and DC-DC converter WLCSP dies are placed within the coreless cavity substrate**

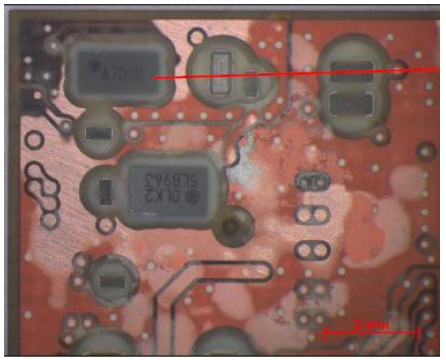


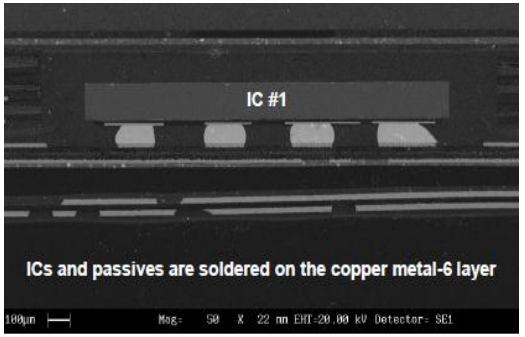






PCB X-Ray





Teardowns courtesy of SystemPlus Consulting

Embedded die package PANEL infrastructure Roadmap

OSAT
players driven

4”x20” – *102x508mm / PCB laminate substrate*

YIELD % to increase

8”x20” – *204x508mm / PCB laminate substrate*

YIELD % to increase

16”x20” – *400x505mm / PCB laminate substrate*

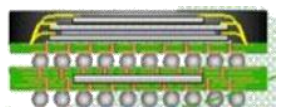
1/4 PANEL

1/2 PANEL

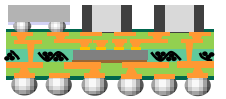
Full PANEL

SHINKO

DIGITAL
thin PoP module applications
- *BB / APE*



RF & MIXED SIGNAL
SiP module applications :
- *PMU / PMIC*
- *RFEM*
- *RF connectivity (WLAN/BT/FM)*
- *Audio/Video Codec*



Substrate
players driven

18”x24” - *457x610mm / HDI rigid PWB* ---YIELD % to increase---> **21”x24” -** *533x610mm / HDI rigid PWB*

20”x13” - *510x340mm / PCB laminate substrate* ---YIELD % to increase---> **20”x16” -** *505x400mm / PCB laminate substrate*

14”x10” - *350x250mm / Flexible PWB roll-to-roll* ---YIELD % to increase---> **24”x24” -** *610x610mm / Flexible PWB & LCD*

DNP Dai Nippon Printing Co.,Ltd

TAIYO YUDEN

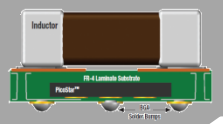
TDK-EPC

HIGHTEC Custom made MicroCircuits

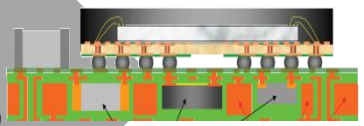
AT&S

Fujikura Ltd.

POWER & ANALOG
small SiP module applications:
- *DC/DC converter*
- *IPD*
- *AF driver*
- *Small ASICs*
- *MOSFET*
- *IGBT*
- *RFID*



RF & MIXED SIGNAL
large SiP module applications :
- *PMU / PMIC*
- *RFEM (SAW, PA, etc…)*
- *RF connectivity (WLAN/BT/FM)*
- *Audio/Video Codec*

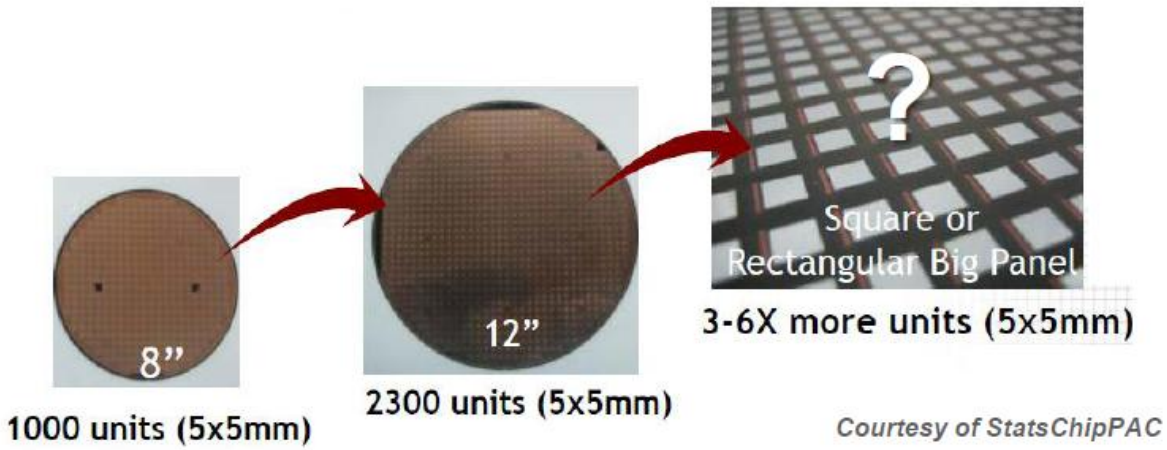


2010 - 2012 | 2013 | 2014 | 2015 | > 2016

First Conclusions on Embedded Wafer-Level-Packages

- **1st generation FOWLP and Embedded die packages is a high volume reality and the two infrastructures are now clearly settled and proven in HVM in each of their very different application space**
  - **Today, first generations of Embedded die package and FOWLP technologies are not really competing at all as they are driven by different players and initially target very different applications.**

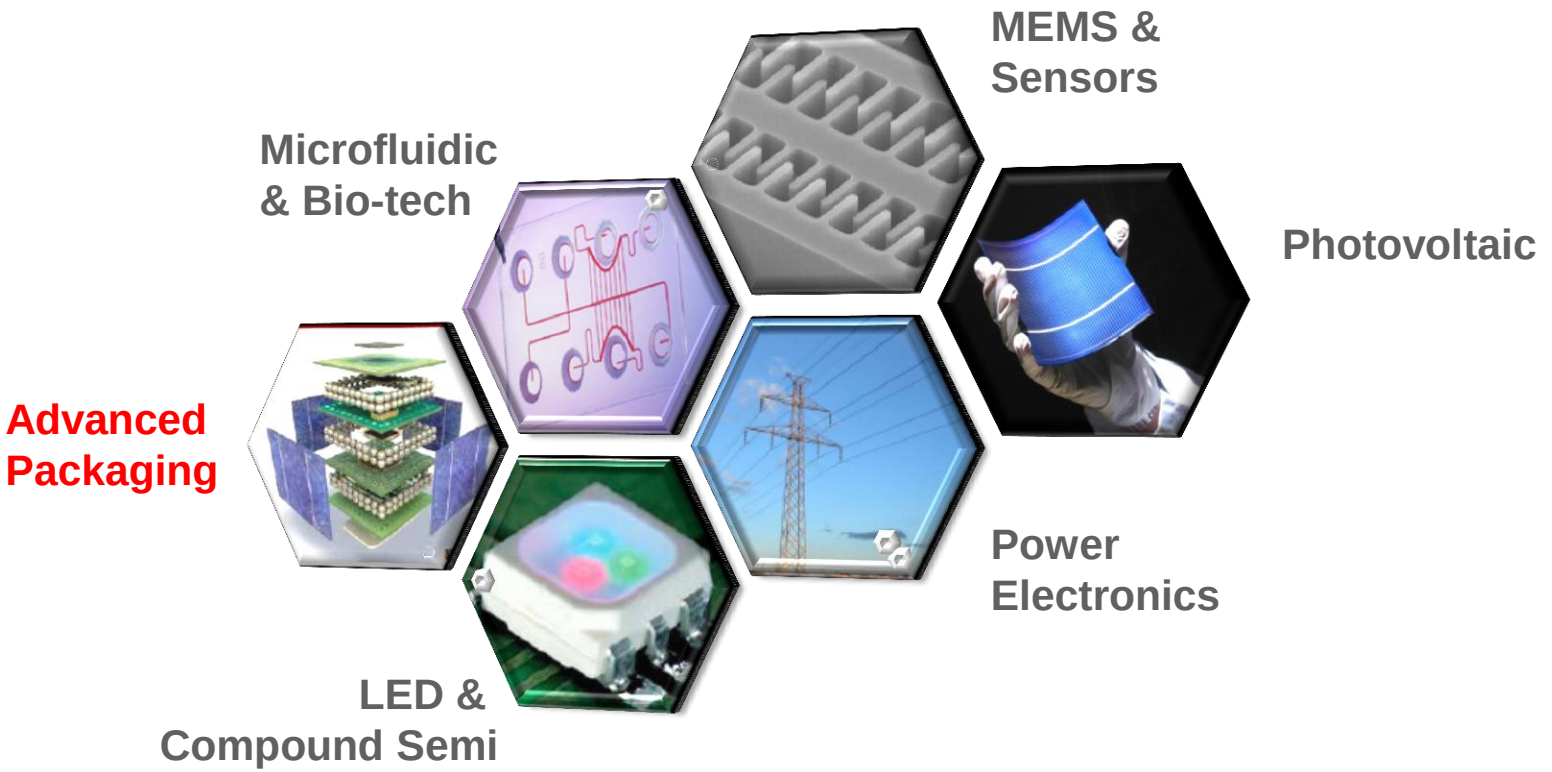
- **However, this situation will totally change in the future with "2nd generation" derivatives of the technologies that are currently under development for future SiP and PoP module realizations, likely on larger format**
  - **We are likely to be witness to a fascinating battle in the years to come in the 3D Packaging space with on one hand, embedded die packaging technologies supported by large panel PCB infrastructure and FOWLP technologies on the other hand, which is looking for moving to larger wafer format, likely square 300mm PANEL first and possibly later on larger PANEL mixing PCB, semiconductor back-end, semiconductor WLP and LCD large area processing know-how**



Yole Developpement
Company Presentation

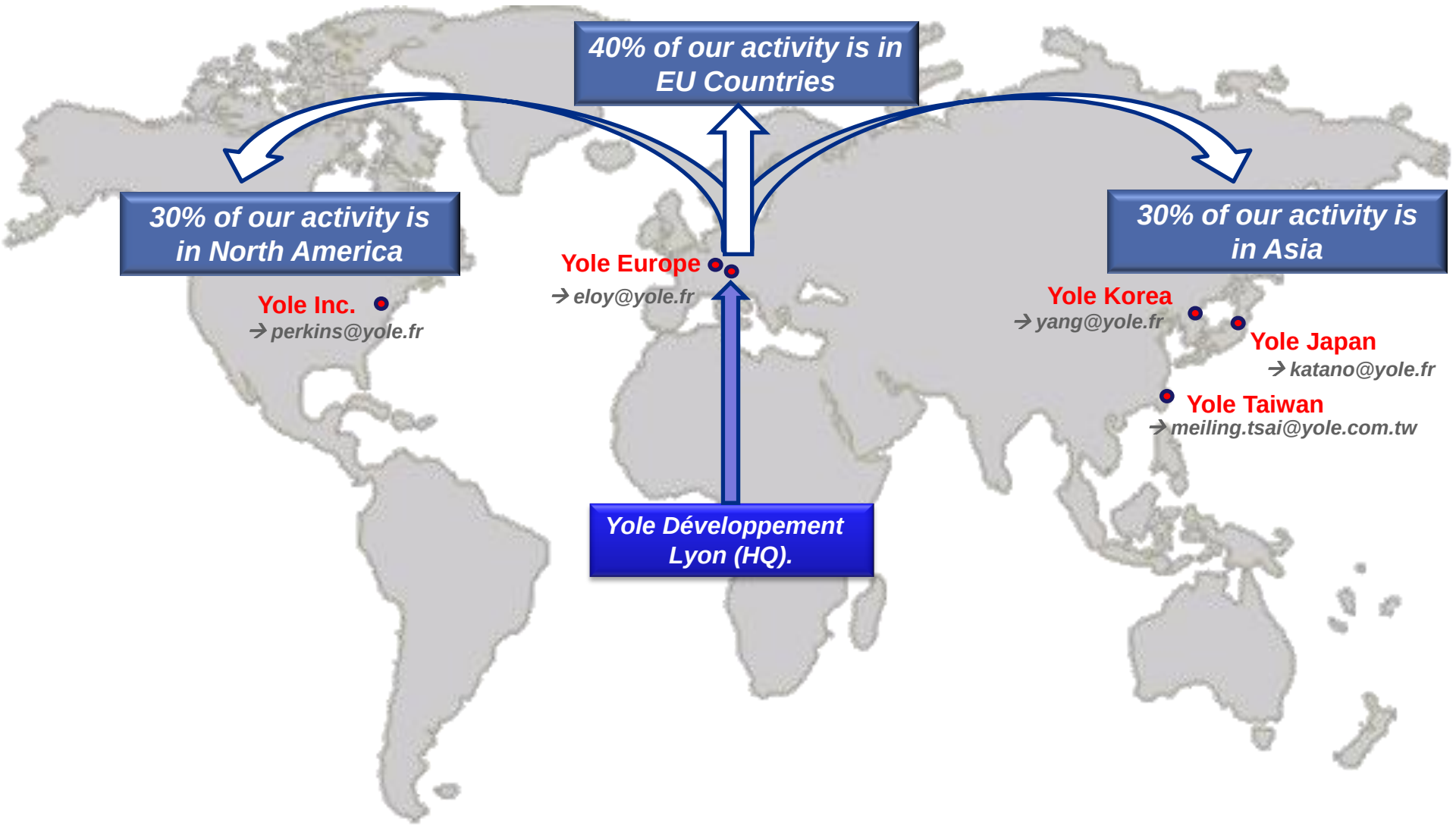
Fields of research activity

- **Yole Developpement is a market research and strategy consulting company, founded in 1998. We are involved in the following areas:**



- **Yole Développement has 25 full time analysts, with both technical and marketing/management background and operate worldwide since 1998**

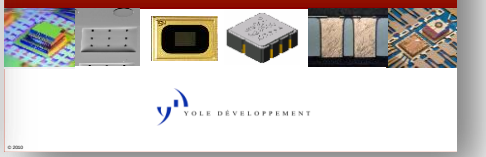
Our Global Presence & Activity



Our latest advanced packaging market research reports

LED Packaging
Market & Technology Trends

MEMS Packaging
Market & Technology Trends



3D IC & TSV
2010 Market Analysis

Via First / Via Last?
3D integration Scenarios

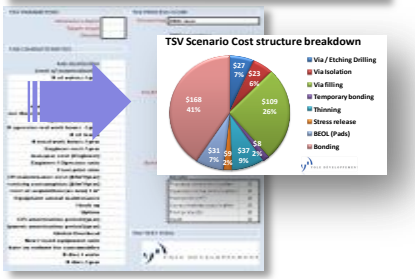
FO WLP & Embedded die

WL CSP
2012 Report update

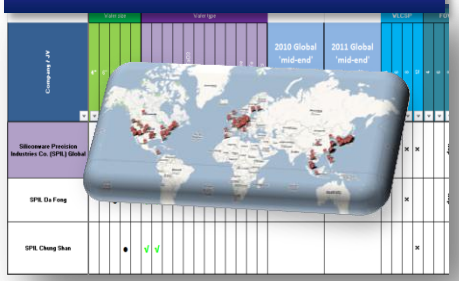
2.5D Glass & Silicon interposers - 2010 Report

IPD - Thin-film
Integrated Passive Devices

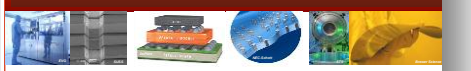
TSV+
Cost Analysis Tool for your 3D IC manufacturing



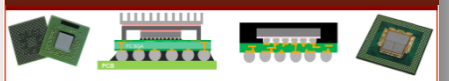
Wafer Packaging Fabs DATABASE



Equipment & Materials
for 3DIC & Wafer-Level-Packaging



Flip-chip
2011 Report



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