

Chip Scale Review®

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Volume 21, Number 4

The Future of Semiconductor Packaging

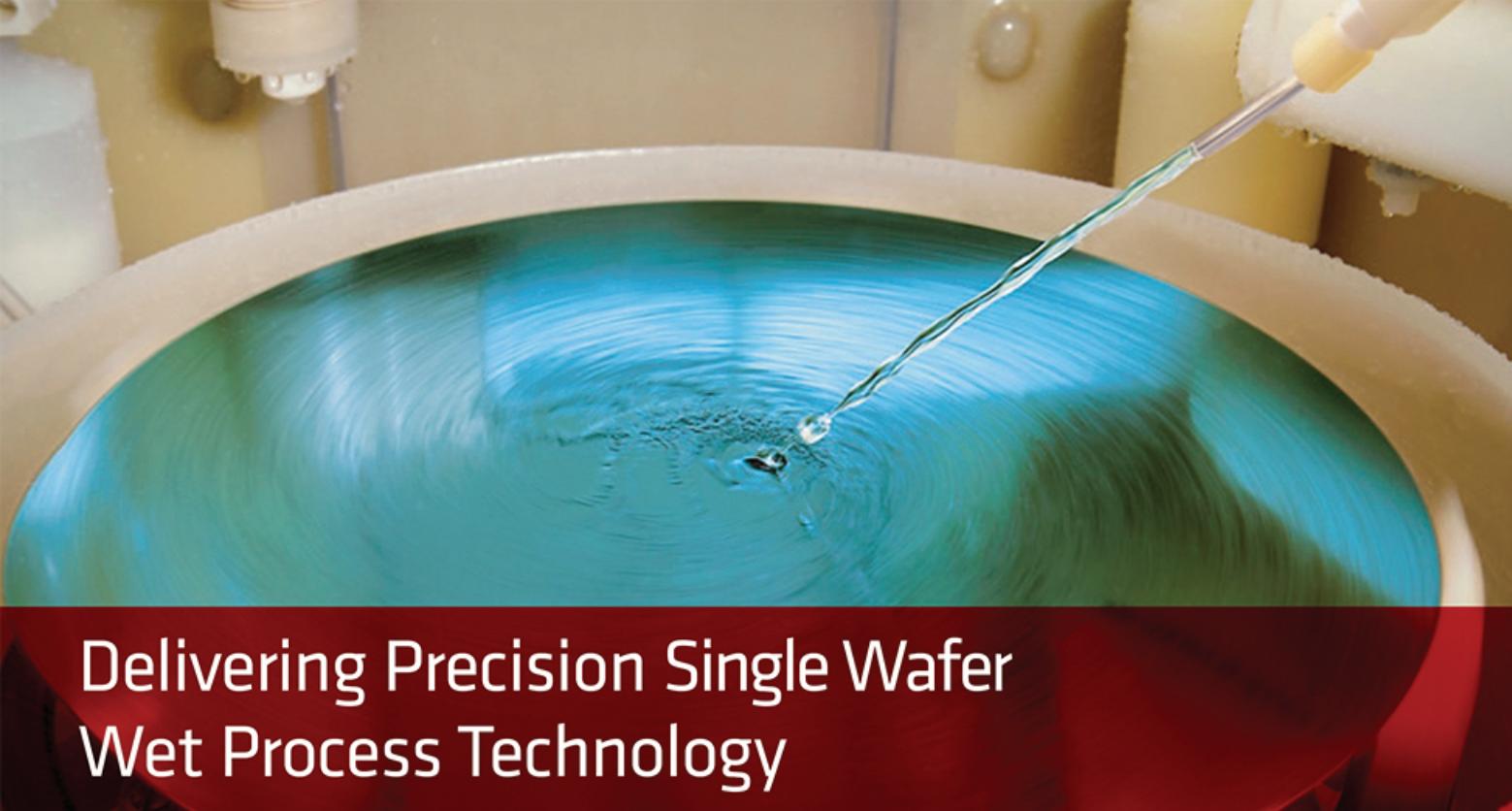
July • August 2017

Wafer Thinning for Advanced Packaging Applications

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- Performance and cost for 2.5D packaging
- TSV technologies for next-gen application challenges
- High-density advanced packaging solutions for today's OSATs & foundries





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TSV Clean ²	✓			
Flux Clean	✓			
PERR		✓	✓	✓



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Inside the WaferStorm® Precision Surface Processing System, a 200mm silicon wafer on an automated handler moves toward the proprietary ImmJET™ heated immersion and a high-pressure spray chamber. Using a single-wafer wet etch process for wafer thinning, the solvent techniques and advanced process control provide a low-cost alternative to chemical mechanical polishing and plasma dry etch processes for advanced packaging applications.

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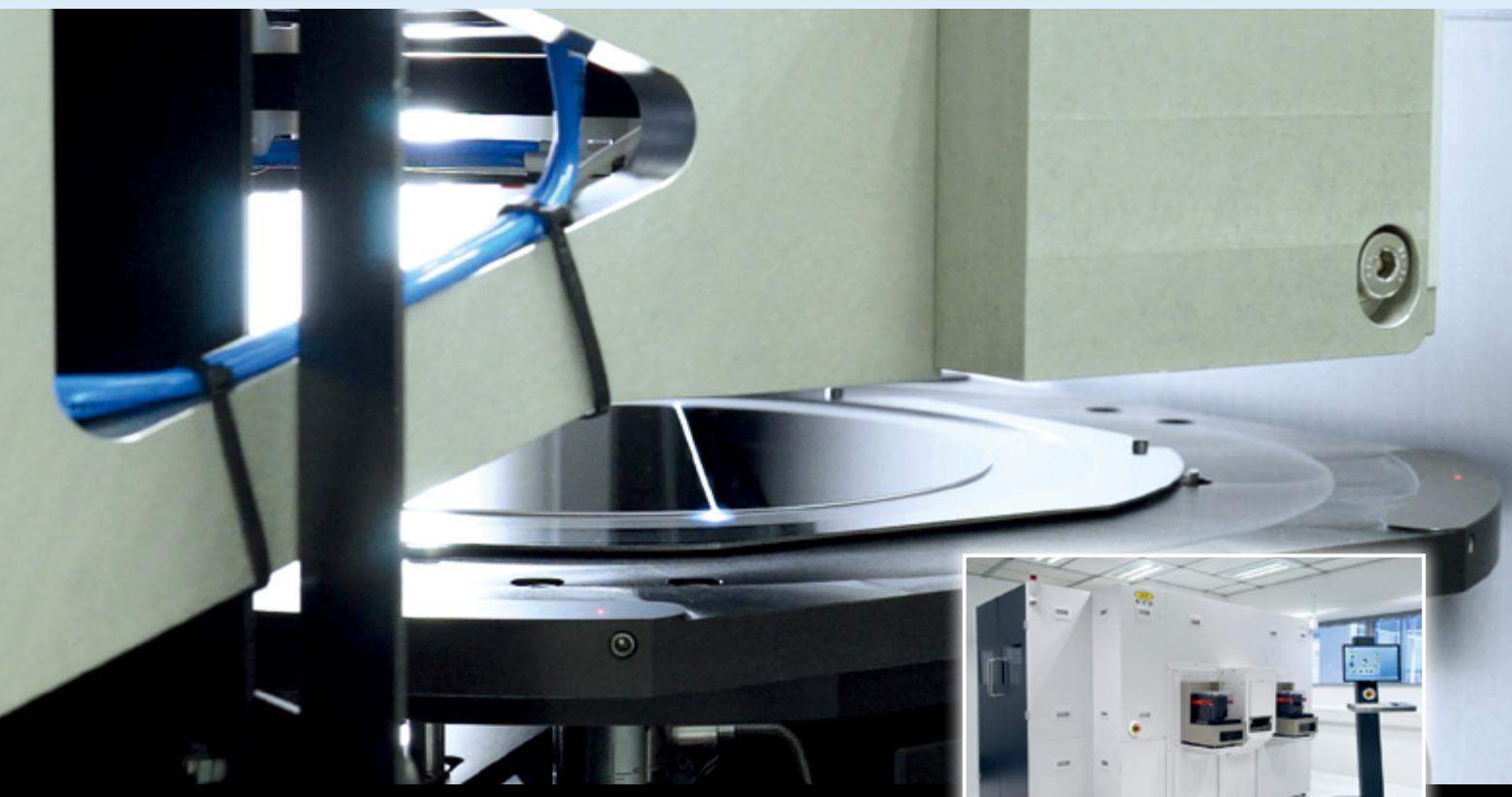
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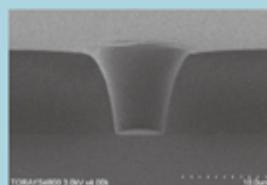
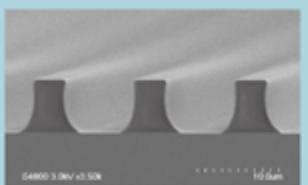
Low-temperature curing for FI/FOWLP

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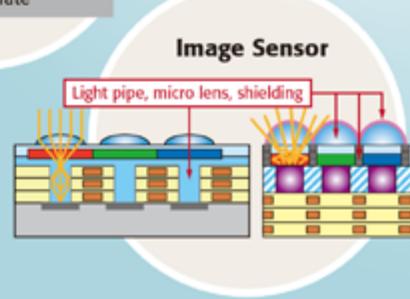
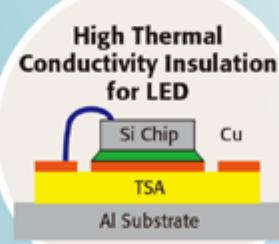
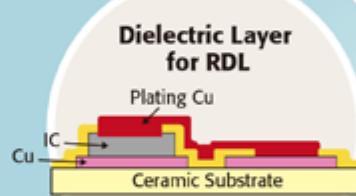
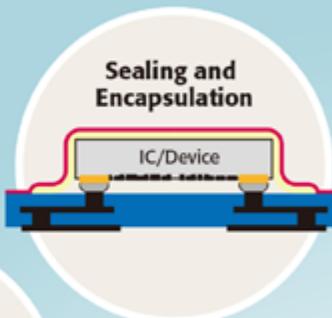
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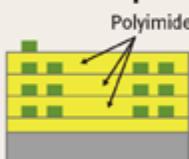
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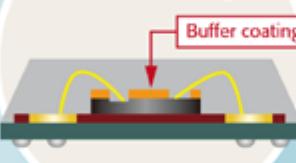
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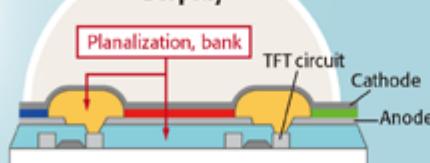
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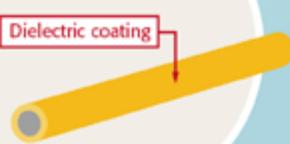
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MARKET UPDATE

OSATS: challenges for revenue growth

By E. Jan Vardaman [*TechSearch International*] and Dan Tracy [*SEMI*]

The top 20 outsourced semiconductor assembly and test (OSATS) service providers accounted for approximately \$23 billion in sales for 2016. With the growth in fabless companies and outsourcing trends by the world's semiconductor companies, OSATS experienced double-digit revenue growth rates. Today, the OSAT sector can be considered a mature market, and with this maturity comes lower growth rates and challenges for continued investment in the next-generation of packaging and assembly capabilities. Changes facing the sector include:

- Maturing smartphone market with slower growth rates than the historic double-digits;
- Downward price pressure as fabless companies merge and consolidate purchasing information; and
- Competition from foundries entering the high-margin advanced packaging space.

Can China's OSATS drive industry growth?

There are several major domestic OSATS in China (**Figure 1**). Over the last several years, these companies have expanded their capabilities to include advanced packaging. Jiangsu Changjiang Electronics Technology (JCET) is located in Jiangyin, China. Jiangyin Changdian Advanced Package Corporation (JCAP) and STATS ChipPAC are members of JCET. Services include wafer bumping, flip-chip assembly, wafer-level packaging (WLP), and fan-out wafer-level packaging (FOWLP). Tongfu Microelectronics (formerly Nantong Fujitsu Microelectronics Co., Ltd) is located in Nantong, Jiangsu Province, China. Advanced packaging services include wafer bumping, flip-chip assembly, and WLP. Tianshui Huatian Technology Co., Ltd. (TSHT) is based in Tianshui City, Gansu Province. The subsidiary in Xi'an offers advanced packaging,

including wafer bumping, flip-chip assembly, WLP, and FOWLP. Another subsidiary, Huatian Technology (Kunshan) Electronics Co., Ltd., offers production of image sensors with through-silicon vias. Production of finger print sensors with through-silicon vias (TSVs) is planned in a fully automated facility. China Wafer Level CSP was founded in Suzhou and provides WLPs for CMOS image sensors, fingerprint sensors with TSVs, MEMS, smart card, and DRAM assembly.

The top three China OSATS accounted for almost 20% of the revenue for the top 20 companies in 2016 and are experiencing double-digit growth that can be traced to more than just acquisitions. With this information in mind, we can therefore say that OSATS are growing as China's fabless companies grow.

China is now the second largest market consuming packaging materials — second only to the broader Southeast Asia region (excluding Taiwan) — with sales estimated to reach \$4.6 billion in 2017. ASE's COO, Tien Wu, calls China the driving force behind the world's semiconductor growth over the next six years. He notes that China plans to expand its fabless IC design sector's global presence to account for 42% of the worldwide IC design industry output value in the foreseeable future. The number of IC design houses in China increased from 681 firms in 2014 to 1,362 in 2016, according to the China Semiconductor Industry Association (CSIA).

SEMI reports the possibility of 62 front-end fabs scheduled to begin operation between 2017 and 2020; 26 are located in China. While no Chinese firms are in the list of the world's top 20 semiconductor makers, plans are underway to change this. China has enormous demand for semiconductors, but lacks adequate

domestic supply. China imports over \$200 billion in semiconductors per year, the biggest trade deficit in the global semiconductor market, according to the state-run Xinhua News Agency.

China's "Made in China 2025" is a long-term Chinese government plan to become self-sufficient in the semiconductor industry. The Chinese government plans to develop its domestic industry through a combination of government and private financial funds, which could total more than a hundred billion dollars over the coming years. The plan calls for China to be 40% self-sufficient in IC devices in 2020 and 70% in 2025. China has set a goal for its IC design industry of generating \$60 billion in output value and a 35% share of the global IC design market by 2025.

The Chinese government has created a new \$2.8 billion holding company. Under the direction of the Chinese government, Tsinghua Unigroup, China's largest chip design firm, acquired a majority stake in XMC, a leading semiconductor maker backed by the national semiconductor fund. One of the goals is a plan to develop a domestic memory industry, including both flash and dynamic random access memory (DRAM). XMC is developing 3D NAND (with stacked cells, not TSVs) and plans to have commercial production equipment installed in the first half of 2018 [1]. XMC is reported to have received \$24 billion in funding for the memory fab. Activities also focus on the development of multi-

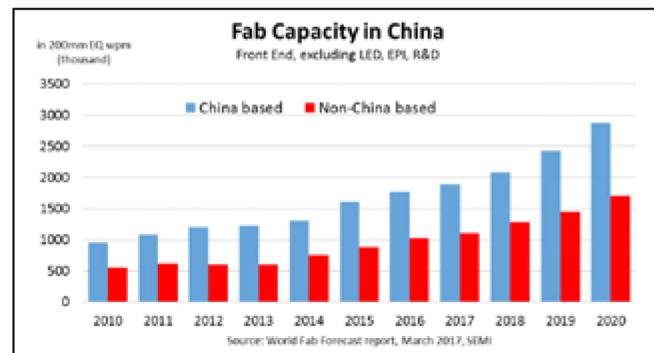


Figure 1: Fab capacity in China. SOURCE: SEMI

core CPUs for PCs and servers and low-power mobile chips. The development of the memory industry (both NAND Flash and DRAM) is also underway.

SiP: a bright spot

Despite the constant price pressure, there are areas for revenue growth. One area is system-in-package (SiP). SiP is a heterogeneous packaging solution that provides increased functionality for a system or subsystem assembled into a standard footprint package. It contains two or more dissimilar die, typically combined with other components such as passives, filters, microelectromechanical systems (MEMS), sensors, and/or antennas. The components are mounted together on a substrate to create a customized, highly integrated product for a given application.

SiPs are found in many products including smartphones, tablets, wearable electronics (including medical products), and other consumer products. High-performance gaming systems, computers, and network systems also use SiP, as do automotive electronics. Emerging applications include autonomous driving solutions, smart homes, energy products, and industrial automation.

The complexity of SiP, including the combination of flip chip and wire bond, added features such as electromagnetic interference (EMI) shielding, antenna fabrication, and test of a more complex package can provide revenue opportunities for OSATS. Competition from electronic manufacturer services (EMS) companies is expected to increase, but today's top OSATS have strong design capability that can provide a good revenue stream over the next few years.

Danger ahead: who can afford to invest?

Incorporation of flip-chip bumping and WLP, including FOWLP, in assembly products also offers potential for higher revenue growth for OSATS, but requires higher levels of capital investment than traditional wire bond assembly. This necessitates an increasingly large revenue base to support expansion into advanced packaging. Advanced packaging, including bumping, WLP, and FOWLP

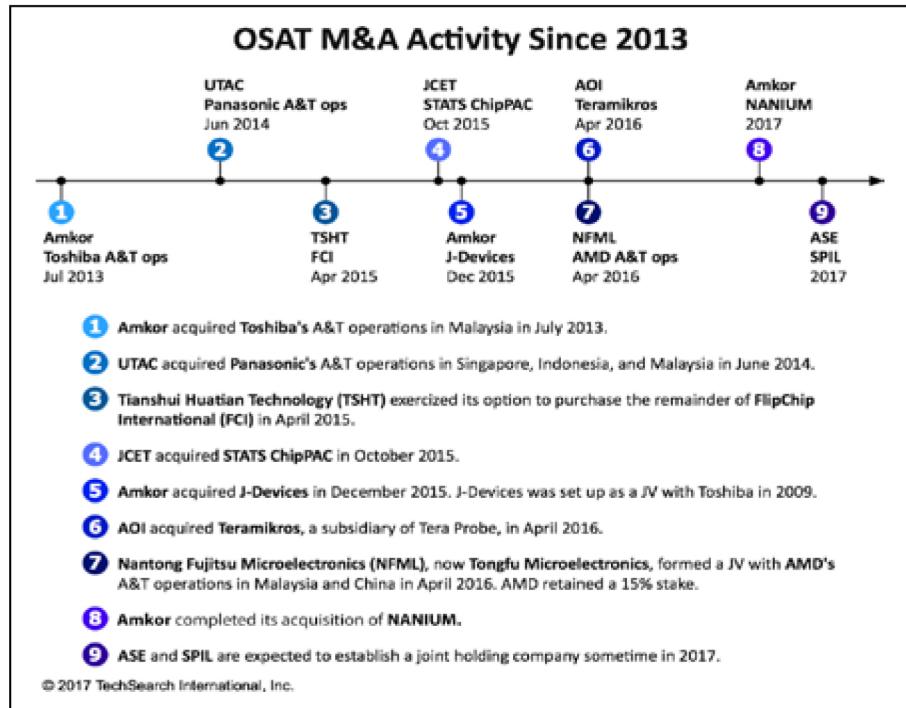


Figure 2: OSAT M&A activity since 2013. SOURCE: TechSearch International, Inc.

require an expensive set of tools, more similar to wafer fab equipment than traditional backend tools.

Many companies are increasingly turning to acquisitions for revenue growth, thereby generating a larger revenue base that will provide more capital for increased investment in advanced packaging (Figure 2). For example, Amkor's 2016 revenue includes the incorporation of J-Devices, while Jiangsu Changjiang Electronic Technology's (JCET) revenue incorporates STATS ChipPAC starting in August 2016. Tongfu Microelectronics purchased 85% of AMD's assembly operations in China and Malaysia. Revenues for Tianshui Huatian Microelectronics includes its purchase of FlipChip International, including the joint venture with Millennium Microtech called FlipChip Millennium Shanghai (FCMS). The trend in mergers and acquisitions is expected to continue as OSATS seek to increase their revenue base.

OSAT offerings will become easier to track even with continued mergers, as SEMI and TechSearch International release a new database with details of the facilities. This database contains

information on more than 100 OSAT packaging and test facilities, including the company and plant name, location, packaging and test services offered, facility capabilities, and more. For additional information please visit <http://www.semi.org/marketinfo>

Reference

1. J. Kang, "How china's new \$28 billion chip market will affect the global semiconductor industry," *Forbes*, Aug. 6, 2016.

Biographies

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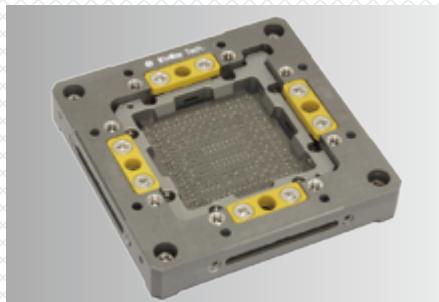
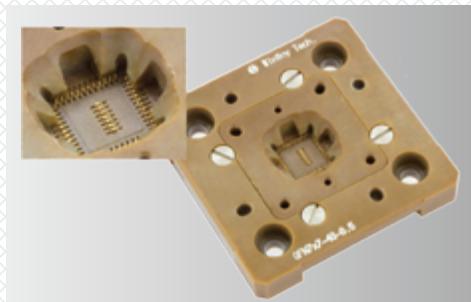
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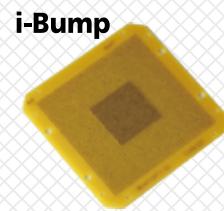
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Gearing up TSVs to solve next-generation application challenges

By Bruno Morel *[aveni]*

After a long and arduous journey from research and development to commercialization, through-silicon vias (TSVs) are now being used in semiconductor devices to form electrical interconnections in the vertical direction (2.5D and 3D), generally between multiple, often heterogeneous, layers. Sensor applications that use TSVs include CMOS image sensors (CIS), which occupy the lion's share of the TSV market, and newer, specialty applications like fingerprint sensors. Additionally, memory applications that use TSVs—namely, high-bandwidth memory and hybrid memory cube devices—are moving into volume production. These stacked memory devices offer higher performance vs. planar layouts and increased capability, especially when combined with other components to serve the graphics-processing, data-processing and server markets. Concurrently, TSVs are making headway in the automotive industry, with increased use in various microelectromechanical systems (MEMS) and sensors.

Some semiconductor manufacturers still expect that TSVs won't move beyond niche applications due to remaining roadblocks, such as thermal issues and the subsequent stress-related reliability issues with stacking memory on logic, as well as cost constraints. For now, at least, they have redirected their efforts toward alternate solutions, such as fan-out wafer-level packaging (FOWLP) at low densities, and hybrid bonding without TSVs at high densities.

However, because of the performance improvements offered by devices using TSVs, we anticipate steady adoption in more applications, leading to significant volume increases. According to industry analysts, TSV markets are expected to show continued growth, particularly in high-performance computing applications such as the growing server market. This article discusses some of the drivers, challenges and benefits involved in fabricating and implementing TSVs.

Alternatives to TSVs

Although it's true that FOWLP is taking off, thanks primarily to Apple adopting TSMC's integrated fan-out (InFO) technology in its A10 processor, it does have limitations. Currently, FOWLP technologies in manufacturing achieve 5µm line/space (l/s) densities. High-density FOWLP, such as Amkor's SWIFT™ and SLIM™, have achieved 2µm l/s features, but these have yet to be commercialized. Efforts are underway to extend high-density FOWLP to system-in-package (SiP), and ultimately to interposer applications, in which a high-density fan-out model is attached to a substrate as an alternative to TSV 2.5D.

FOWLP is undoubtedly a strong competitor in heterogeneous applications involving CMOS image sensors and MEMS devices because high density is not a requirement. However, this is not the case for high-performance computing server applications and heterogeneous stacking of memory on logic because of the l/s limitations. Essentially, FOWLP is disqualified for applications requiring higher-density interconnects in the sub-1µm range.

Another technology being touted as a cost-effective, high-density alternative to TSVs is Cu-Cu/oxide hybrid bonding, invented and patented as Direct Bond Interconnect (DBI®) by Ziptronix. DBI joins the dielectric regions and the metal interconnect regions on each of two wafers, providing both mechanical support and dense electrical interconnects between the wafer pair. Demonstrated at an interconnect pitch of 2µm, DBI is said to be scalable to the lithography and alignment manufacturing capabilities of any application [1]. Additionally, depending on the achievable wafer-to-wafer bond accuracy, it is believed that pitches to 1µm will be possible [2].

In 3D backside-illuminated image sensors, DBI provides a low-cost alternative to TSVs, as it combines the

permanent bonding and interconnect steps into one. Indeed, it could become the technology of choice to replace fusion bonding on account of its ability to make electrical contact and its superior electrical and mechanical properties [3]. However, DBI requires face-to-face interconnection of the bond pads, and therefore it is limited to a two-wafer or two-die stack. It should be noted, however, that work has been done to extend Cu-Cu direct bonding to incorporate TSVs. Imec reports success implementing 5µm-diameter, 50µm-deep via-middle TSVs to connect the hybrid bonded wafer interfaces to the external wafer backside [4].

Among the biggest benefits of TSV interconnects are the signal densities that can be achieved. In general, the distance a signal has to travel along a wire (or interconnect path) is directly related to power usage. TSVs serve to shorten the signal path between the die, allowing the system to run faster while using less power [5]. Shorter wires decrease the average load capacitance and resistance and decrease the number of repeaters needed to regenerate signal on long wires, thereby improving signal density [6].

In applications with interconnect densities in the sub-1µm range and requiring more than two stacked wafers or die-to-wafers, TSVs are currently the only commercially available option. As the server market growth trajectory continues to soar, the volumes of advanced packages implementing high-density TSV interconnects will increase exponentially.

Building a case for high-aspect-ratio TSVs

As CMOS scaling continues in logic devices and we see the likes of Intel, TSMC and Samsung ramping to 10nm and 7nm processes, the need for high-aspect-ratio (HAR) TSVs for stacked devices becomes more critical. Stacking at advanced nodes necessitates a sub-micron technology that is similar to the dimensions of the upper metal

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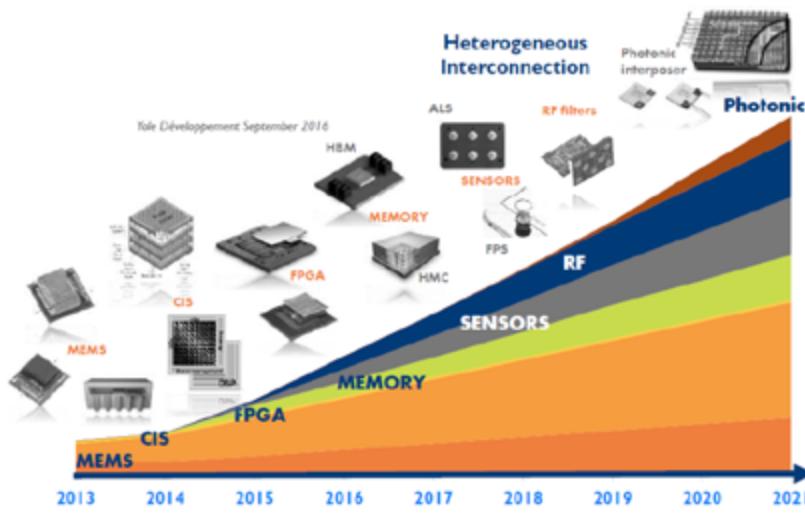


Figure 1: TSV wafer starts by application. SOURCE: Yole Développement

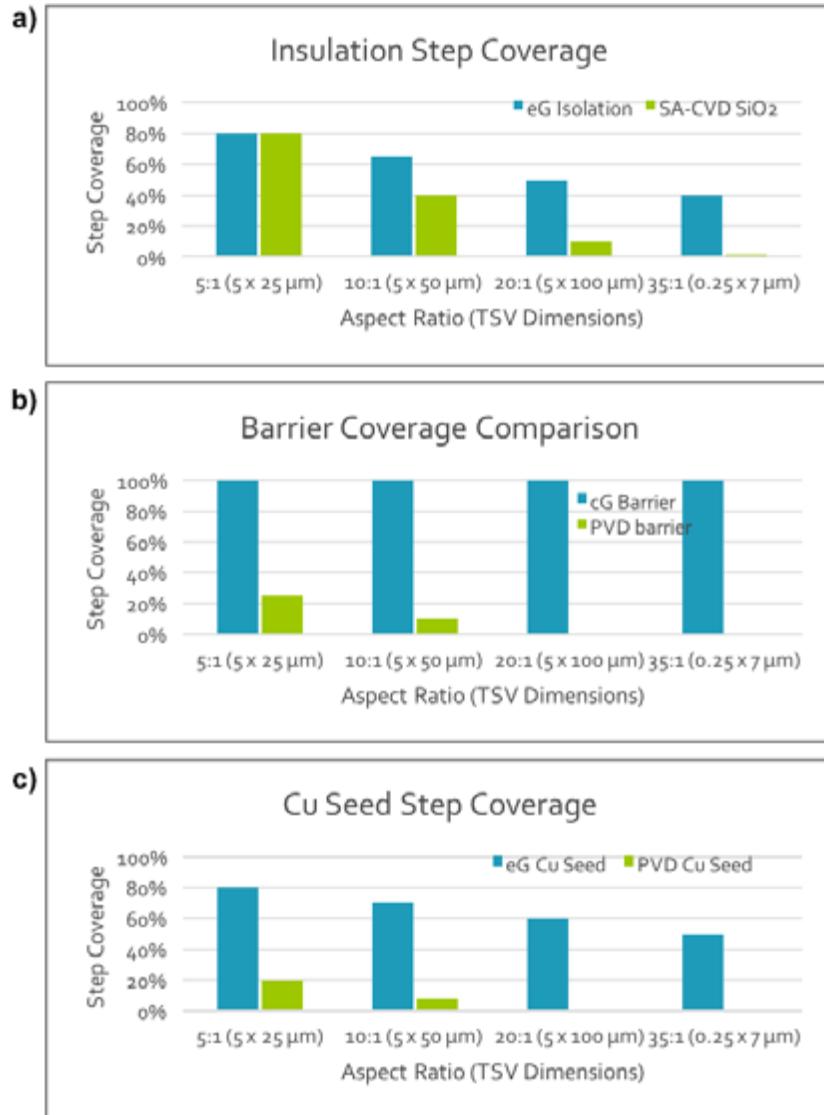


Figure 2: Step coverage comparison of various eG and cG films vs. conventional dry deposition methods for TSV fabrication: a) insulation step coverage; b) barrier coverage; and c) Cu seed.

logic back-end-of-line (BEOL) interconnect, and TSVs can be considered as the 13th layer on a logic device with 12 interconnect layers. This is not a dimension that can be satisfied by alternatives such as FOWLP.

TSVs got their start in MEMS and sensor devices, which have continued to increase usage of TSVs. According to market research company Yole Développement, TSVs in the MEMS and sensors markets are expected to replace CMOS image sensors as the highest revenue generator by 2021. This trend is also evident in wafer starts (**Figure 1**).

Although many consider MEMS to be low-density TSV applications, there are, in fact, no standard dimensions for TSVs in MEMS. However, there are niche MEMS applications that do use HAR TSVs, such as gyroscopes for automotive applications. Photonics is another potentially high-volume application for HAR TSVs. Previously, conventional TSVs did not perform well as a method of interconnect because of the related stress issues, and they were going to be abandoned. However, end users pushed for a redesign using HAR TSVs. As a result, we can expect to see a photonics device in volume production in 2018.

In addition to enabling increased density, HAR TSVs address some of the remaining TSV pain points: namely, thermal and stress issues. Conventional copper-filled 5μm × 50μm TSVs experience thermal stress on account of the coefficient of thermal expansion mismatch between Cu and silicon. While the industry is aware of the issue, solutions to rectify this are still in early development stages, leaving designers constrained to larger-diameter TSVs. In some cases, the lack of solutions has been a roadblock for implementing TSV stacking. For example, stacking memory on logic using TSVs has been thus far unsuccessful, because there is nowhere for the heat to go, creating reliability issues. Therefore, the industry continues to rely on 2.5D interposer solutions, for which heat dissipation is not an issue.

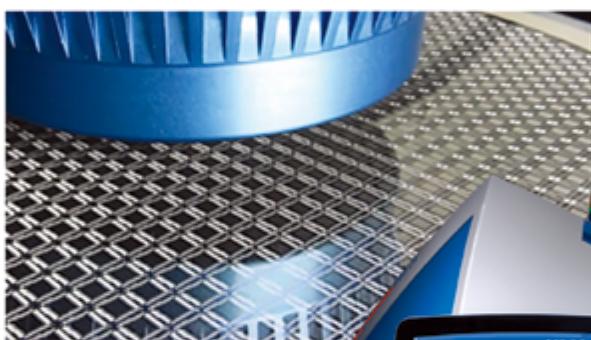
Several approaches using microfluidic technologies for hot-spot cooling are in development, but none have transitioned to a commercialized solution. These are very complicated processes, and implementing them could be a very costly solution for managing thermal dissipation with larger-dimension TSVs, and thereby could be a roadblock for further adoption.

Hybrid wafer-to-wafer bonding is also being studied for its ability to reduce inter-tier thermal resistance by reducing the standoff and using an inorganic material. Imec recently reported a 4× improvement in comparison with 40μm pitch μbump interface required for die-to-die stacking [7].

Reducing the diameter of HAR TSVs reduces the thermal stress, because the stress scales with

XM8000

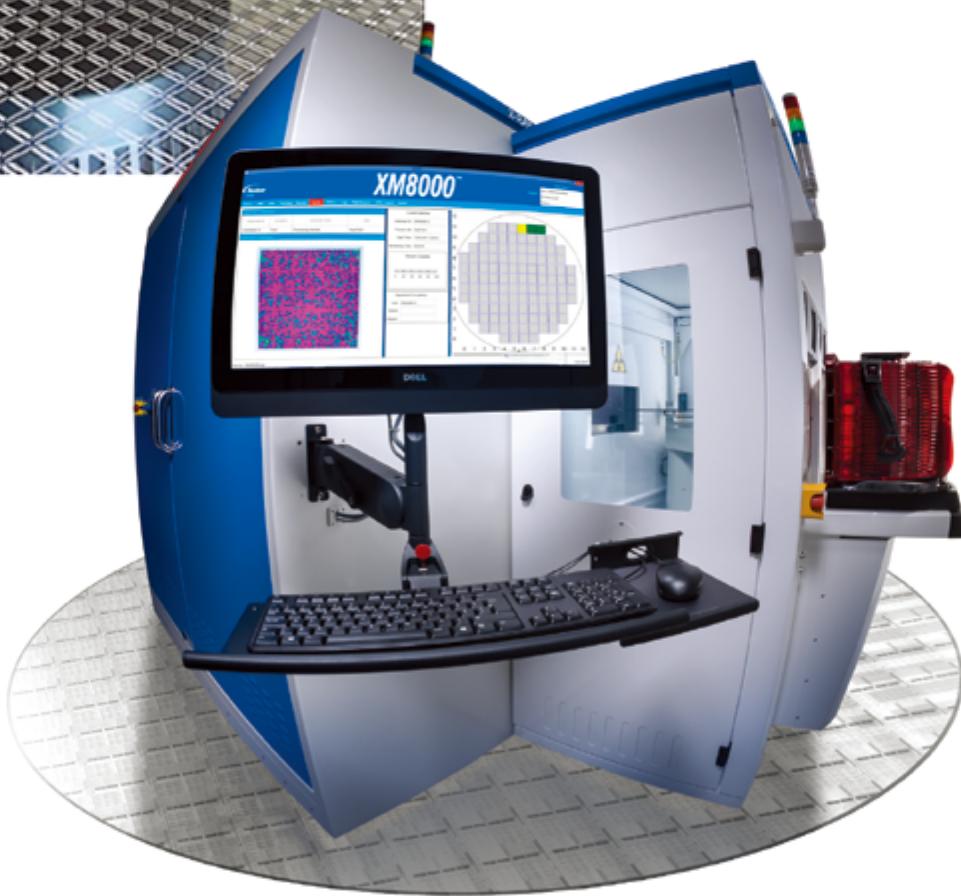
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the square of the TSV radius and elasticity module [8]. When TSVs approach submicron feature sizes, there will be far fewer thermal stress issues to address, reducing the need for thermal-management solutions.

Fabricating HAR TSVs

The advantages of HAR TSVs have not been lost on chip designers, who are beginning to integrate them into their designs, particularly for devices targeting high-performance computing technologies. Although some may call this a niche application, the expected growth in the server market will call for a significant increase in volumes.

Currently, the primary deterrent for designing in HAR TSVs is the cost of fabrication. Therefore, it is critical to adopt fabrication technologies that allow HAR TSVs to meet current and future high-density requirements at competitive costs. One of the main challenges with fabricating HAR TSVs is metallizing deeper, smaller-diameter TSVs.

Far from the $10 \times 20\mu\text{m}$ TSVs being filled today, $5 \times 50\mu\text{m}$ TSVs and smaller present a challenge for conventional dry processes, such as conventional physical vapor deposition (PVD) and ionized PVD (IPVD), because they typically have issues with poor step coverage. At $1\mu\text{m}$ diameters, the next frontier for HAR TSVs, these dry processes become virtually impossible. Using traditional front-end approaches like chemical vapor deposition (CVD) and atomic layer deposition (ALD) is slow and costly, and in some cases not technically feasible for filling the TSVs.

Alternatively, electrografting (eGTM) is a proprietary electrochemical-based process that initiates self-oriented growth of nanometric-scale thin films on conductive, as well as semiconductive surfaces, and is particularly well-suited for HAR TSVs. Electrografting and the related chemicalgrafting (cGTM) technologies (for use on nonconductive substrates) grow films with excellent step coverage compared with conventional dry deposition processes (**Figure 2**) and have been implemented as a proven process of record (POR) for metallizing TSVs at several customer sites.

How electrografting works

eG is a wet deposition process in which chemistry formulations and a charged electrode trigger chemical reactions between specific precursor molecules and the substrate surface, enabling molecular structures to

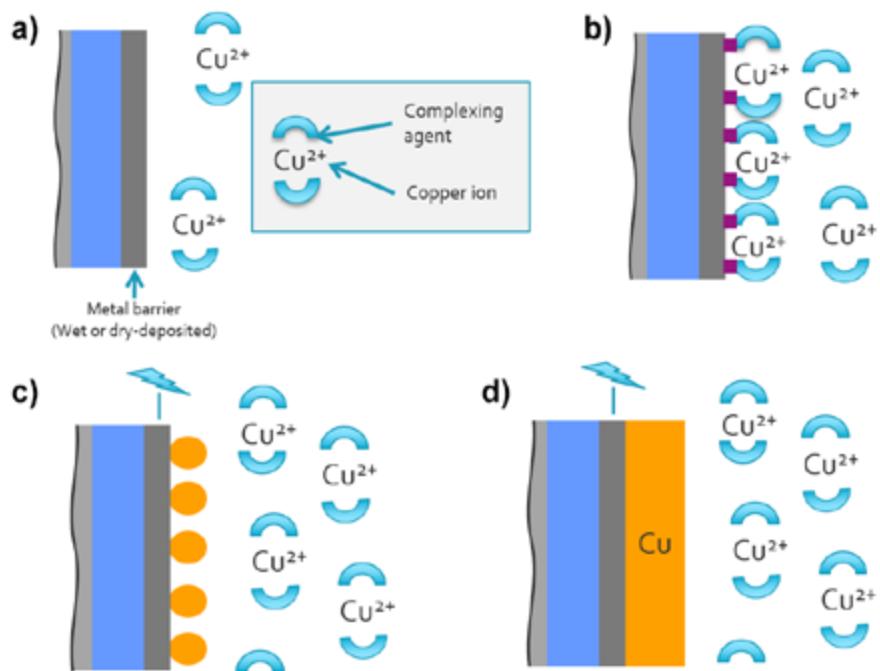


Figure 3: Deposition mechanism for eG Cu seed layer with high adhesion and nucleation density: a) Ions and complexing agent in solution before electrografting; b) Strong adsorption/high nucleation density; c) electrochemical reduction step creates chemical bonding on barrier layer; and d) Cu seed deposition.

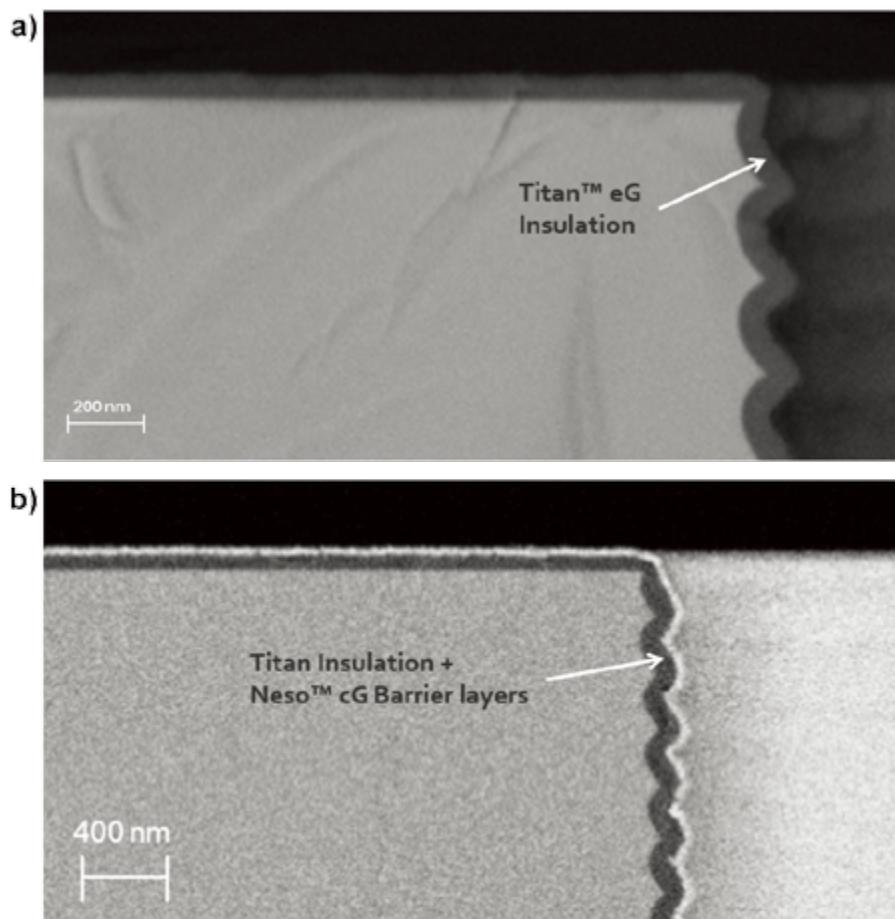


Figure 4: Highly conformal TSV insulation and barrier layers with a) eG and b) cG technologies.

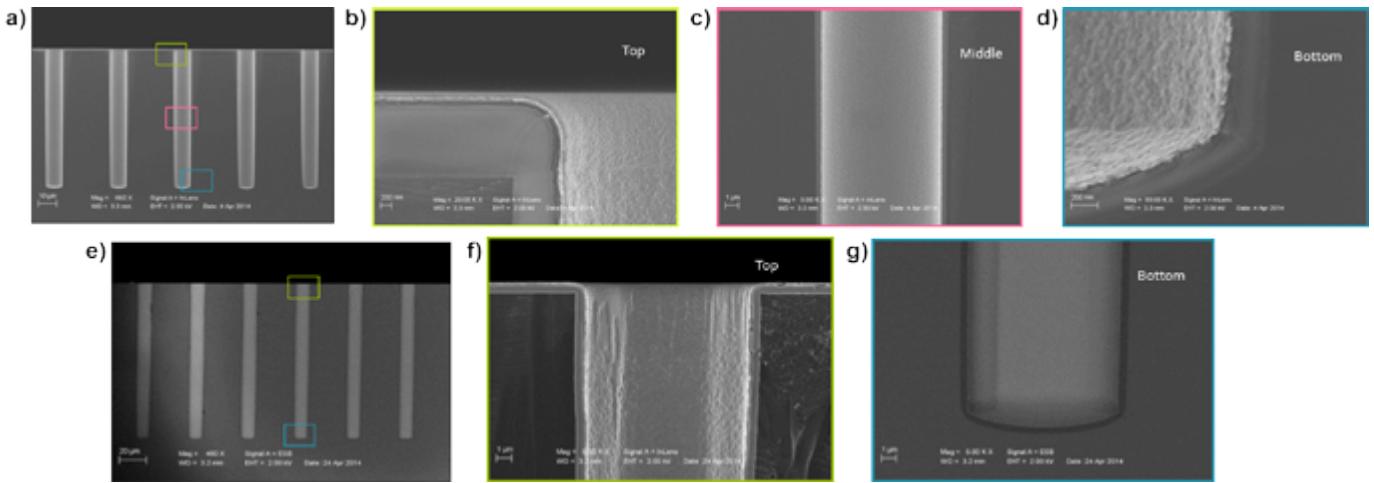


Figure 5: HAR TSVs with eG Cu seed layer on metal organic chemical vapor deposition (MOCVD) titanium nitride (TiN): a-d) 10 x 80 μm TSVs (8:1); and e-g) 10 x 120 μm TSVs (12:1). SOURCE: CEA-Leti

build up and create conformal films on virtually any surface topography.

Unlike traditional electrodeposition processes, eG requires electrode induction only during the initial grafting step to form the chemical bond between the layer and the surface. Subsequent chemical propagation steps using an organic precursor form the first primer-grafted layer and initiate the polymerization of the monomer in solution.

The first electro-induced step is crucial to forming the chemical bond between the polymer and the surface. Polymerization leads to macromolecular chains (-[A-A-A]n-B) grafting onto the first primer-grafted layer. Direct covalent bonds form between the coating and surfaces, creating highly adherent eG films with strong substrate-molecule links. Moving to TSV metallization, aveni has developed Cu diffusion barriers and Cu seed layers that use both chemicalgrafting- and electrografting-based technology (**Figure 3**).

For the barrier layer at 1 μm , ALD is possible, but it is slow and costly. With cG, a Ni-based or Co-based layer is used to create a conformal Cu diffusion barrier. A cost comparison with ALD at 5 μm shows a 40% to 60% cost reduction. eG can deposit Cu seed layers directly onto eG barriers, or onto dry Cu diffusion barriers regardless of the size of the opening or depth of the via. At 1 μm , PVD and ALD are not an option, and CVD experiences contamination and therefore reliability issues. Finally, an eG insulation layer is on aveni's long-term TSV roadmap as an alternative to replace CVD SiO₂ to reduce cost and film stress, as well as to improve conformality in deep structures (**Figure 4**) [9].

Because of eG's exceptional performance regardless of TSV diameter or depth, it is a POR at CEA-Leti for metallizing TSVs at 5 μm and below, as well as any TSV with aspect ratios >8:1 (**Figure 5**). Work is in progress at Leti for TSV barrier and insulation layers. Additionally, eG has been established by Leti as a POR for photonics applications and by DALSA for MEMS applications.

Summary

Although TSVs may remain a niche application, we anticipate that as cost-effective processes to optimize HAR TSVs become well established, they will be the answer to high-density interconnect applications, and possibly others. By 2025, heat-transfer and energy issues in servers trying to accommodate data bandwidth will create a challenge that low-density devices won't be able to address. As the server business expands, so will the need for HAR and high-density TSVs. Unlike conventional dry processes, wet eG processes can metallize any dimension and are becoming more important for TSV barrier and seed steps, particularly at the smaller dimensions required to achieve next-generation HAR TSVs.

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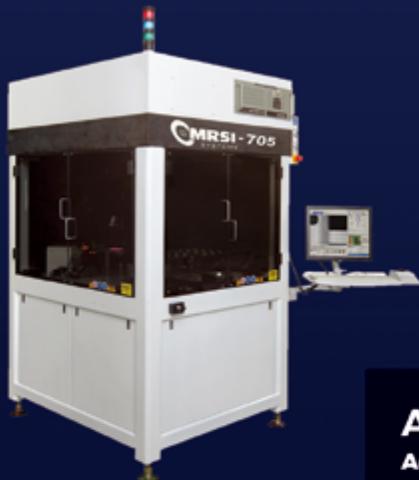
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Wafer thinning for advanced packaging applications

By Laura Mauer, John Taddei, Scott Kroeger, John Clark [Veeco Precision Surface Processing]

Diven largely by the growing need for more data, increased functionality and faster speeds, consumer electronic devices have sparked a revolution in IC design. As it becomes increasingly more expensive and technically challenging to scale down the feature sizes in semiconductor devices, Moore's law is yielding to the concept of "More than Moore," which is driving integrated functionality in smaller and thinner packages. According to market research firm Yole Développement, advanced packaging will represent 44% of all semiconductor packaging services while reaching estimated revenue of \$30 USD billion by 2020—up from \$20 USD billion in 2014 [1].

2.5D and 3D packaging have become critical to new products requiring higher performance and increased functionality in a smaller package. The use of through-silicon vias (TSVs) has been discussed as a method for stacking die to achieve vertical interconnects. However, the high costs associated with this technology have limited TSV use to a few applications such as high-bandwidth memory and logic, slowing its adoption within the industry to only those applications that exact a premium price for the superior performance of TSV architecture. Lower-cost advanced packaging concepts have been developed and are now in production for those applications that do not require ultimate performance. Recently, alternative methods for exploiting the z-direction have turned to variations of fan-out wafer-level packaging (FOWLP), which do not include TSVs.

In many of these concepts there is a need to thin the wafer to remove all of the silicon while being selective and not etching a variety of other films underneath that include oxides, nitrides and metals. In addition, there can be temporary bonding adhesives and mold compounds encapsulating the chips, which must remain undamaged. This

paper discusses the use of wet etch for wafer thinning processes needed for advanced packaging, including new FOWLP applications.

Introduction

Wafer thinning has become a critical enabling process in advanced packaging for a wide variety of device types. Beyond high-bandwidth memory and logic devices, which require thinning to enable vertical stacking with TSVs, wafer thinning is also critical for manufacturing microelectromechanical (MEMS) devices, which typically contain a sensor element, a cap and an application-specific integrated circuit (ASIC). In the case of MEMS, all three wafers must be thinned to achieve the required size reduction for packaging. CMOS image sensors employing via-last processing must also be thinned to support smaller form factors, while backside illuminated CMOS image sensors must be back-thinned

to less than 10 μm in order to open up the photosensitive sensor area for enhanced sensitivity. Thin wafers (in the 60-70 μm range) are also needed for power devices to improve their current-carrying capability, reduce on-resistance, and minimize power consumption.

In general, there are four key requirements in wafer thinning. First, the bulk of the silicon is removed by wafer grinding, which can take a typical 700-800 μm thickness wafer down to 10-50 μm . Second, it is necessary to remove the subsurface

damage and residual stress in the wafer that results from the grinding process. Otherwise, this damage can lead to die cracking during singulation. Third, the surface of the wafer must be smoothed to eliminate grind marks. Both the stress/damage removal and smoothing process are typically done using either chemical mechanical planarization (CMP), or wet etch processing. **Figure 1** illustrates the benefits of utilizing wet etch to eliminate subsurface damage and relieve stress following the grinding process. Finally, these requirements must be met in a cost-effective manner as they are all additive to the overall cost of the wafer.

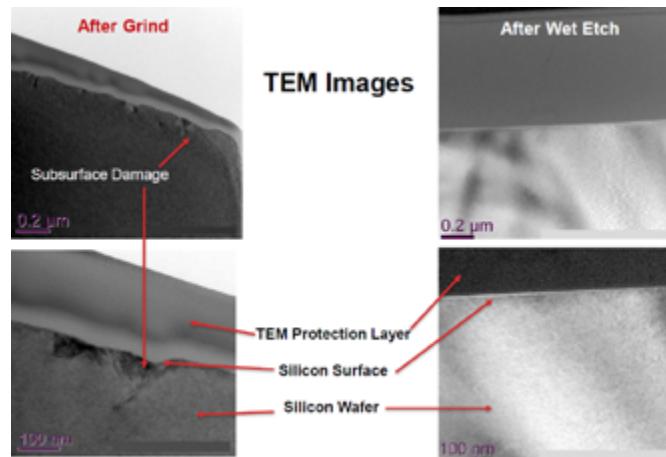


Figure 1: Wet etch relieves stress and eliminates subsurface damage.

Beyond the general needs listed above, TSV reveal and FOWLP have additional wafer thinning requirements. In 3D/TSV integration, the silicon wafer needs to be thinned to reveal the Cu TSVs so that 3D connections can be made. Fast silicon etch rate and good etch uniformity are key requirements for TSV reveal, in addition to smooth surface finishing and cost effectiveness. At the same time, the etch process must avoid any removal of the SiO₂ liner or Cu TSV. The cost and performance benefits of using a single-wafer wet etch process with adjustable

spin etching and integrated thickness measurement to reveal copper TSVs has been previously demonstrated and described [2,3]. The issues surrounding wafer thinning for FOWLP will now be explored in greater detail.

FOWLP wafer thinning requirements

To meet the needs of higher density and performance with lower cost, fan-out wafer-level packaging (FOWLP) has been introduced. This is a disruptive technology because it eliminates the traditional substrate and can be fabricated in different ways. Among the different integration schemes for FOWLP are chip-first and chip-last FOWLP. With the chip-first approach, the die is attached to a temporary or permanent material structure prior to creating the redistribution layer (RDL) that will extend from the die to the ball

grid array/land grid array (BGA/LGA) interface. With the chip-last approach, the RDL is created first, after which the die is mounted on the package. Chip-first and chip-last options offer both processing advantages and challenges. One key advantage of the chip-last approach is that it allows the RDL structures to be tested or inspected for yield loss prior to die mounting, avoiding the potential for placing good die on bad sites [4,5]. A process flow for the chip-last sequence is shown in **Figure 2**.

In many of the various FOWLP sequences there is a need to etch the silicon without affecting the other materials present in the package structure, such as Cu, Ti/TiW, SiO₂, silicon nitride (Si₃N₄), polyimide (PI) and polybenzoxazole (PBO). Another critical element of a successful process is the ability to control the profile of the

silicon etch in order to clear the silicon film evenly across the wafer regardless of overburden depth. The single-wafer wet etching techniques and advanced process control developed for TSV reveal are applicable to these structures and provide a low-cost alternative to chemical mechanical polishing (CMP) and plasma dry etch processes.

Wet etch process description

To successfully execute the silicon etch process, several characteristics must be met: the depth and profile of the excess silicon after initial bulk removal (known as overburden) need to be determined, the overburden thinning etch needs a fast sculpting etchant, and the finishing etchant needs to be selective to materials that will be exposed at the completion of the etch. In addition, the tool used to perform this sequence needs to have the appropriate metrology capability, along with properly chosen etchants in order to achieve the desired result.

The bulk of the silicon is removed by grinding. The remaining silicon may not be uniform in thickness and will therefore need to be etched in a manner that will compensate for these nonuniformities. The first step in the process is to measure the silicon thickness. In this case, Veeco's WaferEtch® Single-Wafer Wet Etch System used in this experiment has an integrated infrared (IR) sensor that conducts thickness measurements at multiple locations radially across the surface of the wafer. Next, the Profile Match Technology™ (PMT) on the system analyzes the thickness measurements to determine the optimized etch profile for each wafer. It then dynamically generates an etch recipe for each wafer. **Figure 3** shows an example of incoming wafer thickness variation and partial etch to improve uniformity of silicon. Measurements are performed before and after etch to track uniformity and etch rate for improved process control and yield improvement.

Among the predominant silicon wet etch options, potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH) provide good selectivity to oxides and metals such as Cu. However, each has tradeoffs. Whereas TMAH has a slower etch rate than KOH, KOH can cause

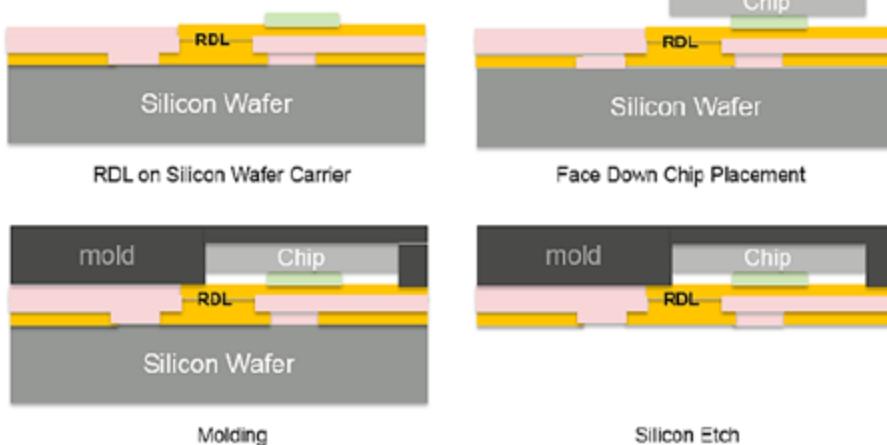


Figure 2: Chip-last FOWLP sequence.

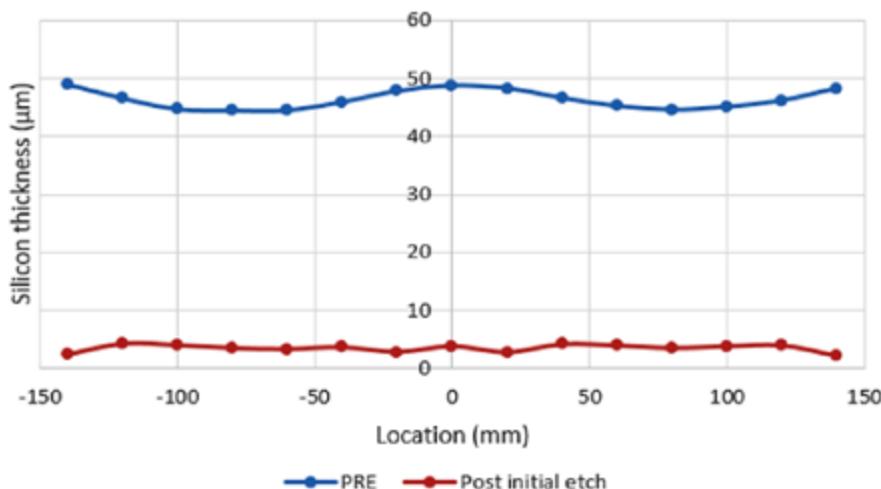
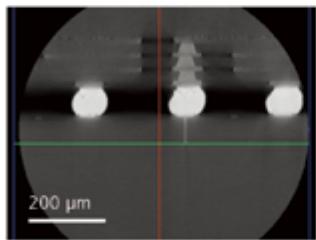


Figure 3: Silicon thickness across wafer.

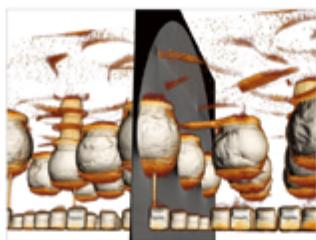
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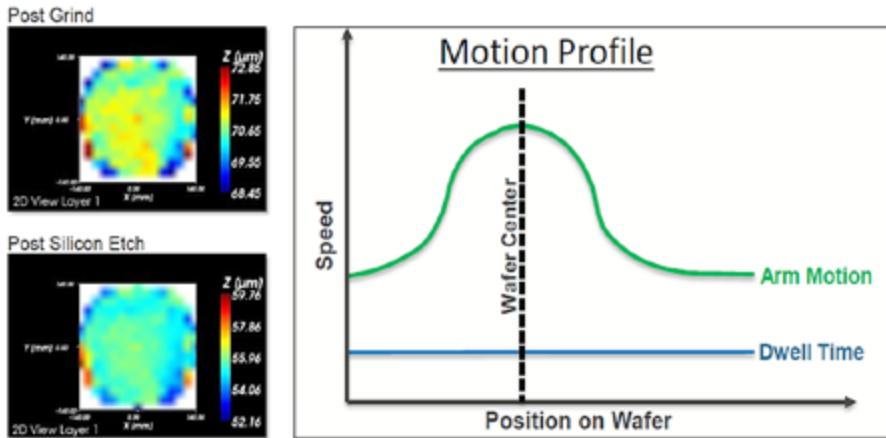


Figure 4: Hyperbolic motion profile of the single-wafer etch process, which compensates for radial non-uniformities resulting in more uniform silicon thickness.

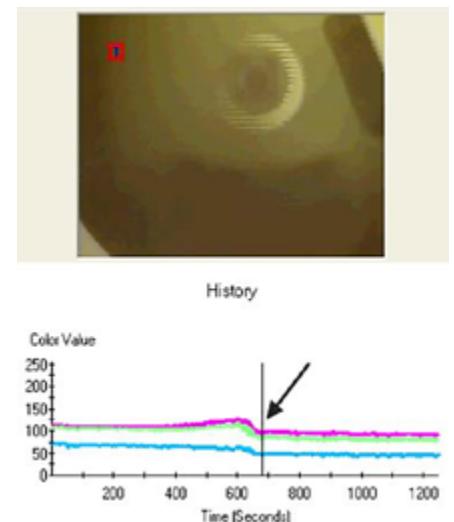


Figure 5: Endpoint detection.

Another feature of the wet etch system is the ability to stop the etch when the silicon has been removed. The single wafer wet etch approach accomplishes this through Veeco's WaferChek® process monitor, which uses a charge coupled device (CCD) camera and software built into the system to determine the end of the process by monitoring color changes in the substrate. As the wet etch system removes the silicon, the reflectivity of light from the surface of the wafer changes. A dip in the signal indicates when the silicon has been completely removed, as shown in **Figure 5**. Depending on the materials that are below the silicon and the selectivity desired, a single etchant process may also be used where the HF/nitric mixture is used for the complete etch. Examples of this include when the underlying layer is a thick oxide or pure polymer (PI or PBO).

A new etch formulation has recently been developed by SACHEM, called ST2011, which demonstrates significantly improved selectivity compared to Reveal Etch at the expense of a lower silicon etch rate, as shown in **Table 1**. Determining which selective etchant is appropriate for a given application depends upon multiple factors, including the materials present in the package, the type of structures that are being etched, and the extent to which the bulk silicon layer is nonuniform, to name just a few.

HF/Nitric Mixture*			SACHEM Reveal Etch™			SACHEM ST2011		
Material	Etch Rate (nm/min)	Selectivity to Silicon	Material	Etch Rate (nm/min)	Selectivity to Silicon	Material	Etch Rate (nm/min)	Selectivity to Silicon
Si	9000		Si	711		Si	150	
SiO ₂	50	180	SiO ₂	0.5	1422	SiO ₂	0.5	300
Si ₃ N ₄	2.7	3333	Si ₃ N ₄	0	>10000	Si ₃ N ₄	0	>10000
Cu	2400	3.8	Cu	12	59	Cu	0	>10000
Ti	750	12	Ti	0	>10000	Ti	0	>10000
TiW	144	63	TiW	1.9	374	TiW	0	>10000
PI	0	>10000	PI	5.6	95	PI	0	>10000
PBO	0	>10000	PBO	7.5	126	PBO	0	>10000

Table 1: Etch rates and selectivity of etch materials, including SACHEM Reveal Etch and new formulation, ST2011.

ionic contamination, which limits its compatibility with CMOS processes. For improved selectivity to the underlying materials, the use of a 2-step etch sequence is implemented. The first step is a fast etch using an HF/nitric mixture, as described previously, to tailor the profile [6]. This step typically takes 1-2 minutes depending on the thickness of the silicon. The amount of silicon that is etched depends on several factors. If the nonuniformity of the silicon is radial in nature, the initial etch process compensates for the thickness variation by adjusting the amount of time that the etchant is dispensed on a particular radial portion of the substrate. This “dwell time” can be controlled by adjusting various process parameters such as the tool arm scan speed, arm acceleration, and the spin speed of the chuck upon which the wafer is spinning during the etching process. **Figure 4** illustrates the hyperbolic motion profile of the etch process that can be used to achieve uniform dwell time over the entire surface of the substrate, resulting in greater uniformity post-silicon etch.

This allows the etch process to come closer to the underlying materials (typically to a silicon thickness of 2µm). If there is non-radial variation, then the amount of silicon that needs to remain for removal by the selective etchant in Step 2 will depend upon the total thickness variation (TTV). For example, if there is a 3µm TTV across the wafer, then 3+ µm worth of silicon should be left after the first step for the selective etch process. The etchant is then changed to a selective etchant. Reveal Etch provides excellent selectivity to etch silicon in the presence of other materials [7].

Table 1 shows data on the etch rates obtained for several of the materials that may be present during the etch process. With the 2-step etch sequence, the finishing etch time with the selective etchant can be kept to a minimum. This is important, as many of the selective etchants have a slow etch rate, and bonding adhesives used in the advanced packaging processes do not always hold up to exposure to the chemistries involved for long periods.

Summary

Wafer thinning is essential to supporting a variety of advanced semiconductor package types, including 2.5D/3D with TSVs, as well as FOWLP. A single-wafer wet etching technique initially developed for TSV reveal has been demonstrated to address the wafer thinning needs for FOWLP and provide a low-cost alternative to CMP and plasma dry etch processes. It provides high selectivity of silicon etch relative to the materials that are present in the package structure. Continuous improvements in etchant formulations are underway through close collaborations between process equipment vendors and materials suppliers.

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Optimization of die attach to surface-enhanced lead frames for MSL-1 performance of QFN packages (part 2)

By Dan Hart [MacDermid Enthone Electronics Solutions] and Senthil Kanagavel [Alpha Advanced Materials]

This article is part 2 of a two-part series. Part 1 focused on a preliminary assessment of the materials for surface compatibility, fbs.advantageinc.com/chipscale/mar-apr_2017/#36

Quad flat no-leads (QFN) semiconductor packages represent one of the steadiest growing types of chip carriers, and they are predicted to continue growing as original equipment manufacturers (OEMs) strive to put more signal handling into a smaller space. Owing to their low profile, condensed form factor, high I/O and high thermal dissipation, they are popular choices for chip set consolidation, miniaturization and chips with high power density, especially for the automotive and RF markets. As with any package, reliability is critical, and due to their widespread acceptance, OEMs, integrated device manufacturers (IDMs) and outsourced assembly and test suppliers (OSATS) demand continued improvements in reliability of QFNs.

Chemical processes that treat the surface of copper lead frames, to enhance mold compound adhesion, and reduce delamination in chip packages, deliver improved reliability in QFNs. These chemical processes result in micro-roughening of the copper surfaces, while concurrently depositing a thermally robust film that enhances the chemical bond between the epoxy encapsulants and the lead frame surface. Typically, this type of process can reliably provide JEDEC MSL-1 performance.

While this chemical pre-treatment process provides improved performance with respect to delamination, it can create other challenges for the lead frame packager. Increased surface roughness magnifies the tendency for die attach adhesives to bleed (epoxy bleed out or EBO), causing the silver-filled adhesive to separate and negatively impact package quality and reliability. Additionally, any epoxy resin that bleeds onto the lead frame surface can interfere with other downstream processes, such as down-bonding or mold compound adhesion.

Anti-bleed or anti-EBO coatings have been developed to control the amount of bleed, but different adhesives can have different physical properties (surface tension, percent solids, viscosity, etc.) that impact the interaction with the anti-bleed coatings. Consequently, the selection of die attach adhesive can be critical to package performance. This article examines the appropriate methods for optimizing both die attach adhesive chemistry with state-of-the-art lead frame technology.

Performance attributes for achieving MSL-1

In part 1 of this two-part series, we saw the effects of the various factors that could contribute to the MSL-1 performance of the package. The EBO of the die attach was one of the key contributors. The other contributor was the adhesion strength of the die attach and epoxy mold compound to the lead frame and die surfaces. The ATROX® die attach adhesives showed better adhesion strength with cohesive failures in the bulk of the die attach, especially at higher temperatures such as 260°C. This confirms that the material has capability to withstand the reflow process after MSL-1 exposure and not compromise the adhesion strength at the die attach interfaces.

In this article, we will evaluate the different die attach adhesives in an assembled package and test them using MSL-1 preconditioning at 85°C and 85% relative humidity for 168 hours followed by three reflow passes at 260°C. The experiment layout in **Table 1** describes the testing plan.

Leg #	Lead frame	Roughening	Anti-Bleed Concentration (%)	Die Attach		
				ATROX® DA1	ATROX® DA2	Benchmark
1	Cu QFN	PackageBond HT	0.50%	X		
2					X	
3						X
4			0.75%	X		
5					X	
6						X
7			5%	X		
8					X	
9						X
10			7.50%	X		
11					X	
12						X
13				X		
14					X	
15						X
16			0%	X		
17					X	
18		Standard – No Roughening				X

Table 1: DOE layout for MSL-1 evaluation testing.

Properties	ATROX® DA1	ATROX® DA2	Benchmark
Chemistry	Non-Epoxy	Non-Epoxy	Epoxy
Weight loss during cure	0.8%	1-35%	5.3%
Cure profile	175C/60min	175C/60min	175C/60min
Volume resistance	0.00008 Ohm-cm	0.0002 Ohm-cm	0.0001 Ohm-cm

Table 2: Die attach adhesive properties comparison.

Experiments

The alloy surfaces were treated with MacDermid Enthone's standard PackageBond HT process – acid cleaner, mild microetch, PackageBond Predip, PackageBond HT coating, and alkaline Postdip. The etch rate was maintained in the 1.50-2.00µm/min range to maintain a consistent surface morphology. The surfaces were then treated with the anti-bleed coating as shown in **Table 1**. Two ATROX® die attach adhesive products (DA1 and DA2), described in **Table 2**, were evaluated, along with an industry standard die attach product as a benchmark. The die attach adhesives were dispensed followed by die placement and curing. The cured parts were then molded using an industry standard mold compound that is rated to survive MSL-1 performance.

Table 2 briefly describes the die attach adhesives that were tested for this evaluation. After assembly, the devices then followed

the standard JEDEC testing procedure for preconditioning of non-hermetic surface mount devices prior to reliability testing as per JEDEC standard JESD22-A113D. **Figure 1** shows the scanning acoustic tomography (SAT) scans of the devices prior to preconditioning treatment.

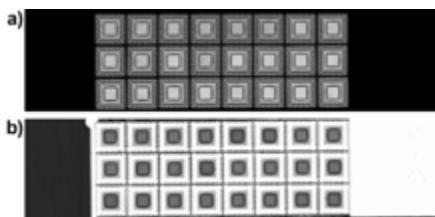


Figure 1: a) C-Scan before MSL-1; b) Through scan before MSL-1.

All parts evaluated with different die attach and anti-bleed treatments were defect-free after SAT inspection prior to MSL-1 preconditioning. Within thirty minutes after preconditioning, the parts were subjected to three sequential reflow passes at 260°C. The reflow profile is shown in **Figure 2**. After the reflows, the units were again examined by SAT. The

delamination results before and after MSL-1 testing are presented in **Table 3**.

Delamination is observed on all experimental legs involving the non-roughened lead frames. This confirms that the roughening treatment is required for MSL-1 performance. DA1 shows a very

wide process window with respect to anti-bleed concentration, which ranges from 0.5–7.5% concentration. DA2 exhibits a narrower window, but within the ranges examined, still possesses a 2.5% (or larger) process window, while the industry standard adhesive doesn't perform well at all anti-bleed concentrations.

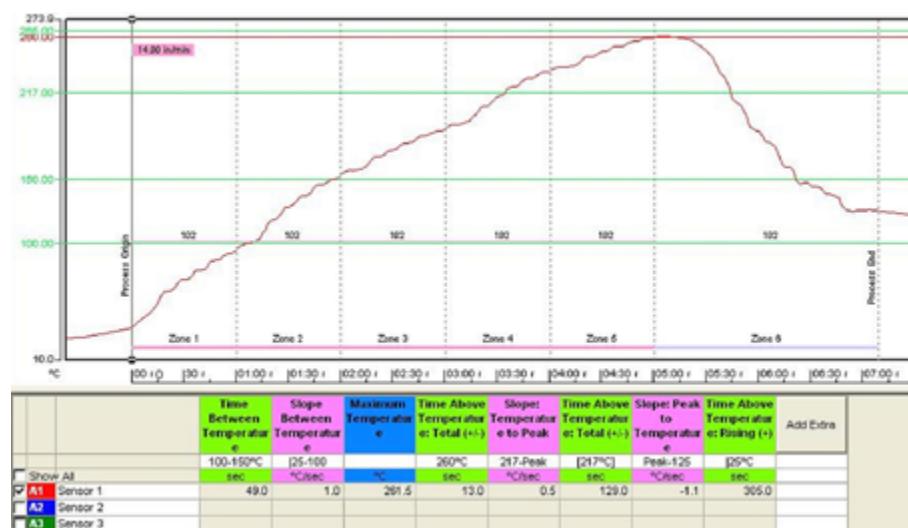


Figure 2: 260°C peak temperature reflow profile.



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DOE LAYOUT FOR MSL-1 Evaluation				MSL-1 performance (Failures/Units)				
Leg #	Die Attach	Lead frame	Roughening	Anti-EBO Concentration (%)	Before MSL-1		After MSL-1	
					C-Scan	Through scan	C-Scan	Through scan
1	DA1	Cu QFN PackageBond HT	Standard - No Roughening	0.50%	0/24	0/24	0/24	0/24
2	DA2			0.50%	0/24	0/24	2/24	14/24
3	Benchmark			0.75%	0/24	0/24	2/24	8/24
4	DA1			0.75%	0/24	0/24	0/24	0/24
5	DA2			5%	0/24	0/24	8/24	16/24
6	Benchmark			5%	0/24	0/24	2/24	6/24
7	DA1			7.50%	0/24	0/24	0/24	0/24
8	DA2			7.50%	0/24	0/24	19/24	24/24
9	Benchmark			0%	0/24	0/24	6/24	6/24
10	DA1			0%	0/24	0/24	16/24	24/24
11	DA2			0%	0/24	0/24	2/24	24/24
12	Benchmark			0%	0/24	0/24	6/24	10/24
13	DA1			0%	0/24	0/24	12/24	12/24
14	DA2			0%	0/24	0/24	17/24	24/24
15	Benchmark			0%	0/24	0/24	17/24	24/24
16	DA1			0%	0/24	0/24	17/24	24/24
17	DA2			0%	0/24	0/24	17/24	24/24
18	Benchmark			0%	0/24	0/24	17/24	24/24

Table 3: SAT analysis results of devices after MSL-1 + 3X reflow at 260°C.

The results show that the ATROX® die attach adhesives outperform the industry standard die attach adhesive on the PackageBond treated lead frames. The reasons for this difference in performance are attributed to the following:

1. Surface roughening treatment to improve adhesion of both epoxy mold compound and die attach adhesive.
2. Reduction of EBO on the roughened surface by the anti-bleed treatment so that the adhesive composition remains consistent and adhesion of epoxy mold compound to the die pad is not affected by cured epoxy bleed from the die attach adhesive.
3. The compatibility of the die attach adhesives with the surface energy of the lead frames resulting from the application of the anti-bleed treatment.

SAT images of ATROX® die attach from Leg 7 after reflow are presented in **Figure 3**. They confirm that there is no delamination after MSL-1 testing with the ATROX® die attach adhesives. **Figure 4** shows microsections of the unit assembled with the ATROX® die attach adhesive, and verifies that no delamination is observed. The bond line is consistent and the wetting on the roughened surface is good.

Figure 5 from leg 18 shows the C-scan and Through scan, respectively, for the industry standard die attach adhesive. These SAT scans show delamination after reflow. Delamination occurs at the die attach/lead frame interface, within the die attach adhesive, and at the epoxy mold compound/lead frame interface.

Figure 6 shows microsections of the unit assembled with the industry standard die attach adhesive, and illustrates the delamination observed. **Figure 7** from leg 9 is a SAT analysis image that illustrates delamination with the industry standard die attach adhesive that occurs at the surface of the treated lead frame. **Figure 8** shows microsections of the unit assembled with the industry standard adhesive, and illustrates that the observed defect was caused by epoxy mold compound delamination that propagated into the die attach.

Results for MSL-1 performance

Delamination is shown to be related to both die attach adhesive and epoxy mold compound adhesion at the lead frame interface. The roughening treatment provides improved adhesion performance after MSL-1 testing for both epoxy mold compound and die attach adhesive. However, even roughening doesn't help to eliminate all delamination unless the anti-bleed coating is applied. Part 1 of this series demonstrated that very high EBO is detected on roughened surfaces without the anti-bleed coating. The current evaluation reveals that delamination can occur at the lead frame interfaces, but also indicates that delamination of mold compound from the lead frame can generate a crack that would propagate into the cured die attach adhesive. These delamination sources are eliminated by roughening the lead frame and eliminating EBO. So, the recommended route to MSL-1 performance is to provide a roughened lead frame surface and a die attach adhesive that wets this roughened surface without generating EBO. To do this successfully, the anti-EBO coating and die attach adhesives need to be

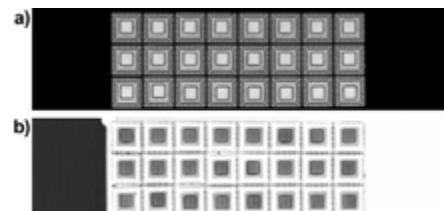


Figure 3: a) C-SAM shows no delamination after MSL-1; b) Through scan shows no delamination after MSL-1.

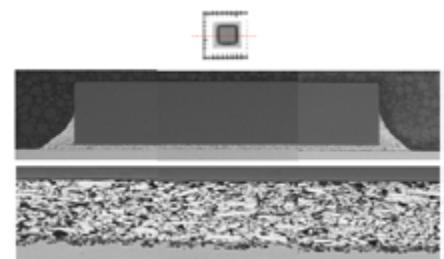


Figure 4: Microsections of a unit assembled with ATROX® die attach adhesive.

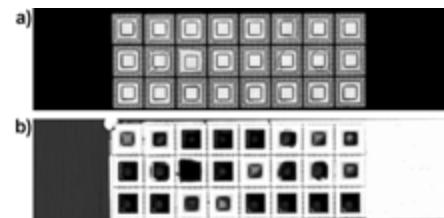


Figure 5: a) C-SAM shows delamination after MSL-1; and b) Through scan also shows delamination after MSL-1.

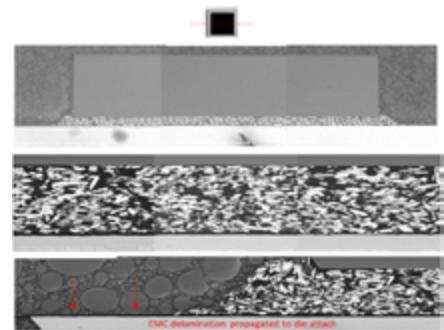


Figure 6: Microsection images of a unit assembled with an industry standard die attach: a) (top panel) Microsection image of a unit assembled with an industry standard die attach; b) (middle panel) Magnified image of the unit showing delamination; and c) (bottom panel) Epoxy mold compound delamination propagated into die attach.

compatible. This poses another issue. Most packaging houses prefer the lead frame manufacturer to provide the anti-EBO coating on the lead frames that they supply.

While the solution noted above is easy, it is not always the best unless both the packaging house and lead frame producer

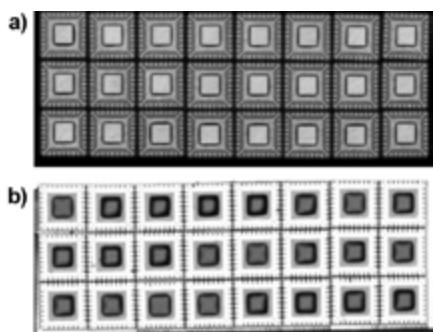


Figure 7: a) C-SAM shows no delamination after MSL-1; b) Through scan shows delamination after MSL-1.

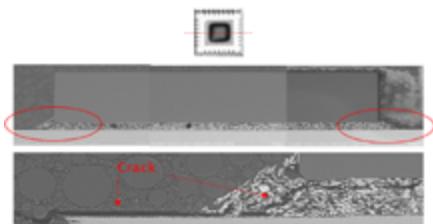


Figure 8: Delamination on lead frame paddle area propagating into the die attach layer.

agree on die attach adhesive and anti-EBO treatment. In general, lead frame companies desire an anti-EBO treatment that will work with all die attach adhesives. The work presented here illustrates the difficulty of achieving MSL-1 performance without considering the anti-bleed and die attach adhesive compatibility. Perhaps a more effective solution would be for the packaging house to install the anti-bleed application so that they can be matched to the die attach adhesive(s) that are used in-house.

Summary

The key finding from this study was that the use of roughening processes is critical for enhancing adhesion strength to lead frame surfaces, however, what is also critical is to choose a compatible anti-bleed material that reduces/eliminates EBO on the lead frame surface and doesn't interfere with adhesion of mold compound or die attach adhesive to lead frame surface. This combination of treatments maintains the joint integrity during high stress such as MSL-1 performance followed by a 260°C reflow process. The two ATROX® die attach adhesives, although different in properties, are shown to be compatible with the MacDermid Enthone PackageBond HT roughening and PackageBond Anti-Bleed surface treatments, which lead to high MSL reliability.

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Advanced process control solutions for fan-out wafer-level packaging

By Dario Alliata, Philippe Gastaldo, Yann Guillou, Gilles Fresquet [[UnitySCJ](#)] and Jean-Philippe Piel, Sylvain Petitgrand [[Fogale Nanotech](#)]

With the increase of costs, delays and complexity at the most advanced front-end silicon technology nodes, advanced packaging has become a key differentiator for achieving next-generation requirements, and thereby continued sustainability in the semiconductor industry. Within the advanced packaging realm, fan-out wafer-level packaging (FOWLP) is gaining momentum due to its high integration, extreme flexibility, performance enablement and cost advantages, compared with more conventional assembly technologies.

Despite the wide adoption of FOWLP during the last few years, there are several challenges remaining about the industrialization of the process. For example, regardless of the FOWLP methodology used, the epoxy molding compound (EMC) is still a potential source of issues, with challenges in total thickness variation (TTV) management, package warpage and die shift. From a pure metrology perspective, the EMC thickness measurement may also be a challenge, because the epoxy material typically becomes opaque above a certain thickness and cannot be measured in the visible or infrared domains by conventional optical metrology techniques.

In this article, we introduce the various metrology technologies used to control the FOWLP process and review the main metrology measurements required during high-volume manufacturing. Additionally, we explore the advantages of using an in-line, integrated 2D/3D metrology solution to characterize the FOWLP fabrication process using the chip-first/face-down approach.

FOWLP manufacturing flow and metrology considerations

In the classical embedded wafer-level ball grid array (eWLB) approach [1], the silicon chips are probed, thinned and singulated during the FOWLP process. These chips are then placed on an adhesive tape that sits on a temporary carrier using standard pick-and-

place equipment. The packaging is completed through the following main process steps: wafer molding, carrier removal, passivation/redistribution layers (RDLs), balling and dicing. Each step presents some challenges, and metrology solutions are required to minimize their impact on the final yield.

Tape lamination and pick-and-place

When the tape is laminated onto the temporary carrier, keeping the TTV of the adhesive layer under control minimizes coplanarity issues when the known-good die (KGD) are picked and placed. **Figure 1** shows the TTV for an adhesive layer on a 300mm Si carrier. The measurement was performed by mapping the whole wafer area with 127 points by spectral interferometry in transmission mode.

One important performance issue for FOWLP is determined by die placement on the substrate. The two operations that most affect die location error are the die placement operation and die migration during the compression molding process. The first contribution is essentially coming from the precision/repeatability of the pick-and-place equipment and by the method of operation used. If a unique die type is positioned over the carrier, the single-gantry mode is typically used. To combine different functionalities (e.g., die types) into the same final package, multiple gantries must be applied. The single-gantry mode typically would affect only the position of each die with a constant offset, whereas multiple-gantry mode would introduce potentially multiple offsets [3]. Line scan 2D/3D confocal chromatic technology was used to verify the X, Y position and tilt of each die. **Figure 2** shows the 3D rendering view on a carrier populated with a single family of dies by using the 4See Series inspection platform. (Note: The 4See Series used 2D/3D line-scan confocal chromatic technology to inspect the whole wafer surface for defectivity and metrology.) Controlling the X/Y position of the dies and retrofitting the information to the

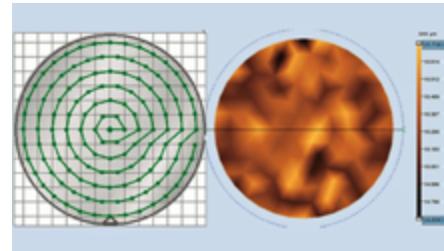


Figure 1: a) (left) Sequence of measured points; and (right) 2D wafer map of adhesive layer thickness distribution.

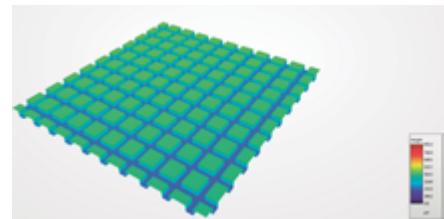


Figure 2: 3D view of KGDs sitting on the carrier.

pick-and-place equipment is demonstrated to be one of the most efficient solutions to recover the drift in the process, allowing for the wafer to be reworked if the die position is not within the expected tolerance.

Molding

Molding KGDs with EMC is one of the most challenging fabrication steps in FOWLP because it can impact the coplanarity and planar position of the embedded dies, as well as the warpage of the reconstructed wafer once the carrier is removed. Die shift affects the alignment of the RDL on the die pad and challenges the photolithography process, while an excess in warpage prevents the possibility of handling the reconstructed wafer with the fabrication equipment. Both potential hazards are caused by thermal expansion of the carrier and mold shrinkage upon cooling. Typically, the impact on those parameters can be anticipated by controlling the thickness and TTV of the EMC layer across the wafer, as well as its surface roughness. EMC thickness measurement is not trivial because the material properties

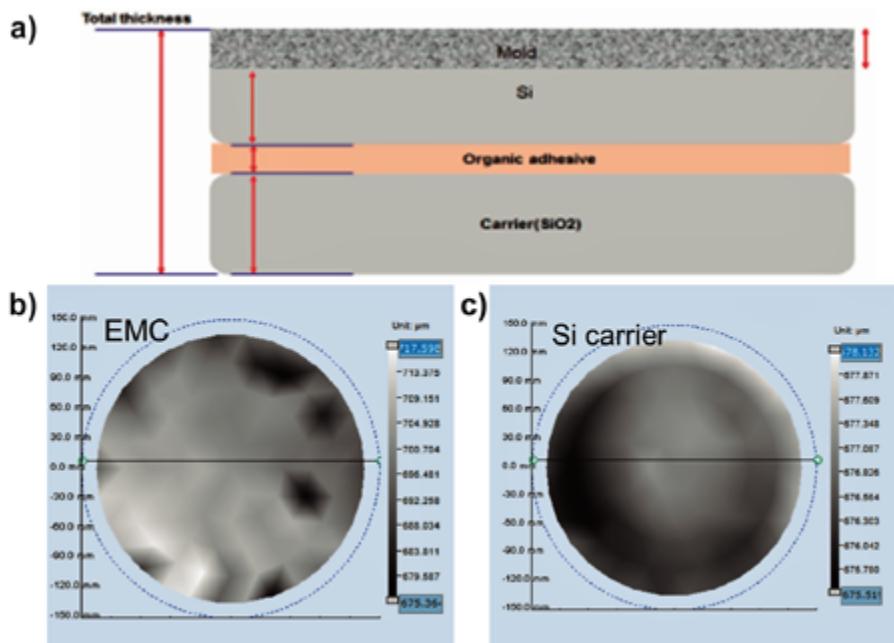


Figure 3: a) (top) Sketch of an eWLB wafer on a carrier stack; and thickness wafer maps of b) EMC, and c) a Si carrier.

change with the thickness and the EMC becomes non-transparent to optical techniques either in visible or infrared (IR)

domains. Typically, if it's thinner than 100μm, the EMC thickness can still be measured by interferometry in transparency mode. When

it's thicker, different methods must be applied. Moreover, the wafer warpage and its local roughness impact the capability to collect the light reflected from the wafer compound surface and potentially prevent the thickness measurement. To overcome this problem, a dual low-coherent IR sensor with high numerical aperture and real time auto-focus is used. The total stack thickness is estimated by measuring the air gap between the two faces of the bonded wafer and the top and bottom interferometric probes; the thickness of each transparent layer in transmission is measured simultaneously. In this way, the thickness of the EMC layer is estimated by subtracting the contribution of the Si and adhesive layers from the total thickness of the wafer.

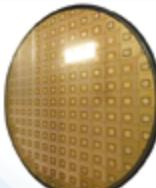
An example is shown in **Figure 3**, where the thickness of the top EMC, the embedded Si device (KGD) and the Si carrier wafer were measured simultaneously using the TMap Series metrology platform. (Note: The TMap Series is a metrology platform equipped with three main technologies to measure distances and thicknesses in wafers: low coherence infrared interferometry, confocal chromatic technique and spectral domain

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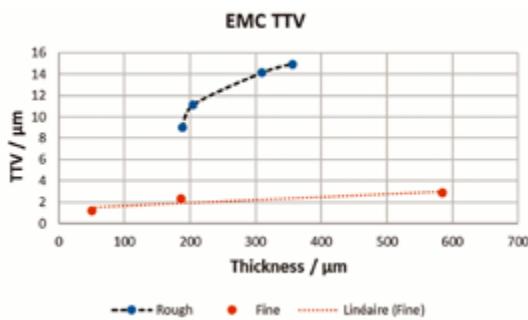


Figure 4: Effect of the grinding process on TTV vs EMC thickness.

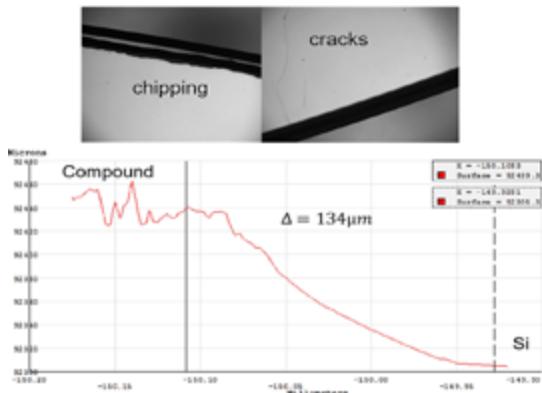


Figure 5: Near-IR images showing defects of interest: a) chipping, b) cracks; and c) line-scan across the wafer edge.

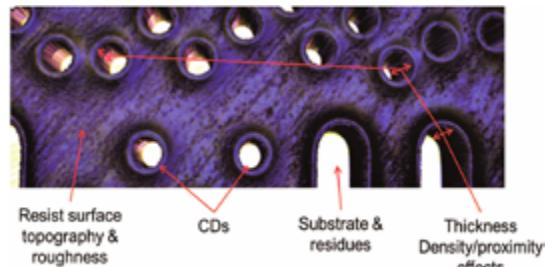


Figure 6: 3D rendering of resist with opening after the photolithography process step.

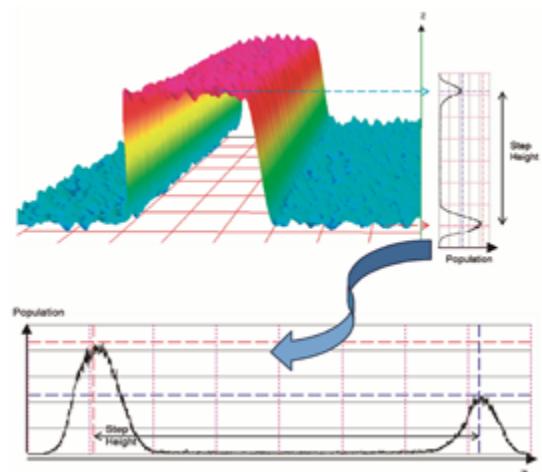


Figure 7: RDL measurement of height and roughness.

reflectometry [3].) The information on TTV can be fit-forwarded to the grinding equipment to fine-tune the thinning process used to remove the over-molded material.

Grinding

The same approach (i.e., the TMap Series) was used to investigate the effect of the grinding process on the EMC thinning step, which is required to avoid over-molding and reduces the final package. The EMC layer thickness of a set of bonded wafers that were processed with two different grinding methods was measured: one more aggressive (rough grinding) and one more gentle (fine grinding). In addition, process time was varied while treating the two sets of samples. **Figure 4** shows the dependence of the TTV across the wafer with the increasing thickness of the EMC for the two sequences of process conditions applied. The TTV increases with the thickness non-linearly for the rough process, whereas TTV increases linearly for the fine grinding process. Optimizing the process condition in the grinding recipe is a key requirement to finding the right compromise between the grinding process speed and final surface condition.

For the purposes of this work, by using the imaging capability of the system, we could inspect the edge of the EMC/Si wafer and catch defects of interest, such as chipping and cracks that may propagate from the edge to the wafer center (**Figure 5**). This is essential to prevent wafer breakage during the remaining processing steps and guarantee good sealing of the final package after dicing. Finally, the edge-trimming symmetry was controlled using a confocal chromatic sensor, as shown in **Figure 5**. By measuring the edge profile across at least four different directions, the eccentricity of the molding process was estimated from quantification of the length of the bevel area.

Redistribution layers (RDLs)

Once the temporary carrier is removed, the reconstructed wafer can be processed with thin-film technologies to fan out the RDL. Once the photoresist is deposited and exposed to open the expected structures, characterization of the resist thickness, lateral critical dimension (CD), depth and aperture volumes are mandatory to avoid over/under-deposition of metal during the plating process. In-line metrology control is required to reject and reprocess the wafers with too-thick resist or CD of opening out of specification. NST Series full-field White Light interferometry was used to reconstruct the resist/opening top layer after photolithography. (Note: The NST Series uses the full-field white light interferometry as a way to scan the sample surface, either in vertical scan mode or phase shift mode per the dynamic vertical range and resolution required.) On account of the sub-micron lateral resolution combined with a nanometric sensitivity in height, the volume for each opening through the photoresist layer can be determined. An example of results on exposed photoresist is shown in **Figure 6**. Here, the effect of opening density and geometry on the photoresist topography after the reveal operation can be investigated. Surface roughness can be determined with nanometer resolution, both for the resist surface and for the substrate in the opening zones. Proximity effects on the opening can be investigated as a function of density.

Controlling the CD of the RDL in width and height, with concomitant estimation of the local roughness, is the proper way to anticipate issues at the interconnectivity level when proceeding with RDL plating. In **Figure 7**, an RDL surface was imaged in 3D at nanometer resolution using interferogram processing techniques to simultaneously measure the roughness on top and bottom of the RDL, as well as measuring the CDs (height, top/bottom width), and to estimate the slope of the two sides.

Characterizing the RDL at the nanometer level is increasingly necessary with the length/space parameters approaching 1 μm. The presence of a transparent layer like the polyimide (PI) that is used to passivate the device surface is another typical challenge for 3D surface metrology. Laser and white light triangulation techniques are not

sensitive to the presence of the polyimide, so they lack accuracy when estimating RDL height from the top of the passivation. Point sensors based on interferometry are limited in spot size and will not be effective for measuring the PI thickness on a small RDL. Alternatively, full-field interferometry allows the simultaneous 3D reconstruction of the RDL area even with the presence of passivation at sub-micrometer lateral resolution. Therefore, measuring the PI thickness on RDL with 2 μ m l/s and below is still possible.

Summary

FOWLP requires advanced metrology solutions to characterize and control the fabrication process chain. Due to the variety of materials used and metrology requirements, flexible platforms equipped with multiple technologies are mandatory to cover the required capability in thickness/distance measurement from millimeter down to the nanometer range. In this article, various metrology measurements performed during the FOWLP manufacturing process flow were reviewed, beginning with the adhesive layer verification and continuing with the in-line process control of the die location accuracy after the pick-and-place operation. The effect of the grinding process on the EMC material to control the fabrication of the reconstructed wafer was studied. Additionally, the TTV of the EMC material across the wafer was characterized, and its intra-wafer dispersion and wafer-to-wafer variation was quantified. Finally, dimensional control at sub-micron scale was achieved on the RDL using full-field interferometry. From the work performed, it is clear that in-line defectivity/metrology characterization reduces the time to development and lowers the total cost of the device fabrication process in FOWLP.

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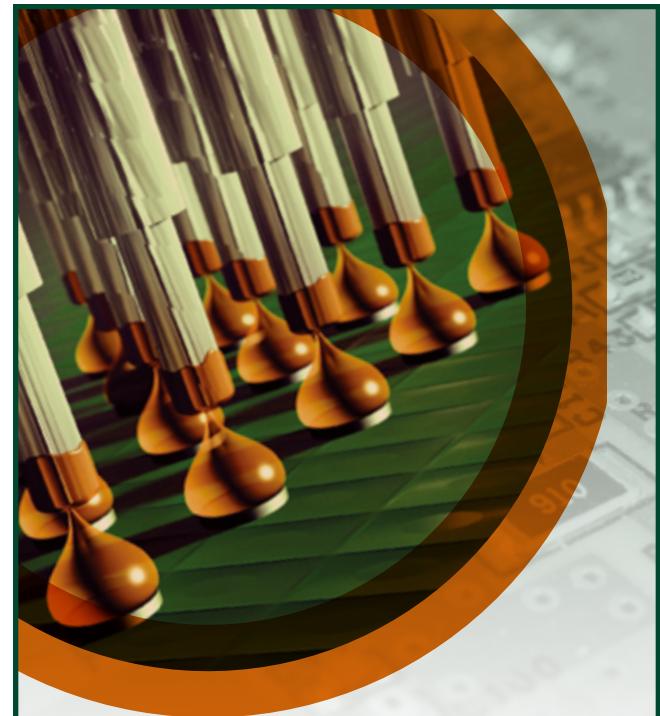
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High-volume manufacturing (HVM) of chip-on-submount (CoS): challenges and solutions

By Daniel F. Crowley, Peter Cronin [MRSI Systems]

The demand for data and bandwidth continues to expand, resulting in the requirement for high-volume manufacturing (HVM) of photonics devices at unprecedented levels. This expansion, with double-digit growth rates, is driven by data consumption from cloud computing, web and mobile-based applications and storage through hyperscale data centers (e.g., Facebook, Google, Microsoft, Amazon). The data bandwidth demand from individual consumers and enterprises creates the need to upgrade long haul networks, metropolitan communication systems, and data centers.

One key photonic device component requiring HVM is the chip-on-submount (CoS). CoS devices present some unique manufacturing challenges. Application-specific die bonders have evolved over decades to address the current manufacturing demands of CoS. This article reviews the required features of a successful HVM die bonder of CoS devices.

The basics of a chip-on-submount (CoS)

The volume for photonic devices is increasing for the reasons mentioned above. Among the critical building blocks for photonic devices, the CoS devices are the core in terms of performance, reliability and required volume.

In fiber optic transmission, the laser diode (LD) CoS, also referred to as a chip-on-carrier (CoC), is the starting point of light generation and transmission, and the photodetector (PD) CoS is the ending point of the light, which is received and translated into an electronic signal. It is quite typical for a 100Gbps fiber transmission to have four sets of LD and PD CoS at a rate of 25Gbps each. Some have 10 sets at a rate of 10Gbps each. The quantity of LD CoS and PD CoS can therefore be four to ten times the quantity of final optical modules.

A common configuration of a LD CoS, includes a eutectically-bonded LD and a back facet monitoring detector, both mounted on the same submount. The quality of the joint between the LD or PD chip to the submount is one of the most critical factors for device

long-term reliability. Eutectic bonding is used for a highly thermally efficient interconnect with long-term reliability. The LD CoS may include additional components, such as thermistors, capacitors and driver chips. The PD CoS typically includes a PD and may also include additional components, such as a transimpedance amplifier (TIA), and in some cases, a thermistor for temperature control. In subsequent process steps the completed CoS may be mounted onto a thermoelectric cooler (TEC) packaged in a "gold box" or TO-can package. In order to achieve the eutectic bonding of these multiple parts within the package, a temperature hierarchy of eutectic solder is frequently required. When using a

TO-can package, it is common that the LD and the monitoring detector are each eutectically bonded on separate CoS and then mounted in a vertical plane just offset from 90 degrees of each other (Figure 1).

Die bonder requirements for HVM of CoS

The majority of die bonders offered today have evolved for generic semiconductor packaging applications. While these semiconductor die bonders may be well-suited for the die bonding requirements of semiconductor packages, they lack the specific unique features required for successful HVM of CoS.

Another approach to solving successful HVM of CoS is to use dedicated highly mechanical die bonders. While these dedicated mechanical solutions can offer high speeds, they often do so by sacrificing flexibility, reliability and machine delivery times. Any changes in the CoS design or type of the devices being assembled result in expensive and time consuming retooling costs.

The best solution is an application-specific specialized die bonder for HVM of CoS that is able to deliver high speeds while maintaining

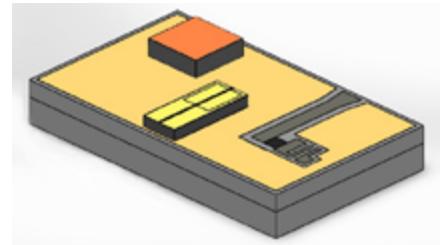


Figure 1: LD CoS.



Figure 2: Eutectic bonding stage.

flexibility. This is best achieved with a standard, flexible, high-speed system that can be easily reprogrammed for new device designs and types. This approach results in shorter delivery times for standardized machines. Short machine delivery times are important to allow customers to scale production rapidly. A HVM CoS die bonder should include many parallel processing features to maximize throughput. The following is a summary of the unique features of a CoS-specific HVM die bonder.

Eutectic bonding optimized for CoS. Because of high power requirements, small component sizes, and the need for the elimination of materials that outgas, many components are attached with a eutectic die bonding process. The CoS substrate sizes are small, typically less than a few millimeters. A small form factor eutectic stage is needed to provide ultra-fast temperature ramping, and ultra-fast cooling cycles. A closed-loop, low-mass, high-power, pulsed heated eutectic stage is required. Stable temperature control and cover gas flow must be optimized throughout the eutectic process. Additionally, the eutectic station must be fully programmable, tailoring the process for a specific bonding recipe. Faster speeds, higher yields and repeatable quality are the outcomes (Figure 2).

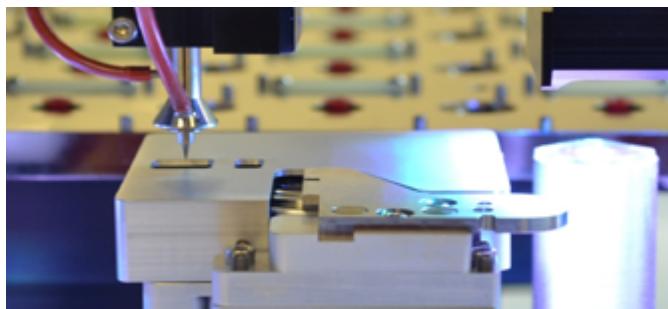


Figure 3: Epoxy stamping well.

Eutectic bonding is the process of using a solder alloy as a third material to form a continuous bond between two components. In the case of CoS, this often means two gold-plated materials being joined by gold-tin solder. When performing eutectic die bonding, the temperature of the assembly is brought up to just above the melting point of the solder. As the solder liquifies, the chip is placed with controlled force. The part is then cooled to below the reflow temperature and the eutectic bond is complete. During the time that the part is subjected to heat, it is important to control the atmosphere. Eutectic bonding is usually performed in an inert environment to prevent



Figure 4: Wafer handling.

oxidation of the bonding surfaces. A 95-5% nitrogen-hydrogen mix should be used so that hydrogen is present for use in the formation of the bond.

Epoxy deposition. CoS components are small and consequently require very small epoxy dots for successful epoxy die attach. Components, such as 200 micron laser diodes, require very small volumes of conductive epoxy with an exact dimension. Epoxy coverage with no voiding and controlled, thin bond lines is critical to maximize thermal transfer, mechanical strength and minimize stresses. Squeeze-out must be controlled to prevent shorting

or bridging, and epoxy must be placed in precise locations to maximize yield.

There are two basic methods for applying epoxy to accomplish the task described above. These include stamping (pin transfer or daubing), and syringe fluid dispensing. The selection of deposition method will largely depend upon the properties of the epoxy used and the minimum dot size required. Factors such as silver grain size, material viscosity, thixotropic index, and packaging methods will all influence the decision on the material deposition method. Often for CoS, the solution is stamping because the process requires dots smaller than 200 microns.

The advertisement features a blue and white design with various images related to technology and materials science. At the top right is the logo for "alpha advanced materials" with a stylized 'a' icon. The central text reads: "MEETING ADVANCED PACKAGING DESIGNS BY REDUCING COMPONENT SIZE AND ENABLING GREATER DEVICE RELIABILITY". Below this, there are several images: a hand holding a small electronic component, three test tubes, a speedometer-like gauge, and molecular models. On the right side, there is a section titled "ATROX® IS" followed by a bulleted list: "• PASTE & FILM • HIGH THERMAL • HVM PROVEN". The bottom left corner contains the text "ASIA • EUROPE • AMERICAS" and the bottom right corner has the website "www.AlphaAdvancedMaterials.com".

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Stamping is used to create very small epoxy dots by touching down in epoxy at the stamping well and then transferring the material onto the substrate. Dot size is determined by the epoxy thickness at the well and the stamp tool profile. In the stamping process, a reservoir of epoxy is presented in a grooved well. The well is rotated so that the material is passed under an adjustable height wiper blade. The height of the wiper blade should be precision adjustable using a micrometer adjustment. The rotating stamping well can have multiple grooves to accommodate multiple types of epoxy.

Stamping does not have to be limited to the transfer of single dots. Gang-arrayed (multiple) stamping tools can be employed to transfer an array of dots simultaneously. These gang stamp tools have multiple points that place the same pattern of dots with each touchdown. This is useful for increased throughput and for precise control over the pattern.

Tool profile is another critical factor of stamping to consider. Tools can be designed with a spherical tip or a flat tip depending on the shape and size that is desired for the dot. When combined with good control of epoxy thickness in the well, the right stamp tool can produce repeatable dots of a very specific height and diameter.

Syringe fluid dispensing is an alternative to stamping. The feature typically includes high-resolution servo driven, positive displacement pumps, for the most accurate dispensing of dots, lines and areas. A precision time/pressure pump can also be used depending on the application, materials and process requirements. Material flow is enhanced by a chamfered design in the needles inside the wall, with the chamfering toward the needle tip. This reduces surface tension, provides for more precise control, and also reduces clogging (Figure 3).

Small die and solder preform handling expertise. CoS components, such as laser diodes (LD), photodetectors (PD), capacitors and thermistors, are commonly as small as 200 microns square and require special handling. Solder can be pre-deposited on some devices such as the LD die. When solder is not pre-deposited, solder preforms are used. These solder preforms require the same precision handling as small die.

Presentation methods include waffle pack, Gel-Pak™ and wafer. Wafer handling must be optimized for the CoS die. These small, thin and fragile die must be delicately picked from the wafer tape to avoid damage. Synchronized movement of the pick head and



Figure 5: Multi-colored lighting.

the ejection needles must be used. By using servo-controlled synchronized systems, yield is increased by avoiding die damage. This is of particular concern for thin, fragile materials and die with internal and surface features. Both LD and PD die are made of fragile III-V compound semiconductor materials, such as GaAs- and InP-based materials that require delicate handling (Figure 4).

The use of programmable closed-loop force feedback, is required to enable delicate handling of these devices. Die must be picked and placed with controlled forces as low as 10 grams. The crystal facets on edge-emitting laser diodes and receptor areas of PDs must not be touched by the bonding tools because the devices can be damaged. Custom vacuum collets are used to avoid touching sensitive areas.

High-precision placement at high speeds. When manufacturing optical components, such as CoS, placement accuracy is a basic requirement. Throughput is only meaningful with achieved accuracy. When manufacturing optical devices, which will couple light, high yield is only achieved with a high-precision, stable machine. The device and epoxy placement location, in the case of epoxy die attach, must be controlled for high yield. Placement accuracy as low as 3 microns at high speeds is needed for CoS and is achieved through the use of linear motors and encoders combined with a thermally and mechanically stable platform.

Parallel processing is used to achieve high speeds. Parallel processing examples include multiple pick-and-place heads, “on-the-fly” tool changing, parallel vision alignment, material handling, and multiple bonding stages with parallel loading and unloading.

Advanced vision and lighting optimized for CoS. Another major feature of HVM CoS is machine vision, a critical factor for accurate placement and required to achieve micron-level accuracies. The vision system must align the die features to substrate fiducials ensuring repeatable and precise placement. The alignment of the laser chip to a photo diode is critical. This requires the ability to perform feature recognition of the LD and PD to ensure proper light coupling.

Machine vision is used for alignment of components with bottom features and flip chips. An upward facing camera captures the image of the die feature on the vacuum collet prior to placement. The integrated vision aligns features on the bottom of the device prior to placement.

Optimal lighting conditions are needed for die recognition and for alignment. Multi-color lighting is required to successfully image process a wide range of materials and enable optimum imaging of low-contrast components. Multi-colored (i.e., red, green and blue) ring lighting is a powerful tool when processing challenging alignment surfaces (Figure 5). Lighting intensity must be programmable and include both ring and collimated lights for a complete lighting solution. It also must be possible to individually program optimal light settings for each die and substrate fiducial alignment.

Summary

This article reviewed the challenges and the required die bonder features for successful HVM of CoS devices. HVM of CoS is an important and challenging problem requiring unique capabilities from the die bonding system. A HVM CoS die bonder should include many parallel processing features to maximize throughput. By combining the features discussed, an application-specific standardized die bonder will deliver a flexible solution, which maximizes product yield, throughput, and process control, to ensure a successful solution for HVM of CoS. This approach also results in fast machine delivery times. Fast machine delivery times allow CoS manufacturers to scale production rapidly, to meet the market demands.

Biographies

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A comprehensive high-density advanced packaging solution for today's OSATS and foundries

By Keith Felton [Mentor]

The increasing growth of innovative IC packaging technologies, such as fan-out wafer-level packaging (FOWLP), multi-substrate/multi-device packages like 2.5D with interposers and system-in-package (SiP), is in response to system scaling demands and the increasing demand for heterogeneous integration. However, these emerging technologies are creating new challenges because they commonly employ silicon-like features and processes, or multi-substrate architectures to facilitate high-performance memory devices such as high bandwidth memory/hybrid memory cube (HBM/HMC).

Today's package design methodologies and tools are at an inflection point. The entry of silicon foundries into the packaging supply chain further disrupts tools and methodologies with their application of silicon process design kits (PDKs) and verification processes to packaging. Thus, high-density advanced packaging (HDAP) design and verification require cooperation and collaboration between design houses, OSATS, foundries, and electronic design automation (EDA) vendors. What's needed is a solution comprising fully integrated tools and the functionality to operate in both the IC and packaging domains. Also, developing and deploying process-optimized design kits such as accessory development kits (ADKs) and PDKs, the OSATS, foundries, and their customers can achieve design, fabrication, and assembly predictability and package performance. This article will cover the implementation of an optimal end-to-end HDAP methodology addressing the needs of OSATS and foundries.

The move to HDAP

The term "high-density advanced packaging" (HDAP) was coined by Mentor to categorize the disruptive packaging technologies that present unique

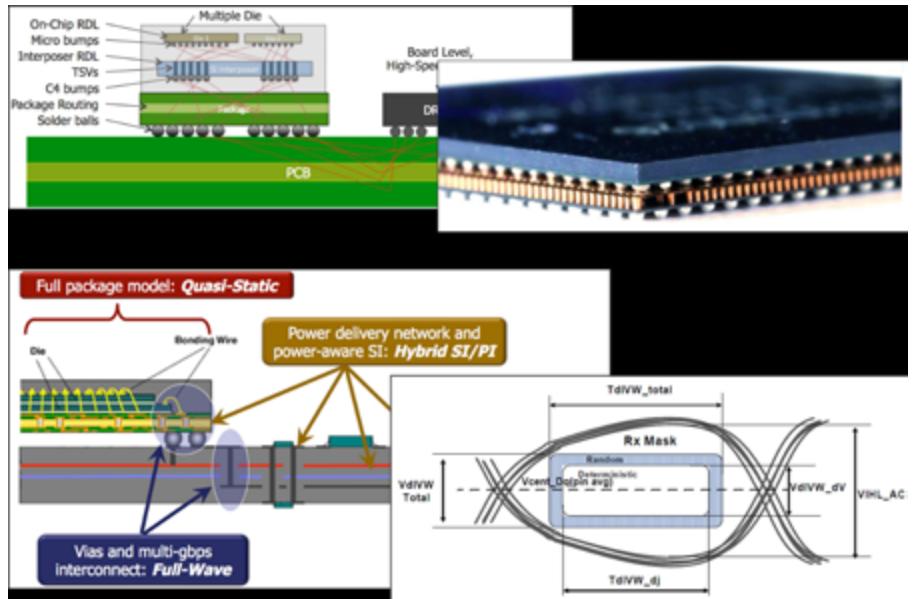


Figure 1: HDAP can be characterized by multi-substrate/multi-device packages that require device/substrate stacking using high pin-count devices or designs.

challenges to traditional design tools and methodologies (Figure 1). The most well-known and publicized form of HDAP is the fan-out wafer-level packaging (FOWLP) that is rapidly gaining popularity in the fabless semiconductor market. FOWLP was given broad public attention through TSMC and its InFO FOWLP process, but there are other suppliers offering proven FOWLP processes. The other common HDAP package types are 2.5D using silicon interposers, chip-on-wafer-on-silicon (CoWoS), and wafer-on-wafer (WoW).

HDAP's use of "IC-like" processes and tools necessitates a higher data resolution and design rule checking (DRC) accuracy for smaller feature sizes. GDSII quality and performance on non-Manhattan geometries can also be an issue for traditional packaging tools. I/O counts on application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and system-on-chips (SoCs) can approach or surpass 10K pins, which impact design tool performance, capacity, and throughput.

HDAP as a new technology "node point" requires a substantially different design flow, similar to how the organic laminate (plastic) ball grid array (PBGA) substrate was a "node point" evolution, which gave rise to new design flows, tools, and processes. Differences between today's well-understood PBGA flow and HDAP (Figure 2) present some unique challenges to existing design tools, methodologies, and processes. Examples include:

- Prototyping and connectivity planning of multi-die integration and optimization (critical for interposer-based designs);
- Device and substrate stacking – 3D interoperability;
- Shrinking feature sizes and new geometries;
- Place and route support for through-silicon via (TSV), micro-bumps, silicon interposer redistribution layer (RDL), and signal routing;
- Increasing pin counts on devices

- and overall design;
- Assembly-level verification (layout vs. schematic, or LVS, and layout vs. layout, or LVL) of individual design substrates and complete assembly;
- Mask-level fabrication verification of individual substrates; and
- Electrical extraction and analysis of the completed assembly.

The importance of prototyping

Irrespective of the type of HDAP, they all benefit from prototyping prior to detailed implementation. Prototyping enables the design engineer and project architects to evaluate die locations (x, y, and z), explore interposer options, build system-level assembly netlists (from die-source Verilog, import of external connectivity (csv), or directly), and evaluate critical interface assignments and implementation viability.

Prototyping before detailed physical design can reduce electronic change orders (ECOs) and provide greater predictability to the design process (**Figure 3**). Prior to HDAP, prototyping was usually done with spreadsheets, known as “bump-ball” maps—more of a documentation process than prototyping, because spreadsheets cannot provide “what-if” views or manage ECO changes in connectivity or assignments.

HDAP prototyping in a graphical environment (where all design elements can be visualized and interacted with) provides an optimal end solution without costly project delays, or iterations caused by late identification of issues. Investing in cross-substrate prototyping and planning during the early stages of design can greatly improve predictability during implementation by finding and fixing early cross-substrate issues. An early-system perspective with cross-substrate visibility improves communication and coordination by providing immediate feedback on decisions that are typically made on an individual substrate basis. Other benefits of HDAP prototyping include: quick evaluation and convergence on the best, most cost-effective configuration(s) from a system perspective; reduced working silos that can result in over-design or needless complexity; and better management of cross-substrate transitions. The macro goals of HDAP prototyping can be summarized as:

- Accurate design connectivity capture, construction, coordination, and management of multiple substrates in one environment with visualization

- across IC-package-PCB;
- Supporting substrate-specific land patterns for a single device including compensation;
- Generation and synchronization of library data for use during PCB design; and
- Targeting of multiple packages or PCBs (if needed).

Once the prototyping phase has yielded a feasible and acceptable design scenario, detailed design implementation is the next step.

HDAP design

Historically, package design and IC design have been isolated processes, with little in common. Bringing them together requires melding the two into a single cohesive flow. ICs are designed primarily in a Linux® operating environment, using electronic design automation (EDA) tools certified by a target foundry or fab and associated with a specific PDK. SoC designs are typically built using Manhattan geometries represented in gridded formats like GDSII or OASIS. When the IC design is sign-off ready, the final approved design files (tapeout) are sent to the foundry for manufacture. When finalized, a die abstract (i.e., the die’s size and the individual pin locations) is passed to a package design team using any one of several formats (LEF, AIF, etc.). Although few common standards exist between these communities, no new standards are needed to bring the two together. Data-format conversion with tool-to-tool interfaces and communication protocols can meet the needs of all the parties involved.

While communicating between Microsoft Windows and Linux can be tricky, this can be achieved using a virtual network connection (VNC). The macro goals of HDAP prototyping can be summarized as:

the entire system must be optimized. An IC designer might be able to design a really small IC but connecting that die into the package is more difficult, thus expanding the package footprint. Similarly, a package designer might be able to design a clean and tight package, but getting the IC designer’s die I/Os to match specific locations may be impossible. To optimize the entire package design, IC designers must understand the intended package, and package designers must know more about the ICs in the package. A number of technical challenges that must be managed by the design tools include:

- Silicon RDL layers, organic RDL layers, or mold/plastic layers: each type has its own unique design rules to increase yield;
- Stress relief: minimizing straight lines helps, but makes verification more challenging;
- Copper areas require complex outgassing perforations to prevent substrate warping and copper density balancing across the design;
- The connection path from die pad to copper conductor path requires filleting: the addition of metal to

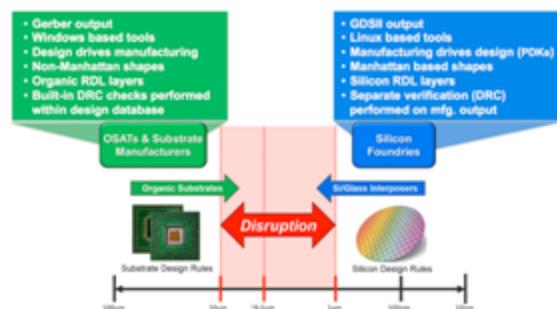


Figure 2: The major differences between traditional PBGA packages and HDAP packages.

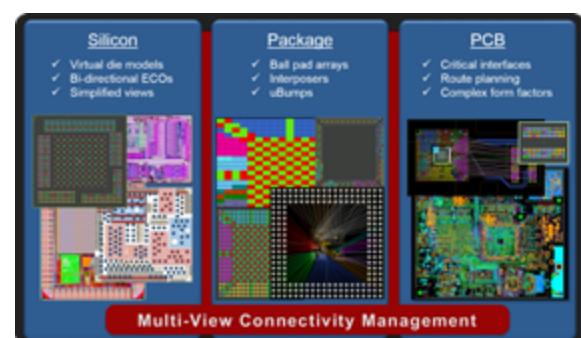


Figure 3: Visual prototyping using abstracts for the completed HDAP design includes a target PCB (if applicable) to provide the engineer/architect with a sandbox canvas to explore options and design viability.

- smooth the transition between geometry dimensions;
- Potential die shift during assembly requires flexible, adaptive patterns; and
- Producing clean fab-ready GDS.

HDAP package design

The Mentor® Xpedition® Substrate Integrator technology helps IC, packaging, and printed circuit board (PCB) co-design teams visualize and optimize complex single or multi-chip packages integrating silicon-on-board platforms.

In the HDAP environment, Xpedition Substrate Integrator and Xpedition Package Designer provide the integration/co-design platform for IC, board, and package that support PCB, multi-chip module (MCM), system-in-package (SiP), RF, fan-out, and BGA designs (**Figure 4**). This flexible, multi-mode design platform provides a single, hierarchical view of the system that is easy to extend through the Microsoft component object model (MS COM) and routing technology. Xpedition users can drive rule-based I/O-level optimization and perform pin and ball-out studies from their respective domains, visualizing the impact across the complete system, and generating an automated central data library in the process. Cross-domain capabilities include:

- Connectivity management;
- Design-domain connectivity models (hardware description language (HDL), table/spreadsheet-based and schematic editing modes);
- Cross-domain signal shorting and splitting with automatic pin-mapping;
- System-level connectivity tracking and verification (source netlist);
- Design tool aggregation; and
- Interconnect optimization focused on layer reduction and improved signal quality (visualize and optimize interconnect across system; ICs, interposers, packages, and PCBs; smart unraveling of interconnect paths).

A common problem with conventional package design tools and methodologies is that the design will pass DRC within the layout tool, but fail once the outputs are checked with manufacturing physical

verification tools. A related problem is the insertion or substitution of shapes into the output files due to lack of support within the layout tool (mesh pads, graduated degassing, etc.). Such HDAP common entities must be handled directly within the design tool, otherwise their absence creates a discontinuity between the layout database and what's actually manufactured.

HDAP package layout

Xpedition Package Designer provides a solution for HDAP layout through to mask-ready manufacturing output. Designers can create today's complex single or multi-die packages using this solution. Additionally, die-attach capabilities support wire bond, flip-chip, stacked die, system-in-package (SiP), and package-on-package (PoP) through to the latest wafer-based methodologies

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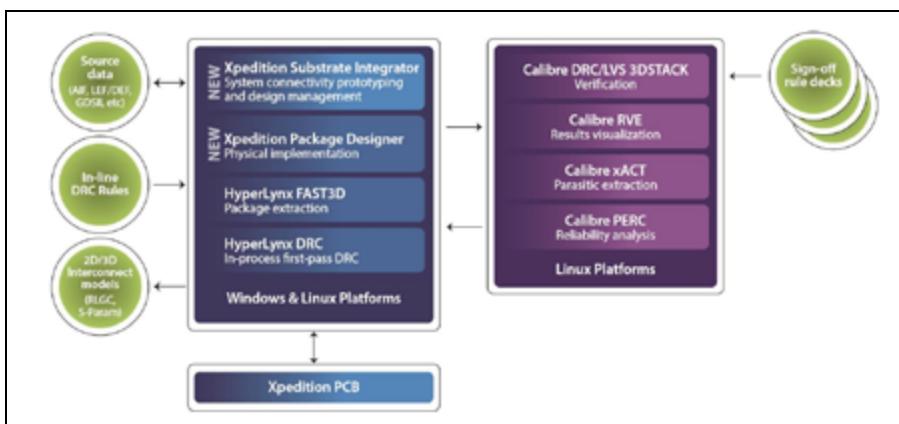


Figure 4: The Mentor® Xpedition® HDAP flow comprises the Xpedition Substrate Integrator, Xpedition Package Designer, HyperLynx® DRC and 3D Signal Integrity/Power Integrity technologies.

such as FOWLP and CoWoS. Among the important design capability that the solutions HDAP focus provides are:

- Comprehensive die and BGA import/creation utilities;
- Fast on-the-fly connectivity creation (layout driven design);
- Auto-assisted sketch routing;
- Integrated 2D-3D editing and visualization.

With many HDAP package types using 2.5D or even 3D for integration of substrates, visualizing and designing in 3D is a necessity. 3D helps designers understand what they are creating while reducing errors and increasing productivity by visualizing and interacting with the design beyond 2D (**Figure 5**).

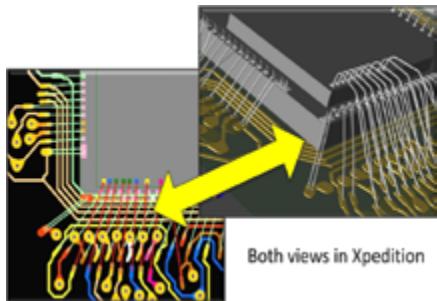


Figure 5: The Xpedition Package Designer tool provides real-time 2D and 3D design viewing and editing.

Achieving fabrication-ready GDS

For HDAP to become a repeatable, predictable design process, the design tools produce fabrication-clean graphic

database system (GDS) or, at minimum, manage GDS corrections identified during sign-off verification (**Figure 6**). Once the design has passed fabrication sign-off, it needs to be verified for assembly.

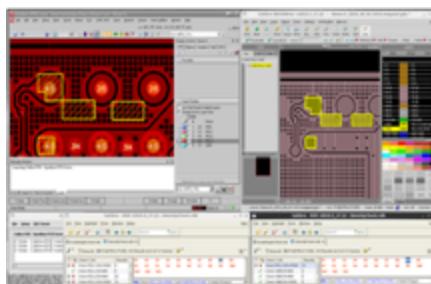


Figure 6: The Xpedition Package Designer and Calibre product are directly integrated across Windows and Linux platforms to produce fabrication-ready GDS.

HDAP verification

HDAP package designs require physical and logical assembly verification and validation. The die must correctly align with its corresponding landing pads on the interposer or package substrate (LVL). Checks required are alignment, pad size, and pitch scaling and pad-to-pad overlaps. On the logical side (LVS), users must ensure that connectivity exists between connected objects/shapes, verify the location of electrical pins, and check for mismatched connections.

Each individual die already will have been checked for its target foundry with respect to DRC and LVS. What's required is to check the interactions between the dies, and that the tool used understands the layering per die and per placement. The

typical HDAP verification process accomplishes the following:

- Verifies individual components stand alone (maintain standard DRC, LVS, PEX processes, and check per-process requirements);
- Defines and checks 3D assembly interfaces (consider: offset, rotation, scaling, etc.; verify die, pad, bump, and ball placements; and trace connectivity through assembly stack-up); and
- DRC and LVS checks (package connectivity to die pins, and physical geometric relationships and overlaps).

Most checks, or design rules and design parameters, will be defined by the foundry or OSAT supplier for their manufacturing process and yield goals. With HDAP design, foundries have a proven process and methodology to define, share, and drive design, verification, and sign-off with their IC design customers, known as a PDK, and associated design rule manual (DRM).

IC designers use PDKs to reduce their risk and improve overall productivity by implementing repeatable, proven verification techniques. Until now, chip design companies and OSATS had no corresponding sign-off verification process to ensure that an IC package meets manufacturability and performance requirements. This lack of qualified verification processes puts package designers at a significant disadvantage versus their IC design counterparts.

Verifying IC packages poses numerous challenges. Different goals between die design and the package design teams create unforeseen integration issues. Chips from different foundries are verified using different processes, so package failures are hard to identify and fix. There is no formal verification process to ensure that connectivity from a single die to the package's BGA is correct. Without good characterization of package processes and requirements, chip designers and OSATS must muddle through on their own. OSATS have built and manufactured packages for years, and developed a variety of tools, but each design team must

write its own rules for each assembly, with no reference sign-off deck to ensure manufacturability and package performance. Also, OSATS rarely hold their customers to a hard and fast rule deck like a foundry does.

What's emerging is a new approach for fabrication sign-off and physical verification of HDAP designs, called an assembly design kit (ADK), to ensure manufacturability and performance. Standardized rules ensure consistency across a process, qualified tool flows, interface formats, and input/output formats—everything needed for successful design, tested and qualified, and proven to produce working products. ADK's benefits include reduced risk of package failure, increased packaging business, and increased use of 2.5/3D packages. An example is the successful use of a conceptual ADK using the first basic building block of Calibre® 3DSTACK created and qualified by Stats ChipPAC using its eWLP wafer-level process. This rule file has been adopted and proven in production at Qualcomm on an assembly comprising two die connected through the package RDL. The rules from Stats ChipPAC include the DRC rules for the package layers

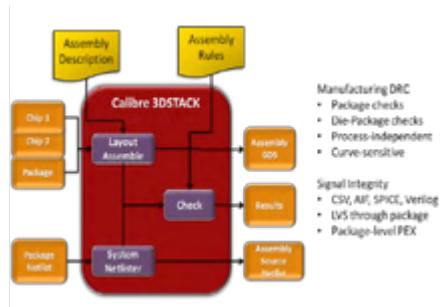


Figure 7: The Calibre 3DSTACK functionality, fully integrated with the Xpedition HDAP design tools, enables and supports all the verification and sign-off needs of HDAP designs.

plus checks to ensure that the dies are interacting and properly connecting within the package. The OSAT or foundry determines the connectivity stack for LVS comparisons on HDAP designs and creates design rules to address package-specific and die-to-package geometric interface requirements (**Figure 7**).

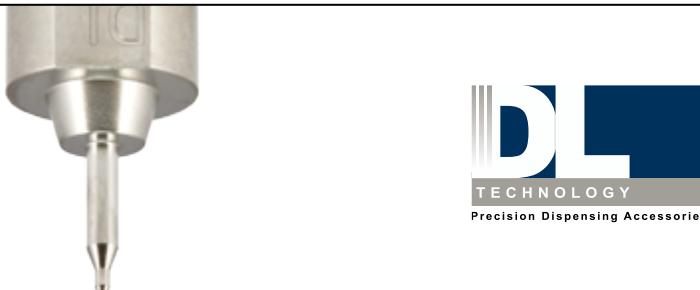
Summary

HDAP design and verification require cooperation and collaboration between design houses, OSATS, foundries, and EDA vendors. With common tools that have the integration and functionality needed to operate in both the IC and packaging domains, companies can reduce turnaround time and the risk of package failure. The HDAP flow described in this article ensures that package designers, foundries, and

OSATS have all the design and verification capabilities needed to take advantage of HDAP packaging technologies.

Biography

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Integrated solid-state capacitors based on carbon nanostructures

By Vincent Desmaris, Rickard Andersson, Amin Muhammad Saleem [Smoltek AB]

The constant demand for miniaturization, added functionality and increased performance of electronic devices systematically drives higher integration by adding more devices and functionality on a single chip. Over the last 40 years, this has been achieved by scaling CMOS technology according to Moore's law, resulting in better power performance and cost per function for each technology node. As the feature size of CMOS devices now approaches quantum or physical limits, the downscaling of devices is slowing down and therefore cannot sustain the lowering of cost and performance per function alone. As a result, a new component packaging strategy called heterogeneous integration, focusing on the performance enhancement and cost reduction at the system level, provides a new dimension and enabler to follow Moore's law in terms of system performance, by the stacking of chips (3D) or using an intermediate substrate, the interposer (2.5 D).

The full deployment of the 3D or 2.5D packaging technologies requires on-chip or in-package capacitors, not only in traditional integrated circuits, but also for integrated components, possibly on interposers, for applications such as decoupling capacitors, voltage stabilization or RF filters. In parallel, the emergence of the Internet of Things (IoT) is right around the corner, requiring not only high capacitance per unit area for the operation of the devices, but also integration of efficient and smart solutions with moderate energy storage and harvesting to operate the individual autonomous devices [1].

Traditionally, electrochemical double-layer capacitors (EDLC) [2] are devices providing the highest capacitance/footprint area [3], using the physical adsorption and electrostatic accumulation of ionic charges at the surface of the electrodes, originating from a liquid or sol-gel electrolyte [4]. However, liquid electrolytes are often toxic and corrosive,

and their encapsulation presents a considerable challenge that hinders their integration directly onto CMOS chips. Consequently, integrated high density capacitors need to be fully solid-state in order to meet the requirements of stability and lifetime. Fully solid-state capacitors have faster charge and discharge rates compared to a liquid electrolyte capacitor (supercapacitors), making them more useful for high-frequency applications.

Besides bulky ceramic discrete capacitors, the simplest realization of a capacitor is the parallel plate capacitor using a thin (a few nanometers in thickness) solid dielectric layer. In this configuration, the capacitance is proportional to surface area, hence the parallel plate capacitors are limited by their footprint area. In ICs, an effective increase of the capacitance area has been achieved using deep trenches in the silicon substrate using dielectrics deposited using low-pressure chemical vapor deposition (LPCVD) [5] or multilayers of atomic layer deposition (ALD) [6]. Further increasing the capacitance requires consuming precious space on the chip, or other cost-increasing and partially reliable methods, in particular irreversible very deep reactive ion etching (DRIE) of the substrate combined with atomic layer deposition. This limits the potential for implementation of integrated capacitors. Recently, IPDiA (now Murata) has shown 500nF/mm^2 capacitors integrated in the silicon interposer at the cost of a minimum etch depth of $100\mu\text{m}$ [7] that potentially weakens the interposer's mechanical stability or imposes a large thickness of the interposer.

With the similar idea of increasing the surface area of the capacitor electrodes in mind, carbon nanostructures have been investigated as electrode materials in combination with thick dielectric layers deposited by ALD. However, such an approach has been, so far, limited by the necessity of transferring the

nanostructures from the substrate on which they are grown to the active area, where they have to be used, because of the growth temperature required by such structures. Capacitors based on transferred carbon nanotubes (CNT) grown at 700°C , subsequently coated by a $10\text{-}15\text{nm}$ dielectric deposited by ALD provided capacitance values of about 40nF/mm^2 [8].

The recent progress and availability of our proprietary technology has allowed the growth of vertically aligned carbon nanofibers (CNF) at a temperature compatible with CMOS technology directly rooted on the active chip, underlying substrate or component. This technology also allows the process on any substrate that can sustain a thermal budget of less than 400°C , and permits the realization and re-visiting of integrated solid-state capacitors with high-capacitance per footprint area. More specifically, integrated novel capacitors can be made of vertically aligned carbon nanofibers as one electrode material, providing a large 3D surface area for a small footprint, and their conformal coating of dielectric and a metallic counter electrode. The more than tenfold enhancement of the active surface, compared to the occupied footprint on the chip, where they are rooted, makes very efficient use of the chip. Such capacitors can therefore take advantage of the unique combination of the intrinsic electrical and surface properties of carbon nanostructures [9], without the economic and technical hindrances of the transfer process after growth, associated with the limited and laborious nature of such a transfer process.

Our enabling technology for the growth of the CNFs is catalytic plasma-enhanced chemical vapor deposition (PECVD) [10] (**Figure 1**), which made possible a completely deterministic and possibly reworkable method to produce CNFs on substrates. The positioning of the fibers on a substrate would depend on the

Low-Stress Bonding & Debonding

presence of a catalyst, whereas the CNF alignment is controlled by the electric field generated by the growth plasma, and the length of the CNF is simply determined by the time and growth conditions. Many PECVD systems using different radio frequency (RF) and microwave sources have also been developed [11-13]. However, the direct current plasma-enhanced chemical vapor deposition (DC-PECVD) has produced, so far, the best results for the fabrication of CNFs at low CMOS-compatible temperature using different pre- and post-processing techniques to cope with the inherent discharge problems that may arise when using insulating substrates [14]. The activity of the catalyst particle is crucial for the growth process [15]. It can consist of one or a few elements [16], however the vast majority of the reports regarding the growth of CNFs deal with catalysts made of transition metals: Fe, Co, Ni [16]. In addition, it is currently believed that the catalyst should form nanoparticles of a favorable size in order to initiate the growth of a CNF. Therefore, the catalyst can be deposited as a film using physical vapor deposition techniques, or directly as nanoparticles using spray coating [17] or spin coating [18], providing that the growth temperature will lead to a dissociation of the film into droplets/nanoparticles of appropriate size.

In a first demonstration of the CNF-based capacitor technology, very low profile 3D capacitors with a profile of 7 μ m have been produced. The CNFs were grown as a “forest” or “bed of nails,” selectively, using DC-PECVD at 390°C in an ammonia and acetylene environment [18] (**Figure 2a**), on a Ti/Au current collector previously deposited using sputtering

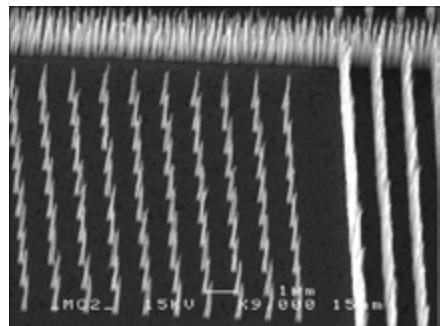


Figure 1: SEM of individual fibers.

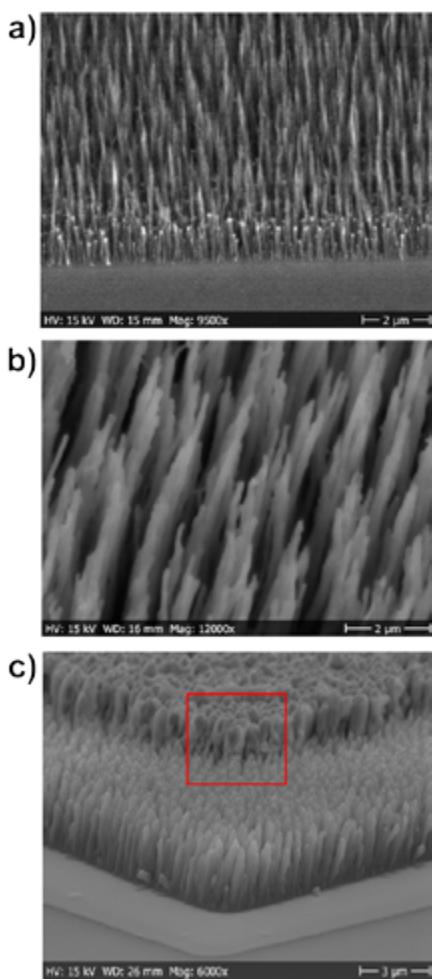
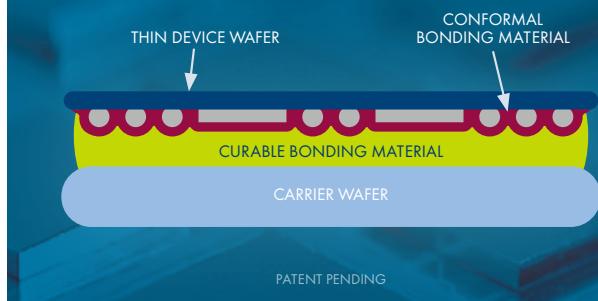


Figure 2: a) CNFs as grown; b) CNF coated with dielectrics; and c) Integrated 3D capacitor.

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on a Si substrate. Low-temperature thermal ALD was used for conformal coating of dielectric Al_2O_3 on vertically-aligned carbon nanofibers (VACNFs) (**Figure 2b**). To define the top electrode, a stack of Ti/Au was sputtered followed by photolithography to define the top electrodes (**Figure 2c**).

The capacitors with a total height of less than 7 μm showed linear dependence of the capacitance per footprint area ranging from $\sim 10\text{-}15\text{nF/mm}^2$ (**Figure 3**). Therefore, they represent a credible solution in the heterogeneous integration landscape, proving truly

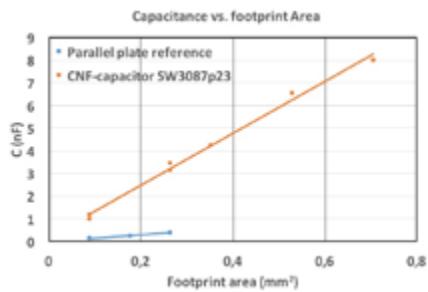


Figure 3: Comparison of Smoltek's solid-state initial integrated capacitor prototype (SmolCACH™) and parallel capacitors.

solid-state and 3D capacitors for on-chip integration for capacitance densities up to $1\mu\text{F/mm}^2$. Further development and optimization will be needed to ready the solution for high-volume manufacturing.

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High-performance and low total device cost using 2.5D packaging

By C. Key Chung, Wen Shan Tsai, Daniel Ng, C.F. Lin, Ally Liao, Steward Pan [Siliconware Precision Industries Co., Ltd.]

Semiconductor packaging using 2.5D technology has demonstrated high-performance with low total cost. Though in its infancy, this packaging is believed to become mainstream with respect to the assembly industry roadmap. It is gaining ground and soon will grow significantly, thereby enabling an alternative to Moore's Law scaling. Meanwhile, 2.5D technology also brings a significant decrease in cost compared with system-on-chip (SoC) devices, which will also be discussed in this article.

Introduction

The development of the semiconductor industry has followed Moore's Law for more than 60 years. The law – in its current iteration – states that the number of integrated transistors on an integrated circuit (IC) chip is doubled approximately every 18 months. However, as technology nodes have progressed to below 10nm, the cost per die size (mm) becomes enormous and difficult to sustain. Various news reports have said that the physical limitation of the transistor gate oxide — now at single digits in nanometers — caused a CPU provider to delay its 10nm node implementation to 2017 [1]. Additionally, foundry fabs face the challenges associated with the technical limitations and yield challenges after implementing 10nm process technology [2]. The fundamental consideration of performance over cost to keeping up with Moore's Law is now nearing its limits and has been heavily debated by semiconductor industry forecasters [3-5]. The major topic now is: Has Moore's Law really come to its limit, or can it be continued, in a manner of speaking, using other means? This paper presents the continuation of scaling (though not in the traditional sense of Moore's Law) that happens in assembly manufacturing using 2.5D as an illustration.

Continuing “scaling” with 2.5D packaging

Moore's Law predicts that the performance or transistor density on an integrated circuit

chip will be doubled every 18 months. With the technology node narrowing down to 10nm and below, it reaches to near-term limits. The investment for new equipment and facilities becomes exceedingly high and demand for high yield determines the success of this single digit node scaling. Below the 10nm node, current leakage and dielectric breakdown are difficult to control: there are only a few electrons within a cell, which makes the operating voltage and the noise within cells very difficult to address [6]. The low yield of foundry fabs [2], and the delayed implementation of the 10nm gate oxide [1] announced in 2015 reflect these challenges. Higher investment cost combined with a lower quantity per wafer due to low yield, amplifies the cost per die as depicted in **Figure 1** [7]. This situation inadvertently has slowed transistor scaling progress.

Our recent research finds that 2.5D packaging [8] is a way to continue Moore's Law by integrating heterogeneous logic and memory dies together so as to deliver higher electrical performance. The package design has 100x improvement in inter-die bandwidth/watt; 50% power savings; 5x latency reduction, and 20x denser wire pitch [9]. More importantly, a lower total device cost with much better yield can be achieved.

We should reflect on what we consider a somewhat surprising development: 2.5D packaging costs are high, and though debated intensively, we now come to a different conclusion. Certainly, 2.5D packaging by itself as compared to other packaging is costly.

However, when we compare its cost to the electrical performance of a device, the cost benefit is obvious. We need to emphasize that the device here is a micro-system within a package, or a system-in-package (SiP).

Commercial products integrate the microprocessors and stacked memory in a single package using a through-silicon interposer (TSI) (**Figure 2**). The TSI provides not only similar performance as compared to the system-on-chip (SoC), but also a better cost advantage. The reason for this is that the integrated microprocessor and other logic dies that are part of the SoC require a larger die size. One cannot compensate for this situation by scaling down the transistor size significantly. Technology nodes at 10nm and below require a huge investment, particularly in the lithographic process. The larger die size will exacerbate a lower yield, thereby increasing the cost per die. This does not bode well for the economics.

In addition to the above considerations, the fabrication processes for microprocessor and memory devices are not compatible and cannot be integrated. Thus, 2.5D

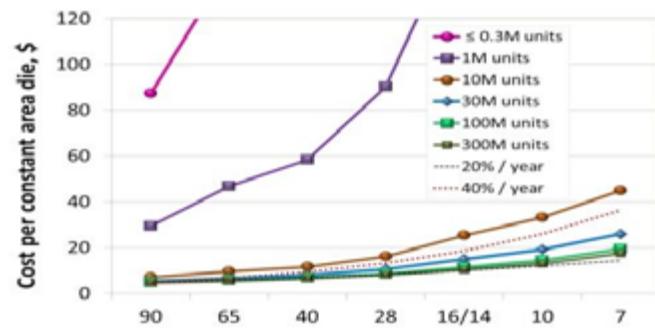


Figure 1: Cost per die trend with technology node [7].

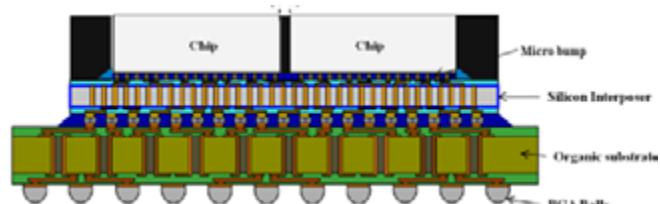


Figure 2: 2.5D IC structure schematics.

packaging provides a sweet spot for the heterogeneous integration of both logic and memory die, which fits nicely with the requirements of higher performance with lower cost. To elaborate how the total cost of 2.5D packaging, which is low when compared with the electrical performance of a comparable device. There are several reasons for this, which are outlined below.

First, the cost model of foundry houses normally sets the silicon yield per wafer at 80~90%. That means a 10~20% yield loss is being shared with the design house. As compared to the assembly house that sets a cost model with a yield over 95%; based on this difference, there is at least a 5~15% yield loss burden cost.

Second, a silicon wafer requires a high number of die per wafer in order to reduce cost. Therefore, the method by which scaling is optimized plays a significant role in maximizing the base. But as the technology nodes scale down to 10nm and below, the scaling effect has also been narrowed down. For SoC devices, the die size is much larger as compared to a single die. This design reduces the number of die per wafer, and hence exacerbates the

yield loss. By leveraging the use of a 2.5D package, one could attain higher assembly yields while meeting similar electrical signal performance. Recently, design houses started splitting the logic and SRAM die into two different wafers so as to increase the number of dies per wafer, which resulted in a cost reduction. The SRAM die is then stacked onto logic dies via a 3D package assembly. This demonstrates that the trend towards 2.5D and 3D ICs is evolving.

Third, 2.5D design rules are more forgiving with respect to using alternative electrical signal routes as redundant rules or having multiple connecting channels to connect between logic and memory dies. This approach provides a much larger assembly yield.

As TSI fabrication technologies become more mature and stable, the organic substrates might be superseded [9]. Actually, a 2-layer TSI using a line-space of 2/2 μ m is equivalent to an 8-layer substrate using 5/5 μ m line-space. This 2/2 μ m line-space is similar to around 12-16 layers of an organic substrate using commonly available technology of 10/12 μ m line-space.

With the above consideration in mind,

what are the risk areas that have not been addressed? Because the assembly of a 2.5D package contains multiple dies, the carrying cost of 2.5D during assembly to the total device cost is high. Therefore, demanding high yield is essential and there are several major challenges associated with this as follows:

1. Larger package size with higher thermal mechanical stress, including warpage;
2. Longer assembling cycle time due to complex process routing;
3. Higher die placement precision for micro bumps;
4. High cleanroom grade to class 100 is needed to avoid particles falling on the micro-bump;
5. One can't use X-rays for validating interconnects because doing so could damage the high bandwidth memory.

2.5D packaging technology is still at the infancy stage, but its relative application will grow explosively according to the market trend. Currently, the design of TSI in the package contains 2~3 metal layers on the top surface and a straight line connecting the upper chips and the underlying substrate. The line width/space of the metal layers is <2/2 μ m level so as to meet the high speed communication requirements. From the viewpoint of wafer fabrication, there is still a great deal of opportunity for scaling down.

The evolution described above demonstrates that Moore's Law will continue to move forward. By increasing the line wiring in the TSI using the wafer fabrication process that is already mature at the sub-micron level, the TSI's line pitch and the density of the connection endpoint (I/O) are expected to grow significantly. This allows multiple dies to be integrated in a package with much higher signal density, thereby greatly enhancing the electrical performances and lower cost, as shown in **Figure 3**.

Figure 4 shows the trend of total cost per device between the 2.5D package and the SoC. Although the 2.5D package is constructed using TSI, logic, DRAM, and an organic substrate, the processes used in its making are relatively mature and have good yields. As the TSI process continues to improve and scale down, the reduction of its size will be achievable. Meanwhile, the number of TSI within a wafer is expected to increase. The overall cost of TSI manufacturing will be reduced. We also have observed a trend that the use of TSI

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has evolved into the logic die to enhance the functionality and reduce the total cost.

In contrast to the SoC chip, an SoC wafer integrates the functions of the digital and analog chips to improve the performance. This makes the I/O counts and the chip size needing to be increased. This integration approach comes with disadvantages, such as the reduction of the number of chips per wafer, and also an increase in the total cost per die. With the limitation on technology node development, this scaling approach to reduce the die size will face its own limitation.

The 2.5D package has its unique advantages to heterogeneously integrate chip functionality. Its interposer stacked with different dies with various functionalities was able to achieve higher performances and reduce the total cost. We can therefore continue to observe a kind of "Moore's Law" with respect to 2.5D packages.

Summary

2.5D packaging is in the initial phase for high-performances electronic device implementation. This package has better cost advantages when compared with the SoC package. As TSI technology continues to evolve, the I/O density within TSI is expected to grow, and the line-space dimensions will scale down in a timely manner. This scaling effort not only improves electrical performance,

but also reduces overall device cost. So, while it is not the traditional form of Moore's Law scaling, we can say that scaling continues in the package assembly as we reach near-term limits at advanced technology nodes.

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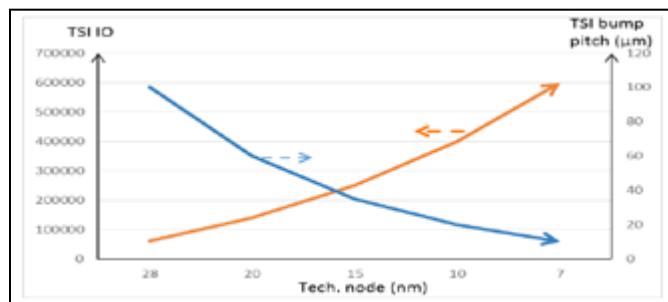


Figure 3: TSI I/O and pitch relationship with the technology node.

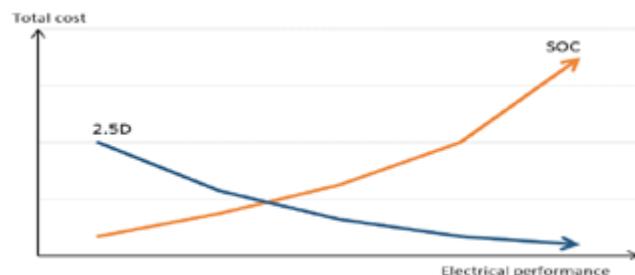


Figure 4: SoC and 2.5 D total cost trend vs. performance requirement.

package to 2.5D/3DIC," Global Summit 2013.

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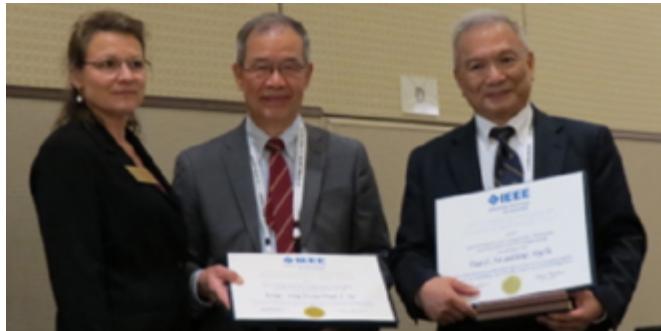
2017 ECTC – a global packaging conference

By Mark D. Poliks [Binghamton University] and Eric Perfecto [GLOBALFOUNDRIES]

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The 67th annual Electronic, Components and Technology Conference (ECTC) sponsored by IEEE/CPMT convened at the Walt Disney World Swan and Dolphin Hotel in Lake Buena Vista, FL from May 30–June 2, 2017. The conference lived up to its reputation as the premium international event of the microelectronics packaging industry with 335 papers presented by authors from 22 different countries, in 41 technical sessions spread over three full days. Sessions on fan-out wafer/panel-level packaging were well attended with over 350 people in the audience at times.

These technical sessions were preceded by a full day of 18 Professional Development Courses and three special/panel sessions on Tuesday. The Tuesday morning Applied Reliability subcommittee special session on “Material and Package Reliability Needs/Challenges for Harsh Environments” opened the conference with invited speakers from Boeing Research & Technology, Bosch, Schlumberger, Heraeus, General Electric, and NXP Semiconductors.



Jean Trewella/GLOBALFOUNDRIES, IEEE CPMT Society President, presented the 2017 IEEE Components, Packaging and Manufacturing Technology Field Award to Paul S. Ho and King-Ning Tu. An IEEE Fellow, Ho is director of the Laboratory for Interconnect and Packaging at the University of Texas at Austin, Austin, TX, USA. Tu is the TSMC Chair Professor at National Chiao Tung University, Hsinchu, Taiwan.



Students enjoy yo-yos provided by Texas Instruments, sponsor of the 2017 ECTC Student Reception.

In the afternoon special session on “Flexible Hybrid Electronics – Electronics Outside the Box,” a panel of experts from the U.S. Air Force and Army labs, Boeing, Jabil, and IBM discussed how innovation in thin silicon device integration and packaging will deliver new electronics for medical and asset monitoring. The Tuesday evening panel session on “Panel Fan-Out Manufacturing: Why, When, and How?” included perspectives from global leaders from TSMC, DECA, NANUM, Fraunhofer, and Qualcomm.



Babak Sabi (left), Intel Corporate VP and Director of Assembly and Test Technology Development, receives a plaque as a keynote speaker from Henning Braunisch/Intel, 67th ECTC General Chair.

The plenary session on Wednesday evening entitled “Packaging for Autonomous Vehicle Electronics” featured key technologists from Georgia Tech, Texas Instruments, Velodyne, Nvidia, and Qualcomm sharing their views on the evolutionary packaging requirements to support widespread implementation of self-driving vehicles on



John Lau of ASM Pacific Technology Ltd., a past recipient of the CPMT Field Award, teaches the 3D IC Integration and Packaging professional development course held on Tuesday afternoon.



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Members of the Interconnect Technical Committee chaired by Katsuyuki Sakuma/IBM (center left) meet on Thursday night at the Program Committee meeting.

the road. The CPMT seminar on Thursday, “3D Printing Tools, Technologies and Applications,” featured speakers from Georgia Tech, Zukan SOZO Center, Nano Dimension, and Fuji Machine Mfg.

General Chair Henning Braunisch of Intel Corporation commented, “We were very pleased to see the 67th ECTC be so highly attended. We were thrilled to welcome 1,439 attendees this year, our third highest attendance ever. I think this is a clear indication of the importance that packaging and interconnect technologies have in helping the industry

to realize more highly functional products and systems. We are very appreciative of all the volunteers, sponsors, presenters, exhibitors, and attendees that helped make ECTC 2017 a great success.”

Mark your calendar for the 68th ECTC: Planning is already underway for the 68th ECTC, which will be held May 29–June 1, 2018, at the Sheraton San Diego Hotel & Marina, San Diego, California, USA. The first call-for-papers has been issued and abstracts must be received by October 9, 2017. For more information, visit ectc.net.

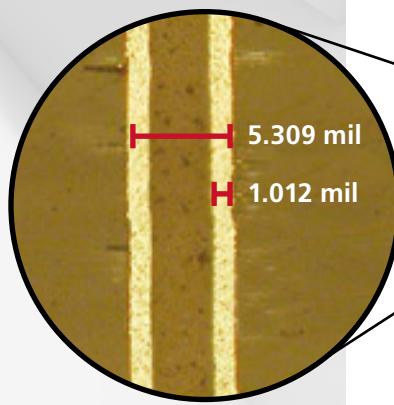


Rozalia Beica/Dow Electronics Material (second from the right), host one of several Women's Networking Tables at the conference luncheons.

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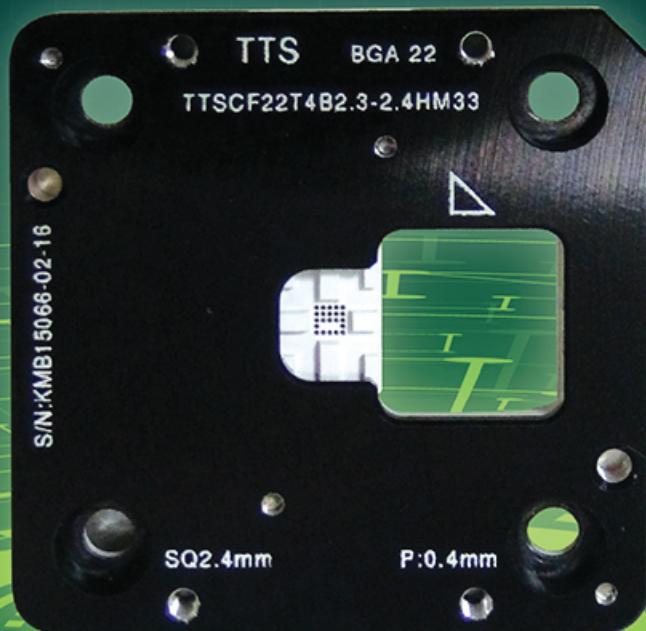
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