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Volume 23, Number 6

November • December 2019

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- Pressure sintering in high-power packages
- Enabling 3D packaging using excimer lasers
- Considerations when selecting a fab location
- Focused adhesives: customized materials for 3D printing
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Photo courtesy of
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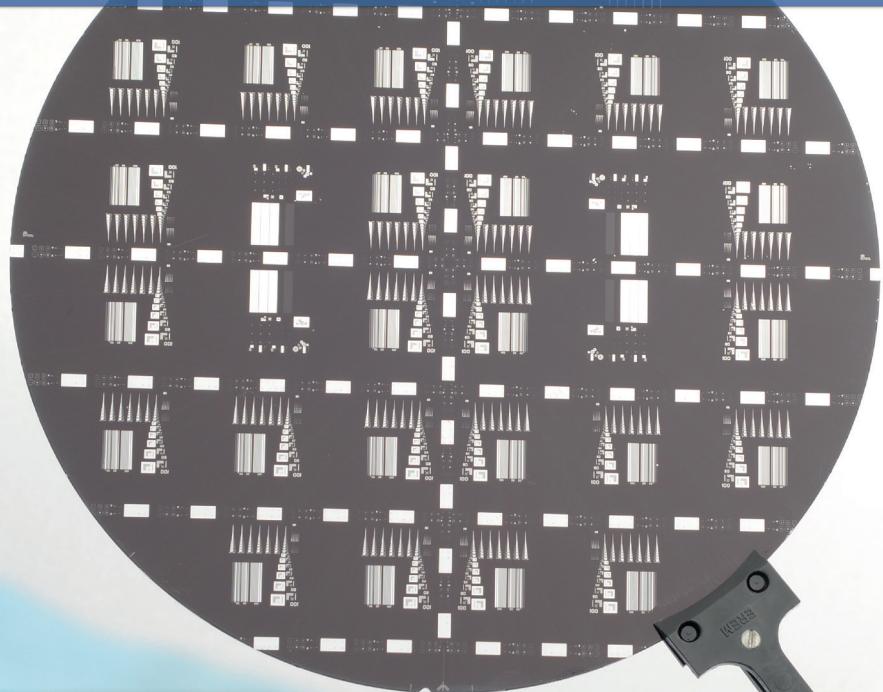
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Stacking technologies: the road ahead

By Favier Shoo [*Yole Développement (Yole), part of Yole Group of Companies*]

The emerging need for a smart high-performing ecosystem requires disruptive capabilities such as artificial intelligence (AI), mass data transfer and lightning-fast connectivity, which largely depend on the underlying technologies. Consequently, there are new developments on the technology front, with the resurgence of existing through-silicon via (TSV) technologies, together with significant innovation in both high-end TSV and TSV-less platforms. Undoubtedly, the industry is coming to accept a new path to enable these digital transformation-led technical requirements and that is through stacking technologies, instead of relying on node scaling.

High-performance computing (HPC), AI computing, crypto mining, data center computing, big data analyses, and the like, all require computing capabilities with low latency, high speed, and low power consumption. Today's packaging technologies, such as TSV, make these requirements achievable combined with footprint reduction on account of vertical stacking. TSV technology is widely used in memory and in Si interposers. When we combine these two functionalities, we have hardware that can meet HPC requirements. TSVs in both memory and interposers are widely used with graphics processing units (GPUs). This was one of the first hardware applications for both technologies (interposer and high-bandwidth memory [HBM]). TSVs became more and more desirable with the entrance of HBM to the market considering the performance it can achieve with a reduced footprint.

Presently, TSV technology is widely used in HPC applications — in what we call the high-end market — where cost is initially less critical on account of its stringent requirements. Hybrid bonding and 3D system-on-chip (SoC) will also have an impact on this market in the coming years, as players like Xperi, together with their partners, are working

on implementing hybrid bonding in HPC hardware. Nevertheless, there is still much that needs to be demonstrated in terms of what TSV technology can do, for example: 1) Can it be used for very fine-pitch applications ($<10\mu\text{m}$)?; 2) Can it demonstrate higher reliability, which would enable its use in markets other than the HPC and high-end segments (e.g., in the automotive market)? Furthermore, can the cost/price of using TSV technology be reduced further so that increased adoption in different mid-/low-end applications can be achieved. Although TSV technology is already established in mid-/low-end applications (e.g., CMOS image sensors [CIS]), its applications have to become more widespread in computing for consumer and enterprise applications in order for additional cost/price reduction to take place.

There are alternatives to TSV interposers, and these depend on the final application, the field of use, parameters, dimensions and requirements. Some technologies are more expensive than others and are therefore more suitable for the high-end market than for mid-/low-end markets. Most of the outsourced semiconductor assembly and test suppliers (OSATS) are developing proprietary solutions. If we dig into the details of each of those technologies, there are many similarities between them. Some are differentiated by the time in the process flow, others by changing the process step order, others still by the chip orientation. But the global technologies are quite similar and can, for the most part, be categorized as a sort of fan-out (FO) technology (e.g., Silicon Wafer Integrated Fan-out Technology, or SWIFT®, fan-out chip-on-substrate [FoCoS], integrated fan-out [InFO] with substrate, and silicon-less interconnect technology [SLIT]).

The cost, together with the performance and footprint of each and every one of these technologies, are three of the key parameters that the customers will be looking at when choosing between those

solutions. Other technologies, like hybrid bonding and 3D SoC, can be alternative or additional technologies for the memory devices intended for the HPC market. At the moment, both technologies are still in R&D for these types of applications (hybrid bonding is already used in CIS). We believe that 3D SoC will begin small-volume production in 2019, with TSMC as the first player to propose this technology (die-to-wafer).

Market growth forecast

The markets delivering exceptional growth these days tend to be in advanced packaging within the semiconductor sector, and one of the fastest-growing platforms is stacking technology. The stacking technology market is projected to register a compound annual growth rate (CAGR) of 26% from 2018 to 2024, to be valued at \$6.2 billion in 2024 [1].

Stacking technology in automotive will be the fastest-growing market for the next five years, with its market size expanding at a compound annual growth rate (CAGR) of 125% between 2018 and 2024. This is because higher computing performance will be required (edge computing), while still subject to stringent automotive regulations in terms of reliability. Adoption is expected in CIS, light emitting diode (LED), and devices in power applications for electric vehicle/hybrid electric vehicle (EV/HEV) needs, in the form of embedded die-in-substrate.

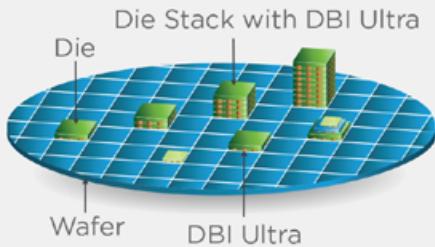
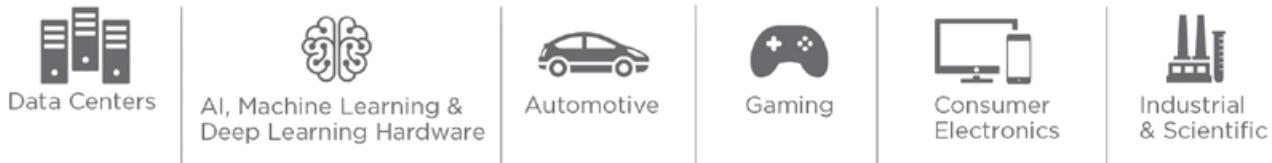
Stacking technology in the HPC and networking markets is showing strong development—securing the second highest growth at 34% CAGR from \$446M in 2018, to \$2,619M in 2024 [1]. This market comprises technologies such as 3D stacked memory (HBM and 3DS), 2.5D interposer, and 3D SoC. These technologies also provide a huge opportunity for telecoms/consumer market players to increase their presence in the enterprise market and to thereby sustain their long-term growth.



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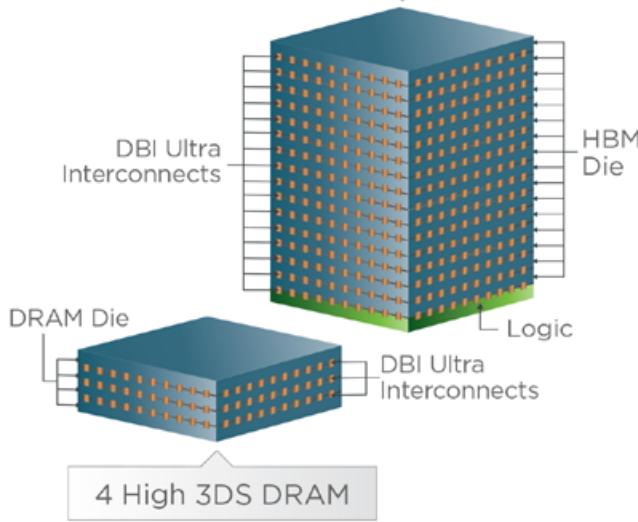
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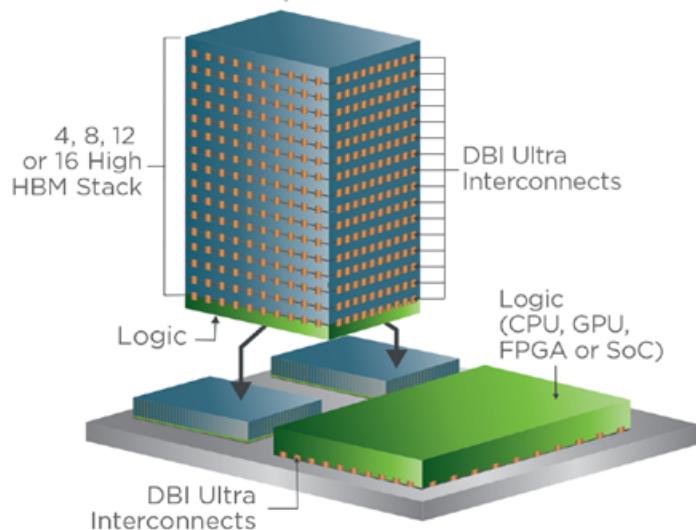
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There is also strong growth in the consumer market (gaming, augmented reality [AR], virtual reality [VR], mixed reality [MR], etc.) followed by other markets such as medical and industrial. Although the consumer market is a major market for stacking, the main growth driver is the need for high-bandwidth low-latency for big data computing calculations for HPC and data centers. These uptrends are underpinned by the rapid pace of digitalization and surge in demand for cloud-based services across the globe, which has prompted the giants to expand their infrastructure footprint to facilitate this remarkable market expansion. The medical market is a small one for TSVs, but the performance, form factor and reliability parameters are becoming more and more important.

The technologies discussed above are expected to form more overlaps—one example being TSV, hybrid bonding, and a combination of TSV+hybrid (**Figure 1**). In years to come, TSV technology will still be dominant, but it will lose market share to hybrid and combination technologies. This will be a consequence of the continuing hybrid bonding marketing and implementation in applications other than CIS, such as memory and 2.5D. In 2018, TSV and hybrid were mostly used in the mid-/low-end segment thanks to the CIS market. This situation will be more balanced by 2024, largely due to a 3 times faster high-end segment growth than the mid-/low-end segment, driven by artificial intelligence (AI) and data centers.

Commercialization of stacking technology

The rapid growth in demand for stacking technology for various end-markets represents opportunities for more innovation in both high-end and mid-/low-end applications (**Figure 2**). TSV, 3D stacked (3DS) memory, 3D SoC and 3D sequential integration are classified as high-end applications. Separately, CIS, LED, MEMS, and sensors are classified under low-/mid-end applications.

Both high-end and mid-/low-end markets are covered in a full report by Yole [1]. In this article section, only the high-end market is discussed. The high-end market segment has its specific requirements, such as lower latency and faster access, lower

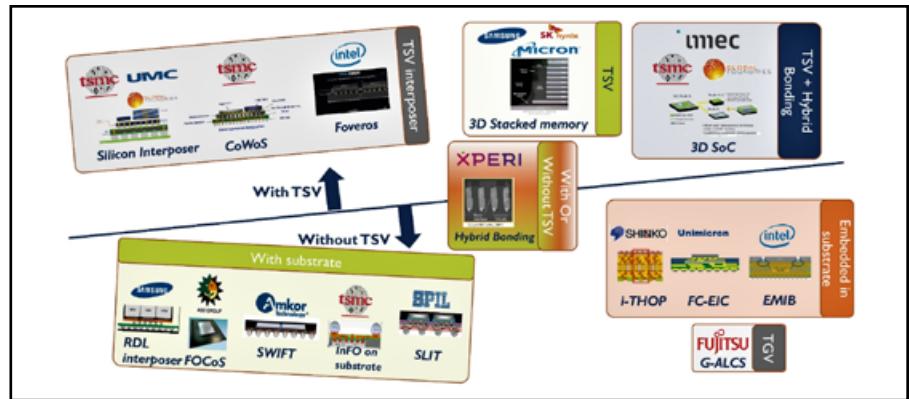


Figure 1: 2.5D and 3D stacking technologies: with or without TSV – foundries vs. IDMs vs. OSATS battle [4].

power consumption, smaller footprint and higher I/O count (**Figure 3**). To realize this high-end performance, 3DS memory and 2.5D with HBM are the common solutions being adopted and utilized in high-performance computing and networking.

There are two types of stacked-memory technologies, both TSV-centric, commercialized in the market. They are 3DS and HBM. 3DS is a type of memory that uses DDR4 DRAM stacked chips and operates as stand-alone memory for HPC and data center markets. 3DS memory has several DDR4 DRAMs interconnected using TSV technology. It can have a total capacity of 64 or 128GB, though Samsung announced availability in a 256GB configuration back in October 2018. HBM is another type of memory that often combines with other devices such as GPUs, CPUs or field-programmable gate arrays (FPGAs) on top of a 2.5D interposer. HBM memory is also a TSV-based device, where 2/4 and 8 DRAMs are interconnected via TSVs. Samsung has just announced a 12 DRAM stack. We can see 1/2/4/6 HBM devices

around a processor in a system dedicated to HPC.

Solutions for 3D stacking and advanced packaging are widely used in the gaming sector. The GPU on interposer is the application for TSV and TSV interposer in this segment. The purpose of using TSV technology in gaming is to optimize performance and have better gaming resolution and responsiveness. The GPU prices for gaming can vary from several hundreds to several thousands of dollars. Gamers and professionals are ready to pay such amounts in order to have an extraordinary experience, or to facilitate their daily tasks. For VR, no advanced packaging is needed to interconnect the organic light-emitting diode (OLED) display with its driver, as the display is grown directly on the thin-film transistor circuit wafer. For AR/MR, micro-LEDs are needed to achieve the required brightness. Advanced packaging solutions are needed to hybridize the display onto its driving circuit. Hybrid bonding seems to be a good candidate for such applications. AR/MR products are not yet on the market but are still in R&D.

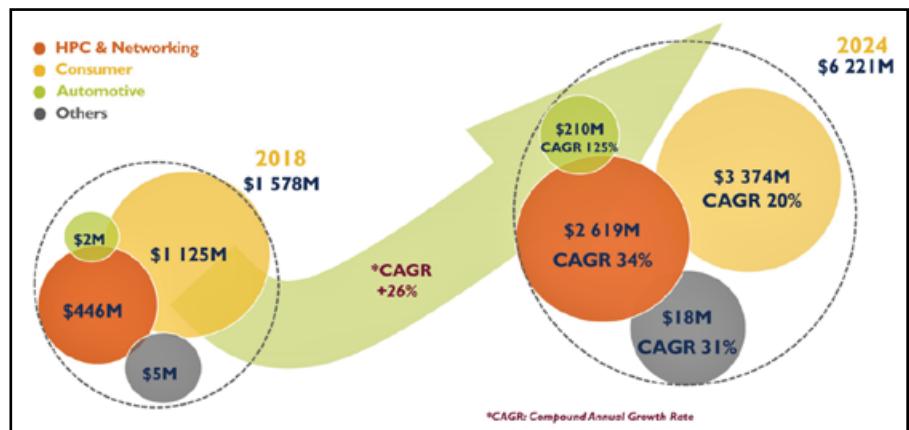


Figure 2: Stacking technologies, packaging revenues repartition per market [4].

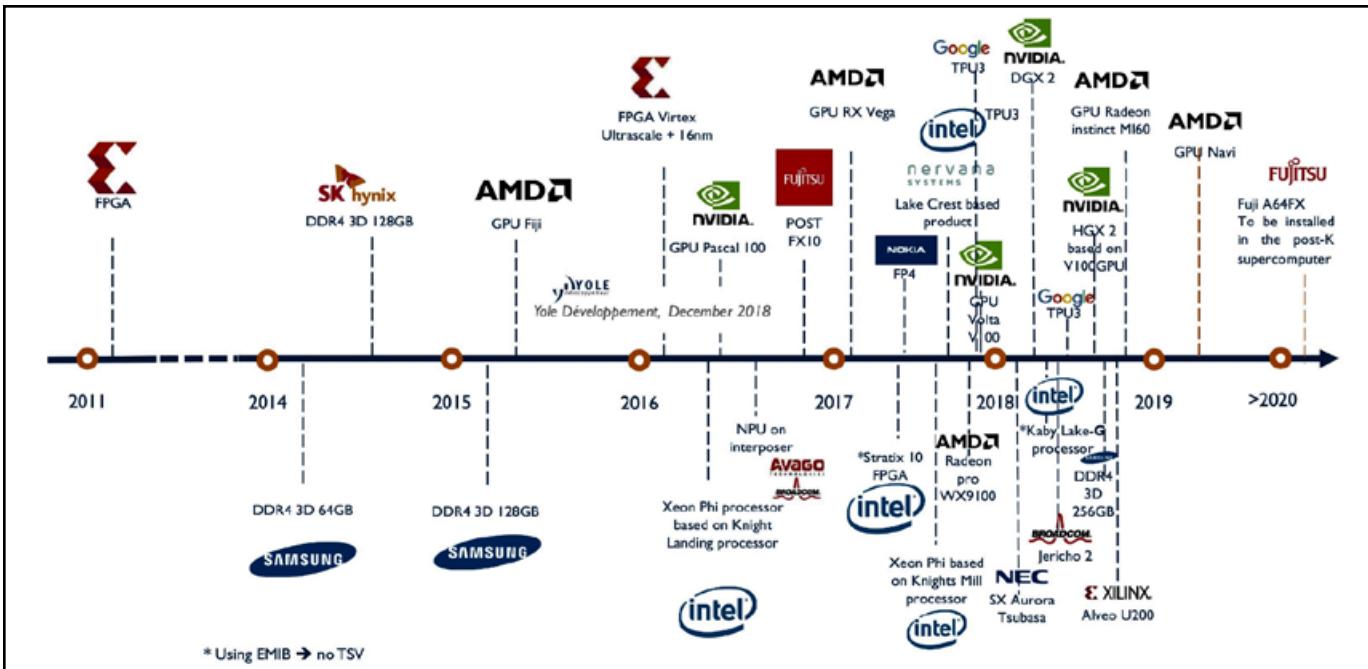


Figure 3: High-end hardware using stacking technologies, products launch [4].

Chip-on-wafer-on-substrate (CoWoS) technology is already widely used for HPC applications, and new TSV technologies will hit the market in 2020. An example is Foveros from Intel, which is based on “active” TSV interposer and 3D SoC technology, with hybrid bonding and TSV interconnections. The Foveros example shows that, although TSV is being challenged by non-TSV technologies, companies still have faith in it.

Separately, other technologies like hybrid bonding and 3D SoC are gaining traction. Hybrid bonding was originally used in CIS. Hybrid bonding can bridge the two main categories (with TSV/without TSV). This technology can simultaneously be competition and complementary to TSV. Since 2016, it started being used in CIS in smartphones, and in the near future it will enter the high-end market segment for memory and 2.5D as an interconnection solution. 3D SoC is a clever partitioning or split of a single-die SoC into two or more parts, each realized by optimum technologies at lower cost per function, and then recombining the SoC using high-density 3D interconnect processes.

3D sequential integration technology is also known as 3D monolithic and 3D VLSI (very large scale integration). CEA recently announced that it is getting closer to commercialization. The applications will be computing and sensor interfacing.

It is now not possible to exclude the emergence of stacked TSV-less technologies in the market. These innovations can be divided into two groups: “with substrate” and “embedded-in-substrate.” Embedded multi-die interconnect bridge (EMIB) technology, already commercialized, is part of the embedded-in-substrate group, where the Si bridge is deep-seated in the substrate. Other substrate technologies are being developed, but are still not in the market, e.g., I-THOP and Flip-chip Embedded Interposer Carrier (FC-EIC®). With-substrate technologies are also used as alternatives to TSV, for example InFO-on substrate, which is used for networking chips from Mediatek, and possibly also HiSilicon. Also, RDL interposer technology is currently being developed and will hit the market by 2020. Last, but not least, FoCoS was developed and commercialized in 2016.

Competitive landscape

Four different types of players want to claim a share of the growing \$6.2B stacking market [1]. Foundries, integrated device manufacturer (IDMs), OSATS, and intellectual property (IP) companies all want their share of the stacking business (**Figure 4**).

Intel was known to be a non-TSV company with the introduction of “EMIB” TSV-less technology, but things have changed. Currently, Intel is the

only IDM that is trying to compete in the stacking sector with “Foveros” TSV-based technology. Foveros takes things a step further in 3D stacking by enabling logic-on-logic integration, which goes beyond traditional die stacking with passive interposers and stacked memory. This will work with high-performance logic circuits, like CPU cores, GPUs, AI processors, etc. Foveros technology can potentially become an \$80M packaging market by 2025 if this technology enters the 2.5D packaging market and is adopted by more applications. As with any new technology, the volumes for the first 2-3 years will be low. Based on the adoption (or not) of this technology, the numbers can drastically change in the future.

In the 3D-stacked memory market, the battle is between the big three IDMs: Samsung, SK Hynix, and Micron. These will continue to reign supreme in the stacked-memory market. Today, Samsung is leading the market with >70% share, followed by SK Hynix and Micron. These three companies are able to handle the full 3D-stacked memory manufacturing process. Currently, Micron is not running high-volume manufacturing (HVM) for HBM, so it depends mainly on Samsung and SK Hynix for an increase in the production volume of HBM.

Type	Company	Technology name	With TSV	Without TSV	With Substrate	Without Substrate	Embedded in Substrate	Stacking technology
Foundry	 	CoWoS	★		★			
		InFO on substrate		★	★			
		3D SoC	★			★		
		TSV interposer	★		★			
IDM	   	3D stacked memory	★					2.5D
		RDL interposer		★	★			3D
		Foveros	★		★			
		EMIB		★	★			
OSAT	 	FOCoS		★	★			2.5D
		SWIFT		★	★			
		SLIT		★	★			
Substrate manufacturer	 	i-THOP		★	★			2.5D & 3D
		FC-EIC		★	★			
IP		Hybrid Bonding	★	★	★	★		

Figure 4: Stacking technologies — key elements for differentiation [4].

Foundries, like TSMC, UMC, and GLOBALFOUNDRIES, dominate the TSV heterogeneous stacking technology market on account of their ability to produce the interposer in-house. 3D SoC is a foundry technology and as such, TSMC is leading the time-to-market race ahead of GLOBALFOUNDRIES. TSMC is expected to be the first to get a product to market, in 2020 (die-to-wafer, memory-on-logic). It will be able to ramp up the production very quickly if a client shows an interest in this technology. TSMC wafer-on-wafer (WoW) technology will be based on SoC wafer stacking using hybrid bonding and is intended for data center usage [2]. HiSilicon (Huawei) may be their first client, with AMD also a potential client.

For the TSV-less technologies, the game is a bit more engaged between foundries, IDMs, OSATS, and substrate makers. Some players, like Samsung, Intel, and TSMC, are involved in “with” and “without” TSV technology development. ASE (an OSAT) introduced its FOCoS technology to the market in 2016, while other players like Amkor

Technology, Inc., have developed their proprietary technology, but are still awaiting orders. The substrate companies, like Shinko, Unimicron, and lately, Fujitsu Interconnect, are still in R&D.

Many OSATS and intellectual property (IP) companies, such as Xperi, are developing their proprietary technologies that can, and may continue replacing TSV in the near future [3]. The competition will be tough in the coming years for TSV technologies. Each type of hardware dedicated to HPC and using TSV technology (GPU, CPU, application specific integrated circuits [ASICs], neural processing unit [NPU], etc.) has its advantages and drawbacks vs. other hardware. Each application is specific and requires dedicated hardware, so no hardware configuration is really better than another. Foundries, IDMs, and IP companies have the advantage over OSATS in stacking technologies thanks to their expertise in wafer-level processing, because the latter encounter difficulties in obtaining orders. This type of technology development is capital-intensive, which is the main roadblock for OSATS.

Acknowledgements

This article has been written in collaboration with Santosh Kumar, Principal Analyst & Director Packaging, Assembly & Substrates, and Mario Ibrahim, Technology & Market Analyst at Yole.

References

1. 2.5D / 3D TSV & Wafer-Level Stacking: Technology & Market Updates report, Yole Développement, 2019.
2. *TSMC's announcement: TSMC will manufacture 3D stacked WoW chips in 2021 claims executive*, posted on i-Micronews.com, April 2014.
3. *Hybrid bonding, an enabling technology, from CMOS Image Sensors to Memory & High-Performance Computing – Interview of Xperi* posted i-Micronews.com, March 2019.
4. 2.5D/3D TSV & Wafer Level Integration Technology & Market updates report, Yole Développement.



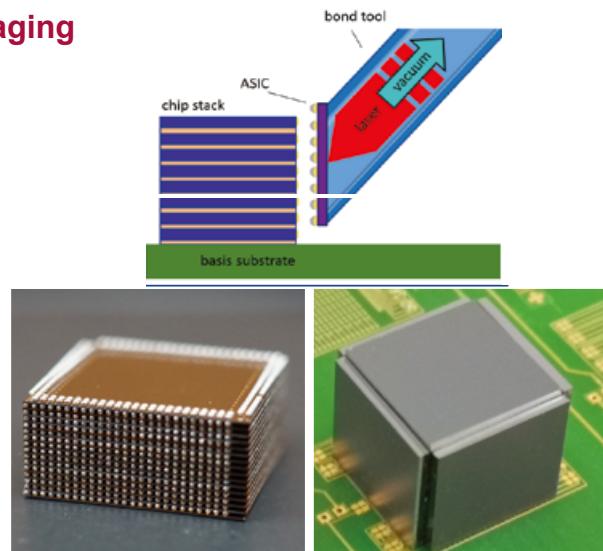
Biography

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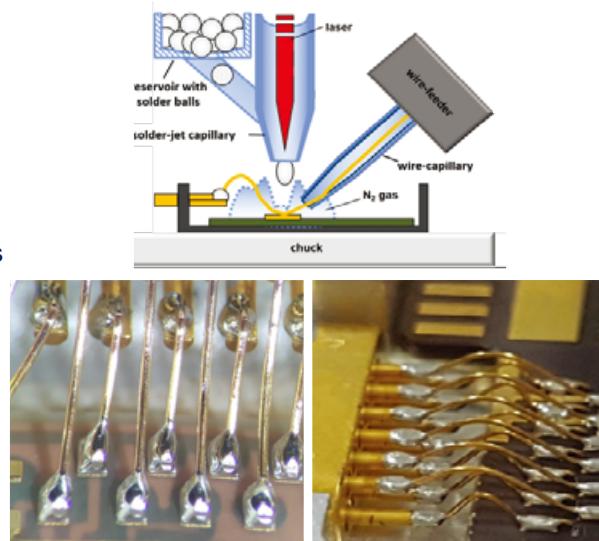
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Fluxless wafer bumping by micro-ball placement

By C. Christine Dong [Air Products and Chemicals, Inc.]

W

afer bumping is a process of forming solder bumps on electrode pads of entire wafers. This process is often divided into two categories: one is for flip-chip (FC) packaging, and another is for wafer-level chip-scale packaging (WLCSP). Bumps on flip-chip packages are typically in the range of 50 to 200 μm in height, while bumps for the WLCSPs are normally in the range of 200 to 500 μm in height. Commonly used solder deposition methods for wafer bumping are paste printing, electroplating, and ball placement. For each different application, a suitable solder deposition method must be selected. For example, paste printing has a low cost, but cannot be applied for fine-pitch micro bumps. In addition, voiding is inevitable due to a significant amount of nonmetallic content inside the paste. Electroplating is more suitable for depositing fine-pitch micro bumps, however, it is relatively expensive, and it is not suitable when bump size is larger than a certain value. As a comparison, the ball placement method for solder deposition can be applied for a much larger range of bump sizes, such as from 50 μm to 500 μm . Other key advantages of the ball placement method include high throughput, good bump uniformity, low cost, and reduced chemical pollution.

The first step of the ball placement process is depositing an organic flux on the wafer pad areas, which can be done by pin transfer or stencil printing. Preformed solder balls are then placed on the flux deposits all over the wafer simultaneously, such as by stencil printing or vacuum transfer. After the ball placement, the whole wafer goes through a reflow step. During this step, the initial oxides on the surfaces of the solder balls and electrode pads are cleaned by the organic fluxes, and then the solder balls are melted, thereby forming a metallic bond between the solder bumps and metal pads. The reflowed wafers will also need to go through a post-cleaning step to clean flux residues that remain on the wafer surface.

With the industrial trend moving toward device miniaturization, the pitch size of the solder bumps is continually shrinking. As

a result, flux residues tend to be trapped between solder bumps, making the post-cleaning step ineffective. Therefore, a fluxless technology is highly desirable. The current study is related to a new technology of wafer bumping that is achieved by micro-ball placement without using organic fluxes. More specifically, a residue-free locating agent is developed to hold the solder balls placed on the electrode pads. In addition, a production-scale reflow furnace containing a hydrogen activation function is used to reflow the wafers in a non-flammable gas mixture of hydrogen (<4 vol%) in nitrogen. Initial oxides on solder balls and electrode pads can be effectively removed under the activated hydrogen at ambient pressure and below the solder's melting point. It is demonstrated in this study that by using this fluxless approach, a good solder ball wetting can be achieved, and the surface of the reflowed wafer is free of foreign materials without the need of the post-cleaning step.

Experimental method

The wafers used in this study to demonstrate the fluxless wafer bumping process by micro-ball placement were supplied by a customer in the semiconductor industry. Metal layers were

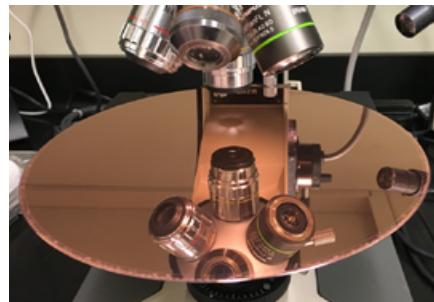


Figure 1: Non-patterned copper wafer used in the ball placement study herein.

uniformly formed on the entire silicon wafer surface with a plated copper layer on the top (Figure 1). The thickness and composition of each metal layer were made exactly the same as that of electrode pads on a real product wafer that this customer would typically use. Each wafer was diced into 25mm X 25mm squares as substrates for ball placement and reflow tests. Atomic force microscopy (AFM) was used to check the roughness of the plated copper surface on the wafer (Figure 2). The root-mean-square roughness value for the copper surface is around 20nm.

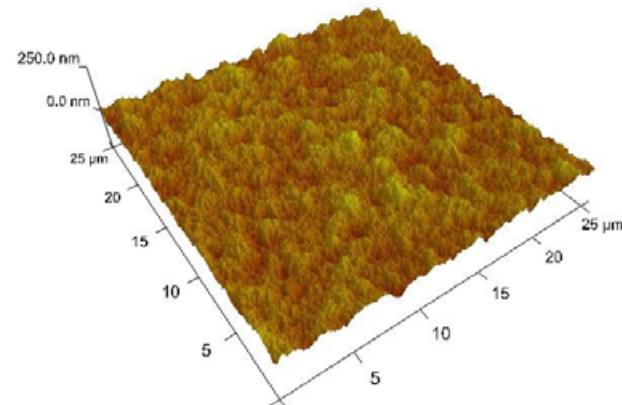


Figure 2: A surface roughness on the copper wafer of about 20nm.

For proving the concept, 400 μm solder balls with a composition of SAC305 (3.0% silver and 0.5% copper to tin balance) were used in this study. The melting point of the solder is 217 to 220°C. A proprietary locating agent was developed to replace the organic fluxes for holding each solder ball on the copper substrate. A pin transfer method was used to deposit the locating agent. More specifically, a fixture containing an array of 16 X 16 metal pins was made to transfer the liquid from a container to each copper substrate. After depositing the locating agent, solder balls were placed on the liquid deposits by using a metal sieve.

A production-scale reflow furnace containing the hydrogen activation function was used in this study. More specifically, the activation of hydrogen gas molecules

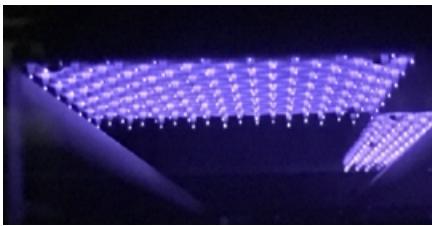


Figure 3: Electron emission apparatus mounted inside the furnace.

is achieved by electron attachment (EA). This novel gas activation technology was developed by Air Products in recent years [1-3] and involves generating a large quantity of low-energy electrons by an electron emission apparatus mounted inside a furnace (Figure 3). Some of the generated electrons can attach to hydrogen molecules and form active species. The reflow furnaces using the EA technology have been manufactured by a furnace manufacturer and have been certified and tested for applications related to fluxless solder reflow [4-5]. The open tunnel furnace contains a roller-featured transportation system, which is capable of transferring 300mm wafers from the entrance to the exit of the furnace. The transportation speed can be adjusted based on specific need. The furnace contains eight zones, including five independently-controlled heating zones, two cooling zones, and one isolation zone at the entrance. The five heating zones include two preheating zones, two EA zones mounted with the electron emission devices, and one reflow zone. The EA zone temperature is typically at a point below the solder's melting point. The maximum temperature at the reflow zone can reach 400°C. Under a forming gas (4 vol% H₂ in

N₂) environment, the oxygen level inside the furnace is normally below 5ppm.

For each test condition, three samples of diced copper wafer substrates with placed solder balls were arranged across the diameter of a 300mm carrying wafer. The wafer was then sent into the reflow furnace with its moving direction perpendicular to the direction of the sample arrangement (Figure 4). Using this arrangement, the quality of the solder reflow across the width of the furnace can be investigated. Before entering the reflow zone, samples are exposed to the activated hydrogen at the EA zones where oxides on the solder balls and the copper substrates are removed at a temperature below the solder melting point, thereby facilitating solder wetting when the samples enter the reflow zone.

Results

During the experiments, each sample was prepared by using the above described liquid deposition and ball placement methods. Figure 5 shows the 16 X 16 array of the transferred locating agent on the copper wafer substrate that was 25mm X 25mm in size. Figure 6 is a side view of the solder ball (400μm) array on the copper wafer substrate before solder reflow. It illustrates that each solder ball is fixed by the deposited locating agent.

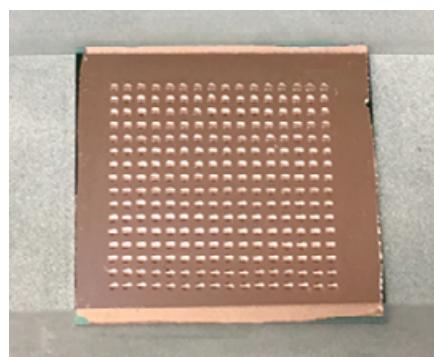


Figure 5: A 16X16 array of the transferred locating agent on the copper wafer substrate.

During each reflow process, test samples were exposed to the activated hydrogen in the

EA zones at a temperature below the solder melting point. After cleaning the initial oxides on the solder balls and the copper substrates, the samples entered the reflow zone at a temperature above the solder melting point. As an example, 100% ball attachment on

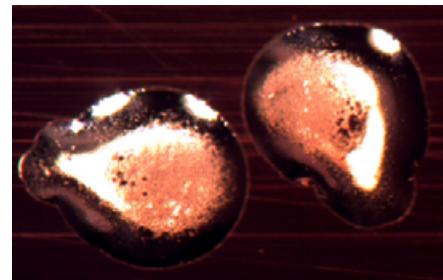


Figure 7: Achieved by EA-based reflow, the figure shows wetted solder balls on the copper wafer surface without residues.

the copper wafer surface was achieved for an EA-based reflow at 260°C peak reflow temperature. As shown in Figure 7, irregular wetting shapes were formed on the substrate

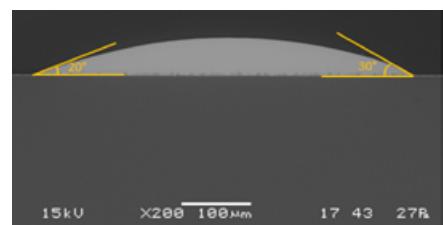


Figure 8: Achieved by EA-based reflow, the figure shows a wetting angle of around 20-30 degrees.

surface. This is because the substrate used in this study is from a non-patterned blank copper wafer, unlike the normal cases of having copper pads on a wafer that constrain solder spreading. Figure 7 also shows that the

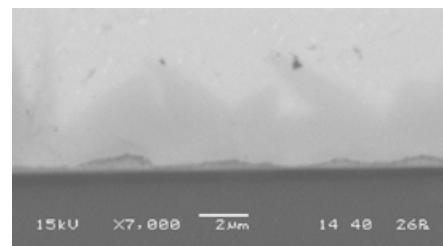


Figure 9: Achieved by EA-based reflow, an IMC layer of around 2-3μm was formed.

copper wafer surface is quite clean without residues. A cross-section analysis of the sample by scanning electron microscope (SEM) shows that the wetting angle is around

Moving direction

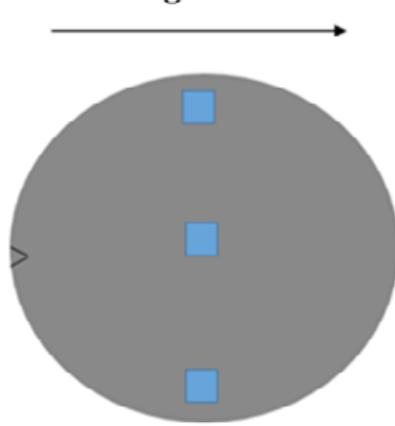


Figure 4: The moving direction is perpendicular to the direction of the sample arrangement.

Figure 6: Side view of the solder ball array on the copper wafer substrate before reflow, showing each ball fixed by the deposited locating agent.

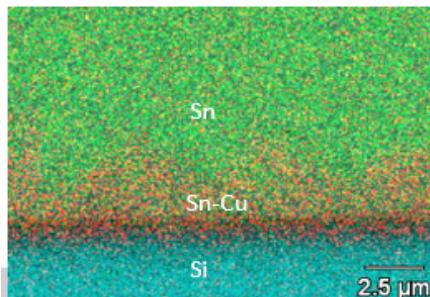


Figure 10: Achieved by EA-based reflow, the composition of the formed IMC layer is tin and copper.

20 to 30 degrees (**Figure 8**). By increasing the magnification of the SEM, one can see a formed intermetallic compound (IMC) layer around 2 to 3 μm (**Figure 9**). **Figure 10** shows the result of an energy-dispersive X-ray (EDX) analysis, which indicates that the composition of the IMC layer is tin and copper.

As a comparison, when EA was not applied during the same reflow condition, solder wetting on the copper wafer

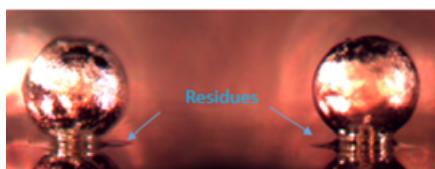


Figure 11: Non-wetting of solder balls and residues occurred when EA was not applied during reflow.

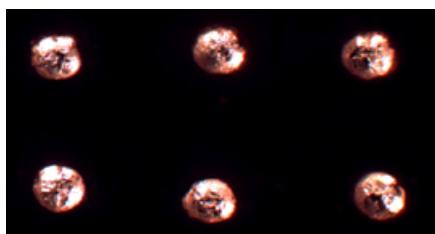


Figure 12: The figure shows a top view of non-smooth solder balls formed when EA was not applied during reflow.

surface couldn't be achieved and residues were formed around the bottom of the solder balls (**Figure 11**). In addition, the top surface of the reflowed solder balls was not smooth (**Figure 12**). By SEM analysis, it was found that the wetting

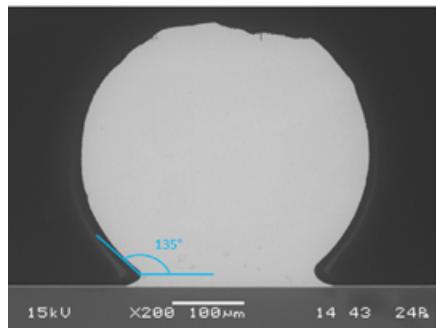


Figure 13: A wetting angle of around 135 degrees is obtained when EA is not applied during reflow.

angle is around 135 degrees (**Figure 13**). By increasing the magnification of the SEM, no IMC layer was detected between the solder and the substrate (**Figure 14**), indicating a weak bonding.

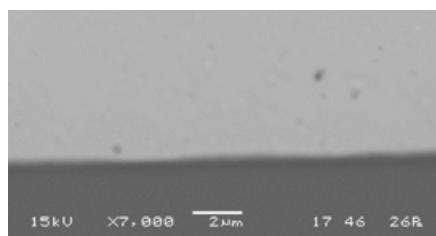


Figure 14: There is no IMC layer when EA is not applied during reflow.

Summary

A technology for fluxless wafer bumping by micro-ball placement is introduced in this study. To replace organic fluxes, a residue-free locating agent is developed that can be deposited by the pin transfer method. The results presented above demonstrate that the locating agent performs well for deposition and holding solder balls on the copper wafer surface. By applying EA-activated hydrogen in a forming gas environment, initial oxides on the solder balls and copper surface can be effectively removed before the solder gets melted, thereby resulting in 100% ball attachment with a good solder

wetting and a strong solder bonding to the wafer. In addition, the locating agent can be effectively decomposed in the EA-activated atmosphere without leaving residues, thereby eliminating the need for a post-clean. In contrast, without applying EA during the same reflow condition, the solder wetting is very poor and the decomposition of the locating agent is not completed.

Acknowledgments

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References

1. C. C. Dong, R. E. Patrick, E. J. Karwacki, “无助焊剂焊接的新突破：氢离子回流焊,” (“A new breakthrough in fluxless soldering: reflow soldering by ionic hydrogen”), SMT China, April/May 2013, pp. 23-30.
2. C. C. Dong, R. Siminski, “Fluxless die attach by activated forming gas,” Proc. of IPC 2013, San Diego, CA, Feb. 19-21, 2013, vol. 3, pp. 1900-1929.
3. C. C. Dong, R. E. Patrick, R. A. Siminski, T. Bao, “Fluxless soldering in activated hydrogen atmosphere,” Proc. of CSTIC 2016, Shanghai, China, Mar. 15-17, 2016, VIIA 1520-1535.
4. C. C. Dong, R. E. Patrick, G. K. Arslanian, T. Bao, K. Wathne, P. Skeen, “Production-scale flux-free bump reflow using electron attachment,” Proc. of CSTIC 2017, Shanghai, China, Mar. 12-13, 2017, VII-0940-0955.
5. C. C. Dong, F. Yu, T. Bao, W. Zhang, F. Dai, D. Yang, “Fluxless bump reflow in activated hydrogen atmosphere,” Proc. of ICEPT 2018, Shanghai, China, Aug. 8-11, 2018, paper 178.

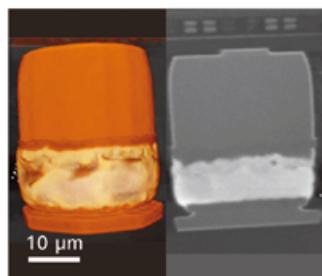
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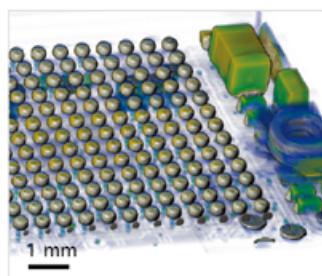
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Seeing beyond

Evaluating a spring probe card solution for 5G WLCSP

By Krzysztof Dabrowiecki [Feinmetall GmbH], Thomas Gneiting [AdMOS GmbH], Jose Moreira [Advantest]

W

ith the deployment of the wireless 5G standard and its support for mmWave frequencies that allow gigabits-per-second data rates on the consumer market, the semiconductor industry needs reliable and low-cost test solutions. The 5G standard allows mmWave range frequencies from 24GHz to 28GHz—to frequencies as high as 44GHz, and possibly even higher. To achieve these frequencies requires reliable, highly efficient, cost-effective chip packaging technology. From that point of view, wafer-level chip-scale packaging (WLCSP) offers one of the most compact package footprints, providing a high level of functionality, and a frequency range with low resistance and inductance path. Despite having a good thermal performance with a finer pitch interconnection to the printed circuit board (PCB), WLCSP is resilient to extreme variations in stress, drop, and vibration. At the wafer test level, WLCSP technology requires a good and consistent contact resistance, a relatively high contact force with short probes, and above all, an effective online cleaning together with easy onsite repair [1]. With respect to those electromechanical wafer test requirements and with added value such as a frequency performance higher than 28GHz, or a high current capability, the spring pin probe card technology is always a favorite on the test floor on account of its cost and versatility and worthwhile to evaluate for high-frequency 5G mmWave applications [2-4].

To define the best possible probe card structure, detailed electromagnetic simulations and analyses are required. RF engineers have several modeling approaches available for this type of simulation, such as a lumped element model (SPICE), distributed element model, or 3D electromagnetic (EM) models. For this study, it was decided to utilize CST Studio Suite 3D EM simulation software. It allows us to build and analyze an exact and detailed 3D-model of the probe card. A probe card acts as an interconnector on the signal transmission path between the wafer chip and automated test equipment (ATE). Therefore, it is vital to keep in mind that, besides the probe

card, there are other challenges with respect to ATE and the PCB side.

On the ATE side, mmWave frequencies already present significant implementation challenges, including the measurement instrumentation and interconnect to the ATE device under test (DUT) test fixture PCB. **Figure 1** shows a picture of the bottom of an ATE mmWave test fixture, where it is possible to observe the blind

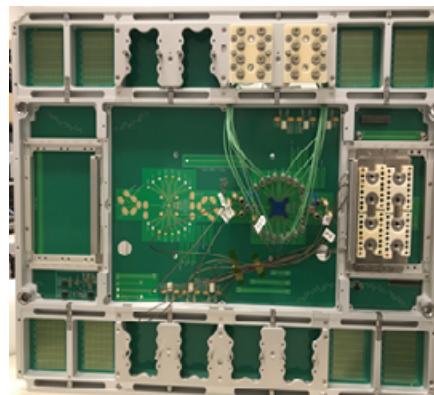


Figure 1: Bottom side of a mmWave Advantest V93000 ATE test fixture for socket testing of a 5G mmWave device.

mating connectors to the ATE system and the coaxial cables. They are connected to coaxial connectors, very close to the socket. The use of coaxial cables in the test fixture is essential because a coaxial cable is significantly less lossy than any PCB signal trace. The PCB test fixture

challenges, however, are not the main subject of this paper.

The system assembly and modeling (SAM) framework was used to investigate and optimize a signal path. It consists of multiple individual components, such as wafer bump, probe head, and PCB. These are described by relevant physical quantities such as field magnitudes or s-parameters. This paper is trying to find an answer and explore three objectives: 1) the impact of different materials and probe head designs on the mmWave performance, 2) analysis of s-parameters and crosstalk, and 3) the probe head design optimization to improve them. Crosstalk is also an important parameter that is taken into account. The presented analysis results reveal the impact of different structure probe head elements on the s-parameter results.

Simulation model

Figure 2 shows an example of what mmWave RF peripheral ports (AN1, AN2) might look like on a 5G DUT. The diagonal bump pitch is 0.4mm, with a bump height of 100mm. The distance, in a row, between RF bumps is 0.566mm. Initially, a spring pin was chosen with uncompressed length

GND		AN1		AN2		AN3
	GND		GND		GND	
PWR		PWR		PWR		PWR

Figure 2: The mmWave RF ballout.

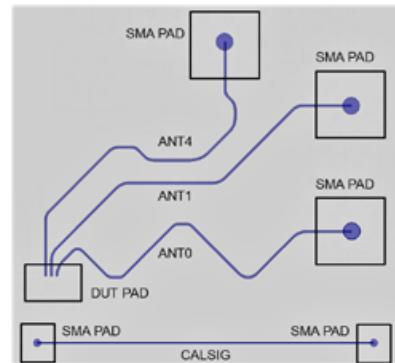
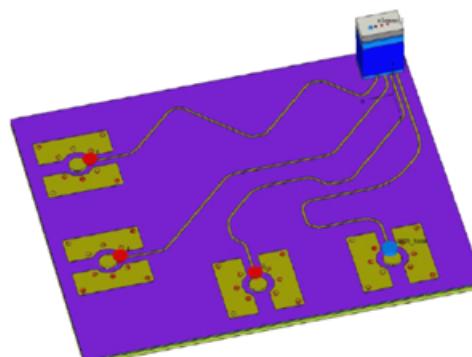


Figure 3: A quarter of the probe card model and traces layout.

$L=3.7\text{mm}$, at working mode $L_1=3.5\text{mm}$. The PCB thickness was 3.8mm and used a hybrid stack-up of the FR4 and Tachyon 100G for dielectric material. The matched trace lengths were designed at 38.8mm . Because of the symmetrical PCB traces layout, the simulation was performed for the critical traces only and one-quarter of the PCB.

The RF 3D model analysis includes the wafer solder bump, probe head, and contact with the PCB, in which the traces are included up to the connector locations. **Figure 3** illustrates a quarter of the probe card model and trace topology.

Figure 4 shows a model of a probe head in contact with the wafer at the bottom and the PCB at the top. The probe

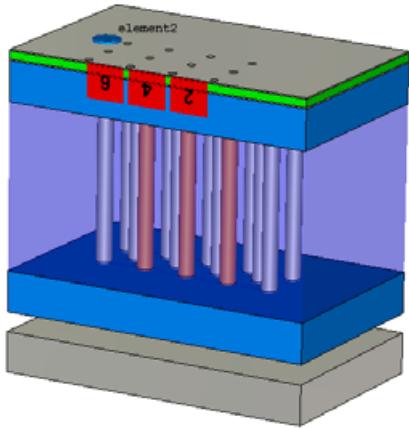


Figure 4: Model of an RF probe head.

head is a 2-layer structure comprising guiding plates and fillers between the plates. The filler layers are the additional materials added between the guiding plates with various dielectric constants and loss tangent. The double plunger spring pins are inserted into drilled holes in the guiding plates and fillers. The pin plunger protrusions at the working mode are formed with a uniform air gap of 0.1mm between the head and the PCB, and 0.25mm between the head and wafer. The created 3D simulation model allows quick verification of results to identify appropriate material properties and geometry before building a test probe card.

Initial simulation results

It is well-known that any impedance mismatch in the signal path will have an impact on the return loss and in that way, degrade the measurement path performance. Therefore, impedance

is a crucial parameter to be checked and controlled. In the PCB industry, the common impedance specification is in the range of $50 \pm 10\text{ Ohm}$ for a single-ended signal. But 5% is possible in certain cases, though at a very high cost.

Figure 5 shows the simulated time domain reflectometry (TDR) plot for the model with various filler materials with a time rise of 29.2ps (for 30GHz). The dashed lines indicate the maximum and minimum impedance tolerances. In the figure, it can be noticed that

the air gap between the guiding plates causes an impedance discontinuity that peaks at 70 Ohms . The material option 1 shows a drop in the impedance discontinuity peak at 41 Ohm . The material B options 2 and 3 significantly reduce the impedance discontinuity to an acceptable range. As a consequence of material B air and option 1, the insertion loss and return loss had a limited frequency bandwidth, as shown in **Figure 6**. In this case, the dashed lines reveal acceptable limits of -1dB for insertion loss, and -10dB for return loss.

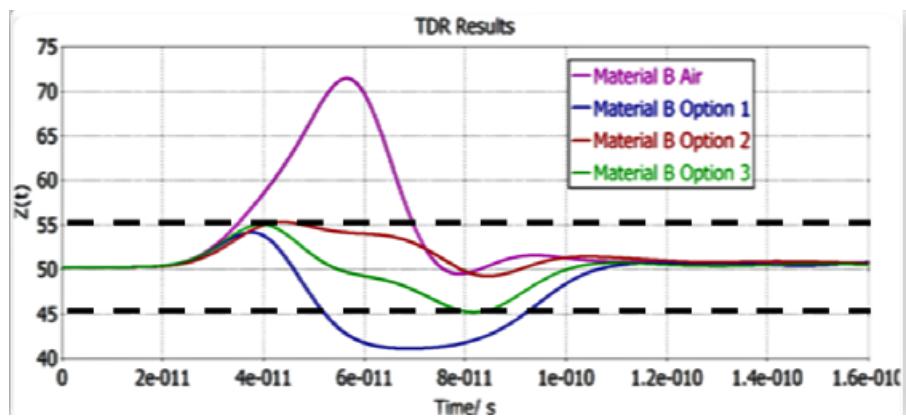


Figure 5: Model impedance plot.

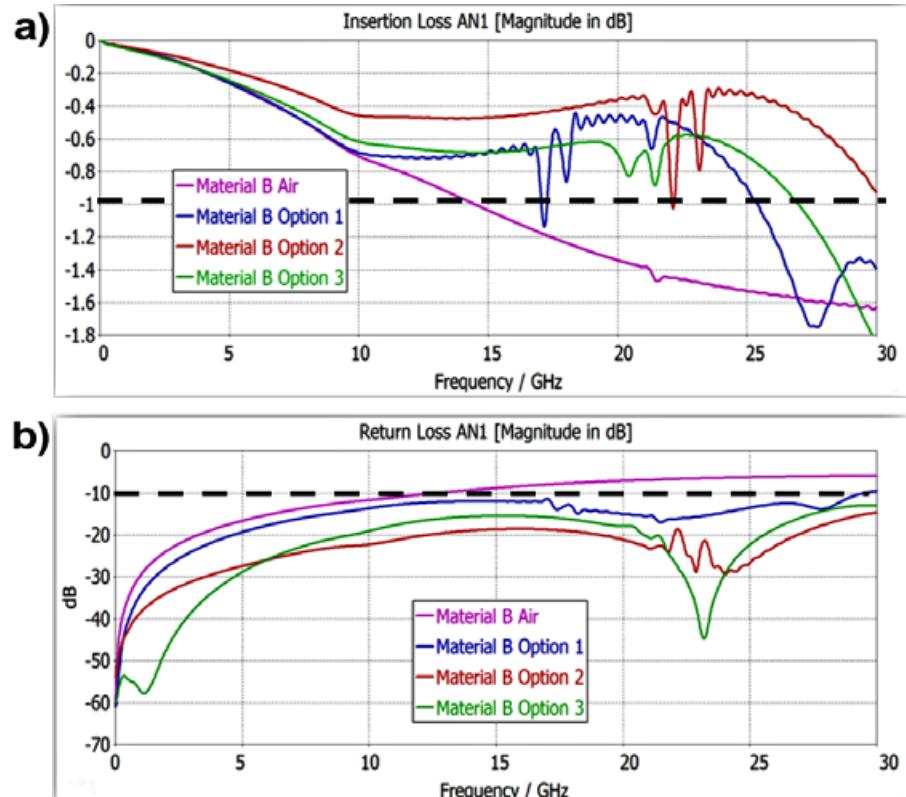


Figure 6: The a) (top) insertion and b) (bottom) return loss for the different material options.

Model optimization

To increase the simulation frequency range up to 50GHz or higher, it was necessary to optimize the probe head model further. For this task, several optimization options were identified and evaluated, such as minimizing the gap between the wafer and probe head, decreasing the gap between the PCB and probe head, reducing the spring pin length, and analyzing various RF and GND contact arrangements. After implementing different optimization options in the model, the impedance profile was simulated for three probe lengths: 3.5mm, 2.25mm and 1.85mm, with a rising time of 17.5ps (at 50GHz). The simulations were performed for an RF and GND configuration for ground-signal-signal-ground (GSSG).

As can be observed in **Figure 7**, the impedance discontinuity for the optimized model is reduced to below 55 Ohm for 2.5mm and 1.85mm probes only. The plots in **Figure 8** show the insertion loss and return loss results for all tested probes. Note that, the insertion loss and return loss are shown as negative numbers on account of the outcome of the simulation program. As expected, a shorter probe L=1.85mm shows the best performance—achieving an insertion loss at 44GHz of -1dB. Because of the shorter length, the resonances caused by the impedance mismatch shift to a higher frequency, which is also seen in the return loss diagram.

The next evaluation step was to arrange those spring pins with an additional shield between signals using pitches of 0.3, 0.4 and 0.5mm, and compare the outcome of the maximum reached frequency for each case. The summary of the simulated insertion loss is presented in **Figure 9**. The green curve depicts a probe length of 3.5mm, the red curve a length of 2.25mm, and the blue curve a length of 1.85mm. The maximum reachable frequency is based on two common assumptions: 1) the insertion loss must be below 1dB, and 2) the return

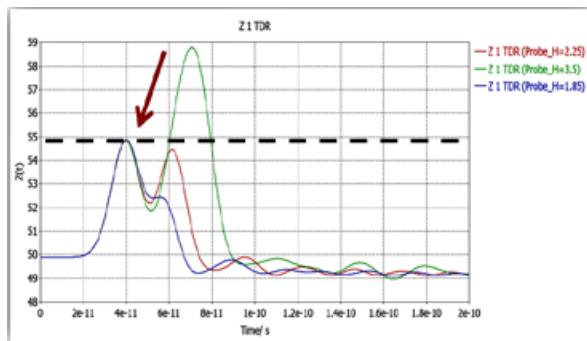


Figure 7: Optimized model impedance plot.

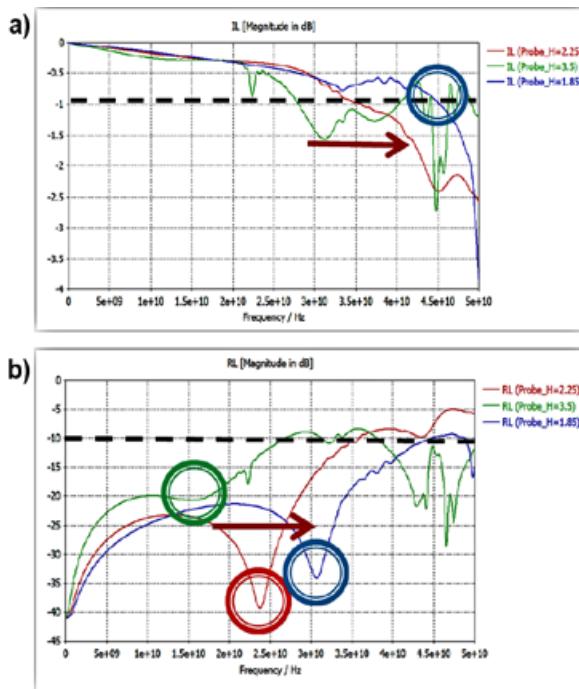


Figure 8: The a) (top) insertion and b) (bottom) return loss for probe lengths of 3.5mm, 2.25mm, and 1.85mm.

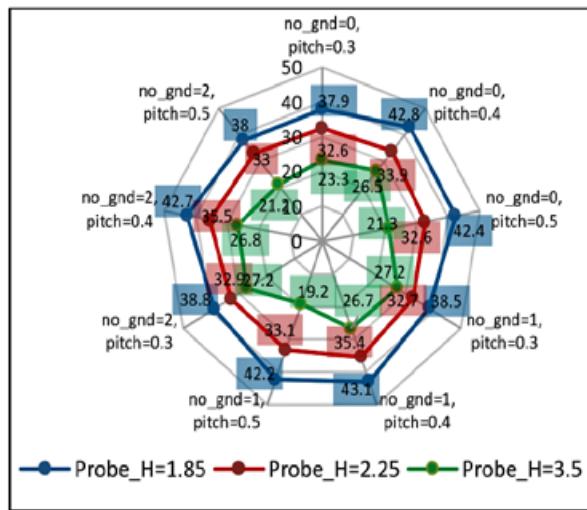


Figure 9: The insertion loss simulations for different probe lengths, pitches, and arrangements.

loss must be above 10dB. A further design parameter is the number of ground pins (no_gnd) between two signal pins. For a variation of these three arrangements of given probe geometries, the chart reveals the highest frequency of 43.1GHz for a probe length of 1.85mm and a pitch of 0.4mm with a ground-signal-ground (GSG) arrangement (no_gnd=1).

Figure 10 illustrates the EM simulation model used for the crosstalk simulation. It is essential to understand the behavior of a spring pin with respect to crosstalk at high frequency. It is crucial because each spring pin does not have a perfect coaxial shield around it. A configuration of a probe with length 2.25mm and one ground pin between the signal pins (aggressor and victim) was considered for this analysis.

As outlined in **Figure 11**, the electrical and magnetic fields were calculated at 25GHz and 43GHz. In this diagram, it can also be noticed that an increase of ground pins between the signal pins leads to a reduction of crosstalk below the first resonance. However, above the first resonance frequency, the crosstalk is independent of the number of ground pins. The explanation of the electrical field behavior at 25GHz has been presented in **Figure 12**, and at 43GHz in **Figure 13** in a cross-section through the probes. A red circle marks the aggressor pin, while the victim pin is shown in blue.

At 25GHz (**Figure 12**), below the first resonance frequency around 35GHz, ground pins are showing a shielding behavior in the electrical field and are protecting the victim pin. The magnetic field, which is not shown here, has a similar action. The high-strength electrical field is limited only to nearby and surrounding pins. However, at 43GHz (**Figure 12**), above the first resonance frequency, it can be observed that ground pins provide a less effective shielding for the victim. The electrical field goes far beyond the surrounding pins of the aggressor, and some of the field lines are reaching the victim pin.

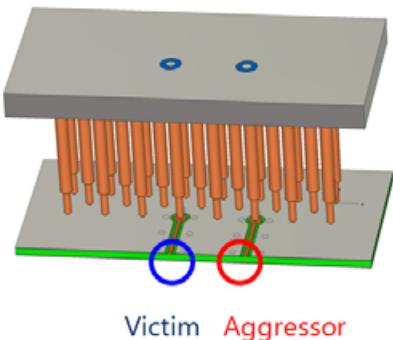


Figure 10: EM spring pin crosstalk model.

Summary

This paper shows that the spring pins solution is feasible for 5G WLCSP (28-42GHz) applications. The presented simulation and optimization of the probe head shows the importance of using 3D-EM models to understand and better predict the probe card behavior at high frequency. The study shows a margin for probe head design improvement, including spring probe design.

Of course, because of its inherent physical design, spring pin technology will

always have drawbacks at high frequencies compared with other probe technologies, and a lower performance. But its versatility in terms of repair and cost makes it the preferred solution with most test engineers for high-volume production testing. The question then becomes, will a spring pin probe head provide enough failure coverage to test a DUT. This paper shows that it is possible to address some of the high-frequency challenges associated with spring pin types of probe heads. It is also important to stress that the probe head only defines a part of the signal path performance. The PCB design and interconnect to the ATE are equally critical factors. Very often, the choice of the right probing solution for 5G WLCSP applications depends on the floor test objectives, volume, cost, lifetime, and maintenance. For that reason, the spring probe solution could be a good and reasonable alternative.

References

1. K. Dabrowiecki “FeinProbe solution for WLCSP applications,” SWTest Workshop, San Diego 2017.
2. J. Sherry, “Testing of high-frequency 5G applications and why simulations are critical to success,” *Chip Scale Review*, Mar-Apr, 2019.
3. J. Mroczkowski, D. Campion, “Production test interface solution for mmWave and antenna in package (AiP),” *Chip Scale Review*, Jan-Feb, 2019.
4. D. Bock, J. Damm, “New test methodologies for 5G wafer high-volume production,” *Chip Scale Review*, Jan-Feb, 2019.

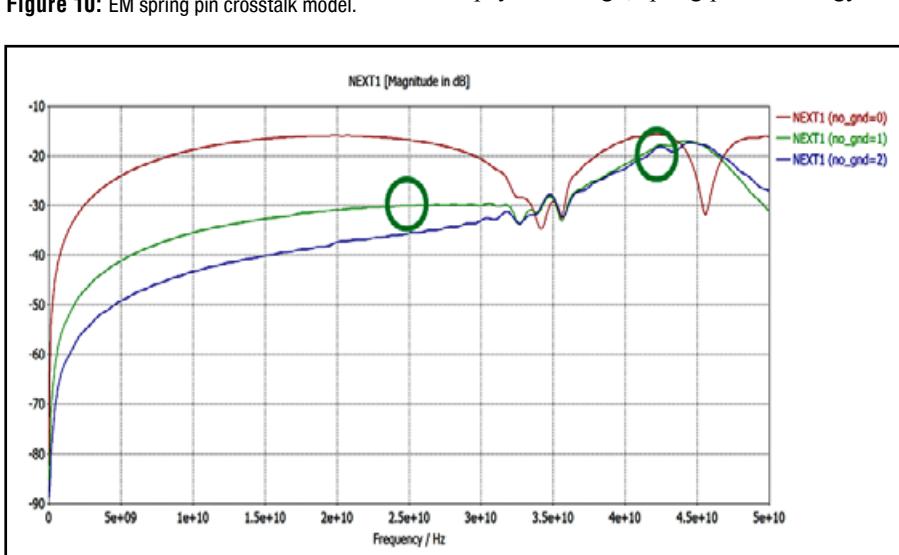


Figure 11: Model analysis at two frequencies.

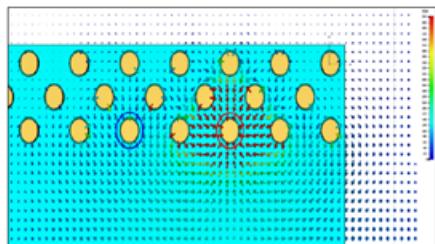


Figure 12: The electrical field at 25GHz.

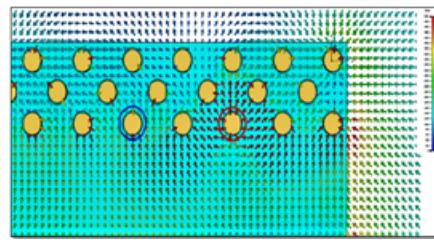


Figure 13: The electrical field at 43GHz.

Biographies

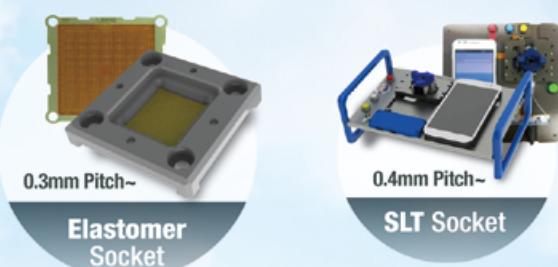
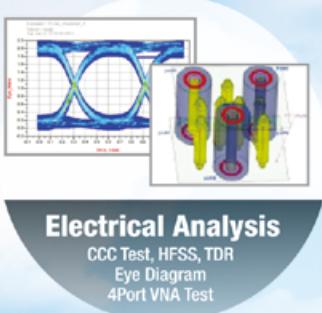
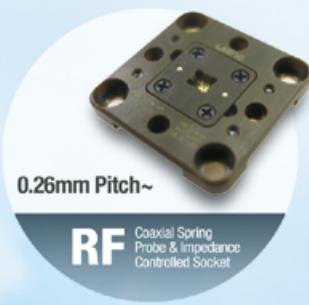
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Advanced black resist processing and optimized litho patterning for photonic devices

By Bozena Matuskova, Martin Weinhart, Roman Holly, Tobias Zenger, Thomas Uhrmann [EV Group] and Yoshinori Taguchi, Hiroshi Taguchi [FUJIFILM Electronic Materials Co., Ltd.]

Increasing demands on photonic device complexity and related optical performance mean that advancements in lithography materials and patterning are essential. Highly functional optical materials are, therefore, gaining attention in photonic applications, particularly shielding materials and infrared-related materials. These innovative materials show promising parameters, taking advantage of micro-dispersion technologies of ultra-fine pigments, dye contents, quantum dots and their integration in the photopolymer chemistry. For example, employing black resist materials as a shielding or blocking layer on wafer-level lenses in CMOS image sensors (CIS) to control the light transmission shows a lower light reflection rate compared with the use of metal layers.

Enhanced shielding effects for various and novel applications can be obtained when the material reflection rate is 2% or less, and the transmittance is 1% or less, for a visible light with wavelength of 400nm to 700nm. Furthermore, the use of black resist material for lens shielding prevents the generation of defects, such as ghosting or flares, caused by light reflection, transmission, and finally, diffraction contamination on the marginal part of the lens [1]. These defects cause harmful unwanted effects on the final image quality.

Black matrix coatings around light-emitting elements in flat-panel displays can also be used to enhance the display contrast and eliminate defects occurrences [2]. Unlike chromium- (Cr) based materials, patternable organic black resist is easier to deposit with significantly lower cost, as no vacuum conditions are required, and is not considered as hazardous for the environment. Moreover, final properties of the black material composition are crucial for the flat-panel industry and can be characterized by numerous requirements, such as simplicity of material deposition,

patterning, resolution, high surface resistivity, as well as thermal, light (transmittance) and chemical stability for further red/green/blue (RGB) color filter processing [3].

In this paper, the parameters required and designed for a new black resist material for photonic devices, along with associated resist processing and optimized lithographic patterning, are discussed.

Methodology

Resist processing methods, including spin and spray coating, are performed depending on the requirements for surface roughness, which has direct impact on final material reflectance and optical performance. Lithographic exposure of this highly functional absorbing material comes with certain challenges. The ultraviolet (UV) light penetration of the coated substrate with functional black resist layer in the near-UV spectrum range is limited. The absorption level of the material is already significant in the upper part of the layer closest to the resist surface, preventing light transmission to the underlying resist during the exposure. This affects the final resist polymerization. As a consequence, the resist development process risks introducing peeling and delamination defects, or not fully resolving structures. Moreover, an enhanced process adjustment and further precise control of the development process is necessary in order to secure overall performance capabilities.

To enable advanced resist processing methods for the deposition of black resist onto the glass wafers, the EVG 100 series was employed as it can combine spin and spray coating processes, in addition to bake, chill and developing processes. For lithographic patterning, the EVG 6200NT mask aligner and a maskless exposure (MLETM) method from EVG was used.

Results

The black material from FUJIFILM is a negative tone photoresist. Optical density and transmittance values were obtained and measured using a UV-3600 Shimadzu spectrophotometer. The spectrophotometer is equipped with three detectors – the photomultiplier tube (PMT), InGaAs and cooled PbS detector – in order to cover the full spectrum from UV to near-infrared (IR) wavelength range.

The substrate surface properties impact the final film formation; therefore, the substrates typically require specific cleanliness and/or substrate energy. In this case, the substrate surface character was prepared by applying a thin interlayer (adhesion promoter) using standard TI-prime from MicroChemicals. An evaluation test using HMDS primer was also conducted, but in comparison with TI-prime, overall deposition results showed a higher tendency of delamination defects. Spin- and spray-coated glass wafers on commonly available Eagle XG from Corning with deposited layer thicknesses from 1.0µm up to 6µm were evaluated and are listed in **Table 1**. Both processing methods were also performed on Borofloat 33 glass wafers and Gorilla Glass wafers. For the purpose of this paper, an Eagle XG glass wafer from Corning was used as a reference.

Wafer #	BR layer thickness [µm]	Processing method
W01	1.0	Spin coating
W02	1.5	Spin coating
W03	1.8	Spin coating
W04	2.0	Spin coating
W05	6.0	Spray coating

Table 1: Black resist-coated wafers with different layer thicknesses and processing methods.

Optical density (OD) is one of the more important parameters to consider for shielding applications, as it describes the

propagation of the light through a coated black material on the surface. The OD value calculates wave propagation losses occurring due to reflection, absorption or scattering. This value can be useful to find the most suitable layer thickness for dedicated optical applications and further patterning resolution requirements. OD values were measured in the wavelength spectrum ranging from 350nm up to 1100nm for both spin- and spray-coated wafers and are graphically visualized in **Figure 1**. The given plot shows optical density values versus wavelength dependency and layer thickness dependency. As seen on the plot, deposited layer thicknesses, as well as processing method, impact the final optical density of the layer. This high optical density material with OD peak close to 6 over the visible spectrum provides excellent shielding performance, fulfilling all photonic application requirements.

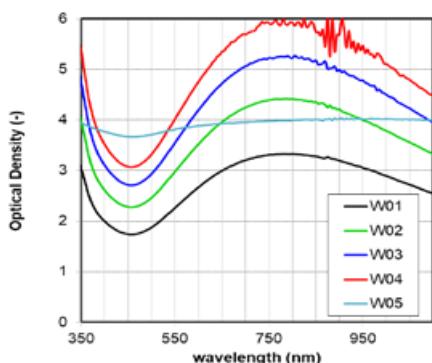


Figure 1: Optical density and wavelength dependency for spin- and spray-coated glass wafers.

In accordance with photonic applications, the transmittance parameter gives the inverse information about the light absorbance as it is a logarithmic function of the transmittance. Transmittance values (percentages) for all black-coated wafers were measured in the same spectrum range as OD, ranging from 350nm up to 1100nm.

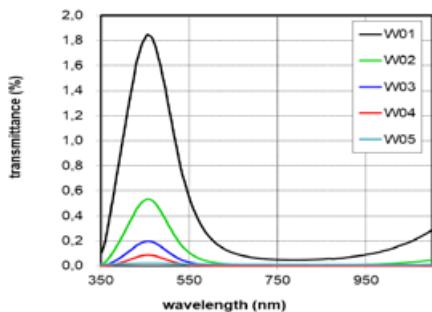


Figure 2: Transmittance and wavelength dependency for spin- and spray-coated glass wafers.

The plot in **Figure 2** shows the relation between transmittance and wavelength range for given spin- and spray-coated wafers coated with five different layer thicknesses. Significant transmittance difference of 1.3% is demonstrated in the region of 350nm to 550nm, especially at the 450nm peak, between wafer W01 with a deposited layer thickness of 1.0µm, and wafer W02 with a layer thickness of 1.5µm. Wafer W04 with a layer thickness of 2µm already shows an excellent transmittance value of 0.1% in the peak range, meaning that 99.9% of the light passing through the deposited black layer is absorbed. The spray-coated wafer with a layer thickness up to 6µm shows the transmittance value reaching close to 0% throughout the whole spectrum range.

Spin coating method evaluation

Deposition of thin black films using spin coating on flat surfaces is, in general, less challenging, as there are fewer process parameters with which to be concerned. However, thickness deviation evaluation after film deposition can be challenging with standard optical methods, such as spectral reflectance or white light interferometry, as the transparency of black material in this spectral range is already below 2% for 1.0µm thin layers and below 0.6% for all layers with thickness greater than 1.5µm. Therefore, uniformity measurements were performed on a Dektak XTL stylus profiler from Bruker, where an average uniformity of 1.5 – 2% was achieved. Black resist material is specially designed for maximum absorbance in accordance with shielding application requirements and final optical image quality. Consequently, achieving high pattern resolution can be challenging, as the majority of UV light is absorbed in the upper part of the resist layer and therefore limits light penetration to the underlying resist material closer to the substrate surface. Conclusively, resolution is in this case a function of the layer thickness. Patterning performance of better than 20µm pattern resolution on 2µm layer thickness can be attained. Layer thicknesses of 1.5µm and 1.0µm show promising results in terms of pattern resolution; however, the impact on the optical density and transmittance values has to be considered and expected. **Figures 3 and 4** show patterning results using an EVG 6200NT mask aligner. Resolution tests were performed on each of the spin-coated wafers with layer thicknesses from 1.0µm up to 2.0µm (W01 – W04). **Figure 3** shows an example of a resolution test done on spin-coated wafer W01 with layer thickness of 1µm with well-resolved lines/spaces (L/S) results achieved up to 14µm L/S.

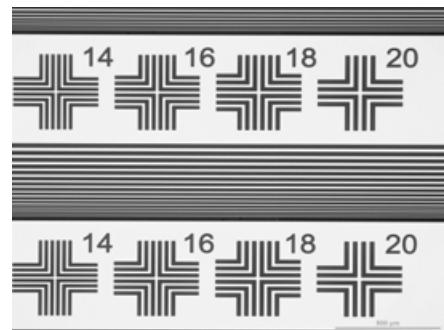


Figure 3: Resolution test, 1µm layer thickness (LT).

Figure 4 shows an example of a darkfield resolution test done on spin-coated wafer W02 with layer thickness of 1.5µm with well-resolved L/S results achieved up to 14µm L/S. Additional resolution tests have been performed. Minimum resolution at

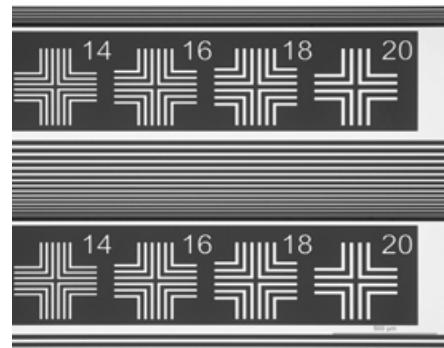


Figure 4: Darkfield resolution test, 1.5µm LT.

2µm layer thickness was achieved up to 20µm L/S. **Figure 5** shows an example of very well-resolved closed patterns with 20µm L/S resolution.

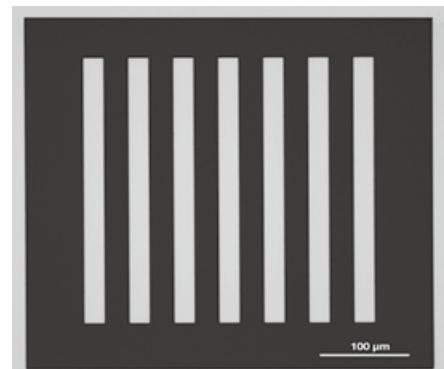
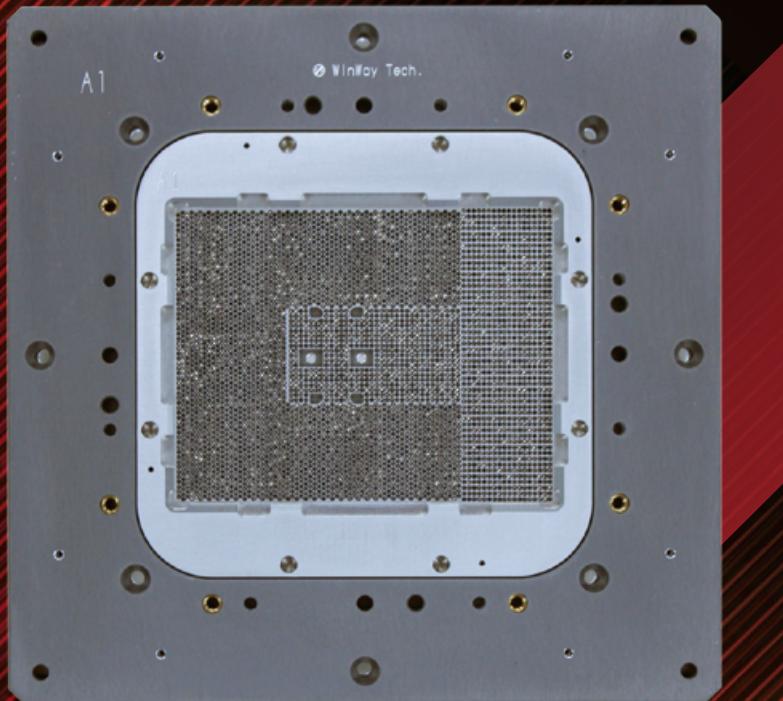
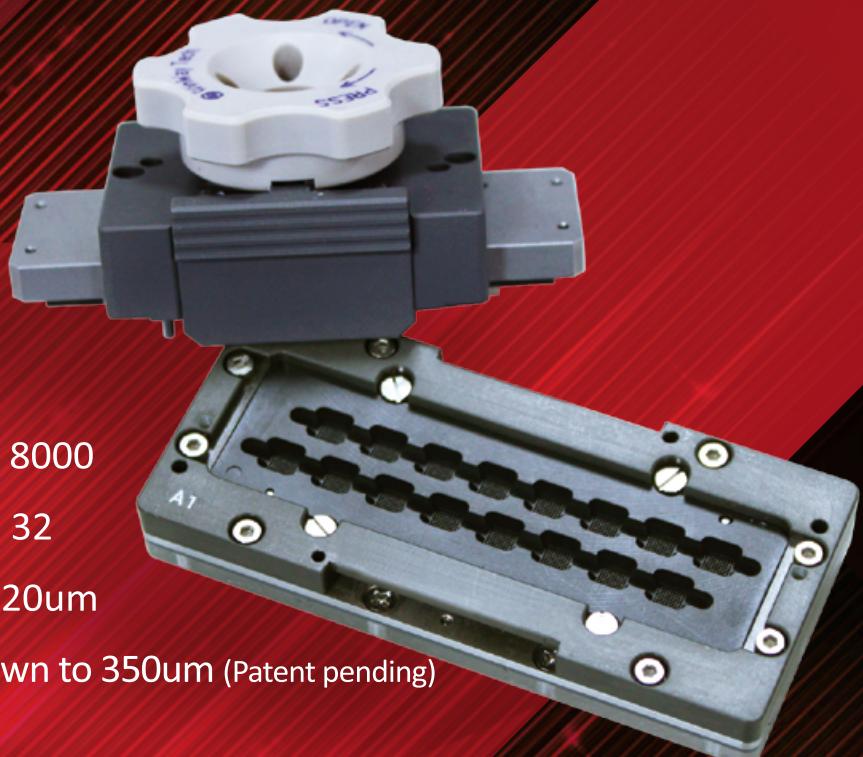


Figure 5: Resolution test example for 20µm L/S at 2µm LT.



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WLCSP Probe Card

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Spray coating method evaluation

Although spin coating is the most commonly used method for resist layer deposition, it suffers from certain limitations influencing final layer uniformity, especially for non-planar surfaces. There is also significant difference in regard to material consumption when comparing spin- and spray-coating. Spray coating for black material deposition was performed on the EVG 100 series by employing OmniSpray ultrasonic atomization technology. This method provides constant narrow-distribution droplet size. Additionally, all key parameters such as nozzle speed and height, absolute position, gas flow, dispense rate, edge overshoot and nozzle power, can be precisely controlled to realize optimized process settings for a broad range of materials and requirements. Ultimately, the aim for utilizing spray coating for black resist deposition was to obtain different surface properties for further study of the deposited black resist layer's optical behavior.

Moreover, deposition of the black resist layer was optimized by using the above-mentioned proprietary spray-coating method. Thanks to this enhanced resist deposition, low reflective properties of the black resist shielding layer can be achieved with respect to surface roughness and therefore, the need for an anti-reflective coating layer can be eliminated. By modifying the parameters of the spray-coating process, the surface topography of the black resist layer can be adapted in order to achieve the desired reflectance of the surface [4]. Two wafers were evaluated using the Dektak XTL stylus profiler: wafer A with a process setup for realizing high surface roughness; and wafer B with surface roughness that was smoothed by adjusting the spray-coating process parameters. The roughness measurements show that surface roughness control – and with this reflectance of the resist surface – is possible by altering the spray-coating parameters. **Figure 6** shows roughness values measured on a 5x5mm area for wafer A reaching values up to 1 μm with an average value of 0.7 μm .

The surface roughness of wafer B presented in **Figure 7** was measured using the same evaluation method. Roughness measurement on a randomly selected 5x5mm area reaches up to 0.02 μm , with an average value of 0.01 μm . Modifying spray-coating parameters with the aim of adjusting roughness has no influence on optical density or transmittance. In both cases, both values were in the same range.

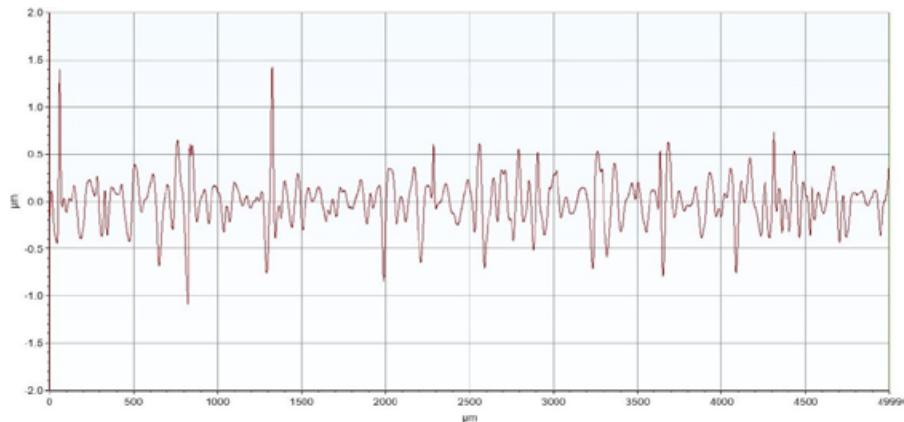


Figure 6: Wafer A roughness plot.

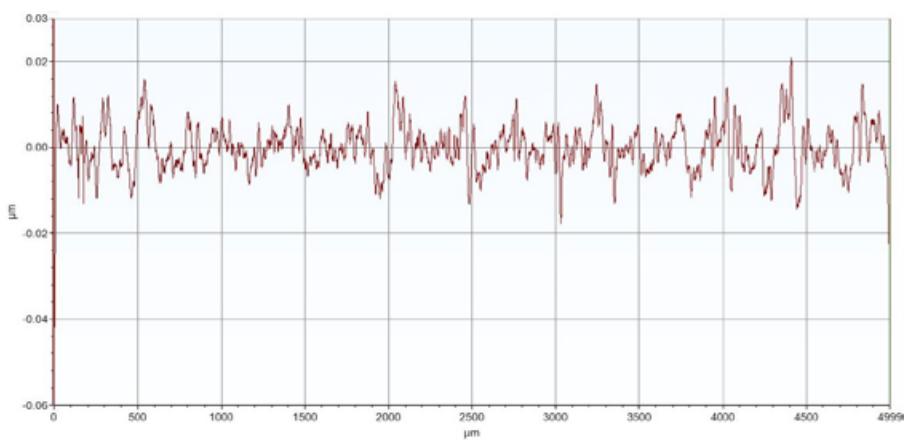


Figure 7: Wafer B roughness plot.

In addition to the above activities, a comparison of reflectance parameters was considered for evaluating the spray-coated surface for both wafer A and wafer B as it describes effectiveness of the radiation reflection. Reflectance is wavelength dependent and is affected by scattering effects occurring on the surface.

Figure 8 shows a significant difference of the surface reflectance for two spray-coated wafers A and B with different roughness topography properties. The comparison results presented on the plot in **Figure 8** reach an average value of 5.95% in reflectance difference in the visible spectrum. Wafer A with higher roughness of the surface reaches

reflectance values below 2%. Based on the surface roughness topography, the reflectance value can be tailored to the application requirements. Moreover, spray coating in particular is a very powerful method to enable uniform coatings on high-topography structures. **Figure 9** shows the uniform coating on the slope of the cavity with a layer thickness of about 5.6 μm .

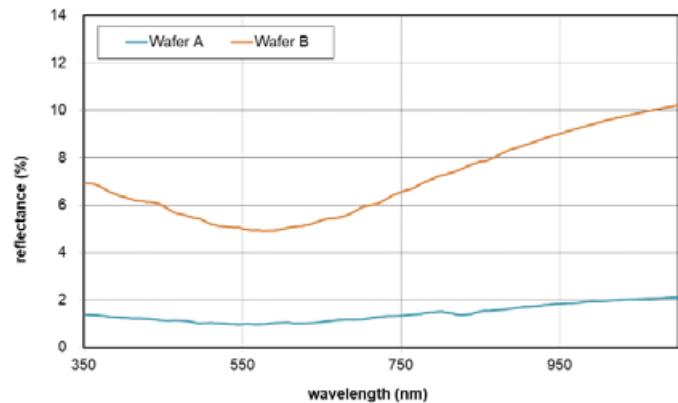


Figure 8: Reflectance comparison for wafer A and wafer B rough surface.



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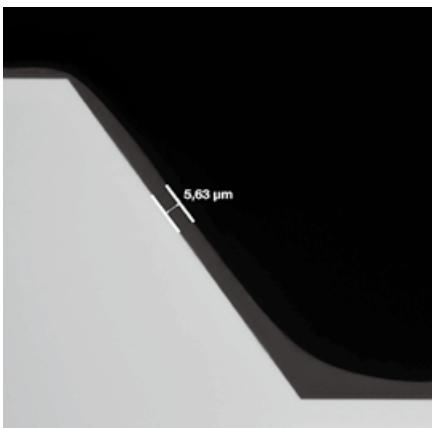


Figure 9: A spray-coated cavity with black resist.

Maskless exposure method evaluation

In addition to standard lithographic patterning for black resist evaluation, a novel maskless exposure technology was also used. This maskless dynamic patterning technology shows significant advantage in terms of patterning flexibility. It is equipped with a multi-wavelength light source; exposure can thereby be precisely adjusted according to the resist absorption spectrum. Maskless flexibility allows quick design adaptations in any arbitrary shape to the application requirements, and therefore shortens development time of new devices. The same patterning performance is also achieved regardless of pattern shape or pattern density on the wafer layout. Numerous designs applicable for various photonic devices have been tested and evaluated. Examples of the patterned results are presented in **Figure 10**.

Development method

On account of the aforementioned characteristics of the black resist material, the resist turns out to be sensitive after exposure, and consequently, the development step is challenging in order to obtain sharp, well-resolved patterns. Conclusively, the development process requires precise parameter setup and becomes as crucial

as the coating and exposure process setup, with the aim to control sidewall sharpness and undercut, while also avoiding delamination of the material from the glass surface. A combination of puddle, rinse and spray development was used by employing the EVG 100 series in order to achieve optimal resolution results accompanied by sharp pattern edges and avoiding delamination or resist off-peeling effects. The key factor is to control the combination, overlap and timing of the development methods resulting in the need for precise process control and overall process stability.

Summary

This joint collaboration enabled optimized black resist processing and high-resolution lithographic patterning for advanced photonic devices. Results are presented for current and future photonic applications. Finally, the black material fulfills shielding properties with optical density values up to $6/2\mu\text{m}$ layer thickness and with the transmittance of 2% and less for a visible light with wavelength of 400 nm to 700 nm. Patterning of this highly light absorbing material is ideally suited for photonic shielding applications while enhancing color filter contrast, minimizing defects, and eliminating the need for Cr-based materials. Ultimately, processing of the black material can be performed at the wafer level, thereby enhancing production cost factors for a wide range of photonic industry applications.

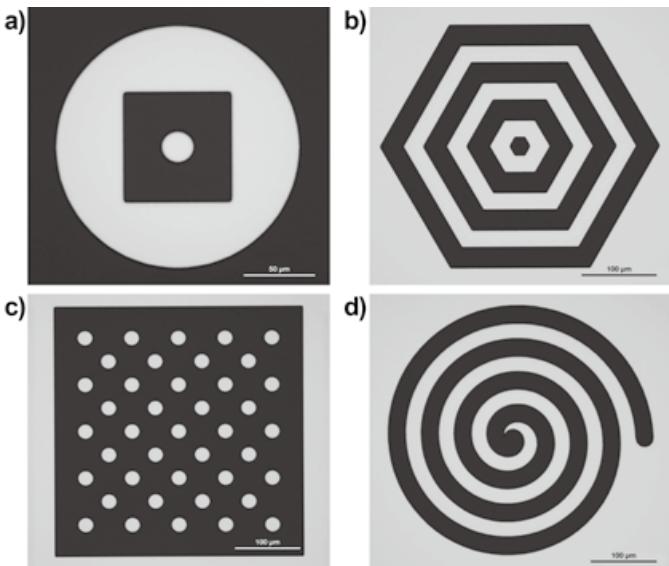


Figure 10: Black resist lithographic patterning and shielding application examples.

Acknowledgements

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References

1. Y. Maruyama, Patent Application EP2466341A1.
2. J. J. Licari, D. W. Swanson, *Adhesives Technology for Electronic Applications* (2011), p. 261–265 (Chap.: “Applications”).
3. J. Sarkar, *Sputtering Materials for VLSI and Thin Film Devices* (2014), pp. 49–50 (Chap: 1.4 “Sputtering materials for liquid crystal displays”).



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Pressure sintering for high-power packaging

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[ASM Technology Singapore Pte Ltd.]

Automotive electrification refers to the use of electricity to power the engine, either as a plug-in hybrid electric vehicle (PHEV), or to complete battery electric vehicles (BEV). A PHEV combines with gasoline fuel to power its internal combustion engine together with the electric motor, while a full BEV gets its power from electrical motors within it. The energy to create propulsion to run these motors comes from the batteries that are contained within the automobile. The electrification of vehicles actually results in many more added features that ranges from infotainment, to advanced driver-assist systems (ADAS). In order to get these to work, electrical control units (ECUs) are designed and built into the PHEV and BEV. The upsurge in the use of ECUs echoes the wider movement of growing amounts of semiconductor electronics in each PHEV and HEV produced going forward. According to IHS Markit, the average semiconductor content increase using 2018 as a baseline is set to increase from \$1,296 to \$1,832 in 2030 [1]. The market value with a compound annual growth rate (CAGR) of 5% is expected to grow from USD\$122KK to \$211KK [1].

ECU is basically a way to control electrical systems that are found in today's PHEV and BEV. The main ECU functions are employed to control modules in the vehicle such as the car engine, brakes, transmission, parking assistance, traction, and even automatic climate control for the comfort of the passengers in the automobile cabin for different types of weather. In this article, we will discuss those ECU packages that are designed and fabricated for supplying high voltage and high current that are also able to operate under high operating temperature conditions such as those under the hood (i.e., car engine), which are typically >150°C. Generally, this class of power package will require pressure sintering

where the die attached pastes are typically silver-type pastes and the copper hybrid is also possible. We will discuss in some depth the assembly flow, starting from the application of the die attach material to the package with the main focus on pressure sintering.

Sintering packaging assembly flow

The starting point for pressure sintering assembly is the application of the sintering material. The sintering material comes in many formats (discussed in the next section). The most common material is paste, based on our discussions with end users, followed by film. **Figure 1** shows two typical sintering assembly flows from paste print to pressure sintering. The top image in **Figure 1** shows the dry flow process, while the bottom view shows the wet flow process.

The difference between the dry and wet flow processes is that the die attach onto the substrate for the dry flow process is performed after the paste drying is completed under a nitrogen gas environment (N_2). In contrast, in the wet flow process the die placement onto the substrate is performed before the drying process is completed (also under a nitrogen gas [N_2] environment). The dry flow process is the most commonly adopted one based on our extensive work

experience with a variety of customers. The reason is that the flow mark is usually found with the wet process before and

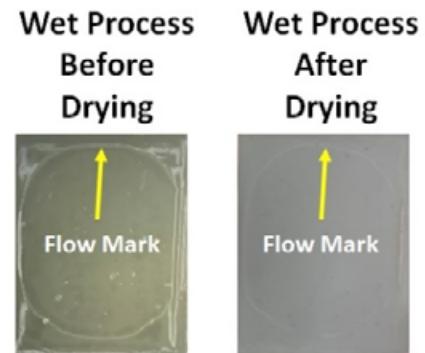


Figure 2: Flow mark in the wet flow process.

after drying (see **Figure 2**).

Paste-printing-on-substrate is a critical assembly process step during power module assembly that needs to be performed correctly in order to achieve reliable and efficient power devices by pressure sintering. If this step is not performed optimally, it can lead to micro voiding in the printed paste, that in turn leads to a break in the thermal conductance path in an assembled power module during operation. There are many factors influencing a good printed sintering paste: 1) paste viscosity at

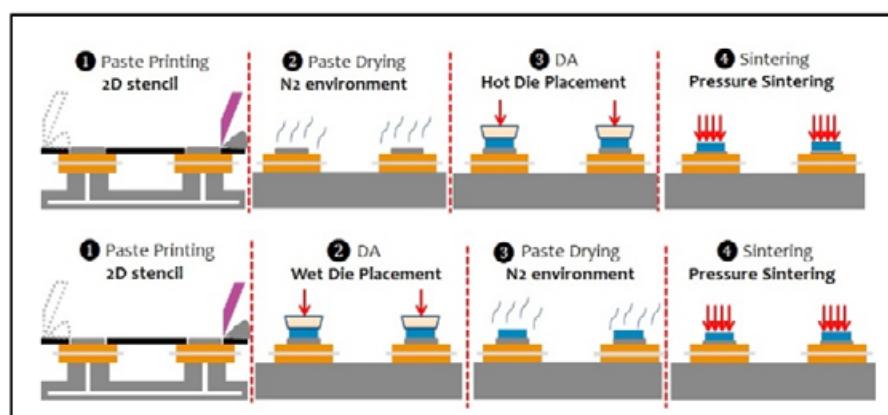


Figure 1: Dry and wet flow process.

room temperature, 2) paste mixing and rollability, 3) printing speed, 4) printing force, 5) printing direction, 6) stencil frame spring force, and 7) squeeze release speed and distance. Some typical defects found as a result of suboptimal printing are shown in **Figure 3** and can include “dog ear” (roll-up paste), incomplete paste printing, and micro voids. Roll-up paste is generally caused by the printing speed and release speed not being optimized. As a result, this “dog ear” can cause issues such as die tilt due to an unbalanced height at the end of the roll-up paste, and even die cracking during pressure sintering. Voiding and incomplete fill are a result of suboptimal mixing preparation of the paste before printing, and a suboptimal printing parameter, respectively.

After printing, the next assembly set for the dry flow process is oven drying under a N₂ gaseous environment to ensure no oxidation. The reasons to use the oven process are: 1) to remove the thinner that is contained within the sintering paste, and 2) to improve the rigidity of the paste so that it will become firm, and therefore, during die placement, the paste will not sputter or roll up. We found that after oven cure, the printed paste evenness is improved.

The next process step after oven cure, as shown in **Figure 1**, is die placement. The challenges that we have observed during die placement are alignment of the die to the printed paste, optimizing the pickup of the sintering film and temperature control during this process. If the AgS (silver sintering) paste is not optimally printed, we can encounter “squeeze out” where it can overflow to the top of the semiconductor die. Another instance can be insufficient AgS paste, i.e., the real estate of paste is smaller than the die size and can result in die cracking during pressure sintering. As for the AgS film, we have observed instances of incompletely attached silver film, broken attached silver film, and excess attached silver film (film size > die size). All these will lead to downstream issues during or after sintering, such as delamination, cracking, and film bridging to the next semiconductor die if the package is a matrix die layout. The optimal design of the pick tool (collet) for die and process parameter for die placement is equally important because a suboptimal design will result in die cracking as shown in **Figure 4**.

The last assembly step from **Figure 1** is pressure sintering. A good pressure

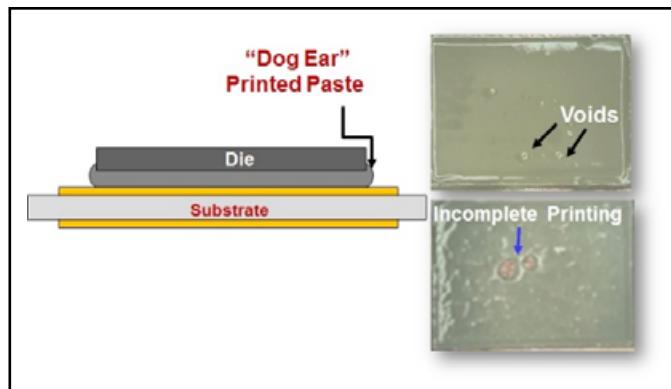


Figure 3: Some typical printing defects.

sintering system (PSS) should be able to accept multiple formats from singulated AMB/DBC, large DBC of 5" x 7", leaded substrates, such as TO247/DPak, and even wafers of 8" diameter. Sealing and leakage-free capabilities of a PSS is critical because the pressure buildup during the sintering process must not be reduced as pressure is a critical process parameter in addition to temperature to ensure an optimized atomic diffusion process. In addition, PSS should not enable entrained air into the system during the pressure sintering process to avoid DBC/AMB oxidation. As such, having a good design to create an inert environment during sintering, loading and unloading of the substrate is equally important. An inert environment can be of two forms: either vacuum, or N₂ (nitrogen gas) fill. PSS temperature heating and cooling control must be designed to be under the correct climate condition when the sintering pressure is building up and ramping down. Temperature and pressure

must be at a sweet spot to ensure that pressure sintering is optimally performed. The duration to sustain this sweet spot is recommended by the sintering material vendor, and such data can be found in the material vendor technical data specification.

Pressure sintering material

Sintering as a technology has been around for a long time – since the days of powder refractory materials such as tungsten, rhenium, and even molybdenum, which has largely come under the umbrella of powder metallurgy. Sintering starts with loose powder—with optimal settings of pressure, temperature and time. The sintering material undergoes atomic diffusion, where surface energy is reduced and forces all the small particles from the powder to merge into larger masses into a densified bulk material with microscopic gaps. These gaps range from micrometer-to nanometer-sized spaces. Currently, the most common metal element is silver (Ag) for pressure sintering die-attach material. Pressure sintering materials come in many formats: paste, film and preform. As previously mentioned, Ag metal is currently used in the market for producing pressure-sintered ECUs. Hereafter, we will use the term “AgS” to mean silver sinter die-attached material. The reason silver is used for die attaching is because compared to solder paste, for example 80Au/20Sn (gold-tin), the melting point of bulk silver is 962°C versus Au/Sn solder paste, which has a melting point of 280°C. The fact that AgS has a high melting point is highly desirable because the operating temperature of some ECUs can be beyond the melting temperature of Au/Sn solder paste.

Comparing the thermal conductivity of a typical AgS which is 419W/m K versus that of Au-Sn, which is 57W/m K — this is a 7 times better heat conduction rate. Heat generated within a pressure-sintered power module can therefore be quickly dissipated, thereby reducing the thermal stress of the ECU. Other notable properties include the electrical conductivity of AgS (62.5S/m) is 10 times better compared to that of Au-Sn



Figure 4: Die crack at die placement.

(6.3S/m). Sintering is normally performed at a lower temperature because the AgS particles are small in size, therefore, they can be sintered at a lower temperature [2]. According to research, decreasing the size of a metal particle to micro-scale and/or nano-scale enables sintering at a lower temperature with optimal pressure. It compares favorably to processing a bulk AgS material at a melting temperature of 962°C [2]. The use of such minuscule particles increases the surface area of contact between the particles contained within the sintering material and it is found to improve thermal and electrical properties [3] of power packages that have insulated-gate bipolar transistor (IGBT) semiconductor devices. There are two ingredients that ease the workability and transportation of the sintering paste during application of the sintering material onto the substrate: they are solvent and binder. Solvent is added to tweak the viscosity of the AgS material, such that it is easy to print. The binders are added to bind the micro/nano particles in the sinter paste and prevent cracking during transportation of the printed paste onto the substrate [4].

Pressure sintering process

Pressure sintering occurs when a sweet spot is achieved among pressure, temperature, and time. These three sintering process parameters can be called the “iron triangle” [4] for good quality pressure sintering to occur (**Figure 5**). These three parameters will affect the final reliability and quality of the pressure-sintered joints. In this tripartite relationship, changing any one of these parameters will be compensated by the adjustment of the other two [5-10]. A number of research studies have been performed with respect to pressure sintering to reduce both the

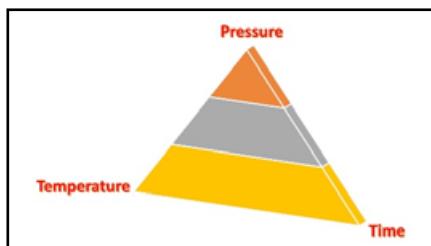


Figure 5: Tripartite relationship of pressure-temperature-time for pressure sintering.

pressure and time while maintaining a moderate temperature for high-volume manufacturing (HVM). The solution is to reduce the particle sizes of the AgS material. When the particle size is reduced, it will inherently increase the surface contact area and curvature, thereby allowing lower pressure and temperature to create successful atomic diffusion with reliable sintered bonding of the interfaces of die to paste to substrate. The constitutive model for sintering can be found in the work of the Mackenzie-Shuttleworth model [9]. **Figure 6** is a schematic showing the various interfaces of a typical power package for pressure sintering. Pressure is applied with the die face up and while heat is applied at the bottom. The two surface contacts with sinter paste are critical.

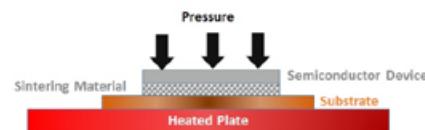
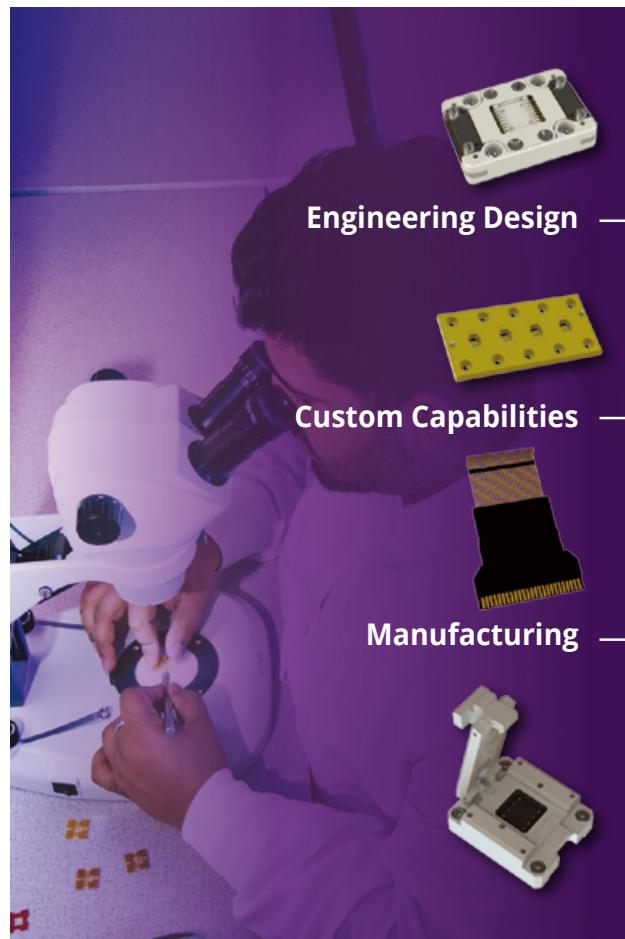


Figure 6: Schematic of a power device.



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The first surface is the substrate and the second surface is the bottom of the semiconductor device. Selection of metallization layer thickness and composition for these surfaces is critical for reliable Ag sinter bonding after the die-attach sintering process. Generally, the industry uses substrates that are obtained by using direct bond copper (DBC) and active metal brazing (AMB). These substrates are usually plated with either gold or silver, to ensure that no corrosion and oxide formation takes place and promotes good adhesion/bonding to AgS metal during pressure sintering. The second interface die to AgS, i.e., the die metallization, are there to: 1) promote adhesion, 2) protection against oxidation, and 3) act as a barrier to block impurity diffusion into the active semiconductor die.

Results of pressure sintered bonding

In this section we share some of the results obtained with the pressure-sintered bond. **Figure 7** shows a cross-sectional view of a pressure-sintered bond interface.

The results indicate that end users should pay attention to: 1) the porosity level, 2) the interface quality between the die and the AgS material, 3) the interface between the substrate and the AgS paste or film and, 4) the bond line thickness (BLT). From our work, we found that the BLT dimension changes at every stage of the sintering assembly process. **Table 1** shows the BLT transition from printed to pressure sintering. It is observed that after printing, the BLT stays flat as long as the printing parameters are optimized. After curing, because of the different types of paste chemistry, the BLT thickness is reduced within a 5 μm range, and there is a further reduction within another 5 μm range after die placement. The significant change of the BLT comes during pressure sintering—it varies between 20–25 μm . This means that the BLT is reduced by an order of 3 to 4 times after printing.

In **Figure 7**, the porosity is identified as the dark spot. The desired porosity level is such that it will result in as few dark spots as possible. Generally, the end user finds it challenging to determine what

should be the acceptable level. However, it is known that the porosity level of a sintered bond will affect electrical resistivity (ER), electrical conductivity (EC), thermal conductivity (TC), the coefficient of thermal expansion (CTE), the elastic modulus (EM), Poisson's ratio (v), and yield stress (YS) [11]. The increase

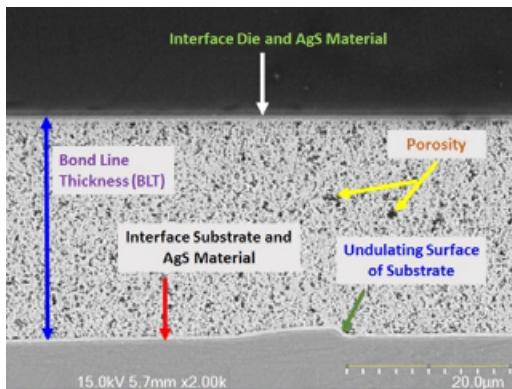


Figure 7: Cross-section view of a sintered bond.

Substrate Plating	Paste Material Model	Printed Paste Thickness (PPT) μm	PPT After curing (μm)	PPT After Die Attached (μm)	BLT After sintering (μm)	Sintering Condition 250°C/ 180s
Cu	A1	80 μm	55–60 μm	45–50 μm	20 μm	15MPa
Ag	A2	80 μm	55–60 μm	45–50 μm	20 μm	15MPa
Cu	A3	80 μm	55–60 μm	45–50 μm	25 μm	15MPa
Ag	A4	80 μm	55–60 μm	45–50 μm	25 μm	15MPa

Table 1: Results of bond line thickness study.

in porosity level will increase the electrical resistivity, but reduce EC, TC, EM, v, and YS, but the CTE will remain unchanged.

The tripartite relationship of pressure-temperature-time for pressure sintering is shown in **Figure 5**, and **Figure 8** further illustrates this relationship for the pressure sintering coverage of a 2x2 matrix die configuration. Starting from the EXP I in **Figure 8**, the 2x2 die shade is the lightest compared to the center EXP II and the darkest image of EXP III in **Figure 8**.

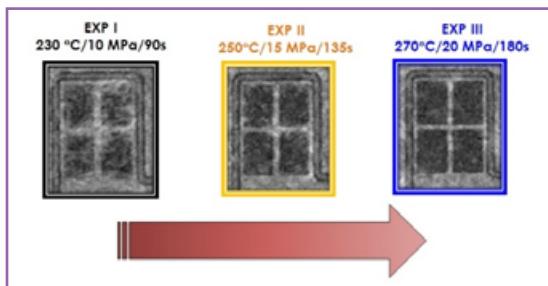


Figure 8: Pressure sintering outcome of pressure-temperature-time variations.

The darkness of the image from EXP III (using ultrasonic scanning microscopy, or C-SAM) signifies that the sintering pressure is uniformly applied during the process, and it is an indication of good pressure coverage as applied onto the die and should result in a high-quality sintered bond. A closer look at the applied

sintering parameters indicate that with a longer sintering period, higher sintering pressure and temperature lead to better sintered quality bond coverage. We found this qualitative method to be cost effective because it avoids quantitative testing, which is generally destructive and takes a longer period to get the end result. This qualitative characterization is justified by the reliability result achieved by the end user with whom we worked.

The only destructive process that we normally use with our end user is die shearing, but the quantity used is limited on account of the cost. **Table 2** shows the results of die shear testing and the impact of shear force due to changes in sintering parameters (the same AgS material is used to conduct the study). Comparing Samples A and B with changes of pressure, ceteris paribus, with temperature and time held steady, and with a higher sintering pressure of 33%, the die shear force increases by 6%. While holding steady the sintering pressure and time, the increase of 8% in temperature will result in a 10% increase in the die shear force. If we only hold time constant and increase the temperature by 8% (Samples A and D) along with a 33% increase in pressure, the die shear force surged by 23.5%. The outcome of die shear testing indicates that the tripartite relationship of pressure-temperature-time is inherently compounded and nonlinear.

Figure 9 shows the warpage level of a singulated AMB substrate as it is processed through the complete pressure sintering assembly. The warpage level is measured at an appropriate process step, which must have the AgS material covered by the semiconductor. The result shows the AMB warpage increases approximately 120% from the as-received condition. The management of the sintered package's warpage is critical to ensure that an ECU module can be assembled seamlessly, because a warped sintered package

Sample	Temperature (°C)	Pressure (MPa)	Time (s)	Average BLT (μm)	Average Die Shear Force (N)
A	250	15MPa	180s	15	1700
B	250	20MPa	180s	14	1800
C	270	15MPa	180s	15	1870
D	270	20MPa	180s	12	2010

Table 2: Results of die shear force testing.

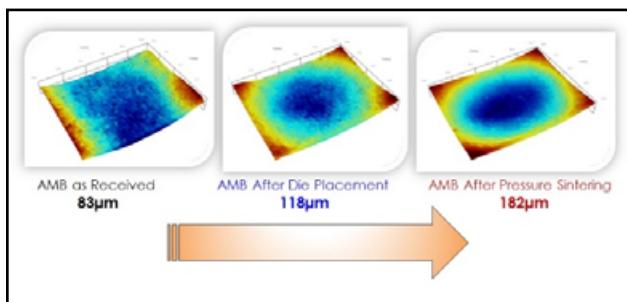


Figure 9: Warpage history of AMB during sintering assembly.

that looks like a “potato chip” can easily crack and be a challenge to transport and assemble. One factor to consider for managing warpage is to design the CTEs of the various input materials of the sintered package so that they do not become extremely mismatched. The second factor is Young’s modulus and the glass transition temperature of materials.

Summary

The rise in ECU usage in the modern internal combustion engine (ICE) and the growth of the EV automotive sector shows a broader trend of increasing amounts of electronics in each of these classes of automobiles. In order for ECUs to be able to operate reliably, pressure sintering is used to create robust and reliable bonding between the semiconductor die and the substrate joined by the AgS material. Various steps of the sintering package assembly flow were described starting from printing, to final pressure sintering. The challenges of each of these assembly operations have been discussed in this article and

key factors that can affect the quality of each process outcome were highlighted. The tripartite relationships among pressure-temperature-time for pressure sintering are key factors to yield a robust and reliable sintering bond. Results from the study of pressure-sintered bonding shared in this work indicate that it is a three-way relationship and that it is nonlinear in nature.

Acknowledgements

We wish to acknowledge and thank our colleagues within the ASMPT organization, our collaborator and material vendors who have worked with us on the various pressure sintering aspects of the study. The goal in sharing the knowledge in this publication is to benefit the wider community of engineers interested in pressure sintering. No names are mentioned to protect the identity of the various parties.

References

1. <https://www.greencarcongress.com/2019/05/20190515-ecu.html>
2. A. Moisala, A.G. Nasibulin, E.I. Kauppinen, “The role of metal nanoparticles in the catalytic production of single-walled carbon nanotubes—a review,” Jour. of Physics: Condensed Matter, 15 S3011–S3035; 2003.
3. G. Chen, D. Han, et al., 2012 “Transient thermal performance of IGBT power modules attached by low-temperature sintered nanosilver,” IEEE Trans. on Device & Material Rel., Vol. 12, No. 1, pp. 124–131.
4. K. S. Siow, Y. T. Lin, “Identifying the development state of sintered silver (Ag) as a bonding material in the microelectronic packaging via a patent landscape study,” Trans. of the ASME, Vol. 138, June 2016, 020804-1 to 020804-13.
5. J. K. Mackenzie, R. Shuttleworth, “A phenomenological theory of sintering,” Proc. Phys. Soc. Sect. B, 62(12), 1949, pp. 833–852.
6. S. Hausner, S. Weiss, B. Wielage, G. Wagner, “Joining of copper at low temperatures using Ag nanoparticles: influence of process parameters on mechanical strength,” Inter. Brazing & Soldering Conf. (IBSC 2015), Long Beach, CA, Apr. 19–22.
7. S. Fu, Y. Mei, X. Li, P. Ning, G. Q. Lu, “Parametric study on pressure-less sintering of nanosilver paste to bond large-area (100mm^2) power chips at low temperatures for electronic packaging,” J. Elect. Material, 44(10), 2015, pp. 3973–3984.
8. M. Knoerr, A. Schletz, “Power semiconductor joining through sintering of silver nanoparticles: evaluation of influence of parameters time, temperature and pressure on density, strength and reliability,” 6th Inter. Conf. on Integrated Power Elec. Sys. (CIPS), Nuremburg, Germany, Mar. 16–18, 2010.
9. W. Schmitt, “New silver contact pastes from high-pressure sintering to low-pressure sintering,” 3rd Elec. System-Integrated Tech. Conf. (ESTC), Berlin, Germany, Sept. 13–16, 2010.
10. J. K. Mackenzie, R. Shuttleworth, “A phenomenological theory of sintering,” Proc. Phys. Soc. Sect. B, 62(12), pp. 833–852, 1949.
11. A. W. Andrew, J. V. Daniel, et al., “Properties of bulk sintered silver as a function of porosity,” Oak Ridge National Lab., Oak Ridge, TN, ORNL/TM-2012/130, 2012.

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Enabling 3D packaging using excimer lasers

By Ralph Delmdahl, Dirk Müller [[Coherent](#)]; Habib Hichri [[SUSS MicroTec Photonic Systems Inc.](#)]

The relentless demand for smaller and lighter products with faster and more powerful processing capabilities continues to be the overarching trend across nearly every sector of the electronics market: from telecom systems to medical sensors, image processing, and of course, smart phones and similar devices. Today, advanced package integration (API) is arguably the key technological enabler supporting this trend, with a focus on vertical stacking platforms – so-called 2.5D and 3D architectures – or fan-out wafer-level packaging (FOWLP) as preferred in high-bandwidth memory (HBM).

A typical example of 2.5D combines separate computing and communications dies in the same package (system-in-package, or SiP) where the heterogeneous chips are massively interconnected using a high-density interposer or embedded multi-die interconnect bridge (EMIB). An example of a true 3D package is where two (or more) thinned chips are stacked on top of each other in the same molded package, such as several memory chips or the combination of a logic chip and a memory chip. In 2.5D/3D packages where two chips are vertically stacked, a structured layer called an interposer is required. In fan-out, the dies are packaged in molding compound while still on a wafer and do not require an interposer, making it more economical than 2.5D/3D for some applications.

Of course, there are several variants of each of these advanced package types. For example, there are three types of fan-out packages: chip-first/face-down; chip-first/face-up; and chip-last or redistribution layer (RDL) first. But, a common requirement for all these is dense high-resolution interconnections, often with extremely thin wafers in order to deliver maximum speed and functionality. As wafers get thinner and electrical lines get smaller, 3D packaging inevitably requires a combination of new processing tasks

and established processes that are being pushed to new levels of miniaturization. In this article, we take a look at several of these processes that now can be optimally performed using excimer lasers – powerful ultraviolet lasers long-established in smart display fabrication and in front-end lithography.

Patterning dual damascene

As packaging technology continues to move towards fan-out architectures, packages with multiple chips requiring intricate designs are becoming more and more prevalent. Current and projected designs feature up to 10 RDLs, line widths as small as $2\mu\text{m}$, via openings of less than $10\mu\text{m}$, and ideally, these designs could be transferred to panel-level packaging. This level of advanced packaging could be used in several applications such as wafer-level chip-scale packages (WLCSP): $200/300\text{mm}$ (RDL, integrated passive devices), fan-out WLP: $>300\text{mm}$ (eQLB, redistributed chip packaging [RCP], other), and embedded IC: $>300\text{mm}$ (flip-chip ball grid array [FCBGA], flip-chip chip-scale package [FCCSP]).

Among the technical challenges of multiple RDL layers, such as small pitch and small vias, one must also consider planarization to stay within the depth of field (DOF) for exposure tools. Additional concerns are the thermal and mechanical stability of dielectric material, efficient removal of Cu overburden and the seed layer without damaging plated metal, as well as the stability of the deposited metal.

Traditional organic flip-chip substrates are facing many challenges when it comes to advanced packaging. Photosensitive spin-on dielectrics for via formation, in combination with RDL photoresist, are unable to meet the technical challenges without causing serious concerns about pattern integrity and reliability. Free-standing RDL lines with $\leq 2/2\mu\text{m}$ L/S size demonstrate

major electromigration concerns, and it is almost impossible to remove the seed layer from narrow trenches—and when it can be removed, it causes severe undercut to the RDL lines. The non-planar surface presents an additional challenge for the next redistribution layer because it requires a larger depth of focus for the exposure system, which then limits the resolution capabilities. Another concern is the warpage of the substrate as more and more layers of RDL are added during processing. This requires careful selection of material while also paying close attention to thermal properties.

The pulsed ultraviolet excimer laser is a widely used tool in the electronics and display industries. Lower power versions are used in front-end chip microlithography and high-power versions are used to anneal silicon for high-resolution displays and to perform lift-off of flexible displays. With a 300W excimer laser for RDL patterning, the rectangular light beam is reshaped and passed through an aluminum photomask that is the inverse of the via or trench pattern. The patterned beam is then projected onto the substrate surface through a reduction lens. In an automated tool like the SUSS ELP300, the pattern is sequentially stepped across the wafer ([Figure 1](#)).

Whereas lithography involves photographic exposure of a resist,

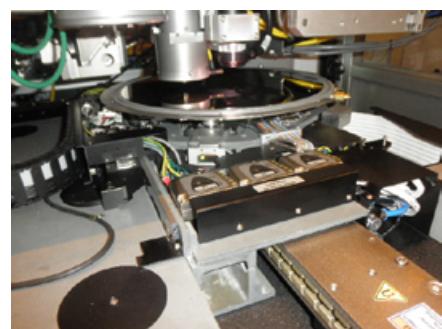


Figure 1: 300mm wafer stage of the excimer ablation stepper tool ELP300.

in this excimer laser-based process, the laser pulses directly remove material. And, because the excimer laser produces ultraviolet output (at a wavelength of 193nm, 248nm, or 308nm), the high-energy photons directly break interatomic bonds in polymers and other materials, ablating the material as vapor in a relatively cold process with virtually no peripheral thermal effects.

Excimer laser ablation is an efficient and cost-effective patterning method that opens wider choices of dielectrics in the package. The wide choices of dielectric materials means you can choose the optimum materials that meet the package thermal (i.e., coefficient of thermal expansion) and mechanical requirements. Another technical advantage for excimer laser ablation is that it allows the fabrication of dual-damascene structures for interconnection in the package. This patterning method consists of fabricating the RDL and via in the same step, while the wafer or substrate is still on the excimer laser chuck. The pattern of via and RDL is embedded into the already cured dielectric—there will be no changes to its profile prior to metallization as compared to the current

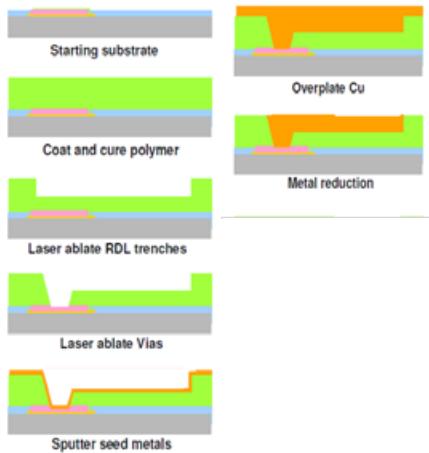


Figure 2: Process flow for an excimer dual laser-based dual-damascene process.

lithography process. The sequence of process steps involved in dual damascene is summarized in **Figure 2** [1].

The excimer laser-based process has several advantages. First, the polymer layer is cured before patterning by the laser rather than after as is the case with lithography. Therefore, the pattern has

inherently very high fidelity with no shrinkage or distortion. In addition, the same tool can create both the vias and the trenches without disturbing either the wafer or optical alignment. This ensures perfect registration and provides good alignment of via to trench. The latter capability optimizes real estate in the package by making vias inside the trench, and eliminates the large pads that compensate for overlay in

the current process-of-record tools (**Figure 3**). In addition, the dry excimer processed dual damascene provides the opportunity to sputter a Cu barrier layer (e.g., TiN/Ti, TiW/Ti or TaN/Ta) followed by a Cu seed before plating. This capability is of great importance when hitting small lines and spaces below 5/5µm. This barrier layer blocks any chance of copper migration into the polymer at high voltage of >3V.

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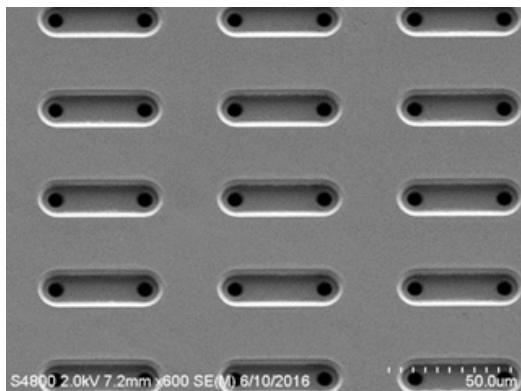


Figure 3: Trench and via ablated simultaneously in cured dielectric material (FujiFilm FCPI2200).

The excimer ablation process also provides superior control over all dimensions of the vias, including both the aspect ratio and the amount of taper. Specifically, the entrance diameter of the via is defined by the mask and projection optics, whereas the taper angle can be increased by lowering the fluence, or decreased by raising it (see **Figure 4**).

The amount of material removed by each pulse at defined fluence (energy) is different for different polymers and principally depends on the polymer backbone whether there is filler (silicon

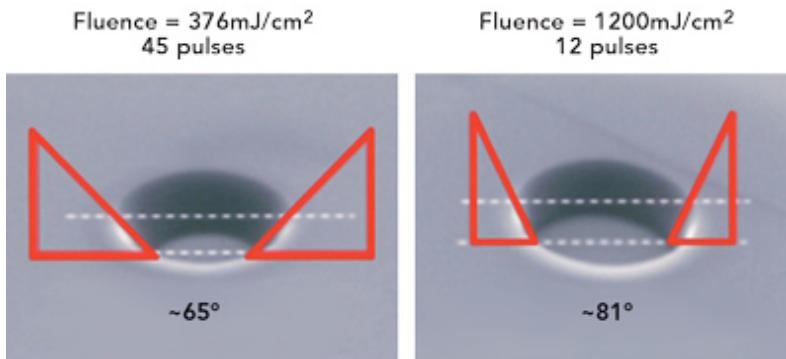


Figure 4: Varying laser fluence enables manipulation of feature side-wall angles, which can be important in subsequent deposition steps [2].

ball) embedded into the polymer or not. The depth of the features is dependent on its size on the mask—the smaller the deeper. The throughput of the excimer laser is independent of the number of vias or features on the mask. It only depends on the material ablation rate: the faster the removal rate per pulse, the faster the throughput.

Another advantage of the process is that via and RDL patterning is performed in one step, and can be

either via-first/trench-last (RDL), or trench-first/via-last. The latter option is the preferred one for advanced packaging as it allows better control of the via profile and its critical bottom dimension.

The dual damascene enabled by excimer laser on a wafer usually is followed by a cleaning step in the form of an O₂ plasma to remove any residual debris. The cleaned wafers will then be sputtered with the Cu barrier and Cu seed, followed by plating.

At the plating step, there are two integration schemes that can be proposed. The first such scheme comprises a regular electroplating process followed by chemical mechanical polishing (CMP) or a fly cutter planarization process to remove the Cu overburden and reduce the RDL metal height to the required level set by the design. The second scheme is a bottom-up fill process using electroplating, which is conceptually similar to through-silicon via (TSV) plating. This process will fill the dual damascene

Seed layer removal

Where CMP is used, it can remove overburden down to the seed layer, followed by another excimer process to remove the seed layer. In fact, excimer ablation is also well-suited to seed layer removal in general, e.g., for under bump metallization (UBM) used under the bumps or copper pillars that are vital interconnects in 3D packages. This is because excimer ablation effectively removes thin seed layers on top of dielectric vias—a process called spallation—but leaves thicker (plated) metal virtually untouched. In contrast, the wet etching traditionally used for seed layer removal can cause undercutting of bumps and pillars, resulting in unacceptable thinning of lines at the high spatial resolution (<10 μm) needed for the latest packages. For example, copper pillars in the <5 μm range can be undercut and rendered so mechanically fragile that bonding yields are simply not sustainable.

In spallation (**Figure 5**), most of the excimer beam penetrates through the ultra-thin seed layer. Because the polymer absorbs the ultraviolet very strongly, all the beam energy is then absorbed in the first few atomic layers

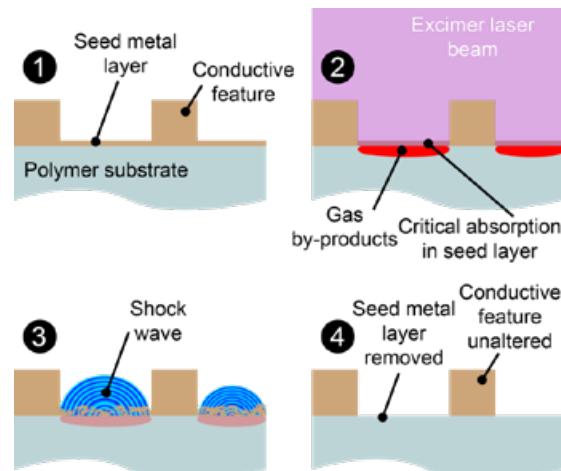


Figure 5: Schematic showing spallation, where the excimer light penetrates the ultra-thin seed metal layer and is absorbed at the polymer interface; the vaporization of the polymer surface causes explosive release of the overlaying seed metal. The conductive features are far too thick to be affected by this subtle process.

with Cu without creating any overburden in the field. This process is followed by a seed layer removal process between the embedded RDLs using either wet chemistry or excimer laser techniques. The second integration scheme offers about a 45% cost advantage as compared to current lithography processes of via and RDL [3].

of the polymer, completely vaporizing it. The expanding vapor, however, is trapped under the mechanically weak seed layer, blowing it away in a single pulse. Importantly, no masking or

optical registration is needed because the thick metal conductors, pillars, etc., absorb the pulse energy, which is then harmlessly dissipated through the metal, without reaching or affecting the underlying substrate in any way.

Because laser spallation is a single pulse process, it supports very fast throughput. Depending on the laser power, a 300mm patterned substrate can be stripped of residual seed layer in just 40-50 seconds [4]. Moreover, because most of the laser light reaches the target at near normal incidence, there are no shadowing effects, and none of the problematic undercutting found with wet etch cleaning processes.

Excimer debonding of thin wafers

3D/2.5D package formats rely on thin chips to minimize size, etc. Some of these silicon wafers are now as thin as 30-50 μm . With wafers as large as 300mm and panels up to 600x600mm, this means that the wafer can no longer self-support during backside processing and packaging. Temporary wafer bonding is now established as the method of choice for handling silicon wafers during both the thinning and the high-temperature backside processing required for the manufacture of 3D device structures. Here, the wafer is attached on its frontside to a rigid carrier that is usually tape mounted. Glass is a common choice for the rigid carrier because of its low cost, availability, and ability to withstand elevated temperatures and other physical stresses that might be encountered in downstream processes.

A variety of different adhesive materials may be spun on the glass carrier and/or the wafer's backside to enable temporary bonding, with an emphasis on "temporary." The choice of temporary wafer bonding (TWB) layer depends on the specifics of post-bonding processes and also the mechanism to be used for final debonding. (Some applications require the TWB materials to withstand temperatures up to 250°C in high-vacuum conditions, and even up to 350°C or higher during the dopant activation step required for manufacturing power devices.)

A key step is to debond the wafer from the carrier after the backside

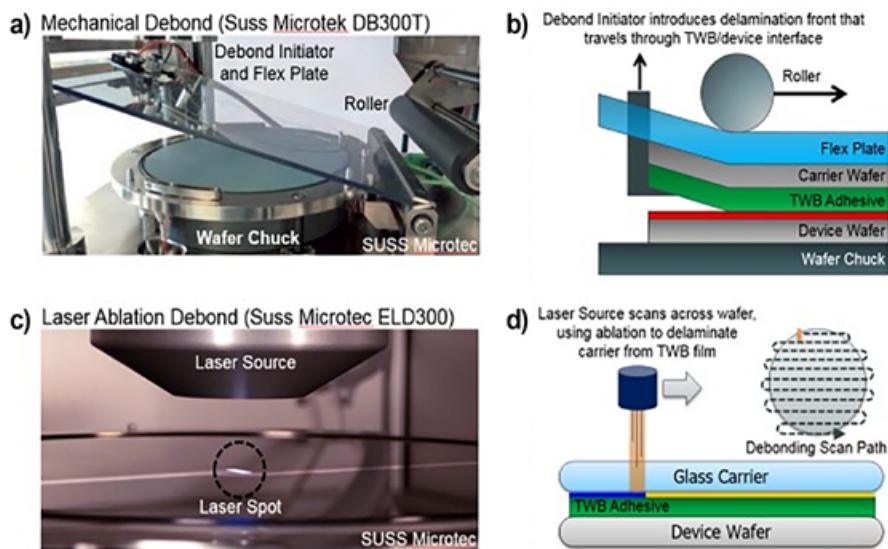


Figure 6: a) Mechanical debond step using a SUSS MicroTec DB300T; b) Debond initiator introduces delamination front that travels through TWB/device interface; c) Laser ablation debond using a SUSS Microtec ELD300; and d) The laser source scans across the wafer using ablation to delaminate the carrier from the TWB film.

processes have been completed. One method for performing this task is mechanical debonding, as illustrated in **Figure 6**. Here, the wafer is held securely on a vacuum platform and the rigid carrier is sequentially lifted. A roller sweeps across the carrier in one single action and prevents overly traumatic lifting across the entire wafer. The debonding may be performed at elevated temperature to reduce the force required. While the mechanical equipment offers attractive capital costs, there are several drawbacks of this approach. In particular, the wafer is subjected to considerable stress as the rigid carrier is peeled away, with the potential to damage the wafer's frontside. A different experimental approach is to use a laminar jet of air flow to perform the carrier lifting, together with elevated temperature to soften the adhesive.

The excimer laser represents a viable alternative process (**Figure 6**), with both the 248nm and 308nm output wavelengths being used for different carrier types and adhesives. Here the large beam with a rectangular cross section is projected through the glass carrier, which is transparent to the laser light. The laser is strongly absorbed by the adhesive material so that all the energy of the laser pulse is absorbed within 20nm. The deep ultraviolet light directly breaks the chemical bonds

and vaporizes (ablates) this thin layer of the adhesive. The gas and debris generated from the ablation drives the carrier to separate easily from the device wafer or panel. This ablation is usually carried out at low fluence, so there is no possibility of laser damage to the active devices on the wafer itself during the ablation process.

The excimer debond process is fast because each location only requires a single laser pulse for complete elimination of adhesion. For example, in the SUSS ELD 300 (equipped with a Coherent COMPex laser operating at a repetition rate of 49Hz), the laser is projected as a 4 x 12mm field size. Fast scanning of this field across the wafer covers the entire area in 50 seconds (**Figure 5**). The modest pulse rate for the laser means a life expectancy of several years without major maintenance, minimizing overall cost of ownership. (The lifetime of excimer laser components are determined by accumulated pulse counts.)

As with the mechanical process, some residual adhesive remains on the wafer, which is then removed using standard chemical methods. The main advantage of the excimer debond process is that the risk of stress damage to the wafer is eliminated. One caveat is that TWB materials have to be compatible with laser ablation. Many already established TWB materials, however, such as PI

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and ABF, absorb strongly at 308nm, ensuring efficient ablation.

Summary

As in other areas of microelectronics fabrication and related industries, advanced packaging is currently overcoming the challenges driven by relentless miniaturization. The excimer laser is again uniquely positioned to provide a high-throughput solution for several of these processes, just as it has previously done in front-end lithography, high brightness display annealing, and laser lift-off for flexible displays. The excimer laser offers multiple advantages for advanced packaging applications, including ablation of via and trenches (dual damascene), seed layer removal, and debonding. This enabling technology is likewise poised to provide a cost advantage for both current and future packaging applications.

References

1. H. Hichri, S. Fujishima, S. Lee, M. Arendt, S. Nakamura, "Fine line routing and micro via patterning in ABF enabled by excimer laser ablation," IMAPS Conf. 2017, Durham, NC, USA.
2. H. Hichri, M. Arendt, "Ultra-fine RDL formation using an alternative patterning solution for advanced packaging," IMAPS Conf. 2018, Pasadena, CA, USA.
3. R. Hallman, O. Dimov, S. Malik, H. Hichri, M. Arendt, "Ultra-fine RDL structure fabrication using alternative patterning and bottom up plating processes," ECTC Conf. 2018, San Diego, CA, USA.
4. H. Hichri, M. Arendt, M. Gingerella, "Novel process of RDL formation for advanced packaging by excimer laser ablation," ECTC Conf. 2016, Las Vegas, NV, USA.

Design-for-reliability and accelerated-testing of solder joint interconnections

By Ephraim Suhir [Portland State University]

The following three reliability-related questions for solder joint interconnections (SJIs) in integrated circuit (IC) packaging are addressed: 1) Could inelastic strains in the SJIs be avoided by a rational physical design of the IC package, and, if not, could the sizes of the peripheral inelastic strain areas be predicted and minimized? 2) Realizing that, because of the inevitable uncertainties, the difference between highly reliable and an insufficiently robust electronic products is “merely” in the levels of their never-zero probabilities of failure, could these probabilities be assessed at the design stage, using an appropriate approach? and 3) Given that SJI accelerated testing by temperature cycling is costly, time- and labor-consuming and possibly even misleading (because of temperature dependency of material properties and a much wider temperature range during temperature cycling than what will most likely be encountered by the package in the field), should it be replaced by a more physically meaningful, less expensive and more trustworthy test vehicle, such as, e.g., low-temperature/random-vibrations bias? In the analysis that follows, the above questions are addressed and critical improvements in the state-of-the-art in SJI reliability are suggested.

Background

SJIs and, particularly, lead-free solders are the most vulnerable structural elements in today’s IC packages (e.g., [1-3]). This is mostly because solder materials typically experience inelastic strains, and, as a result of that, are subjected to low cycle fatigue (e.g., [4]), which makes their fatigue lifetime much shorter than required for many applications. There is an obvious incentive, therefore, to explore ways for bringing down the stresses and strains in the material, possibly even to an extent that the inelastic strains are avoided [5]. If this is achievable, the material’s fatigue

lifetime will be improved dramatically, and the well-established Palmgren-Miner rule of linear accumulation of damages could be used, instead of various Coffin-Manson relationships, to predict it. If not, then the sizes of the inelastic zones could and should be evaluated and possibly minimized [6,7]. The first objective of this analysis is to establish ways for doing that.

The reliability of an electronic material or a product cannot be assured, if it is not quantified. This should be done during the design stage and, because of the inevitable and critical uncertainties, on a probabilistic basis. The reliability evaluations and assurances cannot be delayed until the products are manufactured, burn-in tested, and the burn-in “survivors” shipped to the customer(s). In other words, operational reliability evaluations cannot be left to today’s highly popular prognostic-and-health management (PHM) effort (e.g., [8]) that monitors the product’s behavior and performance in the field, and, when necessary, interferes with the appropriate action(s). With all the usefulness of this effort, it is too late, when relying on it, to change the material or the design, and thereby creating a “genetically healthy” product. The suggested probabilistic design for reliability (PDfR) approach [9] is able to do that.

The PDfR approach should be developed and employed as an effective means for predicting and assuring the operational reliability by assessing the expected probability of failure [10-12]. The challenge is, of course, to assess this probability, and to make it adequate for the particular product and application. If one develops a consistent and a trustworthy way to quantify reliability, then this might open a promising and a fruitful way to optimize it, i.e., to establish, for the given packaged product and application, the best compromise between the product’s reliability, its cost, and the time to market (completion).

Reliability cannot be low, but does not have to be superfluously high either: it has to be adequate for a particular product and application. If a material or a device “never fails,” it is usually an indication that it is “over-engineered,” and is probably unnecessarily expensive for the particular application. The PDfR effort should be based on a physically meaningful, easy-to-use and, since understanding the physics of failure is always critical, failure-oriented-accelerated-testing (FOAT) [13,14] methodology geared to a trustworthy constitutive equation. It has been demonstrated [15-18] that the Boltzmann-Arrhenius-Zhurkov (BAZ) equation (e.g., [19]) can be effectively employed in this capacity. The second objective of this analysis is to establish ways for doing that.

Temperature cycling is today the most widespread accelerated test technique. It is, however, costly, time- and labor-consuming, but, most importantly, can result in misleading information. This is because a material’s properties are temperature dependent, and testing is done over a wide temperature range—much wider than what the material might encounter in actual operating conditions. There is a clear motivation, therefore, to consider an accelerated test vehicle that would be more physically meaningful and, perhaps, less costly and easier to conduct. Because the highest thermal stresses occur at low-temperature conditions and fatigue crack propagation is accelerated by random vibrations, a low-temperature/random-vibrations bias is suggested as an attractive substitute for temperature cycling, especially for applications (e.g., automotive or aerospace) when such a bias reflects the actual loading conditions in the field [20]. The suggested technique has already been reduced to practice in an industrial lab. The third objective of this analysis is to show the attributes of the low-temperature/random-vibrations bias as an appropriate test vehicle.

Findings and considerations associated with the above motivations are set forth below. Future work should focus on experimentations to confirm the obtained findings.

Analysis

The following sections address different aspects of the analysis.

Could inelastic strains in the solder material be avoided? Effective technologies for a rational physical design of low stress SJIs, even sometimes below the yield stress, were suggested and confirmed by analytical modeling and illustrated by numerical data. This could be done by using SJIs with elevated stand-off heights [20-23] (**Figure 1**) and/or by employing inhomogeneous SJI systems, in

surfaces are reliably anchored, and that enough interfacial real estate is provided so that the joints' bonding strength is not compromised. On the other hand, owing to lower stresses in solder systems with elevated stand-off heights, assurance of their bonding strength is less of a challenge than in the case of conventional, BGA, joints. By employing beam-like joints, and, perhaps, in combination with inhomogeneous SJI designs and lower melting temperatures for the peripheral joints, one might even be able to avoid inelastic deformations in the solder material, thereby dramatically increasing its fatigue lifetime. The numerical example carried out for a CGA assembly with a low-modulus and low-fabrication temperature bonding material at the

assembly ends has indicated

that stress relief as high as 34.3% can be achieved compared to an assembly with a homogeneous bond. The stand-off height of a beam-like joint characterized by the elastic state-of-stress should be significant enough to make the shearing stress low. This will take place for height-to-diameter ratios not exceeding, however, 8-12. The further increase in the stand-off heights, even if technologically achievable, is not advisable, because it will lead to undesirable appreciable bending stresses.

Future work in the improved physical design of SJIs should include the finite element analysis (FEA) computations and experimental evaluations, such as, e.g., shear-off testing to evaluate the fatigue lifetime and ultimate shearing stress of typical BGA and CGA assemblies. Significant and even optimized stress relief in the SJIs could be obtained by imposing a requirement that the induced interfacial thermal shearing stress in the mid-portion of the assembly at its boundary with the peripheral portions is equal to the stress at the assembly ends [26,27]. The expected stress relief is dependent, of course, not only on the solder, but also on the soldered materials properties and the assembly geometry.

Could the probability of the field failure be predicted at the design stage? The era in electronic materials science,

when "we heat, we beat and we pray" has gone. In today's research world, when the behavior and performance of a material, and the operational reliability of an electronic product are critical, the ability to predict (quantify) this reliability and, if possible and advisable, even to specify it, is imperative. Furthermore, because nothing is absolutely certain, such a prediction should be done on a probabilistic basis. The PDFR concept enables one to predict, from the highly focused and highly cost-effective FOAT, the expected probability of failure in the field for the given time in operation and for the given (expected) loading conditions. It has been shown that the physically meaningful BAZ model (see, e.g., [9,10]) could be applied to predict this probability from the FOAT data.

Application of the PDFR approach can make a significant difference in the current state-of-the-art in electronics and photonics materials science and reliability predictions. The BAZ equation (model)

$$\tau = \tau_0 \exp\left(\frac{U_0 - \gamma\sigma}{kT}\right) \quad (1)$$

has been extended and implemented in application to electronic materials and structures when operational reliability is paramount and the ability to quantify it is therefore imperative. Here, τ is the mean time to failure (MTTF), U_0 is the stress-free activation energy, T is the absolute temperature, $k = 8.6173324 \times 10^{-5}$ eV/K is Boltzmann's constant, kT is the thermal energy, σ is the applied stress (per unit volume), γ is the sensitivity factor, and τ_0 is the time constant.

Figure 2 shows a solder joint with an elevated stand-off height: predictive modeling and FOAT. **Figure 2a** illustrates the joint in a Si-on-Si design that was modeled as a short cylinder whose butt plains were subjected to radial in-plain strains. **Figure 2b** illustrates that the analytical modeling confirmed by finite element analysis (FEA) shows how the stresses and strains in the solder "bump" increase with an increase in the ratio of its diameter to the stand-off height. FOAT (**Figure 2c**) was conducted until half of the tested population of solder joints failed. **Figure 2d** provides results of a solder joint with an elevated stand-off height where a significant portion of the experimental bathtub curve (BTC) is the wear-out one and should be considered when fatigue lifetime is predicted.

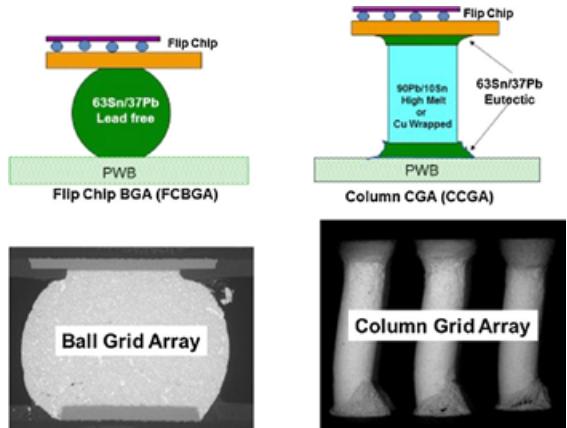


Figure 1: CGA vs. BGA technologies. Elevated stand-off heights in CGA designs increase the interfacial compliance of the SJI system, thereby reducing the interfacial stresses.

which solders with lower Young's moduli at the assembly's peripheral portions are used [24-26]; also, if possible and feasible, under lower soldering temperatures and/or by employing low expansion substrates (such as, say, ceramic ones). Some recent findings associated with the use of inhomogeneous ball grid array (BGA) and column grid array (CGA) technologies (**Figure 1**) for lower thermally-induced stresses indicate that this is indeed possible, but, if not, the size of the peripheral inelastic zones could be predicted and possibly minimized. The incentive for using SJIs with elevated stand-off heights had been indicated about thirty years ago in connection with the Bell-Labs' Si-on-Si flip-chip and multi-chip modules technologies [21].

It is imperative, of course, that if joints with elevated height-to-diameter ratios are employed, their end ("butt")

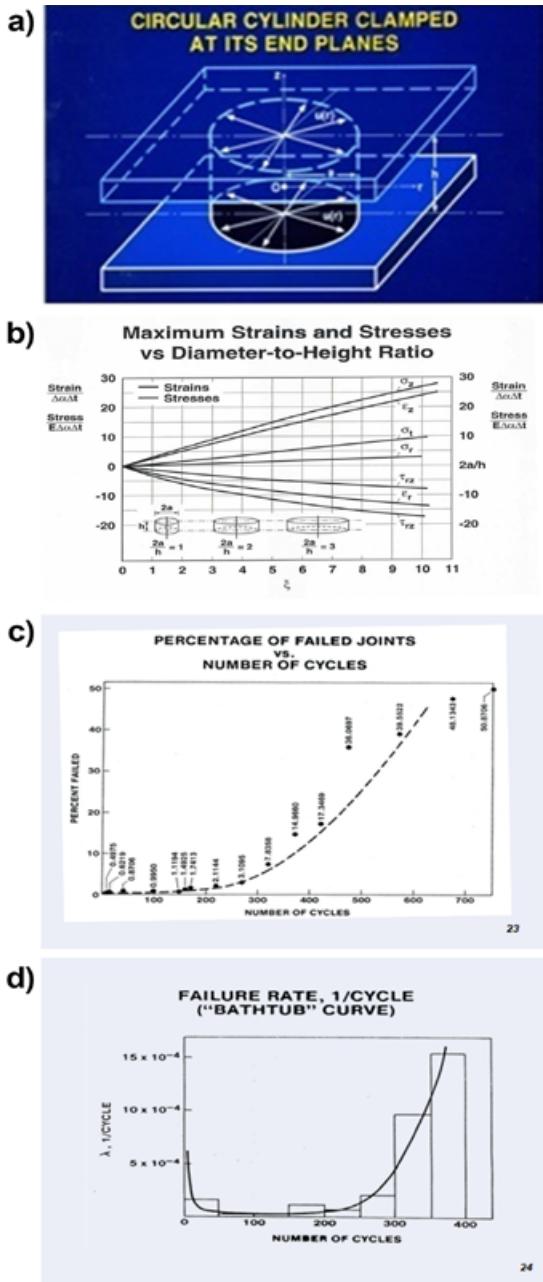
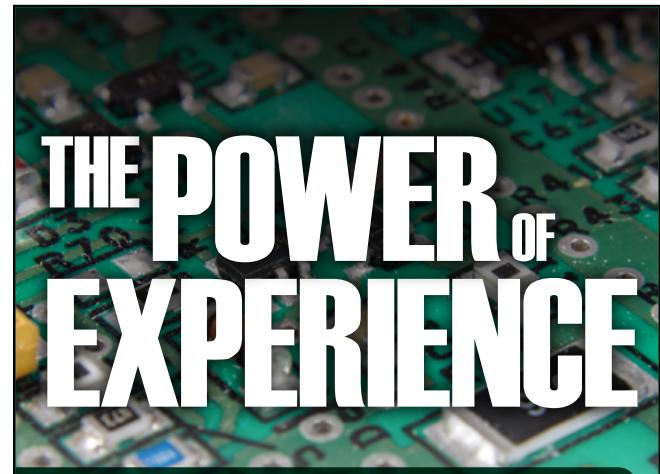


Figure 2: A solder joint with an elevated stand-off height: predictive modeling and FOAT. Refer to the text for discussions of the separate panels (a-d).

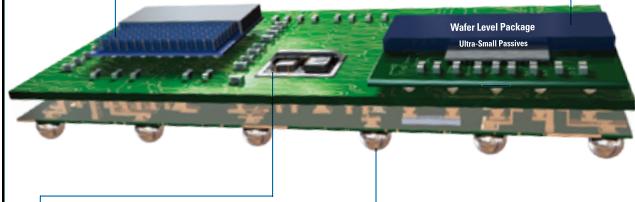
FOAT is the experimental basis of the PDFR concept and should be conducted in addition to and, in many cases, even instead of the highly accelerated life testing (HALT), especially for new products, for which no experience is yet accumulated. FOAT is a “transparent box” and could be viewed as an extension of HALT, a “black box” that is unable to shed light on the physics and the likelihood of failure. HALT can be used, therefore, for “rough tuning” of a product’s reliability, while FOAT could be employed when “fine tuning” is needed, i.e., when there is a need to quantify, assure and even specify the operational reliability of a product. The FOAT-based approach could be viewed as a quantified and reliability physics-oriented HALT and should be geared to a particular technology and application, with consideration of the most likely stressors.



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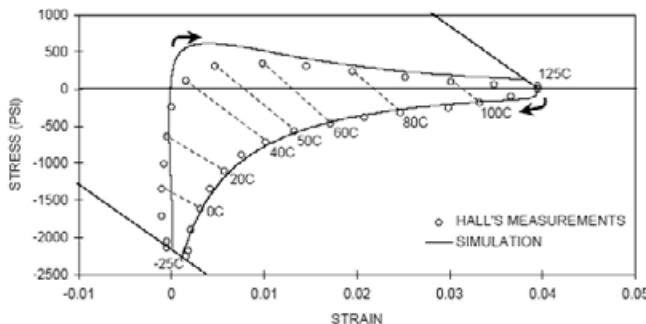


Figure 3: Hysteresis loop obtained for one cycle of SJI testing: P. M. Hall's approach [28,29].

Should temperature cycling accelerated testing for SJIs be replaced? In the effort reduced to practice under a project with NASA Jet Propulsion Lab, random vibrations were considered as a white noise of the given level, characterized as the ratio of the acceleration amplitudes squared to the vibration frequency. Testing has been carried out for two printed circuit boards (PCBs), with surface-mounted packages on them, at the same level (with the mean value of 50g) of three-dimensional random vibrations. One board was subjected to the low temperature of -20°C and another to a temperature of -100°C. It has been found by preliminary calculations that the joints tested at -20°C will still perform within the elastic range, while the joints at -100°C will experience appreciable inelastic strains. No wonder that no failures were detected in the joints of the board tested at -20°C, while the joints of the board tested at -100°C failed after several hours of testing. Using the BAZ model, the probability of non-failure of the SJI experiencing inelastic strains during temperature cycling can be sought in the form (see Figure 3):

$$P = \exp\left[-\gamma R t \exp\left(-\frac{U_0 - nW}{kT}\right)\right]. \quad (2)$$

Here U_0, eV , is the activation energy that characterizes the propensity of the solder material to fracture, W, eV , is the damage caused in the solder material by a single temperature cycle and measured, in accordance with Hall's concept [28,29],

by a hysteresis loop area for the given inelastic strain, T^0, K is the absolute temperature (say, the mean temperature of the cycle), n is the number of cycles, k , eV/K is Boltzmann's constant, t, sec , is time, R , Ω , is the measured (monitored) electrical resistance at the joint location, and γ is the sensitivity factor for

the measured electrical resistance. Equation (2) makes physical sense. Indeed, the probability P of non-failure is "one" at the initial moment of time and when electrical resistance of the solder joint structure is zero. This probability decreases with time because of the material aging and structural degradation, and not necessarily only because of temperature cycling; it is lower for higher electrical resistance (a resistance as high as, say, 450Ω, can be viewed as an indication of an irreversible mechanical failure of the joint); materials with higher activation energy U_0 have a higher probability of non-failure; the increase in the number n of cycles leads to lower effective energy $U_0 - nW$, and so does the energy W of a single cycle. It could be shown that the maximum entropy of the distribution (2) takes place at the mean time to failure (MTTF) τ expressed as:

$$\tau = \frac{1}{\gamma R} \exp\left(-\frac{U_0 - nW}{kT}\right). \quad (3)$$

Mechanical failure, because of temperature cycling, takes place, when the number n of cycles is $n_f = \frac{U_0}{W}$. When failure occurs, the temperature in the denominator in the parenthesis in equation (2) becomes irrelevant, and this equation yields:

$$P_f = \exp\left(\frac{t_f}{\tau_f}\right). \quad (4)$$

Here P_f is the measured probability of non-failure for the situation, when failure takes

place, and is $\tau_f = \frac{1}{\gamma R_f}$ the MTTF. If, e.g., 20 devices have been temperature cycled and the high resistance $R_f = 450\Omega$, considered as an indication of failure was detected in 15 of them, then $P_f = 0.25$. If the number of cycles during such FOAT was, say, $n_f = 2000$, and each cycle lasted, say, for 20min=1200sec., then the predicted time t_f at failure is $t_f = 2000 \times 1200 = 24 \times 10^5$ sec, the factor γ is $\gamma = \frac{-\ln P_f}{R_f t_f} = \frac{-\ln 0.25}{450 \times 24 \times 10^3} = 1.2836 \times 10^{-3} \Omega^{-1} \text{sec}^{-1}$, and the MTTF is $\tau_f = \frac{1}{1.2836 \times 10^{-3} \times 450} \text{sec} = 480.9 \text{hrs} = 20.0 \text{days}$.

According to Hall's concept, the energy, W , of a single cycle should be evaluated by running a specially designed test, in which strain gages should be used. As an example, in the above tests this energy (the area of the hysteresis loop) was $W = 2.5 \times 10^{-4} \text{eV}$. Then the stress-free activation energy of the solder material is $U_0 = n_f W = 2000 \times 2.5 \times 10^{-4} = 0.5 \text{eV}$. In order to assess the number of cycles to failure in actual operating conditions one could assume that the temperature range in these conditions is, say, half the accelerated test range, and that the area, W , of the hysteresis loop is proportional to the temperature range. Then the number of cycles to failure is $n_f = \frac{U_0}{W} = \frac{0.5}{2.5 \times 10^{-4}} = 2000$.

If the duration of one cycle in actual operating conditions is one day, then the time to failure will be $t_f = 2000 \text{days} = 5.48 \text{years}$.

Summary

There are several effective ways to relieve stresses and strains in SJIs of IC packages. Future work should include experimentations to confirm the obtained findings and recommendations.

References

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Biography

Ephraim Suhir is on the faculty of Portland State U., Portland, OR, and is also CEO of ERS Co., Los Altos, CA, USA. He has authored 400+ publications, presented numerous keynote and invited talks worldwide, and received many professional awards, including 1996 Bell Labs DMTS Award, 2004 ASME Worcester Read Warner Medal (he is the third "Russian American," after S. Timoshenko and I. Sikorsky, who received this prestigious award), 2019 IEEE EPS Field award for seminal contributions to mechanical reliability engineering and 2019 IMAPS Life Achievement Award for making exceptional, visible, and sustained impact on the microelectronics packaging industry in technology, business or both. Email suhire@aol.com; www.ERSuhir.com

Focused adhesives: customized materials for 3D printing

By Brian Violette, Michele Thompson [Creative Materials Inc.]

As both chip-scale and board-scale electronic devices continue to increase in complexity while decreasing in size, the requirements for developing more compact electronics steadily drive innovation. This requires new, high-precision application methods in conjunction with specialty materials that allow for miniaturized and targeted deposition.

Requirements for increased functionality and shrinking device footprints drive the need for increased interconnect densities and innovative form factors. Technology companies are now reaching the limits of Moore's law and need to explore different innovative techniques to continue providing higher performance electronics. One method chip and package manufacturers are developing to try and move past Moore's law is using 2.1D, 2.5D and 3D stacked die to improve device functionality and decrease overall size. These design innovations create a new set of challenges regarding interconnects, both at the chip- and board-scales.

Flexible and stretchable substrates are being explored in applications requiring smaller device footprints by allowing for folding and bending of the finished devices. Highly compliant interconnect materials are required to absorb the high stress where these flexible substrates connect to the conventional rigid electronic materials. Traditionally, high solids jetting, screen printing, and stencil printing have been employed to apply interconnect materials in these applications, but these technologies have not adapted to shrinking pad sizes and pitch.

Traditional materials used to interconnect with chip-scale devices include solder pastes and gold wire bonding. These materials have their limits in terms of versatility and reliability. Interconnects introduce a point of failure in the device. The fine gold wires used to bond at the chip scale are very fragile and prone to breaking. Often a secondary adhesive is necessary to hold the chip in place on the package. A third material may be needed for encapsulation for protection from moisture, shock, and abrasion. Wire

geometry combined with the additional materials for encapsulation and protection increase the overall package volume.

Solder pastes are most commonly used for flip-chip bonding and can interconnect with through-silicon vias for 2.5D and 3D stacked-die applications. These pastes are often high stress creating another potential point of failure. More fragile thinned die are not suitable for traditional application methods used for applying solder pastes. Stencil printing of solder paste on these thinned materials creates reliability issues related to the cracking of the die during paste application.

Aerosol jet printing basics

Aerosol jet printing overcomes the limitations of traditional methods associated with fragility and provides a solution to further reduce electronic footprints. Additionally, aerosol jet printing is a non-contact application method, making it ideal for complex geometries and fragile substrates. The digital nature of this application technique makes it incredibly versatile and makes it easy to implement any necessary designs. While this technology has been commercially available for 15 years, it has focused primarily on metal nanoparticle ink technologies, however, polymer-based materials can offer a better range of properties if implemented correctly.

Aerosol jet printing utilizes a focused beam of atomized ink and gases. The aerosol mist is focused by a concentric sheath gas that provides the ability to be applied in extremely small feature sizes. With aerosol jet printing, features sizes can typically be applied from $<10\mu\text{m}$ to $>300\mu\text{m}$. Not only does this technology have the ability to print features in a large range of sizes, it also has the ability to print materials with five axes of rotation. This means that materials can be applied around corners, in wells, and up the walls of three-dimensional parts (**Figure 1**). This versatility allows for more complex and compact designs than previously done before. For example, in stacked die, the connections that would have traditionally been made by wire bonding can be made by writing a

trace up the side of the chip. This both saves space and improves reliability of the stacked die. Because of the non-contact nature of aerosol jet printing, it is ideal for substrates that are very thin and extremely fragile. Ultra-thin polymer substrates, which are prone to tearing, and thinned wafers, are not exposed to mechanical stress during aerosol jet printing and can now be utilized in more complex applications. This allows for a wider range of substrates that can be used, which means more specialized technologies can be created—for example, wearable devices.

Current commercial applications of aerosol jet printing are primarily focused on printing metal nanoparticle inks. Metal inks require sintering for good mechanical and electrical performance. Typical sintering temperatures for a silver paste are in excess of 230°C and can be much higher for other precious metal-based materials. The high-temperature processing required for metal inks can be a limiting factor for boards with integrated sensors, oscillators, capacitors, or fuses that will be negatively impacted by high-temperature exposure. However, functional polymer-based materials don't require metal sintering for performance, they can therefore be suitable for lower, and even ambient-temperature processing. In addition to preserving temperature-sensitive components, lower processing temperatures allow for a wider variety of substrate material options, including textiles, thermoplastic urethanes (TPUs), and other organic substrates.

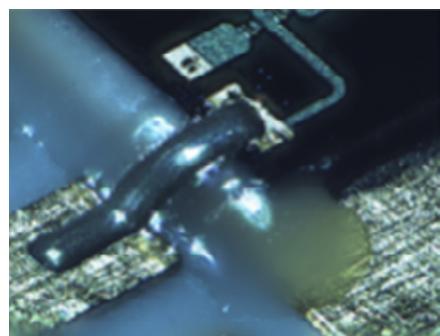


Figure 1: Aerosol jet application of conductive ink up the wall of a chip – replacing wire bond.

Advanced materials for aerosol jet printing

Functional polymer composite inks do provide many advantages over fired nanoparticle inks, but they are at a disadvantage when it comes to minimum feature size and deposition thickness. With current material technologies, the achievable feature size for functional polymer composite materials has not achieved the same minimum feature size as for fired nanoparticle ink technologies. However, line widths as fine as 30 μm have been achieved using functional polymer composite inks. This marks a dramatic improvement in minimum feature size over incumbent application technologies. Typical deposition thicknesses for a sintered metal ink are sub-micron or single-digit microns. Functional polymer materials require higher deposition thicknesses on account of the lower metal content. Typical thicknesses for aerosol jet-printed polymer composite materials are in the range of 3–10 μm compared to sintered metal materials that are typically used at <3 μm .

A major advantage of functional polymer-based adhesive materials is that it allows for customization of a wide array of properties. Polymer chemistry can be adjusted to adhere to substrate types that would not be feasible with other conventional adhesive technologies. This includes silicones, olefin, and Teflon materials. This ability enables new design choices for wearable electronics and IoT/smart packaging markets. New wearable devices push to further improve the comfort and wearability of devices. Silicone is often chosen as a substrate for its biocompatibility and breathability. However, it is inherently difficult to adhere to silicone materials. To overcome this difficulty, silicone-based adhesives are needed for bonding because of the need for good compatibility between the low surface energy materials. The combination of aerosol jet printing and stretchable conductive inks and adhesives for silicone substrates allow for ultra-thin, highly-conformable wearable electronic devices.

Not only can functional polymer-based inks and adhesives be customized based on polymer chemistry, they can also be customized with regards to their thermal properties. Thermal expansion, glass transition temperature, and thermal conductivity can all be modified to improve reliability in thermal cycling. This ability to design the thermal properties also allows materials with dissimilar thermal properties

to be bonded without fear of breaking the bond line. Low-stress materials can be used for bonding substrates with very different coefficients of thermal expansion (CTE). The CTE of the aerosol jet-printable adhesive can be modified to mate the two materials being bonded and can be applied with high accuracy and precision.

Various filler types can also be used to customize and optimize polymer-based material properties and cost. For conductive applications, a variety of precious metals and conductive fillers can be used to achieve desired properties. Where corrosive environments are concerns, polymer adhesives can be filled with gold or platinum for long-term stability. Silver offers several advantages over other conductive fillers because it has the highest conductivity with a lower cost to use compared to other precious metals. For a low-cost conductive option, carbon-based materials can be used in applications where a higher resistivity is acceptable, or even desirable, such as printed resistors. Electrically-conductive inks and adhesives are not the only polymer-based materials that can be utilized for aerosol printing—dielectric materials can also be aerosol printed for providing insulation or creating capacitive features. Printing a dielectric adhesive at circuit cross-over points creates something similar to a multi-layer circuit board, but with the freedom of design associated with using an additive manufacturing process. Utilizing the multiple materials that can be aerosol printed can help manufacture more compact package sizes in previously impossible form factors.

Innovative form factors are required to improve device density to minimize device size. Many manufacturers are exploring placing die and chip-scale devices within a substrate cavity to provide thin form factors with increased performance. Connecting to these devices is not possible using traditional techniques because of the complexity of creating interconnects in the recessed area. The three-dimensional nature of aerosol jet printing allows conductive features to be written on the wall and within recessed cavities enabling this type of device construction. The additive nature of this technique allows for printing onto and over features that can be non-uniform and have high-aspect ratio features (**Figure 2**).

Aerosol jet printing is a digital process. This is beneficial for producing devices that have a high degree of variability. The application path can be adjusted part-to-

part to accommodate large variations in part geometry. This digital nature also allows for low-cost prototype designs. Parts can be designed rapidly thereby allowing for one-off designs and low-volume production runs without the high set up cost of other manufacturing techniques. Drop on demand allows for extremely efficient use of materials by minimizing waste from the priming of equipment, or losses due to start-up and shut-down.

Aerosol jet dispense equipment does place limitations on the types of polymer-based materials that can be used. Special care needs to be taken by materials manufacturers to optimize material properties with regards to particle size and morphology, volatility, viscosity, viscoelastic behavior, drying rate, and volatile content. Understanding of how these material properties affect dispense parameters is critical to determining the best use conditions and equipment settings. Tight control of viscoelasticity, particle size, and particle morphology is critical to achieving consistent material deposition. Aerosol jet printing requires low-viscosity materials, which creates a challenge to material suppliers to control dispersion and settling of dispersed solids over long run times.

Understanding of how different materials are atomized and deposited is critical for ensuring homogeneity of the applied material. Avoiding selective atomization of fillers, solvents, or binder is crucial to ensure stability over long run times. Changes in material behavior on account of selective atomization of its components creates an unstable process that hurts device yields. Proper system formulation is critical to ensuring that material can be applied in a stable production process.

Special considerations of the viscosity in the bulk material needs to be controlled, as well as the viscosity of the deposited material



Figure 2: Aerosol jet printing enables printing features that conform to high-aspect ratio geometries and around corners.

after application. Drying rate and thixotropy need to be optimized in order to allow the material to be applied with a high-aspect ratio and minimal spreading, de-wetting, overspray and other common print defects. Optimization of these properties allows a material to have multiple layers applied with sharp edge definition and well-controlled feature thickness (**Figure 3**). Good control of material deposition is critical as interconnect feature sizes continually decrease, and with smaller footprints, the likelihood for shorting or cross-talk increases.

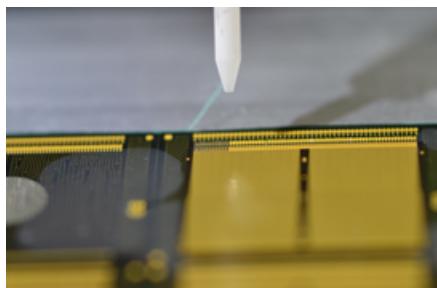


Figure 3: Selective aerosol jet application of discrete fine-feature pads for component attachment.

Summary

Developing adhesives for aerosol jet printing requires designing for more stringent specifications. Furthermore, adhesives for aerosol jet printing are able to be applied in fine-feature sizes on complex geometries that were previously not viable with other application methods. Adhesives developed for this additive manufacturing technique can be applied to features and pitches as small as 30 μm . The adhesives can also be modified to meet specific requirements, such as adjusting for modulus, thermal expansion, glass transition temperature, stress, resistivity, and much more. The fine feature size and customized adhesive property set enable the manufacture of ultra-flexible, high-density devices in complex form factors enabling the next-generation of wearable, mobile, and IoT devices.



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3D-printed substrates for wafer-level and chip-scale fluidic packaging

By Douglas Sparks *[3D Printed Wafer LLC]*

Additive manufacturing (AM), or 3D printing, is finding increasing applications in virtually all fields including electronics and sensors—starting with plastic prototype housings and custom printed circuit boards (PCBs) [1]. The wide variety of materials that can be used, reduced system parts count, and faster prototyping times are the prime incentives for employing AM. 3D printing of individual industrial and automotive metallic sensors and packages [2,3] is still a relatively expensive option for metal working, and in many cases only cost-competitive with computer numerical control (CNC) casting and welded assembly for low-volume prototyping. To overcome this cost disadvantage, multiple sensors can be fabricated during the same print operation. This is the same commercialization path that was taken for microelectromechanical systems (MEMS) sensors decades ago. The first MEMS pressure sensors used the entire 1" silicon wafer, and now more than 10,000 MEMS sensors are made on 150mm and 200mm wafers. AM allows the engineer to move from a computer-aided design (CAD) file to a structured multi-sensor wafer without the cost and time of photomask fabrication. **Figure 1** shows how a 3D-printed metal MEMS 100mm diameter wafer can produce multiple small sensors and leverage wafer fab lithography tooling for building up surface circuitry layers. This titanium wafer was printed using the direct metal laser sintering (DMLS) method.



Figure 1: 3D-printed 100mm titanium wafer.

Most metal additive manufacturing does not stop after the 3D printing step. Challenges associated with AM processes, such as cracks and warpage due to stress, have to be overcome to enable the successful 3D printing of micromachined wafers. For many applications, including micromachined wafers, post-processing will be required. Post-processing of printed metal parts can start immediately after the printing step. Laser and e-beam fabrication metal products are in a stressed state very similar to a welded metal part. As in the case of welding, an anneal step can reduce some of this built-in stress, which reduces the likelihood of warpage and cracking. Polishing is another post-print step needed for most AM MEMS wafers to produce a smooth, flat surface suitable for subsequent photolithography processing. The use of this patent-pending AM process for making wafer-level packaging (WLP) top cap chips is shown in **Figure 2**.

The same types of cavities and bond pad openings made in silicon wafers (left image in **Figure 2**) as a cap over MEMS devices

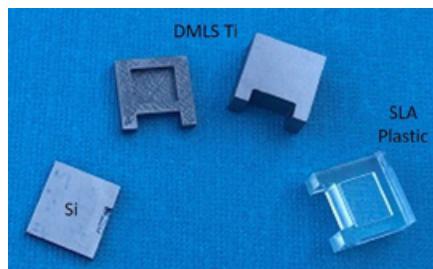


Figure 2: WLP top cap chips, conventional MEMS silicon (left) and 3D-printed DMLS titanium and SLA clear plastic.

using wafer bonding [4,5] can be duplicated with various 3D-printed metals and optically clear plastics. Thick metal wafers for better electromagnetic compatibility (EMC) or rad-hard performance can be printed. Ink jet and 3D-printed coatings of circuit boards have already been explored to provide radiation shielding for space applications [6]. Graded-Z, or graded atomic number, AM layers can enhance the reliability of

components, and shielding can start with a chip-scale package (CSP), or as a post-surface-mount cap over the electronic component for space applications.

AM capping wafers, or device wafers using a chemically-active metal like titanium, enables the fabrication of a gas gettering surface for vacuum packaging without the need for a thin-film getter [7,8] deposition and patterning steps. The rough as-printed titanium surface shown in the cavity recess in **Figure 2** is well suited for a higher surface area impurity-absorbing CSP. The printed wafer material itself can act as this absorbent getter material. Printing a clear plastic, shown on the right of **Figure 2**, or glass, also can be used in optical sensor applications.

As **Figure 3** illustrates, wafer-to-wafer (W2W) bonding is used in conventional silicon WLP to partially or fully enclose the fragile MEMS cantilevers' and resonators' device elements. 3D printing can combine the capping cavity and moving device element into one wafer. One big advantage to AM fabrication of complex MEMS and microfluidic structures is that it can reduce the number of wafer fab processing steps that would have been required with conventional

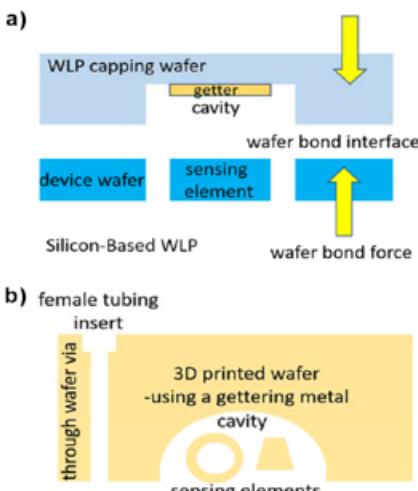


Figure 3: a) (left) Conventional silicon WLP vs. b) (right) 3D-printed WLP.

silicon MEMS processing. The longest, and hence, most expensive MEMS fab processing steps are typically deep reactive-ion etching (DRIE) and W2W bonding. In these steps, only one or two wafers can be processed at a time and they both can take more than an hour to complete. DRIE is also somewhat limited in etching direction, straight down or at a slight, fixed angle, into the silicon or glass substrate. Wafer bonding to form channels can have problems with hermeticity at the bond interface [9] and be prone to burst failure. In general, silicon has low fracture toughness and can rupture under pressure or shock, compared to metals like titanium and stainless steel.

AM can simultaneously form vertical, horizontal and multi-directional channels and other structures, without a bonding interface, as well as use fracture- and corrosion-resistant materials as illustrated in **Figure 3**. Through-wafer vias (TWVs), including fluidic vias with female tubing inserts can be printed along with other WLP elements. As **Figure 3** illustrates, if a thin-film getter is required for vacuum packaging, a chemically-reactive metal can be used to print the wafer, such as titanium [7], which eliminates these processing and lithography steps. Not only can AM reduce the MEMS processing step count by hundreds of steps, 3D printing can form substrate features that cannot be fabricated using traditional silicon-based micromachining. **Figure 3b** shows how TWVs, cantilevers, suspended microtubes, and curved horizontal and vertical surfaces can all be simultaneously printed in one step, which is not possible using a silicon wafer and standard processing.



Figure 4: Epoxy chip attachment failure.

exposure over time. AM offers a way of combining the microfluidic sensor and sub-package into a single, weldable component as shown in **Figure 5**. **Figure 5** shows that both female tubing inserts (left) or male tubing (right) interfaces can be 3D-printed as part of a chip-scale fluidic package (CSFP). A CSFP that can be laser welded for metal or solvent welded for plastic, to the package, and is a big improvement in reliability for microfluidics in aggressive applications. The CSFP overcomes the chip attachment reliability problems found in silicon and glass. The CSFP parts in the main photo of **Figure 5** are used for microfluidic applications like resonant tube flow and density sensors and heat sinks. The inset in **Figure 5** also shows a printed TWV that has an aspect ratio of 10:1, comparable to silicon DRIE. Via printing through 5mm-thick wafers – roughly 6 to 10

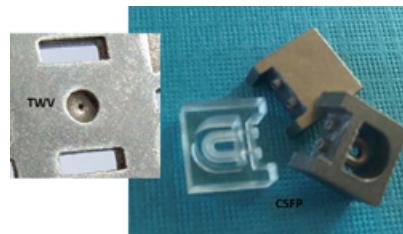


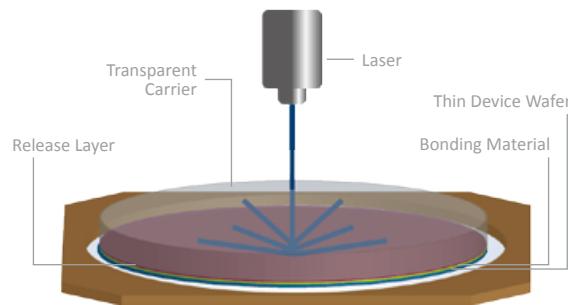
Figure 5: Through-wafer via with female tubing insert (inset) and three chip-scale fluidic packages with male tubing side inlets/outlets (main photo).



Creating Safe Environments

Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with:

308 nm

343 nm

355 nm

times thicker than a typical 100-200mm diameter silicon wafer – has been demonstrated. This technology can be applied to flow and pressure sensors, heat sinks, mixers, micro-reaction chambers, and other microfluidic applications.

For sensors there is often a need for an electrical interface, generally on the device wafer. Screen, ink jet and 3D printing are generally limited to minimum feature dimensions for metal traces of 50 to 150+ microns across. MEMS silicon wafers integrate the electrical interface for sensors using wafer fabrication processes, leveraging integrated circuit (IC) fab technology. This can also be accomplished with AM+MEMS® wafers. By using wafer fab photolithography tools, the minimum feature dimensions for metal traces can go down to 5 to 2 microns for proximity tools, and from 2 microns to less than 90 nanometers for stepper lithography tools. To use fab lithography tools requires a planar surface and a round wafer-shaped substrate, like that shown in **Figure 1**.

CMOS wafer foundries will not allow processing of wafers made from transition metals and alloys like those used in AM+MEMS® wafers. The cross-contamination of silicon CMOS/BICMOS wafers with transition metals can cause high PN junction leakage currents, emitter-collector pipes, degraded minority carrier lifetimes and degraded gate oxide. Many traditional, pure MEMS foundries, which do not process CMOS circuit wafers, have allowed the processing of sodium-containing borofloat glass [4] and other substrates like titanium wafers [10]. This substrate flexibility opens up the possibility not only to the prototyping of AM+MEMS® wafers, but also high-volume manufacturing (HVM). Metal and glass wafers of 100mm, 150mm and 200mm diameters are already being processed in some MEMS fabs, which will be natural manufacturing sites for the speedy commercialization of this new AM+MEMS® technology.

Summary

Additive manufacturing has been used to fabricate metal and plastic MEMS wafers and sensors. Many traditional MEMS and WLP structures have been duplicated using 3D printing. AM enables new chip-scale fluidic packaging in which weldable tubing or female tube inserts can be

formed as part of the microfluidic chip at the wafer level. Using printing and post-processing steps such as wafer polishing, traditional MEMS circuit and sensing layers can be deposited and patterned on these wafers thereby expanding their utility. Leveraging the existing MEMS wafer foundry infrastructure will enable fast commercialization of this new sensor and package manufacturing technology.

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1. E. Macdonald, et al., “3D printing for the rapid prototyping of structural electronics,” *IEEE Access*, Vol. 2, pp. 234-242, 13 Mar (2014), doi:10.1109/ACCESS.2014.2311810.
2. D. Sparks, “Metal-based wafer-level and 3D-printed packaging,” *Chip Scale Review*, Vol. 22, No. 4, pp.14-17, Jul-Aug (2018).
3. D. Sparks, “Using 3D metal printing for flow and pressure sensors,” *Flow Control*, Vol. 24, No. 2, pp. 23-25, Feb (2019).
4. M. Schmidt, “Wafer-to-wafer bonding for microstructure formation,” *Proc. IEEE*, 86, no.8, pp. 1575-1580 (1998).
5. D. Briand, et al., “Bonding properties of metals anodically bonded to glass,” *Sensors and Actuators*, A114 pp. 543–549 (2004).
6. J. Wrobel et al., “Versatile structural radiation shielding and thermal insulation through additive manufacturing,” *SSC13-III-3*, 27th Annual AIAA/USU Conf. Small Satellites, pp. 1-9 (2013).
7. B. Lee et al., “A study on wafer-level vacuum packaging for MEMS devices,” *J. Micromech. Microeng.* Vol. 13 pp. 663-666 (2003) doi:10.1088/0960-1317/13/5/318
8. D. Sparks, “Thin film getters: Solid-state vacuum pumps for microsensors and actuators: with MEMS applications the use of thin film getters for vacuum packaging passes the century mark,” *Vac. Tech. & Coating*, Vol. 11, No. 4, pp. 44-49 April (2010).
9. D. Sparks, “Advances in high-reliability, hermetic MEMS CSP,” *Chip Scale Review*, Vol. 20, No. 6, pp. 36-39, Sept-Oct (2016).
10. M. Aimi, et al., “High-aspect-ratio bulk micromachining of titanium,” *Nature Materials*, Vol. 3(2), pp. 103-105, (2004).

Biography

Doug Sparks is the CEO at 3D Printed Wafer, a subsidiary of M2N Technologies LLC (<https://3dprintwafer.com>). He has previously launched NanoGetters, been the CTO at Hanking Electronics, the EVP at Integrated Sensing Systems, and has a PhD from Purdue U. email sparks@3dprintwafer.com



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GUEST EDITORIAL



Top six considerations when selecting a fab location

By Stephen M. Rothrock [ATREG, Inc.]

This article is derived from “Semiconductor Manufacturing Strategy: Where In The World To Locate A Fab Or Cleanroom?” presented and published on October 3, 2019 at the 52nd IMAPS International Symposium on Microelectronics (International Microelectronics Assembly & Packaging Society) in Boston, USA.

The global market for advanced technology manufacturing assets is becoming ever tighter, compelling semiconductor companies to carefully explore all available options when planning manufacturing operations relating to fabs, tools, and cleanrooms. Despite the semiconductor industry's optimistic growth forecasts, global uncertainty generated by the continuing trade war between the U.S. and China is causing anxiety among advanced technology companies and forcing them to constantly rethink their manufacturing strategies. In 2019, infrastructure-rich cleanroom manufacturing assets continued to play an essential part in shaping these strategies to ensure global competitive advantage as more wafers are needed and more facilities are being built worldwide.

Despite a slowdown in semiconductor mergers and acquisitions activity, the global semiconductor market will continue to consolidate as the manufacturing needs of advanced technology companies evolve with market changes. This has put a strain on manufacturing space and resulted in a number of new capital projects and expansions that may become difficult to fulfill in the current market. A shortage of existing manufacturing space means cleanrooms and operational fabs will sell at a premium. Many companies are also looking at greenfield sites with local government incentives playing an active role. Running in tandem, there is still a shortage of used and new production tools with lead times in excess of one year to purchase new fabs from original equipment manufacturers (OEMs) or equip new fabs.

In light of all these moving parts, successful fab site selection remains crucial for advanced technology manufacturers. This article aims at providing insights into how to best approach manufacturing strategy decisions in the context of today's global semiconductor landscape.

Transaction and consolidation trends

There was a major slowdown in operational fab sales in 2018, in fact, not one operational fab sold last year. This is the first time this has happened since our firm began tracking operational fab sales in 2001. Despite this, we saw resurgence in interest in used operational fabs in the second half of 2018, which has led to multiple sales being announced or closing in 2019.

The market has seen a high level of fab transaction activity in 2019, with five high-caliber assets sold, highlighted by ON Semiconductor's \$430 million purchase of GLOBALFOUNDRIES' 300mm fab located in East Fishkill, NY. 2018 was an anomaly, with no operational fab transactions being bought or sold. Typically, there are between four and eight fab transactions in a year. The lack of supply and high demand for 200mm equipment, facilities, and capacity continues. New operational 200mm fabs will go for a premium. According to a presentation conducted by Infineon at SEMI's 2018 ITPC conference in Hawaii, another nine 200mm fabs are needed to meet the needs of power applications such as automotive and next-generation handhelds, to name just a few (Figure 1).

To cope with rising chip development costs, many semiconductor companies are turning to consolidation. In 2018, the 10 largest companies combined accounted for \$193.6 billion of total sales in the semiconductor industry, or more than 40% of the total market (Gartner). The top 25 companies are projected to grow around

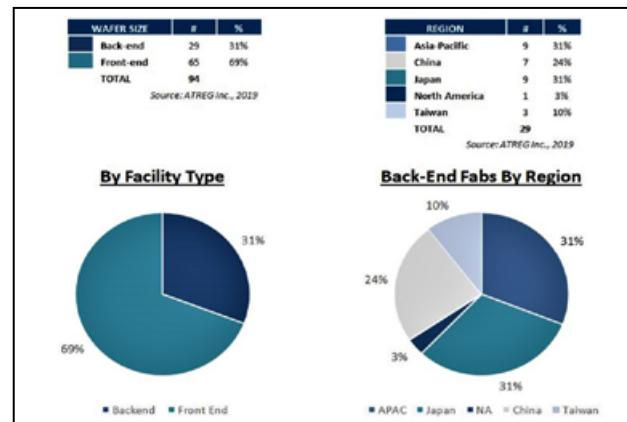


Figure 1: Fab transactions over the last 8 years. SOURCE: ATREG, Inc., 2019

16% and hold 80% market share in 2018. Samsung and Intel together made three out of every 10 dollars in the industry. In 2018, mergers and acquisitions (M&A) and semiconductor industry consolidation activity did continue, although an increasing number of deals were blocked due to regulatory reviews by governments in Europe, China, and the U.S. (e.g., Qualcomm/NXP deal) (Table 1).

	2017	2018	2019
Number of transactions	76	32	35
Value (millions USD)	35,879	48,244	44,192

Table 1: Number of transactions and their value between 2017 and 2019. SOURCE: Stifel, includes announced and closed transactions.

Financial investment

The investment needed to purchase a fab will vary depending on the type and size of fab in which a company is interested. Securing used tools over new ones will reduce the CapEx needed to start a facility. However, finding a complete and integrated used tool line that can be moved from an

existing fab into a new fab is difficult, and these types of opportunities have dried up as the market has tightened, especially for 200mm. Companies looking for a used and complete tool line (either 200mm or 300mm) must consider purchasing a fab operationally and operating it in place for a period of time before the relocation of the tool set could be considered.

Existing loading and supply agreements

Ensuring continuity in manufacturing capacity is of utmost importance, and this is where supply agreements and gradual transitions come into play. The ability for a buyer to neutralize operating costs as they introduce and qualify their own processes is a key component to most operational fab transactions. Here are some recent, real-life examples:

- Acquisition by ON Semiconductor of GLOBALFOUNDRIES' 300mm fab in East Fishkill, NY: transfer of ownership over three years to allow ON to transition from 200mm to 300mm manufacturing (April 2019);
- Acquisition by Diodes Inc. of Texas Instruments' 200mm/150mm fab in Greenock, Scotland, UK: additional fab capacity to support product growth, especially in automotive (February 2019);
- Acquisition by VIS of GF's 200mm Fab 3E in Tampines, Singapore: a way to increase capacity in a global market with limited supply of 200mm manufacturing assets (January 2019); and
- Disposition of Micron's operational back-end facility in Akita, Japan to Powertech Technology, Inc. (PTI) (August 2017).

Local incentives

Advanced manufacturing is slowly coming back to the U.S. because many states offer tax exemptions as well as grants and programs to incentivize companies to build fabs in their state to advance their manufacturing industry and create jobs. A great example is the state of New York, which in September 2019 announced a \$1 billion investment over six years to construct and equip Cree's new greenfield 200mm silicon carbide wafer fabrication facility at the Marcy Nanocenter on the SUNY Polytechnic Institute campus near Utica.



The advertisement features a blue-toned background with a hand pointing at a circular icon containing a stylized circuit board and a double-headed arrow symbol. The text "REGISTER!" and a QR code are overlaid on the icon. The event details "27 - 29 JAN 2020 DRESDEN, GERMANY" are prominently displayed. The SEMI logo is at the top left, and the title "EXPANDING APPLICATION SPACE" is on the right.

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Summary

In today's unstable global context, the selection of a fab site is a crucial part of a sound manufacturing strategy for any advanced technology company. It should therefore be conducted with the utmost care after completing extensive global research to ensure the company's fab specifications are fully met. In addition to the considerations presented in this article, we would like to conclude with these last four tips to ensure a successful fab site selection outcome:

- Gain corporate alignment between managers, executives, and the company board. Agree on a sound product strategy early on to ensure a viable business.
- Depending on your specific manufacturing needs, carefully weigh the pros and cons of greenfield vs. brownfield. Despite large amounts of incentives now available in various parts of the world to attract new fab construction, a sound, existing operational fab may be a better choice for your company in the long run and could ensure faster time-to-market.
- When considering purchasing a second-hand fab, don't get too hung up on the purchase price. Make sure you evaluate the opportunity cost, know all assumed liabilities, and understand all operating expenses. Negotiate a fair supply agreement for both parties to ensure continuity of supply.
- Don't underestimate your fab's local culture. Understand it well to get the most out of your local workforce.

Biography

Stephen Rothrock is Founder, President, and CEO of ATREG, Inc. based in Seattle, WA. Since 2000, he and his team have facilitated about 40% of all global operational wafer fab transactions in the semiconductor industry (front-/back-end, MEMS, solar, display, R&D facilities). Clients include Cypress, Fujitsu, GLOBALFOUNDRIES, IBM, Infineon, Matsushita (Panasonic), Maxim, Micron, NXP, ON Semiconductor, Sony, Qualcomm, Renesas, and TI. Beforehand, Stephen headed Colliers International's Seattle Corporate Services division and was Director for Savills International London. Email: stephen.rothrock@atreg.com

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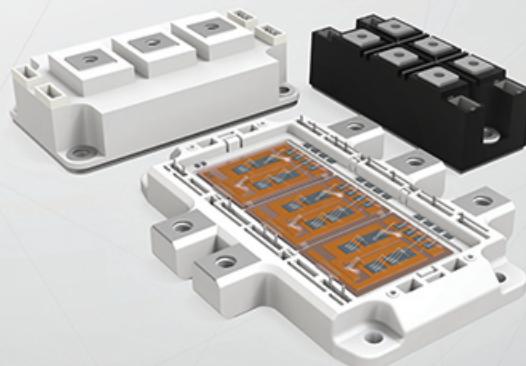
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• Alignment Capability:
+/-12.5um (6 sigma)
• Core Cycle Time: 7secs



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• Oxidation free
• 120°C
• 20-30mins



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