

www.iwlpc.com



10th Annual

International Wafer-Level Packaging Conference & Exhibition

November 5-7, 2013

DoubleTree Hotel, San Jose, CA

IWLPC Conference: November 5-7

IWLPC Exhibit: November 6-7

ORGANIZED BY



SPONSORED BY

PLATINUM SPONSORS



GOLD SPONSORS



SILVER SPONSOR





The International Wafer-Level Packaging Conference has become one of the premier forums focused in three key technology areas: wafer-level packaging, 3D, and MEMS.

Welcome to the 10th Annual International Wafer-Level

The International Wafer-Level Packaging Conference has become one of the premier forums focused in three key technology areas: wafer-level packaging, 3D, and MEMS. The 2013 conference will be held once again in San Jose, California, the heart of Silicon Valley. Four professional development courses will kick start the conference on Tuesday, November 5th. This will be followed by two full days of three technical tracks with two plenary talks and panel discussion on MEMS and 3D. An extensive vendor exhibition will be available. To celebrate the 10th year anniversary of the conference, Paul Wesling, IEEE Fellow and CPMT Distinguished Lecturer, will give the Keynote address on “The Origins of Silicon Valley: Why and How It Happened Here.” IWLPC will be an exciting venue to learn and discuss the latest technology and business trends, and network with colleagues. We hope to see you this November in San Jose.

— Luu Nguyen, Ph.D., TI Fellow, Texas Instruments
Conference General Chair

Technical Committee

Luu Nguyen, Ph.D., Texas Instruments, General Chair
Keith Cooper, SET North America, Technical Chair

3D Track

Peter Ramm, Ph.D., Fraunhofer EMFT, Chair
Laurette Nacamulli, The Dow Chemical Company, Co-Chair
Rozalia Beica, Yole Developpement
Herb Reiter, eda 2 asic Consulting, Inc.
Zhaozhi Li, Ph.D., Intel ATTD
Andy Mackie, Ph.D., Indium Corporation

WLP Track

Steven Xu, Ph.D, Qualcomm, Chair
Curtis Zwenger, Amkor Technology, Co-Chair
Ted Tessier, FlipChip International
Rey Alvarado, Qualcomm
Jianwen Li, Amkor Technology
Gilles Poupon, CEA-LETI Minattec
John Lau, Ph.D., Industrial Technology Research Institute
Janet Love, Rika Denshi America, Inc.
Jiawei Zhang, Broadcom

MEMS Track

Russell Shumway, Amkor Technology, Chair
Roger Grace, Roger Grace Associates, Co-Chair
Andrew Strandjord, Ph.D., PacTech-USA
Maaïke M.V. Taklo, Ph.D., SINTEF ICT

Packaging Conference (IWLPC)!

3D Integration Track

3D integration is recognized as a key technology for heterogeneous products, demanding smart system integration rather than extreme high interconnect densities.

Heterogeneous integration technologies are being developed for functional diversification systems, i.e. integration of CMOS with other devices, such as analog/RF, solid-state lighting, HV power, passives, sensors/actuators, biochips and biomedical devices. This heterogeneous integration started with system-in-packaging technology, and is expected to evolutionally move to 3D heterogeneous integration with TSVs and wafer bonding.

Many R&D activities worldwide are focusing on heterogeneous integration for novel functionalities. Corresponding 3D integration technologies are in evaluation at several companies and research institutions. Furthermore there are significant advances for integrated MEMS systems using 3D integration technologies. The multitude of abstracts submitted to the 2013 IWLPC evidence the vast activities and interest on the subject matter. The 3D sessions intend to bring to you a sample of these advances from processing and technology to TSV and interposers and thermo-compression bonding.

WLP Track

In the quest for smaller size, increased performance, and lower cost, Wafer-Level Packaging (WLP) has become the technology of choice for many semiconductor applications. Fueled by the tremendous growth in the smartphone and tablet markets, WLP has become the fastest growing package type in the entire semiconductor industry. Primarily driven by footprint and thickness reductions for mobile phones, WLP is now used for a wide variety of circuits, such as EMI/ESD protection, power management, wireless connectivity, and emerging MEMS & sensor applications. WLP has traditionally been best suited for small die with low I/O, but advancements in materials and processing have dramatically improved board level reliability. In addition, the emergence of fan-out wafer-level packaging has further widened the application space for wafer-level products. The result is that WLP now competes even more favorably on cost, reliability, and performance in areas once dominated by laminated-based

package technologies. This year's WLP track covers a broad range of topics. Wednesday's sessions focus on the challenges and solutions for wafer-level automation & test, along with recent advancements in wafer-level packaging materials. Thursday's agenda includes innovations in WLP process technologies with a dedicated session on fan-out WLP that covers single die, multi-die, and 2.5D applications.

MEMS Track

The MEMS track will begin with a market analysis study of MEMS packaging diversity and growth expectations. An overview of MEMS package historical trends will be shared as well as future challenges and technologies that lead to wafer-level packaging (WLP). WLP technologies are maturing and ready to shape the fabrication trends of MEMS packaging. Wafer-level bonding has long been applied to hermetically isolate and protect sensitive MEMS transducers from the operating environment for improved performance and reliability. Various emerging wafer bond techniques can additionally provide interconnects between CMOS and MEMS or to external outputs. Product examples of each will be examined that demonstrate an evolution of package configurations from hermetic to substrate carrier to package-less wafer-level packaging (WLP). Finally, MEMS Test strategies will be covered that address cost considerations and a roadmap to address cost pressures of characterization and test.

World-Class Professional Tutorials

On Tuesday, November 5, we will have professional tutorials given by instructors who are the pre-eminent authorities in their fields. Each tutorial represents an outstanding opportunity to meet with your peers in a relaxed atmosphere for an intensive course mentored by an expert.

Tabletop Exhibition

On November 6th and 7th, the IWLPC will present more than 40 exhibiting companies—many of which are the leaders in the semiconductor packaging and test industry. Attendee visitors will be able to see the latest products and discuss a broad range of services in an interactive environment.

The Conference is co-produced by the SMTA, the nation's premier organization for electronics assembly, and *Chip Scale Review*, the leading international publication serving the semiconductor packaging industry.

General chair Luu Nguyen, Ph.D., *Texas Instruments* and technical chair Keith Cooper, *SET North America* as well as the SMTA team and *Chip Scale Review* look forward to seeing you at this year's event!

Tutorials

Tutorial #	Instructor	Day/Time	Topic
T1	Rao Tummala, Ph.D., Georgia Tech	11/5 8:30am-12:00pm	2.5 and 3D Interposer and Package Options: Organic Vs. Silicon Vs. Glass and Wafer Vs. Panel Manufacturing
T2	Luu Nguyen, Ph.D., Texas Instruments Inc.	11/5 8:30am-12:00pm	Wafer-Level-Chip Scale Packaging (WL-CSP)
T3	John H. Lau, Ph.D., Industrial Technology Research Institute (ITRI)	11/5 1:30pm-5:00pm	TSV and Other Key Enabling Technologies for 3D IC Integration
T4	Herb Neuhaus, Ph.D., TechLead Corporation	11/5 1:30pm-5:00pm	Technology Selection: Understanding Cost, IP Landscape, and Infrastructure to Reduce Risk

Tuesday, November 5

8:30am-12:00pm

T1 2.5 and 3D Interposer and Package Options: Organic Vs. Silicon Vs. Glass and Wafer Vs. Panel Manufacturing



Rao Tummala, Ph.D., *Georgia Tech*

Overview

Smart mobile systems are driving unparalleled packaging paradigms in system miniaturization, functionality, and cost. Unlike in the past, with a singular focus on transistor scaling and minimal and incremental advances in the packaging of devices and systems, the new focus needs to

be on total system scaling, system integration and system cost. A new system integration platform is necessary driving lithographic ground rules and pitch to 50µm in the short term and 25-10µm in the long term. The packaging materials for these innovative systems can be organic, ceramic, metal, single crystal silicon, poly-silicon or glass. The packaging architectures can be with TSV, such as 3D ICs, but they can also be without TSV, such as 2.5D, 3D and 3.5 D Interposers and packages. This course reviews a variety of options for packaging and manufacturing platforms.

Organic Packages can be extended by overcoming four of their main limitations: lithographic ground rules leading to small pitch due to poor dimensional stability, poor thermal performance due to low thermal conductivity, low reliability due to the large mismatch in TCE and moisture uptake, and, most importantly, warpage due to low elastic modulus during substrate fabrication and chip and board-level assembly due to high temperature processes which lead to both elastic, below glass transition, and viscos-elastic, above glass transition temperatures. The key question is whether the new class of low TCE and high Tg organic packages can be extended to provide I/O pitch to 25µm in 2.5D and 3D configurations. Silicon Packages address all four of these fundamental limitations. Silicon is the best known material in the electronics industry, but, it has two major shortcomings; its electrical loss is too high and it is available only up to 300 mm in wafer size, making it costly for packaging applications. Glass: Glass is the most well-known material in the display industry. It is available, for the first time, in ultra-thin and roll-to-roll sizes without having to grind and polish. The new availability and production methods, combined with its superb electrical properties, such as its low dielectric constant and its ultra-low loss, make it an ideal candidate for future smart systems packaging. Recent progress by the Georgia Tech's consortium has addressed most of the technology concerns encountered in developing these systems.

Who Should Attend?

Technology developers and end users at device and systems, at all levels including executive decision makers, marketing and strategic planning managers.

T2 Wafer-Level-Chip Scale Packaging (WL-CSP)



Luu Nguyen, Ph.D., *Texas Instruments Inc.*

Overview

Wafer-Level-Chip Scale Packaging (WL-CSP) has gained much success as a packaging form factor in the consumer arena in the past few years that it is almost considered as a "technology commodity." It has been driven by needs for cost reduction, size shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The standard configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability.

Outline

1. Wafer-Level-Chip Scale Packaging (WL-CSP) definition
2. Market drivers for WL-CSPs — portable and wearable
3. Cost and benefits of WL-CSPs
4. Barriers and challenges for WL-CSPs
5. Review of current WL-CSPs in the industry (Bump on Pad, Bump on Polymer, Redistribution with Al and Cu, Fan-out configurations)
6. Wafer-level testing — status and challenges
7. Infrastructure service providers — bumping, turnkey solutions, market shares
8. Extension of WL-CSP concept to other applications (medical, automotive, space, sensors, imaging, MEMS, LEDs)
9. Case studies of WL-CSPs (structures, processing, reliability: thermal cycling, flex, drop, electromigration)
10. Future trends: enhanced lead-free solder balls, large die size, wafer-level underfill, thin and ultra thin WL-CSP, stacked WL-CSP, MCM in "reconstituted wafers", embedded components, etc.)

Who Should Attend?

The course will be useful to the following three groups of engineers and scientists: newcomers to the field who would like to obtain a general overview, R&D practitioners who would like to learn new methods for solving CSP problems, and those considering WL-CSP as an alternative for their interconnect systems.

Lastly, those considering WL-CSP as an alternative for their interconnect systems.

Tuesday, November 5

1:30pm– 5:00pm

T3 TSV and Other Key Enabling Technologies for 3D IC Integration



John H. Lau, Ph.D., *Industrial Technology Research Institute (ITRI)*

Overview

3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration, which will be discussed in this workshop. Emphases are placed on the key enabling technologies for 3D IC integrations, such as TSV (through-silicon via) forming and filling, front and back-side metallization, RDL (redistribution layer), temporary wafer bonding, wafer thinning and handling, wafer de-bonding, thin chip/wafer strength measurement and improving, lost-cost lead-free microbumping ($\leq 15\mu\text{m}$ pitch) and assembly, C2C, C2W, and W2W bonding, and thermal management. Useful characterization and reliability data for 3D IC integration will also be provided. The application of 3D IC integration such as MEMS, LED, logic + logic, memory + microprocessor, wide I/O DRAM, active and passive interposers will be presented. Furthermore, the critical issues of TSV and 3D IC integration will be given and some potential solutions or research topics will be recommended. Finally, the supply chains for high volume manufacturing of 3D IC integration will be discussed and several roadmaps of 3D IC integration will be provided. All the materials are based on the technical papers and books published within the past 3 years by the lecturer and others.

Who Should Attend?

If you (students, engineers, and managers) are involved with any aspect of the electronics, LED, MEMS, and optoelectronic industry, you should attend this course. It is equally suited for R&D professionals and scientists. You will receive more than 300 pages of handouts from the Instructor's books, *"Advanced MEMS Packaging"* (McGraw-Hill, 2010), *"Reliability of RoHS Compliant 2D & 3D IC Interconnects"* (McGraw-Hill, 2011), and *"TSV for 3D Integration"* (McGraw-Hill, 2012).

T4 Technology Selection: Understanding Cost, IP Landscape, and Infrastructure to Reduce Risk



Herb Neuhaus, Ph.D., *TechLead Corporation*

Overview

This half-day course provides a systematic and quantitative methodology to strategically select technologies. Using case studies drawn from MEMS assembly, 3D integration, and wafer-level packaging, the course first teaches the principles and application of yielded cost modeling which enables calculation of accurate manufacturing costs and yields for current capabilities as well as new and emerging technical alternatives. Next the course teaches how to assess the intellectual property landscape to find competitors' IP strengths, exploitable gaps and to evaluate IP synergy among new technologies and a current portfolio. The course then turns to infrastructure and supply chain challenges. What new skills, equipment, and partnerships will enable successful implementation of a new technology? Finally, the course pulls together these seemingly disparate analyses into a coherent, quantitative score card that supports informed and unbiased strategic decisions.

Who Should Attend?

This course covers basic and advanced topics for R&D, product and design engineers; manufacturing, process and assembly/packaging engineers; engineering and operations managers; manufacturing planning and senior design technicians; as well as consultants and academic specialists. Marketing and sales personnel requiring an understanding of the impact of technology choices on manufacturability also benefit from understanding strategic technology selection.

What People Are Saying About IWLPC!

We have participated in the IWLPC for the last two years and have found that the technical presentations have been very enlightening. IMT, being a MEMS foundry, utilizes wafer-level packaging in over 70% of the products that we produce and would not miss this important conference. We also found the exhibit hall experience very valuable.

— Michael Shillinger, *Founder, Innovative Micro Technology (IMT), 2012 IWLPC Best of Conference Award*

IWLPC brings visitors from around the world to a focused event that allows exchange of new developments and ideas.

— E. Jan Vardaman, *President, TechSearch International, Inc.*

The International Wafer-Level Packaging Conference has consistently been an excellent venue for both its technical presentations and vendor exhibits. We have been attending the IWLPC for the last seven years and found it to be very valuable for both our people and company.

— Robert Marshall, *RMM*

IWLPC is the premier conference for emerging packaging technologies from the chip scale to the wafer scale. The conference brings together vendors, users and decision makers and is extremely valuable to EV Group.

— Garrett Oakes, *Technology Director, EV Group*

Special Events

Wednesday Events

November 6th



Keynote Breakfast Address

Free to all conference and exhibit attendees!

The Origins of Silicon Valley: Why and How It Happened Here

Paul Wesling, *CPMT Society Distinguished Lecturer*

9:00am–10:00am, Oak Ballroom

Abstract

Why did **Silicon Valley** come into being? The story goes back to local Hams (amateur radio operators) trying to break RCA's tube patents, the sinking of the Titanic, Naval ship communications requirements, Fred Terman and Stanford University, local invention of high-power tubes (gammatron, klystron), WW II and radar, William Shockley's mother living in Palo Alto, Hetch Hetchy water, and the SF Bay Area infrastructure that developed — these factors pretty much determined that the semiconductor and IC industries would be located in the Santa Clara Valley. Since semiconductor device development and production were centered here, it made sense that Charles (Bud) Eldon of H-P would be asked by his management to start an IRE Group on Product Engineering in Palo Alto, to serve local engineers (which grew into today's CPMT Society). Bud went on to become one of IEEE's presidents.

Paul Wesling, a CPMT Society Distinguished Lecturer, will give an exciting and colorful history of device technology development and innovation that began in San Francisco and Palo Alto, moved down the Peninsula (seeking lower costs and better housing), and ended up in the Santa Clara Valley during and following World War II. You'll meet some of the colorful characters — Lee DeForest, Bill Eitel, Charles Litton, Fred Terman, David Packard, Bill Hewlett and others — who came to define the worldwide electronics industries through their inventions and process development.

10th Anniversary Celebration

Hotel Restaurant—Club Maxx

5:30pm–7:00pm

Hosted by Applied Materials



On behalf of the Technical Committee, SMTA & *Chip Scale Review*, we welcome everyone to the 10th Anniversary of IWLPC! Come celebrate with the speakers, conference attendees and exhibitors at the 10th Anniversary Reception. Thanks to Applied Materials for their support in sponsoring this event. Applied Materials is also a Silver Sponsor. Please plan to visit their booth in the exhibit hall. The 10th Anniversary Reception is free with every registered technical conference pass and one per exhibit booth. Additional tickets will be for sale on-site. Tickets are limited!



Plenary — Metal Based MEMS Offer New Growth Opportunities

William G. Hawkins, *General Electric Global Research Center*

1:30pm–3:00pm, Oak Ballroom

Abstract

Metal based MEMS have already had commercial success, the most notable example being Digital Micromirror Arrays. However, the volume of metal based MEMS remains modest in comparison with more traditional low stress poly, silicon on insulator, and “epi-poly” MEMS. This presentation will

highlight the successful implementation of a new class of metal alloy MEMS, and will then discuss some features of metal alloy MEMS that enable the technology to satisfy new applications that are not yet addressed with silicon based MEMS technology.

GE's development of metal MEMS based technology will be described in the context of the microswitch application. Over an eight year period, high performance microswitches have been developed based on two different pattern electroplated metal alloys. Metal MEMS switches that are capable of switching 240 volts AC and ~10 Amps of current in a single compact chip have been demonstrated and will be discussed. These metal switches can also be fabricated on fused silica substrates, and thereby provide superior RF switching performance. The RF performance achieved will also be presented. These two microswitch examples will be used to highlight the performance advantages that have been achieved with MEMS that are fabricated from optimized plated metal alloys.

Thursday Events

November 7th



Plenary — A Consumer Driven Market — This Changes Everything

Simon McElrea, M.Eng., *Invensas Corporation*

9:00am–10:00am, Oak Ballroom

Abstract

With the dawning of “Generation Mobile” comes a whole new landscape in microelectronics manufacturing. Consumers are more educated about what makes their mobile devices tick and are in the driver's seat for what they want to see next in terms of functionality. What's more, these devices are no longer viewed as luxury items, but rather as necessities for daily living. Then add advancements in interconnect technologies for logic, memory, sensors and more, which have the ability to make every technogeek's dream a reality. So what is the fly in the ointment? Cost of manufacturing and time to market. The traditional semiconductor manufacturing model is antiquated, stuck in the PC era, and can't keep pace with savvy consumer demand. This talk will address these issues and offer insight into what might be needed to inspire change in the ecosystem and infrastructure.

Panel Discussion 3D High Volume Manufacturing — Are We There Yet?

1:30pm–3:00pm, Oak Ballroom

Hosted by Invensas Corporation



When is a product or a technology deemed to be in HVM? It has been several years since the first stacked memory (Flash, DRAM) products were announced. Since then, various parts of the industry's supply chain have steadily geared up for 3D products. This panel will examine the factors that signal the transition of a technology into High Volume Manufacturing and how close we are to achieving it in 3D.

Moderator: Sitaram Arkalgud, Ph.D., *Invensas Corporation*

Panelists:

Laura Rothman Mauer, *Solid State Equipment LLC*.

Jim Walker, *Gartner Technology*

Abe Yee, *NVIDIA Corporation*

Additional panelists to be announced



2013 Exhibition November 6 & 7

In conjunction with the IWLPC Conference

Top 4 Reasons Your Company Should Exhibit at IWLPC!

1. Reach a focused international audience
2. Generate exposure in this highly competitive marketplace
3. Share new products and concepts to the market
4. Enhance relationships with existing customers and generate new leads

DoubleTree Hotel, San Jose, CA

November 6: 10:00am - 5:30pm

November 7: 10:00am - 1:30pm

Included in the cost to exhibit:

- NEW in 2013! Pipe and Draped Booths (8'x10' and 8'x8' Sizes Available)
- Basic booth furnishings: one 6ft standard table, chair, and wastebasket
- Lunch and Coffee Breaks Daily
- One 10th Year Anniversary Ticket
- Attendee List
- Show Directory Listing
- Company Sign
- IWLPC Proceedings on USB Drive
- One Technical Conference Pass (a \$700 value)

Cost: \$1,250 per booth plus \$50 extra for electricity in booth.

...Don't miss your chance to exhibit, each year sells out early!

Attend the Exhibition for FREE!

- Help start off the 10th Year of IWLPC on November 6th by joining us at the Keynote Breakfast for FREE.
- Enjoy FREE refreshments and one-on-one networking with industry's premier supply companies.
- You don't need a conference pass to attend the exhibition, register online today!

November 6 & 7 we will be raffling off door prizes.

Don't be the one to miss out! Take your boss or colleague out for a FREE Lunch.

For more information please contact

CSR Sales Representative at info@chipscalereview.com |
408.429.8585 or Patti Hvidhyld at Patti@smta.org | 952.920.7682



2013 IWLPC Exhibitors

List of exhibitors as of July 1st.

AGC
AI Technology, Inc.
Amkor Technology
Applied Materials
Axus Technology
Boschman
Technologies / APC
Chip Scale Review
cyberTECHNOLOGIES
Deca Technologies
EV Group, Inc.
Hesse Mechatronics, Inc.
Invensas Corporation
J-Devices Corporation
LB Semicon
NAMICS
NANIUM
New Venture Research
Corporation
Newport Corporation
Owens Design, Inc.
Pac Tech USA
Promex Industries
SET North America
Silex Microsystems AB
Smiths Connectors — IDI
Sonoscan, Inc.
STATS ChipPAC Ltd.
Suss MicroTec, Inc.
TechSearch
International, Inc.
Teramikros, Inc.
Unisem Group

Sessions at a Glance: Wednesday, November 6th

8:50am – 9:00am

Opening Comments, Oak Ballroom
Luu Nguyen, Ph.D., *Texas Instruments, Conference General Chair*

9:00am – 10:00am

Keynote Breakfast — The Origins of Silicon Valley: Why and How It Happened Here, Oak Ballroom
Paul Wesling, *CPMT Society Distinguished Lecturer*

10:00am – 10:45am

Exhibits Open, Exhibit Hall, Bayshore Foyer

WLP TRACK

10:45am – 12:15pm

SESSION 1 — WAFER-LEVEL

AUTOMATION & TEST, Monterey
Chair: Janet Love, *Rika Denshi America Inc.*
Co-Chair: Ted Tessier, *Flip Chip Technology*

3D TRACK

10:45am – 12:15pm

SESSION 2 — THERMO-COMPRESSSION BONDING

FOR 3D PACKAGING, San Carlos
Chair: George Li, Ph.D., *Intel Corporation*
Co-Chair: Jiawei Zhang, *Broadcom*

MEMS TRACK

10:45am – 12:15pm

SESSION 3 — WAFER-LEVEL

PACKAGED MEMS, Santa Clara
Chair: Roger Grace, *Roger Grace Associates*
Co-Chair: Luu Nguyen, Ph.D., *Texas Instruments*

10:45 **Overcoming Productivity Challenges in Wafer-Level Packaging**
Shekar Krishnaswamy, *Applied Materials*

A Process Level Comparative Analysis Between D2W Local and Collective 3D Bonding
Robert Daily, *imec*

MEMS Packaging: What Makes It So Special?
Eric Mounier, *Yole Développement*

11:15 **Automating the Design and Layout of Wafer-Level Masks**
Steve DiBartolomeo, *Artwork Conversion Software*

Thin Die Interconnect Process for 3DIC Utilizing Multiple Layers of 50 micron Thick Die on 300mm Wafers with a Tack and Collective Bonding Approach for Manufacturability
Daniel Pascual, *CNSE*

30 Years of Microsystem Packaging: From Automotive to Mobile Electronics and Beyond
Leland "Chip" Spangler, Ph.D., *Aspen Microsystems*

11:45 **Spring Contact Probes in Wafer Test Applications — Structure, Characterization, and Test Method**
Jon Diller, *Interconnect Devices, Inc.*

Exploring Process Interaction of No-Flow Underfill and Thermo-Compression Bonding in D2D Stacking
Giovanni Capuz, *imec*

Packaging for Ultra-Miniature/Low-Cost MEMS Accelerometers
Yang Zhao, Ph.D., *MEMSIC Inc.*

12:15pm – 1:45pm

Lunch, Exhibit Hall, Bayshore Ballroom

WLP TRACK

1:45pm – 3:45pm

SESSION 4 – WAFER-LEVEL

MATERIALS, Monterey
Chair: Steven Xu, Ph.D., *Qualcomm*
Co-Chair: Janet Love, *Rika Denshi America Inc.*

3D TRACK

1:45pm – 3:45pm

SESSION 5 — 3D PROCESSING AND

TECHNOLOGY, San Carlos
Chair: Peter Ramm, Ph.D., *Fraunhofer EMFT*
Co-Chair: Rozalia Beica, *Yole Développement*

MEMS TRACK

1:45pm – 3:45pm

SESSION 6 – WAFER BONDING AND

TESTING FOR MEMS, Santa Clara
Chair: Russell Shumway, *Amkor Technology*
Co-Chair: Ron Molnar, *AZ Tech Direct, LLC.*

1:45 **Single Wafer Resist Removal for Packaging with Improved Process Integration**
Richards Peters, Ph.D., *Dynaloy*

Multi-Die Embedded Polyimide-Based Wiring Board in Stacked Configuration
Koji Manukata, *Fujikura Ltd.*

Advanced Metal-Eutectic Bonding for High Volume MEMS WLP
Sumant Sood, *SUSS MicroTec*

2:15 **Modeling the Imidization Kinetics in Solid State of a Low Temperature Cure Photosensitive PMDA/ODA Polyimide**
Frank Windrich, *Fraunhofer IZM-ASSID*

An Investigation on the Effect of Upstream Processes on the Quality of Cu-Cu Bonding Interconnect Under Controlled Manufacturing Environment
Anh Nguyen, Ph.D., *University of New York at Albany*

Multiple Wafer MEMS WLP
Mike Shillinger, P.E., *Innovative Micro Technology, 2012 IWLP Best of Conference Award*

2:45 **Electroplated Lead-Free Solder for Reliable Flip-Chip Interconnection**
Yi Qin, *Dow Chemical Company*

Interconnect Structure for Room Temperature 3D-IC Stacking Employing Binary Alloying for High Temperature Stability
Eric Schulte, *SET North America*

Examination of Key Packaging Metrics of a Hermetically Sealed MEMS Accelerometer
Joshua Krabbe, *Micralyne*

3:15 **Study of the Electroless Plating Process for Special Materials or Small Pads for UBM Formation**
Donald Gudecuskas, *Uyemura International Corporation*

Temporary Bonding Material Total Thickness Variation
Aaron Jacobs, *Brewer Science, Inc.*

Minimizing Cost of Calibration and Test (COCT) to Drive Cost Reduction of MEMS
Klaus Ruhmer, *Multitest Electronic Systems, Inc.*

3:45pm – 4:30pm

Coffee Break, Exhibit Hall, Bayshore Ballroom

4:30pm – 5:30pm

MEMS PLENARY — Metal Based MEMS Offer New Growth Opportunities, Oak Ballroom
William G. Hawkins, *MEMS Process Development Laboratory, General Electric Global Research Center*

5:30pm – 7:00pm

IWLPC 10th Anniversary Celebration — Hosted by Applied Materials
Hotel Restaurant — *Club Maxx, (Ticket required)*

Sessions at a Glance: Thursday, November 7th

9:00am – 10:00am

3D PLENARY — A Consumer Driven Market — This Changes Everything, Oak Ballroom
Simon McElrea, M.Eng., *Invensas Corporation*

10:00am – 10:45am

Coffee Break, Exhibit Hall, Bayshore Ballroom

WLP TRACK

10:45am – 12:15pm

SESSION 7 — WAFER-LEVEL PROCESS, Monterey
Chair: Yi Qin, *Dow Chemical Company*
Co-Chair: Jianwen Li, *Amkor Technology*

3D TRACK

10:45am – 12:15pm

SESSION 8 — INTERPOSERS, San Carlos
Chair: Andy Mackie, Ph.D., *Indium Corporation*
Co-Chair: Gilles Poupon, *CEA LETI*

3D TRACK

10:45am – 12:15pm

SESSION 9 — 3D METROLOGY AND TEST, Santa Clara
Chair: Laurette Nacamulli, *Dow Chemical Company*
Co-Chair: Robert Daily, *imec*

10:45 The Role of Extreme Agitation in Accelerating Removal Rate of Advanced Packaging Photoresist
Mani Sobhian, *TEL NEXX*

Some Trends in the Field of Interposers
Andre Rouzaud, Ph.D., *CEA-Léti*

Quality in 3D Assembly — Is KGD Good Enough?
James Quinn, *Multitest*

11:15 Solder Jetting and Gang Ball Load Technologies Utilizing 30µm Diameter Solder Spheres for Fine Pitch Micro Ball Bumping of WLCSPS
Richard McKee, *Pac Tech- USA*

Novel Cheap Solutions for 3D Integration on Wafers with Thin Interposers
Semyon Savransky, Ph.D., *The TRIZ Experts*

Inspection and Metrology Solutions For Cu Pillar HVM
Rajiv Roy, *Rudolph Technologies*

11:45 Advances in 300mm WLCSP Spheron™ Cu Platted RDL Technology for Higher Density and Lower Cost Packaging
Andre Cardoso, *Nanium S.A.*

2.5D and 3D Packaging Platform for Next Generation RF and Digital Modules Using Through Glass via (TGV) Technology
Sergio Cardona, *nMode Solutions, Inc.*

3D Packaging Metrology using Virtual Interface Technology
Arun Aiyer, *Frontier Semiconductor*

12:15pm – 1:30pm

Lunch, Exhibit Hall, Bayshore Ballroom

1:30pm

Exhibit Hall Closes

1:30pm – 3:00pm

3D PANEL DISCUSSION — HOSTED BY INVENSAS: 3D High Volume Manufacturing — Are We There Yet?, Oak Ballroom
Moderator: Sitaram Arkalgud, *Invensas Corporation*
Panelists: Laura Rothman Mauer, *Solid State Equipment LLC*; Jim Walker, *Gartner Technology*; Abe Yee, *NVIDIA Corporation*

3:00pm – 3:30pm

Coffee Break, Bayshore Foyer

WLP TRACK

3:30pm – 5:00pm

SESSION 10 — FAN-OUT WAFER-LEVEL PACKAGING TECHNOLOGIES, Monterey
Chair: Rey Alvarado, *Qualcomm*
Co-Chair: Andrew Strandjord, Ph.D., *Pac Tech USA*

3D TRACK

3:30pm – 5:00pm

SESSION 11 — TSV PROCESSING AND IMPLEMENTATION, San Carlos
Chair: Rozalia Beica, *Yole Développement*
Co-Chair: Peter Ramm, Ph.D., *Fraunhofer EMFT*

3D TRACK

3:30pm – 5:00pm

SESSION 12 — 3D PROCESSING, Santa Clara
Chair: Jan Vardaman, *TechSearch International*
Co-Chair: Aaron Jacobs, *Brewer Science*

3:30 Implementation of a Fully Molded Fan-Out Packaging Technology
William Rogers, Ph.D., *DECA Technologies*

TSV Resist and Etch Residue Removal for 3DIC
Kim Pollard, Ph.D., *Dynaloy*

Semiconductor Grade Fluxes for 2.5D and 3D Assembly
Andy Mackie, Ph.D., *Indium Corporation*

4:00 Cost Comparison of Multi-Die Fan-Out Wafer-Level Packaging and 2.5D Packaging with a Silicon Interposer
Chet Palesko, *SavanSys Solutions LLC*

TSV Process Optimization by Monitoring and Controlling Unwanted Impurities and Particles in Cu Interconnect Plating Baths
Fuhe Li, *Air Liquide - Balazs NanoAnalysis*

Low Warpage and Improved 2.5D/3DIC Process Compatibility with High Stability Commercial Polyimide Dielectrics
Robert Hubbard, Ph.D., *Lambda Technologies*

4:30 Choosing Lithography Equipment to Minimize the Cost of Wafer-Level Packaging
Tim McCrone, *SUSS MicroTec*

Recent Results Using Met-Via® TSV Interposer Technology as TMV Element in Wafer-Level Through Mold Via Packaging of CMOS Biosensors
Toby Ebefors, Ph.D., *SILEX Microsystems AB*

Microbump Lithography for 3D Stacking Applications
Warren Flack, *Ultratech Inc.*

Registration Info & Pricing

Technical Conference Package

Your \$600 conference fee includes: Breakfast Keynote, 10th Anniversary Celebration ticket, all technical sessions, two lunches, proceedings on USB drive and exhibits. Register early to receive the discounted pricing. *The conference fee will increase \$100 after October 4th.*

Single Day Registration

Your \$325 fee includes Keynote Breakfast and all sessions of your choice of Wednesday, November 6th or Thursday, November 7th, lunch, exhibits and proceedings. The 10th Anniversary Celebration is not included. *The single day registration fee will increase \$100 after October 4th.*

Tutorials

Tutorials conducted by several of the most respected individuals in their fields. The Tutorial fee of \$250 includes one half-day workshop, handout materials and refreshments during breaks.

Proceedings

Proceedings are free with one- or two-day registrations. The cost for additional copies is \$125 at the Conference or \$150 by mail from the SMTA.

Send Four, Pay for Three!

Your company can save over \$600 by sending four attendees to the IWLPC. All registrants must be from the same company and must register at the same time. Sorry, these rates are not available online. Contact Patti Hvidhyld at 952-920-7682 and save, save, save!

Cancellations

If for any reason you should need to cancel a registration, there will be a \$75 processing fee if received by October 4th. All requests must be in writing.

Early Bird Discount

The full conference and single day registration fees will increase by \$100 after October 4th. Register early to take advantage of the discount. Sorry, this discount may not be combined with the student discount.

Special Discounted Student Rates

The IWLPC offers special rates to full-time students. These rates are not available via web registration. Contact Patti Hvidhyld at 952-920-7682 for details.

Discounted Hotel Rates

The IWLPC has made arrangements with our host hotel, the DoubleTree, San Jose to reserve a block of rooms for Conference attendees at a special rate of only \$189/night. Reservations must be made by October 7th. Please reference the SMTA IWLPC to receive these rates. The hotel's phone number is 1-408-453-4000.

Visit
www.iwlpc.com
to Register Today!



Thank You to Our Supporters



10th Annual

International Wafer-Level Packaging Conference & Exhibition

November 5-7, 2013

DoubleTree Hotel, San Jose, CA

IWLPC Conference: November 5-7

IWLPC Exhibit: November 6-7

INTERESTED IN EXHIBITING? Visit www.iwlpc.com and click on Exhibitor Info Tab or contact CSR Sales Representative at info@chipscaleview.com, 408-429-8585 or Patti Hvidhyld at 952-920-7682, patti@smta.org for more information.

☐ Dr. ☐ Mr. ☐ Ms. Name _____
Job Title _____
Company _____ MS _____
Address _____
City _____ State/Province _____ Zip _____
Country _____
Phone _____ Fax _____
Email _____

How to Register



Online at
www.iwlpc.com



By fax with
credit card
952-926-1819



By phone with
credit card
952-920-7682



By mail with payment to:
IWLPC/SMTA
5200 Willson Road, Suite 215
Edina, MN 55424-1316

Register me for

Conference and tutorial fees will increase by \$100 after October 4th.

- ☐ Tabletop Exhibition AttendeeFree
☐ Technical Conference Package*\$600
☐ Technical Conference Speaker Rate*\$300
☐ Technical Conference, Wednesday Only\$325
☐ Technical Conference, Thursday Only\$325
☐ T1: 2.5 and 3D Interposer and Package Options: Organic Vs. Silicon Vs. Glass and Wafer
Vs. Panel Manufacturing\$250
☐ T2: Wafer-Level-Chip Scale Packaging (WL-CSP)\$250
☐ T3: TSV and Other Key Enabling Technologies for 3D IC Integration\$250
☐ T4: Technology Selection: Understanding Cost, IP Landscape, and
Infrastructure to Reduce Risk\$250
☐ Conference Proceedings on a USB drive (Sponsored by Indium Corporation)\$125 on-site/\$150 mail
☐ Student Rate (Must contact SMTA to verify).\$25

TOTAL \$ _____

☐ Check enclosed (\$USD) – OR – ☐ MC ☐ VISA ☐ AMEX

Credit Card Number _____ Exp. _____

Cardholder's Name _____ Sec. Code _____

* 10th Anniversary Celebration Ticket is included in technical conference package and speaker registration fee.



c/o SMTA
5200 Willson Road
Suite 215
Edina, MN 55424-1316



Scan with a mobile
QR application for
more information.

PRESORTED
STANDARD
US POSTAGE PAID
TWIN CITIES, MN
PERMIT NO. 28788

10th Annual International Wafer-Level Packaging Conference & Exhibition

November 5-7, 2013 DoubleTree Hotel, San Jose, CA

IWLPC Conference: November 5-7 IWLPC Exhibit: November 6-7



ORGANIZED BY



SPONSORED BY PLATINUM SPONSORS



GOLD SPONSORS



SILVER SPONSOR

