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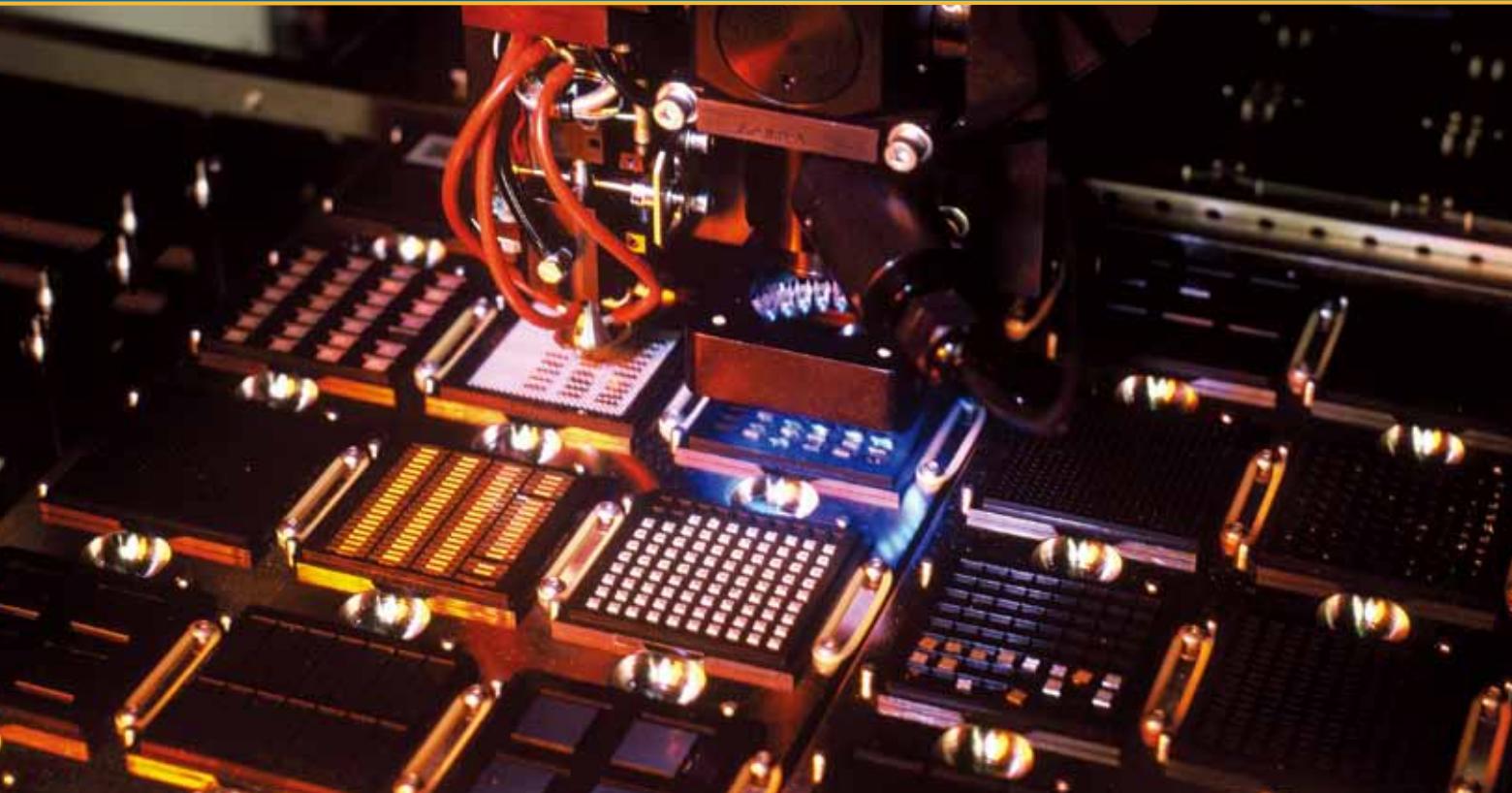
Volume 16, Number 1

January February 2012



- Wafer Cleaning
- Copper Wire Bond
- LED Packaging Trends
- Temporary Bonding/Debonding
- International Directory of Test & Burn-in Socket Suppliers





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The front cover depicts this issue's tribute to the burn-in and test sockets industry. The updated International Directory of Burn-in & Test Socket Suppliers has been published once again to keep the industry current. Supplementing the tribute is an article by Wells-CTI's very own James Forster, Ph.D. entitled "Burn-in Sockets for CSPs: An Update on Challenges" Cover artwork designed by Steve Virga Design.

Chip Scale REVIEW™

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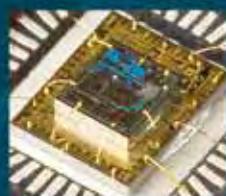
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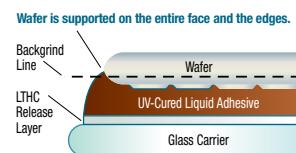
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FROM THE PUBLISHER



Reading CSR's Technology Tea Leaves for 2012

2

012 brings yet another year to all of us, and once again the industry is bouncing back after a challenging 2011. Whether you are an industry newcomer or a seasoned veteran, we welcome a fresh optimistic outlook as perceived by semiconductor industry analysts at large, both domestically and abroad. The sovereign debt and economic worries of the European Union has brought a torrent of dreadful news, yet the industrial indicators within technology and specifically the semiconductor segment reflect increasing stability and projected growth during the coming year. Additionally, forecasts and viewpoints from the EU indicate that increasing capital expenditures on equipment and materials are in focus for the coming year to support demanding cost controls.

As you read this issue, you will find leading edge articles including valuable insight from renowned experts like Georgia Tech's Dr. Rao Tummala, in the "The Future of Packaging"; a Guest Editorial on the INSITE program at imec, as well as Market and Business Trends from Yole Developpement and Quik-Pak. The articles from the authors of ASM Pacific, Fairchild Semiconductor, Suss MicroTec, Kyzen, Nexx Systems bring the latest and greatest in their arenas. Last but not least, James Forster of Wells-CTI brings relevancy and content with his article entitled "Burn-in Sockets for CSP's: An Update on Challenges". CSR's annual 2012 "International Test & Burn-in Socket Suppliers Directory" provides a comprehensive guide for vendor sourcing and product selection.

In addition to co-sponsoring the 10th annual "International Wafer-Level Packaging Conference (IWLPC)" with the Surface Mount Technology Association (SMTA), CSR is also the Official Media Sponsor for the 13th annual BiTS Workshop coming up in March that will bring the burn-in and test community together for "What's Now & Next". David Barnum from Sensata Technologies sums up his side of this business. "The Burn-in socket business is one of the most dynamic segments of the interconnection industry, but it is not for the faint of heart. Continuous changes, updates, and adaptations to different customer requirements, which evolve, as each program evolves, makes for very interesting negotiations and balancing amongst all stakeholders involved." Once again CSR is proud to be designated as the Official Media Sponsor for the 62nd Electronic Components and Technology Conference (ECTC) in 2012.

We here at Chip Scale Review strive to deliver issue-by-issue the highest value-added content and we couldn't achieve that without the support of the authors who contribute timely articles to share their expertise. To the new and loyal supporting advertisers, we couldn't do this without your crucial ongoing support! A huge thank you to each and every advertiser in Chip Scale Review – That is what makes CSR the standard of the semiconductor packaging industry. We optimistically look forward to a very dynamic 2012 – CSR will be there with you and for you.

Kim Newman

Publisher



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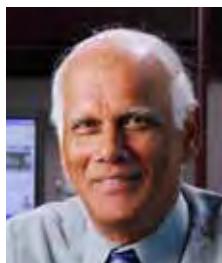
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GUEST EDITORIAL



The Future of Packaging

By Rao R. Tummala, [Georgia Institute of Technology]

The new era of micro- and nano-electronic systems requires that we define and divide packaging into three distinctly different categories: 1) **Semiconductor packaging** of individual devices; 2) package integration of multiple devices by **2D and 3D packaging** that cannot be integrated into monolithic devices; and 3) packaging beyond these devices to form highly-functional and miniaturized systems through **systems packaging**.

Semiconductor packaging was defined in the 1980s as interconnecting, powering, cooling and protecting of active devices.¹ Back then, the focus was primarily on devices, since device scaling and transistor integration was supposed to have led to system-on-chip (SOC). Today however, that is not the primary focus because many of the devices such as RF, Optical, Power and MEMS cannot be integrated into CMOS-based mainstream device technology. Packaging, therefore, must address this integration need. This leads to 2D and 3D packaging.

2D and 3D packaging interconnects two or more similar or diverse set of devices that cannot be integrated cost effectively into single large SOC chips. This trend started in the 1980s when high-performance computing systems required more than 100 similar devices to form a single processor. This led to 2D multi-chip packaging with 100 or more chips interconnected onto single ceramic or thin-film-on-ceramic substrates with lithographic ground rules ranging from 90 μ m in thick films to 6 μ m in thin films. However, systems are more than just devices. Devices comprise approximately 20% of a system in volume and cost. The remaining 80% of the

system includes passives, thermal structures, batteries, and requires interconnection of all these. Thus, this is defined as **systems packaging**.

As shown in **Figure 1**, the most dominant packaging technology practiced to date has been the single-chip package; the trend for which is shown in **Figure 2** starting with lead frame or plastic packaging in the 1970s and moving on to silicon and glass packages in the near future. But its value-add to semiconductor companies at this packaging level is minimal, since packaging at a single-chip level adds no benefit either in performance, cost or reliability.

Some device companies often say that the best packaging is no packaging at all. Why then does the industry practice such a no value-add technology? It is due to two reasons: to electrically-test the die to guarantee its 100% goodness; and to interconnect the die to other components on the system board using surface mount technology (SMT). Packaging at this level can cost more than the device it packages since it involves the package substrate, interconnection, underfill between the substrate and the die as well as thermal structures. As shown in Figure 1, the value-add at this level is very low. For this reason, packaging in the past has been viewed as a necessary evil and single-chip package technology advances have been very cost sensitive and thus are limited.

2D and 3D packaging is entirely different. It adds value in performance, cost, and reliability. It allows for advancements in new technologies. Its practice, however, is limited to 2D in high-performance systems since the 1980s, and 3D systems-

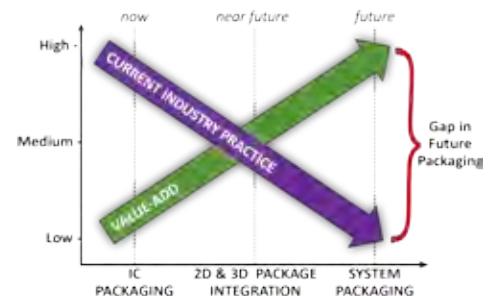


Figure 1: Current industry practice vs. value-add by three packaging types showing the packaging gap to be addressed in future.

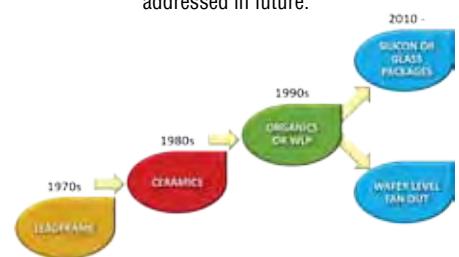


Figure 2: Single-chip packaging since 1970s is the most dominant but adds little value to packaging.

in-package (SIPs), package-on-package (POP) and more recently to 3D ICs and 3D interposers. Such approaches dramatically change the packaging landscape in many ways. For example, with traditional single-chip semiconductor manufacturing, packaging comes as an after-thought. But in 2D, device and package are co-designed and co-developed so as to bring synergy between the two in performance, cost, and reliability. The 3D ICs with TSV go a step further, into something never seen before; they are co-manufactured in the wafer fab even before the back-end-of-the-line (BEOL) I/Os are formed and thus add value to the semiconductor companies. While the practice of this technology shown in Figure 1 is low now, it is expected to grow dramatically.

The end goal of any packaging is systems created through **systems packaging**. The value-add is highest but the current practice is lowest. This



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focus is the next revolution in systems. Since SOC cannot be the basis of this, it is not clear who will drive this next major systems packaging paradigm. It is clear, however, that the technology basis for this must be highly miniaturized actives, passives, interconnections, thermal structures, and power supplies; eventually all at nanoscale. Georgia Tech refers to such a technology as 3D All Silicon System (3D ASSM) based on the SOP concept in **Figure 3**, made possible by ultra-thin Si or glass as a system-package, merging the functions of both package and board into one system package.² In the past, system companies almost totally depended on advanced semiconductor and packaging technologies from device manufacturers and package integrators, but systems packaging had not been their focus and it may never be. They have just migrated to 2D and 3D packaging. Companies like Apple, Sony, Nokia,

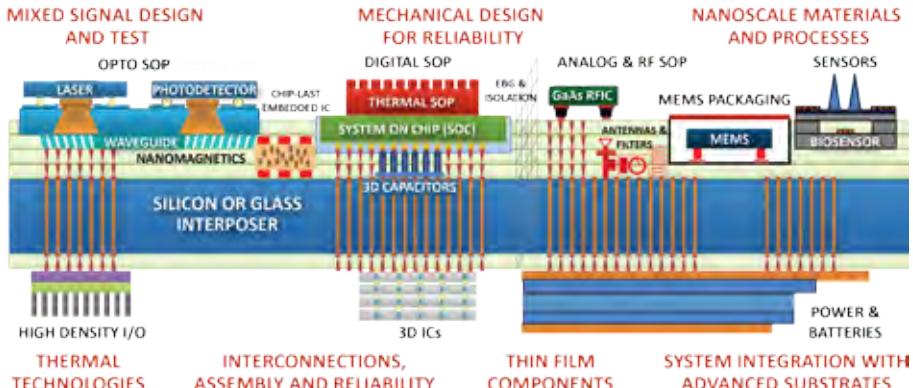


Figure 3: Entire mega-function system on a little 3D package.²

Samsung, Matsushita, RIM and other consumer electronics companies, however, have both the market need and the financial resources to drive this next revolution to 3D Systems. ^{Sp}

2. Rao Tummala, "Moore's Law Meets Its Match," *IEEE Spectrum Magazine*, 43(6), 44-49, 2006.

Rao Tummala, Ph.D., Director and Professor, 3D Microsystems Packaging Research Center Georgia Institute of Technology, may be contacted at rao.tummala@ece.gatech.edu.

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MARKET TRENDS

Dedicated Packaging Tools Help Turn On LEDs

By Eric Virey, [Yole Développement]

With established LED producers assailed on one side by softening demand, and by a large influx of rivals on another, you would be forgiven for questioning their prospects. Yet amid increased levels of competition, the industry's rapid growth is propelling it to a maturity it will need to successfully reach its ultimate destination, comprehensively penetrating general lighting and reaching "critical mass". As a consequence, the first LED packaging equipment down-cycle is set to emerge.

Yole Développement predicts that the general lighting market will help packaged LED sales double from their 2010 level to reach \$20B in 2020 (**Figure 1**). As companies positioned themselves to secure a share of that figure, an unprecedented equipment investment cycle started toward the end of 2009. In Korea, Samsung and LG rapidly adopted LEDs in LCD TV backlighting, simultaneously establishing their own LED manufacturing facilities. Then, more than 40 new LED producers created through strong incentives and

subsidies from China's central and provincial governments drove the global investment further.

As a result, Yole Développement estimates that the market for permanent bonding, die singulation, die attach, substrate separation (including laser lift-off), and testing equipment reached \$625M in 2010. Altogether, the additional investment will mean that on average, the world's LED manufacturing and packaging capacity will briefly exceed 50% more than needed in 2012. That over-investment will lead to a 12-18 month digestion phase, initiating a cyclical pattern of demand in the LED packaging equipment market. Yole Développement predicts that for the five key packaging equipment types it has assessed, the 2010 peak market value will fall by a third to \$415M in 2012. Meanwhile predicted LCD TV sales for 2011 have been revised down from 220M units to 200M. LED backlight penetration is also facing unanticipated challenges, and innovative designs have reduced the number of LEDs per TV. Therefore, in 2011, LED volumes going into TV applications will be one quarter to one third lower than initially expected, causing

a slowdown in overall LED demand. Yole Développement has consequently revised its growth forecast for the LED industry down to 6 % for 2011.

However, the recent rapid increase in the number of manufacturers has brought about a change essential for the industry's future growth, because

back-end tool vendors usually focussed on traditional semiconductor producers are now looking more seriously at LEDs, developing more dedicated equipment better suited to LED production than existing standard semiconductor packaging tools. While LED producers have previously benefited from the rest of the semiconductor industry's experience, moving on to dedicated equipment promises even greater yields, throughput, and material efficiency.

Equipment producers have further incentive to focus on this market beyond the "critical mass" created by the influx of new participants, because although demand for LED packaging equipment is set to be cyclic, it will be a less drastic cycle than the one seen in silicon applications. With LED manufacturing being much less capital expenditure intensive — as a fab costs hundreds of millions of dollars rather than billions — the barriers to expansion are easier to clear. Plus, the nearer tools are to the end of the production process, the less they will alternate between demand highs and lows.

Materials hold steady

Accelerating factors like this will help drive LED packaging material and component suppliers to achieve regular growth at a 27.6% compound annual growth rate (CAGR) between 2011 and 2016. Intensifying competition will see manufacturers seeking to differentiate themselves through an increasingly wide variety of technology options for LED packaging. Substrate material options, and assembly and interconnection techniques will therefore proliferate, and package substrate makers will see an impressive 45% CAGR through to 2016. And while phosphors will experience strong price pressure, they

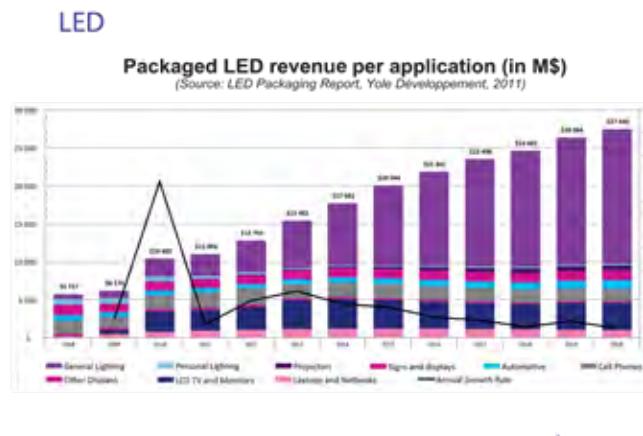


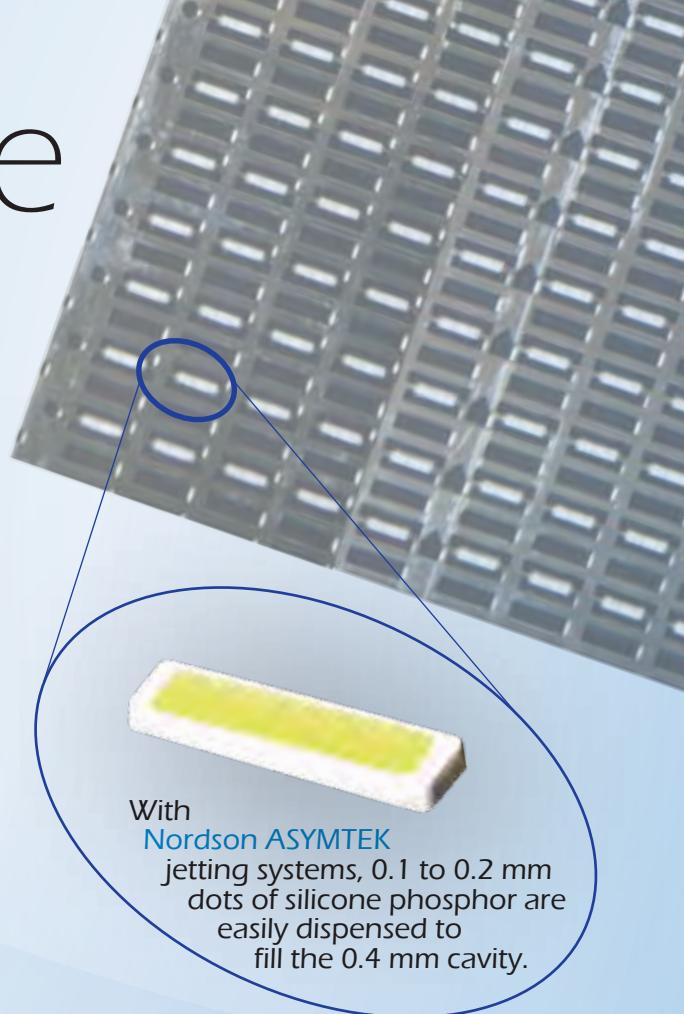
Figure 1: Lighting up LEDs: General lighting is set to be by far the dominant application for LEDs in the future. (Courtesy of Yole Développement)

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will still enjoy double digit growth, with a 12% CAGR.

Among packaging equipment, test tools are the single largest type of packaging equipment, earning \$174M revenues in 2010. Within this category sit wafer-probing tools for testing LEDs' optical and electrical properties, and inspection equipment for mapping defects after both epitaxy and later lithographic processes. More will be spent on these tools as LED production grows, while expenditure on dicing and scribing equipment diminishes further. Furthermore, general lighting applications use much larger LED chips, and can be singulated from wafers with fewer cuts. Throughput can consequently be increased without buying much extra equipment (**Figure 2**).

But there is little standardization in LED package formats being produced, which poses a challenge for test equipment makers. Their tools need to be versatile enough to accommodate 2-inch to 6-inch wafer sizes, and patterned, reflective, or transparent wafers. Die sizes range from 250 μ m x 250 μ m to over 4mm x 4mm, and driving currents vary from 5mA to 20A. The LEDs can have vertical or mesa structures with top or bottom contacts. Combined with the growing need to accommodate flip-chip-mounted packages with different contact locations and configurations, these variations make one-size-fits-all systems impossible (**Figure 3**).

Another area of growing importance in LED packaging is laser lift-off. While difficult to optimize, the process offers the potential for very high yields; close to an extremely desirable 99%. Yole Développement has identified at least eight companies using laser lift-off to produce vertical LED structures. The increased use of such tools could offset the reduction in demand that companies supplying packaging equipment using laser technology for die singulation are set to see.

Such high yields are key for

innovation in LED packaging to become widely adopted. Thanks in part to the emergence of higher yielding tools, growth in LED packaging equipment sales will resume in 2013, after reaching typical 80% industry capacity utilization rates, and peak again in 2015. Though another shorter digestion period might then be expected in 2016, Yole Développement's LED packaging report predicts more than \$2B will be invested

in new equipment for this sector between 2011 and 2016.⁶

*Yole Développement will update its "Status of the LED Industry" and "LED Manufacturing Technologies" reports in 2012.

Eric Virey, Senior Analyst, LED, Yole Développement, may be contacted at virey@yole.fr

LED PACKAGING

Equipment Market : LED Packaging Equipment Market

(Source : LED Packaging Report – Yole Développement, July 2011)

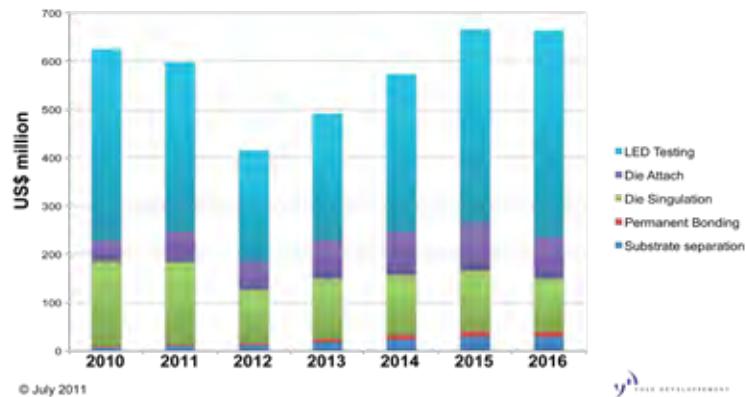


Figure 2: Testing times: As LEDs penetrate general lighting LED chips will get larger, decreasing the need for singulation tools relative to other packaging equipment. (Courtesy of Yole Développement)

LED PACKAGING

Process

(Source : LED Packaging Report – Yole Développement, July 2011)

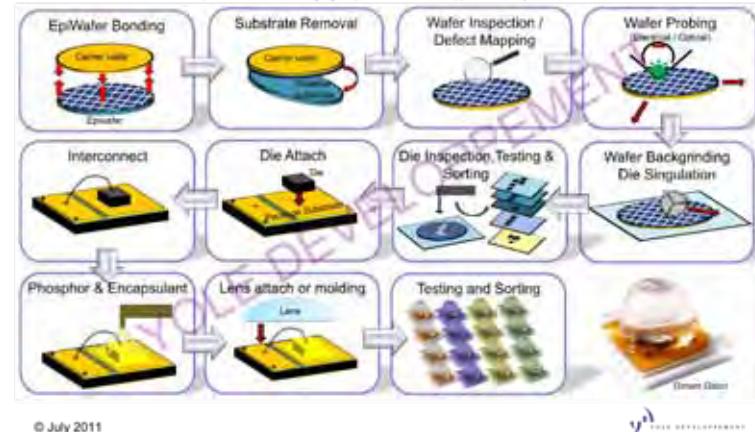


Figure 3: Critical steps: Though the stages of LED packaging are generally similar, different companies' products are typically manufactured using highly individual approaches. (Courtesy of Yole Développement)



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BUSINESS TRENDS

The Need for the Open Molded Plastic Package

By Casey Krawiec, [Quik-Pak]

When you need to meet a project or customer deadline, can you count on your outsourced semiconductor assembly and test (OSAT) provider to get you the parts you need when you need them? If the answer is "no" or "it depends", then you will clearly understand the value of having open molded plastic packages readily available for quick-turn assembly. OSATs are very good at rapidly producing large quantities of a particular packaged device. But what about small quantities of many different packaged devices? The reality is that OSATs aren't structured to support product development and device verification processes. That's where smaller, more nimble companies that stock open molded plastic packages can provide cost-effective solutions for customers who need low to mid-volume packaging.

Choosing the Package

If you are a device design engineer in the U.S., where do you get your initial run of new devices packaged so that you can test them and how do you choose the package? It is comforting and practical if the device is packaged in the same form factor that it will be in when it goes into high volume manufacturing (HVM). The comfort comes from not having to guess how the performance of the tested packaged device will compare to that of the mass-produced packaged device. It's an even better solution if the packages used for prototypes match outlines for which test sockets have already been developed. There are numerous acronyms for standard package outlines. Some of the most popular in use today include quad flat pack no leads (QFN), thin quad flat pack , (TQFP), and small outline integrated circuit(SOIC) (**Figure 1**).

Where to Package

Even when you have selected your package type, you still have to decide where to have the new devices packaged. What if the wafer with the new design is produced in the U.S.? Does it make sense to ship it overseas to be assembled and then have it returned to you so you can evaluate the performance? Even if the large OSAT provides quick turnaround, it can be a time-consuming process, especially if it takes several iterations before you are satisfied with the performance of the packaged device. If time-to-market is important, you don't want to be handcuffed with this kind of supply chain scenario. It might work a little better if the wafer is fabricated offshore near your assembler, but a lengthy iterative validation process may make your sales department go nuts.

There are numerous companies in the U.S. that provide outside assembly services. Nearly all of them focus on something other than high-volume injection molded packaging because it's difficult to be cost competitive with offshore OSAT companies. Labor costs and overhead are too high in the

U.S. To make a living, they focus on assembly services that require special processes or on product that hasn't reached a high enough volume to be of interest to the OSATs.

Therefore, a U.S.-based assembly company can provide a solution. What else do they need to have besides being located in the same continent? It's a given that they need to be able to assemble the devices. What else is needed? In a perfect world, they (the U.S.-based assembler with the solution) will have injection or transfer molding equipment with tooling for every conceivable package outline that you may need to test your device. And the equipment has to be perpetually available. If there is a queue of days or weeks, the OSAT might be the better way to go.

The Open Mold Advantage

Since having all the transfer molds readily available at the drop of a hat isn't feasible for a multitude of reasons, the next best solution is to have open molded plastic packages in stock in all the various outlines. These will be plastic packages

with open cavities. The assembler can place the device in the cavity, wire bond the pads to the leads, and then encapsulate everything with a plastic material. The plastic encapsulation will put the device in an environment that is virtually identical to when it is assembled by the OSAT in high volume with injection-molded plastic. Ceramic or glass-to-

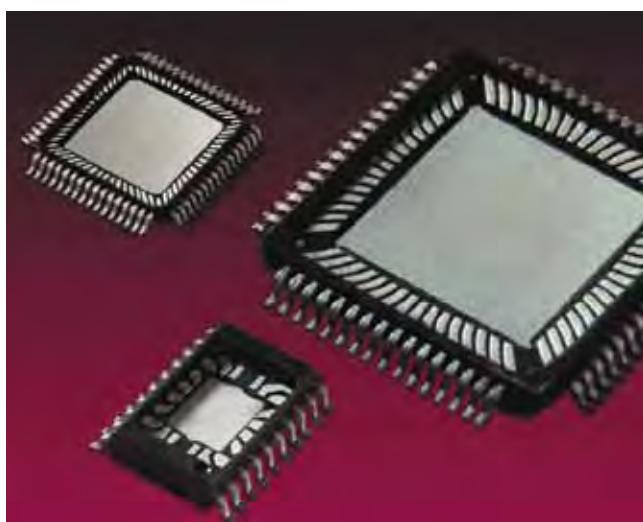


Figure 1: Examples of popular packages



metal seal packages with open cavities can also be used, but there will be a difference in electrical performance since the electric path is composed of materials that are different from the high-volume packaging configuration (**Figure 2**).

An added advantage of using the open molded plastic package instead of injection molded packaging is that the open cavity allows for the device and wire bonds to be left exposed. During product validation, especially for applications that have high frequency signal transmissions, the device design engineer may want to view the wire bonds. Viewing the wire bonds and having access to them can allow the design engineer to optimize the performance. Wire bond length and the shape of the wire bond loop may contribute to the device's electrical performance. So, being able to provide some packaged devices without encapsulation is a real benefit because it can help reduce the number of iterations to determine optimal performance. Another obvious benefit of using open molded plastic packages is that they accommodate devices that require air gaps above them. Imaging devices, MEMS, and MMICs are a few examples of devices that may require air gaps.

So, are there any U.S. companies that have a virtually unlimited number of open molded plastic packages in stock in all sorts of package configurations? There are. They exist.

The key to providing a successful alternative to the overseas OSATs is the amount of time it takes for the

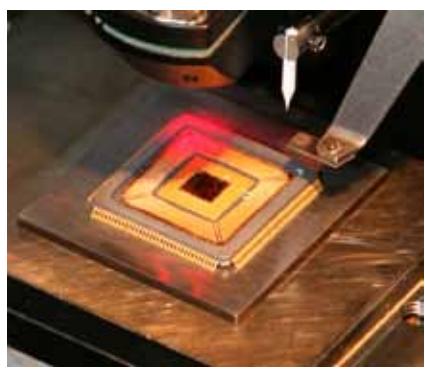


Figure 2:TQFP being wire bonded.

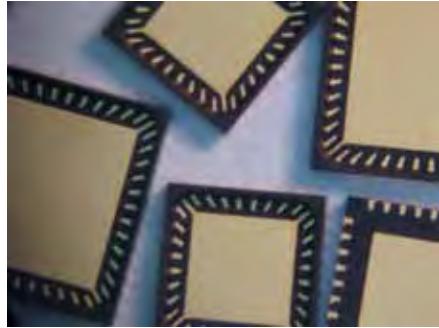


Figure 3:Open molded plastic QFN packages.

U.S. company to turn assembly jobs. They have to have short turn times on prototype builds. Excess capacity isn't necessarily nearly as critical as having manufacturing flexibility to meet surges in demand. A talented, cross-trained workforce is one of the key components to being flexible. Another is the equipment set. Investments in the latest equipment have to be made to stay in step with the leading-edge semiconductor technologies. Newer equipment will tend to be faster and have greater flexibility. Lastly, if the assembly and packaging company can offer some level of wafer processing, it makes the U.S.-based solution even more appealing (**Figure 3**).

Conclusion

The existence of open molded plastic packages enables rapid turnarounds for prototype packaged devices. Die designers are often pushed to validate the performance of their new designs as quickly as possible. The time-to-market is often paramount. OSAT infrastructure and geographical location makes it a challenge for them to support quick turn prototyping for U.S.-based semiconductor design firms. With the availability of open molded plastic packages, companies with flexible assembly operations can provide the support that is required.

Casey Krawiec, Global Sales and Marketing Manager, Quik-Pak, can be contacted at casey@icproto.com

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INDUSTRY NEWS



International Wafer-Level Packaging Conference (IWLPC) 2012 Keynote Announced



SMTA and Chip Scale Review Magazine are pleased to announce the keynote speaker for IWLPC 2012, November 7-8, 2012 in San Jose, CA. John Ellis, Author and CEO at Neodigm Press, CTO at Blue Mustang, will detail the very possible threat of cyber-physical terrorism in his presentation "A Trojan Chip in Your Smartphone? It's Coming..."

For years there have been concerns about malicious circuits being used to disrupt our critical infrastructures. However, there was little chance that rogue chips could receive commands in the coordinated fashion required to cause serious damage. Social networks have changed all of that. Hacking a few, highly-followed, celebrity accounts would

provide a perfect avenue for distributing 'self-destruct' codes to millions of Trojan chips. According to Ellis, a widespread cyber-physical attack, which would have been almost impossible to pull off just a few years ago, could soon become reality.

Ellis's expertise in this area stems from his experience in semiconductor manufacturing and from his time working

Sandia National Labs, where he focused on R&D projects for the Department of Energy, Department of Defense, National Institute of Standards and Technology, and other federal agencies. His experience includes nuclear weapons testing, missile guidance (Advanced Cruise Missile), airborne and space-borne imaging systems (Predator UAV), and semiconductor manufacturing. Ellis also served as VP of technology at SEMI, where he was responsible for global semiconductor manufacturing standards. He holds a Master's degree in Mechanical Engineering from the University of Texas.

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(continued on Page 19)

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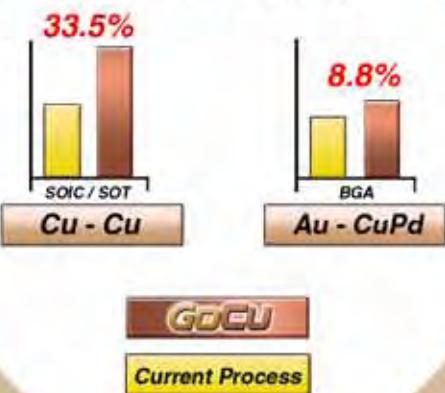
Copper Productivity Index = $\frac{\text{UPH of Cu and CuPd Wire Bonding}}{\text{UPH of Au Wire Bonding}}$

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process technologies focused on Wafer-Level Packaging (WLP) applications, IWLPC 2012 will emphasize numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand WLP solutions for integration, cost, and performance requirements.

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STATS ChipPAC Breaks Ground on Factory in Singapore

Outsource semiconductor test and advanced packaging service provider (OSAT), STATS ChipPAC Ltd. has

broken ground on a new factory in Singapore. According to the company, the new 197,000 square foot building will be located next to its current factory in Yishun, Singapore and will enable STATS ChipPAC to expand its manufacturing capabilities and capacity for advanced wafer level technologies and test solutions. “Advanced wafer level technologies are essential to support our customers’ requirements for increased performance and functionality in a smaller footprint for sophisticated mobile devices such as smartphones and tablets,” said Tan Lay Koon, President and Chief Executive Officer, STATS ChipPAC. “Expanding our global manufacturing footprint in advanced wafer level packaging will further strengthen our leadership in these technologies and reinforce Singapore’s position as a leading location for advanced

packaging technology.”

Lew Hon Sang, Managing Director, STATS ChipPAC Singapore, says the new factory contributes to the company’s strategic growth initiatives. He noted that the combination of Singapore’s infrastructure and semiconductor ecosystem, and STATS ChipPAC’s depth of technical knowledge and advanced packaging production volume experience will enable the company’s operation in Singapore to thrive in the globally competitive OSAT industry. “In 2010, we celebrated the grand opening of our new 300mm eWLB manufacturing in Singapore,” noted Sang, “(This) groundbreaking is another major milestone for STATS ChipPAC Singapore.”

Once the new building is completed, STATS ChipPAC’s combined manufacturing space in Singapore will

(continued on Page 53)

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Quality Across the Board®

A Paradigm Shift in Cu Wire Bonding

By M. Sivakumar, Leroy Christie, and James Song Keng Yew, *[ASM Pacific Technology Ltd]*

Cost effectiveness, flexibility and reliability are predominant factors affecting semiconductor packaging. The semiconductor industry is shifting into a new era of copper (Cu) wire bonding from gold (Au). Cu wire bonding is continuously evolving as a disruptive solution for Au wire bonding. The whole eco system from wafer fab, probe, wire, capillary, wire bonding equipment, molding to packaging materials are trying to adapt to this new evolution.

Generally, Cu wire bonding productivity and mean time between assistance (MTBA) is lower in comparison with Au wire bonding, due to the Cu oxidation and hardness issues. The conventional method of wire bonding is the key bottleneck for achieving better productivity and improving MTBA with Cu wire.

Productivity Challenges

Process complexity and material interaction to qualify Cu wire bonded packages is no longer a secret. Today, more packages are qualified with Cu wire than ever before. Cu wire bonding is already in mass production in many assembly packaging houses, exhibiting the level of maturity Cu wire bonding process is attaining. The key challenges are wire bonding productivity measured in units per hour (UPH), and MTBA. The Copper Productivity Index (CPI) is a new term for measuring Cu productivity. CPI, i.e. the ratio of Cu & Copper palladium coated (CuPd) wire bonding UPH divided by Au wire bonding UPH (**Figure 1**).

The major contributing factors for the lower CPI (less than 1) are copper

$$\text{Copper Productivity Index} = \frac{\text{UPH of Cu and CuPd wire bonding}}{\text{UPH of Au wire bonding}}$$

Figure 1: CPI

oxidation control during Free Air Ball (FAB), first bond formation, and second bond formation.

Cu oxidation control during FAB

FAB formation is one of the most important and critical process factors for Cu wire bonding. There are few differences between the objectives for Au & Cu FAB formation (**Table 1**). Preventing oxidation during FAB formation is the foundation for achieving a reliable process, which is not a concern for Au wire. Conventionally, the bonding sequence to form FAB is set differently for Au & Cu. In Cu wire bonding, the FAB is formed just before the capillary descends towards the first bond to minimize the oxidation of the Cu FAB. In Au wire bonding, the FAB is formed during the ascending motion after the second bond. Forming gas or nitrogen is used to minimize the Cu oxidation on the FAB surface. Cu wire that is exposed to heat from the bonding stage tends to get oxidized before it comes into contact with the bonding surface. This oxidized Cu layer inhibits the effective welding and thus contributes to lower ball-shear and wire-pull values.

First Bond formation

Challenge in Cu wire first bond on the Aluminum (Al) bond pad is Al squeeze out and remnant control (**Figure 2**).

Gold FAB	Copper FAB
Consistent FAB Size	Consistent FAB Size
Concentric Ball	Concentric Ball
	No Oxidation
	No Voids

Table 1: Major objectives In FAB formation and differences

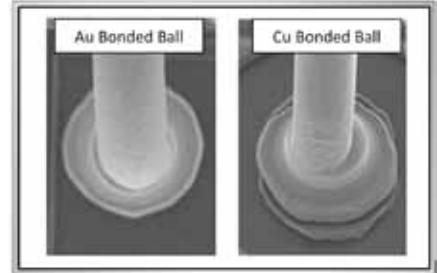


Figure 2: Au & Cu bonded ball, Al splash comparison

Compared to Au wire, Cu wire is harder and tends to get more work hardened during the wire bonding process. The differences between Au and Cu wire bonding are tabulated in **Table 2**. Bonding on non Al pad such as nickel palladium (NiPd), which requires higher activation energy, presents a different set of challenges, where the bonding requires higher activation energy. Higher energy could cause a non-concentric bonded ball. For both cases, a multi-stage bonding concept is needed to achieve a good bonded ball, and has a significant impact on CPI.

Second Bond Formation

For the second bond process, the wedge is formed by pressing the wire on the substrate/lead frame to form a good welding and to form a stitch bond that holds the wire while the capillary moves upward. Defining a process

Au Wire Bonding	Cu Wire Bonding
Objective: Welding	Objective 1: Welding Objective 2: Min. Al Splash Objective 3: Less stress to underpad Objective 4: Uniform Al remnant and ball profile
Solution: Standard Bonding Concept	Solution: Special process control features

Table 2: Major objectives In FAB formation and differences

window to form a reliable welding and a good stitch is a major challenge for thinner Cu wires. The Cu wire oxide in the interface imposes more challenges (**Figure 3**). Higher parameters can lead to form good welding. However, the tail is likely to break prematurely at the stitch area with higher parameters. **Figure 4** shows the impact of excessive energy causing tail breakage.

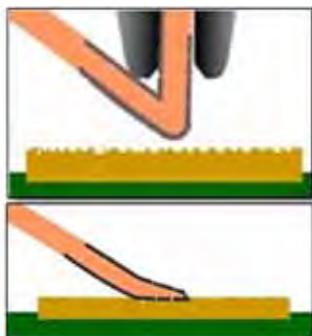


Figure 3: Illustration of Cu wire oxidation inhibiting welding

CuPd wire is used to minimize impact of oxidation. However, the hardness of the CuPd wire requires additional

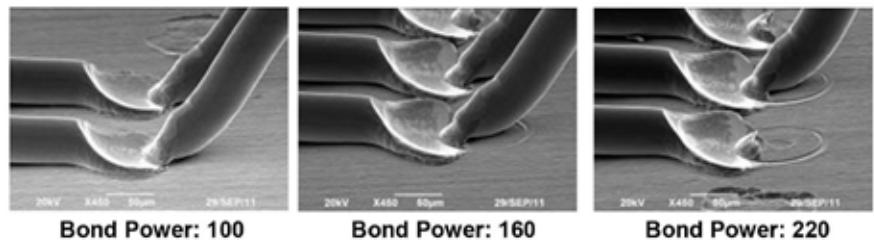


Figure 4: Impact of bond power causing tail break

parameters in second bond formation to achieve a good wire pull and stitch remain after pull test. The process becomes more challenging with micro-roughened lead frame (**Figure 5**) and pre-plated frame (PPF) because higher ultrasonic power or force could lead to poor MTBA. When compared to Au, the second bond process window is reduced and in some cases, where additional scrub features are used to enhance welding, this will lower the CPI and capillary life.

Achieving CPI >1

To achieve comparable or higher productivity in terms of UPH than

current Au wire bonding, a major paradigm shift in wire bonding process is required. Key enablers for achieving higher UPH using Cu and CuPd includes equipment and process changes as follows.

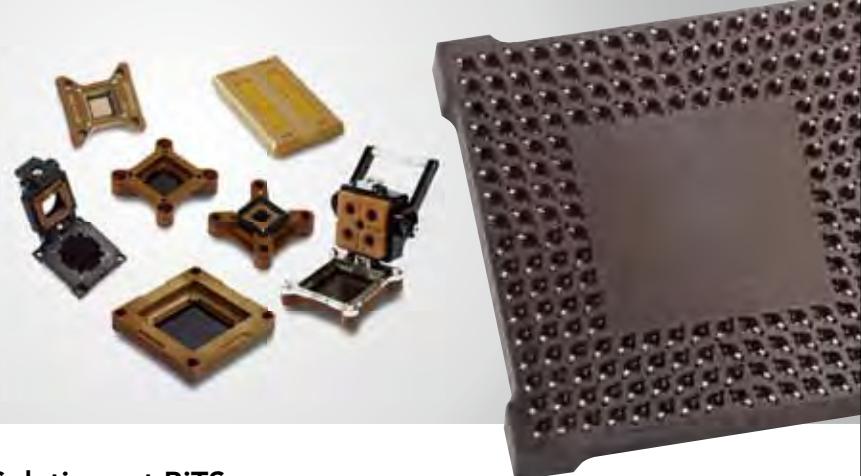


Figure 5: Micro roughened lead frame

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New Nozzle System with Shower Head

For Au FAB process optimization, the key variables are electronic flame off (EFO), current and EFO time. For Cu FAB process optimization, there are more variables such as nozzle design, EFO current, EFO time, Cu nozzle set-up and forming gas flow rate. All these variables have significant impact on the formation, quality, and reliability of the bonded ball. Nozzle design plays a significant role in quality and reliability of the first bond and is an important factor to achieve a reliable and robust bonding process. In Cu FAB formation, the forming gas shall accelerate the solidification through forced convection. The gas delivery, flow rate, and the design becomes crucial. Higher flow rate does not mean the FAB quality is good and a control flow rate must be defined based on nozzle design.

The conventional way to minimize oxidation is having gas flow either during FAB formation or having an additional gas tube pointing towards FAB. A new nozzle design is based on multi-phase fluid dynamic analysis, validated by actual bonding comparison and also dynamic flow visualization. A nozzle with an integrated gas shower head prevents the oxidation of FAB during descent towards the first bond. The gas flow from the nozzle covers some portions of the capillary (flow visualization is shown in **Figure 6**, red

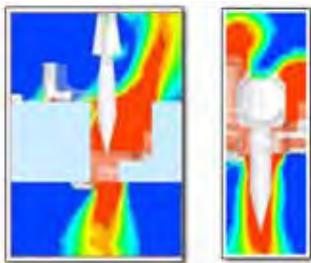
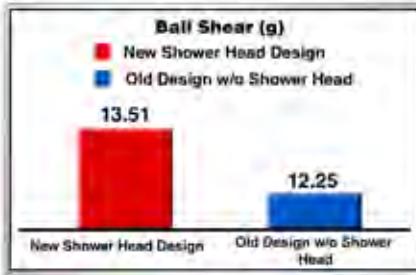


Figure 6: Flow visualization of nozzle with integrated shower

area denotes presence of gas) providing a robust protection for the Cu wire. The integrated shower creates a gas curtain protecting the FAB during descent until welding. It also protects the Cu tail after second bond formation. This protection enables a similar bonding sequence to that of Au wire. Conventionally, Cu



Graph 1: Impact of shower head design

FAB is formed only before descending towards the first bond to prevent Cu FAB oxidation. The new inert environment created by the nozzle will have significant impact on the first bond process parameter window and quality. **Graph 1** shows the improvement in ball shear (ball size 36 μ m) with the new gas delivery module protecting the Cu wire until the welding. The new nozzle also enables an increase in productivity, higher ball shear, and a wider process window. The new nozzle design provides excellent protection for the FAB to enhance good welding and minimize the need for additional energy to break the Cu Oxide on the FAB.

Enhanced Cu First Bond

The Cu wire first bonding optimization has a significant impact on the reliability performance of the first bond. Excess energy during the first bond process may give good quality during time zero (T0). However, the stress induced by this higher energy could lead to excessive, non-uniform aluminum squeeze-out. Conventional bonding concepts lead to more Al splash in ultrasonic direction. These new segmented bonding mechanisms combined with unique motion profiles achieve minimum & uniform Al squeeze-out with higher Al thickness remaining. Consequently, lower stress is transmitted to the under

pad structure with better ball shear (**Table 4**). The new bonding concept with right combination of bonding parameters and new motion profiles enables the distribution of ultrasonic energy evenly in the bonding interface to open a new world of possibility for Cu wire bonding in bonding sensitive dies with complex under pad structures, thin Al pad and non Al bond pad(NiPd) (**Figure 7**).

Second Bond Motion Sequence

There are many challenges on the second bond with new materials emerging such as ENEPIG, NiPd-PPF or MSL1 leadframe where fish tail, short tail or poor bondability may result without proper characterization. When a conventional Cu wire bonding approach is used, there can be a substantial productivity drop due to the segmented profile and slower search speed during second bond weld and stitch formation. At the same time, in a conventional approach, the stitch bond is expected to hold the wire when the capillary descends after the second bond weld formation while the wire clamp is still open. This stage becomes more critical as the wire gets thinner and subsequently, the descending search speed is kept slower to avoid short tail. The new second bond sequence can be enabled by a smart wire handler with mini wire clamp (**Figure 8**). With the introduction of a new mini wire clamp, the wire bonding sequence can be totally reinvented. In the new bonding sequence, when capillary reaches the lead frame/substrate, the mini wire clamp grips the wire holding it in position keeping the stitch bond in place making it less sensitive to the second bond process parameters. This revolutionary sequence allows

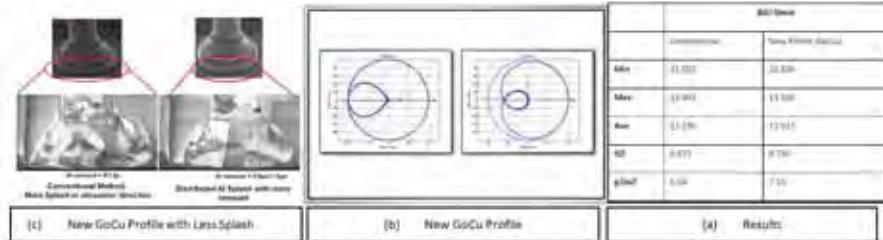


Figure 7: New motion profile and results



Figure 8: Smart wire handler with new mini wire clamp(Patented By ASM) and results.

second bond formation with higher second bond energy in shorter time to concentrate on bond sticking. When the capillary ascends, the return can be at higher acceleration, gaining productivity and achieving better quality. The new smart wire handler, combined with new motion profile, can bond rougher MSL, ENEPIG substrate and PPF lead frames with better cap life (**Figure 9**).

Auto Wire Rethread System & Advanced Looping Trajectories

A revolutionary solution, which was a dream for wire bonding engineers, is

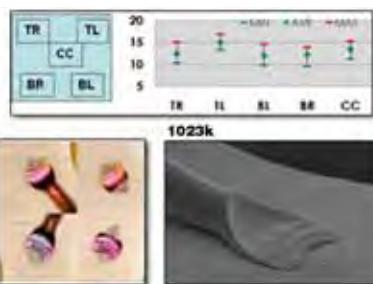


Figure 9: Achieving cap life 1M touchdown with Cu wire.

now a reality. Now, wire bonders can rethread wire when there is insufficient wire for ball formation (short tail) and improve the MTBA. It has been a dream for many engineers to see the machine re-threading wire automatically. It is now possible with a smart wire handler. Whenever there is a short tail due to contamination or poor stitch formation, the machine performs auto wire rethreading. The smart wire handler also ensures there is no more wire pull back (flying). This is a key enabler for handling wire sizes less than 0.8mil.

Cu wire, being harder than Au wire,

requires a new looping profile. Existing Au wire looping parameters cannot be directly ported to Cu wire process. Looping trajectories for Cu and CuPd can be done faster to attain higher productivity.

Note: * Current Au wire bonding UPH

Conclusion

With innovations in Cu nozzle design, new motion profile for first and second bond, smart wire handler to enable second process, an auto wire rethread system, and new looping trajectories, the Cu wire bonding paradigm has shifted. The productivity of Cu and CuPd wire can be higher than current Au wire bonding process and consequently achieving a CPI that can be greater than one. 

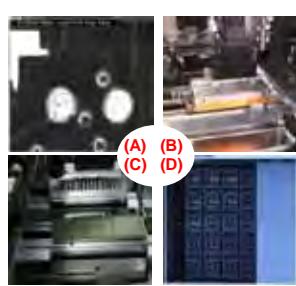
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Room Temperature Mechanical Lift Off Debonding

The Next Step in Temporary Wafer Handling for 3D IC

By Chris Rosenthal /SUSS MicroTec

Looking back I guess we were all naive to think that temporary bonding and debonding of thin wafers would be like making and tearing apart Oreo cookies – a little twist with a pull and “voilà”. Well, as we know, the industry has tried its best over the past several years to come up with a single adhesive to serve as the filling, but unfortunately, the results are just not good enough for more than the simplest process integration schemes. And without the ability to process the most advanced wafers, the performance-to-cost benefit ratio just isn’t there to take 3D IC to mass production.

In the beginning, a single layer of wax was used to mount the wafer so processing could take place. However, this wax was only capable of surviving a few of the required processes as it was prone to many failure modes. Then single layer thermoplastic techniques were tried and found to be more useful than wax, but short comings have become apparent as device wafers have been thinned further, thermal budgets trimmed, and bump heights increased. Simply heating and sliding off or dissolving in copious amounts of solvent will not stand up to the more demanding requirements being put forth today.

Laser debonding methods simplified and significantly sped up the carrier release process. 3M’s usage of a “sacrificial layer” called Light To Heat Conversion (LTHC) solved a lot of problems and was one of the first temporary bonding systems that used a two chemical process: the first chemical being the bulk adhesive and the second being a dedicated release layer. This “division of labor” by material properties appears to be the

direction of the industry.

This concept of a two-part adhesive system for temporary bonding is not limited to using radiation as the separation initiator. Companies like ThinMaterials AG (TMAT) have come up with chemicals that can be separated mechanically ([Figure 1](#)).

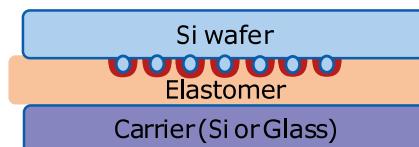


Figure 1: Thin Materials' two part adhesive system. (Courtesy of TMAT)

TMAT's process requires three main ingredients:

- a *carrier* which provides the ultra-thin wafer mechanical stability
- an *adhesive layer* which covers the topography of the wafer
- a *release layer* which defines the force needed for final de-bonding of the ultra-thin wafer

ZoneBond is another relatively new process that mimics a two-part adhesive system. However, instead of applying two chemicals on top of one another, this technology depends on

the creation of a release zone on the carrier wafer to control adhesion of the device wafer to the carrier wafer. The device wafer is truly adhered to the carrier wafer, but only on the outer perimeter of the carrier wafer, while the rest of the wafer remains unbonded but completely supported ([Figure 2](#)).

Integration of a release layer, primer or release zone facilitates a whole new set of options when it comes to debonding. Furthermore, these new bilayer or two part adhesive systems are capable of being debonded at room temperature and this provides a significant advantage over previous methods.

The debonding process is critical to the survival of the wafer and the balls/bumps attached to it. As you can imagine, simply pulling on the entire surface of the carrier would entail applying a tremendous amount of force. A force of this magnitude would easily overpower that of an e-chuck or vacuum chuck and the wafer would simply pop off during the pull. On the other hand, if you tried to grab the wafer just at the edges there is a very high probability that you will create fractures at the contact points and do

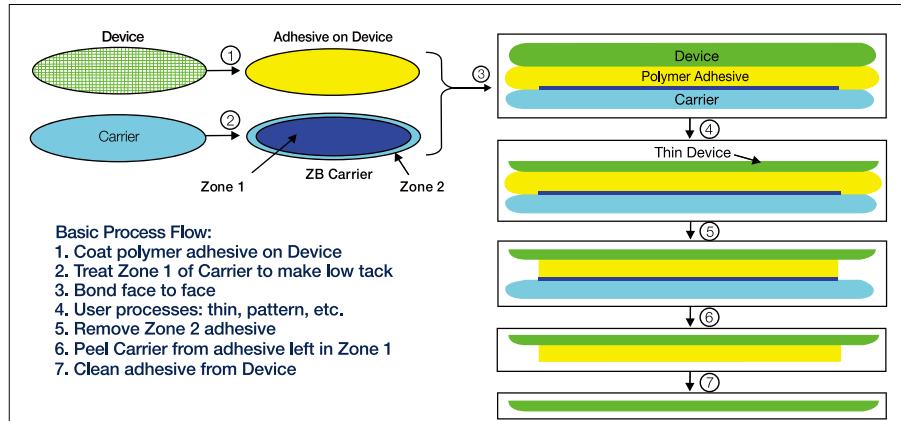


Figure 2: Zonebond processes flow (courtesy of Brewer Science)

permanent damage to the wafer potential leading to 100% yield loss. What is needed to overcome this difficulty is a peeling motion along with a separation initiator. Think of this in terms of peeling a banana. Quite often when you pull on the stem of the banana the skin does not give way and you end up smashing the delicious flesh of the fruit located near the stem as you try to twist, bend and pull. However, with just a nick of the skin the peel of the banana comes right off in one smooth pull. The same strategy can be employed when trying to peel a temporary carrier from a delicate- and expensive- thinned wafer. The only difference being that when it comes to wafer debonding, you cannot be careless and just throw away the peel like you would with a banana. You have to be very careful not to destroy the carrier wafers as they are fairly pricey and need to be recycled in order to preserve a significant portion of the cost-of-ownership (CoO).

One method that is very well suited to gently coaxing apart the temporary carrier from the device wafer at room temperature without damaging the two is the use of a flexible support chuck. By attaching the carrier wafer to a flexible chuck, one can gently bend and peel back the carrier wafer while keeping the device wafer flat and stress free. This controlled peeling method can be used with all of the room temperature debonding materials mentioned above. Once the carrier wafer has been removed without damage, the device wafer can be cleaned and sent off for dicing while the temporary carrier can be readied for reuse through various reclaiming processes.

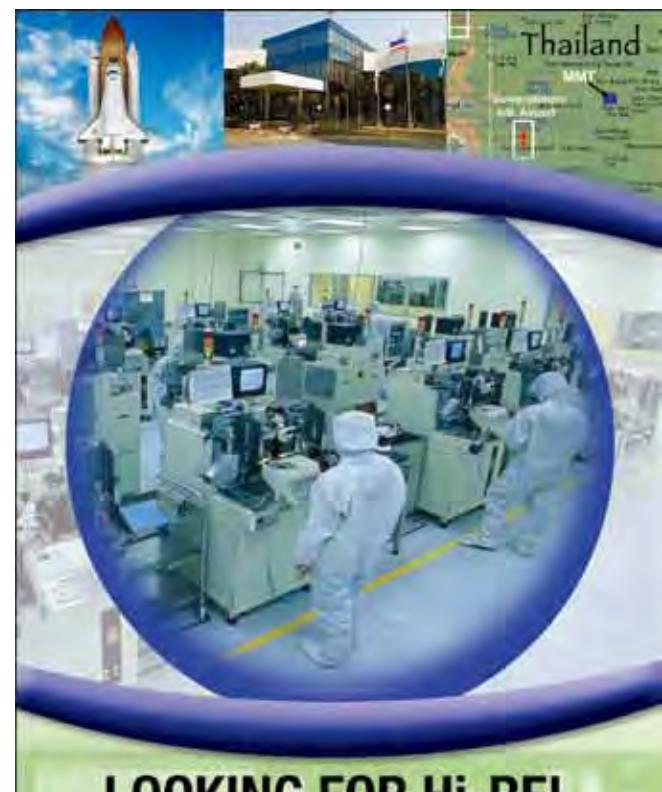
Conclusion

Even with the two-part adhesive systems, there are some very big challenges that require the materials to be engineered precisely. For example, the “tackiness” of the bond between the release layer and the adhesive has to be sufficiently strong to survive the stresses encountered during back grinding; however, the bond also has to be sufficiently weak so debonding can occur without pulling off micro-bumps or solder balls that are embedded in the adhesive film. It is unclear whether a two part material process will be sufficient. Maybe three chemical components or a trilayer will be required. Nevertheless, one thing that appears to be here to stay is room temperature mechanical lift off debonding. ☺

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Miniaturization Drives Advanced Packaging Cleaning Requirements

By Mike Bixenman [Kyzen Corporation]

Electronic assembly innovations drive more performance using highly dense interconnects. Assembly residues may increase the risk of premature failure or improper functionality. The challenge for OEMs is to quantify safe residue levels and determine the residue impact on long-term reliability and functionality of hardware. The question of "how clean is clean enough" is more challenging as conductors and circuit traces are increasingly narrower.

Highly dense advanced packages decrease conductor pitch, spacing, and bump heights. The problem is that current spacing trends can lower the distance between printed circuit traces as small as 2 mils. As electrical fields rise, contamination at these narrower traces becomes more problematic due to voltage swings, high frequencies, leakage currents, and high impedance.

Advanced Packaging Trends

Advanced packaging innovations are driven by market pressures for higher functionality, increased memory, cost reduction, faster cycle times, and improved quality. These innovations fuel integrated circuit

growth with demand greater than 200 billion packages.¹ To achieve increased functionality, electronic products are packaged using smaller form factors (**Figure 1**). Electronic devices increase speed and accessibility using 3D packaging including through-silicon vias (TSV), high-density interconnects (HDI), die shrinkage, package on package (PoP), embedded actives and passives.

Copper pillars provide numerous advantages such as lower bump heights, downward scaling, tighter pitch and package routing, and extension to higher I/O densities, which allows for higher pin densities and reduced die sizes.² 3D TSV packaging reduce form factors, making image sensors and power amplifiers on the back side of silicon chips possible. PoP allows for stacking integrated circuits with solder joints between the top and bottom packages.³ PoP stacked die minimize size, packaging cost, and increase speed. System -in-Package (SiP) creates a functional subsystem utilizing a combination of wire bonds, flip chip, stacked packages, and stacked die.⁴

The mobile phone market continues to drive the demand for smaller and thinner packages.⁵ Assembly trends

include reduced bump pitch from 200 μm to 125 μm . The shift to lead-free creates the challenge of finer pitch bumps and higher reflow temperatures with active and passive devices (**Figure 2**) mounted on top of the substrate. Additionally, discrete passives may be embedded into the device landscape. Highly dense interconnects allow for short connections with line and spacing down to 20 μm .⁶

Recent advances in device miniaturization have placed stringent requirements for all aspects of product manufacturing (**Figure 2**).⁷ Less board real estate allows for shorter communication paths, lower junction temperatures, and integration of logic and memory.⁸ The problem is that improved functionality creates a two-edged sword with multiple benefits but with greater reliability concerns. These innovations affect assembly processes, equipment, design and simulation tools, reliability, and thermal management.

Contamination and its Effect on Reliability

Leakage current across conductors is a growing concern with feature size reduction.⁹ When the distance between conductors narrows, electrons have a



Figure 1: HDI Flux Residues Examples



Figure 2: Flux residue bridges conductors on active and passive components

greater probability of migrating. As a result, device cleanliness grows in importance. One such example is high frequency devices for quickly transferring significant amounts of data.¹⁰

As the current trends toward miniaturization take hold, proper cleanliness levels become more difficult to achieve.¹¹ Smaller spacing between conductors yields a larger electric field, which in conjunction with insufficient cleaning can lead to dendritic growth. Electrochemical migration—the growth of metallic fragments across conductors—may cause electrical shorts and/or intermittent device function. For leakage to occur, monolayers of moisture create an electrolyte solution, which allows ionic contamination to dissolve contaminants across conductors. When the affected component is powered up, the electric field (voltage divided by the distance between conductors) increases as pitch narrows. The reality is that metals are more susceptible to propagation across highly dense conductors, which may eventually short the device.¹²

The current trend toward finer pitch and high density/high impedance designs have resulted in conductor spacings in the range of 20-100 μm . Higher I/O and low gap height can entrap contamination. Tighter spacing results in a higher e-field. With the forces on a charged particle being directly proportional to the e-field, the cleanliness of advanced packages becomes more critical.

To understand this issue more fully, a study is underway to examine the effects of contamination as a function

of the electric field. A series of test boards were designed to study the contamination effects (**Figure 1**).¹³ The study is designed to study four levels of bias:

1. High voltage/high pot.
2. Leakage current
3. Rate of current change
4. Frequency

The results of this study will be presented at the 2012 IPC APEX Technology Conference.

Cleaning Process Considerations

Each advanced package has its

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unique properties. The contaminants present and the sequence within the manufacturing process influence the need for cleaning. When cleaning is required, the first step is to identify the chemical nature of contaminants present on the device and/or assembly. Contaminants can be classified into three categories:

1. Polar / Ionic
2. Non-polar / Non-ionic
3. Particulate(s)

The contaminants present on the device greatly influence the cleaning agent design for dissolving and removing the contaminant.

Engineered cleaning agents are formulated with a range of materials that remove a specific subset of soils, provide a wide compatibility window with cleaning equipment and the devices materials of construction, and designed to operate in the specific cleaning tool design. Predictive theorems drive the formulator's choice of materials. Similar to the electrostatic forces of attraction that drive electronic theory, Coulomb's Law of attraction

also applies to cleaning agents by engineering materials that are attracted to opposite charges (ionic residues). Opposite charges between the cleaning agent and the

soil create a magnetic force that improves dissolution. When non-ionic (covalent) soils are present, cleaning agents incorporate materials that have similar properties to the soil. Engineering the right materials into the cleaning agent helps overcome the intermolecular forces of attraction by allowing the non-ionic contaminant to be dissolved into the cleaning agent.

Component miniaturization increases cleaning difficulty due to marginal Z-axis clearance, low accessibility and entrapment within the body of the device. Selection

of soldering materials that leave a soft soil opens the cleaning process window. For example, selection of water-soluble based flux residue is much easier to clean under the Z-axis than rosin or resin based soil. Resinous based soils require higher levels of solvency (organic cleaning agents) and energy forces, which increases cleaning process factors.

The solder process progressively starts by evaporating flux volatiles, initiates flux activation, raises the device to a temperature that allows the solder to flow evenly onto all surfaces, and reflows the alloys to facilitate solder connections. Excessive exposure to heat can oxide (char), crosslink (polymerize) and harden residues. Temperature excursions and the time exposed to liquidus solder temperatures influence cleaning properties. Optimal soldering processes should only be hot enough to enable the solder to wet the board and components, yet cool enough to not damage the items being soldered, followed by a controlled cool down to

As the current trends toward miniaturization advance, proper cleanliness levels will become increasingly important to device functionality and reliability.

ensure solder joints are sound.

When cleaning high density interconnects, the cleaning equipment must deliver the cleaning agent to the residue. Fluid flow, directional forces, and applied energy are often needed to penetrate low clearances and remove residues.

To remove residues under the die, the cleaning solution must wet, dissolve, and create a flow channel in order to dissolve or displace all residues from under the die surface. The selection of both the cleaning agent and cleaning equipment are

critical and must work hand-in-hand to achieve this demanding cleaning requirement.

Conclusion

High density device miniaturization places stringent requirements on all aspects of product manufacturing. As the current trends toward miniaturization advance, proper cleanliness levels will become increasingly important to device functionality and reliability. These increased demands can place a bottleneck into the manufacturing process. Designing the device with cleaning in mind not only improves reliability but will open the manufacturing process window. 

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An Optimized Process Flow from Interconnect Roots

By Jon Hander, Demetrius Papapanayiotou and Cristina Chu, *[NEXX Systems, Inc.]*

Adoption of via middle processing for through silicon via (TSV) technology requires transferring semiconductor fabrication steps typically performed in a back end of line (BEOL) advanced packaging facility to a front end of line (FEOL) fab. This poses technical and economic challenges that the industry must overcome to benefit from the performance differentiators that TSV offers. Implementation of this technology began as an extension of the metal interconnect process flow in FEOL fabs. However, many challenges that TSV adoption poses are unlike those faced with submicron copper wiring.

TSV Critical Dimensions

Figure 1 illustrates the progress that FEOL fabs have made towards critical dimension (CD) scaling over the last 40 years. The maroon point marked as ‘a’ represents the standard via middle TSV dimension, 5x50 μm , for 2011. From a CD perspective, feature size is not the challenging aspect of TSV adoption. TSV size is not governed by the lateral dimension. Feature depth is the CD for TSV, and is governed by substrate thickness, which is determined by physical handling or manufacturing limitations during the packaging process.¹ It is desirable to minimize the TSV width. Although there are only hundreds to thousands of TSVs on a die, their relatively

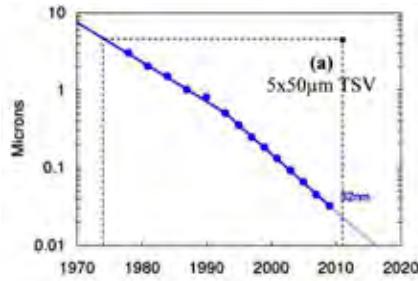


Figure 1: CD scaling as a function of time shows feature size of today's TSV is not a technical challenge for FEOL fabs (a) 2011 standard dimension, via middle TSV.

large size consumes enough substrate area to require an increase in die size. This increases cost per die because the manufacturing cost per wafer is distributed across fewer chips. Larger die area also decreases product yield since wafer defect density leading to bad die per wafer will remain constant and the number of die per wafer decreases.

Adding to a need for a minimal TSV diameter is a keep out zone requirement (KOZ). The coefficient of thermal expansion (CTE) mismatch between Si and Cu induces strain in the substrate near each TSV, affecting electron mobility and slowing transistor performance in the affected area. For this reason, several microns of space around the TSVs cannot be used for transistors, which compounds the effective substrate consumption of each TSV.² A reduction in TSV size helps by shrinking the KOZ space in addition to the actual area reduction of the TSV itself.

Following feature depth definition, the width of the TSV is determined by the maximum aspect ratio at which void-free Cu fill can reliably be achieved. Identifying this process window depends on the interrelated capability of TSV etch profile, barrier and seed coverage within the TSV, and TSV fill using electroplating. The TSV profile should be smooth without overhanging or bowing (**Figure 2a**). From a materials perspective, TSV etch is less challenging than interconnect etch, which requires the formation of straight sidewall trenches over vias through multiple materials such as SiO₂, SiOCH and SiCN. The material properties of these films are designed to be different, so uniform film etching can be challenging. TSV formation is typically into a Si substrate, which is a more straightforward process. The barrier and seed must be continuous and thick enough to transfer current to the bottom of the features to promote bottom-up fill during plating (**Figure 2b**). The TSV

fill should be void-free with minimal overburden (**Figure 2c**). The typical TSV middle aspect ratio is 10:1. Once viable manufacturing processes are available, the industry will drive to $\geq 15:1$ to minimize silicon consumption and overall die size.

Interconnect or Advanced Packaging?

TSV formation and fill can be completed economically assuming high equipment utilization rates while also providing a considerable performance benefit, especially if it enables heterogeneous chip stacking. If the TSV middle approach is used, chemical mechanical planarization (CMP) would probably continue to be

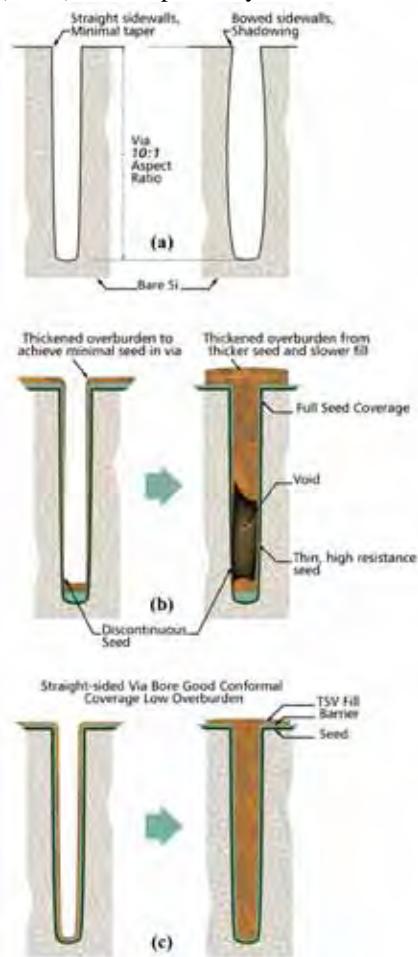


Figure 2: TSV process window: void free fill achieved within maximum aspect ratio shown.

completed in a FEOL fab. After CMP, defectivity and queue time are critical, especially if thin wire metal is exposed. CMP processes for TSV are also similar to those of subsequent damascene processes, and would be unique in an advanced packaging facility. The processing technology required for TSV formation is advanced, but the equipment used for each step has been proven in manufacturing. If an advanced packaging facility were interested in completing the TSV middle steps, it could do so with minimal investment and a short learning curve.

Although TSV formation steps could be completed on an advanced packaging line, continuation of the interconnect process would require the wafers to be returned to a FEOL fab. Additionally, the equipment required to complete the TSV formation steps is readily available in the FEOL fab, providing a significant cost-savings that is unlikely to be overcome. For this reason, it is likely that the TSV middle process will remain in FEOL fabs. However, the sizes associated with TSV (i.e. 5 μm wide by 50 μm deep) are orders of magnitude greater than modern interconnect dimensions (i.e. <100nm wide by <0.5nm deep), and will be unfamiliar to most interconnect engineers.

TSV introduction challenges exist regardless of the manufacturer's core competency. Though advanced interconnect technologies use similar materials to TSV, the unit process and integration challenges are different, and in some cases opposite those encountered with interconnect processing.

Challenges of Reverse Scaling

Introducing a 5 μm x 50 μm feature into a <20nm CD process flow represents a scale-up of one to three orders of magnitude depending on the method of comparison (**Table 1**). Applying similar processes, practices, and equipment to interconnect and TSV is a logical approach to start with, but is unlikely to yield optimal results from either a cost or performance perspective.

TSV seed thickness is governed by a more relaxed set of requirements relative to interconnect fill. For interconnect trenches, the metal diffusion barrier can

consume enough of the trench volume to increase line resistance above the design rules. Volume consumption of the barrier metal is negligible for TSV features. Bottom coverage of higher resistivity barriers such as TaN also needs to be minimized to keep resistance low

	Inter-connect	TSV	Scale Factor
Feature Width	<100 nm	4-50 μm	1000
Feature Depth	<1 μm	50-250+ μm	100
Feature Fill Time	~ 60 s	20-90 min	20 - 200
Seed Thickness	300-500 Å	2000-8000 Å	10

Table 1: Introduction of a 5 μm x 50 μm feature into a <20nm process flow represents a scale up of one to three orders of magnitude.

between interconnect layers, but since the bottom of a TSV feature is etched or polished away during the reveal step, this is of no concern.

For uniform, void-free electroplating, seed thickness is critical and needs to be continuous across the entire surface of the features, or voids will form during the electroplating process. If the seed is too thin, or seed resistance is too high, a phenomenon known as the terminal effect will need to be controlled. The terminal effect occurs during the electroplating process when there is a large change in sheet resistance from the lowest value at the edge of the wafer where the electrical contacts are made, to the highest value at the center of the wafer, which is the point furthest from electrical contact. If this effect is not compensated for, deposition rate in the center of the wafer is suppressed, resulting in a high degree of within wafer uniformity that is difficult to planarize during CMP. Terminal effect becomes the limiting factor for defining the minimum seed thickness when highly conformal seed layers are used. If seed thickness consumes a significant amount of vertical feature area, such as along trench sidewalls, pinch-off voids can occur. For interconnect, the process window continues to shrink with each technology node. The terminal effect, or seed conformality, continues to define a minimum acceptable seed thickness for both applications, while shrinking features

drive down the maximum allowable thickness for interconnects only because feature sizes for TSV are large enough to eliminate the concern of thick seed leading to pinch-off voiding. Since TSV seed thickness requirements are only bounded on the lower end, the problem is easily overcome for this application.

Chemical vapor deposition (CVD) is a potential solution for TSV barrier formation. There are a number of CVD metals with acceptable barrier and adhesion properties that provide much higher step coverage for deep TSV features. The bottom of the TSV feature is removed during the reveal step, so unlike interconnect, bottom thickness of the barrier metal is not much of a concern. Volume fraction of the barrier metal is insignificant, so sidewall thickness does not play a role in the material selection process. However, barrier metal resistivity is a consideration. If the resistivity is low enough, the barrier metal can be used as a seed layer for the electrochemical deposition (ECD) of copper. Alternatively, an additional seed layer should be deposited. This could potentially be accomplished using CVD, but PVD, ECD or electroless seeds are commercially available solutions.

Longer feature fill time for TSV is the product of significantly larger deposit mass and lower deposition rate. It is counterintuitive to think that TSV features would require lower deposition rates since they are so much larger than interconnect features. This requirement is driven by the diffusion rates of the organic additives. TSV chemistry formulations must maintain suppression of field plating relative to the features for a much longer time compared to interconnect. In TSV, the chemistry must promote bottom-up fill, which yields faster plating times with lower overburden compared with chemistries that fill in V-shaped or conformal fashion. Bottom-up fill of most existing TSV chemistries reaches a saturation point after about thirty minutes. Conformal fill takes place once this occurs, further decreasing the fill rate, while substantially increasing the overburden thickness, and increasing the probability of seam voids. This fill time limitation is not an issue for 5x50 μm

TSV features, but not sufficient for larger features, such as interposers, which are typically $10 \times 100 \mu\text{m}$ in size. Several chemistry suppliers are developing new additive packages that extend this bottom-up fill time to over an hour. This capability enables the use of a single chemistry for TSV middle and interposer size features, so the benefits associated with bottom-up fill can be realized for both applications.

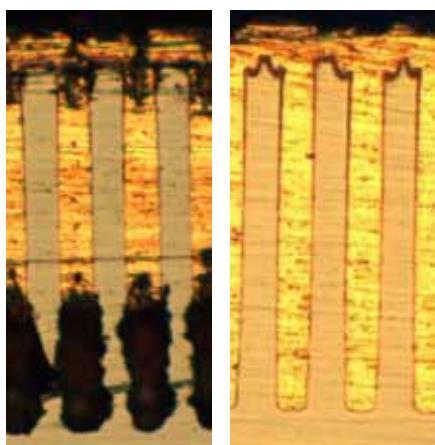


Figure 3: A comparison of fill capability using marginal conditions with and without a vacuum pre-wet step.

Three TSV challenges absent from interconnect are seed wetting, overburden thickness, and protrusions. TSV features do not wet during the electroplating process as efficiently as interconnect structures. The surfactants contained in the additives and capillary action that fully wets interconnect cannot overcome the larger feature sizes required for TSV fill. The solution applied to this problem is vacuum pre-wet, which is performed immediately before the electroplating process, and evacuates all of the air from the TSV structures while backfilling with water or another liquid to promote

faster feature fill. **Figure 3a** shows fill performance with an atmospheric pre-wet step for a high aspect ratio (HAR) structure filled using conditions selected to provide marginal performance. **Figure 3b** demonstrates that complete fill can be obtained for the same process conditions when a vacuum pre-wet is used.

A primary concern with Cu overburden is the cost of removing it through CMP.³ Overburden thickness was a concern

for early interconnect technology nodes such as 130nm, but shrinking feature depths, improvements in ECD chemistry, and CMP consumable cost reduction minimizes this issue for advanced interconnect technology nodes. Cu overburden thickness for TSV can be in excess of $5 \mu\text{m}$ for a $50 \mu\text{m}$ deep structure. This consumes a significant amount of CMP consumables and equipment time. Improved chemistries for ECD fill of the

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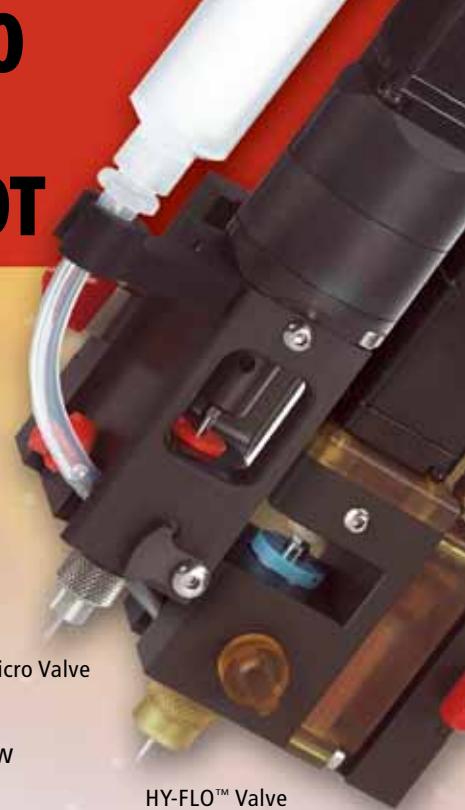
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Table 3: TSV roadmap challenges for production ramp.

Feature	Interconnect	TSV
Horizontal Scale Driver	Critical Dimension	Aspect Ratio
Vertical Scale Driver	Aspect Ratio	Si thickness
Etch profile	Multiple Materials	Only Si
Barrier Volume	Big Concern	No Concern
Bottom Barrier Coverage	Resistance Effect	No Effect
Thin Seed	Within Wafer Uniformity, Voids	Within Wafer Uniformity, Voids
Thick Seed	Pinch-off Voids	No concern
Seed Wetting	Small Concern	Big Concern
Overburden Height	Small Concern	Big Concern
Protrusions	Small Concern	Big Concern
Plating Defects	Big Concern	Small Concern

Table 2: Comparison of feature concerns between TSV and Damascene applications.

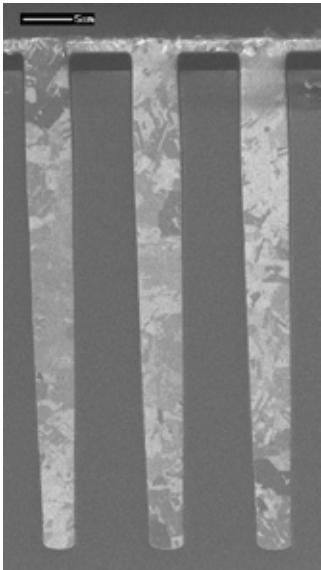


Figure 4: Advanced ECD Cu chemistry formulation fills a void-free 5x50µm TSV structure with a 1µm overburden using a conformal CVD barrier metal. (Structure wafers courtesy of Sematech, imaging courtesy of Atotech.)

TSV can utilize bottom-up fill of 5x50µm structures, reducing the ECD contribution to overburden. PVD seed deposition thickness is typically in excess of 0.5µm, so there is room for optimization here as well. With the appropriate seed and a bottom-up chemistry, Cu overburden of less than 1µm can be achieved.

Cu protrusions occur during high temperature processing steps following overburden CMP, such as SiCN cap deposition.⁴ Completion of grain growth during the anneal step prior to CMP can

minimize the occurrence of protrusions with the help of chemistry optimization. Silicon strain associated with the CTE mismatch between Cu and Si is increased as a function of annealing temperature. Raising the annealing temperature to control protrusions increases the KOZ. This tradeoff will require a solution to achieve acceptable performance.

Five potential solutions are listed in **Table 3**. Identifying a compromising anneal condition to achieve acceptable performance in terms of KOZ and protrusions is the starting point for most process flows. However, the cost associated with increasing the KOZ or dealing with protrusions is high. Protrusion height for a given anneal condition depends on the ECD chemistry selected. Chemistry optimization can reduce the protrusion height, but it is not a comprehensive solution if it results in an increased chemistry cost, or longer fill time. Several novel process flows have identified unique ways to overcome the problems of KOZ and protrusions. Revolutionary changes have their role to play in enabling continued progress. The adoption of Cu interconnects, shallow trench isolation (STI) as a replacement for local oxidation of Si (LOCOS), and 3D interconnect were three ideas. However, most novel process flow solutions are less desirable than the problem that they are attempting to resolve.

TSV interposer is a proven solution that minimizes the footprint of the substrate, while limiting protrusions. Interposers are discrete substrates without active devices containing TSV structures, and in some cases interconnects. Interposers allow multiple ICs to be mounted next to one another using interconnects, or stacked using the interposer TSV. Interposers do not require a KOZ since they do not contain active components. Therefore, Cu anneal can be optimized to minimize protrusions without an expanding KOZ. This approach is low-cost because it consumes no additional surface area on the ICs and is production-ready. Products are already available that utilize this technology. FEOL and advanced packaging suppliers can both fabricate interposer wafers. However, interposer

performance is not as high as what can be achieved through an integrated TSV solution. Interconnect lengths for ICs mounted side by side are longer, and therefore slower than vertically stacked ICs. IC stacking using interposers requires additional substrate bonds, which increase interconnect resistance and stack height.

Reduction of via diameter is the ideal 3D solution to resolving the tradeoff between limiting the KOZ area and protrusion height. Silicon thinning provides some additional advantages, but is less effective than increasing TSV aspect ratio by shrinking via diameter. Smaller diameter vias induce less strain on the surrounding silicon, which allows the post ECD anneal step to be performed at higher temperatures, resulting in reduced protrusion height with a smaller KOZ.

Future Trends

Although true 3D ICs have a lot of promise, the cost and complexity of adoption will drive evolutionary improvements in existing flip chip packaging where cost is a bigger selling factor than size, performance, or power consumption. TSV interposers are expected to offer an intermediate solution, especially for logic devices that require large numbers of TSV's, and also need heat dissipation.

High aspect ratio (HAR) vias will overcome many challenges facing TSV. TSV and KOZ area reduction will minimize substrate area consumption. Smaller TSV volumes will reduce ECD fill times, increasing ECD throughput and reducing Cu overburden, while concurrently improving ECD and CMP costs. There are several reasons this solution has not been adopted. TSV formation, barrier and seed deposition, and via fill using ECD, require evolutionary performance enhancements to permit large scale fabrication of HAR features. Smaller diameter vias would also reduce the Cu to Cu bonding area where bond integrity is already questionable. Finally, bonding overlay issues also become increasing important as TSV diameter shrinks.

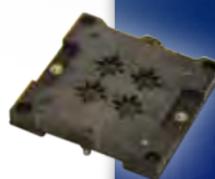
As TSV development transitions from its roots with interconnect into its

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own optimized set of processes, CVD metal barriers are also expected to experience intense adoption. Several fundamental challenges, such as material selection, and whether or not to follow a plate on barrier scheme, need to be resolved.

ECD Cu chemistry for TSV is expected to substantially reduce fill times. The mechanism for this improvement will likely help reduce Cu overburden. Chemistry formulation improvements will allow a single additive set to meet TSV middle and TSV interposer feature sizes, so fabs can utilize a single electroplating tool set to manufacture both technologies.

Conclusion

In general, TSV formation and fill technologies will continue their divergence from interconnect. A baseline interconnect process flow was logical at the outset, to focus on identifying solutions to the integration challenges associated with TSV. However, as illustrated in (**Table 2**), the unit process and integration of these metallization steps differ greatly, and common solutions will probably yield less than optimal results for one or both processes. In many cases, hardware and material divergence will make independent process definition beneficial. Some of these diverging activities are already visible. Equipment dedicated to several steps, such as TSV etch, conformal dielectric liner and electroplating, already exists. Electroplating chemistries and CMP slurries specifically tuned for TSV applications are also commercially available. **Figure 4** shows a 5x50 μm TSV structure utilizing a highly conformal CVD barrier metal that was filled with an advanced ECD Cu chemistry formulation providing void-free fill with a 1 μm overburden.

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Burn-in Sockets for CSP's: An Update on Challenges

By James Forster, Ph.D. [WELLS-CTI]

It seems redundant to begin this update with the common phrases of faster, smaller, hotter or to reference Moore's law or More-than-Moore. I'd rather just reference the introduction from my 1998 article, "The portability revolution in communications, computing and consumer products continues to drive the miniaturization of electronic packaging."¹

Certainly the roadmap presented and updated by The International Technology Roadmap for Semiconductors (ITRS) provides a window into what technologists are working on. But Steve Jobs probably put it best in 1997 when describing Apples' strategy and vision at the World Wide Developers Conference. "One of the things I've always found is that you've got to start with the customer experience and work backwards for the technology," said Jobs. "You can't start with the technology and try to figure out where you're going to try to sell it."²

Consumer products are driving the development of products that were unimagined in the early 1990's when chip scale packages (CSPs) were developed. The ubiquitous handheld device allows us to not only communicate both verbally via the phone, and visually across the net using Skype or some other application; but to also have instantaneous access to the WWW and unfathomable amounts of information. Today, CSPs are a vital part of these products and have enabled and changed the tools and handheld "appliances" of our daily lives.

Since the first consumer electronic product was introduced, the challenge has been to fit more into the same space to enable increased functionality. One of the first commercial products that widely used CSPs was the Sony DCR-PC7 handycam; that product had more than 20 CSPs,³ (**Figure 1**) shows the main board used in the camera and the density is clear. Back

then, the challenge for socket makers was size, and a variety of new contact technologies were developed.

Today, more than a decade later the challenges remain the same: How can we design and make reliable sockets for finer pitches at reasonable cost that enable the testing and qualification of new packages? **Figure 2** shows the front and back of the main board in the iPhone 4. The packages are crammed onto a 10*2cm double sided board to allow space for the battery, touch screen and audio chambers. The complete teardown of the iPhone and other consumer products is available on the ifixit web site.⁴ As with all things, there are significant challenges behind that simple statement and the design engineers at socket companies struggle with how to establish a reliable mechanical and electrical interconnect. So how have the challenges changed? This article will attempt to show some of the latest challenges and describe how we are looking at these problems.

Chip Scale Packages

Early attempts to define a CSP included a definition of its size as a percentage of the silicon size, but this definition was not broadly accepted and chip scale has

come to mean a package that is minimally packaged. The major challenges for socket builders today are pitch – less than 0.4mm, large package size and high I/O counts, small packages, mixed pitches, and irregular/non uniform package sizes. Each one of these is being addressed.

Pitches less than 0.4mm

As pitch has been reduced new contact designs and technologies have been developed. 0.75mm BGA packages saw the development of the dual pinch contact since it did not touch the bottom of the solder ball. These early sockets were typically thru-hole sockets, but as pitches fell to 0.5mm and socket and board costs increased, socket purchasers demanded ease of replacement and reparability. This drove the development and acceptance of compression mount sockets, which are now the accepted interconnect method to the burn-in board.

Pitches at 0.4mm for conventional peripheral leaded packages such as QFP have been available for some time in a thru-hole format, and use a fan-out approach to change the pitch on the burn-in board. 0.4mm area-array packages, such as BGAs, initially presented a significant

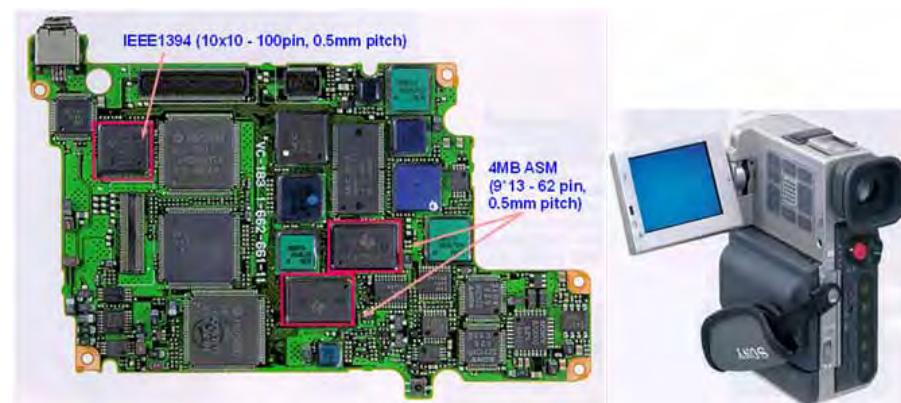


Figure 1: The Sony Handycam DCR-PC7 and the main board showing first consumer production application of CSPs.

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challenge due to the costs of burn-in boards at this pitch. Conventional burn-in sockets at 0.4mm pitch using spring pins were manufacturable, but the costs of large burn-in boards were more than 6X the cost of burn-in boards at 0.5mm pitch. This led to the development of fan-out contact sets by all the major suppliers of burn-in sockets. The package pitch of 0.4*0.4mm is fanned out by a laminate contact system to 0.4*0.6mm. These laminate sockets leveraged high-volume processing such as the use of molded parts and typical contact processing technologies to provide cost effective solutions.

Today, the burn-in board PCB technology has advanced and sockets with spring-pin-type contacts are available at 0.4mm, but the cost of the overall solution, socket and board, is higher than a fan-out type socket. For pitches less than 0.4mm, however, there is no widely accepted solution. Socket vendors have solutions that use elastomeric or spring-pin contact systems, but these are expensive and have limited applicability since they do not solve the problem of pitch on the burn-in board.

There has been much discussion about 0.3mm, however it has not seen wide acceptance perhaps because difficulties at the package level and the cost of boards for consumer products. The ITRS packaging update, table AP5 even includes the comment "Pitch limitations are due to cost and potential yield problems with printed

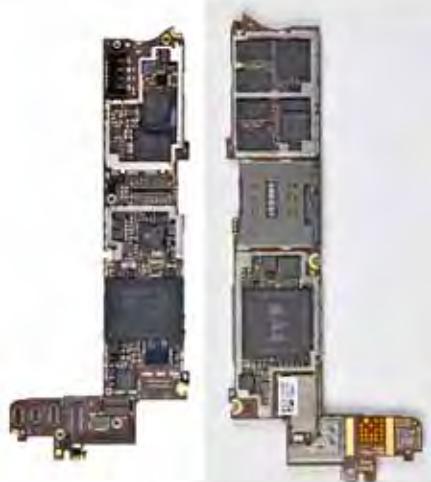


Figure 2: Front and back images of the main board in the iPhone 4. Approx size is 10cm*2cm.

circuit boards. The technology is capable of finer pitch in several of the entries..."

Katahira⁵ and others have provided a detailed summary of the challenges facing the development of 0.3mm packages including IC substrate routing and ball attach. Despite these difficulties, 0.3mm packages are being produced and Brandon Prior of Prismark gave a market update at BiTS Workshop 2011⁶ that forecast the growth of 0.3mm pitch through 2015. Additionally, Brandon's presentation states that sub 0.5mm was only 2% of the overall number of packages in 2008 but will grow to 19% or 11 billion packages by 2015.

Recently, customer interest in solutions has been increasing and it appears that 2012 may be the year for the introduction of the first volume application at 0.3mm pitch. Solutions that leverage the experience from the 0.4mm fan-out solutions are being openly discussed and the major question is what is the fan-out pitch at the burn-in board? One concept is shown in (Figure 3) for a laminate contact set where the 0.3mm*0.3mm package pitch is fanned out to 0.3*0.8mm. The difference between the pitch on the package and the "fanned-out" pitch on the burn-in board is shown in (Figure 4).

The difficulties and costs associated with package manufacturing and integration into end applications has delayed broad acceptance of 0.3mm pitch packages.

Large package size and high I/O counts

As device functionality increases, the number of I/Os increase and 0.4mm packages with I/O counts greater than 1,000 are in production. The impact of these high pin counts drives socket design

options to clamshell-type sockets due to the high forces involved. For example,

at a contact force of 10g, the total force that must be applied to the package is 10,000g, or about 22 lbs., and this is onto a 14mm square package. These forces are challenging when the package pitch is 1mm, but for 0.4mm they become daunting due to the overall size and complexity

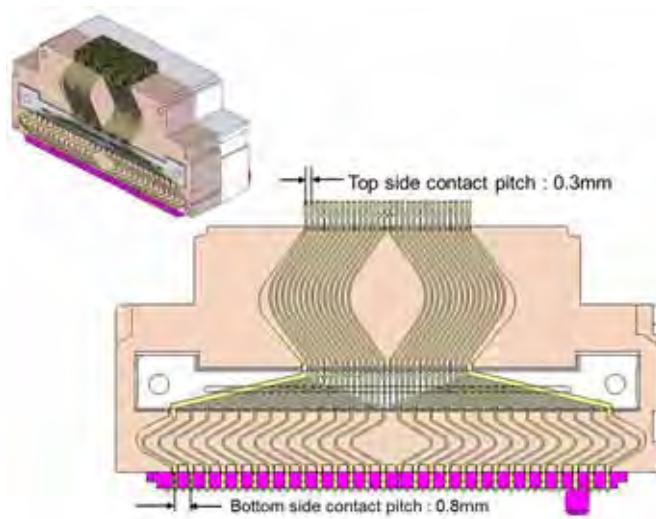


Figure 3: Schematic of a concept for a compression mount fan-out design for 0.3mm pitch CSP packages. The pitch on the BiB could be 0.3*0.8mm

of the socket. Additionally, packages are becoming thinner, and therefore more fragile, and the challenge increases. Force uniformity and distribution is critical if die cracking is to be averted. Now add into the mix a PoP package with I/O on the top surface requiring electrical isolation, and the challenges increase.

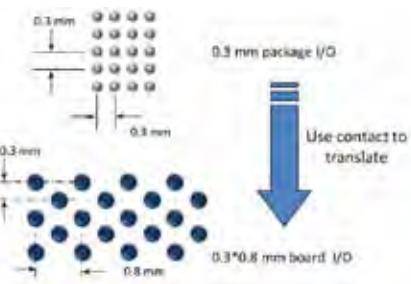


Figure 4: Schematic of fan-out for 0.3mm pitch CSP packages. The pitch on the BiB could be 0.3*0.8mm

Small packages

The original goal of chip scale packages was to reduce the package size — the very name chip scale suggests smaller packages. The comments above focused on smaller pitches and larger packages and

I/O counts. Today the socket designer is being challenged at the other end of the spectrum by extremely small packages such as 1.6mm square with less than 15 I/O. While the force required to press this package onto the contacts is small, the package is barely visible without a microscope, yet the design engineer must develop a socket which accurately locates this package and then forces it onto the contacts.

These force problems — very light for small packages and very high for large packages — are not experienced during assembly into the finished product since the solder is simply reflowed; it is only during test and burn-in when a socket must provide that “temporary electrical interconnection” that the designer has to resolve these difficulties.

Mixed pitches

0.4mm packages appeared in 2002/2003 and today a variety of socket solutions are available. These packages have a conventional simple uniform array 0.4*0.4mm pitch. As bus speeds and device frequencies increase, semiconductor packaging engineers must explore ways to meet the I/O challenge and satisfy signal integrity requirements. This has led to packages with mixed pitches – where specific I/O’s are not on the 0.4 array. This means that the laminate approach is not feasible and alternate solutions must be found. The design exercise is not difficult but can be challenging from a cost perspective since the socket design for these CSP’s is custom because of the specific device size.

Figure 5 shows 2 packages that are very different but are both considered CSPs. One is less than 2mm square while the other is 14mm square with 980 I/O. Interestingly the larger package is more fragile due to the forces it will see when loaded into the socket.

Irregular/non uniform package sizes

Because the size of CSPs can be dictated by the die size, the socket manufacturer must be capable of handling these variations. Tolerances on the “locator” for the alignment and the method of alignment become critical. In many

instances the package cannot be accurately aligned from the edges, so the edges provide an initial alignment and then the socket features use the solder balls for fine alignment of the device to the contacts. Each supplier has a preferred approach, but this is a critical feature to ensure that the interconnect is reliable over the range of burn-in temperatures and times. Failure here can result in damaged solder balls.

Summary

Today’s chip packaging is, and will continue to be, driven by consumer electronics. Integrated handheld appliances incorporate the functions of a number of separate devices that were introduced and state-of-the art just a few years ago. Device packaging proves “it’s a small world after all” and to the horror and dismay of those in the socket industry it continues to get smaller. The major challenge continues to be pitch, and with PoP packages here and through silicon vias (TSVs) on the horizon, the potential for smaller pitches is clear. Add increasing I/O count and current carrying requirements and thermal issues will become more important.

The techniques for fine pitch interconnect are not new, the challenge is integrating those techniques into a cost effective burn-in socket that enables the industry to continue to provide reliable products that delight and excite the consumer.

There is no telling what’s on the horizon, but rest assured that innovative design and interconnect technologies to provide cost effective burn-in sockets will be required to meet these challenges. 

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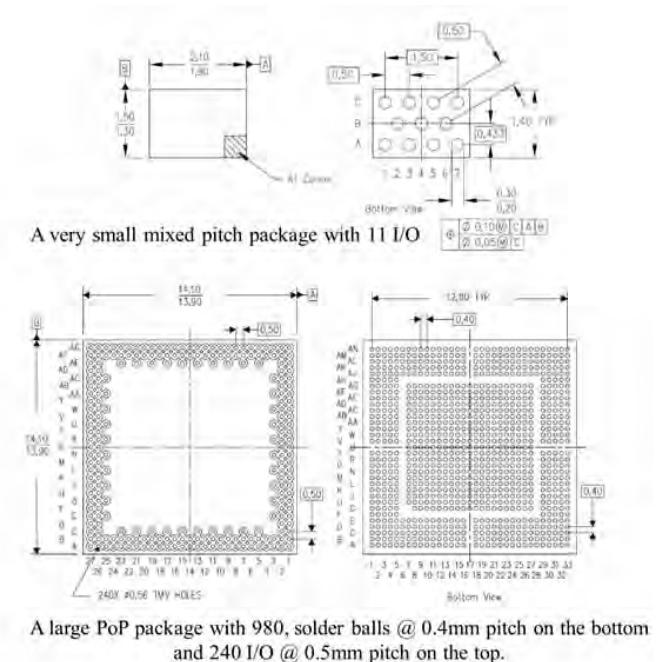


Figure 5: The extremes of very large and very small; package drawings showing the range of 0.4mm packages which must be accommodated.

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Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to +260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to +125°C FQ < 30 GHz CF & CR = CM
Andon Electronics Corporation 4 Court Drive Lincoln, RI 02865 Tel: +1-401-333-0388 www.andonselect.com	P	BA, LA, SM, TH	CP > 1.0 mm CL & FQ = CM OT = -65°C to +240°C CF = CM CR < 1.0 A
AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 4 Merrill Industrial Drive Hampton Beach, NH 03842 Tel: +1-603-926-2517 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
Aries Electronics, Inc.  2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to 155°C CL, FQ, CF & CR = CM
BeCe Pte. Ltd. Block 1, Yishun Street 23, # 01-09 Singapore 768441 Tel: +65-6257-2930 www.bece.com.sg	T	BA, LA	CP = CM CL = CM OT = CM FQ = CM CF = CM CR = CM
Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
Centipede Systems Inc. 41 Daggett Drive San Jose, CA 95134 Tel: +1-408-321-8201 www.centipedesystems.com	T	BA, LA, SM	CP > 0.3 mm CL > 500,000x OT < +160°C FQ = CM CF = CM CR < 2.0 A @ 150°C

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Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com	B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A
Custom Interconnects 2055 S. Raritan Street, Unit A Denver, CO 80223 Tel: +1-303-934-6600 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz CF = CM CR < 5.0 A
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com	B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Enplas Tesco, Inc. 765 N. Mary Avenue Sunnyvale, CA 94085 Tel: +1-408-749-8124 www.enplas-ets.com	B, D, T	BA, LA, SM	CP > 0.4 mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14 - 35) g CR < (0.5 - 1.0) A
Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3 mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30 GHz @ -1dB CF < (15 - 40) g CR < (0.5 - 1.0) A
E-tec Interconnect Ltd. Industrial Zone C Forel (Lavaux) CH-1072, Switzerland Tel: +41-21-781-0810 www.e-tec.com	D, P	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (100 - 1,000k)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40 g CR < (0.5 - 3.0) A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4 mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40 GHz @ CM CF < (10 - 12) g CR = CM
Gold Technologies, Inc. 2360-F Qume Drive San Jose, CA 95131 Tel: +1-408-321-9568 www.goldtec.com	B, D, T	CM	CP > (0.4 - 0.5) mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6 - 16.0) GHz @ -1dB CF & CR = CM
High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > (0.5 - 0.8) mm CL > (50k - 250k)x FQ < (4.4 - 10) GHz @ -1dB CF < (30 - 50) g OT & CR = CM
High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5 mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0 A

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Interconnect Devices, Inc. 5101 Richland Avenue Kansas City, KS 66106 Tel: +1-913-342-5544 www.idinet.com/synergetix	 D, T	BA, BD, LA, SM	CP > (0.4 - 0.5) mm CL > (250k - 500k)x OT = -55°C to +150°C FQ < (9.6 - 20) GHz @ -1dB CF < (17 - 85) g CR < (1.5 - 5.0) A
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	 P	BA, LA	CP > 0.8 mm CR < 10 A CL, OT, FQ, CF = CM
Ironwood Electronics 11351 Rupp Drive Burnsville, MN 55337 Tel: +1-952-229-8200 www.ironwoodelectronics.com	 Ironwood ELECTRONICS B, D, T	BA, LA, SM	CP > (0.25 - 0.4) mm CL > (2k - 500k)x OT = -70°C to +200°C FQ < (6 - 40) GHz @ -1dB CF < 50 g CR < (2.0 - 8.0) A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
JF Technology Berhad (747681-H) Lot 6, Jalan Teknologi 3/6, Taman Sains Selangor 1, Kota Damansara, 47810 Petaling Jaya, Selangor D.E. Malaysia www.jftech.com.my	B, D, P, T	BA, BD, LA, SM	CP ≥ 0.3mm CL 300K - 1000K OT -40C to 155C FQ -1dB@14GHZ CF 30 Grams CR 4.5 A≥
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (300k - 1,000K)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25 - 0.4) mm CL = CM OT = CM FQ = CM CF = CM CR = CM
M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjc.co.jp	B, D, T	BA, SM	CP > 0.2 mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM

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Company Street Address City, State, Country Telephone Website	B = Burn-in D = Development P = Production T = Test Contactor CM = Contact Mfgr.	BA = Ball Array BD = Bare Die LA = Leadless Array SM = Surface Mount TH = Through Hole	CP = Contact Pitch CL = Contact Life OT = Op. Temp. Range FQ = Frequency (Ins. Loss) CF = Contact Force / Pin CR = Current Rating / Pin
Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25 - 50) g CR < (1.0 - 3.0) A
Modus Test LLC P.O. Box 56708 Atlanta, GA 31156 Tel: +1-678-765-7775 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3 mm CL > 1,000,000x OT = +200°C Max. FQ < 20 GHz @ CM CF < 35 g CR < 5.0 A
Multitest Elektronische Systeme GmbH Aeussere Oberaustrasse 4 D-83026 Rosenheim, Germany Tel: +49-8031-4060 www.multitest.com	D, T	BA, LA, SM	CP > (0.25 - 0.5) mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5 - 40) GHz @ CM CF < (26 - 55) g CR < (1.8 - 4.6) A
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong,Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0 - 12.4) GHz @ -1dB CF < (7 - 15) g CR < (0.5 - 1.0) A
Paricon Technologies Corporation 421 Currant Road Fall River, MA 02720 Tel: +1-508-676-6888 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1 - 0.4) mm CL > 1,000,000x OT < 150°C FQ < 40 GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtst.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 1,000,000x OT = -50°C to +150°C FQ > 40 GHz @ -1dB CF = 20-45 g CR > 3.5 A
Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
ProFab Technology Inc. 41817 Albrae Street Fremont, CA 94538 Tel: +1-925-600-0770 www.profabtechnology.com	D, T	BA, LA	CP > (0.26 - 0.45) mm CR < 7.0 A CL, OT, FQ & CF = CM
Protos Electronics 1040 Di Giullio Avenue, Ste. 100 Santa Clara, CA 95050 Tel: +1-408-492-9228 www.protoelectronics.com	D, T	BA, LA, SM	CP = CM CL > 300,000x OT = -55°C to +135°C FQ < 22.3 GHz @ -1dB CF < 20.8 g CR < 4.0 A
Qualmax, Inc. IT Castle, 1-dong, 1101-ho 550-1 Gasan-dong, Geumcheong-gu Seoul, Korea 153-768 Tel: +82-2-2082-6770 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5) mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0 - 4.0) A

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R&D Interconnect Solutions 7115 Northland Terrace, Suite 400 Brooklyn Park, MN 55428 Tel: 763-367-7800 www.rdis.com	D, P, T	BA, BD, LA, SM	CP <0.3mm CL = 150,000x OT = -40° to 150°C FQ > 38Ghz @ -1dB CF = 15g CR = 4A
Rika Denshi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36 GHz @ -1dB CF < (15 - 30) g CP & CR = CM
Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0 A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35 mm OT = -55°C to +150°C FQ < (9 - 10) GHz @ CM CR < (1.0 - 15.0) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Avenue, Suite 100 San Jose, CA 95120 Tel: +1-408-269-2800 www.sanyu-usa.com	CM	CM	CP > 0.2 mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15 - 25) g CR < (4.0 - 5.0) A
Sensata Technologies, Inc. 529 Pleasant Street, P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10 - 25) g CR < 1.0 A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3 - 0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5- 20) GHz @ CM CF & CR = CM
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3 Bayan Lepas, Penang 11900, Malaysia Tel: +60-4-646-6966 www.tts-grp.com	D, T	BA, LA, SM, TH	CP > 0.2 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 20 GHz @ -1dB CF & CR = CM
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: +1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5 - 1.0) A
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com	D, T	SM	CP > 0.4 mm OT = -40°C to +150°C FQ < (6 - 8) GHz @ CM CL, CF & CR = CM

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Wells-CTI 2102 W. Quail Avenue, Ste. 2 Phoenix, AZ 85027 Tel: +1-480-682-6100 www.wellscti.com	B	BA, LA, SM, TH	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (8 - 80) g CR < (0.5 - 2.0) A
WinWay Technology Co. Ltd. 2F, No. 315, Minghua Road, Gushan District Kaohsiung 804, Taiwan Tel: +886-7-552-4599 www.winway.com.tw	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > (50k - 500k)x OT = -50°C to +150°C FQ < (0.2 - 14) GHz @ -1dB CF < (10 - 41.3) g CR < (1.5 - 3.0) A
Yamaichi Electronics Co., Ltd. 3-28-7 Nakamagome, Ota-Ku Tokyo 143-8515, Japan Tel: +81-3-3778-6111 www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4 mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM

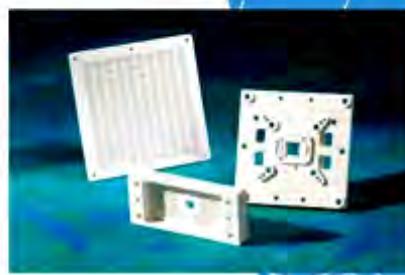
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Study of Solder-Cu Failure Modes with Thermal Aging Stress as a Function of Plating Process Conditions

By Darren Moore [Fairchild Semiconductor]

Use of copper as the under bump metal (UBM) of tin solder joints is now standard industry practice.¹⁻³ Critically important is the intermetallic compound (IMC) formed between Cu and solder material.⁴ Factors that are known to reduce IMC strength include the type of IMC formed, its thickness, and presence of voiding (referred to as Kirkendall voiding).⁵⁻⁷ This joint is known to degrade under typical field operation conditions (on-off cycling and drop impact), and several publications have shown the link between voiding and reduced drop test reliability.⁷ Although drop and thermal cycling tests are the industry standard for solder ball-UBM strength and reliability determination, techniques such as iso-thermal aging and shear analysis continue to be used due to their low cost and ease-of-use.

This article describes the failure modes of joints formed between Cu and a SAC lead-free solder, examined as a response to the quality of UBM copper used. Thermal aging is used to accelerate joint degradation, shown through IMC growth and voiding as measured by SEM analysis. This in turn is related to shear energy. Variations in the copper plating conditions of current density, pulse frequency and duty cycle will be shown to affect the type of failure mode and shear energy. Failure modes are discussed (determined by optical and SEM imaging) and related to pre- and post-shear SEM analysis. Different failure modes are presented, brought on by changes in the IMC layer, its growth, and voiding. The analysis shows that the copper-solder failure mode is a consequence of the thickness of brittle IMC and presence of voiding, and these in turn can be controlled by Cu plating process conditions.

Experimental

Short loop 5x5 daisy chain wafers with oxide substrate were prepared by barrier/seed (Ti/Cu) deposition followed by patterning using a positive tone resist to form 100µm openings. Cu electrodeposition was performed in a ‘vertical’ bath, using a high concentration copper sulphate solution under forward pulse conditions. Low and high current density splits were targeted to achieve plate rates of 1µm min⁻¹ and 1.6µm min⁻¹ respectively. Initially, three forward pulse processes were examined (low, medium & high), with T_{off} conditions set correspondingly to ensure a constant duty cycle. Follow-on work varied the duty cycle used with a fixed pulse. **Table 1** summarizes all process conditions studied.

Target Cu thickness of 10µm was followed by resist strip and barrier/seed etch. A 10µm polyimide coat was patterned before flux clean and solder bumping with 300µm lead-free tin alloy. Reflow at a peak temp of 217°C and 50s completed the process. The top left illustration of **Figure 1** shows the simplified bump structure after WLCSP processing. After reflow, the samples were thermally aged at 165°C for 120hrs and 240hrs. SEM and shear analysis were carried out post reflow and after thermal aging. SEM analysis was used to investigate IMC thickness and composition. Shear measurements were performed at 500 mm/sec, with a 50µm shear height, using a Dage 4000 microtester. This speed was chosen to give pad failures exhibiting approximately

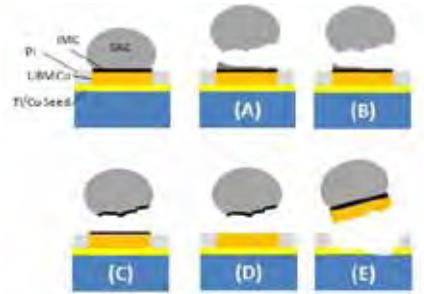


Figure 1: Illustration of possible shear failure modes.

50:50 brittle and ductile fracture, for POR reflowed conditions.

Possible shear failure modes identified are illustrated in (**Figure 1**). These are:

- (a) *Through solder (full ductile)* – this is the preferred mode of failure, yielding highest shear energy
- (b) *Through IMC & solder (quasi-ductile)* – through solder failure, along with IMC-solder failure.
- (c) *Through IMC layer (brittle)* – failure within the IMC region, usually due to build up of a voided ‘seam’.
- (d) *IMC-Cu interface (brittle)* – failure below the IMC region, at the IMC-Cu interface
- (e) *Pad lift (brittle)* – removal of the solder, IMC and Cu UBM.

Most shear failure modes were determined to be a combination of several of the above options. Ideal strength

		Frequency		
		Low	Medium	High
Current Density	Low (1 µm min ⁻¹)	Y	Y	Y
	High (1.6 µm min ⁻¹)	Y	Y	Y

Duty Cycle				
		0.66	0.8	Direct Current
Current Density	Low (1 µm min ⁻¹)	Y	Y	Y
	High (1.6 µm min ⁻¹)			

Table 1: Summary of current density, pulse frequency & duty cycle conditions examined.

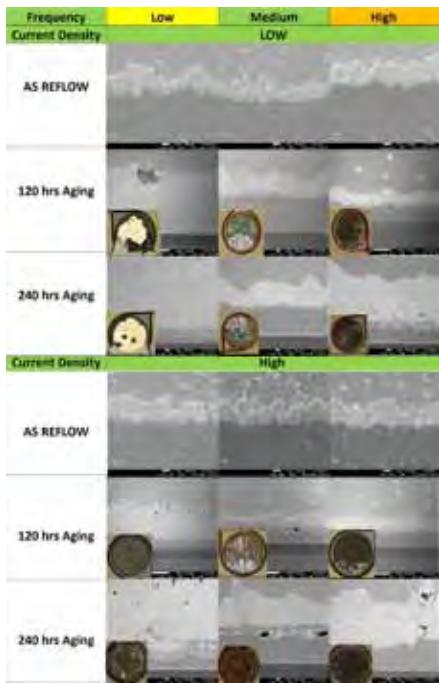


Figure 2: SEM images of current density & pulse frequency splits for samples as reflow and aged to 120 & 240hrs

between the Cu pad, IMC and solder will result in the weak point being through solder ductile cleave.

Pulse Frequency and Current Density Variations

SEM analysis of these six process conditions are shown in (Figure 2) as reflowed, post 120 and 240hr thermal aging. These are the low and high current density processes at low, medium and high pulse frequency. Included are the post-shear optical images to show type of failure.

Low frequency conditions show substantial growth of Cu_6Sn_5 IMC at both low and high current density. The low current split shows total consumption of UBM copper and brittle pad delamination with shear testing. The corresponding high current density process has remaining Cu, and due to a build-up of voids, through IMC mode failure. The optical images show the copper seed layer remaining with pad lift for low current. High current shows a grey roughened IMC surface. High frequency conditions also show extensive, but less, Cu_6Sn_5 growth and voiding with thermal aging. Shear failure is predominantly through IMC or at

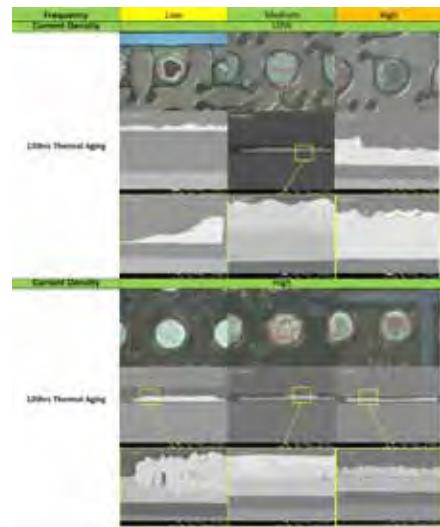


Figure 4: Post-shear SEM images of low & high current density samples aged to 120hrs.

the IMC-Cu interface. The grey area is indicative of remaining IMC, while the orange regions are plated Cu UBM, exposed due to IMC – Cu failure.

Mid frequency conditions show overall best results. Here, limited IMC growth and lack of voiding result in quasi-ductile solder-IMC failure. However, even at these

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optimized frequency conditions, increased current induces void growth with thermal stress. The IMC-Cu voiding that occurs under these high current conditions shows the shear failure at this interface. Shear fracture energies have been shown to correlate to failure mode with higher energies being due to ductile failures. Shear results for this work (**Figure 3**) show a substantial reduction with aging for the high and low frequency conditions; a consequence of the weak IMC region due to its thickness and voiding. Optimized processes still show an energy reduction due to IMC growth with aging.

These failure modes are confirmed with additional post-shear cross sectional SEM analysis (**Figure 4**) for samples aged to 120hrs. Comparison with optical images shows the variation in failure modes that can occur. Location of the shear fracture is not restricted to one region, but can occur at any of the interfaces (Cn-IMC, within IMC or IMC-Cu). This is driven by the location of void growth and build-up of a ‘void seam’. In general, the Cu₃-Sn interface is the preferred location of void agglomeration; however low frequency processes show some occurrence of growth at the Cu₆Sn₅ layer. They show the occurrence of IMC voiding is not relegated to one region, but can occur at the Sn-IMC, within IMC, or IMC-Cu interfaces, resulting in failure at one or more of these regions within the same sample. These failure modes

previously described are summarized in (**Table 2**).

Duty Cycle Variations

Duty cycle (DC) in pulse plating is defined as the pulse time on divided by total time (Ton+Toff). The higher the duty cycle the more current on time, until at the extreme Toff=0 and the process becomes direct current. The optimized frequency (‘medium’ from previous section) at low current density and a duty cycle of 0.66 was compared to the copper processes plated at DC= 0.8 DC=∞ (direct current) (**Figure 5**).

Although as reflowed shows the typical ‘scallop’ Cu₆Sn₅ in all cases, differences again become apparent with aging. Worst case scenario is the direct current (non-pulsed) condition, where severe voiding resulted in negligible shear testing results at 120hrs, with failure occurring at the IMC-Cu interface. Introduction of a Toff cycle and lowering of DC to 0.8, substantially reduced void occurrence.

		Frequency		
		Low	Medium	High
Current Density	Low	Pad Lift	Solder & IMC failure	Through IMC failure
	High	Sn-IMC failure	IMC-Cu failure	Sn-IMC & IMC-Cu failure

Table 2: Summary of failure modes identified.

In both these cases, the void seam starts to appear within or on top of IMC with thermal again. It appears the more DC-like the pulsed process becomes, the more likely this is to occur. This is compounded with substantial IMC

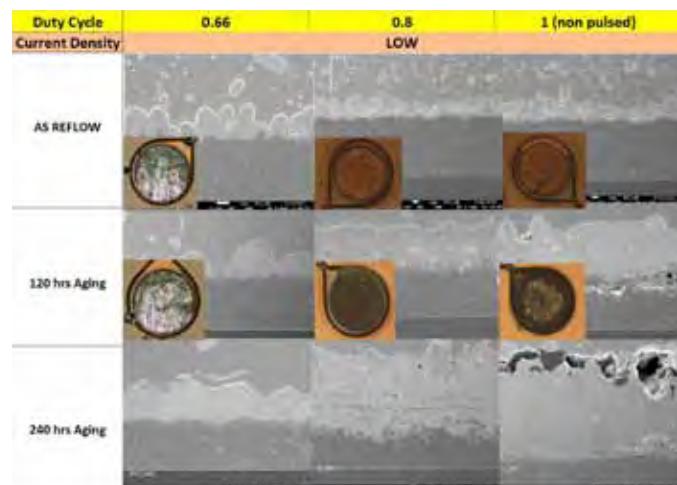


Figure 5:

growth, both of which lead to critically low shear energies and joint reliability.

Conclusion

Optimization of UBM-solder ball reliability is paramount to chip scale packaging. The obvious factors that affect joint integrity include the manufacturing conditions of ball composition and reflow temperature.

The copper plating process operates by biasing the substrate, resulting in a negatively charged layer around the wafer (cathode). This stagnant diffusion boundary layer is named as such as the dominant mechanism for ion (Cu²⁺) movement is diffusion (over convection and migration). Under direct current plating conditions, this layer charges to a defined thickness, Cu²⁺ ions within this layer are driven to the wafer surface and depleted to be replenished by ion diffusion from the bulk solution. With pulse plating, the Toff cycle allows Cu²⁺ replenishment of the region next to the cathode. The time and proportion of Ton and Toff used are

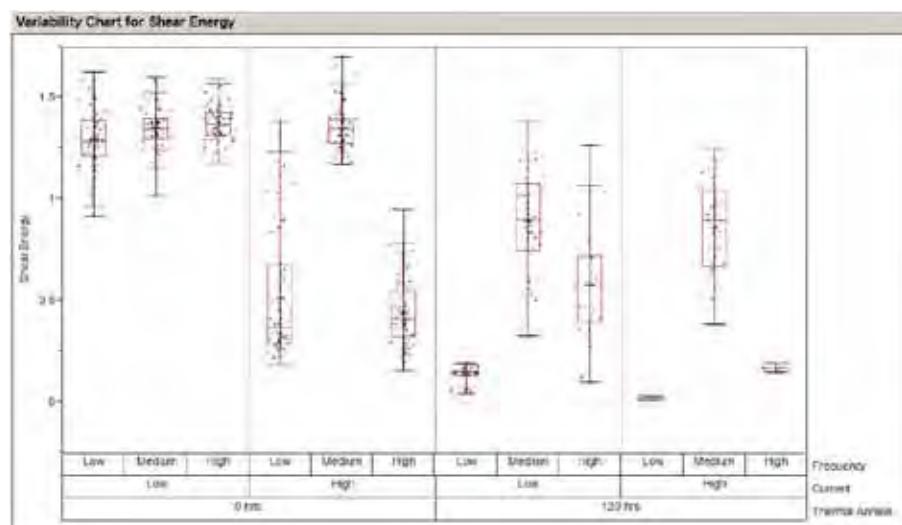


Figure 3: Shear energies of current density & pulse frequency splits for samples as reflow and aged to 120hrs.

critical. Too fast a frequency (or short a Ton) will not allow diffusion to replenish, while too slow (or long Ton) will result in depletion of the boundary layer. Along with copper deposition, grain sizes and incorporation of carbon are also affected by pulse and current conditions.⁸ Carbon incorporation from bath additives is known to be a major factor in the formation of Kirkendall voiding. Increasing carbon incorporation that is concentrated along the grain boundaries can act as a nucleation site for void growth. Build-up of these coalesced voids along an IMC interface occurs as the copper UBM is thermally aged and consumed in IMC formation. A balance is needed to deposit copper that will yield a stable solder joint.

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- Darren Moore, Process Development Engineer, Fairchild Semiconductor, may be contacted at darren.moore@fairchildsemi.com*


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INTERVIEW

Scanning Acoustic Microscopy in Your F/A or Q/A Lab: Yes or No?

By Chip Scale Review Staff



Today, scanning acoustic microscopy (SAM) is a common tool in many failure analysis and quality assurance labs, and more recently has found a home on the production floor. The question is whether the initial cost of the equipment, approximately \$160,000 with transducers, along with the operational learning curve required, provides an appropriate nondestructive testing tool for the F/A or Q/A lab. *Chip Scale Review* spoke with Michael Kearney, SAM Application Engineering Consultant, about this.

CSR: First of all, what is the SAM principle and how does the SAM work?

Kearney: Basically, SAM works on the following principle. When an electrical pulse is applied to a piezo-electric crystal of a specific thickness, the crystal will transmit a sound wave of a specific frequency. This sound wave is then transmitted through a focused lens in water to produce a very finely focused ultrasonic beam point at a specific distance into material of specific density and thickness. The normal frequencies used to inspect microelectronic type packages range from 15MHz to over 200MHz. When the sound is transmitted into a material or multi-level materials of various densities, the sound is reflected back to the transducer and is turned into a pulsed electronic signal that is used to display the returning R/F signals in a time and amplitude raster scan producing a 2D presentation image of the C-SCAN sample.

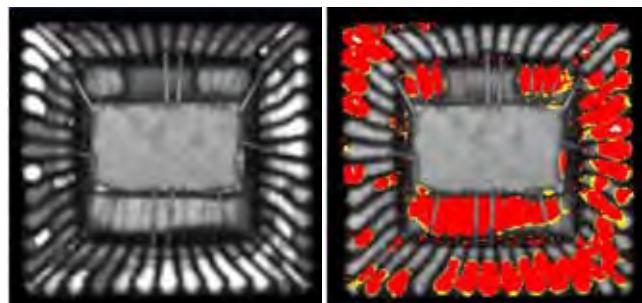


Figure 1: The PLCC scan was taken using a 15MHz transducer. On very thin plastic package such as a TSOP, transducer frequencies up to 75 MHz will be used. (Images courtesy: OKOS Solutions, LLC.)

CSR: How much training is required for the typical F/A or Q/A engineer to become proficient in the system operation?

Kearney: Well, some say that operating a SAM is “an art not a science”, but the same statement can be applied to most of the tools in a typical F/A or Q/A lab. For an engineer to learn the fundamentals of the SAM scanning process on microelectronic packages, it will take anywhere from 40 to 60 hours, which may be spread over an available working time frame. The system operator will actually develop his or her skills over a period of time working with the differing type of packages. The SAM system manufacturers or independent SAM consulting firm like mine can play a major part in training the system operator in developing the necessary skills to maximize scan techniques for varying packages and any detectable discontinuities.

CSR: What do you mean when you say the SAM is a nondestructive testing tool and what can it really do for you?

Kearney: A prime advantage of using SAM in the F/A or Q/A environment is the fact that it is truly performing a nondestructive inspection. The ultrasonic sound waves cause no harm to any microelectronic package. This means that a package can be inspected during the design stages, preproduction stages, or production stages and even during actual application services when necessary. The SAM can provide discontinuity information during and after thermal or non-thermal cycling during any of these periods, up to and including (if necessary), during a package recall from the field.

CSR: What are the applications for this tool?

Kearney: That’s one of the great things about SAM. It’s a very diverse tool and has a long list of applications such as:

- Acoustic Microscope Inspection Capabilities
- Delamination in single packages
- Detecting voids in packages while in JEDEC trays
- Die cracks
- Solder bump defects in stacked die
- Thickness measurements of components in plastic packages
- De-bonds in multi-chip modules
- Sub-surface defects in flip chip packages
- Die-attach issues in wafers
- Counterfeit detection
- Mold compound cure rates and density changes

CSR: Can you provide some specific examples in detail of these applications?

Kearney: Lets begin with detection of delaminations and die-attach problems in plastic PLCC to TSOP type packaging. In (Figure 1), the image on the left was made using amplitude date from the wave form only. The image on the right was made by noting the phase inversion of the wave form caused by the low density reflection in the bad bond area.

Next we'll look at die-attach, mold compound density and ball bond cracking in single or multi layer flip chip packaging or stacked die.

Figures 2a and b were generated in a single scan using a 120MHz transducer. The full scan of this stacked die shows a large (brighter) area that is delaminated at a specific depth. The zoomed corner of this same scan showing a bright spot in the actual solder ball is either a poor bond between the ball and the substrate circuit or a crack in the actual solder ball. These solder balls are actually 100 μ m in diameter. Solder balls as small as 20 μ m are easily detectable and can be scanned using a 200 MHz highly focused transducer.

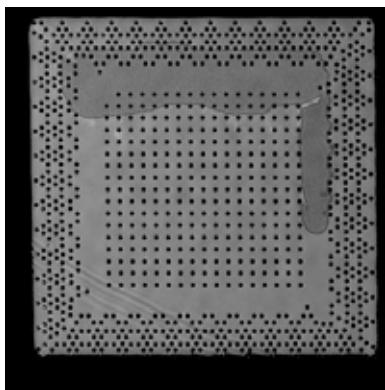


Figure 2: Full view of the “multi layer flip chip” showing a major delamination between layers 5 and 6.

CSR: What are the features of a good Scanning Acoustic Microscope (SAM)?

Kearney: There are features to look for when selecting a good SAM. First and foremost is detectability of various package discontinuities (delaminations, die cracks, compound under fill voids, etc.) in microelectronic packages. Ease of use is also critical. Next, the SAM should have flexible and powerful quantitative analysis software tools for discontinuity location and measurement (such as cluster analysis for incremental change capture during stress testing cycles for percent measurement of bond or increase in delamination area). Lastly, flexible software allowing for simple go/no go for packages in JEDEC trays such as package location and other detailed failure analysis information is an important feature.

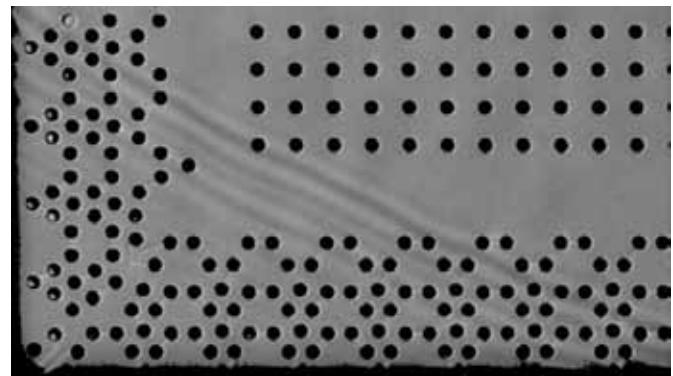


Figure 3: Zooming in on the upper left corner of the same “multi layer flip chip” showing 100 μ m solder balls, some (note small white area) have cracks or bad bonds.

CSR: Since SAM and X-ray are nondestructive testing system, is there an advantage to using a SAM system over an X-ray system?

Kearney: In reality, these two systems are complimentary in nature. X-ray likes discontinuities that are parallel to the X-ray beam and show sharp changes in contrast such as vertical cracks and circuit wiring breaks. SAM likes discontinuities that are perpendicular to the sound beam and have good reflectability, such as delaminations, die attach bond and solder ball cracks. Which system comes first is a matter for internal lab discussions. Personally, I am biased toward SAM as I think it is a more versatile tool. You have to ask yourself the question, is a SAM right for your lab?

Michael Kearney, SAM Application Engineering Consultant, may be contacted at mkearney@OKOS.com.

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GUEST EDITORIAL

New Business Strategy Lowers Risk for Novel Process Technology Adoption

By Diederik Verkest, *[imec]*

Joint research and development (R&D) is the most secure way to develop solutions with next-generation technologies. Take imec's process technology programs for example, which allows partners to do precompetitive R&D together with a group of other technology leaders including major IDMs, materials, and equipment suppliers. These programs are a great way to share the risks and costs of advanced research. But in recent years, a growing interest from fabless and fablite companies has emerged. These companies invest less in fabs and fab technology but concentrate on designing solutions and applications. Still, the designers of these fabless and fablite companies need to know which technologies will become available and how they can use them to their advantage. They have to choose between all the technical options that are (or are becoming) available for lithography, patterning, interconnects, packaging etc. But how can they assess the impact of these options on the product roadmaps they have in mind, as they have no direct access to technology R&D? Will the implementation of the new options impact the way they do circuit, layout, or architecture design?

INSITE – designing with future technologies

Enter imec's INSITE program, which allows product designers to make informed decisions regarding the impact of emerging process technology options on their products. Through participation in this program, companies can anticipate new technologies to design more advanced systems and applications and bring them to market

faster. In reverse, the program supports technology developers in deciding which options make more sense for certain product scenarios. It helps them to assess how product requirements influence technology options at very early stages of technology development. In other words, the INSITE program creates a platform that connects the technology community and the design community, and also supports the co-exploration of design and technology options between all the players in the ecosystem.

INSITE – the approach

The backbone of INSITE activity is the combined development of test chips, models, libraries and path-finding techniques (Figure 1). Together with core CMOS partners, imec develops new technology options, such as 3D through-Si via(TSV) technology, devices for 20nm and 14nm technology, advanced immersion and EUV lithography, interconnect technologies etc. With these options, elementary test circuits are built and processed on Si using the institute's 200mm/300mm processing infrastructure. The test circuits allow for characterization of different quantitative aspects of the new technologies and, in a next step, to create models that are implemented in a process design kit (PDK) (Figure 2). A PDK is the industry's standard way of making technology information available to the designer community in standard formats and flows. These pathfinding PDKs incorporate data about technologies that are still under development, enabling partners to build libraries of gates, standard cells etc. with different variations – and build virtual chips. At this level, final

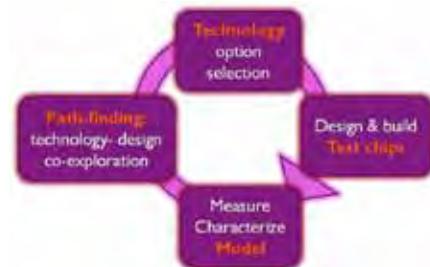


Figure 1: The INSITE framework allows technology research results to be linked with system design opportunities and challenges via a combination of modeling, test chips, libraries and path-finding techniques. evaluation can be performed to asses

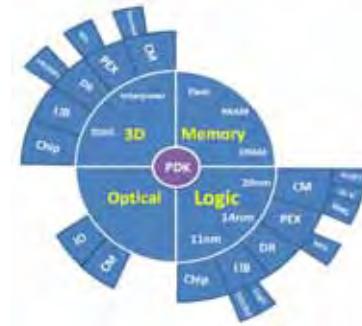


Figure 2: Within the INSITE framework, PDKs are developed for memory, logic, optical and 3D technology options.

whether the designer's targets (area, performance, power, cost) are met, and how different technology options affect these targets. For example, if 2 transistor types are possible for a 20nm technology, then there is a pathfinding PDK with 2 flavors corresponding to those 2 types. The designers can then try out both options in their early designs.

Bringing into practice

Since the launch of the INSITE program two years ago, several use cases have illustrated the effectiveness of this approach. For example, the lithography component of the INSITE program

has delivered pathfinding design flows for assessing patterning options at the circuit level. Additionally, the design rules and models for 3D system-on-chip design have been consolidated, which allows for assessment of the impact of stress on a 3D device's performance. On the logic side, we investigated a.o. logic circuit solutions based on high electron mobility channel devices (III-V). Pathfinding flows allowed participants to assess if they can maintain the same performance as Si CMOS solutions for scaled supply voltages from 1V to 0.5V. Finally, the memory component of INSITE explored different technology options for building e.g. resistive RAM (RRAM) and floating-body RAM (FBRAM) cell arrays.

Among the recent results to be highlighted are findings related to the scalability of SRAM cells – which are excellent vehicles for assessing technology integration. The project started from the observation that the scaling potential of bulk planar SRAM cells is being questioned. While the ITRS roadmap postulates an SRAM area scaling of 55% when going from the 32 to the 20nm node, foundries report a 40% area scaling for a planar SRAM device implementation. The main objective of this project is therefore to assess SRAM cell design scalability by linking design and technology options (in terms of cell architecture and design rules, area trade-offs, device options and VT optimization) to various figures of merit (i.e., area, performance and power, retention and stability). Three different cell architectures were considered: a planar SRAM cell, a UTBox device and a bulk FinFET device. The first part of the approach involved defining a common reference cell architecture in 20nm technology. After that, a symbolic SRAM layout analysis was performed that opens links between litho/technology options and available SRAM design space. This analysis allowed researchers to identify the critical design parameters that limit

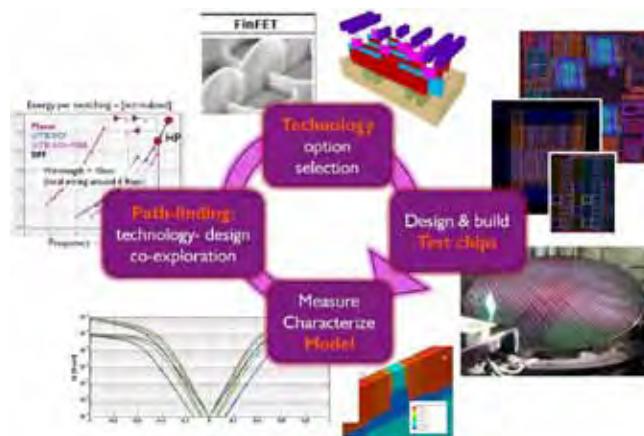


Figure 3: Use case illustrating the INSITE approach: assessing the scalability of SRAM cells.

the cell area. In a final step, figures of allows us to link technology research merit for the various SRAM candidates results to system design opportunities were benchmarked (Figure 3).

One of the main conclusions of this modeling, test chips, libraries and path-INSITE work is that only the bulk finding techniques. The pathfinding FinFET SRAM implementation offers concept is extended to the design level sufficient scalability for pushing SRAM to support co-exploration of technology technology to the next technology and design options. This way, risk node. Moreover, we learned why concerns are addressed early enough to planar SRAM implementations are not allow product teams to assess the impact scaling properly: it's not limited by and potential of the technology options. lithography, but it is related to electrical Complementary, it helps influencing specifications. In order to meet the technology options in a very early stage electrical specifications for the 20nm of technology development, i.e. when node, the planar SRAM device needs to the options can still be influenced. compromise in area, resulting in a loss of 10% area gain. Vice versa, under the *Diederik Verkest, Director of the* same electrical specs, the bulk FinFETINSITE program at imec, can be provides a 30% area benefit and enables contacted at diederik.verkest@imec.be density targets according to the roadmap

(50% scaling). It offers the largest read current per unit area and this excess in read current offers room for improving the leakage current without sacrificing other electrical specifications.

Conclusion

The INSITE framework

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INDUSTRY NEWS

(continued from Page 19)

increase from 595,000 to 792,000 square feet. The new facility is expected to be operational by the fourth quarter of 2012.

Panasonic Factory Solutions Names New President



Panasonic Corporation of North America announced the appointment of M. Faisal Pandit as president of Panasonic Factory Solutions Company of America

(PFSA), effective January 1, 2012. Pandit has been with the company for 20 years in various positions; most recently serving as Director of Solutions, managing the global software organization responsible for product development, sales, deployment, and customer support.

"Faisal Pandit has been a driving force for the expansion of Panasonic's manufacturing execution software across North America as well as overseas markets," remarked Tom Gebhardt, former PFSA President and current Panasonic Automotive Systems Company of America President. "He also spearheaded the concentration of the software business to become US-based, supporting customers worldwide."

Pandit holds a BS from the University of Illinois, MS from the Illinois Institute of Technology, and an MBA from Northwestern's Kellogg School of Management. "I look forward to continuously improving how Panasonic can empower customers to better execute and become more sustainable," stated Pandit.

Koh Young Expands Singapore Facility

Koh Young Technology, supplier of 3D SPI, AOI, and advanced automated inspection equipment for the electronics manufacturing industry worldwide, has relocated and expanded its Singapore sales and service facility to accommodate rapid growth and the need for expanded space.

"Our expanding customer base in the Singapore region is being met with the corresponding expansion of our service and support capabilities, in keeping with Koh Young's ongoing dedication to total customer support," explained Dr. Kwangill Koh, Founder, CEO, and President of Koh Young. He added that the new facility will become the center

of customer support and spare parts supply for Koh Young customers in the Southeast Asia/South Asia/ Pacific regions.

Currently, three (3) direct Koh Young Technology sales and support specialists are based in Singapore and Malaysia, in addition to Koh Young sales and support partners and offices,

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Wafer Thinning and Backmetal Specifications

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Wafer Thickness	>100µm	>100µm	>100µm	>100µm
Metal Type		1) Ti/Ni/Ag 2) Ti/Ni/Au		
Metal Film Thickness	<2µm	<2µm	<2µm	<3µm
TTV	<3µm	<3µm	<5µm	<5µm
Metal Film Non-uniformity	-3%	-3%	-5%	-5%
Exclusion Zone	3mm	3mm	3mm	3mm

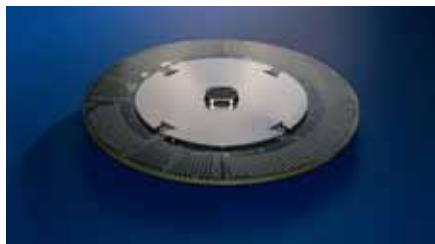


and more than 30 engineering support technicians throughout the region.

Multitest Process Meets Requirements of High Parallel Vertical Probe Card Applications

Multitest, a designer and manufacturer of final test handlers, contactors and load boards, announced that its UltraFlat™ process meets the requirements of high parallel vertical probe card applications.

For applications such as DDR3 memory, the requirements for the flatness of boards at wafer level testing become crucial. For optimizing MLO/MLC attachments and contact element interfaces, a better surface is needed. Additionally, flatter PCBs



Multitest's UltraFlat™ process provides a permanent overall flatness for the PCB

require less compliance from the probe interface and reduce interface wear.

Leveraging the knowledge of PCB stack-up engineering and construction, the company reportedly developed the new "UltraFlat™" process to meet these requirements. The novel process is said to maintain tight overall flatness tolerance by removing the bow/twist in the PCB. Unlike "flat-baking" that provides a temporarily flat PCB, Multitest's UltraFlat™ process

iPhone App Optimizes Heat Sinks

Advanced Thermal Solutions, Inc., (ATS), providers of electronics thermal management solutions, has developed a heat sink design calculator as an iPhone app that identifies the proper heat sinks to solve most component-level cooling issues. The app reportedly allows engineers to input the essential specs and then research online for heat sinks that fit their requirements.

The Heat Sink Design Tool app enables users of Apple's mobile devices to design heat sinks for cooling hot PCB components and other electronic devices. Design parameters that the user can enter include the heat sink material, dimensions and the number and dimensions of the heat spreading fins. When the key heat sink specifications are entered, the ATS app

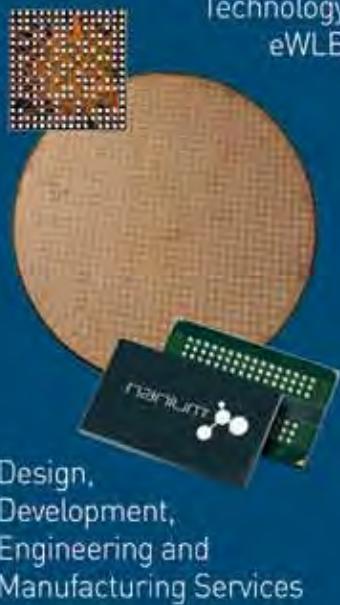
lets users search a number of databases to find if a sink exists that fits or closely matches the entered data. In most situations, a heat sink is available to match the user's needs.

The Heat Sink Design Tool app can be downloaded free from Apple's iTunes App Store. It is compatible with all iPhones, the iPod touch, and the iPad.



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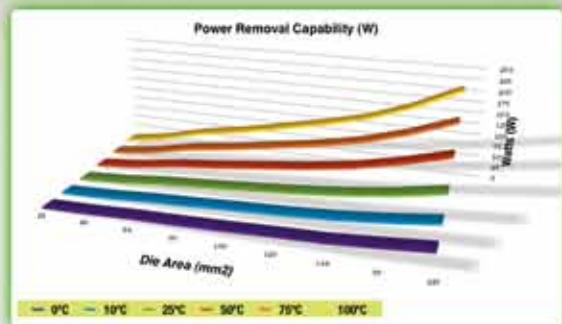
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