

# ChipScale Review®

ChipScaleReview.com

*The Future of Semiconductor Packaging*

Volume 19, Number 2

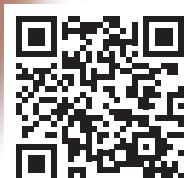
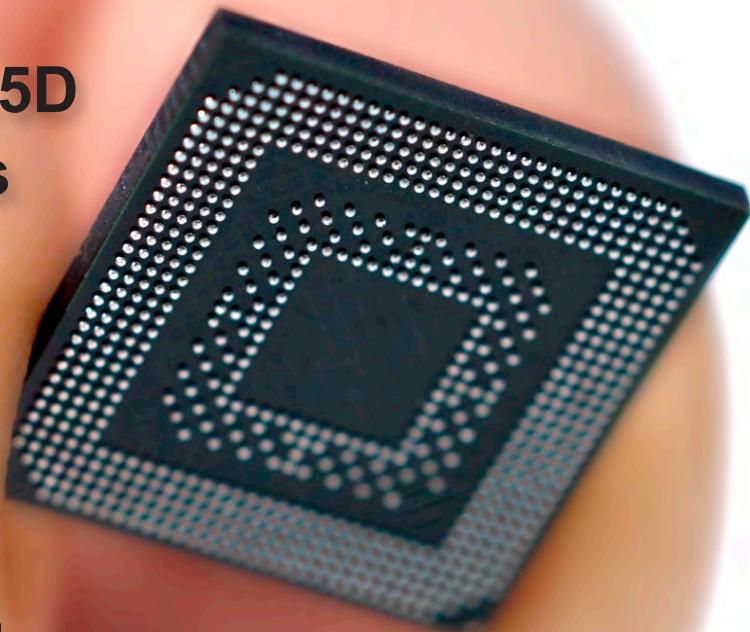
March • April 2015

## Outlook for 3D and 2.5D chips in smartphones

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- RF TSVs for 3D MEMS
- WCSP cost reductions
- Wafer edge inspection for HVM
- Failure analysis at the package level
- RF requirements and spring development

2015 International Directory of IC Packaging Foundries





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A DRAM memory stacked on a logic chip using TSVs and micro-bumps. The micro-bump pitch for the connection of memory-logic is 40 $\mu$ m; the flip-chip bump pitch for the connection of logic-package is 200 $\mu$ m. The stacking was done using thermo-compression bonding and wafer-level applied underfill. The stack was later assembled on the package substrate using mass reflow and capillary underfill. Imec is now assessing similar test vehicles with micro-bump pitch below 5 $\mu$ m and multiple die stacks for 3D and 2.5D technologies.

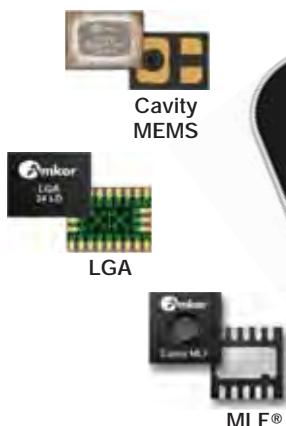
Photo courtesy of imec

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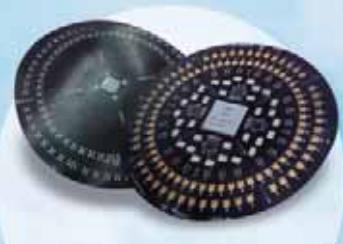
**Logic Test  
Socket**



**RF** Coaxial Spring Probe & Impedance Controlled Socket



Probe Head



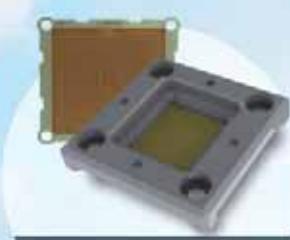
**Wafer Level CSP  
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**Memory  
Socket**



**SLT Socket**



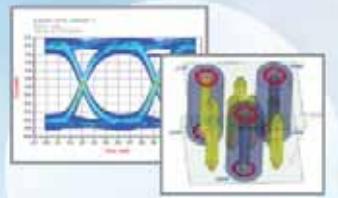
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## IN THIS ISSUE

Welcome to the 2nd edition of *Chip Scale Review* for 2015! In this issue, we cover everything from package design optimization, to failure analysis, inspection, MEMS, test, TSVs, and WLFO. We thank imec – which provides a guest editorial on 3D and 2.5D technologies for smartphones – for the cover photo. The Market Update column was written by several of the industry's leading analysts, who discuss the outlook for OSATs. The issue also contains the updated 2015 International Directory of IC Packaging Foundries.

Our sr. technical editor continues the exclusive Tech Briefs section, which was introduced in the last issue, about recently announced technologies. If your company has a major technology announcement in the areas of advanced semiconductor packaging, TSVs, integration, die-stacking, etc., email the editor at [editor@chipscalereview.com](mailto:editor@chipscalereview.com).

CSR is proud to be a media sponsor of both the MEPTEC MEMS (May 20) and IoT Symposia (May 21). We also continue as the official media sponsor for the 65th ECTC (Electronics Components and Technology Conference) being held May 26-29, 2015.

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# Socket to me, Baby!

## M SERIES H-PIN SOCKET

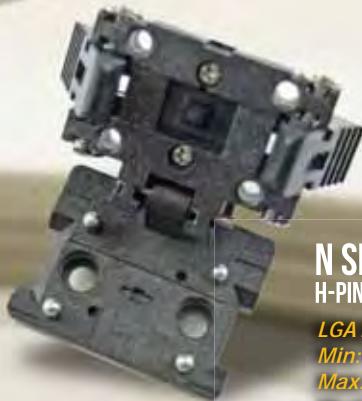
BGA Package size:  
Min: 2mm x 2mm  
Max: 12mm x 12mm

Pin Count:  
576 max



## N SERIES H-PIN SOCKET

LGA Package size:  
Min: 0.50mm x 0.50mm  
Max: 4.0mm x 4.0mm  
Pin Count:  
64 max



## Q SERIES H-PIN SOCKET

BGA Package size:  
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Max: 32.0mm x 32.0mm  
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# MARKET UPDATE

## What does the future hold for OSATs?

CSR asked some of the top industry analysts to provide their views on the status of OSATs and what the future holds for this important segment of the electronics industry.

**T**here are more than 100 companies offering IC assembly and test services, excluding companies that are test houses only. These outsource assembly and test service (OSATs) providers generated revenue of approximately \$22 billion in 2013. The top four OSATs spent more than \$2 billion for capex in 2014, excluding plant construction. A number of industry analysts provided CSR with their thoughts on what the future holds for the OSATs and what changes can be expected.

### Jim Walker, VP Semiconductor Manufacturing Research, Gartner



The OSAT (sometimes called SATS) industry has grown and matured over the last 15 years as both IDMs and fabless companies have adopted the outsourcing business model. It has quadrupled in revenue from 6 billion USD in 1998 to over 25 billion USD in 2013. Over this period, while the foundry market has become dominated by one company (i.e., TSMC) controlling over 50% of the market, there is no such dominance in the back-end packaging and test services market. In 2014, for example, of the more than 150 companies that Gartner has identified in the OSAT market, 37 generated revenue of over 100 million US dollars each and, of these, only five had revenue over one billion USD.

While there is this proliferation of companies that make up the OSAT market, the top OSAT companies have begun to distance themselves from the rest of the pack in the last few years. They are growing faster than the market average, and are taking market share away from other, lower-ranked second- and third-tier

companies. The top companies focus on advanced technologies, including wafer-level packaging and flip-chip, and the emerging TSV market is resulting in increased revenue, as these new packages have higher average selling prices (ASPs). For a few of these top companies, advanced packaging is now approaching nearly half of their total packaging revenue.

As we look forward to the next few years in the OSAT industry, several key factors are emerging that will influence the future of the OSAT landscape. Some of these will include the following:

- 1) Currency depreciation and exchange rates (especially that of Japan against the US dollar) will affect market revenue growth (denominated in US dollars);
- 2) Decreasing package ASPs, which historically have been trending lower by approximately 2 to 5% annually;
- 3) Continued increase in the adoption rate of advanced packaging processes, such as those of WLP, flip-chip, and TSV;
- 4) The convergence of foundry and PCBA manufacturing processes with those of assembly and packaging; and
- 5) The continued divestiture of the IDM packaging factories to the OSAT industry, forcing the necessity of industry consolidation.

### Dan Tracy, Senior Director, Industry Research and Statistics, SEMI



OSAT companies are key players in developing new packaging solutions and ramping those technologies into volume production.

As other analysts have shown, OSATs have grown their share of the overall semiconductor industry's packaging and test manufacturing markets. Corresponding with this is the trend in OSATs spending

a higher percentage of revenues on capex annually. About a decade ago, leading OSAT companies averaged about 15% of revenues spent on capex; in recent years, this percentage has averaged almost 20%, and in some years more than 20%.

In developing and introducing new packaging solutions, OSAT companies have played a prominent role by incorporating new material technologies into packages for improved performance, smaller form factors and lower costs. As an example of reducing material costs, OSATs invested substantial amounts to ramp copper bonding wire technology into production. By eliminating gold wire in many packaging applications, the semiconductor industry has saved billions of dollars in materials cost. OSATs, in partnering with their suppliers and customers, have successfully enabled this important materials transition.

### Bill McClean, President, IC Insights



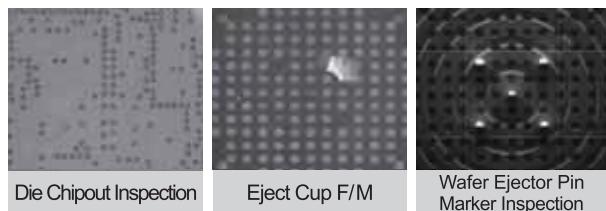
As companies continue to move into a strategy of fabless operation, OSATs play an increasingly important role. Leading assembly and test subcontractors play an increasingly important role in designing the appropriate packaging solution and even introducing new technologies to the industry and their customers. Increasingly, IC suppliers are relying on OSAT companies to design packages and test the final products. In fact, the share of the total worldwide assembly and test market claimed by the OSAT providers remains around 51% compared to just 25% in 2003, and 15% in 1995.

Taiwan-based companies dominate the contract semiconductor packaging

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FOOTPRINT	DIMENSION (Wx Dx H)	1,600mm x 1,230mm x 1,600mm
	WEIGHT	2,600 kg



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and test industry. Half of the top 10 OSAT service providers are Taiwanese companies. Amkor, which is headquartered in the U.S., also has operations in Taiwan. STATS ChipPAC, a Singapore-based business, has sizeable assembly and test operations in Taiwan. It is not by chance that Taiwan is the leading supplier of contract packaging and test services. The country is home to two of the largest foundry operations (TSMC and UMC) and many key package substrate manufacturers.

Merger and acquisition activity among the OSATs is expected to increase in the next few years as the companies continue to consolidate among themselves and acquire more assembly, packaging, and test operations from IC manufacturers looking to get rid of their front-end and/or back-end facilities and outsource those business functions to third parties. Recently, Japanese IC manufacturers have been very active in selling off their back-end operations. For example, in December 2012, Fujitsu sold almost all of its back-end facilities to J-Devices (Nantong Fujitsu Microelectronics was not included in the deal). Also, in June 2014, Panasonic completed the sale to Singapore's UTAC of its three assembly and test facilities in Singapore, Indonesia, and Malaysia.

The top OSAT companies continue to spend money on new capital additions (i.e., factories and equipment, mainly) and on the research and development of new technologies. As a group, the top 10 OSAT suppliers spent about \$3.8 billion in capital expenditures in 2014, an increase of 19% from 2013 spending. As a percent of revenues, the top companies spent approximately 21% on capital additions during the year, which is roughly two percentage points higher than the spending-to-revenue ratio for the entire semiconductor industry.

#### **E. Jan Vardaman, President and Founder, TechSearch International, Inc.**

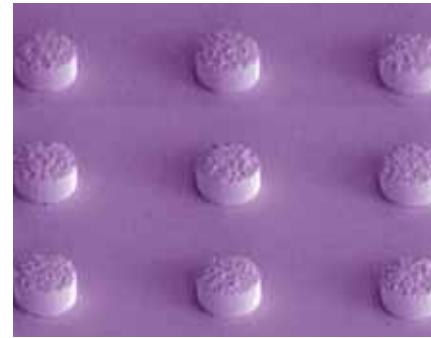
As the electronics industry matures, consolidation continues in all sectors including equipment, materials, IDMs, and IC



package assembly and test service providers. With continued consolidation in the OSAT space, assembly prices may not increase because the number of players is still large and capacity is not expected to decrease. In addition, new players in the market, especially in China, have entered by offering lower prices. Typically, higher prices in the IC package assembly sector have only resulted when there is a capacity constraint, such as availability of substrates, or natural or man-made disasters that force a plant closure.

Providing assembly and test of ICs and components to meet the needs of consumer products with an increasingly short time-to-market requires continued investment in capital equipment by OSATs. Capacity additions to meet the steep production ramps of mobile devices, such as smartphones, have resulted in greater capacity than needed throughout the quarter or the year. In order to recover their capex investments, OSATs may need to develop a pricing model or structure to fill capacity during off-peak times, allowing improved utilization. The difficulty is that this model requires some segment of the industry to hold inventory, a practice the industry moved away from in the early 1990s. Off-peak pricing is common in other industries such as electric utilities, but has not been applied to semiconductor packaging and assembly services.

The development of advanced packages to meet the needs of new electronic products also requires continuous R&D spending by OSATs. The success of some new advanced packages may require a closer financial partnership between the OSAT, the IDM, and the foundry in order to meet future product needs. Closer cooperation at consortia is one way to share this financial burden. There are many examples of consortia today that include these players as well as the material and equipment suppliers. Improved methods to develop future advanced packages in a timely manner will require innovative partnership solutions.



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## Outlook for 3D and 2.5D chips in smartphones

By Antonio La Manna *[imec]*

**3**D TSV technology enables different types of chips to be stacked on top of each other. They are connected by making holes (vias) through the chip and filling these with copper material (through-silicon vias, or TSVs). For example, you could stack different memory chips on top of each other to make compact and high-capacity memory stacks, or a logic and memory chip, or a FinFET-based logic chip and a standard CMOS-based logic chip. So you could say that 3D TSV bridges together different technologies. In this way, it is also an important enabler for future Internet of Things (IoT) products where miniaturized systems based on different technologies will make the scene.

The research community – including imec – has developed all the process steps that are needed to make 3D TSV chips. The technology is now ready, and thanks to the many advantages of 3D TSV technology (miniaturized system, fast communication, bringing together different technologies), more products are entering the market. Some of these products include: the memory cube, the Virtex 7 chips of Xilinx, and the high-bandwidth memory (HBM) of SK Hynix. It mainly concerns high-end products because the technology is still too expensive today to compete with 2D technology (i.e., transistor-based scaling). Still, this market is substantial in size and will allow the technology to further mature, resulting in lower cost.

Some experts at the recent European 3D TSV Summit (1/19-21/15; Grenoble, France) predicted that 3D TSV will be used in high-volume products by 2016. But I don't think it will go that fast. I see a faster adoption in the memory domain, but my guess is that it will take another 5-10 years until 2D technology runs out of power and companies will turn to 3D technology to make their products. It will be an evolutionary process rather than a revolutionary switch.

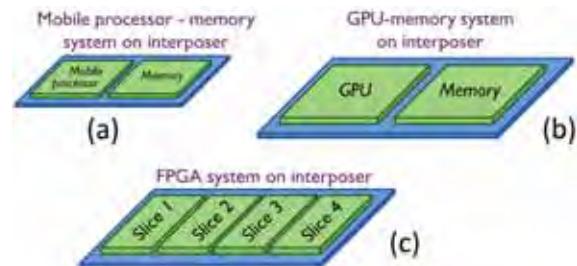
There is a technology – called 2.5D – that will certainly be important to make the evolution towards 3D. It is based on using a silicon interposer substrate on which the chips are put next to each other. It also allows the integration of chips of different technologies,

to increase the communication speed between the chips, and to put the chips closer to each other. It provides less advantages than a “pure” 3D stack, but has less issues in terms of assembly complexities and reliability. I do believe that 2.5D technology can bridge the gap between 2D and 3D technology.

At imec, we are developing the silicon interposer or 2.5D technology taking into account the overall application system. We do believe that to reduce cost it is important to have the full picture in mind. Reducing the cost for each step will definitely help, but proceeding in a step-wise fashion can obscure where the real cost issues lie. On the other hand, if you look at the overall system, you may discover that having capacitors in the interposer may be cheaper than having them as discrete components on the package or on the board (**Figure 1**).

You may also think to add some active or “lite-active” devices. Imagine the area consumed for ESD protection on a CMOS or FinFET logic chip. This area typically does not shrink with scaling. In this manner, a large area of your advanced chip is consumed by components that protect the chip itself from eventual electric discharge. This situation may be very expensive because it limits the effective area of your chip.

Continuing the discussion about ESD protection, ESD diodes do not require top-notch scaled logic technology and could be



**Figure 2:** Exploration of different system applications: a) Mobile processor and memory die; b) GPU processor and memory die; and c) Four FPGA slices on interposer.

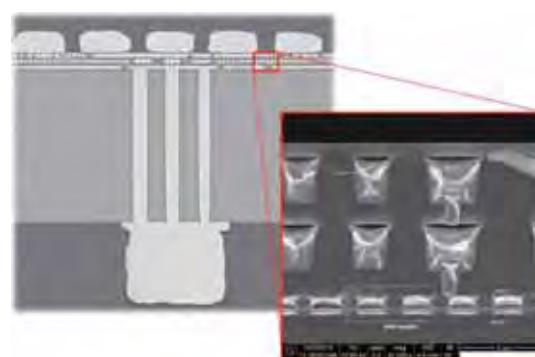
moved to the silicon interposer with a limited cost increase. The area that becomes available can then be used for logic functionalities instead, which will result in an overall cost savings.

In one of our projects, we have developed an interposer front-end that allows one to include lite-active components (diodes, BJTs, SCR, etc.) using a minimal number of additional masks and process steps when compared with a standard passive interposer. With these active components, the system design flexibility is increased and you may also enable a pre-bond interposer testability, thus preventing scrap cost when known good dies (KGDs) are stacked on a faulty interposer.

We have compared three different system applications to investigate what can be the impact of an “active-lite-interposer” (ALIT) on the system cost (**Figure 2**): 1) Mobile processor and memory die stacked on interposer; 2) Graphics processing unit (GPU) and memory die stacked on interposer;

and 3) FPGA system partitioned into “slices” and stacked on an interposer. The impact of ALIT will depend on the number of die-level I/O and the kind of on-chip ESD protection that these I/O signals require. Our assumptions in term of area and I/O for each system are indicated in **Table 1**.

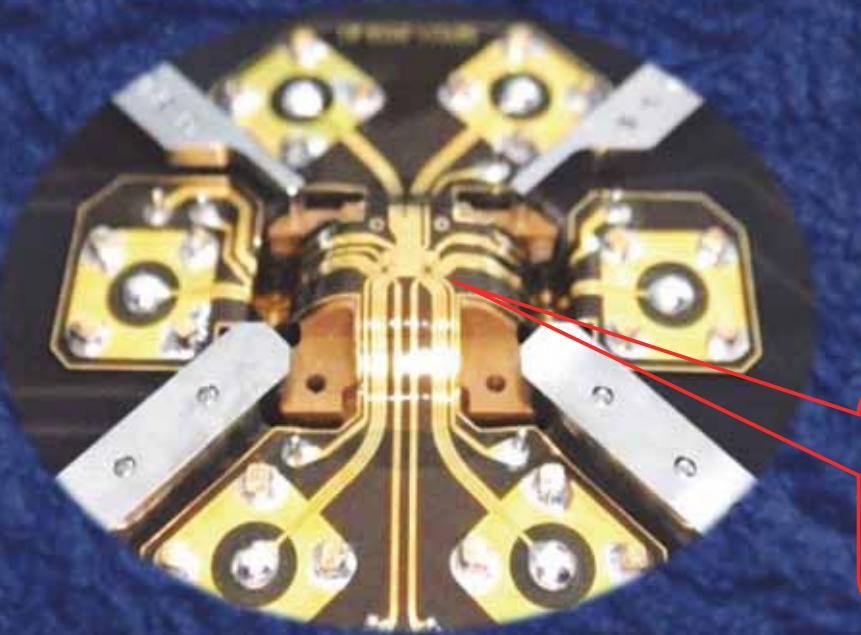
For each system application we have benchmarked the “pure” passive interposer versus the increasing of “ALIT” functionalities. Three different functionalities are



**Figure 1:** Si interposer with MIM capacitors integrated in BEOL.

# Are you looking for a new solution for High Speed Device testing?

## YPX Probe Card



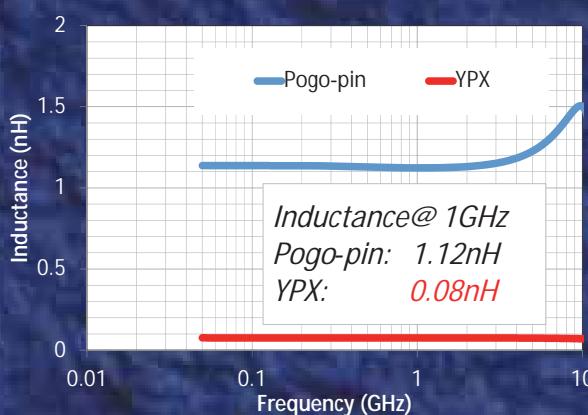
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Inductance Comparison (Pogo-pin vs YPX)

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Stroke	100um
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Trace L/S	20/20um
Insertion Loss	-3dB@20GHz
Return Loss	-15dB@20GHz

Specification

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explored: 1) Interposer test only, where the extra functionalities are only used to enable pre-bond test of the interposer; 2) Interposer test and small diodes for ESD protection; and 3) Interposer test and large diodes for ESD protection.

We mainly compare the case of pure passive interposer versus the cases on which we add some minimal diodes to support pre-bond testing or other diode sizes. In the case of a system with a mobile processor and memory die stacked on an interposer (Figure 3), the impact of the additional ALIT functionalities does not provide an overall system cost reduction.

In the case of a system with a GPU processor and a memory die stacked on an interposer (Figure 4), we see that the major benefit comes from adding the testing functionality. For this system, the active dies (and the interposer die as well) are quite large and with high cost. Because of the large die area, the process yield is also low (resulting in even higher active die cost). Therefore, testing the interposer die prior to stacking prevents scrapping of the expensive active dies. Also for this case, the number of I/O pins is relatively

small. Therefore, removing the ESD protection has practically no impact.

In the case of an FPGA-based system where four FPGA “slices” are stacked on an interposer substrate (Figure 5), we see a major benefit by moving the ESD protection to the interposer. In this system, the number of I/O signals among the four “slices” is large. Therefore, moving the ESD protection on the interposer positively impacts the overall system cost. This impact is significant, especially for ESD diodes with large area.

By running this exercise it appears clear that 2.5D or 3D technologies are not yet ready for “everything.” We need to select the right applications and use them to assess and resolve all challenges.

For the moment, the main challenges that I see, apart from the manufacturing costs of TSV, wafer thinning and stacking, are the availability of suitable design tools, and how to optimize the technology for high volumes. To reduce the cost, the 3D TSV infrastructure that is installed in some fabs has to be fully exploited. In fact, it’s a ‘chicken and egg’ problem: for reducing the cost, we need high volumes, but industry will only go to high

volumes when the cost is reduced. So it’s a matter of finding a killer application that relies on the unique assets of 3D TSV technology. For me, that’s the heterogeneous integration asset: with 3D TSV technology you can combine chips of different technologies. Today, it concerns mainly logic chips (of different technology nodes) and memory chips. In the future, however, it will also become possible to integrate MEMS (e.g., gyroscopes) and photonics chips via 3D TSV technology.

At the same time, this heterogeneous integration capability is also an obstacle. All chips of a specific technology are designed by specific teams and with specific tools. But with 3D TSV, a design tool is needed that can be used for the whole system, and the designers of the different building blocks will have to work together. So, the design issue is definitely the first thing to be solved.

It’s important to note that high volumes will be needed to optimize the process steps and process integration. Some issues (such as the aforementioned ESD) can only be discovered when you run high volumes. I’m convinced that all these issues can be solved by 2020. By then, we will find 3D and 2.5D chips in all kinds of products: in our smartphones, in domestic appliances, in road infrastructure—3D everywhere!

## Biography

Antonio La Manna received his MS in Electronic Engineering from the U. Federico II in Naples (Italy). He is Program Manager for 3D Technologies Integration at imec, Belgium; email Antonio.LaManna@imec.be

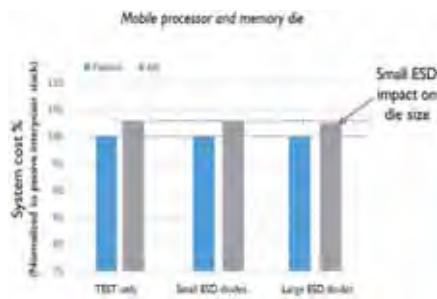
## Acknowledgments

Special acknowledgments go to the ALIT and 3D teams for their continuous work and commitment.

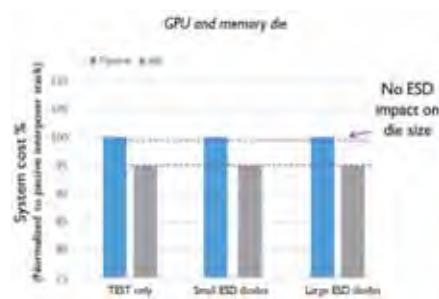
System	Chip	X (mm)	Y (mm)	Area (mm <sup>2</sup> )	Total I/O	External I/O	Internal I/O
Mobile	processor	9.8	10.4	102.7	1041	840	201 <sup>**</sup>
	memory	10 <sup>*</sup>	10 <sup>*</sup>	100 <sup>*</sup>	750	549	201
GPU	GPU chip	24	24	576	2485	1973	512
	memory	20 <sup>*</sup>	20 <sup>*</sup>	400 <sup>*</sup>	1231	719	512
FPGA 4 “slices”	FPGA “slice”	24.7	7.6	186.8	20000	10000	10000

\* Assumed memory die dimensions to match area of logic die on interposer  
\*\* Modified number of I/O to match memory interface

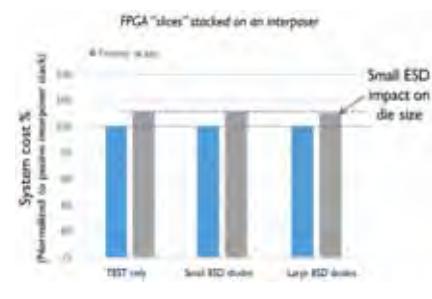
**Table 1:** Different system applications stacked on an interposer. The number of I/Os determine the area requirements for ESD protection.



**Figure 3:** Cost comparison of a system with a mobile processor and a memory die stacked on a passive interposer, versus an “ALIT” interposer. Three different functionality scenarios are explored: a) Interposer TEST only, b) Interposer test and ESD protection considering small diodes, and c) Interposer test and ESD protection considering large diodes.



**Figure 4:** Cost comparison of a system with a GPU processor and a memory die stacked on a passive interposer, versus an “ALIT” interposer. Three different functionality scenarios are explored: a) Interposer TEST only; b) Interposer test and ESD protection considering small diodes; and c) Interposer test and ESD protection considering large diodes.



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# Characterization of RF TSVs for 3D MEMS WLP

By Jessica Liljeholm, Peter Ågren, Niklas Svedin, Thorbjörn Ebefors [Silex Microsystems AB]  
Peter J. de Veen [MASER Engineering B.V.]

## 3

D interconnection technologies, such as through-silicon via (TSV) and through-glass via (TGV), are 3-dimensional technologies that enable vertical chip stacking by bonding. The microelectromechanical systems (MEMS) market is now aiming at high-performance applications, such as radio frequency (RF) MEMS, which drives the need for even smaller form factors with higher performance, longer battery life, along with the requirements of high bandwidth, minimum insertion loss, excellent matching characteristics, and high isolation. One of the main challenges in 3D packaging technology of RF devices is to combine excellent electrical RF performance (low loss) and hermetic encapsulation, together with a successful integration of the packaging process with the RF devices.

Glass substrate is a strong candidate to be used in RF applications because of its superior electrical insulation, low dielectric constant, high hermeticity, low warping, and high resistance to corrosion [1]. Simulation and measurements of TGVs and TSVs for RF application normally show higher insertion losses for the conventional TSVs than for TGVs [2-4]. Silex has developed a high-resistivity Si TSV technology and is now also developing a production-feasible TGV technology [5]. This article highlights the high-resistivity Si TSVs for RF applications with test vehicles and demonstrator fabrication.

The high-resistivity silicon Cu-based TSV demonstrator was partly based on work performed within the European project EPAMO, or “Energy-efficient piezo-MEMS tunable RF front-end antenna systems for mobile devices [4].” Silex’ objective was to achieve fine-pitch through-wafer vias that would allow high-density 3D system integration in ultra-small RF module substrates with integrated components, such as RF inductors. Inductors with a high-quality factor (i.e., high-Q inductors) are critical elements in the overall communication antenna system.

High-Q inductors are able to correct both the real and the imaginary part of the signal in a matching network. Because of the relatively low Q-factor value reported so far for on-chip semiconductor thin-film passive components [6], innovative solutions are desired in order to obtain Q-factors above 30 for a frequency range of 0.5-4.0GHz [7].

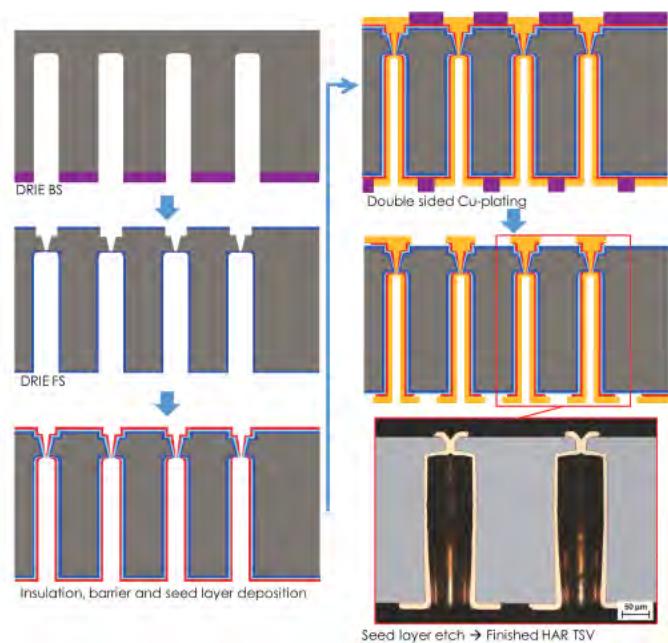
In the MEMS industry, a high yield is important and more efforts are now focusing on novel technologies related to reliability and nondestructive failure analysis, enabling detection of non-functional dies. Reliability evaluations and mechanical thermal cycling experiments of TSVs have just recently started. Interesting developments for the nondestructive analysis of TSVs to screen for defect vias are the emergence of high-frequency GHz scanning acoustic microscopy (SAM) [8] and 3D computed tomography (CT) X-ray microscopy (XRM) [9] tooling.

The rise of plasma-based focused ion beam (FIB) [10] tools enables a faster destructive cross-sectioning analysis of TSV structures, compared to conventional FIB cross-sectioning using Ga ions. The utilization of fault isolation techniques such as, photo-emission microscopy (PEM) [11] and lock-in thermography (LIT) – a method to detect very small temperature differences – on TSVs has also been exploited in literature recently [12]. In this paper,

non-destructive X-ray analysis is explored to better understand the failure mechanisms and further improve TSV production yield.

## Manufacturing of metalized TSVs

To manufacture high-aspect ratio (HAR) TSVs, a double-sided deep reactive ion etching (DRIE) step is required to create an X-shaped via, consisting of a backside (BS) via meeting a front side (FS) via. The X-shaped profile is desired because it locks the structure, thereby improving the mechanical reliability of the TSV and also facilitates the metal filling of the TSV. The BS via is designed with a 90µm diameter and a 280±10µm depth, giving an aspect ratio of 3:1 and a pitch of 240µm, creating a density of 16via/mm<sup>2</sup>. The FS via is designed to have a tapered structure, with dimensions of 30±10µm in depth and surface opening. The established process flow for the TSVs is shown in **Figure 1**.



**Figure 1:** Established Met-Via® process flow of the metalized HAR TSV at Silex, with an optical microscopy image of two mechanically cross-sectioned TSVs after process optimization.



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- Active Optical Cables
- Silicon Photonic Packaging

### MEMS Assembly

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- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

The TSVs were created by using 300 $\mu$ m thick and 200mm diameter high-resistivity engineered silicon wafers (3-10kOhm-cm) from Okmetic Oy, Finland [4]. Using rigid (thick enough) Si-wafers, no carriers or temporary bonding techniques were required.

With decreasing TSV diameter, there is an increasing challenge to achieve a conformal seed layer deposition as well as a conformal Cu plating. In this paper, metal organic chemical vapor deposition (MOCVD) Cu is evaluated for barrier and seed layer deposition. Additionally, optimized Cu-plating chemistry and multistep plating, as described in [13] resulted in void-free hermetic sealed RF TSV structures (**Figure 1**). This plating time is a >20x reduction of the plating time used by Chen, et al. [14] for other RF TSV structures using similar dimensions (i.e., 300 $\mu$ m thick TSVs with 90 $\mu$ m via diameter). More detailed process optimization to solve technical issues is described in Ebefors, et al. [5, 13].

## Via integration

We have experience with a wide range of different MEMS products. For example, TSI™ technology [15] has been successfully implemented by end users as Sil-Via® TSV structures in more than 100 products, including examples such as: 1) A microphone 2.5D functional interposer in high volumes; 2) Vacuum encapsulation of timing and resonator devices; 3) Inertial motion sensors with a combination of gyro and accelerometers for consumer electronics; 4) Micro-optical mirror and micromachined ultrasound transducer (MUT) devices; 5) Microfluidic devices for micro-total analysis system ( $\mu$ -TAS) applications; and 6) Advanced interposers for 3D stacking of application-specific ICs (ASICs) and radiation detectors on both sides of the interposer. Adding functions, such as decoupling high-Ohmic resistors and high-k metal-insulator-metal (MIM) capacitors based on, for example, PZT, will further enhance the device functionality. Such work has been performed by Silex and a schematic example of PZT MIM capacitors integrated with Cu TSV and polysilicon thin-film resistors is shown in **Figure 2a**.

Low-ohmic wafer-to-wafer interconnects are important, especially for high-frequency RF applications; the bonding integration is, therefore, a key process. Our approach is the combination of metal-metal bonds

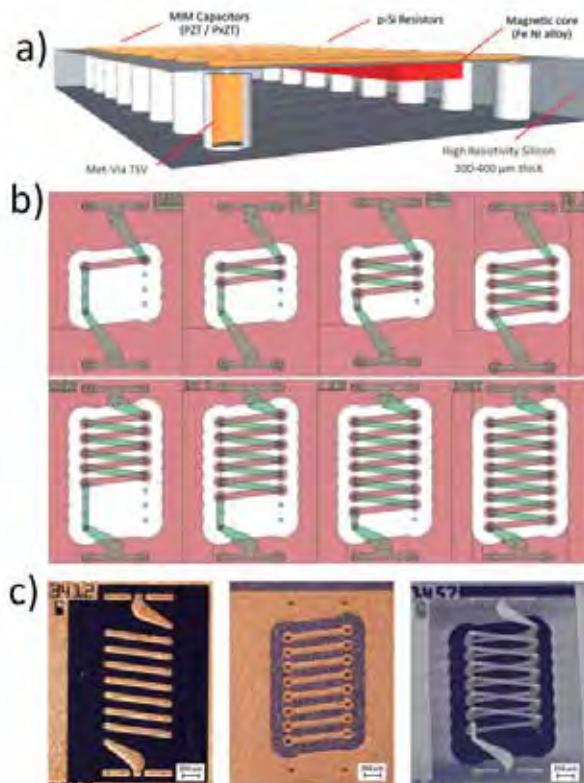
using thermocompression and/or eutectic bonding with noble metals, such as Au and various solders, which allows better integration reliability [16-17]. When bonding wafers with topography (i.e., non-planarized CMOS wafers) to achieve vacuum sealing with integrated TSVs, the preferred bonding processes should have a low melting point (200-400°C). Silex SmartBlock® examples are eutectics-based: Au-Si or AuSn-Au stacks. These stacks enable the formation of wafer-to-wafer sealing that results in improved hermiticity and allows larger topographies on the bonded wafers, as compared to other dry interdiffusion-based bonding mechanisms. A more detailed description of permanent and temporary bonding methods required for successful TSV integration is described by Ebefors [18].

## Electrical characterization

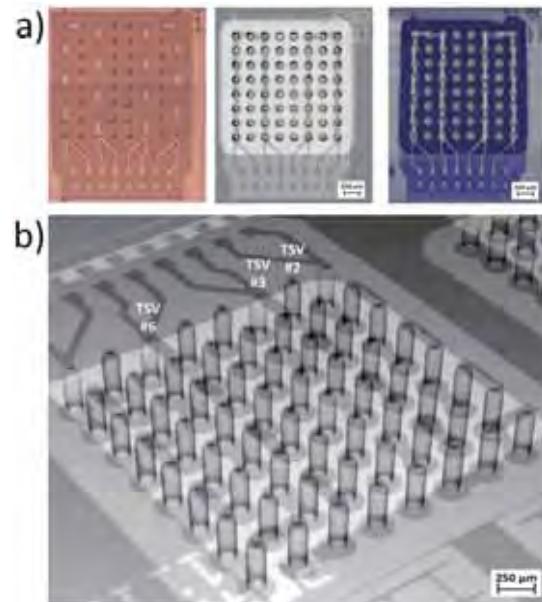
Electrical characterization of the metallized TSVs described above was done for both DC and RF attributes (see sections below). Additionally, RF IPD was evaluated as noted (below).

**DC TSV characterization.** 3D inductors and daisy chains (**Figure 2b**, **c**, and **Figure 3**, respectively) were used to electrically characterize and evaluate the finalized metallized TSVs. The direct current (DC) via resistance was measured with an Agilent 34401A 6 1/2 digital multimeter and a Karl SUSS PM5 probe station. A total of 644 TSVs, divided over four different wafers, were evaluated. The mean DC resistance of the fully functional TSVs was approximately 20.4mOhm.

**RF TSV characterization.** Co-planar waveguide (CPW) structures with 2.35mm long transmission lines were used for RF TSV characterization (**Figure 4**). The results were presented in the work performed by Ebefors et al. [13] and it was



**Figure 2:** a) Schematic example of a wafer-level integrated process flow with Cu TSV (Met-Via®) to form 3D inductors with a magnetic core, with the additional integration of high-k PZT MIM capacitors and polysilicon high-Ohmic decoupling resistors. SOURCE: EPAMO consortium [19]. b) CAD-file image of the 3D inductor design used for characterization of RF IPD inductors; the number of turns varied from 1 to 8 (green represents the FS metal, red the BS metal). c) Optical microscopy images of an 8-turn TSV inductor coil test structure: from left, the FS, BS, and a 3D X-ray CT visualization of the same structure.



**Figure 3:** a) The TSV daisy chain used for the DC via resistance characterization imaged, from left, by optical microscopy, 2D X-ray and 3D CT X-ray microscopy; b) OVHM X-ray image of one of the few incompletely functional TSV daisy chain array test structures; the TSVs #2 (functional), #3 and #6 (suspected non-functional) are indicated.

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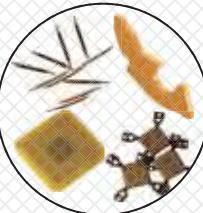


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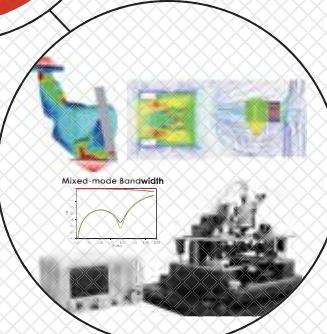
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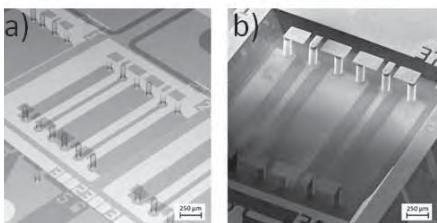
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**Figure 4:** a) 2D oblique view X-ray image of a CPW test structure used for RF TSV characterization; b) SEM image of a CPW structure after a selective wet-etch that removed all Si wafer material.

concluded that the TSVs showed very low losses, less than -0.04dB per coplanar TSV at 5GHz frequency. The measured loss in the case of microstrip lines was less than -0.12dB up to 5GHz (equivalent to -0.5dB/cm at 5GHz).

**TSV RF IPD inductors.** The coil structures of inductors were used for the characterization of the RF IPD, with the number of turns varying between 1 and 8 (**Figure 2b**); these were characterized by the EPAMO partners TNO, VTT and EPCOS NL to verify the results. The coils showed Q-factors above 30 for inductance values up to 5nH, with a self-resonance frequency above 10GHz. Q-values (2 port), derived from measured Y-parameters, of over 30 at 1GHz, were achieved for all inductor designs (**Figure 5a**). The inductors were characterized up to 10GHz and practical RF inductors for frequencies up to 3.6GHz were successfully demonstrated

as well. The inductance value for each inductor design was determined from a fit of a parallel L-C model, with resistive loss in the L section, to the series branch of a pi-model of the measurement data (**Figure 5b**). In the Y<sub>s</sub> branch, there is no obvious self-resonance (<6GHz); instead, a gradual decrease of the effective inductance was observed (**Figure 5c**). More detailed results and discussion are presented in [13].

Additionally, the temperature dependence was investigated; a decrease in the Q-factor could be observed for higher temperatures, most likely related to Si-substrate losses. Complementary measurements were performed by TNO (see **Figure 5d, e**) to investigate if the temperature effect was reversible or permanent. In this set-up, the measurements were repeated at ambient temperature after a high-temperature measurement. The temperatures, measured by a sensor on top of the glass wafer, were: 25°C (for a setting of 25°C), 88°C (for a setting of 80°C) and 112°C (for a setting of 100°C). The measuring sequence was: 25°C - 80°C - 25°C - 100°C - 25°C. The measurements were performed on the inductor coil test structures with 5-, 6-, 7- and 8-turns.

With respect to the effect of temperature on the S-parameters, it was concluded that this is a reversible effect; when returning to ambient temperature, the device behavior is within small variations (<1% S-parameter

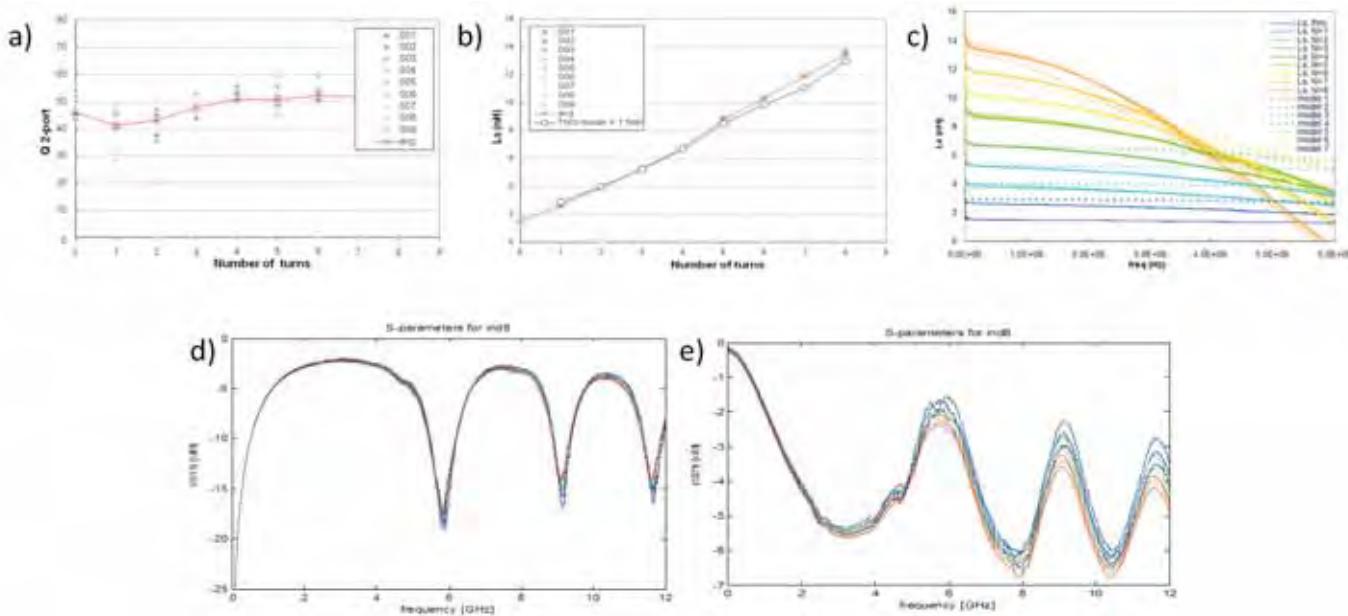
error) identical to the other measurements at ambient temperature.

The high performance of these coil structures makes them suitable for use in multi-band adaptive tuner matching networks for mobile technology. Further simulations and modeling were executed to match Silex inductors with Murata surface mount device (SMD) inductors of 2.7nH and 5.1nH. New designs were proposed and more detailed results are available in the publication from Ebefors and Oberhammer [20].

### Failure analysis of TSVs

Within the European project EPAMO, MASER Engineering was to develop new reliability test and failure analysis procedures in order to be ready for qualification and future field returns of 3D integrated (RF MEMS) applications. A good overall electrical DC yield was obtained after process optimization (in the high 90% range); only a handful out of hundreds of measured TSV daisy chains failed. In this investigation, those failures are addressed; non-destructive X-ray screening was used as an initial failure localization technique to find out which TSVs should be further inspected by a destructive analysis imaging technique (e.g., cross-sectioning).

Visible in **Figure 3b** is a contrast difference in grey color between various



**Figure 5:** a) Q-factors at 1GHz vs. number of turns in the 3D inductor at nine different wafer positions (S01-S09), equally distributed over each tested 8-inch wafer; b) Inductance values at 1GHz vs. number of turns in the 3D inductor structure at the nine different wafer positions distributed over each tested 8-inch wafer, compared with theoretical modeling; c) Inductance measured by EPCOS NL with various frequencies. Higher frequencies result in a gradual decrease of the inductance; d) Comparison of S-parameter measurement results for an 8-turn inductor for several cases: magnitude of  $S_{11}$  (return loss); and e) magnitude of  $S_{21}$  (insertion loss). Measurements at 25°C have been performed three times: initial, after the 80°C, and after the 100°C measurements.

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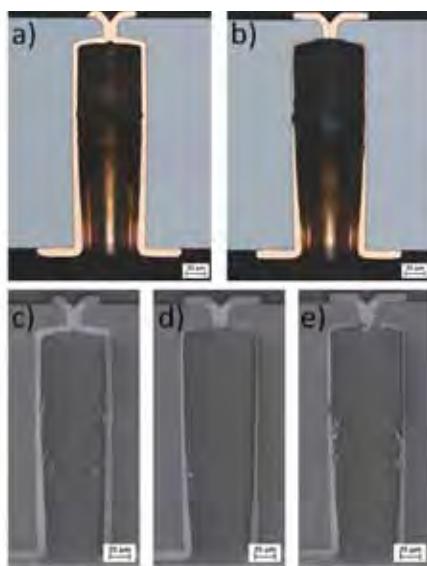
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TSVs; for example, TSVs #3 and #6 appear much brighter than TSV #2. This color contrast difference of the open TSVs indicates variations in the thickness of the Cu plating inside the vias. X-ray screening of more TSV test structures showed that these Cu plating thickness variations seem to be design related. The TSVs (#1, #3, #6 and #8) all connected to a large area redistribution layer (RDL) have a lighter grey color, most likely caused by different current distributions during electroplating. Optical microscopy (OM) and scanning



**Figure 6:** Optical microscopy (OM) images of mechanically-prepared cross-sections through the middle of a) TSV #2 and b) TSV #6. SEM image of the mechanically cross-sectioned TSVs c) #2, d) #3 and e) #6.

electron microscopy (SEM) cross-section images (**Figure 6**) confirm the non-uniformity in Cu plating thickness and also confirm that the thickness of the conformal Cu plating in TSV #2 varies between 8.0 and 10.0 $\mu\text{m}$ , whereas the non-conformal Cu plating thickness in TSVs #3 and #6 vary between 1.0 and 10.0 $\mu\text{m}$ .

As the above results show, Cu-plating thickness deviations, large voids, and other defects in TSVs can easily be detected using conventional X-ray technology. However, the resolution of this technique is limited; small sub-micron defects in the TSVs are hard or impossible to detect. The emergence of high-resolution (HR) or nano-focus X-ray microscopy/CT is, therefore, an interesting development for the nondestructive screening of defect vias [21].

To conclude, the above investigation shows nondestructive X-ray inspection

is a simple screening method to quickly identify a defective TSV, which can then be further inspected using other (destructive) imaging techniques. Based on these failure analysis findings, a new plating procedure has already been established.

### Cost-of-ownership

To ensure low cost-of-ownership (CoO), the electroplating of the open TSVs (as used for the 3D IPD inductor demonstrator) was performed in a specially designed Cu plating tool. This tool enables cost-efficient simultaneous double-sided plating and TSV sealing using thick dry film resist as plating masks for the RDLs and inductor windings.

Because the skin depth of Cu and Au for RF signals in the GHz range is in the  $\mu\text{m}$  range (skin depth at 5GHz is approximately 0.9 $\mu\text{m}$  for Cu), complete filled vias are not needed. A uniform and smooth Cu liner on the TSV results in low enough RF and DC losses. Further, the reliability and overall device yield issues associated with thermal mismatch between metals such as, Au and Cu, and silicon or glass, are minimized when the vias are not completely filled and only rely on a local hermetic seal in the via structure, as shown in **Figure 1**. Therefore, partially-filled TSVs are preferred from a CoO perspective. Furthermore, because there is no multi-metal interface between the front and backside RDLs, the risk for RF losses by impedance mismatch or interface contact resistance are avoided, as is the case with conventional blind via fabrication and via reveal processes. This improves the overall yield, thereby reducing the CoO.

Finally, because the Met-Via® TSV technology does not require a costly temporary carrier bonding with grinding and chemical mechanical polishing (CMP), as other conventional TSV technologies require, the CoO is further lowered.

### Outlook for future research and commercialization

New MEMS processes and new materials in 3D integration technologies (interposer) require new solutions for failure analysis. Key to accomplishing physical failure analysis is to be able to deploy a time- and cost-efficient method for localizing and imaging the fault, without disturbing or destroying the fault

during the analysis process. The outlook for future research at MASER Engineering is to explore high-resolution X-ray CT in combination with other fault localization techniques such as LIT to pinpoint the defect location in 3D more accurately.

Verified cost efficiency and volume manufacturability of MEMS processes at wafer-level for integration of advanced TSV-based MEMS devices are important topics for future research and commercialization. Next-generation MEMS TSV products will likely use novel nonstandard IC materials such as Au, Pt, PZT, NiFe, etc., which place challenges on the integration process.

The Silex partially-filled rigid (thick wafer) Met-Via solution enables a 2.5D interposer platform. It goes beyond the MEMS domain even if it rests on the ability to process and handle mechanically thin and structured wafers. Silex is working with IC foundry partners to combine the metal via base technology with a 4-layer Cu damascene process. When such an approach to form a 2.5D interposer is used, the need for complex temporary bonding/debonding is avoided, as well as the need for an intermediate BGA laminate layer. The top layer of the interposer solution enables a microbump pitch with 2 $\mu\text{m}$  line/space; and at the bottom of the interposer, the silicon substrate has a PCB pitch of down to 400 $\mu\text{m}$ . Most of the high-speed signals will run in the four Cu damascene layers on the top side. This approach will constitute a very attractive, low-entry barrier solution that goes beyond MEMS to solve the 2.5D integration challenge.

### Summary

In this work, a successful manufacturing method for partially-filled metalized TSVs has been described. Excellent RF performance for TSV wafer-level integrated devices has been demonstrated and experimentally validated. The TSV RF characterization using coplanar transmissions lines showed high performance, with very low losses—less than -0.04dB per coplanar TSV at 5GHz.

In addition, an RF IPD 3D-inductor design was manufactured by using the RF TSVs as wafer through-connections, demonstrating a well-working application of the TSVs. The electrical properties obtained made them suitable for use in multi-band adaptive tuner matching networks for mobile technology. A

decrease of the Q-factor was observed for higher temperatures; however, additional measurements concluded that the temperature effect was reversible.

The failure analysis investigation showed that nondestructive X-ray inspection is a simple screening method to quickly identify a significant defective TSV, which can then be further inspected using other (destructive) imaging techniques (e.g., cross-sectioning).

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All OM, SEM and X-ray images in **Figures 1, 2, 3, 4 and 6** are made by and courtesy of MASER Engineering B.V., the Netherlands.

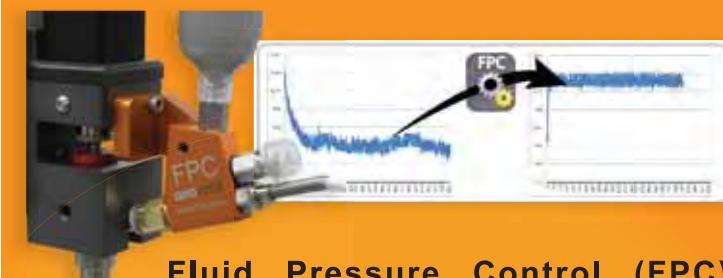
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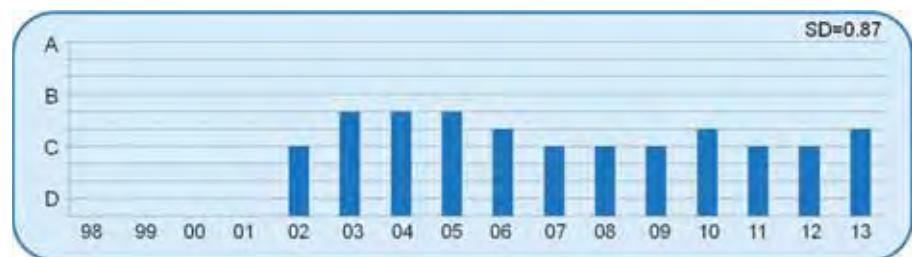
# The role of standards in MEMS commercialization

By Roger H. Grace [Roger Grace Associates], Harrison Bearsley [Global Semiconductor Alliance], Michael Gaitan [NIST], Karen Lightman [MEMS Industry Group], Ravi Subramaniam [IEEE], and Paul Trio [SEMI]

For many years, the development, creation and use of standards has played a valuable role in the successful commercialization of products, services and processes that address many industries and many applications. So it is with microelectromechanical systems (MEMS) [1]. In the annual MEMS Commercialization Report Card [1], standards were identified as one of the 14 critical success factors that have been monitored and assessed since 1998. Standards reporting began in 2002 and is shown in **Figure 1**. Creating standards is a long and deliberate process (**Figure 2**) with the volunteer efforts of many contributors who typically accomplish their goal after several years and many meetings.

Several industry experts who represent various organizations in the MEMS supply chain were interviewed for this article by the lead author. Soliciting the opinions of members of the supply chain is important because it is the suppliers that will adopt, use, and subsequently benefit from the establishment of these standards. They represent many of the entities that are intimately involved with the various functions of the MEMS commercialization process (**Figure 3**).

The consensus of the authors of this



**Figure 1:** The MEMS Commercialization Report Card grades for standards have received lackluster grades, typically in the "C" level, with the 2013 grade being "C+." It has one of the lowest standard deviations over the reporting period at 0.87. Courtesy: Roger Grace Associates

paper is that the lack of adequate standards in MEMS has far reaching consequences to MEMS commercialization. The impact of standards spans definitions, specification performance uniformity, testing methods, product time-to-market, device cost, and device interoperability. We found other examples of industry experts who have weighed in on the vital role that standards can play, as well as the difficulties in creating them. Examples are cited below.

**S. Walsh, U. of New Mexico.** R. Grace, in collaboration with Professor Steve Walsh of the University of New Mexico, has approximated that the median and mean time-to-market for a MEMS device from technology discovery to full commercialization to be approximately 30

years (**Figure 4**) [2]. The lack of creation of adequate MEMS standards has been one of the leading contributors to this prolonged commercialization process.

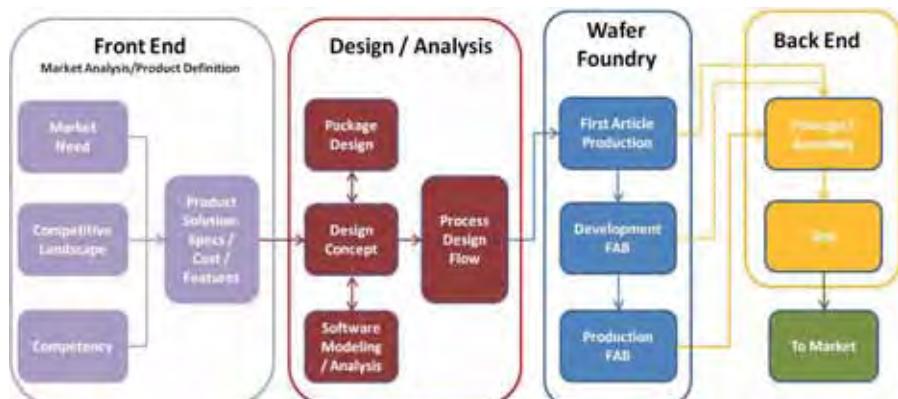
## The need for standards

**H. Bennett, NIST.** At the GaN Roundtable event [3], Herbert S. Bennett of NIST stated, "Knowledge of standards can help facilitate the transition from classroom to professional practice by aligning educational concepts with real world applications."

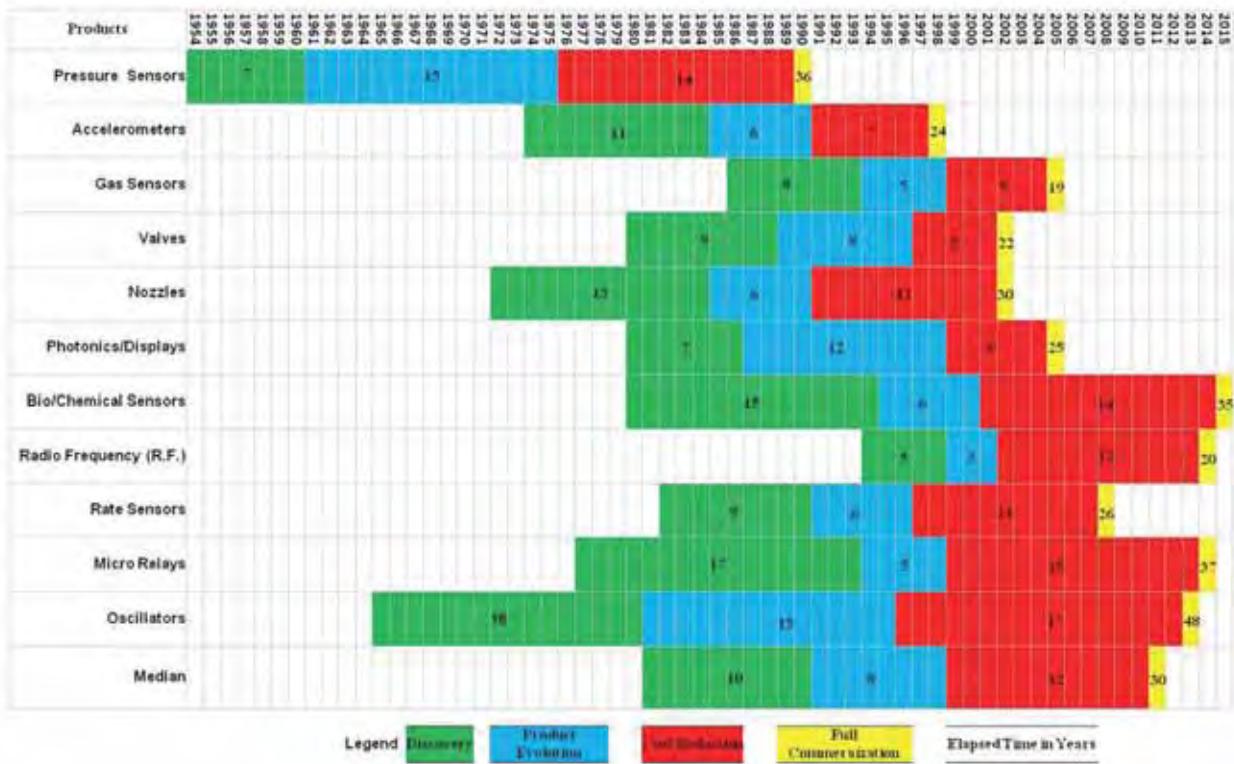
**R. O'Reilly, Analog Devices.** Rob O'Reilly of Analog Devices – interviewed for this article – stated that, "With the involvement of MIG [MEMS Industry Group], a Data Sheet Performance



**Figure 2:** The successful creation of standards is a multi-iterative and multi-element process and requires the dedicated contributions of a wide variety of volunteers expert in the addressed topic and the various specific functions of the standards process. Courtesy: H. Bennett/NIST



**Figure 3:** The MEMS Commercialization process includes many functional elements where standards can play a vital role in the facilitation of successful commercialization. Courtesy: Roger Grace Associates



**Figure 4:** The time period to successful full-scale commercialization of various MEMS devices has established an elapsed time of approximately 30 years from technology discovery to device full-commercialization status. Courtesy: R. Grace/Prof. Steve Walsh-MANCEF

Specification was created that helped level the playing field when it came for a potential customer to have an apples-to-apples comparison of our accelerometer's performance. OEMs could now develop solutions using several sensor providers once the data sheet parameter definitions used across the industry were, by specification, the same."

**J. Wetzel, Novati Technologies.** Finally, Jeff Wetzel of Novati Technologies (also interviewed for this article) has said, "Standards enable IDMs, OEMs and supplier communities to transact business efficiently since specifications, and the means to confirm specifications, are mutually agreed upon, documented and periodically updated. Standards provide manufacturers with the knowledge that their supplier base conforms to known specifications. Adherence to standards by the supplier and manufacturer communities defines a range of available solutions for lowest cost manufacturing."

## The difficulty in establishing MEMS standards

**D. Kirsch, EV Group.** Dave Kirsch of EV Group (also interviewed for this article) noted that, "Semiconductor manufacturing

processes are more established and tend to follow Moore's Law, whereas in MEMS, the manufacturing process can be influenced by the application...and applications tend to be much more diverse than in the IC domain."

**M. Maher, SoftMEMS.** Mary Ann Maher, SoftMEMS, (during her interview for this article) stated that, "Each company involved in manufacturing MEMS has found a way that works for them, and as such, has developed internal standards that they consider proprietary and may consider to be a competitive advantage. Another key point is that, because there are few standard processes in MEMS, we need to find a standard way to exchange information even though the information itself may not be standard. We will also find standards at the interface and connector level as more MEMS become integrated into other systems."

## Full speed ahead: the drive for MEMS standards

Besides the activities to drive standards development by those in both the supply chain and device fabrication space, major efforts have been made by a number of industry organizations. Some of those

efforts are highlighted below.

**Global Semiconductor Alliance.** Recognizing the need to drive MEMS development processes along a path similar to fabless semiconductor development, the Global Semiconductor Alliance (GSA) undertook an effort to bring semiconductor expertise together with MEMS leaders to nurture a mutual understanding and forge a common development environment.

With the thrust towards a trillion sensors and the "Internet of Whatever," it is critical to develop repeatable processes, minimize time-to-market, and drive toward first-pass success for MEMS sensors and products integrated with MEMS devices. Understanding this need, the GSA team meets quarterly to self-educate and develop tools that lead to this ideal. Our team has worked hand-in-hand with MEMS efforts in other organizations to contribute the collective knowledge of our semiconductor members.

In any design environment, it is critical that information exchange is comprehensive and clear. Foundry Process Design Kits are commonly used as guidelines for proven standardized processing platforms. These guidelines ensure that the design can be mass-

fabricated with predictable, high processing yields. The lack of standard processing MEMS platforms prompted the need for alternative methods to exchange design and processing information. The GSA MEMS team has generated a Process Design Documentation (PDD) Quality Checklist that aims to facilitate information exchange between designers and foundries.

The PDD contains a comprehensive list of information that is universal for designers and foundries alike. This list is not product specific, process specific, or foundry specific. The PDD is meant purely as a checklist to ensure that information exchange between MEMS designers and MEMS foundry is complete, accurate and comprehensive. For designers, the PDD helps understanding what information should be requested from a foundry. For the foundries, this checklist can be used to ensure that designers have covered all major processing aspects of the design. The ultimate goal is to make better quality products that are scalable for mass production and can get to the market faster.

**Institute of Electrical and Electronic Engineers (IEEE).** The IEEE Standards

Association (IEEE-SA) was integral in developing IEEE Std 2700-2014 for Sensor Performance Parameter Definitions (<http://bit.ly/175oQGX>), and continues to play an important role in the Internet of Things (IoT), MEMS, and sensors spaces. Prior to the publishing of this standard, there was a void in the industry for defining sensor performance and a recognizable, industry-adopted terminology for describing the various performance parameters exhibited by sensors. An entity-based (one company, one vote) working group was formed to complete this effort. The sponsor for this effort was the MEMS Standards Development Committee, which operates under the IEEE Electron Devices Society. IEEE-SA has also developed many standards and guides for smart grid and personal health care devices that utilize sensors.

The standard from IEEE is an important and key step towards minimizing non-scalable integration challenges and accelerating time-to-market. Future efforts should look at standardized test methods for evaluating sensors, which would enable industry to have an unambiguous

and systematic way to assess sensors. This kind of approach would then lead to the prospect of having interoperable products. Could we envision a future where sensors are certified prior to use? Numerous applications such as biometric screening and toy safety utilize conformity assessment with international consensus standards to ensure proper market rollout including removal of any trade barriers.

With industry adopted standards and a conformity assessment program, manufacturers will have the ability to implement standardized features within their products and compete on differentiating their offerings, which ultimately spurs innovation. From a systems integrator standpoint, they can require certified component that will then ensure proper operation and interoperability. This then brings about a seamless and enjoyable user-experience for all that will instill consumer confidence in the technology.

**MEMS Industry Group (MIG).** Based on discussions at its 2012 member meeting, MIG launched a standards working group. In 2013, MIG announced the first-



ever Standardized Sensors Performance Parameter Definitions (SPD) document, authored by MIG members. In 2014, MIG led the creation of the first-ever IEEE standard for MEMS and sensors performance: IEEE 2700. To advance the adoption performance standards, MIG also has an accelerator performance testing subcommittee that meets regularly to solve the remaining issues affecting performance standards and testing/measurement for MEMS and sensors.

At its MEMS Executive Congress US 2014, MIG announced the open-source sensor fusion algorithm library, the Accelerated Innovation Community (AIC) to reduce time-to-market startup costs, risks and barriers to entry by encouraging inputs and collaboration across the MEMS/sensors supply chain. In three short months, there has been over 400 logins to the AIC website since its release in November 2014!

All of MIG's working groups will meet in person at MIG's MEMS Technical Congress, May 6-7 in Boston ([memstechcongress.memsinindustrygroup.org/](http://memstechcongress.memsinindustrygroup.org/)).

Standards, and in particular, standardization, are critical to the successful commercialization of MEMS and sensors as they create an open playing field for companies big and small. Performance standards, such as the ones authored by MIG, will enable reduction of overall costs and faster-time-to-market, enabling a true and smart Internet of Things/Everything (IoT/E). The MIG organization believes strongly that the IoT/E will not happen if the industry does not address the remaining challenges to MEMS and sensors commercialization, including standards/standardization.

**National Institute of Standards and Technology (NIST).** NIST has worked towards the advancement of MEMS standardization since the early 90s. At that time, the lack of standardization of test structures and test methods resulted in huge variation in important MEMS device design parameters, such as strain and elastic modulus, and their relationship to fabrication process conditions. This was most notable when researchers reported on values measured in a shared fabrication run, such as what was offered by the multi-user MEMS process (MUMPS). NIST brought together leaders in the field to participate in a round robin experiment that was crafted to develop agreement on how to standardize these tests. This consensus building effort was followed by

the development and publication of the first MEMS standards, ASTM E2244, E2245, and E2246, which described procedures for the measurement of film thickness, strain, and strain gradient. The ASTM standards were followed by the development of the SEMI MEMS Standards described in another section of this article.

In 2009, NIST teamed with the MEMS Industry Group to develop the MEMS Technology Roadmap, which is now published yearly alternately by the International Electronics Manufacturing Initiative (iNEMI) and the ITRS. This roadmapping effort has served as a vehicle to develop consensus among the device manufacturers, test labs, equipment suppliers, and systems integrators on the need for standardizing the test methods for characterizing device performance that are published in device data sheets. It also tracks and reports on other gaps in the design and manufacturing process, including requirements for design tools, foundries, and assembly and packaging.

Our experience shows that technology roadmapping is an efficient way to bring manufacturers together to articulate their common challenges, and has led to important results. Responding to the device testing issue, NIST has teamed with the MEMS Industry Group and the IEEE to develop standard sensor parameter performance definitions. These standards are intended to drive harmonization in how the sensor performance is reported in the device data sheets. So far, a terminology standard has been published (IEEE Std. 2700-2014). The sensors included in this terminology include accelerometers, gyroscopes, magnetometers, hydrometers, pressure sensors, and more. Now, the work is focused on the development of standard testing protocols for determining each of the parameters listed in the sensor performance specifications.

**Semiconductor Equipment and Materials International (SEMI).** In 2003, SEMI established a MEMS Standards Committee to address the need for standards in the MEMS industry. Ten standards have been published since inception:

- **MS1** – Guide to Specifying Wafer-Wafer Bonding Alignment Targets
- **MS2** – Test Method for Step-Height Measurements of Thin Films
- **MS3** – Terminology for MEMS Technology

- **MS4** – Standard Test Method for Young's Modulus Measurements of Thin, Reflecting Films Based on the Frequency of Beams in Resonance
- **MS5** – Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures
- **MS6** – Guide for Design and Materials for Interfacing Microfluidic Systems
- **MS7** – Specification for Microfluidic Interfaces to Electronic Device Packages
- **MS8** – Guide to Evaluating Hermeticity of MEMS Packages
- **MS9** – Specification for High Density Permanent Connections Between Microfluidic Devices
- **MS10** – Test Method to Measure Fluid Permeation Through MEMS Packaging Materials

Volunteer industry experts develop these consensus-based documents, motivated by the critical role SEMI Standards play in increasing manufacturing efficiency and producing faster time-to-market. Additionally, SEMI Standards increase market access and acceptance, promote communication within and across industries, enable faster commercialization and interoperability, accelerate product development, simplify installation and testing, reduce costs, and protect users and the environment.

Current SEMI Standards activity for MEMS is generally organized into six areas: microfluidics, wafer bonding, terminology, packaging, materials characterization, and reliability. Standardization discussions range from test methods for electro-osmotic mobility in microfluidic systems, to wafer bonding activities that align with related SEMI 3DS-IC initiatives, to hermeticity of MEMS packaging.

Looking toward the future, the Internet of Things (IoT) will rapidly increase the diversity and volume of MEMS sensors. Driven by industry, the SEMI Standards Program will continue to evolve to provide the important pre-competitive standards for this fertile area of innovation.

## Summary

The recent Data Sheet Performance Specification (IEEE 2700-2014) championed by a MIG-formed committee and NIST is the first IEEE MEMS and Sensor standard. There are many more MEMS standards that need to be

created to further successful MEMS commercialization. These need to address materials, processes, definitions, test methods and procedures, packaging and interoperability. To exploit low hanging fruit, the MEMS industry should assess the approximately 900 SEMI standards that were created for the IC industry, and, building on the 10 SEMI MEMS standards already in existence, create even more MEMS-specific standards that draw on the similar technology and processes of these standards. In this fashion, a broader range of MEMS standards can be created with the least degree of effort and time. The results of these proposed efforts should provide added value to all participants involved in the MEMS commercialization eco-system, especially in light of the exploding creation of MEMS and sensor-based solutions for the Internet of Things (IoT) and wearable applications.

### Acknowledgement

Another source of information regarding MEMS and sensor standards can be found at the IEEE sponsored webinar that was held on February 19, 2015 ([http://standards.ieee.org/events/multimedia/iot\\_mems\\_sensors.html](http://standards.ieee.org/events/multimedia/iot_mems_sensors.html)).

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# Finding and fixing failures at the package level

By Winfield Scott *[Evans Analytical Group]*

**A**dvanced semiconductor processes are enabling more compact, lower-power devices created from smaller and smaller structures. When these devices fail, finding and analyzing the failure's root cause has become increasingly challenging. As little as one individual atom out of place can cause performance issues or defects in devices that may otherwise look as though they were built correctly, putting pressure on failure analysis teams to investigate, understand and resolve problems. Meanwhile, package failures have their own set of mechanisms, and require the same disciplined process, tools, methodology and workflow in order to find and fix them.

## Failure analysis challenges at the package level

System complexity continues to grow with the advent of package options ranging from system-in-package (SiP) and multi-chip module (MCM) to embedded silicon substrate, stacked die, through-silicon via (TSV) and copper (Cu) wire. Today's devices also increasingly feature multi-layer metal stacks, and packages are being produced in flip-chip and other advanced chip-scale form factors that introduce additional new failure mechanisms and associated analysis challenges. As with any other failure, those related to package issues may only occur intermittently, further complicating the challenge. Once the package is inside a system, new challenges are introduced that can vary widely by industry and application. Each functional element within the design may require specialized domain knowledge in order to fully understand a failure's root causes and mechanisms.

Failures involving chip-scale packages (CSPs) can be particularly challenging. As leading-edge CSP substrates move toward 12µm lines and spaces, vias as small as 50µm, and capture pads of 110µm or less – the size advantages that make them so attractive for cellphones and other handheld and wearable electronic products

– also make them fragile and susceptible to damage.

Meanwhile, manufacturing and assembly processes are being squeezed to tighter and tighter specifications, and new sources of variation continue to be introduced. There are unanticipated problems related to such dynamics as differences in scribe line test structures that can push a dicing operation over the edge. Failure mechanisms can be introduced at many different points during manufacturing and beyond, including prior to and during the qualification process when there can be damage from handling, incoming and outgoing quality control (IQC/OQC), socketing, and unbiased stress testing.

## Sample package failures

In general, most CSP failure mechanisms are initiated during reliability stress testing, while the root causes of other package failures tend to be during production or later, in the field. Some of the most common package failures include those associated with mechanical handling damage, die singulation, corrosion, and solder joint issues.

Handling-related defects are particularly common with CSPs, which are so fragile that even grabbing them with a tweezer can damage die edges, leading to a gross failure. Many CSPs have only a thin epoxy layer on the back side of the die to protect them during normal handling, and virtually any amount of mechanical stress can cause craters or cracks to the die and solder joints of CSPs where they are directly connected to the chip. Defects can also arise from impact damage, and even saw cuts or cracks that are so small as to seem harmless may propagate over time and temperature to become larger problems further into the package's lifecycle.

Another challenging package defect is die singulation in CSPs. Because CSPs are processed like a standard IC on a wafer, they are singulated just like other dies. Assembly houses often use a multi-step singulation process, beginning with laser singulation to pre-scribe the die, followed

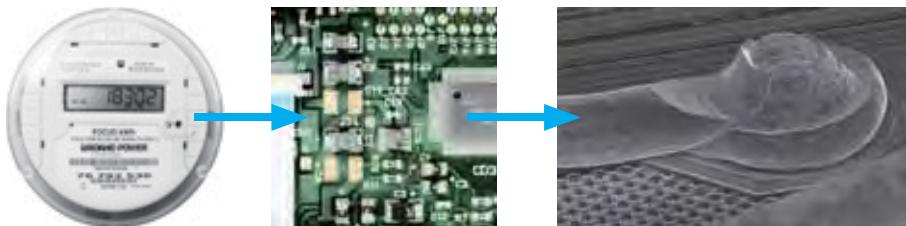
by use of a mechanical saw. If the ablation zone is too large and laser power too high, the melt zone may breach the edges of the die where the seal rings are located. This can cause direct damage or at least create a potential reliability issue down the road from delamination, which creates an ingress point for corrosion from moisture seepage.

Package issues related to corrosion are also a common problem. This is especially true for CSPs, because the previously mentioned protective coatings on the backside of the die can't completely eliminate cracks or separations to the active side of the device. Moisture can infiltrate through these cracks and separations on one or more of the CSP's die edges because they are completely exposed to the external environment. Corrosion also can occur at the bump pads, either where there is exposed under-bump metallurgy or through passivation cracks, and can also create problems in the redistribution layer (RDL) or at solder joints. The solder joints can have other problems beyond cracks, separations and corrosion, including voids and misalignment. There can be issues related to substrate warpage, poor solder and inter-metallic formation, and problems arising from reflow. Regardless of the suspected package failure mechanism, every analysis should take the same disciplined route toward root cause.

## Failure analysis: a methodical process

The failure analysis process must always be extremely methodical in nature. The analyst takes a failing unit and systematically narrows down the "where," "what," and "why" of what happened. This requires a series of steps that starts with the system and moves to the board, component, and on to the underlying failure mechanism ([Figure 1](#)).

The process should include both electrical and physical analyses in order to most effectively identify root causes and associated failure mechanisms so that future failures can be prevented. A



**Figure 1:** A step-by-step process moving from a failing system, to a failing board, to a failing component, and on to the underlying failure mechanism.

system focus is imperative, spanning all electronics, materials, and failure mechanisms that might be occurring, all the way down to the IC transistor level.

Even if the initial suspicion is a package failure, bypassing full system-level analysis can be a costly mistake. Yes, CSPs are fragile and susceptible to certain types of failures, but all too often, what initially appears to be a package anomaly might actually involve other failure mechanisms that could have been caught much earlier with a top-down, system-level approach. The analyst who simply assumes that a CSP experienced a typical temperature cycle failure during an unbiased reliability stress test might miss crucial

evidence that a transistor was also damaged due to unrelated reasons.

At the same time, however, failure analysts can streamline the analysis process by gathering as much information as possible about what they are looking at, including how a good unit is built and is supposed to work, and any information about what failure mechanisms for which they should be looking. The process is similar to that of an emergency room medical doctor, who makes a quick assessment based on observed symptoms and answers to diagnostic questions, and then establishes hypotheses to prove or disprove, taking care not to narrow the investigation so early as to be painted

into an analytical corner. In the absence of clues, the analysis may need to start with a broad look at the entire package including all corners and edges. With a little history of the failure and its electrical failure signature, however, the team can potentially skip certain steps and go directly to key areas of interest.

When creating the failure analysis plan, the first step is understanding the problem. What device is failing? What is the package type? What is the failure mode and rate? How many samples are available for failure analysis, and what is the failure's origin and history? The next step is to determine the scope of analysis – is the goal to learn root cause or just classify the failure (i.e., whether package- or silicon-related), and should the analysis extend to risk assessment, including the possibility of going back to the wafer fab or package assembly house to implement corrective action? The final step is to plan the analysis and schedule resources.

Using a meta-loop process, analysts can then systematically test each failure hypothesis, look for evidence to confirm it, and/or gather more information with

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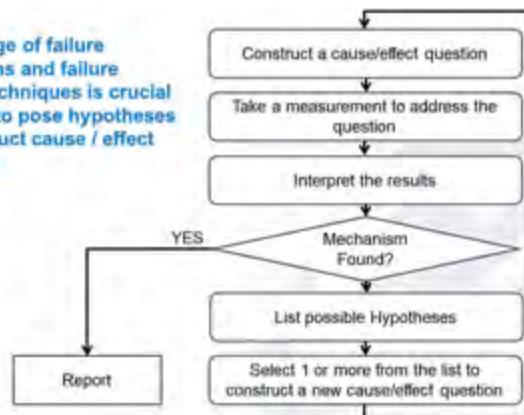


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which to propose a new hypothesis. During each test, the analyst is asking a question – do I have a package integrity problem? A wire bond problem? A die attach problem? Applying short-loop techniques repeatedly throughout the analysis will deliver the underlying failure mechanism (**Figure 2**).

**A knowledge of failure mechanisms and failure analysis techniques is crucial to be able to pose hypotheses and construct cause / effect questions.**



**Figure 2:** A meta-loop analysis process flow to identify underlying failure mechanisms.

In general, it is always best to start the analysis with non-destructive (electrical) testing, including electrical failure analysis, before moving to destructive (physical) failure analysis, which requires dis-assembly of the sample to get a picture of the failure site and mechanism. System characterization will provide a good look at the failure's electrical parameters, which helps to localize the failure and determine next steps for deeper investigation. The analysis then moves to the board level for isolated electrical data that localizes failures to a PCB or component, and then on to the component level to analyze ICs and discrete components while looking for the root causes of the failure.

## The right tools for the job

A number of tools should be at the analyst's disposal in order to most effectively diagnose and resolve package issues. Beginning with tools for non-destructive investigation, the particle impact noise detection (PIND) test is an excellent way to assess cavity packages, and is essentially a process of shaking the sample and listening for loose particles inside. Fine and gross leak testing are both used for evaluating the integrity of hermetic packages. Gross leak testing involves dropping the package into hot fluid and monitoring for bubbles as gas exits any cracks, while fine leak testing is performed by pressuring the sample with helium, placing it in a vacuum, and measuring the amount of leaking gas. Additionally, 2D

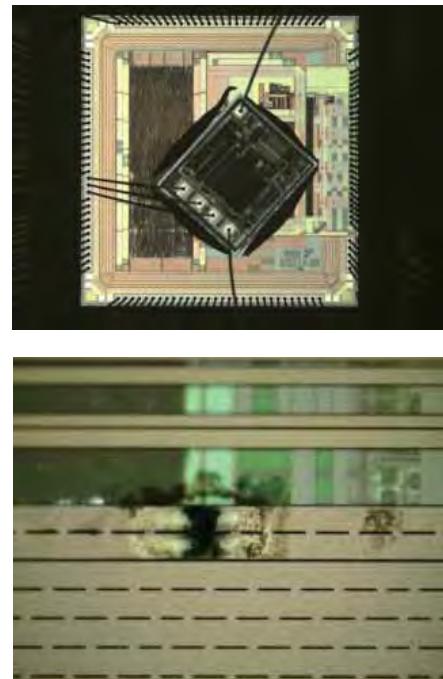
or 3D x-ray imaging is useful for analyzing handling-related defects and provides a look at bond wires, die bumps, detached fillets, substrate package traces, and other package elements to prove whether an initial package integrity hypothesis is true or not (**Figure 3**).

Another important tool for package testing during the non-destructive analysis phase is scanning acoustic microscopy (SAM), which is used in conjunction with other visual examination methods. It works through the use of ultrasound waves to detect changes in a materials' acoustic impedances that, in the case of a failing package, would indicate voids, delamination, or underfill problems.

Time domain reflectometry (TDR) can be used to help determine whether an open/short defect is in the package or at the interface to the die. TDR involves transmitting a high-frequency pulse through the sample, measuring the reflections, and comparing them to those produced by a standard device. These and other tests can help to determine whether a defect is in the package or at the interface to the die.

Other non-destructive optical testing tools include filtered polarized light inspection, as well as backside inspection using reflected IR imaging. This can help with the observation of die singulation issues, for instance, as well as corrosion.

Based on the electrical failure signature and initial non-destructive testing results, the analysis will generally be pointed toward a die edge, pad region, or other area in the circuitry, and hypotheses will be developed that require further investigation through physical failure analysis. At this point, internal visual inspection using low- and high-magnification optical microscopy is often used to further localize the problem. In the case of corrosion, for instance, these imaging tools can reveal evidence of discoloration or residue. Optical and scanning electron microscope (SEM) inspection will also help the analyst to understand morphology and electrostatic discharge (ESD) issues, and can be combined with material characterization tests to identify foreign materials or corrosive byproducts, such as chlorine, that would be

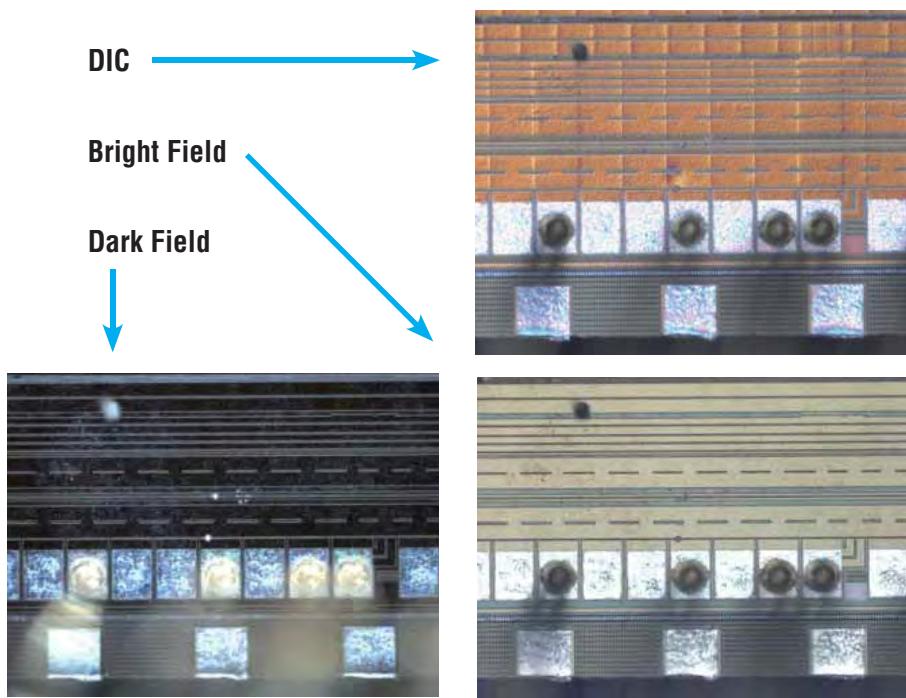


**Figure 3:** Low- and high-magnification microscopes can be used to visualize a package's wires and wire bonds, passivation cracks, electrical overstress and corrosion.

indicative of problems related to moisture infiltration.

Other important tools include backside infrared (IR) thermography and other backside laser inspection techniques, bright-field light microscope illumination to better visualize the area of interest against a dark background (**Figure 4**), and focused ion beam (FIB) mill cross-sectioning to look at joint profiles with SEM and other higher-resolution instruments.

Once the failure has been localized, the final step is to assess the risk of future failures and whether corrective action should be taken. As an example, CSP qualification lots are often invalidated at an unknown point in today's multi-step stressing process, requiring the supplier to start this process all over again. The resulting delays can be particularly problematic because of the pressure to hit milestones in an industry with extremely sensitive launch cycles. If, for instance, the failure analysis process reveals that cracks from improper handling are originating upstream at an assembly house where the devices are diced and bumped, it is then possible to institute an inspection process for all outgoing devices. This process can occur at the assembly house, including 100% top and bottom visual inspection. By doing this, the supplier can screen out all damaged parts before stress tests even begin, eliminating the problem before it starts. Failure analysis that leads to corrective action is increasingly



**Figure 4:** Bright-field microscopy is used to illuminate bond wires and other package elements against a dark background. In the top right image, the addition of differential interference contrast (DIC) is used to further improve visualization of a bond pad where electrical overstress has occurred at the input pin under the metal bus.

important given the dynamics of today's multi-tiered semiconductor supply chain.

### Summary

Electronic system failures are becoming increasingly expensive and challenging problems to solve, especially with the trend to smaller, more complex systems that are built with devices manufactured using advanced technology processes and packaging. Finding and fixing system errors whose root causes lie in today's advanced packages can be especially daunting. It requires a comprehensive, multidisciplinary electronic system failure analysis methodology and workflow that starts by considering all possible root causes from the component to system level, and then leverages specialized expertise and a variety of advanced equipment and toolsets to identify the failure mechanism and determine how to avoid it in the future.

### Biography

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# RF requirements and spring probe development for semiconductor test

By Jason Mrozckowski, Nadia Steckler [[Xcerra](#)] and Tony DeRosa [[Everett Charles Technologies](#)]

The vast array of semiconductor applications translates into an equally diverse set of challenges for test engineers. However, there are two constant drivers that permeate the industry: smaller pitches and higher signal integrity. High bandwidth signal paths and low-inductance power delivery are essential for testing the next-generation of RF devices.

Several factors can impact signal integrity, such as contactor and performance board design, and material selection. However, a successful test strategy must start with consideration of contact technology used to interface the device lead. Spring probes are the technology of choice for most applications when considerations also include mechanical attributes such as reliability and wear, as in high-volume test applications. An effective spring probe design must address the balancing act between electrical and mechanical performance. Developing a spring probe capable of 40Ghz+ bandwidth (@ -1dB) while providing adequate spring force and compliance, not only involves extensive electrical and mechanical simulation, but also advanced manufacturing techniques.

## RF device requirements

Many of today's devices require RF consideration during the test hardware development phase. The wireless evolution has given rise to a vast array of devices that transmit, receive and convert high-frequency RF signals. Many electronic products we use in everyday life require multiple RF devices to make communication to the outside world possible. The RF device chain includes low-noise amplifiers, filters, analog-to-digital converters, RF switches, and power amplifiers. Additionally, the variety of protocols make the number of unique devices astronomical. For instance, wireless networks have several devices depending on the protocol: 802.11a, b, g, n, and ac. Some of these devices operate at 2.4GHz and others that operate at 5.8GHz. Smartphones include LTE, GSM, WCDMA,

HSDPA, and EDGE basebands, that operate just under 1GHz to 4GHz. WiFi devices operate at 2.4GHz and 5.8GHz, while Bluetooth® devices operate at 1GHz and 2GHz. Wireless networks are now including more device technologies than ever before to accommodate the technology needs of the Internet of Things (IoT). Printers, cameras, tablets, appliances and cars are incorporating RF devices to allow wireless communication of data, current status, and warning conditions. Industrial, scientific, and medical wireless networks are commonplace and critical to efficient system performance and monitoring. All of these applications depend on RF semiconductor devices to function.

RF requirements of today's devices range from sub -1GHz (i.e., < -1GHz) up to 86GHz. In the future, devices are expected to reach Terahertz speeds. Besides the sheer speed of RF devices, there are other requirements that make testing a major challenge. These include low noise figure, precise impedance matching, and efficient power delivery. Because of the small amplitude of input signals and power efficiency requirements, it's critical to deliver clean and accurate signal inputs to RF devices.

Power amplifiers are either matched-impedance or low-impedance. Often they require external matching components selected to tune them to specific frequencies of operation. Today, power amplifiers have 20dB of gain with 50% efficiency in band. Soon they will require double the gain with 70% efficiency. Low-noise amplifiers (LNAs) receive extremely small signal levels and must decipher the signal from background noise. To do so requires a very low noise floor or low noise figure value (1dB and below today). Soon LNAs will need to be more sensitive, including noise figure values of <0.25dB.

Test results can limit the specifications that can be published for an RF device. Ideally, RF devices must act as if they are soldered into the end application while in the test environment. For example, if the test environment is noisy, then it may

limit a noise figure specification. If an end application or evaluation board results in a noise figure of 1.0dB, but the test environment noise figure is 1.5dB, then the published specification for the device will have to be 1.5dB. If a competitor can test in a lower noise environment and reduce the specification guard band, then a customer's comparison of the specifications on paper may limit the market available for the device manufacturer. For this reason it's essential to have a transparent interconnect from the test equipment to the device under test (DUT) during high-volume semiconductor test. The spring probe design is critical to achieve transparency. Impedance match, high isolation, and low inductance are necessary to keep the spring probe from being the performance bottleneck in many of today's RF test applications.

## Critical design features

The design features of the spring probe are very important, but not the sole contributor to RF performance. It's also critical to choose the proper probe design for the given package configuration. Package features that must be considered to apply the proper spring probe design are the pitch of the package, the type of the package, and the ground locations. A spring probe that is transparent for one package might be a bottleneck for another package. The diameter of the spring probe, the spacing between spring probes, and the socket material type are all variables that impact the impedance, insertion loss, and inductance of the spring probe.

A spring probe that is matched to  $50\Omega$  at 0.5mm pitch will have a higher impedance at 1mm pitch. Historically, spring probe mechanicals resulted in a slightly higher impedance than ideal for single-ended applications and a slightly lower impedance than ideal for differential applications. Attempting to achieve the desired impedance leads to increasing spring probe diameters for single-ended applications and decreasing spring probe diameters for differential applications—a contradictory requirement that may exist in the same device/package.

Today's pitches are such that flat probe technologies provide the best compromise of impedance in both single-ended and differential applications. The spacing of fine-pitch BGAs and QFNs provide optimal  $50\Omega$  match, and the smaller effective diameter of a flat probe vs. a barrel probe increases the impedance providing a better  $100\Omega$  impedance match for differential signaling. Ideally, spring probes would be designed for the application and the probe diameter would change based on the ground signal configuration, pitch, and signaling methodology (differential vs. single-ended). Practically speaking, this is impossible. High-volume manufacturing efficiencies would be impacted by the variety of probe types and the resulting maintenance challenges. At the mechanical level, spring diameters and force requirements push designs past safety factor limitations to achieve the geometries required for electrical performance.

The compromise between electrical and mechanical performance must always be considered when designing an RF spring probe. The attributes of flat probe technology allow spring probes to reach an acceptable balance point. Everett Charles Technologies'

(ECT) ZIP™ 0 is an example of a flat spring probe architecture and is shown in **Figure 1**. The probe has very good RF characteristics and has been proven to provide high insertion counts. The external spring allows shorter test heights and lower inductance. The sliding contact surfaces keep internal resistance low while providing long insertion life. The flat components have only external surfaces resulting in a more uniform plating with better adhesion than tradition Pogo-style probes in which internal surfaces of a barrel must be plated. Additionally, the base material is resistant to wear against rough and contaminated packages. Of course, a probe that meets all of the technical challenges will not be widely used if the cost is not within the window of acceptance. Therefore, the manufacturing process must support a low-cost probe, and the process must be robust and repeatable.

### Developing a high-bandwidth spring probe solution

Architectural features of a spring probe profoundly affect its RF performance. When designing a spring probe, the goal is to hit RF targets on the first design. Simulation

tools can be extremely valuable to predict, understand, optimize the results, and shorten the time-to-market. Equally important are RF measurements of the probe. Vector network analyzer (VNA) data is used to fine tune the probe models so that simulation results align with actual measurements. Once accurate models are in place, the probe's physical features can be adjusted to achieve desired performance levels.

**Simulation.** The simulation process begins by translating the physical design features of a spring probe into its equivalent electrical model. A precise model is essential to accurately simulate waveforms and predict RF performance. A 3D EM (electromagnetic) simulator is used for the design of complex RF electronic circuit elements, such as a spring probe. It simulates the magnetic and electric fields at many nodes in the model.



**Figure 1:** ECT's ZIP 0 RF spring probe.

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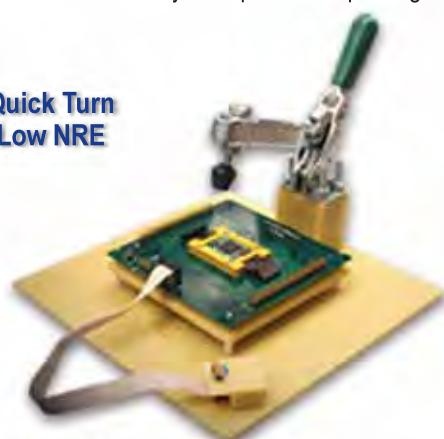
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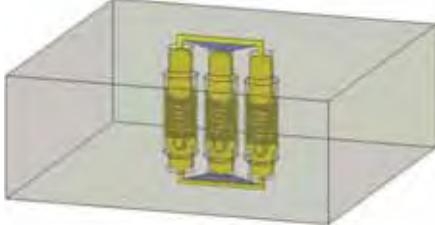
The results can be viewed in the frequency and time domain through s-parameter extraction.

A successful simulation requires a practical mechanical model to accurately predict RF performance levels without simplifications that affect accuracy. The individual probe components and their interaction with one another must be modeled correctly. To do this, the design files from the mechanical design team are converted to standard ACIS text (SAT) format that is fed into the 3D simulation tool. Then key variables that have a direct impact on performance are incorporated into the model, such as dielectric material (in final application), loss tangent, height (path length), pitch (distance between signal and return paths), and material properties.

To more accurately represent the probe's performance in various digital and analog applications, different simulation configurations are modeled. **Figure 2** shows an example of a GSG (ground signal ground) arrangement typically found in high speed analog package designs. The GSG configuration is correlated to the VNA measurement.

#### VNA measurement.

A vector network

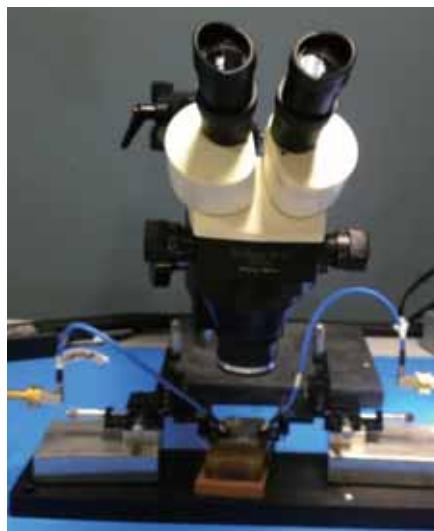


**Figure 2:** GSG configuration of ZIP 0 in 3D simulation.

analyzer emits a sine wave voltage at each port and through the DUT. The VNA measures the amount of energy transmitted through the DUT and reflected by the DUT at different frequencies. It then provides these results in scattering-parameter (S-parameter) format from which we extract insertion loss, return loss, etc.

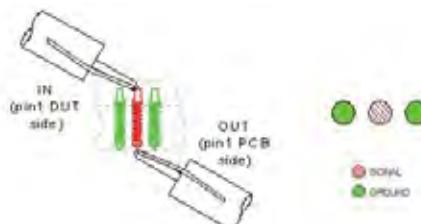
In addition to the VNA, the station needs several pieces of equipment to be effective: light source, microscope, a spring probe fixture that duplicates the contactor cross-section, two manipulators with x, y and z movement capability, and the CPW probes (coplanar waveguide contact) in different configuration, i.e., GS, GSG, GSSG, and SG. **Figure 3** shows the probe station used in the lab.

**Method.** The setup for taking RF measurements of spring probes requires



**Figure 3:** VNA probe station.

custom-designed fixtures and delicate handling of ESD-sensitive equipment (**Figure 4**). Test port extension cables and air coplanar probes are connected and mounted to the VNA and probing station. The VNA



**Figure 4:** Setup for one-way through measurement of GSG configuration.

is powered "on" in advance for temperature stabilization and it is set to the frequency domain of interest. A full 2-port SOLT (short, open, load, thru) calibration is performed on the VNA using the calibration substrate per the manufacturer's recommended procedures. After verifying the calibration, the spring probes are placed into the fixture in GSG configuration. The VNA probes contact directly to the spring probes to accurately capture the RF characteristics of the spring probes.

THRU measurements are required for bandwidth and electrical delay analysis. OPEN measurements are required for capacitance analysis, and SHORT measurements are required for inductance analysis. When the VNA data is verified, it is imported into analysis software for S-parameters extraction. The S-parameters give a clear physical interpretation of the transmission and reflection performance of the device.

**Correlation.** Simulation results are correlated with empirical data based on the layout used on the measurement, (i.e., GS, GSG, GSSG or SG). The S-parameters are then extracted and compared in the 3D simulator software tool.

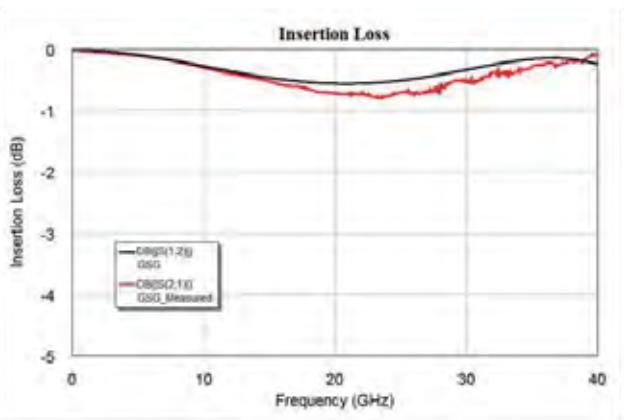
In order to match the VNA measurement, different modeling techniques are used in the 3D simulator tool. One technique involves modeling contact between probe components. It's critical to capture an accurate representation of the physical interaction between probe components under compression.

Impedance mismatch and cross talk (isolation) are two of the main concerns when designing a probe. Therefore, in order to get good signal integrity in designing a spring probe, we need a good understanding of the mechanical and electrical requirements of the test environment. Because the mechanical and electrical characteristics complement one another, considering them together yields good results when testing any product. **Figure 5** shows the insertion loss of ECT's ZIP 0 probe and compares measured to simulated. Correlation matches very closely over the entire frequency range. The low loss and high bandwidth confirm a well matched transmission line through the ZIP 0 probes in typical applications.

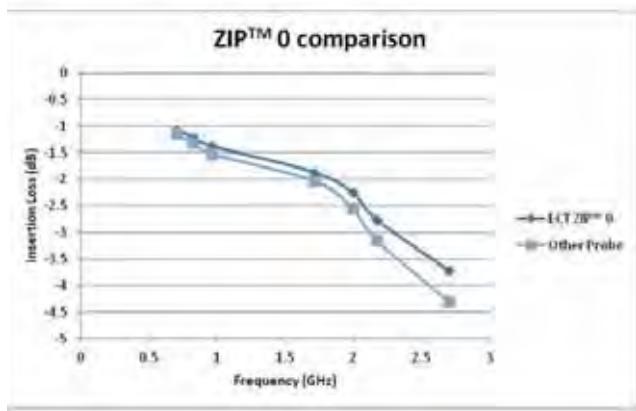
**Field Performance.** Simulating, optimizing, and measuring probe characteristics is important to bring a new spring probe product to market, but no amount of simulation or lab data can predict the performance in a high-volume production environment. Only customers can provide the essential final feedback that a design is successful. Shown in **Figure 6** is the RF performance of ZIP 0 compared to the competition. The result here includes the loss through the PCB, the probe and the device. The only variable compared in the figure was the probe technology used. This plot shows the benefits of the 40GHz ZIP 0 probe are not only noticeable for extremely high-frequency applications, but can also be realized for lower frequency RF applications.

#### Summary

The number of devices that require high-speed test is expanding rapidly. Both mobility and consumer applications are leading the push toward increased RF performance and smaller form factors. These two elements form the basis of a balancing act between electrical and mechanical spring probe design requirements. Flat probe technology with its unique architectural features and



**Figure 5:** ZIP 0 insertion loss, measured vs. simulation.



**Figure 6:** Field performance, ZIP 0 vs. a competitor's probe.

manufacturing processes has shown to be an effective option to achieve high RF performance and mechanical reliability. The use of finely tuned 3D EM simulation tools are instrumental in designing a RF spring probe. Accurate models predict performance and aid in defining the probe's mechanical features. Empirical measurement data validates performance and is used to make adjustments to the probe's simulation

models. Through the use of simulation and empirical data, ECT has developed a reliable spring probe suitable for many of today's RF semiconductor devices.

### Biographies

Jason Mrozczkowski received his MBA from the U. of St. Thomas and is a Signal Integrity Product Manager at Xcerra Corporation.

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# Silicon wafer integrated fan-out technology

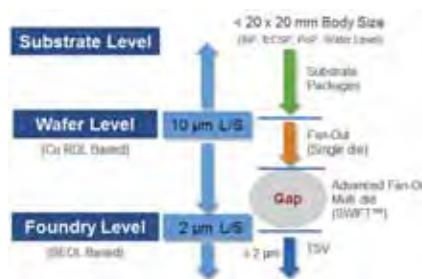
By Ron Huemoeller, Curtis Zwenger [Amkor Technology, Inc.]

The tremendous growth in the mobile handset, tablet and networking markets is fueled by consumer demand for increased mobility, functionality and ease of use. This increased demand, in turn, is driving an increase in functional convergence and 3D integration of IC devices, which require more complex and sophisticated packaging techniques. A variety of advanced IC interconnect technologies, including through-silicon via (TSV), chip-on-chip (CoC) and package-on-package (PoP), are addressing this growing need. In particular, emerging wafer-level fan-out (WLFO) technologies provide unique and innovative extensions into the 3D packaging arena.

As a platform, WLFO is designed to provide increased I/O density within a reduced footprint and profile for low-density, single- and multi-die applications at a lower cost. The improved design capability of WLFO is due, in part, to the fine feature characteristics associated with wafer-level packaging (WLP). This capability allows for the application of more aggressive design rules, compared with competing laminate-based technologies. In addition, the unique characteristics of WLFO enable the creation of innovative 3D structures that address the need for IC integration in emerging mobile and networking applications.

Design rules and 3D integration capabilities of traditional WLFO technologies, however, are limited by processes and equipment used for circuit patterning. For the most aggressive designs, TSV processes must be incorporated, which often exceeds the cost budget and design requirements needed for the device. Consequently, there is a gap between the design capabilities of WLFO and TSV that needs to be addressed.

**Figure 1** illustrates the gap for advanced fan-out applications where



**Figure 1:** IC package technology integration roadmap. Disparate die integration is needed on a single platform. To close this gap, Amkor has developed Silicon Wafer Integrated Fan-out Technology (SWIFT™) as an extension to the fan-out platform. SWIFT incorporates conventional WLFO processes with leading-edge thin-film patterning techniques to bridge the gap between TSV and traditional WLFO packages.

## Conventional wafer fan-out technologies

To appreciate the advantages of this technology extension, it is first important to understand the general process flow for conventional 2D and 3D WLFO packages and the limitations of these platforms, as they exist today.

**2D wafer-level fan-out.** The fundamental WLFO technology is a 2D configuration, based on embedding die into a molded wafer, also called “wafer reconstitution.” The molded wafer is processed through a standard WLP flow to create the final IC assembly structure. The active surface of the die is coplanar with the mold compound, allowing for the “fan-out” of conductive copper traces and solder ball pads into the molded area using conventional redistribution layer (RDL) processing [1].

By eliminating the conventional laminate substrate, and opting instead to leverage WLP's superior design and feature size capabilities, WLFO provides many benefits, including: 1) Increased I/O density; 2) Reduced form

factor (including z-height); 3) Improved electrical and mechanical performance; 4) Multi-chip capability; 5) Outstanding cost/performance capability (through co-design optimization); 6) Scalability within a heterogeneous assembly platform; and 7) Opportunity for advanced 3D structures.

Two-dimensional (2D) WLFO is well-documented as a robust and reliable WLP technology for electronic devices.

**Figure 2** illustrates a cross section of a typical 2D WLFO structure.



**Figure 2:** WLFO cross-section.

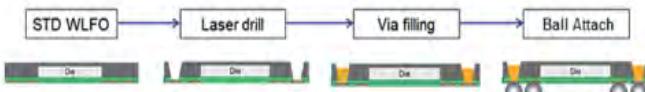
**3D wafer-level fan-out.** Standard WLFO technology can be expanded in the vertical (z) direction when connecting it as a 3D PoP structure, as shown in **Figure 3**. This is a common packaging technique used in mobile products to



**Figure 3:** 3D WLFO PoP package structure.

integrate application processors and memory devices [2]. Advanced laser and via fill processes enable the creation of 3D PoP WLFO structures.

The front side (i.e., active die side) RDL process for 3D PoP WLFO is nearly the same as standard 2D WLFO. However, a laser drilling (or equivalent) process is used to expose an RDL feature from the back side (i.e., the mold side) of the package to create through-mold via (TMV®) interconnects. **Figure 4** illustrates the key process steps for the 3D PoP WLFO fabrication process.



**Figure 4:** 3D WLFO key process steps.

Although the 3D PoP WLFO structure looks very similar to a conventional laminate-based TMV PoP (as shown in **Figure 5**), 3D PoP WLFO has additional technical merits due to WLP technology. For example, the WLP process uses much thinner conductive and dielectric layers compared with typical laminate substrate build-up technology. The resulting WLFO RDL stack-up has fewer parasitic elements, which provides improved electrical performance. In addition, eliminating wire bonds or flip-chip bumps provides the opportunity for cost reduction. And finally, the ability to thin WLFO packages while still in wafer form creates very thin package structures for PoP applications.

## Limitations of standard WLFO technologies

Limited line and space capabilities for the RDL fan-out structure are a key restriction of traditional WLFO. Typically, mask aligners image the photoresist and dielectric materials for WLFO packages. Because of mask aligners' limited depth-of-field, this patterning technique is highly dependent upon the topology of the surface to be developed. Planarizing spun-on liquid dielectrics and photoresists can be very difficult to control on a molded reconstituted wafer, especially when multiple layers of RDL are required. The surface topology is also affected by the inherent warpage associated with molded wafers. Consequently, it is very difficult to achieve fine resolution features of <10/10 $\mu$ m line/space on WLFO.

Additionally, it is difficult to create 3D structures for PoP and other 3D interconnect structures using conventional WLFO technology. The difficulty is due to the challenges of inserting or forming vertical connections within the molded wafer. Because the fan-out copper RDL is created post-mold, complicated laser drilling and copper plating techniques must be applied to the back side of the molded wafer to form 3D interconnects from the front-side RDL layer. An alternative approach is to mold prefabricated 2-layer substrate inserts within the reconstituted wafer [3]. This technique can, however, add significant cost and process challenges.

A final point about traditional WLFO



**Figure 5:** Comparison of 3D/PoP package structure; a) WLF0 type, and b) PCB type.

technology is that its overall yield is highly dependent upon the quality of the RDL build-up technology. Unlike traditional wire bond and flip-chip assembly on organic substrates, where die are placed on known-good substrate sites, WLFO die are

at the mercy of the inherent defect density of the wafer-level fan-out RDL build-up process. This “die-first” assembly flow requires very high RDL yield to avoid scrapping good die.



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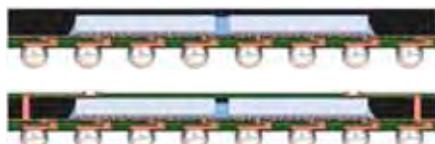
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## SWIFT technology

The new package technology is designed to overcome many of the issues associated with conventional WLFO technology. In addition, it provides increased I/O and circuit density within a reduced footprint and profile for single- and multi-die applications. The new technology's improved design capability is due, in part, to the fine feature capabilities associated with this innovative wafer-level packaging technique. It allows for the application of more aggressive design rules, compared with competing WLFO and laminate-based IC assembly techniques. In addition, the characteristics of the new process enable the creation of 2D and 3D structures that address the need for IC integration in emerging mobile and networking applications.

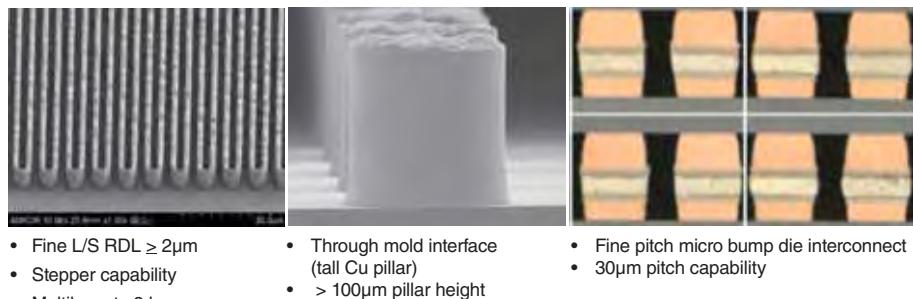
**SWIFT structure and attributes.** **Figure 6** shows cross-section illustrations of 2D SWIFT and 3D/PoP SWIFT dual-die structures. Although the package appears to be a typical fine-pitch flip-chip construction, it incorporates some



**Figure 6:** 2D SWIFT and 3D/POP SWIFT dual-die structures.

unique features not associated with conventional IC packages, including: 1) Polymer-based dielectrics; 2) Multi-die and large-die capability; 3) Large package body capability; 4) Interconnect density down to 2 $\mu\text{m}$  line/space (critical for SoC partitioning applications); 5) Cu-pillar die interconnect down to 30 $\mu\text{m}$  pitch; and 6) 3D/PoP capability using TMV or tall Cu pillars.

Key assembly technologies enable the creation of these distinctive SWIFT features and attributes. Features of 2/2 $\mu\text{m}$  line/space can be achieved using stepper photo imaging equipment, thereby enabling very high-density die-to-die connections required for SoC partitioning and networking applications where 2.5D TSV would typically be used. Fine-pitch die micro bumps provide a high-density interconnect for advanced products, such as application processors and baseband devices. In addition, tall Cu pillars enable a high-density vertical interface for mounting advanced memory devices



**Figure 7:** Key enabling SWIFT technologies.

on top of the SWIFT structure. These enabling technologies are illustrated in **Figure 7**.

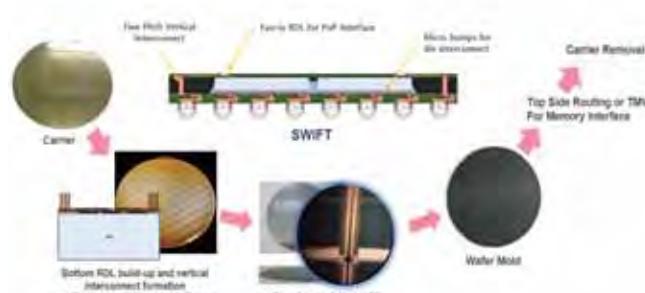
**SWIFT process flow.** Attributes of the new technology are realized by applying a process flow that incorporates both flip-chip assembly and wafer-level processing techniques. The process flow is shown in **Figure 8**.

High-density RDL build-up is performed on a carrier platform using conventional WLP technology. Fine-line and space routing can be applied for high-density interconnect applications. The SWIFT processes' small feature size

capability allows for a reduced package footprint. Tall Cu pillars or TMV solder balls form the vertical interconnects. The flip-chip die is attached to the high-density RDL build-up structure and encapsulated with epoxy-based molding compound. Wafer back-grind creates very thin structures. For 3D/PoP constructions, the solder balls are exposed using TMV technology [4]. Or, for fan-in PoP applications, top-side routing is applied using traditional wafer RDL build-up techniques. After carrier removal, solder balls are attached to the BGA pads and the molded wafer is singulated.

## SWIFT v.s. WLFO technology.

**Table 1** compares some key attributes of the new process versus traditional WLFO technologies. Although the new approach requires Cu pillar processing at the silicon wafer level, it enables the die to be attached to



**Figure 8:** SWIFT process flow.

Key Attributes	SWIFT	WLFO
Die Wafer processing	Cu Pillar	None required
Die dedication	Die last (on Known good RDL)	Die first
Die attach	High accuracy FC bond on known good RDL site	High accuracy D/A (slow)
Patterning	Photo (stepper)	Photo (mask align or stepper)
Line/ Space	2 - 10 $\mu\text{m}$	6 - 10 $\mu\text{m}$
# RDL Layers	1 - 3	1 - 2

**Table 1:** SWIFT vs. WLFO process.

a pre-inspected known-good RDL structure with very fine-pitch interconnect features. This, in turn, helps ensure known-good die (KGD) are not subjected to any yield loss associated with the RDL build-up process. In comparison, for WLFO, KGD are dedicated prior to RDL creation, which increases the risk for die yield loss because of the inherent defect density of the WLFO process. In addition, traditional WLFO technology requires very high-accuracy die-attach equipment and careful process characterization to minimize the die shift and molded wafer warpage issues that are associated with WLFO processing. Finally, because the SWIFT RDL structure is built upon a flat carrier, the dielectric topology can be controlled to allow fine resolution circuit formation in multiple layers. In comparison, conventional WLFO has limitations on RDL layer count and line/space capability because of the wafer warpage and topology variation intrinsic to molded wafer processing.

## Summary

A state-of-the-art fan-out structure can bridge the gap between TSV and traditional WLFO packages. SWIFT technology is designed to provide increased I/O and circuit density within a reduced footprint and profile for single- and multi-die applications. The distinctive characteristics of this technology are due, in part, to the fine feature capabilities associated with this WLP technique. These capabilities allow for much more aggressive design rules to be applied, as compared with traditional WLFO and laminate-based assemblies. In addition, the new technology enables the creation of advanced 3D structures that address the need for increased IC integration in emerging mobile and networking applications.

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# High-throughput wafer edge inspection and monitoring for advanced wafer-level packaging

By Prashant Aji, Cathy Perry-Sullivan, Sumanth Sood [KLA-Tencor] and Thomas Uhrmann, Julian Bravin, Jürgen Burggraf [EV Group]

**W**ith an increasing demand for higher performance and smaller form factor devices, the last few years have seen advanced wafer-level packaging (WLP) and through-silicon via (TSV) technology move to the forefront of semiconductor industry roadmaps, poised for significant future growth. Advancements in high-throughput process control and monitoring tailored for advanced WLP is seen as a key enabler to integrate these packaging technologies into high-volume manufacturing (HVM) process flows and to meet lower cost-of-ownership targets.

In the overall 2.5/3D process flow, device wafer temporary bonding and debonding processes are inevitable. Temporary bonding enables reliable backside processing of devices essential for later stacking of devices in a 3D or 2.5D fashion. The different steps in the temporary bond process flow include coating of the thick bonding adhesive, temporary bonding, device wafer thinning, backside processing, and eventual debonding of the thinned wafer from the carrier substrate. The total thickness variation (TTV) and wafer edge quality are two critical areas of concern on these device wafers after thinning. Chips, micro-cracks and delamination during device wafer thinning pose significant challenges to processing temporarily bonded wafers. Such defects propagate during subsequent process steps and can result in significant yield loss. Several device wafer edge protection techniques have been developed including edge-trim (pre- or post-bond) and oversized carriers, but these techniques significantly modify the wafer edge profile with the end result being non-compliant to SEMI Standards [1].

Device manufacturers are also interested in closely monitoring key dimensions of the device and carrier wafers including, but not limited to, the total height of individual wafers and the bonded stack, as well as the device wafer inset. For example, it is crucial to detect excessive temporary adhesive that appears as a protrusion at the

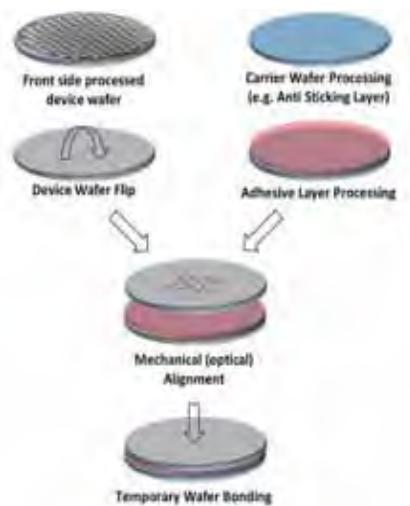
device-carrier bond line. Likewise, it is also important to know whether there is any gap between bonded wafers (undercut) that will significantly increase the chance of breakage during backgrinding or subsequent high-temperature processing.

All the above scenarios present unique challenges and require significant changes in process control and monitoring strategies to ramp-up device wafer yield. One such strategy is implementation of inspection and metrology of the edge of these bonded wafers. For traditional semiconductor manufacturing steps, edge die yield is becoming critical as fabs attempt to save costs and reduce wafer edge exclusion. As a consequence, wafer edge defect inspection and metrology applications are now critical components of the overall yield management strategy in advanced semiconductor fabs [1]. The extension of these automated, high-throughput edge inspection and metrology techniques to WLP applications is important in helping ramp the bonding technologies for HVM.

In the past, the most common way for inspection, review and metrology of a bonded wafer edge was using optical microscopes—a slow and operator intensive strategy. In recent years, edge inspection and metrology of bonded and thinned wafers have emerged as important uses for both memory and logic IC manufacturers. Current solutions for automated edge inspection and metrology cannot handle bonded wafers well because bonded wafers do not have SEMI standard profile shapes.

In this paper, we introduce KLA-Tencor's CV310i advanced wafer edge inspection, metrology and profiling system tailored for advanced WLP. The system enables high-throughput simultaneous wafer edge inspection and metrology for comprehensive data collection from all zones comprising the wafer's edge: top and bottom near-edge; top and bottom bevel; and apex. We discuss the inspection and metrology use cases from a temporary wafer bonding process flow to demonstrate the capability of this system for process control and yield improvement.

## Temporary wafer bonding

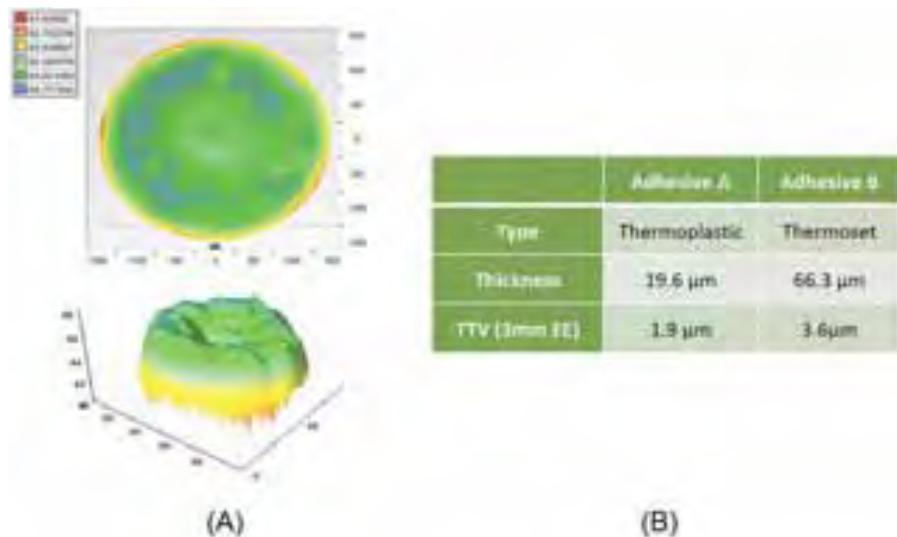


**Figure 1:** Schematic for a temporary bonding process flow for multilayer adhesives.

**Figure 1** shows a schematic process flow for temporary bonding using a multilayer adhesive system, which is a typical case for thermoset materials. Besides thermoset materials, the second common class of adhesives being used in this study is thermoplastics. Both materials are very similar to process. The device wafer with topography is mounted face-down onto a second wafer called the carrier, which can be silicon, or in some cases, glass. The ability of an inspection and metrology system to cope with both carrier wafer materials is essential. Furthermore, the adhesive system has to be applied thick enough in order to embed the device wafer topography completely. At the same time, the material should not be too thick, as adhesive uniformity would become worse. Another fundamental property of the adhesive system is the rigidity during backgrinding. The temporary bonding adhesive must also be compliant with the vertical forces, as well as the shear forces. Crosslinked adhesives, such as thermoset materials, are slightly compressible at room temperature, while thermoplastic

adhesives do not show this effect. Prior to grinding, inspection of the temporary adhesive thickness and TTV is essential. For backgrinding, any local thickness variation of the temporary adhesive will be transferred to the device wafer, leading to difficulties during via reveal process, and thereby adding cost to the backside processing.

Additionally, TTV variation could also lead to uneven device wafer-edge thickness, which could compromise the edge quality. In the case of thermoplastic adhesives, curing is critical to driving out all solvents from the thermoplastic adhesive. Alignment of the carrier and the device wafer is critical and needs to be monitored because the valuable device wafer needs to be supported at all times during grinding, polishing and backside processing. Generally, mechanical alignment inside the bond chamber, generating wafer-to-wafer alignment around  $\pm 50\mu\text{m}$ , is fine for the presented process flow. Alternative process flows may require a more accurate optical wafer-to-wafer alignment. In particular, as more advanced design nodes are applied for backside processing in combination



**Figure 2:** a) Post-bond adhesive thickness map for adhesive B with 66.3 $\mu\text{m}$  and a TTV of 3.6 $\mu\text{m}$ -3mm edge exclusion; b) Average thickness and TTV data for bonded wafers.

with standard edge trimming of the device wafer, accurate alignment is needed. Wafers are subsequently bonded under vacuum applying standard conditions for the thermoplastic adhesive that is used.

### Device wafer edge protection

Device manufacturers employ various types of device wafer edge protection schemes to ensure that the device wafer edge stays safe during the thinning and subsequent processing. The two most

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common techniques are: 1) use of a slightly oversized carrier, typically 1mm larger than the device wafers; or, 2) the device wafer is pre-trimmed at the edge. In the case of an oversized carrier bonded to a standard diameter device wafer, if the device-to-carrier concentricity during the bonding is off, the carrier may not be able to protect the entire device wafer edge. For our study, we went with the more common device wafer edge trimming approach, which has been shown to be most effective for edge protection [2].

## Setup

300mm bare silicon wafers were processed through the edge trimming, temporary bonding, and thinning processes to generate inspection and metrology data. Some process conditions were changed and defects were introduced to highlight specific excursions and defects typical for the temporary bonding process flow.

**Edge trim and temporary bonding.** The device and carrier wafers were 300mm SEMI spec silicon wafers with a thickness of 775 $\mu\text{m}$ . Prior to bonding, some of the device wafers were edge trimmed using a Disco dicing saw. Wafers were trimmed using two types of edge trims, including: 1) ET1: 1.75mm width, 200 $\mu\text{m}$  depth; and 2) ET2: 0.4mm width, 200 $\mu\text{m}$  depth.

The wafer edge trim profiles were collected using the CV310i edge profiler. Following the edge trim, wafers were bonded on an EVG®850 TB XT to silicon handle wafers using two different temporary bonding adhesives: 1) Adhesive A: thermoplastic adhesive with 20 $\mu\text{m}$  thickness; and 2) Adhesive B: thermoset adhesive with 65 $\mu\text{m}$  thickness.

Temporary bonding and metrology of the post-bonding TTV was performed on EVG's 850TB XT-frame. The system is capable of processing oversized glass and silicon carrier wafers (i.e., those not in compliance with SEMI Standards). After temporary bonding to silicon, most of the wafers were subjected to the grinding process to attain typical thicknesses used in production today of 50 $\mu\text{m}$  and 90 $\mu\text{m}$ .

**Post-bond TTV measurement.** A metrology module can be added to the bonding tool, capable of thickness and TTV measurements from different layers of the bonded stack, as well as detecting bonding voids in one single measurement run. The thickness data is collected using non-contact infrared (IR) and white-light (WL) interferometric sensors, making the solution fully compatible with both glass and silicon

carriers. A high-speed scanning stage enables an inspection module throughput that supports 100% inspection of all processed wafers without compromising throughput of the automated temporary bonding system. Typical measurement resolutions of 0.5mm<sup>2</sup> allow for an accurate characterization and yield detection, without influencing the system throughput [3]. **Figure 2** shows the post-bond TTV map for adhesive B, along with data from both adhesives.

**Background.** After bonding, grinding of the test wafers was done by Disco. A standard multi-spindle grinder was used, where most of the wafer thickness is subtracted using a coarse grinding step. Subsequent fine grinding further reduces the device wafer's thickness and at the same time is soft enough to reduce surface defects. Because no more backside processing steps have been done in this test, no further chemical mechanical polishing step was done. Instead, a final dry polishing step was done for particle reduction and further surface flattening.

## Edge inspection and metrology

Edge inspection and metrology was performed on KLA-Tencor's CV310i edge inspection and metrology system tailored for advanced WLP applications. This system captures 5mm of wafer top side, edge and bottom side in one scan. The system utilizes three different channels for defect binning and is capable of 0.5 $\mu\text{m}$  sensitivity. The CV310i has an integrated edge profiler for wafer edge shape and is capable of handling wafers that are not compliant with SEMI Standards. **Figure 3** describes the different defect inspection, monitoring and review uses cases for the temporary bonding process flow.

### Edge profile and metrology.

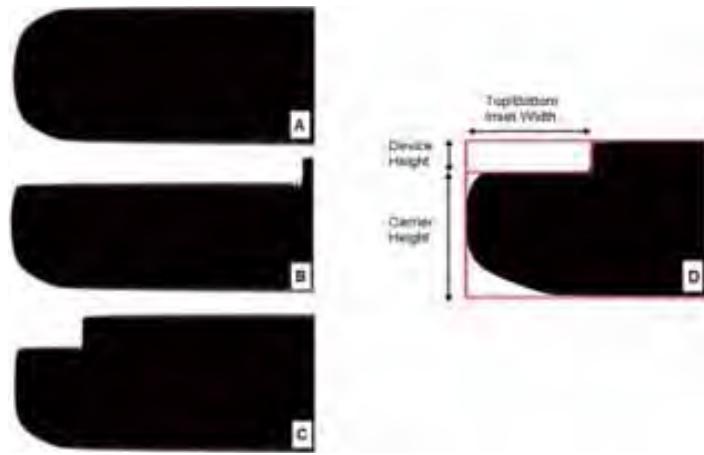
During the edge inspection run time, several edge profile images are captured from the wafer under inspection using the integrated edge profiler. **Figure 4a-c** shows the edge profile images of three different wafers (no edge trim, 400 $\mu\text{m}$  edge trim width

	Edge Inspection, Metrology and Review
Edge Trim	Wafer height, trim width and height metrology Monitor edge trim profile Inspection for edge chips and contamination
Adhesive post	Coat and edge bead profile Coat coverage defects at edge Bevel and back side contamination
Bond	Carrier-to-device concentricity Carrier-to-device notch alignment Adhesive squeeze-out Edge voids/delamination
Background & Polish	Device wafer thickness and edge profile Chips/Cracks Slurry residues
Pre-Bond	Edge delamination Back side residues and particles

**Figure 3:** Typical inspection, metrology and review use cases during a temporary bonding process.

and 1.75mm edge trim width) used in this study. The number of edge profile sites is set by the user. The system then automatically detects numerous salient points, such as device wafer top, device wafer apex, etc. From the determined salient points, multiple wafer edge attributes (as shown in **Figure 4d**) are measured for each individual edge profile site.

Using the edge profile images from different points across the wafer circumference, the user can quickly determine trim quality in non-bonded wafers. Edge profiling and inspection is essential to edge trim process characterization for TSV wafers. Edge profile data can be used to determine the optimized edge trim parameters and replacement frequency of the edge trim blade before it gets worn out. Additional wafer attributes such as wafer thickness, trim width, and device-to-carrier concentricity can be calculated and



**Figure 4:** Wafer edge profiles from a CV310i edge profiler for a) Full wafer thickness, b) 1.75mm edge trim, and c) 400 $\mu\text{m}$  edge trim width; d) Edge trim profile for a bonded wafer stack with the device wafer thinned to 50 $\mu\text{m}$ .

compared within the wafer lot. **Figure 5** shows concentricity measurement based on a bonded and thinned wafer stack where the trimmed device wafer was slightly offset from the carrier. The center of the image shows the panoramic view of the wafer's edge showing max offset at 180°. If the device wafer is significantly off from the

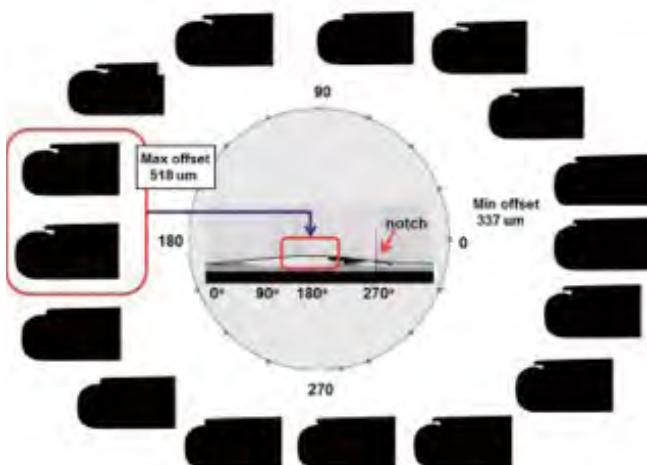
carrier wafer, it can cause the fragile device wafer edge to be exposed and broken during subsequent steps.

Inspection of edge trimmed wafers is also critical because particles from the device wafer edge trim process can transfer to the bevel and backside and become embedded in the bond chamber chucks, causing issues in the bonding process and impacting yields.

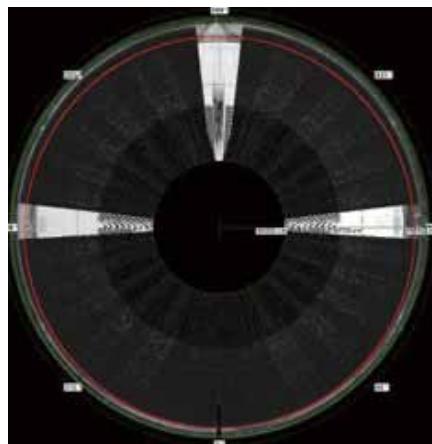
Another important edge usage case for temporary wafer bonding is to identify any edge delamination from CMP and device wafer backside processing. The CV310i is capable of detecting wafer delamination between the device and carrier wafer (**Figure 6**). The wafers are typically scrapped if delamination is detected to avoid the risk of wafer breakage during later process steps causing contamination in downstream tools.

The delamination location relative to the notch can be used to determine the root cause.

**Edge inspection and review.** Finally, it is important to detect any particles, chips and cracks from edge trimmed and bonded wafers, as well as collect images of the defect locations. Problems during handling and transportation of edge-trimmed wafers



**Figure 5:** Device-to-carrier wafer concentricity measurement for a thinned device wafer bonded to carrier.

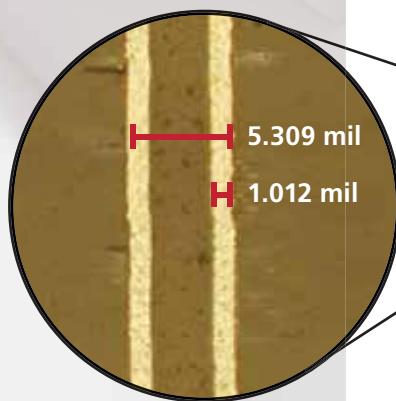


**Figure 6:** Polar view image of the bonded wafer showing three edge delamination locations.

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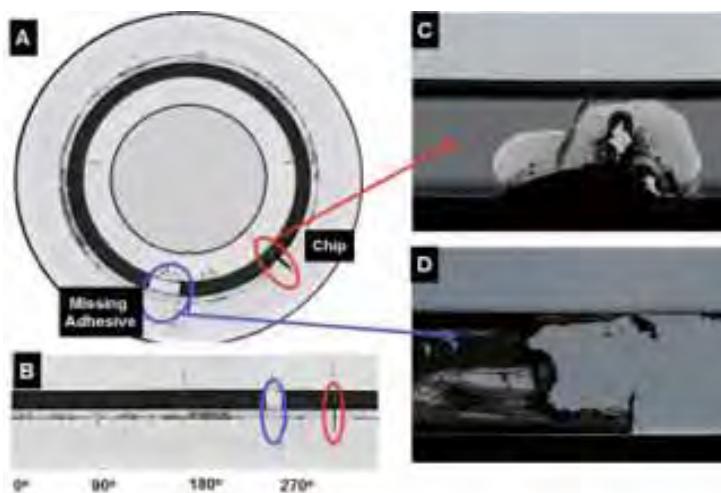
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within FOUPs can cause chips, cracks and particles in the edge trim area. CV310i can detect defects with sensitivity up to  $0.5\mu\text{m}$  at high throughput followed by automated defect review (ADR). Three signal channels (specular, phase, and scatter) provide a high sensitivity advantage by focusing on specific

defect types. After channel selection is confirmed, automated defect binning enables separation of various defects of interest into different bins. The defect map and locations can be output as a polar map, as well as in a panoramic layout as shown in **Figure 7**.



**Figure 7:** Bonded wafer defect inspection and review results, including a) Polar map showing edge defects; b) Panoramic view of the same wafer; c) Defect review image of a chip-in-carrier wafer; and, d) Missing adhesive review image.

## Summary

We have demonstrated the need for edge inspection and metrology, as well as monitoring total thickness variation (TTV) of the bonded and thinned device wafers in the 2.5/3D process flow. We presented wafer edge defect inspection, color review, and metrology

use cases from KLA-Tencor's CV310i automated edge inspection tool. These studies proved the capability of edge inspection and metrology for monitoring edge trim and bonding processes. Planned future studies include a comparison between thermoplastic adhesives and thermoset materials, and detection of micro cracks and analysis for their dependence on the bonding and grinding processes.

As advanced WLP approaches involving temporary wafer bonding are going into high-volume manufacturing, automated edge inspection and metrology are expected to help ramp up edge yields faster when compared to manual approaches, and to significantly lower the overall cost-of-ownership.

## Acknowledgement

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# Wafer chip-scale package cost reductions

By M. Todd Wyant [Texas Instruments]

**F**lip-chip products have long been used when there are size or performance concerns where a plastic-packaged component does not lend well to the capabilities needed. This has created the market niche where wafer chip-scale package, or WCSP, was born. This technology utilizes a solder ball that allows an electrical connection with the outside world, thereby eliminating many back-end assembly processing steps involved in packaging, but it also creates an entirely new set of processing steps and cost pressures that come with these new differences.

With industry concerns now requiring a balance between process controls, quality assurance capabilities create a delicate balance between business wins and losses. This is a long-standing problem in packaging that is not new, but the wafer chip-scale package creates its own unique concerns, risks and cost challenges.

This article will show a typical WCSP process flow and describes its long-standing inspection strategies and shortcomings. The article will also describe a recent trend in companies looking at cost and cycle-time reductions many to lower costs without impacting customer quality or delivery.

## Front-end process flow

**Figure 1** shows the typical flow for a WCSP, or flip-chip package. There are three distinct flows for products. The BE1 flow (back-end 1 flow) is for wafer thinning and drop ball placement processing. The wafers are provided incoming from wafer test operations or can follow ball placement dependent on device type and functionality. The flow shown in **Figure 1** indicates test processing following the back grind and ball placement processing, but it can also take place prior to these processing steps in some standard flows. The first typical step on incoming wafers to assembly is back grind operations. The wafers are thinned via diamond wheel back grind

to the final thickness and the final solder balls are then placed. This is followed by a reflow and flux screen.

The typical final step in the bump facility is to perform machine vision with an automated visual inspection tool. This ensures proper ball placement and that wafers are not mechanically damaged during ball placement processing prior to sending the unit to the assembly site. On many products, tests can be performed following ball placement for final programming, final test trim, or other such tests that need to happen after the final high-temperature reflow process of the BE1 flow.

## Back-end process flow

Back-end 2 (BE2) takes place after ball placement and the optional test flow that is sometimes used in operations. The BE2 processing is where the majority of quality concerns begin. This flow involves visual inspection to contain damaged units during BE2 operations, and historically, it has had quality concerns after test operations. Defect creation generates a long-term need for increased visual inspection and strategies to reduce returns or the likelihood of quality problems to the end customer. This challenge occurs because after

a significantly large number of complex/difficult mechanical processes are done, no test is performed to ensure that quality has been maintained.

BE2 operations begin with a backside coating applied to the back side of the silicon wafers, and in some cases it is skipped

depending on customer and product requirements. The coating process applies a film to the back of the wafer and has a matte finish similar to that of a plastic package. Once applied, the coating is baked at high-temperature to cure the material in place for further processing.

Following the backside coating process, the wafers are processed through a back-side laser marking process. The laser etches a unique product tracking code onto the part for both visual reference and quality tracking. The characters and tracking code capabilities are limited by chip size. The units typically also include a pin one orientation symbol to ease end customer placement and allow for visual verifications downstream.

In the next processing step, the wafer backside is mounted on tape and a ring for transport in and out of a saw ring cassette for the remaining BE2 operations. Following the mount process, the wafers sometimes have a hold or low-temperature bake process to allow for an increase in adhesion level between the backside coat material and the wafer mounting tape.

Once mounted, the material is processed through the wafer dicing/sawing operation, as shown in **Figure 2**. Historically, this is the biggest contributor to quality issues in

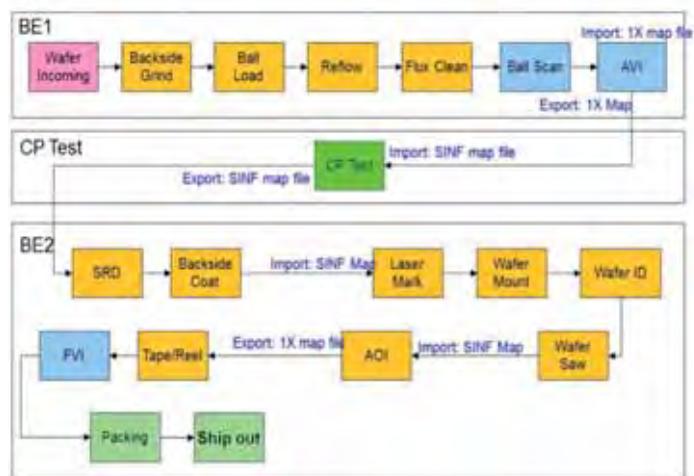


Figure 1: Typical WCSP flow.



**Figure 2:** Mechanical dicing assembly.

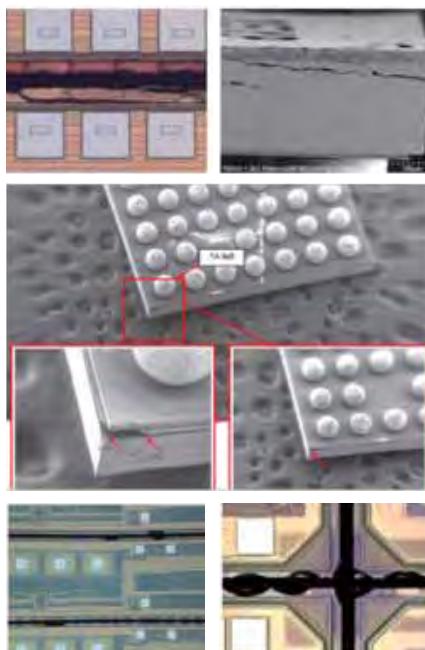
the industry and it has the largest risk for quality problems downstream. The wafer dicing process utilizes a diamond blade that mechanically removes the inactive area between the circuits left during the fabrication process. **Figure 2** is the typical dicing setup. A diamond blade rotating at a high RPM is brought across the silicon to be singulated, while deionized water, sometimes with an additive, is used to remove the excess material and to keep the cutting tool cooled during the process.

Use of a mechanical dicing process promotes multiple failure modes and process-related issues and concerns. The top categories will be covered in this article, but many other failure modes exist that create industry concern and need consistent techniques to contain.

The dicing process is essentially a mechanical saw. The diamond blade chips away material mechanically and creates a groove between the parts. During this silicon removal, the process generates particles that can damage active circuits. These particles can also lead to edge damage caused by chipping and can be encountered on both the top and back side of the silicon as it is being processed. The damage on the front side also puts active circuitry at risk.

**Figure 3** shows some typical dicing defects that can be created during processing with a mechanical diamond blade. These defects occur following test operations and require a significant amount of visual inspection to prevent the rejects from being shipped to the end customer.

Following the mechanical dicing process, the parts are then taken to an automated visual inspection process (AVI). This process utilizes high-power optical inspection with known good and bad algorithms and settings to optically screen mechanical damage, bump damage, and dicing damage to active circuitry on the products. This is accomplished



**Figure 3:** Typical WCSP failure modes.

with expensive dedicated equipment and typically requires a post-process operator to review, classify, and categorize rejects.

After inspection, the parts are sent to the tape and reel process where they are once again visually screened on the input table, picked from the dicing tape and inspected again, before being placed into polystyrene/polycarbonate carrier tape. The components are then sealed into the pockets with a cover tape, and wound on an output reel for delivery to the end customer. This has been the process flow for delivery of bare die, WCSP, and flip-chip for nearly two decades. Equipment improvements and advancements in machine capabilities have enabled labor reductions, but it is quickly offset by increased equipment cost.

### Cost changes to impact process flows

There has been a recent trend to work for cost reductions that creates the need for shortened process flows, integration of processing steps, and improvements in equipment for processing materials. This drives factory labor, factory floor space and capacity improvements that contribute to bottom-line costs.

**Figure 4** shows the best case and lowest cost flow for wafer chip-scale, flip-chip, and bare die processing for BE operations. This flow was optimized to reduce capital expenditure and to

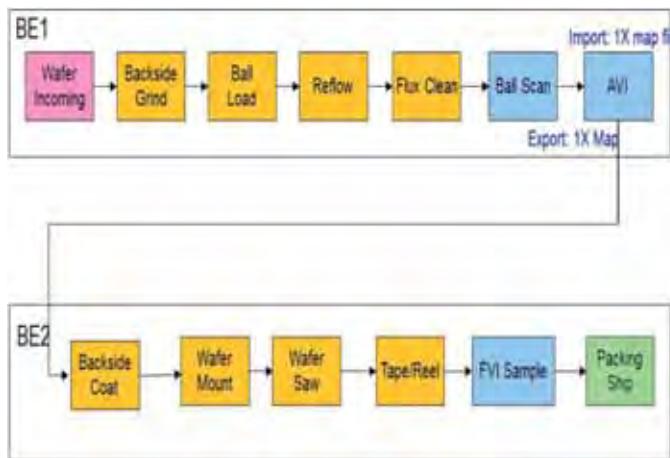
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**Figure 4:** New low cost/fast-turn WCSP flow.

combine processing to reduce labor and floor space at each processing step.

Back-end assembly flow BE1 remains pretty much unchanged. The AVI inspection process was improved to include a 3D sample for bump height with a 2D full scan for bump placement and mechanical type defects. The major change was for a 3D sample to be utilized for significant cycle-time reduction and to eliminate the need for this function in the back-end two (BE2) flow.

The second sequence of flows for BE2 had the most changes. Multiple visual inspections and processing were combined to reduce the processing steps needing monitoring. In addition, this new flow had less associated product movement and labor. The test after the bump test trim process is removed completely on this BE2 flow and only wafer probe is used prior to bump on the selected parts. The next change involves removal of the spin-rinse-dry (SRD) processes. SRD is completed in the wafer bumping area prior to shipment and was redundant in the flow. Upon validation, it was deemed unnecessary for processing purposes.

A new industry development came in the form of a 2-in-1 backside coat and wafer dicing tape at wafer mount that eliminates the processing step of backside coat apply. The backside coating and wafer dicing tape are applied in one application, thereby removing the need for a complete processing step at the BE2 flow. Deionized air blowers were added to wafer backside coating equipment to prevent particles that create air bubbles and to eliminate particle issues.

The mechanical wafer saw remains unchanged from a processing standpoint.

There are significant improvements in laser technologies today, but cost is still the primary driver in keeping this technology at the forefront of mass production. After wafer saw, you will see the largest change in processing flow.

### Advancements in machine integration

New equipment and the merging of technology at the tape and reel processes have allowed for integration of multiple steps into one machine. The new machine combines UV release, full 2D visual inspection for top-side mechanical damage or bump damage, and outgoing visual inspection the die is picked to ensure damage-free components. The advances in optics and processing power have enabled key inspections to take place in a new location with the same results: post-test process-induced mechanical damage is contained at this processing step. Once the die is picked, the equipment will verify the top side via an inspection system to ensure the die was not damaged during the pick process or during the input table inspection that was performed.

The system can also incorporate what is called a six-side inspection that enables visual inspection or visual sampling for sidewall chipping quality after dicing operations. This inspection extends capabilities and detections that were not possible in past process flow. Die can now be screened for both topside and backside chipping prior to placement in the output reel for shipment.

After placement, the machine has a laser symbol integrated into the place sequence, again, to reduce processing steps and allow for more integration of processing. Following placement into the carrier tape, inspection takes place for empty pockets and damage to the backside. This can be accomplished using cover tape prior to sealing the die into the pocket.

Once the tape is sealed, another visual inspection is done to ensure the machine

meets empty pocket specifications. Post-placement seal inspection also enables sealing inspection and integration of all of the final visual inspection operations into one tool. Failed materials are flagged by the system and only reels requiring rework are processed at a separate offline final visual inspection station with the new machine updates.

### Summary

This article shows how taking a fixed long-term flow and utilizing new equipment technology can attack longstanding built-in cost of a manufacturing flow. Keeping with the mindset of “it’s not broke so don’t fix it” is held onto by many companies in the industry. Getting away from that mindset and adopting a change in strategy can lead to much-needed cost reductions for a highly competitive market.

The new processing flow takes three days out of the total cycle time, reduces equipment expenditures by 30% on new capital, and enables significant labor savings. It also reduces the factory work in process (WIP) storage areas between processing steps. These changes enable significant cost reductions on the big three cost inputs: labor, depreciation and facilities requirements.

Cost reductions on long-standing processes can be addressed by enabling new capabilities and working upgrades of existing processing equipment to overcome the previously approved industry processing flows. A focused drive to stay on path will get you to the ultimate goal of cost reductions and much needed efficiency improvements. This is a classic example of enabling changes through equipment capability updates, process integration, and labor modifications. The path to cost reduction is becoming more and more difficult to accomplish, and the big levers to cost reduction are long gone. Taking a strategic approach in equipment changes and staying the course to use data to drive to those needed changes will yield much needed improvements at the end of this long journey. Hard work is never pretty.

### Biography

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# GUEST EDITORIAL



## Next-generation wafer-level processing through customized materials

By Jonathan Knotts, Joseph Morano [Creative Materials]

The trend to move manufacturing processes from single-unit processing to wafer-level processing (WLP) has grown over the last several years. The implementation of WLP, while advantageous from the perspectives of overall cost containment and efficiency, can also present a variety of challenges, and customized solutions may be required in order to achieve successful implementation of this technology. Wafer-level processing involves delaying singulation of the devices being produced until as many steps as possible of the manufacturing processes are complete.

Many companies that have successfully implemented WLP are realizing huge increases in throughput, reduced energy costs, and lower labor costs. Other companies have struggled with new difficulties in controlling yield rates, failure mechanisms and limited materials and experience upon which to draw. Many thermal management, die attach and advanced composite materials are designed for manufacturing processes that are 10, 20, or even 30 years old and do not offer the resolution, uniformity and reliability required to successfully implement WLP. The need for customized products that are unique to the product, process and population of the wafer has become quite apparent to both end users and suppliers. When building an array of parts rather than a discrete part, the challenges fall outside of the normal scope dealt with by back-end manufacturing groups. These new challenges often require expertise from a variety of backgrounds and industries that need to be included in both understanding and engineering the solution to a successful WLP implementation. This article will discuss how these challenges can be successfully managed to develop engineered solutions through the use of highly customized materials.

### Reducing the occurrence of defects

Many potential part defects can be introduced in WLP implementation.

These can cause poor yields and are often challenging to overcome. Difficulties in moving to WLP include but are not limited to, voids, contamination, shorts, opens, warpage, and compatibility with downstream laser marking or vision systems. Further problems are created when adjusting processing parameters to improve yields. As the process is fine-tuned in order to reduce or eliminate one type of defect, another problem is created. Some examples may include: 1) Applying a thicker layer of conductive adhesive to eliminate opens, which can then create warpage or shorts; 2) Using high-temperature curing to increase shear strength can create cracking and warping (see **Figure 1**); and

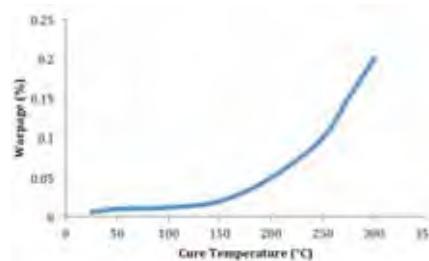


Figure 1: Degree of warpage vs. curing temperature.

3) Increasing shear conditions during application to reduce viscosity can improve wetting, but can also impart air, which creates one type of void, while eliminating another; 4) Adding fillers to improve thermal heat transfer which in turn increases the viscosity will increase occurrences of voiding (see **Figure 2**). The many potential failure mechanisms do not allow for easy process control or adjustment. A material designed uniquely for the narrow performance window allows for creation of a robust process within a narrow window.

Most of the existing functional materials used in back-end manufacturing have been on the market for decades and often are not RoHS compliant, contain high ionic levels

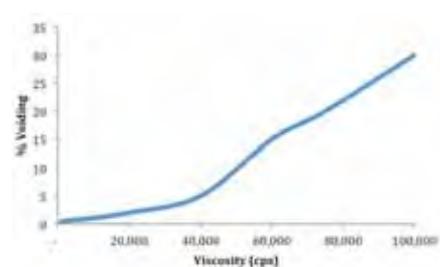


Figure 2: Percentage voiding vs. material viscosity.

particularly hydrolysable chloride, and use outdated materials technology. These materials are repurposed into WLP applications, as they are readily available and familiar from use in older discrete device processes. The lack of available information or vendor responsiveness has caused many manufacturers to find themselves in a bind when the bill of materials includes polymer-based composites that do not meet chip-level requirements. Coarse particles, wide particle distributions, and undesirable modifiers, such as heavy metals or silicone oils, are common in older products. Most of these products were designed for general use bonding and encapsulation and did not rely on the high standards and requirements that guide today's formulators.

With sluggish support from composite manufacturers, especially regarding new uses of older product lines, many fabricators reach out to custom formulators, consultants, and equipment manufacturers looking for guidance. This situation can be taken as an opportunity for the consultant: rather than addressing only the specific problem encountered by the manufacturing team, a new solution can be devised by deconstructing all of the concerns, requirements and processing challenges, resulting in the development of a specialized formulation that resolves the problem. It is essential to include all down-stream processing and device requirements in a new materials property

set. This prospective planning approach to the material design is essential to ensuring reliability of the devices over the expected lifespan and operating conditions.

Many of the challenges simply come from the basic differences in geometries in scale when moving to a WLP. The long expanses or trenches, innumerable sharp intersections, variations of geometries within populations, and lack of hoop stresses take normal back-end processing principles out of the scope of WLP problem solving. Thermal expansion, shrinkage, and many other properties, which are based on an inch-per-inch basis, become centralized across the wafer. This magnifies the stresses, creating warping, cracking and exothermic events. Hoop stresses cause materials to shrink radially inward, promoting strong bonds and intimate contact between layers when coated on the surface of a part. In addition to the advantage of hoop stress, the discrete part manufacturer also has

fewer challenges due to smaller masses of composites used simultaneously, thereby avoiding defects associated with exothermic reactions. The natural behavior of shrinking onto the part or around the part in the case of hoop stress is a benefit often taken for granted in discrete component manufacture. When filling polymeric materials between multiple substrate surfaces, the multi-faceted wetting during the curing process can cause delamination, cracking, or dimpling. Heat dissipation, shrinkage, and stresses are all challenges that become more difficult to manage with these changes in size and geometry. With the continual reduction in the size of devices, the wafer's own dimensional stability is diminished and contributes less and less to the mitigation of these challenges.

Application principles utilized on larger scale products using composite technologies are typically foreign to device manufacturers that are specialized in microscale concepts and problem solving. The combination of macro- and micro-scale backgrounds is needed to ensure good part performance and proper wafer performance and handling prior to singulation. During the customizing, process information is shared both ways. The end user provides requirements and processing capabilities and the custom formulator provides insight into the polymer behaviors, root causes for failures and the many ways to control or mitigate the defects.

C u s t o m formulations create new products with properties that span

both micro- and macro-scale concerns, push tolerances and minimum feature sizes down, and also widen processing windows. The integration of customer needs and processing requirements into the design of the product allow the formulator to fit the product into the WLP goals as a tailor would fit a suit to his client.

Many challenges exist with respect to implementation of WLP that involve the technical aspects of materials and processing, but these tend to be a secondary set of problems. The primary barrier to success tends to be a lack of information sharing. Material suppliers are wary of providing trade secrets or proprietary compositions. Fabricators, needing to protect new products and processes, create a tense and tight-lipped dialogue. This hesitancy to communicate full disclosure of product capabilities and limitations by material suppliers and a bare list of requirements from the fabricator often provide misguided and poor results during initial trials, thus preventing many programs from ever getting off the ground. The much-needed intimacy of efforts on both sides requires a great deal of trust that can be difficult to cultivate. To address this set of challenges, we offer a hands-on approach with on-site support for training and real-time material modification that has the end effects of a closely matched material and process.

With shorter sales cycles for new device ratings and intense competition in most device markets, the speed at which these iterative developments must happen requires significant dedication of resources from both sides. When resources are devoted and a broad base of knowledge is utilized, WLP is both successfully implemented and highly optimized.

## Biographies

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# INDUSTRY NEWS

## Report from BiTS 2015

The Burn-in and Test Strategies (BiTS) Workshop successfully completed its sixteenth annual event in Mesa, Arizona on March 18, 2015. Throughout the three-day event, attendees participated in a hands-on tutorial, a keynote address from Joe Bruen of Freescale Semiconductor, and an invited talk from Brandon Prior of Prismark Partners, as well as technical content from industry experts and participants.



Ila Pal, Ironwood Electronics, and Bud Kundich, E-tec Interconnect.

Heidi Barnes led the hands-on tutorial, "How to make a high-frequency transparent socket," featuring Keysight Technologies' hardware and software. The tutorial offered participants a toolbox of both simulation measurement and signal integrity techniques for characterizing a socket and ways to make it transparent for upcoming multi-gigabit applications. The tutorial preceded the three-day workshop.



Cheryl Allen, Mathias Westenhuber, Emil Schreck, Cohu Inc.



Randy Weaver, Tom Bresnan, Don Thompson, R&D Altanova.

Technical papers, delivered by such leading companies as Advantest, Amkor Technologies, Intel Corporation, Infineon Technologies, STMicroelectronics, Teradyne, Tyco Electronics, and Xcerra, covered topical areas as diverse as test and socket solutions for testing automotive radar devices, device reliability, and test solutions for both



Kim Hause, Tim Dowdle, John Hope, & Jeff Tamasi of Smiths Connectors.



Tony DeRosa, Claude Castiglione, Everett Charles Technologies.



Sensata/Qinex team.

WLCSP and MEMS devices. Best Paper was awarded to "Designing sockets for ludicrous speed (80GHz)" by Don Thompson (R&D Altanova) and Jose Moreira (Advantest).



Ira Feldman congratulates Don Thompson of R&D Altanova.

The BiTS Workshop event, which was focused on the burn-in and test of packaged semiconductors, drew more than 350 attendees. Fabless and integrated device manufacturers, as well as companies from the supply chain delivering burn-in, test, and test consumable products, were well represented. More than 40% of attendees were from international locations. An important component of the workshop has long been the BiTS EXPO, which is open to not only conference attendees, but also industry and academic members of the community. Displays featured the latest products and services from such companies as premier sponsor Smiths Connectors and emeritus sponsor, Test Tooling Solutions Group.

Market outlooks were delivered by representatives of Feldman Engineering and VLSI Research. Opportunities for networking and social activities rounded out the 2015 event. General Chair, Ira Feldman

# INDUSTRY NEWS

of Feldman Engineering, declared the event a success as he announced that attendance was up by ~10% from 2014's event. In one of his addresses to the attendees, Mr. Feldman also announced that BiTS Workshop will hold a seminal Asian event in Shanghai in October, 2015. BiTS 2016 will return to Mesa, Arizona on March 6-9, 2016.

## IHS Technology issues market tracker on top 10 MEMS manufacturers in 2014

IHS Technology has issued a summary from its Q1 MEMS market tracker report that lists the top 10 MEMS manufacturers in 2014 (Figure 1, Table 1). According to Jérémie

Bouchaud, Sr. Director, MEMS & Sensors at IHS, Bosch reinforced its leadership in the MEMS industry in 2014 with a 16.6% increase to \$1167 million, up from \$1001 million in 2013. "Bosch alone held 12% of the very fragmented MEMS market in 2014 compared to 11% in 2012," noted Bouchaud. Bosch took the leadership in 2013 because its accelerometer had been designed into the Apple iPhone 5s and iPad. "Apple boosted Bosch's MEMS revenue in 2014 again, as Bosch is the sole supplier of the pressure sensors added to the iPhone 6 and 6+."

Besides its revenue growth courtesy of Apple, Bosch enjoyed a strong growth of its motion combo sensors with Sony, both for gaming with the Sony PS4, and for handsets and tablets. "Bosch started going after the consumer MEMS market in 2005 when it created Bosch Sensortec," explained Bouchaud. "It added MEMS microphone to its portfolio with the acquisition of Akustica in 2009." Bouchaud noted that Bosch's bet on consumer applications paid off as this segment now accounted for a third of that company's total MEMS revenue in 2014, compared to less than 18% in 2012.

Besides the above applications, the legacy automotive business continues to dominate Bosch's MEMS revenue with 67% in 2014, said Bouchaud, who called Bosch the undisputed leader in automotive MEMS—it had a 30% market share in 2014, with revenue more than three times as high as the second largest automotive MEMS maker, Denso.

Coming in second in the IHS rankings was Texas Instruments, which enjoyed a rebound of its Digital Light Processing business in 2014 with an estimated \$805 million, up from \$709 million in 2013. "The business growth in 2014 was seen mostly in the main business line of the DLP business projector segment using TI's Digital Micromirror Device (DMD)," said Bouchaud. "TI's DLP business had declined from 2010 to 2013 as Epson – TI's DLP's main competitor with its (non-MEMS) LCD technology – won shares in the projector business." Bouchaud observed that the business projector market suffered in the past few years because of the competition from low cost LCD flat panels being used as an alternative to projectors for many conference rooms, especially in the Asia region. "TI won back shares in the projection display market against Epson's LCD technology last year."

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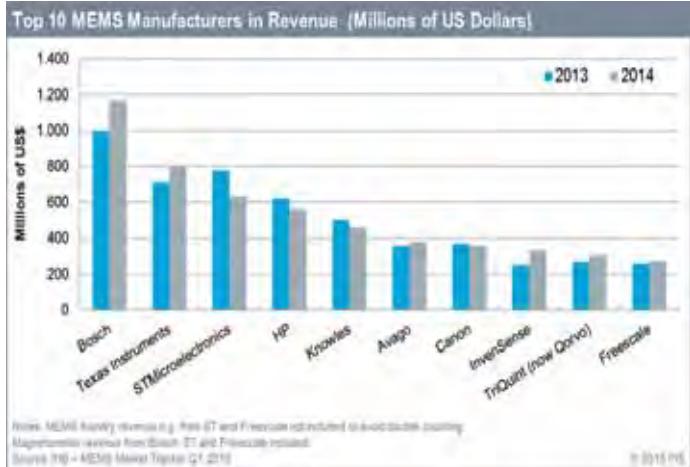


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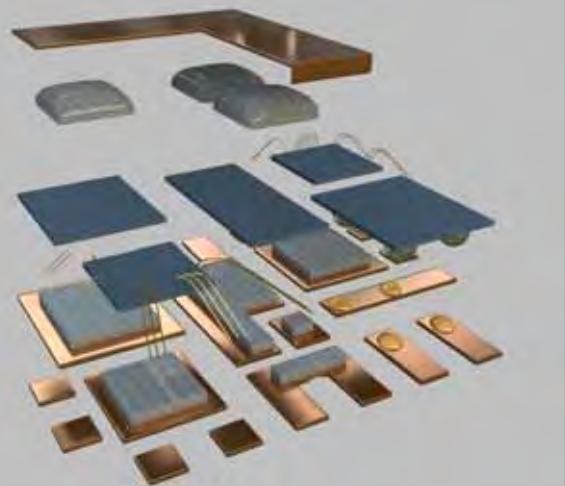
**Figure 1:** Top 10 MEMS manufacturers in revenue (millions of US dollars).  
SOURCE: IHS - MEMS Market Tracker Q1 2015

Top 10 MEMS Manufacturers in Revenue (Millions of US Dollars) – IHS Technology			
	2013	2014	YoY Growth (%)
1 Bosch	\$1,001.0	\$1,167.0	+16.6%
3 Texas Instruments	\$707.9	\$805.0	+13.7%
2 STMicroelectronics	\$777.0	\$630.0	-18.9%
4 HP	\$620.4	\$560.0	-9.7%
5 Knowles	\$505.0	\$460.0	-8.9%
6 Avago	\$358.2	\$380.0	+6.1%
7 Canon	\$367.8	\$357.5	-2.8%
8 InvenSense	\$248.2	\$332.0	+33.8%
9 TriQuint (now Qorvo)	\$265.8	\$305.0	+14.8%
10 Freescale	\$256.1	\$271.4	+6.0%
Others	\$3,844.8	\$4,190.4	+9.0%
Total Top 10	\$5,107.4	\$5,267.9	+3.1%
Total MEMS market	\$8,952.2	\$9,458.3	+5.7%
Top 10 percentage of total	57%	56%	

Note: MEMS foundry revenue e.g. from ST and Freescale not included to avoid double counting.  
Magnetometer revenue from Bosch, ST and Freescale included.  
Source: IHS, March 2015

**Table 1:** Top 10 MEMS manufacturers in revenue (millions of US dollars).  
SOURCE: IHS 2015

In third position, STMicroelectronics' MEMS business suffered a 19% decline in revenue from \$777 million to \$630 million. "ST is still the #1 MEMS manufacturer for consumer and mobile applications with 15% of this segment," said Bouchaud. "The historical MEMS business of ST, i.e., motion sensors for consumer applications, has been hit as ST lost its spot in the latest iPhone for the accelerometer in 2013, and for the gyroscope in 2014, and as well as for the combo motion sensors in the Samsung Galaxy S5." Even so, Bouchaud pointed out that ST mitigated the damage by winning 100% of the pressure sensor in the Galaxy S5. "ST has laid, in 2014, the foundation for a rebound of its MEMS business in 2015." The company's MEMS microphone is growing very fast thanks to the design win in the iPhone 6, in addition to its existing microphone sales into the iPad. "ST's MEMS microphone shipment grew more than 2.5 times in 2014, and IHS expects the Apple design win to attract further customers."



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## Biographies

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## Presto collaborates to develop 4G test solutions for automotive applications

by Debra Vogler, Sr. Technical Editor

**P**resto Engineering recently announced that it has joined a France-based collaboration to reduce the cost-of-test (CoT) of automotive-grade 4G radio-frequency (RF) devices. The ultimate goal is to commercialize such 4G chipset solutions by 2018. Other organizations involved in the consortium include: Parrot SA, ACCO Semiconductor, Sequans Communications, Qualtera, Virtual Open Systems, CEA-LETI, IMS Laboratory in Bordeaux, and the XLIM Lab of the University of Limoges. The program is backed by the French Strategic Investment fund, supervised by the French Public Bank of Investment (BPIFrance). The program was launched in November, 2014, and will be carried out over the course of three years. News of this collaboration is significant because, as Cédric Mayor, Chief Technical Officer, at Presto Engineering, Inc., explained, connected objects and

development of 4G solutions represents a huge market potential. "According to industry reports, 50 to 80 billion devices will be connected in the next ten years, and 2 billion will require 4G connectivity," Mayor told

*Chip Scale Review.* "For example, LTE-4G is perceived as the most promising RF chipset technology for automotive connectivity."

*Chip Scale Review* asked Mayor to discuss some of the specific challenges associated with developing a high-volume test solution for RF chipsets. Basically, RF chipsets comprise different elements such as, the analog front-end (e.g., transceivers, multi-band power amplifiers) and the digital circuitry. "As silicon integration increases, dependency between the digital/analog parts represented by the modem and the RF analog part has become tight," said Mayor. He explained that it is standard practice to perform single tone, multi-tone, and RF structural testing in addition to loopbacks at chip-level testing. This methodology allows most of the unit testing to be in parallel, thereby keeping the test cell RF resources low and the CoT to a reasonable threshold. "However, it is fundamentally different when testing each circuit element at the module-level where calibration and tuning takes place, and which requires modulated signals. There, parallelism is pretty low and capital cost per unit is a key metric."



Cédric Mayor, CTO,  
Presto Engineering, Inc.

The fact that CoT is a major issue for automotive grade RF chipsets can be seen in a comparison between consumer and automotive quality requirements. Mayor pointed out that if one considers the manufacturing of an automotive chip grade 2, according to the Automotive Electronics Council (AEC), the share of burn-in represents almost 5%, while at the same time, the cost of test reaches about 11%, and assembly 25% of the total cost. "When you specifically focus on analog-RF ICs, especially if they require grade 2 certification, the total of burn-in and test costs turns out to reach 19%," said Mayor. "To compare with that 19%, the same RF IC in its consumer version will barely exhibit a total CoT of 5-6%." Mayor pointed out that these automotive test costs are the consequences of high quality standards to capture earlier failures and achieve the 0 defect objective.

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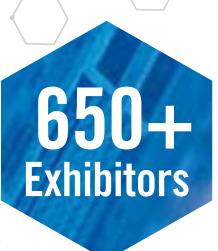


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**What's New in Flexible Printed Electronics**—This program will examine the impact of flexible, hybrid electronics on new products and innovation, and investigate flexible hybrid manufacturing techniques. Industry leaders will discuss the latest thinking about electronics on plastic, paper, and glass, also the implications of flexible electronics designs for long-lasting and always-on IoT.

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**The Path to Future Interconnects, Co-sponsored by the Electron Devices Society of IEEE**—Reviews challenges in materials and processing to manufacture interconnects needed for high performance computing.

**Packaging for Digital Health and Automotive Devices**—Explores packaging implications for new IoT devices.

# Mentor Graphics introduces IC-package-PCB co-design/optimization solution

**M**entor Graphics Corporation recently announced its new Xpedition® Package Integrator flow for integrated circuit (IC), package, and printed circuit board (PCB) co-design and optimization.

The new product automates planning, assembly and optimization of complex multi-die packages and incorporates a virtual die model concept for IC-to-package co-optimization. This solution ensures that ICs, packages and PCBs are optimized with each other to reduce package substrate and PCB costs by efficient layer reduction, optimized interconnect paths, and streamlined/automated control of the design process (Figure 1). The product also provides a formal flow for ball grid array (BGA) planning and optimization based on an “intelligent pin” concept, defined by user rules.

John Park,  
Methodology  
Architect,  
Systems  
Design Division at Mentor Graphics, told



**Figure 1:** Multiple target platforms (PCB form factors) can be considered during chip/package planning and optimization.  
SOURCE: Mentor Graphics Corporation



John Park, Methodology Architect, Systems Design Division, Mentor Graphics Corporation

Design Division at Mentor Graphics, told *Chip Scale Review* that typical EDA design tools only support one package or one board, or one chip, but users want multiple capabilities. Major drivers for a multi-capable design solution are the growth of devices needed for the Internet of Everything (IoT) applications (i.e., multiple devices in a single package) and the disruptive nature of the introduction of silicon interposers and TSVs, which impacts what used to be a “nice, clean hand-off between the fabs and OSATs,” explained Park. “fabs are adding ‘packaging’ expertise and

OSATs are adding ‘IC layout’ experts, and both need to retool.” Additionally, the industry is sensitive to packaging costs, which, for some devices, can exceed the cost of the device itself, noted Park.

In a paper co-authored with Intel (J. Park, G. Brist, “A novel approach to IC, package and board co-optimization,” ISQED, 3/4/15), it was noted that, “Traditional chip-level abstract models typically do not contain enough detail about the chip to allow the co-design engineer to make smart decisions when optimizing the chip-to-package interaction.” Incorporation of a virtual die model into the new tool addresses this need for more accuracy for today’s more complex designs. “Simple die abstract models are not accurate enough for true chip-to-package co-design,” Park told *CSR*. “A more detailed model of the die is now required, including IP blocks (i.e., macros), top metal layers (i.e., RDL, power), obstructions (noise-sensitive areas), and I/O buffers (pads).”

The new product leverages other Mentor Graphics tools such as the HyperLynx® signal and power integrity product, FloTHERM® computational fluid dynamics (CFD) thermal modeling tools, and the Valor® NPI substrate fabrication checking tool. To complete the co-design solution, Nimbic was acquired by Mentor Graphics in 2014. Nimbic technology provides Maxwell-accurate, 3D full-wave electromagnetic (EM) high-performance simulation solutions that calculate complex electromagnetic fields for chip-package-board simulation.

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The IW LPC Technical Committee would like to invite you to submit an abstract for next year's program.

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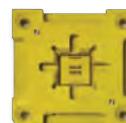
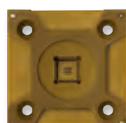


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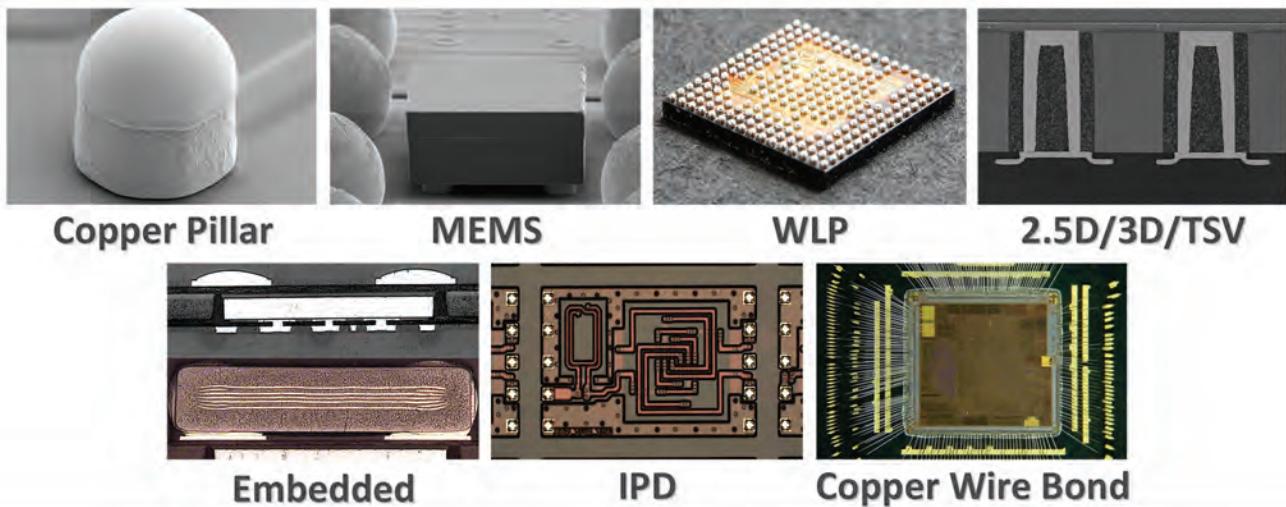
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