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The Future of Semiconductor Packaging

Volume 23, Number 2

March • April 2019

```
mirror_mod.use_y = False  
mirror_mod.use_z = False  
elif _operation == "MIRROR_Y":  
    mirror_mod.use_x = False  
    mirror_mod.use_y = True  
    mirror_mod.use_z = False  
elif _operation == "MIRROR_Z":  
    mirror_mod.use_x = False  
    mirror_mod.use_y = False  
    mirror_mod.use_z = True
```

```
#selection is the end face of the chip  
mirror_ob.select 1  
modifier ob.select 1  
modifier ob.modifiers.add("mirror", ob)
```

- Packaging of implantable devices
- The growing demand for power devices
- Multiscale models for electroplating of TSVs
- Failure relief for WLP and PLP polymer layers
- Automotive IC production wafer test in a zero-defect world
- Silicone surface contamination for optimizing package assembly
- Testing of HF 5G applications and why simulations are critical to success



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Whether it's 5G applications, bioimplantable electronics, the growing demand for power devices, or other challenges, the semiconductor packaging industry, powered by human brainpower, has always risen to the occasion. Looking ahead, we may be looking at artificial intelligence to help power the future of packaging design, manufacturing, and test. Enjoy the issue!

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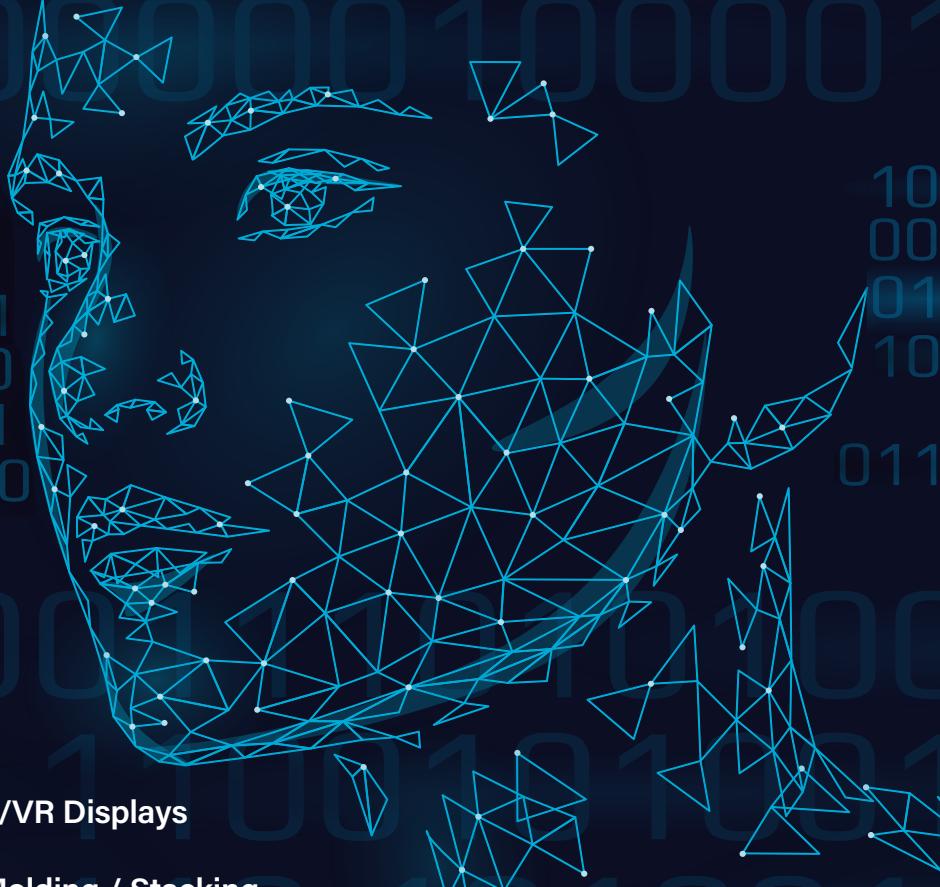
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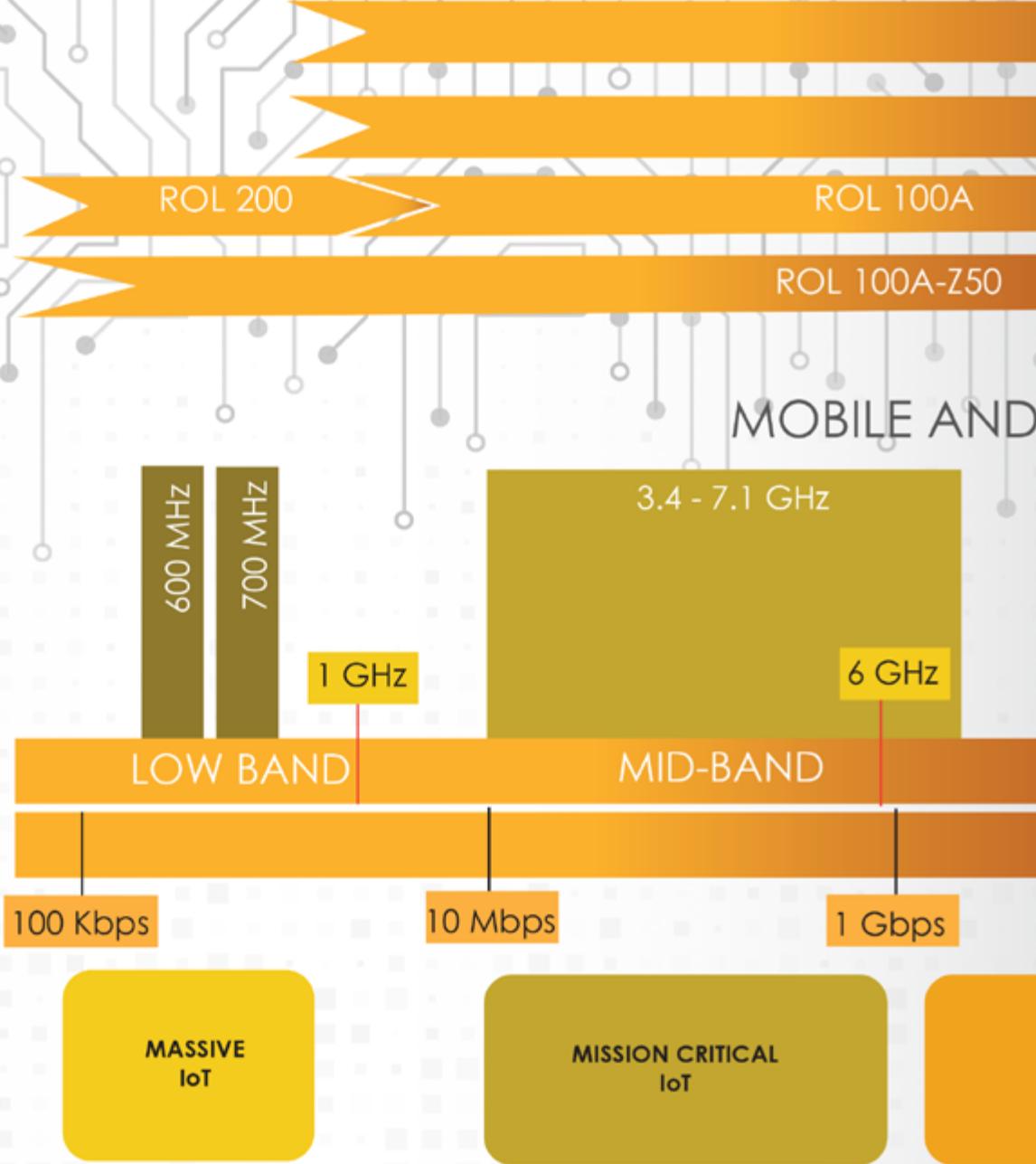
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Anti-Theft Systems

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LOS P-P 70GHz

77 GHz

110 GHz

10 Gbps

40 Gbps

100 Gbps

Enhanced Mobile
Broadband [eMBB]

Advanced Mobile Broadband
[Low Latency]

Automotive Network

FRASTRUCTURE

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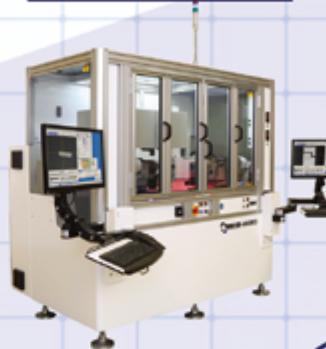
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TECHNOLOGY TRENDS



The growing demand for power devices

By Dan Tracy, Jan Vardaman [TechSearch International, Inc.]

Power devices are experiencing strong growth driven by demand in a variety of areas.

Applications including energy generation and infrastructure, electric and hybrid vehicles (EV and HEV), electric vehicle charging, data centers, industrial automation, smart cities and buildings, home appliances, and transportation are driving demand for power devices.

Power packaging includes lead frame-based packages in the transistor outline (TO), small outline (SO), quad flat no leads (QFN), and intelligent power module (IPM) form factors. Thermally-enhanced SO form factors have been used in power applications since the 1990s, and are available in packages with eight leads to over 40 leads. QFN form factors have increased in usage for power applications, with some adoption of Cu clip instead of wire bond. Embedded power modules are typically based on printed circuit board (PCB) technology for low- to medium-power applications, and on direct bonded copper (DBC) or insulated metal substrates (IMS) for high-power applications. High-power chips soldered to a DBC substrate typically use heavy wire bonds for the topside interconnect.

Power device applications

Switching power converters have a large field of application encompassing mobile phones (up to 10W), automotive (several kW), and large solar and wind energy operations (MW). Single-chip packages are used for metal-oxide semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), and diodes that are typically found in low-power applications. Power modules are used for mid- and high-power applications, and include IGBTs and diodes in half-bridge configuration. High-power applications typically require electrical isolation to the backside.

General purpose inverters are used in building air conditioners, elevators and escalators, manufacturing equipment, and machine tools. Input voltages are alternating current (AC) 600V or lower for general-purpose inverters, and 75kW or lower for AC drive motors. Inverters of 300kW are also being included in the “general purpose” category. Small-capacity inverters with voltages of 4kW or less account for 80% of the market in volume, but the market for higher functions and performance is expanding for new applications [1].

Power semiconductors and packaging have been labeled as key to enabling the growth of electric vehicles (EV), along with battery density, faster charging times, lower cost, and charging infrastructure. In an EV powertrain, there are high-power semiconductor modules that convert current from direct current (DC) to AC, inverters, and converters. There are numerous microcontroller units (MCUs) to manage the electric power delivery for traction systems and other systems such as on-board charging. On average, the EV semiconductor content is estimated to be six to 10 times more than an internal combustion engine (ICE) powertrain. Key components of EVs include the

battery management system, power distribution module, inverter/converter, electric drive module, powertrain control module, and charging related modules. Advanced packaging for the powertrain is one core technology for which development is required to expand the performance and market of EVs.

The switch to wide band gap materials

While many companies continue to expand production of silicon-based power devices, there is also demand for devices based on new wide band gap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN). Driven by the need for increased power density and system efficiency, these WBG materials are being adopted in many applications and may require new packages, materials, and assembly methods.

Silicon as a semiconducting material suffers from relatively low electron mobility, which leads to slow switching response and loss. Silicon also has poor resistance to high junction temperatures, which increases the cooling requirement. WBG materials such as SiC and GaN, on account of their relatively large band gap (measured in eV) compared with that of traditional silicon materials, have inherently superior properties that allow them to be used at higher voltages, frequencies, and temperatures (see **Table 1**). Devices based on these WBG

	Si	GaN	SiC
Band gap E_g [eV]	1.1	3.4	3.3
Electron saturation velocity V_s [cm/s]	1×10^7	2.2×10^7	2×10^7
Dielectric constant	11.8	10	9.7
Critical electric field E_c [V/cm]	3×10^5	2.2×10^6	3×10^6
Thermal conductivity (W/cmK)	1.3	1.3	4.9

Table 1: Electrical properties of Si and WBG materials. SOURCE: TechSearch International, Inc., adapted from STMicroelectronics.

materials are used because they can allow design of smaller, more efficient power module packages. Companies are also investigating new technologies and materials such as vertical GaN devices and gallium oxide substrates.

SiC power devices are in mass production in a variety of applications,

including automotive, trains, elevators, and industrial heating and cooling systems. SiC power devices can already be found in production automobiles. For example, Honda introduced its Clarity Fuel Cell vehicle in March 2016 with SiCs in the powertrain. Tesla uses 23 SiC inverters in its EVs. In automotive applications, lower loss in power devices translates to higher efficiencies and higher power output, and the ability to design smaller and lighter weight systems. Increased power inverter efficiency can positively affect the performance of an ICE.

While SiC devices are predominantly used in high-power applications, GaN is often suitable for higher-frequency applications where fast switching is required, such as on-board charging (OBC) and electric charging stations. Other applications for GaN power devices include AC-DC and DC-

DC converters, uninterruptable power supplies (UPS), industrial motor drives, and photovoltaic (PV) inverters. GaN power devices are in production for a variety of applications, including wireless charging, robots, and electric scooters.

High-power chips are typically soldered to the DBC substrate with heavy wire bonds used for the topside interconnect. The high inductance of wires is too high for fast-switching SiC and GaN. In addition, lifetime is limited by bond wire reliability. Examples of power packages at various voltage level are shown in **Table 2**.

Copper clip packages are also increasingly used for power devices (**Figure 1**). The thermal efficiency of the Cu clip package makes it a good choice for power devices in industrial, telecommunications, computing, and automotive applications. The packages

are increasingly used for telecommunication and computer applications. Some of the Cu clip packages are single die, but many are multi-die either in a side-by-side configuration or a stacked (3D) configuration.

Wire bond has been the mainstay for power devices, though specialty packages such as Cu clip are increasingly being used. Embedded die packages are another option. Several embedded component solutions have been introduced for power devices including DC/DC converters. Embedded component technology is also being introduced in SiC power modules for automotive and avionics applications and for GaN power devices.

New materials

The majority of today's devices use Pb-based solder for die attach, and companies are often reluctant to take the

risk and incur the qualification cost to convert to a Pb-free solution. Some companies are beginning to adopt Pb-free solders, but the challenge is in meeting the reliability requirements of power devices for all applications. With the market demanding increased power and performance from Si-based semiconductors, the operating junction temperature of these devices is beginning to exceed 150°C, the temperature at which conventional high-Pb solders, Pb-free solders, and electrically conductive adhesives (ECAs) operate. The adoption of high-temperature devices fabricated from WBG materials, such as SiC and GaN, is pushing operating junction temperatures to 175°C and beyond. This trend is driving the need for higher-performance die attach materials, and companies are exploring the use of nano-sintered material in both the die attach and Cu clip attach.

Summary

Power devices represent an exciting area of growth in packaging with options ranging from traditional TO packages to new embedded die options. With demand for EVs and improved energy efficiency, the demand for new devices and packages shows no sign of slowing!

Reference

- “Versatile Inverters Boost Energy Savings for Industrial Uses,” AEI, July 2018.

Biographies

Dan Tracy is a Sr. Analyst at TechSearch International, Inc.; he received his BS in Chemistry from State U. of New York (SUNY), College of Environmental Science and Forestry; an MS in Materials Science & Engineering from Rochester Institute of Technology; and a PhD in Materials Engineering from Rensselaer Polytechnic Institute; email dan@techsearchinc.com

Jan Vardaman is President of TechSearch International, Inc., Austin, TX. She received her BA from Mercer U., and MA in Economics from the U. of Texas.

Category	Package Examples
Low power (10V to 200V)	SOT; SC-70; TO-3, TO-92; PQFN; PowerSO, BGA
Medium power (200V-650V)	TO-247; PowerSO; PQFN; IPM
High power (>650V)	TO-220, TO-251, TO-252, TO-263; IPM; modules

Table 2: Examples of power packages. SOURCE: TechSearch International, Inc.

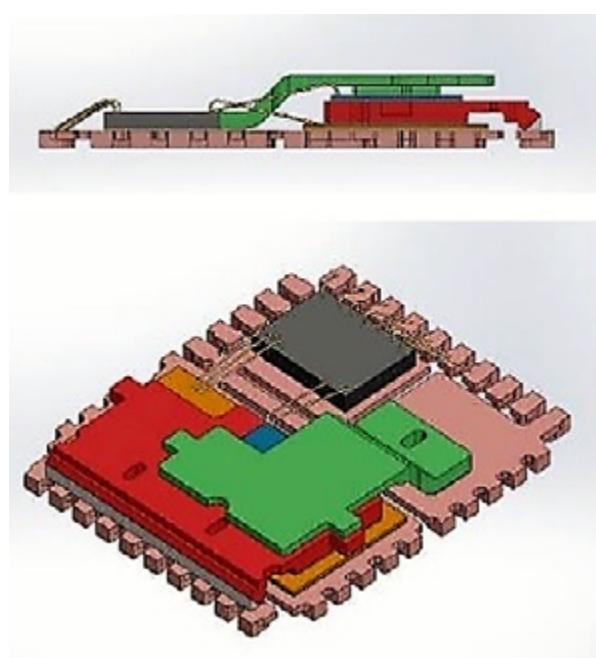


Figure 1: Stacked Cu clip module QFN. SOURCE: UTAC



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Package it.

Multiscale models for electroplating of TSVs

By M. S. Bharathi, K. H. Khoo, H. Ramanarayan, J. Hongmei, S. Wu, C. A. Joshi, S. S. Quek, D. T. Wu, N. Sridhar [[Institute of High Performance Computing](#)]; L. MingRui [[National University of Singapore](#)]; K. R. Mangipudi [[Indian Institute of Technology, Bhubaneshwar](#)]; J. J. Cheng [[Institute of Materials Research and Engineering](#)]

Through-silicon vias (TSVs) used in three-dimensional integrated circuits are a means of realizing vertical interconnects of stacked silicon wafers architecture to achieve superior electrical performance at a lower cost. Nevertheless, as the package size get smaller, the aspect ratio of the TSVs increases, which can result in defects in them during their deposition. These defects, which include voids, seams, impurities and grain boundaries, degrade the electrical and mechanical performance of the system.

Apart from the aspect ratio and plating conditions, the deposition of TSVs are heavily influenced by the chemical and transport properties of the additives used in the plating solution. A full understanding of these various factors, and therefore the electroplating process, can be achieved through an integration of multiscale modeling and experimental characterization and tests of the process. Yang, et. al, coupled a nucleation model at the micro-scale along with a current distribution model to understand the multiscale behavior of electroplating [1,2]. They also developed a dynamically-coupled kinetic Monte Carlo (KMC) model for surface reactions with a finite volume model for transport and chemical reactions and a level-set model that tracks the metal/electrolyte interface macroscopically. These modeling methods, however, do not include first-principle methods essential to compute the adsorption and transport properties and the reaction pathways and activation barriers of the additives. Here, we present sequential multiscale modeling tools including first-principle calculations and a KMC model to provide growth guidelines for defect-free electroplating of high aspect ratio Cu interconnects.

The electrolyte for the electroplating of copper has multiple additives, which have varying reactive, adsorption and transport properties. Apart from the chemical interactions of the additives in the electrolyte, the adsorption and transport properties of the additives determine their local concentrations and gradients in the TSV. As the role of additives is to enhance metallization at the bottom of the TSV (and suppressing metallization near the top), it is essential to optimize the concentration gradients of the additives in the TSV. Due to the different time and length scales of these processes during the electroplating, we employ multiscale modeling tools to study the process. The chemistry of the electroplating process, which includes studying the roles of the various additives, is carried out using density functional theory (DFT) and molecular dynamics (MD) simulations. The filling of the TSVs by electroplating is studied at the continuum scale using level-set methods to track the growth interface. A KMC model has been developed to bridge the scales between these two schemes of studying the electroplating of copper. These models will study the electroplating of TSVs as a function of parameters including the concentrations, diffusivities, adsorption properties of ions and additives, applied current density, and temperature. In this work, we present the results of our DFT studies on the mechanisms of the additives and the KMC model to understand the transport and adsorption properties of additives during electroplating of TSVs.

Density functional theory studies

We have studied the mechanism for the accelerating effect of bis-3-sulfopropyl disulfide (SPS) and suppressing effect of polyethylene-glycol (PEG), both of which are widely used additives in TSV copper plating. We employ first-principles DFT calculations to study the energetics

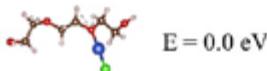
of several adsorptions, dissociation and displacement reactions that have been proposed to explain the action of the additives [3,4]. In our calculations, the Cu electrode and adsorbate molecules are modeled at the DFT level and the water solvent is represented through an implicit model based on the Poisson-Boltzmann equation [5]. This model incorporates the dielectric screening on account of the permittivity of the solvent and the electrostatic shielding due to the mobile ions in the electrolyte. The tuning of the electrochemical potential is achieved by charging the system and tracking the changes to the workfunction [6]. The free energy of the electron-ion pairs in electrochemical reactions are evaluated using the computational hydrogen electrode (CHE) and linear free energy relationship for electrode potentials (LFER-EP) [7]. In addition, we have also tried to include the dispersion forces using the DFT-D2 scheme to compensate for deficiencies in GGA xc-functionals [8].

PEG suppressor

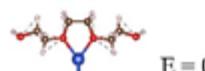
In copper deposition from a Cu^{2+} solution, the basic plating reaction proceeds via two steps, from Cu^{2+} to Cu^+ , which is the rate determining step, and Cu^+ to Cu , which is much faster. The plating in the presence of additives occurs through a large number of possible interconnected reactions that happen between the Cu surface, additives and various ions [3]. The first reaction is the adsorption of the suppressor PEG at the outer surface of the via, as PEG diffuses slowly and adsorbs quickly. In a Cl^- -containing solution, it was proposed that PEG grasps the positive Cu ions to form a complex, which then binds to the negatively-charged Cl^- ions on the Cu surface [9]. This results in the formations of a $\text{PEG}-\text{Cu}^+-\text{Cl}^-$ complex on the copper surface that has been verified by surface-enhanced Raman

PEG-Cu-Cl structures

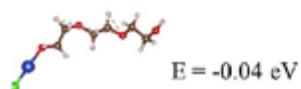
a) Cu bind to single O atom



Cu bind to two O atoms



Cu bind to side O atom



b) Cu bind to single O atom



Cu bind to two O atoms

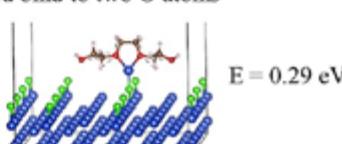


Figure 1: Formation of PEG-Cu-Cl complex. Total energy for: a) Cu atom binding to an O atom in different positions; and b) binding of PEG-Cu-Cl complex to the Cu electrode.

PEG-Cu-Cl interaction with Cu slab

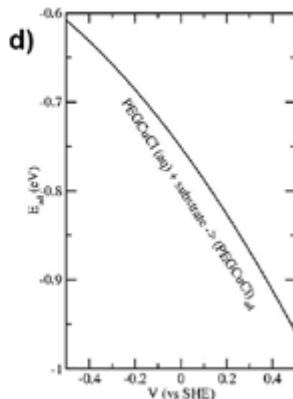
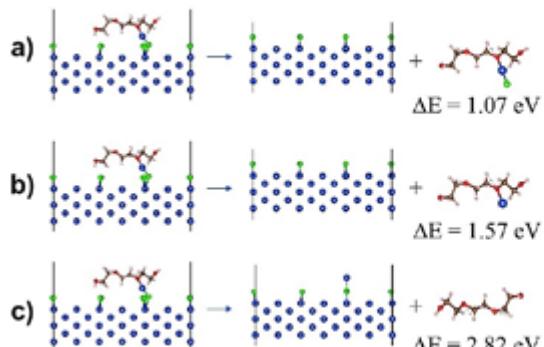


Figure 2: Dissociation energies computed for: a) Cu(sub)-Cl bond; b) Cl-Cu(complex) bond; and c) Cu(complex)-O bond shown in d) as a function of applied bias.

spectroscopy measurements [10], and this inert layer prevents further plating on the surface, thereby achieving a suppressing effect. To study this process, we have performed calculations of a PEG complex adsorbed on a chloride-covered Cu (110) surface with 0.25 coverage. To make the calculations feasible, we have represented PEG with a segment of three monomers $\text{HO}(\text{C}_2\text{H}_4\text{O})_3\text{H}$ due to size constraints. Also, we found that chloride ions prefer the bridge site at 0.25 coverage.

By performing total energy calculations on isolated PEG-Cu-Cl complexes in the presence of our model dielectric solvent, we have identified that the Cu ion prefers to bind to the side oxygen of PEG. Next lowest in energy is for the Cu to bind to one of the middle O atoms, and the configuration with Cu bound to two middle oxygen atoms on PEG is least

stable (**Figure 1a**). This might be due to the electrostatic repulsion between the O atoms in this configuration. Because the real PEG polymer in the experiment contains many more middle than side oxygen atoms, we only consider binding to middle O atoms when studying PEG-Cu-Cl complexes adsorbed on the electrode surface (**Figure 1b**). We find again that the energy of a PEG-Cu-Cl complex with its Cu binding to one middle O atom is preferred to that where it binds to two.

Using the result discussed above, we focus on geometries where the Cu in the complex is bound to a middle O atom on PEG and investigate different modes of decay for the complex adsorbed on Cu (110). We computed the dissociation energy of the PEG complex through breaking the (a) Cu(slab)-Cl bond (**Figure 2a**), (b) Cl-Cu(complex) bond (**Figure 2b**) and (c) Cu(complex)-O

bond (**Figure 2c**). These calculations are performed on neutral systems in the presence of our model solvent. As can be seen, the system is stable to decay for all three modes with the lowest energy mode being breaking the Cu(slab)-Cl bond. Next, we specialize to this mode and investigate the dependence of the binding energy of the PEG-Cu-Cl complex on the applied bias (**Figure 2d**). It can be seen that the adsorption energy of PEG-Cu-Cl varies from ~ -0.6 to -1eV over a range of $\pm 0.5\text{V}$ vs. standard hydrogen electrode (SHE). The adsorption gets weaker for more negative voltages and this might be due to the repulsion between Cl^- and the negative charge on Cu. Also, this is consistent with the experimental observation that the suppression effect of PEG in a chloride solution disappears for sufficiently negative voltages as the PEG complex gets desorbed [11].

SPS/MPS accelerator

For the accelerator, bis-(3-sulfopropyl) disulfide (SPS) diffuses faster than PEG on account of its smaller mass and quickly descends into the via, thereby promoting plating in the via. Outside the via, PEG dominates initially as it adsorbs much faster than SPS, and plating is slowed. One of the proposed accelerating mechanisms is shown in **Figure 3** [4]. SPS is first physisorbed on Cl^- -covered Cu and diffuses to areas of exposed Cu. The Cu then catalyses the decomposition of SPS into two adsorbed mercapto-1-propanesulfonate (MPS) molecules by breaking the S-S bond, and there is partial desorption of these molecules into the solution. One of the acceleration mechanisms is that the adsorbed SPS and MPS competes for space with the suppressor, thereby allowing plating where PEG is absent or replaced by the accelerator. Another possible reaction is the conversion of MPS to SPS accompanied by the reduction of Cu^{2+} to Cu^+ ions, an important precursor for copper plating. Finally, the desorbed MPS can also dissociate the PEG-Cu-Cl complex by attacking the Cu-O bond, resulting in the release of PEG and adsorption of MPS on copper. In addition to the above reactions, we have studied two MPS formation reactions where Cu^+ is oxidized to Cu^{2+} and SPS is converted to MPS [3].

To study the above reactions, we first compute the adsorption



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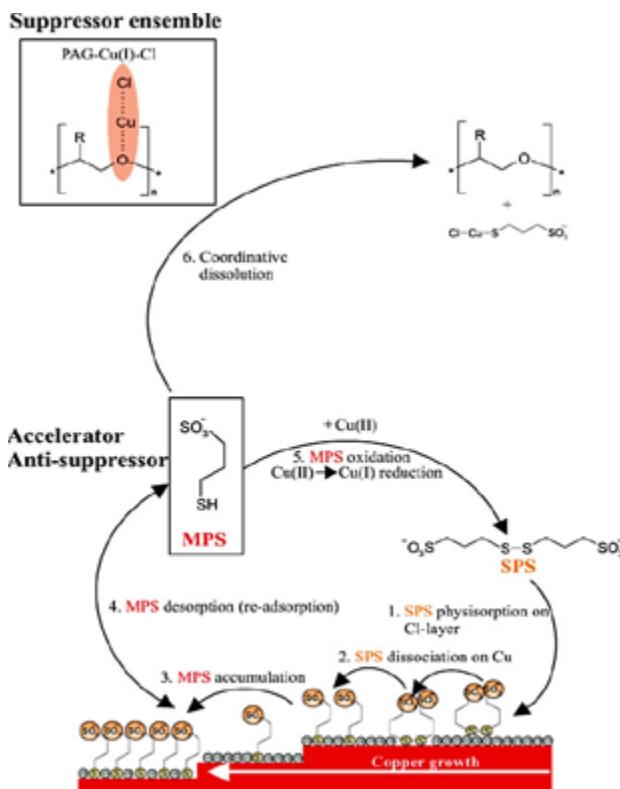


Figure 3: One of the proposed mechanisms of the accelerator.

Adsorption of SPS, MPS and PEG

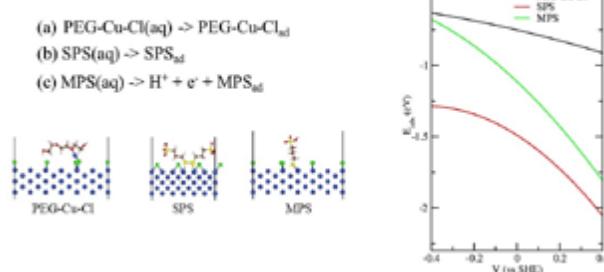


Figure 4: Adsorption energy of PEG-Cu-Cl complex, SPS and MPS on the electrode surface.

MPS formation

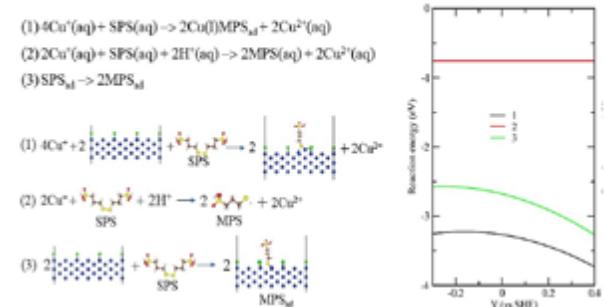


Figure 5: Reaction energies as a function of applied bias for proposed mechanisms for the formation of MPS.

energies of SPS and MPS on Cu (110) with 0.25 Cl⁻ coverage. As before, we study the adsorption energies over a range of applied biases using the charging method and model dielectric solvent [5-7], and the results are plotted in **Figure 4**. Both SPS and MPS are known to adsorb on the thiol end [11] and MPS preferentially adsorbs on a Cu bridge site, while SPS approximately adsorbs with S atoms sitting on the top sites of Cu. These energies show some dependence on applied bias with adsorption decreasing for more negative biases. Importantly, E_{ads} is larger for both MPS and SPS than for the PEG complex. This is in good agreement with the fact that SPS and MPS are good accelerators that can block out or replace the PEG complex on the Cu surface, and lends support to our primary accelerating mechanism.

Next, we assess the previously proposed MPS formation reactions and these are depicted in **Figure 5a** with the reaction energies plotted in **Figure 5b** [3,4]. As can be seen, all the reaction energies are negative, and they are all feasible reaction routes. Between reactions (1) and (2) that both oxidize Cu⁺ to Cu²⁺ and convert SPS to MPS, the first reaction that results in MPS adsorbed on Cu is energetically much more favorable than the one with solvated MPS, mostly because an additional Cu⁺ ion is captured onto the surface and binds to MPS relative to the second reaction. For reaction (3) where SPS is deposited and decomposed into two adsorbed MPS molecules, the reaction is also energetically very favorable, with the adsorption of SPS accounting for half of the reaction energy and dissociation of adsorbed SPS to two adsorbed MPS molecules giving rise to the other half. We also see that the second reaction, which does not involve the substrate or change in number of electrons does not have a bias dependence, while reactions (1) and (3) are more favorable for positive biases around 0V vs. SHE.

It was also proposed that the MPS in solution may dissociate the PEG-Cu-Cl complex by attacking it at the Cu-O bond, replacing it with MPS-Cu-Cl and releasing PEG in the process [3,4]. In our calculations, we consider two possible geometries for the final MPS-Cu-Cl complex. One is with the complex adsorbed on the surface, with its Cu binding to both surface Cu and Cl (reaction 1). The second calculation is that the complex is solvated (reaction 2). With this set up, we computed the reaction energies as shown in **Figure 6**, and the case with MPS-Cu-Cl solvated is energetically unfavorable, while the case with the complex adsorbed on the surface is much more favorable. This result is due to the strong slab-complex bond that needs to be broken for the case where MPS-Cu-Cl is solvated. Finally, we have also studied the reaction where MPS reduces Cu²⁺

Displacement Reactions + MPS to SPS conversion

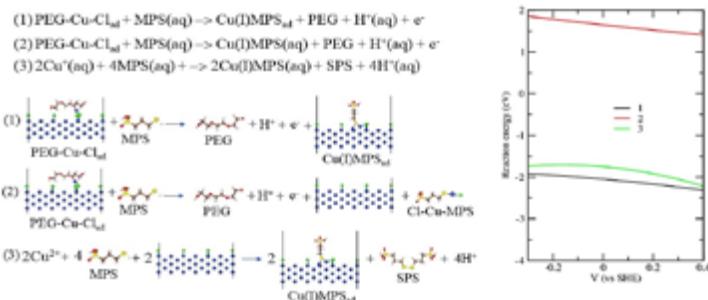


Figure 6: Reaction energies of the proposed acceleration mechanism of MPS by dissociation of PEG-Cu-Cl complexes.

to Cu⁺ and gets converted back to SPS (reaction 3), and it was found to be energetically favored. Additionally, it can also be seen from **Figure 6b** that the reaction energies are slightly more favorable at positive biases, but only weakly dependent on bias.

In summary, using our DFT calculations we have verified that the PEG-Cu⁺-Cl⁻ complex formation is the essential step in the fast adsorption of the suppressor. For the accelerator mechanism, we have shown that the dissociation of SPS to MPS is the intermediate that can replace the suppressor and also enable the reduction of Cu²⁺ to Cu⁺.

Kinetic Monte Carlo model

In the following we present a kinetic Monte Carlo (KMC) model developed to understand the role of the reaction and transport kinetics of the ions and various additives during the electrodeposition of the TSVs. The KMC model has been developed as a bridge between the first-principle DFT calculations and the continuum phase-field models. A solid-by-solid (SBS) KMC model for the surface reactions, which also includes migration of ions in the electrolyte as a random walk developed by Kaneko et. al [12], could show the formation of voids and their influence on bottom-up filling. A two dimensional model, including the role of additives, has been developed by Fukuiage, et al. [13], applying different waveforms of applied current. In our KMC model, the various reactive and transport processes are executed with probabilities proportional to their rates. These rates will be calculated from the activation barriers obtained by DFT and molecular dynamics simulations. The results from the KMC simulations can aid in identifying the relevant parameter space for detailed continuum models like phase-field simulation models. In this model, apart from the Cu²⁺ metal ions and the copper electrode, we consider the roles of the accelerators and suppressors in the reaction kinetics. The features of these additives are as follows:

1. Accelerator(A) diffuses faster than suppressor(S)
2. $D_{Cu^{2+}} > D_A > D_S$
3. The presence of a suppressor decreases the rate of attachment of the metal ion to the electrode.
4. The presence of an accelerator increases the rate of attachment of the metal ion to the electrode by altering the energy of the affinity (bond) of the metal ion to the electrode.
5. There is a dependence of metallization on the curvature, i.e., the corners have a lower attachment barrier compared to the side walls.
6. Activation barriers for the attachment of Cu²⁺ ions to the TSV substrate Cu with and without the additives is represented by:

$$E_{att}^{Cu-Cu^{2+}}(A) < E_{att}^{Cu-Cu^{2+}} < E_{att}^{Cu-Cu^{2+}}(S)$$

7. The accelerator replaces the suppressor in the growth front according to:

$$E_{att}^{Cu-Cu^{2+}} < E_{att}^{Cu-A} < E_{att}^{Cu-S}$$

8. The concentration of the accelerator is 1-2 orders less than that of the suppressor as follows:

$$c_s \sim (5 * c_A, 100 * c_A)$$

9. The concentration of the suppressor is 1-2 orders less than that of the metal ion as follows:

$$c_{Cu^{2+}} \sim (5 * c_A, 100 * c_S)$$

10. $E_{nuc}^{Cu-Cu^{2+}}$ represents the barrier for nucleation of a new metal layer on the substrate, which is proportional to the number of metal adatom-substrate bonds.

11. The different barriers for nucleation on flat surfaces and on corners is given by the ratio:

$$r_{nuc} = \frac{E_{nuc}^{Cu-Cu^{2+}}(\text{corners})}{E_{nuc}^{Cu-Cu^{2+}}(\text{flatsurface})}$$

12. Details of levelers, different types of metal ions, actual bond energies, concentration and electric field dependence are not included in our model.

In our model, we consider the following events:

- Deposition of Cu ions on the electrode (substrate);
- Migration of copper ions and additives;
- Decay of additives;
- Attachment of additives to the substrate; and
- Enhancement or reduction of the attachment barrier for Cu to the substrate in the presence of additives.

The top of the TSV is open to the electrolytic bath, which acts as a source of Cu ions and additives.

The KMC model with the above mentioned features has been developed and the simulations results can guide the phase-field

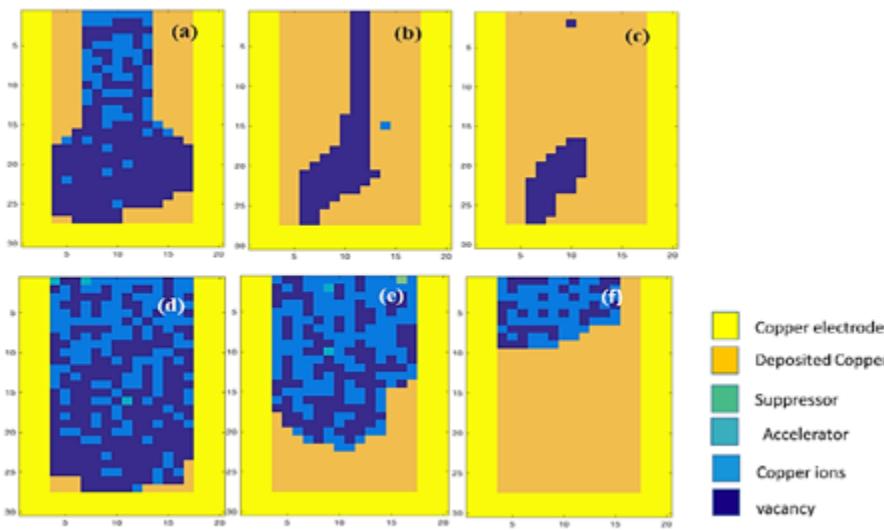


Figure 7: Formation of voids in TSV fillings for different ratios of nucleation barrier (r_{nuc}) for side walls to corners. In (a-c): $r_{nuc}=0.1$ and in (d-f) $r_{nuc}=0.01$.

simulations by identifying the relative parameter space for the different players in the electroplating process. In all the results presented below, we have used the following parameters:

$$c_S=0.05; c_A=0.01; c_{Cu^{2+}}=0.3; T=0.1; E_{diff}(Cu^{2+})=0.1; E_{diff}(A)=0.05; E_{diff}(S)=0.09;$$

In **Figure 7a** we show the simulation results with different nucleation barriers for the side wall relative to that at the corners. For a ratio $r_{nuc}=0.1$ shown in **Figure 7a-c**, the metallization on the side walls is enhanced compared to the bottom (**Figure 7a-b**). In **Figure 7c**, a void can be seen clearly at the bottom as a result of the closing of the via at the top. In **Figure 7d-f**, the results of the simulations for a ratio $r_{nuc}=0.01$ is shown. In this case, metallization starts from the two corners in the bottom (**Figure 7d**), which results in bottom up growth (**Figure 7e**) and therefore, void-free filling of the TSV (**Figure 7f**). A lower attachment on the walls could be caused by an increase in suppressor species, which is a slowly diffusing additive. The higher attachment at the corner is due to the corner effect (enhancement by curvature) in addition to the increase in accelerator species, as it is a faster diffusing additive and can reach the bottom faster than the suppressor. As the suppressor is a slowly diffusing additive, it is mainly effective in the top of the via and thereby reduces the growth at the top of the via and delays the pinching off of the void. **Figure 8** shows the KMC model results for two different aspect ratios.

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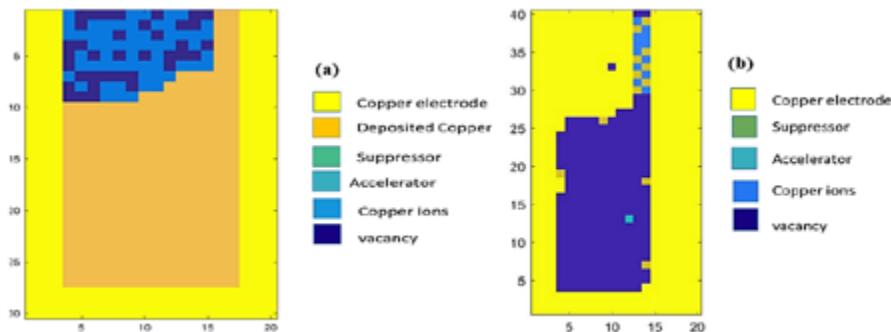


Figure 8: The role of aspect ratio in TSV filling: a) Bottom up filling for an aspect ratio of 1.5; and b) Void formation for an aspect ratio of 2.

Figure 8a shows the bottom-up filling for an aspect ratio of 1.5 and **Figure 8b** shows formation of the void for an aspect ratio of 2. As the aspect ratio increases, it takes longer for the Cu²⁺ ions and accelerator to reach the bottom of the via than the growth time at the walls. This results in faster growth at the top of the via resulting in a void. These results are consistent with the results obtained in experiments [14].

Summary

The various energies and barriers for the different species in the system that are required for the KMC model will be obtained from the first-principle calculations described in this article. The results of the KMC model can identify the parameter space of efficacy for the continuum phase field model. The objective of the continuum phase field model is to simulate the electroplating process and predict the microstructure in the TSV. In summary, we have developed first-principle calculations to understand the reaction mechanisms and chemistry and a KMC model to incorporate these data to obtain the rate kinetics of the electroplating process. These tools, in addition to the continuum models being developed (level-set and phase-field models), will form a single platform to model and optimize the electroplating of through-silicon vias with different aspect ratios.

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Understanding the impact of silicone contamination on semiconductor package performance

By Jaimal Williamson *[Texas Instruments]*

The detrimental effect of polysiloxanes, or silicones, and their contribution to delamination and contamination at various material interfaces dates back decades. Their impact is as ubiquitous in microelectronics as the widespread use of copper interconnects. For example, it is reported in past literature [1] that as little as 10 parts per million (ppm) of silicone adsorbing from the atmosphere on an electrical contact was sufficient to degrade contact performance. As described in the cited literature, the catastrophic effects of silicone contamination are notorious and well documented across multiple industry sectors and applications [2,3].

This article examines atomic mass unit distribution of a wide range of silicone oligomeric compounds (based on a standard silicone encapsulant packaging material), including a series of analytical techniques to understand material outgassing behavior during cure. Specific analytical tools like thermogravimetric analysis/Fourier transform infrared spectroscopy (TGA-FTIR), direct insertion probe – mass spectrometry (DIP-MS), time-of-flight secondary ion mass spectroscopy (ToF-SIMS), and X-ray photoelectron spectroscopy (XPS) were used in tandem as complementary techniques to study silicone outgassing behavior and contamination adsorbed on semiconductor-based copper (Cu) lead frame package and silicon die surfaces. Cure profiles were compared and simulated using TGA-FTIR and DIP-MS to determine qualitative and quantitative amounts of silicone contamination outgassing. Surface-sensitive ToF-SIMS and XPS techniques were used to analyze the adsorbed silicone contamination on the aforementioned chip and package surfaces post cure.

To elucidate chemical information of the silicone contaminant, DIP-MS data was overlapped between mass-to-charge ratio (m/z) and time (on the x-axis) to understand

the mass unit (degree of polymerization) and the specific time the silicone fragment outgassed as a function of cure temperature. Chemistries of silicone fragments generated from DIP-MS were compared qualitatively to chemical structures of silicone species found on the die surface from the ToF-SIMS analysis. XPS was used to compare atomic concentration of silicone contaminant adsorbed on the Cu lead frame surface based on the binding energy associated with siloxanes and silica as a function of the cure condition. The synergy obtained from the use of multi-analytical instrumental techniques was essential to determine the effect of cure temperature and time on silicon contamination. Results directed a path for the optimization of the semiconductor package assembly process flow.

Silicones are a universal choice for original equipment manufacturers (OEMs) and outsourced semiconductor assembly and test (OSAT) sites as materials to support die attach, glob top, lid attach, and general encapsulation for an array of semiconductor package applications. Because silicone chemistry is impervious to moisture and thermally stable across a wide temperature range, it is an attractive material for a myriad of microelectronic applications. However,

formulating a silicone material with ideal physical and chemical properties, such as a high degree of chemical inertness and resistance to extreme temperatures, leads to consequences in a semiconductor package assembly environment. For example, enabling material versatility in silicone formulations can be made polydisperse, where many short chain oligomers of varying mass unit can outgas at different periods during the cure profile. In addition, solvents added for rheological control can exacerbate the outgassing phenomenon of silicones contaminating onto adjacent surfaces and components.

For these reasons it is important to fully characterize the impact of cure conditions in terms of the ramp time, terminal temperatures, and dwell times in relation to the outgassing effect. This article focuses on using TGA-FTIR, DIP-MS, ToF-SIMS and XPS to study the silicone oligomeric fragments outgassing during cure to enable a path to mitigate the magnitude of adsorbed silicone contaminants on adjacent silicon and the lead frame surface that impact adhesion. The information extracted is used to improve chip to package integrity (i.e., chip and lead frame adhesion to mold compound) and optimize package assembly process flow.

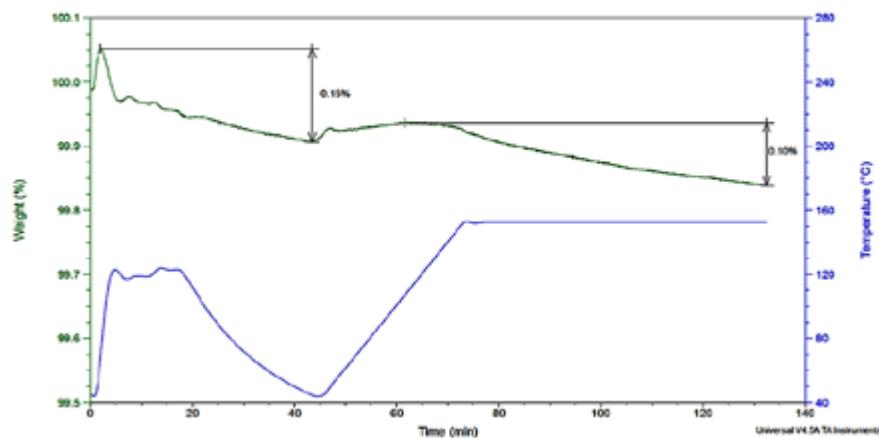


Figure 1: TGA thermogram plot showing the weight of a silicone material from a generic cure profile up to 150°C.

TGA-FTIR / DIP-MS analysis

In an initial exercise, a generic cure profile was simulated via TGA to understand weight loss of a silicone material commonly used for die (silicon chip) encapsulation. Per **Figure 1**, it is observed that there is 0.15% weight loss or 1,500ppm of material outgassing in the initial stages of the simulated cure profile. As mentioned previously, weight loss of 1,500ppm is 2x orders of magnitude beyond what is sufficient for a silicone contaminant to adsorb on a surface as reported in related literature [1].

From the FTIR spectra (see **Figure 2**), where an IR spectrometer interfaced with TGA, the data collected is consistent with siloxane outgassing as evidenced by absorption at $\sim 1090\text{cm}^{-1}$. The 1090cm^{-1} wavenumber is characteristic of Si-O-Si stretching mode signifying the siloxane bond. From the FTIR spectra, the Si-O-Si peak is apparent, but weak and further attenuates with increasing temperature.

To add more granularities to the results, DIP-MS was used as a supplemental experiment to gain more resolution to the TGA-FTIR data from both a qualitative and quantitative material identification standpoint. From the DIP-MS technique, the sample is located on a tip of the probe and introduced to an ionization source in a vacuum chamber. The evaporated or pyrolyzed gas species is instantly ionized, and swiftly transferred to the mass analyzer. The mass spectrometer interfaced with the DIP allows the chemical structure of polysiloxane oligomer to be identified as it corresponds to its mass unit. Another added benefit of the DIP-MS analysis is that the breakdown of siloxane fragments allows an account of the degree of polymerization of the oligomers. This data provides a glimpse of the polydispersity of the silicone formulation, where understanding molecular weight distribution is helpful for correlating the ToF-SIMS results (presented later in the article).

From **Figures 3a-c**, the relative abundance (or peak ion intensity) of the outgassing species is compared vs. time or vs. the mass-to-charge ratio (m/z) on the x-axis. Using **Figure 3a** as the reference, **Figure 3b** includes the mass spectra from $\sim 0.5\text{min}$ and 3.25min , which corresponds to the spectra illustrated by the blue brackets in **Figure 3a** from $\sim 50^\circ\text{C}$ to 150°C . **Figure 3c** shows the mass spectra covering the balance of the data from $\sim 4.7\text{min}$ and 9min (again referencing

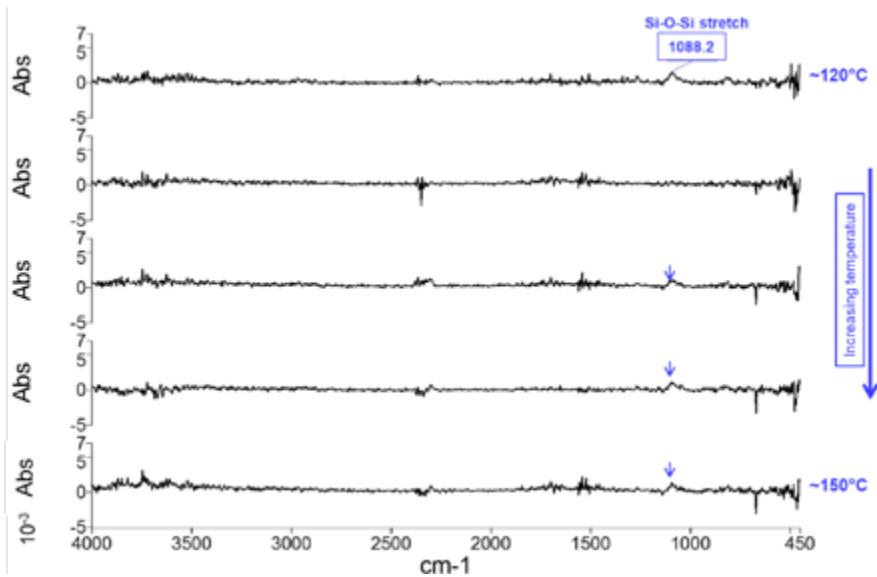


Figure 2: IR spectra showing siloxane moiety detected as an outgassing component.

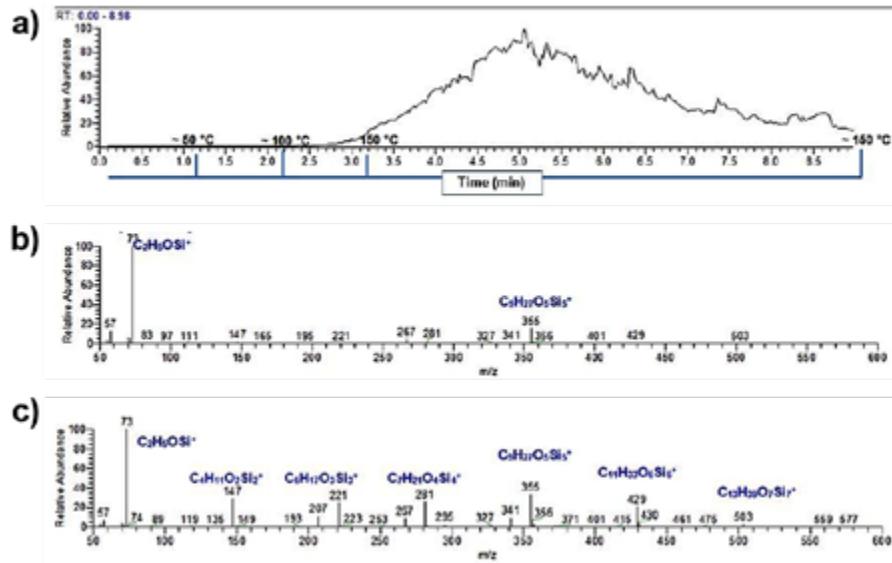


Figure 3: a) DIP-MS plot overlaying temperatures of $\sim 50^\circ\text{C}$, 100°C , and 150°C corresponding to simulated cure time; b) DIP-MS plot showing outgassing components between $\sim 0.5\text{ min}$ and 3.25 min corresponding to temperatures of $\sim 50^\circ\text{C}$, 100°C , and 150°C ; c) DIP-MS plot showing outgassing components between $\sim 4.7\text{ min}$ and 9 min corresponding to a temperature of 150°C .

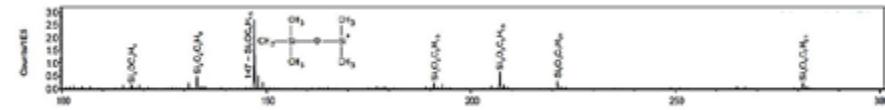


Figure 4: ToF-SIMS positive ion spectra showing various siloxane fragments and sizes of outgassing.

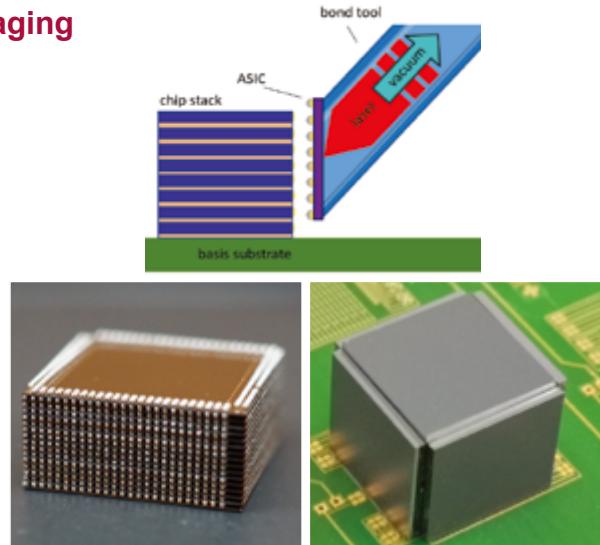
Figure 3a across the isothermal period at 150°C). In **Figure 3b**, which shows mass spectra results upwards to 150°C , a high-intensity siloxane fragment $\text{C}_2\text{H}_5\text{OSi}^+$ of $73\mu\text{u}$ is apparent. This mass unit is consistent with the molecular weight of a dimethyl siloxane fragment. In contrast,

Figure 3c denotes an isothermal curing period at 150°C and indicates a much wider atomic mass unit distribution of siloxane fragments. The main takeaway is that the mass spectra from **Figure 3c** provide evidence of the polydispersity of the silicone formulation.

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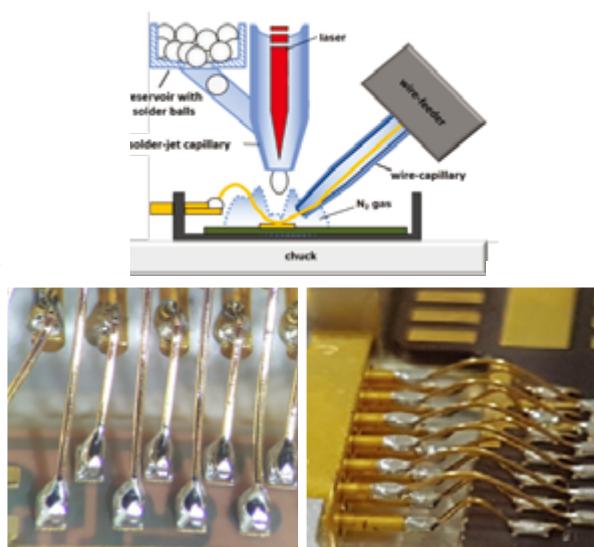
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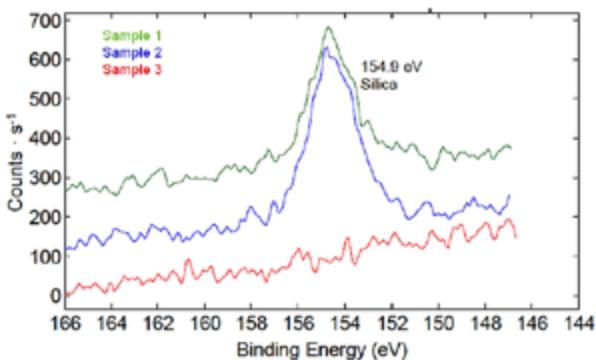


Figure 5: High-resolution XPS data of silicon Si 2s peak.

Connecting the dots between analytical techniques

With a fundamental understanding of the outgassing behavior of the silicone material based on the aforementioned TGA-FTIR and DIP-MS studies, surface analysis was performed on actual semiconductor package samples where adhesion was compromised on account of silicone contamination. Key findings from the TGA-FTIR and DIP-MS results, such as an indication of the polydispersity of the formulation and mass units of siloxane fragments as a function of time and temperature, were leveraged for relative qualitative correlation to chemistry found from ToF-SIMS spectra. Although it is understood that ToF-SIMS data is considered semi-quantitative (at best) and depends on matrix effects, ionization probabilities, sample charging, topography, etc., the general cross-reference of chemical species is the goal to assist assembly process optimization efforts.

From ToF-SIMS, both silicon die and Cu-based lead frame surfaces were analyzed. In **Figure 4**, the die surface was analyzed for silicone contamination based on its close proximity to a silicone encapsulant material employed in the assembly process. The positive ion mass spectra show similar polydispersity of silicone fragments as illustrated from the DIP-MS data (see **Figure 3c**) and upwards to a carbon number of seven.

Interestingly, no siloxane content was found on the Cu lead frame surface. The reason for no silicone content was hypothesized as a chemical reaction taking place with the adsorbed silicone contaminant and plating material on the

Cu lead frame surface yielding silica. XPS was not performed on the die surface because of the difficulty of discerning between the siloxane (silicone contaminant) and silicon die passivation material, which are detected at similar binding energies. However, XPS was performed on Cu lead frame surface and corroborated the ToF-SIMS results with no siloxane detected.

No atomic concentration of silicone contaminant on the Cu lead frame surface reinforced the aforementioned hypothesis based on silica being detected. **Figure 5** shows high-resolution XPS data of the silica detection.

The data obtained from TGA-FTIR, DIP-MS, ToF-SIMS, and XPS provided a consistent story. The silicone contaminant is polydisperse and multiple outgassing species are deposited on the silicon die surface. Most importantly, the data provided observations at what point in the cure process a maximum amount of silicone contamination was adsorbing on chip and package interfaces. A fundamental knowledge of materials science is a key driver in interpreting these comprehensive results as generated from curing profile simulation and surfaces with adsorbed silicone contamination. This knowledge can be transferred to optimizing the assembly process flow (i.e., cure profile) and/or the material set for improved chip-to-package interaction.

Summary

A unique mix of analytical tools covering TGA-FTIR, DIP-MS, ToF-SIMS, and XPS enabled silicone characterization at both macro and monolayer scales to direct a path for semiconductor package assembly optimization. Macro scale analysis was performed on a bulk silicone encapsulant packaging material via TGA-FTIR and DIP-MS to understand outgassing behavior as a function of cure time and temperature. Surface-sensitive analytical tools, such as ToF-SIMS and XPS, were used to study

actual silicon die and Cu-based lead frame surfaces of semiconductor package units susceptible to silicone contamination.

DIP-MS and ToF-SIMS spectra proved the polydispersity of the silicone encapsulant formulation. Results showed a wide range of siloxane fragments with varying mass unit. DIP-MS spectra demonstrated two key factors:

- 1) The time when the specific siloxane fragment outgassed during cure with respect to cure temperature; and
- 2) The mass-to-charge ratio of the siloxane component.

Using DIP-MS results as a cross reference, common silicone chemical fragments were compared from the ToF-SIMS spectra for relative qualitative assessments to associate contamination on the silicon die surface from actual semiconductor package units. Specifically, the cross-reference data enabled a link to understand how silicone outgassing behavior during the cure process affected adsorption of chip and lead frame surfaces of a semiconductor package. Ultimately, the methodical process of examining the silicone material in bulk and as an adsorbed contaminant at macro and monolayer scales, respectively, facilitated a path to optimize the assembly process flow and/or material set.

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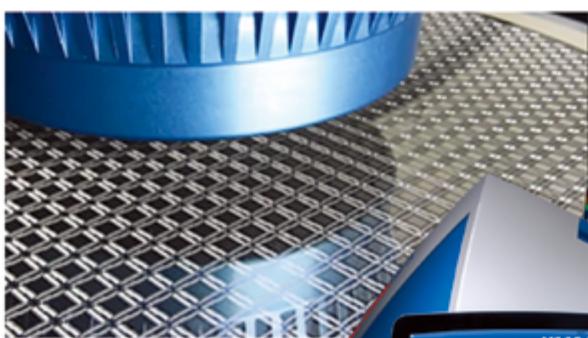
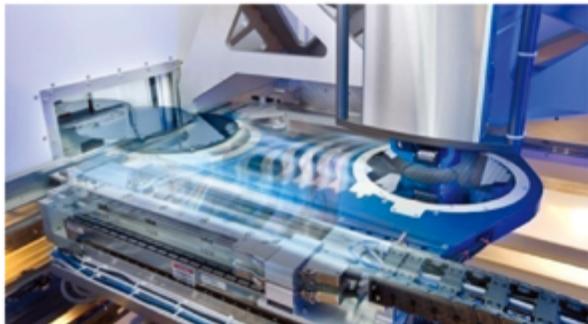


Biography

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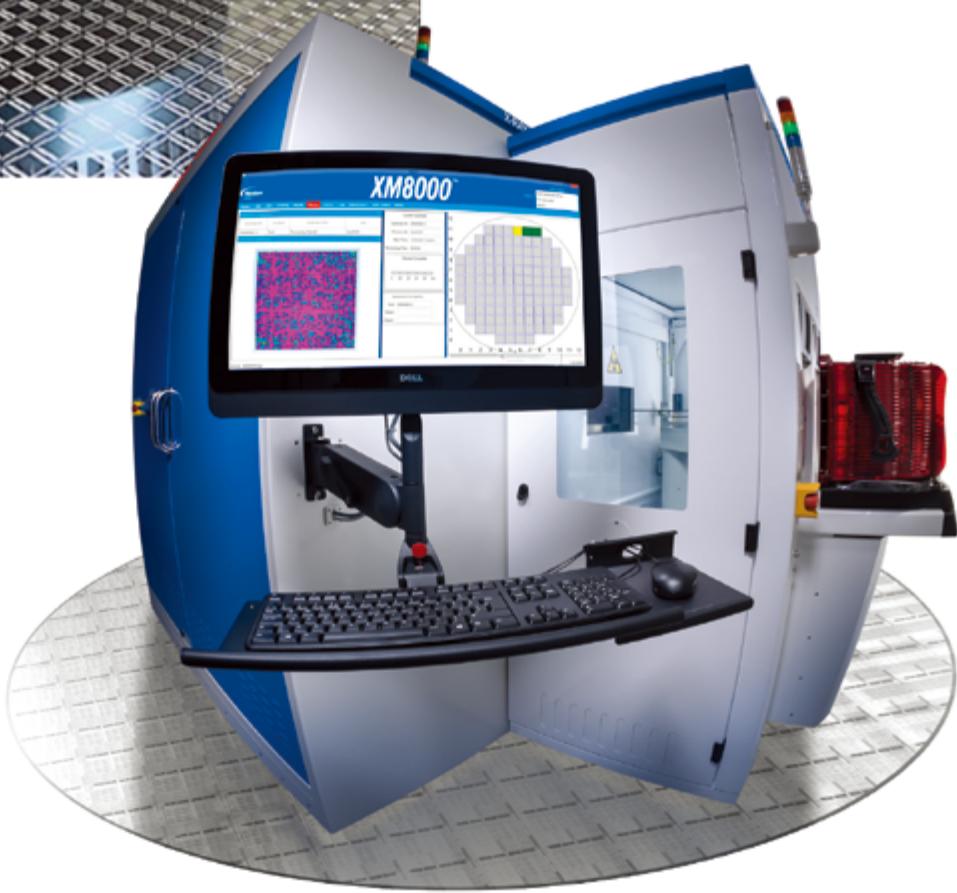
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Failure relief in WLP and PLP polymer layers

By Robert L. Hubbard *[Lambda Technologies, Inc.]*

This article was originally published in the Proceedings of the International Wafer-Level Packaging Conference 2018.

To avoid material stresses in fan-out wafer-level and panel-level packages that create warpage, cracking, delamination, and thermal instabilities, the use of coefficient of thermal expansion (CTE) matching and the lowest possible process temperatures has been a focus with this technology. Data is provided to show that this approach is actually causing more stress and crack propagation than is necessary, especially for large wafers and panels. An understanding of the source of these chemical, mechanical, and thermal instabilities is offered with methods for avoiding these issues. Reduced warpage and bow, increased fracture energies, and wide-area film uniformity data will be shown to be possible on the largest of substrates with the use of low-temperature curing by variable frequency microwave curing. A method is also described for increasing the speed and reducing the cure temperature even further with customized resins.

Introduction

There are as many different constructions and processes used in wafer-level and panel-level packaging (WLP/PLP) as there are practitioners, but a common stack-up consists of an array of silicon die encapsulated in a thermoset polymer with multiple redistribution layers of metal traces and thermoplastic dielectric coatings. As with most packaging designs, there are silicon and metal layers with low CTE values, and organic polymer layers with high CTE values. This well-known “CTE mismatch” creates stress at the interfaces when temperatures are changed during subsequent process steps and when the products are in the field. Additional stresses are developed in the polymer layers during the chemical reactions necessary in thermal polymerization steps (“curing”). An example of the layers used in fan-out wafer-level packaging (FOWLP) is shown in **Figure 1** (not to scale).

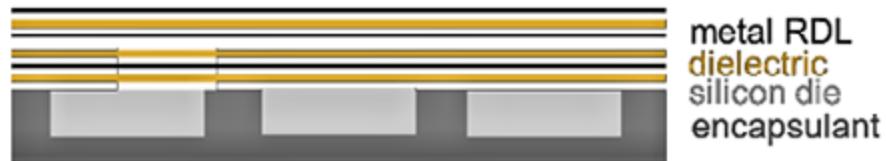


Figure 1: Generic FOWLP construction (not to scale).

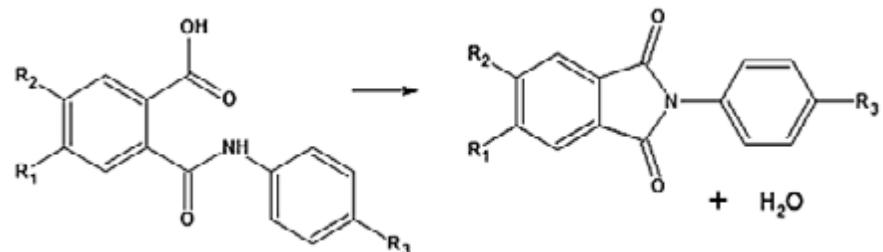


Figure 2: Polyimide curing.

Many users of the chemicals in thermal polymerization are unfamiliar with the sources of these stresses and the mechanisms that create delamination, cracking, part movements, and instabilities in these materials. The resultant polymer layers often do not have the expected properties listed on the technical data sheets from the material suppliers.

In many cases there are intentional short cuts taken in the cure processing temperatures and times to produce more cost-effective but “good enough” quality. These short cuts appear to produce workable results at each step but contribute to incipient failures at later steps or failures in product lifetimes. The failures are not always traced back to the “good enough” choices made during processing and result in costly poor reliability at the customer.

As the size of packaging increases from single-die to multi-die packages, and now to wafers and panels, these issues become not only more numerous, but size specific. New methods for producing very large (and more cost-effective) panels lead to more possible sources of failure in process and product. A better solution would be to understand the inherent properties of

the materials and to take steps to produce reliable chemical, mechanical, and thermal stability at each manufacturing step.

Polymer cure fundamentals

The following sections discuss some fundamentals of thermal polymerization that may not be widely known. The critical nature of cure temperature is common to both thermoplastics (for redistribution layers) and thermosets (for encapsulation) despite very different cure mechanisms.

Thermoplastic dielectric layers. Most polymer dielectric films are thermoplastic, which simply means that the supplied resin is an already polymerized long chain structure that has features along the chain that can be changed in a manner that creates a more rigid insoluble film. When cured thermoplastics are heated above their softening points, they can be cooled back down to a different shape than where they started. The most popular of these is the polyimide (PI) film made from a polyamic acid or ester resin. The reaction creates closed rings along the chain as shown in **Figure 2**.

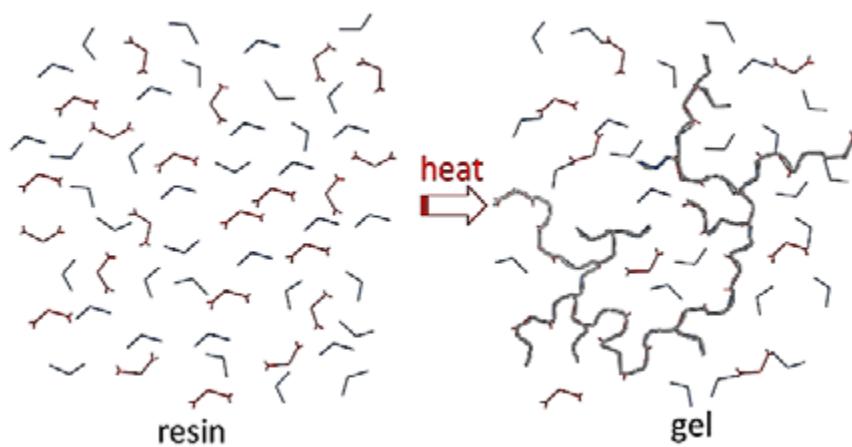


Figure 3: Thermoset polymerization.

Polyimides have high thermal, chemical and mechanical stability at the price of high curing temperatures (350°C or higher). Polybenzoxazoles (PBO) are a similar thermoplastic dielectric that can have the advantages of lower cure temperature ($225\text{-}320^{\circ}\text{C}$) and can be developed in aqueous solutions. The CTE of PBOs is also much higher ($60\text{-}80\text{ppm}/^{\circ}\text{C}$) than PIs ($30\text{-}40\text{ppm}/^{\circ}\text{C}$) when fully cured. There are claims of even lower cure temperatures, but to obtain the desired stable properties, the cure temperatures end up being in excess of 200°C . Inadequate cure temperatures for PI and PBO films are responsible for film cracks and brittleness, which would seem to be the result of over-heating the polymer [1], but are just the opposite.

Thermoset encapsulants and adhesives. Thermoset polymers are the result of two or more small components that combine in polymerization (curing) to form matrix-like networks with dense crosslinks between adjoining chains as portrayed in **Figure 3**. As the chains grow and crosslink, there is a point at which a continuous chain ("infinite polymer") is formed across one dimension of the entire sample (**Figure 3**). This is the point of gelation where the resin with Newtonian liquid properties becomes a gel with Hookean solid properties [2]. At this point the gel is so viscous that heating must be increased to allow the unreacted monomers and ionomers to diffuse to the growing central chain. The role of temperature is critical in thermosets and the behavior and network structure is highly amorphous and complex. It is not

surprising that the time of cure is no longer linear but at least parabolic. The role of temperature is even more important with thermosets than with thermoplastics.

It is necessary for the temperature of cure to be adequate to complete the cure to develop the expected and needed chemical, mechanical, and thermal properties. As the temperature of cure (T_{cure}) increases, the glass transition temperature (T_g) increases with $T_{\text{cure}} > T_g$ until an "ultimate" T_g ($T_{g,\infty}$) value is reached. At this point, the polymer matrix is as fully reacted and complete as possible. A completed polymerization with an ultimate $T_{g,\infty}$ will have the highest thermal stability and fewest unreacted "defect" sites that result in brittleness. The CTE is at a minimum as is the damping factor ($\tan\delta$) and modulus above $T_{g,\infty}$. The adhesion is maximized, as is the fracture energy (G_{Ic}) as measured from the integral of the area of a stress-strain curve (**Figure 4**).

Vitrification of thermosets. If the resin $T_{\text{cure}} < T_g$ at any point during the cure, the material will become glassy (vitrified). The material will appear cured, but is not only incompletely cured, but thermally unstable and brittle as shown in **Figure 5** [3]. A cure with T_{cure} always at least 15° above T_g will proceed directly through gelation into

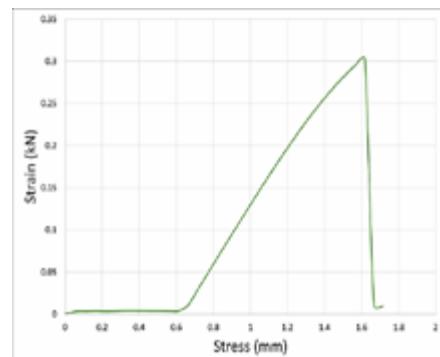


Figure 4: Tension stress-strain curve example.

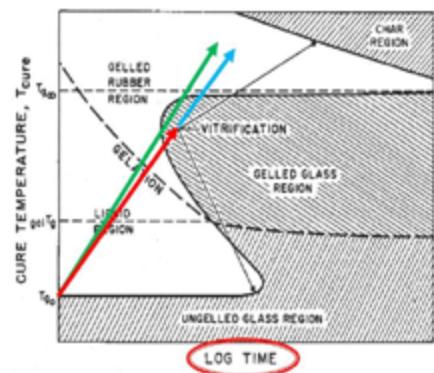


Figure 5: Time-temperature transition graph.

the rubber region as shown by the green arrow. A cure reaction with $T_{\text{cure}} < T_g$ will stop in the gelled glass region (red arrow). If there is another heating process with the $T_{\text{cure}} > T_g$ the material will continue towards completion (blue arrow). It is not feasible to use additional time to complete the cure once it is vitrified because the glass does not allow movement of the molecules to react. Note that the time axis is log(time).

A vitrified glass is incompletely cured, which not only means it has a lower T_g than expected, but also will not have developed adequate adhesion to any surfaces. In **Figure 6**, the example of an epoxide-amine thermoset polymerization develops hydroxyl functional groups during cure. This is the primary source of adhesion of the polymer to metals, ceramics, and other polymers. Fewer cure reactions produce fewer adhesion reactions.

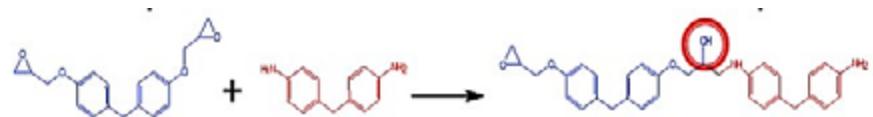


Figure 6: Adhesion production from polymerization.

“Good enough”?

The phrase “good enough” is often used to represent a level of quality that is adequate for the process or product that may not be ideal, but less costly in terms of time, temperature, or resources. There is currently a strong incentive to reduce process temperatures and times to allow higher throughput and less costly material. The reduction of thermoset cure temperatures is directly related [4] to the chemical shrinkage stress in the final material as shown in **Figure 7**.

This is a direct incentive to reduce the cure temperature, and there is also the decrease in stress at lower cure temperatures from mismatched CTE values for polymers and silicon as shown in **Figure 8**. For an underfill cured at 100°C instead of 165°C, there is a nearly 1000ppm difference in thermal expansion. This can be enough stress relief to reduce warpage and double the reliability of the assembly [5,6]. Unfortunately, the amount of time to cure at a lower temperature, even if vitrification doesn’t occur, could be weeks.

The conclusion is that even though lower temperature curing of polymers has significant advantages in stress relief, the greatly extended cure times and the risk of poor chemical, thermal, and mechanical reliability is very high.

A real example

A company wanted to incorporate lower temperature plastics into its mobile products [7]. To avoid melting some of these parts, lower processing temperatures were requested: 1) a 125°C Tg value of the adhesive; and 2) a 60°C cure temperature. The adhesive supplier provided something that might be “good enough:” 1) a 114°C Tg value of the adhesive; and 2) an 80°C cure temperature. There is clearly a problem here because the $T_{cure} < T_{g}$. Sure enough, the measured Tg of the adhesive was only 67°C as seen in the thermomechanical analysis (TMA) graph of **Figure 9**. Adhesion was poor and cracks and delamination resulted.

Specific WLP and PLP temperature sequences can vary across the industry, but an understanding of the critical nature of cure temperature should be a primary consideration for the multiple polymerization steps now being used to make these technologies cost effective and reliable for mass production. The

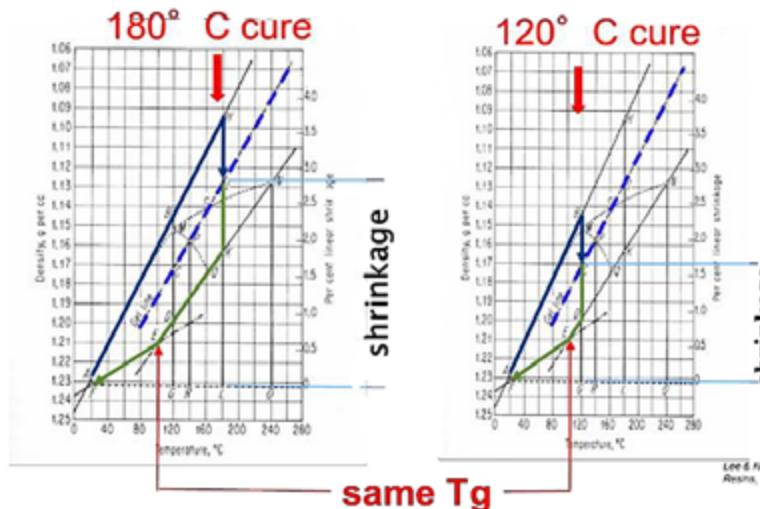


Figure 7: Chemical shrinkage stress.

following scenario highlights the negative effects of inadequate and unstable thermal, mechanical, and chemical properties that can arise. Failure analysis can be more easily determined by examining the hierarchy of process conditions at each step.

If the initial cure of the encapsulant around the reconstituted dice is not complete, the vitrified CTE might be only 30ppm/ $^{\circ}\text{C}$ rather than the target of 12ppm/ $^{\circ}\text{C}$ which leads to more expansion effects (unequal in X and Y) during each of the subsequent much higher cure temperatures (200-300°C) during the redistribution layer (RDL) cures. The encapsulant is continuing to cure at these higher temperatures no matter how short the cure times. The RDL cures might not be complete, leading to CTE values of 100ppm/ $^{\circ}\text{C}$ rather than the expected 60ppm/ $^{\circ}\text{C}$. Any subsequent high

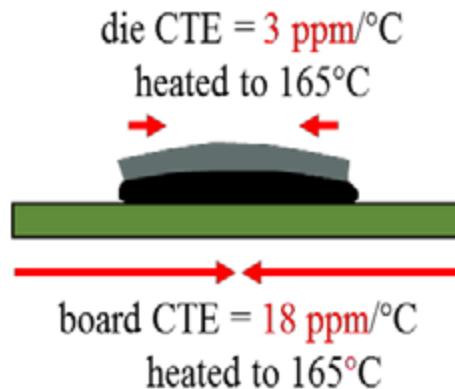


Figure 8: CTE-mismatch stress example.

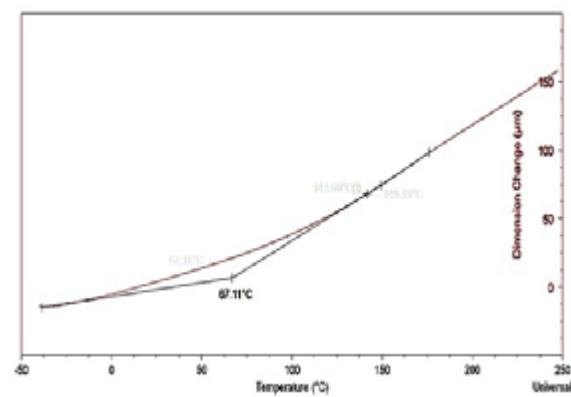


Figure 9: Modulated-TMA graph of adhesive.

are in manufacturing. Each example of incomplete cure produces defects that lead to cracks, which lead to fractures. Stress is usually additive, so it is typically better to minimize stress than to “compensate” for it later. Unfortunately, with conventional heating methods, producing low-cure

temperature materials has been a significant challenge. There is an inverse relationship between thermal stability and low temperature cure in the chemistry of polymer design.

The microwave option

Although microwave systems have been used in volume manufacturing in microelectronics for decades, it will be useful to briefly survey the unusual heating mechanism and the unexpected benefits of this technology for polymerization.

Infrared (IR) electromagnetic energy has been used for many decades in ovens to heat electronic assemblies. Microwave electromagnetic (EM) fields are more recent but create molecular rotation rather than the bond vibrations of IR as seen in [Figure 10](#).

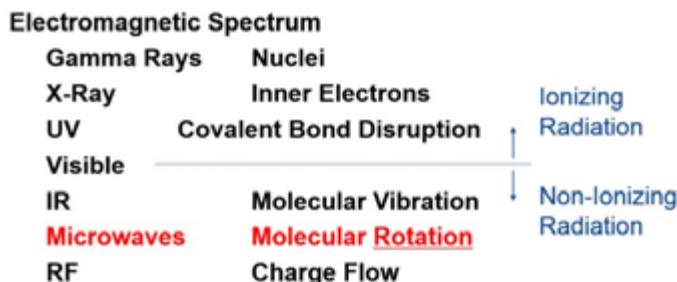


Figure 10: Effects of electromagnetic waves.

The heating mechanism of IR (with air convection) involves short wavelengths, so the depth of penetration into organic materials is only a millimeter. This situation, in turn, means that a thicker bulk eventually carries the heat by incremental induction through the material. Microwaves are longer wavelength energy, so the depth of penetration through organics is on the order of meters. That means the rotational energy activates all of the sample at the speed of light.

Of course a single frequency microwave field, as used in home ovens, would not be practical for industrial use because of nonuniformity and arcing, so the use of variable frequency microwave (VFM) technology was developed and moved into practical applications. The VFM frequency range in the C-band (5.85-6.65GHz) is divided into 4096 frequencies of 25 μ s each over 0.1s before being repeated. This provides a highly uniform field over as much as one cubic meter volume. [Figure 11](#) of an infrared image of a VFM-heated 300mm polyimide-coated (PI) wafer displays the temperature uniformity. The issue of metal arcing is removed because a charged surface cannot be created in only 25 μ s.

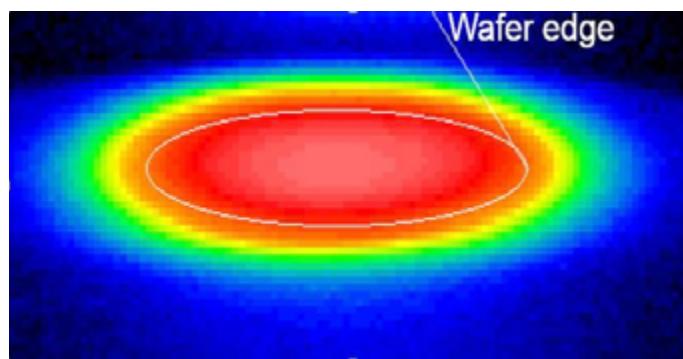
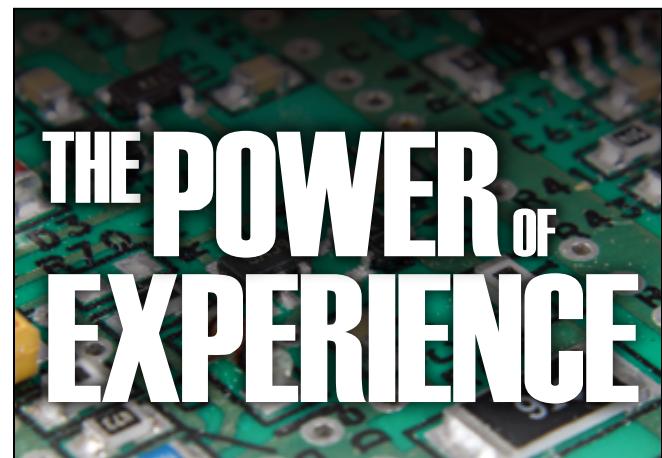
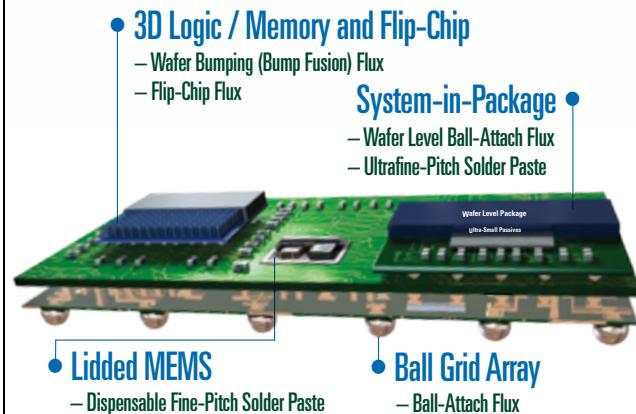


Figure 11: IR image of VFM-heated PI-coated wafer.



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VFM low-temperature curing

The VFM curing of PI dielectric layers for stress-buffer or redistributed layers has been shown at 200-250°C with microwaves rather than 350-400°C by oven. PBO films have been VFM-cured at 170-185°C in as little as 30min cycle time. The extent of cure is sometimes even better than the higher oven cures. Warpage at lower cure temperatures has also been reduced (**Figure 12**). Uniformity of cure in 25 wafer batches has been measured at 1.7% over 300mm wafer.

Thermoset adhesives and encapsulants

Findings of low-temperature polymerization of thermoset adhesives and encapsulants are provided below.

It was expected that VFM would offer a very fast curing method for both thermoplastic and thermoset chemistries and 10X faster is common. The surprise was that cure temperatures near or even below T_g began to be reported by several sources [8] as shown in **Figure 13**. In each case, the measured T_g was the same for the VFM and oven cures and none of the samples had vitrification. The oven cure temperatures shown were recommended by the supplier for complete cures at two hours or less. The VFM cures were 30min or less. In most cases the VFM cure was below the T_g which should not be possible.

A polymer journal article in 2016 [9] demonstrated for the first time that a well-documented epoxy reaction could be completely cured at more than 30°C below T_g with VFM. It was also demonstrated that the VFM mechanism preferentially created chain extension over cross linking before gelation. Apparently, the usually fixed pre-exponential terms (Z for collision frequency and ρ for steric factor) of the collision-modified Arrhenius rate equation (**Eq. 1**) are dramatically increased by entropic rotation of the infinite polymer even after gelation. This would explain a much higher diffusion of reactants and substantially lower complete cure temperatures.

$$k = Z \cdot \rho \cdot e^{-E_a/RT} \quad (\text{Eq. 1})$$

Lower temperature (complete) curing should result in lower stress and warpage in assemblies but does it result in reliability improvements? In publications by IBM [5,6], application data was given that confirmed lower temperature VFM curing of real assemblies with 22% lower warpage and twice the package reliability. TSMC [10] has patented a VFM process to reduce package-on-package (PoP) warpage as well.

Warpage and stress reduction fillers. Thermosets for adhesion and encapsulation/molding include large percentages of silica filler particles (40-90%) that decrease the CTE of the material to more closely match the silicon, substrate, and metal components they attach or enclose. This should reduce stress and warpage in assemblies. Elastomeric additives (5-15%) are also used for the purpose of decreasing the elastic modulus and thereby reducing stress.

To evaluate any interactions between fillers and VFM cure processing, an underfill supplier provided blends with 40, 45, and 60% silica as well as blends with and without elastomeric fillers [8]. The results of curing this matrix of underfills between a large (17mm x 17mm) flip-chip silicon IC (1440 I/O) on a 40mm x 40mm multilayer substrate are shown in **Figure 14**. Warpage of the die surface was measured by optical interferometry (+/-2nm).

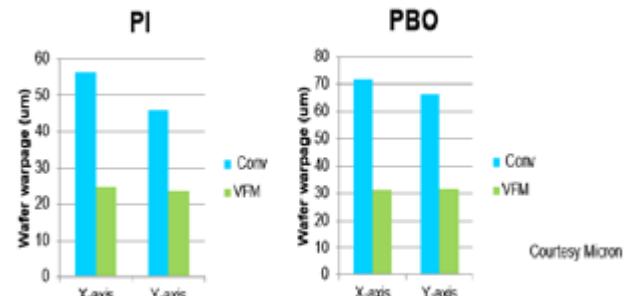


Figure 12: PI and PBO cures at 100°C lower.

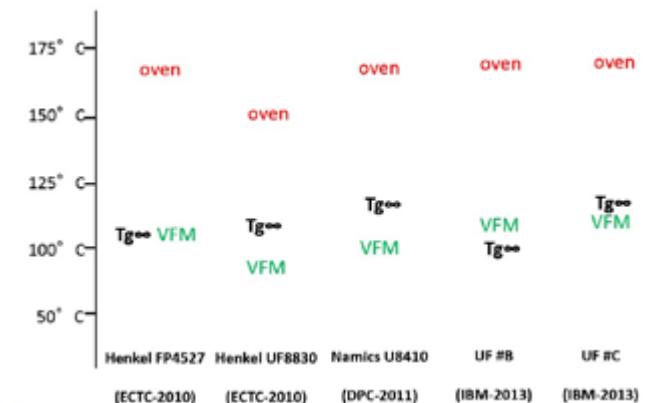


Figure 13: VFM cure vs. oven cure temperatures.

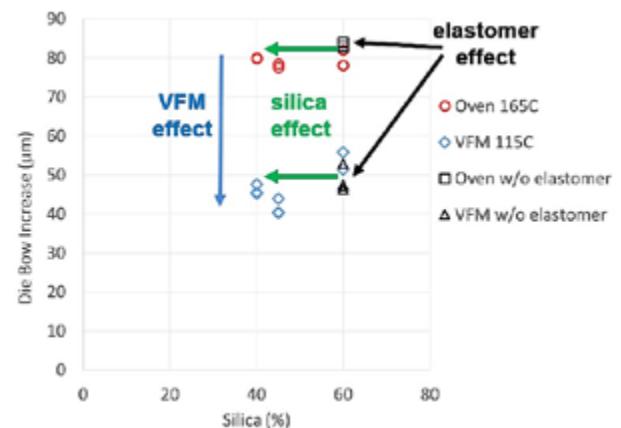


Figure 14: Sources of warpage and stress.

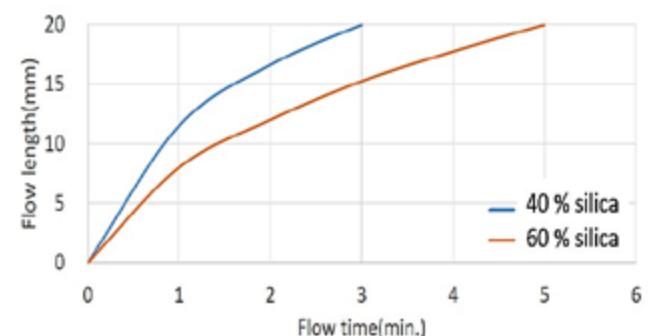


Figure 15: Dispense rate vs. silica filler percentage.

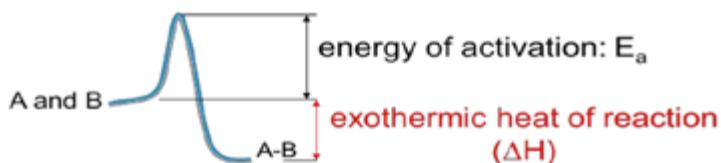


Figure 16: Exothermic reaction profile.

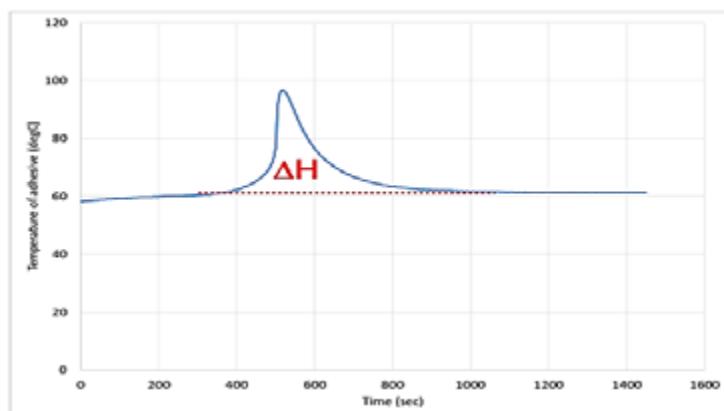


Figure 17: Unintended heating from exotherm.

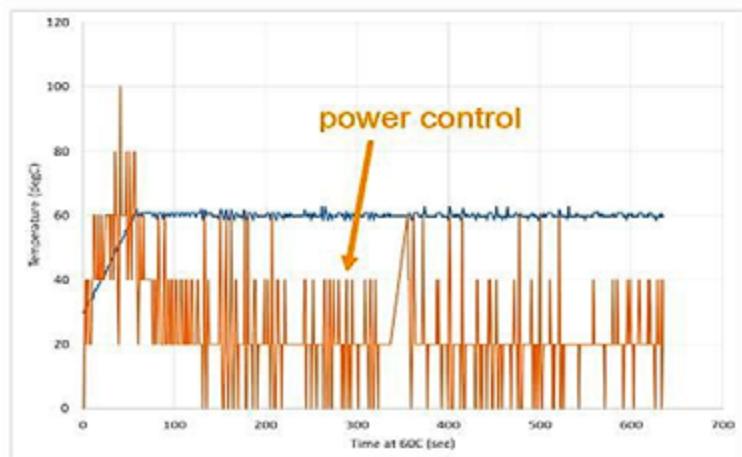


Figure 18: Sample temperature by power control.

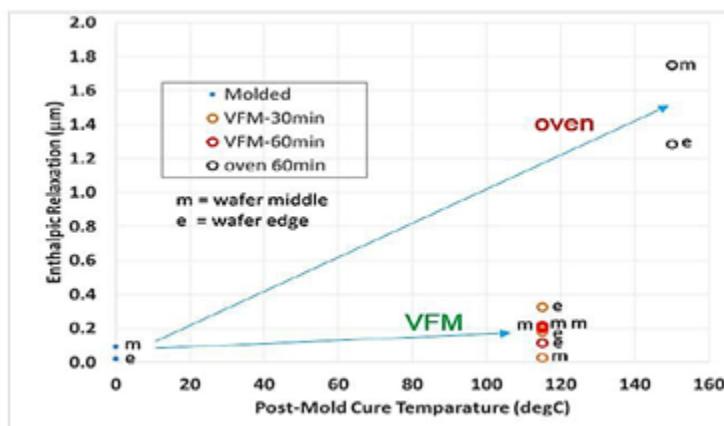


Figure 19: PMC with VFM on a FOWLP wafer.

The oven cures were at 165°C for 1h and the VFM cures were at 115°C for 50min. Both cure methods produced the same complete cure $T_{g\infty}$ of 115°C.

There was no significant warpage change with the addition of elastomer for either cure method. Warpage actually increased by about 8mm with an increase of silica filler from 40% to 60%. The warpage decrease with the lower temperature VFM cure was 35mm (almost half).

The throughput of underfill and encapsulation dispense as well as silica clumping issues are dependent on the amount of silica filler in resins, so it might be more beneficial to use a lower silica filler amount and cure with VFM (**Figure 15**). The use of costly elastomers is also questioned because the warpage is primarily dependent on the method of cure.

Additional benefits of microwave curing

Additional benefits of using microwave curing are discussed below.

Exotherm control. When oven cure temperatures are specified, the assumption is that the sample temperature is the same as the temperature of the air in the oven. In fact, thermosets are usually exothermic reactions (as shown in **Figure 16**) with internally generated enthalpy (ΔH). With a temperature probe in contact with a curing thermoset, the additional enthalpy can be seen in **Figure 17**. In this example, the additional temperature rise to 97°C greatly exceeds the intended cure temperature set at the oven of 60°C. Of course, this results in higher chemical shrinkage stress, CTE mismatch stress, and possibly damage to temperature-sensitive components or materials.

For the same reaction but using VFM, it can be seen in **Figure 18** that the temperature is maintained at the required 60°C by digital control of the applied power with a closed-loop feedback system that monitors the actual temperature of the sample every 0.1s.

Elimination of post-mold cure (FOWLP). Often a thermoset molding compound will have a two-step cure. The first step cures in a mold to around 125°C to limit the chemical shrinkage stress while providing a firm (glassy) substrate for subsequent processing. Then a second post-mold cure (PMC) step finishes the cure around 180°C.

An initial oven mold cure was performed at 125°C (~84% extent of cure) on three 300mm wafers coated with a popular WLP/PLP epoxy resin. One of the wafers was then PMC-cured at 150°C for 60min in an oven. A second (PMC) cure was performed on the second two wafers at only 115°C by VFM for 30min and 60min each. The data is plotted in **Figure 19**. Measurements were taken at the edges (e) of the wafers and at the middle (m) of the wafers.

The enthalpic relaxation “anneal” of the wafers during PMC was measured by modulated TMA. The additional stress of oven PMC is clearly shown compared to practically no stress with VFM PMC. The 30min VFM PMC was adequate for $T_{g\infty}$. The suggestion is that the original mold cure at 115°C with VFM would have resulted in lower total stress with no need for a secondary PMC step.

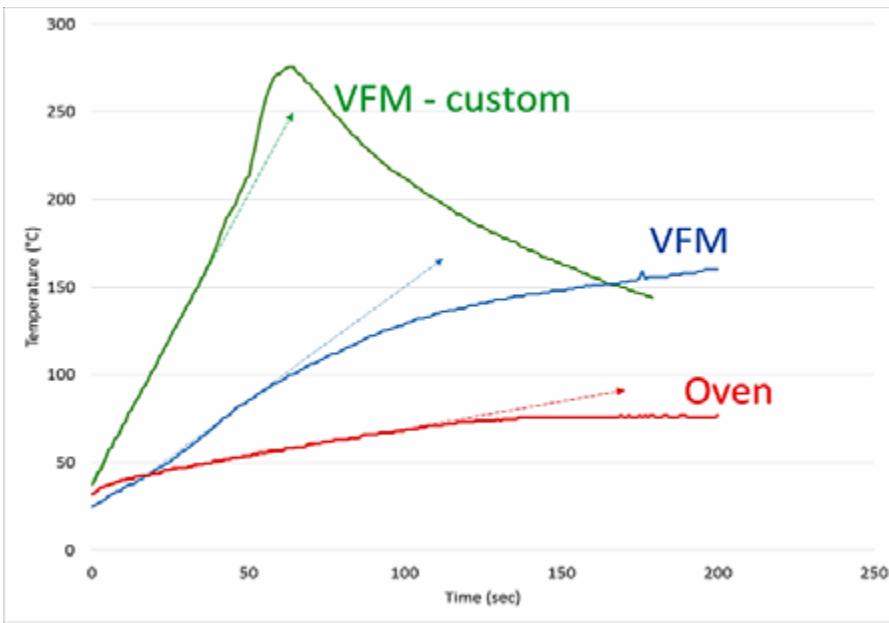


Figure 20: Custom material effects.

Materials customization. The list of thermoplastics, thermosets, and elastomers now being cured by VFM keeps growing, but there have only been a few efforts to better match the chemical structure of reactants to microwave fields. Unlike infrared energy, which has specific functional group sensitivities, microwaves excite organic materials uniformly across the spectrum. In 2006, the VFM cure temperature of a series of PBO films was reduced to 170°C with resin chemical modifications [11]. Recent investigations in this lab have been able to create a statistically predictive model for designing epoxy resins that will triple the reactivity of the commercial blends that have been tested to date. **Figure 20** depicts the two actual reactivities of an epoxy resin cured by oven and by VFM; as well as a “custom” (structurally-modified) resin cured by VFM. This model should be useful for many other types of chemical reactions.

Summary

By making sure that polymer layers in electronic assemblies are completely cured at appropriate temperatures, many

common failure issues like cracking, delamination, chemical attack, poor adhesion, mechanical movements, and instabilities can be avoided. Reduced stresses in joints, layers, and devices can be produced by the lowering of those cure temperatures.

A unique method for reducing cure temperatures, while producing complete cure and maintaining chemical, mechanical and thermal reliability, is the use of variable frequency microwave technology (VFM). This production technology is already available and being used in the microelectronics arena, while improvements in the speed of VFM cure and lowered temperatures have the promise of accelerating reactivities for many polymeric systems.

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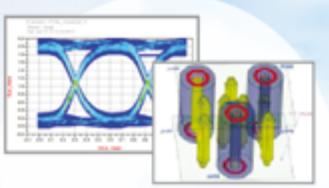
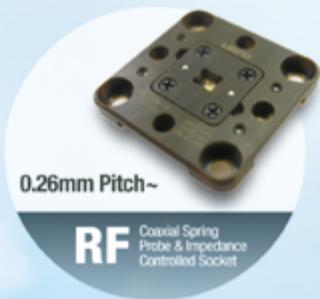
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Biography

Robert L. Hubbard is Director of Technology Development at Lambda Technologies, Inc., NC, USA. He has a doctorate in Organic Chemistry, currently holds ten patents, and has held previous positions of Engineering Manager at Tektronix, Senior MTS at Texas Instruments and Medtronic, and Senior Fellow at Honeywell; email bhubbard@microcure.com

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Packaging of bioimplantable electronics

By P. Markondeya Raj [Florida International University],
Nithin Nedumthakady, Rao Tummala [Georgia Institute of Technology]

B

ioimplantable electronics interface with the human body to extract precise medical data and generate and affect biological functions by providing electrical stimuli. The term “implantable” indicates that the device is intended to be totally or partially introduced, surgically or medically, into the human body and remain there for an extended period. These electronics have numerous applications, including sensing and monitoring of physiological conditions, therapy for chronic diseases and disorders, functioning as artificial organs, and enabling prostheses of limbs to replace lost functions in the body.

Packaging technologies are becoming critical to achieve the next generation in integration, functionality, miniaturization, and long-term reliability and operability of implantable bioelectronic systems. Such systems represent true heterogeneous integration because power, radio frequency (RF), analog and digital functions are integrated in 3D and ultra-miniaturized form factors in hermetic and biocompatible packages with electrode arrays and interfaces that directly interact with the human body. Implantable electronics should seamlessly integrate high-density electronic sub-systems with multi-terminal electrode arrays on flexible substrates with biocompatible materials, while achieving power delivery through efficient power transfer, conversion, and storage. In addition, these systems must operate reliably in aqueous media over an extended time. Several major innovations that combine high-density feedthroughs, integrated magnetic and capacitor components, advanced biocompatible polymer and metal electrodes and interfaces, and embedded or fan-out packaging in flexible substrates aim to create new breakthroughs in this area.

Implantable/bioelectronics

Implantable or bioelectronics comprise three fundamental elements: a) an electronics hub that receives and

processes power and data and sends control signals to b) the electrode array, which transmits the control signals or receives the recorded signals and sends to the signal amplifier in the electronics hub, and c) hermetic and biocompatible cases or layers that protect the system from its environment. A cross section of a generic bioelectronic package is shown in **Figure 1** and described in more detail.

3D electronics hub. Bioelectronics require heterogeneous integration of several functions including: power transfer and conversion, data processing, controller for power delivery to the neural interfaces, and analog-to-digital controllers with signal amplification and conversion. Such systems need to provide sensing, analog, and digital functions to process signal, power, and data telemetry functions from an external unit while maintaining compatibility with the environment and functioning reliably. These requirements need to be achieved within millimeter dimensions. The electronics hub is 3D-integrated in ultra-thin packages with the highest component densities to meet the application needs. This central electronic unit is encased in 3D-integrated, miniaturized, hermetic packages using high-density electrical interconnections in and out of the package without compromising hermeticity and biocompatibility.

The key function of the electronics hub is power and data reception and conversion. The power telemetry subsystem is made up of two parts: the antenna and the rectifier (also referred to as a rectenna). The antenna receives the RF energy that is rectified to DC power and stored within a capacitor or used to charge a battery. To have the greatest

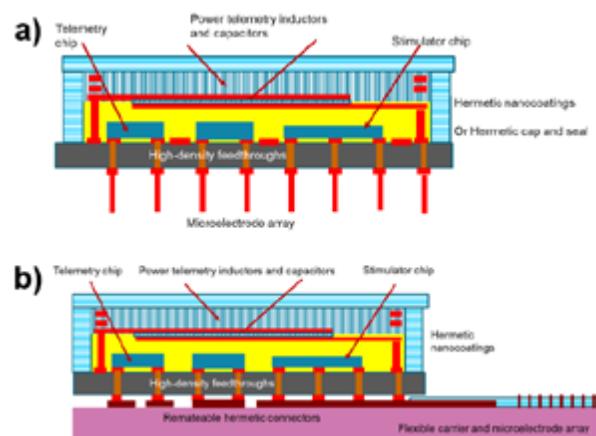


Figure 1: (top) Simplified schematic representation of an emerging 3D bioelectronic package; and b) (bottom) Processing hub integrated with a flexible electrode array.

efficacy, a rectenna must be designed for high-performance energy reception and compatibility with the transmitting antenna. The key requirements are efficient power conversion with new topologies, better designed pulse duty cycle, high-Q components, and integration of actives and passives on a hermetic, flexible system on a package. The efficiency of a rectifier is heavily influenced by the required power density and rectenna array configurations.

Flexible electrode arrays. The hub is hermetically packaged and interfaced with electrode arrays, preferably with removable connections for removal and replacement in a surgical environment. The electrode arrays are made to be chemically inert and reliable in the body. The electronic hub package is directly terminated with high-density electrode arrays that interface with neurons. The electrode system needs to be flexible to conform to the shape of the organs and withstand large stresses. The flex electrode array connector, created using biocompatible dielectrics and electrodes, is used to accomplish this.

Biocompatible and hermetic packaging for long-term reliability. Bioelectronics have high liabilities

from failures, which can directly result in fatalities and expensive surgical interventions. Therefore, implantable bioelectronics systems must be biocompatible and mechanically robust over a long period of time in reactive aqueous conditions. Biocompatible materials prevent unwanted responses, such as oxidative stress, from the body. Package failures occur at the electrode-nerve interfaces, electrode-package interfaces, or at interconnections or connectors, primarily from the diffusion of reactive species. Hermetic packaging is required to prevent diffusion of moisture and ions into the system. Mechanical and material challenges arise from the need for hermetic sealing and encapsulation while preventing significant mechanical stresses. Suitable adhesion layers, diffusion barriers, and biocompatible materials are being developed to address this challenge. Inorganic barriers provide the best diffusion properties but affect mechanical reliability and flexibility of the package and connectors.

Impact of emerging bioelectronics on packaging

Current bioelectronic packaging approaches for neural sensing and stimulation involve packaged devices in large enclosures with leads and connectors that are not scalable to ultra-thin or flexible form factors. With such traditional packaging approaches, bioelectronic interfaces are generally achieved with passive microelectrode arrays that are tethered to a central neural stimulation or recording system package that acts as a hub. A highly-miniaturized fully-implanted high-density electrode array that is actively powered on or close to the electrode array itself with integrated data processing using an embedded data processing chip can enable new applications and opportunities for healthcare. Realization of such systems require miniaturized, heterogeneous integration of several functions including power transfer and conversion, data processing, high-density but biocompatible electrode-tissue interfaces, and miniaturized, hermetic, flexible packages. Emerging bioelectronics seek to achieve this. Five major categories of emerging bioelectronics are described below: a) electronic stents and pacemakers, b) cochlear implants, c) retinal prosthetics, d) neuromuscular stimulators, and e) deep brain recording and stimulation.

Pacemakers and electronic stents. Pacemakers regulate heart rhythm, typically preventing the heart-rate from slowing down to a critical extent. Traditional pacemakers are implanted with a large surgical incision and placed in a pocket under the skin. Leads from the pacemaker reach into the right ventricle of the heart to deliver the required electrical pulses. This distal electronic package consists of ICs for sense amplifiers, controllers, pacing, and power management. Pacemakers are also combined with implantable cardioverter defibrillators (ICDs) that detect irregular conditions such as bradycardia and tachycardia, and step-up conversion circuits to convert the 3V battery to above 500V using voltage converters, transformers and tripler diodes.

Leaded pacemakers create several complexities during surgery. Medtronic has addressed these limitations by creating lead-less pacemakers with a 12-year battery life that are 93% smaller than leaded pacemakers and contain low-power circuits (**Figure 2**). Another



Figure 2: Leadless pacemaker and its implantation (Micra™ Transcatheter Pacing System from Medtronic).

major advance is the incorporation of imperceptible wireless power, wireless pacemaking, and cardiac fibrillation [1,2]. This battery-less and wireless pacemaker has dimensions of ~16 x 4mm and houses a wireless power telemetry link, AC-DC rectifier, power management unit, storage capacitor, CMOS chip, and PMOS switch. For wireless charging without a bulky inductor coil, power is received from microwaves in the GHz range. The frequency of the pacing system is adjusted by either increasing or decreasing power transmitted to the receiving antenna. Electronic stents are coupled with integrated circuits that either sense the status of the artery and monitor in real time for signs of restenosis or occlusion, or mitigate the cellular growth that causes restenosis or

occlusion. These functions are achieved by integrating microelectromechanical systems (MEMS) sensors with wireless communication technologies.

Cochlear implants. Cochlear implants, unlike hearing aids that simply amplify sound, restore impaired hearing by helping to send sound from the ear to the brain. Cochlear implants convert sound into an electrical signal and transmit it to the brain by stimulating the auditory nerve via electrode arrays inserted directly into the cochlea. The implant comprises an external unit housing the microphone, sound processor, transmitter, and an internal unit containing a receiver and stimulator. Power and data are wirelessly transferred between the two units through electromagnetic induction [3]. The signal processing and controller chips and passive components are assembled onto a printed circuit board (PCB), encased in a titanium case, and overmolded with silicone. Multichannel electrodes are bundled and isolated in silicone and inserted into the scala tympani canal. The exposed tips act as multiple stimulation sites and are positioned alongside the basilar membrane at set distances relative to each other. Individual electrodes are mapped to specific frequencies using speech-coding strategies to isolate the incoming audio signal into frequency bands.

Retinal prosthetics. Retinal prosthetics scan and sense incoming light from the surrounding environment, capture image data, and process visual information. The captured image information is encoded as time-varying electric potentials with spatial patterns and delivered to a multi-electrode array. The energized electrodes stimulate the retinal cells and transmit visual information to the cortex. There are two main approaches for stimulating retinal ganglion cells: epiretinal and sub-retinal.

Typical epiretinal visual prosthetics consist of two parts: an external system, which collects visual data, and an internal system consisting of an application specific integrated circuit (ASIC), which converts the visual data into an array of electrical stimulus that can be fed to a microelectrode grid [4]. Using a neural net, the images are transformed into corresponding signals appropriate for electrical stimulation of the retinal ganglion cells. These signals are transmitted to an implanted receiver unit by inductive telemetry. The unit's integrated circuitry decodes the signals and transfers the decoded data to a stimulation circuitry that selects stimulation electrodes

to generate current pulses, evoking action potentials in retinal ganglion cells and causing a visual sensation. This approach is illustrated in **Figure 3**. Critical performance metrics of these implants include: a) high resolution of the images; b) long-term reliability and life span of the implants (typically greater than 10 years); and c) low input power to prevent tissue damage.

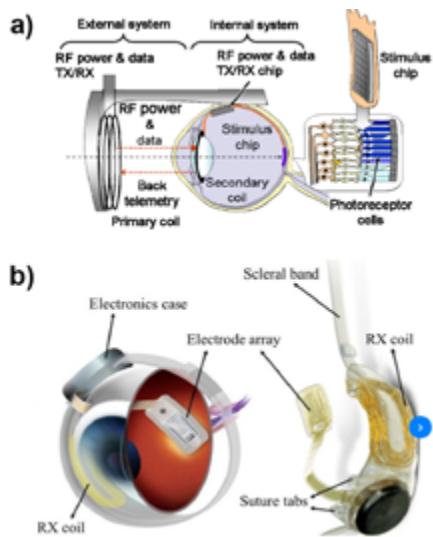


Figure 3: a) Schematic of a retinal prosthesis system [5], and b) its package integration implementation with epiretinal approach in Argus® II retina prosthesis by Second Sight Medical Products, Inc.

The implanted receiver consists of a telemetry inductor receiving coil, a hermetic package electronics case that houses the amplifier, analog-to-digital converters, stimulator and controller circuits, and a flexible electrode array that interfaces with the retinal cells (**Figure 3**). Hermetic packages are realized with chips assembled onto a ceramic substrate with hermetic feedthroughs and encased with a titanium or ceramic cap brazed to the substrate. The electrode count is limited by the pitch of the feedthroughs in a hermetic substrate that are generated with ceramic thick-film co-firing technologies. This has constrained the number of electrodes and created several challenges in delivering stimulus patterns to the retina through the microelectrode array. Initial systems comprised a 16-electrode array. When tested in humans, subjects could sense light, darkness, motion, and recognize large objects. Further resolution is achieved with 60 electrodes spaced less than $200\mu\text{m}$ apart. Thousand-array electrode systems are being developed as packaging technologies continue to advance.

In the sub-retinal approach, the degenerated photoreceptors are replaced with a stimulation electrode array that is inserted in between the sclera and the retinal nerve cells. As opposed to epiretinal implants, the sub-retinal implants can also use an implanted micro-photodiode array instead of an external video camera. The external system consists of a power unit and a transmitter for power and external instructions. The internal system has a chip comprising a micro-photodiode array, which can be mounted in the sub-retinal cavity to replace damaged photo-receptor cells. Negative pressure within the sub-retinal cavity simplifies surgical placement and structural integrity of these chips. The micro-photodiode array needs to have more than $40,000$ electrodes/ mm^2 resulting in the distance between two electrode arrays being less than $5\mu\text{m}$ [6]. The chip also has a signal conditioning circuit that processes the signal from the diodes to deliver conditioned and amplified electrical pulses. These pulses are then fed to the signal processing cells of the undamaged retina. A schematic package for the sub-retinal implant is shown in **Figure 4**.

Neuromuscular stimulator. Neuromuscular stimulators generate functional electrical stimulation to induce

precisely controlled muscle contractions that produce specific movements required by the patient (**Figure 5**) [7]. Additional functions of neuromuscular stimulators include pain management and elimination of atrophy in paralyzed limbs. The system also provides sensing and stimulation through bidirectional telemetry when powered and controlled by an external transmission coil. The system with self-contained electrodes is located at the site where stimulation or sensing is required and powered with an external magnetic field through inductive coupling from the external transmitter coil. The telemetry link also communicates data by RF carrier modulation. In one package implementation, the analog and digital control chips are assembled onto a ceramic circuit board and sealed in a glass capsule. Pt/Ir and tantalum capacitor electrode feedthroughs from the glass capsule provide the required current pulses. The tantalum electrodes are anodized to store adequate charge at high voltage and directly interface with tissue to provide stimulation pulses.

Brain neural recording and stimulation. Brain neural recording and stimulation systems are used to restore functions, provide therapy, or decode parameters associated with electromyography (EMG)

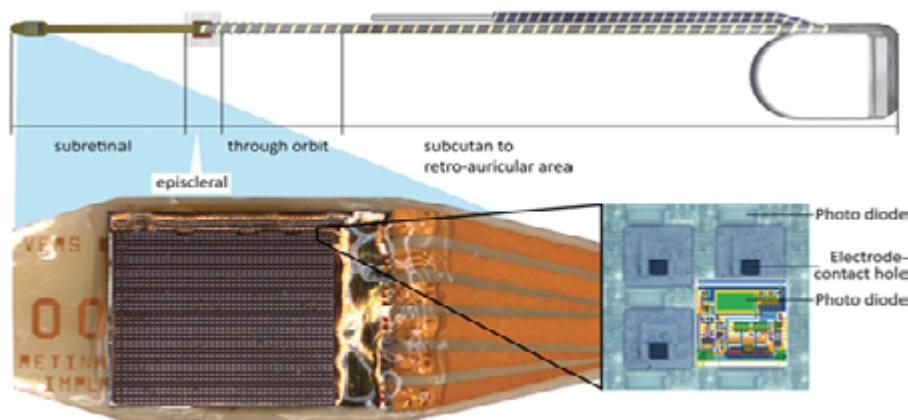


Figure 4: Internal system of flexible sub-retinal implants (Alpha IMS Implant from Retina Implant AG) [6].

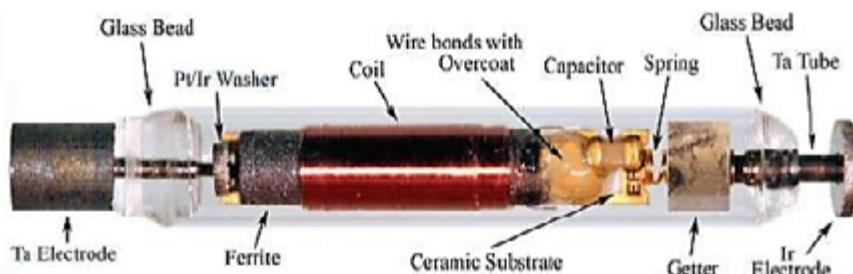


Figure 5: Components and integration in a neuromuscular stimulation implant [8].

and kinematics. Deep brain stimulation (DBS) regulates brain neural activity through an implanted device that stimulates specific, precise targets within the brain, via electrodes. DBS is primarily used to alleviate or heal diseases and associated symptoms that affect motor activity like Parkinson's disease (PD), dystonia, or essential tremors. DBS is shown to improve the basic quality of life, prolong healthy life, reduce the need for medications related to motor functions, and minimize side effects.

Electrode arrays are implanted through the skull via small holes interconnected to a pulse stimulator, which is typically located in the chest area. The wires reach from the top of the skull and down the neck. A major drive for future miniaturization is to integrate the neurostimulator chip directly within the electrode array, eliminating the separate neurostimulator and long interconnections to the electrode array and minimizing mechanical damage and failures in DBS devices that typically occur within the subcutaneous wire and the connectors.

Powell et al., has developed an ultra-miniaturized, 3D neural recording system, comprising high-density electrode arrays through glass [9]. A schematic package representation and its implementation are shown in **Figure 6**. The ASIC chips are flip-chip assembled onto the top and the package is sealed with a glass cap using low-temperature glass-to-glass sealing. The telemetry inductor and other components are integrated onto the top of this 3D package. The electrode array comprises micromachined silicon probes that are protected with parylene-C coating, while only the exposed tips are coated with Pt. The system is implanted in the subdural space for long-term recording with wide bandwidth and high reliability.

Summary

Emerging healthcare initiatives and massive investments are driving major paradigm changes in packaging of

bioelectronic implants, transforming them from traditional 2D packages with rigid enclosures to high-density 3D packages. Implantable bioelectronics should meet more dense packaging and high-reliability criteria than conventional electronics. They represent true heterogeneous system integration because power, RF, analog and digital functions are integrated in 3D and ultra-miniaturized form factors in hermetic and biocompatible packages with electrode arrays and interfaces that directly interact with the nerves. In addition, bioelectronic implants should seamlessly integrate high-density electronic subsystems with multi-terminal electrode arrays on flexible substrates with biocompatible materials. Power delivery through efficient power transfer, conversion and storage is another key barrier for these applications. Several major innovations that combine high-density feedthroughs, integrated magnetic and capacitor components, advanced biocompatible polymer and metal electrodes and interfaces, and embedded or fan-out packaging in flexible substrates will create new breakthroughs in this area.

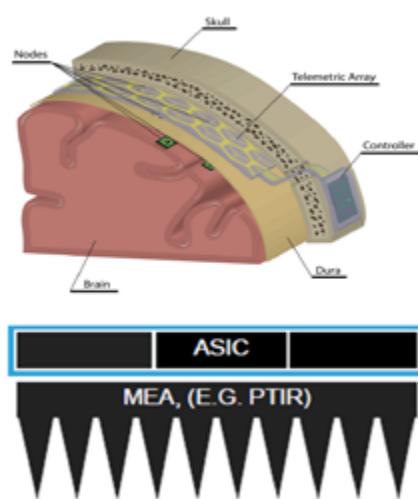


Figure 6: Schematic 3D glass package for electromagnetic transparency and hermeticity with low-cost sealing in a sub-dural interrogation node [10].

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Testing of high-frequency 5G applications and why simulations are critical to success

By Jeff Sherry [Johnstech International]

The pervasive drive towards ubiquitous connectivity, high content/fast data links, and Internet of Things (IoT) hyper-growth prompts the 5G air interface standard to quickly supersede 4G. The rapid adoption of the 5G standard poses a dilemma for the supporting ecosystem, particularly in providing the required infrastructure and allied devices to launch the overall functioning system. Faster time to market means accurate and timely device test models and simulations to avoid costly iterations upon product release. The 5G frequency bands per 3GPP Rel 15 consists of two spectral clusters namely FR1 (Frequency Range 1) from 450-6000MHz, and FR2 (Frequency Range 2) ranging from 24-53GHz. More than 10X the incumbent 4G/LTE data rates are achieved on account of much wider bandwidths (100MHz for FR1, 400MHz for FR2) than 4G's bandwidth of 20MHz.

This paper demonstrates examples of electrical modeling to support customers working in 5G frequency ranges and shares why the data is so important to make sure the full test system implementation is successful. Data that compares simulations that only include measured dielectric constant and loss tangent or dissipation factor for one frequency, to results that use measured material performance over the full bandwidth will demonstrate how having the correct material properties can lead to more accurate simulations. This leads to expected measured results causing fewer redesigns, and therefore a shorter time to market. In some examples, simulated results will be compared to third-party measurement data.

Simulations are critical to development success in high-frequency 5G applications. Carefully executed, modeled simulations will closely match actual results, which avoids the added costs and guess work in high-frequency product development. This paper will do the following:

- Produce examples of measured versus modeled data in those introduced 5G frequency bands; and
- Outline the effects of metal and non-metal material properties on testing results.
- Outline the modeled effects of S-parameter convergence to get simulations to closely represent measured results.

Introduction to 5G simulations

5G applications will move to much higher frequencies to support the immense amount of data. In the semiconductor industry, higher frequencies translate to smaller wavelengths, which means that smaller contacts and shorter path lengths will be standard to support 5G applications.

In any discussion of testing, it is important to recognize that both the assumptions and inputs into the model need to be correct. The more accurate the inputs to any simulation, the more accurate the results of the simulation. However, if the inputs are too simplified, there is danger that the answer will be inaccurate and not predictive of the real-world application.

Material properties are a big factor in the system performance and many non-metal materials sometimes vary greatly over frequency. In addition, the material's properties may change over temperature, humidity, or other test conditions making it more difficult to predict accurately measured real-world results. To further complicate things, many material suppliers test their materials at really low frequencies that are well outside the 5G frequency bands. Most material specification sheets have the dielectric constant and dissipation factor or loss tangent specified at 10MHz,

which meets the requirements of the method used to call out the testing of the material. Many materials properties are less reliable the higher the frequency range, and for 5G applications could yield results that deviate significantly from what is modeled resulting in costly redesigns and the building of more prototypes to test, causing delays for the system to get to market.

Figure 1 shows the third-party measured versus modeled results of Johnstech's 0.5mm pitch ROL®100A. In the figure, one can see measured return loss as compared to an equivalent circuit of contact and modeled data of the contactor, which includes a 50 ohm board and device pad. Notice that the HFSS modeled data with board and device matches the 50 ohm measured results closely at 20GHz. In this model, housing materials were tested to 20GHz. In testing alternative materials, we found that material properties can sometimes cause results to vary by more than 30% at elevated frequencies. At very high frequencies, the best data model to use is the transmission line model vs. lumped elements that were used to develop the equivalent circuit to match measured results. As viewed in **Figure 1**, the

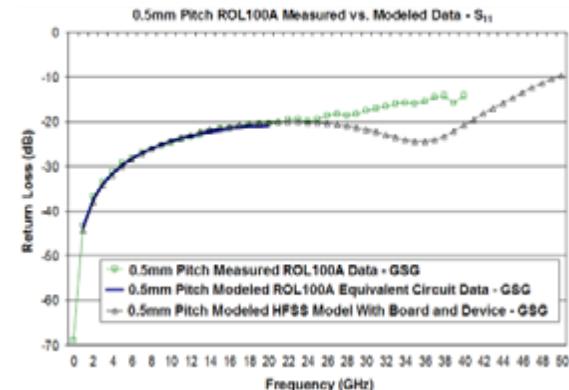


Figure 1: Third-party measured vs. modeled results of Johnstech's 0.5mm pitch ROL®100A measured return loss compared to an equivalent circuit of contact.

lumped element equivalent model used an optimizing routine to match magnitude and phase of the measured data for both the ground-signal-ground (GSG) and ground-signal-signal-ground (GSSG) configurations to enhance the accuracy of the model.

Figure 2 shows measured versus modeled results of Johnstech's ROL®100A contact for insertion loss. The graph compares results of equivalent circuit of contact and modeled data of the contactor, which includes a 50 ohm board and device pad with third-party

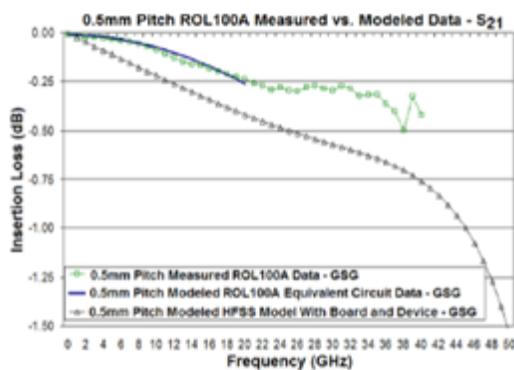


Figure 2: Measured vs. modeled results of Johnstech's ROL®100A contact for insertion loss.

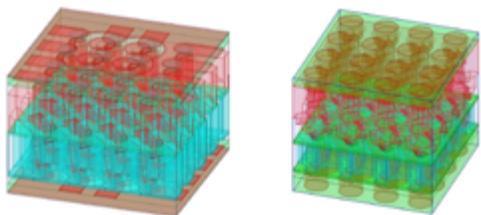


Figure 3: BGA simulation models with a) (left) contactor interfaces vs. b) (right) with probes.

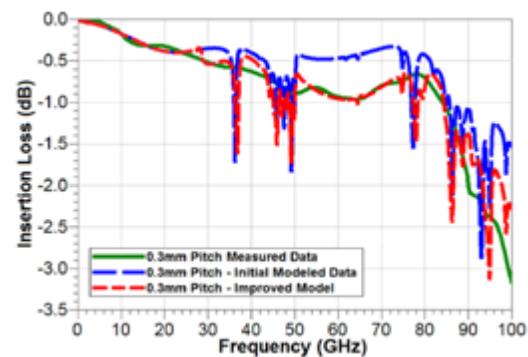


Figure 4: Insertion loss plot comparing measured results for a 0.3mm pitch test contractor solution from an independent third party (solid green line) compared to modeled results with materials properties tested to 22GHz (blue large dashed line).

measured data. In this figure, the modeled insertion loss includes a portion of the load board interface pad and device pad, so the length of the model is longer for the HFSS simulation, which results in a longer transmission line in the model, and therefore, more insertion loss. As shown in the figure, as the frequency increases, more insertion loss occurs. Measured data was only acquired to 40GHz. Third-party test houses can measure electrical parameters to 100GHz or above, so a -1dB bandwidth could now be measured beyond 40GHz. Because the equivalent circuit is a comparison to the measured data, it is never as accurate as the measured data, so if both are available it is always better to use actual measured data.

Figure 3 shows two different HFSS models for an on-center ball grid array (BGA) solution. **Figure 3a** is a model that includes the load board interfaces and board pads designed to be a 50 ohm interface to the test contactor. It also includes the package balls with their diameter and protrusion, and a 50 ohm trace to the output port that is de-embedded so just the ball performance is added to the simulated results. Most models are designed with generally nominal ball sizes, which is usually 60% of the device pitch. To get the most accurate results, a 4x4 array of balls is simulated so the model can be used to provide data on devices with edge, corner and field radio frequency (RF) signals, and to accommodate designs with different locations of ground or return signals. The pitch of BGA models has a big impact on electrical performance. As pitch decreases, the contacts get closer together, creating higher mutual capacitances and inductances. Also, as the pitch is reduced, the ground or return path also gets shorter, sometimes increasing the bandwidth that the contactor can support. Above 80GHz for a design with a larger than 0.5mm pitch and contacts with a length over 2.0mm, it is very hard to design a broadband

system without an amount of electrical degradation. The model (**Figure 3a**) also includes two right angle interfaces (at board and device interfaces), which degrade performance from the modeled results shown in **Figure 3b** where probes are in-line with the signal flow.

Figure 3b is an HFSS model with 50 ohm high-frequency probes that touch the contactor at both the load board interface and at the package interface. The probes are setup to be 50 ohms and de-embedded so just the contactor performance is obtained just like the third-party test house measures the contactor. The S-parameter set can be treated like a black box and used in customer simulations because there are literally thousands of potential board materials and thicknesses and different devices with different ball sizes and protrusions.

Figure 4 shows an insertion loss plot comparing measured results for a 0.3mm pitch test contactor solution from an independent third party (solid green line) compared to modeled results with material properties tested to 22GHz (blue large dashed line) and 80GHz (red short dashed line). In the 22GHz model, above 22GHz the materials in the model were assumed to be constant; and with the 80GHz model, the material properties were assumed to be constant above 80GHz.

Because of the frequency range of simulation to 100GHz, the number of ports needed to be solved (32 ports for 16 contacts in a 4x4 array) and the number of curved surfaces, the S-parameter convergence was set to 0.025 and solved on a large system. The red traces with 80GHz frequency dependent material, in general, have the same form as the measured data with some fluctuations. The fluctuations (**Figure 5**) were shown to be the results of the model not being solved to a tight S-parameter convergence. When the convergence limit was reduced by more than 3X, the fluctuations were reduced, resulting in modeled data correlating with measured results very well.

Figure 4 shows that the modeled results predict measured results when the S-parameter convergence is reduced — by more than 3X in this case — and the correct material properties are used in the model over frequency. However, this 3X improvement in model accuracy or S-parameter convergence has a cost of increasing the model run time by 4X. Above 90GHz, the modeled results show

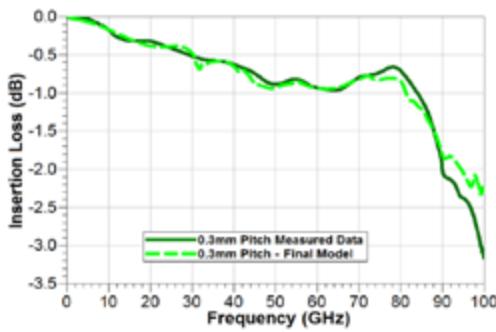


Figure 5: 0.3mm pitch BGA measured insertion loss vs. modeled results with corrected material properties and accurate S-parameter convergence.

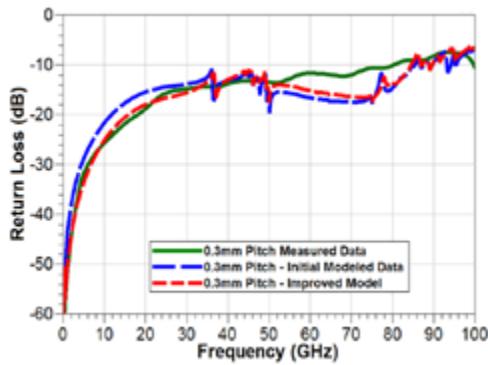


Figure 6: Return loss modeled data.

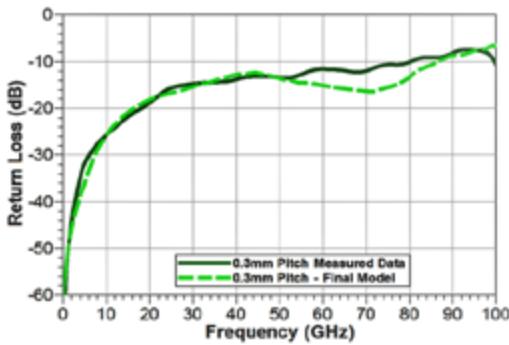


Figure 7: 0.3mm pitch BGA measured return loss vs. modeled results with corrected material properties and accurate S-parameter convergence.

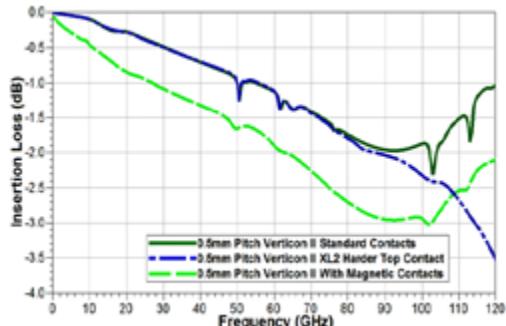


Figure 8: Contact materials — magnetic vs. non-magnetic materials.

less loss, which could mean further material testing needs to be done above 80GHz. Other potential differences could be mechanical tolerances because at very high frequencies, a 1 micron difference between the actual housing feature and the model could change enough to cause this error because the wavelength is small at higher frequencies.

In comparing **Figure 4** to **Figure 5** you can see that using improved material properties helps the model correspond closer to the measured results. And in **Figure 5** you can see how decreasing the S-parameter convergence eliminates some of the variances in data and tends to result in modeled data mimicking the measured results. The return loss modeled data, shown in **Figure 6**, tracks measured results extremely well to 50GHz and above 80GHz. The discrepancy in the 50-80GHz band could be due to probes used in the model not being exactly 50 Ohms.

Other potential differences that could result in modeled data varying from the measured results arise from mechanical tolerances on account of the fact that at very high frequencies, a 1 micron difference between the actual housing feature and the model could result in a fairly large change in return loss because the wavelength is small. In addition, the tolerance in the housing slot that holds the contact and allows the contact to move, could impact the return loss. For rigid one-piece contacts this change is minimal, but for other contacts using multiple parts, this effect needs to be simulated.

Figure 7 shows simulated Return Loss results of contactor for a BGA device comparing measured results (dark green) with HFSS simulated results (light green) with measured material properties to 80GHz and solved with tighter S-parameter convergence.

A contact with magnetic properties greatly affects the

performance. Magnetic contacts have significantly more insertion loss than standard contacts across the whole frequency band. As shown in **Figure 8**, a magnetic contact has a -1dB insertion loss of 26GHz, where other non-magnetic contacts with the same profile have close to 50GHz for a -1dB insertion loss. Harder XL-2 material has a very similar performance to standard gold-plated contacts up to 90GHz, but offers more resistance to wear due to it being a harder material. In all simulated results the board and device interfaces are the same and the contact profiles are all identical. Adding a plating, such as gold, to a magnetic material can make a contact with a magnetic core look like the standard contact. As more plating is added, the contact can be simulated to be entirely out of plating if the plating is more than 4 times the skin depth with minimal error. Below is the formula for skin depth. As the frequency of operation increases, the skin depth decreases. Skin depth defines where the current density is just 37% of the current density at the surface. A layer 4 times the skin depth means 98% of the current will flow in that layer. At a high enough frequency, a gold-plated contact with enough plating will operate electrically as a solid gold contact.

Eq. 1: Electrical performance for plated contacts depends on

$$\text{Skin Depth} = \delta = \sqrt{2/\omega\mu\sigma}$$

Where $\omega = 2\pi f$; $\sigma = 1/\rho$;

$$\mu = \mu_0 * \mu_r; \mu_0 = 4\pi \times 10^{-7} \text{ (H/m)}$$

Where f = frequency

Where σ = conductivity;

ρ = resistivity; μ = permeability

Summary

The most important thing that can be taken from this paper is the more accurate the model is both mechanically and with respect to the material properties, the closer the simulation should be compared to actual measured data. At times it can be very hard to get accurate material properties over temperature because suppliers typically provide the minimal amount to satisfy material requirements testing. As a result, the materials need to be tested at the frequencies they are intended to be used. Many material data sheets don't contain data as to how much the material properties vary vs. frequency

because that might inhibit sales, and in some cases, be very expensive to obtain.

From a mechanical perspective, it is best to draw up any contactor model from quality measurements to get accurate performance. If multiple similar parts are being made, it might make more sense to model lower and upper tolerances in addition to nominal so the variation in performance can be determined prior to testing.

For metal materials, plating properties are very important at high frequencies because the contacts will act more and more like the plated material at higher frequencies. In addition, the more plating that is applied compared to skin depth, the more the contact will act like the plated material as opposed to the core material. Current carrying capacity however, is a function of conductivity of both the plated and core materials. A magnetic material has properties that tend to degrade its electrical performance over frequency, so even low frequency values on a specification sheet might lead to big simulation errors if magnetic materials are used. The amount of plating thickness can determine electrical performance. If one applies enough gold plating on a contact, that contact can be simulated as a solid gold contact for practical purposes and ease of simulation.

Modeling how a contactor is built reduces modeling risks and increases accuracy when trying to predict measured results. Reducing the convergence limit on S-parameters does improve accuracy of the modeled data, but does cost in terms of solve time for the model. Although material properties, plating, S-parameter convergence, and magnetism were discussed in this paper, modeled results are also affected by the configuration of the device and can vary greatly depending on pitch, number and location of grounds, device impedance, and load board properties and thickness.



Biography

Jeff Sherry is Principal RF/HSD R&D Engineer at Johnstech International in Minneapolis, MN. The holder of 18 engineering patents and several more pending, Jeff has been an integral member of the Johnstech team for over 18 years. He holds a Master's in Electrical Engineering from the U. of Minnesota and has been working in MMW applications for over 30 years. Email jsherry@Johnstech.com



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Enabling high-density chip-to-chip connections with a new FOWLP approach

This work has been presented at the 2018 International Wafer-Level Packaging Conference (IW LPC) conference.

By Arnita Podpod, Eric Beyne [imec]

Today, many electronic systems still consist of a multitude of components that are packaged individually after wafer dicing, and are interconnected using conventional printed circuit boards. However, for more “demanding” applications, advanced 3D integration and interconnect technologies have emerged through the years – which have largely reduced the size of the electronic systems, and have enabled faster and shorter connections between their sub-circuits. One of these technologies is wafer-level packaging (WLP), where multiple dies are packaged while they are still on the wafer. Because the entire wafer is now packaged at once, this solution is more cost-effective than the traditional packaging approaches. In addition, the resulting packaged chips are smaller and thinner in size, which is an important consideration in footprint-sensitive devices, such as smartphones. In today’s smartphones, an average of five to seven wafer-level packages can already be found, and the numbers continue to increase.

Fan-in and fan-out

There are two main types of wafer-level packages: fan-in and fan-out. They differ in the way the redistribution layer (RDL) is incorporated in the package. RDLs, usually organic layers, are used to re-route the dies’ connections (I/Os) to the desired (bump) location on top of the die surface. With fan-in, the redistribution layer traces are routed inwards, creating a very small package (roughly corresponding to the size of the die itself). But the redistribution process can also be used to expand the available area of the package,

by spreading or “fanning out” the contacts beyond the dimensions of the chip. In general, this fan-out WLP (FOWLP) technology provides a larger I/O count than fan-in WLP technology.

In mobile applications, FOWLPs are gradually replacing the more traditional package-on-package (PoP) memory-on-logic solutions. These PoPs are much thicker than fan-out concepts and suffer from limited interconnect bandwidth and density, and from limited pitch scaling (a few 100 μm). In these applications, FOWLP is preferred over other available high-bandwidth 3D technologies as well, such as 3D stacking (in which hot spots in the logic die may affect the memory retention) or 2.5 stacking (where the longer interconnects generate a higher interconnect power and additional cost).

Two basic fan-out process flows

Various FOWLP approaches have been developed and established over the past years to answer the increasing need for high data rates and wide I/O count, and to answer the demand for increased function integration on the package. All these approaches start from one of the two basic fan-out process flows: the mold-first or the RDL-first flow.

Following the mold-first approach, dies are first assembled on a temporary carrier, followed by wafer overmolding.

The function of the epoxy molds is to protect the individual components and hold them all together. In a final stage, the RDL is created and connections are made. Following the RDL-first approach, die assembly and wafer overmolding is performed after the creation of the RDL.

Each of these approaches comes with its own set of drawbacks. In the mold-first approach, for example, the dies usually shift during or after overmolding, and this makes it very challenging to achieve interconnect pitches below 100 μm . With the RDL-first approach, the achievable density is limited by the line and space resolution enabled by the (organic) RDL.

Flip-chip on FOWLP

To answer the need for higher-density, higher-bandwidth chip-to-chip connections, the imec team has developed a FOWLP approach on 300mm wafers, referred to as flip-chip on FOWLP (Figure 1). This new concept basically uses a mold-first approach, but the dies are now overmolded after the formation of the chip-to-chip interconnections. This way, contrary to the standard mold-first approach, chips are already interconnected before being shifted during the overmolding process. The advantages of this approach (e.g., lower die shift) will be explained below, along with the challenges.

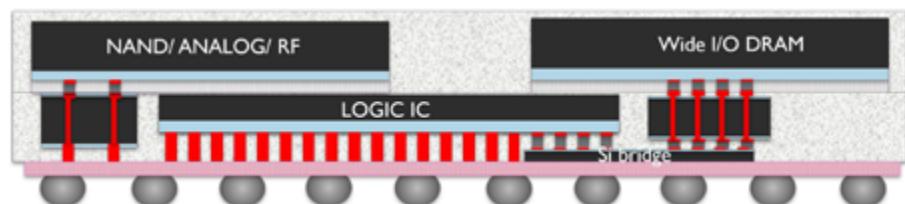


Figure 1: Concept of the flip-chip on fan-out wafer-level package.

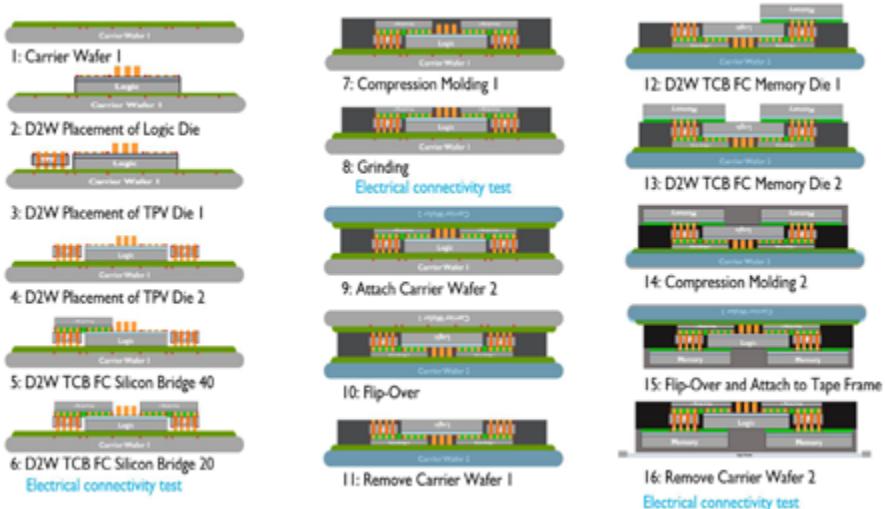


Figure 2: Flip-chip on FOWLP: assembly process flow.

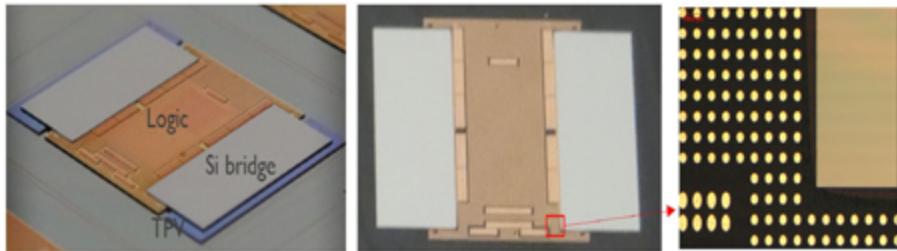


Figure 3: Pictures illustrating steps 5 to 8: a) (left) after die placement and bridge bonding; b) (middle) after molding and back grinding, and c) (right) exposed Cu pillars on the package surface.

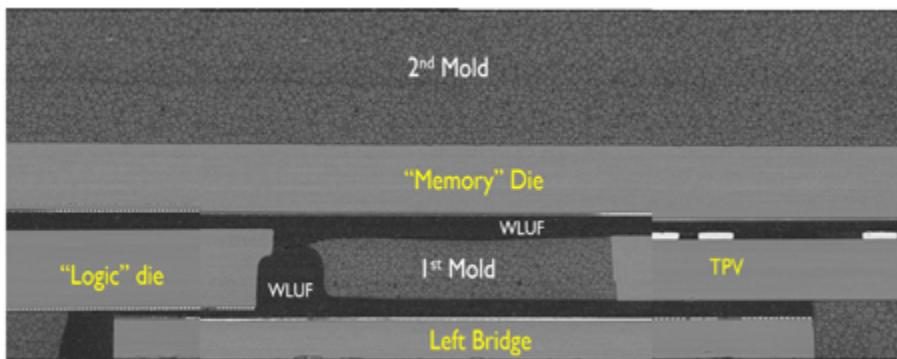


Figure 4: A cross section after flip-chip on a FOWLP package assembly and final, second wafer-level molding.

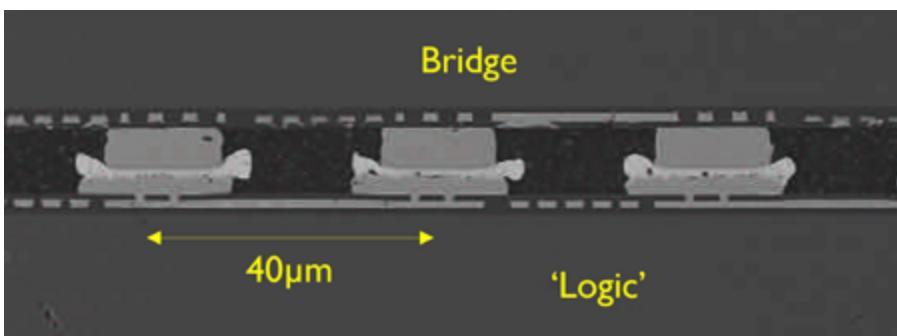


Figure 5: Illustration of the successful bridge-to-logic bonding at 40µm pitch, compatible with a 20µm pitch microbump assembly.

Key components: TPVs and Si bridges

In this work, a test vehicle was used to demonstrate the feasibility of the new fan-out concept. The test vehicle is composed of seven individual chip components: wide I/O dynamic random access memory (DRAM), Flash memory, logic, two through-package vias (TPVs) and two Si bridges. The test vehicle is used to obtain practical learnings. Therefore, the logic and memory dies are not fully functional: they are “mimic” dies, used to test the electrical continuity between the bump connections.

The interconnecting Si bridges and the TPV chips are key components to realize the high-density connections. TPV chips are Si dies with through-Si vias (TSVs) and bumps of 40µm pitch. The Si bridges have bumps of 40µm and 20µm pitch. These components form a bridge between the functional dies (e.g., the logic and memory dies), enabling ultrahigh chip-to-chip interconnect densities with 20µm bump pitch.

Another key differentiator with respect to standard mold-first approaches is the tight alignment step. During this critical assembly step, the individual dies are placed with high precision on a flat temporary bonding Si wafer.

A closer look at the process flow

In the first step of the assembly process flow (Figure 2), the TPV and logic dies are placed on a carrier wafer with a temporary bonding layer on top. Next, the Si bridge (with 40µm and 20µm bump pitches) is attached using a thermocompression bonding (TCB) step (Figure 3). In this process step, bumps with 40µm pitch are attached to the TPV side, and to the left side of the logic die. The 20µm pitch bumps are attached to the right side of the logic die. In the next step, the wafer is overmolded by a liquid mold compound. Tests revealed a complete filling, even of the area under the bridge. Afterwards, the Cu pillars are exposed through grinding – to connect with the RDL later on. After flipping the thinned wafer to a second carrier and removal of the first carrier, the memory dies are assembled using flip-chip technology. A second wafer-level molding and

removal of the second carrier complete the process flow (**Figure 4**). In between process steps, continuity tests are performed to verify the electrical paths. The result is a complete package of only 300-400 μm thickness (excluding the solder balls).

Major challenges and solutions

The process flow came with its own set of challenges that needed to be overcome to ensure fully functional package solutions with ultrahigh chip-to-chip interconnect density. One of

the concerns was the possible tilting of the dies during the assembly process flow, especially for the long and narrow TSVs and Si bridges. Tilting of these dies might break the interconnections between the sub-components. To assess whether and when tilting takes place, the imec team applied different forces for placing the TPVs. The team observed that, even for the largest placement force, tilting was limited to below 5 μm – sufficiently low to maintain the connections.

Next, the alignment between the logic and through-package dies has received considerable attention, and can be considered a key differentiator of the FOWLP approach (**Figure 5**). The logic and through-package dies should be placed very close to each other, and a precise alignment step is needed to enable the subsequent 40 μm and 20 μm bump pitch stacking of the Si bridge. For example, to achieve the required 20 μm bump pitch, a misalignment of max +/-3 μm between the logic and through-package dies can be tolerated. To reach this exceptionally small misalignment, the team incorporated alignment marks into the carrier and die designs. Logic dies were first aligned to the carrier. Next, through-package dies were placed, aligned to the carrier and to the logic dies. Finally, a high accuracy placement and stacking TCB tool was used to attach the Si bridge.

During the subsequent molding process, the dies can still shift – thereby damaging or breaking the bump connections between TPV and bridge, or between logic and bridge. The imec team therefore performed dedicated electrical tests, before and after the molding. The tests revealed that the molding process did not affect the integrity of the connections. Based on these results, it can be assumed that, if the dies shift upon molding, they do this in the same direction, as a whole, without breaking the connections.

Summary

With this approach, the imec team demonstrated a record high chip-to-chip interconnect density with 20 μm bump pitch in a fan-out context. In the near future, the technology will be further improved, and the electrical and RF behaviors will be evaluated in different configurations.

The presented technology is especially attractive for mobile applications, as it enables a cost-effective wide I/O memory-to-logic interconnect in a very small form factor. Ultimately, flip-chip on FOWLP may also become an enabling technology for heterogeneous integration, targeting high-performance applications. It can provide a way to incorporate multiple dies – including high-performance compute, memory and optical communication blocks – in an electrical highly interconnected package.



Biographies

Arnita Podpod graduated with a Master's degree in Materials Science and Engineering, and with a Bachelor's degree in Applied Physics from U. of the Philippines. After graduation, she started at NXP Semiconductors as a Project (Materials) and Process Engineer, and progressed to being a Senior Package Development Engineer with Fairchild Semiconductor Phils. Arnita joined imec (Leuven, Belgium) in 2013 as a Senior R&D Engineer and is currently responsible for both flip-chip on FOWLP projects, and pre-assembly module integration within the imec 3D program.

Eric Beyne obtained a degree in Electrical Engineering in 1983 and a PhD in Applied Sciences in 1990, both from the Katholieke U. Leuven, Belgium. Since 1986 he has been with imec in Leuven, Belgium, where he has worked on advanced packaging and interconnect technologies. Currently, he is imec Fellow and Program Director of imec's 3D System Integration program. He received the European Semi Award 2016 for contributions to the development of 3D technologies.

TECHNOLOGY TRENDS



Automotive IC production wafer test in a zero-defect world

By Amy Leong [[FormFactor, Inc.](#)]

Chip Scale Review asked FormFactor's Chief Marketing Officer, Amy Leong, to respond to questions that provide insights into the challenges associated with automotive IC production wafer testing amid the requirement for zero-defects.

CSR: What are the unique production wafer test requirements for automotive ICs?

FormFactor (FFI): Semiconductor technology is key to smarter and safer cars and, ultimately, to enabling autonomous driving. According to semiconductor industry market research firm, IC Insights, the automotive IC is one of the fastest growing applications at 14% CAGR (2016-2021), and projected to reach \$43 billion by 2021. We are seeing the soaring proliferation of radar, LiDAR and image sensors to help cars "see" better; RF/mmWave chips to enable vehicle to vehicle (V2V) and vehicle to infrastructure (V2I) communications; and microcontrollers to help vehicles make more intelligent decisions in order to support an increasing level of autonomy.

These innovations in automotive semiconductor ICs post a high bar for wafer test. Due to its inherent safety requirements, automotive IC test is becoming more difficult and more time-consuming. Defect levels for automotive ICs are at least 10X more stringent than those for mobile and consumer applications, demanding parts per billion (ppb) failure rates and mandating zero-defect manufacturing. In addition, the test conditions are more extreme, such as cold temperature (-40°C) and hot temperature (>=160°C), high power (10,000V) and high current (600A) requirements. Supply chains are also getting more complex as automotive IC chipmakers globalize their production footprint. Supplier scale and sustainability now become more crucial than ever.

CSR: What is the significance of supplier scale and sustainability as it pertains to automotive ICs, and how do those attributes directly affect your solutions in this area?

FFI: Unlike mobile phones, which we often change every two to three years, a car is expected to work for more than 10 to 15 years. Once an automotive IC is designed in a car model, the entire supply chain needs to be prepared to support the chip for a very long time. In addition, an automotive IC maker can have a network of wafer fabrication and test sites across the globe. Our customers expect suppliers to provide local support wherever they test the wafer, for as long as the chip is being used in the car. Therefore, scale and sustainability are essential for a supplier to automotive IC makers.

A sustainable supply chain starts with trust. We have established 10 design centers and 22 service centers worldwide, with our latest addition being in France. For an automotive IC maker, FormFactor's support team is stationed across US, Europe and Asia, where probe card designers are close to customer chip designers to minimize design cycle-time, and service engineers are rapidly on hand to maximize uptime. We enable customer success through our technology, partnership, "First Time Right" product quality, and global customer support.

CSR: How can productivity improvements be achieved while maintaining zero defects?

FFI: Testing of automotive ICs is becoming more complex and time-consuming. The key challenge for wafer test suppliers is how to provide good enough test coverage to meet the high quality requirement for

automotive ICs, without driving up the cost of test. The biggest bang for the buck to reduce test cost is to test as many dies in parallel as possible to dramatically increase productivity.

As an example (excluding test program impacts on the actual throughput), to test a 300mm wafer with 1000 dies, if we test 10 dies at a time with a test time of 1 minute per wafer touchdown, it will take 100 minutes to complete testing of the wafer. If we can test 100 dies at a time, the total test time would be reduced by a factor of 10 to 10 minutes. At a test cell hourly rate of \$60 per hour, a reduction of test time by 90 minutes would lead to a \$90 test cost saving per wafer. At a chip design running at 20K wafer starts per month (WSPM), this would translate to an annual savings of over \$20 million—a remarkable profitability enhancement for automotive IC makers. This parallel test concept is certainly not new. It has been widely utilized for DRAM wafer test for more than two decades, and now we have extended this capability to automotive ICs, with parallelism in the range of 3000 DUTs.

Wafer probing is a "contact sport." The more force the probe puts on the wafer test pad, the greater the chance to create defects to the circuitries underneath the pad. To support a zero-defect manufacturing process, probe cards must be designed with the gentlest force possible to eliminate any chance for under-pad cracking, while maintaining a high enough force to ensure stable electrical contact and optimal test yield.

CSR: What are the design features of the TrueScale Matrix 300mm MEMS probe card that accomplish the goals referenced above?

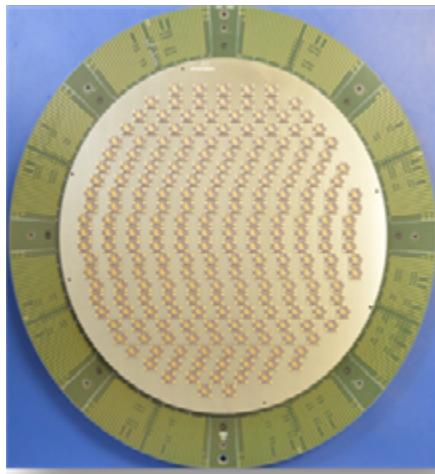


Figure 1: FormFactor TrueScale Matrix 300mm full-wafer probe card with “rainbow” touchdown pattern to maximize test throughput.

FFI: Our solution enables test cost reduction by maximizing test throughput and a zero-defect probing process by using ultra-low force MEMS probe

technology that we pioneered. A few capabilities include:

1. Maximize probing area to cover the entire 300mm wafer: This provides opportunities to test as many dies as the tester channel allows, without any area limitation. In contrast, many alternative probe cards have a limited probing area of 100mm to 150mm.
2. A proprietary touchdown optimization tool to create inventive patterns to maximize throughput: As you can see in **Figure 1**, the “rainbow” pattern typically provides lower touchdowns compared to a rectangular probe card’s “solid wall” pattern. Simply put, a circular probing pattern is more efficient for a round wafer.
3. FormFactor’s proprietary TRE™ (Test Resource Enhancement) technology provides a boost to

wafer test throughput: The TRE option can intelligently split a single tester resource to test multiple dies, without compromising test quality.

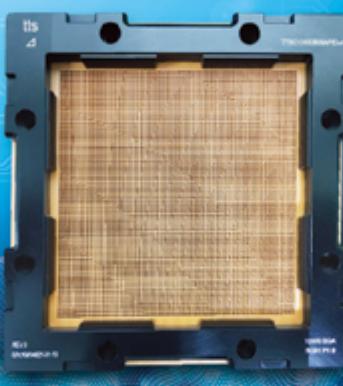
4. Ultra-low force design to support zero-defect manufacturing: The probe is designed with ultra-low force—less than 2 grams probe force per probe—to ensure that the active circuitry below the probing pad is undisturbed after multiple probing insertions at the same pad location.

The test cost reduction example shown in **Figure 2** is an automotive microcontroller (MCU) production case using TrueScale Matrix. The microcontroller is the brain for smart cars that makes rapid intelligent decisions. It is equipped with high embedded memory content, which exponentially drives up the test time



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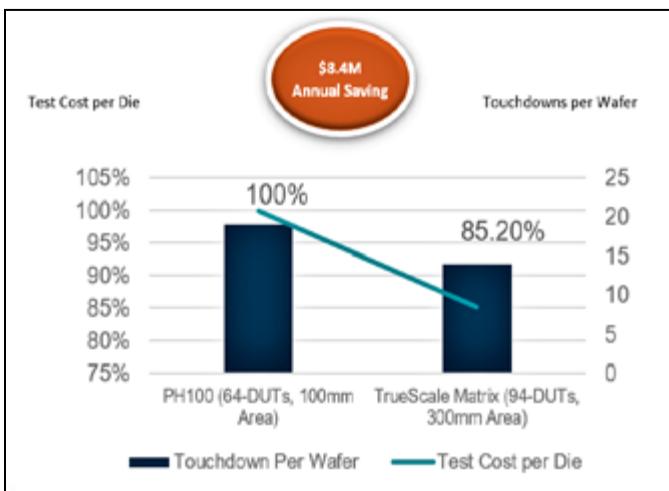


Figure 2: Automotive microcontroller wafer test cost reduction through parallel test.

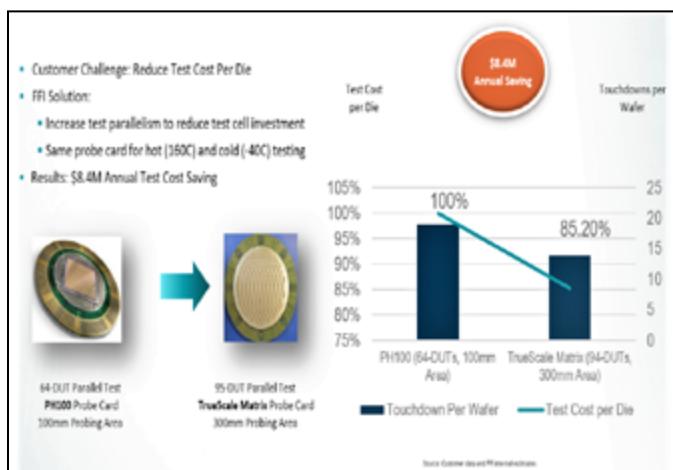


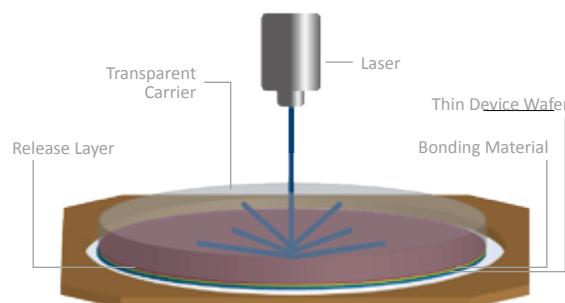
Figure 3: Case study: automotive microcontroller production test productivity improvement through high-parallelism probe card.

and test cost compared to other digital ICs. To reduce test cost, the customer in this example used TrueScale Matrix to increase throughput from 64 devices under test (DUTs) per touchdown to 95 DUTs, as well as optimized test patterns to further reduce touchdowns per wafer. As a result, the test cost per die was reduced by 15%, and led to an annual savings of \$8 million ([Figure 3](#)).

CSR: What technical challenges did FFI overcome to enable 300mm full-wafer test for automotive ICs?

FFI: As we increased the probing area to 300mm for automotive IC wafer test, a couple of new challenges emerged:

1. Control of the probe tip planarity within 30 microns to ensure stable electrical contact for every DUT:
With 20,000 to 100,000 probes per probe card—even at an ultra-low force of 2 grams per probe—several hundreds of kilograms of force are exerted over a 300mm probing area.



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2. Thermal expansion control over a wide temperature range:

One unique test requirement for automotive ICs is that they need to be tested at both cold (-40°C) and hot (>=160°C) temperatures. A silicon wafer has an average coefficient of thermal expansion (CTE) of 2.8 ppm/°C. When testing at 160°C, a silicon wafer will expand approximately 125 microns across its diameter. Therefore, the pads located at the perimeter of the wafer will shift outward by approximately 60 microns, relative to the center of the wafer. In order to probe these pads, the probe card must match the 125-micron expansion. Otherwise, the probe mark will fall outside the probe pad, which is typically 50 microns in size.

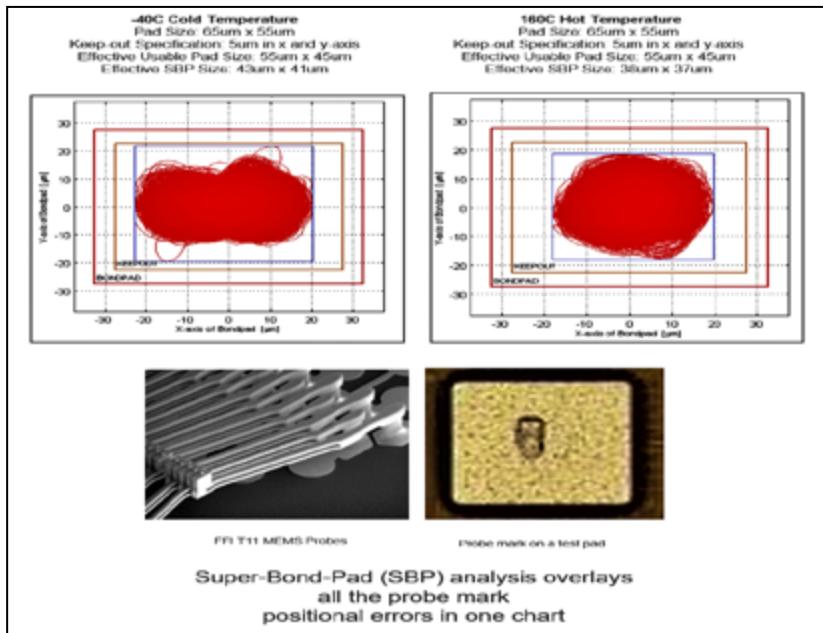


Figure 4: Super-bond-pad (SBP) analysis for an automotive microcontroller at cold (-40°C) and hot (160°C) test temperatures.

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TrueScale Matrix has a DUTlet architecture (i.e., tiny ceramic blocks with MEMS probes) to address critical thermal mechanical challenges. This architecture assembles a bunch of DUTlets into a wafer-side-stiffener (WSS). A variety of different WSS materials with different CTEs can be selected to match the specific thermal test conditions of each customer. This allows the probe tip to dynamically follow the probe pad as the wafer expands or contracts with temperature changes, achieving consistent probe to pad alignment (PTPA). In contrast, competitive architectures are limited to one specific CTE of the ceramic material alone—that is, one CTE for all applications.

To maintain all the probe tips at the same planar level within 30 microns, TrueScale also incorporates a tester-side-stiffener (TSS), which provides the stiffness required to counter the large system deflection as the probes touch on the wafer.

CSR: Explain the significance of the super-bond-pad (SBP) analysis.

FFI: FormFactor uses an SBP measurement to verify that the probe mark falls inside the probe pad. After probing the entire wafer at hot temperatures, we measure the bounding box of each probe mark on every probe pad on the wafer, then superimpose all the measurements onto a “Super Pad.” This procedure is then repeated for cold temperatures. This approach provides a holistic view of the probe mark performance across the entire wafer over the full temperature range. As you can see in **Figure 4**, using the same probe card design, at both cold -40°C and hot 160°C, all the probe marks fall within the pad with good margin to the edge.

Biography

Amy Leong has been with FormFactor since 2012 and is CMO at the company. Prior to this, Ms. Leong was the VP of Marketing at MicroProbe—from 2010 through the 2012 closing of FormFactor’s acquisition of MicroProbe. Before joining MicroProbe, Ms. Leong worked at Gartner, Inc. (2008–2010) as a Research Director covering the ASSP system-on-chip and microcontroller markets. From 2003 to 2008, Ms. Leong worked at FormFactor where

she served as Senior Director of Corporate Strategic Marketing and Director of DRAM Product Marketing. Prior to FormFactor, Ms. Leong worked in a variety of semiconductor process engineering and product marketing roles at KLA-Tencor and IBM. Ms. Leong holds an MS in Material Science and Engineering from Stanford U. and a BS in Chemical Engineering from the U. of California, Berkeley. Email aleong@formfactor.com

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INDUSTRY NEWS



69th IEEE EPS ECTC

The IEEE EPS 69th Electronic Components and Technology Conference (ECTC) will be held from May 28-31, 2019 at The Cosmopolitan of Las Vegas, Las Vegas, NV. The conference will start on Tuesday, May 28th, with morning and afternoon professional development courses. Special sessions will feature invited panelists to discuss some of the most exciting topics and trends in our industry including: Transient Electronics: A Green Revolution for Packaging; Photonics on the Cutting-Edge of Technology Evolution; and Sensor Packaging for Autonomous Driving. The EPS President's Panel on "Future Visions of Electronics Packaging," hosted by IEEE EPS President Avi Bar-Cohen and Prof. Karlheinz Bock, explores the future of packaging science and technology and proposes possible scenarios for 2025. Visions of future packaging technologies will be presented and discussed with invited experts in the field of electronics packaging. The authors of the best selected submissions of the EPS packaging technology vision conquest will also join the discussion panel. The involvement of our young professionals will bring fresh perspectives and new ways of thinking. The intention of this panel is to identify significant future packaging technologies in order to best serve IEEE and the electronics community. The Thursday night IEEE EPS seminar will feature experts to outline and discuss the "Roadmap of IC Packaging materials to Meet Next-Generation Smartphone Performance Requirements."

This year's luncheon keynote speaker will be Prof. John A. Rogers, Director of the Center for Bio-Integrated Electronics at Northwestern University on the topic of

"Soft Electronic and Microfluidic Systems for the Skin." He will describe how recent advances in materials, mechanics, and manufacturing have established



the foundations for classes of high-performance electronics and other microsystems technologies that have physical properties precisely matched to those of the human epidermis. The resulting devices can integrate with the skin in a physically imperceptible fashion to provide continuous, clinical-quality information on physiological status. This talk will summarize the key ideas and presents specific examples in wireless monitoring for neonatal intensive care, and in capture, storage, and biomarker analysis of sweat.

The conference will feature 36 oral sessions, four interactive presentation sessions and a student poster session. Topics of the oral sessions include: Wafer-

Level Fan-Out Process Integration, RDL and Additive Manufacturing, Advancements in Automotive and Power Devices, Emerging Flexible Hybrid Electronics, Technologies Enabling 3D and Heterogeneous Integration, High-Bandwidth 3D and Photonic Integration, MEMS, Sensors, IoT, 5G, mm-Wave & Antenna-in-Package, RF & Power Components and Modules, and Advanced Biosensors and Bioelectronics. Also planned are student and young professional receptions, and an ECTC/ITherm Women's Panel and Reception focused on, "Unleashing the Power of Diversity in our Workforce." All the latest details about the 69th ECTC, conference and hotel reservations can be found at www.ectc.net.



The poster for TestConX China 2019 in Shanghai features a background image of the Shanghai skyline at dusk. At the top left is the ECTC logo, followed by the text "TestConX 中国" and "China". Below this is the "PREMIER SPONSOR" logo for "tts" with the tagline "innovate collaborate deliver". To the right, there is promotional text: "Experience new regional and international presentations at the event that connects electronic test professionals to solutions. Limited EXPO spaces and sponsorships are available." A QR code is located in the bottom right corner. In the bottom right corner, a purple circle contains the text "CALL FOR PRESENTATIONS Visit the website testconxchina.org for details". The main title "SHANGHAI 2019 上海" is prominently displayed in large orange letters, with "专业电子测试解决方案" (Professional Electronic Test Solutions) in smaller blue text below it. The tagline "CONNECTING ELECTRONIC TEST PROFESSIONALS TO SOLUTIONS" is at the bottom.

ECTC

The 2019 IEEE 69th Electronic Components and Technology Conference

May 28 - May 31, 2019

The Cosmopolitan of Las Vegas
Las Vegas, Nevada, USA

Don't Miss Out on the
Industry's Premier Event!

The only event that
encompasses the
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Automotive Electronics
Harsh Environment
Bio/Medical Devices
Thermal/Mech Simulation
Interconnect Reliability
Optical Interconnects

HIGHLIGHTS

- 41 technical sessions including:
 - 5 interactive presentation sessions, including one featuring student presenters
- 18 CEU-approved Professional Development Courses
- Technology Corner Exhibits, featuring more than 100 industry-leading vendors
- 6 special invited sessions
- Several evening receptions
- 3 conference luncheons
- Multiple opportunities for networking
- Great location

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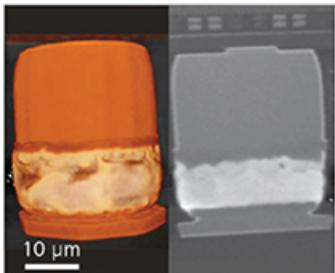
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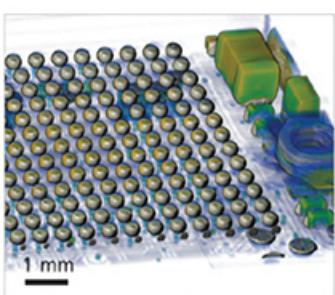
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DRAM interconnect within a 10 mm x 7 mm x 1 mm package containing 4-die stack, 0.8 $\mu\text{m}/\text{voxel}$, showing solder extrusions; imaged by Xradia 620 Versa.



3D image (left); virtual cross section (right) of 25 μm diameter Cu-pillar microbump.



3D microCT scan of smartwatch showing SMT components and BGA bump array, 2.85 $\mu\text{m}/\text{voxel}$.

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