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Volume 22, Number 5

The Future of Semiconductor Packaging

September • October 2018

High-resolution 3D X-ray microscopy

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- Embedded RDL
- Effective, scalable EMI protection
- The clouded view of W CSP inspection strategies
- Surviving the three phases of HDAP design
- Metrology and inspection needs of next-generation processes

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The ZEISS Xradia 520 Versa X-ray microscope (XRM) provides non-destructive package-level failure analysis and 3D volumetric and linear measurements on packaging structures with submicron resolution. The photo, taken inside the XRM chamber, shows a loaded sample being prepared for measurement just after placement by the robotic arm. The XRM system collects 2D projection images from the rotating sample, which is positioned between an X-ray source and detector, and then uses proprietary software to reconstruct 3D volume data that may be visualized and analyzed. Scintillator-coupled microscope objectives enable it to maintain resolution regardless of package size.

Cover image courtesy of Zeiss

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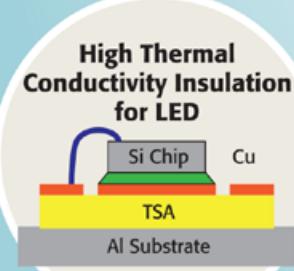
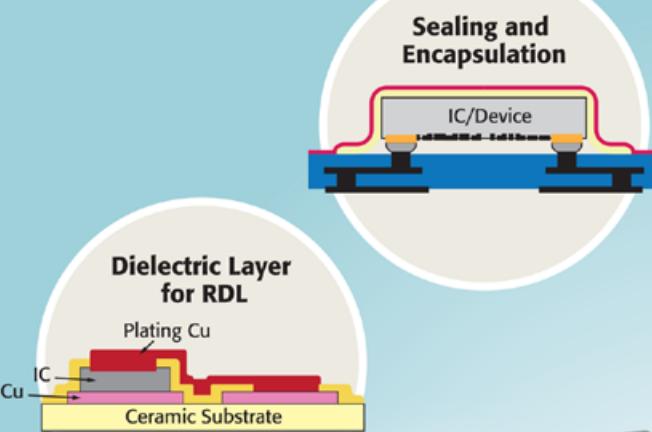
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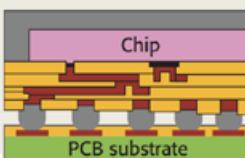


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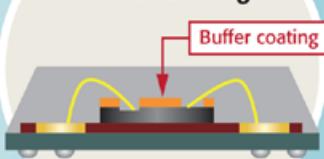
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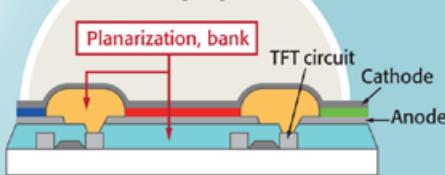
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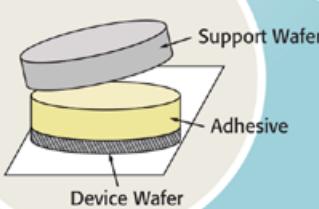
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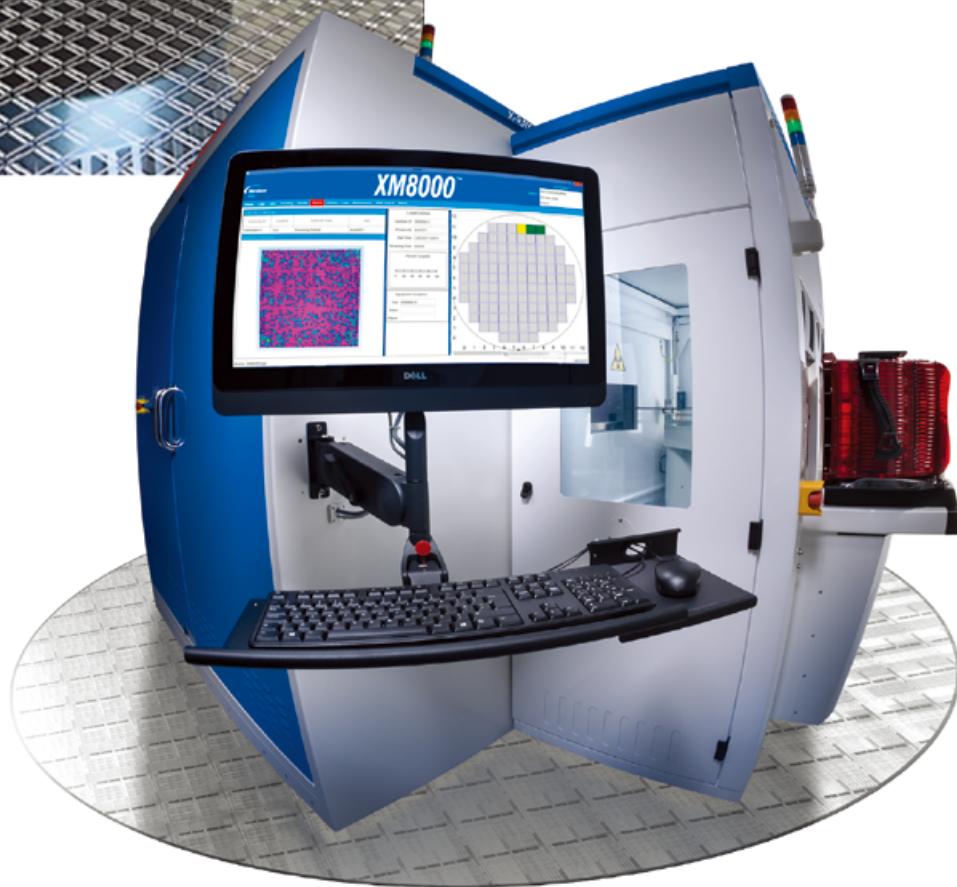
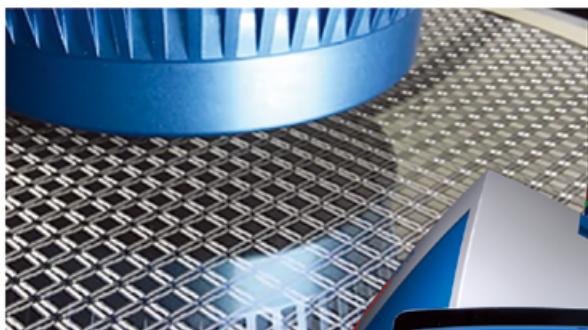
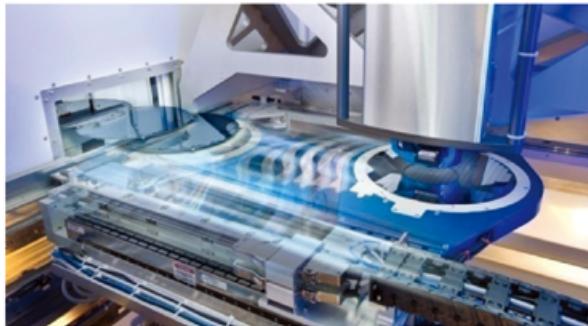
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TECHNOLOGY TRENDS



Meeting the metrology and inspection needs of next-generation advanced packaging processes

By Timothy Kryman *[Rudolph Technologies, Inc.]*

Advanced packaging (AP) technologies have imported many processes from front-end wafer fabrication to the back end of the manufacturing process. Controlling these processes in the back end requires similar approaches to inspection and measurement. Like the front end, shrinking feature sizes are driving requirements for improvements in accuracy, precision, sensitivity and throughput. But AP processes also present measurement and inspection challenges that are unique to back-end applications, such as bump metrology and nonvisual defects. These unique needs, coupled with the greater diversity and rapid evolution of AP processes, are creating demand for flexible measurement and inspection systems that can be used to control a variety of parameters, such as both two-dimensional (2D) and three-dimensional (3D) geometries, and can be adapted to new requirements as they arise. Combining these capabilities in a single platform permits the most efficient and effective use of capital. Keeping pace with the industry roadmap will require innovative solutions from

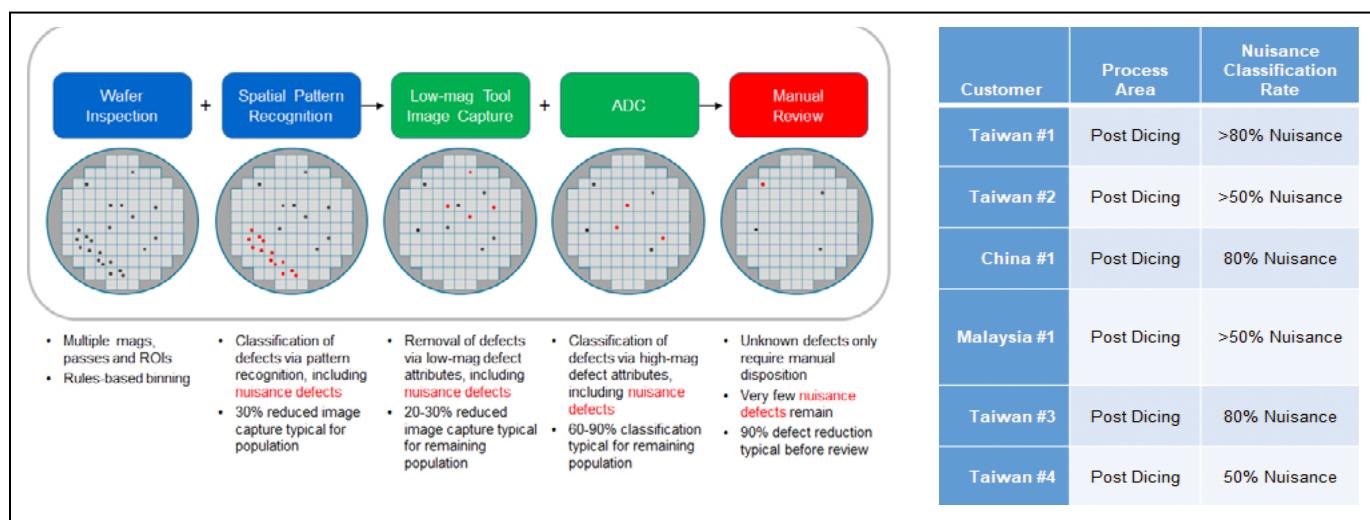
equipment suppliers that are focused on the specific needs of AP processes.

Manufacturers are also facing increasing market pressure to improve quality and reliability. This is especially true of market segments like automotive, where consumer safety is a significant consideration. Current-generation automobiles already contain thousands of semiconductor components, and with the prospect of fully autonomous vehicles, that number may grow by orders of magnitude. A component failure rate of one in a million equates to a vehicle failure rate of 1 in 100 for a vehicle with 10,000 components—a rate that is not acceptable. Meeting this challenge in current and next-generation packages requires defect sensitivity down to the micrometer level and the ability to distinguish killer defects quickly and reliably within enormous streams of raw data. Statistical tools like gauge repeatability and reproducibility (R&R) studies and sophisticated software capabilities like spatial pattern recognition will become increasingly important. More data alone is not enough—engineers need systems that can turn raw data into actionable process information.

Improving throughput, sensitivity, accuracy and precision

Throughput, sensitivity, accuracy and precision are fundamental performance characteristics for any inspection and measurement system. Throughput ultimately determines the cost of ownership. Sensitivity determines the smallest defect that can be reliably detected. Accuracy and precision determine how tightly the process can be controlled. All are becoming more challenging to improve as package feature sizes continue to shrink.

Conventional imaging systems that use 2D area-scan sensors impose unavoidable trade-offs among resolution, sensitivity and speed. Rudolph's latest-generation system (Dragonfly™ G2) incorporates an advanced imaging sensor and optical design that circumvent these limitations to provide both significantly faster imaging and sensitivity to defects as small as 1µm. The optical system is specifically designed to accommodate larger package sizes. Streamlined image processing routines provide the analytical speed required to keep pace with the accelerated data flow. Stage speed and accuracy have also been increased to meet the requirements of the



Customer	Process Area	Nuisance Classification Rate
Taiwan #1	Post Dicing	>80% Nuisance
Taiwan #2	Post Dicing	>50% Nuisance
China #1	Post Dicing	80% Nuisance
Malaysia #1	Post Dicing	>50% Nuisance
Taiwan #3	Post Dicing	80% Nuisance
Taiwan #4	Post Dicing	50% Nuisance

Figure 1: The table on the right shows a representative sampling of the percentage of nuisance defects detected in various applications at user facilities. All are greater than 50%, one is greater than 80%. The graphic on the right illustrates the data analysis process that automatically classifies 90% or more of defects, including most nuisance defects, before any manual operator review.

new imaging scheme. Initial customer evaluations have reported throughput increases of 50% and more.

Nonvisual and nuisance defects

Advanced packaging processes face unique inspection challenges, including nuisance defects and nonvisual defects. Nuisance defects are false positives that can occur in large numbers, overwhelming detection systems and consuming significant resources to review and reject. They are caused by the variable grain patterns of metal conductors that appear to the inspection algorithm as deviations from the standard. These same grain patterns can hide true defects. Another class of defects, known as nonvisual, are caused by residues of the organic materials used to insulate conductors and planarize the surface. These materials tend to be transparent under conventional illumination and yield little signal in bright field and dark field inspection. They can be especially troublesome when they occur on contacts, such as bumps and pillars.

The impact of nuisance defects can be greatly reduced through an effective application of optical principles and sophisticated defect review software. Clearfind™ Technology suppresses the variable contrast patterns generated by metal grains, thereby reducing the nuisance defects these patterns can cause and providing improved sensitivity to structural defects in conductive lines and pads. Reducing the number of nuisance defects in the initial data stream also reduces the load on subsequent review software. This automated process proceeds stepwise through classification with spatial pattern recognition, removal based on low-magnification attributes, and automatic defect classification (ADC) using high magnification attributes (**Figure 1**). Typically, the automated review software can classify 90% or more of the defect population, including nuisance defects, without manual review.

The technology also addresses the issue of nonvisual defects by generating a strong, high color-contrast signal from organic materials. This distinctive signal makes residues of organic materials on metals and other inorganic materials, or traces of metals on organic surfaces, easy to detect (**Figure 2**). In some AP processes, such as post-lithography inspection, the technique can be used exclusively,

with no need for conventional bright field and dark field passes.

2D/3D bump metrology

Many AP processes use vertical integration schemes that require interlayer connections as small and reliable as the multilayer interconnect technologies used within the chip. Most of these vertical connections involve the creation of a conductive “bump” protruding through an insulating layer to carry the signal to the next layer above or below. Controlling the bumping process requires a combination of 2D and 3D inspection and measurement techniques that is unique to AP applications. Total bump process control requires 2D defect detection of voids and shorts, foreign material, and misprocessing; 2D measurement of bump diameter, bump position, bump presence; and 3D measurement of bump height and coplanarity. Bumps are already trending to smaller dimensions as low as 10µm diameters and 5µm heights. As a result, repeatability and resolution requirements are going beyond the capability of conventional white light techniques and now require laser-based technologies. Inspection systems are also challenged by the increasing number of bumps, with total bump counts already exceeding 80 million per wafer.

Achieving consistent bump height and coplanarity is critical to ensuring reliable connections. A bump that is not high enough will not connect, while one that is too tall may prevent connection by neighboring bumps. Even the slightest bump height variations can cause weak connections and lead to costly failures in the field. Bump height measurement has become more challenging with the introduction of processes that eliminate the under-bump metallization (UBM) layer

used to improve bond strength between the solder ball and the copper redirect pad. The intermetallic compounds (IMC) formed there are mechanically weak and subject to fracture under the thermally-induced mechanical stress generated by the different expansion coefficients of the silicon die and the package substrate. UBM-free integration (UFI) eliminates the UBM and uses a thick polymer protection layer (PL) to secure the solder in place and provide stress relief between the chip and the substrate. In addition to eliminating the IMC as a source of failure, UFI reduces package cost and cycle time by eliminating layers and allows a significant reduction in final package thickness. Unfortunately, the PL, which is semitransparent and varies in thickness, causes errors in bump height measurements.

A new hybrid approach to bump height measurement (Truebump™ Technology) uses a high-accuracy sensor that combines interferometry and reflectometry to measure the top of the bump, the top and bottom of the PL and step heights at the edges of opaque materials underlying the PL with nanometer-scale accuracy and precision. The system then calculates corrections and applies them to bump height measurements made with a high-speed sensor in a subsequent 100% inspection.

Summary

Advanced packaging processes are becoming more complex and package feature sizes are shrinking, leading to process control requirements similar to the front-end applications where many AP processes originated. As feature sizes continue to decrease, performance requirements for inspection and measurement tools are becoming more difficult to meet. In addition to improvements in basic performance characteristics, like speed and sensitivity, these tools must also incorporate innovative solutions to problems that are specific to AP applications, including accurate bump height measurements and sensitivity to nonvisual defects. Ultimately, the process control needs of AP processes are best met by a flexible system that can deliver the full range of required capabilities in a single, high-throughput, capital-efficient platform.

Biography

Timothy Kryman is Senior Director, Corporate Marketing at Rudolph Technologies. He received his Bachelor of Science degree from Lock Haven U. and MBA from DeSales U. Email timothy.kryman@rudolphtech.com

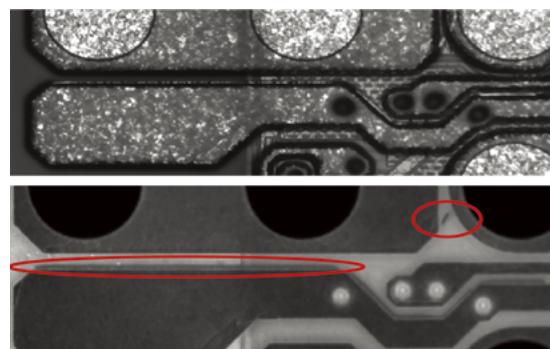
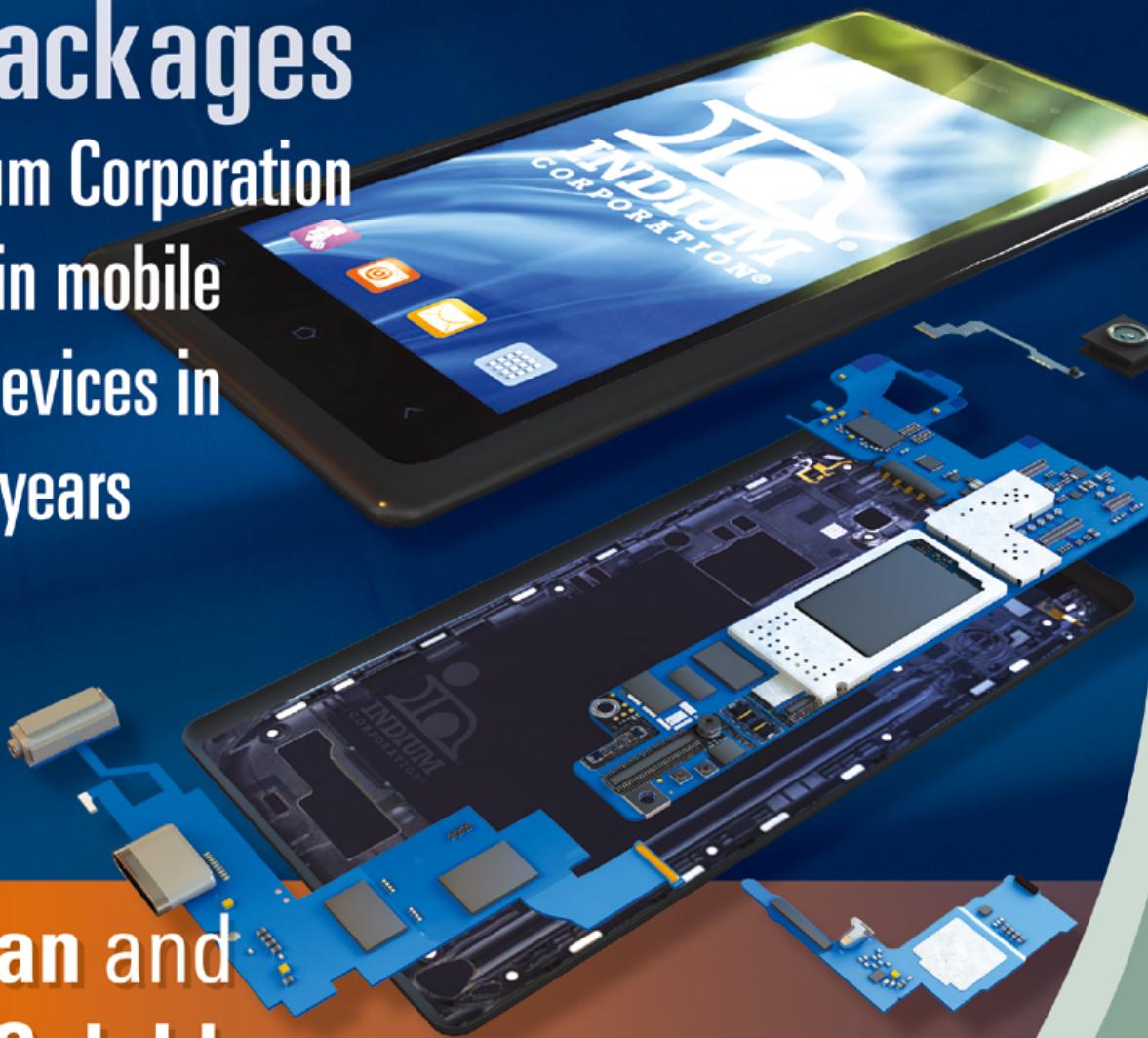


Figure 2: Nonvisual defects: a) Bright field image of RDL, the metal surface with rough grain structure looks noisy, but it cannot show the under-etch metal residue because the white light reflected from the metal residue and the organic underlayer look the same; b) Image using Clearfind Technology clearly shows the under-etched metal.

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Creating planar embedded RDL structures without CMP

By Richard Hollman [TEL NEXX Inc]; Habib Hichri, Markus Arendt [Suss Microtec Photonic Systems]; Ognian Dimov, Sanjay Malik [Fujifilm Electronic Materials]

Packaging technology is increasingly migrating to fan-out architectures, in many cases with multiple chips in a package. Current and projected designs require multiple redistribution layers, in some cases between 5 and 10 layers, with conductor linewidths down to 2 μm and via openings below 10 μm (Figure 1).

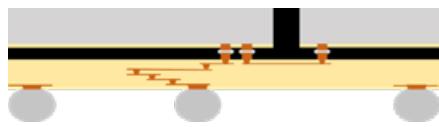


Figure 1: Multiple interconnect layers in μ -out packaging.

The high-density packaging challenges

Traditional organic flip-chip substrates are encountering challenges to scale to these dimensions. Photosensitive spin-on dielectrics for via formation, together with redistribution layer (RDL) patterned with photoresist, face serious technical challenges, causing reliability and pattern integrity concerns (Figure 2). Free-standing RDL lines with $\leq 2/2\mu\text{m}$ L/S size may cause electromigration concerns, and removing



Figure 2: Conductors patterned with photoresist, which is stripped after patterning.

the seed layer from the narrow trenches is almost impossible, or causes severe undercut to the RDL lines. The non-planar surface presents an additional challenge for the next redistribution layer because it requires a larger depth of focus for the exposure system, which in turns limits its resolution capability. Finally, warpage of the substrate during processing is increasing with additional RDL layers, so careful selection of the material with respect to thermal properties is key.

Dual-damascene process

A viable solution to overcome these challenges is to apply a dual-damascene fabrication process to deliver an embedded RDL structure. This process is well known from CMOS fabrication in the front end. A polyimide is patterned to create RDL trenches, but not stripped after development (Figure 3). A seed layer is deposited on the patterned and fully cured polyimide, followed by Cu electroplating to fill the trenches and vias. Because the seed layer is present everywhere on the polyimide surface, plating also occurs on the top surface as



Figure 3: Conductors embedded in polyimide.

well as the trenches and vias. Once the desired features are filled, it is necessary to remove the excess Cu and seed layer, which is done using the chemical-mechanical planarization (CMP) process. This CMP step adds complexity and cost to the process flow, and is a serious impediment for the adoption in advanced packaging.

To overcome these barriers, this article features a cost-saving dual-damascene fabrication process to create embedded redistribution layers for fan-out packaging. This process uses mask-based excimer laser ablation to pattern trenches and vias, a non-photosensitive dielectric with excellent thermal and resolution properties, and an innovative plating process that achieves planarization without the need for CMP. We report experimental results where RDL trenches were filled with less than 0.5 μm overburden, which is easily removed by a combination of de-plating and either wet etching or excimer laser ablation, with no damage to the embedded conductors.

Excimer laser ablation patterning

One of the key enablers for the improved embedded conductor process is patterning of the dielectric layer by excimer laser ablation tool (Figure 4). As reported in [1], this provides several important advantages over the photosensitive polyimide process:

- The dielectric material can be selected for its mechanical properties, and thermal and chemical stability. The potential to use non-photosensitive material gives access to a wider material selection and can help to significantly reduce material cost. The ability to use a wider variety of dielectric material will also provide relief with respect to wafer warpage.
- The dielectric material is patterned after final curing rather than before, minimizing dimensional and profile

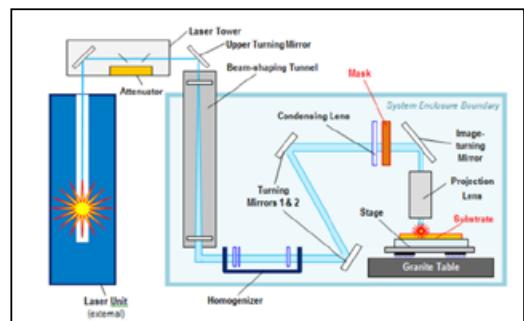
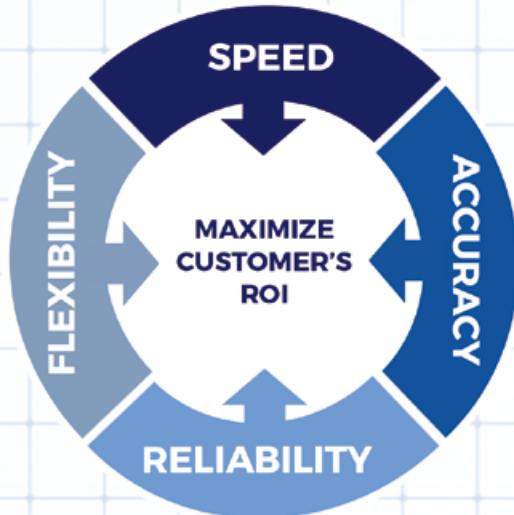


Figure 4: Excimer laser ablation stepper tool (Suss Microtec Photonic Systems).

changes and allowing smaller features.

- The development step and the descum process are eliminated along with associated equipment and materials.
- Vias and trenches can both be formed in one process step, requiring only a reticle change while the wafer is chucked on the tool.
- The technology can also be used to remove thin residual metal layers on top of a polyimide surface. This process step is critical to

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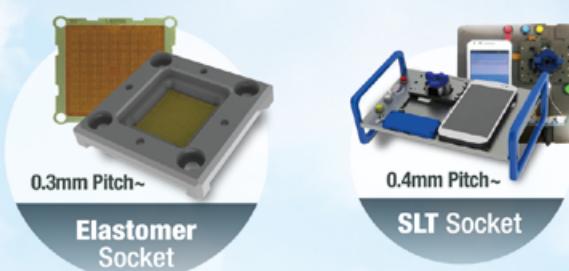
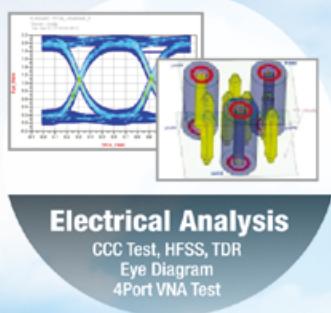
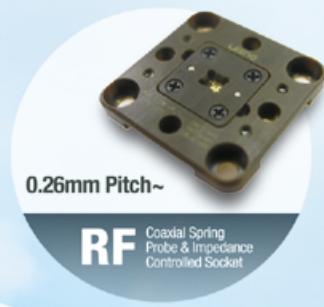
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the successful creating of planar embedded RDL structures without CMP, as described later in this article.

Excimer laser ablation patterning provides a unique flexibility not available in other patterning methods, and this flexibility turns out to be critical in making this process successful. This ablation process is available and validated for a variety of substrates, including panels.

Dielectric for embedded conductor lines

As mentioned above, the use of ablation patterning permits a choice of dielectric that is not restricted to photosensitive materials. For this work, we used FCPI-2100 polyimide from Fujifilm Electronic Materials. It exhibits excellent physical, thermal, electrical and chemical properties for this application, as shown in **Table 1**. The thermal stability is illustrated in **Figure 5**, showing negligible change in patterned feature size with baking. The thermal expansion coefficient can be modified to match a variety of substrates, including panels. It has also been shown to be compatible with a wide variety of solvents, acids and bases, including those that are likely to be encountered in the process flow.

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Moisture uptake (80%RH/80°C)	0.97%
Dielectric constant/Dielectric loss (1-20 GHz)	3.2 / 0.015
Peel strength	1.3Kgf/cm (Before HAST) 0.6Kgf/cm (after 500 hours HAST)

Table 1: Properties of FCPI-2100 polyimide (Fujifilm Electronic Materials).

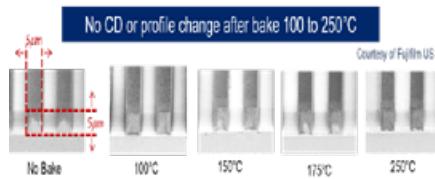


Figure 5: Thermal stability of FCPI-2100 (Fujifilm Electronic Materials).

Metalization

Metalization involves two separate processes: vacuum deposition of a seed layer, and electroplating to fill the vias and trenches.

Seed layer deposition. The seed layer provides a current path to a contact at the edge of the wafer or panel during the plating process. However, it serves the equally critical function of providing adhesion between the underlying polyimide surface and the conductors, which will be plated. Without good adhesion, delamination of the conducting lines and vias may occur after plating or during downstream process steps.

For this process, the seed layer was deposited using a TEL NEXX Apollo PVD tool. Adhesion was guaranteed by the use of an Ar-based inductively coupled plasma (ICP) etch before deposition to clean and activate the polyimide surface, and by depositing the Ti and Cu in the same chamber with no break in vacuum.

Electroplating. In previous versions of the embedded conductor process, CMP is required to remove excess metal deposited in the electroplating step. So, to eliminate CMP it is necessary to minimize the excess metal to the point where it is possible to remove it by simpler methods.

Using a modified version of a commercial TSV plating chemistry, an efficient bottom-up plating process was developed (**Figures 6, 7**). This process can fill trenches 6μm deep with overburden less than 0.5μm.

We can begin to understand the mechanism for bottom-up filling in this case in terms of TSV plating, although there are important differences, as we

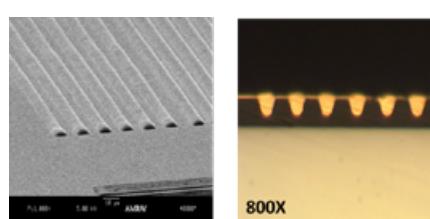


Figure 6: 2–3 μm trenches filled using a bottom-up plating process.

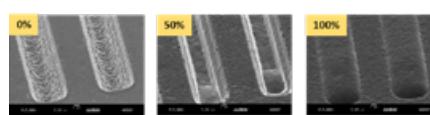


Figure 7: Surface evolution during plating showing bottom-up trench fill.

shall see. A TSV plating chemistry includes three organic additives: an accelerator, which catalyzes the deposition reaction; a leveler, which strongly inhibits this reaction; and a suppressor, which moderates the surface kinetics of the two other species. In TSV plating, bottom-up filling is achieved because the leveler, which is a slower-diffusing molecule, is initially present in a much smaller concentration at the bottom of the via than at the top surface. So, the plating deep within the via is dominated by the accelerator, while plating is suppressed on the top surface and the upper parts of the sidewall.

For embedded conductor structures, the diffusion distances are a few microns at most, and aspect ratios are 1:1 or less. So, segregation of the leveler purely due to diffusion does not appear likely. However, the increase in effective surface area presented to the solution, from the sidewalls of the ablated features and the

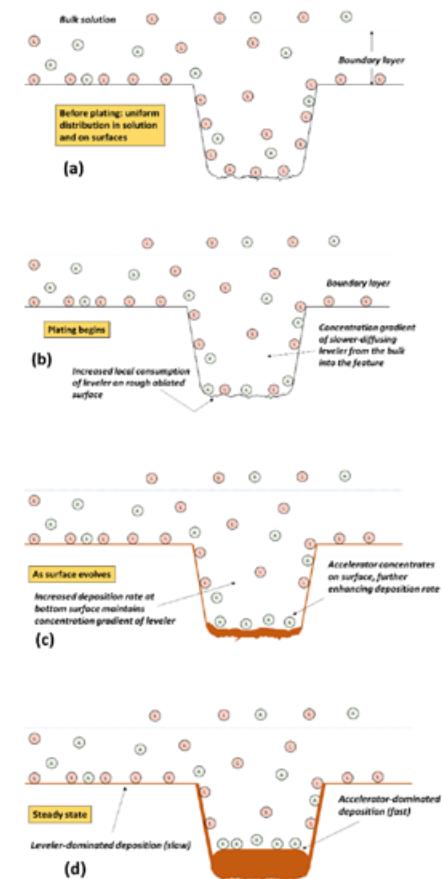


Figure 8: Illustration of the “leveler depletion” hypothesis to explain bottom-up plating:
a) initial state, b) at start of plating, c) leveler and accelerator concentrations adjust, and d) steady-state plating condition. The suppressor is not shown here.

roughness of the ablated surfaces, may cause a modest increase in the initial consumption of leveler in these locations, plus a modest geometric buildup of accelerator as the Cu surface evolves. Once established, this can become a self-perpetuating process (**Figure 8**), with leveler-dominated plating at the top surface and accelerator-dominated plating in the ablated features.

This plating process exhibits the phenomenon of “momentum plating,” i.e., the deposition proceeds at a faster rate on the trench feature even after the trench has been completely filled. This phenomenon is also seen when the plating includes a via to connect two layers (**Figure 9**).

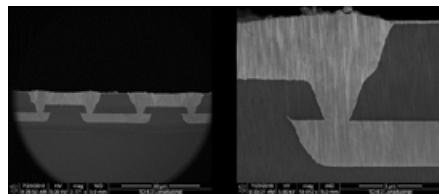


Figure 9: Cross section SEM of a bottom-up plated dual-damascene structure.

Challenges for a planar process

There are two critical challenges which must be met in order to provide a practical process. First, while the overburden is very small, it is not zero, and this metal, plus the original seed layer, must be removed before subsequent processing can occur. Second, the efficient bottom-up plating is very sensitive to the size of the ablated features. In our tests, trenches up to 10 μm in width could be filled with a reasonably small overburden, but for 15 μm and wider lines the fill was incomplete.

Residual metal removal. The first challenge, removal of residual metal without CMP, has been demonstrated in two different ways. In both cases, the metal removal begins in the plating step itself. Once the ablated features are filled, the plating current can be reversed. Nearly all of the Cu can be removed from the top surface without compromising the plated conductors themselves. This leaves a very small residue of Cu to be removed, along with the Ti adhesion layer. The second step, to complete the residual metal removal, has been demonstrated with two different approaches

(**Figure 10**): either with a brief wet etch, or by excimer laser ablation. Although metal layers of 1 μm or greater thickness serve as an effective etch stop for excimer laser ablation, very thin layers on a polyimide surface can be efficiently removed. Either approach provides the desired savings in equipment and materials cost and process complexity from elimination of CMP.

Feature size dependence. In larger features, an efficient bottom-up plating becomes more challenging because the concentration of the leveler at the bottom of the feature is significantly higher than in smaller features, which leads to a slower plating speed. A potential solution to this problem is to modify the surface texture of these larger features that allows the accelerator to dominate the plating process inside the patterned structures. We are currently investigating suitable methods for surface texturing that will allow preferential bottom-up plating in large features, as well as small lines and vias. The plated features should ideally be nearly flush with the surrounding surface, so that, after application of the next layer of dielectric, a sufficiently planar surface is presented for the next sequence of RDL layer formation.

Summary

Planarization is an essential part of any multilayer RDL stack structure. Embedded conductors are a means to this end, but deposition processes to this point have included significant metal on the top surface, requiring CMP for removal. This not only represents an added expense in equipment and materials, but may be a barrier to panel applications. We have shown that, with the right combination of materials,

patterning method, and metallization, an embedded conductor structure can be fabricated with minimal residual metal, which can be removed with simpler and less expensive techniques. One key aspect of this is the use of bottom-up electroplating, adapted from TSV processing.

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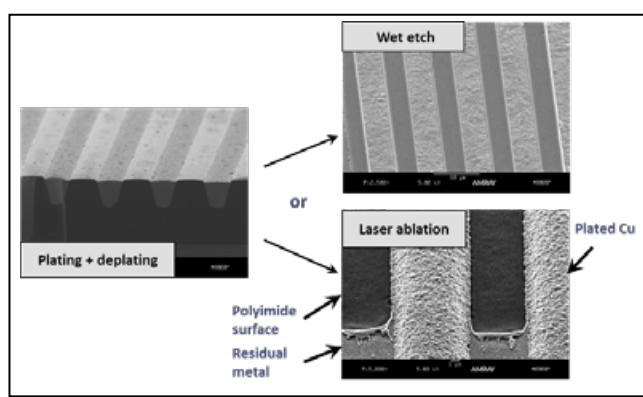
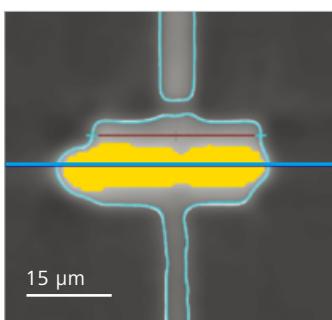


Figure 10: Residual metal removal without CMP: deplating plus wet etch or ablation.

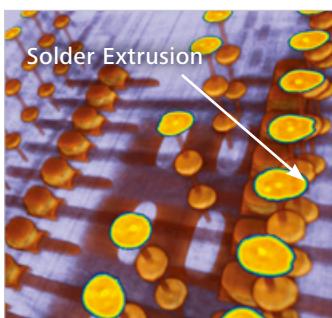


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Virtual XRM cross section of a TSV-ubump structure for solder extrusion for measurements of solder extrusion (in yellow)



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High-resolution 3D X-ray microscopy for semiconductor advanced packaging measurements

By Cheryl Hartfield, Allen Gu, Raleigh Estrada [ZEISS Semiconductor Manufacturing Technology, PCS Strategic Business Unit]

The demand for increased miniaturization and higher I/O in mobile and high-performance devices has driven an explosion of innovations that enable high-density multi-chip architectures, including but not limited to 2.5/3D memory and logic packages, wafer-level packages (WLP), and system-in-package (SiP). Increasingly, these designs are driving packaging interconnects into the third dimension. Measurements at critical process steps are a key enabler for the introduction and production of new and advanced technologies that have narrow process margins or are difficult to control. Because the structures in today's advanced packages are often inaccessible or too small for measurements by commonly used nondestructive methods (for example, 2D X-ray), new approaches are required to accomplish these measurements with a practical throughput to enable the fastest time-to-market for new products.

Submicron 3D X-ray microscopy (XRM) offers a new approach to enable rich volumetric and linear measurements in a streamlined way that can be automated and without the need for time-consuming, manual cross sections. **Figure 1** shows the power of analyzing a bulk volume in 3D (**Figure 1b**) versus analyzing a plane of structures (**Figure 1a**) [1]. There are greater numbers of structures accessible in the 3D volume, enabling better measurement statistics and opportunity for new types of measurements that are not possible from 2D cross section images. Additionally, 3D XRM can provide better measurement repeatability, especially as the continued shrink of structures accelerates the difficulty to perform a cross section accurately to a desired measurement plane while simultaneously avoiding polishing artifacts.

XRM measurement of advanced package structures

A key advantage of 3D XRM aiding both failure analysis and measurement applications is the ability to image any plane from any angle within the virtual 3D dataset. Defects and structural variations can be observed from a desired view and exactly in the plane of interest. The observation is typically accomplished by viewing successive virtual cross sections through manual interaction with the data set. Because it is a virtual data set, any cross-sectional slice may be viewed at any point in the 3D volume from any direction. This offers tremendous benefit over physical cross sectioning, where only one cross-sectional plane is available to view [2].

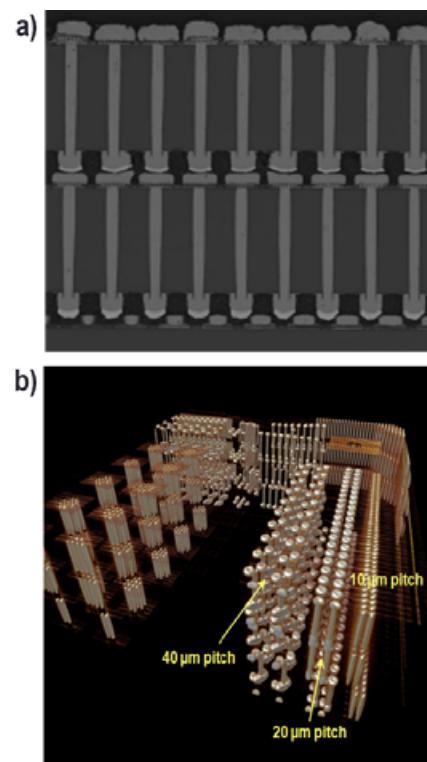


Figure 1: a) SEM image of a physical cross section; b) 3D X-ray microscopy image of the same structures. 3D images enable direct volumetric measurements in addition to linear measurements.

For the application of measurements, after acquiring the XRM tomographic data, a semi-automated measurement workflow is used to extract useful structural information from the sample. Involving multiple steps, the workflow is often scripted in a measurement template to speed up measurement and eliminate human errors. The workflow is described below.

First, surfaces of structures of interest are precisely extracted by a local adaptive algorithm. Second, the structures to be measured in the 3D data are registered in a coordinate scene by object alignments. Third, key geometric elements and features are created on the registered volume. Finally, the relevant measurement results are directly extracted and reported. The result is not limited to linear or 2D metrics. Various volumetric parameters and 3D features can be generated through this workflow. Because the measurement template can be repeatedly applied to other data, automation is possible to enhance measurement efficiency.

The 3D reconstructions from XRM scans provide rich data for statistical analyses, which are vital to ramping the manufacturing yield of new complex advanced packages. Fast nondestructive measurements allow process integration engineers to look at data from statistically relevant sampling percentages from a manufacturing line. XRM 3D reconstructions and their data can also be stored for archival purposes. If required, 3D volumetric measurements can be converted by the software to 2D linear measurements to allow for comparisons to later destructive measurements.

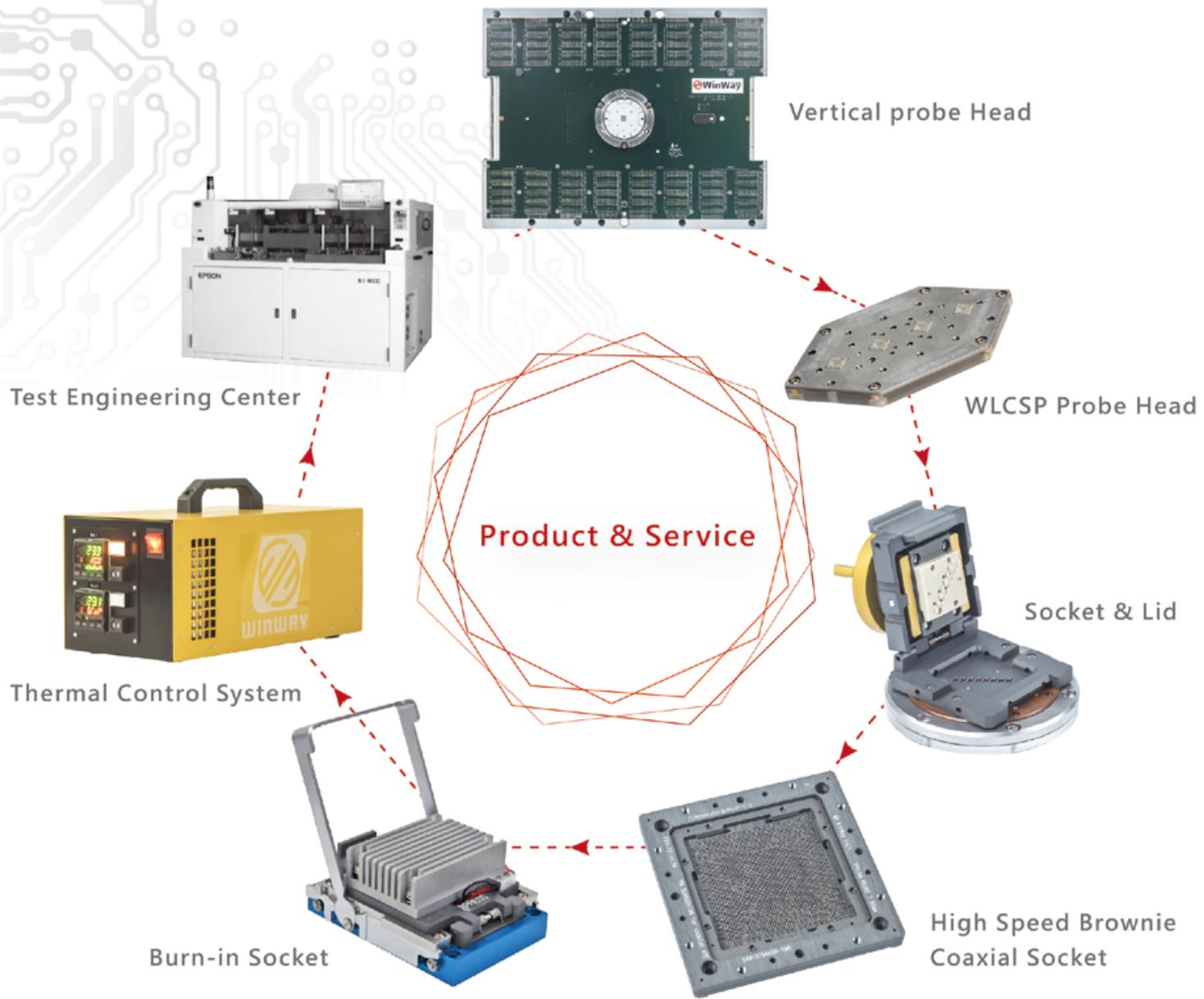
Case study: CMOS image sensor package for smartphone cameras

CMOS image sensor (CIS) devices are small and efficient parts of the cameras in mobile handsets, with most advanced



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smartphones today featuring two or more CISs. Pixel counts continue to increase, while functionalities like autofocus add complexities to the required hardware in the CIS package. Gold (Au) bump height uniformity is a critical parameter that is controlled for high yield and reliability and is the subject of this case study.

A corner of the image sensor package was chosen for XRM analysis using $2.5\mu\text{m}$ voxel resolution, which is more than adequate for these $\sim 100\mu\text{m}$ diameter structures. The scan location is indicated in **Figure 2a** and the resulting 3D dataset shows details of the low-temperature co-fired ceramic (LTCC) and Au bump structures (**Figure 2b**). The virtual cross sections aid in the setup of the measurement workflow on the structures of interest – in this case, the Au bumps.

For XRM measurements to be practical, they must be repeatable and have reasonable throughput, including the times for image acquisition. The 3D XRM scan duration for an advanced package typically ranges from 20 minutes to 4 hours, depending upon the resolution desired and the required signal-to-noise ratio (S/N). For a specific target resolution and changing only the sample dimensions, larger packages require longer scan times than smaller packages.

To establish ideal imaging parameters for CIS Au bump measurement accuracy and throughput, different voxel sizes and scan times were tested for the CIS package. The results in **Figure 3** show that algorithms can extract relatively accurate measurements from noisy data. Considering a 3-hour scan time at $2.5\mu\text{m}/\text{voxel}$ as the standard for generating a quality image for measurement with low noise, a 20-minute scan at $2.5\mu\text{m}/\text{voxel}$ produces image quality sufficient for good measurements, as shown by the virtual cross section images in **Figure 3b** and **3c**, and the resulting measurements of Au bump heights from each, shown in **Figure 3d**. A 20-minute scan, therefore, provides actionable information from samples, which had previously required 3 hours of XRM scanning, or 10+ hours of preparation using epoxy embedding and mechanical cross-sectioning. In addition to bump height, the XRM data also enables measurement of Au bump volumes (**Figure 3e**), which, combined with the height measurements, give insights into the bumping process. While the data shows that smaller bump height measurements in

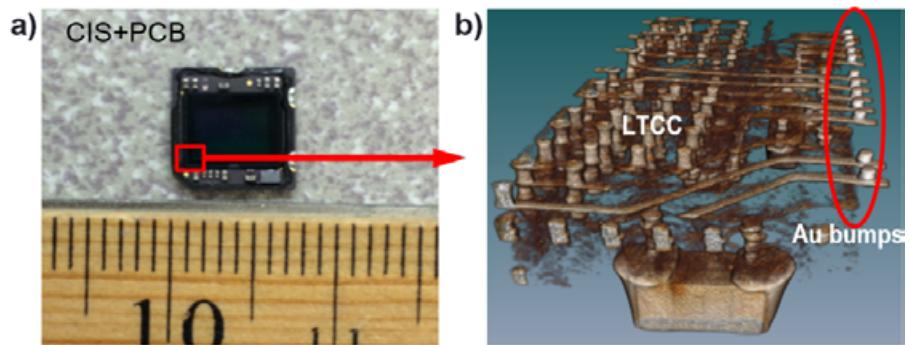


Figure 2: CMOS image sensor sample showing Au bump locations: a) The image sensor package showing the scan location; b) The XRM generated 3D dataset with the Au bump locations highlighted.

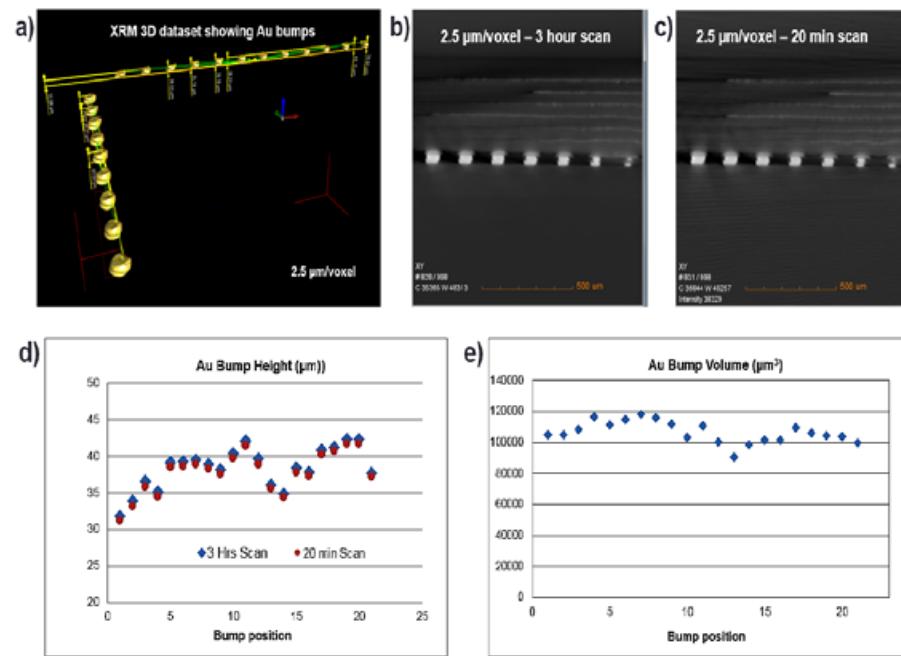


Figure 3: CIS Au bump height and volume measurements: a) The XRM 3D dataset; b and 3c) a virtual cross-section extracted from an XRM dataset acquired in 3 hours (3b) vs. 20 minutes (3c) using $2.5\mu\text{m}/\text{voxel}$; d) Au bump height measurements from both 3 hour and 30 min scans showing good correlation; and e) Au bump solder volume measurements from the same dataset.

this corner of the package correlate well with lower bump volume measurements, the shortest bump height measurements do not, which may indicate something else besides solder volume is influencing bump heights during the assembly process.

Case study: DRAM die stacks

For the highest-speed computer systems today, electrical signal traces between transistors and functional circuit blocks must be minimized in length to prevent system delays. In high-speed memory packages, through-silicon vias (TSVs) typically made of copper (Cu) metal encapsulated within thin cladding layers of barrier materials are used to

connect stacks of DRAM chips. The TSVs are fabricated across the silicon wafer before it is diced into individual chips, and nonuniformities in wafer-scale fabrication processes, such as deposition and etch, can induce height variations in TSVs across each chip.

In addition, though interconnect pitches $>30\mu\text{m}$ are still used today, the bump roadmap shows pitches going down to $5\mu\text{m}$ for stacked chips [3]. In order to enable smaller I/O pitches and greater I/O density, Cu-pillar microbumps are used together with thermocompression bonding (TCB). Because stacked DRAM employs thinned silicon on the order of $50\mu\text{m}$ (and projected to decrease to $20\mu\text{m}$), wafer and die warpage become

a challenge. There is a minimum of available solder volume in Cu-pillar microbumps to compensate for warpage-induced surface unevenness, and thus process windows become smaller as co-planarity requirements increase. This means the TCB process must be well-controlled to achieve the required high yields of >99.8% per attached die. For these reasons, bond line thickness (BLT) measurements are a key metric used to develop and monitor the TCB process.

The capability of 3D XRM to address BLT measurements was assessed. A 64GB DRAM chip stack, currently in high-volume manufacturing with ~6 μm diameter TSVs and ~30 μm diameter bumps, was analyzed. Conditions were set so a 0.7 $\mu\text{m}/\text{voxel}$ image from a region containing TSVs and microbumps could be obtained in just 30 minutes. **Figure 4a** shows the reconstructed 3D data set from this region, and **Figure 4b** shows the virtual cross section with the extracted features used for BLT measurements highlighted in yellow. The BLT was measured at the site of every bump within the 3D volume, resulting in close to 100 individual BLT measurements. This quantitative data is plotted by bump position in the graph shown in **Figure 4c**. As indicated by the “Die tilt?” arrow in the graph, XRM can extract information revealing a gradual shift in BLT, which could be due to a pressure or temperature variation at this die location. This sort of information can be fed back to the manufacturing process engineers to highlight the need to look for TCB process variations.

Information about other DRAM features in the stack, such as die-to-die alignment, can also be easily seen in other 2D virtual cross sections. Also, the influence of the TCB process on the solder shape can be assessed to evaluate the risk of shorts or opens. The capability of 3D XRM to evaluate structures from any direction is especially helpful for this type of evaluation. **Figure 5** shows an analysis of solder shapes to learn about solder extrusion resulting from the TCB process. In **Figure 5a**, a false color image shows a cross section perspective through a 3-row stack of TSV/microbumps. The solder, only ~6 μm thick, is highlighted in red for visibility, while the TSVs and 30 μm diameter Cu pillars are green. In this view, the amount of solder extrusion (as defined by the amount of solder

extending past the area of the Cu pillar) appears to be minimal. However, a plane-view perspective, as shown in **Figure 5b**, indicates that some bumps have significant amounts of solder extrusion, in particular, those located in the lower right quadrant of the image.

These qualitative images are useful for understanding the TCB process. However, to manage large amounts of data on a recurring basis, free from the subjective bias of a human operator, quantifiable information is desired. **Figure 5c-f** show how the 3D XRM data can easily be converted from qualitative images of solder extrusion into quantifiable measurements based on the concept of “solder projection.”

Figure 6 explains the overall concept of “projected area.” The perimeter or outline of a feature can be projected in any desired plane. An example of a hidden 3D feature contained within a bulk volume is shown in **Figure 6a**. Projections of this feature onto X, Y and Z planes are represented by red, green and blue, respectively. By using this method, projected areas of a targeted structure are obtained in a desired plane.

Projected areas of extruded solder, obtained as described in **Figure 5**, are plotted per bump position in **Figure 6b**. Additionally, projected solder areas are included of the larger bumps connecting to substrate traces (visible in the bottom row of **Figure 5a**). The consistency in microbump projected solder area contrasts with the varied results for the larger bumps, which tolerate a larger process window on account of having larger solder volumes. In order to test the repeatability of the data, the measurements were acquired three times. As shown by the blue, green and red data points, these 30-minute XRM measurements have good repeatability.

Summary

Submicron XRM technology is commonly used for failure analysis of advanced packages and is now being extended to the quantitative measurements of advanced package structures. In order to continue to shrink interconnects and increase I/O density, XRM volumetric data becomes important for characterizing package interconnects.

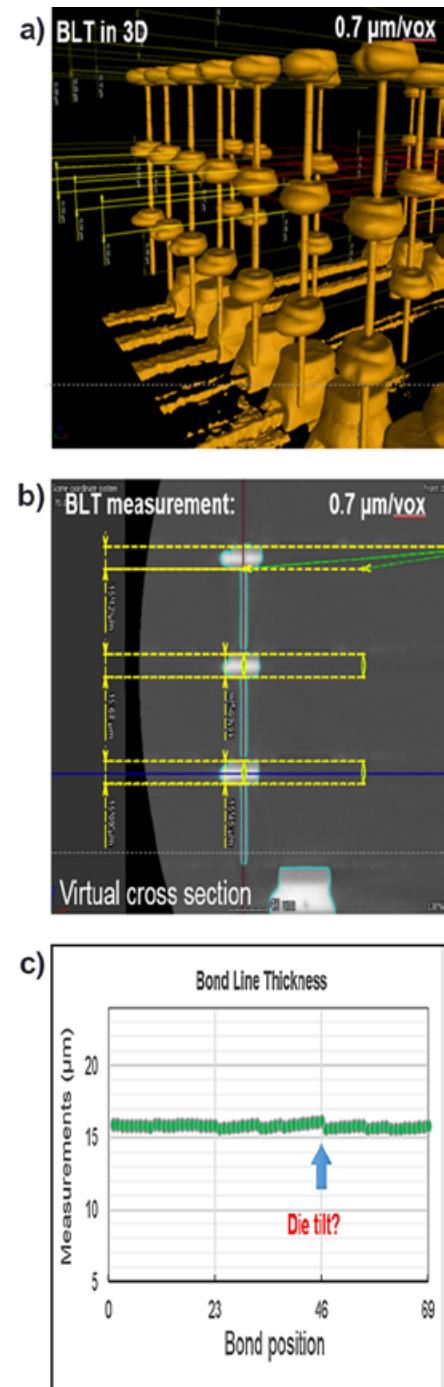


Figure 4: Bond line thickness measurement from a 64GB DRAM chip stack: a) The XRM 3D dataset acquired in 30min at 0.7 μm voxel resolution. 4b) Virtual cross section of XRM dataset with extracted features highlighted and the bond line measurement highlighted in yellow; c) Graph of bond height measurements by bump position.

This new approach of submicron 3D XRM enables rich volumetric and linear measurements in a streamlined way that can be automated and without the need for time-consuming, manual cross sections.

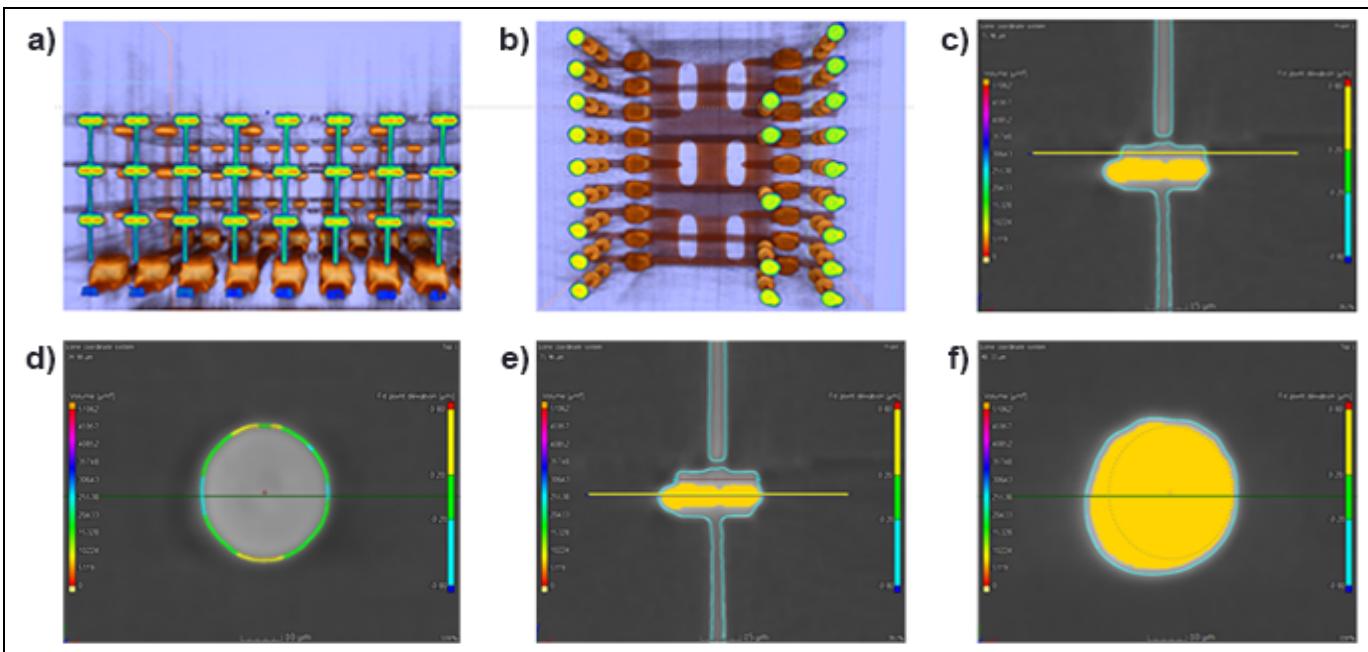


Figure 5: Quantifying solder extrusion using 3D XRM: a) 3D volume viewed from the bond height perspective; b) Top down perspective showing the direction and degree of solder extrusion; c) High-resolution virtual cross section of a single bond structure, with a yellow line defining the Cu-pillar plane (5d) chosen for projected area analysis; e) The same image as 5c with a yellow line indicating the solder plane (5f) chosen for projected area analysis. The faint dotted line is the outline of the Cu pillar projected area shown in 5d.

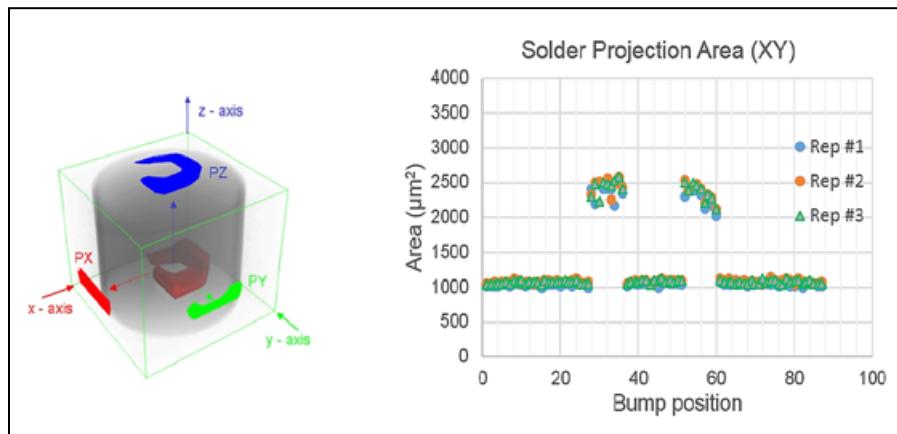


Figure 6: Using a 3D XRM data set to quantify the degree of bond line solder extrusion: a) A buried feature contained within a volume is projected onto X (red), Y (green) and Z (blue) planes. Each color represents the projected area for that plane; b) Projected solder areas are plotted per bump position for microbumps, as well as the first layer of larger solder bumps.

There are greater numbers of structures accessible in the 3D image, enabling better measurement statistics and opportunity for new types of measurements that are not possible from a 2D cross section. Solder volumes and shapes can now be measured and combined with 2D measurements to better understand advanced packaging processes, such as thermocompression bonding. Additionally, 3D XRM may provide better measurement repeatability than can be obtained from mechanical cross sections, especially as the continued shrink of structures accelerates the

difficulty to cross-section accurately to a desired measurement plane while simultaneously avoiding polishing artifacts. Practical timeframes of 20 and 30 minutes have been demonstrated.

Biographies

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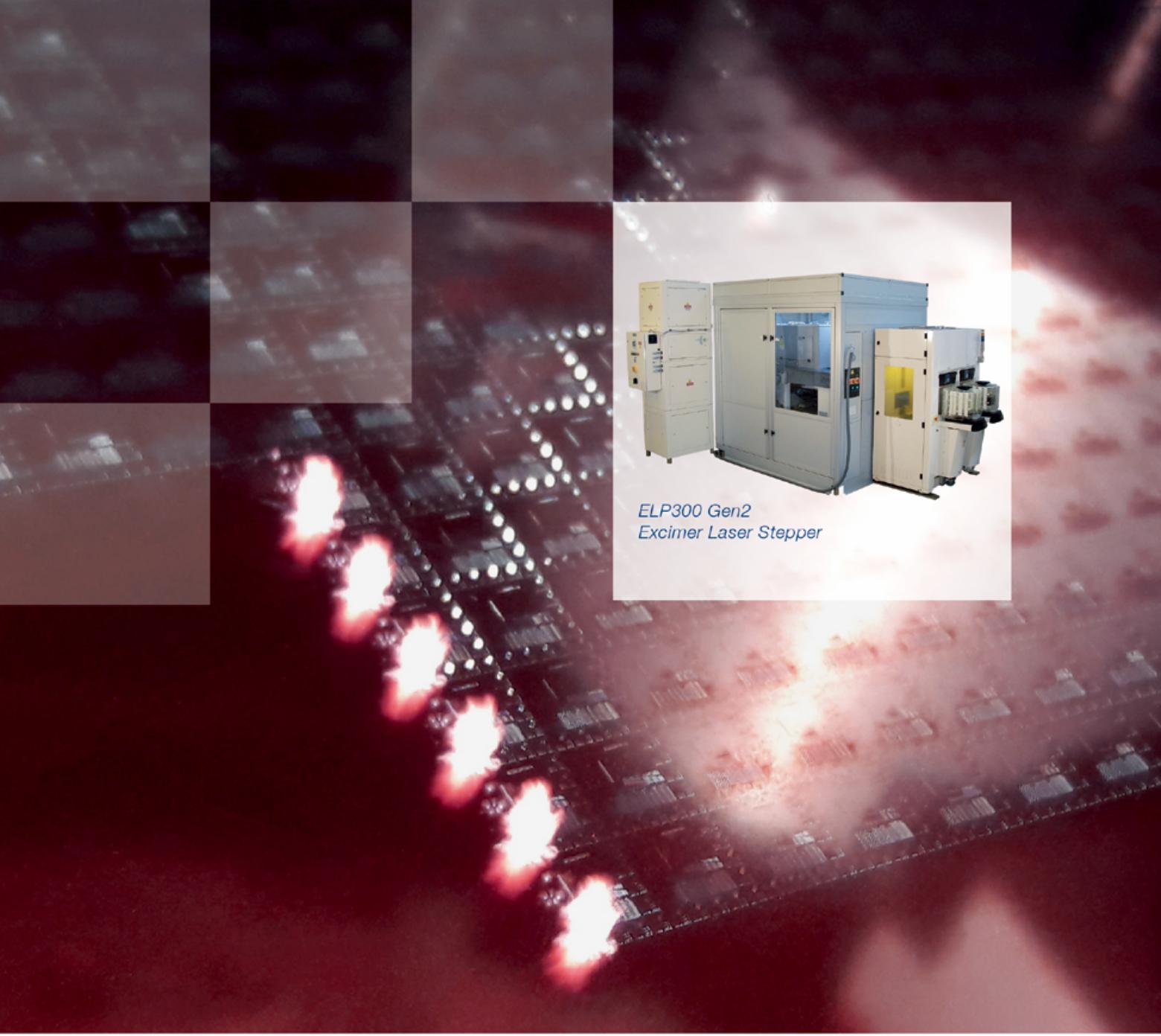
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HANMI Semiconductor Co., Ltd. 532-2 Gajwa-Dong, Seo-Gu Incheon, 404-250, South Korea Tel: +82-32-571-9100 www.hanmisemi.com	2D, 3D CM MP - CM PKG, SUB, PCB		

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Hitachi Engineering & Services Co., Ltd. 3-2-2, Saiwai-cho, Hitachi-shi Ibaraki 317-0073, Japan Tel: +81-294-22-7111			3D PR MP - 360 mm WFR, PKG, SUB, PCB
Intekplus Co., Ltd. (Tamilip-dong), 263 , Yuseong-gu, Daejeon, Korea (34026) Tel: +82-42-930-9900 www.intekplus.com	2D, 3D PR MP - CM SDP, PKG, SUB, PCB		
Jordan Valley Semiconductors, LTD. Zone #6, Ramat Gavriel Industrial Zone Migdal Ha'Emek 23100 Tel: 972-4-654-3666 www.jvsemi.com	2D, 3D PR MP - 300+ mm WFR, PKG		
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Koh Young Technology Inc. 14F,15F Halla Sigma Valley, 53 Gasandigital 2-r Geumcheon-gu, Seoul 08588 South Korea Tel: +82-2-6343-6000 www.kohyoung.com	3D PR MP - 810 mm PKG, SDP, SUB, PCB		
Landrex Technologies Co., Ltd. No.570, Jianguo Rd., Yingge Dist., New Taipei City 239, Taiwan (R.O.C.) Tel: 886-2-26787966 www.landrex.com.tw	CM PR CM WFR, SUB, PCB		
Lloyd Doyle Ltd. Molesey Road, Walton on Thames Surrey KT12 3PI, England Tel: +44-1932-245000 www.lloyd-doyle.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Machine Vision Products Inc. 3270 Corporate View, Suite D Vista, CA 92081, USA Tel: +1-760-438-1138 www.visionpro.com	3D PR MP - 600+ mm PKG, SDP, SUB, PCB		
Machvision Inc Co., Ltd. NO. 2-3, Gongye East 2nd Road II, Hsinchu Science Park, Hsinchu 30075, Taiwan, R.O.C Tel: +886-3-563-8599 www.machvision.com.tw	2D, 3D PR, NP MP - 600+ mm SUB, PCB		

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Microtronic Inc. 171 Brady Avenue Hawthorne, NY 10532 Tel: 1-877-642-7687 www.microtronic.com	2D PR, NP MP - 300 mm WFR		
MIRTEC USA 3 Morse Road Oxford, CT 06478 Tel: 203-881-5559 www.mirtecusa.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Nantronics Automation 777 Flynn Road Hollister, CA 95023 Tel: 1-831-630-0700 www.nantronics.co	2D, 3D PR MP - 200 WFR		
Nikon Metrology Europe Geldenaaksebaan 329 3001 Leuven, Belgium Tel: +32 16 74 01 00 www.nikonmetrology.com	2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Nordson DAGE (Dage Precision Industries Ltd.) 25 Faraday Road Aylesbury Buckinghamshire HP19 8RY Tel: 44.1296.317800 www.nordson.com/en/divisions/dage		2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB	
Nordson YESTECH 2747 Loker Ave West Carlsbad, CA 92010 Tel: 760.918.8471 www.nordson.com/en/divisions/yestech	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
North Star Imaging Inc. 19875 S Diamond Lake Road Rogers, MN 55374 Tel: +1-763-312-8836 www.4nsi.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Okos Solutions, LLC 7036 Tech Cir Manassas, VA 20109 Tel: +1 703.880.3039 www.okos.com			3D PR MP - 900 mm WFR, PKG, SUB, PCB
Orbotech Ltd. Shderot Hasanhedrin Yavne 81101, Israel Tel: +972-8-942-3533 www.orbotech.com	2D PR MP - 1,118 mm SUB, PCB		
PVA TePla Analytical Systems GmbH Deutschordenstrasse 38 73463 Westhausen, Germany Tel: +49-7363-9544 0 www.pva-analyticalsystems.com			3D PR MP - 420 mm WFR, PKG, SUB, PCB

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Rudolph Technologies, Inc 16 Jonspin Road Wilmington, Massachusetts 01887 Tel: 978.253.6200 www.rudolphtech.com	2D, 3D MP - 300mm PL WFR		
Saki Corporation DMG MORI Tokyo Digital Innovation Center 3-1-4, Edagawa, Koto-ku, Tokyo 135-0051 Japan Tel. +81(0)3-6632-7915 www.sakiglobal.com	CM PR MP - 500 mm SDP, SUB, PCB	2D, 3D PR MP - 510 mm WFR, PKG, SUB, PCB	
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Semilab USA LLC. Address: 101 Billerica Avenue Building 5, Suite 105 North Billerica MA 01862 USA Tel: +1 508 647 8420 www.semilab.hu			
Sonix Inc. 8700 Morrissette Drive Springfield, VA 22152 Tel: +1-703-440-0222 www.sonix.com			3D PR MP - 350 mm WFR, PKG, SUB, PCB
Sonoscan Inc. (Nordson Sonoscan) 2149 E. Pratt Blvd. Elk Grove Village, IL 60007 Tel: +1-847-437-6400 www.sonoscan.com			3D PR MP - 610 mm WFR, PKG, SUB, PCB
SUSS MicroTec Inc. 220 Klug Circle Corona, CA 92880-5409 Tel: +1 951 817 3700 www.suss.com	2D, 3D PR, NP MP - 300 mm WFR (BONDED)		
Teradyne, Semiconductor Test Division 700 Riverpark Drive North Reading, MA 01864 Tel: +1-978-370-2700 www.teradyne.com/products/semiconductor-test		2D, 3D PR, NP MP - 450+ mm PKG, SUB, PCB	

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Test Research Inc. 7F., No.45, Dexing West Road., Shilin District Taipei City 11158, Taiwan Tel: +886 2 28328918 www.tri.com.tw	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Mars Tohken Solutions Co. Ltd. Shinjuku-gyoen Muromachi Bldg., 1-8-5, Shinjuku, Shinjuku-ku, Tokyo 160-0022 Tel: +81 3 3352 8537 www.mars-tohken.co.jp/en		2D, 3D PR MP - 400 mm WFR, PKG, SUB, PCB	
Toray Engineering Co., Ltd 6th Floor, Yaesu Ryumeikan Building 1-3-22 Yaesu, Chuo-ku Tokyo, 103-0028, Japan Tel: +81+3+3241-1541 www.toray-eng.com	3D PR MP - 300 mm WFR		
VI Technology (Mycronic AB) Rue de Rochepleine 38120 Saint Egrève FRANCE Tel: +33 4 7675 8565 www.vitechnology.com	2D, 3D PR MP - 600+ mm SDP, PKG, SUB, PCB		
Quality Vision International Inc. 1711 W. 17th Street. Tempe, AZ 85281 Tel: +1-480-295-3150 www.viewmm.com	2D, 3D PR, NP MP - 300+ mm SDP, PKG, SUB, PCB		
Veeco - Ultratech 3050 Zanker Road San Jose, CA 95134 USA Tel: 408 321-8835 www.veeco.com	2D, 3D LS, PR, NP MP - CM SDP, PKG, SUB, PCB		
Viscom AG Carl-Bederus-Straße 9 - 15 30455 Hanover Germany Tel: +49 511 94996-0 www.viscom.com	2D, 3D PR, NP MP - 508 mm, 660mm, 750mm (optional 2000mm) PKG, SDP, SUB, PCB	2D, 3D PR, NP MP - 450mm, 610mm, 722mm PKG, PCB, SPD	
Vitrox Corporation Berhad 746, Persiaran Cassia Selatan 3 Batu Kawan Industrial Park 14110 Bandar Cassia Penang, Malaysia. Tel: +60-4-646 6227 www.vitrox.com	2D, 3D PR, NP MP - 762 mm SDP, PKG, SUB, PCB	3D PR MP - 609 mm WFR, PKG, SUB, PCB	
VJ Group Inc. 89 Carlough Road Bohemia, NY 11716 USA Tel: +1-631-589 8800 www.vjt.com/vje/vje		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	

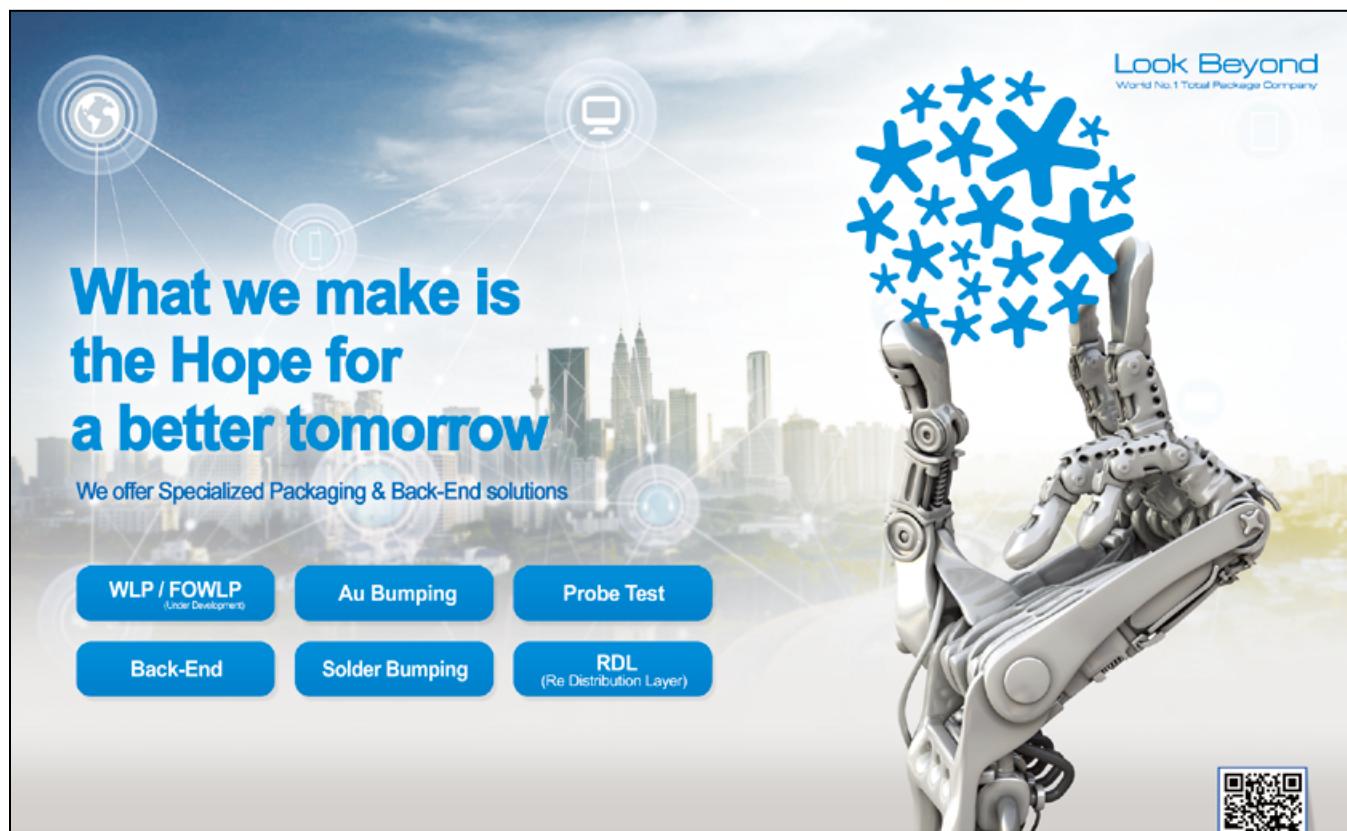
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YXLON Int'l Inc. (COMET Group) 5675 Hudson Industrial Parkway Hudson, OH 44236 Tel: +1 234 284 7849 www.yxlon.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
ZEISS 4385 Hopyard Rd #100 Pleasanton, CA 94588 Tel: +1-925-701-3548 www.zeiss.com/pcs	2D, 3D LS, PR, NP MP 300+mm, PL WFR, PKG, SDP, SUB, PCB	2D, 3D PR, NP MP - 600+mm WFR, PKG, SDP, SUB, PCB	
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The clouded view of WCSP inspection strategies

By M. Todd Wyant *[Texas Instruments]*

Semiconductor parts continue to shrink at alarming rates.

As parts approach greater than one million units on a three hundred millimeter (mm) analog wafer, many visual containment actions are being pushed past the breaking point. System improvements for detection are limited as algorithms, and detection strategies are still limited when it comes to small defects on traditional flows. **Figure 1** shows the progression from 1mm part sizes down to 0.125mm, highlighting the difficulty encountered when trying to detect defects on such small components.

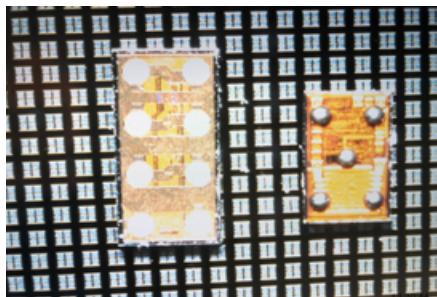


Figure 1: This graphic shows the progression from 1mm-part sizes down to 0.125mm, highlighting the difficulty encountered when trying to detect defects on such small components.

Today, more than ever, there is an increased pressure to ship parts without defects and achieve single-digit defective parts per million (dppm) levels. The continued industry push is to apply new technology and methods to ultimately create a situation where all defects are contained or eliminated prior to shipment. Today's inspection equipment can scan parts quickly and produce detailed inspection reports to drive improvements, but with part sizes exponentially shrinking and key return defect modes not shifting, the push now is to further improve inspection capabilities to detect problems even with the smallest of components.

The continued push to increase resolution has reached the tipping point. Resolution is becoming so detailed that all components are starting to look different.

The variation being introduced with this high resolution is leading to false rejectivity that is hindering the situation and time needed to drive improvements (**Figure 2**). Implementing filtering and other methods to prevent false rejectivity is leading back to release of the same returned items into the pack solutions that ultimately end up back into the customer's hands. In addition, this complexity drives engineering time and effort that ultimately impacts cost.

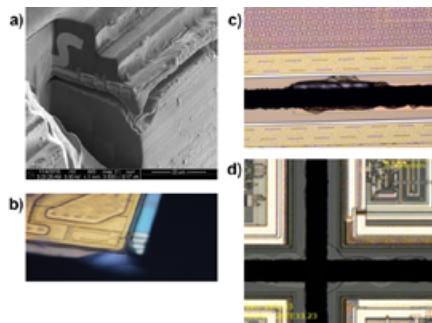


Figure 2: Examples of challenging rejects: a) Side wall crack; b) Corner crack; c) Common edge chip; and d) Hairline cracks.

This balance between over-rejection and rejected shipments has been a long-standing problem, and demonstrates the real challenge of implementing a quality assurance system. Meeting modern manufacturing demands of delivering fast and accurately is challenging, while simultaneously driving cost through scrap reductions and improved process efficiency.

Current working path

Today, assembly sites are driving to implement inspection solutions that use infrared (IR) or standard high-resolution imaging to detect, measure, and contain

defects. These methods rely heavily on lighting, imaging and software to detect and contain rejectivity. However, the issue with this method has shown that false rejectivity will be a way of life. During testing on many different platforms, anywhere from 2-8% of false rejectivity has occurred with the best case settings. Depending on the system type, productivity loss can be anywhere from 5-50% for increased inspection time required.

The new methods have also demonstrated limitations in finding and detecting all rejectivity. In addition, as shown in **Figure 3**, the use of rotated silicon structures prevent IR from passing through the substrate during visual inspection. In

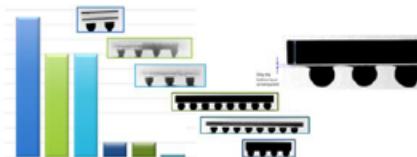


Figure 3: Rotated silicon effects on IR transmissivity.

the system during inspection, the silicon lattice prevents clean exit of the infrared light penetration through the component. The result of IR on these products is a black surface that is not visible with detection software. The chart shows the difference with varying substrate rotation, with and without backside coatings below, and highlights the challenges of inspection using IR technology solutions.

Challenging defects are really what is driving inspection capability increases, while cost and end users continue to drive parts smaller. **Figure 4** shows the dilemma with any inspection process as defect sizes are very small. Cracks and damage cross

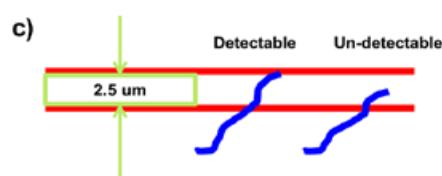
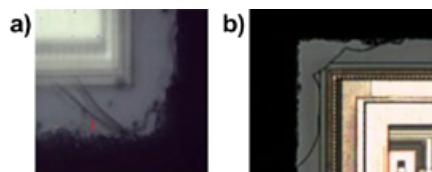


Figure 4: Examples of marginal defects: a) Whisker crack; b) Corner hairline crack; and c) Crack failure limit.

into active circuitry areas, but the length is not meeting crack length measurement thresholds that would allow detection.

The clouded view of visual inspection

What we see today are countless operations fighting the vision conflict in high-volume manufacturing (HVM) operations. It is a delicate balance between scrap, yield, and meeting customer demand.

The long-standing view is to improve reactivity through visual containment followed by engineering analysis to drive continued improvements. In addition to line learnings, customer returns are driven to root cause analysis and corrective actions to prevent recurrence. With anywhere from 2-8% false reactivity, discerning data and driving improvement is becoming very challenging due to the effort needed to get the data to steer improvements.

Figure 5 shows a typical fault tree assessment for a mechanical dicing defect and all inputs that factor into the manufacturing process step that can create cracks and chipping. It is important to target improvements from a design standpoint that limit interactions in the dicing street that lead to chipping, peeling and cracking of circuits. Having a solid design and manufacturing feedback loop as part of the design process is critical to long term success in reductions.

The final front for improving visual inspection is tied to innovation in dicing technologies. Advancements in this area will be especially advantageous as copper densities increase, and chips become smaller and thinner. Many new technologies exist that could improve the efforts in getting to the next step. These include stealth dicing, Mahoh dicing, plasma, and ablation equipment, which are all starting to be utilized more and more. The downside to implementing any new technologies is the expense involved in implementing and developing them into a manufacturing system. However, weighing the cost to implement new technologies with the cost of handling returns and customer dissatisfaction are what should propel the selection, and ultimately will lead to adoption of the new technology. Once use of the new technology is underway, the impact should carry across the industry as competition will drive quality sameness and improvements to gain business wins in the long run.

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Future path needed

For a successful drive to zero defects, significant shifts are needed in today's manufacturing processes. Three key changes are recommended to make step function strides in defect elimination.

Step 1. Step 1 is elimination of traditional mechanical dicing. In our industry, we spend significant cycle time and yield to screen for chipping and wafer damage. New technologies will significantly minimize this issue. This includes any of the new laser- or plasma-type dicing technologies available. These technologies eliminate the mechanics of abrasive dicing and replace today's aggressive process by eliminating failure modes and processing problems that must be screened.

Step 2. Step 2 is to eliminate the automated optical inspection process that typically follows dicing today. This process, with implementation of new dicing technologies, becomes redundant

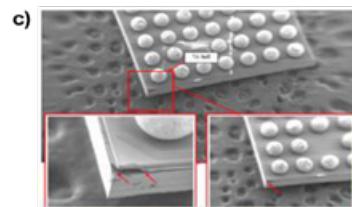
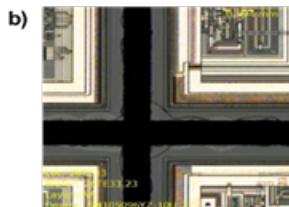
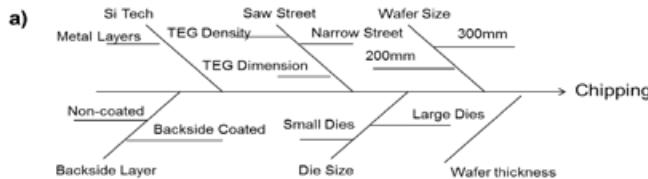


Figure 5: a) Fault tree for chipping factors; b) Common edge chip; c) Corner crack examples.

with respect to any final inspection process. Keeping this process in place without the need for mechanical dicing screening just adds unnecessary cost to the final product.

Step 3. Step 3 is to strategically implement a final inspection capable die attach or tape and reel process to successfully screen parts for issues encountered during die pick processing. In general, die are processed without issue during the full front-end-of-the-line (FEOL) flow only to be damaged during the die pick process. Once this process is complete, detection capabilities today are limited. Implementing visual inspection at this point in the process with a control system to flag lots that have pick issues or trigger limits puts a system in place to control and prevent the customer from receiving damaged parts.

Summary

A drastic change is needed in the semiconductor back end assembly flow. With today's push toward higher resolution images, today's processes are creating cases where overkill and dispositions are becoming a way of life for the back-end-of-line (BEOL) assembly areas.

This trend cannot continue long term, as fundamental changes with the dicing processes and technologies used continue to improve. This article discussed the use of new dicing technologies and proposed the elimination of long-standing expensive inspections that still typically do not prevent or contain damage created at the pick processes downstream. The key to solving the challenges is to fix these chipping issues, and direct process controls and containment procedures at the die attach and tape and reel level to detect out of control set-ups and pick issues during processing.

Our collective goal is to eliminate chipping at the source and redirect the focus of long-standing inspections to stop and contain downstream processes. If we do that, we can resolve the many "dppm" issues our industry experiences today, which are where the majority of the challenges arise when customers raise the flag.

Reference

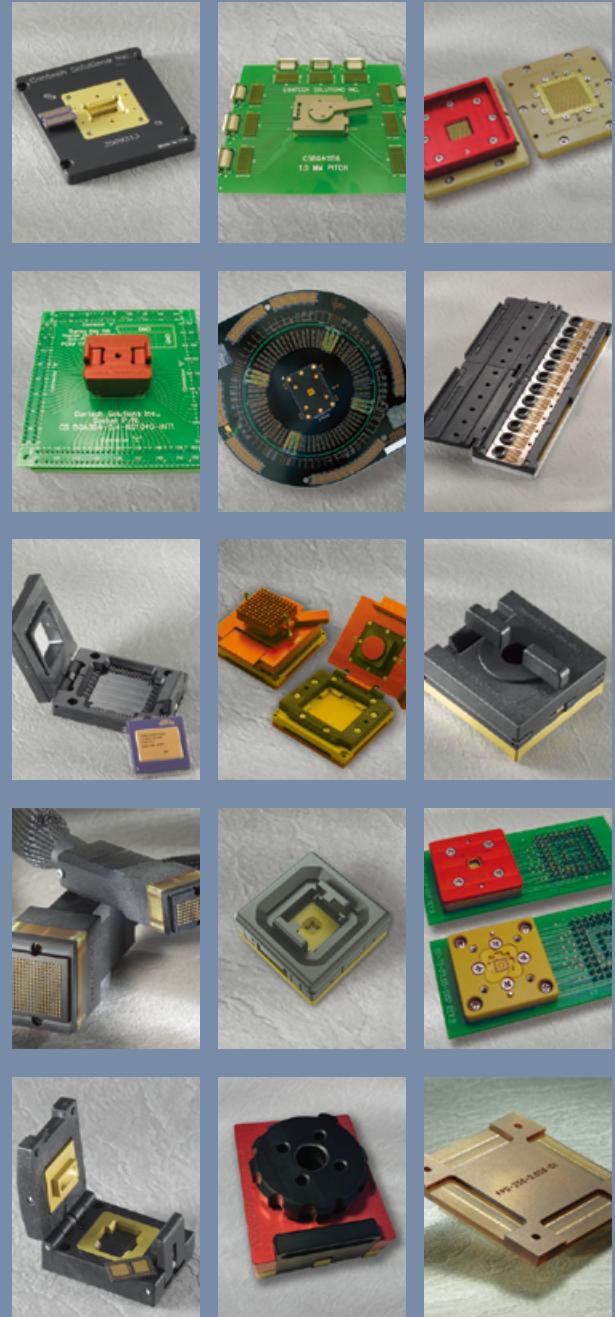
1. M. Todd Wyant, "Wafer chip-scale package cost reductions," Mar/Apr 2015, *Chip Scale Review*, Vol. 19 No. 2, pp. 54-56.

Biography

Todd Wyant earned a BSME from Purdue U. in Mechanical Engineering and a Six Sigma Black Green Belt from AIT; he is the Manufacturing Technology Manager at Texas Instruments; email m-wyant@ti.com



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Effective, scalable EMI protection for semiconductor packages

By Xinpei Cao, Jinu Choi, Junbo Gao, Dan Maslyk, Andrew Sun, Qizhuo Zhuo [Henkel Corporation]

The connectivity of everything and growth of the Internet of Things (IoT) have fueled the massive expansion of wireless, memory and data processing components, enabling consumers to enjoy historic levels of convenience, connection and control. With an increase both in the quantity and functionality of these radio-frequency (RF) emitting devices alongside their miniaturization, however, comes the need for more effective isolation to protect against electromagnetic interference (EMI) from other components in close proximity, as well as within devices that contain multiple chips such as a system-in-package (SiP) device, for example.

To be sure, there is now greater integration at the package level than ever before. Devices have much smaller and thinner profiles to accommodate shrinking end-product dimensions and it is not uncommon to have chips with different operating frequencies within the same package. Without segregation of wireless-enabled devices, unwanted cross-talk among components can cause electrical performance degradation and/or failures. Therefore, to ensure functional reliability, it is essential to address electromagnetic compatibility (EMC) through the elimination of noise at the component level.

Conventional solutions for EMI shielding

Historically, EMI shielding has been achieved through the use of metallic cans that cover a component or an assembly and attach to grounding pads on the substrate (**Figure 1**). However, with today's high-density designs dictating thinner, smaller components placed within tighter dimensions, conventional metal enclosures are not practical for many applications due to their size and the board layout restrictions required to accommodate them.

Miniaturization has, therefore, driven the use of package-level solutions such as physical vapor deposition (PVD) – also known as sputtering – to deposit metal coatings on package exteriors for interference protection. PVD, though, is not without its shortcomings in terms of

processability and cost. It is well understood that this technique has operational challenges that include surface treatment requirements, limited material selection, low units per hour (UPH) rates, stringent maintenance, a large equipment footprint, and high costs. Until recently, however, coping with PVD's drawbacks have been the tradeoff for its thin EMI protection. And, while PVD offers external package shielding to protect against outside interference, it obviously does not prohibit cross-talk within multi-chip devices.

Next-generation EMI shielding developments

To tackle the industry need for thinner, more adaptable EMI solutions with greater process flexibility, two new material technologies have been developed. The first is a conductive, silver-based ink platform that

is applied via spray-coating using readily-available spray technology, and the second is a conductive paste solution that is used to effectively isolate chips housed within the same device. The sections below discuss conformal coating of spray-coated metal inks and high-viscosity compartmental shielding paste.

Conformal coating spray-coated metal inks. Two key elements of the conformal coating of spray-coated metal inks are (A) processing and (B) performance as discussed below.

(a) Processing

Compatibility with any commercially available spray technology makes the new metal inks extremely versatile, allowing for cost-effective deployment within manufacturing operations that may already have spray technology onsite, can easily and

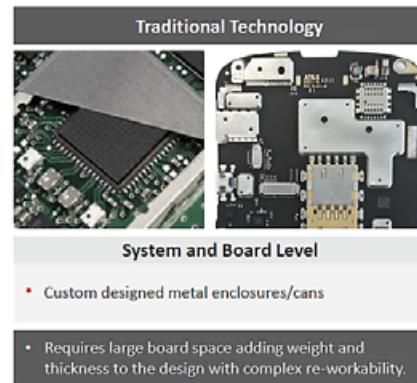


Figure 1: Traditional metal cans enclose components to protect against electromagnetic interference.

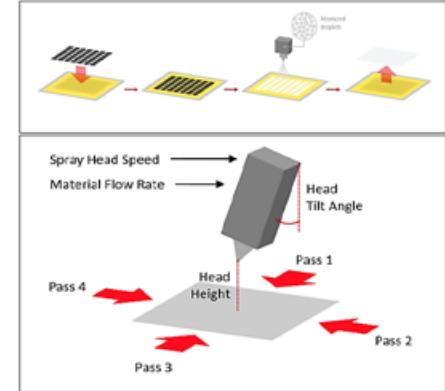


Figure 2: Component configuration and spray coating of new EMI shielding conformal coatings.

Material Name	New Conformal Coating Metal Ink
Technology	Electrically Conductive
Application Method	Spray
Volume Resistivity ($\Omega\text{-cm}$)	7.9×10^{-6}
Coating Thickness Range (μm)	3 ~ >40
Viscosity, ξ_{rpm} (cps)	550
Thixotropic Index	1.3
Curing Temperature and Time	175°C, 1 hour, in air
Far-field Shielding Effectiveness (dB)	90 with 3-5 μm thickness
Adhesion on EMC, Cu (ASTM D3359)	5B (0% peel)

Table 1: Material properties of the conformal coating metal ink as tested.

affordably acquire a system or partner with a third party that provides spray coating services. Processing finished components is simple and allows for high throughput with multiple parts being processed in parallel.

Prior to application of the coating, singulated packages are placed on a carrier in a configuration with a pitch to package height ratio of 1:1. The spray head then makes four tilted angle passes (Figure 2) so that coverage of all package sidewalls and the package top is thorough for optimal EMI protection.

(b) Performance

Recently, testing to evaluate the coating quality, adhesion performance and reliability of one of the new conformal coating metal inks was conducted. The work also compared the far-field and near-field shielding effectiveness of one of the series of new materials to that of conventionally sputtered (PVD) materials. The volume resistivity of the tested material is $7.9 \times 10^{-6} \Omega\text{cm}$, which is equivalent to pure copper and significantly higher than traditional organic inks. Properties of the new metal ink are shown in Table 1 and the performance analysis follows.

The evaluated conformal coating material as applied via spray atomization (Figure 2) showed full, uniform coverage of the package top, sidewalls and corners. A thickness ratio of 1:0.5-0.6 was achieved for the top to sidewall thickness with a package pitch-to-height ratio of 1:1. When pitch between the packages was increased, the coating thickness ratio increased slightly to a ratio of 1:0.7-0.8. The uniformity and ability to achieve full coating in a very fine layer also allowed good visibility of laser markings. Unlike PVD, with the conformal coating materials, no treatment is required to enable adhesion compatibility with the molded package. As tested, adhesion of the sample material using the ASTM D3359 standard yielded excellent results with no delamination on epoxy mold compound or copper surfaces. The material showed a 5B adhesion rating at 5 μm and 10 μm after the pressure cooker test (PCT) and after high-temperature storage (HTS) analysis, as well as for the moisture sensitivity level 3 (MSL3) testing for up to 1,000 cycles at -40°C to 150°C.

In addition to adhesion and reliability testing, the metal ink material was evaluated for far-field and near-field shielding effectiveness and compared to other materials. Using standard testing methods for the measurement of relative permittivity and magnetic permeability of solid materials at microwave frequencies and shielding effectiveness of planar materials, the coated test vehicles were evaluated for far-field bulk shielding effectiveness. With a coating thickness of

3 μm -5 μm , it was demonstrated that the material can deliver far-field EMI shielding of up to 90dB at 1.6GHz, which is higher than that of conventional organic-based inks (Figure 3). Near-field testing was also conducted according to the IEEE 299 standard in order to measure the shielding performance at the package level. With a top coating thickness as low as 5 μm , the tested material was shown to have similar or higher shielding effectiveness as PVD at a comparable thickness (Figure 4).

While the performance of the tested conformal coating metal ink has proven its EMI shielding effectiveness, the scalability and cost-effectiveness of the application process and associated equipment is also appealing. Implementation of a traditional PVD line requires significant floor space and can cost as much as several million US dollars, whereas the spray-on coating can be incorporated using affordable equipment at a fraction of the cost and requiring significantly less floor space. So, for a



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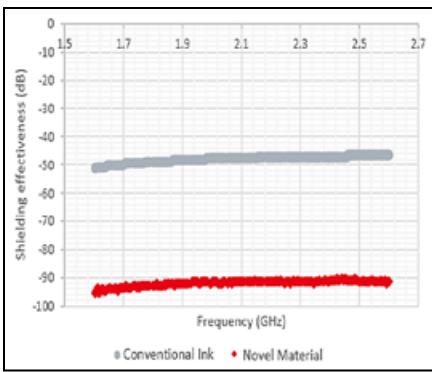


Figure 3: Far-field shielding effectiveness of new conformal coating metal ink vs. conventional ink at 1.6~2.6GHz.

solution with equal or better performance than PVD, the operational costs are significantly less (**Table 2**).

High-viscosity compartmental shielding paste. For some package configurations, where multiple chips of varying frequencies are housed within the same device, external EMI protective coatings alone may not deliver adequate protection as cross talk can occur between chips inside the package. In this situation, isolating certain die within the package may be advantageous and here, too,

new material technology has been developed to facilitate effective in-package segregation to minimize the impact of EMI. The solution, referred to as compartmental shielding, utilizes highly-conductive, highly-flowable materials to separate active, RF-emitting chips from one another.

Processing is simple and effective (**Figure 5**): Once the target dies are selected, a narrow channel is routed through the

molded package using precise laser cutting techniques. The trench is then filled with the new compartmental material via jet dispensing. Because the cut channels often have high aspect ratios (X dimension/Y dimension) ranging from 5:1 up to 10:1, filling is challenging and requires simultaneous air displacement and paste deposition to optimize EMI shielding performance through void minimization. Adhesion and shrinkage

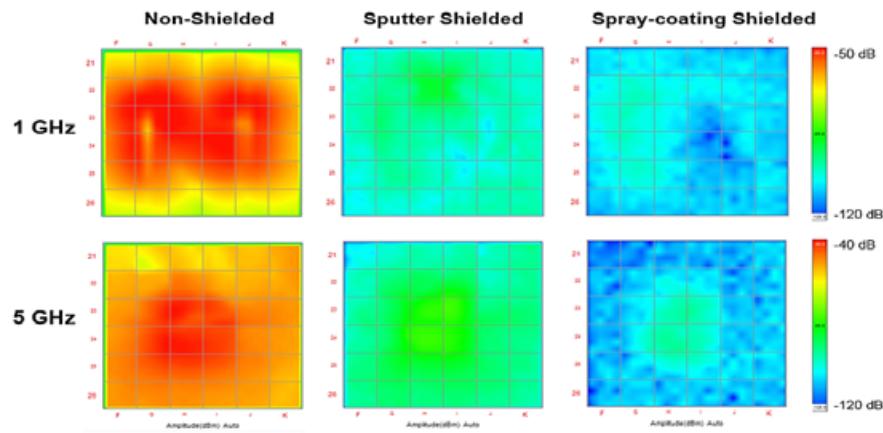
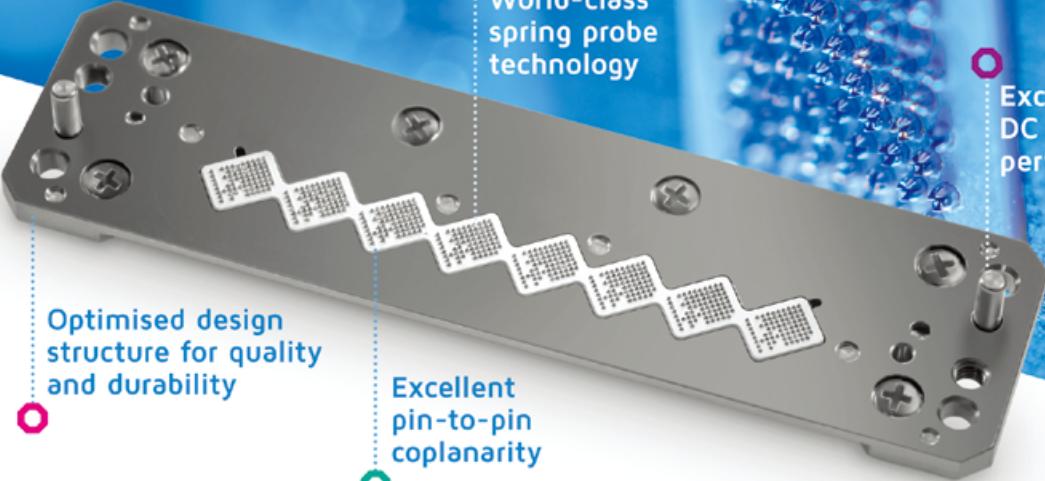


Figure 4: Near-field shielding effectiveness of new conformal coating EMI protection materials as compared to sputtered materials and non-shielded samples at 1GHz and 5GHz.

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Key Requirements	PVD/Sputtering	Spray-Coated Metal Ink
Footprint	Large	Small
Total Cost of Ownership	Extremely high	Up to 60% lower
Throughput (UPH)	Moderate	Up to 400% higher
Required CAPEX	Extremely high	Up to 90% lower
Process Flow	Complex	Simple
Deployment Scalability	Low	High
Required Coating Thickness	3~6 um	3~6 um
Laser Mark Visibility	Good	Good
Coating Uniformity	Good	Good
Coating Structure	Multi-Layer	Single or Multi-Layer
Top:Sidewall Thickness Ratio	1:0.4~0.5	1:0.5~0.6

Table 2: Operational and performance comparisons of conformal coated metal ink vs. PVD (sputtering).

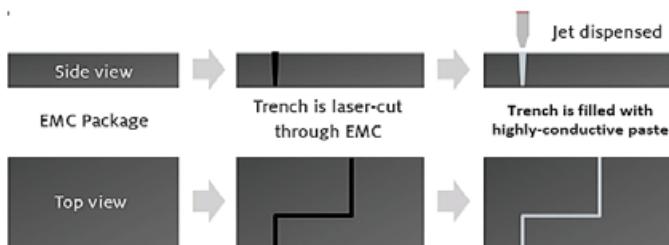


Figure 5: Compartmental shielding for in-package EMI chip segregation.

properties of the material are also critical so that, once cured, the paste adheres to the floor and trench sidewalls with no separation. Highly flexible, the newly-developed compartmental materials are compatible with conventional metal cans, organic metal inks and the new conformal coating metal inks.

Summary

The speed at which RF devices are being developed and deployed is staggering, and the challenge to effectively protect them from EMI interference while accommodating the reduction in package sizes and increase in functionality has become more pronounced. New technologies such as conformal coating metal inks – which have been shown to outperform traditional conductive inks with 80% higher shielding effectiveness – and compartmental shielding pastes will be essential for the future of a more reliably connected electronic ecosystem.

Biographies

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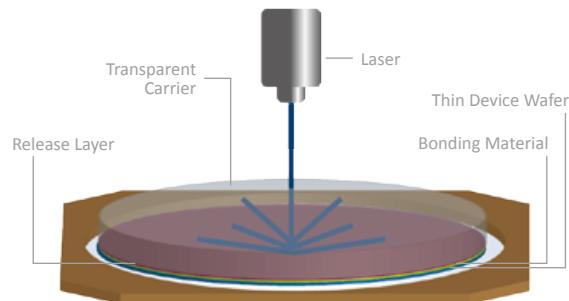
Qizhuo Zhuo received his PhD in Polymer Science from U. of Akron and is a Technology Manager at Henkel Corporation.



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TECHNOLOGY TRENDS

AI/ML accelerate transition from standard components to application-specific, system-level solutions

By Herb Reiter *[eda 2asic Consulting]*

The recent Design Automation Conference (DAC) as well as SEMICON West, confirmed that machine learning (ML) and artificial intelligence (AI) are fast emerging twins and will be an important core technology to serve a wide range of new “Killer Applications” in the rapidly changing markets for semiconductors.

IC revenue growth, driven by smartphones, has significantly slowed. So far, IC vendors couldn't identify a high-growth AND high-volume market to replace smartphones as industry drivers. However, many lower volume, customer and application-specific opportunities for smart electronic devices that can increase entire systems' values, are emerging. Most of these new opportunities have several important things in common: 1) They interface with the real world through sensors and actuators, 2) need to transfer some of the captured data efficiently to a hub or the cloud, 3) need to be smart and “learn on the job,” 4) should be remotely reconfigurable, and 5) can only consume very small amounts of power. Looking at these criteria, my mind tells me that a combination of AI/ML and multi-die ICs, containing heterogeneous functions, should be a pretty good fit for serving a broad range of these low/lower volume opportunities and give our industry a broad range of new “Killer Apps.”

Packaging opportunities with AI/ML technologies

Semiconductor suppliers that want to profit from the many opportunities AI/ML can serve need to develop hardware platforms with lots of compute power, large amounts of memory, add heterogeneous functions to interface with the real world, and meet stringent power and size constraints. Implementing all these functions into single-die system-on-chip (SoC) devices isn't economical, especially not for low volumes. The traditional way of using multiple single-die SoCs, mounted on printed circuit boards (PCBs), will not meet

the required performance per Watt, nor allow attractive form factors.

Due to the progress advanced IC packaging has made in recent years, it's now faster, easier and more cost-effective to combine logic, memory, analog, RF, MEMS, sensors, etc., at the die-level in an IC package, called system-in-package chips (SiPs) or 2.5/3D ICs. They offer modularity and make it much easier, faster, and more practical to customize and/or differentiate a multi-die solution.

Adjusting to new ways of serving many new markets

If you have ever experienced a line down and missed a revenue target by millions of dollars because you couldn't get a 10-cent component on time, you'll value higher levels of integration. Just like ASICs helped customers to integrate more digital functions, multi-die ICs will take the integration benefits a big step further towards system integration. Today's multi-die ICs include logic, memory, analog, RF, MEMS, image sensors, even passive components (RLC) and antennas. Other functions are in development.

No single semiconductor supplier has the resources to serve all these diverse market requirements well, nor economically. The demand for continued specialization further increases the need for coordination and cooperation across the entire semiconductor

supply chain. SEMI, the manufacturers industry organization, has demonstrated for many years that better worldwide cooperation, agreeing on best practices and standards, defining hand-off points and responsibilities for all manufacturing steps, offer significant benefits. On the design side, EDA experts have worked for about 20 years with wafer foundries, jointly developing process design kits (PDKs) and die-level reference flows to enable designers to fully utilize the capabilities of every new wafer processing technology. This strategy enabled the rapid growth of the fabless/foundry business model.

As more of the IC and system value creation is now moving from individually packaged die, to integrating heterogenous functions into small and low-power (sub) system solutions in a single IC package, it became mandatory to expand the focus of EDA tools from (silicon) die design, to optimizing dice-package-board-system interactions. To achieve this, EDA design tools vendors need to broaden their focus to also include material suppliers, IC assembly/test houses, PCB and system manufacturers, and jointly develop assembly design kits (ADKs), that contain accurate data about package and PCB materials characteristics, capabilities of manufacturing and test equipment, as well as other relevant advice and data. In addition, data exchange

STRATEGIC ASSOCIATION PARTNERS

Global Supply Chain Collaboration

Electronic System Design Alliance

Figure 1: SEMI and its Strategic Alliance Partners.

formats, hand-off/sign-off criteria between the different design and manufacturing steps and reference flows are needed for broad adoption and profitability of this new “system-in-package business model.”

SEMI recognized the need for broadening its traditional scope into dice-package-board-system design and won the Electronic System Design (ESD) Alliance (with members like ARM, Ansys, Cadence, Mentor, a Siemens Business, Synopsys, and others) as an additional Strategic Alliance Partner (**Figure 1**). Now they jointly span the entire supply chain from planning and design to manufacturing and test of system-level solutions.

Examples for highly visible advanced packaging solutions

AMD, Broadcom, DARPA, Hynix, IBM, Intel, Marvell, Micron, Nvidia, NXP, Qualcomm, Samsung and others have already demonstrated the power of multi-die ICs and advanced packaging technologies. However, these pioneering projects required lots of design expertise, manpower,

long development times and enormous coordination efforts. To allow more companies to follow, we need better supply chain coordination, more user-friendly dice-package-board-system design tools, further advances in materials, equipment and manufacturing flows, as well as economies of scale to reduce and eventually eliminate the currently high entry barriers.

Summary

Every new semiconductor technology I helped to introduce – from PLDs, ASICs and application-specific standard products (ASSPs), to today's multi-billion gate SoCs and SiPs – stressed the suppliers' and customers' ability to invest significantly. In addition, the needed employees in both camps had to contribute a lot of their time and the willingness to learn how to make these new technologies successful. Having organized very large-scale and disruptive engineering training efforts before, I recommend starting with small teams of motivated experts all across the supply chain, charter them to develop solid ADKs,

reference flows and a compelling degree of design and manufacturing automation, BEFORE training thousands of design and manufacturing engineers on all the multi-physics and multi-dimensional aspects of multi-die ICs and system-level integration.

I already see several ongoing development efforts in exactly the direction outlined above and hope that the Strategic Alliance Partners, together with their member companies, will broaden these efforts, encourage utilizing AI/ML also for automation of design and manufacturing process steps, and of course increase industry-wide cooperation to further grow semiconductor revenues and profits for our \$2Trillion EcoSystem (**Figure 2**).

Biography

Herb Reiter received his MSEE and an MBA degree in Austria, another MBA at San Jose State U. and attended 40+ continuing education courses at Stanford U. He is the founder and President of eda 2 asic Consulting; email herb@eda2asic.com

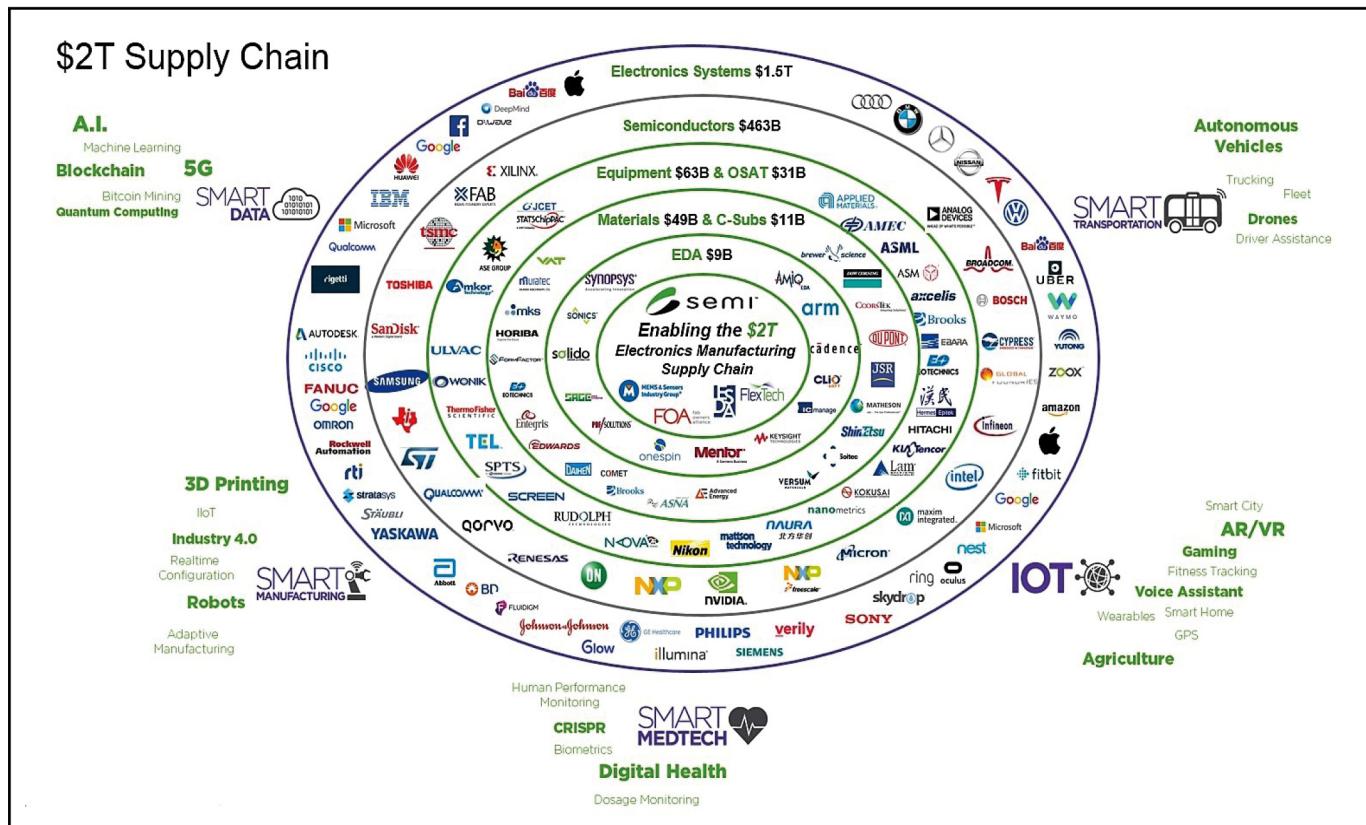


Figure 2: The \$2T Electronic Systems Supply Chain. SOURCE: Dave Anderson, President SEMI Americas, Semicon West, 2018.

Surviving the three phases of high-density advanced packaging (HDAP) design

By Keith Felton [Mentor, A Siemens Business]

Cost, risk, and the limitations of monolithic scaling are driving growth of multi-die (heterogeneous) advanced integrated circuit (IC) packaging solutions, creating opportunity throughout the design process. These high-density advanced packages (HDAP) are driving a convergence of the traditional IC design and IC package-design worlds.

Emerging technologies, such as fan-out wafer-level packaging (FOWLP), silicon interposers, chip-on-wafer-on-silicon (CoWoS), and wafer-on-wafer (WoW) require design teams to work together to optimize the entire system, not just the individual elements. These new technologies lead to new challenges that companies and design teams must face and overcome. Such challenges typically fall into three categories: increased engineering

costs, manufacturing delays, and functional failure of devices (**Figure 1**). Survival of these three areas requires a process transformation that typically falls into three areas discussed in the sections below.

Validation and verification. 1) Layout-versus-schematic (LVS)/layout-versus-layout (LVL) of final 2.5D/3D assembly and individual substrates; 2) Multi-substrate electrical extraction and analysis; and 3) Electrical modeling.

Manufacturing-focused implementation. Database capacity and tool performance; 2) Robust, in-tool shape processing (area fill and planes); and 3) Accuracy and quality of GDS output.

Multi-substrate/devices architectures. 1) Connectivity/interface planning across substrate boundaries; 2) 2.5D/3D stacking,

device transforms and scaling; and 3) Management of heterogeneous data and formats.

While the order of these three may seem backwards (i.e., reverse order), this is typically the order in which design teams approach HDAP challenges, i.e., start with extensive validation and verification of the completed design before it moves to fabrication and assembly. This initial approach does not disrupt the current design process or methodology, but ensures that problems/issues are found before manufacturing. Once this is mastered, take the knowledge of what implementation related issues are consistently found and put methodologies, processes and tools in place to mitigate them. Finally, look at the architecting and planning process as part of a left-shift strategy that drives the process with a validated, optimized concept that will greatly reduce implementation and final validation/signoff surprises. The result will be an optimized and predictable development schedule without any significant late stage engineering changes that could be caused by unseen design issues.

Phase 1: validation and verification

HDAP packages typically contain multiple devices and multiple substrates, often stacked, and typically designed by distinctly separate designers and teams who may, or may not, interact well.

A common theme across these packages is they all present some unique challenge to traditional design tools and methodologies. Many of today's packages incorporate some element of multiple substrates or multiple devices to deliver solutions for system scaling. They bring a number of potentially new

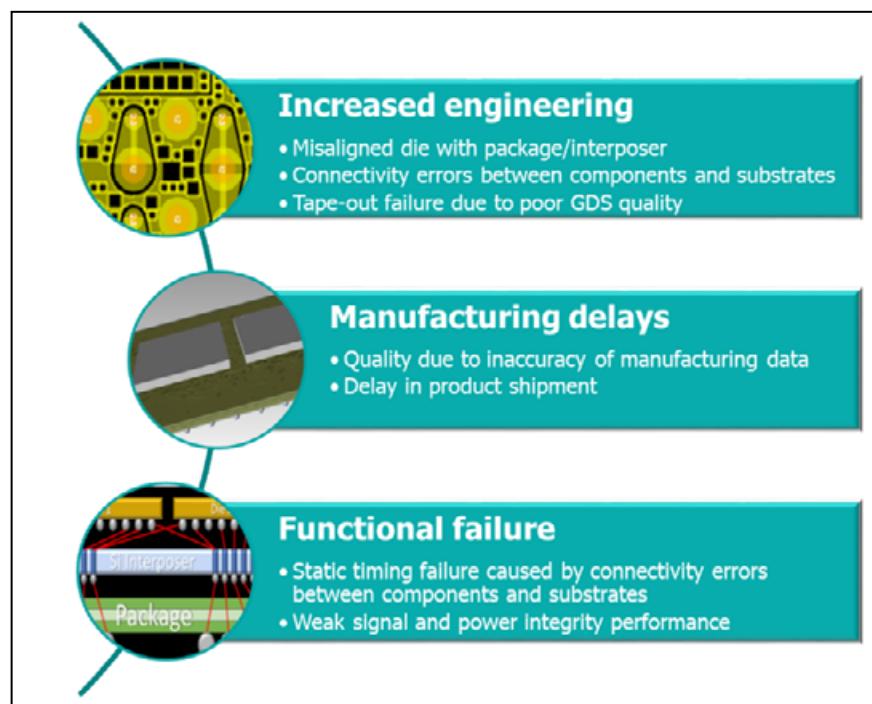


Figure 1: The three challenge categories of high-density advanced package (HDAP) design.

challenges to the design team, such as connectivity planning and coordination of high-performance interfaces across substrate boundaries, device and substrate stacking ensuring 3D interoperability, electrical extraction and analysis of the completed assembly, and lastly, mask-level verification of individual substrate and the completed package assembly. While size and scale may vary across these packaging technologies, there are challenges at both ends of the spectrum.

With explosive growth of FOWLP, there is increasing use of “IC”-like processes and tools that necessitates a higher data resolution and design rules checking (DRC) accuracy for smaller feature sizes. GDSII quality and performance on non-Manhattan geometries can also be an issue for traditional packaging tools. When these multiple designs are finally integrated together, a number of system-level verification and validation steps are required to ensure that they are connected together correctly from a logical and physical perspective (**Figure 2**). Ideally, the solution should be minimally

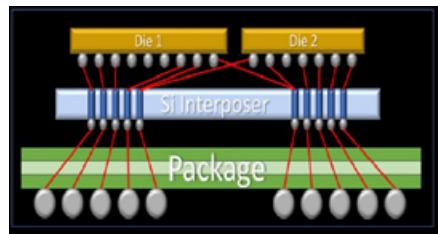


Figure 2: Three levels of substrate from different design teams.

disruptive to the overall design process while providing comprehensive DRC, LVL, and LVS of individual components, as well as the final, assembled package. The solution also needs to be capable of managing the complexity and scale of such a fully-integrated 2.5D/3D assembly where die pins can equal/exceed 40,000, and total interposer pins can easily exceed 250,000. Such levels of validation and verification are commonplace in chip design, but a new phenomenon for package designers.

The technology needed to perform the critical checks discussed above exists today, but has to be integrated

into the package design flow and process and ideally be capable of providing results that can be displayed with the packaging design tools. Typically, the checks required fall into two categories: physical geometric and connectivity. For the physical, or LVL, the focus is on analyzing and verifying alignment, scaling, and overlaps between devices and substrates, as shown in **Figure 3**.

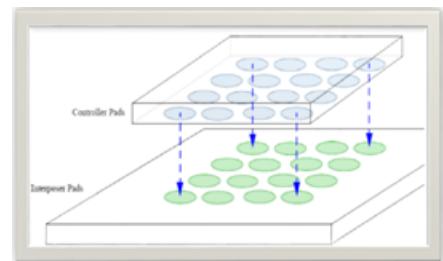
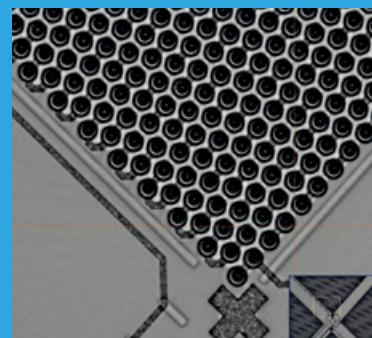


Figure 3: Layout-versus-layout (LVL) checking of die to interposer.



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Connectivity verification between all components and substrates, or LVS, verifies the connectivity between connected shapes, mismatch connections and the locations of electrical pins as shown on the simple example below (**Figure 4**).

The typical process is to validate individual components (die, interposer, package) standalone using their process-specific requirements,

then define and check the 3D assembly of the interfaces between the components, preferably using a single rule deck or assembly design kit (ADK).

Assembly verification can be simplified when we realize that you do not need to check every geometry in every die. Each individual die will already have been checked for its target foundry compliance with respect

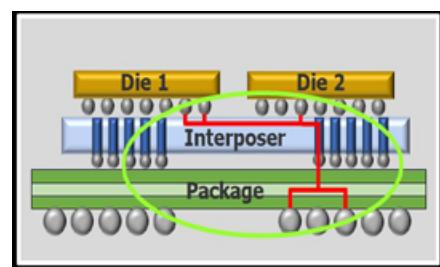


Figure 4: Layout vs. schematic (LVS) across the package system.

to DRC and LVS. All we really need to do is check the interactions between the components. That is not to say this is trivial; in some cases, this can require extracting several layers within each die to evaluate their impact. Regardless of the configuration, it requires that the tool understands the layering per die and per placement. This includes the ability to distinguish between two die with the same layer name, i.e., RDL1. The key needs for this sign-off level of verification are the definition of the assembly stack-up of the components and a “golden” LVS source system net list.

With the approach described above, you start by importing the physical design data – typically manufacturing GDS. You will also independently import the source net list of the entire system, which in itself can be a challenge, but we will address that later. You will also need some instruction as to how everything is assembled, as well as the foundry/outsourced semiconductor assembly and test (OSAT) process-specific rules. The verification tool runs and compares the data—either you get the smiley face that everything is good, or an error report, ideally one that can highlight and then cross-probes back to the original layout database.

Phase 2: multi-substrate/devices implementation

Typically, design teams start with using their existing legacy design tools and processes, which are normally great for organic plastic ball grid array (PBGA) designs, but with HDAP, they really start to struggle or just fail. One of the areas where traditional tools fail is around the insertion or substitution of shapes into the output files on account of a lack of support within the layout tool, such as mesh



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pads and graduated degassing. Another area of failure occurs when the design will pass DRC within the layout tool, but fail once the outputs are checked with the 3D verification/sign-off tool (**Figure 5**). This can be due to a number of factors, but typically includes one or more of these: 1) weak area fill algorithm; 2) lack of arc constructs; 3) quality of graphic database system (GDS) output; 4) paths vs. polygons; 5) polygon merge, and finally, 6) lack of database accuracy or resolution in the layout tool.

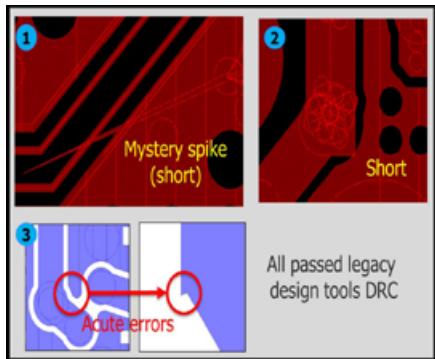


Figure 5: Typical areas of weakness of legacy design tools.

The problems described above bring into play a work-around flow that creates a discontinuity between the layout database and what is actually manufactured (**Figure 6**). Such post-design GDS edits rarely, or never, get back-annotated to the layout database, so any analysis (SI/PI, thermal, etc.) results must be considered

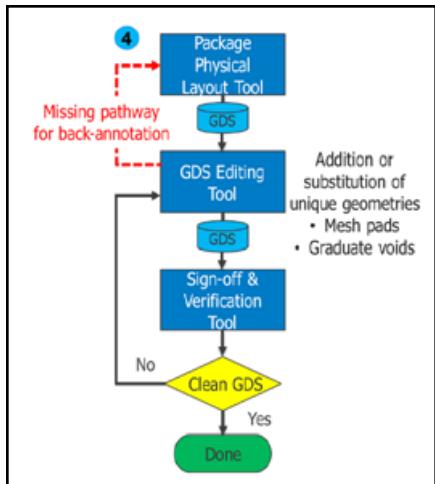


Figure 6: Graphical database system (GDS) work-around flow.

suspect as they are typically executed using the layout database.

In order to survive Phase 2 of HDAP design, users need a design solution that, at a minimum, has the following characteristics:

- Enables design in a fully integrated 3D environment;
- Provides capacity and performance for very high pin count designs: at least 250K+;
- Has advanced area fill algorithms with accurate representation of nanometer geometries;
- Support for graduated degassing, density, acute angle and stress relief checks; and
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Phase 3: Multi-substrate/devices architectures

As discussed at the beginning of this article, the third phase, while typically adopted last, is in fact

the most impactful and beneficial for any heterogeneous advanced package design. Think about the characteristics of today's designs and the interdependency between devices

and substrates. Consider a critical element like high-speed interfaces or power delivery and how a decision on one substrate can have a ripple effect and impact adjacent substrates, or the whole system. A great example is allocation of timing budget. What makes this additionally challenging are different databases, manufacturing processes, design tools, format, etc. The basic needs of heterogeneous architectural design and planning can be defined as:

- Accurately capturing all the data, and defining assembly stack and device relationships;
- Plan and prototype connectivity across substrate boundaries – typically focused on high-performance interfaces; and
- Communicating design intent to other tools for detailed implementation.

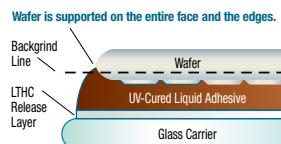
These capabilities need the ability to manage different combinations

Figure 7: Heterogeneous packaging interdependencies.



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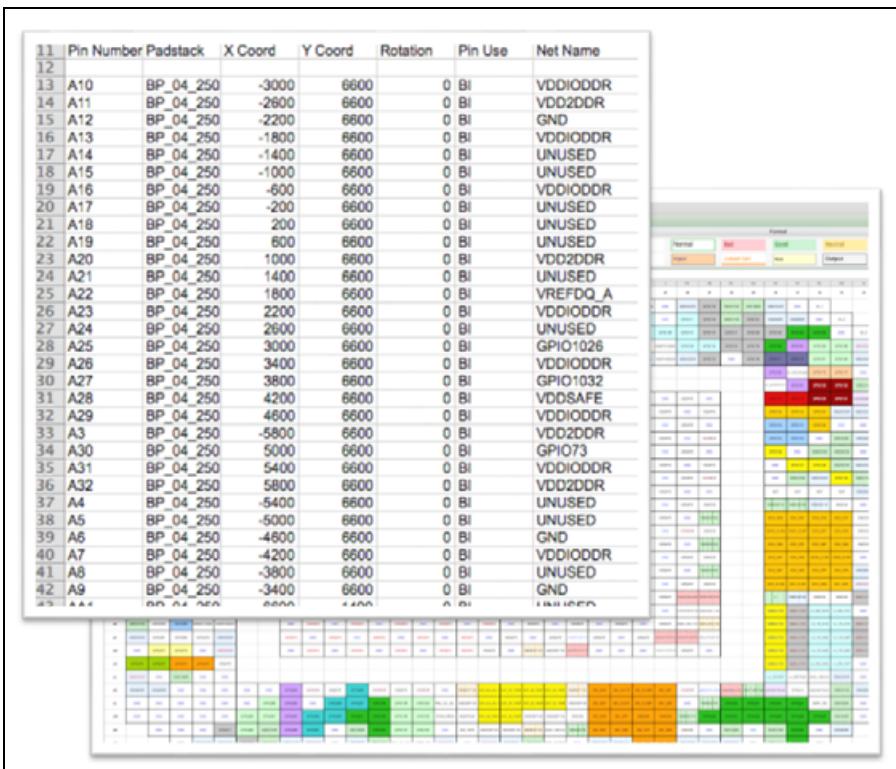


Figure 8: Typical planning approach with tables/spreadsheets.

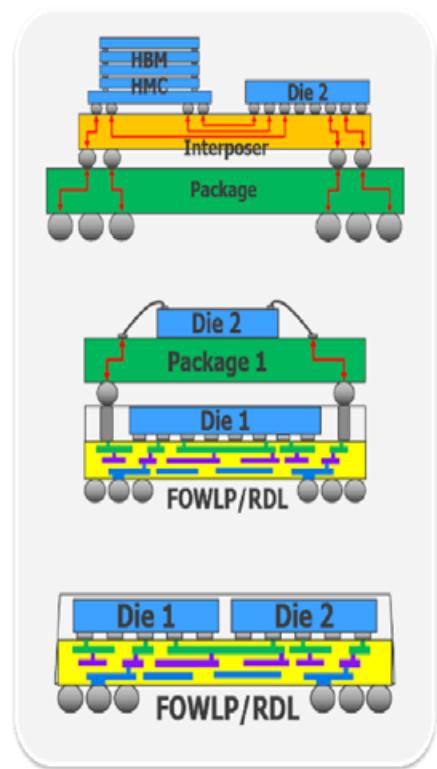


Figure 9: What technology is best for my design?



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of substrate scenarios, such as die-interposer-package, or die-package-PCB (**Figure 7**). Most package design teams rely on spreadsheets and/or ASCII files, while some develop internal tools or scripts.

In the case of die/package planning, we typically think about pin and net assignments and their impact on routing and layer count (cost), but there's more to consider:

- SPG ratios and patterning to ensure quality return paths and power delivery;
- Route planning – escape sequencing, layer assignments, and feasibility;
- PCB-driven assignment, or pin compatibility with the previous generation; and
- Differential pair management and propagation.

With spreadsheets as the primary exchange mechanism (**Figure 8**), how are the above considerations communicated? Will it scale with increasing complexity and pin counts? What will the interaction look like with geographically diverse teams or external resources? And how long is the cycle time for feedback?

Summary

A true dynamic, heterogeneous prototyping and planning capability will accelerate your design process, prevent implementation mistakes, and enable system-level optimization and trade-offs. The ideal methodology should also enable early static timing analysis (STA) and LVS of different scenarios, optimize a die for multiple target packages, or optimize a package for multiple target PCBs (**Figure 9**). Heterogeneous prototyping and planning enables:

- Coordination and management of multiple substrate design in one environment;
- Evaluation of different packaging technologies or schemes;
- Planning, management, and visualization of system connectivity across IC-interposer-package-PCB;
- Rapid evaluation of electrical and thermal performance;
- Generation and management of a hierarchical system net list; and
- Facilitation of the collaboration and communication across geographical/department boundaries.

Biography

Keith Felton is the Xpedition IC Packaging Solutions Manager at Mentor, A Siemens Business; email Keith_Felton@mentor.com

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INDUSTRY NEWS

The International Wafer-Level Packaging Conference (IWLPC) is pleased to announce the support and endorsement by the IEEE Electronic Packaging Society (EPS) and the Panel-Level Packaging (PLP) Consortium



The PLP Consortium is an international collaboration comprising 17 enterprises focused on taking production to the next level in making the transition from fan-out wafer-level packaging to fan-out panel-level packaging. Formed in 2017, the R&D consortium came together at the Fraunhofer Institute for Reliability and Microintegration IZM in Berlin—the initiator and organizer of the group. Joining the consortium are leading Subject Matter Experts and global players paving the way for research. Tanja Braun, Dr.-Ing. at Fraunhofer IZM, comments, “Today we have overcome the initial need to be evangelists for panel-level technology, and now we are facing the down to earth challenges of working on material and process optimization, standardization, and cost.”

Explore “Driving an Interconnected World” at this year’s IWLPC. Industry leaders, technologists and innovators will attend the 15th Annual International Wafer-Level Packaging Conference & Exhibition (IWLPC). Held in San Jose, CA, The IWLPC continues to be the premier semiconductor packaging conference and exhibition focused on wafer-level packaging. The conference has a rich history of bringing together attendees from over 16 countries in the heart of Silicon Valley to immerse themselves in the latest technology and business trends. This year’s conference theme, “Driving an Interconnected World,” emphasizes the growing importance of advanced wafer-level interconnect technologies to enable advanced system-level packaging solutions for applications such as, automotive, communications, and high-performance computing. The IWLPC is co-produced by *Chip Scale Review*, the leading international magazine addressing the semiconductor packaging industry, and SMTA, the distinguished global association representing electronic assembly and manufacturing professionals.

The conference comprises three key technology areas with two full days of presentations on wafer-level packaging, 3D integration, and advanced manufacturing and test. Three keynote speakers are featured on October 23 and 24. A groundbreaking panel discussion will be led by Jan Vardaman of TechSearch International, and Tanja Braun of Fraunhofer IZM. These sessions gather world-class experts and enable attendees to broaden their knowledge. The technical program includes a two-day expo where 65+ exhibitors showcase their latest technologies and products. The conference provides a collective network of over 800 industry professionals, including vendors from leading semiconductor companies, foundries, and OSATs, as well as key technology, equipment, and materials suppliers in the exhibit area. Attendees will be inspired by the quantity and quality of the featured new developments and emerging technologies.

Register today for the IWLPC at www.iwlpc.com



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Fan Out Packaging – Technology Evolution (PDC1)

John Hunt, ASE (US) Inc.
October 25, 2018
8:30am–12:00pm



www.iwlpc.com/courses.cfm#PDC1

Modeling Failure Modes for Chip package Interactions and Package Level Reliability (PDC2)

Gil Sharon,
DfR Solutions
October 25, 2018
8:30am–12:00pm



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Fan-Out Wafer/Panel-Level Packaging for 3D IC Heterogeneous Integration (PDC3)

John Lau, Ph.D.,
ASM Pacific
Technology
October 25, 2018
1:30pm–5:00pm



www.iwlpc.com/courses.cfm#PDC3

Polymers and Processes Used in Wafer Level Packaging (PDC4)

Jeffrey Gotro, Ph.D.,
InnoCentrix, LLC
October 25, 2018
1:30pm–5:00pm



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INDUSTRY NEWS

EPTC 2018 is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). It will take place December 4-7, 2018 at the Resort World Sentosa (RWS), Singapore, and will feature keynotes, technical sessions, short courses, forums, an exhibition, as well as social and networking activities. EPTC2018 provides a good coverage of technology developments in all areas of electronics packaging from design to manufacturing and operation.

Conference topics include:

- Advanced Packaging
- TSV/Wafer Level Packaging
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EPTC2018 is a major forum for the exchange of knowledge and provides opportunities to network and meet internationally renowned experts in all areas of electronics packaging from design to manufacturing and operation. In particular, this year marks the 20th anniversary of EPTC and a day of special technical presentations by invited experts has been added to celebrate the occasion.

Selected keynotes and invited presentations by leading experts include:

- Ivor Barber, VP, AMD, USA
- David McCann, VP, GLOBALFOUNDRIES, USA
- Avram Bar Cohen, Ph.D., Raytheon Corporation, USA
- Stevan G. Hunter, Ph.D., On Semiconductor, USA
- Bill Chen, Ph.D., Fellow, ASE Group, USA
- Robert Kao, Prof., National Taiwan University
- Jeffrey Suhling, Prof., Auburn University, USA
- Evelyn Napetschnig, Ph.D., Infineon Technologies
- Mr. Sam Karikalan, Broadcom Inc., USA
- Mr. Paul Werbaneth, Intevac
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For more details about EPTC2018, please visit the website: <http://www.eptc-ieee.net>.



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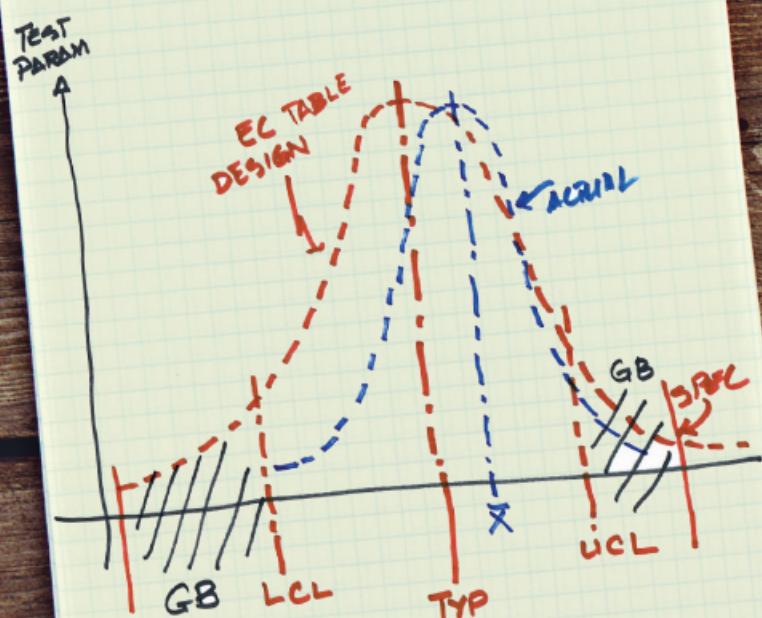
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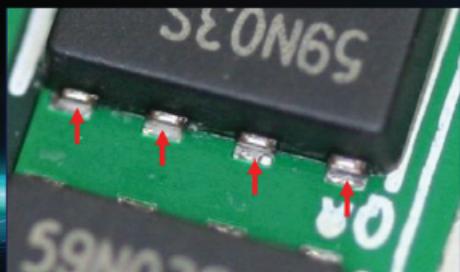
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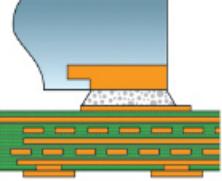
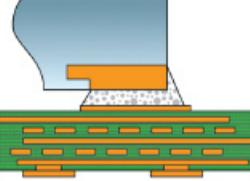
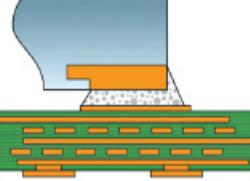
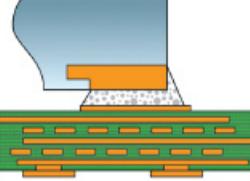
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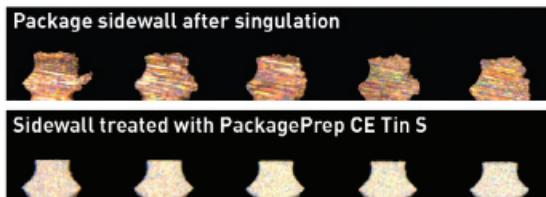


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