

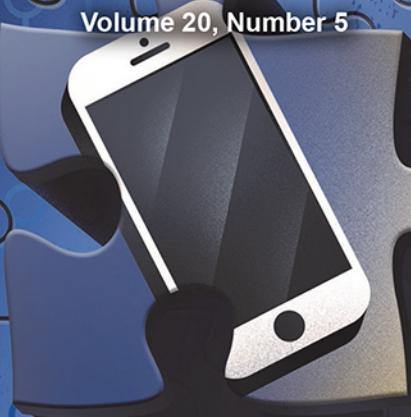
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Volume 20, Number 5

The Future of Semiconductor Packaging

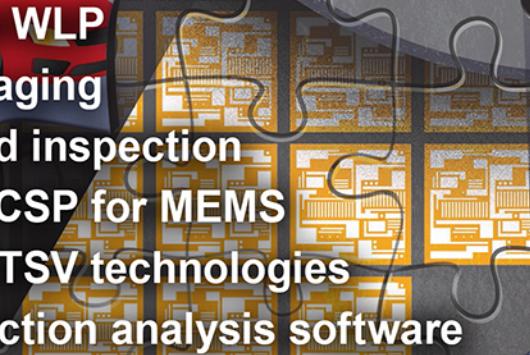
September • October 2016



Evolution of temporary bonding technology

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Thin wafer handling by temporarily bonding device wafers to a supporting carrier has been widely used for advanced packaging of high-efficiency and high-performance devices used in computing, networking, sensors and consumer electronics applications. Temporary bonding material is a significant factor in this process and has evolved substantially over the last decade to enable handling of extremely thin wafers in harsh environments during wafer processing.

Cover image courtesy of Brewer Science Inc.

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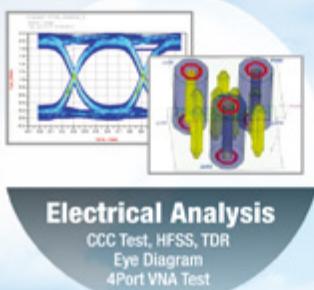
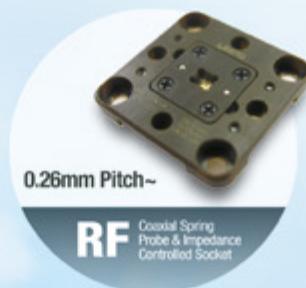
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MARKET UPDATE



Panel-level packaging: a promising market

By Santosh Kumar [Yole Développement]

Currently, there is a lot of interest in the semiconductor industry about panel-level packaging, and many players, including equipment and materials suppliers, are involved. The demand for lower cost and higher performance has driven the semiconductor industry to develop innovative solutions. One such approach is to switch from wafers to a larger panel format in order to reduce cost. At Yole Développement (Yole), analysts expect the panel packaging industry to reach US\$109 million by 2017, with a market value of US\$405 million by 2020 [1]. The panel-level package market is a competitive one, attracting many new entrants compared to existing advanced packaging market segments.

Panel-level packaging is a process in which chips are assembled or packaged at the panel level on a rectangular or square surface. The assembly process comprises the fabrication of redistribution lines, die attach, molding, and bumping at the panel level. It also includes fine-feature, next-generation substrates that require advanced tools and materials to fabricate the structural features (lines, microvias) and leverages various manufacturing infrastructures such as Si (back-end-of-line [BEOL]), printed circuit board

(PCB), liquid crystal display (LCD) and photovoltaics (PV). It pushes the limits of mature PCB and laminate infrastructure. The purpose of using a variety of infrastructures is to obtain fine features at a low cost for specific applications.

Yole has identified five key packaging platforms that can be processed on a larger (rectangular or square) surface or panel (**Figure 1**): fan-out wafer-level packaging (FOWLP), organic interposer, glass panel interposer, hybrid interposer and embedded die. Some of these advanced packaging platforms (embedded die and organic interposer) are already available on panel, while others like FOWLP and glass interposer have a strong potential for migrating to panel. In particular, the fan-out on panel platform is attracting a great deal of interest in industry from multiple players,

including equipment and materials suppliers actively working on it.

Further scopes of application for panel can be segmented into three categories defined by the required resolution. There are a number of applications that could play a part in panel's success story. High-end products, such as networks, CPUs/GPUs, field-programmable gate arrays (FPGA), and servers, will necessitate a reduced resolution of 2 μ m. For that reason, this area is likely to be dominated by 300mm lines, where the front-end is already well-established and has the line/space (L/S) capability to achieve such resolution. Midrange products, including basebands, processors, power management modules and RFICs, should be the main FOWLP target using panel and glass panel interposers, while organic interposers should be restricted to low-

Resolution trends (L/S: Line/Space): packaging area roadmap

(Source: State of Panel Level Packaging Manufacturing report, Yole Développement, November 2015)

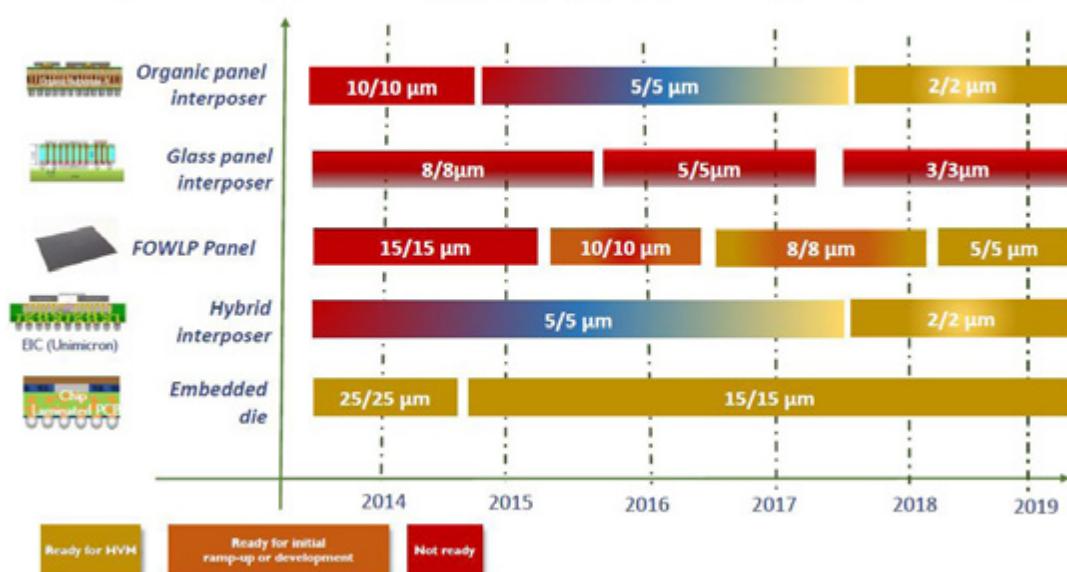


Figure 1: Resolution trends (L/S, or line/space): packaging area roadmap. SOURCE [1]

end products like mobile, consumer, WiFi, and power management.

Fan-out on panel

Fan-out on-panel-level packaging could result in a lower cost per chip. It has been estimated that migrating from wafers to a panel fan-out platform would lead to a 30–40% reduction in cost. Many outsourced semiconductor and test services (OSATS) and equipment and materials providers are involved in FOWLP-on-panel's process development, but at present, only J-Devices has the established infrastructure for FOWLP on-panel, while ASE uses its flip-chip infrastructure for low-cost FOWLP-on-panel production. Powertech Technology (PTI) is in an advanced stage of development in fan-out panel packaging technology and will go into production in H1 2017.

Even though all major OSATS players have FOWLP-on-panel on their roadmaps and are internally developing panel capabilities, the technique has to overcome a few challenges before it can be adopted in HVM. These challenges include the cost of, or investment into, panel line, supply chain readiness, standardization and market availability, and technical challenges such as warpage and fabrication of fine line/space $<10/10\mu\text{m}$ on large panel. We believe that FOWLP-on-panel will initially be used to package low I/Os and single die with coarse line/spacing ($>5/5\mu\text{m}$) features before migrating to fine line/space features when the market is available and equipment is ready at low cost. However, some players are working on fan-out panel-level packaging (FOPLP) with the same specification as advanced FOWLP ($</=5/5\mu\text{m}$ L/S) for mobile processor applications, which is very challenging. Their success remains to be seen.

Embedded die

Embedded die-in-substrate is a promising packaging technology whose key benefits are small form factor and size, high integration capability, and good thermal and electrical

performance. However, despite these benefits and the multiple players working on this technology, it hasn't really taken off in terms of high-volume manufacturing. There are quite a number of players involved in embedded die activity, but currently only a few players (TDK, AT&S and Taiyo-Yuden) are mass producing them.

Certain factors have impeded the growth of embedded die technology on account of the lack of driving applications and standardization, which make it difficult for end-customers to multi-source. These challenges are gradually being addressed, and we believe that things are starting to happen that will propel this technology onto a path of high growth. The first major challenge is that embedded die lack a driving application. Even though mobile is the main driver of semiconductor packaging, because of the technical limitations of fine pitch, the embedded die product has had difficulty penetrating this market. However, at Yole, we have identified power, wearables and the Internet of Things (IoT) as key applications that will launch the embedded die market into a high-growth trajectory. The second major challenge is that lack of standardization makes it difficult for end-customers to multi-source. With TDK and ASE establishing their "ASE Embedding Electronics" joint venture in 2015 (under which products incorporating TDK's SESUB technology will be manufactured), we see companies starting to address the multi-sourcing challenge. We expect more licensing and multi-sourcing activities in the future that will bode well for embedded die packaging. Also, substrate suppliers such as AT&S are working with industrial bodies like IPC to create standards. Another major challenge is supply chain readiness. Only PCB and substrate suppliers are pushing embedded die technology. Integrated device manufacturers (IDMs) and OSATS seem less interested in pushing the adoption

of this technology. The business model for embedded die differs from what IDMs are used to addressing. It requires PCB manufacturers to temper their expectations and define responsibilities. Except for ASE, OSATS have no experience or understanding of the substrate assembly process. They are more focused on using FOWLP to increase their value and profit by keeping substrate out as part of the supply chain. However, there are business opportunities available if OSATS can collaborate with their substrate partners to leverage their experience and technology to develop the supply chain and create a value-added product that will be a win-win scenario for both. One example is the collaboration between NANUM S.A. and AT&S for E2CP (Embedded Embedded Component Package). Embedded die packaging is expected to be a US\$298 million market by 2020. The main drivers are power electronics and the wearables and IoT segments, which will pave the way for HVM of embedded die packaging [2].

Interposers

The benefits of organic interposers as a substitute for Si interposers for high-performance applications are subsiding. This is mainly the result of technical challenges associated with the fabrication of fine features ($<5/5\mu\text{m}$) on organic substrate at high yield (and hence at a reasonable price). It has been established that only substrate costs do not make a significant difference in overall manufacturing costs for 2.1/2.5D applications. It is the price of fabricating fine features and of assembly that make a difference in overall cost. As long as IC processes and equipment are required to manufacture fine features for organic substrates, it will be a major challenge to replace Si interposers. Serious investments will be required for the equipment to manufacture organic interposers with $2/2\mu\text{m}$ L/S features. The required equipment includes lithography,

sputter, chemical mechanical polishing (CMP) and excimer laser equipment; and manufacturing must be performed in a clean room. New materials with low coefficient of thermal expansion (CTE) and low loss are necessary to address the challenge of assembly and performance. Organic interposers are not yet ready for high-volume markets.

Glass is a potential material for use in panel-form interposers because of its insulating properties, high modulus, and the ability to tailor CTE. In addition, glass has already been used for many years in the LCD industry and large panels are available. Thanks to the fusion process, glass substrates can be fabricated in different sizes. Once the wafer-level glass interposer is accepted by the industry, it will be simple to use existing infrastructure to manufacture glass interposers on a panel level. There is still a strong interest in developing glass-based infrastructure with panel-size processing capabilities, combining a range of processing knowledge such as semiconductor wafer fab manufacturing (front-end)/semiconductor packaging (back-end), PCB/PWB, LCD/flexible displays and solar/PV.

The commercialization of glass panel interposers is limited by its formation and metallization. Substrate-makers and glass-suppliers are pushing to validate the value of glass panel interposers, but OSATS, which have no control over the cost structure of glass and possess limited experience, are not likely to invest in the development of glass panel technology. The supply chain for manufacturing glass panel interposers is still unclear and not yet in place. We speculate several scenarios for the market adoption of glass interposers. Key among them and the most likely are: glass companies such as AGC, Corning, Schott and PlanOptik will take care of TGV formation, including via etching. Substrate suppliers and IDMs might perform downstream processing of via fill or redistribution layer (RDL) and then go to OSATS for assembly and testing. Another likely scenario is that

glass companies such as AGC, Corning, Schott and PlanOptik will take care of through-glass via (TGV) formation including via etching. Substrate suppliers will be involved in the via fill and then will go to OSATS or IDMs for assembly and testing.

Readiness for panel manufacturing

Today, equipment infrastructure in the advanced packaging supply chain primarily processes 300mm round wafers. But to process a larger surface, new equipment and optimized materials are required. For some process steps (e.g., plating, physical vapor deposition [PVD], molding, die attach and dicing), most of the tools are readily available on the market and can be adapted from PCB, flat-panel display or LCD industries and are likely to be reused for producing panels. Some key process steps inherent to advanced packaging, for example, lithography, necessitate the development of new tool capabilities to support thick-resist lithography, panel-handling capabilities, exposure field size, and depth of focus. Moreover, above 8–10 μ m L/S, the PCB design rule dominates, and the equipment and materials infrastructure in this area is already established. The area below 8 μ m represents a space where various equipment vendors like Rudolph, SUSS MicroTec and Atotech are competing today. These vendors either come from PCB infrastructure, or acquire other companies in order to bolster their knowledge of flat-panel display. Given the remaining challenges that need to be solved for panel processes in advanced packaging, there will be huge business opportunities that could attract new equipment entrants from the PCB, LCD and PV industries and who might have the ability to apply existing panel-based tools to panel-scale packaging technologies. Equipment readiness is a key bottleneck in the adoption of panel-level packaging. However, after some initial resistance and several years of promotion and breakthroughs in the technology, suppliers are now eagerly embracing panel-level packaging. On the materials side, the

trends for key materials suppliers is to use their current market-ready products for LCD and advanced packaging applications and optimize them to meet panel package requirements.

Packaging devices at large-panel scale will bring the cost down on account of higher efficiency and economies of scale. There is considerable interest in panel-level manufacturing in the semiconductor industry, and many players are working on this. Among the various packaging platforms mentioned in the article, fan-out on panel is attracting serious interest, with ASE already in production and PTI likely to go into production next year. Equipment suppliers have also realized the potential of panel-level packaging, and multiple suppliers now have the tools ready for it, or are working on it. Embedded die in substrate packages are already on the market, but still have limited volume with only a few players (e.g., TDK, AT&S and Taiyo-Yude) producing appreciable volumes. However, ASE's entry into the market, by licensing TDK's SESUB technology, is a game-changer, and with new drivers like the IoT and wearables, we expect sharp growth in the embedded die packaging market. Glass interposers have strong potential for packaging RF devices, and glass suppliers like Corning and AGC have shown considerable progress in TGV processing. The supply chain for glass interposers, however, is not yet ready for mass production.

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Biography

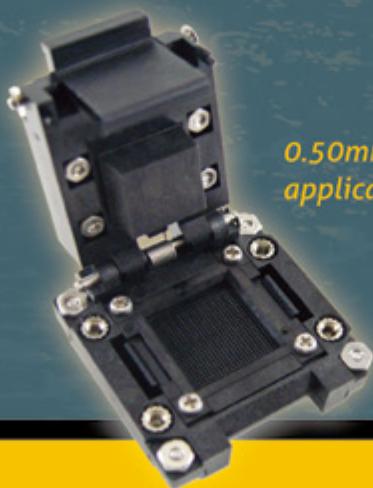
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Heterogeneous multi-die ICs complement SoCs and enable efficient system design

By Herb Reiter *[eda 2asic Consulting, Inc.]*

I strongly believe that 2.5D ICs, 3D ICs, as well as wafer/panel-level processing and other multi-die packaging solutions currently in development are the semiconductor industry's best alternatives to continue growing its revenues and profits in the next 10+ years. These technologies bring die-level IP blocks closer together and increase performance, while significantly reducing the power dissipation, currently wasted in I/Os and chip-to-chip interconnects. They also make combining heterogeneous functions (logic, memory, analog, RF, MEMS, etc.) in one IC package easy. All these are critical enablers for electronic system scaling and allow designers and manufacturers to create more cost-effective, higher performance and lower power electronic system. The ability of multi-die technologies to "quickly assemble heterogeneous die-level building blocks in one IC to the needed solution" enables semiconductor vendors to respond much faster to new market opportunities and to high-value customer requests with system-level solutions, instead of typically low-margin components.

Multi-die IC technologies are clearly one of the most promising, but also the most complex innovation to which I have contributed. Why is introducing multi-die IC packaging so difficult? After enjoying 50 years of a "cruise control-like" scenario following Moore's Law, market requirements now demand more than the traditional system-on-chip (SoC) ICs can offer economically and in a timely fashion. Significant changes to most segments of our very complex semiconductor ecosystem are needed, to continue serving our customers well and securing our industry's growth.

The high-growth automotive segment is a good example for market requirements moving from the component-level thinking (e.g., CPU, DRAMs, UART, etc.) in PCs to the subsystem and even system-level

(fuel injection, ABS, rearview camera, adaptive cruise control, etc.) thinking in new markets. Automotive is just one market segment that's demonstrating the need for significantly more electronics and more heterogeneous semiconductor functions. Reliability, high performance at low power dissipation, as well as small form factors are important features too, for the success of electronic systems. Industrial and networking equipment, even consumer products, like smartphones and wearables, demand more and more heterogeneous capabilities—a big change, compared to the digital-only components dominating computers only a decade ago.

To address the shift from component-level to system-level thinking, the Electronic System Design Alliance (ESD Alliance) has created a System Scaling Working Group. The objective of the working group is to make sure that the necessary automation, modeling and analysis tools and services are identified so that system scaling technologies can proliferate. Not only will this help grow the market for multi-die ICs, but also provide tool and service vendors with new growth opportunities.

Heterogeneous functions have already exceeded logic revenues

Figure 1 demonstrates the increasing demand for heterogeneous functions. 2015 was the first year when ICs with heterogeneous functions (green) generated more revenues than the previously dominant digital circuits (black). Additional information about this analysis is at [1].

Figure 1 also shows which functions today surround a primarily

logic-containing SoC on a PCB. These functions, highlighted in green, add significant value to the mostly digital SoC by interconnecting it with the mostly non-digital world and complementing its digital functions to build a useful sub-system or system. By mounting the mostly digital die-level SoC together with heterogeneous die-level building blocks on an interposer or IC package substrate, a lower-power, higher-performance and smaller form factor (sub)system can be created quickly. When market-driven or customer-specific changes are needed, only the impacted die-level IP building block(s) need to be replaced or modified, which results in a significant saving of non-recurring engineering (NRE) costs, and development time and risk, compared to a complete SoC redesigns.

Single-die SoCs and costly heterogeneous integration

At the recent Design Automation Conference (DAC 2016 in Austin), the world's premier foundry showed in a very clear and compelling way that integrating heterogeneous functions on a single chip using the latest process is not available. To integrate heterogeneous functions on a single chip requires the use of larger

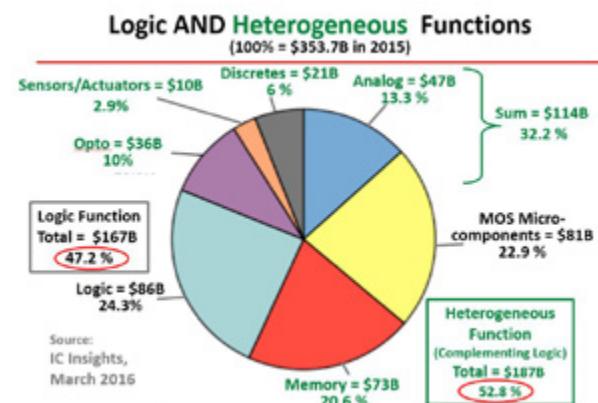


Figure 1: Market shares of logic and heterogeneous functions. SOURCES: IC Insights/Electronic System Design Alliance

feature sizes, limiting the number of transistors available, the performance of the digital functions and increases power dissipation. Also, adding heterogeneous capabilities to a logic process increases the number of masking layers, tooling and wafer cost. In addition, the more complex manufacturing flow reduces yield and increases die cost even further.

I have to mention here that the always visionary TSMC management team initiated in 2014 the development of ultra-low power process technologies with relatively large feature sizes (55 and 40nm) to serve the IoT market. These processes may make implementing heterogeneous functions, together with logic, easier. However, SoCs using these processes will not offer the modularity and time-to-market advantages of multi-die ICs.

Multi-die ICs in use today

Altera, AMD, eSilicon, IBM, Intel, Marvell, Nvidia, Open Silicon, Semtech, Xilinx, and others have already demonstrated, in cooperation with their suppliers, the benefits of 2.5D ICs, combining dies with homogeneous and/or heterogeneous function side-by-side on an interposer. The “Multi-die IC User Guide” ([2]) provides details.

The large memory suppliers SK-Hynix, Micron and Samsung, offer 3D ICs, a.k.a. “memory cubes,” comprising vertically stacked memory dies in volume production. Additional information is available on p. 204 in [2]. Tezzaron, a smaller memory vendor, outlines its memory cubes and product line in depth [2].

Call to action for customers

After highlighting some of the benefits of advanced packaging technologies, explaining why we need them and listing current users, I hope to have raised your interest in multi-die ICs. Are you interested enough to consider one of the available and proven solutions for your next design? If yes, check with your supply chain partners to see what they can offer.

Call to action for suppliers

My experience, gained on the bleeding edge of several new technologies, tells me that for the success of advanced packaging

technologies in the broad market, we need good cooperation between IC and package designers, EDA vendors, assembly and test experts, as well as material suppliers. We need to transform the existing capabilities for specific design and manufacturing steps into user-friendly and cost-effective flows. For reference, it is important to note that SEMI has outlined its plans for the Heterogeneous Integration Roadmap effort from a primarily manufacturing perspective [3].

Figure 2 outlines the Electronic System Design Alliance’s plans for the System Scaling Working Group. Plans include coordinating IC design-centric efforts and EDA tools developments, such as: 1) The creation of a die-package CO-design flow; 2) Efficient exchange of proprietary design and manufacturing data in encrypted form; 3) Accurate modeling of material characteristics and capabilities of cost-effective manufacturing flows; and 4) High-level modeling of chiplets = IP building blocks in die-form, for integration on interposers, such as the suggestion of UCLA’s Subramanian Iyer [4].

Summary

In the late ’90s, I had the opportunity to drive, in cooperation with the top ten ASIC vendors, the Primetime STA sign-off wave. Also, jointly with TSMC, my team at Synopsys developed their first two Reference Flows. Both IC design methodologies have since been significantly enhanced and are still dominant today. These multi-year programs taught me two very important things. First, EDA tools and flows are only as accurate and useful as their inputs. Accurate modeling of IC materials, library elements, IP blocks, package characteristics, etc., is very important for an EDA design tools success. To achieve this, supply chain partners and their mutual customers need to work together!

The second lesson is that good EDA

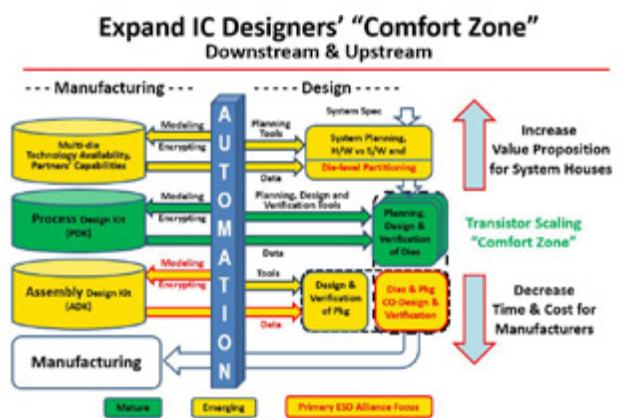


Figure 2: Expand IC designers “comfort zone” downstream and upstream.
SOURCE: Electronic System Design Alliance

tools and flows enable designers to walk the fine line between costly over-design and unreliable under-design and get an IC much faster to market than building multiple prototypes, to test what works and what doesn’t. Good design methodologies are essential to make a new technology cost competitive and reliable!

Acknowledgment

To become a member of the ESD Alliance and join the System Scaling Working Group, please contact the author at herb@eda2asic.com.

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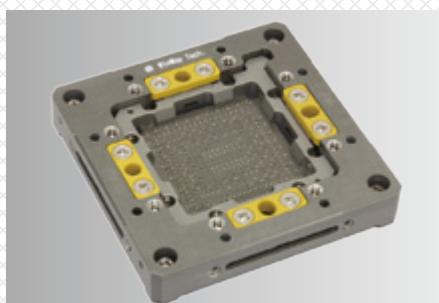
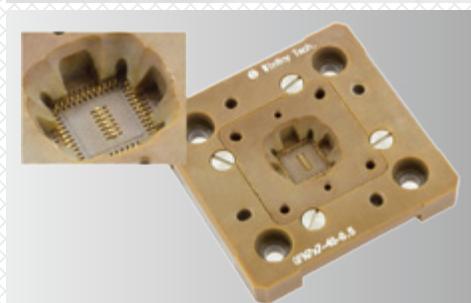
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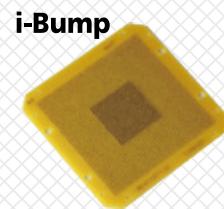
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Evolution of temporary bonding technology for advanced semiconductor packaging

By Ramachandran K. Trichur, Tony D. Flaim [Brewer Science, Inc.]

Over a decade ago, no one could have predicted the impact of the now ubiquitous smartphone and personal devices such as wearables on our everyday lives. The convergence of several revolutionary developments in hardware, software, and user experience over the past ten years has led us to the current state. For example, a redefined mobile phone hardware and a reinvented interface changed the portable phone from a mere voice communication tool to a powerful, multifunctional device that is now a central link in the internet of things (IoT) and serves as a portal to social media, video streaming, and a growing menu of productivity applications. These and still-emerging applications in mobile and consumer electronics are driving the semiconductor industry to focus on higher integration and scaling to meet increasing demands for performance and functionality as well as reductions in cost, form factor, and power consumption.

Much the same can be said for the growth and diversity of applications for thin wafer handling (TWH) technology that utilizes temporary bonding of a device substrate to a supporting carrier. TWH technology was introduced about 15 years ago to solve problems with thinning and handling of fragile III-V and compound semiconductor substrates. Since that time, it has found widespread application in advanced semiconductor packaging such as for the fabrication of 2.5D interposers with TSVs, 3D-ICs, and fan-out wafer-level packages (FOWLP). Temporary bonding technology has been used successfully for handling of thin substrates through all of the backside processes commonly encountered in the fabrication of these advanced package forms [1]. Several generations of adhesive bonding materials and new bonding and separation (debonding) techniques have been introduced along the way to meet the challenges that are unique to each end application. In this paper, we will review the evolution of TWH technology and the processing requirements

and intricacies that define the selection of a bonding material and debonding method.

Temporary bonding technology

Temporary bonding technology is a method of mechanically stabilizing a device substrate by mounting it temporarily to a rigid carrier by means of a polymeric bonding material or adhesive. In many instances, the polymeric adhesive is used in conjunction with a second polymeric layer applied to the carrier and to which it adheres. The second layer facilitates separation of the bonded structure after backside processing has been completed. The bonding materials and the carrier substrate mechanically support the device wafer during thinning and subsequent

was the main adhesive material used for temporary bonding when backgrinding wafers to thicknesses below 100 μm . However, its poor rheological properties, limited heat stability, and difficult application have led the advanced semiconductor packaging community to seek better bonding material solutions. As a result, several generations of polymer adhesives have been developed to offer greater in-process thermo-mechanical stability and more facile debonding at the end of the process. These materials enable the handling of ultra-thin substrates (<50 μm) and also substrates that are highly prone to warping and deforming such as reconstituted wafers and panels encountered in advanced FOWLP processes. **Table 1** illustrates the

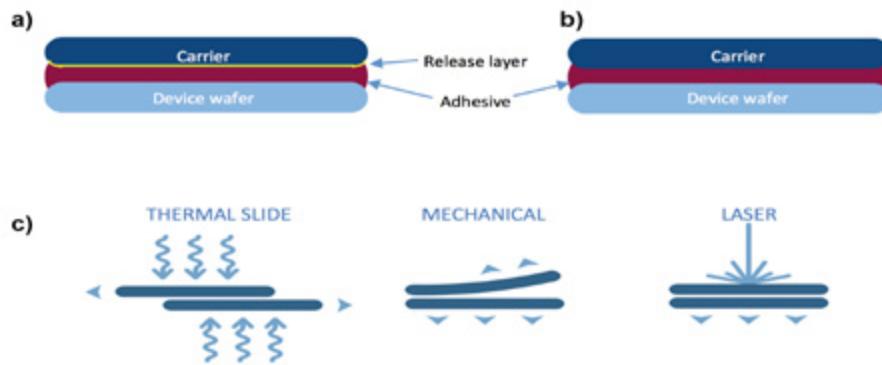


Figure 1: Schematic diagrams of temporarily bonded carrier and device wafers a) with a release layer, b) without a release layer, and c) an illustration of the predominant debonding methods.

backside processing. The predominant methods of separating the structure, or debonding, are thermal sliding, low-force peeling (mechanical debonding) between the adhesive and second layer, and laser ablation of the second layer (laser debonding) to release the carrier. These processes are depicted in **Figure 1**.

Originally, wax

Key Technology Challenges	
Substrate size	▲ 300-mm wafers moving to panels (for FO pkg)
Substrate thickness	▼ 50 μm and reducing
Downstream process temperatures	▲ Increasing from 180°-250°C to ~400°C
Substrate stress	▲ High residual stress
Requirements for mechanical stability	▲ No movement or decomposition of bonding material during processing

Manufacturing Expectations					
Yield	▲	TWH process complexity	▼	Throughput	▲ Cost of ownership

Table 1: Key trends in thin wafer handling technology and expectations for high-volume manufacturing.



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Typical Applications

Semiconductor Packaging

- Medical Imaging
- Multichip Modules
- 3D / 2.5D Packaging
- Wafer Scale Packaging
- RF / Microwave Modules

Photonic Packaging

- Optical Engines
- LED Assemblies
- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

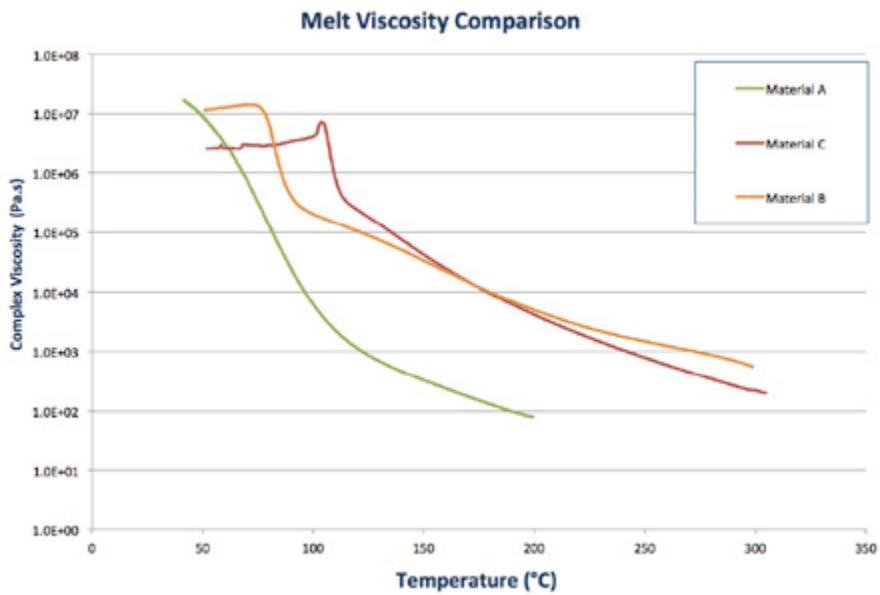


Figure 2: Melt viscosity curves of three thermoplastic adhesive platforms, illustrating the change in complex viscosity with respect to temperature. Note that complex viscosity is plotted on a logarithmic scale.

Technology Generation	Bonding Material	Use Range	Material Type*	Mode of Release**
Commercial	GEN 1	WaferBOND® HT-10.10	150°C - 200°C	High-flow, non-polar resin blend
	GEN 2	BrewerBOND® 220	150°C - 200°C	Very high-flow, non-polar resin blend
	GEN 3	BrewerBOND® 305	180°C - 250°C	Mid-flow, non-polar thermoplastic
Developmental	GEN 3+	Beta stage products	Multiple ranges < 275°C & < 350°C	Low-flow, polar thermoplastic with strong device adhesion
	GEN 4	Experimental Products	250°C - 400°C	Non-flowing, polar thermoplastic & HT-stable curable layer
Laminate Systems	Various compositions in dry film format	Multiple ranges	Low-flow, polar and non-polar thermoplastics	Chemical release

* Flow behavior of each material type corresponds to the rheological property of the material

** Chemical release Thermal slide Mechanical debond Laser release

Table 2: Brewer Science temporary bonding material generations and key characteristics.

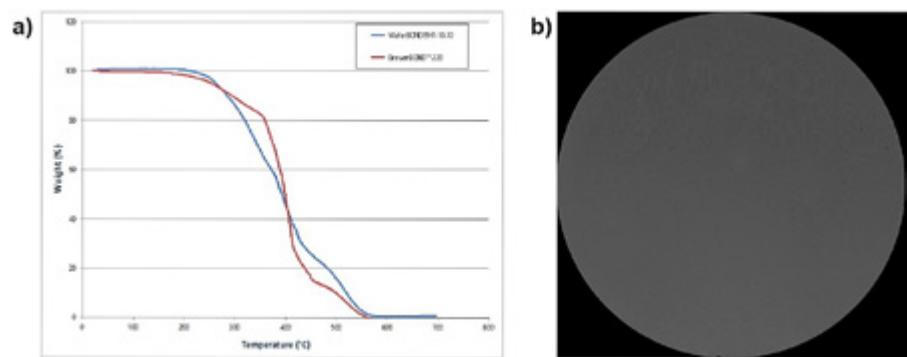


Figure 3: a) TGA of GEN1 and GEN 2 bonding materials; b) CSAM image of a bonded wafer with BrewerBOND® 220 material after grinding to 100µm and exposure to 250°C for 30min.

key trends in TWH technology and the expectations for this technology in high-volume manufacturing.

Thermo-compressive bonding with thermoplastic adhesives. Thermoplastic adhesive materials offer several advantages for temporary wafer bonding. These include: 1) The ability to tune the softening temperature, viscosity, adhesion, and modulus by the choice of compositional parameters, which in turn control the bonding temperature and the level of stress imposed by the bonding material on the structure; and 2) The ability to remove the thermoplastic material from the device wafer by solvent dissolution after the structure has been separated at the end of processing. These features afford compatibility with all the major debonding methods, including chemical dissolution, mechanical peeling, thermal sliding, and laser-assisted debonding. At the same time, the properties of thermoplastic bonding materials stand in contrast to liquid, curable-type adhesives that become cross-linked during the bonding process and, therefore, cannot be dissolved after separation. They must instead be peeled as a monolithic layer from the substrate, which can easily detach metal device features and leave complex residues on the device wafer surface.

Melt rheology. One of the key properties of thermoplastic polymers that make them suitable as temporary adhesive materials is reversible softening that occurs with the application of heat. This behavior can be described by their melt rheology, which is the relationship between dynamic viscosity of the polymeric material and temperature. While absolute viscosity is a measure of a fluid's internal resistance to flow, dynamic viscosity is the measure of tangential force required per unit area to move a horizontal plane at a unit velocity while maintaining a unit distance apart in the fluid with respect to another horizontal plane. Dynamic viscosity is indicative of how a thermoplastic bonding material will behave under the shear forces and stresses encountered in backside processing of a temporarily bonded wafer stack. Determination of an adhesive's melt rheology is useful for optimizing the bonding conditions, estimating the maximum in-use working temperature, and predicting bond line stability under the compressive and tensile stresses that occur during backgrinding and deposition processes. **Figure 2** shows the melt rheology curves of three distinct thermoplastic adhesive platforms, illustrating the change in viscosity with respect to temperature for each platform.

The thermoplastic behavior of each platform in **Figure 2** is typified by the shape of the melt rheology curve. (Note that complex viscosity is plotted on a logarithmic scale in the figure.) At a characteristic temperature known as the softening point, the melt viscosity decreases rapidly and then decreases more or less linearly as temperature increases. Materials B and C, which are high molecular weight, single-component thermoplastic systems, have sharp softening points that correspond to their transition from a glassy state to a hard rubbery state. On the other hand, Material A, which is a mixture of a low-molecular-weight resin and a very high molecular weight polymer, softens much more gradually and drops to a much lower viscosity than the high molecular weight, single-component polymer compositions.

Various elements in the formulation of the thermoplastic adhesive affect the melt rheology of the final product, and thereby, the maximum usable downstream process temperature. While the molecular weight, which can be thought of roughly as the average length of the polymer chains, dominates the flow behavior above the softening temperature, other factors that can affect the melt rheology include the addition of fillers to the neat polymer, branching, dipolar and crystalline interactions of the polymer chains, molecular weight distribution, and homogeneous or heterogeneous blending of polymers in the adhesive. These elements can be adjusted to create a bonding material formulation that is the most suitable for a specific device manufacturing process.

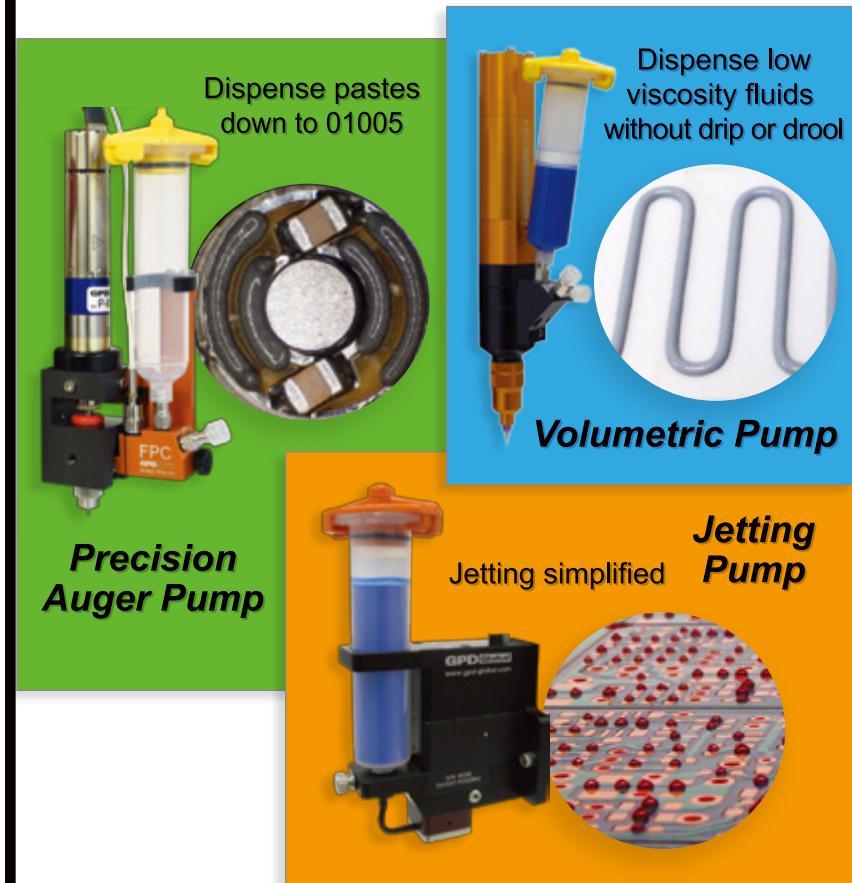
Advancement of temporary bonding materials

We have developed several generations of temporary bonding materials to address the thin wafer handling challenges in different advanced packaging applications. The need for bond line stability at increasingly higher working temperatures and the ability to maintain adhesion at high-stress points in the bonded wafer stack have been the main drivers for advancing product performance. **Table 2** lists the key material characteristics for each generation of bonding material in our portfolio.

GEN 1 and GEN 2 high-temperature (HT) bonding materials for moderate-stress applications. Our first two generations of thermoplastic bonding materials were designed for greater thermal stability and solvent resistance than prior art systems such as hot-melt waxes and pressure-sensitive adhesives could provide. They have been

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Film Thickness (μm)	Wafer bow with BrewerBOND® 220 material (μm)	Wafer bow with BrewerBOND® 305 material (μm)
25	-1.67	
50	5.26	83.71
75	0.16	

Table 3: Wafer bow measurement on a wafer coated with bonding material.

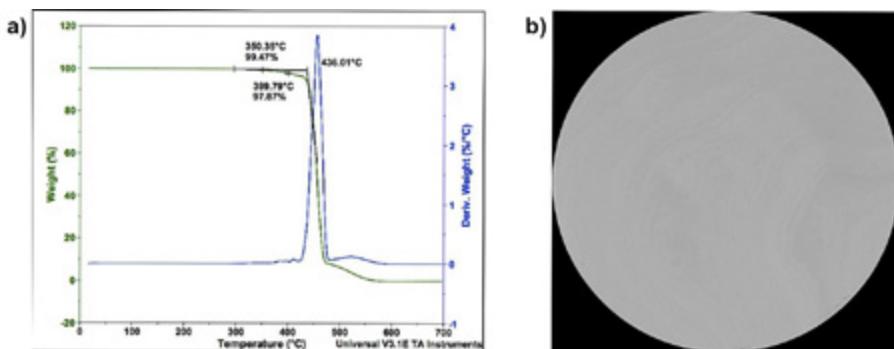


Figure 4: a) TGA of GEN 3 bonding materials; b) CSAM image of a bonded wafer with BrewerBOND® 305 material after exposure to 270°C for 30min.

used primarily for wafer thinning and TSV-reveal in 2.5D and 3D integration schemes. These bonding materials are blended polymer systems with two components that work together to control flow and melting temperature of the final bonding material formulation. They have comparatively low softening points of 60°-80°C to allow bonding at a temperature of 140°-190°C while providing stability up to about 200°C in backside processes. **Figure 3a** shows the results of thermo-gravimetric analysis (TGA) of the GEN 1 and GEN 2 bonding materials; both exhibit less than 2% weight loss up to 200°C. **Figure 3b** is a through-bond conformal scanning acoustic microscopy (CSAM) image of a bonded wafer stack after backgrinding and applied heat stress. The absence of any defects in the bond line indicates the excellent stability of BrewerBOND® 220 material under these conditions. The components used in the GEN 1 and GEN 2 bonding materials are non-polar, hydrocarbon-like components that are resistant to all common photoresist solvents and even powerful solvents, such as NMP that are used in photoresist cleaning processes. Likewise, the bonding materials are unaffected by aqueous acids, bases, and plating chemicals. These bonding materials contribute very low stress when applied to the device wafer even at thicknesses up to 100 μm . This is evidenced by the formation of less than ~5 μm of post-bond bow (for full-thickness wafers),

whereas other bonding material platforms can induce bow in the range of 80-150 μm at comparable thicknesses. **Table 3** displays the typical wafer bow for substrates coated with BrewerBOND® 220 material, a GEN 2 material, and BrewerBOND® 305 material, which is a GEN 3 material designed for higher temperature applications. The bow values were determined after coating and baking the bonding materials on ultra-flat wafers.

higher temperatures and shear forces that can damage thinned device wafers, this method is less suitable for manufacturing situations that demand high throughput. Moreover, the method is incompatible with device substrates that have high topography features on the out-facing side of the device wafer because that face must be gripped by a heated chuck during the separation process. As a result, our GEN 3 series of thermoplastic bonding materials were developed to offer in-process stability up to 250°C and to access low-force debonding methods.

BrewerBOND® 305 material, a GEN 3 thermoplastic bonding material, is a polymeric bonding material system. The material softens in the range of 80°-150°C and maintains high melt viscosity up to 180°C, which in turn stabilizes the bond line at high processing temperatures to prevent adhesive reflow and delamination under mechanical stress. The material can tolerate processing temperatures in the range of 250°C and possesses exceptional resistance to thermal decomposition ($T_d > 400^\circ\text{C}$) and also excellent resistance to all photoresist solvents and other process chemicals.

The GEN 3 bonding materials were also developed to take advantage of a mechanical debonding method [2] that allows wafers to be separated at room temperature using very low mechanical force. In this method, the GEN 3 bonding material in contact with the device wafer bonds to a carrier wafer that has been coated with a polymeric layer that forms a strong physical bond with the bonding material surface, but does not react chemically with the bonding material surface. Debonding occurs by initiating a crack between the two polymer layers and then propagating the crack across the

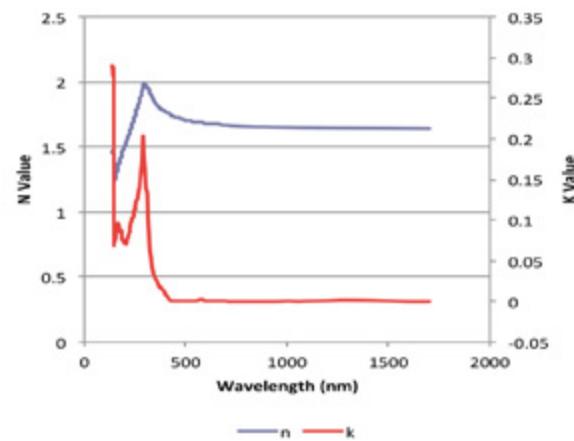


Figure 5: n and k measurements for laser release material showing high absorbance in less than 400nm wavelength. Inset shows the successful debonding of wafers using a 355nm laser source at a power level of 3.5W.

interface by slightly deflecting the carrier wafer and applying a low peeling force. Debonding occurs in a matter of a few seconds. Several spin-applied surface treatments have been developed to create a low-energy surface on the carrier to control how strongly the bonding material can bond to it.

The GEN 3 bonding materials can also be debonded using laser-assisted methods. In laser debonding, a high-temperature-stable, ultra-thin polymer coating system such as BrewerBOND® 701 material is applied to a transparent glass carrier and bonds physically to the GEN 3 bonding material. When the thin layer is scanned with a UV excimer laser through the carrier, it ablates (or decomposes), releasing the carrier. The laser release layer is sensitive to the commonly employed scanning wavelengths of 248, 308, and 355nm. It is also designed to ablate cleanly at a low laser fluence, $\sim 180\text{mJ/cm}^2$, to enable high-throughput debonding. The release layer provides an excellent bonding surface for most adhesives and can survive high backside processing temperatures without decomposing or flowing. Our adhesives do not absorb at the UV wavelengths used for ablation of the laser release material, which eliminates concerns about the formation of charred residues on the bonding material surface that contacts the laser release layer. **Figure 4** shows the refractive index (n) and k -value of the laser release layer versus wavelength. Note the strong absorbance in the deep UV portion of the spectrum (200-350nm) as indicated by the high- k values in that region of the curve. The inset shows a device wafer and transparent carrier device after successful laser debonding.

GEN 3+ bonding materials for FOWLP. In FOWLP, known-good dies are picked and placed on a substrate and then over-molded with an epoxy molding compound to create a reconstituted wafer. Reconstituted wafers have large internal stresses on account of their hybrid composition of silicon and epoxy materials. Significant bowing and warping usually occur when these substrates are thinned to less than 400 μm and then heated above 150°C, which renders them almost impossible to handle in standard wafer handling equipment. As a result, it is becoming common practice to temporarily bond thin reconstituted wafers to a carrier for processing prior to singulation.

GEN 3+ bonding materials were developed to provide strong adhesion to the surface of reconstituted wafers comprised of silicon, silicon nitride, various metals, and polymer dielectric layers such as polyimide, polybenzoxazole (PBO), and benzocyclobutene (BCB). Therefore, the

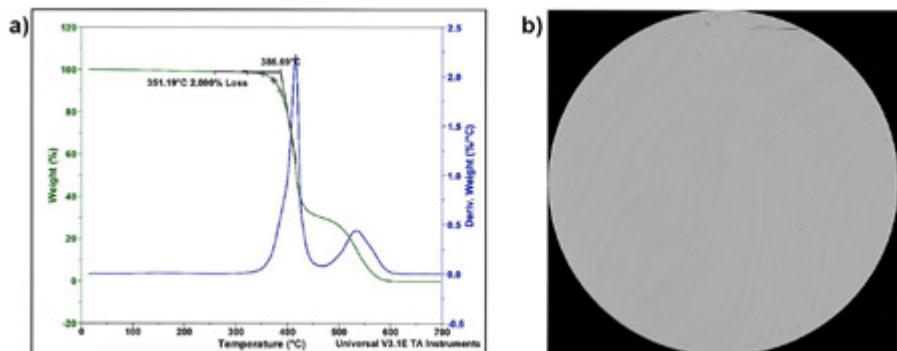


Figure 6: a) TGA of GEN3+ bonding materials; b) CSAM image of a bonded wafer with GEN3+ material and release layer after exposure to 260°C for 2 hours.

material composition was shifted from a non-polar thermoplastic to a polar thermoplastic to achieve higher adhesion strength. Polar thermoplastics generally adhere strongly to device materials and release layers, making the bond line more resistant to delamination and void formation during high-temperature processing where the bonding material exists in a softened state.

GEN 3+ bonding materials are thermoplastic adhesive systems with softening temperatures in the range of 100°-150°C. The materials

exhibit good wetting and adhere strongly to semiconductor and reconstituted wafers and can boost in-process thermal stability to beyond 225°C, in some cases stabilizing the bond line up to 300°C. **Figure 6a** displays the TGA spectrum of a GEN 3+ material, indicating that less than 2% weight loss occurs up to 350°C. The same material showed good bond-line stability during applied heat stress of 260°C for 2 hours as can be seen in the CSAM image of a bonded wafer pair in **Figure 6b**. GEN 3+ bonding materials can be used in

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conjunction with a variety of companion mechanical and laser release layers. The polar GEN 3+ materials offer rapid and complete dissolution in solvents such as cyclopentanone to afford faster cleaning than earlier generation thermoplastic bonding material systems.

During processing, reconstituted wafers can impose inordinate amounts of stress on the interface between the adhesive layer and various release layers. We have recently developed a new polymeric mechanical

release layer to provide a stronger interfacial bond with the bonding material while still maintaining the ability to perform low-force mechanical separation. The ultra-thin (0.15–0.25 μm) polymeric mechanical release layer is spin-applied on the carrier and requires only a short bake at about 200°C. After backside processing and debonding, the release layer is removable with solvent for easy carrier recycling. Additional GEN 3+ bonding material platforms with higher

softening points and more limited flow up to 250°–275°C are under development.

Summary

Temporary bonding material development has been driven by the changing needs for thin wafer handling in advanced packaging processes. Applications in FOWLP, 2.5D, and 3D-IC integration all pose unique demands on the bonding material in terms of handling residual stresses and meeting the adhesion, in-process thermal stability, outgassing, chemical resistance, and separation requirements. An in-depth understanding of the relationships between the polymer structure of the bonding material and its properties such as melt flow behavior, thermal stability, solubility, and surface energy is essential for developing a temporary adhesive system that can satisfy these difficult and oftentimes conflicting requirements. A single material cannot address the requirements for the many different manufacturing process flows now in place, which has necessitated the need for a portfolio of temporary adhesive systems. We expect that temporary bonding materials will need to survive still higher in-process temperatures (350°C+) for emerging applications such as die-to-wafer permanent bonding that involve high temperatures and pressures. A fourth generation of high-performance materials that utilize an innovative bond line architecture are already being field tested in response to this anticipated need.

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2. T. D. Flaim, J. McCutcheon, "Method for reversibly mounting a device wafer to a carrier substrate," U.S. Patent 9,111,981; Aug. 18, 2015.

Biographies

Ramachandran K. Trichur received his MS in Electrical Engineering from the U. of Cincinnati, and BS in Electrical and Electronics Engineering from Bharathidasan U.; he is a Business Development Manager at Brewer Science Inc.; email rtrichur@brewerscience.com

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System Performance

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12~18 Sec (Fine Pitch Package(2 Dotting/Strip))
25~30 Sec (Fine Pitch Package(2 Dotting/Strip))
YIELD PERFORMANCE : 99.98%
Placement Accuracy : +/- 0.02mm
Fine Pitch Capability : 0.100mm_Ball size / 0.180mm_Ball pitch
Strip Handling Capacity : 50 ~ 95mm Width x 180~260mm Length
Product Flexibility : All kinds of laminated Substrate BGA Package series
Quick Conversion Time : Ball tool, Flux tool, Lift Block
Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)
Foot Weight : 3,000kg

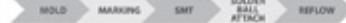
BPS-8200 Process (Stand-alone type : Magazine Input)



BPS-8200S
Ball Placement System

Cycle Time : 12~14 Sec (Normal Package(1 Dotting/Strip))
12~18 Sec (Fine Pitch Package(2 Dotting/Strip))
25~30 Sec (Fine Pitch Package(2 Dotting/Strip))
YIELD PERFORMANCE : 99.98%
Placement Accuracy : +/- 0.03mm
Fine Pitch Capability : 0.100mm_Ball size / 0.180mm_Ball pitch
Strip Handling Capacity : 50 ~ 95mm Width x 180~260mm Length
Product Flexibility : All kinds of BGA Package series
Quick Conversion Time : Ball tool, Flux tool, Lift Block, Stripper(Optional)
Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)
Foot Weight : 3,000kg

BPS-8200S Process (Inline type: Substrate Input)



BPS-7200FC
Ball Placement System for Flip Chip

Cycle Time : 15~18 Sec (Single Boat without Flipper) / 22~25 Sec (Matrix Boat without Flipper) / 27~30 Sec (Matrix Boat with Flipper)
YIELD PERFORMANCE : 99.98%
UPH : 3,600 EA(24up Boat)
Placement Accuracy : +/- 0.03mm
Fine Pitch Capability : Min. 0.20mm Ball size & 0.40mm Pitch
Product Flexibility : All kinds of Flip chip BGA on boat
Quick Conversion Time : Ball tool, Flux tool, Vacuum Block, Pre-aligner, Flipper(Optional)
Foot Print & Weight : 2,800(L) x 1,800(W) x 1,870(H)
Foot Weight : 3,500kg



wBPS-2000
Wafer Solder Ball Placement System

Cycle Time : 120sec/wafer(12"wafer -880,000 Ball)
High Capability : +/- 0.02mm
Fine Pitch Capability : 0.050mm
Ball size & 0.120mm mm Pitch
Target Device : 8,12inchwafer
High Productivity : Max. 30WPH
Wafer Chuck - XYZ axis
PRS vision -Look Up type
Stencil, Wafer Vacuum Chuck
Lm Guide + Ball Screw
Wafer Loading/Linear motion
Vacuum ejector
Inlet PRS Vision
Flux Y axis servo motion
Flux Squeegee Blade
ABL™ (Air floating Ball Loading unit)
Foot Print : 2900(L) x 1300(W) x 2100(H)

Package EMI Shielding System

H-VAM Application



PSS-8000SL
Package Sorting System

System Performance

UPH : 13,000
Yield Performance : 99.9%
Placement Accuracy : +/- 0.15mm
Picker : 14 Pickers x 2 Head
Package Type : 3x3 mm ~ 20x20 mm LGA, BGA
Product Flexibility : LGA, BGA PKG Applicable
Quick Conversion Time :
Detach tool, Picker pad, Precise tool
Foot Print : 3,460(L) x 2,090(W) x 1,760(H)
Foot Weight : 3,500kg



PSS-8000SUV
Package Sorter System with Vision

UPH : 12,000 / 8,000
Yield Performance : 99.9%
Placement Accuracy : +/- 0.15mm
Picker : 14 Pickers x 2 Heads
Package Type : 3x3 mm ~ 20x20 mm LGA, BGA
Product Flexibility : LGA, BGA PKG Applicable
Quick Conversion Time :
Detach tool, Picker pad, Precise tool
Foot Print : 3,460(L) x 2,090(W) x 1,760(H)
Foot Weight : 3,500kg

PI-TAPE Application



PSS-7000SL
Auto Package Loading P&P System

System Performance

UPH : 13,000
Yield Performance : 99.99%
Placement Accuracy : +/- 0.02mm
Product Flexibility : 3x3 mm ~ 20x20 mm LGA, BGA PKG Applicable
Quick Conversion Time : 3x3 mm ~ 20x20 mm LGA, BGA
Product Flexibility : LGA, BGA PKG
Applicable Quick Conversion Time : 3x3 mm ~ 20x20 mm LGA, BGA
Reject sorting : Rework Tray
Vision System : Top Frame Align - 1.4K (FOV 20.0x15.0, Resolution 14um)
Top Picker Align - 5M (FOV 22.0x16.0, Resolution 9um)
Bottom Align - 4M (FOV 20.5x20.5, Resolution 10um)
Motion Picker : 10ea x 2set (Individual Z, T Motion)
Detach Picker x 2set



PSS-7000SUV
Auto Package Loading P&P System

UPH : 10~12K (Based on 860Unit/Frame)
Placement Accuracy : +/- 0.05mm with Theta axis
Product Flexibility : 3x3 mm ~ 20x20 mm LGA, BGA PKG Applicable
Quick Conversion Time : Picker Pad: Less than 20Min
Reject sorting : Rework Tray
Vision System : Top Frame Align - 1.4K (FOV 20.0x15.0, Resolution 14um)
Top Picker Align - 5M (FOV 22.0x16.0, Resolution 9um)
Bottom Align - 4M (FOV 20.5x20.5, Resolution 10um)
Motion Picker : 10ea x 2set (Individual Z, T Motion)
Detach Picker x 2set
Foot Print & Weight : 2,050(L) x 2,000(W) x 1,800(H) / 2,500kg

Pre-competitive initiative to boost panel-level packaging for FOWLP

By Michael Töpper, Tanja Braun, Rolf Aschenbrenner, Karl-Friedrich Becker, Klaus-Dieter Lang [Fraunhofer IZM]

Without any doubt, wafer-level packaging using redistribution layer (RDL) technology has been the winner for being the optimal chip-scale package (CSP) for lowest cost, smallest size and best electrical performance. This package was the only possibility to solve the dilemma for moving flip-chip assembly to printed wiring boards (PWBs). At the end of the 1990s, there was a strong need for extreme miniaturized packages to build smaller cell phones. Motorola started to use flip-chip-on-board (FCOB) — the direct assembly of naked dies on the board — for the StarTac in 1996. But others like Nokia, which, at the time was the largest cellphone manufacturer, stopped these activities on account of unsolvable issues for the direct assembly on PWB. In addition, reliability was a concern. WLP using RDL was, therefore, the perfect solution because the bump pitch was similar to the existing ball grid array (BGA) packages, but offered true die size, which is essential for miniaturized consumer hand-held products. WLP is currently the most often used package for smartphones. Moore's Law, however, has still been in play, resulting in shrinking of the die size from year to year. This situation has brought back the issue with ball pitch (**Figure 1**).

To enable the increasing number of I/Os that have to be routed on the decreasing die surface area, the ball size has to be decreased, which brings back the issues that still had not been solved for the FCOB platform twenty years ago. Because the main limitation of WLP using RDL is simple: the fact that only the die surface can be used for the BGA pattern. A finer bump pitch requires a higher routing density on the substrate that will be used for the next level of packaging. In addition, the bumps have to be smaller to feed the smaller BGA pitch; therefore, the reliability of assembled WLPs is reduced. Fan-out WLP has therefore been developed to stay on a relaxed BGA

pitch through the creation of additional space by embedding the chips or other components into the planar molding compound. The components are separated from each other by a space filled with the epoxy resin that is used to enlarge the footprint for the RDL. A kind of reconfigured wafer is created. Only pre-tested known good dies (KGDs) are used for this embedding process. The components are glued on a carrier foil or glass plate and are overmolded. The carrier is then removed and the active side of the components can be used for the RDL.

Fan-out wafer-level packaging (FOWLP) has already been proven as one of the most versatile packaging technologies in recent years; and is reaching a market value of over \$170M USD on account of the tremendous increase in hand-held applications. The technology combines high-performance and increased functionality with a high potential for heterogeneous integration and a reduction in the total form factor. FOWLP has been in volume production for mobile and wireless applications (mainly wireless baseband) and is now moving to automotive and medical applications. The first commercial version of this package was the embedded wafer-level BGA (e-WLB)

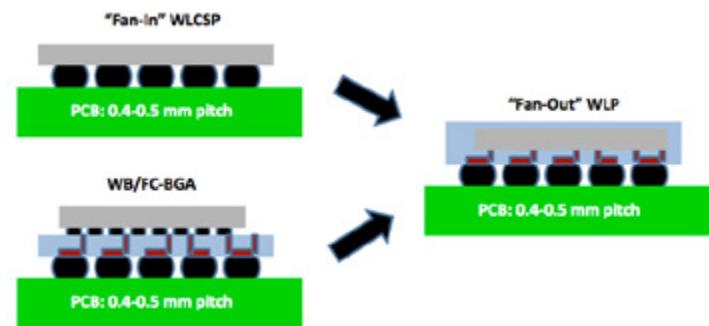


Figure 1: Comparison of FI-WLP, WB/FC-BGA and FO-WLP. SOURCE: Yole Développement, 2015

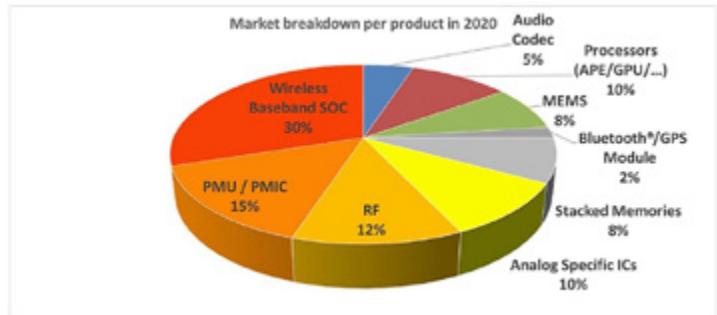


Figure 2: FO-WLP market in 2020. SOURCE: Yole Développement, 2015

from Infineon in 2008 [1]. The first product was a wireless baseband system-on-chip (SoC) with multiple integrated functions such as GPS, FM radio, etc. This technology was later licensed to the outsourced semiconductor and test suppliers (OSATS) NANIUM S. A. (Portugal), STATS ChipPAC (Singapore, now JCET) and ASE (Taiwan). Freescale's redistributed chip package (RCP) process, is a similar technology that has been licensed to Nepes [2]. Other companies involved in R&D and starting production are J-Devices, TSMC, and others. It is now widely assumed that the Apple A10 processor will be the first large FOWLP produced by TSMC as the InFO package.

Today, FOWLP is dominated by wireless baseband SoC, but this will expand to a broader product portfolio as Yole has shown in its study in 2015 (**Figure 2**). Yole is

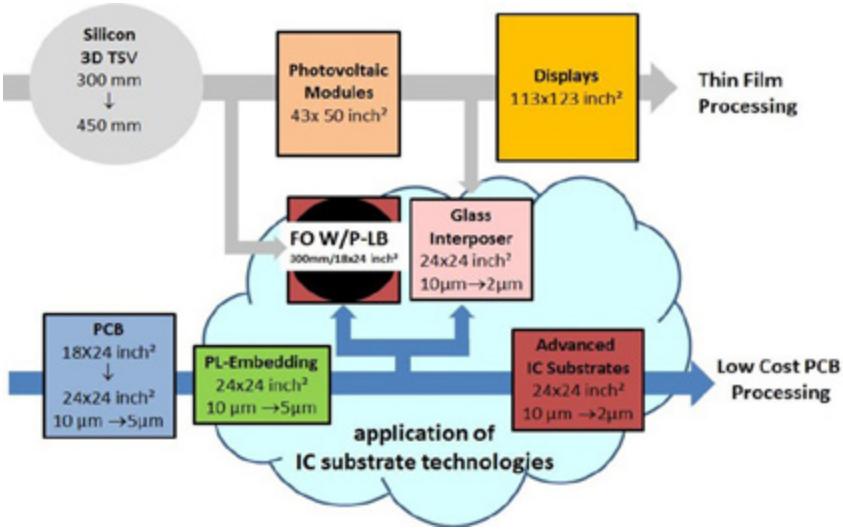


Figure 3: Comparison of thin-film processing infrastructure with PWB.

IZM Panel Level Embedding Line from Wafer Scale to Panel Scale 610 x 456 mm²/24" x 18"

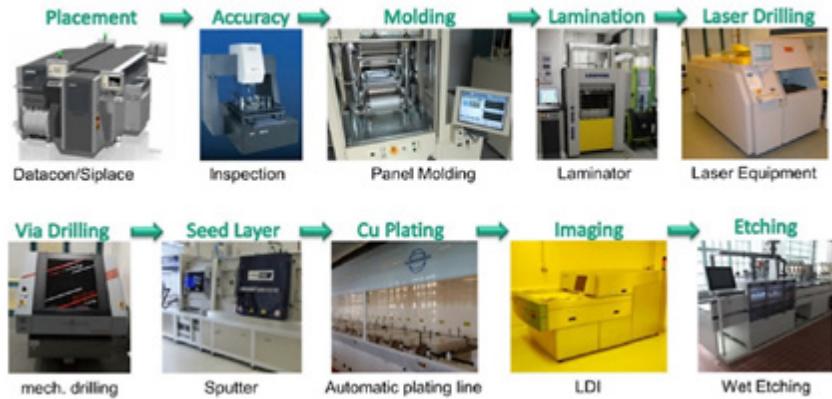


Figure 4: Panel-level line (18" x 24").

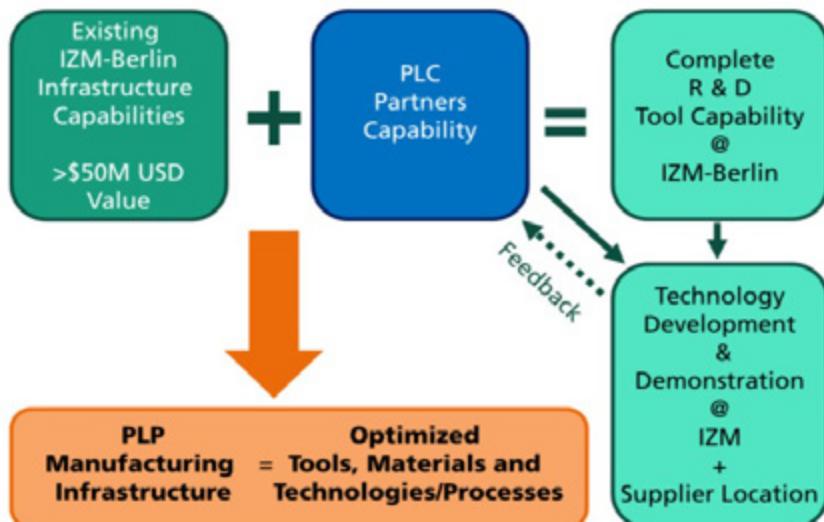


Figure 5: Synergy of the PLP project.

forecasting a packaging market of over \$676M USD for the year 2020. For further cost reduction, the most promising way is to increase the substrate size, which has been successfully proven for the semiconductor, LCD, and PWB industries (Figure 3).

The move of FOWLP from 200mm to 300mm, or to 330mm technology is a dead-end pathway on account of the limits of existing wafer size formats that will not change in the near future. Additionally, the 450mm wafer size is still postponed. The move to panel-level processing will push the technology further to a real low-cost processing. This can be viewed as a merge between the embedded die technology based on PWB infrastructure, and FOWLP technology based on the wafer level [3].

Fraunhofer IZM in Berlin has initiated a Panel Level Packaging Consortium with the goal of acquiring advanced process technology steps for the move to a large format. A fully-equipped wafer processing line for Si wafer and glass wafer sizes between 100 and 300mm is running for prototyping together with a full panel-level line for substrates up to 18" x 24" in size, as shown in Figure 4.

In total, Fraunhofer IZM has invested several millions of euros to install a completely new and state-of-the art panel-level processing line. This investment enables pre-competitive activities to be carried out by the consortium. All partners of the consortium are champions in electronic packaging and add synergy to the panel-level packaging line in Berlin (Figure 5).

The PLP Consortium will be an international, pre-competitive initiative targeting fan-out panel-level packaging and it will aim to develop a reference process ready for industrialization. The project has two levels of membership: full members, and supply chain members, both using the infrastructure of Fraunhofer IZM. Within different thrusts, or areas of interest, the basic requirements of the PLP concept will be explored (Figure 6). Out of the process flow shown in Figure 6, five main areas of interest have been defined: 1) Assembly; 2) Embedding; 3) Redistribution layer (RDL); 4) Cost model; 5) Dissemination and standardization.

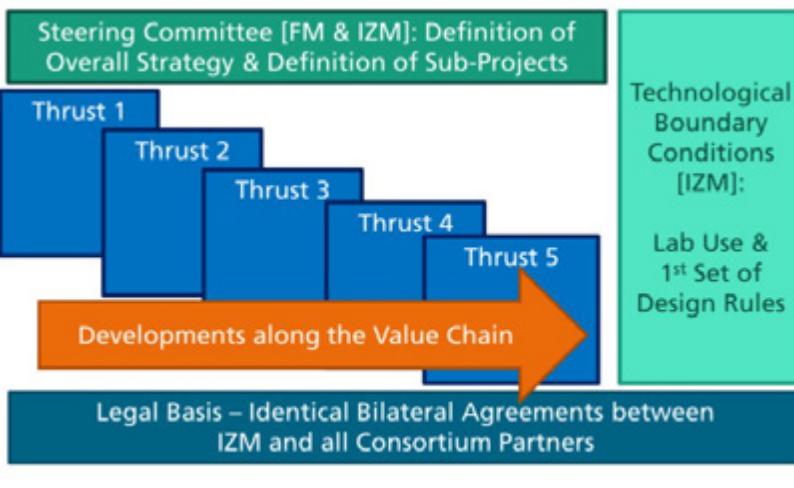


Figure 6: Structure of the PLP Consortium.

Within the consortium's main areas of interest listed above, other detailed sub-projects will be defined based on the interest and participation of the partners. General monitoring and controlling of the research program will be done by the steering committee. A technology focus being developed is a mold-first fan-out panel-level packaging approach. However, within the first year, a basic study on the potential of an RDL-first approach at the panel level will be included. The PLP Consortium is a two-year initiative. The main objectives of the consortium are the evaluation of materials and equipment for world-class PLP technology, the development of all necessary processes, the consolidation of the process flows, the evaluation of yield and cost issues, and the establishment of standardized equipment and material solutions for FOWLP. The research objective of the first year is to explore, develop and demonstrate basic panel-level process steps in close cooperation with the project members. In the second year, technology will be further developed with the goal of higher performance meaning ultra-fine multilayer wiring adopted to demonstrators given by the steering committee. The focus for technology demonstration will be on an RF test vehicle, which will be defined by the partners in the first year of the consortium. In the beginning of the project, a test vehicle will be

designed for process development and material evaluation at Fraunhofer IZM. A test vehicle evaluation kit including different designs will also be provided to the consortium partners for their own evaluations and demonstrations.

Summary

FOWLP is currently the hottest topic in the area of advanced packaging. It is the only process to span the limits of all existing chip packaging technologies with the potential of connecting multi-dies to heterogeneous systems or systems-in-package (SiP) platforms. The main advantages of FOWLP are the substrate-less package that combines lower thermal resistance with higher performance owing to shorter interconnects, together with direct IC connection by thin-film metallization instead of wire bonds or bumps. In particular, the inductance of the FOWLP package is much lower compared to flip-chip ball grid array (FCBGA) packages. In addition, the cost reduction for electronic packages is a key target for the next-generation of electronic products, such as those enabling the IoT (Internet of Things), which have an extreme growth potential. The PLP Consortium is a cooperative effort between Fraunhofer IZM and partners all along the value chain — including end users and OSATS with the following tasks and targets: 1) Providing research excellence and PLP infrastructure at

one place: Fraunhofer IZM in Berlin; 2) End users defining future demands for the package; 3) Equipment and material suppliers working on applied research for process industrialization and driving standardization; and 4) OSATS working on process integration.

Acknowledgment

Readers interested in the Panel Level Packaging Consortium, please contact the lead author.

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Implementing fault detection classification for advanced packaging applications

By Eric Dunton [TEL NEXX]

The backend packaging industry is moving towards fab-wide fault detection and classification (FDC) systems to deliver higher quality end products. Consumable degradation and inherent process variations can challenge advanced packaging engineering teams in their efforts to maintain strict process control. A powerful complement to fab-wide FDC is integrating additional FDC software packages on the process equipment. We have worked to implement e-diagnostic and predictive analysis on our next-generation backend packaging process equipment in efforts to prevent scrap, improve serviceability, and increase yield.

E-diagnostic and predictive analysis software is currently available from multiple software companies. Process and equipment data can be collected in real time from multiple sensors installed on the process equipment. The software then stores and analyzes the data on servers installed on the system allowing quick access by the engineering team and vendor support team. Typically, the data is collected from each module or cell on the process system. The data is then used for real time cell performance analytics, historic cell-to-cell analytics, predictive analytics, preventive maintenance (PM) counters, and consumable lifetime counters, among other uses. Depending on fab requirements and regulations, this data can be accessed either on-site or remotely and input into dashboards present on the process equipment. The dashboards can be used for visual display of the analyzed data for quick review and action in the fab. The signals can be viewed real time or polled for historic performance.

Third party software programs have user-defined models that can manipulate the collected data to identify correlations between the system signals, system performance and/or on-wafer results. Using drag-and-drop model generation, the engineer can shape the collected data to define and generate new data and alarms on the fly. The building blocks for the models

have multiple predefined functions available for use. A quick dump rinse (QDR) is used to rinse wafers after metal plating. Reservoir levels are used to monitor chemical levels for plating processes. **Figures 1** and **2** are examples of two models created on two separate software vendor's platforms. Inputs and outputs can be from collected data signals, constants, reference signals, calculated values, and even from database queries. The model development software allows for collection and manipulation of data that is coming into the system as a string, a number, or a Boolean value. For each type of data entered, there are multiple operations and tests that can be performed, such as comparisons, curve fittings, min/max calculations, and conversions between numbers, strings and Boolean values.

Because of the ease of model generation, users have the ability to create a multitude

of models and workflows. Once a model or workflow has been defined, it can easily be transferred to another system that is running the e-diagnostics package. These models or workflows can include notifications that ensure variations are identified and alert the engineering team. The collection, analysis, and notifications happen in real time as the system is functioning. Because the database is on its own server, there is no impact to system processing. The real time response allows the engineering team to quickly ascertain the impact of the reported deviation and resolve the irregularity prior to impacting the wafers, thereby preventing yield loss.

The generated models can be as simple as putting a guard band on a signal using an offset from a reference point. A simple guard band could be used to validate signal performance and ensure the data is not varying. Because the guard band can be set

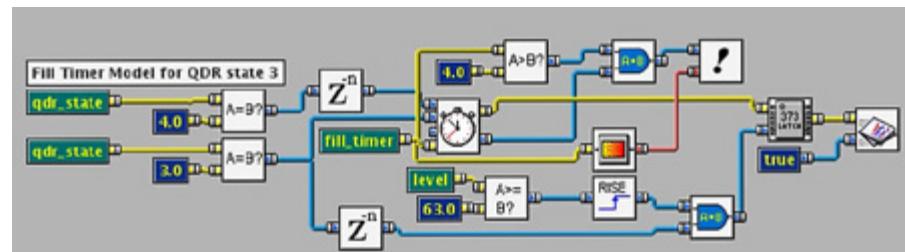


Figure 1: Quick dump rinse fill timer model.

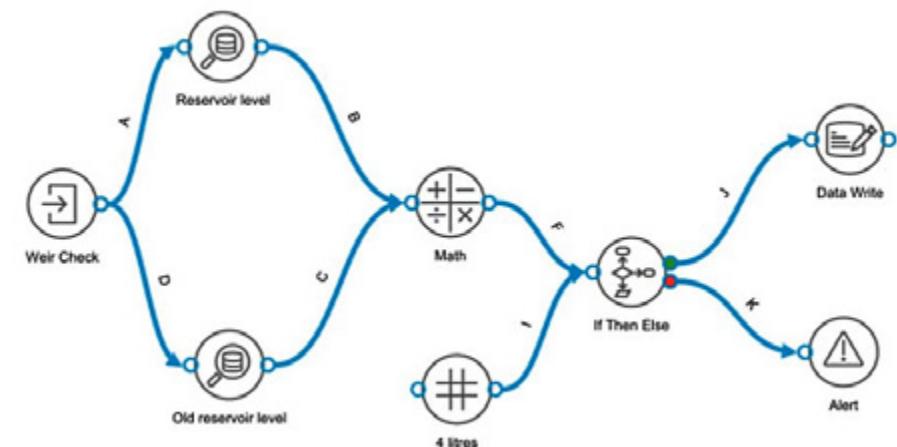


Figure 2: Reservoir level model.

at a percentage of the reference point, there can be different levels of control as shown in **Figure 3**. These can be used in addition to any warning or alarm limits that are included in the system software. The guard bands can be set as tight as needed and notifications can be sent.

The models can be more complex and include manipulation of collected signals to create new signals. Examples of more

complex models are seen when monitoring rinse performance on a plating system. The TEL NEXX Quick Dump Rinse (QDR) module is used to rinse wafers during a process sequence. The wafers enter the QDR module after each metal plating step. The module is then filled with deionized (DI) water where the fill time can be calculated. Once full of water, the wafers will dwell for a time period defined by the process

requirements. During the dwell time, the slope of the level change can be calculated. A large valve is then opened and the water is quickly dumped from the module, allowing the calculation of the dump time. Each QDR cycle may have multiple fill/dwell/dump steps depending on the recipe set up by the process engineer. **Figure 4** shows a single fill/dwell/dump cycle. Several valves are actuated during the process to control the filling, dwelling and dumping of the QDR module. **Figure 5** is an example of a QDR cycle that has an extended fill time. The extended fill time could be attributed to multiple issues such as low DI water pressure, low DI water flow, sticky or slow acting fill or dump valves. Variations in fill or dump times, dwell levels or dwell slopes can be indicators of equipment degradation. If these variations are not addressed or allowed to continue, it is possible that the wafers could suffer yield loss. Multiple models have been created to monitor fill time, dump time, minimum levels during a dwell, and dwell slopes of a rinse cycle. **Figure 1** shows a slightly more complex model developed to monitor the fill time on a rinse cell. Using two pieces of incoming data collected with the e-diagnostics software of `qdr_state` and `level`, the model will generate a fill time value during the process when the `qdr_state` is defined as filling.

The model example shown in **Figure 1** has two outputs. The first output is an alarm that is generated if the fill time is longer than a user definable value (`fill_timer` in this example). The alarm generated can look at other values collected during the run, for example, DI water pressure, to determine the most likely component that is causing the extended fill time. This alarm could include multiple actions such as notification sent to the dashboard, an email sent to the engineering team, or a signal sent to the processing equipment. The second output is a new data point that is equal to the time that it took for the rinse module to fill. This new data value – fill time – is saved in the database and is available for use in later calculations and statistical analysis.

The creation of the new data value allows the engineering team to perform more detailed statistical analysis on the rinse cell performance. The available analysis tools include trends, histograms, multivariable correlations, box plots, and variability plots among others. **Figure 6** shows an example of a box plot chart comparing fill times across multiple rinse cells. The fill time values used to populate the chart in **Figure 6** were

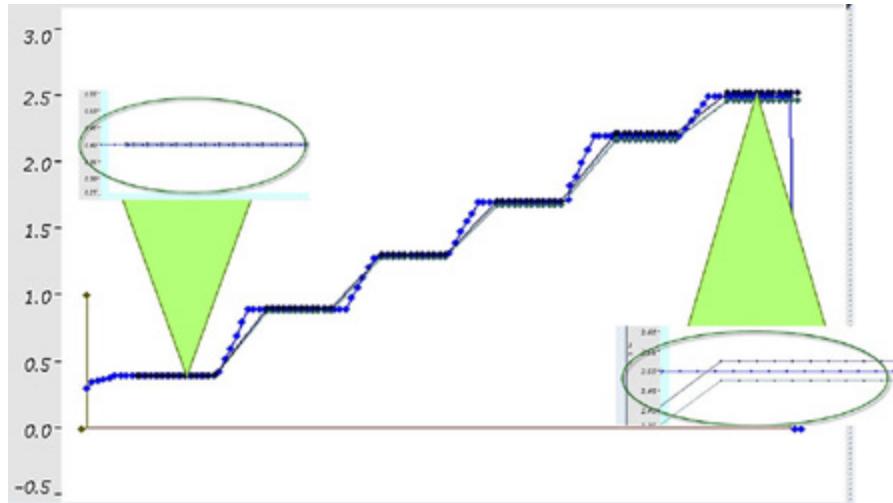


Figure 3: Signal guard band.

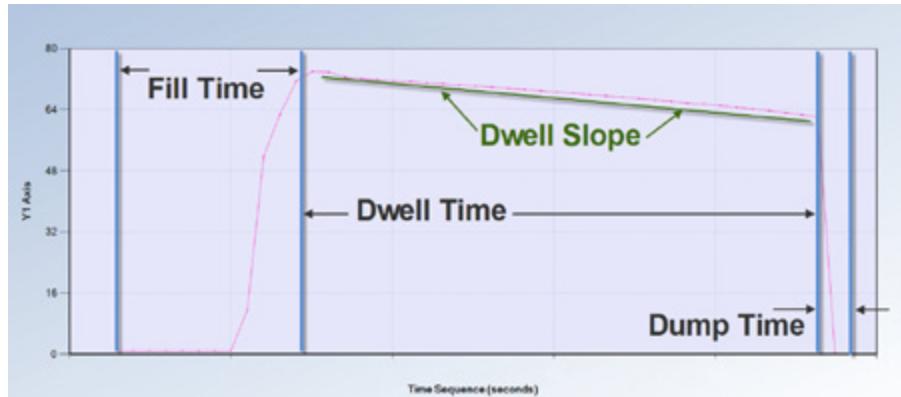


Figure 4: Rinse description.

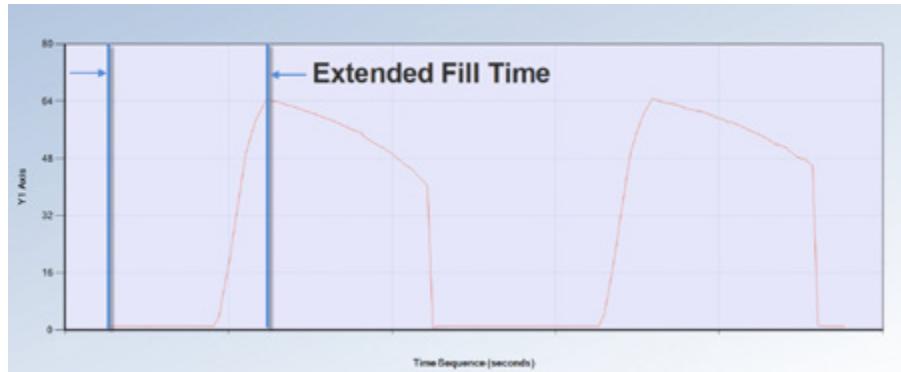


Figure 5: Extended fill time.

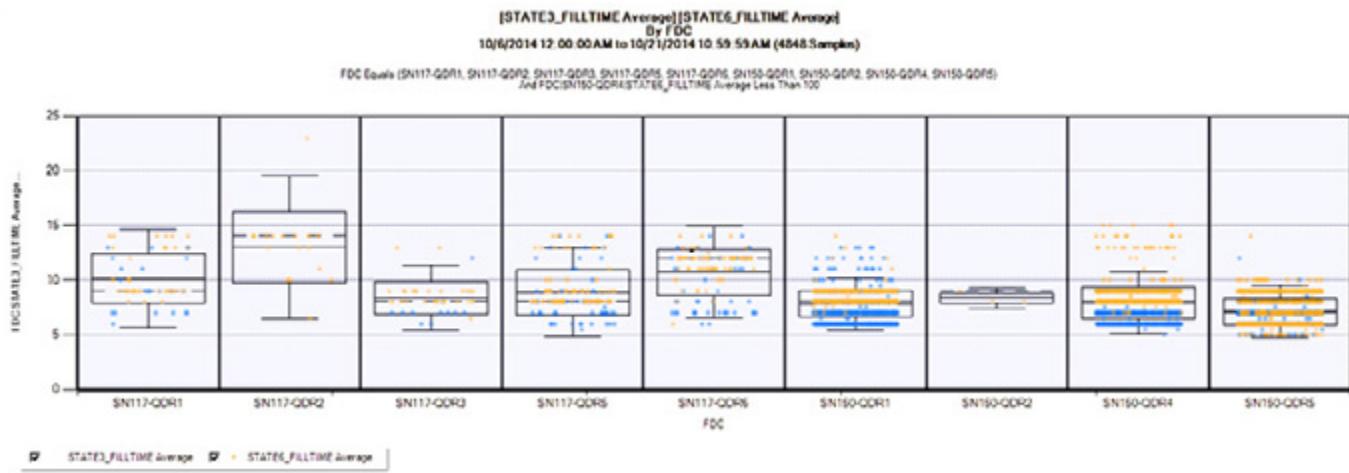


Figure 6: Fill time analysis.

generated by the model shown in **Figure 1**. Having the ability to review and compare statistical data, such as that shown in **Figure 6**, supports the engineering team with quicker review of problems and leads to faster resolution of issues.

Benefits of FDC

The benefits of on-board system FDC are wide ranging. Model creation does not require in-depth software programming knowledge: field service engineers, process engineers, and equipment engineers can all create these models. The vendor engineering team uses its knowledge to build these models and roll them out to multiple systems and customers without requiring system software changes. If the fab allows remote access, another significant benefit is the ability to respond to excursions as soon as they are identified with quick turn solutions. With remote access available to the vendor, equipment and process engineers are able to diagnose and resolve issues remotely saving both time and money. Scrap prevention, serviceability improvements and yield improvements are also possible for packaging fab improvements.

Scrap prevention. The real time aspect of on-board FDC and e-diagnostics can help to reduce scrap events as any variance in process or system performance can be identified immediately. The notification systems that can be used, allow for the engineering team to quickly rectify the differences seen, thereby reducing the chances of a scrap event. A real world example for the packaging industry would be the ability to analyze trends in deposition currents and voltages on plating systems to identify excursion prior to reaching a level that will scrap product.

Serviceability improvements. FDC and

e-diagnostics help to improve serviceability of process equipment in multiple ways. User-defined models can be set up to determine and track the lifetime of system components. Because system responses can be tracked real time, periods between PM activities can be extended. PM activities no longer need to be time dependent. Data review can also be used to determine correct part replacement during PM or unscheduled maintenance actions. Also, using a common set of data collected, for example, a “fingerprint” of system variables, allows for PM quality to be verified prior to releasing systems back to production. This fingerprinting of the process equipment is also useful for startup of a new system.

Yield improvements. In the advanced packaging sector, more and more customers are moving towards 100% bump inspection. With systems that process wafers in multiple cells or modules, it is important to ensure that each cell is performing the same. Slight cell-to-cell, and tool-to-tool, variations can be identified using the FDC and e-diagnostic analysis functions. If these variations are identified and corrected quickly, the fab can improve its overall yield performance. As **Figure 3** shows, cell performance can be tracked and analyzed, looking for any possible divergence from the expected performance. Once a divergence is seen, the e-diagnostics system will alert the engineering team to address the divergence prior to wafer impact.

Moving forward

The models described above are the building blocks upon which more powerful models can be developed to analyze real-time process results and system performance. This is where we start to look at predictive analysis. Utilizing the on-board capabilities of

the data collection we are able to collect large amounts of data. The software is then able to use multivariate analysis (MVA) methods including principal component analysis (PCA) to identify critical process parameters. These benefits could be extended to new developments as they occur.

Summary

The inclusion of FDC, e-diagnostic, and data analysis tools on-board advanced processing equipment expands the capabilities of fab-wide FDC solutions. On-board data collection and analysis tools offer the engineering team the ability to review known issues, highlight possible new issues, develop new models and create new alerts in real time. The engineers are capable of doing this without the requirement for software development resources, thereby saving time and efforts. Once newly created models are validated, they can be put online across multiple systems without the need for system software change. With the rise of the internet of things (IoT) and the increase in the number of sensors available to collect data, the use of on-board analysis allows for automated predictive trouble shooting. Integration of e-diagnostic software on advanced processing equipment allows the equipment vendor and the fab engineering teams improve serviceability, reduce the possibility of scrap, and improve yield performance.

Biography

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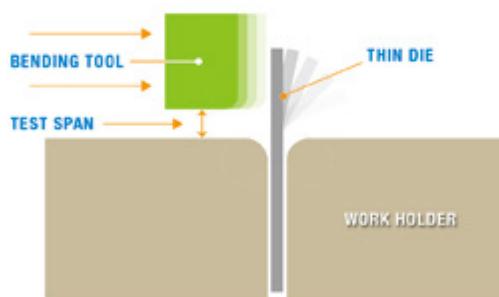
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TSV-less interposers

By John H. Lau [ASM Pacific Technology Ltd.]

Recent advances in through-silicon via-less (TSV-less) interposers such as those developed by Xilinx/SPIIL, Amkor, ASE, Mediatek, Intel, ITRI, Shinko, Cisco/eSilicon, and Samsung/Hynix are discussed in this article. New trends in this technology will also be discussed.

Organic build-up package substrates

Almost 25 years ago, IBM in Japan at Yasu invented the surface laminar circuit (SLC) technology [1-3], which formed the basis of today's very popular low-cost organic package substrates with build-up layers vertically connected through microvias [4] to support flip chips. In general, a package substrate with ten build-up layers (5-2-5) and a 10 μm line width and spacing is more than adequate to support most of the chips.

TSV interposers

In the past few years, because of the very high-density, high I/O count, and ultra-fine pitch requirements, such as the sliced field-programmable gate array (FPGA), even a fourteen-layer (e.g., 2 core layer and 12 build-up layer (6-2-6)) package substrate [5] (**Figure 2** of [6]) is not enough to support the chips, and therefore, a TSV-interposer or 2.5D IC integration is needed [5-11]. For example, the upper left-hand corner of **Figure 1** shows the Xilinx/TSMC's sliced FPBG chip-on-wafer-on-substrate (CoWoS) [9, 10]. It can be seen that the TSV (10 μm diameter) interposer (100 μm deep) has four top redistribution layers (RDLs); three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between FPGA chips are connected mainly by the 0.4 μm pitch (minimum) RDLs of the interposer. The minimum thickness of the conductive wiring and dielectric layer of the RDLs is ~1 μm . Each sliced FPGA has more than 50,000 microbumps (200,000+ micro bumps on

the interposer) at 45 μm pitch. So far, using a TSV-interposer is very expensive [12-14]. In order to lower the cost, enhance the electrical performance, and reduce the package profile, some TSV-less interposers have been proposed in the past three years, which are the focus of this study.

Various TSV-less interposer technologies

Below is a summary of a number of TSV-less interposer technologies that have been introduced to the industry.

TSV-less interposer: Xilinx/SPIIL's SLIT. In 2014, Xilinx/SPIIL proposed a TSV-less interposer for sliced FPGA chips called silicon-less interconnect technology (SLIT) [15]. The upper right-hand corner of **Figure 1** shows the new packaging structure along with the old one, which is shown in the left-hand corner. It can be seen that the TSVs and most of the interposer are eliminated and only the four RDLs needed for performance, mainly, the lateral communication of the sliced FPGA chips, remain.

The SLIT process flow is shown in **Figure 2**. It starts off by fabricating the RDLs—examples on a bare silicon wafer can be seen in [16, 17] (**Figure**

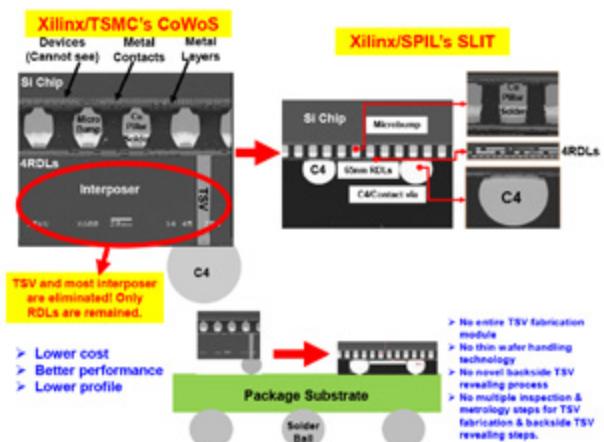


Figure 1: TSV-less interposer: Xilinx/SPIL's SLIT technology.

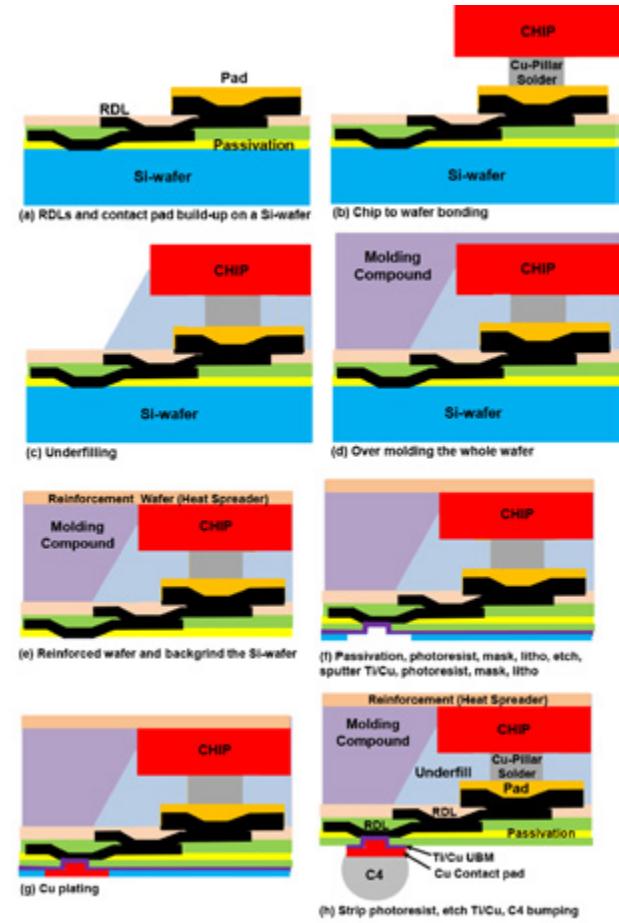


Figure 2: Process flow for implementing SLIT technology.

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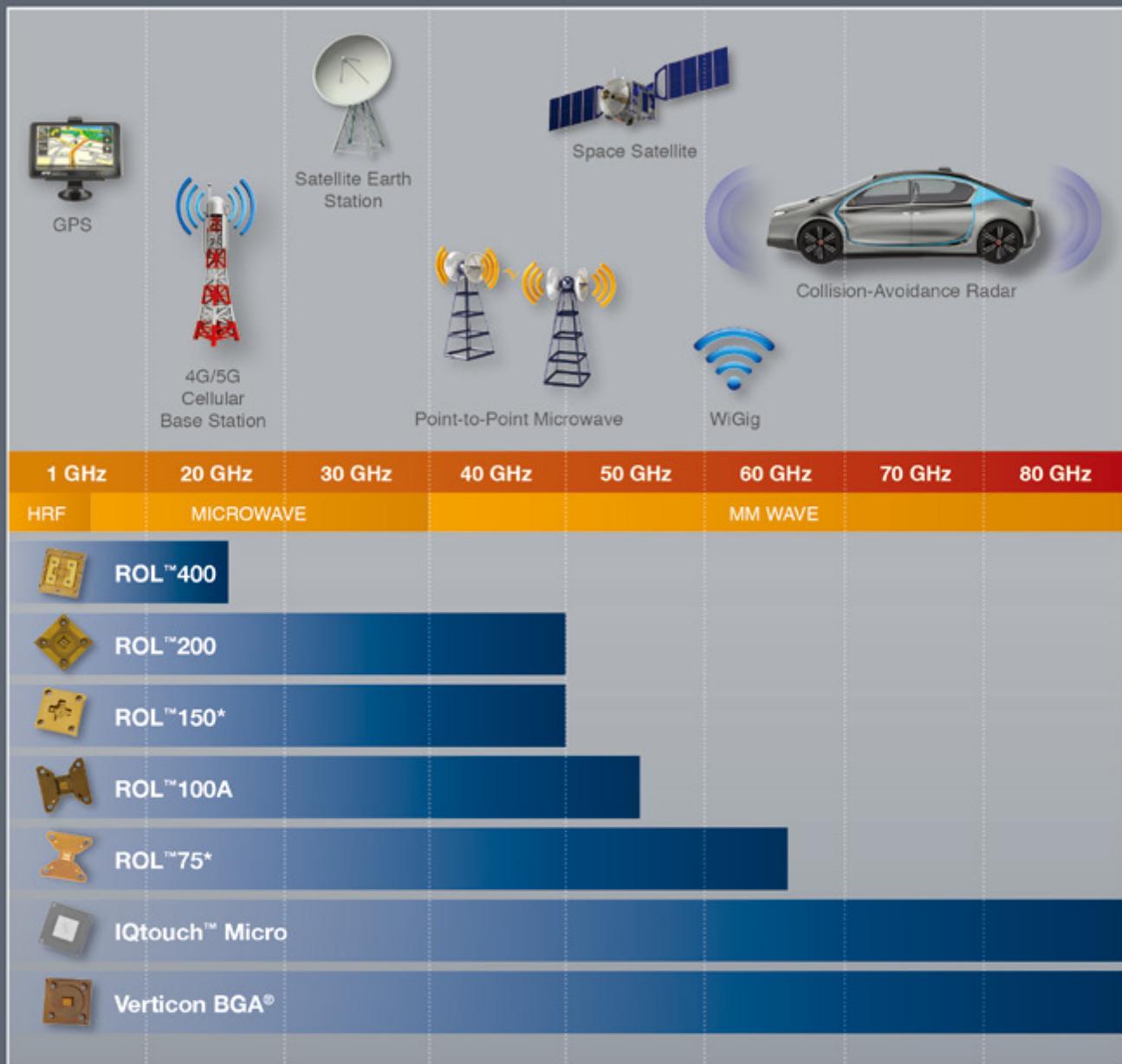
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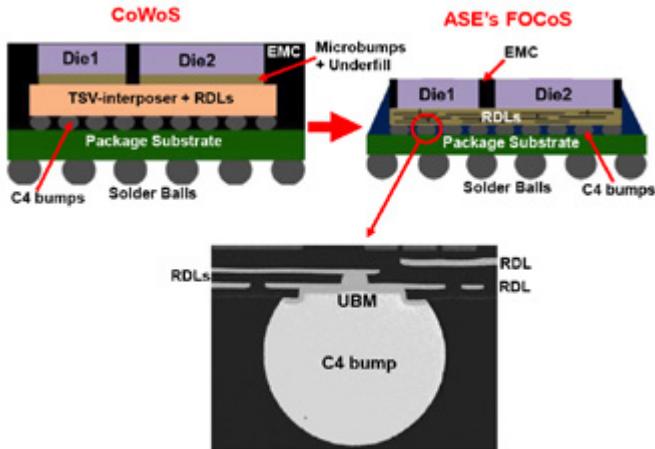


Figure 3: TSV-less interposer: ASE's FOCoS.

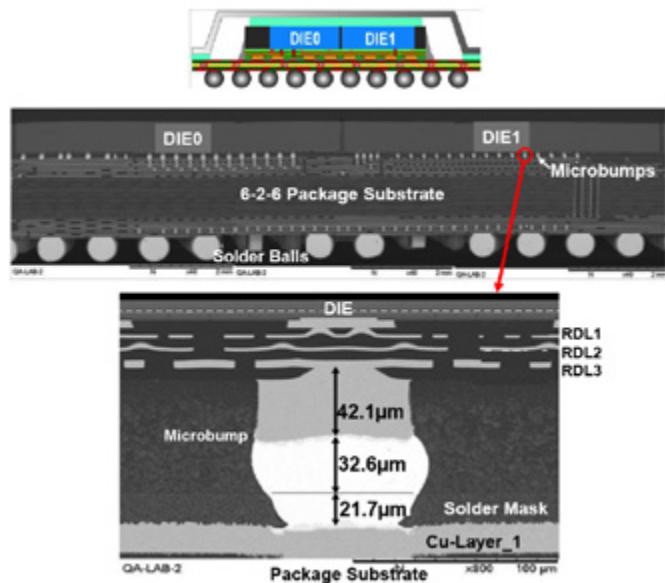


Figure 4: TSV-less interposer: Mediatek's RDLs by FOWLP.

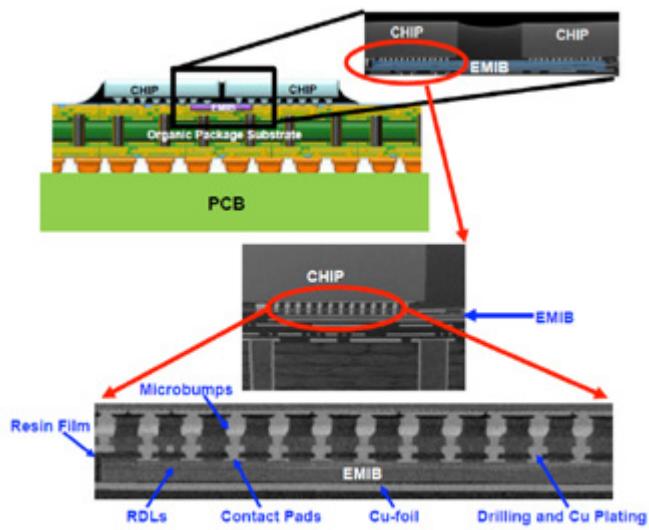


Figure 5: TSV-less interposer: Intel's EMIB.

2a). That process is followed by chip-to-wafer bonding (i.e., bonding the FPGA chip to the silicon wafer with RDLs; **Figure 2b**), and underfilling/curing (**Figure 2c**).

These processes are followed by over molding the whole wafer with an epoxy mold compound (EMC) (**Figure 2d**). It is followed by backgrinding the over mold to expose the backside of the chips and attaching an optional reinforcement wafer on the backside of the chips (**Figure 2e**).

Then come passivation, photoresist, mask, patterning, etching, sputtering TiCu, photoresist, mask, and patterning (**Figure 2f**). Finally, Cu contact-pad plating (**Figure 2g**), photoresist stripping, TiCu etching, and controlled-collapse chip connection (C4) wafer bumping are done (**Figure 2h**).

Depending on the linewidth/spacing of the RDLs' conductive wiring, the fabrication method of the RDLs can be accomplished either by using a polymer for the dielectric layer and Cu plating of the conductive wiring (line width/spacing $\geq 5\mu\text{m}$), or by using plasma-enhanced chemical vapor deposition (PECVD) to make the SiO₂

dielectric layer and Cu damascene plus chemical mechanical polishing (CMP) to make the conductive wiring (linewidth/spacing $< 5\mu\text{m}$). In 2016, SPIEL/Xilinx published a similar paper [18] with more characterization results including warpage data and called it non-TSV interposer (NTI).

TSV-less interposer: Amkor's SLIM. In 2015, Amkor announced a very similar technology to SLIT and is called silicon interposer-less integrated module (SLIM) [19].

TSV-less interposer: ASE's FOCoS. In 2016, ASE [20] proposed using the fan-out wafer-level packaging (FOWLP) technology (chip-first and die-down on a temporary wafer carrier and then over molded by the compression method [21, 22]) to make the RDLs for the chips to perform mostly lateral communications as shown in **Figure 3**; the technology is called fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 bump as shown in **Figure 3**.

TSV-less interposer: Mediatek's RDLs by FOWLP. In 2016, Mediatek [23] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in **Figure 4**. Instead of the C4 bump, they used a microbump (Cu-pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate.

TSV-less interposer: Intel's EMIB. Intel proposed an embedded multi-die interconnect bridge (EMIB) [24] to replace the TSV interposer. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the organic package substrate as shown in **Figure 5** [25]. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB.

To make the EMIB, one must first build the RDLs (including the contact pads) on a Si-wafer. The way to make the RDLs depends on the line width/spacing of the conductive wiring of the RDLs. Finally, attach the non-RDL side of the Si-wafer to a die-attach film, and then singulate the Si-wafer.

To make the substrate with an EMIB, first place the singulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate (**Figure 6a**). It is followed by laminating a resin film on the whole organic package substrate. Then, drilling (on epoxy resin) and Cu plating to fill the holes (vias) to make connections to the contact pads of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown in **Figure 6b**. Then, it is followed by laminating another resin film on the whole substrate and drilling (on resin) and Cu plating to fill the holes and make contact pads (**Figure 6c**). (Smaller pads on a finer pitch are for microbumps, while larger pads on a gross pitch are for ordinary bumps.) The organic package substrate with an EMIB is ready for bonding of the chips as shown in **Figure 6d**.

Figure 7 shows AMD's Radeon R9 Fury X GPU (graphic processor unit) shipped in the second half of 2015. The GPU is built on TSMC's 28nm process technology and is supported by four high-bandwidth memory (HBM) cubes manufactured by Hynix. Each cube consists of four dynamic random access memories (DRAMs) and a logic base with TSVs straight through them. The GPU and HBM cubes are on top of a TSV interposer, which is fabricated by UMC with a 64nm process technology. The final assembly of the TSV interposer on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

On November 9, 2015, Altera/Intel announced [26] the industry's first heterogeneous system-in-package (SiP) devices that integrate stacked HBM from SK Hynix with high-performance Stratix® 10 FPGAs and SoCs as shown in **Figure 8**. It can be seen that the TSV interposer is gone and replaced by Intel's EMIB.

It is interesting to note that in order to use the EMIB, the chips will have different kinds/sizes of bumps as shown in **Figure 8**, i.e., C4 bumps and microbumps (Cu-pillar + solder cap). Wafer bumping and flip-chip assembly could be challenging.

TSV-less interposer: ITRI's TSH. On August 16, 2012, ITRI proposed the use of a through-silicon hole (TSH) interposer to replace the TSV interposer

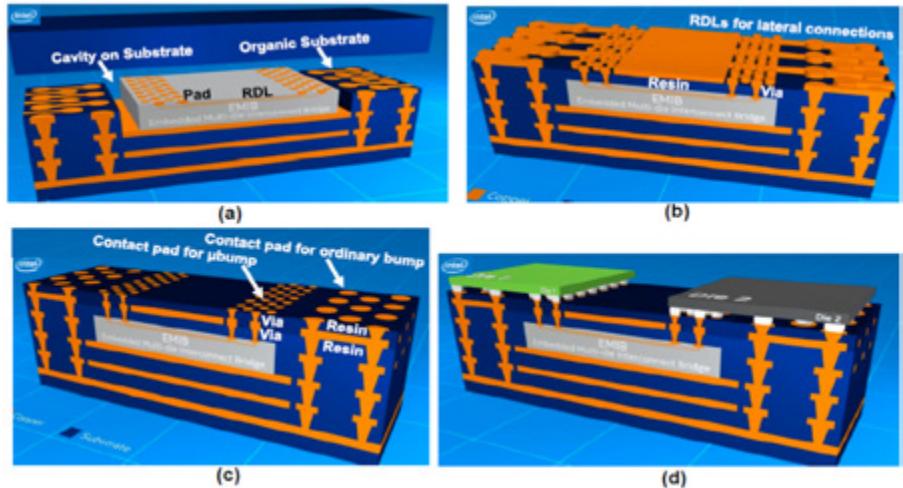


Figure 6: Process flow in making the package substrate with EMIB.

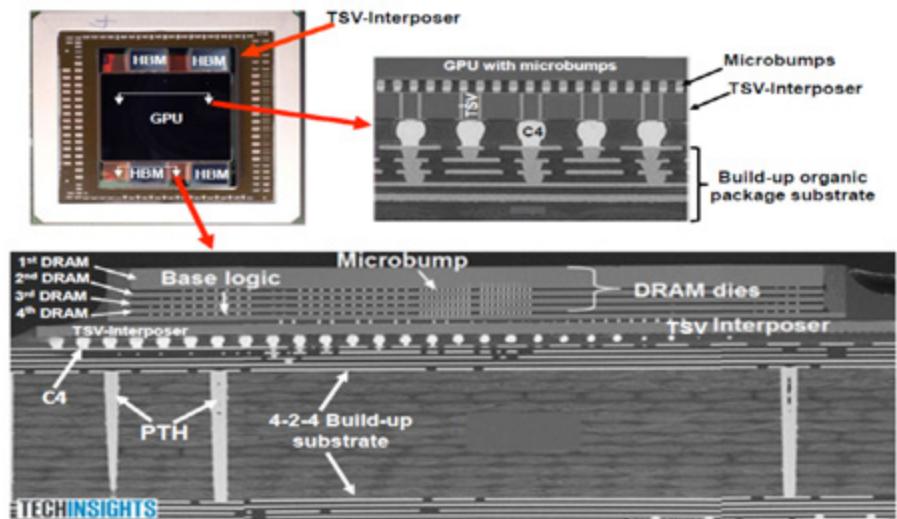


Figure 7: AMD's GPU with HBM on a TSV interposer.

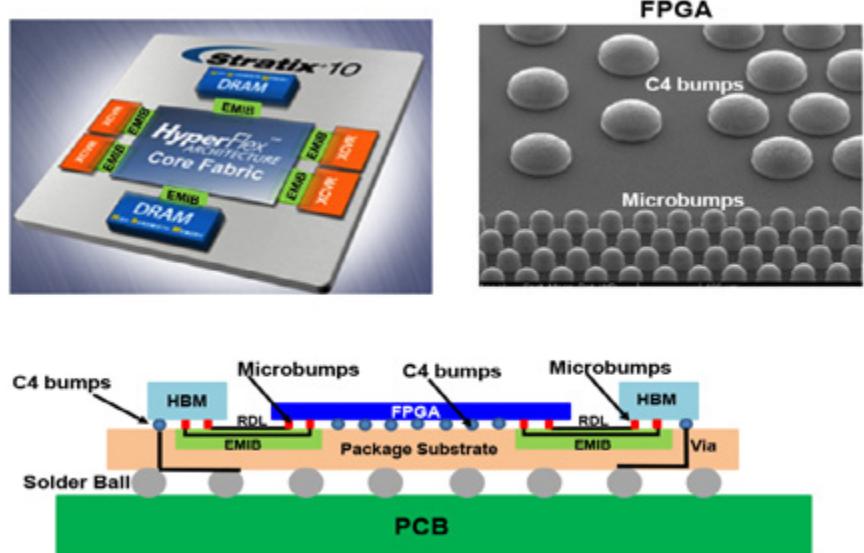


Figure 8: Heterogeneous integration using Intel's EMIB and Altera's FPGA technology.

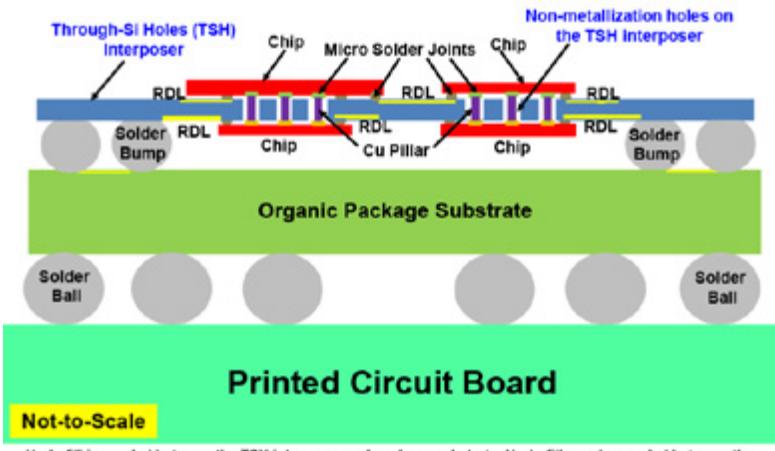


Figure 9: TSV-less interposer: ITRI's TSH.

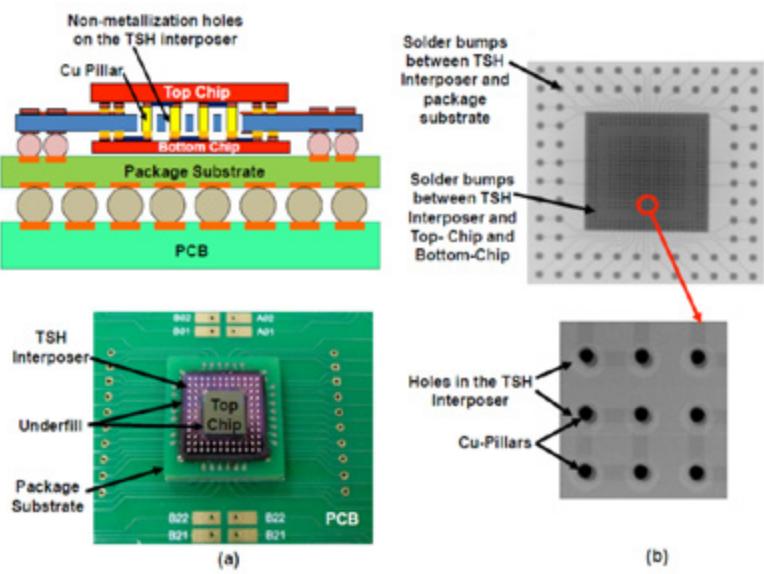


Figure 10: ITRI's TSH: a) Test vehicle; and b) X-ray images.

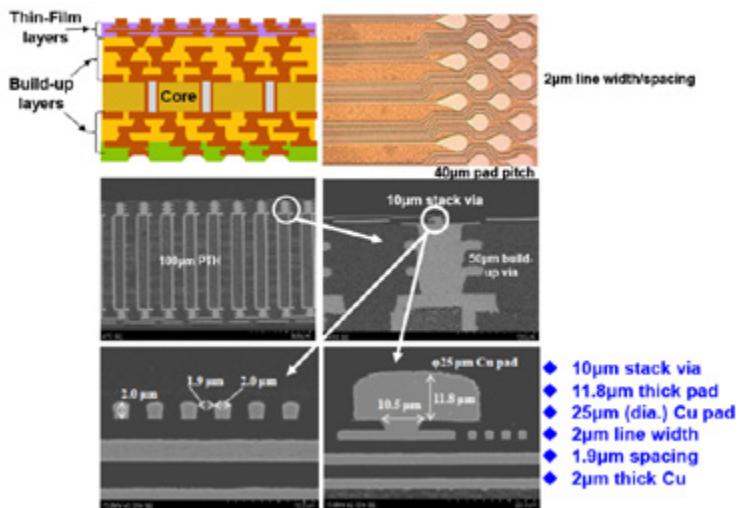


Figure 11: TSV-less interposer: Shinko's i-THOP.

[27-29]. **Figure 9** shows a TSH interposer supporting a few chips on its top and bottom sides. The key feature of TSH interposers is that there is no metallization in the holes and the dielectric layer, barrier and seed layers, via filling, CMP for removing overburden copper, and Cu revealing are all eliminated. Compared with the TSV interposers, TSH interposers only need to make holes by either laser, or deep-reactive ion etching (DRIE) on a piece of silicon wafer. Just like the TSV interposers, RDLs are needed by the TSH interposers for lateral communication of chips.

The TSH interposers can be used to support chips on the top side as well as the bottom side. The holes can let the signals coming from the chips on the bottom side be transmitted to the chips on the top side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH interposer. Physically, the top and bottom chips are connected through Cu pillars and micro solder joints. In addition, the peripherals of all the chips are soldered to the TSH interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom side of the TSH interposer have ordinary solder bumps that are attached to a package substrate.

The test vehicle is shown in **Figure 10a**. It comprises a TSH interposer, which is supporting a top chip with Cu pillars and a bottom chip with UBM and solder. The interposer module is connected to a package substrate and then attached to a PCB. **Figure 10b** shows the x-ray images of the final assembly. It can be seen that: a) the Cu pillars are not touching the side wall of the TSH interposer, and b) the Cu pillars are almost at the center of the TSH. It has been shown [28] that the electrical performance of the TSH interposer is better than that of the TSV interposer. Also, the structural integrity of the TSH interposer assembly has been demonstrated by drop and thermal cycling tests [29].

TSV-less interposer: Shinko's i-THOP. In 2013, in order to replace the TSV interposer, Shinko proposed making thin-film layers on top of the build-up layer of an organic package substrate. **Figure 11** shows Shinko's integrated thin-film high-density organic package (i-THOP) substrate [30] for very high-performance applications. It is a 4+(2-2-3) test vehicle, which means there is a two-layer metal core, three build-up metal layers at the bottom (PCB) side, two build-up metal layers on the top (chip) side, and the first number "4" represents that there are four thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer. The thickness, line width and spacing of the Cu RDLs can be as small as 2μm. The thin-film Cu RDLs are vertically connected through a 10μm via, as shown in **Figure 11**. The surface Cu pad pitch is 40μm and the Cu pad diameter is 25μm with a height of 10 to 12μm. The i-THOP substrate passed the warpage and reliability tests and there was no via delamination observed [30].

In 2014, Shinko demonstrated that [31] ultra-fine pitch flip-chips can be successfully assembled on the i-THOP substrate. **Figure 12** shows the two chips' lateral

communications by the 2 μ m line width/spacing RDLs of the two thin-film layers, which are built on top of the 1-2-2 build-up organic substrate: 2+(1-2-2). **Figure 12** shows the 40 μ m pitch microbumps (Cu-pillar + Ni + SnAg) of the test chips and the 40 μ m pitch of the flip-chip bonding pads (25 μ m diameter). Typical images of the cross section of the flip-chip assembly with optimized conditions are shown in **Figure 13**. It can be seen that good solder joints are confirmed at all areas of the assembly [31].

TSV-less interposer: Cisco/eSilicon's organic interposer. **Figure 14** shows a 3D system-in-package (SiP) designed and manufactured with a large organic interposer with fine-pitch and fine-line interconnections by Cisco/eSilicon [32]. The organic interposer has a size of 38mm x 30mm x 0.4mm. The linewidth, spacing, and thickness of the front-side and back-side of the organic interposer are the same and are, respectively, 6 μ m, 6 μ m, and 10 μ m. A high-performance application-specific IC (ASIC) die measured at 19.1mm x 24mm x 0.75mm is attached on top of the organic interposer along with four HBM DRAM die stacks. The 3D HBM die stack with a size of 5.5mm x 7.7mm x 0.48mm includes one base buffer die and four DRAM core dice which are interconnected with TSVs and fine-pitch micro-pillars. (This structure is very similar to AMD's, except Cisco/eSilicon used the lower-cost organic interposer instead of the higher-cost TSV interposer.)

TSV-less interposer: Samsung/Hynix's organic interposer. During the IEEE Hot Chips Conference (Aug. 21–23, 2016), Samsung/Hynix announced [33, 34] the HBM3, which is also called “low-cost HBM.” The TSV-interposer, just like with the Cisco/eSilicon version, will be replaced by an organic interposer.

Summary

Recent advances in TSV-less interposers have been investigated in this study. Some important results and recommendations are as follows:

TSVs are best used for device chips such as TSVs straight through the same DRAMs (3D IC integration) to enlarge the memory capacity, lower the power consumption, increase the bandwidth, lower the latency, and reduce the form factor.

An interposer (2.5D IC integration) is just a piece of dummy silicon (a part of the package substrate) without devices but with TSVs and RDLs. Because TSVs involve many semiconductor processes, e.g., DRIE, PECVD, physical vapor deposition, electrochemical deposition, CMP, and Cu revealing, TSV technology is very expensive for a package substrate. In order to lower the cost, the TSV should be eliminated from the interposer, i.e., a TSV-less interposer, such as those developed by Xilinx/SPIL [15], Amkor [19], SPIL/Xilinx [16], ASE [20], Mediatek [23], Intel [25–26], ITRI [27–29], Shinko [30–31], Cisco/eSilicon [32], and Samsung/Hynix [33,34]. More research and development should be done on innovative interposer (package substrate) solutions without using the TSVs for high-density and high-performance flip-chip applications.

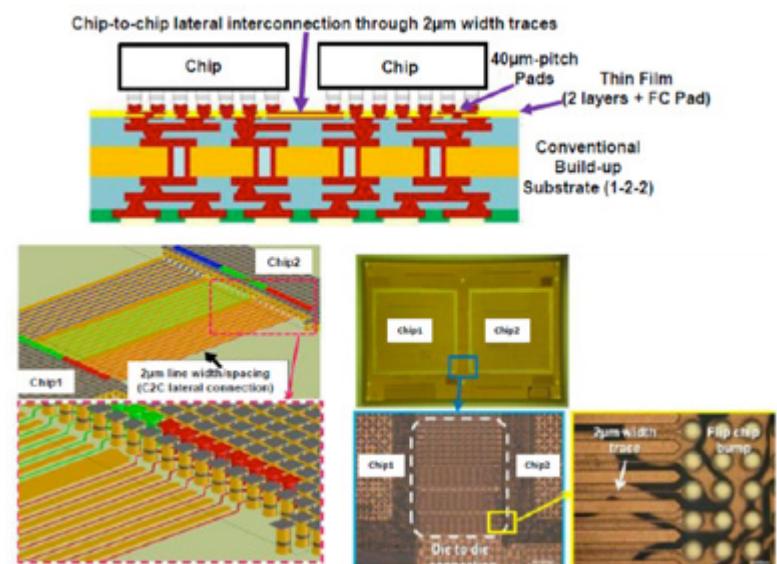


Figure 12: Shinko's i-THOP test vehicle.

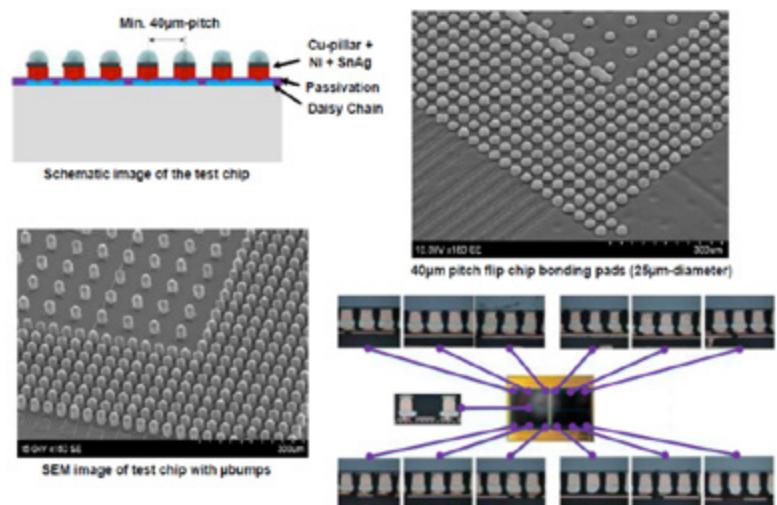


Figure 13: Shinko's i-THOP test chip, substrate, and assembly.

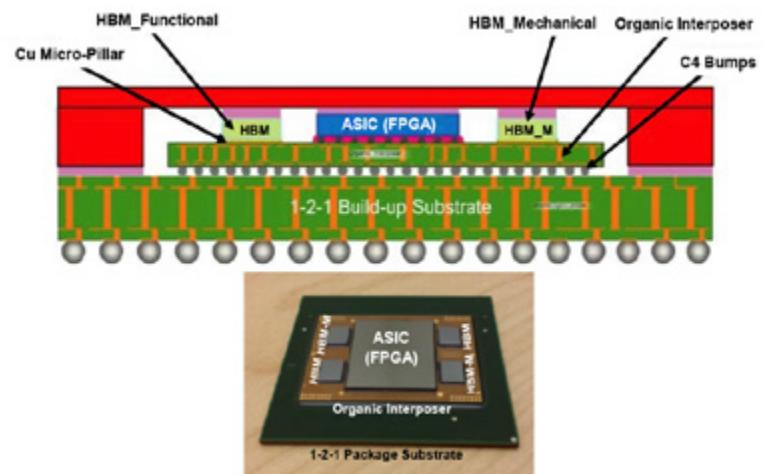


Figure 14: Cisco/eSilicon's TSV-less interposer for 3D SiP.

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continued on page 62

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Advances in high-reliability, hermetic MEMS CSP

By Doug Sparks [Hanking Electronics LLC]

Many MEMS devices such as gyroscopes, oscillators, FBARs, accelerometers, pressure and IR sensors, rely on wafer-level packaging to produce vacuum-sealed silicon chip-scale packages (CSP). Hermeticity of these CSPs is critical for many applications, especially automotive, aerospace, and industrial sensors and actuators that must operate in the field under warranty for 10 to 20 years. Helium, neon and krypton pressurized bomb testing is the most common method of checking the reliability of electronic packages [1,2]. This testing method typically involves pressures of 210-520 KPa for 1 to 16 hours. To date, no silicon MEMS CSP has been found that remains hermetic long-term (>40 hours) in pressurized helium [3,4]. MEMS devices such as gyroscope resonators and Pirani gauges can pass long-term helium pressure testing when packaged in ceramic or metal packages [4], however these packages are larger and more expensive than CSP devices and this solution precludes the use of MEMS sensors in gas applications that involve continuous helium or hydrogen exposure. Because of this limitation, work was undertaken to develop a MEMS CSP for improved high-reliability devices like gyros and oscillators that require vacuum packaging and MEMS gas sensors, which can be used in pressurized helium and hydrogen applications.

Prior work in this area with resonators, pressure sensors and Pirani gauges have shown helium ingress into Si CSPs that were formed using wafer-to-wafer bonding methods such as reflowed glass frit, silicon direct bonding, anodic bonding, Au-Si eutectic bonding [3,4], as well as CVD oxide and polysilicon sealing [5]. Because of the use of different sensing devices and thicknesses in the silicon cavity walls, results of past hermeticity studies have failed to indicate if helium ingress was due to leaking, or effusion through the sealing interfaces, or diffusion through the silicon cavity walls.

For an ideal comparison between different packaging methods and fabs, the same device and package wall thicknesses are

desired. Experimentally, in this study, the same sensor, a vacuum-sealed piezoresistive pressure sensor (Figure 1) was employed for all wafer bonding methods. This device provides an easy way to change wafer bonding methods without a mask design change. In addition, many commercial samples can be obtained with the same low-pressure sensitivity range for a comparison between different bonding methods and wafer fabs. The MEMS sensors tested in this paper came from five different MEMS fabs. The silicon diaphragm thickness of the experimental and commercial samples varied between 20 and 25 microns, which is a much closer range than past hermeticity studies of different MEMS devices. This type of chip is essentially a vacuum-sealed MEMS cube with one side thinned to form a diaphragm with a built-in strain gauge. As the internal cavity pressure changes due to helium ingress, the diaphragm deflection will change resulting in an offset change in the Wheatstone bridge.

Experimentally, absolute pressure sensors were made using silicon-to-silicon direct bonding employing opposing wafer surfaces that were polished starting material. An EVG 850 with an ultrasonic spray clean was used prior to bonding, and an infrared (IR) inspection was done after bonding, followed by a high-temperature anneal. The EVG 850 is designed for Si-Si wafer bonding

for silicon direct bonding. Wafer bonding experiments using metal-to-metal sealing were done on an EVG 520 bond system and post-bonding inspection was done using an ultrasonic inspection system. Commercially available absolute pressure sensors were also obtained that used silicon-to-glass anodic bonding, from two different companies and hence, wafer fabs, as well as silicon-to-silicon bonding using reflowed glass sealing material and parts using silicon-to-silicon direct bonding. The commercial parts using the reflowed frit glass and silicon direct bonding had an IC amplifier connected to the Wheatstone bridge. The vacuum cavity was not centered in these chips resulting in a seal width ranging from 100 to 400 microns.

After bonding, dicing and wire bonding, the sensors were tested and then subjected to long-term helium pressure testing. Figures 2 and 3 show how the bridge offset voltage

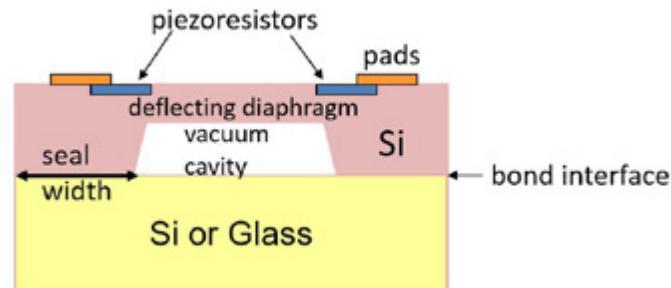


Figure 1: MEMS pressure sensor cross section.

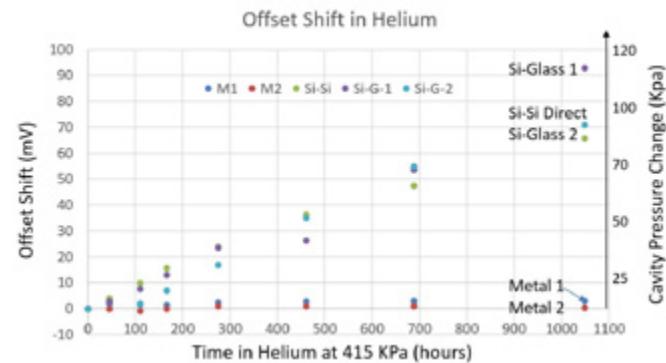


Figure 2: Bridge offset vs. time in helium for the Wheatstone bridge MEMS. and is considered the best in class method and therefore, internal cavity pressure,

Low-Stress Debonding

changed over time during the MEMS chips' exposure to high-pressure helium (415KPa; 60psi). While the majority of the CSP parts did show ingress of helium, the Metal Seal #2 parts did not show any indication of helium ingress. Unlike prior work, this study found a wafer-to-wafer bonding method that enabled diced, vacuum-bonded chip-scaled packages to pass 1000 hour, high-pressure helium testing with no change in sensor output due to helium ingress.

Comparative helium pressure testing of various bonding method with the same sensor type resulted in different leak rates, indicating that the sealing method, not helium diffusion through silicon, is the cause for loss of helium hermeticity. Metal Seal #1 parts showed a slow helium ingress issue, while the silicon direct and anodically-bonded silicon-to-glass bonded parts showed a much faster change in bridge output or cavity pressure over time. For the commercial pressure sensors with an amplified output (Figures 3), the silicon-to-silicon direct bonded parts shifted 24 times faster than the silicon-reflowed frit glass-silicon bonded parts did. Clearly, helium diffusion through the silicon diaphragm is not the cause for the helium ingress into the vacuum cavity.

As Figures 2 and 3 show, wafer-to-wafer vacuum bonding with silicon-to-silicon direct, anodic silicon-to-glass and silicon-to-silicon bonding using a reflowed frit glass resulted in helium ingress into the vacuum cavity. The differences on sensor output changes with helium exposure time suggest that helium effusion through the different types of bonding interfaces, not diffusion through the thin silicon diaphragm, was the mechanism for helium ingress into the cavity. Wafer bonding using a liquified metal seal performed the best in slowing, and for Metal 2, preventing helium penetration into the vacuum cavity.

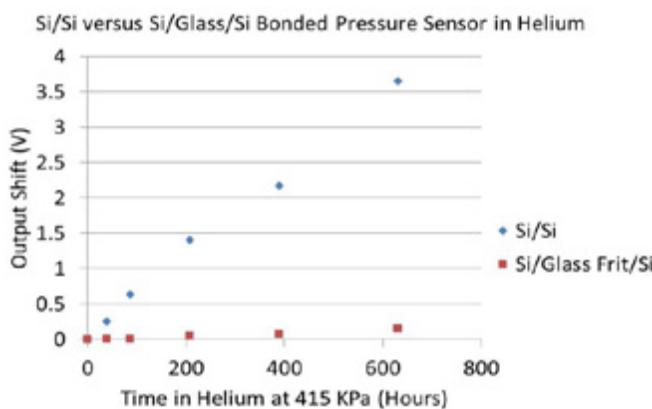


Figure 3: Amplified output shift of commercially available absolute MEMS pressure sensors that use silicon/silicon direct and silicon/glass frit/silicon wafer bonding in vacuum.

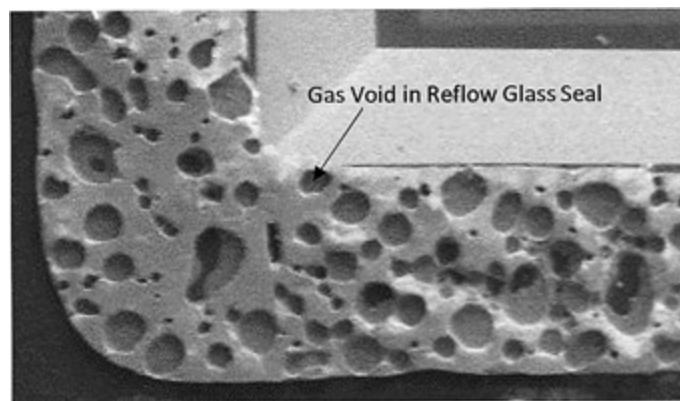
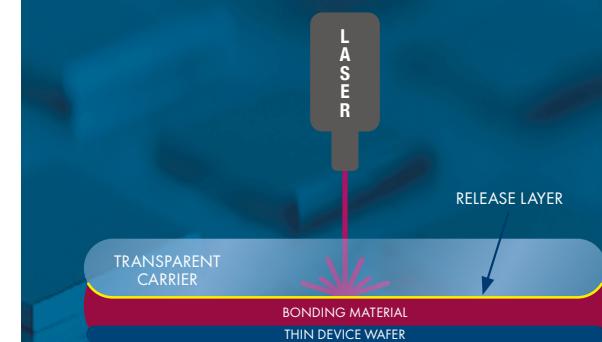


Figure 4: Gas bubble voids in a reflowed glass seal.

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Reflowed metals and glass are more conformal and can cover particles, scratches and other surface topography challenges. Glass is reported to have a faster gas permeation rate than metal seals [6] and as **Figures 4** shows, can contain voids due to trapped, frit paste binder-related organic gases, and oxygen from lead oxide reduction. Organic contamination and surface oxidation can result in voids with metal seals as well. **Figures 5** shows an example of a void found using ultrasonic inspection of one of the

experimental wafers sealed using reflowed metal. Oxidation of surfaces can be caused by the diffusion of the adhesion layer metals (Ti, W) through the metal solder bond surface. This situation can occur during wafer bonding or a pre-bonding degas bake. A reducing gas can be employed to eliminate this thin oxide layer during the bonding process.

Improvements in any wafer bonding process can be obtained by varying the bonding temperature, ambient gas, or vacuum levels, bonding force, time, and

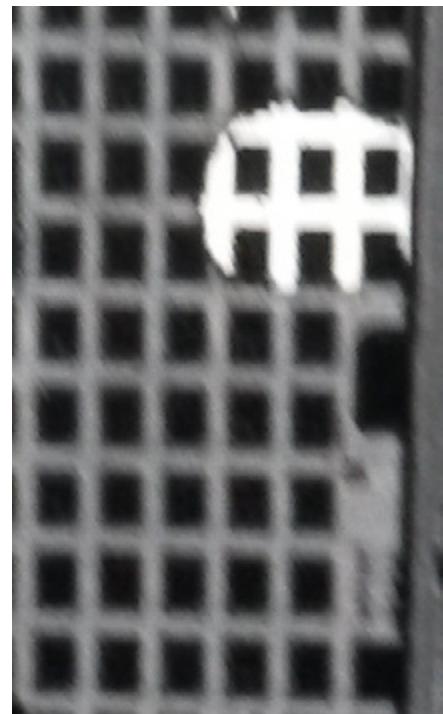


Figure 5: Void formed in a metal-to-metal sealed wafer stack.

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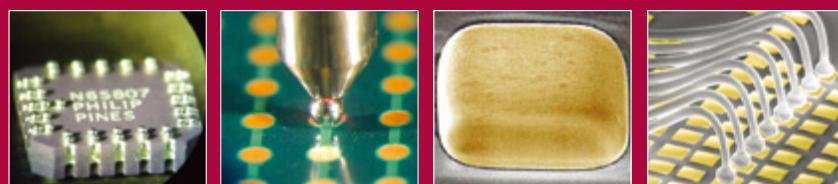
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Eutectic Alloy/Metal	Melting Point (°C)
In	157
Sn	231
Cu-Sn	231
Ag-Sn	250
Au-Sn	260
Ni-Sn	300
Au-Si	363
Al-Ge	419

Table 1: The melting point of various metals and alloys used in wafer-to-wafer bonding.

changing the reflowed metals or opposing surface metals. **Table 1** gives examples of some of the potential metal seal materials and their melting points. Some eutectic metal bonding combinations, such as Si to Au, are most commonly employed with one material like silicon on the device wafers, while the other bonding material - gold in this case - will be patterned on the opposing capping wafer. Ideally, the entire opposing surface seal ring will meet at the peak temperature, forming a lower melting point eutectic interface that does form a liquid interface. In reality, particles or scratches of a hard surface (silicon) may prevent this contact during the bonding process resulting in a possible interface leak where the low melting point eutectic alloy does not form. Prior work with AuSi eutectic bonding [4] found the devices would pass a 90 hour helium pressure test,



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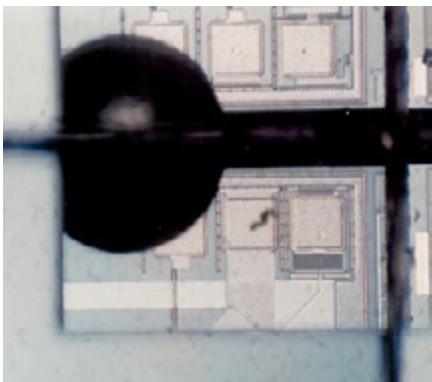


Figure 6: Solder ball formed during wafer bonding and extending into the bond pad area.

which, according to Jarrett [2], extrapolates to a 10-15 year lifetime in air for a typical MEMS gyroscope application. These same CSP devices failed during longer helium storage, which indicates that they would not be suitable for a gas sensing application.

The current experiments indicate that helium-proof CSP packaging is obtainable if a metal seal wafer bonding process is employed that uses a metal that forms its liquid phase during the bond process. It is up to the user to determine the ideal process for

the application and type of metal bond that is compatible with the application. While a liquid metal or solder seal is needed to form a long-term hermetic CSP seal, too much of a good thing can have risks. **Figure 6** shows a solder ball that formed during the wafer bond process of a MEMS gyro that extended into the bond pad area of the chip. Metal seal thickness, design and bonding force must be optimized to provide a high-yield, hermetic product without undesired defects like that shown in **Figures 6**.

Summary

CSP vacuum packaging of MEMS devices has been found to have varied hermeticity performance during long-term pressurized helium testing. Wafer-to-wafer bonding using reflowed metal seals was found in this study to provide the best performance and for at least one type of metal seal a long-term helium tight solution. This indicates that diffusion of helium through thin silicon walls is not a failure mechanism and that truly hermetic silicon CSP packages can be manufactured to be highly reliable and used for helium and hydrogen gas sensing applications.

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Biography

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Micromechanical testing of thin die

By Alan King [Nordson DAGE UK]

The need for micro testing thin die 100 microns and below is being driven by the increased demand for thinner mobile products with package-in-package (PiP) and system-in-package (SiP) devices for smartphones and tablets. This, combined with a need for ultra-thin die 50 microns and below for RFID tags, ID cards, and related products, is presenting an emerging challenge for micro testing at the die level and bond testing interconnect at the package level. This article takes a look at how micro materials testing and advanced bond testing has evolved to provide solutions.

The challenges

Inorganic semiconductors are brittle and their strength is greatly affected by the presence of surface flaws created by dicing and handling. These flaws manifest themselves as chips and scratches. Die can experience high levels of stress because of coefficient of thermal expansion (CTE) mismatch, or flexure of the substrate or board to which they are mounted. Flexural testing is ideal for assessing the impact of defects (cracks) and surface damage on the strength of brittle materials. The standard way of assessing the unfavorable effects of dicing and grinding is to perform a bend test on a statistically significant population typically greater than 25 samples, and this is normally done in accordance with industry standards such as: SEMI G86-0303 (Three-point bend test of die), or SEMI G96-1014 (Chip (die) strength by cantilever bending).

Different bend methods such as 3-point, 4-point, ring-on-ring and ball-on-ring (spherical bend) result in different stress distributions. The failure modes for 3- and 4-point bend testing are sensitive to both surface and edge cracks.

Micro testing of ultra-thin die

Three-point bend testing is not ideal for ultra-thin die 50 microns and below as their increased flexibility dictates that the supports should be close together, which causes practical difficulties, making testing in accordance with SEMI G86-0303 inconvenient. Therefore, an alternative method (Figure 1) should be adopted: the SEMI-G96-1014 cantilever bend method. This particular method involves landing a shear tool (bending tool) on the surface of a work holder and then stepping back (up in

Z) to a precise controlled test height before moving the Y stage towards the transducer in order to apply a load to the face of the die.

Young's modulus is reduced with die of 50 microns thickness and below, and therefore the traditional 3-point bend method becomes difficult to use. Figure 2 shows the transition point between the 3-point bending region and the cantilever bending region.

Bond testing stacked die

Rapid advances in semiconductor packaging technology continue to drive bond testing capability. The testing of interconnects on stacked die, which are commonly used in SiPs presents a number of new and exciting challenges. One of these challenges is being able to land on a compliant thin-stacked die surface and accurately stepping back to a preset shear height before performing a shear test on a ball bond.

Overhanging die in particular can be difficult to bond test because of the complications, such as thickness of the die (flexing during load tool landing and step back) and the small spacing between the bonds. This has been addressed with the aid of specialized software and the problem of die surface deflection associated with the load tool landing has been solved.

The Nordson DAGE Series 4000Plus (Figure 3) has a software option that enables the operator to set a soft land step distance (measured in millimeters). When landing the shear tool on a compliant surface, the small downward force applied by the shear tool is enough to move the surface. After the tool has clamped and lifted (step back) to the designated shear height, the surface of the die will deflect upwards towards its

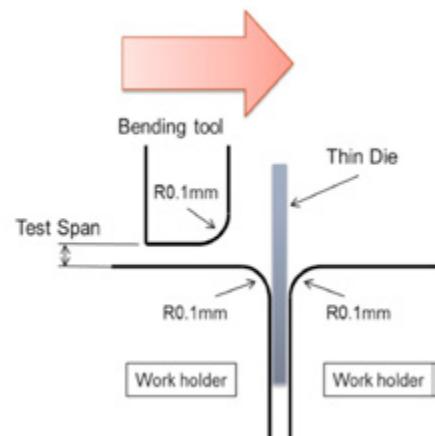


Figure 1: Illustration of a thin die held in a work holder ready for load to be applied during the cantilever bend method.

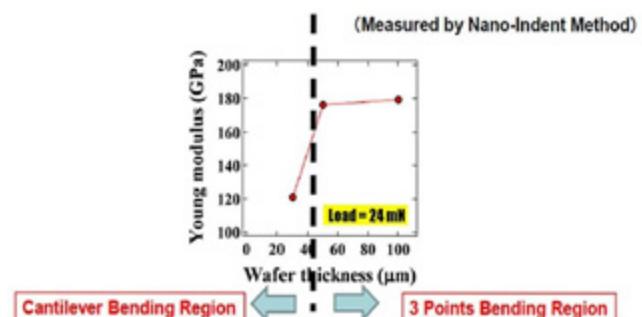
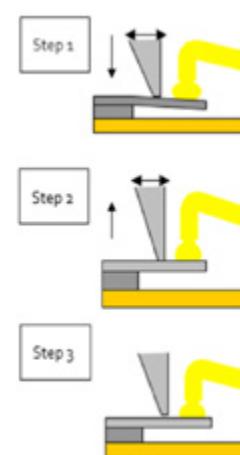


Figure 2: The graph shows that die below 50 microns in thickness should be tested using the cantilever bend method; and die above 50 microns-thick can be tested using the 3-point bend method.



Step 1 Shear tool lands and the XY stage oscillates producing a measurable force on the transducer.

Step 2 Shear tool slowly raised until the oscillating force is reduced to zero.

Step 3 Shear tool will now step back (up) in Z to a preset test height.

Typical landing forces (S25) 4 Grams with a step back accuracy of +/- 0.25 microns.

Figure 3: Soft landing procedure.

WS-575-C-RT Ball-Attach Flux

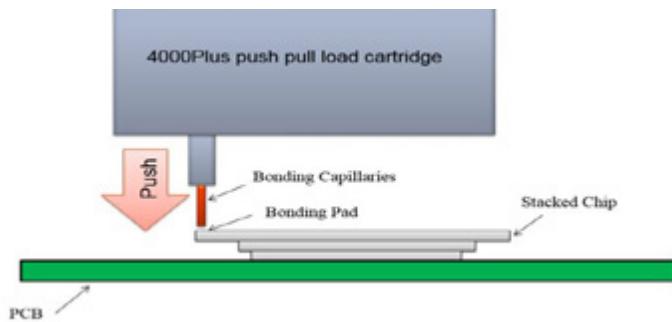


Figure 4: Showing the stacked thin-chip bend test method.

Die thickness	Typical destructive force
30 um	48 to 70 Grams
40 um	90 to 130 Grams

Table 1: Typical test results from a 4000Plus platform using a 500 gram push/pull load cartridge.

original position. The resulting shear height relative to the surface is now significantly less than the step back height selected.

Having landed and clamped the shear tool, the XY table makes small scrubbing movements back and forth. The cartridge load cell detects the movements of the table while in contact with the surface and is raised in steps until no contact is detected. At this point, the die has returned to its original position and the load cartridge will reset to zero and step back to the desired height before performing the ball shear test.

Measuring the deflective strength of thin stacked die

Stack die technology is also incorporated in memory products such as NAND flash memory, USB memory, SD and SRAM, and as such, it's not uncommon to encounter overhanging die in many of these package styles. As a result, there is an emerging need to be able to use bond testing to duplicate the downward force that a wire bonding capillary would apply during the bonding cycle on the overhanging portion of the die. This is typically a destructive test with the peak force being known as the "deflective strength." This particular application would involve a 4000Plus mainframe with a 500 gram push/pull load cartridge with a bonding capillary fitted to the load cartridge (Figure 4). Typical test results obtained with this solution are shown in Table 1.

Summary

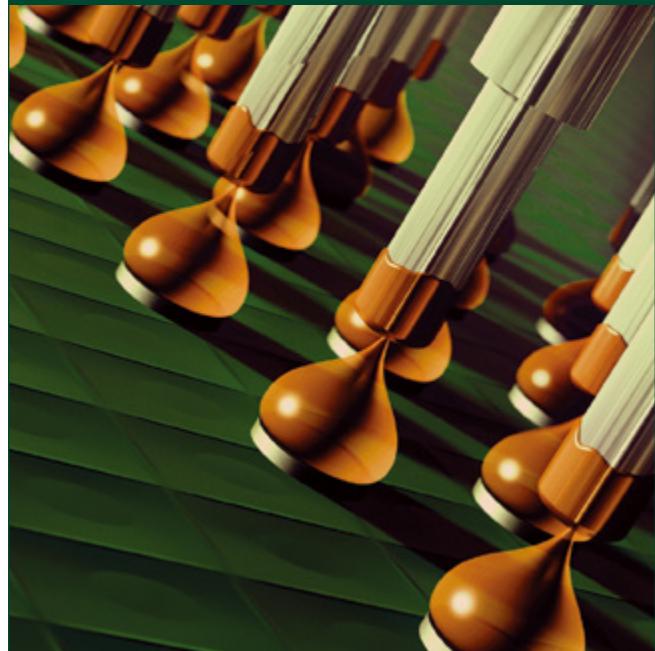
With the advent of new materials, technology, and advanced packaging trends, it's critical that traditional bond testing techniques are evolved to accommodate more of a micro materials testing environment. Many new and diverse testing techniques are needed to meet the challenge, and as a result, there is no longer a divide between bond testing and materials testing, it's all essentially micro testing.

Acknowledgements

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Biography

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Backlights and headlights: illuminating LED packaging

By Arabinda Das [\[TechInsights\]](#)

Lighting technology has changed drastically in the past 25 years. Incandescent and fluorescent lamps are now being replaced by light emitting diodes (LEDs). Advantages of LEDs include cost to fabricate, and their energy efficiency. They have broader applications than illumination, and are making their way into industries such as: greenhouse farming, water purification, medical, cosmetics, printing and prototyping, etc. According to “Strategies Unlimited” market reports, the global high-brightness light-emitting diode (HB-LED) market has reached the double-digit billion dollar range.

This article looks at two major applications of LED use in consumer goods. First, we analyze the backlight module of the iPhone 5, including the package, color temperature, and type of phosphor of the LED. Then we look at LEDs employed in automobile headlights, specifically the teardown of a Lexus headlamp and configuration of the lighting module.

iPhone 5: backlight module

Most handheld devices use liquid crystal display (LCD) screen technology. LEDs are typically employed as the backlight in LCD modules, and are often configured to be edge-lit (meaning LEDs are placed along the sides of the display, facing inwards towards the screen). These LEDs are mounted in a strip and connected to light guides, which disperse the light uniformly across the screen. **Figure 1** shows five LEDs attached to the flexible substrate found in a 16GB Apple iPhone 5 smartphone.

Figure 2 is a compound picture of two optical images of a single LED – the left one is with the package and the right one is without – exposing the bare die. The left is an optical image of a single LED in a surface-mount package, from an oblique, overhead angle. The packaging material was a heat resistant polymer, on top of which, was a silicone resin acting as a diffuser with phosphor incorporated in it. The resin was transparent and looked yellowish due

to the embedded phosphor. The one on the right shows an optical image of the de-encapsulated LED from the top view. The LED die has a length of 0.7mm by 0.2mm, giving an area of 0.14mm^2 . Both electrodes were on the same side of the die.

Electro-optical analysis: iPhone 5 backlight module

LED

To understand the electrical characteristics of the LED, we conducted some basic electro-optical measurements. We determined the chromaticity of the LED, which characterized the color of the light emitted by a light source.

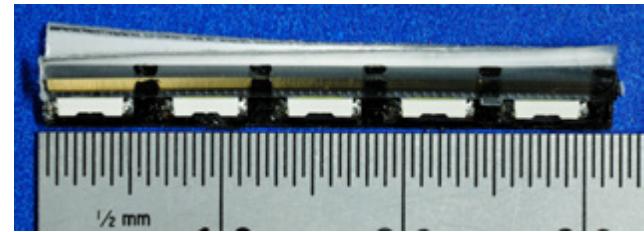


Figure 1: Backlight module from the 16GB Apple iPhone 5 smartphone.

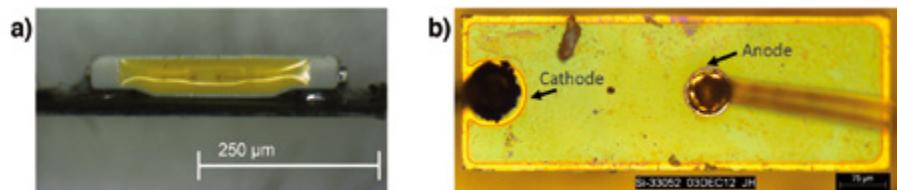


Figure 2: a) (left) A single LED package; and b) (right) the bare die removed from the package.

The concept of chromaticity is based on the spectral emission of a black body, which is defined by Planck's Radiation, and is therefore dependent on temperature. The overall color appearance is quantified as correlated color temperature, and is expressed in a two-dimensional plane of C_x and C_y coordinates. The correlated color temperature (CCT) characterizes the light source by comparing it to the temperature of a black body radiator. For example, this LED, at 25°C for 0.1A, the C_x was 0.2875 and the C_y for the same parameters was 0.2676. These values drop as the current increases or the temperature increases. **Figure 3** shows the lines on the chromaticity diagram. Each line represents constant correlated color temperature. The LED

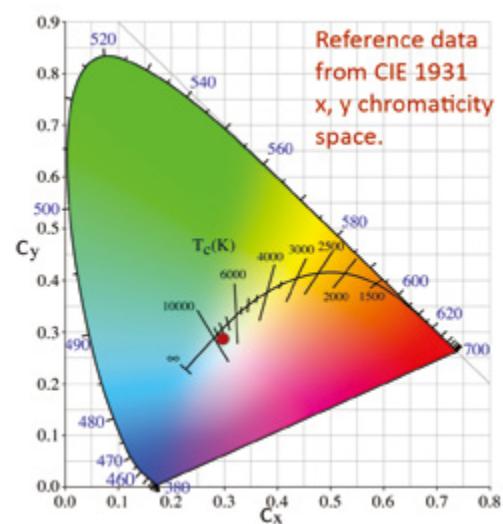


Figure 3: Chromaticity diagram of the iPhone 5 backlight LED.

is injected into the PN junction. The electron and holes combine in the active region and release energy in the form of light. Actual LED structures are more complex involving epitaxial layers, and are discussed in [1]. White LEDs are nitride-based LEDs, and are also known as GaN-based LEDs. These devices are direct band gap semiconductors, and exhibit an emission of light over a wide spectral range (from ultraviolet to infrared), depending on the composition of the device structure. These GaN-based LEDs have taken a major share in today's optoelectronic industry, ever since Nichia Corporation managed to fabricate commercial blue LEDs by depositing GaN on sapphire [2].

The white light observed was a combination of a dominant wavelength at 450nm (blue) and a complementary wavelength at 550nm (yellow). The dominant wavelength was generated by the blue LED and the complementary broad wavelength comes from a fraction of the blue light interacting with the phosphor. The combination of blue and yellow light generated the white light. **Figure 4** plots the spectral radiant flux vs. wavelength

for a current of 20mA at three different temperatures. The change in peak position was not significant with temperature, which implies that the color of the LED did not change much with temperature. This is important because during operation the LED can get hot, and that can change its emission and overall color appearance, potentially affecting the backlight properties of the display.

iPhone 5 backlight module: LED package cross section

Figure 5 shows a package cross section of the LED. The LED diode was placed in a cavity on a lead frame. The LED die thickness was 110 μ m. The transparent substrate (sapphire) was placed directly on the lead frame. The bond pads and wire bonds were over the top surface of the die. Phosphor with resin was deposited directly on the die. Several

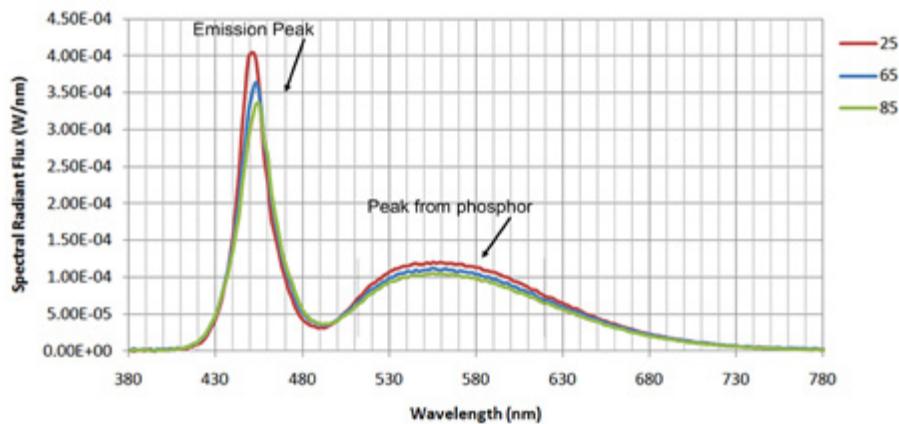
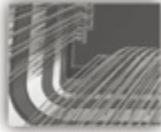


Figure 4: Spectral radiant flux vs. wavelength, grouped by temperature in Celsius for an applied current of 20mA.

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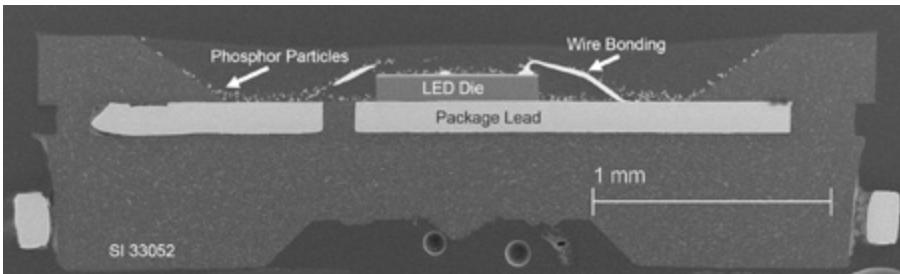


Figure 5: SEM cross section of the iPhone 5 backlight package.

micron-sized particles were distributed in an epoxy resin. SEM EDS analysis was used to identify the material composition of the phosphor particles. During the EDS analysis different grains were analyzed with varying accelerating voltages and different acquisition times, to obtain the EDS spectra. Three types of phosphor were identified in the resin covering the LED: 1) Phosphor #1: $\text{Y}_3\text{Al}_5\text{O}_{12}/\text{Ce}$; 2) Phosphor #2: $(\text{Y,Gd})_3\text{Al}_5\text{O}_{12}/\text{Ce}$; and 3) Phosphor #3: $\text{BaMgAl}_{10}\text{O}_{17}$.

$\text{Y}_3\text{Al}_5\text{O}_{12}/\text{Ce}$ has a color emission around 550nm, while the same compound with Gd and Y additions shifts the wavelength to 600nm, and $\text{BaMgAl}_{10}\text{O}_{17}$ has an emission at a wavelength shorter than 500nm. This combination of three different phosphors emitting at different wavelengths results in uniform white light.

In the **Figure 5** SEM image, the wire bonds are connected to the electrodes on the surface of the die. The final light output is directly influenced not only by the composition of the epitaxial layers, but also by the configuration of electrodes on the surface of the die. It is critical for GaN-based LEDs to form a high-quality ohmic contact between the epi-layers and the electrodes, especially for p-type electrodes. For n-electrodes, it is often quite straightforward: in most cases Au is directly deposited on n-doped GaN. For the p-electrode, a careful consideration of the work function is needed. In this case, the p-electrode is a stack of metal layers consisting of ITO, Rh, W, and Au layers, and these layers are deposited on top of p-doped GaN layers.

Figure 6 is a SEM cross section highlighting the mesa structure and the patterning of the sapphire substrate. Heteroepitaxial growing of GaN-on-sapphire is not an easy task. The lattice constants of the sapphire (0001) C-face surface and of Wurtzite GaN differ by 15% and the thermal expansion coefficients are also dissimilar. It was only around 1986 that Prof. Akasaki's group at Nagoya University demonstrated the growth of GaN layers on sapphire by using metal-organometallic vapor phase epitaxy (MOVPE). The main innovation was to introduce a sequence of buffer layers

between the sapphire substrate and the n-doped GaN epitaxial layers. These buffer layers were grown at different substrate temperatures with varying lattice parameters to match the lattice parameters of the sapphire and GaN layers. This technique was further improved by Shuji Nakamura at Nichia Corporation. Nevertheless, the problem of lattice mismatch has remained and continues to generate dislocations and other defects. Many techniques like selective-area growth (SAG) and epitaxial lateral overgrowth (ELO) methods are used to mitigate the propagation of dislocation density [3]. These methods use masks and etched facets to create restricted areas of growth. The film grows initially in island-like structures and then coalesces to form a uniform sheet.

The epitaxial layers grown on sapphire form the central part of the LED structure. The LED emission region is a multi-quantum well structure that consists of a repeating pattern. The well is sandwiched between two high band gap layers that are also un-doped. These details are discussed in [1].

Toyota Lexus headlamp

We move to another major application of LEDs: automotive headlights. The

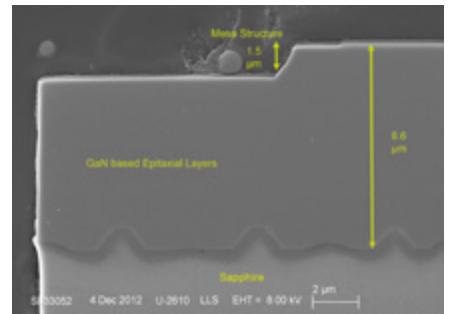


Figure 6: SEM cross section showing the mesa structure of LED removed from the iPhone 5 backlight module.

drive for reliable, low-cost and low-power consumption lighting is forcing automobile headlamps to evolve rapidly. In the 1960s, tungsten filament lamps were used. This was replaced by high-intensity discharge (HID) lamps, where a mixture of rare metals and gases were heated to produce a bright white glow. HID lamps consumed less power than the tungsten filaments or halogen ones. Then in the 2000s, LED lights started replacing HID lamps in high-end German cars. Now, most car manufacturers use LED lamps. There have been many discussions about the brightness of HID and LED lamps; some believe that HID lamps are brighter than LEDs. But LED lamps beat all other competitors when it comes to power consumption and how fast they reach their maximum brightness.

Figure 7 shows the teardown of a headlamp module from a Lexus. In **Figure 7**, the image of the front side of the light socket shows cylindrical structures that are light pipes that have engineered lenses at one

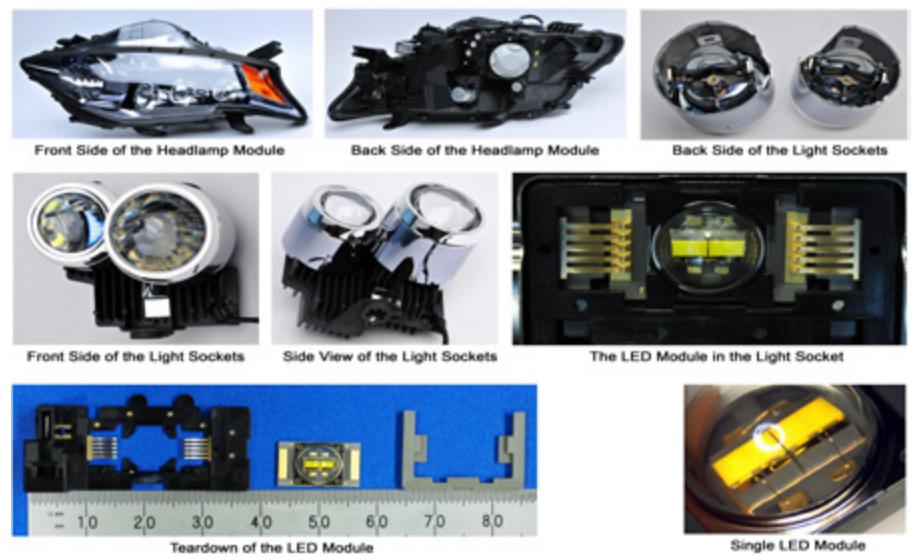


Figure 7: Teardown of a Lexus headlamp.

end. Long, polished cylindrical pipes help to collimate the light beam and give the overall impression of an elongated head light.

Figure 8 shows the LED module without the lens and the phosphor removed from the surface of the LED. Each LED package comprises four LED dies, mounted on the die mounting blocks, with two dies per block covered by a single lens. The external electrodes were located along the sides of the package. The round rings were the edge of the mesa structures of n-electrodes, seen through the top surface of sapphire. The LEDs were flip-chip mounted on the supporting substrate (more details are in [1]).

Figure 9 is a collection of two SEM images, indicating how the LEDs are placed on the mounting block. The top image shows two mounting blocks on the LED package substrate. The bottom image is a topographical image showing how the two LEDs were placed on each mounting block. The LEDs were flip-chip bonded to the mounting blocks. The leads were routed from the electrodes, through the LED package substrate, to be routed underneath the lens frame. Wire bonding was used to connect LEDs mounted on different blocks.

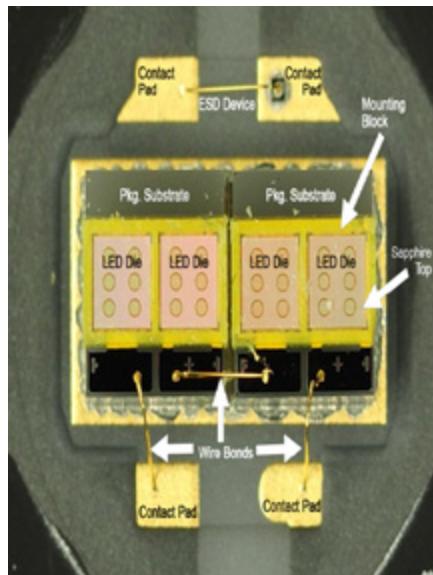


Figure 8: Optical image of the LED with the phosphor on top removed.

The mounting blocks were made of AlN and are used as heatsinks.

The flip-chip bonding of the LED is seen more clearly in **Figure 10**. The n-electrode consists of tungsten, platinum

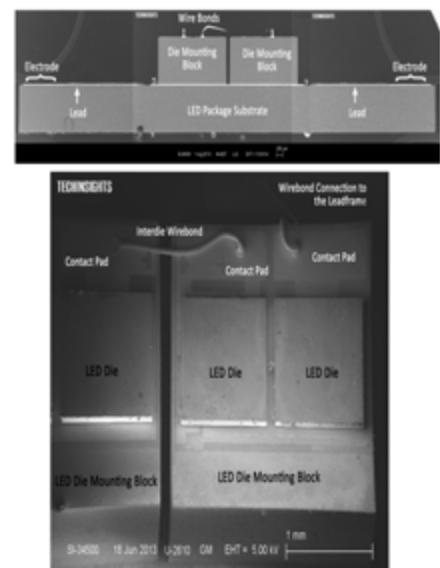


Figure 9: SEM images showing how the LEDs are mounted on the mounting block.

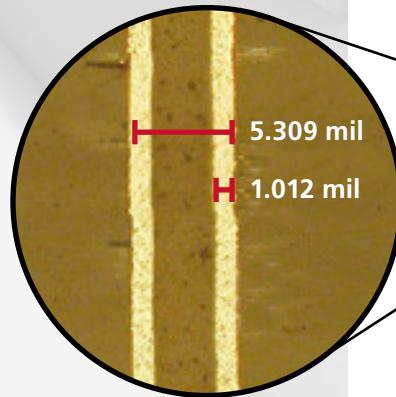
and gold-copper alloy layers. The p-electrode consists of nickel, gold and gold-copper alloy layers.

Figure 11 is a package cross section of the LED to visualize the conformal

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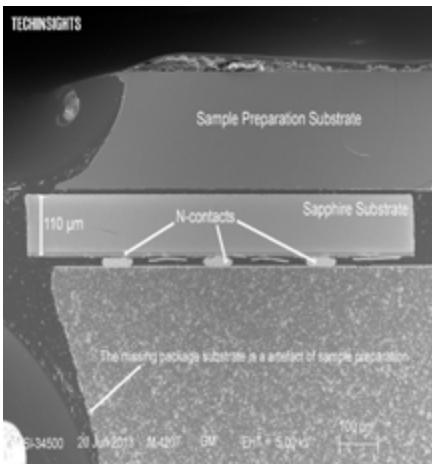


Figure 10: SEM cross section showing how the LED is flip-chip bonded to the mounting block. The p-contact is not seen in this plane.

coating of phosphor. The phosphor was coated on top of the sapphire. SEM-EDS analysis, like in the previous case, indicated that the phosphor used in the LED from the headlight is YAG:Ce, a single phosphor with homogeneous grain size for high conversion efficiency.

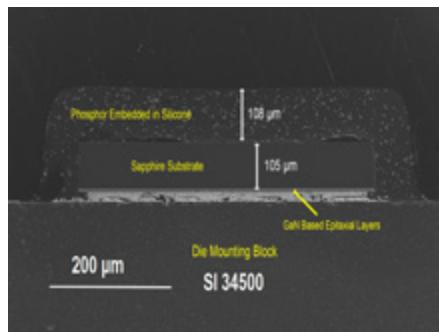


Figure 11: SEM cross section showing the phosphor coating on sapphire.

Summary

The epitaxial layers of both LEDs looked similar, but their electrode configurations were very different. For the LED in the backlight module, the sapphire was mounted on the lead frame, with the phosphor on top of the epitaxial layers. In the headlamp, the LED was flip-chip mounted, and the phosphor was on top of the sapphire. This orientation allows the LED to be mounted on heat sinks in order to handle the higher wattage consumed during operation. In both cases, the dielectric sapphire substrate remained,

even though removing it could have improved heat dissipation. In the case of the backlight on a mobile device, the objective is to have minimum power consumption and a vivid and uniform light distribution, which is why multiple phosphors are used in combination. In the case of headlamps, a greater intensity is needed. Here, the light module had four LEDs on two mounting blocks that were interconnected and placed under one lens. This configuration, in a single unit, emits the combined luminescence of four LEDs.

The desire to have better display image quality, and the need for bright light, will probably shorten the reign of LEDs. Likely in the future, quantum dots will replace LEDs, because quantum dots can boost the color appearance, as well as, the intensity, thereby improving the picture quality in a display [4]. QDs are nano-particles in the range of 2 to 10nm in diameter; the color of light that a QD emits is directly related to its size and has a narrow spectral distribution. The biggest advantage with QDs is that combining different sizes of QDs, each emitting at different wavelengths, white light can be generated, so the need for phosphor can be eliminated. Be it LEDs, quantum dots, or lasers to excite a chamber filled with phosphors, they all contribute to the advancement of lighting technology. All are compact, consume low power, environmentally friendly, and the intensity can be modulated by changing the duration of the current applied to the optoelectronic device in a given period of time. Expect to see continued advancement in lighting technology and its application.

Biography

Arabinda Das received his Master's degree in Physics from the Indian Institute of Technology, N-Delhi, India and his Doctorate degree in Material Science from U. of Pierre & Marie Curie-Paris-VI, Paris, France. He is a Senior Process Analyst in the Technical Services division of TechInsights; email adas@techinsights.com

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Advanced wafer-level packaging (WLP) enables high-frequency ADAS radars

By Babak Jamshidi [STATS ChipPAC]

Over the past two centuries, technology has played a critical role in the evolution and creation of new trends in a human's daily life. The recurrence of this disruptive pattern accelerated in the mid 20th century by introduction of the semiconductor industry and the enormous values it offered by enabling flawless system control, miniaturization and performance improvement. The modern automotive industry has gone through many phases of innovations, primarily motivated by safety regulations. Its most recent mandates have been in the field of advanced driver assistance systems (ADAS), which uses sophisticated systems of hardware and software to alert drivers to potential hazards and problems, mostly outside the driver's line-of-sight, in order to avoid collision. Although some single-application ADAS devices, such as microwave radars and adaptive cruise control, have been used in pilot production cars, it was not until the year 2000 when United States and European regulatory agencies recommended specific aid, warn and assist categories of ADAS features. These features cover a wide range of applications from single-task rear camera view, park assist and forward collision warning, to ultimately sophisticated systems of autonomous and autopilot driving. The mandates from worldwide regulatory agencies, market demand and aggressive targets for assisted and autonomous driving have created a tremendous momentum across the automotive electronics supply chain (Figure 1). It is expected the global value of the ADAS segment to pass \$60 billion by 2020, and reach the \$200 billion mark by 2024.

The outlook of ADAS system architectures to include a higher number of multi-functional electronics control units (ECUs), using Ethernet, WiFi® and ZigBee® for connectivity, and stacking more sophisticated data-driven algorithms will require up to fourteen sensors (detectors) in a car. These sensors are typically microwave or ultrasound radar chips, light detection and ranging (LiDAR) sensors and cameras (Figure 2). The performance, cost and environmental

sensitivity (rain, dirt, etc.) will determine which sensor will be the best fit for each specific ADAS application.

Over the past few years, microwave radars have evolved from a niche sensing to a mainstream automotive solution. Today, a majority of the radar chips are in the range of 24 to 48GHz for short range detection such as rear collision or blind spot detection. It is expected, however, that the short range radar chips will be replaced by high-frequency (77 to 79GHz) radar devices that could detect across a longer range and wider angle. Although a single solution for all radar applications is quite an attractive proposition for both original equipment manufacturers (OEMs) and system integrators, sensitivity of high-frequency RF radar chips to insertion loss is a challenging task to tackle. In addition to performance, the device packaging must continue to meet the recommended reliability, offer design flexibility and a path to multi-chip integration, all in a cost-effective manner. The short range radar devices are assembled using mainstream wire bond lead, laminate, and, in limited cases, flip-chip package solutions currently offered in the market. These solutions offer a low cost path to support a low GHz frequency range and meet Grade 1 reliability requirements (per Automotive Electronics Council AEC-Q100). However, the high-frequency radar devices would require a much tighter RF signal isolation, which imposes a number of constraints

on the package of choice. If we look inside an automotive radar module (Figure 3), the two main printed circuit board (PCB) components

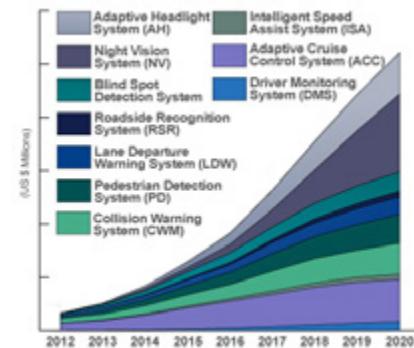


Figure 1: ADAS overall value world market by system type. SOURCE: ABI Research and CE Outlook.

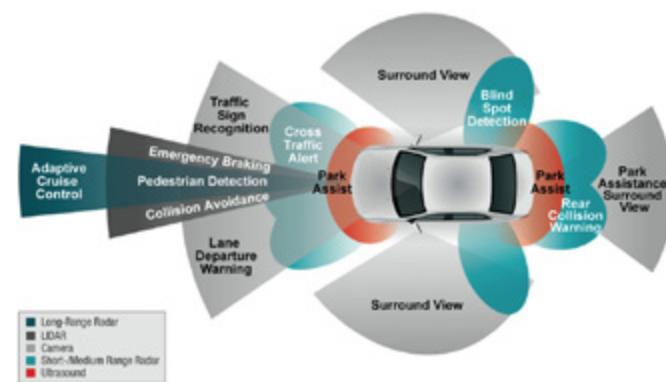


Figure 2: ADAS sensor types and applications. SOURCE: AVEASIA

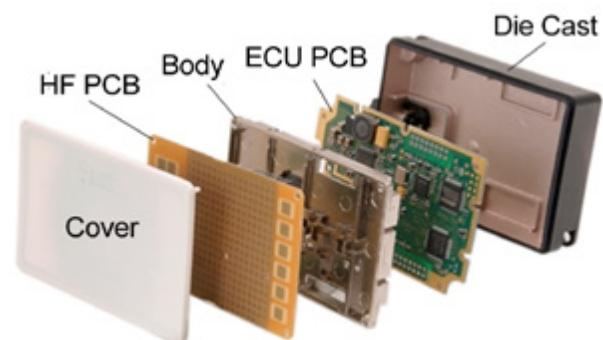


Figure 3: Exploded view of a typical automotive radar module. Picture courtesy of Autoliv.

are ECU and HF (high frequency). The rest of the parts protect the functionality of the PCBs by creating a secure housing and heat dissipation. If we look closer, the ECU PCB, or the processing board, has multiple discrete chips such as digital signal processors, microcontrollers, memory chips, controller area network (CAN) transceivers, periphery integrated circuits (ICs), and many passives.

The HF PCB also has a long list of chipsets that are solder mounted such as HF

transmitters and receivers, frequency synthesizer, switches and additional periphery devices. However, the new generation of high-frequency radar chips will experience a revolution in circuitry design using GaAs or

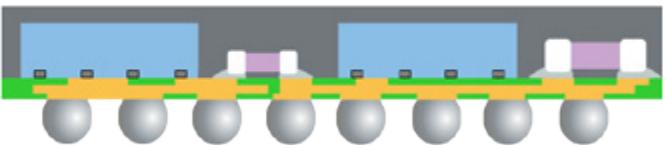


Figure 4: Multi-chip FOWLP SiP (also known as eWLB SiP).

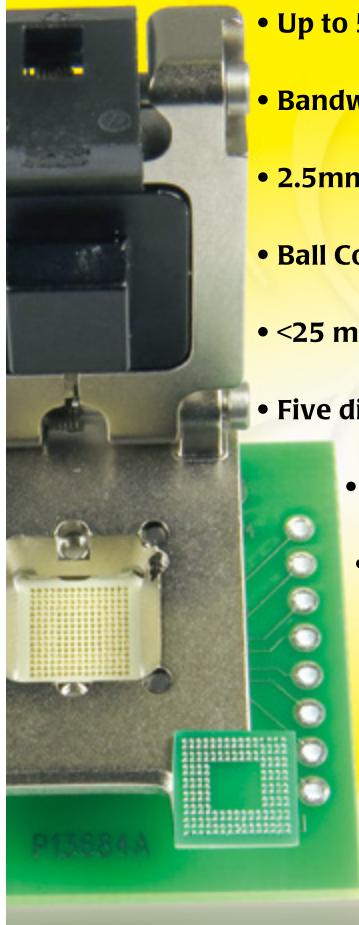
silicon monolithic mm-wave ICs, as well as a transition to finer silicon node technology, to enable integration of several functionalities, traditionally supported by multiple chipsets and passives. The tradeoff of offering a highly integrated radar chip while meeting or exceeding aggressive performance targets in the automotive industry can only be enabled using advanced packaging technologies. In addition, the packaging method has to offer production scale, a reliable and cost-effective supply chain, design flexibility and competitive cycle time.

System-in-package (SiP) integration, flip-chip, fan-in wafer-level packaging (FIWLP) or wafer-level chip-scale packaging (WLCSP) and fan-out wafer-level packaging (FOWLP) are among the major packaging technologies that have been considered and applied across a wide range of radar assembly applications. However, despite the fact that each packaging method satisfies a subset of requirements, performance is the deterministic factor for high-frequency radars that cannot be delivered by a majority of the package types due to laminate (or PCB) high insertion loss. All laminate-based fan-out methods offer design flexibility and match target ball map, at the expense of introduction of additional impedance owing to the PCB dielectric constant (Dk) and manufacturing tolerances and variations.

Many sectors of the semiconductor industry have vast experience with the losses described above and how to accommodate for them to meet product specifications. However, in very high-frequency RF systems (77 to 79GHz), the electrical signal transmission line losses due to Bismaleimide-Triazine epoxy (BT-epoxy) or FR-4 materials become quite significant, which result in using advanced low-loss materials or an additional amplifier, thereby making a very expensive package. On the other hand, WLCSP does not have the high-loss laminate component, but the fan-in construction of the package effectively limits the number of possible inputs/outputs (I/Os), does not offer any 2D integration, and any 3D integration will require an expensive through-silicon via (TSV) technology, and the assembly line is restricted to a certain wafer size. Therefore, WLCSP has a limited value proposition for products such

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as high-frequency radars. Figure 4 shows an example of multi-chip FOWLP (also known as embedded wafer-level ball grid array, or eWLB) system-in-package (SiP). The standard FOWLP architecture eliminates the need for a laminate substrate and replaces it with copper redistribution layers that inherently have a shorter connection distance and significantly reduced impedance. It also offers more design flexibility for less routing interference and sufficient isolation for RF channels.

FOWLP has historically been an attractive package for automotive radar systems and was selectively used for assembly of multiple generations of high-frequency radar chips. However, over the past few years, FOWLP has significantly evolved from an advanced fan-out method for very niche and selective applications to become a packaging method that can enable a thinner profile and a higher level of integration for a wider range of applications. The design flexibility of this method allows for integration of multiple dies, passives in discrete or copper redistribution layer (Cu RDL) [2], exposed-die architecture and 3D pre-stacking (Figure 5). FOWLP uses thin-film processing for RDL, which currently delivers less than 10µm/10µm line-width/

line-space ratio and is following a roadmap to reduce the line and space pitch by 80% down to 2µm/2µm in the near future. The capability to place components at less than 100µm gap from each other enables SiP footprint

reduction, hence a smaller ECU board which positions the radar chips as suitable for both automotive and other types of applications (i.e., industrial and robotics).

In addition to the above considerations, the RF performance benchmark tests show an eWLB RF device introduces less than 2dB transmission loss, which falls within an acceptable range across the RF industry. The raw measurements of signals show a nearly identical response between FOWLP packages and control samples (including board, transition, and transmission line loss). In addition to the performance, it is critical

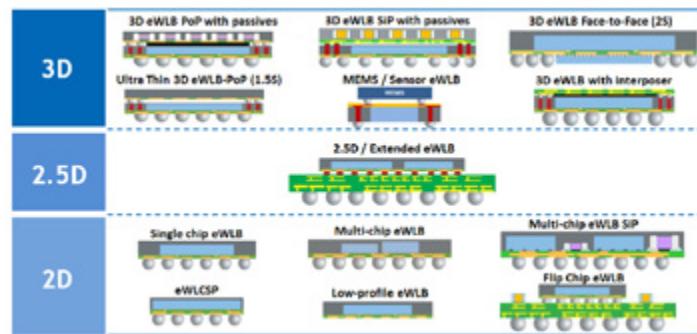


Figure 5: FOWLP package portfolio evolution to address emerging market trends.

for a package to meet automotive reliability requirements. Per AEC-Q100, an ADAS radar device must meet Grade 1 temperature cycling, storage life, and solder joint component-level reliability, which falls within standard FOWLP state-of-the-art reliability level. On the board-level reliability (BLR), eWLB successfully passes 500 cycles of temperature cycling in the range of -40°C~125°C, JEDEC standard drop test, and passes 1000 hours of temperature humidity test bias test under 85°C/85%, RH, 5V (while mounted on a PCB). eWLB packages have shown quite effective heat dissipation and thermal performance (for

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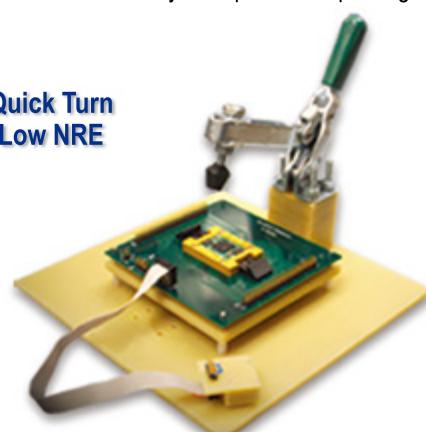
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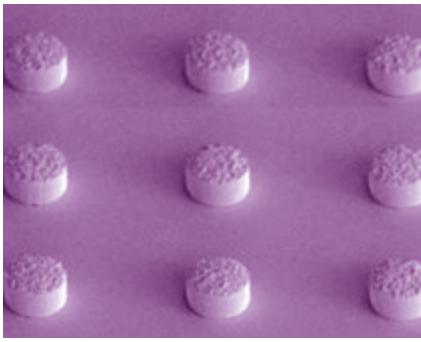
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example: 12x12mm with 8x8mm die size has shown 21.70ja(°C/W) with no thermal enhancement). Furthermore, the interest for miniaturization and lower cost SiP can be supported by eWLB advanced design rules.

eWLB integrated passive device (IPD) architecture offers significant product footprint saving that can reduce package size by more than 50% [3]. Therefore, the ECU PCB size can be reduced by designing the IC using mainstream silicon fabrication nodes and integration of the CMOS die with an IPD using the standard FOWLP process. Also, the ability to provide 3D SiP and package-on-package (PoP) solutions with embedded passives and active components provides a direct vertical interconnection across all embedded devices (Figure 6). This capability offers a cost-effective alternative with streamlined and efficient eWLB infrastructure compared to the TSV technology. However, the main impact is the ability to vertically stack components that were traditionally assembled using surface mount technology (SMT), yielding larger size motherboards. In the case of advanced automotive radars, multiple passives or IPDs can be removed from the PCB using an eWLB-PoP structure (Figure 6a). Moreover, if the radar product design allows, the antenna can be flip-chip bumped or assembled in an eWLB package and use pre-stacking technology to assemble as the top package in the 3D eWLB configuration (Figure 6b).

In conclusion, while the ADAS market continues to grow at a fast pace (41% CAGR by 2020) [4], the high-frequency radar chips will continue to proliferate and become a significant portion of the ADAS sensor bill-of-materials (BOM). The drive for higher degrees of system integration will demand additional control and ownership by OEMs, which will eventually trickle down to suppliers including outsourced semiconductor assembly and test suppliers (OSATS). Therefore, any packaging solution has to offer a robust manufacturing process and infrastructure with an established supplier base with a low risk and high degree of redundancy. Currently, the eWLB assembly

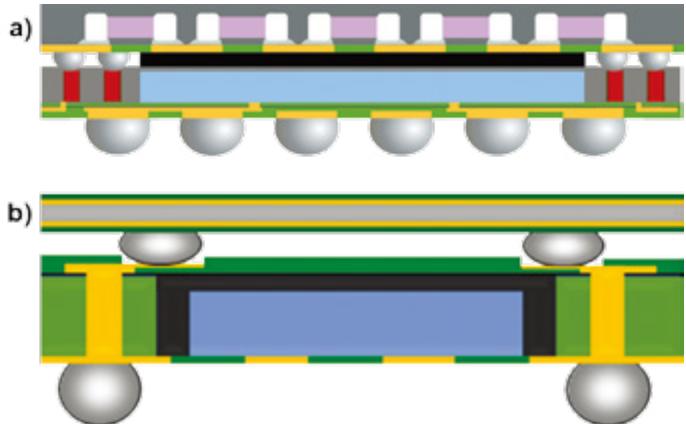


Figure 6: FOWLP offers a disruptive 3D eWLB PoP packaging method for advanced miniaturization: a) With collection of passives and filters in the top package; and b) With transmitter, receiver or antenna components designed and pre-stacked in the top package.

process offers many years of experience in high-volume FOWLP manufacturing with well-established processes for all 2D, 2.5D and 3D packages using a FlexLine™ manufacturing flow. This method allows integrating multiple dies, agnostic from their original wafer size, which can accelerate and facilitate the proliferation of FOWLP in radar devices without any need for a new CMOS design, especially for devices that transition from wire bond to wafer-level packaging. eWLB also offers a simplified BOM list, shorter material acquisition cycle time, and supplier dependency, which is especially important for quick turn for first-article products.

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Biography

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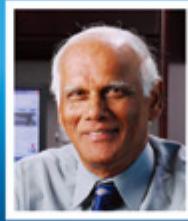


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Enabling fast-feedback loops with a probe card inspection process

By Martin Kunz [NanoFocus AG]

Wafer test is one critical step in the manufacturing of semiconductors as it comes along with certain risks for losses from a productivity point of view, and is also known to be the source of expensive quality issues with even more severe implications. When a wafer undergoes final test of its functional structures, the complete chain of value creation in the front-end-of-line (FEOL) processes is completed. Sometimes, even back-end-of-line (BEOL) process steps, such as bumping, are applied to the wafers already. This, in turn, means that a loss of a number of components, or even complete wafers caused by final wafer test, poses a strong negative impact to the capitalization of products at a very late stage. Further complicating the situation is the fact that many semiconductor manufacturers do not move tested wafers to their own internal or outsourced BEOL processes, but also deliver the tested wafers to their customers directly. This means that there is another effect that may even be more critical than the productivity losses mentioned. It happens that, during final wafer test, wafers can become damaged completely unnoticed; there are a number of well-known examples of such damage having caused costly product recalls in the past. While there are a number of pain points that cause damage that can go unnoticed during final test, it is the damaging of wafers by defect probe cards that is the focus of this article.

Defect probe cards can cause significant productivity losses during final wafer test or, in the case of damage that goes unnoticed, product recalls with unpredictable consequences. In comparison to probe card related damage that is detected before shipment to end users and that certainly causes financial loss, damage that goes unnoticed will result in wafers being shipped to customers. These damaged wafers will eventually be discovered—but only after they have already compromised production lots. The worst case will be when the defective components become part of more expensive packages comprising multiple functional

elements. If the damage continues to be undetected until final test of the end packaged “system,” the financial losses are even greater, not to mention the losses that occur if these devices are shipped to end users such as automotive manufacturers. While this scenario can seem overly dramatic, it has happened before—and all because of an undetected defect probe card.

To be more specific, unwanted, overlooked objects on a probe card that penetrate the clearance (i.e., the zone on a probe card beneath the probe tips that must be free of any obstruction when a probe card is pushed to a wafer) may imprint a wafer under test, thereby severely damaging functional structures, or even the complete wafer. Because there are many applications that are not tested by full array probe cards, an overlooked object often does not just generate a single imprint on a wafer, but rather several imprints that get distributed all over the wafer matching the number of touchdowns. Depending on where this overlooked object is located, the functional test can be completely successful while the products become destroyed by the subsequent touchdowns having caused damage that was undetected. These incidents have been known to remain hidden, even when there was additional optical wafer inspection after final test.

Objects imprinting on a wafer could be screws or bolts that affix the probe head to the connector board, which were not properly secured during maintenance and repair, or that simply were the wrong length (**Figure 1**). Other possible sources of imprinting on a wafer caused by probe card components include capacitors, coils, or resistors that were improperly chosen, mounted or remounted, respectively. Because probe card manufacturing and

maintenance is done using manual labor almost exclusively, these kind of mistakes have to be taken into account.

Another way defects can occur is when probe card components become loose on account of repeated heating and cooling of the probe card, or mechanical stress. Another potential impact is caused by particles that land on a probe card during cleaning or grinding processes, or even through abrasion that occurs during the wafer testing process itself.

Beyond the damage discussed in the above situations, the contacting components of a probe card itself can become the source for damaging or destroying a wafer during final test. During final test operations, the probe tips are exposed to mechanical stress with every touchdown, and are also subject to electrical phenomena, such as discharging arcs or high-current welding effects. This means that with every touchdown and testing cycle, there is abrasion, and wear and tear; so, the longer a probe card is in operation without re-checking its condition, the greater the risk of testing with a damaged probe card. Of course the malfunction of a probe card is obvious when one or multiple test channels of a probe card fail repeatedly on two or more touchdowns, but in many cases, wafer testing still delivers good results even when the probe tip is already damaged, or is in poor condition. It bears repeating, that this situation can cause damage to components and wafers.

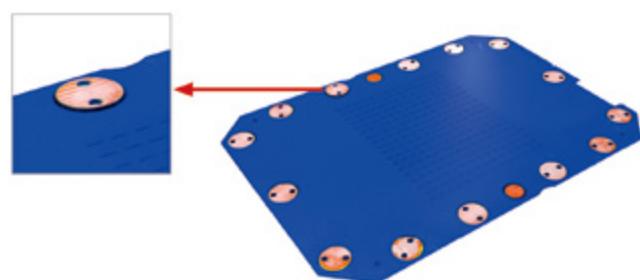


Figure 1: A µsprint hp-opc 3000 image data render of a vertical probe head containing a 1,260 probe tip array in the center. One can clearly see the bolt elevated above the probe head surface plane, penetrating the clearance area.
SOURCE: NanoFocus AG, operations

A probe tip has to fulfill certain requirements in order to be determined to be in satisfactory condition, such as: 1) the tip diameter, 2) the tip height, or 3) the planarity of the tips, respectively, and 4) the position of the tips. All of these must meet specific requirements to insure a proper testing process. If one or more of these geometric parameters is not within the specification range considered acceptable, the result will be similar to the case with the unwanted effects that can cause damage, as well as, a potential loss in productivity, and in the worst case, undetected damage of product.

As an example of what can occur, improper geometric conditions could, for example, be tip diameters that are too small. This situation is known to be a likely cause of the cracking of structures underneath the contact pads on the wafer to which the probe tips are applied. Additionally, there can be misplacement of the tips and bent tips that can scratch the contact pad out of bounds. Alternatively, when the tips are greatly bent and out of their specific positions, such tips can even be in the category of unwanted objects, causing imprints on the wafers as previously mentioned. Referring to the

electrical phenomena such as discharging arcs and high-current welding effects noted previously, there can occur burnt tips, as well as tips that pick up contact pads from wafers. For example, when a fusion of the tip and the pad material occurs, it is frequently related to high currents paired with small tip diameters. A picking up or a “ripping off” of contact pads often is the result. Furthermore, electrical discharges may lead to burnt probe tips, even to partial damage of the probe heads, and can also severely influence neighboring probe tip conditions.

Probe tips that have diameters that are too small are a common problem of new incoming vertical probe cards and probe cards that were serviced by repointing the tips. Tip diameters down to 4 microns are not unusual, though it is known that tip diameters below around 8 microns are very likely to crack contact pads or the layers underneath. On the other hand, tip diameters growing too large by normal process abrasion (i.e., a pyramid-shaped tip’s diameter increases in size as a result of the abrasion process), or becoming damaged on account of the electrical influences previously mentioned, will lead to an insufficient “scratching” or

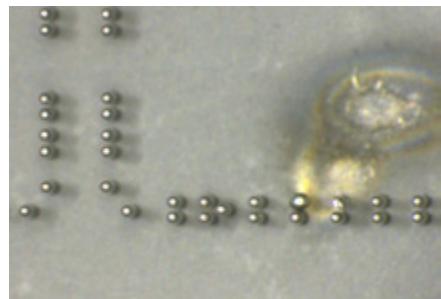


Figure 2: Microscope image of a vertical tip array damaged by an electric arc. One can see the impact on the probe tip, the burnt ceramic head plate and even a shape change of the neighboring tip. SOURCE: NanoFocus AG, photo archive

“scrubbing” of the pad (needed for electrical contact). Either there will be a bad contact in the wafer testing process, or a damage of the wafer as discussed before. From this point of view, the two damaged tips in **Figure 2** significantly differ in diameter, height and shape from the surrounding tips that are in good condition.

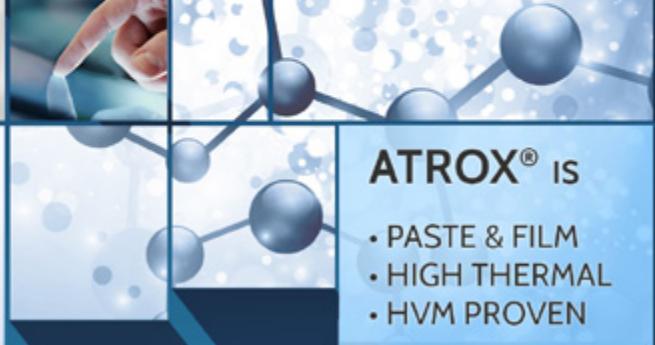
Misplacement of probe tips is typically related to mechanical impacts. They can be caused by human error or even careless handling, but can also be caused by the



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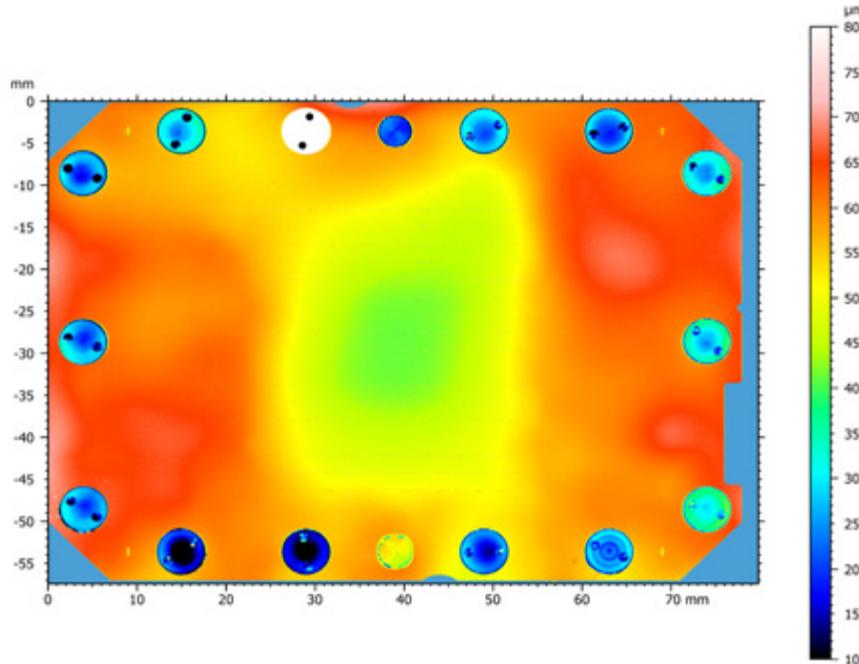


Figure 3: A *μ*sprint hp-opc 3000 topography image of a ceramic probe head guiding a centered array of 1,260 probe tips. There is a certain surface warp influencing the “scrubbing” behavior that is subject to thermally-induced changes. It can also be seen that the bolt head surfaces are distorted differently depending on the force that was used during mounting of the head (without a torque wrench). SOURCE: NanoFocus AG, operations

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wafer test process itself. In particular, when a wafer is not tested with a full array probe card, sometimes probe tip arrays are located above and beyond the wafer’s edge during a touchdown so that the entirety of the components on a wafer can be tested without testing any components repeatedly. The wafer edge is a well-known source for bending of the tips, however, exposing the tips to the wafer edge often cannot be avoided.

With the above examples in mind, along with their financial consequences and implications for a company’s business reputation, how could such events be avoided? One

way is to create a fast probe card inspection process that enables a clear decision to be made about whether a probe card is “OK” for testing or not. Such an idea, however, is far from being applicable to the reality of a wafer test operation. Therefore, a closer look at the implied requirements must be taken. To the point, the following requirements are needed to ensure an intact wafer after test:

1. A continuous and reliable observation of a probe card to identify unwanted objects. This will allow one to make a decision about whether there will be any imprinting of a wafer or not.
2. A continuous and reliable observation of the geometric parameters of the probe tips. This will allow one to make a decision about whether the probe tips are going to “scratch” or “scrub” the contact pads on a wafer correctly or not.
3. The observation of aforementioned conditions and parameters must be fast, which will allow one to check and re-check probe cards often, thereby enabling a closed-loop observance of probe card conditions during the process.

Besides the information about possible damage to a wafer emerging out of probe card conditioning, one could also derive process control relevant information from such a probe card inspection process. For example:

1. The precise assessment of probe tip geometries allows one to judge in advance about whether a tip will assure proper mechanical pre-conditions for a good electrical contact to the pad.
2. The precise assessment of probe head geometry allows conclusions about temperature-related changes of a probe head surface that can lead to different “scrubbing” or “scratching” behavior.
3. The fast feedback allows one to check and re-check probe cards frequently following touchdown counters or production lots processed.
4. The continuous availability of information about probe tip and probe head conditions can be correlated with scrubs by statistics when doing automated optical inspection (AOI) after the testing (**Figure 3**). This is especially interesting in terms of the probe head, as “scrubbing” or “scratching” behavior essentially depends on the probe head shape and positioning.
5. The fast feedback and the detailed

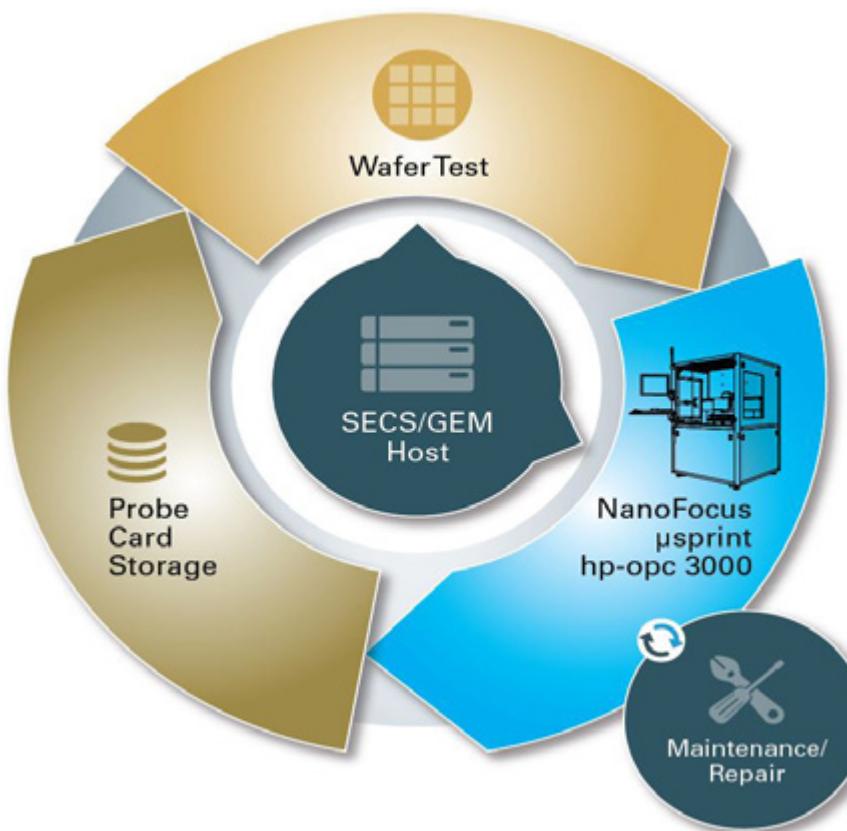


Figure 4: A closed-loop inspection cycle as targeted with the µsprint hp-opc 3000 tool to assure outgoing wafer quality after test and to be in full control over all probe cards in the test site at any time. SOURCE: NanoFocus AG, photo archive

	MEMS Micro Cantilever	Microprobe Vertical
Height Precision	<0.50µm	<0.50µm
Size Precision	<0.50µm	<0.50µm
Position precision	<0.50µm	<0.50µm
Relative accuracy	<2.00µm	<2.00µm

Table 1: Key data for precision, accuracy and correlation, respectively, of the µsprint hp-opc 3000 tool. The correlation was conducted in comparison to established equipment used at the customer's production site to ensure that no deviating process information is introduced by the new tool.

failure information of the process allows shorter and more focused repair and maintenance cycles. The nature of a defect and its location can be pointed out fast and clearly, and a full re-assessment of a probe card can be done very quickly before the probe card is routed back to the process.

Having well understood the necessity of a process capable of the aforementioned requirements, we developed, together with a

customer, a tailor-made solution for wafer test sites to address the typical pain points leading to productivity losses and quality issues. The result of that collaboration is the µsprint hp-opc 3000 tool. This tool enables a process (**Figure 4**) that allows one to frequently assess a probe card's overall condition in the wafer testing process following the requirements described above. The inspection can be done quickly after a certain number of touch downs, after each lot tested, or the other way round, before a probe card is set for operation. The new tool is designed according to SEMI standards for front-end-of-line (FEOL) cleanrooms and incorporates a SECS/GEM interface. The tool also works in conformance with established probe card analyzing tools and therefore does not introduce new or deviating information to existing processes (**Table 1**).

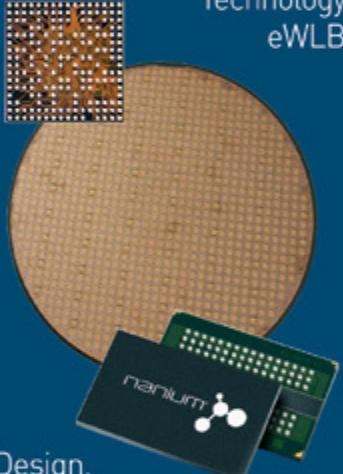
Biography

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Alpha Advanced Materials' new conductive die attach film addresses requirements for limited real estate applications

By Debra Vogler, Sr. Technical Editor

Alpha Advanced Materials has introduced a die attach film (ATROX® CF.100-7B) that is currently being evaluated and qualification tested at end user sites. The film has a thermal conductivity $\geq 10\text{W/m-K}$ and is a low stress material suitable for small to medium size die packages ($<25\text{mm}^2$). The company has noted that the film can be laminated on a wafer backside under moderate temperatures ($<100^\circ\text{C}$) and pressures ($<30\text{N}$) and it produces a high thermal and electrical conductivity silver bond using conventional die attach film processes.

Senthil Kanagavel, Global Product Manager for Electronic Polymer at Alpha Advanced Materials, told *Chip Scale Review* that the film addresses package miniaturization and the desire of packaging houses to be able to use existing materials and processes. "The presence of multi-die in a package and limited real estate area drive the need for using alternate technologies for attaching dies," said Kanagavel. "This new conductive film is an enabling technology that allows packaging engineers to place dies close to each other with similar or better performance compared to paste." The other driver for conductive film is thinner wafer profiles ($<4\text{mil}$), which have been pushing the envelope on die attach paste materials, noted Kanagavel. "The film allows packaging houses to achieve higher yields and faster throughputs with minimal concern in assembling thin die packages."

One feature of the new material is that it can achieve uniform bond line thickness and minimum flow compared to conductive pastes (Table 1). Kanagavel

told *CSR* that die attach paste has a tendency to flow after die placement and during cure. "Die attach paste also needs a fillet area that is typically $>100\mu\text{m}$," said Kanagavel. "Die attach paste will have some variation in the bond line thickness from part to part and because it is a wet paste, it will have limitations on achieving very tight die tilt tolerances." The new conductive film overcomes both issues, noted Kanagavel, because it is a pre-formed film material laminated onto the wafer. "These two key features make the film a compelling solution to achieving controlled bond line thicknesses and low spread during the die attach process." It was also noted that the controlled film thickness and the predictable performance in terms of spread make the film an excellent choice for thin wafer packages.

The company believes that the new conductive film is a key enabling technology in advancing existing package designs into future packaging requirements of tighter and higher performing package constructions. "The film will allow semiconductor packaging technologists to further push their technology envelopes to achieve the key performance attributes of the package," said Kanagavel.

Packaging challenge	Limitation of paste (current technology)	Advantage of film (enabling technology)
Thin package	Paste products cause overflow of die attach causing potential shorting in packages.	Film technology assists package technologists to use current package designs with no change, enabling thin package designs.
Multi-die; low tolerance	Paste technology causes bridging between dies with low tolerances ($<100\mu\text{m}$) thereby causing potential shorting in packages.	Film technology enables packaging technologists to assemble parts closer, thereby enabling tighter tolerance packages.
Wire bonding limitation	Paste products have limitation of wire bond pads proximity to die ($>100\mu\text{m}$) thereby using more real estate on the package.	Film technology allows package technologists to place wire bond pads closer to die, thereby reducing wire bond distance and achieving lower resistance in packages.

Table 1: Comparison of ATROX® conductive film vs. paste technology.

Indium to address requirements for SiP assembly

By Debra Vogler, Sr. Technical Editor

Indium Corporation's Sze Pei Lim, Semiconductor Product Manager – Southeast Asia, will present at the 13th International Wafer-Level Packaging Conference (IWLPC 2016, Oct. 18-20, San Jose, CA). Lim's presentation, "System-in-Package (SiP) Assembly vs. Solder Paste Attributes," addresses the increased demand for SiP caused by the rapid development of "smart" devices for Internet of Things (IoT) applications. The continued push toward miniaturization creates a demand for assemblies with smaller components and greater density. Lim's presentation will focus on the attributes of fine powder size solder pastes, review the tests conducted for critical-to-function characteristics, and discuss the results.

"Smaller packages drive smaller components and pad sizes, and hence smaller solder paste deposit volumes," Lim told CSR. "Consistency in solder paste printing transfer efficiency, absence of slumping, pad-to-pad print volume, stencil life, good wetting (solderability), graping resistance, and minimal voiding are key attributes of solder paste used for SiP, so consistent paste rheology becomes critical." Lim further explained that finer powder sizes have a higher surface area, and this metal surface can react with highly activated flux, causing rheological instability and reflow-related issues, such as graping, solder balls and wetting issues. "For a water-soluble paste, this is quite a significant challenge."

Among the findings of Indium's research that Lim will be discussing at IWLPC is the result that acceptable print process capability (Cpk) can be achieved while printing on very small aperture openings ($120 \times 60 \mu\text{m}$) with a small pad-to-pad distance ($50 \mu\text{m}$), and stencil thicknesses of 35 or 50 microns, through a good board support system, solid stencil designs, and the appropriate solder paste. "Even with a stencil aspect ratio of 0.4 (standard industry rule of thumb proposes an aspect ratio of more than 0.66), acceptable print results can be achieved with optimized process parameters (Figure 1)." Lim also told CSR that a vacuum board support system produces better printing performance compared to using a pallet only (Table 1). "The reflow profile affects the void performance, and different pastes may require different profile types—each paste should be characterized properly."

To develop the new solder pastes for SiP applications, the researchers also had to achieve a balanced paste rheology that delivers consistent transfer efficiency without slumping. "This means optimizing the flux activity and using minimal thixotropy," Lim told CSR. "This is a rheological property that is usually characteristic of water soluble pastes, and which must be minimized to prevent variation in the viscosity, and hence prevent large variation in print and slump properties over time."

Variable	N	Mean	StDev	Minimum	Q1	Median	Q3	Maximum
0.40AR Paste A	3600	96.21	17.32	44.15	84.50	96.35	107.66	157.29
0.40AR Paste B	3600	108.39	17.19	10.04	98.30	109.56	119.76	158.45
0.40AR Paste C	3600	99.44	17.56	0.00	86.41	99.04	111.36	169.99

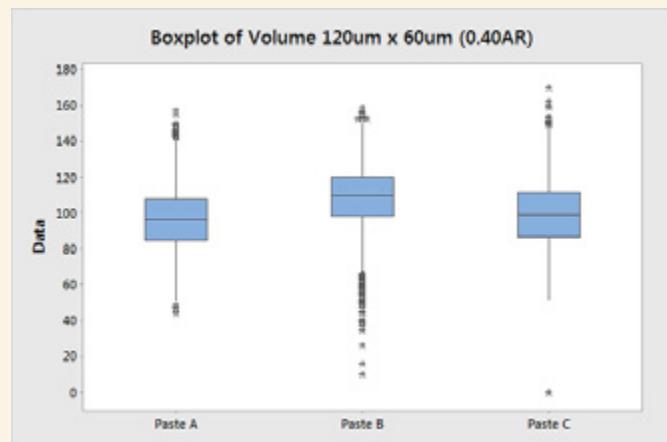


Figure 1: Box plot of volume $120\mu\text{m} \times 60\mu\text{m}$ (0.40AR). SOURCE: "System-in-Package (SiP) Assembly vs. Solder Paste Attributes," IWLPC 2016

Support	Aspect Ratio	Cpk	Ppk	Cp
Pallet	0.68	2.52	1.07	3.20
Pallet	0.64	2.70	1.10	2.97
Pallet	0.60	2.39	1.11	2.61
Vacuum	0.68	2.82	1.29	3.37
Vacuum	0.64	2.91	1.60	3.27
Vacuum	0.60	2.73	1.38	3.19

Table 1: Pallet vs. vacuum comparison. SOURCE: "System-in-Package (SiP) Assembly vs. Solder Paste Attributes," IWLPC 2016

INDUSTRY NEWS

The balancing act between consumer and harsh environment packaging

A report from the SEMICON Europa Advanced Packaging Conference (APC) committee co-Chair

By Steffen Kroehnert [[NANIUM S.A.](#)]

System integration is continuing to move forward. Denser and high performing systems, however, require advanced packaging, assembly and test providers to work more closely. Additionally, these players must be involved in the collaboration along the full supply and value chains from the earliest beginnings of projects. The package is becoming a functional part of the product, and with it, a differentiator for the product's success in the market.

Europe has a strong automotive industry that increasingly requires excellence in automotive electronics. One cannot think of automotive electronics packaging without thinking about advanced packaging, assembly, and test. Therefore, the Advanced Packaging Conference (APC) committee, co-chaired by myself and Andy Longford of PandA Europe, United Kingdom, put together a program with the theme: "The balancing act between consumer and harsh environment packaging." Seventeen high-quality presentations were accepted for this year's conference, which will take place October 25-26, 2016, in conjunction with SEMICON Europa in Grenoble, France—the largest microelectronics event in Europe.

From this year onward, the APC committee is reinforced by test experts. Test topics that interact with advanced packaging technology will be covered in one of the sessions at APC. The conference focus will be on the current industry needs and the transfer of solutions into manufacturing, rather than on basic research results. World-leading specialists in their fields will give four keynotes. Jan Vardaman, President of TechSearch International (Austin, Texas, USA), will open the "Market and Solutions" session, and will set the stage with her talk "Market drivers and packaging trends for automotive: Leveraging mobile device packaging technology." The second session "Technology and Modeling" will be opened by Gabriele Ernst, Engineering Director at Robert Bosch GmbH, Germany, with her keynote "Rapid introduction of new technologies for future automotive systems." Session number three, the "Testing and Qualification" session, will start with the keynote "Semiconductor test: A moving target cost, a changing landscape" by Cedric Mayor, CTO of Presto Engineering, France. The fourth and final session of the conference will deal with "Applications and Processes," and will commence with another keynote, given by Tobias Helbig, Senior Director CTO Innovation Management & Programs at NXP Semiconductors. He will speak on the topic of "Application-driven challenges in automotive packaging."

The latest advanced packaging technology development has always been driven by the consumer market – mobile and wireless communication applications – with the goal of finding solutions for those key critical aspects of packaging: performance, form factor, and cost. Years after the introduction of advanced packaging technologies, usually after a certain level of maturity and wider acceptance was achieved, other markets such as industrial, medical and healthcare, automotive, and even military and aerospace, tended to reuse those technologies, adapted to their typically higher requirements. Why did the industry undertake this adaption, and why does it continue to do so even more today? Because they are under the same continuously increasing pressure to address that critical triad of packaging: performance, form factor, and cost. Is automotive packaging with its specific performance and reliability requirements at consumer packaging cost possible or not? Join us at the conference, and you will see the industry's efforts to make it happen.

Xcerra, Spirox collaborate to provide advanced technology for the MEMS market in China

Xcerra recently announced that it has shipped the first complete fully tri-temp capable MEMS test cell for gyroscope test and calibration to SITRI, the Shanghai Industrial μTechnology Research Institute. The complete test cell solution includes an LTX-Credence Diamondx tester, Multitest InStrip handler, the Multitest InGyro sensor test module and a functional test program. The system is the first shipment of the new InGyro module to support testing at temperatures from -40°C to +125°C. Spirox Corporation, Xcerra's business partner in Taiwan and China, worked closely with SITRI to define this new solution, which supports the MEMS growth strategy of the Chinese government.

Charles Yang, President of SITRI noted that the group considers MEMS and sensors the main source of value in IoT systems. "They add the capability that gives "things" the ability to sense and respond to the environment," said Yang. "Therefore, MEMS/sensors is one of our areas of focus." The new Xcerra MEMS Test Cell expands the group's capabilities into characterization and production test.

Andy Nagy, Senior Director Marketing HG & TCI Operations, noted that by combining Spirox's knowledge of the Chinese market and expertise in MEMS applications support with equipment from Multitest and LTX-Credence, it was possible to develop the high-volume production test TCI solution. "The modular and highly flexible test cell allows SITRI to reconfigure the set-up easily to meet the requirements of future applications," said Nagy.

Yole makes the case for 2016 as the turning point for the fan-out market

Yole Développement (Yole) has announced that 2016 is a turning point for the fan-out market because both leaders — Apple and TSMC — changed the game and may create a trend of acceptance of fan-out packages ([Figure 1](#)). According to the research organization, TSMC investment in fan-out wafer-level packaging (FOWLP) and development of its solution, called InFO, changed the WLP landscape. The research group noted that following high-volume adoption of InFO and further development of embedded wafer-level ball grid array (eWLB)

technology, a wave of new players and FOWLP technologies may enter the market. In its latest report, Yole explains that TSMC's FOWLP solution will be used to package the Apple A10 application processor, implemented in the new iPhone 7 series.

"Production starts in 2016 and represents a big change in the fan-out industry for several reasons," noted Jérôme Azémar, Market & Technology Analyst, Advanced Packaging & Manufacturing at Yole. He observed that in terms of volume, capturing the Apple processor market is a big asset for fan-out technology because iPhone 7 phones are expected to be sold in more than 200 million units. According to Yole's advanced packaging and semiconductor manufacturing team, the market will actually be split into two types: the "core" FO market and the "high-density" FO market. Additional details can be found in the company's latest report: "Fan-Out: Technologies & Market Trends 2016."

Fan-Out activity revenues forecast (M\$) Breakdown by Fan-Out market type

(Source: Fan-Out: Technologies & Market Trends 2016 report, July 2016, Yole Développement)

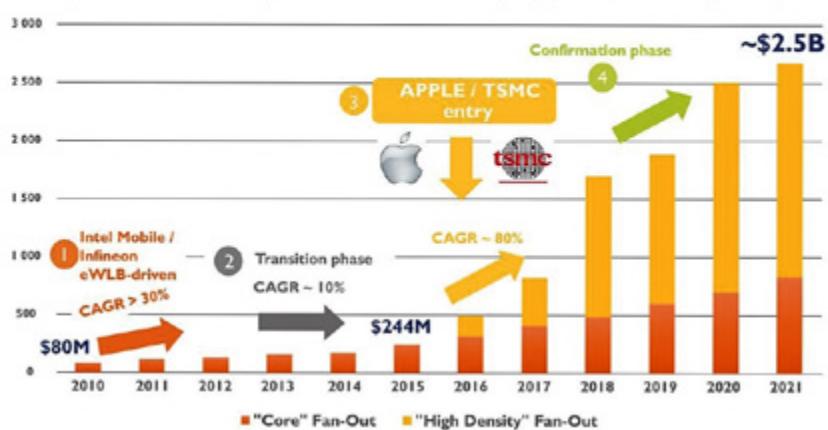


Figure 1: Fan-out activity revenues forecast (M\$); breakdown by fan-out market type. SOURCE: Fan-out: Technologies & Market Trends 2016 Report, Yole Développement

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New plasma dicing line emerges from Orbotech's SPTS collaboration with Novati

SPTS Technologies, an Orbotech company, has announced its collaboration with Novati Technologies to establish that company's new plasma dicing line at its state-of-the-art fab in Austin, Texas. "Plasma dicing has many advantages over conventional singulation methods and offers designers and manufacturers greater flexibility with regards to die shape, size and position," stated Kevin Crofton, President of SPTS Technologies and Corporate Vice President at Orbotech. According to SPTS, its Mosaic™ plasma dicing system with the Rapier-300S overcomes many of the design limitations of conventional dicing methods, particularly for smaller, thinner, more fragile die, as well as offering the potential for significant increases in yield and throughput.

"Novati provides customers with technology building blocks, engineering expertise, professional program management and a broad complement of flexible processing equipment that enable the accelerated development of 200mm and 300mm production-worthy solutions," stated John Behnke, President of Novati Technologies. "In order to remain at the forefront of novel process development, we must provide our foundry customers with the latest process solutions capable of manufacturing next-generation devices."

FormFactor expands its regional operation in Tech Hub, Suzhou, invests in a new facility

FormFactor, Inc. recently marked an important corporate milestone: ten years in China enabling local semiconductor manufacturers with essential wafer test technologies. To celebrate the occasion, company executives hosted an open house at FormFactor's new facility in Suzhou, near Shanghai. CEO Mike Slessor and FormFactor's China General Manager, Limin Yan welcomed local officials to the event, as well as customers, suppliers and employees.

Since 1993, the company has provided an extensive portfolio of high-performance probe card technologies and expertise to the global semiconductor industry. The cards are used to test integrated circuits (ICs) that power nearly every smart phone on the planet, as well as electronic systems used in computing, consumer and automotive applications. Over the years as IC complexity soared, FormFactor says it continually innovated to equip manufacturers with customized solutions to test their foundry & logic, DRAM, and Flash devices. The company employs approximately 1500 people globally.

Speaking at the open house event, Slessor said, "China's semiconductor industry is evolving fast, and presenting exciting opportunities for FormFactor. For ten years, we have shared valued collaborations with Chinese customers, beginning at the earliest design phase, and extending through final test where our technologies are deployed. Boosting our presence in China means we can partner more deeply and with a greater number of customers to help enrich their IC innovation. We're very pleased to be doing that from our new facility in Suzhou."

FormFactor's operations in Suzhou's high-tech hub began in 2006. The company, then known as MicroProbe, was a subsidiary of a US probe card company by the same name. When FormFactor acquired MicroProbe in 2012, the Suzhou operation became FormFactor China.

Now, to support its steadily-growing customer base in the region, the company has moved to a larger facility, also in Suzhou. The new 1410 sq. meter (15,170 sq. ft.) site houses the company's dedicated sales and support team for China, as well as technical experts that work closely with China-based customers to develop optimum test solutions for their unique IC designs. The company employs more than 80 people at this location.

FormFactor's China General Manager, Limin Yan, said, "FormFactor has a long tradition of working closely with customers to increase test yields and ensure faster time-to-test, while also reducing overall test costs. We will continue to follow the same collaborative approach, and are committed to investing in local R&D to produce high-quality test solutions and enable test success for our customers in China."

Applied Materials and A*STAR's Institute of Microelectronics to advance R&D in FOWLP

Applied Materials, Inc. and the Institute of Microelectronics (IME), a research institute under the Agency for Science, Technology and Research (A*STAR), has announced a five-year extension of their research collaboration at the Centre of Excellence in Advanced Packaging in Singapore. The organizations will expand the scope of their R&D collaboration to focus on advancing fan-out wafer-level packaging (FOWLP), a key technology inflection expected to help make chips and end-user devices smaller, faster and more power efficient.

With an anticipated additional S\$188 million of combined investment, the Centre will expand to a second location at Fusionopolis 2, in addition to the existing facility at Singapore's Science Park II. The two facilities combined will span an area of approximately 1,700 square meters and be staffed by a team of close to 100 researchers, scientists and engineers. The Centre was built to develop new capabilities in advanced packaging through a full line of Applied Materials' WLP processing equipment, and has successfully delivered advancements in semiconductor hardware, process and device structures.

"Our collaboration with A*STAR over the past five years has been instrumental in establishing Applied Materials' presence in Singapore and building up our R&D capabilities," said Russell Tham, Regional President, Applied Materials South East Asia. "With the entire R&D value stream from ideation to product development being carried out locally via this joint lab, the expansion will further Applied Materials' development of new technologies and products for global markets, while remaining a key contributor to Singapore's innovation economy."

Dr. Raj. Thampuran, Managing Director, A*STAR, said, "Our relationship with Applied Materials transcends a new milestone with the extension of our collaboration in R&D into new areas. The progress we have made from our initial collaboration is a testament to the successful partnership A*STAR has with Applied Materials. As we look towards the future, we remain committed to advancing innovations in the semiconductor industry and being at the forefront of leading edge ideas in this rapidly evolving technological landscape."

Qualcomm opens a semiconductor test facility in Shanghai

Qualcomm Incorporated has opened Qualcomm Communication Technologies (Shanghai) Co. Ltd., a semiconductor test facility in the Waigaoqiao (WGQ) free-trade zone in Shanghai, and its first foray into providing manufacturing services for semiconductors. By working with Amkor Technology, Inc., the new company will combine Amkor's test services experience and state-of-the-art cleanroom facilities with Qualcomm Technologies' cutting-edge product engineering and development.

According to Qualcomm, the new manufacturing facility demonstrates its commitment to continue to invest and help develop semiconductor expertise in China, and is indicative of growth in semiconductor market leadership in the country. Through the ownership and operation of a semiconductor test center, the company expects to enhance its focus on customer service, continue to develop its expertise in operational excellence, and increase its business presence in China. "The test facility is part of our continued mission to streamline supply chain operations and improve operational efficiency," said Roawen Chen, Senior VP, QCT global operations, Qualcomm Technologies, Inc. The Shanghai-based facility is set to begin operations on October 18, 2016.

IHS Markit: Medical imaging chip global unit volume to soar over the next five years

Robbie Galoso and Tom Hackenberg of IHS Markit released that company's opinion about the medical imaging chip market. According to the analysts, given the medical imaging industry's growing requirements for power savings, higher resolution and the need to support integrated security and communications, the unit volume of semiconductors used in medical imaging will continue to increase (**Figure 2**). The market grew at a five-year compound annual growth rate of 8.2%, from 46 million in 2015 to 73 million in 2020. Even with increasing demand for energy-efficient and integrated components, year-over-year global revenue growth from semiconductors used in medical imaging was flat, due to optical component price erosion, reaching \$1.1 billion in 2015.

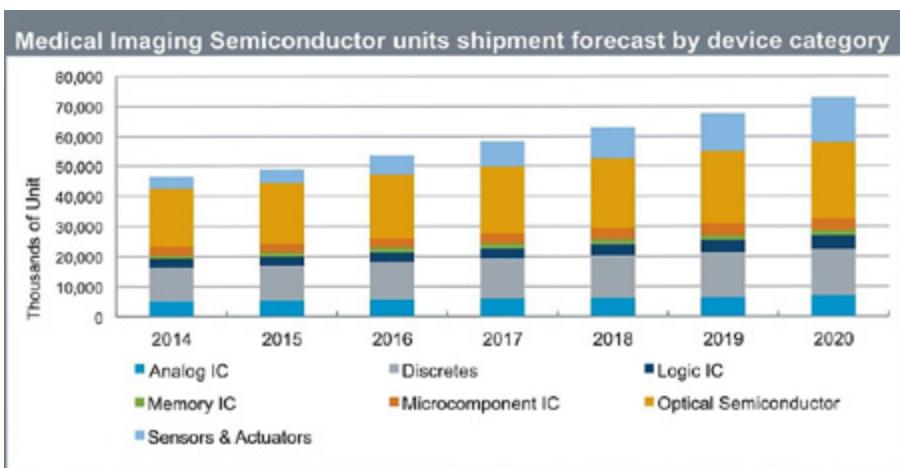


Figure 2: Medical imaging semiconductor units shipment forecast by device category. SOURCE: IHS

The researchers further noted that one of the most important trends in the semiconductor industry today is the development of chip solutions that integrate several components into a single chip package to minimize size, save energy and lower production cost without sacrificing functionality. "As the size of semiconductors continues to decline, imaging systems that used to cost more than a million dollars — and which traditionally required a lot of space to install — have evolved into smaller, less-expensive systems that can be used in small clinics or doctors' offices," explained the analysts.

The analysts also released information about the IHS Markit Industrial Semiconductor Market Tracker, which tracks the following four major types of medical imaging equipment (the following medical imaging data comes from the IHS Markit Medical Devices and Equipment service):

1. The ultrasound market is forecast to grow 4.7% over the next five years. Portable ultrasound in China is not growing as fast as previously expected, due to less capital investments and strategy shifts toward higher-end systems from major suppliers. "With ultrasound typically costing less than computed tomography (CT) and magnetic resonance imaging (MRI), healthcare reform is likely to favor the more widespread adoption of ultrasound, which bodes well for patients and doctors opting for systems that minimize radiation exposure," said the analysts.
2. The X-ray market is expected to grow 5.3%, led by mobile X-ray replacing existing analogue mobile systems with more efficient and higher-priced digital X-ray systems — especially in the APAC region.
3. The MRI market is expected to grow 6.4%, due to higher demand for open MRI in emerging markets, which is more cost-effective than closed systems. Open MRI has not gained traction in the United States and other mature markets, because of its lower field strength and weaker image quality compared to closed MRI.
4. The CT market is expected to grow 4.2%, led by 64-slice systems that are more cost effective than the 128-slice systems, but still provide sufficient image quality for diagnostic purposes. As the 128-slice system market matures and the devices become more affordable, it will gradually gain momentum, said the analysts. "The demand for less-than-16-slice systems and 17- to 63-slice systems will continue to decline, because emerging regions are price-sensitive and quality is not a primary consideration," noted the analysts.

Galoso and Hackenberg also observed that the demand for high-quality and innovative medical imaging has increased the advancement, performance and penetration of semiconductors and sensors. Ongoing component price erosion continues to intensify across the semiconductor industry, as semiconductor manufacturing continues to increase significantly in China. “Complementary metal–oxide–semiconductor (CMOS) image sensors are highly predominant in CT-scan and X-ray systems, allowing amplified cross-sectional image slices of scanned body areas with higher resolution, faster data throughputs and better diagnostics,” said the researchers. “CMOS is an emerging technology that is preferred over charge-coupled device (CCD) technology, due to lower cost, higher readout speed and less noise. Scanner performance improvements and innovations have significantly increased slice count, leading to faster and clearer images. It is also a lot safer for patients, thanks to its reduced radiation dosage levels.”

More power discrete and module semiconductors are required for motor control and input-power refinement — especially in MRI systems requiring greater magnetic-field strength, with the transition to 3 Tesla (3T) technology, said the report’s authors. “Analog semiconductors are also prevalent in the medical imaging market, due to the integration of low-noise amplifiers, voltage-to-current amplifiers, and multi-channel analog-to-digital converters (ADCs) into single analog front-end integrated circuits (AFE ICs), noted the report. These circuits are much smaller, and dissipate less power, than earlier-generation parts, while providing twice the performance. “Analog advancements have addressed the low-power and low-cost needs of CT scanners with high slice counts and clearer images,” said the analysts. “A high-resolution ADC must be used during an MRI scan to produce a strong magnetic field.”

The report also noted that processors are another crucial component and differentiator in medical imaging devices, including microcontrollers (MCUs), microprocessors (MPUs), digital signal processors (DSPs), applications/media processors (APs) and configurable system-on-chip (CSoC). AP is defined under application-specific logic, explained the researchers. Configurable processors, including field programmable gate arrays (FPGAs) and CSoCs, are defined under programmable logic devices. “Processor trends in medical imaging reflect – and even exemplify – trends that are occurring across the semiconductor industry,” said Galoso and Hackenberg.

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Biography

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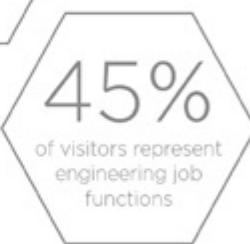


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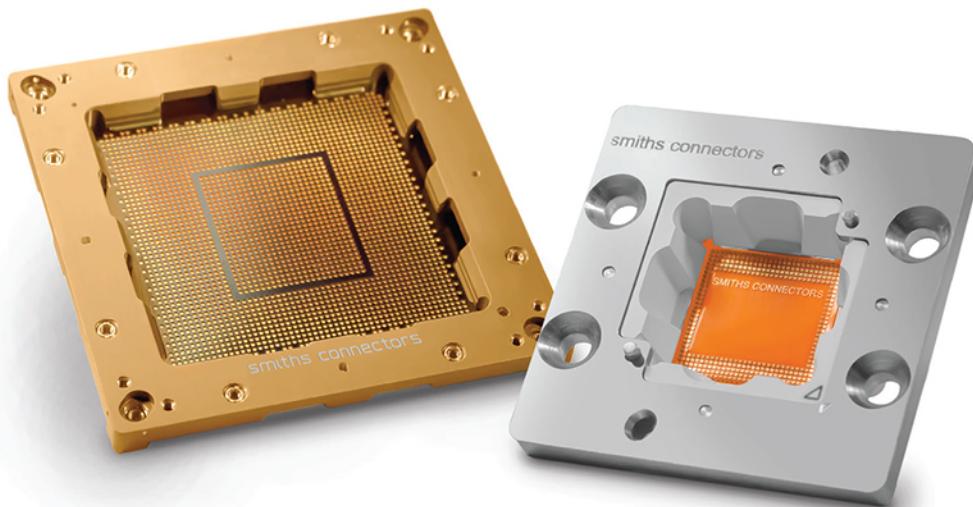
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