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The Future of Semiconductor Packaging

Volume 20, Number 4

July • August 2016

Advanced eutectic packaging

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- Direct bonding technology
- Materials development for SiP
- MEMS packaging in the IoT era
- Conductive elastomer contactor applications
- Silicon 3D integration for small power devices





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Eutectic bonding is an area of particular interest to photonics, microwave and RF electronics, because of the need for a clean, highly thermally efficient process, as well as for long-term reliability. Increasing demand for communications data and bandwidth accelerates the adaptation of full automation and the improvement of processes in advanced eutectic packaging for volume production. These advances result in high-precision, high-throughput, improved yield, and new products for the component and module manufacturers.

Photo courtesy of MRSI Systems

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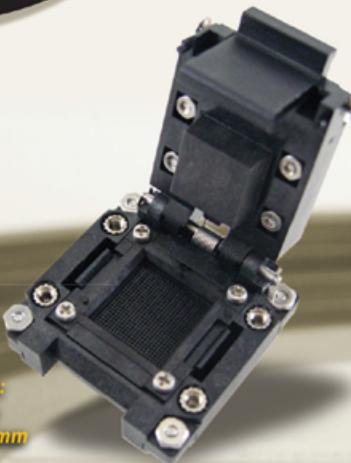
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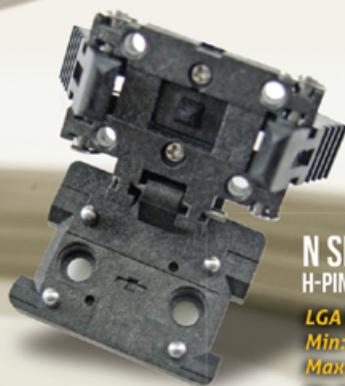
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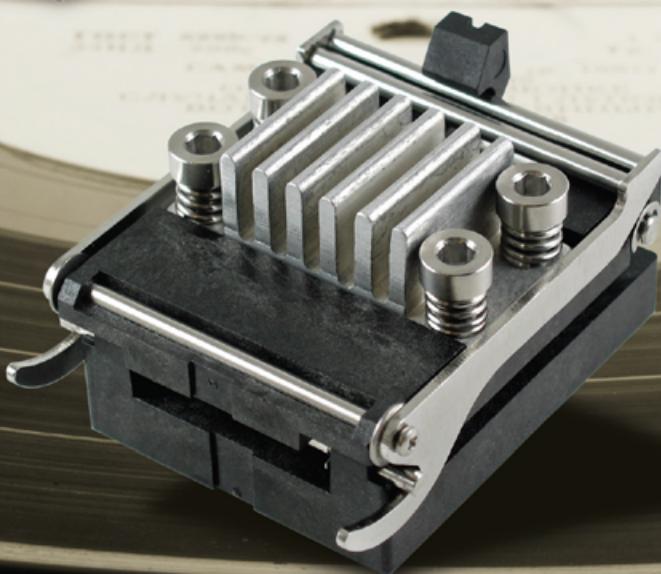


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Liquid crystal polymer air cavity plastic packaging in RF applications

By Alex Elliott, Jim McDearmon [RJR Technologies]

In the highly competitive RF communications market, manufacturers need RF power transistors and packaging solutions that help them support higher linearity, higher average output power, and wider operating bandwidths. At the same time, given that the power transistor represents the single most expensive device in the power amplifier (PA), they need to find new ways to drive down costs. Together these relentless price/performance requirements are pushing designers to migrate from traditional ceramic or ceramic-metal packages or over-molded package solutions to alternative liquid crystal polymer (LCP) air cavity plastic (ACP) package options that use less expensive copper thermal bases for higher thermal performance.

ACP packages are becoming a proven, lower cost alternative to air cavity ceramic (ACC) packaging for cellular base stations and other communications systems. Moreover, the advantages of LCP packages are enabling IC manufacturers to target a host of new RF energy applications such as lighting, consumer cooking, automotive, emerging medical markets and industrial use. This article will look at why low-cost LCP packaging is driving designers to explore alternatives to over-molded and ACC packaging.

Driving down cost

Over-molded plastic packaging has for years been the preferred lower cost packaging technology of choice, particularly for commodity products such as memories or small signal transistors. The technology encapsulates the IC in a polymeric material that acts not only as a dielectric insulator, but also helps protect the device from mechanical and environmental degradation. Supported by high-volume manufacturers and suppliers, over-molded packaging is particularly attractive from a cost perspective. With a cost-per-lead running in

the fractions of a cent including die and wire bonding, this approach can offer designers an order of magnitude cost advantage over traditional ceramic packages.

For RF system designers seeking to take advantage of the cost benefits noted above, the primary obstacle has been rising performance requirements. Unlike in air cavity packages, the polymer material in over-molded packages comes into direct contact with the die and bond wires, which limits package performance. Given that polymers exhibit a higher dielectric constant than air, an over-molded package will experience higher parasitics that can lower power output and gain depending upon the design and tolerance of the encapsulated die. Another issue has been reliability. The technology's high moisture absorption rate can lead to a "popcorn" effect when moisture collects and explodes in the assembly process.

Traditional alternative

Historically, device manufacturers have primarily relied on ACC packages to meet stringent RF power performance requirements. The ACC package has proved attractive because it combines a thermally and electrically conductive metal base with a ceramic ring that isolates the input and output leads. In turn, these packages deliver higher electrical isolation for the silicon die than comparable over-molded packages and are especially well-suited for high-frequency, high-power applications. Equally important, the ACC package provides excellent durability for the high-temperature soldering used in the assembly process. Widely implemented in RF applications, the ACC package is available today in a wide range of designs from multiple established suppliers.

ACP packages feature a metal base comprising a laminated structure of copper/copper-moly/copper (CPC) that is joined to a metallized and plated ceramic ring

via a high-temperature brazing process. Typically, the ceramic base is gold-plated to allow the die to be attached by a eutectic process. A ceramic lid with pre-applied epoxy is typically used to seal a near-hermetic ACC package by attaching the lid to provide environmental protection.

Clearly the metal-ceramic packages widely used today offer designers a reliable, proven solution for high-performance RF applications. But they also present some distinct disadvantages. One issue is cost. In today's highly competitive base station market, designers are constantly searching for new cost efficiencies. The ACC package relies on a relatively expensive high-temperature fired ceramic and brazed assembly process to form the air cavity package. As a result, today a ceramic package represents a large portion of the total cost of a finished power RF device.

As base station design specs moved to wider bandwidths, higher power levels and higher frequencies, thermal efficiency has also proved to be a major challenge. Designers want to use a copper heat sink because it offers 30% better thermal conductivity than current CPC flanges used in ceramic packages at much lower cost with higher performance. With a coefficient of thermal expansion (CTE) approximately three times as large as current ceramic flange material, ACC packages can't use a copper flange material because the CTE mismatch will cause the ceramic ring to crack during the brazing process.

New advances

One option to address the issues described above is to migrate to ACP packages. ACP technology uses an air cavity structure similar to a ceramic package to maximize electrical isolation of the silicon die. These ACP solutions support a wide range of applications with frequencies from L to V band. Moreover, they offer the high performance at improved cost, not only from

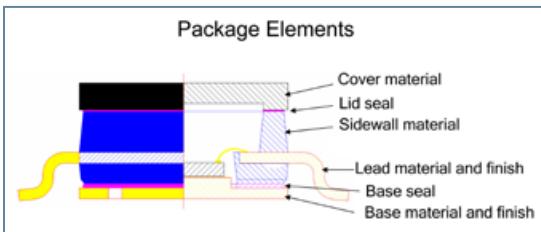


Figure 1: ACP packages use an insert-injection molding process that combines a metal alloy lead frame with an LCP sidewall and matching lid with a pre-applied B-staged epoxy.

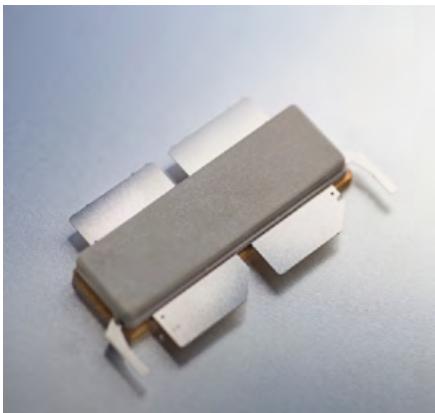


Figure 2: ACP packages allow designers to use lower cost, higher conductivity copper bases.

a piece-part perspective, but also from an assembled one because ACP packages can be assembled in-strip, thereby eliminating all the non-value added labor needed to transfer singulated packages from their shipping tray into expensive Auer boats.

Packages using ACP technology employ an insert-injection molding process that combines a metal alloy lead frame with an LCP sidewall and matching lid with pre-applied B-staged epoxy as shown in **Figure 1**. Also, ACP packages can employ any eutectic die attach process used with ACC packages. The use of this lower temperature, compliant epoxy material essentially makes the package independent of the flange material. As a result, manufacturers can use any of a variety of base/flange materials to meet specific CTE matching and thermal management requirements. These base/flange materials range from ceramic LTCC and HTCC to copper alloys, OFHC copper and diamond, with thermal conductivity capabilities that range from 10W/K to 1000W/K.

ACP packages, shown in **Figure 2**, have been successfully used with CuW,

Cu-MoCU-Cu, Al-diamond and copper flanges. It is the only packaging technology that allows designers to use lower cost, higher conductivity copper bases. Furthermore, today's ACP packages feature a flat sealing surface from lid to package and sidewall to the flange. This reduces the epoxy cross-sectional thickness between the lead and the package and increases the shear/adhesion strength of the lid to package. Another major advantage of ACP is it has one-third the dielectric constant of ceramic, therefore, providing improved RF performance. ACP technology offers the designer a fully matched CTE solution. With a low water absorption rate of just 0.02%, ACPs also offer near-hermetic reliability.

Furthermore, ACP technology makes the package assembly process easy to fully automate for high-volume production. Prior to ACP, assembly houses purchased ceramic power RF packages as singulated components, which require the use of expensive carriers to process the singulated packages. This requirement not only adds more labor to the process, it also drives up material costs. In many other types of semiconductor packaging, the in-strip or array formats let manufacturers maximize efficiency by assembling in a multi-up format.

Summary

Given the long term trend in RF power transistor performance requirements and the key role they play in the overall

reliability and cost of RF systems, it seems clear that traditional ACC packaging will offer only limited utility in the years ahead. As performance requirements continue to be more demanding over time, designers will need a more reliable packaging solution at lower cost. By delivering a matched CTE solution with near-hermetic reliability at low cost and capable of supporting high-volume assembly techniques, ACP packaging offers designers a new high-performance option for today's rapidly growing RF markets.

Biography

Alex Elliott attended Coatbridge Technical Institute; he is Senior Engineer at RJR Technologies; email aelliott@rjrotechnologies

Jim McDearmon received his BS degree from California State U., San Diego, and is Director of Operations at RJR Technologies.

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Flip-chip LED packaging

By Martine Simard-Normandin, Christina Banks, Roderick Sparks [[MuAnalysis Inc.](#)]

Light emitting diodes (LEDs) have been around since the 1960s, but it is only in the last decade that they have become of significant technological and economic importance. Advancements in III-V semiconductor epitaxial technology have led to the development of high-brightness emitters. LED packaging followed suit in order to take advantage of these devices and maximize their efficiency. This paper examines two significant improvements made in LED packaging for high-intensity LEDs.

Introduction

LEDs are no longer relegated to such roles as low output power indicator lights on panels or as seasonal decorative light strings. They have found applications in small displays, TVs, large displays, camera flash, lighting: A19, fluorescent tube replacement and other light bulbs, architectural and street lighting, automotive, bio-medical instrumentation, and as part of sensors for the Internet of Things (IoT).

Different applications need LEDs of different colors. For general lighting and back panel lighting in LCD displays, white LEDs are used. For very large outdoor displays, RGB (red, green, blue) LEDs are preferred. In automotive, every available color is used depending on the function and placement (dashboard, turn signals, cabin, etc.). High-intensity LEDs are current-controlled devices that generate significant heat during operation. The main goals of LED packaging are to dissipate the heat, send the emitted light when it is intended, and protect the semiconductor die from harm.

The major improvements in LED packaging have been driven by

improvements in the efficacy of blue GaN LEDs and by the need to solve reliability issues associated with phosphor darkening as LEDs age.

Flip-chip packaging

Several high-intensity white LEDs have a die size of up to 1mmx1mm and draw current reaching 1A. The traditional geometry of two wire bonds connecting the anode and cathode does not work for these devices. Too much of the anode surface would need to be covered by metal to avoid current crowding and local overheating. Most high-intensity devices use one form or another of flip-chip geometry. The GaN is transparent, therefore light has no problem escaping. In most cases the sapphire wafer has been removed and the GaN thinned down to under 10 μ m. The active region, where light is emitted and where the heat is generated, is within the first quarter micrometer of the surface on the p-side. Putting the p-doped surface in contact with the package metal is an efficient way to extract the heat away from the semiconductor. With the die upside-down and thinned, the cathode is fully accessible and the earlier devices from Cree and Osram

placed an electrode on the cathode surface. Lumileds used an array of vias drilled through the anode to contact the cathode from the package side, avoiding any obstruction to the light path. This approach is now used almost universally.

The GaN layer is the very thin surface layer seen in the Cree device in [Figure 1](#). The electrode metal is in contact with the n-GaN. The p-GaN is in contact with the thick die, made of a highly conductive material, and the anode bond wire is beside the die. Different materials are used for the conductive die: silicon, germanium and metal alloys are common.

Lumileds makes contact with the cathode and anode metals using gold bumps in classic flip-chip approach. A thick redistribution layer is used to carry the signals to the appropriate bump and to extract the heat. The space between the bumps is packed with silica-filled epoxy underfill material. This underfill is clearly seen in [Figure 2](#). The surface of the p-GaN is usually coated with silver in order to reflect all the emitted light back through the GaN. The redistribution layer makes contact with the silver layer in a series of windows that cannot be seen from the top because

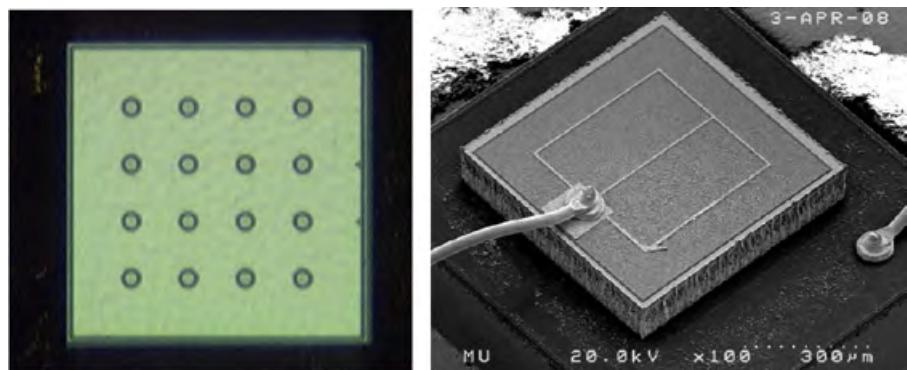


Figure 1: A Lumileds LED and a Cree LED viewed from the top.



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the silver is opaque. One such layer is shown in [Figure 2](#).

Osram uses a different approach. Vias to the n-GaN connect to a conductive die that serves as the cathode. The silver-coated p-GaN and associated electrode metal are isolated from the cathode by a layer of dielectric material. A bond pad is created in the corner to connect to the anode.

Phosphor plates

The conversion of the blue light emitted by the LED to white light is achieved by a phosphor layer. Typically, small particles of rare earth compounds, approximately $10\mu\text{m}$ across, are embedded in silicone and deposited on the LED surface and the package surface. A thick over-layer of clear silicone or a lens is often deposited on top. Although silicones can resist high temperatures, high-intensity LEDs often operate at temperatures higher than their tolerance. The silicone can decompose and/or carbonize. It darkens and loses transparency, affecting the color temperature of the LED and its intensity. Newer devices use a phosphor plate. The phosphor particles are ground fine and incorporated in a thin refractory ceramic plate. This plate is glued to the LED surface using a thin layer of clear silicone.

Cross sections of two different devices are shown in [Figures 3](#) and [4](#). The active GaN layer is less than $10\mu\text{m}$ thick in each case, therefore it cannot be seen in the optical cross-section image. However, it is visible in the electron microscope image taken at much higher magnification. The GaN layer is softer than the phosphor plate and substrate, and has a tendency to crumble during a polished cross section. In devices with an anode bond wire, the plate is notched. A thick white silicone layer surrounds the plate and prevents intrusion of contaminants under the plate. The anode metal can be seen in the cross-section image as a thin white layer covering the substrate and connecting to the bond wire and

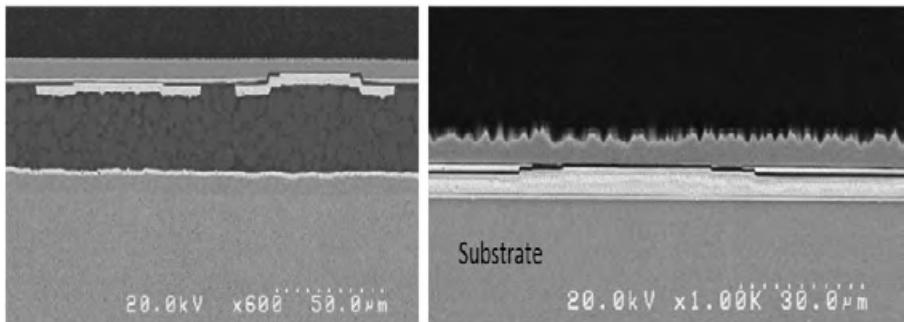


Figure 2: Cross section of a Lumileds and an Osram device intercepting a via to make contact with the n-GaN. The Osram device uses a solder layer between the GaN and the substrate.

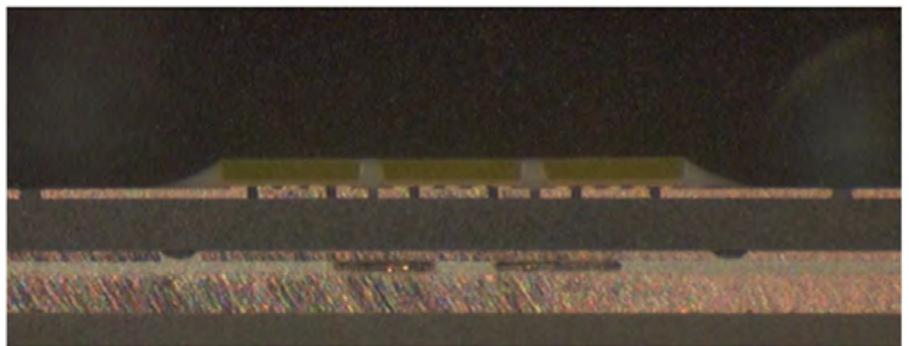


Figure 3: A multi-chip LED with phosphor plates. The GaN LEDs are so thin, they cannot be seen at this magnification.

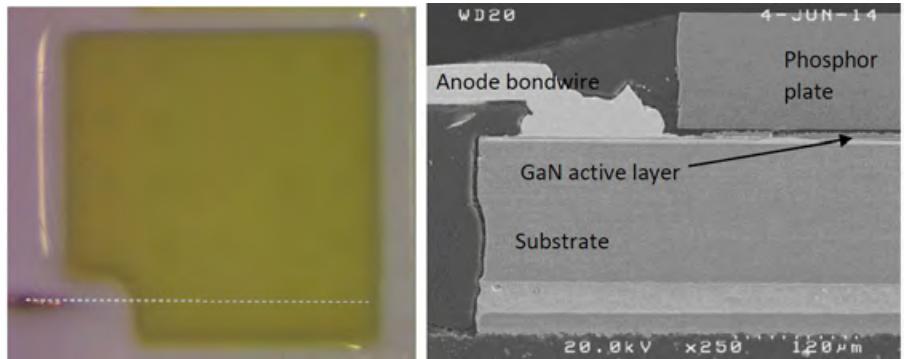


Figure 4: Plan view and cross section of an Osram flip-chip device with a phosphor plate. The cross section is at the location of the dashed line and intercepts the bond wire.

to the GaN. In the optical plan-view image, an array of round cathode vias can just be seen through the plate, but the vias have very poor contrast. The cross section does not intercept a via.

These ceramic phosphor plates have higher thermal conductivity than silicone and help dissipate the heat generated by the LED. They are principally used in high-intensity LEDs. The thin layer of silicone attaching the plate to the LED is

protected from overheating because it can shed heat to the phosphor plate.

Failure modes

Every system has a weak point and this is where failures occur. In flip-chip devices using solder in the vias, like the Osram device shown in [Figure 2](#), the current crowds in the vias and the solder alloy forms voids that increase the contact resistance, which in turn increases the local heating. At the edges of vias, the

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anode metal and cathode metal are only separated by a thin layer of deposited dielectric. Any electrostatic discharge risks causing a dielectric breakdown. In devices that use a silicone lens on top of the phosphor plate, we have observed badly burned silicone while the phosphor plate remains intact. The plate can get hotter than the silicone lens can tolerate. One needs to be careful not to overdrive such emitters. A popular application of this type of flip-chip device is in camera flash. In flash mode, short bursts of very intense light are emitted and the device cools off rapidly. In flashlight mode or video mode the device can be on for long periods and could overheat. However, in most devices, the LED controller chip reduces the current in such cases and pulses the part in synchronization with the video rate to avoid overheating.

Cost reduction

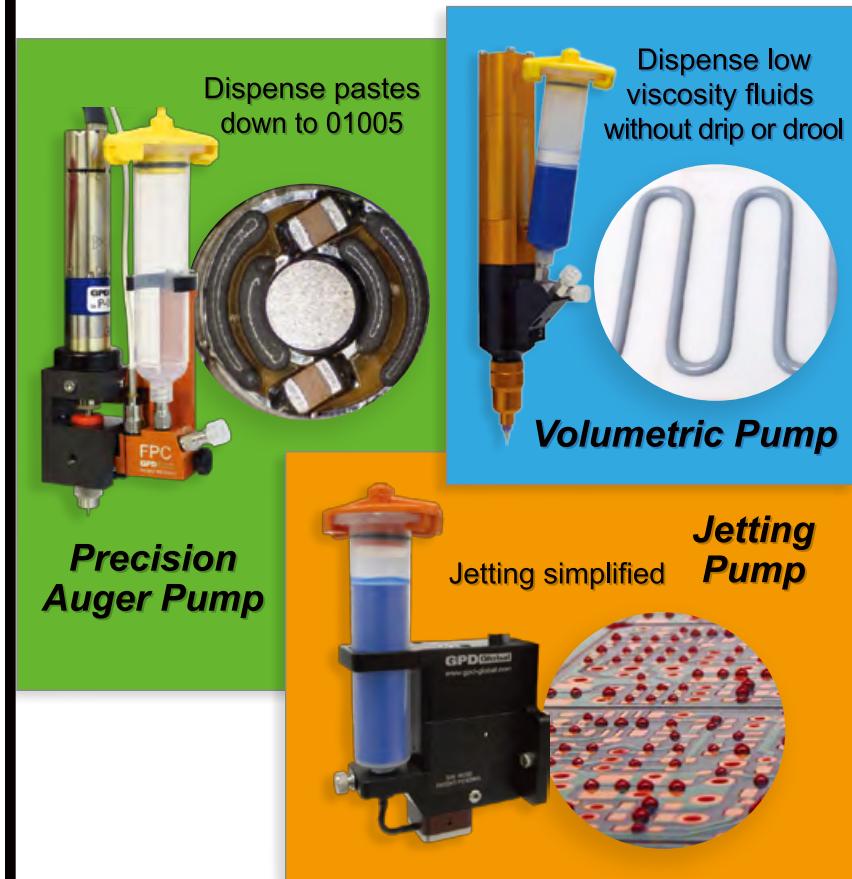
Ceramic phosphor plates are very expensive and the technology reserved for high-end products. Cheaper versions of the same principle are being developed. Phosphor particles embedded in glass or thermoplastics are seen in medium- and low-intensity LEDs. Chip-scale packaging is rapidly gaining popularity for small LEDs, avoiding the complexity of wire bonding and reducing packaging costs. The evolution of LED packaging is going in the direction of no packaging, or as little packaging as possible.

Biographies

Martine Simard-Normandin holds a BSc in Physics from the U. de Montréal, and MSc and PhD degrees in Astronomy from the U. of Toronto. She was awarded an Industrial Postdoctoral Fellowship from the American Physical Society and is President of MuAnalysis Inc.; email martine@muanalysis.com

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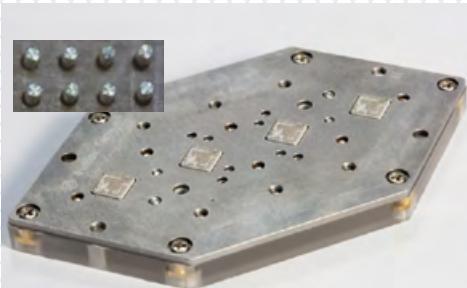
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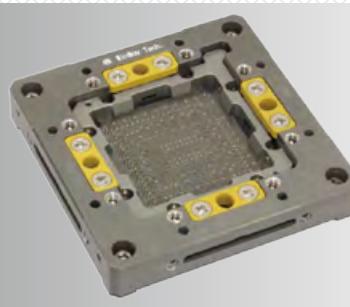
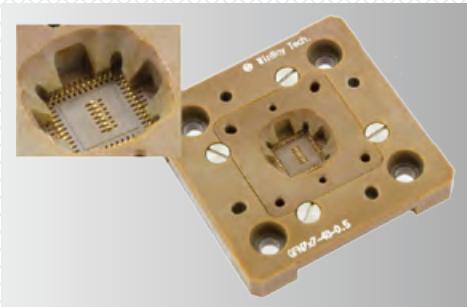
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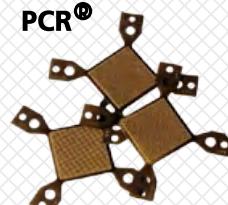
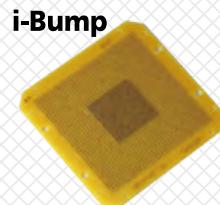
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Package warpage: the “twist” to an unnatural failure mode in a board-level FCBGA environment

By Jaimal Williamson [Texas Instruments]

Warpage in semiconductor packaging applications is an occurrence as natural as the ubiquitous events of drinking and eating in everyday life. The multiple conformations a package can exhibit during heating and cooling can lead to a myriad of challenges if not properly characterized, ranging from reliability to surface-mount (SMT) issues. One of the main responsibilities of packaging engineers is finding clever methods to control or minimize warpage generated by coefficient of thermal expansion (CTE) mismatch, which is an inherent consequence when two dissimilar materials are in contact (i.e., silicon chip to organic package or organic package to printed circuit board). Some of the methods for warpage control include, but are not limited to, optimal material property selection of package bill of materials including core and build-up dielectric layers, balancing copper density between package layers, or increasing core thickness. Other warpage control methods can involve innovation during the assembly process to counteract the CTE mismatch in play.

To add fuel to the fire of the everlasting challenge of warpage control, there is an industry-wide proliferation to reduce the thickness of flip-chip ball grid array (FCBGA) substrates (Figure 1) by designing fewer build-up layers. This enables lower cost opportunities and improves electrical performance. For packaging engineers, the challenge to qualify a thinner FCBGA package and maintain warpage control ostensibly seems a paradox, but it could translate into a lower stress state on account of fewer copper (Cu) and build-up dielectric layers. From a composite substrate or package stand point, the trend is a CTE reduction with fewer build-up stacks [1]. This is due to the substrate core material playing a more dominant role in the overall stack

as a result of lower Cu density with fewer substrate layers. The lower CTE of the package/substrate creates a better match to the adjoining silicon chip, thereby improving temperature cycling reliability at the first-level solder joint between chip and package. However, the lower CTE of the package/substrate creates the opposite effect with respect to CTE matching between the package and the printed circuit board (PCB). As a result, second-level solder joint reliability (between package BGA joint and PCB) is compromised on account of greater CTE mismatch between package and PCB. Second-level joint reliability will be a focus of this article, where comparison between an eight-layer, 3/2/3, and a thinner six-layer, 2/2/2, build-up stack (see Figures 2 and 3) are showcased.

Comparison between 3/2/3 and 2/2/2 build-up stacks

In this study, two daisy FCBGA packages of mostly comparable package attributes were evaluated during board-level reliability (BLR) as shown in Figure 4. The BLR condition was -40°C to 125°C based on the IPC-9701 specification [2]. The main difference between the 3/2/3 and 2/2/2 build-ups is that the latter has one layer removed above and below the core as illustrated in Figures 2 and 3. Weibull analysis based on in situ measurements was performed to illustrate the BLR results at 5% and 63.2% cycles to failure between the two aforementioned build-up stack configurations (refer to Figures 5 and 6). The thinner 2/2/2 build-up substrate design showed about a 35% reduced fatigue life

compared to the 3/2/3 counterpart at 5% cycles to failure. Following a similar trend, the fatigue life reduced ~27% at 63.2% cycles to failure with the thinner 2/2/2 substrate design as compared to the 3/2/3 version.

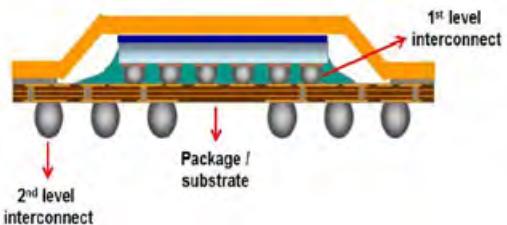


Figure 1: Example of an FCBGA package.

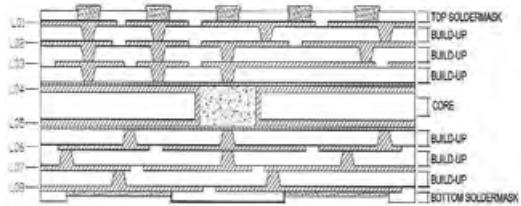


Figure 2: Example of a conventional 3/2/3 build-up stack (eight layers) in an FCBGA package.

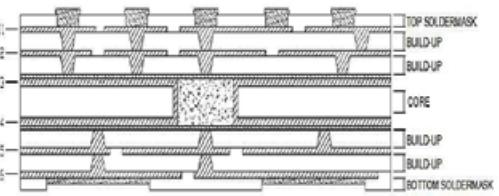


Figure 3: Example of a conventional 2/2/2 build-up stack (six layers) in an FCBGA package.

Description	Case 1	Case 2
Body size (mm x mm)	40 x 40	40 x 40
Build-up stack	3/2/3	2/2/2
Core thickness (μm)	800	800
BGA pitch (mm)	1	1
Bottom-most substrate layer Cu thickness	15	22

Figure 4: Comparison of cases 1 and 3 between a 3/2/3 vs. a 2/2/2 build-up FCBGA package.

Ball Placement System

(Micro Solder Ball Mount Technology)



BPS-8200
Ball Placement System

System Performance

Cycle Time :
12~14 Sec (Normal Package(1 Dotting/Strip))
25~30 Sec (Fine Pitch Package(2 Dotting/Strip))
40~45 Sec (Fine Pitch Package(2 Dotting/Half Strip))
YIELD PERFORMANCE : 99.98%
Placement Accuracy : +/- 0.02mm
Fine Pitch Capability : 0.100mm_Ball size / 0.180mm_Ball pitch
Strip Handling Capacity : 50 ~ 95mm Width x 180~260mm Length
Product Flexibility : All kinds of laminated Substrate BGA Package series
Quick Conversion Time : Ball tool, Flux tool, Lift Block
Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)
Foot Weight : 3,000kg

BPS-8200 Process (Stand alone type : Magazine Input)



BPS-8200S
Ball Placement System



BPS-7200FC
Ball Placement System
for Flip Chip



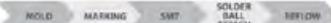
wBPS-2000
Wafer Solder
Ball Placement System



Cycle Time : 120sec/wafer(12"wafer ~880,000 Ball)
High Capability : +/- 0.02mm
Fine Pitch Capability : 0.050mm
Ball size & 0.120mm mm Pitch
Target Device : 8,12inchwafer
High Productivity : Max 30WPH
Wafer Chuck - XYZ9 axis
PRS vision -Look Up type
Stencil, Wafer Vacuum Chuck
Lm Guide + Ball Screw
Wafer LoadingLinear motion
Vacuum ejector
Inlet PRS Vision
Flux Y axis servo motion
Flux Squeegee Blade
ABL™ (Air floating Ball Loading unit)
Foot Print : 2900(L) x 1300(W) x 2100(H)

Cycle Time : 12~14 Sec (Normal Package(1 Dotting/Strip))
25~30 Sec (Fine Pitch Package(2 Dotting/Strip))
40~45 Sec (Fine Pitch Package(2 Dotting/Half Strip))
YIELD PERFORMANCE : 99.98%
Placement Accuracy : +/- 0.03mm
Fine Pitch Capability : 0.100mm_Ball size / 0.180mm_Ball pitch
Strip Handling Capacity : 50 ~ 95mm Width x 180~260mm Length
Product Flexibility : All kinds of BGA Package series
Quick Conversion Time : Ball tool, Flux tool, Lift Block, Stripper(Optional)
Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)
Foot Weight : 3,000kg

BPS-8200S Process (inline type: Substrate Input)



Package EMI Shielding System

H-VAM Application



PSS-8000SL
Package Sorting System

System Performance

UPH : 13,000
Yield Performance : 99.9%
Placement Accuracy : +/- 0.15mm
Picker : 14 Pickers x 2 Head
Package Type : 3x3 mm ~ 20x20 mm LGA, BGA
Product Flexibility : LGA, BGA PKG Applicable
Quick Conversion Time : Detach tool, Picker pad, Precise tool
Foot Print : 3,460(L) x 2,090(W) x 1,760(H)
Foot Weight : 3,500kg



PSS-8000SUV
Package Sorter System with Vision

PI-TAPE Application



PSS-7000SL
Auto Package Loading
P&P System

System Performance

UPH : 12,000 / 8,000
Yield Performance : 99.9%
Placement Accuracy : +/- 0.15mm
Picker : 14 Pickers x 2 Head
Package Type : 3x3 mm ~ 20x20 mm LGA, BGA
Product Flexibility : LGA, BGA PKG Applicable
Quick Conversion Time : Detach tool, Picker pad, Precise tool
Foot Print : 3,460(L) x 2,090(W) x 1,760(H)
Foot Weight : 3,500kg



PSS-7000SUV
Auto Package Loading
P&P System

UPH : 10~12K (Based on 860Unit/ Frame)
Placement Accuracy : +/- 0.05mm with Theta axis
Product Flexibility : 3x3 mm ~ 20x20 mm
LGA, BGA PKG Applicable
Quick Conversion Time : Picker Pad: Less than 20Min
Reject sorting : Rework Tray
Vision System : Top Frame Align - 1.4K (FOV 20.0x15.0, Resolution 14um)
Top Picker Align - 5M (FOV 22.0x16.0, Resolution 9um)
Bottom Align - 4M (FOV 20.5x20.5, Resolution 10um)
Motion Picker : 10ea x 2set (individual Z, T motion)
Detach Picker x 2set
Foot Print & Weight : 2,050(L) x 2,000(W) x 1,800(H) / 2,500kg

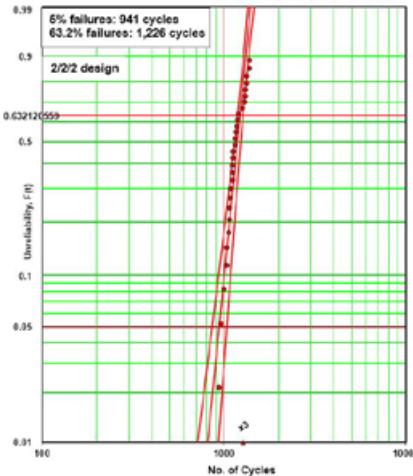


Figure 5: Weibull plot of a 2/2/2 build-up substrate design.

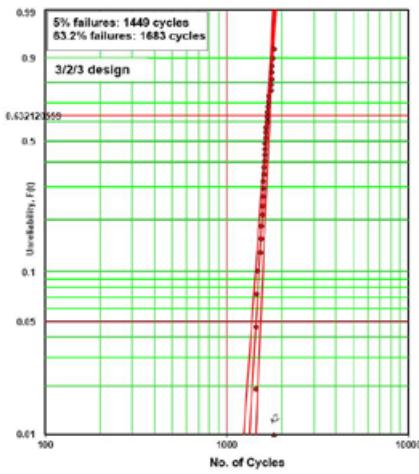


Figure 6: Weibull plot of a 3/2/3 build-up substrate design.

Despite the disparity from Weibull analysis, BLR results from the 2/2/2 substrate design were well within failures in time (FIT) life calculations and use conditions for the device. Upon detailed failure analysis of the 2/2/2 substrate design, two failure modes were evident (**Figure 7**). The expected failure mode of solder fatigue in the bulk SAC305 (Sn3.0Ag0.5Cu) solder joint occurred in the die shadow region of the package—deep into temperature cycle testing. The die shadow region is a high-stress area due to CTE-driven chip area warpage. Stress modeling corroborates a high-stress region at die shadow area (**Figure 8**).

The second failure mode found at the package corner between the brittle intermetallic compound (IMC) layer and the package side Cu pad was surprising, as it is not a fatigue-induced failure generated by shear stress. Since it is logical that IMC

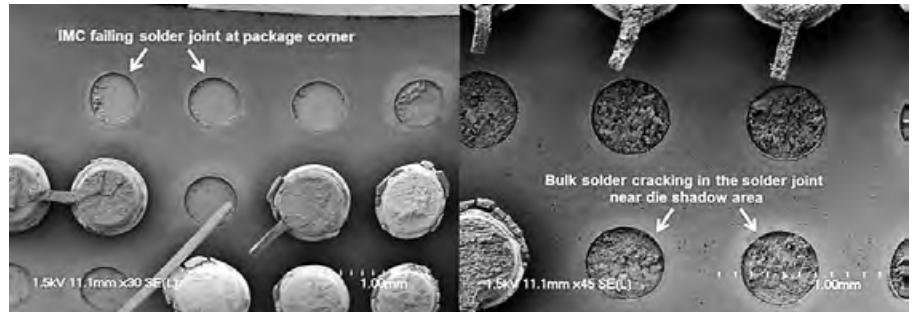


Figure 7: Failure analysis showing brittle IMC (left) and bulk solder cracking (right).

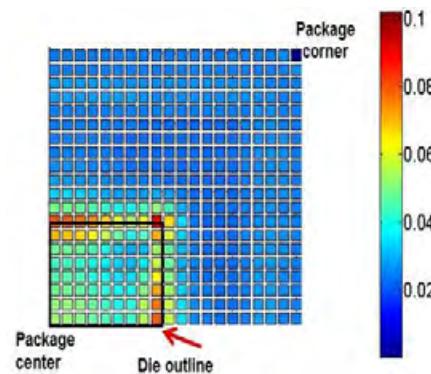


Figure 8: Modeling simulation of high damage area in the die shadow region of the package.

failure is manifested by a tensile or peel stress [3,4], warpage characterization was carried out to better understand this unnatural failure mode during BLR.

Warpage review

Shadow moiré was performed to characterize package warpage at various temperatures. Warpage measurements were taken from 25°C to 260°C to simulate a lead (Pb)-free solder temperature profile. Temperatures of 25°C, 100°C and 150°C were used as reference temperatures to compare package displacement during BLR temperature cycling. JMP® statistical analysis revealed that the most significant difference in warpage between the 3/2/3 and 2/2/2 build-up stacks was at 25°C (see **Figure 9** – connecting letters report). Again referring to **Figure 9**, JMP data also shows that the standard deviation has a much wider spread with the thinner 2/2/2 build-up stack than its 3/2/3 counterpart. Warpage values consistently deviate more from the mean value at 25°C, 100°C and 150°C with the 2/2/2 substrate design, as compared to the 3/2/3 substrate design at common temperatures.

It is believed that this variation in warpage, specifically with the 2/2/2 build-

up stacks, creates the tensile stress in the solder joint to fracture the IMC during BLR temperature cycling. For example, shadow moiré 2D plots show an inversion in package shape upon heating and cooling at 25°C (**Figure 10**). Because the region between lid seal and underfill fillet (reference **Figure 1**) is not supported, this area of the substrate can be readily deflected. With the 2/2/2 build-up stack having two fewer layers, thereby inherently more flexible than its 3/2/3 build-up counterpart, wider warpage variation manifests between the two packages. Shadow moiré data also confirms the expected trend of higher warpage upon cooling, where CTE mismatch drives out-of-plane deformations of package bending and twisting.

This trend of higher warpage will be even more exacerbated at the low-end BLR temperature cycle of -40°C. The various package conformations formed upon cooling are anticipated to lead to the unnatural IMC failure during BLR testing. To accentuate the point of warpage variation playing a role in the unnatural IMC failure between the two substrate designs, stress modeling illustrates slightly higher warpage at the low end of the BLR temperature cycle. This is simulated from 125°C to -40°C with the 2/2/2 build-up stack as compared to the 3/2/3 build-up stack (**Figure 11**).

Summary

Reducing substrate layer count can provide a double bonus of improved electrical performance and lower cost. However, before adopting this approach to kill two birds with one stone, stress modeling and package warpage characterization should be carried out as a precursor to empirical evaluation to predict any reliability performance impact. In this study, both reduced reliability margin and multiple



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Dispenser

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Semiconductor Packaging

- Medical Imaging
- Multichip Modules
- 3D / 2.5D Packaging
- Wafer Scale Packaging
- RF / Microwave Modules

Photonic Packaging

- Optical Engines
- LED Assemblies
- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

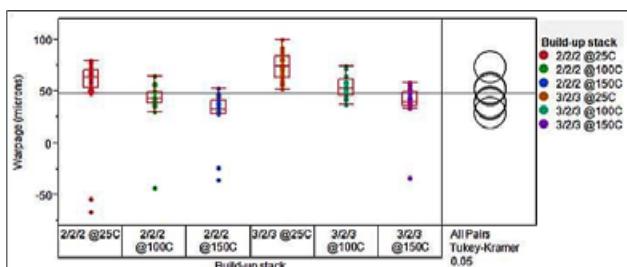


Figure 9: JMP statistical analysis of warpage over temperature for a 2/2/2 and a 3/2/3 build-stack.

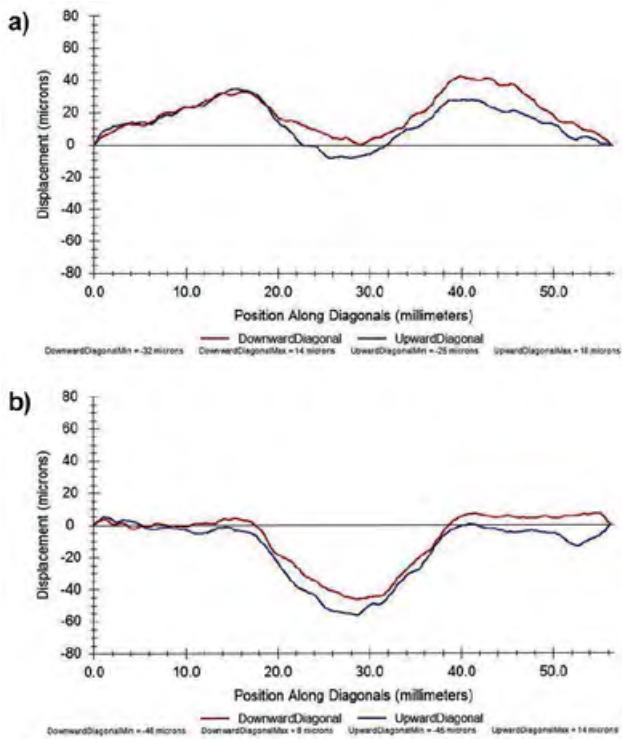


Figure 10: Shadow moiré 2D plots on heating a) and cooling at 25°C b).

fail modes were observed in the 2/2/2 build-up substrate design. In particular, an atypical failure mode of brittle IMC failure manifested itself at the package corner in addition to the typical bulk solder joint fatigue generated by shear stress during BLR temperature cycling.

solving approach [5] that synergistically uses stress modeling, empirical studies, and sound failure analysis tactics, one enables the investigative pieces to come together to combat the warpage challenge. This fundamental approach can open the doors for cost reduction

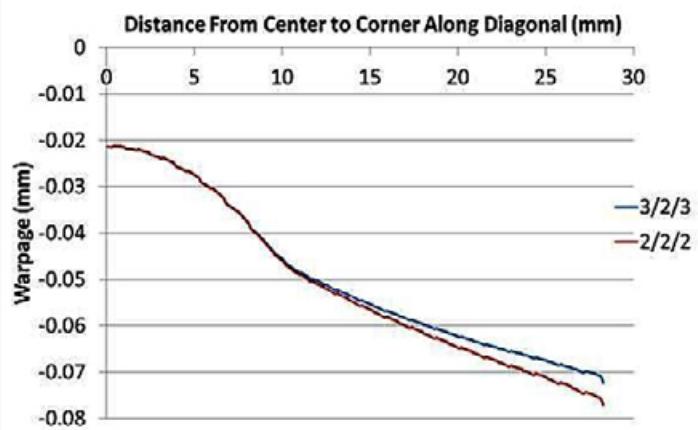


Figure 11: Warpage comparison of 2/2/2 and 3/2/3 build-stacks from package center to corner.

Shadow moiré analysis illustrated multiple package conformations due to bend and twist contortions upon cooling — making brittle interfaces like IMC layers susceptible to failure in a temperature cycling environment. Understanding the temperature-dependent impact on package shape as it factors into this unnatural IMC failure mode starts and ends with deliberate failure analysis to elucidate the failure mode, which led to warpage characterization. Conquering the inherent warpage challenge is easier said than done, as evidenced by the litany of technical articles and papers published on its contribution to package reliability and performance. Nonetheless, by establishing a grassroots problem

and improvement of the bottom-line for more efficient original equipment manufacturer (OEM) devices.

Acknowledgment

The author would like to acknowledge Guangxu Li for stress modeling support.

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Biography

Jaimal Williamson received a BS in Chemistry from Grambling State U. and an MS in Polymers from the Georgia Institute of Technology. He is a Packaging Engineer and Member Group Technical Staff within Texas Instruments' Worldwide Semiconductor Packaging group; email jaimal@ti.com

Advanced eutectic packaging for volume manufacturing of photonics, microwave and RF electronics

By Daniel F. Crowley, Yi Qian /MRSI Systems

Increasing demand for data and bandwidth requires high-volume manufacturing of photonics and RF electronics at a level we have never seen before. This accelerates the continuing adaptation of full automation and the improvement of processes in advanced eutectic packaging for volume production as well as advanced product designs. This article presents the most recent advances in the areas of automation and the eutectic processes particularly for the challenges facing photonics and RF electronic components and microwave modules. These advances result in high-precision, high-throughput, improved yield, and new products for the component and module manufacturers.

There is an interesting metaphor between the telecommunication industry and America's railroad system. By way of reference, in 1850 there were 9,021 miles of tracks, and by 1916, that figure had escalated to 397,014 miles. During the first wave of backbone railroad development between big cities, there were not enough goods and people that were carried by railroad. The railroads overbuilt the system and then paused to wait for demand to catch up. Then gradually, along the railroad routes, new train stations were built, and new shops were opened. They built more short distance routes to reach small towns, villages and farms. Finally, commerce expanded beyond the railroad system's capacity, forcing another cycle of build-up to start. History has shown that driving forces emerge over time producing continual cycles of change.

In recent years, the telecommunication industry has entered its own cycle of change with a rapid expansion phase driven by various macro technology and economic factors. We all remember the last cycle ended with the dot-com bubble bursting around 2000. Although it should be noted, this last cycle did create a great legacy, with a major deployment of long haul infrastructure during that period of time. This has set up a great foundation for the current expansion of metro and access networks to access individual consumers and enterprises worldwide. This

expansion with double-digit growth rates is driven by data consumption from web- and mobile-based applications.

Cloud computing is transforming traditional business models as the multi-nationals from IBM to Cisco grapple with new business models that rely on mobile-based devices and the internet. Increasing mobile data streaming through wireless and cloud-based computing and storage through hyperscale data centers result in demands for increasing capacity, particularly in data communication areas, including wireless and data center infrastructures. In return, the data bandwidth demand from individual consumers and enterprise creates the need to upgrade long haul networks, data centers and metropolitan communication systems. Just a few data points worth noting include IDC's forecast of data growth, which predicts the industry is on track to hit a data size of 35 zettabytes, or 44 times 2009 numbers. Some analysts claim data traffic on mobile devices is growing at 61% annually. Right now, we are in a cycle with a relatively healthy balance between the pull of consumer demand and the push of infrastructure construction.

Photonics and RF electronics have always been on the frontier of network infrastructure expansion. Recently, the transition to 10Gps to 40Gps and then 100Gps/200Gps/400Gps optical network systems enabled an array of new generations of photonic components such as laser chip-on-submount (COS), micro-iTLAs, 100G/200G/400G modulators, intradyne coherent receiver (ICR), 100G CFP2-ACO, and QSFP28+ transceivers. Wireless base station build-out needs critical components, such as RF power amplifiers, made with GaAs or GaN. Most of these products have multiple dies bonded on a common platform or base plate inside a metallic package.

Typical bonding processes include both eutectic and epoxy materials. Eutectic bonding is one area of particular interest to photonics, microwave and RF electronics due to the need for a clean, highly thermally efficient process and for long-term reliability.

This article, therefore, specifically focuses on the challenges and automation solutions related to eutectic processing.

Challenges in volume manufacturing

The forecasted volumes for the new generation of photonics and RF electronic components are unprecedented. This demand level increases the pressure for lower cost manufacturing. However, with the trend of increasing labor costs in popular manufacturing bases, such as in China, it becomes necessary to use a much higher level of automation in the industry. In addition, the higher precision equipment required for advanced packaging with higher density, demands automation because manual and semi-automatic processes are much less effective both from a cost and a quality perspective.

Given these demands and this environment, the challenges include: throughput and accuracy, handling delicate materials, the ability to handle a large and diverse component inventory, stability requirements of 24/7 operations, the scalability needs once demand takes off, and finally, the market requirements surrounding traceability of parts. Each of these challenges is described in more detail in the sections below.

Throughput and accuracy. Automation will always deliver higher levels of throughput compared with manual or semi-manual operations, in any sector. Specifically, in the world of die attach, automation can have 3x to 10x of throughput compared to its manual counterpart depending on the exact process. On the other hand, the throughput is only meaningful with achieved accuracy. With the technological advancement of component products and new processes, for example, silicon and InP photonics integrated circuit (PIC), we see the 5 μ m pick and place accuracy ($\pm 3\sigma$, the current main stream) moving to requirements of 3 μ m ($\pm 3\sigma$) accuracy or better, specifically in photonic and imaging applications.

Handling delicate materials. III-V materials such as thin GaAs, InP and GaN

dies require delicate handling. The crystal facets on edge-emitting laser diodes, the top emitting surface of vertical-cavity surface-emitting lasers (VCSELs), and other active areas must not be touched by the bonding tools because the devices can be damaged. It is even more critical when flip-chip bonding is required. Because all GaN RF transistor die are typically very thin and have a large aspect ratio, the force and pressure control is crucial in picking and placing the die. It is very useful to have a real-time, closed-loop feedback in the force and height control when long-term reliability is an issue.

Managing multiple parts with various sizes. Optical and RF applications frequently require handling a large range of devices from small to large, as well as odd shaped. Many of the devices used in packages are small, including laser diodes and monitoring diodes. Thin metal preforms must be oriented and delicately handled. These preforms are tedious to manually handle. Increasingly, extreme aspect ratio devices are used for arrays. These devices can have an aspect ratio as extreme as 15:1. The housings may also be odd shaped, with small housings of large packages with protruding connectors and pins. Flexibility is key for an automatic machine to be able to perform a variety of die attach processes on one platform. The ability to handle a large number of component types from 150 micron diodes to large odd-shaped lids and attach them eutectically, with epoxy or with thermocompression, is a tremendous advantage over manual or semi-automatic assembly.

Stability. Volume manufacturing often requires 24/7 operations or overnight operation with minimal operators. The automatic equipment stability becomes critical in order to avoid or minimize errors and thus loss of materials and productivity. The system stability can be tested through rigorous steps, but more importantly, the platform needs to be proven in the field. A reliable automation supplier with competent local technical services and expertise in photonics, microwave and RF applications is key for success.

Scalability. In today's dynamic market, it's not just about being first to market but it's also about having the capability to scale quickly and safely when higher volume is demanded. How quickly can your manufacturing partner scale production? Increasingly, product cycles are measured in months rather than years.

Markets change quickly demanding that all vendors in the supply chain react quickly. It is important to have a product and a process that is scalable, because it often makes a difference between the vendors who dominate and those who do not. Short product cycles mean frequently changing production lines. Manufacturing systems need to be suited for dedicated high-volume manufacturing, yet flexible enough to allow small lot production and changeover between designs.

Traceability. Traceability is required for device tuning and component selection at integration. For these reasons, it is important to track individual die lot and serial number information with the serial number of the device being built. Manual record keeping of this pedigree information can be time-consuming, tedious, and vulnerable to human error. Automation equipment must continually compile information and export to log files for later inspection. This should enable all relevant information to be delivered with the completed product.

Fully automatic eutectic bonding

While the volume manufacturing of photonics, microwave and RF electronic components present some unique requirements and challenges, there are attractive solutions, which involve cost-effective automation to reduce manufacturing costs and increase capacity. The rest of the article will review how the eutectic process and characteristics can solve these problems.

Solder reflow eutectic bonding. Eutectic bonding is the process of using a solder alloy as a third material to form a continuous bond between two components. In the case of optoelectronics, this often means two gold-plated materials being joined by lead-tin, gold-tin, or gold-germanium solder. To achieve this bond, typically, a solder preform is placed on one component - usually a carrier or submount - and then the second component, often a microwave monolithic integrated circuit (MMIC), photodetector or laser chip, is placed on the preform. The temperature of the assembly is brought up to just above the melting point of the solder either by heating the base on which the assembly rests, or by flowing heated gas over the assembly. Just as the solder liquifies, the chip is placed with controlled force. The part is cooled to below the reflow temperature and the eutectic

bond is complete (**Figure 1**). Depending upon the device type and construction, scrubbing may be used during the placement process.

The scrubbing step consists of applying a vertical force to the chip while also

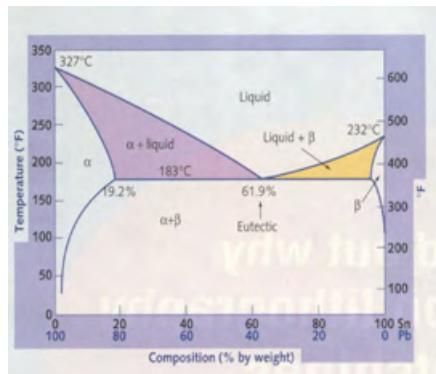


Figure 1: Eutectic transitions for a given metal composition—in this case, tin-lead.

applying a lateral force. The chip is usually moved three to five mils in the negative, and then in the positive x or y direction for several cycles, and then possibly in the alternate direction as well. Rotational scrubs are sometimes employed. Scrub parameters consist of amplitude, speed, and frequency in the x, y, and theta directions. Parameters are determined by process requirements such as the surface area of the chip or the mass of the carrier and process constraints such as proximity to adjacent die. Scrubbing is done as a component of the process of forming a common material (bond) among the three materials. Forcing out air reduces voiding. Also, the solder is better distributed across the die, and the pressure assists the diffusion process.

During the time that the part is subjected to heat, it is important to control the atmosphere. Eutectic bonding is usually performed in an inert environment to prevent oxidation of the bonding surfaces (**Figure 2**). A 90-95% nitrogen-hydrogen mix can be used so that

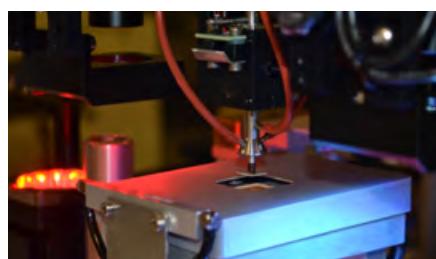
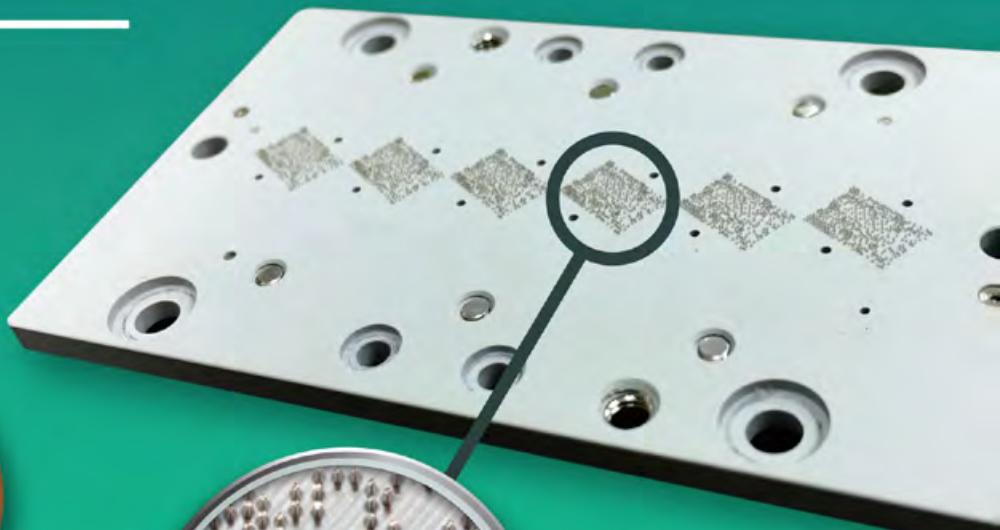


Figure 2: A pulse-heated, fast-ramp eutectic stage.

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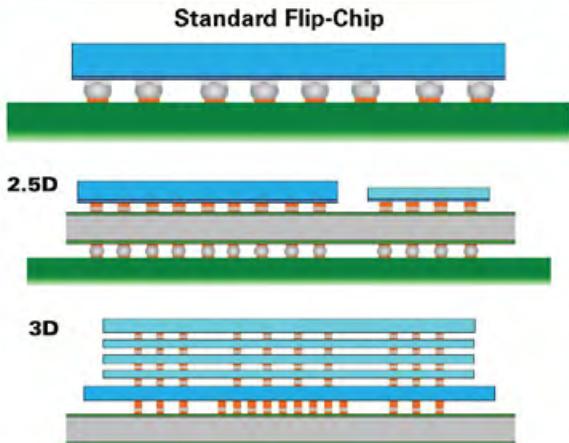
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hydrogen is present for use in the formation of the bond.

From the perspective of the equipment manufacturer, control of the eutectic process involves several key elements and processes. These include the ability to accurately control the temperature of the device, to accurately control contact forces, to introduce a scrub to break through the oxides, to introduce energy to spike the temperature and to mix the various metals contained in the solder, to provide an inert atmosphere with cover gas or a fluxing agent with cover gas, and to control cooling and collets.

Thin GaAs and InP die require delicate handling. The crystal facets on edge-emitting diodes, as well as the surface of the emitting implant on vertical-cavity diodes and other active areas, must not be touched by the bonding tools because the devices can be damaged. **Table 1** illustrates the sort of delicacy required.

Multiple die eutectic bonding. Some advanced photonics devices require multiple dies, bonded on a sub-mount or carrier—all by eutectic bonding for a range of purposes, such as high thermal conductivity, high reliability, and special hybrid integration. A more complicated tunable laser chip on a carrier may include other additional components such as capacitance for bandwidth optimization. Sometimes other mechanical components for fiber alignment may also need to be bonded through eutectic bonding on the same carrier where the laser sits.

In order to achieve the bonding of multiple parts within a package, a temperature hierarchy is frequently required. To achieve this temperature hierarchy, fast ramping heated workstations are used. There are many reasons for a temperature hierarchy. For example, a monitoring diode may need to be eutectically bonded to a spacer at one temperature (for example, gold-germanium at temp Y) and the subassembly (monitoring diode and spacer) may then need to be bonded to a substrate using a lower temperature solder (for example, gold-tin at temp X). The substrate may then need to be mounted to a package utilizing a lower reflowing solder (e.g., lead-tin at temp Z) (**Table 2**). This fast ramping is achieved by utilizing a low-mass hot plate.

In-line eutectic processing. In-line eutectic provides a means to achieve high production volume. By utilizing a progressive hot plate system that indexes through heat zones, eutectic die attach is performed on the same “boat” or carrier that transports parts through the conveyer line that loads and unloads automatically.

Strict temperature control is achieved by indexing parts through pre-heat, assembly, and post-heat zones. Temperature profiling of each heat zone enables fast processing of high-mass parts. High throughput is achieved by limiting the temperature ramping time at the bond station. All temperature zones are under a cover gas of

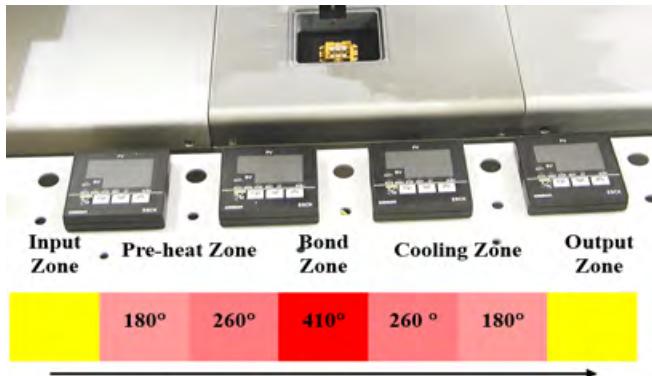
Force
□ 15-20g for .020 square die
□ 40g for .050 square die
□ 80g for .070 square die
Scrub
□ Typically .003 to .008 inches in X, Y, or both directions
□ Usually 3 to 5 cycles

Table 1: Handling requirements for thin GaAs and InP die.

Solder Alloy Melting Points

• Pb38 -- Sn62	183° C
• Au80 -- Sn20	280° C
• Au88 -- Ge12	356° C
• Au97 -- Si03	363° C
• Au06 -- Pb94	304° C
• Au82 -- In18	451° C

Table 2: Different metal compositions have specific reflow profiles.



Heated Boat Indexer

Figure 3: In-line eutectic die bonding.

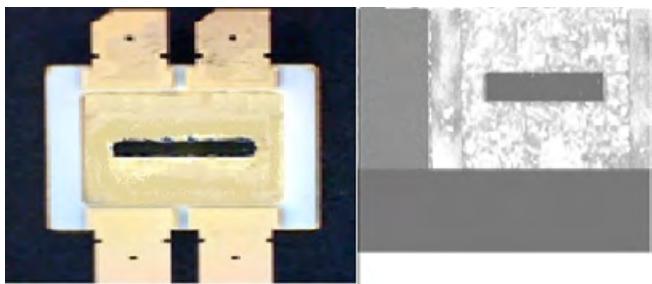


Figure 4: Eutectic package (left) with Sonoscan inspection results (right).



Figure 5: Programmable lighting intensity and color.

nitrogen and hydrogen mix to prevent oxidation of the heated parts (**Figure 3**).

For gold-silicon eutectic, the vision system aligns the package and then picks and places the die, using a scrub action (variable amplitude and frequency) to accomplish the eutectic bonding. A heated cover gas of hydrogen and nitrogen is present over the bonding area. For solder reflow eutectic bonding, such as gold-tin (Au/Sn) attach of gallium arsenide (GaAs) and gallium nitride (GaN) die, the system aligns the package and picks and places a preform onto the heated package (if required, the preform can be pre-deposited) (**Figure 4**). The die is then picked and placed, while the temperature at the bonding position is ramped using a pulse heated eutectic stage and scrubbed (variable amplitude and frequency) to accomplish

the eutectic reflow. The boat is indexed to the next substrate position and the above process is repeated until all the boat positions have been bonded. As the indexer transfers the boat, the parts are incrementally cooled by passing over a cool down zone. When completed, the indexing conveyor transfers the boat to the output magazine loader. Finally, there is a capability that sits above any die eutectic bonding process: an advanced vision system, which is discussed below.

Advanced vision systems. Machine vision is critical for accurate placement. Having a proven ultra-accurate machine platform that is mechanically and thermally stable, with no cantilevered parts, is a baseline to achieve accurate device placement. In addition, the accurate alignment of device fiducials is required to achieve micron-level accuracies.

Many other key features

are required for accurate final placement. Local and global vision alignment is used for nested substrates and feature alignment. The software must allow the user to align die relative to substrate fiducials, die edges, or features of previously placed die. The alignment of the laser chip to a photo diode or a lens to a VCSEL are common photonics examples. Another example is the alignment of a critical die, such as with MMICs and beam lead diodes. This capability ensures repeatability and precise alignment of optical and microwave devices.

Multi-colored lighting is required to successfully vision process a wide range of materials. Tricolor (i.e., red, green and blue) programmable lighting provides the capability for processing challenging alignment surfaces, such as gold traces on alumina (**Figure 5**). Lighting intensity must be programmable and include both

ring and collimated lights for a complete lighting solution. It also must be possible to individually program optimal light settings for each die and substrate fiducial alignment.

Advanced vision must rapidly perform robust substrate fiducial alignment regardless of material contrast and detect and orient die over a full 360°. Both pattern recognition and boundary trace tools provide a complete solution to locate the die center, edges, or application-critical features. This enables fast, error-free processing of complex assemblies.

The optics and camera system must include multiple magnifications for both upward and downward facing cameras. Machine vision is used for alignment of component bottom features and flip-chips. An upward facing camera captures the image of the die feature on the vacuum collet prior to placement. The integrated vision aligns features on the bottom of the device prior to placement. Software, hardware, lighting and optics are integral. One example is the manufacturing of a photodetector. The downward facing camera first aligns a feature on the substrate package. The upward facing camera then aligns the lens on the bottom of the die, and the system places and bonds the device.

Summary

This article discusses the recent trends in the demand of the communication market, the needs of photonics, microwave and RF electronic devices and processes, and the technology advances of automation in eutectic die bonding. The recent proliferation of mobile-based applications and cloud-based computing and storage, drives higher demand in bandwidth, making photonics and RF electronic devices among the most critical components for communication infrastructure expansion. The high-volume production and more advanced products require high speed, high precision and reliable automatic die bonding solutions for a successful manufacturing environment. The integral parts of these solutions are equipment performance, dedicated software applications, advanced vision systems, process understanding, and technical support services.

Biographies

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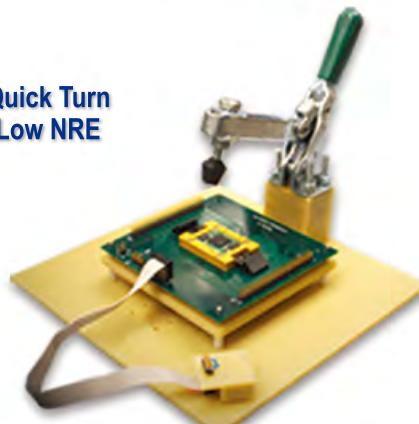
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Meeting solder paste printing challenges for SiP in “smart” IoT devices

By SzePei Lim, Kenneth Thum, Andy Mackie [Indium Corporation]

System-in-package (SiP) is an increasingly important package type that comprises a variety of assembly materials and processes that minimizes volume, without sacrificing computational intensity. This market is mostly being driven by mobile Internet of Things (IoT) devices, such as smartphones and smartwatches. Materials deposition techniques, especially solder paste printing, are also changing to match this need.

The development of ultra-fine solder powders and solder pastes began in the late 90s, as the standard flip-chip assembly process of wafer/under bump metallization (UBM) solder bump, onto solder-on-pad (SOP) on the substrate became strongly established. The size and nature of the die-side flip-chip solder bump has also evolved, as illustrated in **Figure 1**.

Major changes in flip-chip solder deposition processes have taken place over the last 10 years, and are outlined in **Table 1**. The extensibility of solder paste usage for very fine-pitch solder bumps

was originally believed to be pushing the need for even finer solder powder types such as type 8, and even a putative type 9—powder size distributions that are not even defined by IPC standards to this day ([2] and **Table 2**). The extensibility was curtailed quite rapidly as fundamental limits of printability and reflow (especially voiding) made other solder bumping processes, especially plating, more favored.

Solder paste and SiP

Semiconductor assembly and packaging in SiP are driving the use of embedded devices, wafer-level chip-scale packaging (CSP), and similar space-saving techniques [3], while passive devices are also getting smaller and smaller. The adoption of 0201, 01005, and now even 008004 components (to be used in high-volume manufacturing (HVM) production in 2017) is underway, and these devices are, or are becoming, the norm in high-volume consumer “smart” IoT devices.

Challenges

Shrinking the final package size places constraints on the assembly materials and processes, some of which will necessitate major changes, as will be discussed in this section.

Solder powder. As devices shrink, the size of the solder powder deposit must also shrink. A large deposit of solder paste can effectively be considered a continuum. However, as the deposit

Type	% by weight / volume				
	Less than 0.5%	<=10% between	>=80% between	<=10 less than	
5	40	25	40	15	25
6	25	15	25	5	15
7	15	11	15	2	11

Units: microns

Table 2: J-STD-005A definition of particle size distribution by particle diameter.

volume decreases, the finite size of the solder powder starts to become a problem, causing increases in the variability in the deposit size. The result of a simple analysis [4] using an allowable variability of $\pm n$ solder powder particles per deposit is shown in **Table 3**. This demonstrates, for example, that for a 100 micron diameter bump with an allowable height variability of $\pm 1.0\%$, a type 7 solder powder must be used (if the bump-to-bump variability is due to the number of particles per deposit varying by ± 5 or more particles (print-to-print variation)).

Cleaning: no-clean versus water-soluble fluxes. It is no surprise that as devices get smaller and the footprint efficiency (total device area/package area) increases toward its 1.0 maximum (absent 3D packaging, of course), that cleaning is becoming more of a challenge. As we have shown previously, similar device and feature shrinkage is driving flip-chip assembly from water-soluble fluxes to ultra-low residue no-clean fluxes [5]. A similar technology change will occur with system-in-package (SiP), where both shrinkage and the increasing closeness of other components are already making cleaning a major challenge.

Paste rheology and printing. The rheology of the solder paste is critical; not only must the paste print consistently over a long stencil life, it must also print without slumping. This means that it must have a low shear yield stress of a few N/m², which is still low enough

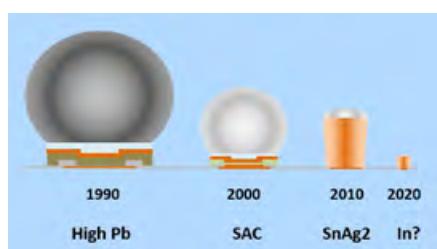


Figure 1: Flip-chip solder bump evolution.

Pitch:	185	165	150	130	100	80
Die	Bump (Paste)	Bump (Paste)	Bump (Plated)	Bump (Plated)		
				Microbump (Plated)	Microbump (Plated)	Microbump (Plated)
Substrate	SOP (Paste)	SOP (Paste)	SOP (Sphere)	SOP (Sphere)	Cu-OSP	Cu-OSP

At 130 microns, ODM may stay with organic substrate and standard solder bump, while an OSAT may move to copper pillar and interposer

Table 1: Flip-chip solder roadmap [1].

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		Equivalent diameter (d) of solder particles (microns)									
		n=									
Variability (+/- x microns)	Variability as % of Mean Diameter	1	2	3	4	5	6	7	8	9	10
0.5	0.50%	24.62	19.54	17.07	15.51	14.40	13.55	12.87	12.31	11.84	11.43
1.0	1.00%	30.97	24.58	21.47	19.51	18.11	17.04	16.19	15.48	14.89	14.37
2.5	2.50%	41.82	33.19	29.00	26.35	24.46	23.01	21.86	20.91	20.11	19.41
5.0	5.00%	52.25	41.47	36.23	32.91	30.55	28.75	27.31	26.12	25.12	24.25
10.0	10.00%	64.71	51.36	44.87	40.77	37.84	35.61	33.83	32.36	31.11	30.04

ICA Particle Type	Typical Max Diameter
Type 3	45micron
Type 4	38micron
Type 5	25micron
Type 6	20micron
Type 7	15micron
Type 8	10micron

Table 3: Solder powder size effect on deposit size variance.

to allow the paste to roll. It is also low enough to allow the paste to release from small apertures. A long stencil life necessarily reduces print-to-print variability over time, and also maximizes the usage of the paste.

Solder paste testing. A detailed printing test was carried out to study the printing performance of different solder pastes. A test vehicle consisting of different pad sizes, and different gaps between two neighboring pads, was specifically designed for the printing test, which will be described in the next section.

Experimental

Four different solder pastes were used for the printing tests. The water-soluble solder paste is halogen-free, and the no-clean solder paste is ultra-low residue, having been specifically developed for tight-clearance SiP applications (Table 4).

The test vehicle is 237mm in length, 62mm in width and 0.5mm thick. The land

patterns are grouped into five columns with gaps of varying sizes between pads, and three rows of different pad sizes. Each board has an array of two of these. The patterns are arranged in 0- and 90-degree orientation to simulate different directions of squeegee passes (Figure 2).

The test vehicle consists of three 008004 pads and one 01005 pad. In this study, however, we focused on the 008004 pads as shown below:

- 125µm x 150µm
- 100µm x 150µm
- 112.5µm x 150µm
- The gaps between pads are 50µm, 80µm, 100µm, 130µm and 150µm

The pad metallization was a standard NiAu (ENIG). The stencil used was 50µm thick, laser-cut with a final electro-polish. The stencil aperture was designed to be 1:1 to the size of pad to be printed. The aspect ratios (AR) for the various stencil openings are shown in Table 5 where a DEK Horizon printer was used to deposit the paste, and a Koh Young SPI was used to measure print volume.

Results and discussion

Gap size effects. Note that bridging is observed for all the pastes with 50µm gaps between pads, hence the results for 50µm gaps are omitted in this paper. However, even with the non-optimized printer setup condition, there is no problem printing all the pastes at gaps of 80µm and more. Future studies will focus on improving the printer clamping system and developing a support system for thin substrates and E-fab stencils, to achieve better printing performance for 50µm gaps.

Table 4: Solder paste types.

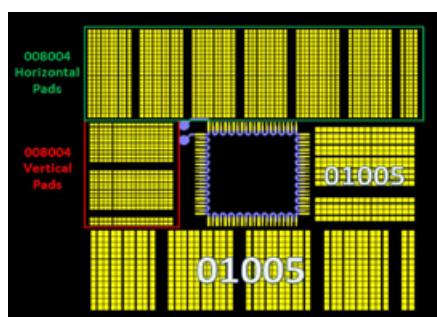


Figure 2: Outline of the print test vehicle.

Stencil Opening	Aspect Ratio
125 x 150µm	0.68
100 x 150µm	0.6
112.5 x 150µm	0.64

Table 5: Stencil openings and aspect ratios evaluated.

All paste print behavior is similar; a wider gap results in increased solder paste volume. The box plot in Figure 4 shows the volume vs. gap distance for paste D. This may be due to a stiffer stencil with a wider gap, therefore causing better solder paste release.

Solder pastes: As shown in the box plot (Figure 3), pastes A and D perform better than pastes B and C, with reduced minima and higher volumes. We observed more paste insufficiencies with lower aspect ratio apertures.

Metal loading: In order to further study how the viscosity and rheology of a particular paste affect fine-feature print performance, a solder paste sample with 0.5% less metal loading than that used for

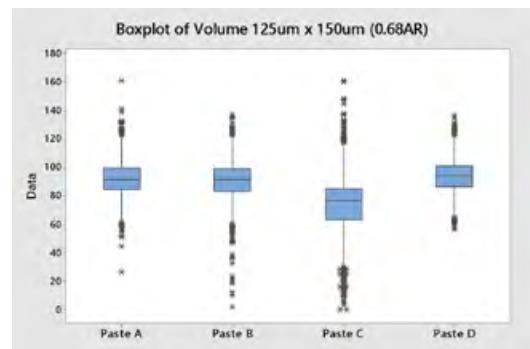


Figure 3: Paste comparison on 0.68AR pads (as example of data).

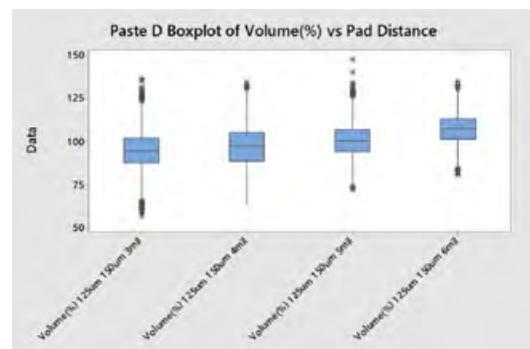


Figure 4: Example of paste D volume compared to different pad distances.

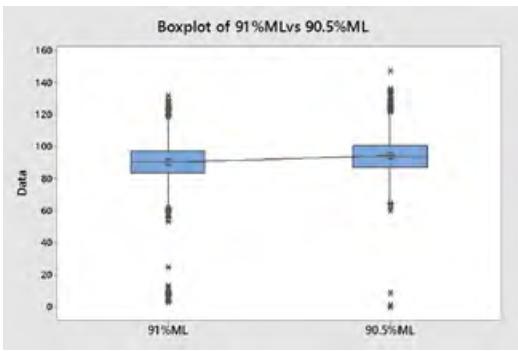


Figure 5: Comparison between different metal loading of paste D.

Pad Dimension	Aspect Ratio	Cpk	Ppk
125µm x 150µm	0.68	3.70	1.64
112.5µm x 150µm	0.64	3.51	1.78
100µm x 150µm	0.60	3.30	1.72

Table 6: Cpk of different pads using paste D.

paste D was prepared and printed. The results are shown in **Figure 5**. We observed that this apparently trivial reduction in metal load caused the average solder paste volume to increase. A two-sample T test was performed to investigate whether the results were statistically significant. A significance level of $\alpha=0.05$ and a P-value of 0 indicates that this was the case for 90.5% (much better), and 91% metal loading was statistically different, showing that 90.5% does perform significantly better than the 91% metal load.

Print consistency: We also performed print process capability (print volume consistency) using Paste D with 90.5% metal loading, and the Cpk for various pad sizes are shown in **Table 6**. This further confirms that Paste D with 90.5% metal is capable of reliably and reproducibly printing 008004 components.

Reflow testing: Reducing voiding in the final solder joint is an important consideration for mechanical reliability. Extensive studies were carried out to show that choosing the correct reflow profile could easily minimize voiding, and a more complete overview of these results can be found at [6].

Future technology drivers

The future trend of discrete passive devices for IoT is uncertain. Some ceramic capacitor manufacturers, for example,

have chosen not to develop 008004 and lower technology, resulting in a shrinking supplier base. At some point in the next five years, embedded passive devices will become favored, and at that point the need for increasingly finer solder paste for SiP will disappear. For the near term, this is clearly a trend, and many OSATs and contract manufacturers are investing in resources to make sure they are ready to deploy fine feature printing in the range of 100-120µm stencil opening for HVM.

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Silicon 3D integration for small power devices

By Jean Charbonnier, Myriam Assous, Jean Philippe Bally, Aurélia Plihon [Univ. Grenoble Alpes – Leti, an institute of CEA Tech, MINATEC Campus], Christian Hartler, Joerg Siegert, Franz Schrank [ams AG], Klaus Pressel, Hermann Gruber [Infineon Technologies AG]

Miniaturization and functional density are increasingly required for electronic power systems. 3D technologies [1-3] provide an interesting response to this demand if adapted to power specifications. In the framework of the ENIAC JU funded project for the Enhanced Power Pilot Line (EPPL), a new type of device has been proposed based on a silicon interposer for power devices. This paper presents a power system prototype in which Infineon power chips are assembled on an ams/Leti through-silicon via-last (TSV-last) passive silicon interposer. The full conception to meet power specifications of 10A and 600W is reported from the interposer design strategy to the integration process flow and mounting operations in a 200mm fabrication line. In this paper, we present electrical and morphological characterizations of the silicon interposer.

Design

The aim of this work is the investigation of a power device architecture concept for applications in the high-current range of 10A where the electrical resistance between power chips must be as low as possible. Furthermore, the distance between the driver and the four power devices has to be reduced to reach the highest switching frequency possible. Therefore, a global architecture of assembly is proposed. A schematic of the different layers is shown in **Figure 1**.

This architecture has been determined by the following characteristics:

- The current enters to the power chips by 500 μ m diameter solder balls to allow compatibility with existing mounting technology and immediate application.
- A thick copper redistribution layer on interposer back side (BRDL) is used to gather the current from the solder balls.

- A TSV matrix with thick copper deposition is used to route the current to the interposer front side.
- In order to implement the CMOS and silicon interposer co-integration, three aluminum lines connected by arrays of W vias have been inserted in the path of the current.
- A second thick copper level is used for gathering the current from several TSVs and, finally, a matrix of copper pillars (105 μ m diameter) brings the current to the silicon power device, flip chipped onto the interposer.
- Copper pillars and a thick copper redistribution layer (FRDL) on the front side of the interposer carry the current to the next power device, without going through the aluminum lines.

Silicon interposer process

The manufacturing of the Si interposer described in this work is based on a TSV-last approach [4]. The wafers are processed in a standard CMOS flow that can be, in principle, from any technology node. The only significant deviation is a slight adjustment of the metal 1 layer that will later serve as the landing layer for the TSVs.

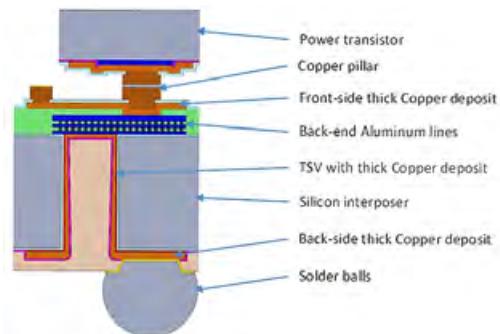


Figure 1: Technology schematic.

Process flow

The silicon interposer process flow is described in **Figure 2**. The front side process and the back side TSV formation until the insulation deposition and spacer etch are performed at ams AG's fab (steps 1-3 in **Figure 2**). The wafers are then sent to Leti for copper TSV and back side redistribution layer (BRDL) metallization, and the under bump metallization (UBM) process (steps 4 and 5 in **Figure 2**). To complete the silicon interposer process on the front side, the wafers are flipped and re-bonded on a temporary carrier, which allows processing the copper-pillar interconnection (steps 6-8 in **Figure 2**). The final mounting (**Figure 3**) will consist of stacking the Infineon power device on the silicon interposer.

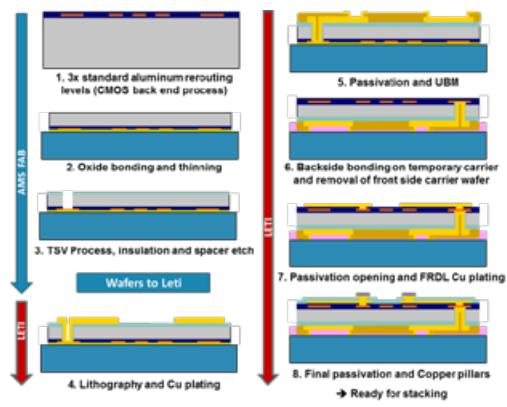


Figure 2: Silicon interposer process flow overview.

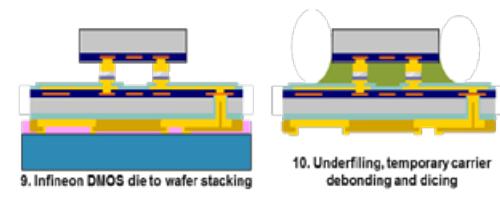


Figure 3: Mounting process.

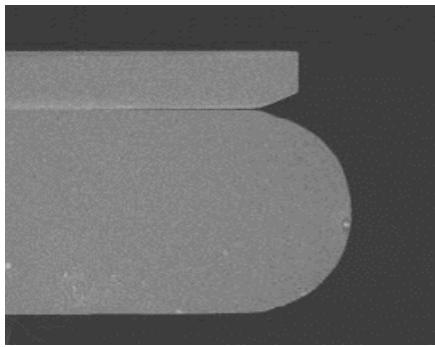


Figure 4: SEM image of a cross section of a bonded wafer pair after edge trimming and thinning.

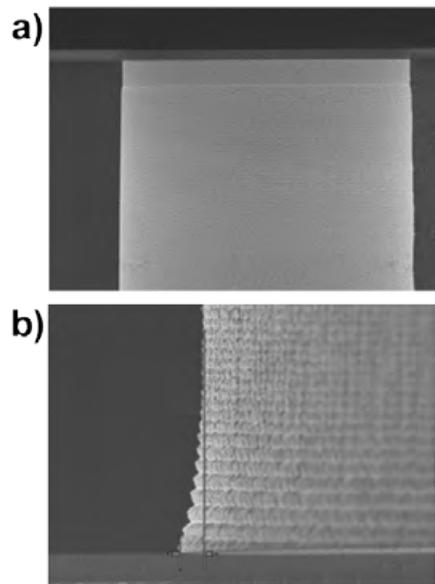


Figure 5: SEM image of a TSV after DRIE: a) top and b) bottom

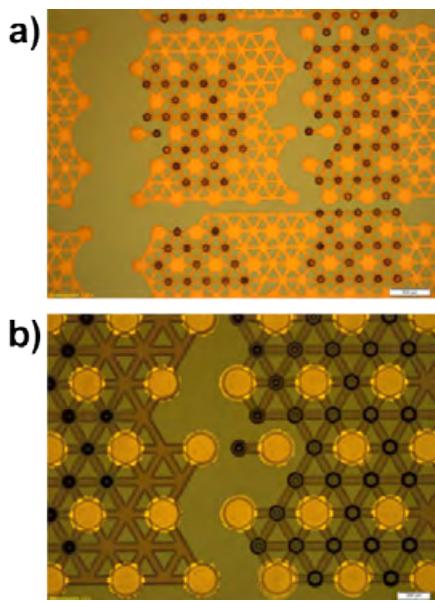


Figure 6: a) Back side processing TSV and BRDL metallization, and b) passivation and UBM.

After the CMOS flow is completed, the wafers have to be mounted onto a handling wafer to process the back side. This step protects the front side during the subsequent TSV process and also allows the handling of otherwise very thin wafers on standard equipment.

The wafer bonding technology of choice has to be compatible with the thermal budget in the TSV flow, which is relatively high (deposition temperature of insulation SiO_2 at 400°C). This rules out conventional temporary bonding owing to the limitations of organic materials. Instead, the CMOS wafer surface is planarized and made suitable for direct bonding, in which a rigid connection between the CMOS surface (composed of SiO_2) and a Si handling wafer is formed.

Once the wafers are bonded, the CMOS wafer is trimmed in size so that its edge is always within the boundary given by the handling wafer and thinned to $200\mu\text{m}$. Thereby, the thin device wafer is protected from damage that would be caused by handling. **Figure 4** shows a cross section of such a bonded wafer pair after edge trimming and thinning. Wafer thinning is followed by deposition of a SiO_2 backside insulation layer and lithography to define TSV locations. Using an automated IR-aligner, a front-to-backside alignment accuracy of better than $4\mu\text{m}$ can be achieved, which is sufficient for the $80\mu\text{m}$ large TSV structures.

Following the above steps, TSV formation can start. After an oxide etch to remove the backside isolation locally and expose the Si substrate, deep holes with an aspect ratio of 2.5:1 are created by means of deep-reactive ion etching (DRIE) using the Bosch process. It is important to minimize the roughness on the TSV sidewall because considerable challenges exist for residue removal and deposition of subsequent layers. A certain topography is inherent to the Bosch process (scallops) and undercut due to the stop on the inter-level dielectric (ILD) of the CMOS (notching). Great care was taken to optimize the performance of the TSV etching process, resulting in smooth structures with a minimum amount of notching (**Figure 5**).

The electrical insulation of the Si substrate is achieved by SiO_2 deposition. A stack of different oxides (including both plasma enhanced [PECVD]

and sub-atmospheric chemical vapor deposition [SACVD] processes) is needed to provide sufficient sidewall coverage, insulation and mechanical performance (stress, adhesion, etc.).

Finally, the SiO_2 is removed from the bottom of the TSV exposing metal 1 from the CMOS and leaving an insulation spacer on the TSV sidewalls. This maskless process creates a lot of polymers. The complete removal of residual polymers is crucial in order to avoid the delamination of subsequently deposited metal layers.

After the spacer etch process is finished at ams, the process flow continues at Leti (**Figure 2**, steps 4-8) starting with TSV metallization. Here, a dedicated copper-plating recipe is applied to the wafers. This recipe has been optimized to reach top-to-bottom copper deposition conformality greater than 80% for the aspect ratio 2.5:1 TSV of $200\mu\text{m}$ depth and $80\mu\text{m}$ diameter. Both TSV and BRDL plating (**Figure 6a**, and **Figure 9**) are achieved in a single step. The minimum space and line dimensions of the BRDL level are both equal to $20\mu\text{m}$.

Several process splits have been carried out to evaluate the impact of different copper thicknesses on the resistance of TSVs and the front side BRDL. The copper line thickness on

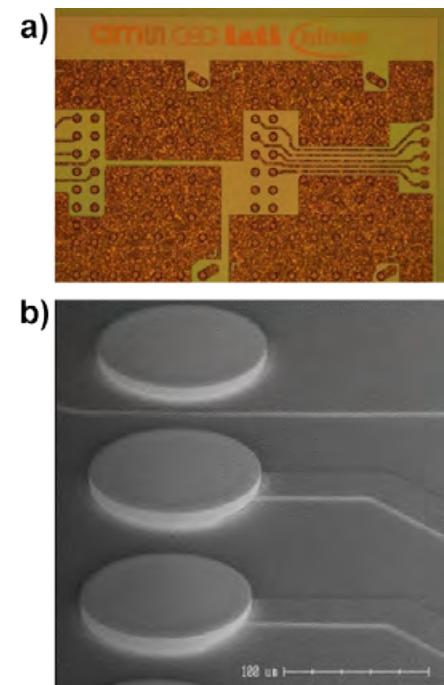


Figure 7: a) Front side processing FRDL, passivation and copper pillars optical view, and b) SEM observation.

the wafer surface ranges from $2.5\mu\text{m}$ to $5.5\mu\text{m}$. The copper is then passivated with an organic material and the UBM is formed (**Figure 6b**). The UBM contains a nickel layer of $1\mu\text{m}$ thickness in the metallic stack to satisfy the specifications of mounting operations on the board.

Once the interposer back-side processing is complete, it is bonded on a temporary carrier, while the original carrier is removed on the front side. This so-called flip-flop process allows reprocessing the wafer's front side. After passivation opening, a $3\mu\text{m}$ -thick copper FRDL is processed to redistribute and spread the electrical signal coming from TSVs and aluminum lines underneath (**Figure 7a**). The design rules are more aggressive at the FRDL level than at the BRDL. The minimum line and space FRDL dimensions are both equal to $5\mu\text{m}$.

After FRDL passivation, $105\mu\text{m}$ diameter copper pillars are formed [3]. They are composed of a copper/nickel/gold metallic stack (**Figure 7b**). The silicon interposer is then ready for the mounting operation. These pillars will receive the power device copper bumps during the stacking to electrically connect both parts of the system. In this approach, the wafers are still bonded on their temporary carrier (**Figures 2** and **3**), which therefore means there are no special requirements needed for handling.

Mounting process

Standard mounting processes have been applied to the prototype, including stacking, reflow and underfilling still bonded on the temporary carrier. The $200\mu\text{m}$ thin power device dies are stacked on the silicon interposer (**Figure 8**) using a die-to-wafer process with collective reflow.

The distance between each power device on a single silicon interposer is $150\mu\text{m}$ in the x direction, and $60\mu\text{m}$ in the y direction. The standoff between power dies and the interposer ranges from $40\mu\text{m}$ to $60\mu\text{m}$ depending on the copper bumps process splits. This wafer-level process approach reduces significantly the process costs compared to the chip-level standard process. It furthermore allows a subsequent power die's front-side grinding, which could be an advantage for cooling efficiency. To complete the fabrication, the wafers are then debonded from their temporary carriers,

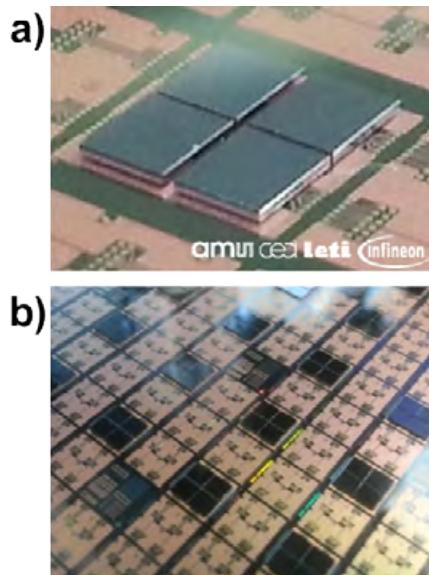


Figure 8: a) Infineon power-device chips stacked on an ams/Leti Si interposer after reflow and b) after underfilling.

mounted on tape, and diced.

Morphological characterization

Figure 9 and **Figure 10** introduce a global cross section of the silicon interposer before mounting and a zoom on the TSV top corner, respectively.

The top copper pillar lands on the FRDL, which is in contact with the three Al lines. Those lines are in contact with copper at the TSV bottom and they reroute the signal to the back side of the interposer. It is easily possible to confirm the continuity and conformality of the copper liner inside the TSV. On **Figure 10**, the interface between the TSV copper liner and the first aluminum line is clear of any residue and perfectly flat. The morphological quality of the contact is mandatory to ensure a low TSV Kelvin resistance. Moreover, the overall structure reveals no major defects or delamination.

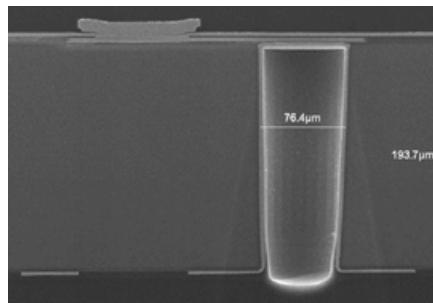


Figure 9: Technology global cross section of the ams/Leti mixed process: copper pillar, front-side rerouting (FRDL) and three Al lines, TSV and BRDL.

Electrical characterization

By performing two different Kelvin-type TSV measurements (**Figure 11**), it is possible to determine the effective thickness of the metallization inside the TSV. **Figure 11a** shows the necessary rerouting scheme to obtain the contact resistance, whereas the measured resistance in **Figure 11b** consists of the contact resistance, the TSV, Al lines and Cu BRDL. Both RDL parts have a width of $80\mu\text{m}$. The length of the Al lines is $15\mu\text{m}$, and the Cu BRDL is $25\mu\text{m}$

The measured contact resistances for different deposition thicknesses are shown in **Figure 12**. The median values are 2.1 , 2.5 , and $3.1\text{m}\Omega$, respectively, with a maximum standard deviation of $0.2\text{m}\Omega$ and a minimum yield of 98% (criteria: 10% deviation of the median).

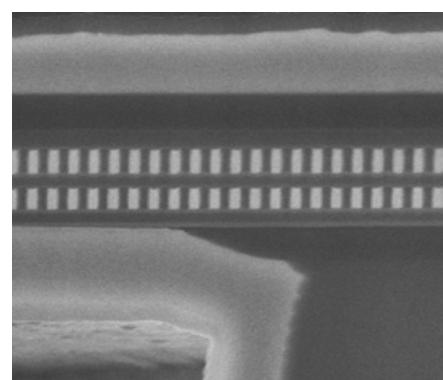


Figure 10: Zoom on TSV top corner: electrical contact between copper TSV and Al lines.

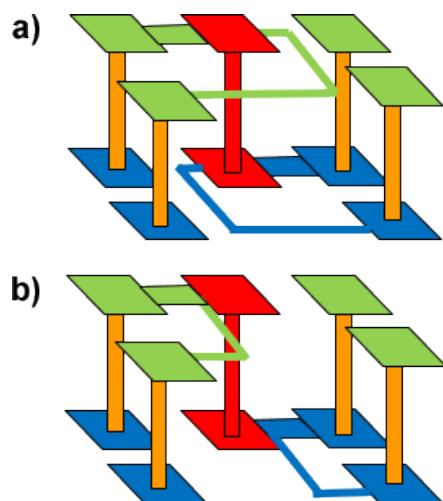


Figure 11: Kelvin-type TSV test structures used for electrical characterization: a) Contact resistance, and b) overall resistance of the TSV, including the contact resistance and the RDL on the front and back side. The red-marked areas are the measured TSV structures.

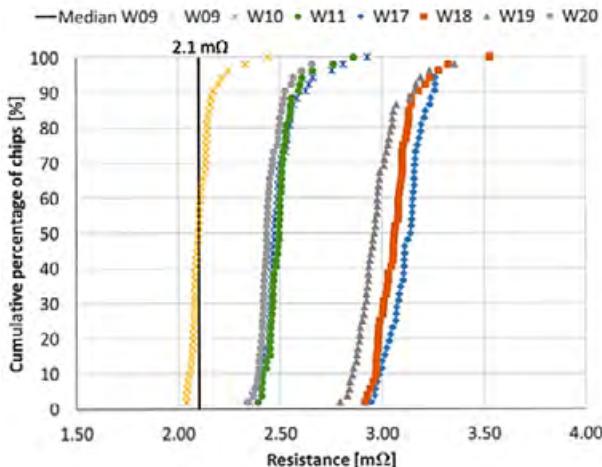


Figure 12: Cumulative percentage graph of the contact resistance for three different copper deposition thicknesses.

The total resistance measurements results using the test structure (**Figure 11b**) show median values of 14, 16 and 18mΩ for each TSV split, respectively, with a maximum standard deviation of 1mΩ. Extracted isolated TSV resistances without contact resistance are 3.3, 4.3 and 5.6mΩ, respectively, to the median values. These values are lower than previously reported for the same type of annular TSVs in the range of tens of mΩ [5–7]. From this data, copper wall thicknesses of each split have been calculated leading to 4.7, 3.6, and 2.7μm, respectively. These values are in agreement with SEM cross sections and surface profilometer measurements, which confirms the conformality of the copper liner inside the TSV.

Summary

A new complete 3D-integrated power system has been proposed, designed and processed through the collaboration of Infineon, ams and Leti. Dedicated process modules, design and design rules have been developed and applied for this power application in the range of kilowatts, including thick copper rerouting, 3mΩ low resistance TSVs, and optimized interconnection arrays. All the preliminary functional tests done on the prototypes fulfill the specifications. The results confirm the path for a new type of 3D applications in the field of small power devices. A final device should also include the CMOS driver in a single module for higher density, lower consumption and

faster switching rate. Reliability studies, temperature behavior testing and modeling are underway. Moreover, ongoing prototype operating evaluation will be the topic of a future paper.

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The challenges of MEMS packaging in the IoT era

By David Mount [ULVAC Technologies, Inc.]

Over the past 25, or so years, there has been much written regarding the challenges in the packaging of MEMS, but very little information regarding “how-to” has wound up in the public domain. MEMS packaging technology has always been regarded as highly proprietary and costly, imparting as much as 75% of the cost of the entire MEMS device. MEMS device packaging challenges are about to become even more complex in the rapidly emerging Internet of Things (IoT) era because the billions of sensors (MEMS devices) projected will need to have selling prices of under 10 cents, for the most part. Furthermore, to achieve these pricing targets, alternative substrates, other than silicon, will have to be used (glass, flexible plastics), and manufacturing technology will likely change, with cost efficient roll-to-roll processing playing a greater role. However, the MEMS device still has to interact with the environment, whether it’s a pressure sensor, or MEMS microphone, etc. This article will serve to elaborate on the significant challenges that lie ahead for MEMS device packaging in the IoT era and provide some details as to how this may be accomplished.

devices or smart objects. The examples range from billions of devices to one trillion+ connected devices. It has been posited that these connected devices will be MEMS-type sensors and actuators. It should be pointed out that “revenue” projections for the IoT are very aggressive, with some estimates put at as much as \$4T, by 2020. The bulk of this revenue will come from software and data storage, i.e., Big Data. The revenue generated from MEMS-type sensors and actuators manufacturing will be much more modest, as indicated by the forecast noted in **Figure 3**.

Looking at the revenue market forecast for the MEMS market, there is certainly good growth indicated (**Figure 3**), but it is not anywhere near the growth projected for the units market forecast. It begs the question, if device volume is going up, where’s the revenue? The simple answer is that the average selling prices of the devices is expected

to fall, as the manufacturing volume of the MEMS-based sensors and actuators ramps at a high rate. **Figure 4** depicts this type of trend very well. As the reader will note, we are in the area of sensor pricing falling way below \$1.00, with other analysts predicting pricing of some sensors to be below 10 cents. John Greenough, of *Business Insider*, predicts that the IoT is on track to be an absolutely huge market, with a massive \$1.7T of value to be added to the economy in the form of revenues and efficiency cost savings by 2019; but the

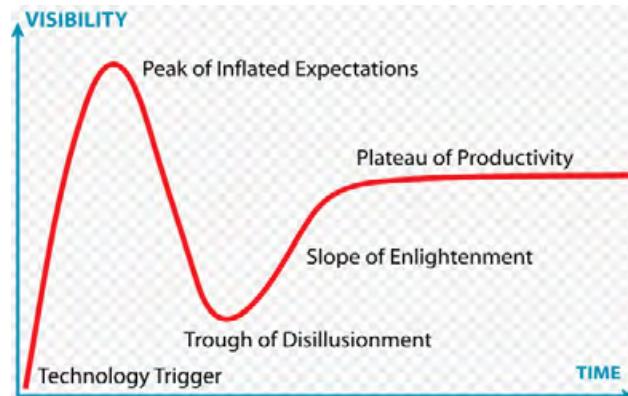


Figure 1: Hype cycle. SOURCE: Gartner

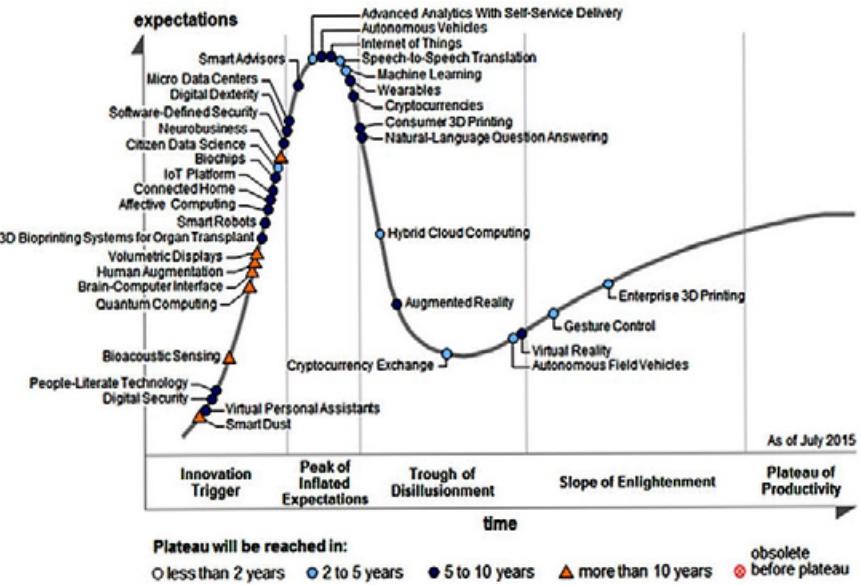


Figure 2: Hype cycle for emerging technologies, 2015. SOURCE: Gartner

cost of internet-connected sensors is coming down. *Business Intelligence* states that: Many IoT devices rely on multiple sensors to monitor the environment around them. The cost of these sensors has declined 50% in the past decade, according to Goldman Sachs. *Business Insider* expects prices to continue dropping at a steady rate, leading to an even more cost-effective sensor.

This kind of cost reduction will not come about by continuing to work with silicon-based MEMS sensors and actuators. There will be a transition from rigid semiconductors made with silicon and other hard materials to flexible circuits on polymeric materials. These flexible circuits will be fabricated on substrates of PET, or other polymers, and even paper. The predicted sensor cost reductions will come as a result of manufacturing sensors and actuators that are either printed, or vacuum-deposited on flexible “plastic” substrates. For printed sensors, manufacturing would be on printing-press equipment (screen printers, inkjet, or rotogravure systems). Batch process sensors would be manufactured on vacuum roll-coating systems, using large rolls of substrate materials similar to those materials used in printing. In the case of printed or flexible electronics, the areas covered would be enormous, with substrate feed rolls being up to 2-meters wide and up to hundreds of meters long. It is not very likely that all manufacturing in the MEMS industry will transition to some flexible or printed processes where the sensor form factor is simple, but this just may be the case for simple internet-connected environmental or medical sensors. Flexible sensors are already beginning to ramp in volume, but there will always be a requirement for silicon-based MEMS sensors and actuators.

ID TechEx forecasts the market for products fabricated on flexible substrates to grow from \$6.4B last year to \$14.9B in 2025. As stated on April 7, 2016, in *Semiconductor Engineering* [16]: “Currently on the market, the most common flexible sensors are based on a set of electrodes. For example, there are capacitive touch sensors that can be layered on any surface or biopotential that measure your heartbeat in a smart garment,” noted Guillaume Chasin, an analyst and consultant with ID TechEx Research.

With regard to the IoT applications of smart objects, it is not just all about the sensors. Sensors need to communicate to, and/or, through other smart devices, such as smartphones and tablets, etc., which requires MEMS devices that are being packaged with other types of ICs. The packaging of individual MEMS die is still very proprietary, but the wafer-level packaging of sensors

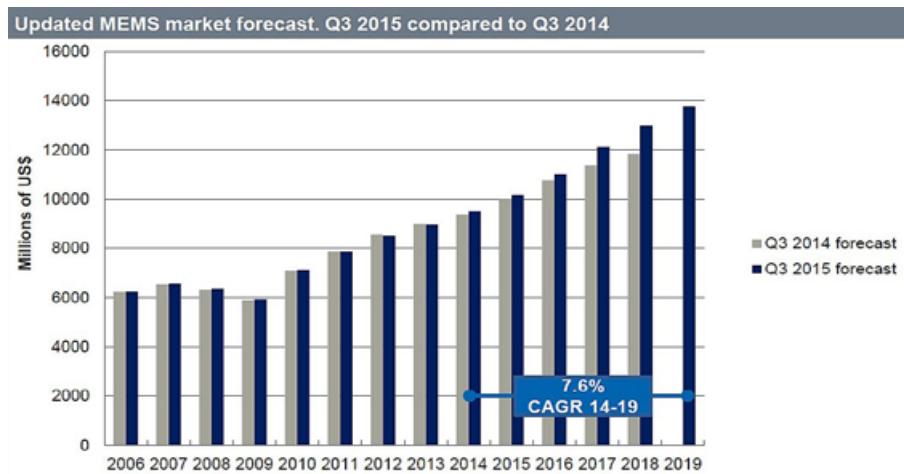


Figure 3: Revised MEMS market forecast. SOURCE: IHS - MEMS Market Tracker - Q3 2015 and Q3 2014

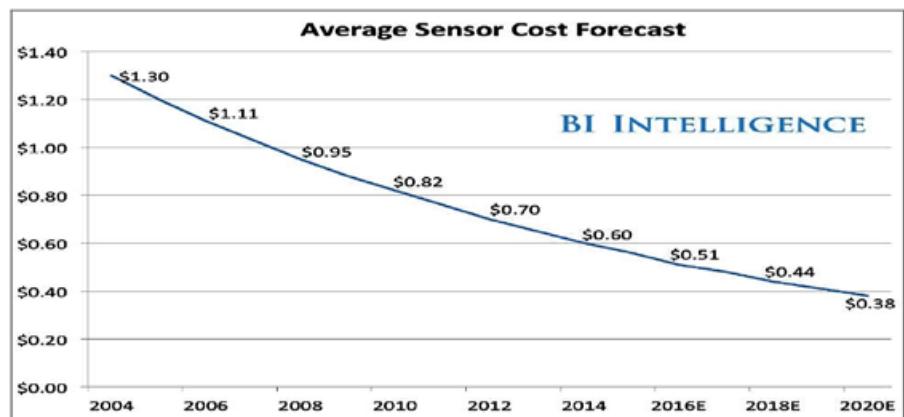


Figure 4: Average sensor cost forecast. SOURCE: Goldman Sachs, BI Intelligence

and other MEMS devices that form “intelligent systems” is of increasingly more importance. Pursuant to this article there is an abundance of wafer-level packaging (WLP) information available in the literature. The packaging process for

silicon-based MEMS sensors and devices that has gained the most traction and is the most prevalent form of packing is known as fan-out wafer-level packaging (FOWLP). FOWLP has been identified as a promising packaging technology suitable to better serve the needs of both mobile/wireless, and the upcoming IoT markets compared to other packaging technologies, such as organic laminated substrate-based flip-chip ball grid array (FCBGA) and lead frame-based quad no-lead package (QFN). Fan-out wafer-level packaging represents a sort of compromise between die-level packaging and wafer-level packaging. The semiconductor (MEMS)

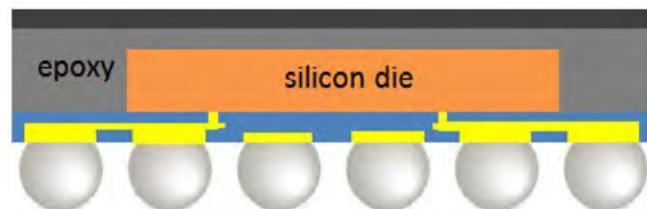


Figure 5: Fan-out wafer-level package, an introduction, simplest construct.
Source: SPTS

wafer is diced and the singulated ICs are embedded in a new “artificial” wafer. On embedding, enough space has to be ensured between the individual dice to allow for the fan-out redistribution layer (RDL). **Figure 5**, illustrates this very clearly. A unique feature to FOWLP is that more than one die can be integrated in a single WLP by stacking. FOWLP technology is an enhancement of the standard WLPs developed to provide a solution for semiconductor devices requiring a higher integration level and a greater number of external contacts. It provides a smaller package footprint and a higher input/output (I/O) along with improved thermal and electrical performance.

In conventional WLP schemes, I/O terminals are located over the chip surface's area. Using this method, there is a limit to the number of I/O connections. Fan-out WLP takes individual die and embeds them in a low cost material, such as epoxy mold compound, with space allocated for each die for additional I/O connection points—avoiding the use of relatively expensive silicon real estate to accommodate a high I/O count. This involves embedding known good die (KGD) into mold compound, then building up interconnect layers from die to BGA balls on the mold compound, or substrate. Redistribution layers (RDL) are formed using physical vapor deposition (PVD) seed deposition and subsequent electroplating/patterning to re-route I/O connections on the die to the mold compound regions in the periphery. FOWLP also allows for panel-sized packages to be used as systems scale in size.

As stated in the previous paragraph, FOWLP allows for chip stacking. In **Figure 6**, a very good example of a FOWLP multi-sensor stack is shown. A recent Yole Développement graphic depicts the extent to which FOWLP packaging schemes are being used for mobile devices (**Figure 7**).

For silicon-based systems, FOWLP is not without its challenges. The first immediate challenge is that the molding compound used in the redistribution layer (RDL) outgases substantially. Degassing can create a substantial bottleneck for several of the process sequence steps noted below. For scaling up to panel-scale sizes, there are several different process sequences that may be used. Dr. Beth Keser of Qualcomm Technologies, Inc., identified a couple of these sequences during her talk at The International Wafer Level Packaging Conference (IWLPC) 2015 (San Jose, CA; Oct. 15, 2015). Dr. Keser described a sequence used by J-Devices of Japan (J-Devices PLP Process Flow), where the package was formed on a metal panel. This involved a complex process sequence as follows:

1. Die attach to metal panel plate
 2. Resin lamination*
 3. Via formation*
 4. Seed layer formation (copper)*
 5. Photo-resist coating for copper wiring*
 6. Exposure and development*
 7. Copper plating*
 8. Resist removal*
 9. Seed layer etching*
 10. Solder resist formation
 11. Solder ball mounting
 12. Singulation
- *repeated for each layer

FOWLP Multi-Sensor Stack

- Manufacturing of functional demonstrators
- FOWLP Multi-Sensor Stack consisting of
 - Pressure Sensor/ASIC package with thin film RDL and RDL opening above sensor membrane
 - Acceleration sensor/ASIC package with PCB based RDL and Through Mold Vias (TMV) for package stacking

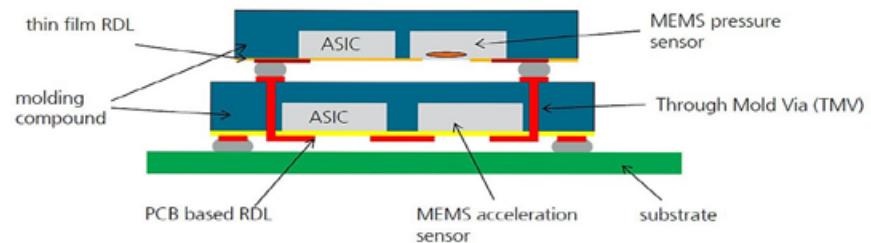


Figure 6: FOWLP multi-sensor stack. SOURCES: Bosch/Fraunhofer IZM (SEMI MEMS Tech SEMINAR; Sept. 26, 2013, Cornaredo, Italy)

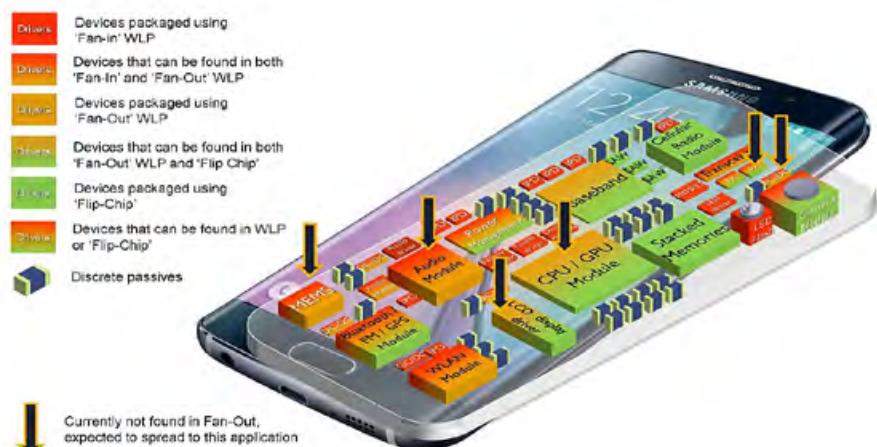


Figure 7: AP platforms in mobile devices: overview per application. SOURCE: Status of the Advanced Packaging Industry Report 2015, Nov. 2015, Yole Développement

Depending on the geometries used and number of layers, this process sequence can be very challenging.

Dr. Keser also described a packaging process sequence used in a dielectric process flow (involving positive material). This sequence is noted below:

1. First polymer coating
2. Pre-bake
3. Exposure
4. Development
5. Cure and plasma clean
6. Seed layer sputtering
7. Photo-resist and Cu plating
8. Photo-resist stripping
9. Second polymer coating
10. Pre-bake
11. Exposure

12. Development
13. Cure and plasma clean
14. Under bump metallization (UBM) and solder ball

This could also be a very challenging process sequence, depending on I/O count, geometries, and number of layers.

The readers will note that there are several energetic and thermal processes associated with each process sequence (etching, sputtering, PR stripping, baking and curing). A lot of which would seemingly be incompatible with flexible substrates of PET, other polymers, or paper.

There is quite a lot of research to be done before flexible sensor packaging can be integrated with fan-out wafer-level packages, now in use for Si-based packages. There are a lot of problems to be solved. It should be

noted that inexpensive flexible sensors will hold a prominent place in the Internet of Things era.

The challenges are many, but there are many good scientists from around the world working on the problems. In the MEMS world there are several industry consortia working together to address common areas of collaboration. Starting with the MEMS & Sensors Industry Group, which has a special cooperative relationship with iNemi, the International Electronics Manufacturing Initiative and has established a Joint SEMI/MEMS Task Force to address standards and road-mapping activities, in active collaboration with SEMI, the Semiconductor Equipment and Materials Initiative. This is in addition to several government organizations, such as NIST, etc. On the printed and flexible electronics side, the development of flexible sensors is coalescing around NextFlex, the Flexible Hybrid Manufacturing Institute. The FlexTech Alliance, an industry organization, last summer received a \$75M grant from the Department of Defense to establish and manage a Manufacturing Innovation Institute (MII) for flexible hybrid electronics. FlexTech has since become a “strategic association” partner with SEMI. It has been discussed within the MEMS/SEMI Task Force, efforts to seek further collaboration with the FlexTech Alliance. The future for MEMS sensors in the IoT era looks very promising.

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Biography

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3D performance and cost advantages enabled by direct bond technology

By Paul M. Enquist *[Invensas]*

3D technology is increasingly used as a solution to improve performance and reduce the cost of a wide variety of functions required in semiconductor products. These can range from cost-sensitive, power and form-factor limited handheld consumer devices, to high-bandwidth industrial computing. Direct bonding has recently emerged as an enabling technology to achieve improved cost-effective functional density. This article will provide an overview of direct bond technology, benefits that have been realized by early adopters of the technology, and additional applications likely to adopt the technology.

Direct bond technology

Direct bond technology enables the stacking of wafers or die-to-wafer without the use of adhesives, high temperature, pressure, or voltage that may damage the parts being stacked, or be incompatible with the bond environment or post-bond fabrication requirements. Advanced implementations of this technology that enable a strong homogeneous insulating bond at room temperature and a hybrid insulating and conductive bond for scalable in situ 3D interconnect are featured in this article. These bond technologies, known as ZiBond® and DBI®, respectively, have been extensively reviewed [1-3]. Both technologies were invented and developed at Ziptronix, Inc., and are being further developed by Invensas Corp. These are currently available from Tessera Technologies Inc. [4].

Low-temperature homogeneous direct bond technology: ZiBond. This low-temperature direct bond technology is distinguished by being capable of achieving at least about half the strength of silicon by simply aligning and placing suitably prepared die or wafer surfaces together at room temperature. Subsequent annealing of the room temperature bonded surfaces at as low as 150°C can cause the bond strength to exceed the strength of silicon. The surface preparation technique for this technology can include a combination of mechanical and chemical processes. This can be accomplished with industry standard tools and processes and the subsequent wafer or die placement can be done in an atmospheric

manufacturing ambient. For example, the mechanical planarity and root mean square (RMS) surface roughness specifications can be accomplished with industry standard chemical mechanical polishing (CMP) tools, pads, and slurries. The polished surface material can be a wide variety of dielectrics used in semiconductor manufacturing such as silicon oxide, silicon nitride, silicon oxynitride, silicon carbide nitride, and low-k dielectrics. Depending on the thickness and type of material being bonded, it may be necessary to meet SEMI standards for wafer bow and warp. The chemical surface activation can be accomplished with industry standard plasma tools and processes. For example, a low-power nitrogen reactive ion etch, compatible with stringent electrostatic discharge requirements, has been shown to be effective at providing high nitrogen bond interface concentrations and high bond energies at low temperatures. Finally, the alignment and placement requirement can be met with commercial, industry standard tools for die or wafer bonding. The choice of the tool is subject to the alignment accuracy requirement of the application. The ability of this technology to bond directly between CMOS materials without adhesives, high temperature, pressure, or voltage and to leverage industry standard tools and processes for the surface preparation enables a high-throughput, low cost-of-ownership bond technology.

Low-temperature hybrid direct bond technology (DBI). DBI has both insulating and conductive bond portions. The insulating portion consists of the homogeneous direct bond technology described above and the conductive portion can be a metallic bond. A variety of metals have been used for a metallic bond including copper, nickel, and gold. The hybrid nature of this technology enables an electrically isolated in situ 3D interconnect to be made between die or

wafers that are bonded with this technology. The hybrid bond surface can be built with industry standard damascene technology capable of sub-micron metal feature size and pitch and planarized with dielectric. Suitable preparation of this hybrid bond surface can then first result in a strong homogeneous bond between the die and/or wafer insulating surfaces that are simply aligned and placed together at room temperature in an atmospheric semiconducting environment. A subsequent batch thermal anneal without external pressure may be used to facilitate creation of a metallic bond and low resistance electrical connection between bonded die and/or wafers. This can occur when the metallic hybrid bond component expands and is compressed by the strength of the dielectric hybrid bond component without requiring any external pressure as shown in **Figure 1**. This enables a sub-micron 3D interconnect pitch between bonded die or wafers if tools with sufficient sub-micron alignment and placement accuracy are used. The strong dielectric bond upon placement prevents slip during the thermal cycle and is therefore fundamentally capable of finer pitch than copper thermo-compression and other technologies that require temperature and/or pressure to form a bond. These other technologies also require an underfill after metallic bonding, the need for which is eliminated by DBI hybrid bonding.

The surface preparation for this hybrid direct bond technology is similar to that of the low-temperature direct bond technology.

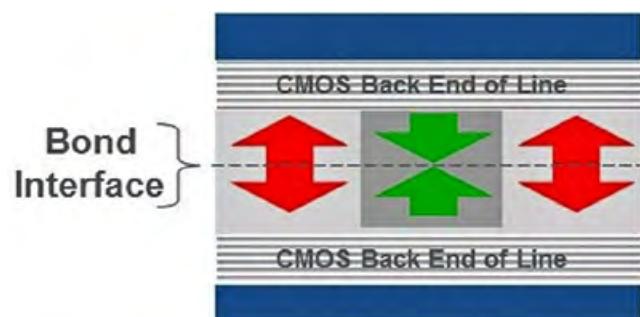


Figure 1: Cross-sectional schematic showing internal compression without external pressure of a metallic DBI hybrid bond portion by a dielectric hybrid bond portion with high strength at low temperature when the metal expansion at elevated temperature is constrained by the dielectric bond portion.



Figure 2: Die-to-wafer bonding: A die pick and place tool picks die from a lower carrier plate and places them on an upper 200mm wafer.

The chemical processing can be the same, but the CMP may have an additional requirement that controls the relative height of the dielectric surface to the conductor's. For example, by recessing the conductor's surface below the dielectric's, a void-free bond interface can be obtained using industry standard tools and processes with standard high-volume manufacturing requirements. The recess specification and thermal cycle required depend on the conductor type and geometry. As with the low-temperature homogeneous direct bond technology, the ability of this technology to bond directly between CMOS materials without adhesives, high temperature, pressure, or voltage, and to leverage industry standard tools and processes for the critical surface preparation enables a low cost-of-ownership for this technology.

Wafer-to-wafer integration. A straightforward implementation of these direct bond technologies is wafer-to-wafer (W2W) bonding where wafers of comparable size and shape are aligned and placed together. These wafers can be CMOS device wafers and/or substrates made of silicon, other semiconductor, or non-semiconductor materials. Practically, any wafer type and size is possible as long as the surface preparation specifications described above are implemented. The W2W format can be implemented in a variety of supply chain configurations including wafer foundry, wafer-level packaging or outsourced semiconductor and test (OSAT) supplier. For example, an integrated device manufacturer (IDM) adopter may prefer implementation within the wafer foundry on account of

the synergy of the bond technology with wafer fabrication, while a merchant adopter may prefer implementation in a wafer-level packaging facility because of cost and allocation considerations.

Die-to-wafer (or die) integration. These bond technologies can also be implemented in a die-to-wafer (D2W) or die-to-die (D2D) format where wafers are singulated into die prior to alignment and placement. The mechanical surface preparation component is preferably implemented at wafer-scale prior

to singulation, while the chemical surface processing component may be implemented before or after singulation, subject to the type of singulation used and the die handling prior to alignment and placement. A natural implementation of the D2W and D2D formats could be in an OSAT because of the existing singulation and die handling infrastructure. Proper die cleaning and handling are typically required to realize void-free bonds with singulated die. An example of D2W bonding is shown in **Figure 2**.

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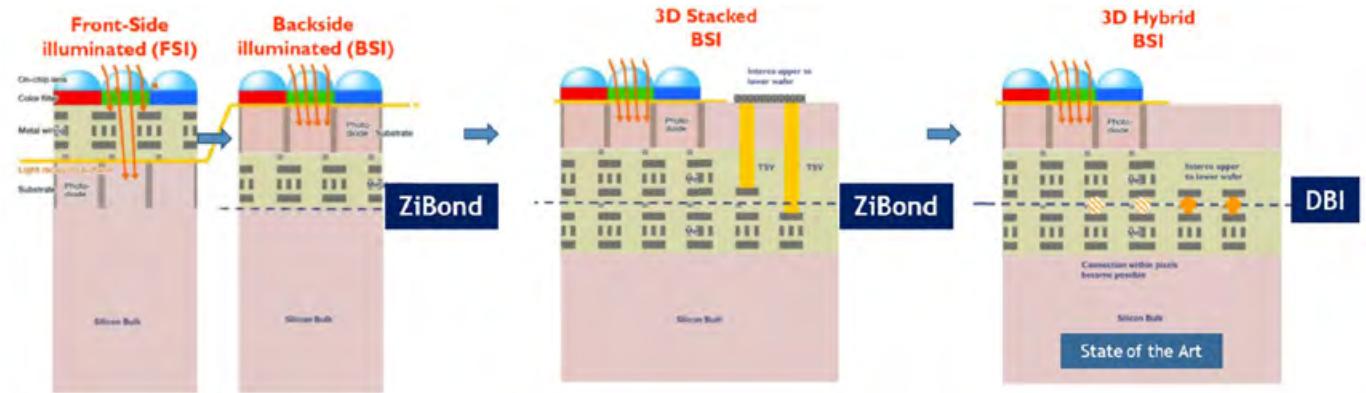


Figure 3: Evolution of CMOS image sensors: a) Frontside illuminated; b) Backside illuminated; c) Stacked BSI with TSV; and d) Stacked DBI BSI without TSVs. SOURCE: Yole

Early adopter application: CMOS image sensors

CMOS image sensors (CIS) have experienced substantial growth over the last 20 years because of the ability of their fabrication technology to scale rapidly. Although much of this growth has come from traditional node scaling, pixel performance has required the implementation of a new volume manufacturable fabrication technology to support further pixel scaling. These requirements have been uniquely met with homogeneous and hybrid direct bond technologies, as shown in **Figure 3**. These technologies have enabled multiple generations of bonded 3D image sensor manufacturing and lucrative commercial success for its adopters. In particular, Sony has become a CIS image sensor leader after licensing ZiBond and DBI technologies and has estimated potentially \$13B of CIS revenue by 2017 [5].

First bonded CIS generation: backside illuminated. The first generation of bonded CIS used low-temperature homogeneous direct bonding to bond the frontside of a CIS wafer to a silicon handle wafer followed by thinning the CIS wafer and backside completion of photodiode fabrication. This enabled backside illuminated (BSI) pixels that improved light absorption and facilitated pixel scaling below $1.75\mu\text{m}$, as shown in **Figure 3b**, compared to the conventional frontside illuminated (FSI) CIS solution shown in **Figure 3a**. The low-temperature direct bond technology enabled the success of this scaling by uniquely providing compatibility with post-bond wafer fabrication requirements, including a high bond strength at low temperature that minimized bond distortion required for scalable backside pixel fabrication. The BSI configuration also benefited from an improved chief ray angle resulting from

illuminating photodiodes closer to the surface instead of buried below multiple layers of metallization, as in the FSI configuration.

Second bonded CIS generation: stacked BSI with through-silicon via interconnect.

The second generation of bonded CIS also used a low temperature, low distortion homogeneous direct bond. However, the frontside of a first CMOS wafer was bonded to the frontside of a second CMOS wafer, resulting in a stacked CMOS configuration. Through-silicon vias (TSVs) outside the pixel array were used to connect the stacked CMOS layers to each other as shown in **Figure 3c**. This stacking of CMOS wafers

enabled a number of improvements that provided a sustainable competitive advantage over the first generation. One advantage was a reduction in die size by about half due to the stacking architecture that allowed the CIS design to be partitioned into pixels on one wafer that could be stacked on logic circuitry in the other wafer. This also reduced fabrication cost by increasing the number of die per wafer. Another advantage was the ability to use different process nodes for the different layers in the stack resulting in a substantial reduction in CMOS cost. Sourcing two different types of wafers also provided supply chain management advantages,

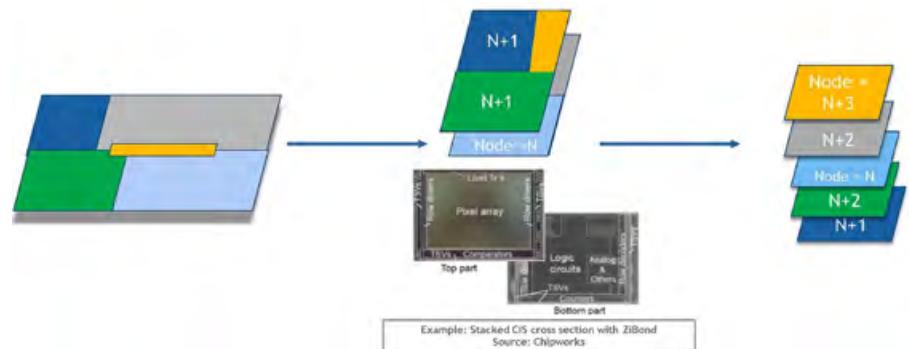


Figure 4: The concept of partitioning an SoC with multiple nodes into two dies with different nodes, as shown in the example, and finally into true 3D SoC partitioning. SOURCE: Chipworks

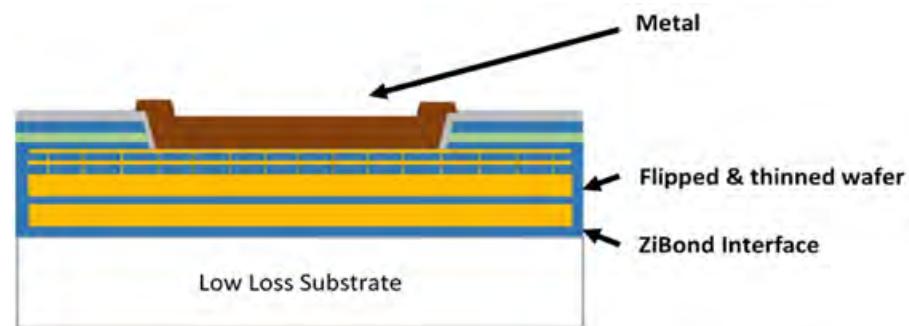


Figure 5: A schematic cross section showing ZiBond layer transfer to a low-loss substrate for an RF application.

for example, different foundries were able to be used for each wafer or one of the wafers could be sourced internally. Another advantage of this stacked architecture was improved thermal performance by removing logic from immediately adjacent to the pixels to underneath the pixels and closer to a heat sink.

Third bonded CIS generation: stacked BSI without TSV interconnect. The third generation of bonded CIS replaced the low-temperature, low-distortion homogeneous direct bond used in the first two generations with a low-temperature, low-distortion hybrid direct bond. This eliminated the requirement of costly TSVs in the second generation to interconnect the stacked CMOS and enabled 3D electrical interconnections interior to the pixel array as shown in **Figure 3d**. In addition to cost reduction, the adoption of the hybrid bond enabled higher performance and new CIS architectures. For example, the hybrid bond 3D interconnect reduced both the electrical parasitics compared to the TSV plus routing parasitics of the second CIS generation, which enabled a higher bandwidth interconnect between stacked layers. Furthermore, sub-micron, scalable, per-pixel connections become available, which can enable architectures like global shutter for scaled pixels with good response and superior parasitic light sensitivity. It is also possible to have architectures with less than one connection per pixel, for example, when implementing full chip pixel dual auto focus [6].

Follow-on applications

While CIS has been a very successful application for direct bonding technology, there are a number of other applications that are benefiting, or are expected to soon benefit, from use of this high-performance, low cost-of-ownership, high-volume manufacturable technology. A few of these are discussed below.

3D system-on-chip. A 3D system-on-chip (SoC) is a partitioning of a conventional SoC into two or more layers and stacking those layers in a 3D configuration. Such partitioning can enable the confinement of the most aggressive and expensive node to one layer, and utilize less expensive older nodes at other levels to enable a power/performance optimized product at lower cost. One example of a 3D SoC is the stacked BSI CIS described above that has benefited greatly from adoption of direct bond technology. Many of the advantages of stacking that have benefited CIS can similarly benefit SoC

applications that are not thermally limited. A generic cross-sectional schematic of a 3D SoC with potential sub-micron 3D hybrid bonding interconnect is shown in **Figure 4**.

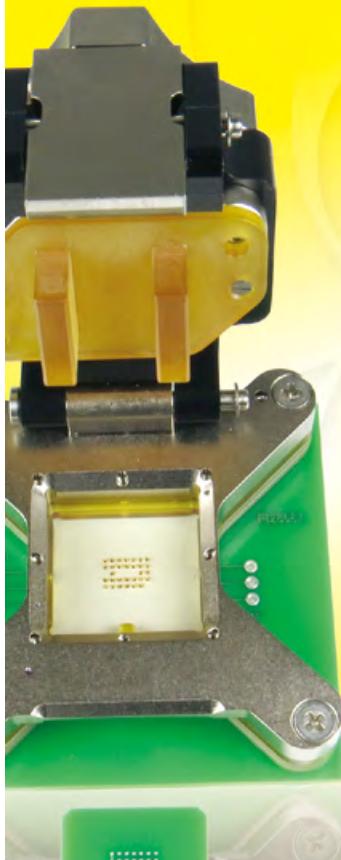
RF front-ends. RF front end components like switches and filters are often made from either silicon with high RF loss, more expensive silicon-on-insulator material with limited node availability, or even more expensive low RF loss materials like GaAs or InP. The direct bond technology can be

used with any process node to replace silicon substrate material with high RF loss with lower RF loss material enabling higher RF performance and lower cost with smaller die. A schematic cross section of this application is shown in **Figure 5**.

3D memory. 3D memory refers to the stacking of memory layers to achieve improved performance such as density and latency that is beyond the capability of conventional scaled 2D memory. The layers

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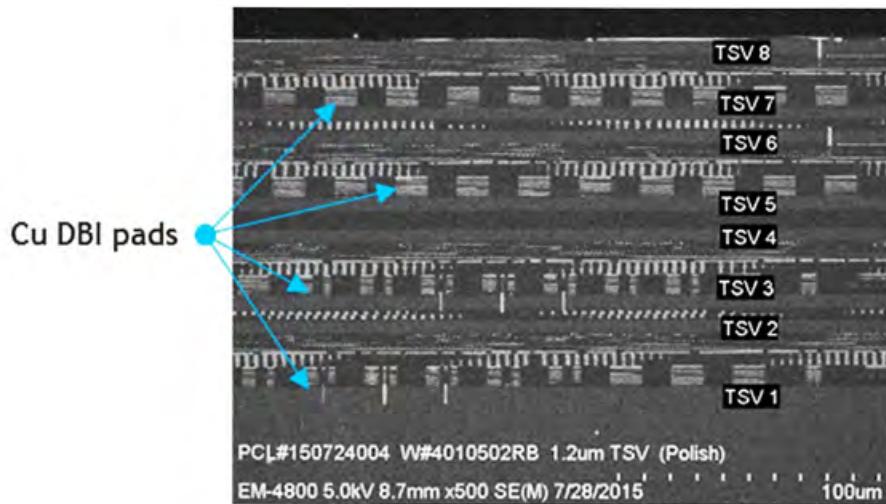


Figure 6: DBI pads connecting 8 layers of CMOS circuitry for advanced logic applications. Courtesy: Tezzaron Semiconductor Corp.

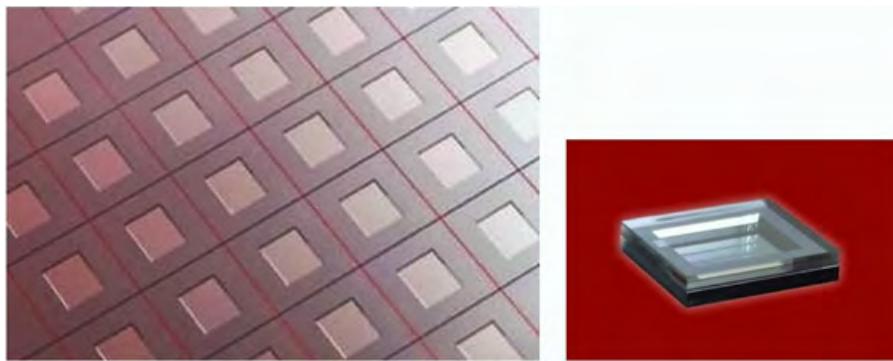


Figure 7: Photograph of a MEMS cavity wafer encapsulated with a glass wafer using ZiBond. Inset of a singulated die shows the ZiBond surface.

in a high-performance 3D memory are typically on top of a logic controller layer, although some lower cost memory solutions stack only memory. 3D memory can be built by stacking either die or wafers. Die stacking, using conventional solder bumps and underfill to build 4-high stack high-bandwidth memory (HBM) or RDIMM modules, is in production by SK Hynix and Samsung, respectively. Development of a W2W 3D memory requires test and repair strategies to circumvent combinatorial yield loss. Stacking of 8 CMOS layers with a $<3\mu\text{m}$ DBI hybrid bond interconnect pitch has been reported demonstrating the process feasibility of W2W DRAM stacking as shown in **Figure 6**. Development of D2W DBI stacking as a lower cost, higher performance alternative to conventional die stacking technologies is underway at Invensas and the results will be reported elsewhere.

MEMS. Direct bonding technology also has considerable potential for a variety of MEMS applications where the encapsulation and packaging can account for a significant

portion of the MEMS cost. Both ZiBond and DBI can potentially provide lower CoO options with comparable or superior hermeticity compared to other bonding technologies. **Figure 7** is an example of ZiBond encapsulation developed for a micro-mirror application.

2.5D/interposer assembly. The final, but by no means the last, application described in this article for direct bond technology is that of 2.5D or interposer assemblies. This application currently uses thermo-compression or solder bumps and underfill for assembly of dies to a typically large interposer that results in assembly yield and thermal performance challenges for high-density solder interconnects. Direct bond technology enables room-temperature assembly with similar material sets on both the die and interposer without underfill, which significantly reduces warpage and improves assembly yields. Also, the reduced stacking interconnect parasitics of hybrid bonding significantly improve the signal-to-noise ratio [7]. The hybrid

bond interconnect scaling advantage has the potential to improve interconnection densities by several orders of magnitude and enable 2.5D/interposer assembly architectures not possible today. The promise of high-yield, flexible architecture design and scalability make this technology attractive for future generations of integrated processing applications.

Summary

Direct bond technology offers a low cost-of-ownership for bonding and has been proven in high-volume manufacturing. It has enabled substantial cost and performance improvements in CIS and RF applications and is expected to further enable cost and performance improvements in other applications including 3D SoC, 3D memory, MEMS, and 2.5D/interposer assembly, among others.

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Biography

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Contact sheet for conductive elastomer contactor applications

By Jiachun Zhou (Frank), Kiley Beard, Kevin Deford [Smiths Connectors, Smith Group]

A conductive elastomer is a special semi-conductive compliant material that has been developed and applied in various industries over the years, such as sealing rings in automobiles. The integrated circuit (IC) chip test industry started to use it in contactors about 20 years ago. With its low profile, conductive elastomer has shown its advantages over other mechanical conductive compliant systems since its introduction, especially in signal integrity (SI) performance. As the speed or frequency of semiconductor IC chips increases, some traditional contactors do not perform to expected levels and greater interest is being generated in conductive elastomer contactors.

There are various types of conductive elastomer contactors in the package test market. These elastomer contactors have a common structure: an elastomer sheet inserted by conductive elements, such as Ni, Ag, or Au particles or Au-plated Cu wire. The thickness of the conductive elastomer at a compressed state is typically <1.5mm, providing an electrical path that is often much shorter than that of other contactors (usually >2mm for spring probes). As a result, the conductive elastomer contactor shows much better SI performance than other contactors. To take advantage of this strength, the initial use of conductive elastomer

in package testing was to place a package directly on an elastomer with direct contact of package balls or pads on the conductive components in the elastomer, as shown in **Figure 1**. This direct contact structure provides reliable contact with very low contact resistances (C_{res}). As a whole, conductive elastomer contactors perform better than most other contactor technologies, such as spring probe contactors. However, the weakness of conductive elastomers appears when they are introduced in automated test equipment (ATE) high-volume testing. The direct contact of the package and the elastomer generates contamination on the surface of the elastomer caused by solder migration from the solder balls.

Efforts have been made to make improvements in the industry. Using a separate contact sheet on the elastomer is one solution. This article introduces the basic structure of contact sheets, and offers a deep discussion on considerations in contact sheet design in order to optimize the performance of conductive elastomer. Cleaning methodologies of the contact sheet will also be discussed.

Contact sheet: structures/design considerations

A typical conductive elastomer with a contact sheet is shown in **Figure 2**. The contact sheet is placed above the

elastomer sheet as an interface between the chip and the elastomer. The major function of this contact sheet is to provide reliable contact between the chip and the conductive elements of the elastomer while preventing contamination on the elastomer so as to extend the useful life of conductive elastomers. Adding another interface above the conductive elastomer will cause the performance of the system to be affected. To minimize its impact on the performance of the elastomer contactor, the following considerations should be made in contact sheet design:

Minimize the electrical length of the contact sheet. The major advantage of conductive elastomer is its low profile and excellent signal integrity. The contact sheet increases the electrical path of the contactor and may generate signal loss and generate noise, impacting the signal integrity performance of the whole contactor structure. To minimize the impact, the contact sheet should be kept as low profile as possible.

Minimize force while maintaining effective compliance. Differing from spring probes, the compliance of elastomer is low and creates a weakness for large sized device applications. The primary cause of low compliance is due to the high compressive force needed to achieve increased compliance, which can be much higher than the allowable force of the handler in package testing. The contact sheet sits above the elastomer and should keep the same compliance as the elastomer itself. If the contact sheet has limited allowable compliance or needs extra force, the elastomer contactor may not provide enough compliance for large size package applications.

Optimized contact sheet structure

As mentioned above, low compliance with high compressive force is one of

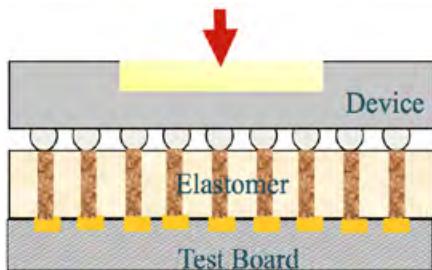


Figure 1: BGA chip on an elastomer contactor.

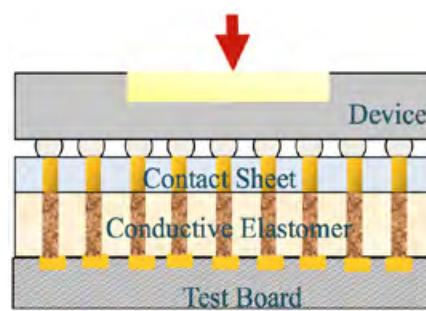
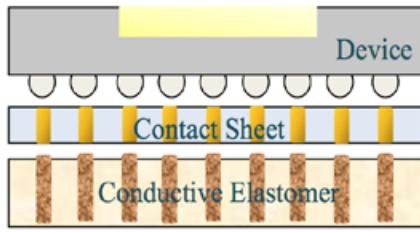
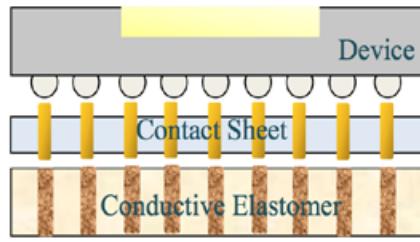


Figure 2: Contact sheet in an elastomer contactor.



Type a. Embedded head in polymer



Type b. Moving head in polymer

Figure 3: Two types of contact sheets.

the limitations in conductive elastomer applications. Adding a contact sheet above an elastomer may increase compressive force significantly, depending on the structure of the contact head. **Figure 3** shows two examples of contact sheets, described below.

The type A contact sheet has contact heads bonded onto one elastic polymer sheet and is widely used in the industry. The advantage of this contact sheet is a reduced thickness of the contact head to minimize the impact on SI performance of the elastomer. During the compression process, the elastic polymer deforms and allows the

contact heads to move down. But the tension stress inside the elastic polymer during the compression process may increase the total compressive force significantly depending on the elastic modulus. The elastic polymer sheet should have a low elastic modulus.

The type B contact sheet is represented by individual plungers placed in the cavities of the contact sheet. The vertical movement of the plunger is determined by the conductive element itself and independent of the contact sheet body material. The body material may be either general test socket material or another low elastic modulus composite material. The weakness of a free moving

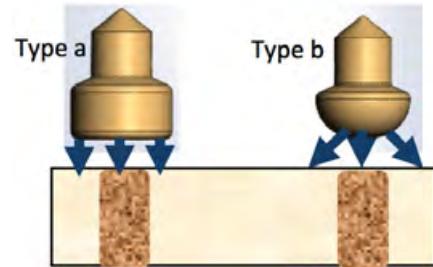


Figure 4: The two-nail structure of contact heads: a) flat nail; b) round nail.

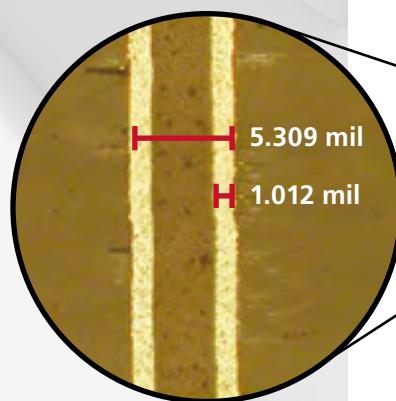
plunger structure is in its impact on SI performance of the whole contactor as it may be longer than the elastomer. Specific contact sheet cavities must be developed for this application.

The main influence on the elastomer contactor compressive force comes from the bottom or nail structure of the contact head in the contact sheet. **Figure 4** presents two structures of contact heads, one with a flat nail and another with a round nail. The flat nail head (**Figure 4a**) contacts the elastomer with a flat, circular area. When the head is compressed, the force on the contact boundary faces down to the elastomer, or

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is in the Z direction, without a side force in the X-Y directions. The compliance comes from compression of the elastomer under the contact head and produces a significant mechanical resistance against the head depressing, as shown in **Figure 4**.

The other contact head has a round nail structure. This geometry allows side force in the X-Y directions when compressed, as shown in **Figure 4b**. Squeezing the elastomer in the X-Y directions allows more compliance in the Z-axis with less force. The chart in **Figure 5** compares the force-compliance relationship of these two contact heads. The measurements show the type 2 contact head has much less force while having larger compliance in the Z-direction.

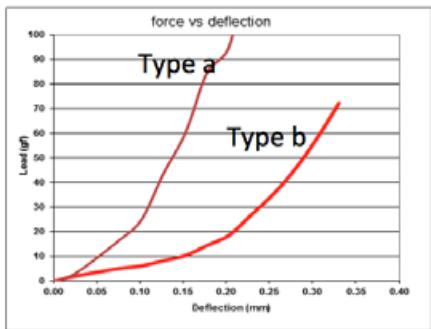


Figure 5: Force-compliance charts.

Thin contact sheet for best SI performance

The contact sheet will affect SI of the elastomer contactor. Studies have been done to demonstrate the effect of introducing a contact sheet on SI performance of elastomer contactors. Generally, the mechanical structure and material of the contactor determines the SI performance. The general guidelines of contactor design influencing SI performance are therefore applicable for contact sheet/conductive elastomer and should be considered.

Total length of the contactor (contact sheet head + elastomer thickness). As shown in **Figure 6**, the bandwidth decreases significantly when the contactor length is >3 mm. Most conductive elastomer thickness is ~ 1 mm. After adding a contact sheet, the total contactor length is around 2~3 mm. Using a minimal contact sheet thickness is critical for contact sheet design. Thinner contactors minimize the noise in signal transmission. Other considerations are as follows:

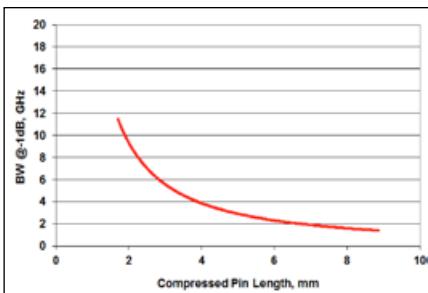


Figure 6: Bandwidth vs. contactor length.

1. The contact head diameter should be similar to the elastomer's conductive column diameter to avoid the sharp variation in signal path. Generally, larger diameter contactors have less inductance, while smaller diameter contactors have higher bandwidth at the same pitch structure.
2. Contact sheet head material usually uses Cu plus Au/Ni plating with minimal elastic polymer material options. Contact sheet materials, therefore, do not have a significant impact on SI of the elastomer contactor.

Cleaning methodology

Cleaning is always a concern for conductive elastomer contactors. Protection of the conductive elastomer is another major advantage of contact sheet. Direct contact of chip devices on the elastomer affects elastomer life significantly because of the quick contamination on the elastomer surface as shown in **Figure 7**. The contact sheet heads have similar crown structures and materials as spring probes or other contactor technologies. These crown structures provide reliable contact with ball grid array (BGA) balls or land grid array (LGA) pads. **Figure 8** is an example of a contact head crown with a ball. The contact crown can be very similar to the spring probe top crown. For a lower profile contact sheet, partial crown structures can be applied as shown in **Figure 9**. The contact boundary and mechanism with package ball or pads are the same as spring probe contactors. So, as a general guideline, the cleaning methodologies used in other metal contactors can be applied to the contact sheet on conductive elastomer contactors. Some cleaning methods, for both the contact sheet and elastomer, are outlined below. The

proper cleaning frequency should be selected based on actual device testing yield and contamination on the contact sheet surface.

On-line cleaning (contact sheet only). The conductive elastomer with the contact sheet is kept on the test board with the socket. Use the following procedure for cleaning:

1. Use Mipox or a cleaning sheet with a manual compression lid or auto test handler to clean the contact sheet head crown.
2. Use a soft nylon brush and compressed air if the environment allows, to clean the contact sheet head crown.

Off-line cleaning. The contactors are removed from test boards and disassembled from the sockets. Use the following procedure for cleaning the contact sheet and elastomer:

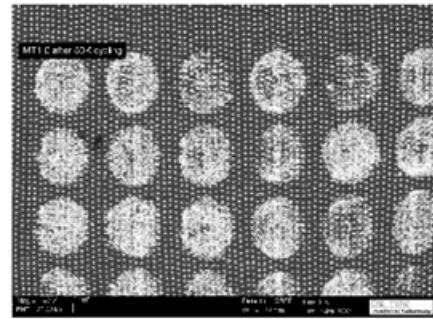


Figure 7: Contaminants on an elastomer sheet.

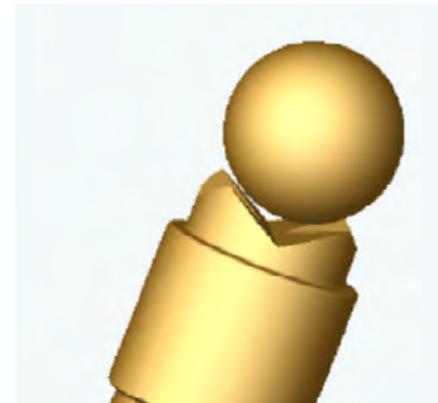


Figure 8: Example of head crown.

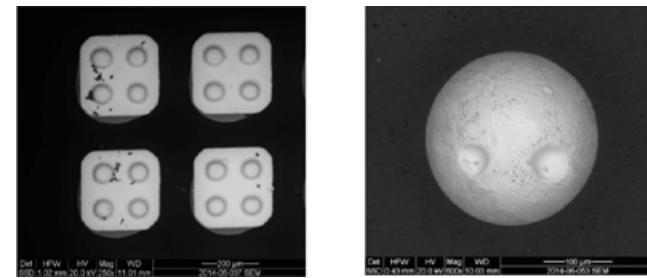


Figure 9: Contact head crown and contact marks on the ball.

Contact sheet. 1) General cleaning with a soft nylon brush and compressed air to blow off debris; and 2) The contact sheet can be removed from the socket allowing both sides to be cleaned with chemicals, such as 99% isopropyl alcohol. If cleaning chemicals are used, the contact sheet must be completely dry prior to re-installing with the elastomer. The same holds true if the PCB is cleaned with chemicals.

Elastomer. 1) A stiff/wire brush should never be used. Alcohol or other cleaning chemicals should also never be used. If these chemicals are used to clean the contact sheet or the PCB, then they must be completely dry prior to contact with the elastomer. 2) Compressed air should be used first to blow dust and debris from both sides. 3) If there is debris that cannot be removed by air, a soft animal hair brush or a light adhesive, such as a Post-it® note, can be used to gently

remove any remaining debris. Contaminants can also be removed by carefully using tweezers under a microscope.

Summary

For many years, conductive elastomer contactors applied in IC package testing have demonstrated their strength through excellent signal integrity performance. However, the rapid performance degradation due to contamination on the elastomer surfaces has affected their wider market acceptance. Using a contact sheet with an elastomer is an effective approach to protecting the elastomer and increasing service life. To minimize the impact on elastomer performance, the following key factors should be considered when optimizing the contact sheet structure:

1. Minimize thickness of the contact sheet for better RF performance.
2. Apply all knowledge of contact geometries from other contactor technologies on the package ball contact to reduce contamination and increase self-cleaning.
3. Maintain enough compliance in the contact sheet to ensure contact while minimizing the impact on compressive behavior of the elastomer sheet.
4. Avoid extra compression force on the elastomer sheet through proper head structures.
5. Cleaning methods commonly used in package testing can be applied to contact sheets.

We have done extensive research to optimize the contact sheet performance with a patented contact sheet structure. The experimental and field application data have shown the contact sheet can be used for more than 2 million cycles with cleaning at every 100K cycles, which provides a significant advantage for users.

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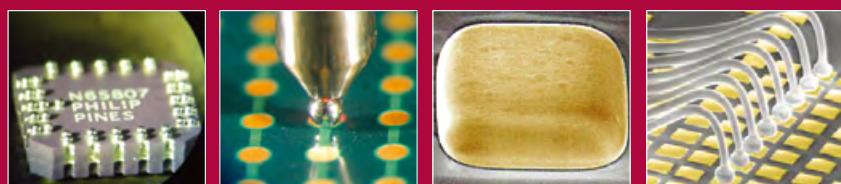
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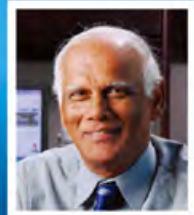
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An environmentally friendly packaging platform for SiP

By Dyi-Chung Hu /SiPlus Co.

The 2015 Paris agreement highlights the need for worldwide efforts to ease climate change. For the electronic packaging industry as a whole, the question is: can we contribute to reducing carbon and energy in the electronic packaging industry? There are several directions that our industry can contribute to a greener planet: 1) Remove unnecessary materials used in electronic packaging systems; 2) Reduce the overall processes used during the manufacture of the electronic packaging system by simplifying the electronic packaging structure; 3) Reduce the recycling efforts after the end of the product life of the electronic system. At the other end of the spectrum, society is moving rapidly to the era of The Internet of Things (IoT) where everything is connected. Additionally, bandwidth and processing speed are needed in the evolution of the electronic packaging system. It is desirable to develop electronic packaging platforms that meet both the high-performance and environmentally friendly requirements. It is the intent of this article to introduce a system packaging platform that meets both high-performance and environmentally friendly requirements.

Conventional electronic packaging structure

As Moore's law progresses from 14nm, to 10nm, or even to 7nm, the needs of fine-line interconnections are in demand. Traditionally, laminated printed circuit boards (PCBs) have been widely used in the electronic packaging industry. However, as IC density increases, the line width used by the subtractive method in the manufacture of PCBs cannot meet the density requirements of the IC chips. Therefore, the laminated substrate using a semi-additive process to make finer lines was introduced to meet industry demand. Current subtractive PCB technology can reach 40 to 50 μm line widths in mass production and the substrate technology that uses a semi-additive process can reach

10 μm line widths in mass production in 2015. However, the industry need for even finer line connections is ever increasing. This situation has led to the development of silicon interposer technology. A silicon interposer, or 2.5D substrates, can achieve fine lines up to 1 μm and even to sub-micron lines, which meet the electronic packaging requirement. However, this introduces one additional level of substrate. Current packaging structure is shown in **Figure 1**. First, we connect chips to the fine-pitch 2.5D interposer, then connect it to the substrate, and lastly, connect to the PCB as indicated in **Figure 1** [1]. If we look into the packaging structure closely, we find some of the materials that are not necessary for interconnection. The first ones are TXVs (whether through-silicon vias (TSVs), through-ceramic vias [TCVs], through-laminated vias [PCBs/TLVs], through-glass vias [TGVs]) and cores. In each level of technology, the interposer, substrate and PCB use a different manufacturing line. The core is most commonly used to support the dielectrics with connection to a copper trace. Cores and TXVs are needed to support the connections between the top copper circuitry and the bottom copper circuitry. Theoretically, one can reduce the thickness of the cores to zero without losing the interconnection function of the substrate. In fact, there is a small fraction of substrate called "coreless substrate" used in the laminate substrate packaging industry [2]. There are also studies of removing silicon substrates from the silicon interposer. Examples include (silicon-less interconnection technology (SLIT) and Silicon-Less Integrated Module (SLIM™) technology proposed by Xilinx, and Amkor [3,4], respectively. This clearly indicates that the cores and TXVs do not have to be in the interconnection system.

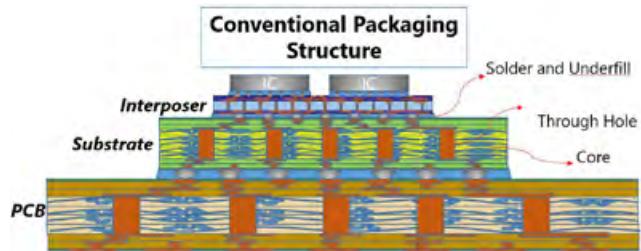


Figure 1: A conventional high-performance packaging structure.

To complete the interconnection system, one needs to connect the interposer, substrate and PCB. Lead-free solder is used for this purpose. Sometimes, underfill between the interposer and the substrate are needed to enhance the reliability. The question is: are the solders and underfills really needed? The answer is: maybe not. It is clear that the industry tries to remove solder between dies and the substrate. The structure of fan-out wafer-level packaging (FOWLP) is for that purpose. One of the most well-known FOWLP platforms is the integrated fan-out wafer-level package (InFO-WLP) promoted by TSMC [5]. Using FOWLP, the solder joints between the chips and substrate have been removed. The removal of solder joints between interposer and substrate was first proposed by this author in the EIC (embedded interposer carrier) structure [6]. Therefore, the removal of solder joints and underfills do not affect the interconnection function of the system. The removal of solder joints has many benefits. First, the removal of solder joints can reduce the Z height. Second, long-term reliability of solder joints is always a concern in the industry. Third, the cost of solders and the furnaces for solder reflow needed for the solder joining process can be reduced or eliminated. It is better to have no solders in the packaging structure. One additional benefit is that by the removal of the core structure, the system weight and z height can be reduced. These benefits become important to IoT and wearable device systems.

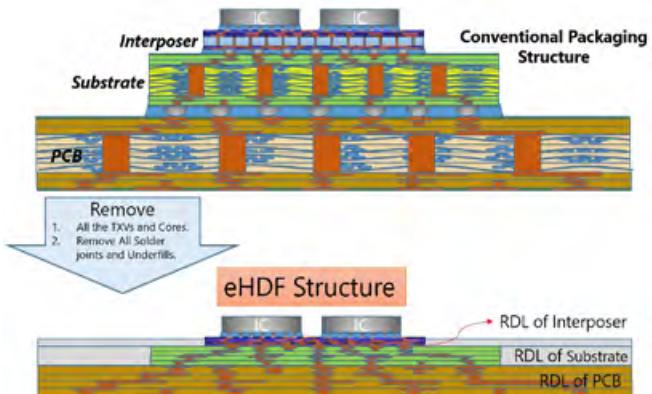


Figure 2: The embedded high-density film (eHDF) structure after chips have been attached. Notice how it contrasts with the conventional system packaging structure.

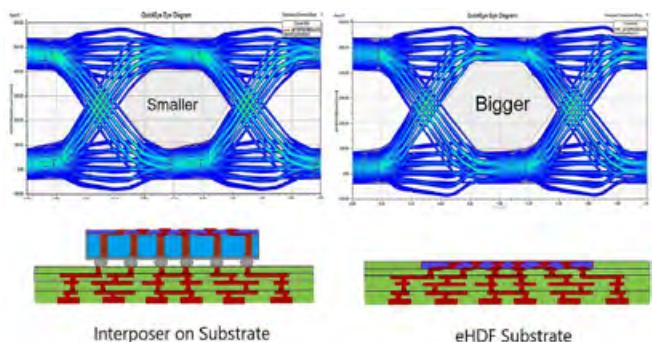


Figure 3: Signal integrity of the simulation of an eye diagram for conventional and eHDF structures.

	Chip on Interposer on Substrate Module (ColoS)	eHDF Module
Cores	2 (Silicon Substrate + Laminate Core)	None
TXVs	2 (TSV+TLV)	None
Solder Joints	2 (Chip bonding, Interposer joining)	1 (chip bonding)
Z heights	Baseline	Lower
Weight	Baseline	Lighter
Process steps	More	Less
Electrical Performance	Baseline	Better
Mechanical Strength	Better	Baseline
Thermal	Baseline	Better
Cost	Baseline	Less (ref. this article)
Compatibility to current OSATS infrastructure	Complex	Better Compatibility

Table 1: Compare conventional ColoS (chips-on-interposer-on-substrate) and eHDF structure.

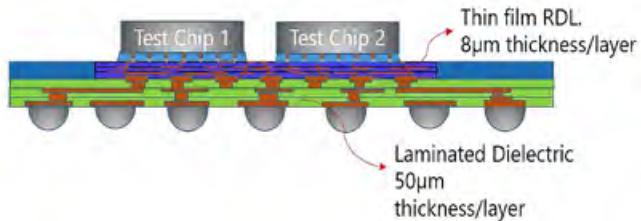


Figure 4: Diagram of an eHDF test vehicle.

The embedded high-density film (eHDF) structure

The embedded high-density film (eHDF) structure was first proposed by this author [1,6]; **Figure 2** shows the basic concept of this structure. In **Figure 2**, it can be seen that the eHDF structure does not have cores and the associated TXVs. In addition, all the solder joints and underfills are removed from the eHDF packaging structure. One can regard this as an integration of substrate technology. It integrates the interposer, substrate and PCB into “one structure.” The eHDF substrate does not require extra core materials, TXVs, solders and underfills and the extra processes associated with manufacturing them. Therefore, the eHDF platform needs less direct and indirect materials and it also requires fewer processes and energy to process them.

Up to this point, we have not mentioned the impact of conventional structure (**Figure 1**) to the signal integrity.

Figure 3 shows the simulation of signal integrity for signals that travel from chip 1 to chip 2. It is clearly shown from this simulation that structure 2 does not have TSVs, solder joints and underfills, and has better electrical performance based on the simulation of the eye diagram. This difference between the two structures is obvious because the signal passes through a longer distance in the conventional structure and also has passed through solder joints that have a higher impedance. **Table 1** compares the pros and cons of the proposed eHDF system with the conventional electronic packaging system that has TXVs and solder joints.

In short, eHDF is an environmentally friendly electronic packaging platform. It also has a better electrical performance. The eHDF concept is based on removing all the unnecessary components in the electronic packaging system. It only retains the connection functions that are necessary for the system integration. All the components are connected by “one substrate” that fits the needs of the packaging system. By doing so, it greatly simplifies the electronic packaging system. Additionally, the eHDF substrate is compatible with the existing electronic packaging infrastructure.

Evaluation of the eHDF platform

The test vehicle includes development of an eHDF substrate and connecting two silicon test chips to the eHDF substrate. Four layers of copper trace with 3/3µm design rule in three layers of dielectrics were processed. The dielectric thickness was 8µm with a copper thickness of 3µm. This high-density interconnection is indicated in the blue area of **Figure 4**. The dielectric used is a commercially available polyimide. The build-up of the high-density thin film is carried on a temporary glass carrier. Later, ABF-type of build-up materials are laminated on the back of the high-density thin film substrate. The copper RDL width in the laminated dielectric layer is about 15µm. The thickness of the laminated dielectric is about 50µm. Three build-up (BU) layers were applied by using the laminated substrate technology: laser drilling, E-less copper plating and semi-additive copper plating. The total thickness of the final substrate was about 180µm. A test vehicle of two chips was obtained: one is 9x9mm² in size and mimics an application processor (AP), and the other is 10x10mm² in size and mimics a wide I/O memory chip with an I/O pitch of 40µm. The chip’s UBM comprises 5µm Cu, 3µm Ni with 5µm Sn2.5Ag soldering material on top.

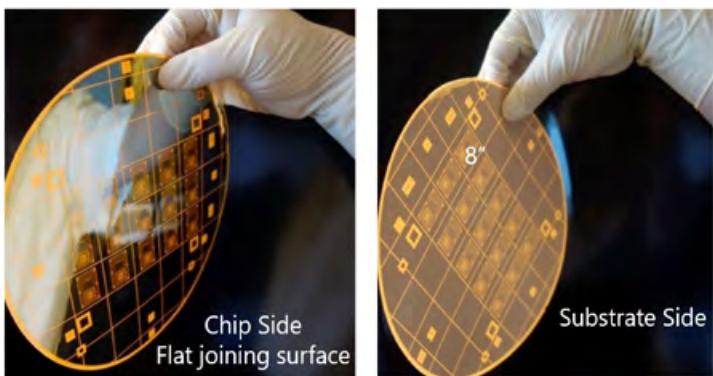


Figure 5: An eHDF substrate released from the carrier: a) (left) Connections to the chip side; b) (right) The connection to the PCB side.

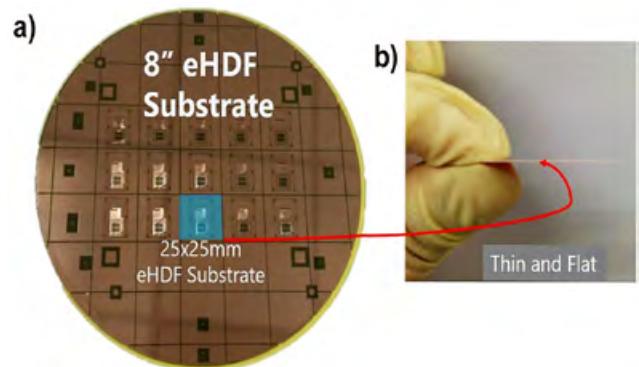


Figure 6: a) (left) An 8" eHDF mother substrate; b) (right) A 25x25mm eHDF substrate singulated from the 8" eHDF mother substrate.

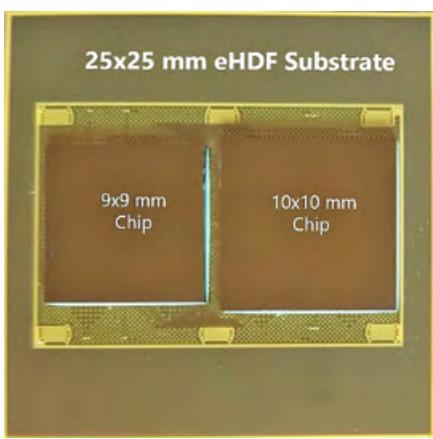


Figure 7: Two test chips are bonded to an eHDF substrate.

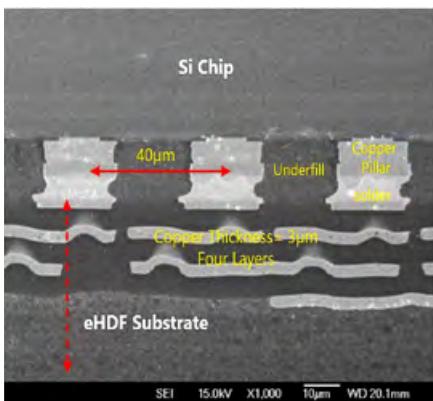


Figure 8: Cross-sectional view of an eHDF substrate with chips assembly. The pitch between the bump is 40μm.

The finished eHDF substrate can be released from the glass carrier. **Figure 5** shows the eHDF substrate released from the carrier. Even though the total thickness of the eHDF is only about 180μm, it is easy to handle without too much warpage of the substrate. **Figure 6a** shows the location of a 25x25mm eHDF test vehicle. **Figure 6b** shows

a 25x25mm eHDF test vehicle after singulation. The singulated substrate is very flat with good warpage control.

Figure 7 shows two chips are bonded to the eHDF substrate using TCNF bonding. The SEM photo shown in **Figure 8** presents the cross-sectional view of the eHDF substrate. The picture indicates good connection between the test chip and the eHDF substrate. The pitch between the copper pillars is only 40μm. A 40μm pitch is required for a wide I/O memory chip interconnection. In addition, no delamination or cracks were found in the substrate cross section.

Summary

An innovative and environmentally friendly electronic packaging platform called eHDF was proposed. The structure eliminates cores, TXVs, and solder with underfills that are in the traditional package. Part of the solder mask and surface finishing can also be eliminated. This new packaging platform, therefore, has a lower overall system cost because there are less direct and indirect materials, and fewer processes were used. Additionally, because the electrical signal does not need to pass the cores and solders in the substrate, the quality of the electrical signal is better—especially at higher operating frequencies. The result is a very simple structure in which the “three” levels of packaging substrates were greatly simplified to “one.”

Also demonstrated were two dies with a die size of approximately 10x10mm² connected on top of the eHDF substrate. Future work is planned to evaluate functional chips based on the eHDF structure, as well as

optimization of materials used for the eHDF structure.

Acknowledgements

The author wishes to thank Unimicron Technology Co., Princo Co., and ITRI EOL Division for their help in the development of the eHDF substrate and die interconnections.

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Biography

Dyi-Chung Hu received his PhD in Material Science and Engineering from the Massachusetts Institute of Technology. He is the CEO of SiPlus Co.; email hu.siplus@gmail.com

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GUEST EDITORIAL

Yield management turns green

By David W. Price, Douglas G. Sutherland, Kara L. Sherman, Stephen Hiebert [KLA-Tencor]

In all segments of the semiconductor industry, there has been increased effort by companies to reduce their environmental impact. fabs have been building Leadership in Energy and Environmental Design (LEED)-certified buildings [1-5] as part of new fab construction and are working with suppliers to directly reduce the resources used in fabs on a daily basis. Outsourced semiconductor assembly and test (OSAT) and other packaging facilities are also implementing environmental policies and investing resources in reducing waste and resource consumption [6-10].

Advanced packaging technologies, such as wafer-level chip-scale packaging (WLCSP), fan-out wafer-level packaging (FOWLP), and 2.5D/3D IC integration, offer device performance advantages, such as increased bandwidth and improved energy efficiency. The packaging production methods, however, are more complex—involving the implementation of typical front-end IC manufacturing processes, such as lithography, chemical mechanical planarization and high aspect ratio etch, and unique processes, such as temporary bonding and wafer reconstitution. These complex packaging methods require an increasing number of process steps resulting in each step needing to reach higher yield levels in order to produce a functioning final product. Process control solutions can be used from the wafer-level to final component to help address challenges associated with advanced packaging technologies. In addition, the implementation of process control can help packaging facilities reduce scrap and rework, thereby reducing overall resource consumption. Specifically, by implementing capable process control solutions

and adding additional process control steps, packaging facilities reduce scrap and net resource consumption per good component out (**Figure 1**).

Semiconductor manufacturers monitor the amount of resources that go into each wafer/chip. They are continually trying to reduce the overall resources used per good die out, but this is becoming more and more challenging as the process complexity increases and node-to-node more layers and material are added to the manufacturing process. As an example, a single cm^2 of device can require more than 1kWh of power, and 6 liters of city water to manufacture. This is prior to entering the packaging stage, which adds additional resources to the overall resource consumption for a given packaged chip. Because of the increase in the number of layers for both the front-end- and back-end-of-line processes, some semiconductor manufacturers have shifted to reporting environmental goals based on an 8" equivalent layer rather than the resources/ cm^2 [5].

Improved process control performance

Process control is used to identify manufacturing excursions, providing the data necessary for packaging engineers to make dispositioning decisions and to take the corrective actions required to fix process issues. To be effective,



Figure 1: The basic equation for improving a packaging facility's environmental performance includes reducing resource use and increasing yield. Capable process control solutions help packaging facilities do both by identifying process issues early, thereby reducing scrap and rework.

however, the quality of the process control measurement is critical. If an inspection or metrology tool has a lower capture rate or higher total measurement uncertainty (TMU), it can erroneously flag an excursion sending wafers for unnecessary rework or scrap, known as overkill. All of the resources that went into producing the die are wasted when it is unnecessarily scrapped due to overkill in the packaging process. Alternatively, if the measurement fails to identify a true process excursion, also known as underkill, the yield of the product is negatively impacted and more bad dies/packages continue to be processed, which are not detected until final testing or worse, are sent on to the customer—again, resulting in less desirable environmental performance.

The example shown in **Figure 2** examines the environmental impact of

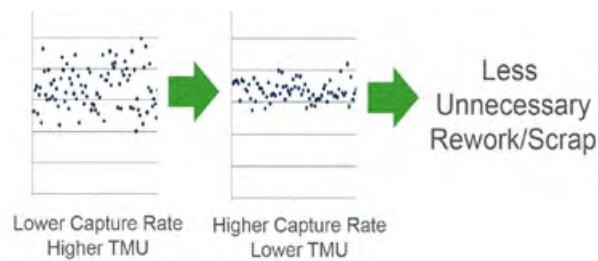


Figure 2: Higher quality process control tools produce better process control data within the advanced packaging line, enabling a 1.0% reduction in unnecessary scrap or overkill that results in better environmental performance.

the process control data produced by two different inspection tools used in component inspection. By implementing a higher quality inspection tool, the quality of the process control data is improved and the engineers are able to make better process decisions resulting in a 1.0% reduction in unnecessary scrap or overkill. In a packaging line that processes 70 million units a month, this 1.0% reduction in scrap results in approximately 8 million kWh of power and 50 million liters of water not being wasted over the course of a year—and a proportional percentage reduction in the amount of packaging materials consumed.

Earlier excursion detection reduces waste

Packaging facilities are also reducing process excursions by adding process control steps. **Figure 3** shows two examples of deploying an inspection tool in a wafer-level packaging facility. In the first case (**Figure 3**, left), inspection points are set such that a lot is inspected at the beginning and end of a redistribution

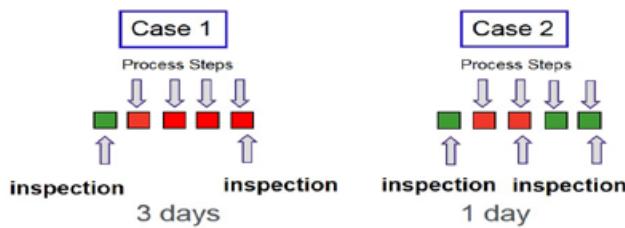


Figure 3: Adding an additional inspection point to the line will reduce the material at risk should an excursion occur after the first process step.

layer (RDL) loop, with four process steps in between. If a process excursion that results in yield loss occurs immediately after the first inspection, the wafers will undergo multiple processing steps, and many lots will be mis-processed before the excursion is detected. In the second case (**Figure 3**, right), inspection points are set with just two process steps in between. The process excursion occurring after the first inspection point is detected two steps sooner, resulting in much faster time-to-corrective action and significantly less yield loss and material wasted. Furthermore, in Case 1, the process tools

at four process steps must be taken offline; in Case 2, only half as many process tools must be taken offline.

With typical processes taking 1-2 days per RDL layer there can be a significant amount of product at risk. This two-day delta in detection of a process excursion for a wafer-level packaging line processing 50k WSPM of application wafers with just a 10% yield impact results in a savings of approximately 98,000kWh of power and 619K liters of water. While these environmental benefits were obtained by sampling more process steps, earlier excursion detection and improved environmental performance can also be obtained by sampling more sites on the wafer, sampling more wafers per lot, or sampling more lots. When a careful analysis of the risks and associated costs of yield loss are balanced with the costs of additional sampling, an optimal sampling strategy has been attained [11-12]. With a trend toward an increasing amount of RDL layers, faster time to information and correction in the wafer packaging line becomes even more critical and can have an even bigger impact on environmental performance.

Summary

Advanced packaging facilities can obtain several environmental benefits by implementing

higher quality process control tools, optimal process control sampling, and faster cycles of learning. A comprehensive process control solution not only helps packaging facilities improve yield, but also reduces scrap and rework, reducing their overall impact on the environment.

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INDUSTRY NEWS



Institute of
Microelectronics

A*STAR's IME kicks off consortia to develop advanced packaging solutions for next-generation internet of things applications and high-performance wireless data transfer technologies

Innovative capabilities developed will lead to higher power efficiency and lower costs for MEMS and silicon photonics devices

Singapore — A*STAR's Institute of Microelectronics (IME) has launched two consortia on advanced packaging, the Silicon Photonics Packaging consortium (Phase II) and the MEMS Wafer Level Chip Scale Packaging (WLCSP) consortium. They will develop novel solutions in the heterogeneous integration of micro-electromechanical systems (MEMS) and silicon photonics devices, which will boost overall performance and drive down production costs. The new consortia will leverage on IME's expertise in MEMS design, fabrication, wafer level packaging process, as well as silicon photonics packaging modules and processes.

The proliferation of the Internet of Things (IoT) is driving the rapid growth of diversified technologies which are key enablers in major application domains such as smart phones, tablets, wearable technology; and network infrastructures that support wireless communications.

However, this trend requires the complex integration of non-digital functions of "More-than-Moore" technologies such as MEMS with digital components into compact systems that have a smaller form factor, higher power efficiency and cost less. The onset of big data, cloud computing and high speed broadband wireless communications also calls for novel use of silicon photonics. Silicon photonics are a critical enabler of high density interconnects and high bandwidth, to meet high optical network requirements cost-effectively.

In the previous Silicon Photonics Packaging Consortium (Phase I), IME and its industry partners developed new capabilities in necessary device library and associated tool boxes to enable the integration of low profile lateral fibre assembly, laser diode and photonics devices. By employing a laser welding technique, the consortium demonstrated a fiber-chip-fiber loss of less than 8 decibel (dB) with

less than 1.5dB excess packaging loss. These capabilities enabled integrated silicon photonic circuits to provide higher data rates at lower cost and power consumption.

Building on these achievements, the Silicon Photonics Packaging Consortium (Phase II) will develop a broad spectrum of silicon photonics packaging methodology. The consortium will further develop low loss silicon coupling modules, and provide a series of packaging solutions for laser diode integration. It will also focus on developing accurate thermal models, as well as improve overall module thermal management, reliability and radio-frequency (RF) performance to meet very high data bandwidth demand. All these new developments will lead to a more integrated packaging solution which promises better assembly margins and lower module costs.

IME's MEMS WLCSP Consortium has also been established to develop a cost-effective integration packaging platform for capped MEMS and complementary metal-oxide semiconductor (CMOS) devices. This platform could be used for any MEMS devices with cavity-capping such as timing devices, inertial sensors, and RF MEMS packaging.

Conventional chip stacking that relies on a through-silicon via (TSV) and wire bonding on substrate method will usually result in high costs and large form factor. The consortium aims to lower production costs and achieve smaller footprint by developing a TSV-free over-mold wafer level packaging solution for MEMS-capped wafer using a novel metal deposited silicon pillar and wire bonding as a through mold interconnects.

The consortium aims to reduce form factor of integrated MEMS and CMOS devices by approximately 20 per cent, and lower manufacturing costs by approximately 15 per cent. These cost-effective packaging solutions are also expected to produce better electrical and reliability performance.

"These consortia partnerships play a critical role in developing innovative solutions to meet emerging market demands. Through these collaborations, we will elevate our capabilities from developing MEMS and silicon photonics devices to developing advanced solutions in heterogeneous integration. The capabilities developed will enable our industry partners to capture new growth opportunities in the IoT space and accelerate market adoption of cost-effective technologies," said Prof. Dim-Lee Kwong, Executive Director of IME.

"Silicon photonics packaging is a crucial technology for the commercialisation of silicon photonic devices. The partnership generated remarkable results in the Silicon Photonics Packaging Consortium Phase I, and we are pleased to continue with the second phase, which will expand the application of silicon photonics with innovative approaches in terms of LD integration and RF performance. Through this consortium, Fujikura will accelerate the development of compact and cost-effective optical communications for diverse markets," said Mr. Kenji Nishide, Executive Officer, General Manager, Advanced Technology Laboratory, Fujikura Ltd.

"Currently, it is anticipated that the demand for sensors will grow from billions to trillions by 2050. This demand is being driven by the emergence of sensor based smart systems fusing computing, connectivity and sensing in the context of the Internet of Things. IME's packaging consortium partnership will allow us to identify and develop MEMS packaging innovative solutions in order to scale up for the Internet of Things," said Mr. Mo Maghsoudnia, Vice President of Technology and Worldwide Manufacturing of InvenSense.

Mr. Shim Il Kwon, Chief Technology Officer, STATS ChipPAC said, "As the number of MEMS devices in emerging IoT applications continues to grow, semiconductor packaging will have a

significant impact on the performance, size and cost targets that can be achieved. By collaborating with our partners in the consortia, we will be able to help drive the cost effective integration of MEMS and ASICs in high performance, high yield WLCSP solutions for IoT products.”

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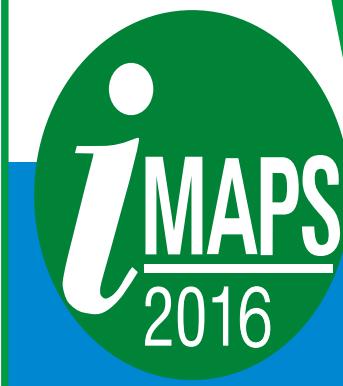
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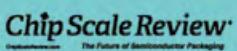
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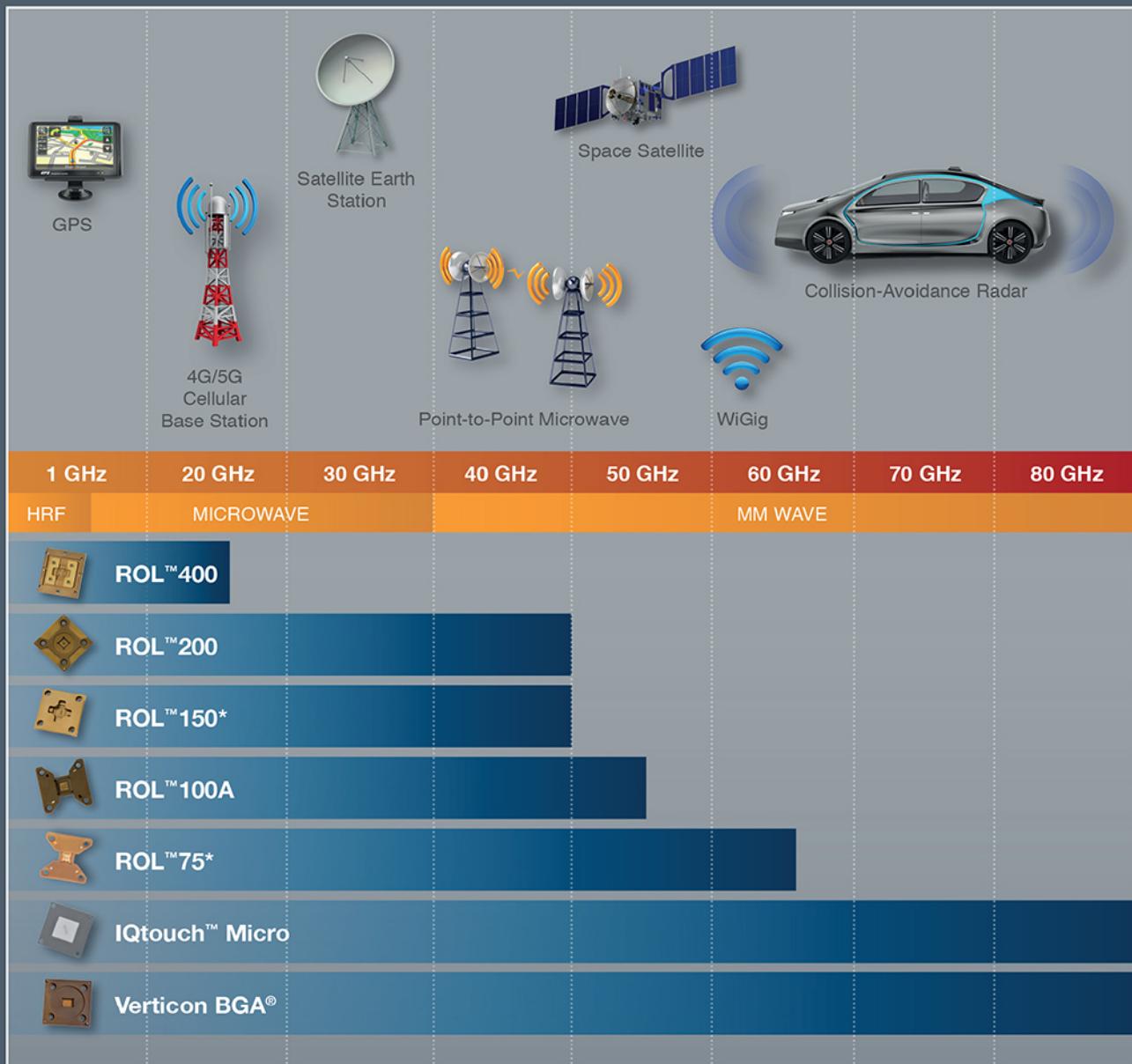
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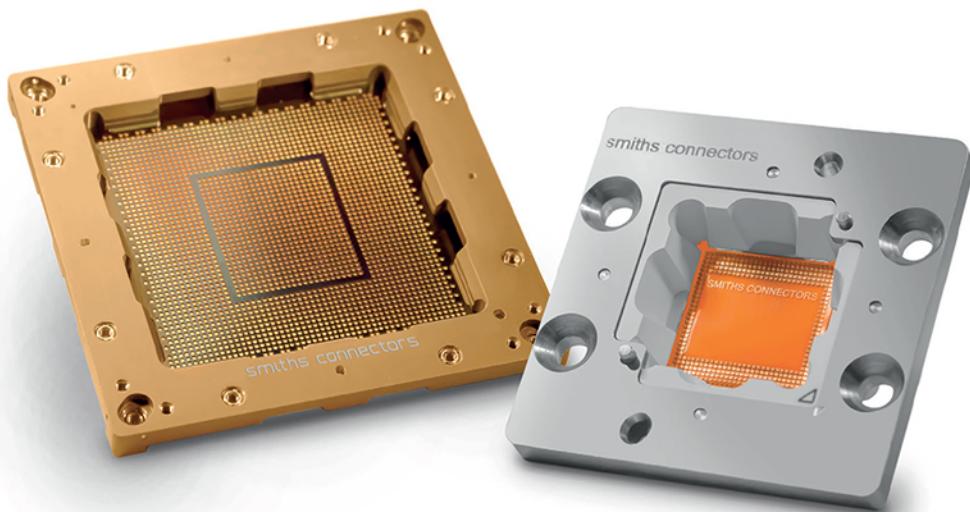
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