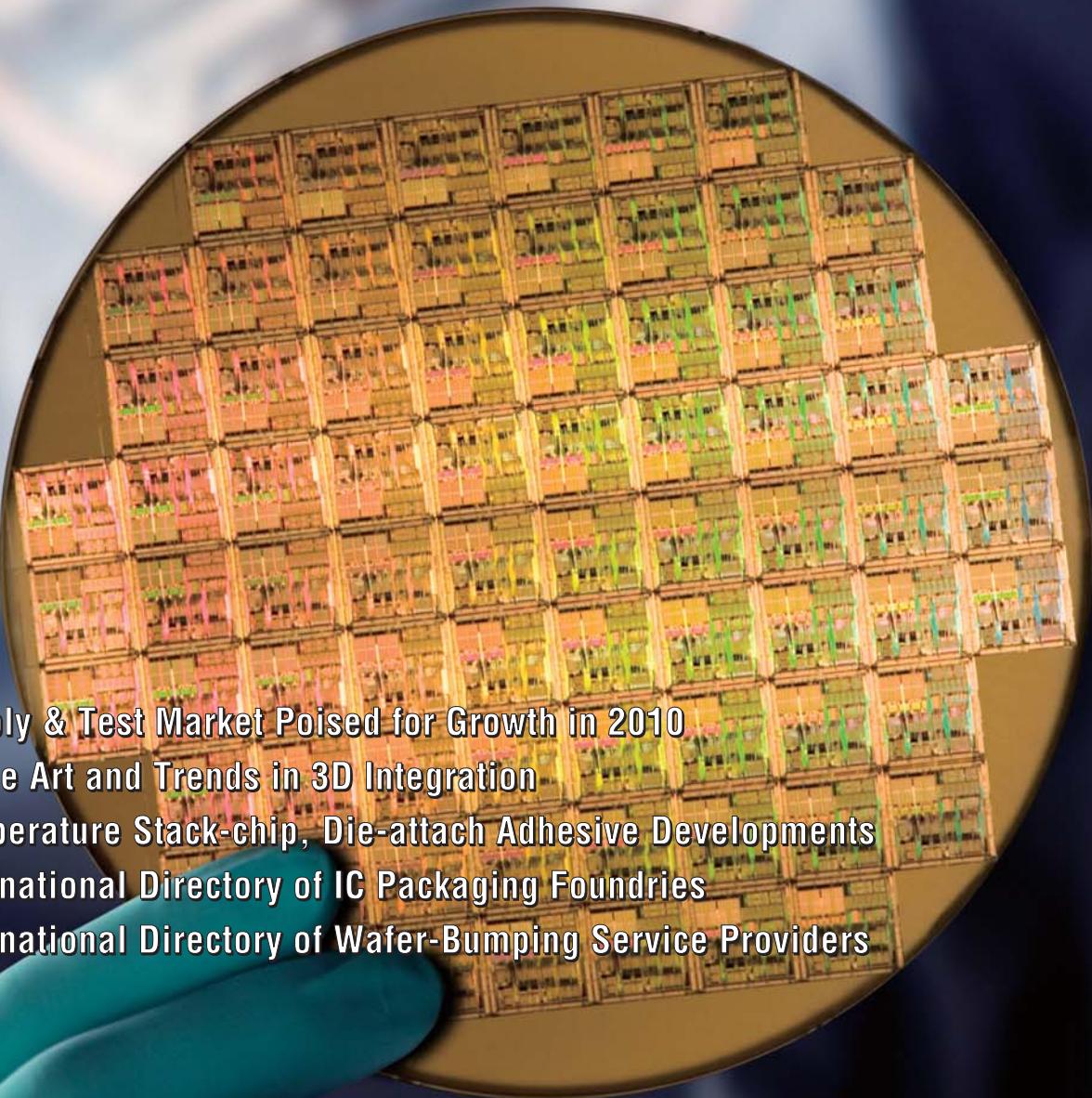


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March-April 2010



- IC Assembly & Test Market Poised for Growth in 2010
- State of the Art and Trends in 3D Integration
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- 2010 International Directory of IC Packaging Foundries
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CONTENTS

March-April 2010

Volume 14, Number 2



Photograph by Steve McAlister
This edition's cover depicts a large wafer being displayed by a clean-room technician.

These wafers substrates are the primary foundation for the microelectronic devices.

This process starts at the semiconductor fabrication plants, John H. Lau's article (page 22) goes in-depth in "State-of-the-art and Trends in 3D Integration."

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FEATURE ARTICLES

IC Assembly & Test Market Poised for Growth in 2010 The market and the Top 10 (11) players are analyzed Ron Molnar, AZ Tech Direct, LLC	13
State of the Art and Trends in 3D Integration Making good progress, but major challenges still lie ahead John H. Lau, Industrial Technology Research Institute (ITRI)	22
Next-Gen Advanced Packages Spell Opportunity for Burn-in and Test Community Françoise von Trapp, 3D InCites Group, LLC	29
High Temperature Stack-chip, Die-attach Adhesive Developments Kevin Chung, Ph.D AI Technology, Inc.	31

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DEPARTMENTS

From the Publisher Kim Newman, <i>Chip Scale Review</i>	4
Editor's Outlook <i>Variety Is the Spice of Life But too much is oh, so costly!</i> Ron Edgar, Technical Editor, <i>Chip Scale Review</i>	6
Industry News	8
2010 International Directory of IC Packaging Foundries	16
Emerging Trends Economic Outlook 2010 Sandra Winkler, Contributing Editor, <i>New Venture Research</i>	21
2010 International Directory of Wafer-Bumping Service Providers	35
What's New!	37
Product Showcase	39
Advertiser Index, Advertising Sales	40

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STAFF

Kim Newman Publisher
knewman@chipscalereview.com

Ron Edgar Technical Editor
redgar@chipscalereview.com

Gail Flower Contributing Editor
gail897@hotmail.com

Françoise von Trapp Contributing Editor
francoise@3dincites.com

Dr. Tom Di Stefano Contributing Editor
tom@centipedesystems.com

Paul M. Sakamoto Contributing Editor Test
paul.sakamoto@dftmicrosystems.com

Sandra Winkler Contributing Editor
slwinkler@newventureresearch.com

Dr. Ken Gilleo Contributing Editor
ken@ET-Trends.com

Jason Mirabito Contributing Legal Editor
mirabito@mintz.com

Carol Peters Contributing Legal Editor
cpeters@mintz.com

SUBSCRIPTION INQUIRIES

Chip Scale Review
T 408-429-8585
F 408-429-8605
subs@chipscalereview.com

Advertising Production Inquiries:

Kim Newman
knewman@chipscalereview.com

EDITORIAL ADVISORS

Dr. Thomas Di Stefano Centipede Systems
Ron Molnar Az Tech Direct, LLC.
Lee Smith, Amkor Technology Inc.
Dr. Andy Mackie Indium Corp. of America
Dr. Thorsten Teutsch Pac Tech USA
Dr. Fred Tuckerman Tessera Technologies
Charles Harper Technology Seminars
Dr. Guna Selvaduray San Jose State University
Prof. C.P. Wong Georgia Tech
Dr. Ephraim Suhir ERS Company
Nick Leonardi Premier Semiconductor Services

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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$85 per year to Canada or \$95 per year to other countries. In the U.S. subscriptions by first class mail are \$75 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at San Jose, Calif., and additional offices.

POSTMASTER: Send address changes to *Chip Scale Review* magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER



Timing is Everything ... So True!

By Kim Newman

With years of experience in the *Chip Scale Review* organization, transition to this new position has required that I become an author for this column. It is now obvious, based on phone calls, recipients of this magazine do read (and critique) our "From the Publisher" column. Case in point, use of "cautiously optimistic" in the prior issue, drew comments and expertly constructed graphs on trends exceeding industry forecasts. Timing is everything and just a few short weeks after that column, actual trends and indicators continue to be optimistic. With the trends in mind, it is my pleasure to share information on current publication activities and key industry events.

Phoenix, Arizona was the place to be; as Media Sponsor, our staff manned the *Chip Scale Review* booth at the 11th Annual BiTS Conference and Exhibition. Fred Taber, General Chair, confirmed the momentum seen at the event with details on attendance, stating, "2010 full conference attendance was up 40% from 2009 with 25% international participation." There was positive feedback on our publication and current update of the International Socket Manufacturer Directory, with many of the 41 exhibiting companies being part of this listing. You will find more details and photos on the BiTS event further into this issue.

The Annual IMAPS Device Packaging Conference was also held in Phoenix, showing good attendance at the many technical presentations and strong exhibitor participation. It was also an opportunity to speak with Ron Molnar, Executive Director of AZ Tech Direct - Consulting Resource Network, our newest member of Editorial Advisors.

In addition to the Advisory role, AZ Tech Direct has been contracted to manage supplier communications and the updating of expanded Supplier Listings, with both Subcontract Assembly and Wafer Bumping in this issue.

There have been opportunities in past weeks to speak with new advertisers, article authors and industry experts, with each knowing the important part that timing will continue to play on the industry as we enter Q2 for 2010!

As we are in the microelectronics industry, we are continually challenged to provide a high amount of precision and accuracy in everything we do. As a journalist and publisher, I must ensure that *Chip Scale Review* is factual, accurate, and reflects the best our industry has to offer to all in the community, while being a conduit of events and news relevant to the trade.

There is and has been on-going commentary in the 2nd tier industry media that is specifically aimed at CSR, as the preeminent publication of this industry. Sometimes it is with the goal of carving some market share, sometimes motivated to convert product and services advertisers and sometimes just to be vindictive. While I am a firm believer of competitive markets, as this keeps us all sharp and innovative, I am not a proponent of published materials and statements that are short on fact, short on merit, and deliberately misleading. We here at CSR have chosen to rise above this.

The circulation and distribution of CSR is a matter of public record. We are more than open to sharing this with interested parties, as the more you know about us, the better we believe you will like us. What we are not open to is confrontation, dialog and acknowledgement with unprofessional, unethical and desperate self-described contenders in our community. It's always best to go to the source and for the facts. We hope that you will continue to support our cause of giving cutting-edge, factual and relevant information that helps all of us be the very best we can in this constantly changing and fast-paced environment we work in. 

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EDITOR'S OUTLOOK



Variety Is the Spice of Life But too much is oh, so costly!

By Ron Edgar redgar@chipscalereview.com

Spring—at last—and the Earth is reborn. In my part of America the snow is gone, the crocuses are blooming, and the grass is just starting to turn green. The migratory birds are returning and the peepers are singing in the swamp. It's been a long winter and we struggled with the cold, the wind, the floods, the power-outages, but like a bad dream, we awaken and find it's all behind us. Life is good. And you know, I'm starting to feel this way about the economic recovery—early days, but full of promise. But let's not get too excited: signs are that the recovery in 2010 will be more modest than some are hoping; however, it will be a whole lot better than 2009!

I make no apology for talking about nanotechnology again: I get excited by its possibilities. The following is adapted from a recent IMEC press release. *IMEC, Leuven, Belgium, just announced PRIMA, a new partnership under the EU's 7th framework program for ICT (FP7), with the goal of improving the efficiency and cost of solar cells through the use of metallic nanostructures. Together with IMEC, the project coordinator, the partners involved in PRIMA are Imperial College (London, UK), Chalmers University of Technology (Sweden), Photovoltaic (Belgium), Quantasol (UK) and Australian National University (Australia). Certain nanostructured metallic surfaces show unique characteristics: they can absorb and intensify light at specific wavelengths. This is because the incoming light results in a collective oscillation of the*

electrons at the metal's surface. This phenomenon, studied under the name plasmonics, has many promising applications. It can be exploited to transmit optical signals through nanosized interconnects on chips, in nanoparticles that recognize and interact with biomolecules, or in solar cells. These nanostructures have huge possibilities, not just in solar, apparently. I read recently about a NEMS structure which rolled like a sheet of paper into a tube and is so fine it can be used as a syringe capable of penetrating cell walls without damage. The possibilities for medical applications are seemingly endless.

As the saying goes, “Variety is the spice of life.” True, but unlike MTV’s “Too much is never enough,” there is a flip side. I was visiting the National Semiconductor web site recently and, while I know there are a lot of package types, I was staggered at how many. In their *Selection Guide by Package Type* they show 42 plastic package types and 15 hermetic types. Nested under each type are numbers of actual packages. Now, I know we need a variety of package types and some need a few I/Os and some need a lot, but I started thinking about the huge cost of supporting them all. It seems to me that if we could cut back on the huge variety that we, as an industry, could save a lot of time and money. Can you imagine if we only had to deal with half the variety? We could save billions. What is needed is a visionary to consolidate and standardize. Who will take the lead?

John H. Lau of the Industrial Technology Research Institute, Taiwan, ROC, is the author of our principal feature in this edition. This detailed *State-of-the-art and Trends in 3D Integration* article, with its many detailed illustrations, is worthy of a thorough read since there is so much useful information in it. Die-attach is a big part of our business and Kevin Chung, PhD, of AI Technology has written *High Temperature Stack-chip, Die-attach Adhesive Developments*, reviewing current offerings but pointing out that a new generation is needed. *IC Assembly and Test Market Poised for Growth in 2010* is the subject of Ron Molnar's article and it analyzes the current market and looks in detail at the Top 10 in the industry. This article is also a preamble to the extensive *Directory of IC Packaging Foundries*. Both Ron and the directory come to us from AZ Tech Direct, LLC.

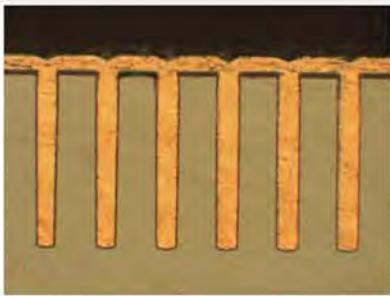
François von Trapp, contributing editor, offers us insight into how *Next-Gen Advanced Packages Spell Opportunity for Burn-in and Test Community*. Another regular is Sandra Winkler, contributing editor, who authors our Emerging Trends column. She writes on the *Economic Outlook for 2010*. Be sure to check out our *Industry News* and *What's New* pages for the latest in what is happening and a look at some new products.

I like spring. The sudden appearance of vivid colors after the winter drab is heartwarming and encouraging of the future. Unlike nature, for man-made things too much variety can be bad in terms of the cost. So let's look to where we can economize and if one design will do, why make two?

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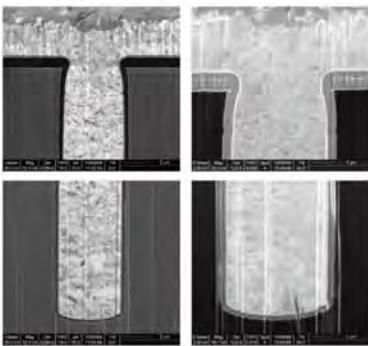
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INDUSTRY NEWS

Asia-Pacific Semiconductor Suppliers Defy the Downturn in 2009

"In a dismal year for the chip industry, suppliers based in Asia-Pacific managed to eke out some growth in 2009 as they focused on hot semiconductor products and capitalized on strong demand from the region," said Dale Ford, senior vice president, market intelligence services, for iSuppli. Two major semiconductor product segments escaped the downturn of 2009: LEDs and NAND flash memory. Only four of the Top 25 semiconductor suppliers were able to increase their

revenues in 2009. Three of the four companies that were able to grow are memory suppliers: Samsung, Hynix, and Elpida Memory. The hardest hit companies among the Top 25 suppliers were Sony Corp. and Freescale

Semiconductor Inc. with revenue declining by more than 30 percent during the year. To view the full report, visit <http://www.isuppli.com/News/Pages/Asia-Pacific-Semiconductor-Suppliers-Defy-the-Downturn-in-2009.aspx>

2008 Rank	2009 Rank	Region	2008 Revenue	2009 Revenue	Percent Change	Percent of Total	Cumulative Percentage
1	1	Asia/Pacific	126,200	119,511	-5.3%	52.0%	52.0%
2	2	Japan	55,426	43,957	-20.7%	19.1%	71.1%
3	3	Americas	39,283	35,167	-10.5%	15.3%	86.4%
4	4	Europe/EMEA	39,328	31,282	-20.5%	13.6%	100.0%
Total:			260,237	229,917	-11.7%	100.0%	

Source: iSuppli Corp. March 2010



Plasma-Therm Joins Fab Owners Association

Plasma-Therm, a global supplier of plasma process equipment, is pleased to announce it has recently joined the Fab Owners Association (FOA). Through quarterly meetings, FOA members work collaboratively to discuss problems and provide solutions on issues relevant to the semiconductor manufacturing industry. "Members like Plasma-Therm are extremely important to our trade association: They bring tomorrow's solutions to our device maker members today," said L.T. Guttadauro, Executive Director of the Fab Owners Association. "We are happy to have Plasma-Therm as one of our newest members." Through active membership participation, Plasma-Therm will provide industry insight of common practices and solutions to problems in dry etch and PECVD technologies. "The Fab Owners Association gives key

industry players a valuable forum to discuss relevant issues and share solutions that will benefit technological advancement in many different markets," said Abdul Lateef, CEO of Plasma-Therm. [www.plasmatherm.com]

International Recognition for Henkel

Henkel has been included in the list of the "World's Most Ethical Companies" for the third year in a row. The ranking, prepared by the US Ethisphere Institute, recognizes companies from around the globe for their exemplary ethical approach to corporate governance and their commitment to sustainable development. Henkel, headquartered in Düsseldorf,

Germany, was the only German company to make the list. The multistage assessment process was based on business conduct as demonstrated in a range of categories including social engagement, management style, and innovation strength.

"We are delighted to have received this international accolade," said company CEO, Kasper Rorsted. "Our commitment to sustainable development also serves to motivate our employees, enhancing their identification with the company and, through this, further contributing to our commercial success."

[www.henkel.com/sustainability]
[www.ethisphere.com]

Ellipsiz Named Distributor for Axus

Axus Technology, a supplier of custom CMP and wafer thinning solutions based in Chandler, AZ, USA, has named Ellipsiz, headquartered in Singapore, as their exclusive distributor for Singapore and Malaysia. "This is an important development for Axus Technology, as



Casper Rorsted



Barrie VanDevender

well as for our customers in Asia who we feel will benefit greatly from the direct and immediate support offered by a local distributor," said Barrie VanDevender, VP of Sales and Marketing for Axus.

"Ellipsiz brings the expertise and scale of operational network that are essential



Lim Beng Lam

to support our key production customers in the region," said Lim Beng Lam, Vice President of the Distribution & Services Solutions

Division of SGX mainboard-listed Ellipsiz Ltd. "Backed by Ellipsiz' team of skilled professionals throughout Asia, especially in Singapore and Malaysia, we are confident of extending Axus' presence in the region."

Commission Rules in Carsem's Favor

An Administrative Law Judge (ALJ) has issued a Supplemental Initial Determination (ID) in Carsem's on-going patent litigation with Amkor Technology in the U.S. International Trade



Peter Yates

Commission (ITC) in Washington, D.C., ITC Investigation No. 337-TA-501. Carsem of Ipoh, Malaysia, has received a "No Violation" decision in this case.

Following the Commission's Notice of Reversal and Remand that was issued in February this year, the ALJ has now determined that all of Amkor's asserted patent claims are invalid, not infringed, and/or not enforceable at the ITC, and that Carsem has not violated Section 337 of the Tariff Act by importing the MLP products Amkor had accused of infringement. Peter Yates, Carsem's Group Managing Director, stated, "We

are extremely pleased with the ALJ's latest determination and look forward to the Commission's final determination in July." [\[www.carsem.com\]](http://www.carsem.com)

Vi Technology Inc. Partners with Lewis and Clark

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Jean-Marc Peallat

the signature of a partnership with the American based company, Lewis and Clark, a prominent name in selling and servicing SMT second-hand equipment. Both Lewis and Clark and Vi Technology will extend their product offerings. Lewis and Clark will be able to service all Vi Technology's AOI and SPI equipment from installation and basic operation to advanced support. Vi Technology will integrate the unique Lewis and Clark experience of trading used equipment as new solution for customers.

"This partnership seals a long term collaboration between both companies," explained Jean-Marc Peallat, CEO, Vi Technology Inc. Adds Frank L. Clark, Jr., President/CEO, Lewis and Clark, "Our goal is to give Vi Technology's customers timely service as well as the opportunity to trade in unused assets toward new VIT equipment." [www.vitechnology.com] [www.lewis-clark.com]

Rudolph Technologies Partners in Europe

Rudolph Technologies, Inc., a provider of process characterization equipment and software for wafer fabs and advanced packaging facilities, recently announced that it has selected the John P. Kummer Group to distribute its probe card test and analysis (PCTA) products in Europe, significantly increasing the sales and support resources dedicated to PCTA systems in critical European markets. The move was made in anticipation of growing demand as the semiconductor manufacturing industry continues its recovery and manufacturers look for

new methods to reduce the cost and optimize the performance of their testing processes. "We are very pleased to be able to bring these resources to bear in our European operations," said Martin

Molan, general manager, Rudolph Technologies Europe. Rex Sandbach, director of Kummer UK adds, "We have 15 years of experience in this and related markets." [www.rudolphtech.com]



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Poster Sessions

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www.iwlpc.com



IC Assembly and Test Market Poised for Growth in 2010

The market and the Top 10 (11) players are analyzed

By Ron Molnar *[AZ Tech Direct, LLC]*

After dismal 2008 and 2009 performances, the semiconductor market and its subset, IC assembly and test, are poised for substantial growth in 2010. Bill McClean, President of IC Insights, a leading market research firm, reported at the recent Global Business Council meeting in Scottsdale, AZ, that the worldwide IC market is expected to grow 27% in 2010 to \$303 billion. The worldwide 2010 semiconductor market revenues are expected to eclipse the previous high achieved in 2007.

Semiconductor packaging has become a major differentiator of semiconductor products and a major factor in product performance. For some high performance applications, packaging, assembly, and test (PAT) now represents a significant portion of the IC product cost. For many hand-held consumer applications, advanced packaging in the form of chip-scale, leadless DFN or QFN plastic packages, and wafer-level packaging (WLP) enable the miniaturization demanded by consumers. To minimize capital expenditures and unit costs, and to achieve vital time-to-market product introductions, integrated device manufacturers (IDMs) are outsourcing more and more of their PAT manufacturing processes to semiconductor assembly and test services (SATS) companies around the world.

Fabless semiconductor companies have embraced the outsourcing model since the mid-1980s and now form a solid base of customers for the SATS industry. Over the last decade, they have grown their revenues 5-10x faster than IDMs and have captured nearly 25% of the global semiconductor market. Based on their 2009 revenues, the largest fabless IC companies are Qualcomm, AMD, Broadcom, MediaTek, Nvidia, Marvell, Xilinx, LSI Logic, and Altera. Each of them contract with one or more SATS companies for their IC packaging, assembly, and test needs.

2009 Rank	2008 Rank	Company	Headquarters Country	2008 Revenue (\$M)	2009 Revenue (\$M)	2009 Growth (%)
1	1	ASE	Taiwan	2,952	2,597	-12.0
2	2	Amkor Technology	United States	2,658	2,179	-18.0
3	3	SPIL	Taiwan	1,918	1,722	-10.2
4	4	STATS ChipPAC	Singapore	1,658	1,326	-20.0
5	5	Powertech Technology	Taiwan	994	982	-1.2
6	6	UTAC	Singapore	711	600	-15.6
7	7	ChipMOS Technologies	Taiwan	519	368	-29.1
8	11	JCET	China	349	342	-2.0
9	8	King Yuan Electronics	Taiwan	413	319	-22.8
10	9	Unisem	Malaysia	373	300	-19.6
Total Top 10				12,545	10,735	-14.4
Others				7,556	6,452	-14.6
Total Market				20.101	17,187	-14.5

Table 1. Top 10 SATS Companies' Revenues, 2009. (Source: Gartner, February 2010)

SATS Market

In April 2008 Chip Scale Review reported, "The outsourced assembly and test industry boasted two of its best years in 2006 and 2007, with several key players setting new records for income and revenue." However, this didn't last long, and the SATS industry suffered negative growth in both 2008 and 2009. Devastating quarterly declines were reported from the end of 2008 through early 2009. The U.S. stock market rebounded relatively sharply from its March 2009 lows due in large part to the unprecedented government actions and subsidies. Early forecasts predicted the SATS market would decline by as much as 30% in 2009, but it rebounded with the upturn in the economy.

The total SATS industry revenue of \$17.2 billion in 2009 actually declined only 14.5% from the \$20.1 billion in 2008 — considerably less than predicted. The SATS industry continues to rebound. Jim Walker, Research VP, Semiconductor Manufacturing, of Gartner/Dataquest states, "For 2010, the SATS industry will

experience growth of over 26% to \$21.6 billion, with a 5-year CAGR of 12.2%." He goes on to say, "Going forward, the SATS market should account for more than 50% of the IC assembly and test market by 2012." That's a major milestone for the SATS industry.

SATS Ranking

The top ten SATS companies accounted for approximately 62.5% of the total global SATS market revenue in 2009. The largest seven SATS companies of the Top 10 in the world retained their positions from 2008 to 2009 as reported by Gartner/Dataquest in their recent March 1, 2010, *Market Share Alert: Preliminary SATS Market Share, Worldwide, 2009 report* (**Table 1**).

Rounding out the last 3 positions of the Top 10 for 2009 are Jiangsu Changjiang Electronics Technology (JCET), King Yuan Electronics (KYEC), and Unisem. At No. 8, JCET is the first China-based company to achieve a Top 10 ranking. Carsem dropped from the Top 10 list in 2009 one spot to No. 11.

Billion Dollar Club

Industry giants ASE and Amkor continued their strong grasp on the top two positions in the ranking and remained the only two SATS providers with annual revenues eclipsing the \$2 billion threshold.

In 2009, Advanced Semiconductor Engineering (ASE) of Taiwan again ranked first. "Like our industry peers, ASE did not go through 2009 unscathed. However, with a good cost structure in place we were able to manage a small growth on the net earnings, and recorded overall sales revenues of \$2.6 billion, maintaining our industry leadership position," said Rich Rice, ASE's Sr. Vice President, Sales, North America. He added, "In the past few years, ASE has made substantial progress in copper wire bond. Today, with gold prices fluctuating over \$1,000 per ounce, copper is a huge cost advantage when considering gold is the single largest cost factor in most wire bond package types. Through dedicated investment we now have over 1,500 copper wire bonders installed in multiple factories serving over 50 customers in volume production."



Figure 1. Copper wire bond line at ASE's Kaohsiung assembly facility (Source: ASE)

In 2009, Amkor shipped nearly 7.7 billion packages, which is over 5% of the world's total IC units sold. Amkor agreed to form a new assembly and test joint venture with Nakaya Microdevices and Toshiba in Japan to be called J-Devices. Amkor also was honored in 2009 with Frost & Sullivan's Technology Innovation of the Year award for their line-up of new package technologies: FusionQuad, through-mold via (TMV), package-on-package (PoP), and flip-chip molded BGA.

Siliconware Precision Industries Ltd. (SPIL), specializing in high-end ball grid array packages and flip-chip solutions, maintained its No. 3 position in the SATS

industry. A breakdown by package type of SPIL's 4Q09 net revenues showed 45% from substrate-based packages, 28% from leadframe-based packages, 17% from bumping and flip-chip BGA packages, 8% from testing, and 2% from other sources. Last month SPIL announced an agreement to sell its DRAM testers and LCD driver assembly and test operation lines to ChipMOS Technologies.

In 2009, STATS ChipPAC finished again in the No. 4 position. Compared to SPIL, they derived 57.9% of their 2009 net revenues from substrate-based packages, 15.1% from leadframe-based packages, and 27.0% from test and other sources. Their top 10 customers in 2009 accounted for 71.8% of net revenues. Last November, STATS ChipPAC announced that it had successfully demonstrated the reliability of its first generation, embedded wafer-level ball grid array (eWLB) technology and ramped into high volume production. The next generation is under development with its partners, STMicroelectronics and Infineon, for product offerings targeted to start in 2010.

Half Billion Dollar Club

SATS providers that focused heavily on memory assembly and test did not fare so well in 2009, as witnessed by the 29.1% decline in ChipMOS Technologies revenues. Early evidence points to a surging DRAM market in 2010 which should lift ChipMOS revenues back over the \$500 million threshold. Oddly, Powertech Technologies (PTI) was the best year-over-year performer in 2009 with only a 1.2% decline in revenue. PTI's production agreements with Kingston Technology certainly helped prevent a major decline like that felt by others focused on the memory segment. PTI, UTAC, and ChipMOS retained their respective 2008 rankings.

United Test and Assembly Center (UTAC) Group, noted primarily for its test services, retained its No. 6 position. UTAC Group recently expanded their manufacturing presence by acquiring ASAT Ltd., adding a southern China facility to complement their other manufacturing sites in Singapore, Taiwan, and Thailand. This new acquisition has since been renamed UTAC Dongguan

Ltd. In 2004, only 6 years ago, ASAT Ltd. ranked as the 10th largest SATS company in the world.



Figure 2. UTAC Dongguan Ltd. manufacturing facility (Source: UTAC Group)

Rest of the Top 10

JCET is the first China-based SATS provider to advance into the Top 10 ranking, settling in the No. 8 position for 2009. Focused mainly on low leadcount, discrete assembly and test, JCET has annual capacity of more than 25 billion discrete units, and 5 billion IC units. The company was founded in 1972 and went public in 2000.

King Yuan Electronics Co., Ltd. (KYEC), founded in 1987, is one of the world's largest providers of integrated circuit test development engineering, wafer probing, pre-assembly (wafer thinning and dicing), and final test. While offering no assembly services, KYEC held onto the No. 9 position for 2009.

Unisem (M) Sdn. Bhd., headquartered in Malaysia, rounds out the Top 10 list in 2009. Unisem extended its range of plastic package offerings in July 2009 when it entered into a cross-licensing agreement with ASAT, Ltd. (now part of the UTAC Group). Included in the agreement were Unisem's etched leadless package (ELP), taped leadframe package (TLP) and ASAT's thin array plastic package (TAPP), and thermal leadless array (TLA) package.



Figure 3. Carsem post-saw MLP package pick-and-place line (Source: Carsem)

Honorable Mention

Carsem (M) Sdn. Bhd. slipped from the Top 10 list in 2009, but deserves honorable mention. Carsem, like JCET, offers both assembly and test of a wide range of IC packages, but predominantly lower leadcount, plastic packages. In October 2009 they introduced an extremely thin micro leadframe package (MLP) having two leads and measuring only 0.6 x 0.3 x 0.3 mm (similar in size to 0201 surface mount components). This tiny package was developed for thermal voltage suppression diode applications.

Packaging Foundry Directory

The 2010 directory of worldwide IC packaging foundries, compiled this year by AZ Tech Direct, LLC, lists 61 companies offering IC assembly and test services. It expands from 38 listings in the 2009 directory and includes 26 companies headquartered in the U.S. alone.

Many of the U.S.-based companies are small and service their geographic regions of the country, offering quick turn assembly of prototypes and preproduction volumes. Their ability to quickly assemble new IC designs in 1 to 5 days for characterization and testing is invaluable to IC designers. In general, they are capable of assembling cavity packages, such as hermetic or epoxy-sealed ceramic packages and/or liquid epoxy encapsulated (glob top) plastic packages. Most provide wire bond and/or flip-chip assembly processes. Only a few of the larger SATS suppliers in the U.S. offer transfer molded encapsulation due to the sizeable investment required for presses, molds and trim/form die sets to cover the broad range of package types. It comes as no surprise that more and more domestic suppliers are planning to establish molding capacity to offer the increasingly popular leadless DFN and QFN packages. These relatively new package types can be assembled on pre-plated, etched leadframes, transfer molded in an array, singulated with dicing saws, and don't require dedicated trim/form tooling or a lead finish plating line.

The focus of this directory has been, and continues to be, on those SATS providers offering primarily the assembly of discrete

diodes/transistors and integrated circuits in single-chip, JEDEC-standard packages. As a result, companies offering primarily contract test services, other than KYEC which ranks as one of the Top 10 SATS companies in the world, have been excluded. Also, those companies mainly engaged in assembly of traditional hybrids, multichip modules, chip-on-board (COB)

modules, system-in-package (SiP), MEMS/MOEMS, high power packages, optoelectronics including light emitting diode (LED), packages and assemblies have also been excluded from this directory.

To update listings in the directory for next year's publication, please contact the author at surveys@aztechdirect.com before January 31, 2011.⁸⁸

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INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Memory Card	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Advanced Semiconductor Engineering, Inc. No. 26, Chin 3rd Rd., N.E.P.Z. Kaohsiung, Taiwan R.O.C. Tel: +886-7-361-7131 www.aseglobal.com	JP(1), KR(1) MY(1), SG(1) TW(2), US(1)	PB, PL, PN	SD, BP, WP WD, WT AS, FT FT, BI	AD WB, FC MP, UF LP, BA
Advotech Co., Inc. 632 W. 24th Street Tempe, AZ 85282 Tel: +1-480-821-5000 www.advotech.com	US(1)	CB, CL, CN PC	SD, BP WD, AS FT	AD, ED WB, FC GT, UF BA, HS
Amkor Technology Inc. 1900 S. Price Road Chandler, AZ 85286 Tel: +1-480-821-5000 www.amkor.com	CN(2), JP(1) KR(3), PH(2) TW(3), SG(2) US(1)	CB, CL, CN PB, PL, PN	SD, BP WD, WT AS, FT ET	AD, ED WB, FC MP, UF, GT LP, BA HS
AmTECH Microelectronics, Inc. 6541 Via Del Oro San Jose, CA 95119 Tel: +1-408-227-8885 www.amtechmicro.com	US(1)	CL, CN PL, PN	SD, WD AS ET	AD, ED WB, GT BA, HS
Aspen Technologies 5050 List Drive, Suite C Colorado Springs, CO 80919 Tel: +1-719-592-9100 www.aspentechnologies.net	US(1)	CB, CL, CN PC	SD BP, WD AS	AD, ED WB, FC GT, UF BA, HS
Azimuth Industrial Co., Inc. 30593 Union City Blvd., Suite 110 Union City, CA 94587 Tel: +1-510-441-6000 www.azimuthsemi.com	US(1)	CL, CN PL, PN	WD, AS	AD, ED WB, MP LP, HS
Carsem (M) Sdn. Bhd. Jalan Lapangan Terbang, P.O. Box 204 30720 Ipoh, Perak, Malaysia Tel: +60-5-312-3333 www.carsem.com	CN(1), MY(2)	CB, CN PB, PL, PN	SD, WP WD, WT AS, FT EI	AD, ED WB, FC MP, UF LP, BA HS
Catalyst Microtech LLC 5321 Industrial Oaks Blvd., Suite 105 Austin, TX 78735 Tel: +1-512-899-8422 www.catalystmicrotech.com	US(1)	CB, CL, CN PC	WD, AS	AD, ED WB, FC GT, UF BA, HS
Chipbond Technology Corporation No. 3, Li Hsin 5th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C. Tel: +886-3-567-8788 www.chipbond.com.tw	TW(2)	PF	SD BP, WP WD, WT AS, FT ET	AD, FC GT, UF
ChipMOS Taiwan No. 1, R&D Rd. 1, Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C. Tel: +886-3-577-0055 www.chipmos.com	CN(1), TW(2)	PB, PL, PN PF	SD, BP WD, WT AS, ET	AD, WB FC, UF GT, MP LP, BA
Chip Supply, Inc. 7725 N. Orange Blossom Trail Orlando, FL 32810 Tel: +1-407-298-7100 www.chipsupply.com	US(1)	CB, CL, CN PB, PN, PC, PF WL	SD BP, WP WD, WT AS, FT ET, BI	AD, ED WB, FC GT, UF MP, BA HS
Circuit Electronic Industries Public Co., Ltd. 45 Moo 12 Rojana Industrial Park Ayutthaya, Thailand 13210 Tel: +66-35-226-280 www.cei.co.th	TH(1)	PL, PN PF	SD WD, WT AS, FT ET	AD WB MP LP

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Cirtek Electronics Corporation 116 E. Main Ave., Phase V, SEZ, Laguna Technopark, Binan Laguna, Philippines Tel: +63-49-541-2310 www.cirtek-electronics.com	PH(1)	PL, PN	SD, WP WD, WT AS, FT ET	AD, WB MP, LP HS
Colorado Microcircuits, Inc. 6650 N. Harrison Avenue Loveland, CO 80538 Tel: +1-970-663-4145 www.coloradomicrocircuits.com	US(1)	CB, CL, CN PN, PC	SD WD AS	AD, ED WB, GT MP, HS
Corwil Technology Corporation 1635 McCarthy Blvd. Milpitas, CA 95035 Tel: +1-408-321-6404 www.corwil.com	US(1)	CB, CL, CN PB, PL, PN PC	SD BP, WP WD, WT AS, FT ET, BI	AD, ED WB, FC GT, UF MP, BA HS
EEMS Italia SpA. Viale delle Scienze, 5 02015 Cittaducale Rieti, Italy Tel: +39-07-466-041 ? www.eems.com	CN(1), IT(1) SG(1)	PB, PL, PN	SD, WP WD, WT AS, FT	AD, WB MP, LP BA
Endicott Interconnect Technologies, Inc. Building 258, 1093 Clark Street Endicott, NY 13760 Tel: +1-866-820-4820 www.endicottinterconnect.com	US(1)	PC	SD WD ?, WT ? AS	AD, WB FC, UF GT, BA
Engent, Inc. 3140 Northwoods Pkwy., Suite 300A Norcross, GA 30071 Tel: +1-678-990-3320 www.engentaat.com	US(1)	PB, PN PC	SD, BP WD, WT AS, FT ETT	AD, WB FC, UF GT, MP BAP
First Level Inc. 3109 Espresso Way York, PA 17402 Tel: +1-717-266-2450 www.firstlevelinc.com	US(1)	CL ?, CN ? PC	SD BP WD AS	AD, ED WB, FC GT, UF BA, LA HS
Formosa Advanced Technologies Co., Ltd. No. 329, Ho-Nan St., Touliu, 640 Yunlin, Taiwan R.O.C. Tel: +886-5-557-4888 www.fatc.com.tw	TW(1)	PB, PL	SD, WP WD, WT AS, FT BI	AD, WB MP, LP BA
Greatek Electronics, Inc. No. 136, Gung-Yi Rd., Chunan Cheng, Miaoli Hsien, Taiwan R.O.C. Tel: +886-37-638-568 www.greatek.com.tw	TW(2)	PL, PN	SD, WP WD, WT AS, FT BI	AD, WB MP, LP BA
HANA Semiconductor (Ayutthaya) Co., Ltd. Hi-Tech Industrial Estate Authority of Thailand, 100 Moo 1, T. Baan-Len, A. Bang Pa-In KM. 59 Asia Road, Ayutthaya 13160, Thailand Tel: +66-35-729-300 www.hanagroup.com	CN(1) TH(2) US(1)	PL, PN PF	SD WD, WT AS, FT ET	AD WB, GT MP, LP
HEI, Inc. 1495 Steiger Lake Lane Victoria, MN 55386 Tel: +1-952-443-2500 www.heii.com	US(3)	CN PB PN PF	SD WD AS	AD, WB FT, UF MP, BA
i2a Technologies 3399 W. Warren Avenue Fremont, CA 94538 Tel: +1-510-770-0322 www.ipac.com	US(1)	PB, PL, PN PC	AS	AD, ED WB, GT BA

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IDS Electronics Sdn. Bhd. IDS Park, Seri Iskandar, Bota, Perak, Malaysia Tel: +60-5-371-2288 www.idsesb.com.my	MY(1)	PL PN	WP WD, WT AS, FT ET	AD, WB MP, LP
Infiniti Solutions Ltd. 122, Middle Road, Midlink Plaza #04-01 Singapore 188973 Tel: +65-6336-0082 www.infinitisolutions.com	PH(1) US(1)	CL, CN PL, PN	SD, WP WD, WT AS, FT	AD, ED, WB MP, LP HS
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	US(2) MX(1)	PC, PF	SD AS	AD, WB FC, UF GT
Jiangsu Changjiang Electronics Technology Co., Ltd. No. 275, Binjiang Rd., Middle Jiangyin, Jiangsu, China Tel: +86-0510-8685-6417 www.cj-elec.com	CN(3)	PL, PN	WD, WT AS, FT	AD, WB MP, LP
Kingpak Technology Inc. No. 84, Tai-ho Rd., Chu-Pei 302, Hsin-chu Hsien, Taiwan R.O.C. Tel: +886-3-553-5888 www.kingpak.com.tw	TW(1) CN(1)	PB, PN MC	SD WP, WD, WT AS, FT	AD, WB GT, MP BA
King Yuan Electronics Co., Ltd. No. 81, Sec. 2, Gongdaowu Road Hsin-chu 300, Taiwan Tel: +886-3-575-1888 www.kyec.com.tw	TW(4)	n/a	WP, WD, WT FT, BI	n/a
Kyocera America Inc. 8611 Balboa Avenue San Diego, CA 92123 Tel: +1-858-576-2600 http://americas.kyocera.com/kai/semparts	US(1)	CB, CL, CN PB, PL	SD WD, WT AS, ET	AD, ED WB, FC UF, GT LP, BA HS
Lingsen Precision Industries Ltd. 5-1, Nan 2nd Road, T.E.P.Z. Taichung 42701 Taiwan R.O.C. Tel: +886-4-2533-5120 www.lingsen.com.tw	TW(2)	PB, PL, PN MC	SD, WP WD, WT AS, FT ET	AD, WB MP, LP BA
Majelac Technologies, Inc. 262 Bodley Road Aston, PA 19014 Tel: +1-610-459-8786 www.majelac.com	US(1)	CL, CN PB, PL, PN PC	SD WD AS	AD WB, FC GT, MP, UF BA, HS
Maxtek Components Corporation 2905 SW Hocken Avenue Beaverton, OR 97005 Tel: +1-503-627-4521 www.maxtek.com	US(3)	CL, CN PB	SD WP, WD AS, FT ET, BI	AD, ED WB, FC MP, UF BA, HS
Millenium Microtech Group 17/2 Moo 18, Suwintawong Rd., Tambon Saladang Bannumprielu, Chachergsao 24000, Thailand Tel: +66-38-845-530 www.m-microtech.com	TH(1) CN(1)	CL, CN PL	SD, WP WD, WT AS, FT ET, BI	AD, ED WB, MP LP, HS
Optocap, Ltd. 5 Bain Square Livingston, Scotland, UK EH54 7DQ Tel: +44-1506-403-550 www.optocap.com	UK(1)	CL, CN	SD, WD AS, ET	AD, ED WB, FC GT, UF, MP BA, HS

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Orient Semiconductor Electronics No. 9, Central 3rd Street, N.E.P.Z., Kaohsiung 811 Taiwan R.O.C. Tel: +886-7-361-3131 www.ose.com.tw	TW(1) PH(1)	PB PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB FC, UF MP, LP
Pantronix Corporation 2710 Lakeview Court Fremont, CA 94538 Tel: +1-510-656-5898 www.pantronix.com	CN(1) PH(2) US(1)	CL, CN PB, PL, PN PC	SD WD, WT AS, FT ET	AD, ED WB, MP FC, UF LP, BA HS
Powertech Technology Inc. No. 26, Datong Rd., Hsinchu Industrial Park, Hukou, Hsinchu 30352 Taiwan R.O.C. Tel: +886-3-598-0300 www.pti.com.tw	CN(1) TW(3)	PB, MC PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB MP, LP BA
Promex Industries, Inc. 3075 Oakmead Village Drive Santa Clara, CA 95051 Tel: +1-408-496-0222 www.promex-ind.com	US(1)	CL, CN PL, PN PC	SD, WD AS, ET	AD, ED WB, MP FC, UF GT, HS
Psi Technologies, Inc. Electronics Ave., FTI Special Economic Zone, Taguig Metro Manila, Philippines Tel: +63-2-838-4966 www.psitechologies.com	PH(2)	CL, CN PL, PN	SD, WD AS, FT ET	AD, ED WB, MP LP, HS
Quik-Pak 10987 Via Frontera San Diego, CA 92127 Tel: +1-858-674-4676 www.icproto.com	US(1)	CL, CN PB, PL, PN PC, PF	WD, WT AS, ET	AD, ED WB, GT FC, UF BA
Semi-Pac Inc. 1206 #F Mt. View Alviso Road Sunnyvale, CA 94089 Tel: +1-408-734-3832 www.semipac.com	US(1)	CL, CN PC	WD AS	AD, WB GT, HS
Signetics Corporation 483-3 Buphung-ri, Thanhun-myun, Paju-si Gyungki-do, Korea 413-840 Tel: +82-31-940-7660 www.signetics.com	KR(2)	CB, PB PL, PN	SD, WP WD, WT AS, FT ET	AD, WB FC, UF MP, LP BA
Sigurd Microelectronics Company No. 436, Sec. 1, Pei-Shing Rd., Chu-Tung Hsin-chu, Taiwan R.O.C. Tel: +886-3-595-9213 www.sigurd.com.tw	CN(1) TW(3)	CN PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB MP, LP
Silicon Turnkey Systems 801 Buckeye Court Milpitas, CA 95035 Tel: +1-408-432-1790 www.siliconturnkey.com	US(1)	CL, CN PC	WP, WD AS, FT ET, BI	AD, ED WB, FC GT, UF HS
Siliconware Precision Industries Co., Ltd. No. 123, Sec. 3, Da Fong Rd., Tan tzu, Taichung 427, Taiwan R.O.C. Tel: +886-4-2534-1525 www.spil.com.tw	CN(1) TW(3)	CN PB, PL, PN PF WL	SD, BP WP WD, WT AS, FT ET	AD WB, FC MP, UF LP, BA
Solitron Devices, Inc. 3301 Electronics Way West Palm Beach, FL 33407 Tel: +1-561-848-4311 www.solitrondevices.com	US(1)	CN PL, PN	SD, WD AS, FT ET	AD, ED WB, MP HS

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Economic Outlook 2010

By Sandra Winkler, Contributing Editor
slwinkler@newventureresearch.com

According to the Chinese calendar 2010 is a tiger year, and certainly, by comparison to 2009, the year will roar ahead. IC revenue is expected to grow at 18.8% and unit growth at 18% in 2010, considerably better than the 8.8% decline in revenue and 6.9% decline in units in 2009.

What's Hot in ICs

DRAMs are anticipated to be the largest growth area for ICs with 40% revenue growth in 2010. Numerous analog chips including regulators and references, computer, communications, automotive, and industrial applications; special purpose logic chips including consumer, computer, communications, and automotive; flash, EEPROM, 32-bit MCU, standard cell, and PLD chips will all see revenue growth rates in excess of 15%.

Why the Upturn?

Low interest rates, low oil prices, and the stimulus packages that were instituted around the world are all contributing to a stabilizing economy and upturn. Purchases were less than the replacement market in 2009, and pent up demand is pulling the market in a positive direction.

Cell phones, particularly the high-end smartphones, will see high growth rates. Smartphones are gaining in popularity and are becoming a larger piece of the cell phone pie. Anything handheld and somewhat affordable that keeps us connected to the rest of the world seems to be doing well. New product introductions such as Apple's iPhone and iPad are becoming hot topics, and the Blackberry by Research in Motion (RIM) has been doing well for some time.

Netbook computers, with prices as low as \$200 during holiday sales, and notebook computers are quite popular. Other high growth areas include 3D and digital TVs, DSL/cable modems, flash drives, memory cards, set top boxes, digital cameras, automotive, and an assortment of audio applications.

The economy is stabilizing, which is easing fears of spending on consumer goods. The housing market, which took down the economy by taking the credit markets down with it, is stabilizing, and the ratio of income to housing expenditure is more balanced than it was previously. The automotive market, which is host for numerous ICs, had fallen substantially during the downturn. This market did benefit from the cash-for-clunkers program and, although automotive sales fell back after the program ended, it became a booster to spending. Automotive is expected to turn up in 2010 and beyond, particularly in places such as China. Overall, spending is higher now than it was in the depths of 2009. And that is what is pulling this year of the tiger up and out of the sloth of 2009, and will carry us to a more positive future. ☺



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State-of-the-art and Trends in 3D Integration

Making good progress, but major challenges still lie ahead

By John H. Lau [Industrial Technology Research Institute, Taiwan, ROC]

3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration. They are different and in general the TSV (through-silicon via) separates 3D IC packaging from 3D IC integration and 3D Si integration since the latter two use TSV but 3D IC packaging does not. TSV for 3D integration is a more-than-26-year-old technology. Even the coplanar GaAs RF MMIC (monolithic microwave integrated circuit) used via hole grounding technology in 1975 (35 years ago), but it was not for 3D integration. In this investigation, TSV (with a new concept that every chip could have two active surfaces) is the focus. State-of-the-art, key differences, trends of these three technologies, and a 3D integration roadmap are presented.

3D IC Packaging Technology

3D IC packaging consists of two or more conventional components (packages) stacked in the vertical direction. The most common is 3D memory stacking (Figure 1).

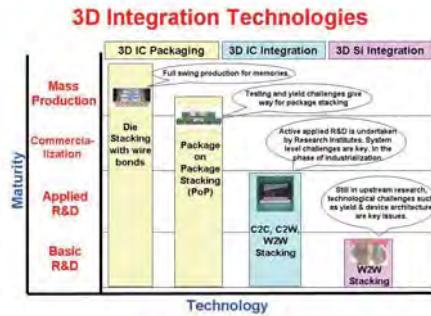


Figure 1. 3D Integration Technologies versus Maturity

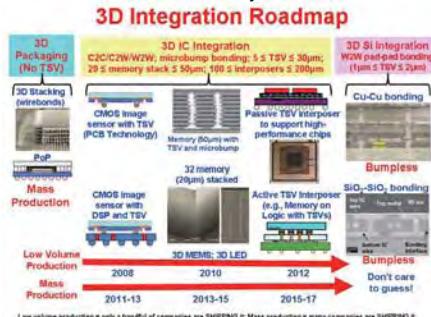


Figure 2. 3D Integration Roadmap

and Figure 2) by stacking memory chips with wire bonds and die attachments. Today, 28-chip memory stacking is not uncommon. Package-on-package (PoP), such as a flip-chip with solder bumps attached to a substrate which is supporting two stacked chips with wire bonds, is shown in Figure 2. 3D memory stacking and PoP are mature technologies in high volume production (Figure 1 and Figure 2)^{1,2} and will not be discussed.

3D IC Integration Technology

As shown in Figure 3, while they are different, both 3D IC integration and 3D Si integration are more-than-Moore technologies.

FEOL (Front End of Line) is usually performed in semiconductor fabrication plants (commonly called fabs) to pattern active devices such as transistors. The process is from a bare wafer to passivation, which covers everything except the bonding pads for the next level of interconnects.

BEOL (Back End of Line) is usually performed in packaging assembly and test houses and it involves everything after passivation, for example, UBM (under bump metallurgy), wire bonding, metallization, wafer bumping, backgrinding, dicing, assembly, and testing right before PCB assembly.

MEOL (Mid-End of Line) is performed by combining some of the FEOL and BEOL technologies into a 3D IC integration technology which involves, for example, TSV, microbumps, thin-wafer handling, metallization, UBM, wafer bumping, backgrinding, dicing, assembly, and testing. Thus, 3D IC integration must be executed in the fabs and packaging assembly and test houses. However, since the fabs' equipment and personnel are too expensive for making 3D IC integration and final test right before the printed circuit board (PCB) assembly (which are not their core competence or major business), eventually

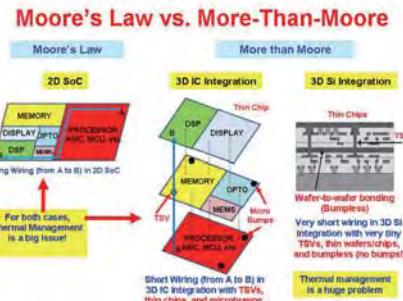


Figure 3. Moore's law versus more-than-Moore

(when there are volumes) the packaging assembly and test houses will do it all.

The Holy Grail of 3D IC integration (heterogeneous integration) is shown in Figure 3, where some of the chips, for example, microdisplay, microelectromechanical systems (MEMS), opto, memory, microprocessor, optoelectronic, multiple output dc-dc converter, application specific IC (ASIC), microcontroller unit (MCU), digital signal processor (DSP), microbattery, and analog-to-digital (A/D) mixed signal are combined and stacked in three dimensions. Two examples are shown in Figure 2. Eight memory chips, each 50µm thick, are stacked with microbumps and TSVs. Thirty two chips, each 20µm thick, are stacked in a chip from Samsung. Usually the electrical performance of 3D IC integration is better than that of 2D SoC (system-on-chip) as shown in Figure 3. However, there are major challenges in this quest.

Just as with many other new technologies, 3D IC integration still faces many critical issues^{1,2}:

- Known good dice (KGDs) are required.
- Design guidelines and software are not available.
- Test methods and equipment are lacking.
- TSV with redistribution layers (RDL) are usually required.
- Microbumps are usually required.
- Wafer thinning and thin wafer handling during processing are necessary.
- High equipment accuracy is necessary for alignments.

- Fast chips must be mixed with slow chips.
- Large chips must be mixed with small chips.
- 3D IC stacking inspection methodology is needed.
- 3D IC stacking expertise is lacking.
- 3D IC stacking infrastructure is lacking.
- 3D IC stacking standards are lacking.
- Thermal issue - the heat flux generated by stacked multifunctional chips in miniature packages is extremely high.
- Thermal issue - 3D circuits increase total power generated per unit surface area.
- Thermal issue - chips in a 3D stack may overheat if proper and adequate cooling is not provided.
- Thermal issue - the space between the 3D stack may be too small for cooling channels (no gap for fluid flow).
- Thermal issue - thin chips may create extreme conditions for on-chip hot spots.

Key enabling technologies for 3D IC integration are TSV w/o RDL, thin wafer strengthening and handling, microbumps, and thermal management. Design, test, reliability, and cost are always important but they are out of the scope of this study.

TSV w/o RDL

The most important key enabling technology for 3D IC integration is TSV w/o RDL. It provides advanced vertical interconnects and system-in-package (SiP) solutions such as C2C (chip-to-chip), C2W (chip-to-wafer), and W2W (wafer-to-wafer) stacking; wafer-level packaging and redistribution; interposer packaging; and the shortest electrical path (vertical-electrical feed-through) and lowest signal loss between two sides of a silicon interposer (either passive or active).

3D IC Integration of Memory and CPU (an active Si interposer)

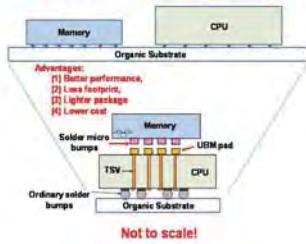


Figure 4. With TSV, every chip could have two active sides

Unlike 3D IC packaging which put, for example, wire bonds, solder bumps, gold stud bumps or anisotropic conductive adhesives on the bonding pads of the passivation wafer made by the FEOL, the first thing which the 3D IC integration (MEOL) does is to “dig” holes (TSVs) through the passivation and between the devices/circuits of the wafer. This is novel, which opens up the doors for many new and useful applications. For example, a memory can use a CPU as its active interposer (Figure 4). A MEMS device can be integrated with an ASIC chip¹ and LED devices can be mounted on an active chip¹, all of which can be assembled into a 3D structure. All of these are in the 3D IC integration roadmap (Figure 2) and their advantages are better performance, smaller form factor, less footprint, lighter weight, and potentially lower cost.

It should be pointed out and emphasized that a few years ago, once the (active) front-side of a chip was flipped on a substrate or PCB, there was nothing that could be done on its backside except attaching a heat spreader/sink. With TSVs, there is no distinction of front-side and backside anymore, which implies that a chip can have both top and bottom sides with circuits (Figure 4). This opens the doors wide for many innovative applications.

3D IC Packaging versus 3D IC Integration

The biggest difference between 3D IC integration and 3D IC packaging is that 3D IC integration utilizes the TSV to connect chips in the vertical direction while the 3D packaging does not. The advantages of 3D IC integration over 3D packaging are smaller footprint, smaller form factor, less weight, higher performance, less power, and potentially lower cost. These are key goals for system houses. Some of the challenges (opportunities) facing 3D IC integration are high-yield TSV w/o RDL fabrication, thin chip/wafer strengthening/handling, microbumps, thermal management, inspection and testing, cost reduction, and reliability. Of course, design and characterization are always important.

3D Si Integration Technology

3D Si integration is one of the more-than-Moore technologies and is a very old idea^{3,4,5}. It consists of two or more

Three Ways to Get Control Over Your Burn-In and Test Costs:

layers of active electronic components integrated vertically through TSV (it used to be called vertical interconnection) into a single circuit. It was triggered by the advance of silicon-on-insulator (SOI) technology, first reported by Gat and his colleagues more than 30 years ago, when semiconductor people thought Moore's law could be hitting the wall by the 1990s. Of course, the facts show that it did not.

3D IC Integration versus 3D Si Integration

The biggest difference between 3D IC integration and 3D Si integration is that the latter does not use bumps (bumpless), such as Cu, solder, or Au, or conductive adhesive to bond/connect two wafers together (**Figure 2** and **Figure 3**). There is no (or infinitesimal) gap between wafers and thermal management can be a very big problem. In addition, W2W is the only way to perform the bonding operation. Unlike 3D IC integration, which utilizes C2C, C2W, or W2W bonding methods, the yield is a big issue (some bad chips are assembled on good chips). Furthermore, TSV size for 3D Si integration is much smaller (~1μm and eventually sub-micron, see **Figure 2**) and thus the TSV manufacturing yields are lower.

Finally, the bonding condition requirements for 3D Si integration such as surface cleanliness, surface flatness, and the class of clean room (which heavily affects the yield) are much tougher than those for

3D IC integration (**Table 1**). There are two different W2W bonding methods for 3D Si integration, Cu-to-Cu⁴ and oxide-to-oxide⁵ as shown in **Figure 5** and **Figure 6** respectively.

The advantages of 3D Si integration over 3D IC integration are better electrical performance, less power, lower profile, less weight, and potentially lower cost. The thermal management of 3D Si integration is much tougher than that of 3D IC integration. Semiconductor personnel have been trying 3D Si integration for more than 25 years and there is no volume production in sight in the next 10.

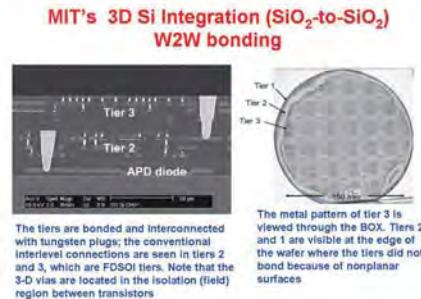


Figure 6. MIT's W2W (SiO₂-SiO₂) bonding

TSV Process Flow

There are many TSV processes, for example, via first, via last, and via middle. The most likely manufacturing process used by the industry for making TSV w/o RDL for 3D IC integration is shown in **Figure 7**. There are five key steps to making the TSV:

1. Via formation by either deep reactive ion etch (DRIE) or laser drilling
2. SiO₂ deposition by either thermal oxidation for passive interposers or PECVD (plasma enhanced chemical vapor deposition)
3. Barrier and seed layer deposition by physical vapor deposition (PVD) or electrografting (eG)
4. Cu plating or W (tungsten) sputtering to fill the vias
5. CMP (chemical and mechanical polishing) of Cu plating residues (overburden)

For bare wafers and passive interposers, a SiO₂ layer is needed before the photoresist. For active chips (for example, ASICs and processors) and active interposers, because of their passivation layer, only cleaning is needed. Next, the front-side metallization/

UBM is made on the blind TSV wafer, which is usually thicker than 300μm.

In most 3D IC integration applications, the thickness of the passive/active interposers ranges from 100μm to 200μm and of the stacked memory chips, from 20μm to 50μm. Thus, most of the TSVs fabricated are blind vias and a support wafer (carrier) is needed for the remaining processes.

Once the carrier is temporarily bonded to the blind TSV wafer, it can be thinned down to expose the TSV. Next are, for example, backside metallization/UBM and wafer bumping. Then the carrier is debonded from the TSV w/o RDL wafer. Finally, the TSV wafer is ready for either W2W bonding (recommended only for very high chip yield wafers or one of them is not an active wafer, for example, the cap wafer for MEMS or the lens wafer for LED applications) or diced into individual chips for C2C or C2W bonding.

The TSV size should be as small as possible (≤30μm) because of less thermal expansion mismatch between the Si (thermal expansion coefficient (TEC) = 2.5x10⁻⁶/°C) and Cu (TEC = 18.5x10⁻⁶/°C)¹, less Cu plating, higher throughput, and more space for routing. 5μm to 10μm vias for 3D IC integration are not uncommon.

As of today, the only 3D IC integration volume product (CMOS image sensor with TSV) is not using expensive "semiconductor" equipment such as the DRIE, PECVD, PVD, or CMP, but low-cost PCB technology tools⁶. Beside CMOS image sensors, due to their simplicity, 3D MEMS¹ and 3D LED¹ are the most likely candidates for applying low-cost 3D IC integration technology. However, for high-performance memory stacking and passive/active interposers, the PCB technology may not be able to handle the large number, small size, and/or fine pitch of vias, and the

TSV 3D IC Integration Process Flow

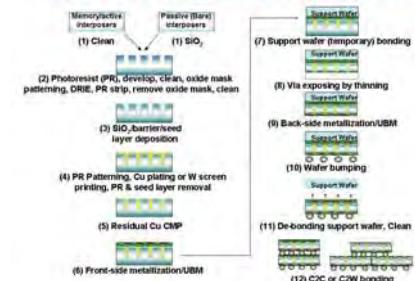


Figure 7. The most likely TSV manufacturing process

	Solder Microbump	Pad-to-pad (Bumpless)
Bonding Method	Thermal compression	Metal fusion bonding
Bonding Temperature	< 350 °C	> 350 °C (Room temperature bonding is far in the future)
Bump size	~ 8μm	< 5μm
Pitch	~ 15μm	< 10μm
Bonding Pressure	Medium	Very High
Surface Requirement	Surface pretreatment easy	Surface pretreatment to remove oxidation is very complicated. Also, surface roughness requirement is <1.0nm RMS
Applications	3D IC Integration	3D Si Integration
Cost	Low	High

Table 1. Solder microbump bonding versus bumpless bonding

IBM's 3D Si Integration (Cu-to-Cu W2W)

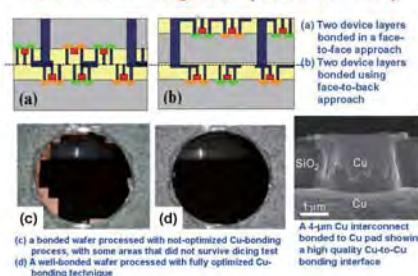


Figure 5. IBM's W2W (Cu-Cu) bonding

expensive “semiconductor” equipment is needed.

Critical Issues for TSV

As with many other new technologies, TSVs still face many critical issues. In the development of TSVs, the following must be noted and understood^{1,2}:

- Today, the only TSV 3D IC volume product is the CMOS image sensor made by the most simple PCB process⁶
- TSV cost is higher than that of wire bonding
- TSV design software is lacking
- TSV design guidelines are not commonly available.
- Copper filling helps on thermal problems but increases TCE (thermal coefficient of expansion)
- Void-free copper filling usually takes a long time (lower throughput)
- The TSV cost for poor-yield IC wafers is high because many TSVs are wasted on the bad dice
- There is a high cost for low TSV wafer manufacturing yield, especially for high-cost dice
- TSV wafer yields are high (>99.99%)
- Single-point touch-up on the TSV wafer is difficult
- TSVs with high aspect ratios are difficult to manufacture at high yield
- TSV wafer warpage is a problem owing to the TCE mismatch between silicon and copper
- Thin TSV wafer handling is necessary during all the processes
- Test methodology and software for TSV are lacking
- High-volume production tools are lacking and/or expensive
- TSV inspection methodology and software are lacking
- TSV expertise, infrastructure, and standards are lacking
- What are the cost-effective and reliable TSVs and for what IC devices?
- How large is the TSV market?
- What is the life cycle of TSV?

Figure 8 and **Figure 9** show a high performance chip which (cannot be supported by an organic bismaleimide triazene (BT)-substrate) is supported by a passive TSV interposer (Si-substrate) with

two redistribution layers on top and one at the bottom^{7,8}. A very simple BT-substrate is used to fan out all the I/Os, power, and ground to the PCB. The advance of semiconductor technology (because of Moore’s law) is many times faster than that of PCB, BT, and polyimide technologies, thus silicon is used as the substrate to reduce the cap. **Figure 9** shows the TSV with RDL wafer and the chip with its cross sections clearly showing the RDLs of the interposer^{7,8}. **Figure 8** (top) shows a 3D X-ray with computed tomographies (CT) reconstruction of the Cu-filled TSVs with seams/voids. After process improvements, **Figure 8** (bottom) shows a 3D X-ray with CT reconstruction of the Cu-filled, void-free TSVs. Thus, 3D X-ray is a powerful tool for nondestructive inspection of TSV. **Figure 10** shows a very high-performance Si memory chip attached to a microprocessor chip (active Si interposer) with 2400 TSVs on a 25µm pitch and the aspect ratio (thickness/via-diameter) AR = 200/15 = 13.3⁹.

In order to improve the TSV manufacturing yield and enhance the TSV quality, the requirements, tasks, and methods for each step are given in reference 1, where the hidden costs for 3D IC integration are also provided and discussed.

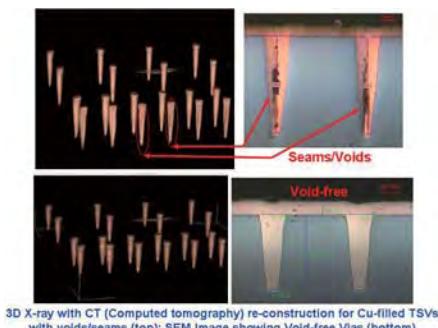


Figure 8. 3D X-ray with CT reconstruction for Cu-filled TSVs

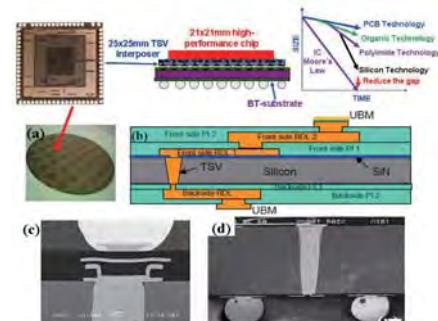


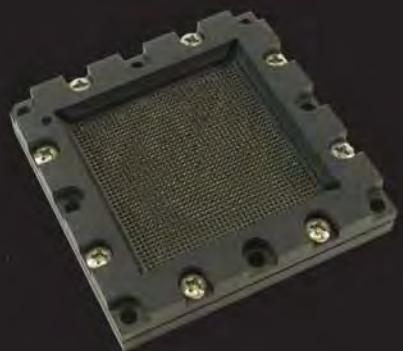
Figure 9. Cross sections of the TSV Si interposer

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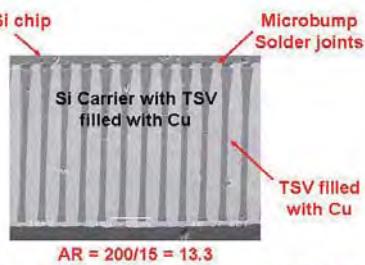


Figure 10. Cross section showing the high aspect ratio (13.3/1) TSV

Thin Wafer Handling

To have high performance, low profile, and lightweight products with 3D IC integration technology, the thickness of the chips/wafers is usually very thin. Making a wafer thin is not a big problem. Most of the back-grinding machines can do the job and grind the wafers to as thin as 5 μm . However, handling thin wafers through all the semiconductor fabrication and packaging assembly processes is difficult. Usually, the thin wafer is temporarily bonded on a support wafer. Then it goes through all the semiconductor fabrication processes such as metallization, passivation and UBM, and the packaging processes such as backgrinding and solder bumping. After all these, removing the thin wafer from the support wafer poses another big challenge. Two equipment groups are available for thin-wafer handling today, namely, 3M+SUSS and EVG+Brewer Science.

Figure 11 shows a very simple and low-cost support-wafer method for thin-wafer (50 μm) handling. In order to reduce the residual stress and remain crack-free during de-bonding, one must reduce the pitch of the release holes (1mm in diameter) on the perforated wafer to 2mm and increase the number of perforations on the edge of the

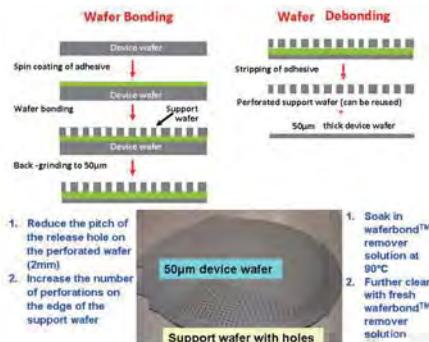


Figure 11. A low-cost, thin-wafer handling method

support wafer. These two optimized debonding methods allow more chemical solution to uniformly penetrate into the bonding adhesive and eventually debond the wafer successfully¹⁰.

Low-cost, Lead-free Solder Microbumps

For 3D IC integration, chips are very thin and thus conventional flip-chip solder bumps (~100 μm) cannot be used. Instead, very tiny bumps ($\leq 25\mu\text{m}$) are needed. **Figure 12** shows lead-free Sn bumps (on a high-performance memory chip), Ni-Au UBM (on a logic chip) formation, and their assembly. The lead-free solder joints are on an 8 μm pad, 15 μm pitch, and 16 μm standoff height¹¹.

Underfill is usually needed between two chips (one with Cu-filled TSVs and the other without) because of thermal expansion mismatch (the equivalent TCE of a Cu-filled TSV silicon chip could be as high as $10 \times 10^{-6}/^\circ\text{C}$ ¹). Due to the very tiny gap between the chips, underfills with small filler sizes (maximum $\leq 3\mu\text{m}$, average $\leq 0.5\mu\text{m}$) are recommended¹.

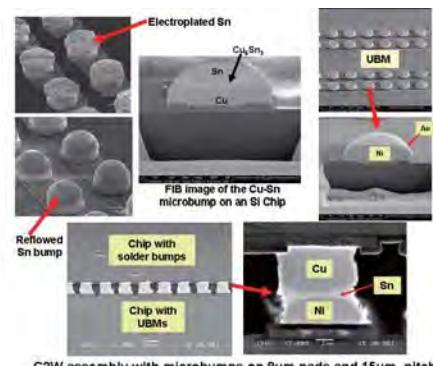


Figure 12. Fine-pitch, small-pad, low-standoff, lead-free microbumps

Thermal Management of 3D IC Integration

Low-cost and effective thermal management design guidelines and solutions are desperately needed for widespread use of 3D IC integration systems. Even with the most advanced software and high-speed hardware, it is impossible to model all the TSVs in a 3D IC integration system. Usually, based on heat transfer theory and CFD (computational fluid dynamics), the equivalent thermal conductivities of a TSV interposer/chip with various TSV diameters, pitches, and aspect

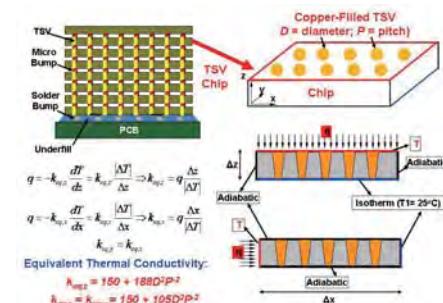


Figure 13. Equivalent thermal conductivity of TSV chip/interposer

Hot Spot for Different TSV Chip Thickness

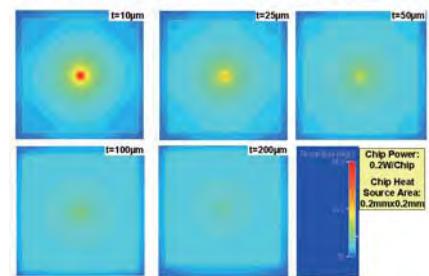


Figure 14. Hot spot of TSV chip with various thickness

ratios are developed. These equivalent thermal conductivities are then used (with the TSV chip/interposer as a block) to perform simulations. **Figure 13** shows the equivalent thermal conductivity of a TSV in the vertical direction ($k_{eqz} = 150 + 188D^2/P^2$) and horizontal direction ($k_{eqx} = k_{eqy} = 150 + 105D^2/P^2$)¹. By using these equations, the hot spot of a TSV chip with different thickness can be determined as shown in **Figure 14**¹. The heat on the chip surface is well dissipated for typical chip thicknesses of 100 to 200 μm subjected to a generated power of 0.2W. For the 200 μm -thick chip, the temperature distribution is almost uniform and equal to 35°C. However, the hot-spot temperature on the chip increases to 69°C if the chip thickness is reduced to 10 μm . The hot-spot area is clearly shown.

Conclusions and Recommendations

1. TSV for 3D integration is at least a 26-year-old technology. However, with TSV and the new concept that every IC chip could have two active surfaces (3D IC integration), the doors are wide open for many innovative applications.
2. The key difference between 3D IC packaging integration and 3D IC/Si integrations is that the latter two use TSV.
3. The key difference between 3D IC integration and 3D Si integration is that the latter is bumpless.
4. High volume products with 3D Si

integration technology is far in the future. The electronics industry should strive to make more high-volume products with 3D IC integration technology

5. IC chip yield (Y_p) plays the most important role in TSV manufacturing cost. If Y_p is low for a particular IC device, then it is not cost effective to use the TSV technology (because it makes the good dice too expensive), unless it is compensated for by density, performance, weight, and form factor.
6. TSV manufacturing yield (Y_{TSV}) plays the second most important role in TSV manufacturing cost. Since this is the first post-wafer processing after the IC semiconductor fabs, the packaging assembly and test houses should strive to make $Y_{TSV} > 99.99\%$. Otherwise, it will make the subsequent steps very expensive by wasting material and process on the damaged TSV dice.
7. Wafer-bumping yield ($Y_B > 99.99\%$) plays the third most important role in TSV manufacturing cost. The wafer-bumping/packaging assembly and test houses should strive to make $Y_{TSV} Y_B > 99.98\%$ to minimize the hidden cost, since they cannot afford to damage good dice already having TSVs.
8. Dates in the 3D IC integration roadmap most likely will be postponed because of the tough requirements of TSV manufacturing yield ($Y_{TSV} > 99.99\%$) and the very high hidden costs².
9. Based on what happened about 20 years ago to the low-cost, solder-bump, flip-chip, and wafer-level packaging technologies, it will not be a surprise to see that, at the early stage, semiconductor foundries would like to do TSV and wafer bumping, but when the volumes pick up, the packaging assembly and test houses will do it all because they are flexible. Also, their core competence and major business are to build packages for the chips from the wafers given (made and tested) by the semiconductor foundries and to perform the final packaging test. Then they ship only the good ones to EMS (electronics manufacturing services) who perform the PCB assembly, in-circuit test, system (also called final or functional) test, and ship the product to the system houses'

hubs for distribution. Some system houses prefer to have their EMS ship them the in-circuit tested good PCBs, perform the final test in-house, and then ship the product. This is the infrastructure and how the electronics industry works. Of course, for some special reasons or niche applications, there are always a few exceptions.

Appendix

There are at least two different vias on a chip. One is very tiny ($\leq 0.1\mu\text{m}$ today) and the other is very large ($\geq 5\mu\text{m}$ today). The tiny ones are connected to devices such as transistors (4 tiny vias for each transistor) to build the first metal layer (Figure 15). Today, the number of these tiny vias, for many chips, already exceeds the world population of over 7 billion. On the other hand, for the large vias that we call TSV for 3D IC integration, the number is much less ($\leq 100,000$ today) and the size is larger (a $5\mu\text{m}$ TSV is shown in Figure 15 to show their contrast). Foundries are too expensive to make 3D IC integration TSVs. This is also true for the via-middle approach, which makes the TSVs before the metal layers.

Acknowledgement

The author would like to thank Ian Yi-Jen Chan, PhD, of the Electronics & Optoelectronics Labs of ITRI for his strong support. He also would like to thank X. Zhang, PhD, and A. Yu, PhD, for their useful discussions. ☺

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Figure 15. Comparison of tiny vias with 3D integration TSVs

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Next-Gen Advanced Packages Spell Opportunity for Burn-in and Test Community

By Françoise von Trapp, Contributing Editor [[3D InCites](#)]

I wore a different hat at this year's BiTS Workshop, held March 7-9, 2010, in Mesa AZ. Yup - I set aside the 3D crown and my trusty keyboard for a day, put on the burn-in and test hat provided by Fred Taber, CEO of BiTS Workshop, and stepped in front of the video camera to interview keynote speakers and be the roving reporter on the exhibition floor. Here's a synopsis of some of those discussions.

Benefits of adaptive test

In his keynote address, Ken Butler, Fellow at Texas Instruments, discussed the concept of adaptive test, comparing it to traditional test approaches that involve applying a fixed sequence to every device in the same way. "When you move to an adaptive approach, you take into account that processes vary, materials vary, and likewise test must vary to do the best possible thing for each product," said Butler. Rather than just performing a one-off test to make rapid decisions, adaptive allows for data acquisition, movement, and analysis. While adaptive test doesn't eliminate the need for burn-in, it optimizes its use. In some cases it equals test time reduction, but more importantly it allows you to learn as much as possible from each wafer in terms of process learning, device debugging, and quality improvement.

From a cost perspective, while adaptive test may cost more as a unit, the benefit of increased yield drives the overall cost down. Butler emphasized the importance of looking at packaging and test processes holistically, rather than at each unit cost, to get the big picture.

Unfortunately, despite the obvious benefits, the industry is slow to adopt adaptive test. Butler says this is partly due to lack of infrastructure to support

it: better data bases, better data communication mechanisms. But this also turns into opportunity, he noted, citing several start-ups such as Optimal and Test Advantage that are working on the EDA tools and software for adaptive test.

Butler's loudest message to the masses was the importance of collaboration. Gone are the days when everyone benefits by keeping information close to the vest. In the adaptive test world, sharing of information is critical to everyone's success.

Test in tray - If you don't have one, get one

Tom Di Stefano, Centipede Systems, took the podium to talk about one area of manufacturing where the back-end guys could take some tips from the front-end guys to reduce cost and time to test: handling. "Parts are becoming more complex faster than we can develop the tools to deal with them," he remarked.



His idea is to create a "lights-out automation" process, similar to the one used in wafer fabs, made easy by the existence of the front opening unified pod (FOUP). However, the front-end has the advantage of standard wafer formats; all the varied package configurations pose a challenge to the back-end. According to Di Stefano, this can be solved by reconstituting packaged dice into a rectangular array

and creating a standard carrier that appears the same to the automation tools. His company's test-in-tray technology enables full automation from the time the wafer is diced through final assembly, packaging, and test. "It provides a vehicle for handling parts," explained Di Stefano. "You can test a part before stacking and after in the same type of tray." This sounded to me like it could be adapted to testing delicate 3D TSV stacks. "Absolutely," said Di Stefano. In fact, he says they've been prototyping test-in-tray for thin silicon for two years. While this doesn't solve the test issues themselves, it's his opinion that it should take care of the handling portion.

It's ALWAYS about cost

Brandon Prior, Prismark Partners, focused his market update report on low cost packaging and small form factor packages, offering suggestions on how to reduce manufacturing and production costs on mostly mainstream packages. He talked about what packages are being used in the industry and why, and what's driving folks to lower cost solutions.

Addressing the slow moving trend in the industry, he said wire bond still holds 80-85% of the market in terms of units. There's been a migration away from leadframe packages towards array based or substrate based approaches, and beyond that, flip chip packages,



flip chip bare die, wafer level CSP, chip-on-flex, and embedded die are all becoming more important.

Prior pointed out that, despite all the hype around 3D, it still represents less than 1% of all packaging value, and he doesn't expect it to reach 10-15% until 2020. He reminded me that flip-chip took 30 years to be considered main stream, and still when you talk to companies working in high volumes like Qualcomm and ST Microelectronics, they say it's still more expensive and only used when the performance and form factor benefits are required. "A new technology may be great and a lot of people might use it, but it will take a long time before it becomes a cost competitive approach."

60 seconds of fame

We gave exhibitors 60 seconds of air time to talk about the products they were showcasing. It's amazing what these guys could cram into that amount of time. Here are a few interesting tidbits:

- At the Multitest booth, Bob Chartrand explained the benefits of the company's new flat pin technology manufactured from a proprietary based metal resulting in pins that are three times harder and have 10 times the feature sharpness of regular pogo pins. This allows them to achieve Kelvin on fine-pitch wafer scale and BGA packages. Additionally, Multitest has launched a burn-in group division for high-powered burn-in testing.
- Nick Langston of Yamaichi talked about the company's conductive, super hard coating (CHS) that is said to extend the life of spring probes or any electrical contact. Additionally, it reduces the amount of solder adhesion, thereby lowering the cost of test.
- R&D Circuits was showcasing its embedded component technology which Tom Bresnan said had been generating lots of interest among customers looking for better power performance right at the DUT board.



- Roger Weiss described his company, Paricon Technologies, as a custom contact house that uses its core technology to manufacture contactors for devices requiring tight control and finer pitches, while at the same time serving a variety of structures. The core technology is a high-performance elastomer interconnection material made from very fine particles of silver plated nickel, blended with silicone through an extrusion process. The resulting material is then integrated into fixtures and structures.
- HCD was promoting its SuperButton proprietary interconnect technology for higher electrical performance as well as its SuperSpring interconnect for enhanced mechanical compliance. Amit Varma, HCD's representative, explained that there's a trade-off between electrical and mechanical performance. "When you're working with high electrical characteristics, you're going to have to compromise on mechanical performance," he noted.
- Jim Johnson at Brush Wellman also offered a glimpse of the paper they were presenting on a high-temperature clad metal that can be used at temperatures above 200°C. "It's remarkable and hasn't been done before," he noted.
- Self-described inventor, Bill Sinclair, CEO of Aries Electronics, offered a detailed description of the company's novel burn-in test socket that works sideways rather than up and down. Sinclair says this flexible design accommodates an assortment of device sizes, and increases productivity for the simple reason that you can get more into the burn-in oven at one time.



- Plastronics jumped on the 3D wagon with booth signage that required 3D glasses to read. According to Larry Furman, they were looking for a fun way to get their customers to look at sockets in a different way. "We want them to look at the component groups and decouple the design, rather

than look at a fully integrated socket," he explained

- Ila Pal of Ironwood Electronics gave a preview of the paper being presented at BiTS on a development device to test a 3D package-on-package (PoP) device. Pal explained that it's not easy to test a development device in the back end, because it's a two level connection. In the front end, you need a four level connection to test the same two packages. Once everything is good to go at the development stage, only a 2-level test will be needed in production.
- Self-described inventor, Bill Sinclair, CEO of Aries Electronics, offered a detailed description of the company's novel burn-in test socket that works sideways rather than up and down. Sinclair says this flexible design accommodates an assortment of device sizes, and increases productivity for the simple reason that you can get more into the burn-in oven at one time.

To see the full videos of these interviews, logon to <http://www.vbits.semneedle.com>.

Final Thoughts

In challenge, there is always opportunity. It's clear that the burn-in test community continues to rise to the ongoing challenges of increased density, performance, and the form factor needs that each generation of advanced packages dishes out, while keeping cost in mind.

High Temperature Stack-chip, Die-attach Adhesive Developments

Currently solving many problems, but a new generation is needed.

By Kevin Chung, Ph.D. [AI Technology, Inc.]

The majority of die-attach applications for chip packaging are done with singulated dice and dispensed die-attach adhesive paste. Film adhesives have also been used for at least 10 years for stack-chip applications.

In recent years, the use of film die-attach adhesives in wafer-level packaging has been in high-volume use for DRAM applications with great success. In this type of thin wafer-level packaging where the resulting device size and thickness are critical to commercial success, die-attach film has been steadily reduced to 10 μm or less in comparison to the 1-3mils bond line thickness for traditional die-attach semiconductor packages.



Figure 1. CPU is one of the great successes of flip-chip application

DRAM is usually rectangular with a total overall die-attach area smaller than one square centimeter. This enables the use of thin bond lines of less than 10 μm without excessive internal stress-induced failures even when the bond is reduced to much less than the commonly acceptable bond line of 1.5-3mils for reliable die-attach thickness¹.

While electronic packages using die-attach adhesive can achieve substantial relief of the interfacial stresses with the use of thicker, low modulus

adhesives^{2,3}, the use of epoxy film adhesive with a coefficient of thermal expansion (CTE) in the range of 40-60ppm/ $^{\circ}\text{C}$, modulus of more than 10 million PSI, and the bond-line thickness of 10-20 μm have produced parts of adequate reliability for at least the DRAM packages.

In this paper, we will examine the criteria for wafer-level die attach with higher efficiency, more reliability and higher performance.

We will also examine the effects of interconnection from chip to package on the choice of die-attach solutions. The packaging, using wire bonding, flip-chip soldering, or the direct mechanical contact attach from flip-chip to bond pads, effectively dictates the choice of different wafer-level, die-attach solutions.

Wire bonding and flip-chip interconnections

Wire-bonding is the predominant choice for chip-to-package interconnections. The proven efficiency and reliability result in a cost effective solution for high volume DRAM applications.

Most of the stack-chip packaging for smaller volume production uses pre-cut, die-attach film with great success and high reliability. These earlier stack-chip solutions have been building DRAM with 8 or more chips for many high-end applications. These standard die-attach



Figure 2. Stack-chip packages can be interconnected with wire bonding or special design inter-chip interconnection bridges



Figure 3a. Lamination of wafer onto dicing die-attach film (DDAF)



Figure 3b. Dicing wafer with DDAF



Figure 3c. Shining UV



Figure 3d. Pickup dice from DDAF



Figure 3e. Examining dice for packaging

film adhesives tend to be a controlled thickness of 2-4mils. **Figure 2** shows two examples of these 3-D high density packages.

As more chips are stacked on top of each other, wire-bonding interconnection becomes more difficult to execute. Many ingenious packaging schemes have been developed by, for example, Vertical Circuit Inc.⁴, on board flip-chip attach by Shellcase, and through-silicon via (TSV) from Sharp, Fujitsu, and others⁵.

In high volume commercial applications, the use of 10-20 μm die-attach film adhesive has proven to be reliable for this size and

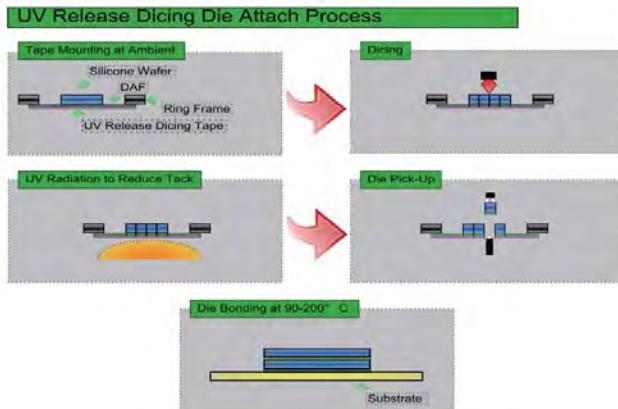


Figure 3. Dicing die-attach film processing °C die-attach film must be compatible with UV release layer and have the ability to flow and cure rapidly, or flow with light pressure and cure without pressure, in order to maintain productivity

shape of chip for stacked chips from two to three layers. With that number of stacked chips, wire bonding can still be managed. The use of 10-20 μm film adhesive not only yields thinner devices that are attractive for cameras and other commercial applications, but also provide a more uniform and controlled flow of the adhesive and thus more reproducible wire-bonding interconnections.

Standard wire-bonding chip packaging uses backside die attach that can use more traditional epoxy die-attached film adhesives that are available from die-attach film adhesive manufacturers from the USA^{6,7} and Japan^{8,9,10}. **Figure 3** shows a pre-laminated wafer with 15 μm die-attach film adhesive.

Typical manufacturing process in using wafer-level packaging is now integrated in terms of using dicing tape and die-attach film that are directly laminated on the wafer before dicing. The layering of such configurations is illustrated in **Figure 2** and the process represented in **Figure 3**.

Adhesive properties and device performance

The material technology challenges that enable the processes described in **Figure 3** are many and have been met so far by dicing die-attach film (DDAF) adhesives from the USA and Japan. The following are some of the challenges:

- Very thin and stable film adhesive (typically epoxy-based) of 10-25 μm

for the largest wafer today (12 inches).

- DAF film adhesive must be compatible with the use of UV release dicing tape to release chip after dicing operations.
- Ability to allow stack-chip bonding with high efficiency.
- Ability to provide die-bonding stability for wire-bonding operation of up to 250°C for the highest production rate possible.

- Most of the existing DDAF are meeting the performance requirements of JEDEC IPC level 3 or better for moisture sensitivity after packaging.
- Depending on the bonding stability and moisture sensitive properties of DAF and the molding, encapsulation, or other electro-mechanical protection, the finished devices range from level 3 (in most cases) to the best solutions meeting the level 1 requirement.
- In case of high temperature applications beyond 150°C, newer non-epoxy DAF can now withstand long-term usage of 200°C and beyond.

Die-bonding adhesive and stress relief protection

Traditional flip-chip uses wire bonding and solder-bump reflow for most requirements. Higher speed,

performance, and cost continue to drive semiconductor packaging toward shorter path interconnections between each level of the stack-chip packages.

The need to lower the cost of packaging has led to many innovative packaging solutions. The lowest cost electronic devices such as UHF RFID tags have been successfully produced in large volume using direct flip-chip mechanical compression contact¹¹. However, they are limited to an operational temperature of less than 60°C and they are not very stable against moisture.

The fact that contact resistance can be properly maintained for long-term usage within specified temperature and environmental constraints provides hope that solutions for high performance applications can be achieved with more engineered materials and packaging. **Figure 5** illustrates such flip-chip, direct contact interconnection.

The key for performance for this type of package is the flip-chip underfill that must also perform as a stable die-bonding adhesive. For the flip-chip underfill adhesive to function properly, it must possess at least the following characteristics:

1. Underfill adhesive must be easily placed either on the substrate or on the interconnection front side of the chip. Dicing die-attach film (DDAF) is still applicable. If paste underfill adhesive is to be useful,



Figure 4. Semi-conductor packaging from wafer DDAF to component



Figure 5. Flip-chip interconnection with direct mechanical contacts between precious metal bumps and preservations on chip and package substrate respectively

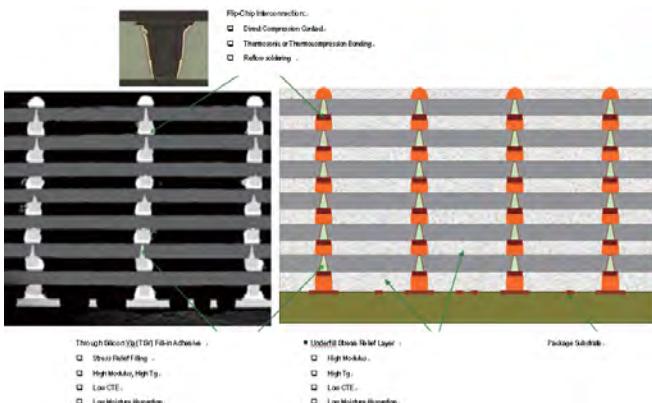


Figure 6. Specialty fill-in adhesive and underfill adhesive with low CTE, high modulus and high Tg is essential in the reliability of stack-chip packages using through TSV technology

- it must stay in place after dispensing onto the substrate or chip.
2. The underfill adhesive must not prevent contact when the chip and package substrate interconnections are lined up and compressed for bonding. Unlike the use of Z-axis, uniaxial, conductive adhesive, any particulate could be detrimental to the achievement of interconnections.
 3. High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
 4. The underfill adhesive should be as low in coefficient of thermal expansion (CTE) as that of higher filled traditional epoxy underfills (< 30 ppm/°C).
 5. In order to provide reasonable productivity, the underfill adhesive must be capable of curing at 175-250°C in less than 10 seconds.
 6. To meet the JEDEC IPC Level 1 moisture sensitivity requirements, the moisture absorption should be well below 0.5% in saturation.

There are now non-epoxy based, high temperature, underfill adhesives in paste or film format in thickness of 25-75µm for such applications.

TSV, specialty underfill, and via filling for stress relief

TSV¹² stack-chip packaging represents the ultimate chip interconnection performance for stack-chip packages. The requirement for

stress relief is even more critical to filling in the vias of the TSV structure and between the stacking chips.

For filling in the TSVs, the specialty fill-in adhesive requires the following characteristics:

- The fill-in adhesive must have extreme low viscosity to wick into the vias easily with the capillary forces.
- Once cured, they must have very low coefficient of expansion (CTE) and preferably substantially below 30ppm/°C.
- High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
- Fill-in adhesive should cure in less than 10 seconds at 175-250°C.

There are now non-epoxy based high temperature fill-in paste adhesives that can easily fill in vias of 20µm for such applications. **Figure 6** depicts the TSV structure and the lamination between layers to provide stress relief.

Conclusions

Flip-chip electrical interconnection between a chip bumped with gold studs and its package substrate can be done by direct compression contact with high reliability and manufacturability. A new generation of flip-chip underfill adhesives are needed with low moisture absorption, high Tg, low CTE, and high modulus to provide the stress relief that enables even high I/O counts devices to be packaged with high reliability and low moisture sensitivity.

Similar flip-chip underfill adhesive can also be very effective for fill in of through silicon vias and provide stress relief between stacked chips. 

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Company Address City, State, Zip Country Phone Fax Founding Year	⌘ Number of Employees ✖ Maximum Wafer Size (mm) ⌘ Bump Pitches (µm) ● Bumping Services	★ Equipment A=Aligners, B=Stencil Printers, C=Steppers ◆ Bumping Technologies J=Jetting, P=Plating, BP=Ball/loading placement, S=Sputtered, SP=Stencil printing, CP=Copper pillar, O=Other ✿ Bump Alloys SAC=SnAgCu, Au=Gold, Eu=Eutectic, LF=Pb-free, HL=High lead, LA=Low alpha	WebSite ✿ Contact Additional Offices
Advanpack Solutions Pte Ltd 54 Serangoon North Ave 4 Singapore 555854 Tel: +65-6482-5995	⌘ CM ✖ CM ⌘ 50 – 150 ● Wafer Bumping and RDL and WLP Capabilities	★ CM ◆ P, S, CP, O ✿ Au, LF, HL, Cu	www.advanpack.com
Amkor Technology Inc. 1900 South Price Rd. Chandler, AZ 85286 Tel: 480.821.5000 Fax: 480.821.8276 1968	⌘ 5,000+ ✖ 300 ⌘ 60 to 300 ● 150-, 200- and 300mm wafer bumping/test/die processing	★ A ◆ BP, P (electroplating), S ✿ Eu, LF, HL, LA	www.amkor.com
ASE Group Kaohsiung, Taiwan 811 Tel: +886.7.361.3094 1984	⌘ CM ✖ 300 ⌘ CM ● CM	★ CM ◆ P, SP ✿ CM	www.aseglobal.com ASE (U.S.) Inc. Santa Clara, CA 95054 Tel: 408-986-6500
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ChipMOS Hsinchu Science Park Hsinchu, Taiwan Tel: 866-3-577-0055	⌘ CM ✖ 200 ⌘ CM ● Gold Bumping Services	★ A, C ◆ S ✿ Au	www.chipmos.com ChipMOS USA San Jose, CA 95134 Tel: 408-922-2777
FlipChip International Div. of Rose Street Labs 3701 E. University Dr. Phoenix, AZ 85034 Tel: 602.431.6020 1996	⌘ CM ✖ 200 ⌘ 70 (R&D), 150+ (production) ● Flip chip and wafer bumping, Ultra CSP, Elite CSP, copper pillars, thinning, plus backend to tape & reel or chip trays	★ A, C ◆ Sputtered UBM, electroless Ni/Au UBM, SP, BP alloys, CP ✿ CM	www.flipchip.com
i2a Technologies 399 West Warren Ave Fremont, CA 94538 Tel: 510.770.0322 1993 (formerly IPAC)	⌘ CM ✖ 200 (300 soon) ⌘ 50µm Au stud, 180µm solder bump, 400+ WLP ● WL-CSP and flip chip ranges, bumped wafers, finished package (WLP and FC), die in tape & reel or waffle	★ B ◆ SP ✿ Eu, LF, SnAgCu	www.i2a-tech.com
IC Interconnect 1025 Elkton Dr Colorado Springs, CO 80907 Tel: 719.533.1030 1998	⌘ 12 ✖ 200 B 200µm+ ● ENi/UBM combined with stencil printed solder, low cost wafer bumping	★ CM ◆ SP, BP ✿ Eu, HL, electroless UBM, SAC	www.icinterconnect.com

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International Micro Industries (IMI) 1951 Old Cuthbert Rd. Bldg 404 Cherry Hill, NJ 08034 Tel: 856-616-0226 Fax: 856-616-0226 1971 (Founded)	⌘ 21 ✖ 300 ⌘ CM ● Bumping and WLP utilizing electro deposition process and specializing in high aspect ratio, fine pitch and pillar bump technology	★ Aligners ◆ P, S, CP, O ⌘ SAC (SnAgCu)Au, E, LF, HL	www.imi-corp.com
Minami Co., Ltd. EMS Tsukuba Factory 38-32 5-Chome, Minami-Cho Fuchu-Shi, Tokyo 183-0026, Japan Tel: +81.42.368.8311 1980	⌘ 30 ✖ 300 ⌘ 80µm (45µm diameter) ● Ball placement, reflow, washing, inspection, quick delivery, low cost, high quality	★ CM ◆ SP T P, SP, BP ⌘ Solder paste and balls, SnAgCu	www.ho-minami.co.jp
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Pac Tech GmbH Division of Nagase & Co., Ltd Am Schlangenhorst 7-9 & 15-17 14641 Nauen, Germany Tel: +49.3321.4495.100 Fax:+49.3321.4495.110 . 1995	⌘ 150 ✖ 300 ⌘ UBM 40µm, bump pitch solder 80µm ● Wafer bumping for Ni/Au UBM, Ni/Pd/Au and thick Au for wire bonding; wafer level solder bumping, BCB repassivation, wafer level redistribution, wafer thinning, wafer dicing, chip singulation, tape & reel	★ A ◆ SP T SP, BP, electroless UBM, J ⌘ UBM: NiAu, NiPdAu; Solder: SnAgCu, SnPb, AuSn	www.pactech.de Pac Tech USA Inc., 328 Martin Ave., Santa Clara, CA 95050 Tel: 408.588.1925 Pac Tech Asia Sdn Bhd., Bayan Lepas Industrial Zone, 11900 Bayan Lepas, Penang, Malaysia
Siliconware Precision Industries Co. Tantzu, Taichung, 427 Taiwan Tel: +886.4.25341525 1984	⌘ ~14,800 ✖ 300 ⌘ 180 ● CM	★ A, B, C ◆ P, SP, BP, sputtered UBM ⌘ Sn63/Pb37, Sn5/Pb95, SnAgCu, SnAg, SnCu, Au bump	www.spil.com.tw Siliconware USA Inc., San Jose, CA 95110 Tel: 888.215.8632
STATS ChipPAC Ltd. Singapore 569059 Tel: +65.6824.7777 1994	⌘ 14,873 ✖ 300 ⌘ CM ● Printed, plated and ball drop bump, redistribution, flip chip interconnect and WLCSP	★ A, B, C ◆ P, SP, BP, sputtered UBM ⌘ Eu, ultra low alpha HL, LF	www.statschippac.com STATS ChipPAC Inc., Fremont, CA 94538 Tel: 510.979.8000

All Companies listed have in-house wafer bumping capabilities

Listing does not include capability for Gold Wire Ball Bumping.

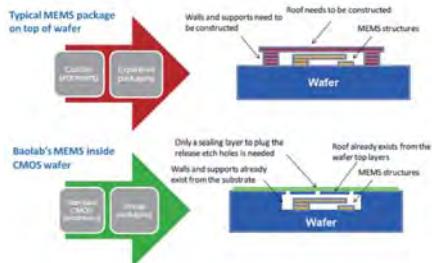
The 2010 International Directory of Wafer Bumping Service Providers is compiled by AZ Tech Direct LLC.

To update listings in the directory for next year's publication, please contact the author at surveys@aztechdirect.com before January 31, 2011.

WHAT'S NEW!

Nanoscale MEMS Made Inside a CMOS Wafer

A new technology to construct nanoscale MEMS within the structure of the actual CMOS wafer itself using standard, high volume CMOS lines, has been announced by Baolab Microsystems of Barcelona, Spain. The technology uses the existing metal layers in a CMOS wafer to form the MEMS structure using standard mask techniques. "We have solved the challenge of building MEMS in a completely different way," explained Dave Doyle, Baolab's CEO.



Baolab has successfully created MEMS devices using standard 0.18µm, 8" CMOS wafers with four or more metal layers, and has achieved minimum feature sizes down to 200 nanometres. The prototype stage has already proven the NanoEMS technology and evaluation samples will be available later this year. These are aimed at handset designers and manufacturers, and Power Amplifier and RF Front End Module markets. [www.baolab.com]

Gantry Robots Get More Capacity

DENSO, headquartered in Kariya, Japan, has announced that it has increased the payload capacity of its XR-Series four-axis, compact gantry robots from 3 kg to 5 kg. The new 5kg capacity, which represents an increase of over 60 percent, allows the robots to handle a significantly wider range of applications. The XR-Series robots feature a ceiling mounted, SCARA robot combined with a long-stroke Cartesian robot. They can operate in many applications without the need of a conveyor.



The robots have a reach of 200mm to 300mm, an x-axis stroke of 850mm to 1,660mm, a cycle time of 0.53 seconds, and repeatability of ± 0.015mm. Typical applications include assembly, dispensing, material handling, and parts feeding. DENSO Robotics offer robots, controllers and software covering a wide range of applications. [www.densorobotics.com]

Need a Class 100 Oven?

The No. 836 is a 750°F, electrically-heated, Class 100 cleanroom oven from Grieve, Round Lake, IL, USA, and can be used to bake various coatings onto products at a customer's facility. Workspace dimensions of this oven measure 36" wide x 36" deep x 39" high. Incoloy sheathed tubular heating elements provide 30KW of heating and a maximum temperature of 750°F. A 1000CFM, 1.5HP recirculating blower maintains horizontal airflow across the load. The oven has 6" insulated walls, a 2B finish stainless steel interior, and an aluminized exterior.



Additional equipment on this Grieve oven include a 30" x 24" x 6" thick stainless steel high temperature HEPA recirculating air filter, digital programming temperature controller, manual reset excess temperature controller with separate contactors, recirculating blower airflow safety

switch, and a 10" diameter circular chart recorder. [www.grievecorp.com]

New Test Socket Claims 500,000 Insertions

Ironwood Electronics of Burnsville, MN, USA, has recently introduced the new high performance socket for the 602PGA-SS-PGA27/602A-01. The contactor is a spring pin (pogo) with 27 grams actuation force per ball and



cycle life of 500,000 insertions. The self-inductance of the contactor is 1.1nH with 50Ω matched impedance. The current capacity of each contactor is 5 amps. Socket temperature range is -55°C to +150°C. Kyocera's PB602AUE63-1 and other PGA ICs that are 35x35mm body size, 1.27mm pitch, and 27x27 pin array can be tested. The Socket is constructed of aluminum which provides heat sinking up to several watts and custom heat sinks can easily be designed for higher power dissipation. This socket can be used for functional test and extreme thermal cycling test with the most stringent requirements.

[www.ironwoodelectronics.com]

Bond Tester Has More Features

The Condor EZ, a new bond tester from XYZTEC, Gilroy, CA, USA, offers



a single platform with multiple test capabilities. In addition to standard bond testing applications such as wire

pull, ball shear, and die shear, the Condor EZ has the capability to perform peel testing, push testing, and roller testing. All of these tests can be done on one test head that features

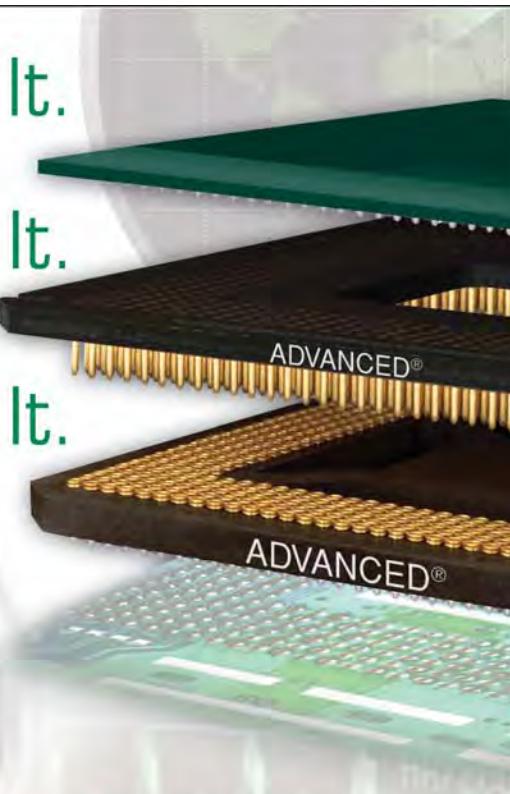
four different measurement sensors. The system can perform mechanical shock testing by changing the test head for impact testing or ribbon peel testing of photovoltaic cells. All

important software functions can be controlled by a single touch of a button to ensure simplicity. XYZTEC equipment is used worldwide throughout the semiconductor, automotive, solar and raw materials industries. [www.xyztec.com]

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Incal Introduces 'Inspire 8160 HX' Power Burn-In System

Incal Technology, Inc. has just introduced its latest 'Inspire 8160 HX' System for the power device burn-in market.

The 'Inspire 8160 HX' System provides individual temperature control for low to medium power SOC and mixed signal devices up to 60Watts. It uses thermal sockets and the well established Incal XP-160 driver and Inspire system software.

As thermal control and management is at the DUT level, no conventional thermal chamber is required. Since XP-160 /Inspire continue to be the main system architecture, all currently available burn-in system capabilities (drive and monitoring) and features are available for this 'NEW' system, including the 'Analog Option'. This 'Inspire 8160 HX' System addresses the increasing concern of power dissipation of high-power semiconductor devices. The power consumed by high-power semiconductor devices can vary by up to 50%, due to variation in fabrication process.

This causes a large variation in temperature among the same devices in the burn-in chamber. In order to burn-in all devices at the same junction temperature, there is a need for Individual 'Temperature Control' per DUT. This 'Inspire 8160 HX' system provides individual temperature control at the DUT. Two major Independent Test Laboratories have purchased this 'system', adding this to many Incal standard HTOL Infinity/Inspire systems on their floor. [www.incal.com]

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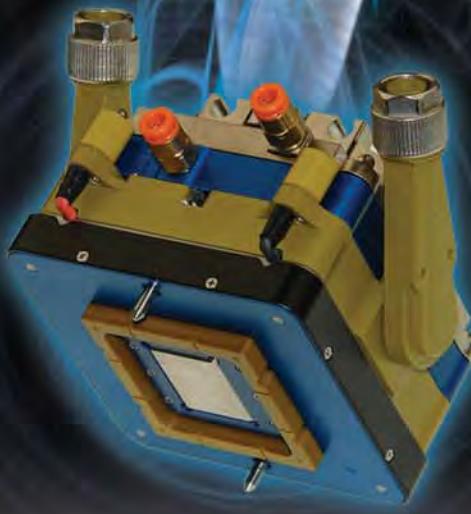
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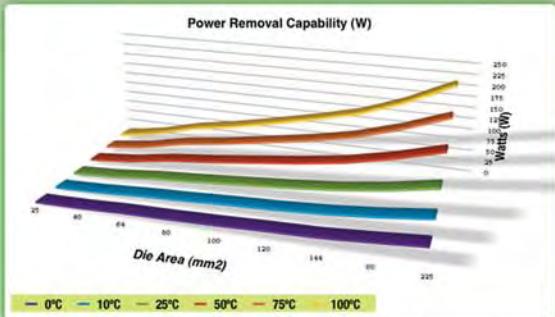
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