

Chip Scale® REVIEW

ChipScaleReview.com

The International Magazine for the Semiconductor Packaging Industry

Volume 18, Number 2

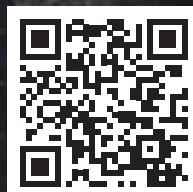
March • April 2014

Advancements in PoP technology in next-generation smartphone processors

Page 14

- OSATS market update
- TSV reliability challenges
- Die bonding for large panel FOWLP
- Die attach films for GaAs-based packages
- Trends in fluid dispensing for packaging today's devices

International Directory of IC Packaging Foundries



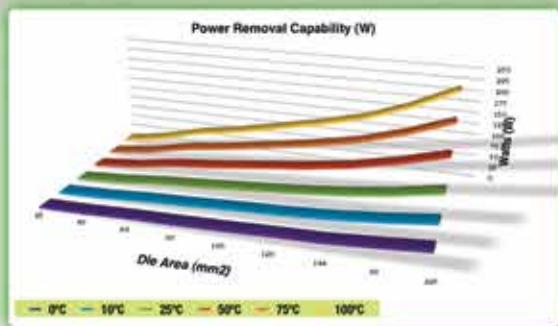
introducing

Advanced Thermal Management

...it's elemental



Essai's New Generation Thermal Management Systems Offer Performance & Versatility for I.C. Temperature Testing



Highly efficient thermal response with Thermo-Electric Cooler, Liquid & Heater assist based technologies

Distributed force loading between the Die & Substrate that prevents silicon cracking while maintaining proper thermal contact

Smaller footprint that can fit in various applications – manual or automated System Level & Final Test handlers

Integrated vacuum pickup designed for handler applications

Cold test capable with efficient condensation abatement features

Available for **wide range of packages**: Bare Die, Lidded, Thin Core, and Ultra Small Form Factor devices

essai
www.essai.com

CONTENTS

March • April 2014
Volume 18, Number 2



Advanced PoP technology configurations such as Bare Die and Molded-Laser Package each offer advantages for the smartphone and tablet markets.

Photo: Courtesy of STATS ChipPAC

Chip Scale[®]
REVIEW
ChipScaleReview.com

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

FEATURE ARTICLES

	Advancements in package-on-package (PoP) technology for next-generation smartphone processors Hamid Eslampour, SeongWon Park, HanGil Shin, JaeHan Chung, YoungChul Kim <i>STATS ChipPAC</i>	14
	Simulation of 3D IC fabrication Sudarshan Krishnamoorthy, Xiaopeng Xu <i>Synopsys</i>	22
	Evaluating conductive die-attach films for gallium arsenide-based packages Andrew Laib, Howard Yun, <i>Henkel</i> , and Frank Wei, Hiroaki Yamada, <i>DISCO</i>	26
	Fluid dispensing for packaging today's devices Akira Morita, <i>Nordson ASYMTEK</i>	30

SERVERS

Technology Leadership in
Copper Pillar, 3D and Wirebond Stacking



Visit Amkor Technology online for the most current product information and locations.

www.amkor.com

Packages not shown actual size. © 2014 Amkor Technology, Inc.

LEENO has 100% in-house manufacturing to provide our customers with the best Quality & Delivery”



**Logic Test
Socket**



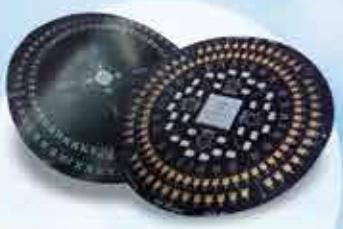
RF Coaxial Spring Probe & Impedance Controlled Socket



**PoP Test
Socket**



Probe Head



**Wafer Level CSP
Probe Card**



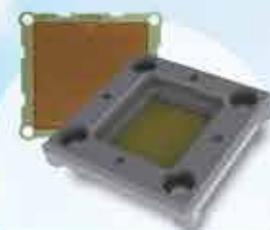
**Memory
Socket**



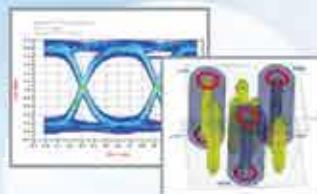
**Spring Contact
Probe**



SLT Socket



**Elastomer
Socket**



Electrical Analysis
CCC Test, HFSS, TDR
Eye Diagram
4Port VNA Test



The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

STAFF

Kim Newman Publisher
knewman@chipscalereview.com
Lawrence Michaels Managing Director
lxm@chipscalereview.com
Debra Vogler Senior Technical Editor
dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Dr. Thomas Di Stefano Contributing Editor
tom@centipedesystems.com
Jason Mirabito Contributing Legal Editor
mirabito@mintz.com
Paul M. Sakamoto Contributing Editor Test
paul.sakamoto@comcast.net
Dr. Ephraim Suhir Contributing Editor Reliability
suhire@aol.com

EDITORIAL ADVISORS

Dr. Andy Mackie (Chair) Indium Corporation
Rolf Aschenbrenner Fraunhofer Institute
Dr. Thomas Di Stefano Centipede Systems
Joseph Fjelstad Verdant Electronics
Dr. Arun Gowda GE Global Research
Dr. John Lau Industrial Tech Research Institute (ITRI)
Dr. Venky Sundaram Georgia Institute of Technology-3D Systems Packaging Research Center
Fred Taber BiTS Workshop
Dr. Leon Lin Tingyu National Center for Advanced Packaging (NCAP China)
Francoise von Trapp 3D InCites

SUBSCRIPTION--INQUIRIES

Chip Scale Review
Effective immediately
All subscription changes, additions, deletions to any and all subscriptions should be made by email only to
subs@chipscalereview.com
Do not leave subscription inquiries on the company voicemail system.

Advertising Production Inquiries:
Kim Newman
knewman@chipscalereview.com

Copyright © 2014 Haley Publishing Inc.
Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$100 per year to Canada or \$125 per year to other countries. In the U.S. subscriptions by first class mail are \$95 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January-February, March-April, May-June, July-August, September-October and November-December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER

This month, *Chip Scale Review* highlights how semiconductor packaging is more and more being tasked with meeting the needs of tomorrow's technology demands—including keeping costs under check as front end costs (i.e., costs per transistor) are increasing post-22nm. Outsourced assembly and test suppliers (OSATS) are stepping up to meet these cost challenges as the semiconductor industry develops devices that facilitate the Internet of Things (IoT). Author Steffen Kroehnert, of NANIUM S.A., notes that an estimated 80-90% of the semiconductor, assembly, and test industry has moved to Asia during the last three decades. And recently, such advanced packaging capabilities as TSV and 3D ICs have become a significant driver for the entire industry. Readers can keep up to date by using the IC Packaging Foundries database included in this issue.

Kim Newman
Publisher

FEATURE ARTICLES

	Ranking the top OSATS in IC packaging Sandra L. Winkler	35
	Semiconductor packaging, assembly and test in Europe Steffen Kroehnert, <i>NANIUM S.A.</i>	46
	Electronics reliability cannot be assured if it is not quantified Ephraim Suhir, <i>Portland State U.</i>	50
	Large panel fan-out wafer-level packaging: accuracy is king Johann Weinhaendler, <i>Amicra Microtechnologies, GmbH</i>	54
	Precision epoxy dispensing combined with traceability Willibald Konrath, Klaus Scholl, Haiko Schmelcher, <i>TESAT Spacecom GmbH & Co. KG</i> Cyriac Devasia, Ravi Balasubramanian, <i>MRSI Systems, LLC</i>	57

DEPARTMENTS

	Guest Editorial Challenges and opportunities in advanced IC packaging Chin-Yu (Max) Lu, <i>SPIL</i>	5
	Industry News	10
	International directory of IC packaging foundries	38
	Profile Innovation for industry <i>Chip Scale Review</i> staff interviews Laurent Malier, <i>CEO of CEA-Leti</i>	60
	Advertiser Index, Advertising Sales	64



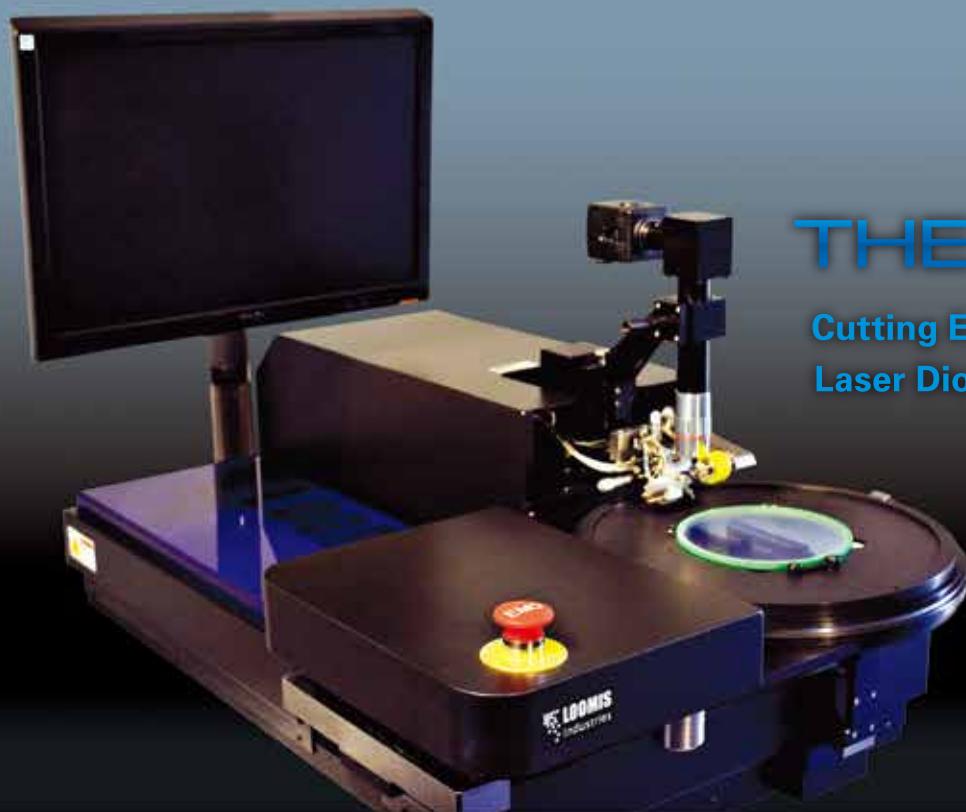
Patented Scribe and Break Dicing Technology

Loomis Industries, Inc.

1204 Church Street
St. Helena, CA 94574

T. 707-963-4111
F. 707-963-3753

info@loomisinc.com
www.loomisinc.com



THE LSD-155

Cutting Edge automated III-V
Laser Diode and Wafer Processing

KEY ADVANTAGES:

- Increased Operator Productivity
- Integrated Scribe and Break Capabilities
- Bar Array Dicing (Grids of Laser Bars)
- Multiple Cleaving Options
- Multiple Wafer Holding Media Options
- High Resolution Optics
- Pattern Recognition with Micron Level Accuracy
- Cleaved Edge, Vision, When standard pattern alignment is not good enough.

EASE OF OPERATION:

- Easy to Navigate User Interface
- Password Protected Levels of Access
- Hands-Off Media Rotation
- Software/Recipe Controlled Process Parameters, Pressures, and Speeds

LOOMIS LSD-155

Speed, product quality and yield speak for themselves.
Contact Loomis Industries for information or a demonstration.

GUEST EDITORIAL



Challenges and opportunities in advanced IC packaging

By Chin-Yu (Max) Lu [[SPIL](#)]

IC packaging not only provides the physical/mechanical support for the device, the package is also responsible for the interconnection between the chip and external terminal (such as the printed circuit board, PCB). Without a successful IC packaging process, the chip is not able to become a real product or solution to fulfill the end customer requirement, no matter how good the design and wafer process might be. In previous generations, semiconductor manufacturing technology was driven by PC applications and followed Moore's law in technology migration. Packaging technology also simultaneously developed solutions to overcome the thermal, mechanical and electrical challenges that came with each new node.

In 2013, mobile applications formally replaced PC applications to become the main driver of the semiconductor industry. Small form factor, thin profile, high performance, multi-function integration and low cost are the most critical requirements for mobile applications and trigger numerous studies in the process, materials, and manufacturing equipment sectors, respectively. Some package solutions are developed to address the different product requirements in the market already. The merit of each solution will be described in this article.

It is widely known that the substrate comprises the majority of IC package/assembly costs. Addressing substrate cost is a straightforward way to reduce costs and increase overall product competitiveness. Industry has developed single-layer package (SLP) and embedded trace substrate (ETS) technologies as a way to provide a cost-effective advantage compared with existing solutions.

For some products, a 2L non-plating

line substrate is the cheapest substrate and has been the standard for years. SLP, however, was developed as a way to continue driving cost reduction and achieve simplicity in design. The SLP process enjoys the advantages of having a coreless substrate without the mechanical strength issue because it uses a prepreg lamination process, which was implemented with the carrier to enhance the structure. Equal or better control of warpage along with the capability for passive surface mount technology (SMT) before die bonding (D/B) are the two major strengths compared with a 2L non-plating line substrate. SLP technology is well qualified and on the market already.

Embedded trace substrate (ETS, refer to [\(Figure 1\)](#)) is another new idea for substrate fabrication. Compared with a traditional core substrate, ETS can simplify the substrate fabrication process and enable a finer trace width (~15/15 μ m) requirement. The traditional SAP process requires primer material. Primer, however, is more expensive than prepreg material and will increase the overall substrate cost. Conversely, ETS requires no primer and can achieve better adhesion on a finer trace. ETS technology is already qualified and supported by major substrate suppliers; it has also been considered as a cost-effective substrate solution for its comparable workability, warpage performance, and assembly process relative to flip-chip packaging. Going forward, multi-layer/dies and fine-pitch trace will be the major development directions to explore.

As IC technology

has migrated from 40nm to 20nm, I/O pad pitch shrank from 180 μ m to 90 μ m. Traditional solder ball pitches cannot fulfill the need for such fine-pitch requirements. As a result, Cu pillar technology was developed. In general, Cu pillar can be used for bump pitches <130 μ m without limiting the product application. Actually, Cu pillar is a better solution than solder in high-power applications; it has better electrical and thermal performance. Additionally, using a Cu pillar bump-on-trace (BOT) design will enhance the metal trace routability and potentially reduce substrate fabrication costs (e.g., reduce the metal trace layer or enable a smaller form factor).

PoP packaging

Just as the CPU drove the semiconductor industry during the PC era, the application processor (AP) is the most important component in every mobile product and thus, drives the industry. Because of dimension and power limitations, APs require a unique and integrated package solution to meet thermal, electrical and mechanical requirements.

A package-on-package (PoP) structure is one option that can fulfill the requirements listed above and has already been widely adopted by the

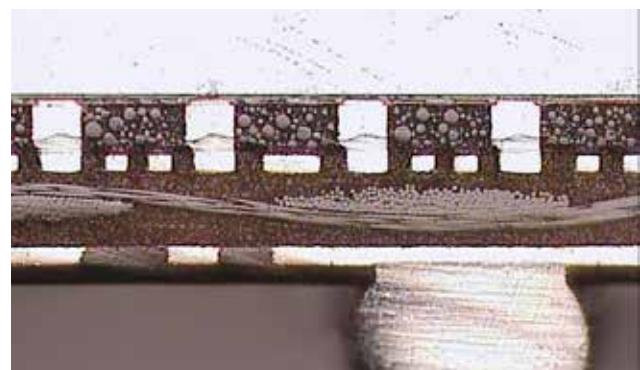


Figure 1: Cross section of an embedded trace substrate (ETS).

manufacturers of smartphones and tablets. Basically, in PoP, the AP acts as a bottom package and connects with the DRAM (upper package) through solder balls. Because of the short interconnection distance (from package to package) compared with through-substrate metal trace routing, PoP can achieve high performance and low power consumption, which are key attributes for competitiveness in the mobile market. The key challenge of a PoP structure is to overcome the tendency for warpage because of the intrinsic coefficient of thermal expansion (CTE) mismatch between silicon and the substrate. A tendency toward substrate warpage will induce the potential non-wetting of the die bond and further the potential for failure after certain stress conditions.

One approach being used to ensure assembly success and achieve a sufficient process margin is to use a molding compound to flatten the bottom of the PoP package before connecting it to the upper DRAM package. To overcome the drawback of warpage that is induced by the molding compound, a polishing process can be considered to get a reduced warpage of the bottom of the package.

Besides warpage, reduction of the total package height (Z-height) is another hot topic when using a PoP structure. Whether for smartphones or tablets, a thin profile is the most important product feature that must be considered. To be able to meet end product requirements, PoP Z-height has been pushed down from 1.2mm to 1.0mm, and beyond. Bare die PoP has been proposed to counter the reduction in Z-height. Along with a core-less substrate, bare die PoP can take into account both warpage and Z-height reduction. All the above mentioned PoP technologies are well developed and production solutions are now available in the industry.

The existing PoP form factor is limited by the upper DRAM package (especially, I/O count and ball pitch) because of the interconnection by way of the solder balls between the upper and bottom package. Using solder balls has its limitation with respect to fine-pitch requirements. For example, if more I/O connections are needed, two

major considerations are having to enlarge the form factor or reducing the upper package ball size. Unfortunately, enlarging the form factor is not acceptable for mobile applications. However, reducing the upper package ball size also faces the challenge of micro ball evaluation.

To satisfy the need for high I/O connections, a next-generation PoP (so called high-bandwidth PoP, or HBW PoP) is being developed now. The concept of HBW PoP is to add one upper substrate on top of the bottom package. This additional substrate acts as an interposer to make the connection between the upper and bottom packages. This routable substrate interposer is quite flexible and easily supports a full array ball placement that may be required for some single or multi-chip applications. The metal trace routing of the upper substrate depends on how many I/O connections there are between the upper and bottom packages. Typical substrate technology should be able to fulfill the requirement even for up to 500 or more I/O connections.

Another key feature of the upper substrate is the PoP ball material. Cu stud technology (for the bottom package) has been introduced to fulfill the fine-pitch requirement and keep a sufficient clearance between the bottom die and the upper substrate. Industry is now developing a <0.3mm pitch Cu stud that can allow four rows and up to 800 I/O connections (if the package size is 15x15mm²). Cu stud plating and height uniformity are critical success factors to ensure a good joining with the upper substrate. (Of course, reduced warpage of the upper substrate is another key success factor of HBW PoP.) Industry will treat this technology as a potential solution to enable a micro/sub-system design in a single package.

In past decades, Moore's law dominated semiconductor trends and led the direction of technology development. The system-on-chip (SoC) concept is now widely used in all kinds of product designs and enhances product competitiveness. Being able to integrate more and more functional blocks into a single chip requires wafer fabrication to quickly migrate to advanced nodes. The complexity of SoC integration, however,

will lengthen the R&D process and weaken product competitiveness from a time-to-market point of view. System-in-package (SiP) and 3DIC (which includes 2.5DIC with silicon interposer) are two technologies that could provide a comprehensive "More than Moore" solution.

System-in-package (SiP) integration

SiP can integrate multi-function chips into a single package and offer a small form factor and a low-cost system solution for many wireless connectivity applications. By utilizing existing package solutions (such as wire bond, flip-chip, hybrid or stacked die), an SiP module can provide a unique opportunity to address cost, performance, and time-to-market.

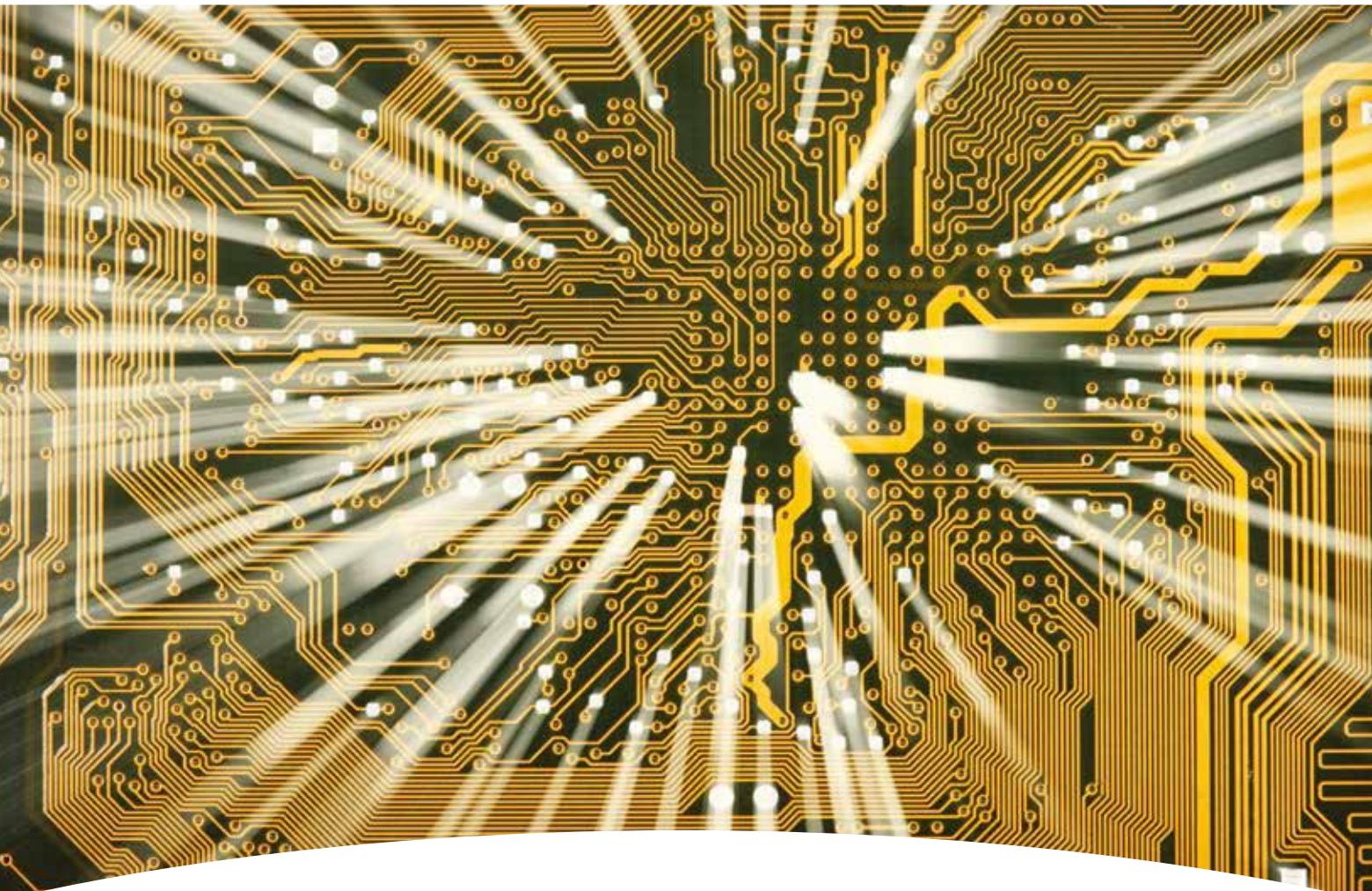
In 2012, more than 70% of SiP modules were used in the cellular phone market and the majority are for RF-related applications. With the continued growth of the cellular market, the importance of SiP technology cannot be ignored.

Besides the cellular phone market, the Internet of Things (IoT) and the wearable devices markets are two emerging applications. Considering the limitations of power consumption and form factor, bluetooth low energy (BLE), and wireless internet connectivity for embedded devices (WICED) will become the major requirements for SiP platforms. As more and more high-frequency wireless devices are integrated into the same package, electromagnetic interference (EMI) shielding will be even more critical. Prevention of intra- and inter-chip interference requires a systematic approach to integration that incorporates all the expertise from electrical, material and mechanical fields. Without a knowledgeable system design capability, it is quite challenging to balance all the individual chip functions. Optical integration is another new challenge that will be important moving forward.

3D IC technology

3D IC technology can be treated as a platform solution to allow end users to integrate multi-function chips, thereby enabling heterogeneous integration in one

reduce soft errors



Deliver more density on flip chip IC packages without increasing soft errors, using low alpha plating anodes.

Honeywell RadLo™ low alpha packaging materials help minimize soft errors and single event upsets by reducing alpha emissions, a significant source of these problems. Our low alpha plating anodes are used in wafer bumping applications for today's high-performance, high-density

devices. We provide Pb and Sn-based plating anodes in various low alpha grades, helping you meet critical alpha emission levels.

Honeywell reliability. Reliable low alpha. In addition to plating anodes, Honeywell RadLo products include solder feedstock and plating solution materials—all backed by our robust supply chain and industry-leading expertise in low alpha refining and metrology.

Honeywell

Find out more by visiting us at www.honeywell-radio.com

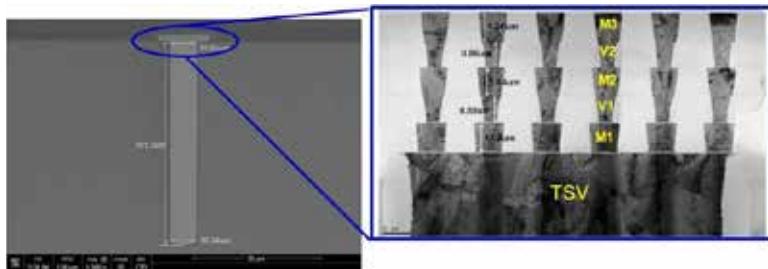


Figure 2: Cross section of a TSV silicon interposer.

package. The major difference between 3D IC technologies and other IC package technologies is the introduction of through-silicon vias (TSVs). TSVs enable the shortest interconnection distance that will reduce the power consumption and enhance speed performance.

Unlike traditional IC packages that have a clear supply chain role established, a new segment of the supply chain — the so called middle-end-of-line (MEOL) — was identified for TSV wafer handling (includes TSV wafer thinning and via reveal). Many wafer foundries and OSATs have built MEOL capability, but it will be end users who will have to decide the

supply chain based on equipment and process capability. Besides a “true” 3D IC technology, industry has developed a passive TSV (known as the 2.5D IC silicon interposer, refer to (Figure 2) that plays the role of interconnecting chips. In the 2.5D solution, chips are placed side by side on top of the silicon interposer and connected by a fine-pitch metal trace and a micro-bump. The benefit of 2.5D IC technology is that there is no need to change the chip design, so it has less impact on time-to-market. Field-programmable gate arrays (FPGAs) and graphics chips will be leading the wave of 2.5D IC technology in the industry.

From a technology point of view, the key challenge 3D IC technologies is thin wafer handling. Thinned TSV wafer handling with temporary bonding/debonding equipment is still new to this industry and requires more time for learning and process improvement.

Summary

The challenges facing the semiconductor industry present great opportunities for semiconductor packaging. Through collaboration, several new package solutions (e.g., SLP, ETS, Cu pillar, PoP, SiP and 3DIC) have been introduced to address the critical requirements for mobile applications. Continuing to press forward with R&D will be necessary to achieve cost-effective solutions.

Biography

Chin-Yu (Max) Lu received his Masters degree in Electrical Engineering from Taiwan National SUN YAT-SEN U. and is Deputy Director of the Engineering Center at SPIL; email maxlu@SPIL.com.tw



BPS-7200HD

Solder ball Attachment System
for All kinds of BGA Packages
on PCB Lamination Strip Form.

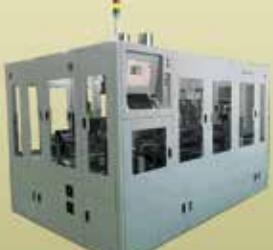
- Max Substrate capacity(mm) : 95x260
- Cycle time : 12~14sec
- Fine Pitch capability(mm) : 0.15ball & 0.30pitch.



BPS-7200FC

Solder ball Attachment System
for Flip Chip Package on Unit
PCB Form with Matrix Boat.

- Max Boat capacity(mm) : 150x310
- Cycle time : 15~28sec
- Fine Pitch capability(mm) : 0.20ball & 0.40pitch.



ASA-7200

Stiffener Attachment system
for Thin Unit PCB and Warpage
Free operation.

- 4 Chase Press by Servo Motor with Easy Conversion
- Stiffener handling : Tube or Tray
- UPH : 1300units.

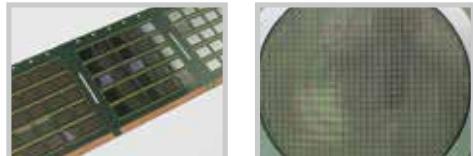
“For additional information, Please visit our website or contact us.”

www.sspinc.co.kr sale@sspinc.co.kr +82-32-822-0881~4

FLIP CHIP BONDER

All New "10" Advanced Features!

- High Productivity
- Precision Bonding Capability
- Flux Vision Inspection Function
- Auto Flatness Check Capability
- Wafer Map Shift Prevent Function
- Foreign Material Detect Inspection System
- Chip Out Detect Inspection System
- Lower Vibration Control System
- User Friendly MMI for Easy Operation
- Lower Temperature Control



FLIP CHIP BONDER-A110



■ General Specifications

SECTION		FLIP CHIP BONDER-A110
PRODUCTIVITY	UPH	15,000 (Based on Dry Run)
ACCURACY	X-Y PLACEMENT	±6µm @ 3σ
	CHIP ROTATION(θ)	±0.1µm °@ 3σ
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)
FOOTPRINT	DIMENSION (LxWxH)	1,600(L) x 2,200(W) x 2,000(H)
	WEIGHT	2,600kg



Semiconductor

#532-2, Gajwa-Dong, Seo-Gu, Incheon, 404-250, Korea
TEL. +82-32-571-9100 www.hanmisemi.com

INDUSTRY NEWS

BiTS Workshop – The Next 15 Years



BiTS Steering Committee.

Wow! The Burn-in and Test Strategy (BiTS) Workshop just turned 15! The world of semiconductors has certainly changed over the years. And the BiTS Workshop has kept up with what is “Now & Next” in the burn-in and test of packaged integrated circuits (ICs). These achievements were celebrated in style by

the more than three hundred participants at the recently held 2014 BiTS Workshop in Mesa, Arizona.

“When the BiTS Workshop started in 2000, there were no practical forums for test engineers and managers to discuss solutions to the challenges of burn-in and test,” said **Fred Taber**, BiTS Workshop General Chairman. “BiTS has become the premier global go-to resource to learn what works

in test and burn-in. International interest has continued to increase as forty percent of the attendees were from overseas. From consumables - such as sockets, load & burn-in boards, and wafer-level chip scale packaging (WLCSP) probe cards – to capital equipment – to new test strategies, we have it all.”

The excellent technical program spanned three days with twenty two papers plus three

featured speakers and two poster sessions. Sunday, the Tutorial Day, started with **Peter Ehlig** (Texas Instruments Fellow) “Test 101: A Holistic View of Test” followed by a TechTalk by **Jeffrey L. Roehr** (Texas Instruments) “The Most Common Mistakes in Test”. These extended in-depth presentations were greatly appreciated by everyone.

Two excellent market overviews examining trends in package technology “book-ended” the technical program. The Distinguished Speaker **Brandon Prior** (Prismark Partners) kicked things off Sunday night with “Packaging And Interconnect Trends: QFN, WLCSP, Fine Pitch And Modular/3D Solutions.” Invited Speaker **E. Jan Vardaman** (TechSearch International) closed the program Wednesday with “Trends in Wafer Level Packaging: Thin is In!”

In his Keynote Address, “Interconnectology

Expect More From Your Burn-In Equipment

The TAHOE Burn-in Test System

By Incal Technology

- High or low power use
- Individual DUT Temperature or Chamber Temperature Control
- 24 independent BIB slots. Each slot has:
 - Twelve 54-Amp power supplies
 - Four 12-Amp power supplies
 - 160 on-the-fly bidirectional channels
 - Four independent analog channels
 - Tristate per pin
 - Monitor for vector output or sign of life
 - Measure individual DUT voltage and current
 - Datalog everything!
 - Plus more...



Celebrating our 25th Year in Business

510.657.8405 | www.incal.com

– The Road to 3D”, **Simon McElrea** (Invensas Corporation) explained the drivers for advanced packaging including next generation package-on-package (PoP) and 2.5/3D integration technology. As classical photolithography scaling no longer provides the cost savings required at advanced nodes to keep track with Moore’s Law, advanced packaging enables

reputation for excellence. Rest assured the technical program and exhibits will continue to provide great insight into what is “Now & Next”.

This year’s presentations are already available in the Premium Archive at www.bitsworkshop.org. The multimedia versions –

audio synchronized with the presentation slides – are in the process of being posted. Since early submissions are eligible to win a prize, we are happy to receive your abstracts for 2015 now!

Looking forward to seeing you at the next BiTS Workshop in Mesa, Arizona March 15-18, 2015!



Simon McElrea, Fred Taber.

greater functionality at lower costs.

There was plenty to explore at the BiTS EXPO. For the fifth year in a row, the EXPO sold-out early with fifty-one exhibitors, requiring expansion into an adjacent ballroom. In addition to meeting with the exhibitors, attendees enjoyed great food and drink during the EXPO.

Besides working hard to learn and explore, there was plenty of time for networking to meet new colleagues and catch up with old friends. An extra special social event “Celebrando BiTS” - complete with Mexican culinary treats and an authentic Mariachi band - was held in honor of the 15th anniversary. The perfect weather made for an enjoyable celebration to drink margaritas and beer poolside!

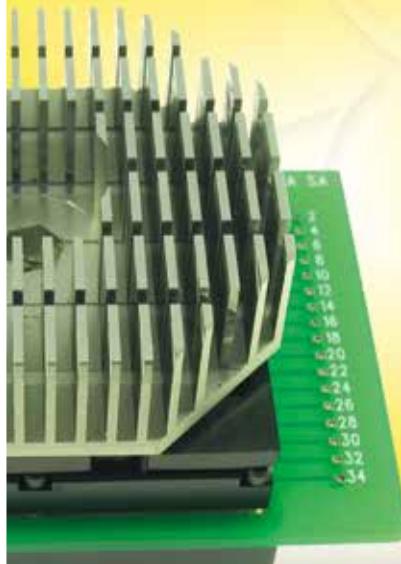
Looking forward to the next fifteen years, I am honored to serve as the General Chairman of the BiTS Workshop starting in 2015. **I promise to work hard to make BiTS the best event for everyone in test and burn-in!** The committee and I will continue to improve the BiTS Workshop to maintain its well-earned



Ira Feldman.

GHz BGA/QFN Sockets 0.3mm to 1.27mm

Industry's Smallest Footprint



- Up to 500,000 insertions
- Bandwidth up to 40 GHz
- 2.5mm per side larger than IC
- Ball Count over 3500, Body Size 2 - 100mm
- Five different contactor options
- Optional heatsinking to 100W
- Six different Lid Options
- <25 mOhm Contact Resistance throughout life



**Ironwood
ELECTRONICS**
www.ironwoodelectronics.com

1-800-404-0204



The 64th Electronic Components and Technology Conference (ECTC)
Walt Disney World Swan and Dolphin Resort
Lake Buena Vista, Florida, USA
May 27 - 30, 2014

The Program and Executive Committees invite you to join the 64th Electronic Components and Technology Conference (ECTC). This premier international conference is sponsored by the IEEE Components,



Alan Huffman
64th ECTC Program Chair

Packaging, and Manufacturing Technology Society (CPMT).

The ECTC Program Committee has selected more than 300 papers that will be presented in 36 oral sessions and 5 interactive presentation sessions, including a student interactive presentation session. The oral sessions will feature peer-reviewed papers on 3D and TSV technologies, wafer level packaging, electrical and mechanical modeling, RF packaging, system design, and optical interconnects. Session topics will cover advanced packaging technologies, material development and characterization, reliability, assembly and manufacturing, and interposers. Four interactive presentation sessions showcase peer-reviewed papers in a format that encourages more in-depth discussion and interaction with authors about their work. Similarly, the student interactive presentation session will focus on the research being done at academic institutions

around the world by emerging scientists and engineers. The Program Committee has created sessions covering the ongoing technological challenges of established disciplines, as well as addressing emerging topics of interest to the industry. Authors from companies, research institutions, and universities from more than 25 countries will present their work at ECTC, illustrating the conference's global focus.

ECTC will also feature panel and special sessions with industry experts covering a number of important and emerging topic areas. On Tuesday, May 27, Karlheinz Bock of Fraunhofer EMFT & University of Berlin will chair a session entitled "Flexible Electronics - Packaging Technology and Application Trends" where a panel of experts will discuss the recent advancements and market perspectives for this emerging technology area. Tuesday, Manos Tentzeris of Georgia Institute of Technology will chair a special session

CSC Pure Technologies

CSC PURE TECHNOLOGIES
426033, Izhevsk, 50 let Pionerii str., 41, Russia,
Tel.: +7 (3412) 736812 Fax: +7 (3412) 736820
e-mail: info@cscptech.com
<http://www.cscptech.com>

The last word in low alpha materials

CSC Pure Technologies (ISO 9001 certified) has extensive experience in manufacturing ultra Low Alpha (LA) Solder Alloys (Lead-Free and Lead-Tin), LA Lead, LA Tin in the form of cylinders, slugs, rods, flakes, spheres, any kind of LA Anodes, LA PbO and LA SnO powder with alpha emission from 0.01 cph/cm² to 0.001 cph/cm² and less.

For more information, visit: www.cscptech.com

sponsored by the Electronic Components & RF technical subcommittee on “Wireless Power Transfer Systems.” The ECTC Panel Discussion “Emerging Technologies and Market Trends of Silicon Photonics” on Tuesday, May 27 will be chaired by Ricky Lee of Hong Kong University of Science and Technology and Jie Xue from Cisco Systems with panelists from various segments of the industry to discuss the growing influence of photonics technologies on microelectronic systems. Nancy Stoffel of GE Global Research will chair the ECTC Plenary Session titled “Influence of Packaging on System Integration and Performance” on Wednesday evening where a panel of experts will discuss system integration and the role that component packaging technologies play. On Thursday evening, the CPMT Seminar titled “Latest Advances in Organic Interposers” will be moderated by Kishio Yokouchi of Fujitsu and Venky Sundaram from Georgia Institute of Technology will be Supplementing the technical program. Technology Exhibits will be open Wednesday and Thursday. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions. Dr. Peter Bocko of Corning Glass Technologies will be the invited keynote speaker at the ECTC Luncheon on Wednesday.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something for everyone in the packaging industry. Make your plans now to join the 64th ECTC and be a part of the exciting technical and professional opportunities. A special thanks to *Chip Scale Review* the Official Media Sponsor which for 5 years running provides ECTC with world-class coverage.



Last Call for Papers for IWLPC
The 11th Annual International Wafer-

Level Packaging Conference & Tabletop Exhibition is open through April 18th.

Submit an abstract at www.iwlpc.com related to Wafer-Level, 3D Package Integration or MEMS Packaging. For more information

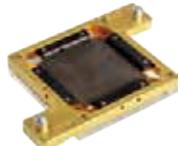
contact Keith Cooper of SET North America General Chair kcooper@set-na.com or Steven Xu of Qualcomm Technical Chair at stevenxu@qti.qualcomm.com www.iwlpc.com



WinWay Technology Co., Ltd.

The Partner You Can Trust in Testing

while you are engineering the future



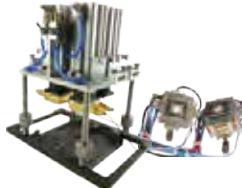
Test Socket for Engineering and High Volume Production

- * PoP Socket
- * Coaxial Socket
- * CIS Module Socket
- * Elastomer Socket



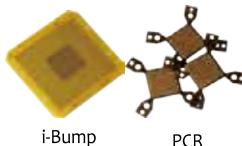
Probe Card for ATE Traditional and Direct Dock Wafer Testing

- * WLCSP Probe Card
- * Direct Dock Probe Card



Active Thermal Controller for Characterizing Your Product in Low and High Temperature

- * Manual ATC
- * Plunger ATC
- * Seiko Epson Handler ATC Changeover Kit

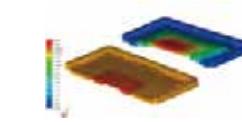


Contact Elements for Satisfying Various Test Requirements

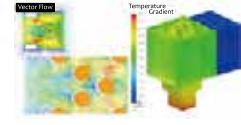
- Spring Probe
- W-Pin



RF Measurement & Simulation



Mechanical Simulation



Thermal Simulation

We Provide Comprehensive Worldwide Support

 <http://www.winwayglobal.com>

 sales@winwayglobal.com



Advancements in package-on-package (PoP) technology for next-generation smartphone processors

By Hamid Eslampour, SeongWon Park, HanGil Shin, JaeHan Chung, YoungChul Kim [STATS ChipPAC]

Package-on-package (PoP) has become a dominant packaging technology in high end smartphones and tablets, and is increasingly being adopted in the mid- to low-end market where cost is a critical factor. While the benefits of vertical integration are clear – shorter signal path between the memory and application processor (AP) device, better signal integrity, and faster data rate transfer – further reductions in overall package height are required to meet market demand for mobile products that are thinner and have smaller form factor. The continuous demand to achieve lower package heights, smaller package footprint, and higher memory speed is pushing advancements in PoP technology and memory interface (MI) pitch reduction.

Two main PoP package types addressing this trend are bare die and molded laser-via package (MLP). Bare die PoP offers the lowest height and lowest package cost compared to other PoP configurations. Bare die PoP has been typically used for applications with MI pitch of 0.65mm or 0.50mm. However, in applications where aggressive package height reductions or 0.4mm MI pitch is required, MLP has gained traction in addressing height reduction, partly due to its superior warpage performance. Introduced in the market in late 2010, MLP unfortunately comes with a cost premium, which is an issue for cost sensitive markets such as low-end smartphones. Recent developments in bare die PoP, on the other hand, have resulted in a very thin 1.2mm maximum stack height with a 0.4mm MI pitch as a lower cost mobile market package solution.

Background

Bare die PoP has been in volume production for some time. PoP

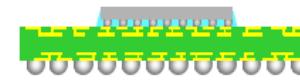
package technologies in general are measured and designated by a few key metrics including MI pitch, BGA pitch, and, most importantly, package height. The key performance metric that all PoP package types must adhere to, in addition to the typical reliability requirements, is package co-planarity and package warpage, both in high temperature (HT) and room temperature (RT).

Historically, bare die PoP packages were reserved for applications with MI pitch of 0.65mm or 0.50mm. A pitch of 0.4mm MI was not considered feasible in bare die PoP due to the stack geometries and tight vertical clearances between the top and bottom package imposed by this pitch. Additionally, the push to achieve thinner package heights posed challenges in meeting package warpage and co-planarity specifications [1]. As a result, in applications where aggressive package height reductions were required or 0.4mm MI pitch was required, MLP was adopted as the ideal solution. MLP, with its over-mold configuration, provides better warpage performance

compared to bare die PoP, especially at RT. Additionally, because of its inherent structure of embedding solder balls on the MI pads, MLP provides acceptable vertical clearance between the top and bottom package at 0.4mm MI pitch. Unfortunately, although MLP provides a robust solution for 0.4mm MI pitch, it does so at a premium because of added process steps and differences in strip design. These additional costs make MLP a problematic solution in some cost sensitive segments. Further developments in bare die PoP, however, have achieved 0.4mm MI pitch, resolving the vertical clearance issue through the adoption of Cu column flip-chip (FC) bumps and bond-on-lead (BOL) [2-4].

Package trends

MI pitch reduction is usually associated with pin count increase in the top memory package and enables higher input/output (I/O) pins for higher data transfer rate. Typically, bare die PoP packages have die thickness of 100 μ m with die height above the substrate measuring around



	2009	2010	2011	2012-13
Die size (mm)	7x7	5x5~8x8	8x8	~10x9~11x10
Die thickness (μ m)	100	100	100	100
FC bump pitch (μ m)	180	150~160	230	150
Pkg size (mm)	14x14	12x12~14x14	12x12	14x14~15x15
Substrate type/ Core thickness (μ m)	1-2-1 PPG/ 150 μ m	1-2-1 PPG/ 100~150 μ m	1-2-1 PPG/ 250 μ m	1-2-1 PPG/ 150~200 μ m
Core CTE (ppm/ C)	10~11	10~11	6~7	3~4
MI pitch / BGA pitch (mm)	0.5/0.5	0.5/0.4	0.5/0.4	0.5/0.4
Max pkg height (mm)	0.76	0.77~0.8	0.85	0.7~0.75
Co-planarity spec (μ m)	120 μ m	120 μ m	80 μ m	120~160

Table 1: Bare die PoP package features and trends.

40+ years of perfect pitch.



And now, the perfect name



Qinex [kuh-neks] 1. Over 40 years of reliable burn-in and custom connections; 2. Quality interconnects for **nex**-gen solutions.

Introducing Qinex, the new brand name for superior interconnection solutions from Sensata Technologies. Qinex, the new word in perfect pitch.

QUALITY. High-value interconnection solutions since 1970.

- 24/7 global engineering
- 24/7 global support teams
- Local engineering and sales
- Six Sigma quality management
- Proven, reliable high-volume manufacturing
- Expert molding, design, and customization

INNOVATION. More I/O choices, smaller form factors, superior performance in less time.

- Latest 3D design tools
- On-site model shops
- Rapid prototyping
- Advanced thermal analysis
- Design on demand
- Broad range of innovative contact designs

PARTNERSHIP. In a fierce global market, only Qinex reliably supports the innovation, reputation and competitiveness of your business. We'll work with you to get it right, the first time.

**40+ years of perfect pitch.
And now, the perfect name.**

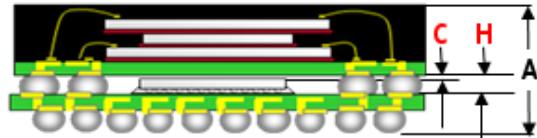


WEB www.qinex.com

EMAIL qinex@sensata.com

CALL 1-508-236-1306





Top ball (MI) pitch	0.5mm	0.4mm
# of memory I/O	2 rows, 168 balls	2 rows, 216 balls
Cavity size	9.3x9.3mm	9.9x9.9mm
Top pkg ball height (post reflow)	0.25mm	0.18mm
Die thickness	100µm	60µm
Collapse height (H)	0.21mm	0.14mm
Clearance between top & bottom pkg (C)	0.03mm	0.02mm

Table 2: Bare die PoP comparison, 0.5mm vs. 0.4mm MI pitch.



Package Type	MLP PoP		MLP PoP-ED**
MI pitch (mm)	0.5	0.4	0.4
Mold cap (um)	280	250	150
Die thickness (um)	100	100	100
Substrate / Core thickness (um)	1-2-1/ 100um	1-2-1/ 100um	1-2-1/ 150um
Max pkg height (mm)	0.82	0.78	0.72
Co-planarity (um)	100	100	120

* MLP PoP Exposed Die (ED)

Table 3: MLP PoP package configurations and typical package height for 0.5 and 0.4mm MI pitch.

160-180µm, depending on the bump pitch and diameter used in the FC die. Substrate thickness, which depends on core thickness, type of dielectric layer, and number of build-up (BU) layers, typically measures around 400-500µm. BGA ball pitch, which in earlier designs measured at 0.5mm, is now almost exclusively seen in 0.4mm pitch to allow for higher number of BGA balls for power/ground and I/Os, and allows reduction of the package body size that would have otherwise resulted in higher package cost. **Table 1** shows the trends in bare die PoP.

Meanwhile, in an effort to increase double-data rate (DDR) memory data transfer rate or bandwidth, and to lower overall stacked PoP package height, MI pitch reduction from 0.5mm down to 0.4mm was needed, and the JEDEC memory package outline for 0.4mm

BGA pitch was defined as a result. MLP PoP was soon developed to address market demand for package height reduction and, in some cases, the need for further improvement in package co-planarity for robust board mount and surface mount yield. The advent of MLP further enabled the reduction of MI pitch to 0.4mm.

Table 2 shows the issues encountered in bare die PoP at 0.4mm MI pitch, comparing the same bare die package with 0.5mm MI pitch. Because of the reduction in collapse height dimension, H, caused by the smaller BGA solder balls used for the 0.4mm memory package BGA pitch, the package-to-package clearance, dimension C, is reduced from 50µm nominal to 20µm nominal even after thinning the Si die from 100µm down to 60µm. On the other hand, MLP with 0.4mm MI

pitch provides the same 50µm nominal package-to-package clearance as with 0.5mm MI pitch through the proper scaling of top solder ball size and mold cap, while still using a 100µm die thickness.

The co-planarity improvement that is realized with MLP over bare die PoP is due to the use of over-mold or mold cap, which is inherent in the MLP package configuration. Mold shrinkage and other mold cap material properties, such as glass transition temperature (T_g) and modulus, are modulators that can be optimized to provide a more flat package at RT and improved co-planarity. The presence of the mold cap also allows for reduced package height through implementation of film-assisted molding (FAM) that enables molding of the package with die backside being exposed and flushed to the mold top. **Table 3** shows conventional MLP with over-mold and the exposed die (ED) version that is achieved using the FAM process.

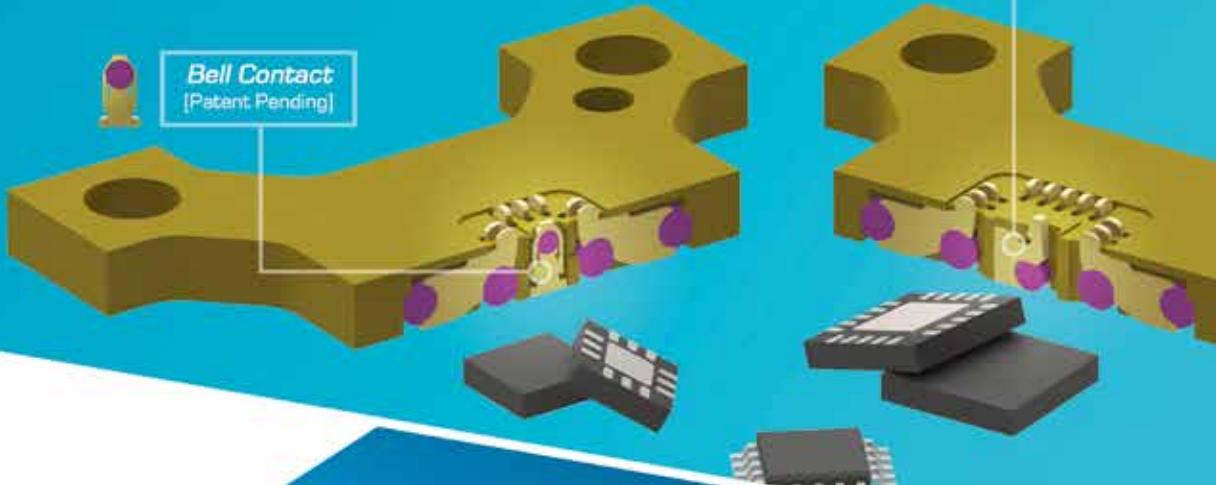
Height reduction in MLP can be achieved through reduction of die thickness, reduction of FC bump stand-off height that is enabled by converting FC solder bumps to Cu column, and further reduction of substrate thickness. **Table 4** shows a number of MLP package options where the bottom package height is reduced from 0.82mm down to 0.59mm. Some of these package options are in development today, and the main challenge is conformance to co-planarity and RT/HT warpage, especially as package thickness is further decreased.

Further advancements utilizing Cu column technology, however, have achieved a lower cost bare die PoP package, which is now qualified with 0.4mm MI pitch. This technology features Cu column and BOL processes that enable lower die stand-off height [5]. This decreased stand-off height results in more space between the top memory package and bottom package, thereby providing a robust solution for PoP stacking and surface mount technology (SMT) operation. Additionally, the use of Cu column and BOL technology offers a number of further cost reduction benefits resulting from substrate design rule



Need Compliant Grounding for
small packages of 2x2 and above?*

We have the solution.



Need Short Wiping of 0.1mm
for your wettable/dimple pad?*

We have the solution.

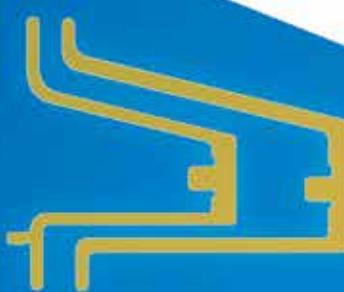


Zigma
[Patent Pending]

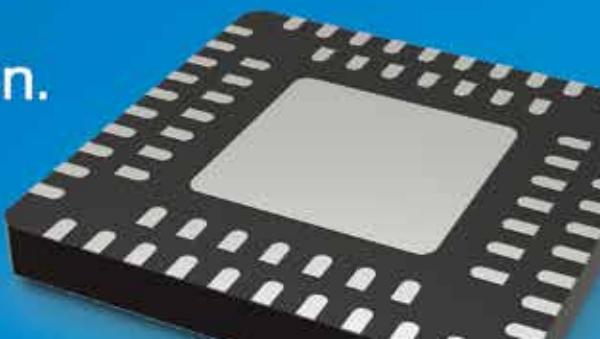


Need Scrubbing
Solution for Dual
Row packages ?*

We have the solution.



Alpha
[Patent Pending]



Explore these
new exciting and
outstanding solutions on
our website or with our nearest
sales channel partner today.

Find out more at:
<http://www.jftech.com.my>
World class company in semiconductor industry

Or e-mail us at:
sales@jftech.com.my



Flip-Chip Technology & PoP Trends

	0.82mm	0.70mm	0.67mm	0.62mm	0.59mm	Thinner PoP
Max height	0.82mm	0.70mm	0.67mm	0.62mm	0.59mm	
Bump pitch (inline)	150um	130um	100um	80um	60um	
Interconnect	Solder bump		Cu column			
Bonding			Mass Reflow			

Table 4: MLP PoP package height reduction trends.

simplification, elimination of tight solder resist registration (SRR) rules, and elimination of solder-on-pad (SOP) [3,6].

Characterization of low-cost bare die fcPoP

The package used for characterization of bare die PoP with 0.4mm MI pitch was a 12x12mm body size, 6-layer substrate with pre-preg (PPG) BU, core thickness of 150µm, and BGA ball pitch of 0.4mm. The maximum package height including all tolerances is estimated at 0.73mm based on 70µm FC die thickness.

The Si used in this package was a 32nm extra-low-k (ELK) daisy-chain die so that open/short testing and white bump (WB) screening could be done to validate the integrity of the chip-attach (CA) process and feasibility of using Cu bumps in combination with the fragile ELK layers. The Cu column bumps on die and BOL trace design on substrate implemented design rules with open solder resist, non-solder mask defined (NSMD) pads, and non-solder-on-pad (NSOP), which all result in a lower cost substrate [5]. The schematic of Cu column and substrate trace design (BOL) is shown in **Figure 1**.

The Cu column with lead-free SnAg

solder cap dimensions were designed so that the bump stand-off height measures to 35µm nominal. The peripheral I/O pitch on this device was 120µm bump pitch with one escape trace routed between the bumps, resulting in an effective bump pitch of 60µm. As such, the Cu column was designed to have a maximum diameter of 60µm as shown in **Figure**

1. The capillary underfill (CUF) process with these gap heights was previously qualified in other PoP devices, with actual production experience, validating the high-volume manufacturing (HVM) capability of this process [5]. **Figure 2** shows the UF fillet shape achieved at both dispense and exit side with a 70µm-thick die used in the process.

To further validate the robustness of the CA process with respect to interlayer dielectric (ILD) cracks or WB, a multi-

reflow hammer test post-CA and without UF was performed, and, as shown in **Table 5**, no WBs were detected in up to 30 cycles of reflow test conducted using two core thicknesses of 150µm and 100µm. The robust margin seen with respect to the ILD crack is partly due to the reduced flip-chip joint stresses achieved through the Cu column and BOL design, which has proven to increase the ILD crack process margin through both experimental data and modeling validation [7].

Package co-planarity and RT/HT warpage performance are critical to successful qualification of PoP packages

Run	Sample Size	Substrate Layer	Multiple Reflow (unit: s)						
			0x	10x	15x	18x	20x	25x	30x
1	100	150um core, 6L	0/100	0/100	0/100	0/100	0/100	0/100	0/100
2	100	100um core, 6L	0/100	0/100	0/100	0/100	0/100	0/100	0/100

Table 5: Multi-reflow hammer test results on 32nm ELK Si up to 30 cycles.

in general. Co-planarity data, shown in **Figure 3**, meets the 80µm specification limit with adequate process C_{pk} ; thermo moiré warpage plot indicates a maximum HT warpage of 60µm, which meets the 80µm specification required in most applications. **Figure 4** contains a cross section of an actual pre-stacked PoP package illustrating a top memory package stacked on a bottom package, with actual stack height measuring less than 1.26mm.

MLP PoP advancements and height reduction

As noted, the benefits of MLP PoP include smaller MI pitch, reduced package height because of the effect of mold compound shrinkage on package height and protection of the thin FC die by mold cap that would have otherwise been exposed to die crack and damage due to handling and socket testing during final test. Additionally, MLP offers the capability to increase die size within the same package body size. This is achieved through the adoption of a molded underfill (MUF) process, which is not applicable to bare die PoP that employs CUF instead.

MUF has been developed and qualified on various package types and was also recently qualified on a 14x14mm

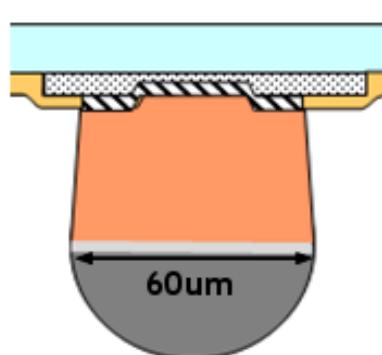


Figure 1: Cu Column and BOL design.

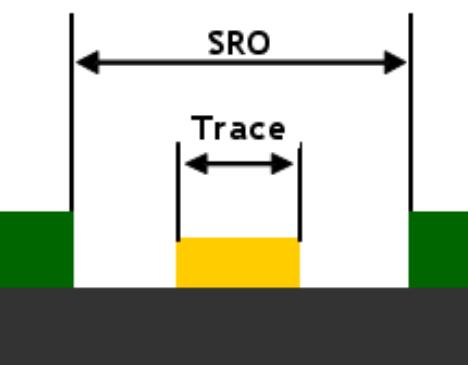


Figure 2: CUF process and UF fillet at dispense and exit side with 70µm thick FC die.



KYZEN

All around the world Kyzen cleaning experts work with our customers to find the best possible solution to their cleaning challenges.

With Kyzen You Can Expect:

- ✓ Increased Product Reliability
- ✓ Residue Removal From Fine Pitch and Low Standoff Packages
- ✓ The Latest Cleaning Technology and Process Design
- ✓ Experienced Process Engineers
- ✓ Environmentally Friendly Solutions
- ✓ Proven Results

 **KYZEN**

Nashville, USA ♦ Manchester, USA ♦ Maldegem, BE
Penang, MY ♦ Shenzhen, CH ♦ Shanghai, CH ♦ Guadalajara, MX

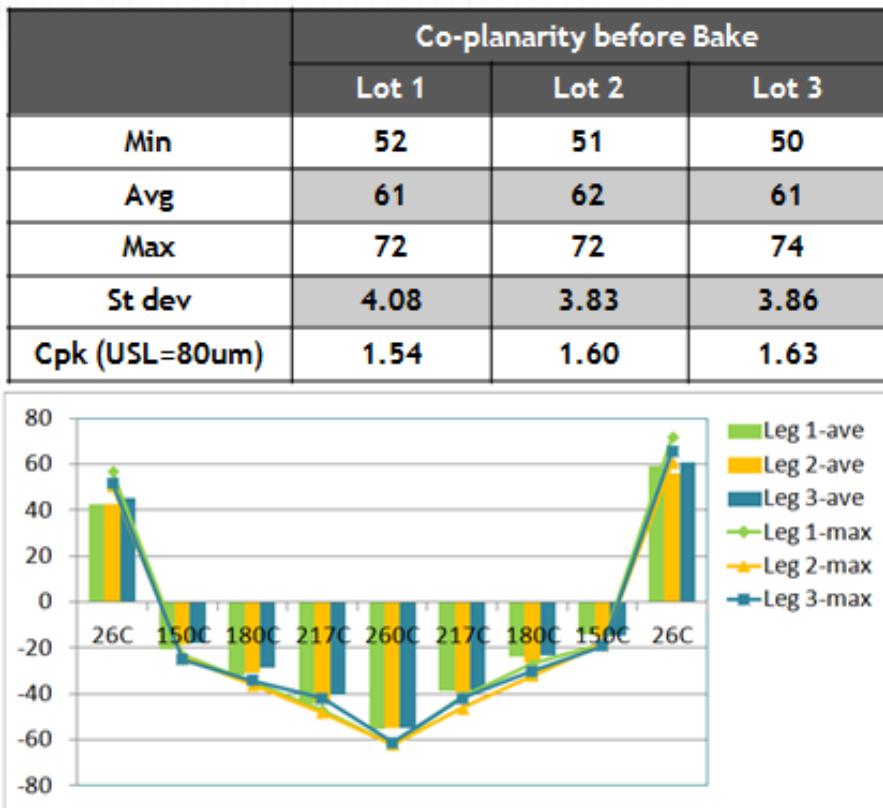


Figure 3: Package co-planarity and thermo moiré warpage plots.

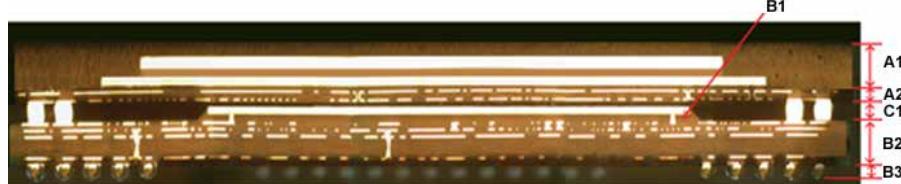


Figure 4: Cross section of a pre-stacked PoP package with two die stacked on top of the memory package.

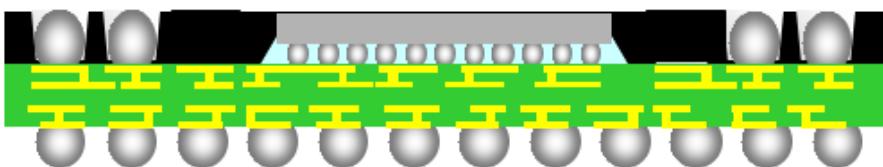


Figure 5: MLP PoP ED package with CUF.

Leg #	Substrate	Pre-Preg	SubT (mm)	Bottom Pkg T (max) mm	Min	Max	Avg	Std	Cpk (100um)
1 *	200um Core, 4L	25um PPG	0.36	0.70	68	95	81	4.18	1.49
2 *	200um Core, 4L	35um PPG	0.36	0.70	66	86	78	3.81	1.95
3 *	200um Core, 4L	31um PPG	0.36	0.70	62	85	72	3.25	2.89
4 *	150um Core, 4L	25um PPG	0.31	0.65	97	132	114	5.61	-0.81
5 *	150um Core, 4L	31um PPG	0.31	0.65	92	117	104	4.26	-0.33
6 *	100um Core, 4L	35um PPG	0.26	0.60	123	159	138	6.07	-2.08

* EMC material = A

Table 6: 14x14mm MLP PoP ED co-planarity vs. range of core thicknesses.

MLP package with die size as large as 11x11mm and with bump pitch down to 150μm, using a 28nm fab node Si. As a result, in those cases where both MLP and bare die PoP are potential package options, the MLP value proposition is the larger die size, its better co-planarity and RT warpage performance.

Figure 5 shows the schematic of MLP PoP with FAM process, known as MLP PoP ED (exposed die), with 0.40mm MI pitch, using CUF. This package with 14x14mm body size and 10x10mm die was characterized using 4-layer PPG BU substrates with various core thicknesses, including 100μm, 150μm and 200μm. Mold compound type and material properties were previously optimized for package warpage, and the various substrate thickness options were evaluated for their corresponding package warpage performance. **Table 6** shows the package co-planarity based on a number of core thicknesses and PPG thicknesses, and illustrates that an acceptable co-planarity Cpk with a 200μm core is achievable while maintaining a maximum package height of 0.70mm. **Figure 6** shows the HT warpage at peak reflow temperature of 260°C for each leg, where 200μm and 100μm core thicknesses meet the maximum 80μm HT warpage requirement.

A pre-stack evaluation of the package shown in **Figure 5** with various substrate core thickness samples and two different ball sizes for a top memory package was conducted. Actual package heights based on sample cross section measurements are shown in **Table 7**. Based on the top memory package thickness, using 150μm core thickness and 200μm BGA ball size for the top memory package, a total pre-stack package height of less than 1.1mm is achieved.

Summary

PoP has become the mainstream package technology for smartphones because of the level of integration it provides in this segment of the mobile handset market where space limitation and height reduction are the main drivers. Package options, such as smaller MI pitch and the evolution of



HT warpage (at 260C peak reflow temp)

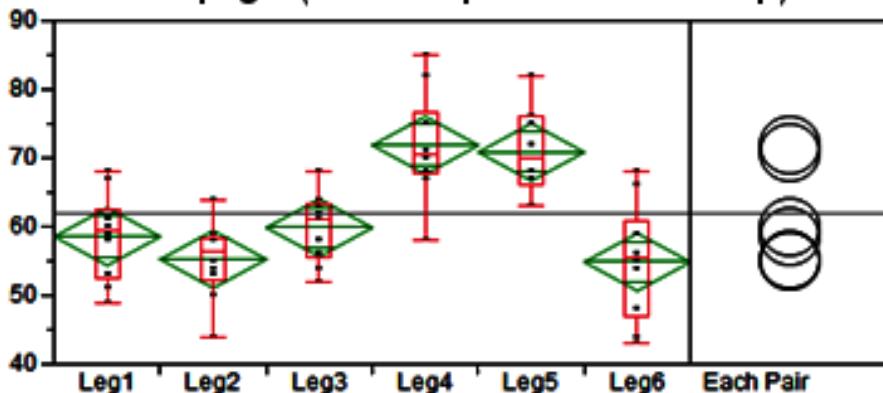
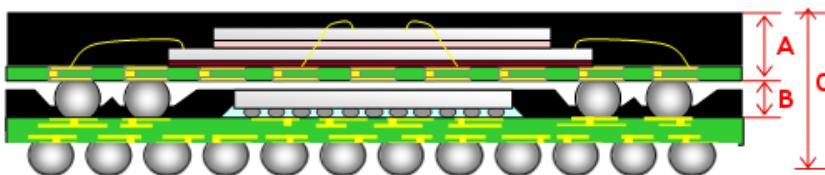


Figure 6: 14x14mm MLP PoP ED HT warpage vs. range of core thicknesses.



Core Thickness/ Core Type	Memory Pkg BGA Ball Size (um)	A (top pkg thickness)	B (PoP ball height)	C (total pkg thickness)
150um / A	250	488.4	212.4	1102.9
	200	494.0	167.8	1088.3
150um / B	250	490.1	205.6	1128.9
	200	494.0	165.8	1115.3
100um / A	250	493.4	216.4	1092.7
	200	490.8	165.3	1084.6

Table 7: MLP PoP ED pre-stack height vs. substrate core thickness.

the conventional MLP PoP with over-mold to an exposed die configuration, have been developed to address the demand for lower package heights, smaller package footprints, and higher memory speeds. While MLP PoP ED with 0.4mm MI pitch enables lower package height and provides a higher number of memory interface I/Os for increased memory bandwidth, it comes with a cost premium. By leveraging the Cu column and BOL design, bare die PoP with 0.4mm MI pitch was developed and qualified to become the lower cost package option.

There are a number of trade-offs between the two package types noted above with respect to package warpage and co-planarity performance and their scalability beyond 0.4mm pitch.

An additional benefit of MLP is the realization of larger die size through the use of the MUF process. Going forward, MLP will be the vehicle of choice to meet 1.00mm maximum package pre-stack height requirements, and is in development today. Further increase in memory I/O will be possible by reduction of MI pitch beyond 0.4mm.

References

1. H. Eslampour, et al., "Advanced thin PoP technology," IMAPS Conf. 2011.
2. M. Joshi, et al., "CuBoL (Cu column on BoL) technology: a low-cost flip-chip solution scalable to high I/O density, fine bump pitch and advanced Si node," Proc. 61st Elec. Comp.

and Tech. Conf., FL, May 2011.

3. R. Pendse, et al., "Low cost flip-chip (LCFC): an innovative approach for breakthrough reduction in flip-chip package cost," Proc. 60th Elec. Comp. and Tech. Conf., Las Vegas, NV, June 2010.
4. US Patent Nos.; US7368817, US7700407, US8188598, US8076232, US7973406 and US7901983. R. Pendse, "Bond-on-lead flip-chip interconnection," Nov. 2004.
5. H. Eslampour, et al., "Low cost Cu column fcPoP technology," Proc. 62nd Elec. Comp. and Tech. Conf., San Diego, May 2012.
6. H. Eslampour, et al., "fcCuBE™ technology: a pathway to advanced Si-node and fine-pitch flip-chip," Proc. 62nd Elec. Comp. and Tech. Conf., San Diego, May 2012.
7. E. Ouyang, et al., "Improvement of ELK reliability in flip-chip packages using bond-on-lead (BOL) interconnect structure," Proc. IMAPS Conf., Oct. 2010.

Biographies

Hamid Eslampour received his MS in Mechanical Engineering from San Diego State U. and is Director of Business Development at STATS ChipPAC; email hamid.eslampour@statschippac.com

SeongWon Park received his BS in Metallurgical Engineering from Korea U. and is Senior Manager of R&D at STATS ChipPAC Korea.

HanGil Shin received his BS in Electronic Engineering from Kyungwon U. and is Manager of R&D at STATS ChipPAC Korea.

JaeHan Chung received his BS in Electronic Engineering from Kyungnam U. and is Deputy Director of R&D at STATS ChipPAC Korea.

YoungChul Kim received his BS in Metallurgical Engineering from Hanyang U. and is Senior Director of R&D at STATS ChipPAC Korea.

Simulation of 3D IC fabrication

By Sudarshan Krishnamoorthy, Xiaopeng Xu [[Synopsys](#)]

Over the last several years, the semiconductor industry has made significant strides in demonstrating the technical feasibility of 3D IC integration. From the point of view of process development and transistor performance, the fabrication and integration of TSVs within a 3D IC system presents a number of challenges that, though manageable, need to be taken into account. Copper is the material of choice for the via conductor because of its excellent electrical conductivity and pervasiveness in modern interconnect stacks. However, copper and silicon have very different coefficients of thermal expansion. Because the TSV fabrication steps involve thermal operations, the thermal mismatch of these materials induces stresses in the silicon surrounding the TSV. These stresses in turn alter the carrier mobility and drive of the transistors fabricated in the proximity of the TSV, by way of the same piezoelectric effect in silicon that is responsible for boosting the transistor performance in strained-silicon technologies. This so-called TSV stress proximity effect has a range of several microns and can either produce enhancement or degradation of the current. In addition to the TSVs, the micro bumps used for inter-die connections and the solder bumps, used to attach the die stack to the bumps, also induce stresses in their proximity. High stress levels can also affect the structural integrity of the 3D IC with adverse consequences to the reliability.

In this article we discuss the application of technology computer aided design (TCAD) modeling software called Sentaurus Interconnect to the simulation of the stress resulting from the 3D IC fabrication process and its impact on the reliability and performance of the 3D IC.

Complexity of 3D IC manufacturing

A typical 3D IC structure utilizes

through-silicon vias (TSVs) to interconnect silicon dies that are bonded together using micro-bumps [5]. As shown in **Figure 1**, the stacked structure is a complex assembly of various materials with very different thermal and mechanical properties.

The constituent materials, which include silicon, low-k dielectrics, oxide, copper, and under-fill, are exposed to multiple thermal ramps during fabrication and stacking. During wafer fabrication, intrinsic stresses are introduced when thin films are deposited. In addition, the process steps and thermal ramps involved in the fabrication process introduce thermal mismatch stresses because of the difference in the coefficient of thermal expansion (CTE) of the materials comprising the stack, particularly surrounding the TSVs. Wafer thinning, die singulation, stacking and packaging add further stresses. The final stress distribution can affect the structural integrity and reliability of the 3D IC. Moreover, as silicon is a piezoresistive material, stresses can also affect transistor performance.

3D IC manufacturing process and stress effects

Figure 2a shows the process steps used to fabricate a 3D stack containing two die, TSVs and micro-bumps [7]. This sequence uses a typical via-middle technique and serves as an example for analysis discussed in this article.

The TSV and micro-bump layout is shown in **Figure 2b**. For Die 1, the TSV fabrication is performed after front-end-of-line (FEOL) processing. TSV process steps include deep etching, barrier deposition, copper plating and filling. **Figure 2c** shows the intermediate structure after the TSVs are formed inside the bottom die. After the TSV formation, the back-end-of-line (BEOL) process is performed on the front side of the die, and the die thinning and redistribution layers (RDL) metallization process is performed on the back side of the die. The Die 1 process ends with the formation of micro-bumps in the back side of the die, and the bumps contain copper and solder materials as depicted in **Figure 2d**. Similarly, micro-bumps are formed on the front side of Die 2 after its FEOL and

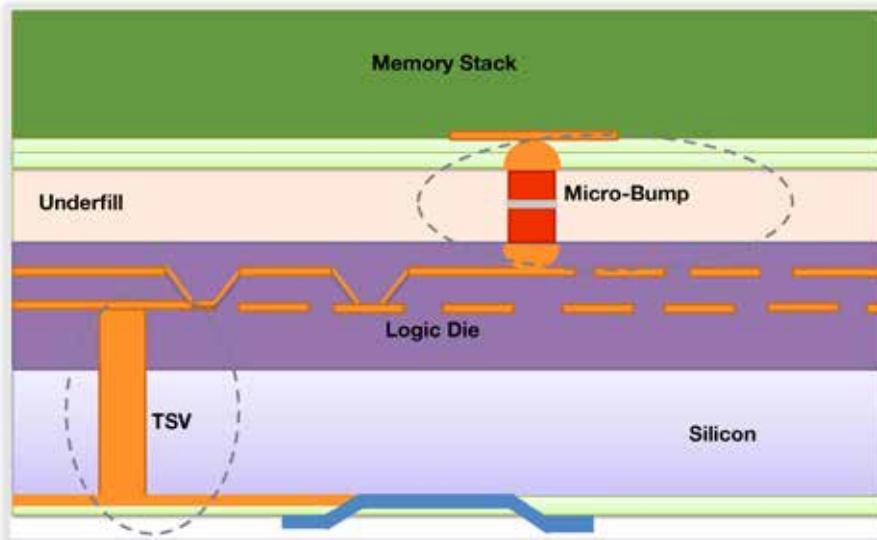


Figure 1: Key components of 3D IC stacks.

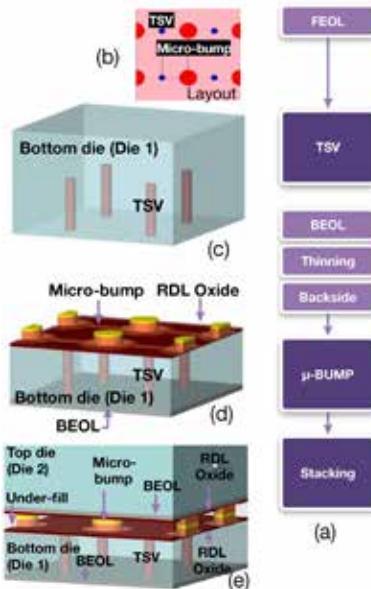


Figure 2: Example of a 3D IC fabrication flow for a via-middle technique.

BEOL process steps. The stacking process attaches these micro-bumps from two dies and fills the remaining space with underfill materials, as shown in **Figure 2e**.

Figure 3 shows material and design parameters that affect TSV stress [2]. They include via material and diameter, insulation liner material and thickness, and TSV array pitch and height. The stresses generated during the thermal cycles used in the fabrication process depend on the material properties and the geometry. Mechanical stresses affect the performance of transistors in the proximity of the TSVs. High stresses can also affect the reliability through mechanical failures. We now discuss both of these effects in more detail and illustrate the benefit of TCAD modeling in optimizing the process and geometry to characterize and mitigate the impact of stress on performance and reliability.

Reliability impact of TSV insulation liner properties

The resistance to deformation of a material is related to its modulus. In **Figure 4** (top, middle), the two images compare the top surface deformations under the same temperature rise for two TSV structures with different insulation liners. The top case uses a typical BEOL oxide liner while the middle case uses a low k dielectric liner. The deformation is simulated with Sentaurus Interconnect.

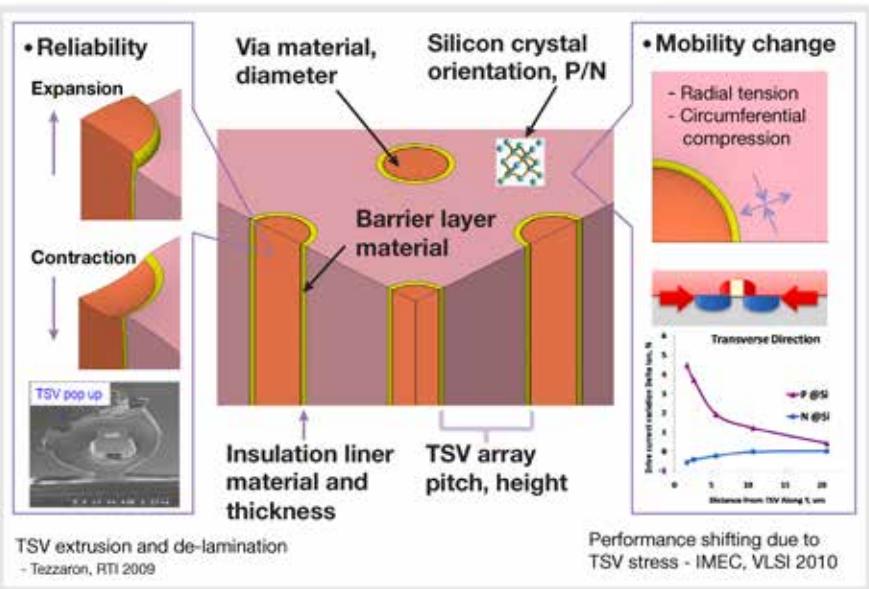


Figure 3: Impact of TSV-induced stresses on reliability and transistor performance.

Only one quarter of the TSV is shown because of the symmetry. The thermal steps in the 3D IC manufacturing process result in a larger deformation of the copper TSV relative to the BEOL oxide liner because the low-k material offers

less resistance to the thermal expansion of the copper TSV.

The larger deformation of the low-k insulation makes mechanical failure more likely and the reduced planarity may adversely impact the process

KYEC
The Testing Industry Division

Your Strategic Partner for Testing MEMS and CMOS Imaging Sensors

www.kyec.com

- HQ in Taiwan & Worldwide Offices, covering USA, Japan, Europe, China and Singapore
- Over 2000 sets of test systems and growing
- Professional testing services, covering Wafer probe, Final test, Pre-Assembly, Burn-in, Back-end
- Complete testing Solutions and equipment , such as Memory, Logic, SOC, RF, CIS, MEMS

Address: 101 Metro Dr. #540 San Jose, CA 95110 Tel: 1-408-452-7680 Fax: 1-408-452-7689

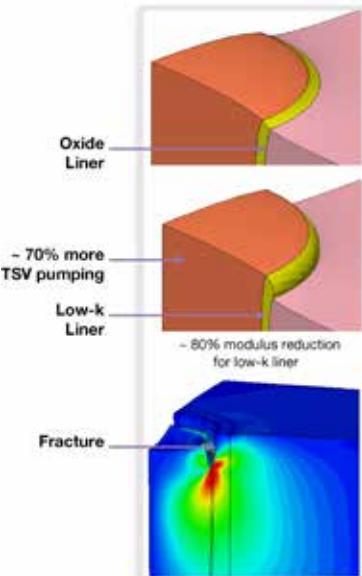


Figure 4: Deformation of a TSV structure for two types of liner insulation.

window of subsequent process steps. To evaluate this likelihood, Sentaurus Interconnect simulates the driving force for the propagation of cracks, in this case resulting from interfacial shear stresses. This analysis helps with the selection of liner materials with the requisite properties to meet the reliability and planarity constraints of the process [2].

Performance impact of TSV dimension and pitch

Stress fields in the silicon surrounding a TSV alter electron and hole mobility (and consequently the drive current) of transistors placed near the TSV. This effect is simulated with piezo-mobility models implemented in Sentaurus Interconnect. The stress distribution around a TSV is a function of design parameters such as TSV diameter and pitch. **Figure 5** (bottom) shows the simulated changes to the electron and hole mobilities as a function of distance from the TSV for two TSV diameters ($5\mu\text{m}$ and $10\mu\text{m}$) with a pitch of $25\mu\text{m}$. The plot is along a vertical cutline. Because the stress distributions are not radially symmetric, cutlines along other directions yield different results, attesting to the complexity of the effect. The effect is stronger for the larger diameter and is particularly prominent for PMOS [2].

Figure 5 (top right) shows the mobility variation for TSV pitches of 10 and $20\mu\text{m}$ with a TSV diameter of $5\mu\text{m}$ and

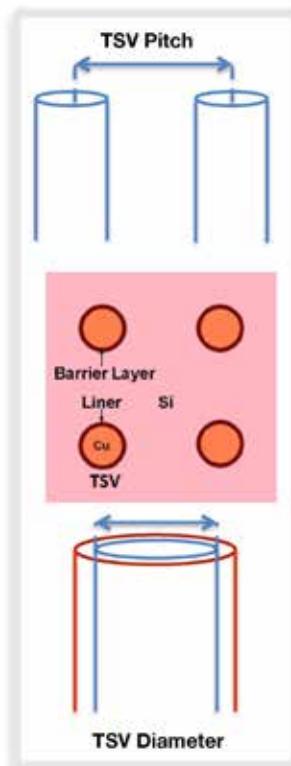


Figure 5: Impact of TSV diameter and pitch on the mobility of NMOS and PMOS transistors placed in proximity to the TSV.

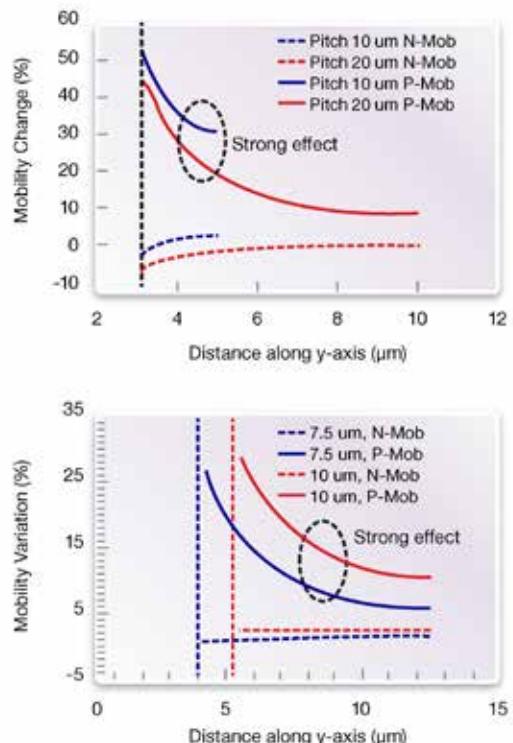
insulation thickness of $0.5\mu\text{m}$. The tighter TSV pitch leads to higher carrier mobility variation. This type of analysis is very important to constrain the TSV geometric variables – diameter and pitch – and hold them within ranges that keep the changes to transistor performance below a target threshold.

Other stress effects in 3D IC fabrication

Beyond the two effects discussed above, 3D IC fabrication uses other components that affect the stress state of the structure (**Figure 6**). Among these, the thermal process used to fabricate the micro-bumps and the selection of underfill material have been shown to have a primary impact, thereby motivating the use of simulation to characterize the effect and identify process option for mitigating the reliability and performance impact using similar methods to the ones described above [7].

Summary

3D IC manufacturing introduces stresses that impact reliability and performance. These effects are simulated with Sentaurus Interconnect. The simulations guide the



Source: A. P. Karmarkar, MRS Spring Meeting, 2010

selection of materials, fabrication flow and design rules to reduce the levels of stress in the 3D IC structure to meet the reliability and performance targets. The use of simulation reduces the number of experimental cycles needed to complete the integration of the TSV and other elements needed to realize the 3D IC, thereby reducing development time and cost.

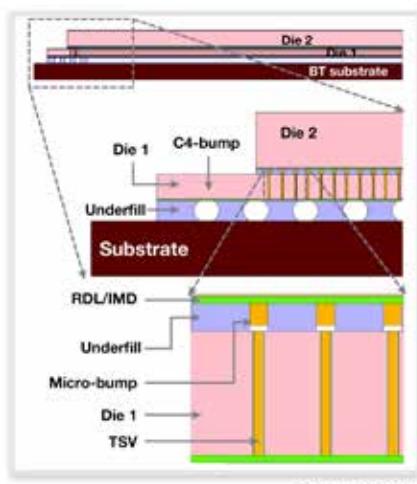


Figure 6: Additional stress sources in 3D IC fabrication.

Acknowledgement

For more information on Sentaurus Interconnect and the applications described in this article, please contact tead@synopsys.com.

References

1. A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, et al., "Comprehensive analysis of the impact of single and arrays of through-silicon vias induced stress on high-k/metal gate CMOS performance," 2010 IEEE, IEDM10-26.
2. A. Karmarkar, X. Xu, S. Ramaswami, J. Dukovic, K. Sapre, A. Bhatnagar, "Material, process and geometry effects on through-silicon via reliability and isolation," Materials Research Society Symp. Proc., Vol. 1249, Warrendale, PA, 2010, 1249-F09-08.
3. C. Shah, A. Karmarkar, X. Xu, "Modeling interconnect stress evolution during BEOL process and package," IEEE IITC Proc., pp. 1-3, 2013.
4. K. B. Yeap, U. D. Hangen, T. Wyrobek, L. W. Kong, A. Karmarkar, X. Xu, et al., "Elastic anisotropy of Cu and its impact on stress management for 3D IC," Jour. of Materials Research, pp. 339-348, 2011.
5. M. Nakamoto, R. Radovicic, W. Zhao, V. K. Dasarapu, A. P. Karmarkar, X. Xu, "Simulation methodology and flow integration for 3D IC stress management," CICC, pp. 1-4, 2010.
6. A. P. Karmarkar, X. Xu, K.B. Yeap, E. Zschech, "Copper anisotropy effects in three-dimensional integrated circuits using through-silicon vias," IEEE Trans. on Device and Material Rel., Vol. 12, No. 2, 2012.
7. A. Karmarkar, X. Xu, "Microbump impact on reliability and performance in through-silicon via stacks," MRS Spring Meeting Proc., Vol. 1335, 2011.

Biography

Sudarshan Krishnamoorthy received his Master's degree in Electrical Engineering from Arizona State U. He is a Sr. Technical Marketing Manager at Synopsys; email: sudarshan@synopsys.com

Xiaopeng Xu received his PhD in Engineering from Brown U. and is an R&D Manager at Synopsys.

Dispensing Control

Enhanced Dispense Process Control



Fluid Pressure Control (FPC) maximizes the dispense capabilities of your pump. Through engineering and software, a constant supply of fluid is delivered to the pump displacement mechanism – not too much and not too little, regardless of fluid level in the reservoir.

With a constant supply of fluid, you'll see repeatability in dispensing like never before. Your dispense process could use an FPC injection!

Consistent & Reliable Process Results

MAX Series Precision Dispensing Systems will improve the reliability of your dispense process. Standard features of 0.0254 mm (0.001") accuracy, close-loop nozzle calibration, and nozzle cleaning eliminate setup variations between operators. MAX Series systems will compliment your microelectronics and semiconductor dispense processes.



With a wide range of available dispense pumps, the MAX Series will take you to the next level.

Supplying a full range of precision dispense products.

GPD Global
Precision Dispensing Systems

+1.970.245.0408 • request@gpd-global.com • www.gpd-global.com

Evaluating conductive die-attach films for gallium arsenide-based packages

By Andrew Laib, Howard Yun [Henkel] and Frank Wei, Hiroaki Yamada [DISCO]

Gallium arsenide (GaAs)-based devices are found in several applications such as optoelectronics, photovoltaics and RF electronics commonly found in wireless and telecom products. As compared to silicon (Si), GaAs has different electronic properties. First, GaAs has a direct band gap that enables electron-hole recombination to generate photons and vice versa, making GaAs suitable for use in optoelectronic devices like LEDs and photo-detectors. Indirect band gap semiconductors, such as Si, do not permit photon generation from electron-hole recombinations. Second, GaAs has higher carrier mobilities than those in Si. Electrons can move much faster in GaAs-based devices than in Si devices. For signals in the radio frequency (RF) range, Si devices are unable to respond to the switching speeds of the electric fields. On the other hand, the carriers in GaAs can move back-and-forth fast enough to process and transmit the signals. This property is a prerequisite for telecommunication applications. Third, GaAs has a higher band gap energy than in Si. Undoped GaAs is more insulating than undoped Si substrates, allowing for higher sensitivities in devices fabricated on the surface. Consequently, GaAs-based devices have complemented Si-integrated circuits (IC) since the early very large-scale integration (VLSI) era and have fulfilled needs in the aforementioned market sectors. In recent years, the rapid proliferation and adaptation of wireless smart devices have further punctuated the need for continued development of small form factor GaAs device packages for telecommunications and other applications.

Generally, manufacturing of single-

crystal, compound semiconductor substrates is more technically challenging and costly than making Si wafers. The current industry standard wafer size for logic Si IC fabrication is 300mm, while GaAs wafers are 200mm and below, with 150mm and 100mm wafers being the most common. Requirements for the utilization of the GaAs wafer surface area are extremely stringent. Furthermore, GaAs device dies may be much smaller than Si-logic devices, which may result in numerous dies per wafer.

GaAs wafer dicing considerations

In general, dicing is a process that deliberately eliminates real estate between dies following a single-point, serial process to singulate the devices. The aforementioned utilization and die size constraints make blade dicing of GaAs wafers challenging. To satisfy the needs of cost- and environment-conscious GaAs processes, laser dicing is preferred over blade dicing. The continuous development of laser and optics technologies have enabled through-thickness cutting of 100 μm -thick GaAs wafers with extremely narrow kerf width [1]. **Table 1** contrasts the industry-recommended GaAs blade

Enhancing GaAs package reliability and architecture

In terms of reducing overall material cost and improving package quality, using conductive die attach film (cDAF) as opposed to traditional die attach paste has several advantages for GaAs devices. First, cDAF is a semi-solid material, so excess material (often referred to as squeeze out) and die top contamination are not concerns for device manufacturing as they can be with paste-based materials that can move out and onto the die top. Because it is a specific thickness film material, cDAF offers strict bond line control that improves bonding capability with wafers thinner than 100 μm , which is a common thickness for GaAs devices.

Second, because die-to-die spacing on the wafer can be tighter when using film-based die attach materials, saving pad area allows for communication manufacturers to add many small devices on the same pad, further reducing overall form factor. Additionally, because cDAF has a low degree of squeeze out, the pad real estate required is much less than that for conductive paste, allowing for shorter

Process Name	Process Feed Speed [mm/sec]	Number of Passes	Kerf Width [μm]
Blade Dicing	5 to approx. 20	1X – 2X	Approx. 15-25
Laser Dicing	225	2X	<15

Table 1: Comparison of process parameters for blade and laser dicing of GaAs wafers.

dicing processes with the laser dicing process demonstrated in this article. Advantages of the laser process on GaAs wafers are clearly shown. Laser dicing supports high-throughput processing and enables narrower required kerf widths, which leads to higher die densities on the wafer.

interconnections inside the package. Shortening the connections increases the device frequency, which is an important advantage for communication devices [2].

To fully analyze the process compatibility of the through-thickness laser dicing process with GaAs wafers

on cDAF, the authors conducted a thorough study to determine viability, reliability and performance results.

Design of experiment

The sample preparations included the acquisition of blank, undoped ø100mm GaAs <100> wafers with various backside metallizations. The metal depositions had film stresses and thicknesses similar to those used in the electronics industry. Using a wafer grinding process, the GaAs substrates were then thinned to 100µm from the original wafer thickness – a typical required thickness in modern GaAs device package. Then, the thinned

wafers were mounted onto cDAF and dicing tape for laser dicing into 1.0mm x 1.0mm dies. The sputtered metal was facing down and in contact with the cDAF materials. **Table 2** shows the experimental details. Samples also included Si dies that were diced using a blade as a control for comparison of results. “A” and “B” types of dicing tapes corresponded to two different tackiness levels of the tape adhesive. cDAF 1 and cDAF 2 refer to two different types of cDAF films.

Figure 1 outlines the die singulation process. All wafer types shown in Table 2 were successfully diced using through-thickness laser dicing. For this

study, a high-energy pulsed laser source combined with an optics set suitable for through-thickness GaAs cutting was installed on a fully-automatic laser saw. Prior to dicing, a protective layer was spin-coated onto the dicing surface inside the tool. This water-soluble layer protected the die surfaces from the laser ablated debris. After dicing, the machine then automatically washed off this layer along with the ablated debris before unloading the dicing frame.

During dicing, the high-energy laser pulses ablated and vaporized the substrate material to create the narrow die separations. Some heat affected zones (HAZ) formed along the sidewalls of the dies. In the subsequent step, the HAZ underwent a wet etching treatment, which lasted approximately two minutes, to eliminate any incipient micro-cracks remaining inside. Presumably, such micro-cracks formed due to stresses induced by the numerous rapid thermal cycles of ablation/vaporization, GaAs materials recast, then cooling onto the sidewalls during each of the extremely short laser pulse cycles.

cDAF Type and Dicing Tape	GaAs Wafer Description
CDF 1 "B" Type Dicing Tape	100µm GaAs No backside metal
CDF 1 "B" Type Dicing Tape	100µm GaAs with Ti/Au back, 200Å/1kÅ
CDF 1 "B" Type Dicing Tape	100µm GaAs with Ti/Ni/Ag back, 1kÅ/3kÅ/1kÅ
CDF 1 "A" Type Dicing Tape	100µm GaAs with Ti/Au back, 200Å/1kÅ
CDF 2 "B" Type Dicing Tape	100µm GaAs with Ti/Au back, 200Å/1kÅ
CDF 1 "A" Type Dicing Tape	Control – 100µm Si with Ti/Au back, 200Å/1kÅ Blade dicing

Table 2: Sample preparations of GaAs wafer, cDAF, and dicing tapes.



HPB-4

High-Power Burn-In with Test System

MEETING the CHALLENGE

- Individual temperature control for each device up to 600W
- Test devices at a maximum temperature of 150°C with a liquid-cooled heat-sink per device
- Programmable clocks with leading and trailing edges per pin, one-nanosecond resolution, and 8 on-the-fly timing sets
- System capacity of 14 burn-in boards (112 devices)
- 12 vector formats per-pin per-cycle with memory testing extensions
- 128 I/O signals per board
- High-speed clock range of 2 to 400 MHz
- 64M vector memory, 8G scan
- 19 programmable voltage regulators provide 2060 amps of device current per burn-in board
- 16 high-current supplies
 - (0-3.2 Volts up to 125 Amps each)
- 3 low-current supplies
 - (0-6 Volts up to 20 Amps each)


**BURN-IN
CERTIFIED**


**MICRO
CONTROL
COMPANY**





7956 Main Street NE, Minneapolis, MN 55432 • Phone: 763-786-8750 • Toll Free: 800-328-9923 • Fax: 763-786-6543 • www.microcontrol.com

Chip Scale Review • March • April • 2014 [ChipScaleReview.com]

27

After die singulation, the GaAs-on-cDAF 1.0mm x 1.0mm dies were attached onto lead frame substrates, and overmolded with encapsulant.

Laser Dicing Process

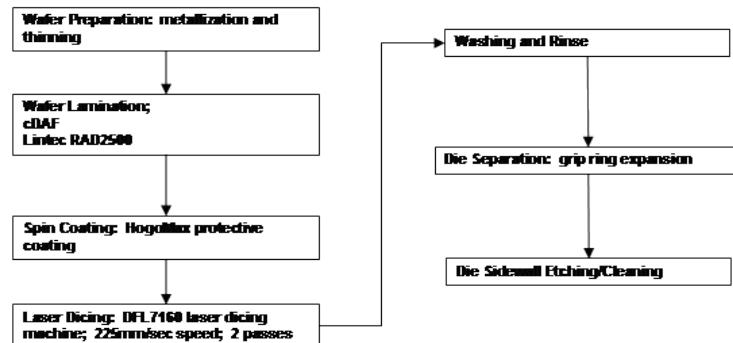


Figure 1: Laser dicing/die singulation process flow.

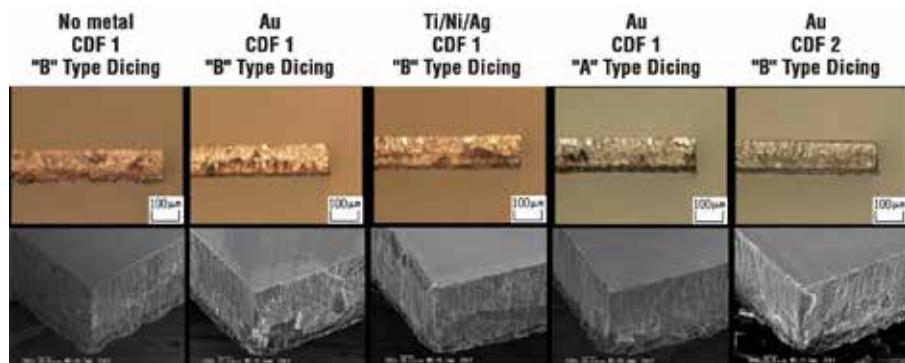


Figure 2: Post-dicing inspections of the die sidewalls.

Packaging and Reliability Process

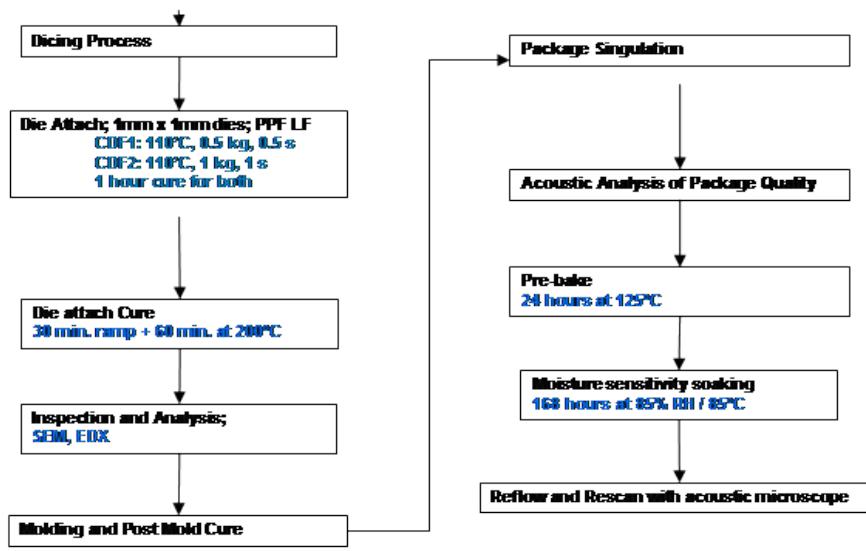


Figure 3: Packaging and reliability testing process.

Moisture-sensitivity reliability tests and cross-section analyses were carried out in order to characterize the package quality.

Results and analysis

After full laser singulation and wet etching, the die sidewalls were examined under optical microscope and SEM. Figure 2 shows the inspection results. As expected, no micro-cracks are present at the die edges. Neither handling nor the die-attach process resulted in any die breakages or delaminations of the cDAF under the dies. To evaluate the dicing quality and package reliability, the following procedures were used (Figure 3).

To begin the packaging process, the diced wafer was die-attached onto metal lead frames and cured. Clean dicing without die cracking was observed for all legs in the study. No die top contamination was observed by EDX scanning, which further guarantees wire bonding will have no problems in later processing (Figure 4). In other words, laser dicing showed no higher organic contaminations on the top of GaAs dies compared to those shown on the top of the control, the Si dies sawn by mechanical blade dicing.

Next, the attach quality was analyzed through acoustic imaging quality testing. The parts were then wire-bonded and molded. Acoustic imaging was used to confirm good initial wetting before putting the parts into the chambers for moisture sensitivity level (MSL) testing, which consists of exposing the packages to an 85% relative humidity (RH) environment at 85°C, and three times emulated reflow at 260°C (Figure 5). After the test, the acoustic imaging did not show any failures, i.e., achieved MSL 1 qualification results [3]. Laser-diced GaAs die packages showed the same die attach quality as the Si-control packages.

Figure 6 shows cross-sectional analyses on the packages post-MSL 1. Good adhesion of the cDAF to the lead frame and die is demonstrated. No voids or overmold material penetration is observed at the various interfaces inside the packages.

Summary

The course of processing and characterization of cDAF laminated GaAs wafers showed no anomalous behaviors for all sample types. Subsequently, MSL 1 reliability test results of the encapsulated packages indicated that the bond between the

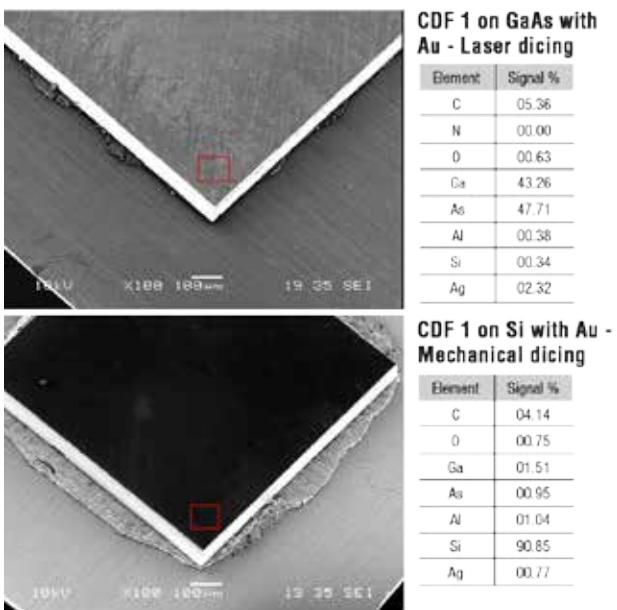


Figure 4: EDX results of die top contamination.

MLS 1



Figure 5: Acoustic images of dies in overmolded packages after MSL 1 reliability tests. All devices-under-test maintained original die attach quality after testing.

Cross-section Analysis

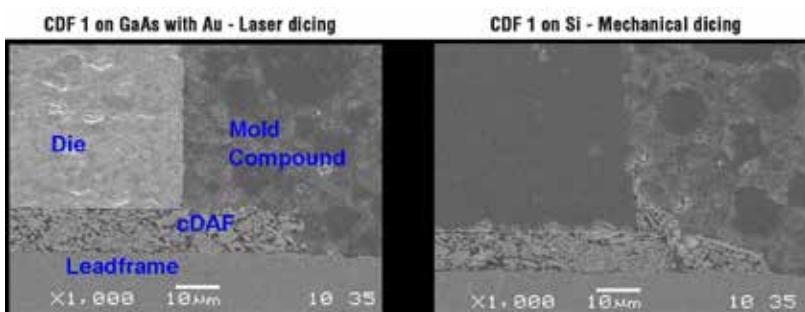


Figure 6: Cross-sectional images of attached dies in package after the MSL1 reliability test. cDAB's bulk integrity is not affected.

Acknowledgements

The authors would like to thank LGA Thin Films, Santa Clara, CA for sputter depositions of the metallization layers; Toshiyuki Sakai and James Verzosa of DISCO Hi-Tec America, Santa Clara, CA for the grinding preparation of the GaAs wafers; and DISCO R&D Laser Department, Tokyo, Japan for internal discussions.

References

1. "Laser dicing for quality GaAs die separation," DISCO e-News, 2012, Vol. 107 <http://is01.disco.co.jp/psc/enews3.nsf>
2. Loctite Ablestik CDF 200P – Pre-cut dicing and electrically conductive die-attach film in one, Henkel Press and Media Relations, 2012; <http://www.henkel.com/press/press-releases-2012-20120813-loctite-ablestik-cdf-200p-36809.htm>
3. Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Device, J-STD-020D.1, March 2008; <http://www.jedec.org/standards-documents>

Biographies

Andrew Laib received his BS degree from the Milwaukee School of Engineering and is a technical service engineer at Henkel Electronic Materials; andrew.laib@us.henkel.com.

Frank Wei received his PhD degree from the Massachusetts Institute of Technology in Materials Science and Engineering. He is the R&D manager for DISCO Hi-Tec America, Inc.

Howard Yun received his PhD from Pohang U. of Science and Technology in Chemical Engineering, South Korea. He is a technical service manager at Henkel Electronic Materials.

Hiroaki Yamada received his BS degree from Sojo U. of Japan in Electrical Engineering. He is a laser applications engineer at DISCO Corporation, K.K.

Fluid dispensing for packaging today's devices

By Akira Morita [[Nordson ASYMTEK](#)]

Fluid dispensing systems are evolving in order to address the challenges that system-in-package (SiP) and micromechanical systems (MEMS) packages face, especially in regard to tight geometries and assembly processes. These packages, used in smartphones, have become more miniaturized, and as a result, have created added value in the market. However, they include a variety of small dies or devices inside, including RFICs, MEMS, application specific ICs (ASICs), discrete passives, and others, which are more tightly allocated in the package. The dispensing system has to dispense various fluids, including underfill, solder paste, flux, and encapsulation, into tight locations and onto smaller pads in order to fit the device size.

The packaging assembly process is also changing because of miniaturization. Packaging companies see different prospects in yield and "buy or produce" for the devices. For example, the integrated device manufacturer (IDM) usually purchases discrete passives and their yield is quite high because they are pre-tested and their assemblies are simple. The IDM produces active devices and their yield is lower than discrete passives. These different prospects guide the assembly sequence: high yield devices follow low yield devices in assembly, while testing after low yield device assembly prevents high yield device waste. Discrete passives have now become expensive because of their small, grain-like size. This makes the assembly process sequence from low yield to high yield result in even greater savings. The additional cost of the discrete devices, however, also makes the accuracy of applying the fluid even more important. Because both high and low yield devices can't be assembled at the same

time, the latter have to be applied very carefully in tight spaces between the devices. Screen printing can't be used, so the solder, tacky flux, surface mount adhesive, or other fluid has to be applied in that tight space, very close to the active devices on the board. This is challenging for the dispensing system.

One of the typical MEMS devices following this miniaturization trend is the microphone, which is used in increasing volumes for mobile applications. The microphone mainly consists of a MEMS diaphragm component, ASIC, wire bonds, substrate, and metal cap with a hole. Two types of dispensing are usually done for this package: dispensing sealant between the substrate and cap, and encapsulation on the ASIC. As the package has shrunk, the diameter of the MEMS diaphragm hasn't changed because the diaphragm size is defined to capture sound. However, the size of the MEMS diaphragm die has shrunk significantly over the years. The peripheral die area of the diaphragm has decreased by 80% from 2006 to 2011, but the diaphragm area has not changed. As the MEMS diaphragm die size has decreased, the entire package size of the microphone has also been decreasing: 6 x 4mm² in 2008 to 3 x 2mm² in 2011 to 2.2 x 1.5mm² in 2013. Tighter component allocation in the overall package becomes more critical. This tight clearance requires very

straight sealing lines with no rippling or waviness.

These trends create realigning and redefining requirements in the dispensing assembly process and adapting dispensing equipment and processes to produce today's products so they function reliably and at peak performance. Some of these dispensing application challenges are: 1) Fluid dispensing for holes; 2) Small dot dispensing for flip-chip bonding and discrete passives; 3) Maintaining tight keep-out zones for underfilling; and 4) Sealant dispensing for MEMS cap assembly. This article presents solutions for the challenges these new trends create.

Fluid dispensing for holes

SiP and MEMS substrates often have holes. The holes are used for through-hole device assembly and for access between inside sensors and the outside environment. These holes have annular rings with a width of 250 microns and diameters that range in size from 1.5mm down to 1mm ([Figure 1](#)). In the assembly process, solder has to be deposited around these holes to hold the pin in place to make the electrical connection. Tacky flux is usually applied around the holes to prevent the components from slipping during reflow. A common way to apply these fluids is with screen printing. However, when fluid is deposited using screen

Annular rings: width 250µm

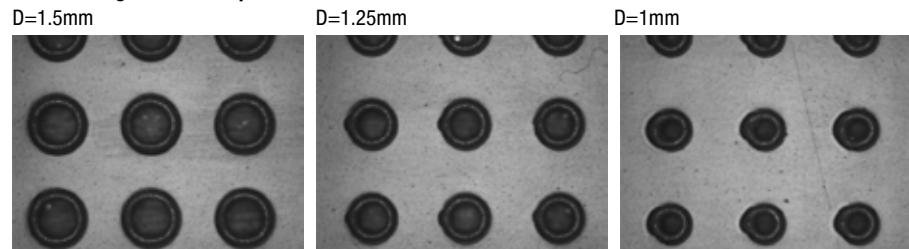


Figure 1: Typical solder paste dispensing for different circle diameter sizes.

printing, these holes present a real problem because fluid tends to run down into the holes. Dispensing is a good way to deposit the fluid because it can aim the fluid at specific locations around the holes; however, the holes are so small that only a dispenser that can deposit or jet very accurately placed small dots each and every time can be used. Therefore, small dot dispensing and equipment that can jet these small dots precisely and repeatably around the holes has taken on increased importance.

Flip-chip bonding and discrete passives

Many SiP packages include flip-chip devices. The flip-chip bumps are inside the package so the bond needs to mesh with the bond on the substrate. They can be gold stud bumps, copper pillars, solders, or any material. The bump pitch and bump diameter on those flip-chips have become smaller and the package size has shrunk. In the middle of the assembly process, bonding materials such as solder and silver epoxy have to be deposited on the substrates into the tight spaces between components that have already been placed. Screen printing can't be used because the other components don't allow the screen to attach to the substrate. Dispensing can be used to apply the fluid, but the dispensing system has to be able to produce small dot sizes and tight location accuracy for those applications.

Another consideration is the keep-out zone (KOZ). This is the area between the components that must be kept free of fluid and contaminants. As the packages have shrunk, the KOZs have also shrunk so the fluid has to be deposited in a very thin line extremely close to the component. This is especially important when depositing underfill next to the component. High-density flip-chips on strip, where the chips are close to each other and they need to be underfilled, also pose this challenge. Small droplets need to land between the chips so the chips can both be underfilled at the same time. The fluid under the chips cannot be connected. Some of the automated fluid jetting equipment on the market today is designed especially to underfill close to the die to reduce the KOZ.

For small dot dispensing of flip-chip packages, an auger valve that can achieve $100\mu\text{m} +/- 14\mu\text{m}$ dot diameter dispensing at 3-sigma repeatability with silver epoxy is necessary. **Figure 2** shows small dot dispensing on the top of flip-chip bumps. **Figure 3** shows the dot sizes and accuracy that can be achieved.

Small dot dispensing technology can be applied to small discrete passives as well. Many small discrete passives

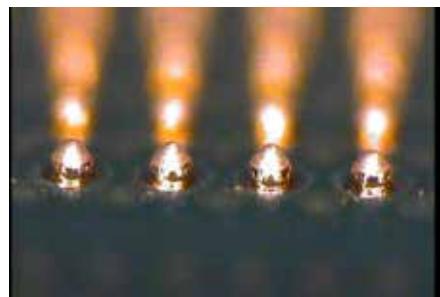


Figure 2: Small dot dispensing on the top of flip-chip bumps.

Our Point Is... DL Technology Needles Work Precisely For Any Application.



DL Technology needles are designed and crafted to dispense material accurately, efficiently and to provide for better material release. Our needles are constructed in a variety of sizes, configurations, and patterns to meet your needs for any application.

EZ-FLO needles available in footed and non-footed surface mount, encapsulation, luer, and cone. Designed to provide precise, repeatable volumes. Stainless steel and ceramic needles available.

Easy Release Luer-lok dispense needles available in stainless steel and plastic. Used for applications such as epoxy, solder paste, solder mask and a variety of other materials.



Custom Needles can be designed according to unique requirements and specifications.

DL Technology has been the leader in micro dispensing technology for over 15 years. For more information, or for size or specifications on our line of needles, pumps or valves, visit www.dltechnology.com.

DL Technology
216 River Street, Haverhill, MA 01832
P: 978.374.6451 | F: 978.372.4889
sales@dltechnology.com



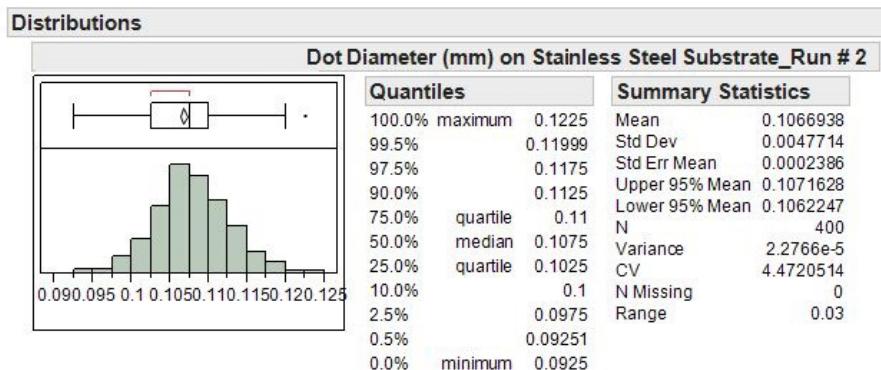


Figure 3: Statistical data of small dot dispensing.

Short lines and dots: size 600-250 μ m

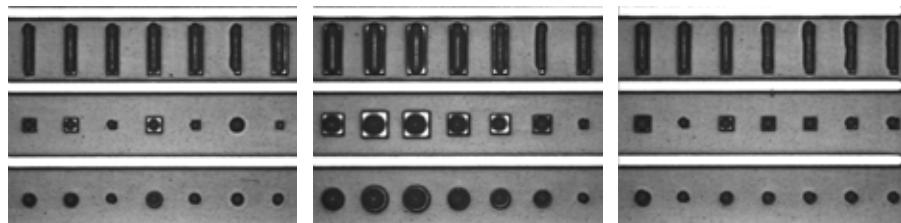


Figure 4: Solder dispensing samples for SiP and MEMS packages.

such as 0201 ($0.6 \times 0.3 \times 0.23\text{mm}^3$) are applied to SiP and MEMS packages because of their tiny size. They need a $250\mu\text{m} \times 250\mu\text{m}$ pad size. As with flip-chip packages, these passives are assembled into these small spaces after the active devices are assembled, so small dots of fluids, such as solder, have to be dispensed on the pads with extreme precision, such as in short lines and dots ranging from 600 microns down to 250 microns (Figure 4).

Sealant dispensing for MEMS cap assembly

The space, or buffer clearance, between the MEMS die and the sealing lines for attaching the MEMS cap

decreased to $150\mu\text{m}$ (Figure 5). This tight clearance requires very straight sealing lines with no rippling or waviness. Deviations from a straight line path or inconsistency in the line width negatively affects how close to the die edge this line can be dispensed without risking fluid landing on top of the die or on neighboring components, resulting in product failures. Line straightness and width consistency are also important for solder paste and sealant line dispensing applications. In such applications, however, there are two additional considerations that affect fluid dispenser design and performance: oscillations (ringing) after cornering, and thin line

width. Transitioning from a high speed move in one direction to a perpendicular direction causes ringing oscillations in the subsequent dispensed line caused by motion system inertia. When determining how close to the die to target a line path, ringing effects of the system at the target line speed must also be considered to avoid having fluid land on top of the die. This situation will also affect the minimum KOZ.

When using an auger valve, a consistent dispense gap between the dispenser tip and the substrate is required to achieve straight sealing lines. Maintaining this consistent dispense gap is critical to achieving smooth lines with less rippling. This is called the z-gap and is defined as the vertical distance between the fluid ejection point and the substrate surface. Achieving a minimal z-gap not only requires precise control in the z-axis motion, but also precise detection of the surface height relative to the reference z-home position. Maintaining this minimal z-gap along the dispense path requires the ability to ensure that there is minimal variation in both the surface height and the reference z-home position throughout the target dispense

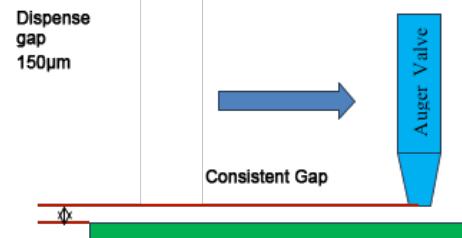


Figure 6: Dispense gap consistency requirement.

area (Figure 6).

In high-volume production environments, a dispensing system needs to make sealing lines for hundreds of microphones at a time. Typically, a $250\mu\text{m}$ wide sealing line will require a $150\mu\text{m}$ dispense gap. Being able to achieve such a gap, let alone maintaining it across a substrate surface while the dispenser is moving rapidly across the area, is quite challenging (Figure 7). In addition to tight control of the z-axis oscillations, making lines that closely follow a set path requires precise movements in the x-y plane of the dispenser head. In order to meet the needs of these applications, the

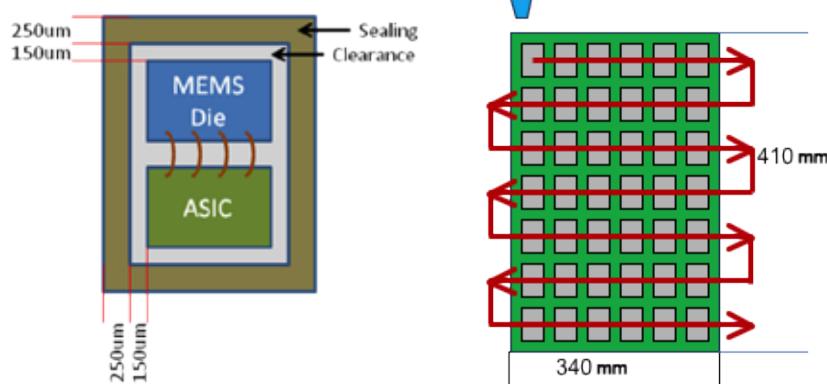


Figure 5: Buffer clearance and sealing line dimensions in a MEMS package.

dispensing system must have tight accuracy control in all three dimensions, x, y, and z. This is often accomplished through improving the stiffness of these axes.

Dispensing system accuracy

New dispensing systems specifically address these types of high-accuracy applications. Achievable accuracies are listed in **Table 1**.

Item	Specification
X and Y axis accuracy	$\pm 40\mu\text{m} @ 3\sigma$
X and Y axis repeatability	$\pm 15\mu\text{m} @ 3\sigma$
Z axis repeatability	$\pm 15\mu\text{m} @ 3\sigma$

Table 1: Achievable accuracies for new dispensing systems.

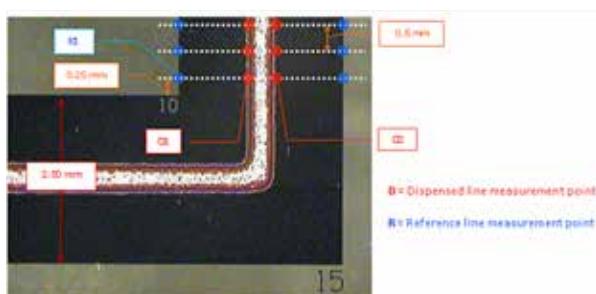


Figure 7: Measurement method between line and reference.

Auger valves have been validated for line straightness by measuring the center of dispensed lines. **Figure 7** shows the measurement methodology. Placement error was determined by measuring the positional offset between the center of the reference line and the center of the dispensed lines.

$$\text{Error} = ((D_1 + D_2)/2) - ((R_1 + R_2)/2)$$

Data in **Figure 8** shows the x and y axis accuracy that has been validated with $>1.3 C_{pk}$ with $\pm 40\mu\text{m}$ specification limits. It was clearly observed that the lines are quite straight and corner

radiiuses are very small (**Figure 9**). Dispense gap consistency is difficult to measure directly during dispensing. However, line straightness and width control are ultimately the core concern and acceptable metrics by which to judge a system's performance. These are metrics that haven't been given a lot of consideration previously and will require more testing and attention as they are a more valid measure for achieving the desired results than just speed or line width.

Summary

SiP and MEMS packaging requirements continue to push for increasingly smaller devices and packages requiring fluid dispensing continue to evolve. These conditions call for smaller volume dispensing into tighter spaces. Therefore, dispenser capabilities to achieve these targets must continue to improve and the ability to evaluate these capabilities must also evolve. Fluid dispenser accuracy must keep

PROVIDING QUICK-TURN PACKAGING AND ASSEMBLY SERVICES FROM PROTOTYPE THROUGH PRODUCTION

- Open-molded Plastic Packages (OmPP), Open Cavity Plastic Packages (OCPP), Ceramic, Laminate, COF, COB
- Wire Bonding, Die Bonding, Flip Chip, Encapsulation, Molding, Marking
- Wafer Preparation, Dicing, Backgrinding, Reticle Die Sorting

ISO 9001 Certified

OPEN-molded Plastic Package

WWW.QUIKPAK.COM
a division of Delphon

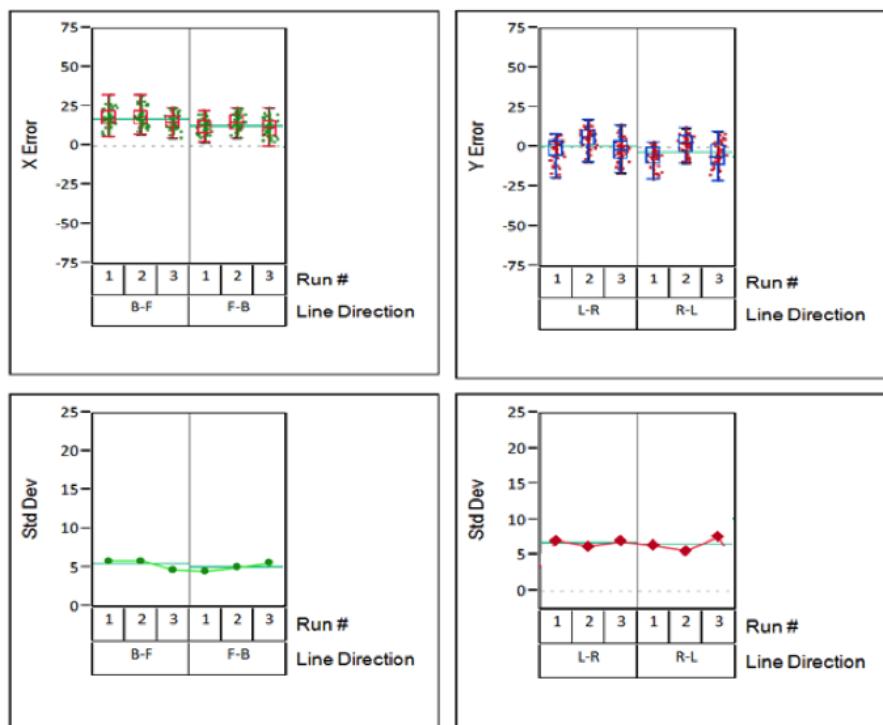


Figure 8: Difference between line and reference in the X and Y axis.

pace with, or stay ahead of, the market. Challenges include dispensing around holes, dispensing in tight spaces accurately and reliably, the ability to achieve tight keep-out zones, and maintaining a consistent and very small dispense gap during high speed operation to achieve a perfectly straight line during dispensing.

The stiffer and more accurate the dispenser and ability to achieve $\pm 40\mu\text{m}$ straight sealing lines from the target path with a $>1.3 C_{pk}$, and the ability to address the tight clearance requirement between the MEMS dies and surrounding package structures are making manufacturing of these packages possible. New test methods are being used to evaluate fluid path accuracy

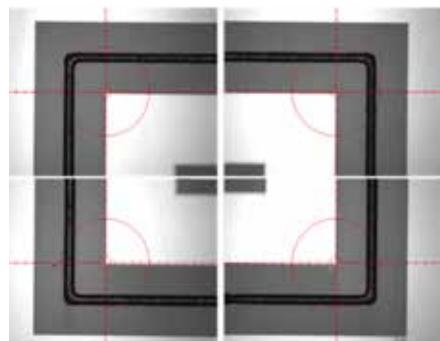


Figure 9: Sealing lines are quite straight and corner radii are very small.

and z-gap control to closely reflect actual customer use. New dispensing systems have been designed to take these factors into account and compensate for them.

Dispensing systems have been redesigned so the motion system can achieve accuracy and precision in all three axes, further improving path accuracy and narrow line width control. Some of the newer systems on the market have demonstrated the ability to increase some customers' units per hour productivity by over 25%, while also reducing keep-out zones and achieving line widths and dot diameters below $200\mu\text{m}$. Although dispensing equipment manufacturers are constantly working with customers to develop systems to build these new products, when designers look at new products and applications, it's also important for them to consider the manufacturing processes and the equipment and capabilities available to achieve them.

Acknowledgments

The authors would like to thank Dr. Hanzhuang Liang, Ms. Floriana Suriawidjaja, Ms. Linh N. Vu Rolland, Mr. Dan Ashley, and others from Nordson ASYMTEK, and Mr. Colin Robertson from Blackstone Global/Assembly Products for their help.

Biography

Akira Morita received his MBA at Rensselaer Polytechnic Institute, an MS in Physics at Ritsumeikan U. Graduate School, and a BS in Physics at Ritsumeikan U. He is a Business Development Manager at Nordson ASYMTEK; email akira.morita@nordsonasymtek.com

PLASMA ETCH

PROGRESS THROUGH INNOVATION

INTRODUCING THE PE-25-JW

The Plasma Etch, Inc. PE-25-JW is a fully automated plasma cleaning system.

Surface energy modification with plasma treatment yields improved markability, adhesion and ease of assembly with a low environmental impact.

Removes organics and improves bonds.

LOW STARTING PRICE
\$ 5,900 USD

TO LEARN MORE, VISIT www.PLASMAETCH.COM
OR CALL US TODAY AT 775-883-1336

Ranking the top OSATS in IC packaging

By Sandra L. Winkler

Today's electronics are required to provide more functionality, added performance, high speed, smaller form factor, and also need to be portable, fit in our pocket, and allow us to communicate via the Internet so that anyone with a smartphone or tablet has a wealth of information, literally, at their fingertips. Both the front and back end of semiconductor manufacturing and assembly have gone through dramatic changes over the years to meet these demands.

The cost per transistor is now going up with advanced technology nodes – at 22nm and 14nm, for example – when traditionally, the cost has always gone down. Increasingly, then, the backend (i.e., IC packaging) rather than the front end sector, is being looked at as a way to meet the needs of tomorrow's technology demands.

Outsourced assembly and test (OSAT) companies who provide semiconductor package assembly and test services to fab and fabless customers must therefore be prepared to deliver package assembly services that can meet the needs of the Internet of Things (IoT).

What follows is a list of some of the important IC package solutions that can meet the demands of tomorrow's technology, and how the top OSAT companies rank today in how well they are filling these demands. More information on these advanced IC package solutions can be found in New Venture Research's IC Packaging report series. Advanced IC packaging solutions are discussed below.

Stacked packages

Stacked packages are essentially a vertical multi-chip package. They come in many forms, including die stacks, package-on-package (PoP), package-in-package (PiP), thin small outline

package (TSOP) stacks, quad flat no-leads packages (QFNs), multi-chip modules (MCMs), and wafer-level packages (WLPs). Now found in all cell phones, stacked packages are in a market that is in high demand.

The order of ranking of the top companies by units and revenue are listed in the following tables. Amkor Technology and STATS ChipPAC are the leaders in this realm, a cut above the rest. **Tables 1** and **2** exhibit the unit and revenue rankings for the top OSAT companies assembling stacked packages.

Stacked package units (largest to smallest)
Amkor
STATS ChipPAC
PowerTech
SPIL
ASE
Signetics
Unisem
Carsem
Hana Micron
UTAC

Table 1: Stacked package units (largest to smallest).

Stacked package revenue (largest to smallest)
STATS ChipPAC
Amkor
PowerTech
SPIL
ASE
ChipMOS
UTAC
Signetics
Unisem
Hana Micron
Carsem

Table 2: Stacked package revenue (largest to smallest).

Through-via technology, 2.5D, and 3D

Through-via technology is used in both 3D and 2.5D technology. 3D interconnect stacks die vertically and utilizes vias that go through the silicon die to electrically connect one die to the next in a vertical stack, in place of wire bonds or other forms of connection that would wrap around the lower die. Because the die are made of silicon, these electrical interconnects are known as through-silicon vias (TSVs). Redistribution layers (RDL) between the dies are necessary to reroute the vias around the lines and traces carrying the electron, so that the vias go through the bulk silicon only.

2.5D is a variant of 3D interconnect, in which the die are partitioned and placed side by side on an interposer with through-vias to the package substrate below. The interposer replaces the RDL with an interposer as the routing layer, so that the through-vias run through the interposer rather than through the active die.

The order of ranking of the top companies by units and revenue are listed in the following tables. The OSAT companies can play in the 2.5D realm, although this technology is in its infancy. **Table 3** lists the companies that are the leaders in having a program associated with this technology.

TSV units (largest to smallest)
Amkor
STATS ChipPAC
ASE
SPIL

Table 3: TSV units (largest to smallest).

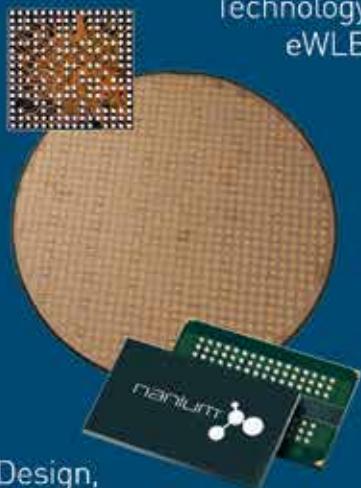
System-in-package

A system-in-package (SiP) is a customized package with multiple elements inside, creating a functional block within a standard JEDEC footprint. This JEDEC



Semiconductor Packaging, Assembly and Test

Leading Edge Fan-out WLP Technology



Design,
Development,
Engineering and
Manufacturing Services



www.nanium.com

footprint differentiates it from an MCM. A functional block in the electronics world is a system of electronics that combines functional units onto a single substrate to enable the shortest electrical distance between parts for superior performance. Such an arrangement also enables a simpler printed circuit board (PCB) for the final product, thus potentially reducing system costs.

SiPs are often used for RF functions and within cell phones. Increasing wireless conductivity is fueling the growth of SiPs. Active devices and passives can be embedded within the substrate in addition to these devices placed on top of the substrate as is customary.

SiPs cover a wide range of packages, and range from very sophisticated, to far simpler. ASE is by far the leader in revenue from assembly of SiPs. **Table 4** lists the SiP units assembly rankings, while **Table 5** presents the revenue ranking.

SiP units (largest to smallest)

Hana Micron

Amkor

ASE

ChipMOS

PowerTech

STATS ChipPAC

Unisem

UTAC

Carsem

Table 4: SiP units (largest to smallest).

SiP revenue (largest to smallest)

ASE

Hana Micron

Amkor

ChipMOS

UTAC

STATS ChipPAC

PowerTech

Carsem

Unisem

Table 5: SiP revenue (largest to smallest).

Fan-out wafer-level package (FOWLP)

Size is important in handheld devices, and wafer-level packages (WLPs) are the ultimate in small size. These little packages also offer superior electrical performance, with an exceptionally short electrical path, which leads to an extended battery life. All of these features result in a desirable package for

small, handheld applications.

WLPs are formed on the die while they are still on the uncut wafer. The process can be thought of as an extension of front-end manufacturing in that it involves the entire wafer, but is more similar to bumping for flip chip and tape automated bonding (TAB) operations, as benzocyclobutene (BCB) layers are involved. Being assembled in a batch process, WLPs are also low cost. The result is that the final packaged product is truly die sized, more so than "chip scale." Singulation of the device occurs after the device is fully packaged, unlike traditional forms of packaging.

Reconfigured FOWLPs were introduced in 2006. After devices are manufactured on a wafer, the devices are sown and transferred on a carrier to another larger wafer that has gaps between die, which are filled with overmold material that also coats the back side of the devices for protection. This process allows for a larger surface on which to extend an RDL, thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a PCB.

The leaders in FOWLPs are ranked in **Tables 6** and **7**. STATS ChipPAC is the runaway leader in this area.

FOWLP units (largest to smallest)

STATS ChipPAC

ChipMOS

Amkor

ASE

Table 6: FOWLP units (largest to smallest).

FOWLP revenue (largest to smallest)

STATS ChipPAC

ChipMOS

Amkor

ASE

Table 7: FOWLP revenue (largest to smallest).

Fan-in quad flatpack no-leads

QFN, or quad flat no-leads packages, are a more recent package introduction than the more established packages, such as the small outline (SO) package, but they have quickly attained popularity. The QFN is in the chip-scale package (CSP) category, being close to die-sized. It has leads on four sides of the package that are encapsulated within

the mold compound so that the package rides flat on the PCB. The lack of visible leads protruding from the bottom gives rise to the term “no lead” in this package name.

To further increase the reach of this package, the latest development in QFN packages is to extend the number of rows of leads from the usual one to two or three rows of leads. The lead frame is stamped or etched as in any other lead frame solution, but the leads are of various lengths, either two or three different lengths. When bent downward for connection to the PCB by trim and form equipment, the result is a multi-row, array-patterned package solution with a hole in the center, or fan-in QFN. This allows the number of package leads to extend into the hundreds, up from generally fewer than 50. The resulting package is a high-density, lead frame array package.

The fan-in QFN has the ability to capture the lower end of the QFP (quad flat pack) market. This includes extending its reach to higher bit MCUs and both logic and analog communications chips, largely bound for RF handheld gadgets that require a small form factor package.

Tables 8 and 9 illustrate the rankings of the leading OSAT companies for fan-in QFNs.

FIQFN units (largest to smallest)

STATS ChipPAC
Carsem
UTAC
ASE
Amkor

Table 8: FIQFN units (largest to smallest).

FIQFN revenue (largest to smallest)

Carsem
ASE
STATS ChipPAC
UTAC
Amkor

Table 9: FIQFN revenue (largest to smallest).

Flip-chip

Flip-chip is a form of electrical interconnection between the die and the substrate or lead frame. As the name implies, the die is flipped face down (or active side down) so that the circuitry faces the substrate. Unlike wire bonding, in which the connections are made at

the periphery, flip-chip connections are in an area array covering all or part of the face of the die. Flip-chip is almost always performed on packages with substrates, although a few designs utilize lead frames. The die does not have to be face down with lead frame designs; the lead frame can be designed to reach over the top of the die in a face-up position for interconnection, as is the case with Carsem’s flip-chip on lead frame (FCOL) package. This design maintains the face-up position away from the PCB, preventing cross talk with the PCB, which is important with RF chips.

The electrical connection is made through bumps on the face of the die, which then connect directly to the substrate below. The bumps are in an array pattern on the face of the die, and are placed on the surface of the die while the die are still on the uncut wafer. Individual die can also be bumped, but this is not a cost-effective solution.

Table 10 displays the flip-chip ranking of the leading OSAT companies.

Flip-chip ranking (largest to smallest)

Amkor
ASE
Unisem
Carsem
STATS ChipPAC
SPIL
Hana Micron
ChipMOS
PowerTech
Signetics
UTAC

Table 10: Flip-chip ranking of the leading OSAT companies (largest to smallest).

Biography

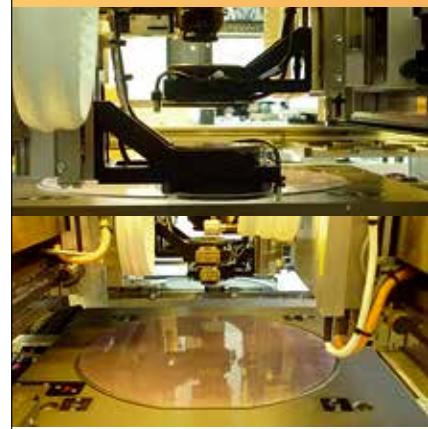
Sandra L. Winkler received an MBA from Santa Clara U. She is on the executive planning committee of the IEEE/CPMT Santa Clara Valley chapter, and serves as Luncheon Program Chair.

Contact information

For more information on these advanced IC packaging solutions, please contact Karen Williams; email: kwilliams@newventureresearch.com



SEMICON WEST 2014
NORTH HALL, BOOTH #6260



High precision Die & Flip Chip Bonder

NOVA PLUS

- Dual Bond Head system
- Die Attach & Flip Chip System
- Fully automatic System
- ± 2,5 µm Placement accuracy
- Cycle time < 3 seconds
- Working area up to 600 x 600 mm



Amicra Microtechnologies GmbH
Wernerwerkstr. 4
D-93049 Regensburg, Germany
Tel: +49- 941-208209 0
e-mail: sales@amicra.com
www.amicra.com

MORE THAN PRECISION

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Advanced Semiconductor Engineering, Inc. No. 26, Chin 3rd Rd., N.E.P.Z. Kaohsiung, Taiwan R.O.C. Tel: +886-7-361-7131 www.aseglobal.com	JP(1), KR (1) MY(1), SG(1) TW(2), US(1)	PB, PL, PN	SD, BP, WP WD, WT AS, FT FT, BI	AD WB, FC MP, UF LP, BA
Advotech Co., Inc. 632 W. 24th Street Tempe, AZ 85282 Tel: +1-480-736-0406 www.advotech.com	US(1)	CB, CL, CN PC	SD, BP WD, AS FT	AD, ED WB, FC GT, UF BA, HS
Amkor Technology Inc.* 1900 S. Price Road Chandler, AZ 85286 Tel: +1-480-821-5000 www.amkor.com	CN(1), JP(1) KR(3), PH(2) TW(3)	CB, CL, CN PB, PL, PN PC, PF WL	SD, BP WP, WD, WT AS, FT ET, BI	AD, ED WB, FC GT, MP, UF LP, BA, LA HS
AmTECH Microelectronics, Inc. 6541 Via Del Oro San Jose, CA 95119 Tel: +1-408-227-8885 www.amtechmicro.com	US(1)	CL, CN PL, PN	SD, WD AS ET	AD, ED WB, GT BA, HS
Azimuth Industrial Co., Inc. 30593 Union City Blvd., Suite 110 Union City, CA 94587 Tel: +1-510-441-6000 www.azimuthsemi.com	US(1)	CL, CN PL, PN	WD, AS	AD, ED WB, MP LP, HS
BOS Tech 216 Doha-ri, Mun Beak Myeon, Jin Cheon-gu Chungbuk, 365-861 Korea Tel: +82-43-532-1785	KR(1)	CL PL, PN PF	SD WD, WT AS	AD, ED WB MP LP HS
Carsem (M) Sdn. Bhd. Jalan Lapangan Terbang, P.O. Box 204 30720 Ipoh, Perak, Malaysia Tel: +60-5-312-3333 www.carsem.com	CN(1), MY(2)	CB, CN PB, PL, PN	SD, WP WD, WT AS, FT ET	AD, ED WB, FC MP, UF LP, BA HS
Chipbond Technology Corporation No. 3, Li Hsin 5th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C. Tel: +886-3-567-8788 www.chipbond.com.tw	TW(2)	PF	SD BP, WP WD, WT AS, FT ET	AD, FC GT, UF

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
ChipMOS Taiwan No. 1, R&D Rd. 1, Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C. Tel: +886-3-577-0055 www.chipmos.com	CN(1), TW(2)	PB, PL, PN PF	SD, BP WD, WT AS, ET	AD, WB FC, UF GT, MP LP, BA
Cirtek Electronics Corporation 116 E. Main Ave., Phase V, SEZ, Laguna Technopark, Binan Laguna, Philippines Tel: +63-49-541-2310 www.cirtek-electronics.com	PH(1)	PL, PN	SD, WP WD, WT AS, FT ET	AD, WB MP, LP HS
Colorado Microcircuits, Inc. 6650 N. Harrison Avenue Loveland, CO 80538 Tel: +1-970-663-4145 www.coloradomicrocircuits.com	US(1)	CB, CL, CN PN, PC	SD WD AS	AD, ED WB, GT MP, HS
Corwil Technology Corporation 1635 McCarthy Blvd. Milpitas, CA 95035 Tel: +1-408-321-6404 www.corwil.com	US(1)	CB, CL, CN PB, PL, PN PC, PF	SD BP, WP WD, WT AS, FT ET, BI	AD, ED WB, FC GT, UF MP, BA HS, LP
Deca Technologies 7855 S River Parkway, STE 111 Tempe, AZ 85284 Tel: +1-480-345-9895 www.decatechnologies.com	PH	WL	BP, WP WD, WT FT	
EEMS Italia SpA. Viale delle Scienze, 5 02015 Cittaducale Rieti, Italy Tel: +39-07-466-041 ? www.eems.com	CN(1), IT(1) SG(1)	PB, PL, PN	SD, WP WD, WT AS, FT	AD, WB BA, MP, LP
Engent, Inc. 3140 Northwoods Pkwy., Suite 300A Norcross, GA 30071 Tel: +1-678-990-3320 www.engentaat.com	US(1)	PB, PN PC	SD, BP WD, WT AS, FT ET	AD, WB FC, UF GT, MP BA
First Level Inc. 3109 Espresso Way York, PA 17402 Tel: +1-717-266-2450 www.firstlevelinc.com	US(1)	CL ?, CN ? PC	SD BP WD AS	AD, ED WB, FC GT, UF BA, LA HS

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Formosa Advanced Technologies Co., Ltd. No. 329, Ho-Nan St., Touliu, 640 Yunlin, Taiwan R.O.C. Tel: +886-5-557-4888 www.fatc.com.tw	TW(1)	PB, PL	SD, WP WD, WT AS, FT BI	AD, WB MP, LP BA
Greatek Electronics, Inc. No. 136, Gung-Yi Rd., Chun'an Cheng, Miaoli Hsien, Taiwan R.O.C. Tel: +886-37-638-568 www.greatek.com.tw	TW(2)	PL, PN	SD, WP WD, WT AS, FT BI	AD, WB MP, LP BA
HANA Semiconductor (Ayutthaya) Co., Ltd. Hi-Tech Industrial Estate Authority of Thailand, 100 Moo 1, T. Baan-Len, A. Bang Pa-In KM. 59 Asia Road, Ayutthaya 13160, Thailand Tel: +66-35-729-300 www.hanagroup.com	CN(1) TH(2) US(1)	PL, PN PF	SD WD, WT AS, FT ET	AD WB, GT MP, LP
HEI, Inc. 1495 Steiger Lake Lane Victoria, MN 55386 Tel: +1-952-443-2500 www.heii.com	US(3)	CN PB PN PF	SD WD AS	AD, WB FT, UF MP, BA
i2a Technologies 3399 W. Warren Avenue Fremont, CA 94538 Tel: +1-510-770-0322 www.ipac.com	US(1)	PB, PL, PN PC, PF WL MC	SD, BP WP, WD WT, AS FT, ET	WB, FC GT, MP LP, BA LA
i3 Electronics, Inc Building 258, 1093 Clark Street Endicott, NY 13760 Tel: +1-866-820-4820 www.i3electronics.com	US(1)	PC	SD WD ?, WT ? AS	AD, WB FC, UF GT, BA
IC Chip Packaging 13490 TI Blvd., Suite 100 Dallas, TX 75243 Tel: +1-972-470-9290 www.icchippackaging.com	US(1)	PB, PL, PN PC	AS	AD, ED WB, GT BA
IDS Electronics Sdn. Bhd. IDS Park, Seri Iskandar, Bota, Perak, Malaysia Tel: +60-5-371-2288 www.idsesb.com.my	MY(1)	PL PN	WP WD, WT AS, FT ET	AD, WB

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Infiniti Solutions Ltd. 122, Middle Road, Midlink Plaza #04-01 Singapore 188973 Tel: +65-6336-0082 www.infinitisolutions.com	US(1) PH(1)	CL, CN PL, PN	SD, WP WD, WT AS, FT	AD, ED, WB MP, LP HS
Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	US(2)	PB, PL, PN, PC, WL, MC	SD, AS, FT	ED, WB, FC GT, MP, UF, BA, LA
Jiangsu Changjiang Electronics Technology Co., Ltd. No. 275, Binjiang Rd., Middle Jiangyin, Jiangsu, China Tel: +86-0510-8685-6417 www.cj-elec.com	CN(3)	PL, PN	WD, WT AS, FT	AD, WB MP, LP
Kingpak Technology Inc. No. 84, Tai-ho Rd., Chu-Pei 302, Hsin-chu Hsien, Taiwan R.O.C. Tel: +886-3-553-5888 www.kingpak.com.tw	TW(1) CN(1)	PB, PN MC	SD WP, WD, WT AS, FT	AD, WB GT, MP BA
King Yuan Electronics Co., Ltd.* No. 81, Sec. 2, Gongdaowu Road Hsin-chu 300, Taiwan Tel: +886-3-575-1888 www.kyec.com.tw	TW(4)	n/a	WP, WD, WT FT, BI	n/a
Kyocera America Inc. 8611 Balboa Avenue San Diego, CA 92123 Tel: +1-858-576-2600 http://americas.kyocera.com/kai/semparts	US(1)	CB, CL, CN PB, PL	SD WD, WT AS, ET	AD, ED WB, FC UF, GT LP, BA HS
Linwave Technology Ltd. Digitek House, Whisby Way, Lincoln Lincolnshire, England, UK LN6 3LQ Tel: +44-1522-681-811 www.linwave.co.uk	UK(1)	CL, CN PC	WD AS FT	AD, ED WB GT HS
Lingsen Precision Industries Ltd. 5-1, Nan 2nd Road, T.E.P.Z. Taichung 42701 Taiwan R.O.C. Tel: +886-4-2533-5120 www.lingsen.com.tw	TW(2)	PB, PL, PN MC	SD, WP WD, WT AS, FT ET	AD, WB MP, LP BA

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal I
Majelac Technologies, Inc. 262 Bodley Road Aston, PA 19014 Tel: +1-610-459-8786 www.majelac.com	US(1)	CL, CN PB, PL, PN PC	SD WD AS	AD WB, FC GT, MP, UF BA, HS
Microelectronic Assembly Frankfurt(Oder) GmbH Otto-Hahn-Strasse 24 Frankfurt(Oder) 15236, Germany Tel: +49-335-387-1963 www.maf-ffo.de	DE(1)	CL, CN PL, PN PC	WD AS	AD, WB MP, LP
Microelectronic Packaging Dresden GmbH Grenzstrasse 22 Dresden 01109, Germany Tel: +49-351-213-6100 www.mpd.de	DE(1)	CL, CN PL, PN PC	WD, WT AS	AD, WB FC, UF GT, BA
Micross Components, Inc 7725 N. Orange Blossom Trail Orlando, FL 32810-2696 Tel: +1-407-298-7100 www.micross.com	US(1)	CB, CL, CN PB, PN, PC, PF WL	SD BP, WP WD, WT AS, FT ET, BI	AD, ED WB, FC GT, UF MP, BA HS
Millennium Microtech Thailand 17/2 Moo 18, Suwintawong Rd., Tambon, Saladang, Bannumprielu, Chacherngsao 24000, Thailand Tel: +66-38-845-530 www.m-microtech.com	TH(1)	CL, PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, ED WB, MP LP, HS
NANIUM S.A * Avenida 1º de Maio 801, 4485-629 Vila do Conde, Portugal Tel: +351-252-246-000 www.nanium.com	PT(1)	PB PN, PC WL	SD, BP WP, WD, WT AS, FT ET, BI	AD, ED WB, FC GT, MP UF BA
Optocap, Ltd. 5 Bain Square Livingston, Scotland, UK EH54 7DQ Tel: +44-1506-403-550 www.optocap.com	UK(1)	CL, CN	SD, WD AS, ET	AD, ED WB, FC GT, UF, MP BA, HS
Orient Semiconductor Electronics No. 9, Central 3rd Street, N.E.P.Z., Kaohsiung 811 Taiway R.O.C. Tel: +886-7-361-3131 www.ose.com.tw	TW(1) PH(1)	PB PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB FC, UF MP, LP
Pantronix Corporation 2710 Lakeview Court Fremont, CA 94538 Tel: +1-510-656-5898 www.pantronix.com	CN(1) PH(2) US(1)	CL, CN PB, PL, PN PC	SD WD, WT AS, FT ET	AD, ED WB, MP FC, UF LP, BA HS

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Powertech Technology Inc. No. 26, Datong Rd., Hsinchu Industrial Park, Hukou, Hsinchu 30352 Taiwan R.O.C. Tel: +886-3-598-0300 www.pti.com.tw	CN(1) TW(3)	PB, MC PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB MP, LP BA
Promex Industries, Inc. 3075 Oakmead Village Drive Santa Clara, CA 95051 Tel: +1-408-496-0222 www.promex-ind.com	US(1))	CL, CN PL, PN PC	SD, WD AS, ET	AD, ED WB, MP FC, UF GT, HS
Psi Technologies, Inc. Electronics Ave., FTI Special Economic Zone, Taguig Metro Manila, Philippines Tel: +63-2-838-4966 www.psitechologies.com	PH(2)	CL, CN PL, PN	SD, WD AS, FT ET	AD, ED WB, MP LP, HS
Quik-Pak* 10987 Via Frontera San Diego, CA 92127 Tel: +1-858-674-4676 www.quikcpak.com	US(1)	CL, CN PB, PL, PN PC, PF	SD, WD, WT AS, ET BP	AD, ED WB, GT FC, UF BA, MP LP, HS
Samtec Microelectronics 5050-C List Drive Colorado Springs, CO 80919 Tel: +1-719-592-9100 www.samtecmicroelectronics.com	US(1)	CB, CL, CN PC	SD BP, WD AS	AD, ED WB, FC GT, UF BA, HS
Semi-Pac Inc. 1206 #F Mt. View Alviso Road Sunnyvale, CA 94089 Tel: +1-408-734-3832 www.semipac.com	US(1)	CL, CN PC	WD AS	AD, WB GT, HS
Signetics Corporation 483-3 Buphung-ri, Thanhun-myun, Paju-si Gyeonggi-do, Korea 413-840 Tel: +82-31-940-7660 www.signetics.com	KR(2)	CB, PB PL, PN	SD, WP WD, WT AS, FT ET	AD, WB FC, UF MP, LP BA
Sigurd Microelectronics Company No. 436, Sec. 1, Pei-Shing Rd., Chu-Tung Hsin-chu, Taiwan R.O.C. Tel: +886-3-595-9213 www.sigurd.com.tw	CN(1) TW(3)	CN PL, PN	SD, WP WD, WT AS, FT ET, BI	AD, WB MP, LP

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Silicon Turnkey Solutions 801 Buckeye Court Milpitas, CA 95035 Tel: +1-408-904-0200 www.sts-usa.com	US(1)	CL, CN PC, CB	WP, WD AS, FT ET, BI	AD, ED WB, FC GT, UF HS
Siliconware Precision Industries Co., Ltd. No. 123, Sec. 3, Da Fong Rd., Tan tzu, Taichung 427, Taiwan R.O.C. Tel: +886-4-2534-1525 www.spil.com.tw	CN(1) TW(3)	CN PB, PL, PN PF WL	SD, BP WP WD, WT AS, FT ET	AD WB, FC MP, UF LP, BA
Solitron Devices, Inc. 3301 Electronics Way West Palm Beach, FL 33407 Tel: +1-561-848-4311 www.solitrondevices.com	US(1)	CN PL, PN	SD, WD AS, FT ET	AD, ED WB, MP HS
SPEL Semiconductor Ltd. 5 CMDA Industrial Estate, MM Nagar (Chennai) 603209, India Tel: +91-44-4740-5473 www.spel.com	IN(1)	PL, PN	SD, WP WD, WT ? AS, FT ET	AD, WB MP, LP
Stars Microelectronics (Thailand) Public Co., Ltd. 605-606 Moo 2, EPZ, Bang Pa-In Industrial Estate, Klongjig, Bang Pa-In, Ayutthaya 13160, Thailand Tel: +66-35-221-777 www.starsmicroelectronics.com	TH(2)	PL, PN	SD, WD AS, FT ET	AD, WB MP, LP
STATS ChipPAC Ltd. 10 Ang Mo Kio Street 65, #05-17/20 Techpoint, Singapore 569059 Tel: +65-6824-7777 www.statschippac.com	CN(1), KR(1) MY(1), SG(1) TW(1)	PB, PL, PN WL	SD, BP WP, FT WD, WT AS, ET BI	AD, WB FC, UF MP, LP BA, ED
Taiwan IC Packaging Corporation 2, South 3 Road, Kaohsiung Export Processing Zone Kaohsiung, Taiwan R.O.C. Tel: +886-7-815-8800 www.ticp.com.tw	TW(1)	PL, PN MC	SD, WD AS, FT	AD, WB MP, LP
Team Pacific Corporation Electronics Ave., FTI Complex Taguig City 1630, Philippines Tel: +63-2-838-5005 www.teamglac.com	PH(1)	CN PL	SD WD AS, FT ET	AD, WB MP, LP HS

INTERNATIONAL DIRECTORY OF IC PACKAGING FOUNDRIES

Directory data was compiled from company inputs and/or website search and may not be current or all-inclusive as of the date of publication.

COMPANY HEADQUARTERS	MANUFACTURING LOCATIONS	PACKAGE TYPES	CONTRACT SERVICES	ASSEMBLY PROCESSES
Company Street Address City, State, Country Telephone Website	Country (Qty) CN = China ID = Indonesia IN = India IT = Italy JP = Japan KR = Korea MX = Mexico MY = Malaysia PH = Philippines PT = Portugal SG = Singapore TH = Thailand TW = Taiwan UK = United Kingdom US = United States	Ceramic CB = Ball Array CL = Leads/Pins CN = No Leads Plastic (Molded) PB = Ball Array PL = Leads/Pins PN = No Leads Plastic (No Mold) PC = Cavity/Dam PF = Film/Tape Other WL = Wafer Level MC = Multi-Chip	SD = Substrate Design BP = Wafer Bumping WP = Wafer Probing WD = Wafer Dicing WT = Wafer Thinning AS = Assembly FT = Final Test ET = Environmental Test BI = Burn-In	AD = Adhesive/Glass ED = Eutectic/Solder WB = Wire Bond FC = Flip Chip GT = Glob Top MP = Molded Plastic UF = Underfill LP = Lead Plating BA = Ball Attach LA = Lead Attach HS = Hermetic Seal
Tektronix, Inc 2905 SW Hocken Ave. Beaverton, OR 97005 Tel: +1-800-462-9835 www.component-solutions.tek.com	US(3)	CL, PN PB	SD WP, WD AS, FT ET, BI	AD, ED WB, FC MP, UF BA, HS
Teledyne Microelectronic Technologies 1425 Higgs Road Lewisburg, TN 37091 Tel: +1-931-359-4531 www.teledynemicro.com	US(1)	CB, CL, CN, PB PL, PN, PC, PF WL	SD, BP, WP, AS FT, ET, BI	AD, ED WB, FC GT, MP UF, BA LA, HS
Tong Hsing Electronic Industries, Ltd. 55, Lane 365, Yingtao Road, Yinko, Taipei Hsien, Taiwan R.O.C. Tel: +886-2-2679-0122 www.theil.com	PH(1) TW(1)	CN PB	SD, WP WD, WT AS, FT ET	AD, ED WB, MP FC, UF BA, HS
Unisem (M) Berhad 9th Floor, UBN Tower, No. 10 Jalan P. Ramlee, 50250 Kuala Lumpur, Malaysia Tel: +60-3-2072-3760 www.unisemgroup.com	CN(1), ID(1) MY(1), UK(1) US(1)	PB, PL, PN WL	SD, BP WP, WD, WT AS, FT ET, BI	AD, WB FC, UF MP, LP BA
United Test & Assembly Center Ltd. 5 Serangoon North Ave 5 Singapore 554916 Tel: +65-6481-0033 www.utacgroup.com	CN(3), SG(2) TH(1), TW(1)	PB, PL, PN WL, MC	SD, WP WD, WT AS, FT ET, BI	AD, WB FC, UF MP, GT LP, BA
Vigilant Technology Co., Ltd. Ladkrabang Industrial Estate, Export Processing Zone 3, 322 Moo 4 Chalongkrung Rd., Laplatiew, Ladkrabang, Bangkok 10520, Thailand Tel: +66-2-739-6203 www.vigilant-techno.com	TH(1)	PL	SD WD, AS FT, ET	AD, WB MP, LP
VLSIP Technologies Inc. 750 Presidential Drive Richardson, TX 75081 Tel: +1-972-437-5506 www.vlsip.com	US(1)	PB, PL, PN PC	SD, WD AS, FT ET	AD, ED WB, FC GT, UF, MP BA, HS
Walton Advanced Engineering, Inc. No. 18, North First Road, K. E. P. Z. Kaohsiung 806, Taiwan R.O.C. Tel: +886-7-811-1330 www.walton.com.tw	CN(1) JP(1) TW(1)	PB, PL	SD, WP WD, WT AS, FT ET, BI	AD, WB MP, LP BA

Semiconductor packaging, assembly and test in Europe

By Steffen Kroehnert [NANIUM S.A.]

The advance of semiconductor technology has slowly been moving away from developments at the front end of the process line towards improving both cost and performance of the chip packaging assembly and test processes at the back end of the line. So much so, that advanced packaging capability, such as TSV and 3D IC, has now become a significant driver for the whole of the industry.

High-volume manufacturing moved to Asia

It is estimated that some 80-90% of the semiconductor, assembly and test industry has moved to Asia during the last three decades (**Table 1**). In Europe, even the major IDMs such as, Infineon Technologies AG, STMicroelectronics, NXP and Robert Bosch GmbH, moved the majority of their packaging, assembly and test manufacturing to Asia. However, Europe continues to be strong in the design, development and production of semiconductor manufacturing equipment related to packaging, assembly and test and has

strong R&D supported by academic and institutes such as, Fraunhofer, CEA-Leti, and imec. Yet production packaging, assembly and test remains mainly for low- and mid-size volume sensitive, and more complex products. With few exceptions, high-volume manufacturing (HVM) of consumer and commodity products was moved mainly to Asia, generally for cost reasons. The result, which has been learned during the last few years, is that R&D without a certain level of manufacturing “onsite” in Europe does not work long-term, as the manufacturability feedback is missing. The newly established pilot lines might help, but they do not solve the problem.

The advanced packaging in Europe today concentrates mainly on system-in-package (SiP), wafer-level packaging (WLP), MEMs and sensor packaging, the packaging of photovoltaics and optoelectronic devices. It is clearly application driven and crucially serves, in many cases, quite attractive niche markets such as, industrial, security, medical, defense, aerospace and aeronautics by offering packages for

hermetically sealed, high-reliability and advanced designs. Inherently, this means “low-volume” at typically “high-value.” The residual European packaging process can be summarized to be the following steps: application design (ASP), prototype, pre-production, outsource production, which, simplified, means export of designs and know-how. But there is now a change underway.

Semiconductor packaging is becoming fairly more complex

Historically, semiconductor packaging was seen as a post-innovative process step to put some ceramic or plastic around the chip and get either metal leads, solder balls out, or simply larger contact pads exposed to the outside in order bring the chip into the component tester and later solder it to a PCB. The package was not supposed to negatively influence the electrical and thermal performance of the product too much, and it was not supposed to be a cost adder, as it was not perceived to bring added value to the product. Those days are definitely gone.

Today, simple single-chip solutions are being pushed more and more aside in the advanced packaging area by smart system approaches (**Figure 1**). High-speed requirements are driving needs for low package parasitics, mobile applications are pushing the reduction of form factor—mainly height and thermal dissipation challenges need to be solved at the system level. This has slowed down the system-on-chip (SoC) euphoria, leading to partial reduction with integration of SoC moving to the heterogeneous integration of several active chips and passives in the package. This so called system-in-package (SiP) is the reality. This is also known as the “More-than-Moore” versus “More Moore,” which is driven by the continued reduction of the wafer processing technology nodes for SoC.

Sector	Innovation	Design	Manufacturing	Utilization
Aerospace	USA	Europe	Europe	USA
Automotive	Europe	Europe	Asia	Europe
Broadcast	Europe	USA	Asia	Europe
Communications	Europe	USA	USA	USA
Computing	USA	USA	Asia	USA
Consumer	Asia	Asia	Asia	Asia
Industrial	Europe	USA	Asia	Asia
Medical	USA	Europe	Europe	Europe
Military	Europe	USA	Europe	USA
Security	Europe	USA	USA	USA

Table 1: Market generators: Where innovation, design, manufacturing and main utilization happen today, for different markets and applications. Source: PandA 2010

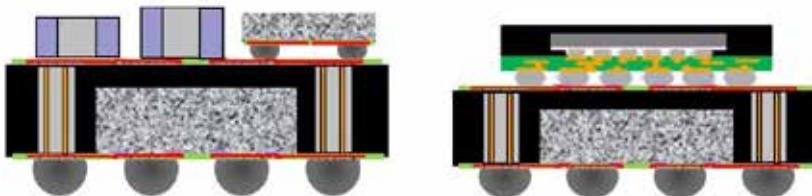


Figure 1: Advanced packaging is getting more complex. Thin package-on-package solutions under 1.0mm total package height using fan-out WLP/eWLB-based bottom package with fan-in WLCSP, flip-chip in package and SMT as top package for mobile applications. (Source: NANUM 2013)

Packaging is coming back to Europe

The package is now very much an integral part of the product and its performance now adds significant value to the product. This is, at last, being acknowledged by the chip designers and system architects, who now have to move closer together to co-design and co-develop new system solutions.

What are the reasons for semiconductor packaging, assembly and test coming back to Europe? First of all, there are the more complex system needs, requiring new technologies and a collaborative approach through the entire supply chain. Also, increasing costs in Asia are making packaging in Europe viable and attractive again. Industry players, especially medium and small size companies, are not only looking at the cost figures, but are also looking at other considerations that can be better provided by the European companies. These are: high level engineering capability, an experienced and knowledgeable workforce right down to the operator level, the high commitment of each employee, low work force churn rates, easy communication, little or no time differences, insignificant costs for travel to the service provider, no real need to install resident engineers onsite and, not the least important – the IP protection.

European industrial strategy for micro/nanoelectronics



The “EU 10/100/20” Factsheet summarizes the cornerstones: on May, 23, 2013, Mrs.

Neelie Kroes, European Commission Vice-President, launched an ambitious new strategy to get 20% of global semiconductor manufacturing market

back to Europe by 2020. This will be achieved by an unprecedented public/private investment partnership: €10 Billion public/private funding for research and innovation, plus € 100 Billion from industry for manufacturing. This strategy is more than just a vision, it is a major opportunity to participate in large-scale investment projects. The strategy is also important, as this is the first clear statement by public

FAST & ACCURATE

NEW



Accurate Dual Valve Dispensing



Self-Actuating Tilt Jetting



SPECTRUM II

Nordson ASYMTEK's Spectrum™ II

high-speed, high-accuracy dispensing platform sets a new standard for precision dispensing applications in microelectronics & semiconductor manufacturing and MEMS & LED assembly. Jet small dots and thin lines into tight spaces with Tilt Jetting and Precision Z-gap Control. Maximize productivity with Dual Valve Dispensing while saving manufacturing floor space with Spectrum II's small footprint.



www.NordsonASYMTEK.com/S2
Watch the Video or contact us at
info@nordsonasymtek.com

See Nordson ASYMTEK
at IPC APEX Expo
Booth #1937



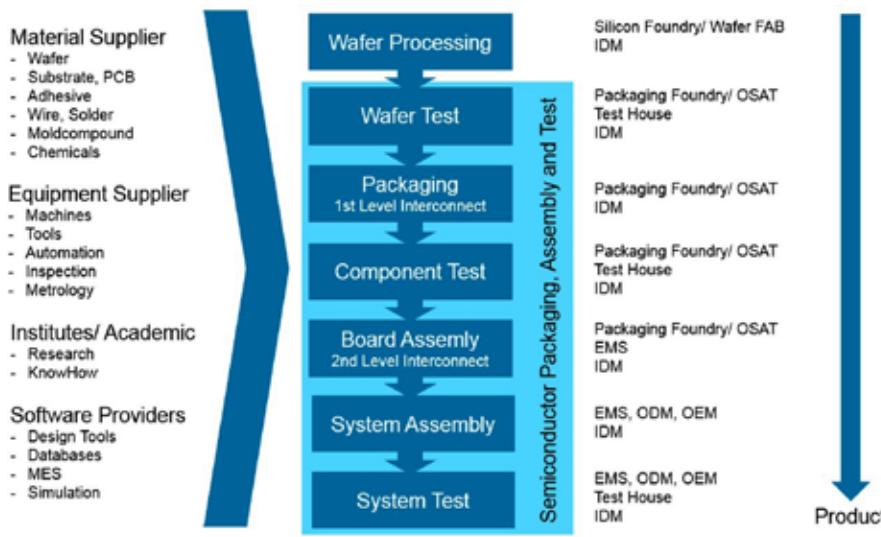


Figure 2: Semiconductor supply chain: the main focus today is still on wafer processing, but the entire supply chain needs to be considered, including semiconductor packaging, assembly and test.

authorities in Europe that they are committed to reinforcing semiconductor manufacturing-related investment in Europe.

The strategy will, along with other measures, reverse Europe's declining trend in micro- and nanoelectronics manufacturing, focus on Europe's strength, and support cross-border cooperation to create critical mass in knowledge and financing, investments in "More-than-Moore" on 200mm and 300mm, "More Moore" on 300mm, and the 450mm transition.

The strategy is targeting the integration of leading manufacturers, research centers and small and medium-sized enterprises (SMEs) into the value chain by offering access to the latest technology and state-of-the-art research facilities, and the entire supply and innovation chain (research, design, materials, equipment, manufacturing processes, device makers) (**Figure 2**). Furthermore, the strategy will focus on European clusters of excellence (Dresden, Grenoble, Eindhoven/Leuven) and there will be cooperation with specialized clusters elsewhere. Europe, however, does not have an existing specialized European packaging, assembly and test cluster of excellence yet, especially when talking about manufacturing. So the European players in this arena should consider the formation of such a cluster.

By estimating that just 10% of the supply chain is related to packaging,

assembly and test manufacturing services, the investments in this area, driven by the EU 10/100/20 initiative will be around €11 Billion, of which €1 Billion is publicly/privately funded, and €10 Billion is invested by the industry. Looking at the packaging, assembly and test industry that remains in Europe, it is obvious that support from the large European IDM and/or from the large packaging foundries and outsourced semiconductor assembly and test services (OSATS) such as, ASE Group, Amkor Technology, STATS ChipPAC, SPIL and UTAC Group, would be welcome to invest in Europe to build long-term manufacturing capabilities and capacities and bring manufacturing jobs to Europe.

Positioning of European semiconductor packaging, assembly and test

Following an initiative of the largest European packaging foundry/OSAT, NANUM S.A. in Portugal, together with specialized consultancy PandA (Packaging and Assembly) Europe, an industry interest group called "ESPAT" (European Semiconductor Packaging, Assembly and Test) has been started. ESPAT intends to work closely with the European branches of the industry associations, including SEMI



Preliminary: European semiconductor packaging, assembly and test

(Semiconductor Equipment and Materials International) and its Advanced Packaging Conference (APC) Committee, the GSA (Global Semiconductor Alliance), and IMAPS-Europe.

The ESPAT initiative is set down as follows:

Scope. European semiconductor packaging, assembly and test manufacturing companies of all types and sizes are included:

- High, medium and small volume manufacturing sites;
- Manufacturers of prototypes, samples and small series in lab scale;
- Engineering and manufacturing services of equipment suppliers;
- Packaging, assembly and test activities of European IDMs in Europe; and
- Companies interested in investing in packaging, assembly and test manufacturing in Europe).

Objectives. The objectives are several:

- To promote the increasingly important role of ESPAT in the semiconductor supply chain:
 - More-than-Moore, heterogeneous system integration, system-in-package; and
 - Chip-package-board co-design and co-development.
- To build-up a platform for European semiconductor packaging, assembly and test manufacturing players;
- To give them a voice at the European Commission in Brussels; and
- To build European strength in assembly and test by proposing cooperative efforts to complement and develop capabilities.

Strategy. The strategy is two-fold:

- Influence and participate in "EU 10/100/20" Industry Strategy/Horizon2020 funded projects (when considering the entire semiconductor supply chain, ESPAT makes up an estimated 10% of this supply chain, so the funding should be appropriate); and
- Build-up manufacturing capability and capacity in Europe for pilot lines and beyond.

Tasks. First of all, the new ESPAT Industry Interest Group will interact

with its members and partners to analyze what is available in terms of semiconductor packaging, assembly and test manufacturing in Europe, and what are the strengths. The aim is to create and make available a “Packaging, Assembly and Test Manufacturing Service Provider in Europe Directory” showing who is doing what, and showcase and promote those services in a consolidated way to the customers.

The next step is to analyze the gaps by comparing current capabilities and capacities with international package technology roadmaps provided by recognized market research institutes and associations and customer roadmaps. The gaps will need to be made known to the decision makers in the European Commission. We will discuss together what is needed to close those gaps. The themes for funded project calls have been influenced in a way to support those topics. In order to close those gaps, we will need to build-up cooperative efforts, targeting ways to motivate smaller and mid-sized manufacturing companies to participate in funded cooperative projects in order to benefit from the new industry strategy. It is essential for success that we ensure the creation of a “win-win” situation for all participating packaging, assembly and test manufacturing companies.

Mid-term, it is planned to convert the ESPAT Industry Interest Group into an officially registered Special Interest Group (SIG), possibly inside the SEMI organization, in order to run the necessary advocacy work and underline the importance of this part of the semiconductor supply chain.

It is planned to have a first face-to-face meeting of the ESPAT Industry Interest Group at Semicon Europa 2014 from October, 7-9, 2014, in Grenoble, France.

Additionally, during the Advanced Packaging Conference (APC), held in conjunction with Semicon Europa 2014, a panel discussion “Packaging in Europe – High Value, Low Volume?!” is planned. This will be the first opportunity to showcase ESPAT European packaging, assembly and test capabilities, capacities, and plans in a consolidated way.

Finally, during Q1/2015, a SEMI Europe Networking Day is planned

at NANUM in Vila do Conde, Portugal. At this event, ESPAT will again showcase “European Packaging, Assembly and Test” and bring the European manufacturing supply chain together with policies, associations, customers, and suppliers.

Biography

Steffen Kroehnert received his master's degree in Electrical Engineering

and Microsystems Technologies from the Technical U. of Chemnitz, Germany, and is Director of Technology at NANUM S.A.; he is also a co-chair of the SEMI Europe APC Committee; email steffen.kroehnert@nanium.com; and/or Andy Longford, Managing Director, PandA Europe, and a co-chair of SEMI Europe APC Committee; email andy@pandaeurope.com



LITHOGRAPHY SOLUTIONS FOR HIGH-VOLUME MANUFACTURING

- Advanced Packaging for Logic and Memory
- Ultra-High Throughput and Productivity
- Mid-End and Back-End Interconnect Applications



GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com



Electronics reliability cannot be assured if it is not quantified

By Ephraim Suhir [Portland State U.]

"A pinch of probability is worth a pound of perhaps." James G. Thurber

Despite all the existing effort, electronic products that underwent highly accelerated life testing (HALT), passed qualification testing (QT) and survived burn-in testing (BIT), often fail in the field. Are today's reliability assurance efforts and practices adequate? If they are not, what could be done differently so that the failure-free performance of a product that passed QT is assured? On the other hand, HALT, if successful, is supposed to create significant (although unknown) safety margins. Could this result in an over-engineered product whose cost is considerably higher than necessary? Reliability cannot be low, but it does not have to be higher than necessary either; it has to be adequate for a particular application. The best product is the best compromise between its reliability, cost-effectiveness and time-to-market. Could a superfluously high reliability of an over-engineered product

be reduced so that the product's cost is as low and its time-to-market is as short as possible? To answer these questions one has to be able to quantify reliability. This is particularly important for industries and applications where high reliability is imperative and the performance of many non-electronic systems is strongly dependent on the reliability of electronic and opto-electronic products.

Accelerated testing

Shortening of a product's design and development time does not allow for time consuming reliability investigations in today's industrial environment. The major goals of a manufacturer are: achieve maximum reliability information in minimum time and at minimum cost, and shorten the time-to-market. Accelerated testing (AT) is therefore both a must and a powerful means in electronics design and manufacturing when making a viable device into a reliable product (**Table 1**).

HALT is the most widespread accelerated test today used to discover failures.

Today's HALT

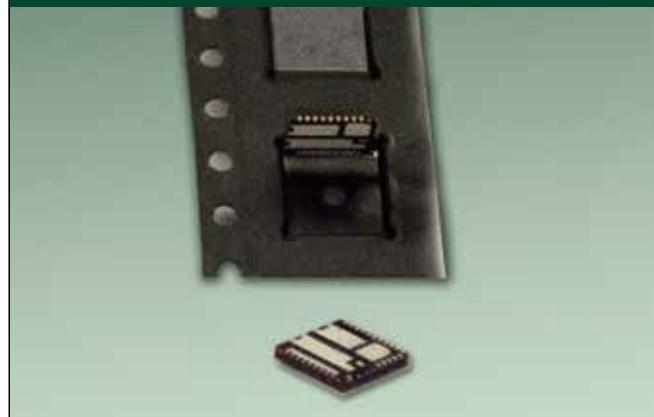
There is a widespread perception that today's HALT is able to assure operational reliability. Well, if so, why do the products that underwent HALT and even passed the existing QT, often fail in the field?

HALT began about 40 years ago with an objective to discover product's weaknesses and to obtain large safety margins over the expected in-use conditions by subjecting the product to stresses well beyond the expected field stresses. HALT uses all stresses, not necessarily limited to those that might indeed occur in the field, but all those, or at least many of those, that could possibly cause failures. For example, random vibrations are often used to weed out infant mortalities, even if the device is not expected to encounter shocks or vibrations

Accelerated test (AT) type	Product development testing (PDT)	Highly accelerated life testing (HALT)	Qualification testing (QT)	Burn-in testing (BIT)	Failure oriented accelerated testing (FOAT)
Objective	Technical feedback to assure that the taken approach is acceptable	Ruggedize the product and assess the reliability limits	Demonstrate that the product is qualified to serve in the given capacity	Eliminate the infant mortality part of the bathtub curve	Understand physics of failure, confirm use of a particular predictive model, assess the probability of the field failure
End point	Type, time, level, and/or the number of observed failures	Pre-determined number or percent of failures	Pre-determined time and/or the number of cycles and/or excessive (unexpected) number of failures	Pre-determined time and/or loading level	Predetermined number or percent of failures
Follow-up activity	Failure analysis, design decision	Failure analysis	Pass/fail decision	Shipping of sound products	Failure and probabilistic analysis of test data, predicted probability of field failure
Ideal test	Specific definitions	No failures in a long time	No failures in a long time	No failures in a long time	Numerous failures in a short time

Table 1: Accelerated test types.

BiAgX™ High Temperature Pb-Free Solder Paste Technology



BiAgX™

- Drop-in replacement for high-Pb solder paste
- Pb-free and Sb-free
- Solidus >260°C after reflow
- MSL1 proven per IPC/JEDEC J-STD-020D



Learn more:
<http://indium.us/E036>

From One
Engineer
To Another®

www.indium.com
askus@indium.com



ASIA • CHINA • EUROPE • USA

©2014 Indium Corporation

in its actual use. HALT can be performed on any level: assembly, device, package, module, board, subsystem, or system.

While HALT's objective is to create significant margins of safety with respect to the field conditions, it does not suggest how to establish (quantify) these margins. HALT tries, often successfully, to "kill many unknown birds with one stone." That is why many practicing reliability engineers are convinced that HALT has demonstrated over the years its ability to improve robustness of a product through a "test-fail-fix" process.

Temperature cycling is usually viewed as the most crucial type of HALT. Vibration – particularly random vibration tests – are viewed as its second most important type. It is often recommended that HALT starts at low stress levels and steps up the stresses during the test process until failure occurs. Then the failure is analyzed. After the cause of the failure is determined and improvements are made, the initial stress is increased and the process is repeated. HALT stops when an acceptable, although unclear, technological limit is determined.

HALT is not associated with any predictive modeling (PM) and does not measure reliability. Since the imposed stresses are not limited to the field stresses, HALT is unable to separate relevant from irrelevant failure modes. HALT is not a knowledge-oriented effort and is not aimed at understanding the physics of failure, not to mention any quantitative evaluations. In today's practice, HALT might be a rather expensive undertaking, both because it is run as a "black box" activity and because it is often conducted as an iterative process.

Thus, it should be concluded that although the current HALT practices and techniques can improve a product's operational performance, HALT does not quantify reliability, and, as a consequence of that, is unable to assure it. In addition, HALT might lead to an over-engineered and, hence, to an unjustifiably expensive product.

Probabilistic design for reliability (PDfR) concept

Application of the probabilistic design for reliability (PDfR) concept [1] enables one to quantify electronics and opto-electronics reliability and has a potential, therefore, to dramatically improve the state-of-the-art in the field. The concept proceeds from the rationale that nothing is perfect, and that the difference between a highly reliable and an insufficiently reliable product is "merely" in the level of the never-zero probability of its failure. The PDfR concept has a solid experimental basis because it includes highly focused and highly cost-effective failure-oriented-accelerated-testing (FOAT). It has also a strong and well substantiated theoretical basis because it employs effective, easy-to-use and physically meaningful PM, both analytical (mathematical) and computer-aided (simulations). PM enables one to validate the relevant models, to better understand the underlying physics of failure and, based on the FOAT data, predict the probability of failure in the field. Extensive sensitivity analyses (SA) are the third important constituent of the PDfR concept. SA are carried out when there is a need to determine what could possibly be done to improve, if necessary, the predicted operational reliability of the product. All the modeling is done on a probabilistic basis.

FOAT: a part of PDfR, and extension of HALT

FOAT should be geared to a particular predetermined PM

that enables one to bridge the gap between what is observed as the result of FOAT, and what will most likely take place in the field. FOAT's objective is, first of all, to confirm the validity of a particular pre-established PM [2], such as, e.g., Arrhenius' equation, Boltzmann-Arrhenius-Zhurkov's (BAZ) model [3], crack growth models, various Coffin-Manson's relationships, etc. It should be emphasized that all these models can be interpreted in terms of the probability of failure under the given loading conditions and after the given time in operation, and that the accumulated experimental data based on numerous non-BAZ models can be represented in the form of the BAZ model, particularly when a multi-parametric BAZ model is employed. FOAT enables one to establish the underlying physics of failure, determine the numerical characteristics (activation energy, time constant, exponents, if any, etc.) of the particular PM of interest, and, since the principle of superposition does not work in reliability physics, decide on a suitable and meaningful combination of the applied loads (stresses).

Understanding the underlying reliability physics is always critical, and, if one sets out to identify and to understand the physics of failure in an attempt to create a failure-free product, conducting a well thought out and adequately interpreted FOAT is certainly crucial. Well planned, carefully carried out, and properly interpreted FOAT provides a consistent and a "reliable" basis for the prediction of the probability of failure in the field. Various structural, materials and/or technological improvements can be "translated" using FOAT data and SA into the probability of failure of the product for the given duration of operation under the given service (environmental) conditions. Numerous practical examples can be found in references below.

FOAT is not in contradiction with HALT. On the contrary, FOAT should be viewed as a modification and an extension of HALT and could be considered, planned and conducted as part of the general HALT effort. HALT is a "black box." This well established and, in general, successful methodology could be conducted, in terms of its inputs and outputs, without a clear knowledge of the underlying physics and the anticipated

likelihood of failure. FOAT is a "white box" that can enhance the merits of HALT and compensate for its shortcomings. FOAT can complement HALT when there is a wish and a need to understand the underlying physics of failure and quantify reliability. There might be also situations when FOAT can be used as a substitution for HALT and even for the QT, especially for new products, when acceptable QT standards do not yet exist and best practices have not yet been developed.

While HALT does not measure (quantify) reliability, FOAT does. HALT can be used, therefore, for "rough tuning" of the product's reliability, and FOAT should be employed when "fine tuning" is needed. FOAT could be viewed as a quantified and reliability physics oriented HALT.

FOAT should be conducted for the most vulnerable elements of the design. These elements could be determined, for example, from the HALT tests. The scope and the cost of FOAT should be different for different products and applications. Use of FOAT can dramatically facilitate the solutions to many engineering and business-related problems associated with cost effectiveness and time-to-market. This is because FOAT, along with an appropriate PM and SA, enables one to create a reliable product with the predicted, assured and, if necessary and appropriate, even specified operational probability of failure. The role of the human factor can be considered, if necessary, within the framework of the suggested PDfR concept when there is a need to quantify the success and safety of a particular mission in which human performance, equipment reliability and uncertain-and-harsh environment contribute jointly to a particular mission success and safety [4].

Like HALT, FOAT should be conducted in addition to, and before the QT. Although the FOAT-based predictions might not be perfect, at least at the beginning, until more or less accurate methodologies and algorithms are developed and validated, it is still better to pursue FOAT and master it, rather than to turn a blind eye on an always non-zero probability of failure and trying to convince the engineering community that HALT is the perfect and ultimate tool for assuring electronics reliability.

Summary

Electronics reliability has to be quantified to be assured, and therefore, the widely used today's HALT methodologies and procedures, although able to improve the operational reliability of the product, cannot assure it. FOAT should be employed when reliability is imperative and therefore the ability to quantify it is highly desirable. FOAT could be viewed as a modification and an extension of HALT. The PDfR concept can not only help to understand the physics-of-failure of an electronic product, but, most importantly, can enable one to predict, quantify and assure its failure-free performance in the field. The use of the PDfR concept can also be helpful in the development and implementation of the new generation of the most feasible and effective QT methodologies, practices and specifications.

References

1. E. Suhir, "Probabilistic design for reliability," *Chip Scale Review*, vol.14, No.6 (2010).
1. E. Suhir, "Predictive modeling is a powerful means to prevent thermal stress failures in electronics and photonics," *Chip Scale Review*, vol.15, No.4, July-August (2011)
2. E. Suhir, A. Bensoussan, "Application of multi-parametric BAZ model in aerospace optoelectronics," 2014 IEEE Aerospace Conf., Big Sky, Montana, March (2014).
3. E. Suhir, "Human-in-the-loop, and the likelihood of vehicular mission-success-and-safety," *J. of Aircraft*, vol.49, No.1, (2012).

Biography

Ephraim Suhir received his MS from the Polytechnic Institute, Odessa, Ukraine, and PhD from Moscow State U. Among his honors, he is a Fellow of the American Physical Society (APS), the Institute of Physics (IoP), UK, Institute of Electrical and Electronics Engineers (IEEE), and the International Microelectronics and Packaging Society (IMAPS). He is on the faculty of Portland State University, Portland, OR. Email: suhire@aol.com



without
limits.

EXPAND YOUR BUSINESS WORLDWIDE



Discover the Power of SEMI[®] Global Expositions

Whether you are looking to explore new regions, technologies, or markets, SEMI Expositions are the ideal platform to showcase your brand, connect to customers, and grow your business worldwide. Let SEMI help you build an exhibition and marketing program that gains maximum exposure and takes your business to the next level!

For the complete schedule of SEMI Expositions,
visit www.semiexpos.org

Upcoming SEMI Expositions

SEMICON Singapore 2014
April 23–25
Singapore
www.semiconsingapore.org

SEMICON Russia 2014
May 14–15
Moscow, Russia
www.semiconrussia.org

SEMICON West 2014
July 8–10
San Francisco, USA
www.semiconwest.org

SEMICON Taiwan 2014
September 3–5
Taipei, Taiwan
www.semicontaiwan.org

SEMICON Europa 2014
NEW VENUE October 7–9
Grenoble, France
[www.semconeurope.org](http://www.semiconeuropa.org)

**PE 2014 Exhibition
and Conference**
October 7–9
Grenoble, France
www.plastic-electronics.org

SEMICON Japan 2014
NEW VENUE December 3–5
Tokyo Big Sight, Japan
www.semiconjapan.org

SEMICON Korea 2015
February 4–6
Seoul, Korea
www.semiconkorea.org

LED Korea 2015
February 4–6
Seoul, Korea
www.led-korea.org

SEMICON China 2015
March 17–19
Shanghai, China
www.semiconchina.org

FPD China 2015
March 17–19
Shanghai, China
www.fpdchina.org

LED Taiwan 2014
March 25–28
Taipei, Taiwan
www.pvtaiwan.com

Large panel fan-out wafer-level packaging: accuracy is king

By Johann Weinhaendler [Amicra Microtechnologies, GmbH]

Diven by ever smaller portable and wearable mobile data devices, fan-out wafer-level packaging (FOWLP) and its embedded wafer-level ball-grid array (eWLB) variant are on a roll to market penetration and technological maturity. Thinner packages and wide I/O are the top considerations. Cost, expressed as process throughput and yield, and reliability, are moving to the forefront as volume manufacturing takes hold.

Fan-out wafer-level processing: a promising option

A rapidly developing outsourced semiconductor and test (OSAT) infrastructure led by dedicated technology pioneers has paved the way to first, FOWLP single- and multi-die implementations, such as DSP baseband, RF transceivers, or power management, realizing high I/O complexity of up

to a 1000 "pins." This situation is contributing to the improving cost situation when compared to other options in complex packaging concepts, such as 2.5D TSV integration.

A recent FOWLP packaging roadmap outline provided by French market researcher Yole Développement, places FOWLP Gen 2, comprising multi-chip package (MCP), system-in-package (SiP), and PoP package-on-package (PoP) right at the transition of 2013 to 2014. Dynamic random access memories (DRAMs), NAND Flash, APE/BB modems, RF functions, as well as PMU/PMIC, low-end ASICs, and MCUs, have been in production since 2012 (**Figure 1**).

Historically, there is a fork in the road – one side pointing to the continued wafer size evolution from 300mm to the envisioned 450mm era (not expected before 2018), the other to the deployment of ever larger rectangular

panels, which could outdo the circular wafers. This fork in the road occurred in 2011. From there, panelization has evolved to standard sizes of 204 x 508mm, or 8" x 20" (comprising semiconductor and PCB substrates), as well as 300 x 300mm (LCD and PCB).

But FOWLP Gen 4 is already waiting in the wings: with still larger panel formats of 650 x 830mm (LCD), 400 x 505mm (PCB), 470 x 370mm (LCD Gen 2), and 380 x 380mm (WLP/LCD). There is opportunity to address placement accuracy and the mechanical handling of these oversize panels.

Prepared for WLP Gen 4

According to Yole's roadmap sketch of 2012 (**Figure 1**), the transition to Gen 4 is predicted to take place in 2015 – with ADL, Qualcomm, STMicroelectronics, and others, at the helm. Looking out further to the future, Yole is prognosticating the fusion of the WLP/PCB/LCD manufacturing infrastructures in 2016 and beyond.

To get to WLP Gen 4, assembly yields of 98% are required – and achievable. This necessitates a capital-intensive manufacturing and supply-chain infrastructure to be developed from the modest beginnings of today, if not a full-scale consolidation of the front end and back end process segments into one single fab environment. At present, the move to panelization (reconfigured boards vs. large-diameter original wafers) seems to take precedence – driven by a cost perspective, because the existing 300mm equipment and process setups can be re-used and applied to large FOWLP applications.

The challenge for WLP equipment vendors, then, is to catch the wave of the present Gen 1 and Gen 2 applications and provide suitable equipment, while at the same time, keeping all options open for the anticipated roadmap progress toward Gen 4.

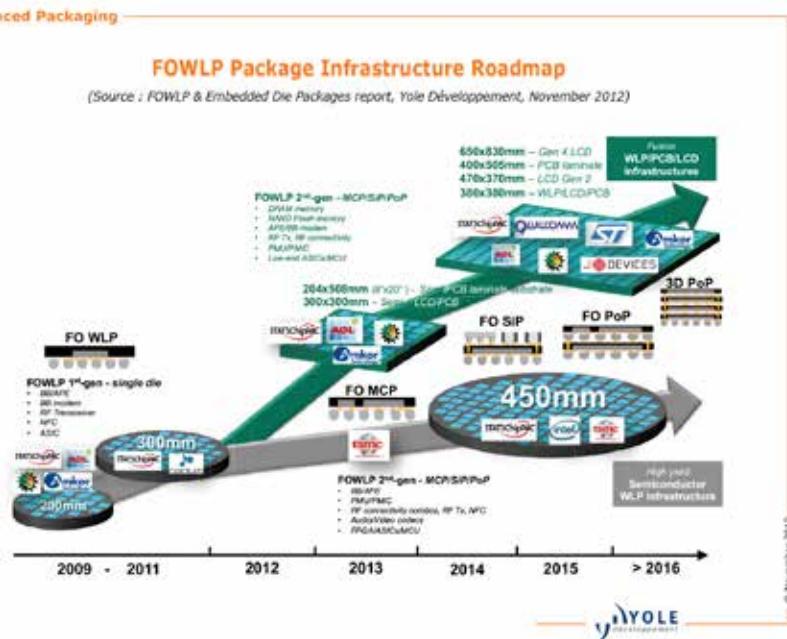


Figure 1: Fan-out packaging infrastructure roadmap according to French market researcher Yole Développement. Source: Yole Développement, 2012.

Placement precision takes precedence

As evidenced by one-on-one discussions with end users of die bonding and die-attach equipment at the recent Productronica 2013 in Munich, it turned out that an automatic dual-head die-attach and flip-chip bonding capability at a placement accuracy of $+2.5\mu\text{m}$ at 3 sigma is high on the wish list of machine users; and if possible, at cycle times below 3s.

The most appropriate way to get there appears to be an evolutionary path based on a modular machine concept to accommodate various process variants and applications. The solution must also aim for volume production of WLP, TSV, and embedded chip structures. That would automatically provide a competitive advantage to both machine vendor and user, especially in regard to the larger panel sizes coming into play right now. Most of the OSATS are still using standard placement machines for FOWLP applications. But this type of

equipment clearly does not measure up to the requirements on bonding accuracy necessary for large FOWLP. Best suited for such applications would be a modular machine concept combining an integrated dispensing system, two mounting heads and a flip-chip module.

Another requirement these days is the capability of processing 300mm wafers, as well as rectangular panels. Even panels of up to 600 x 600mm in size – presently far ahead of the roadmap curve – should possibly be accommodated. Also helpful in this regard is a fan-out wafer chuck configuration that is laid out for future 450mm wafers.

And the wish list continues: a large automated panel transport for fan-out panels up to 370 x 470mm would be of advantage to manufacturers. Also advantageous would be an input buffer providing a working area of up to 600 x 600mm (**Figure 2**); such a capability would enable end users to be ahead on the learning curve of process technology.

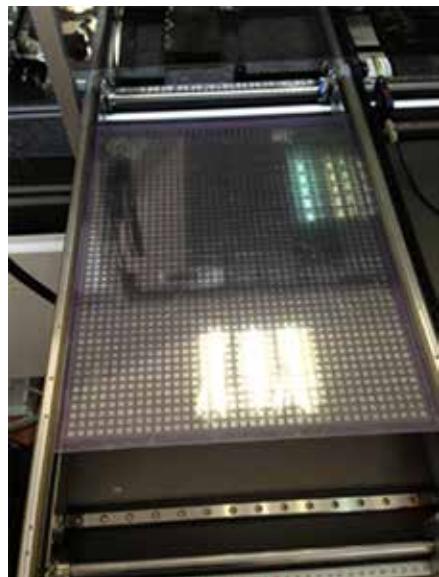


Figure 2: Input buffer unit for panels up to 600 x 600mm in size. Source: Amicra

Measurement results of a 300mm application

A real-world application of a NovaPlus system at an Asian end user's

High Speed / Low Cost Development, Test & Burn-In Sockets

Compression, SMT, & Thru-Hole PCB Mounting

Lead pitches as low as 0.4mm, up to 125,000 insertions.



Quick
On/Off Lid



Easy Screw - Lid
removed to show detail.



Easy Knob
configuration

Multi-Cavity Sockets

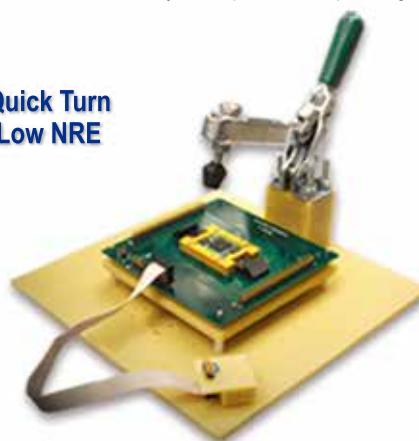
Significantly reduce your socket & labor costs with these multiple IC test and burn-in solutions.



Custom Test Fixtures

Fully automated or manually operated solutions to test any lead pitch & IC package

Quick Turn Low NRE



ET[®] **EMULATION
TECHNOLOGY, INC**

1-800-232-7837

www.emulation.com

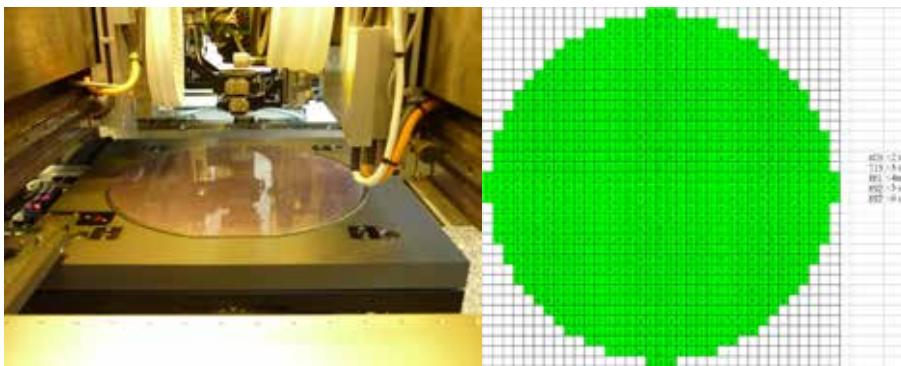


Figure 3: a) (left) 300mm (12") diameter wafer in the transport channel of the NovaPlus; b) (right) End user measurements in a 12" wafer application. Source: Amicra

facility required the bonding of die (not flipped) to 12" (300mm) glass and metal wafers, coated non-conductive epoxy on glass wafers, and non-conductive foils on metal wafers. There were no reference marks provided. All die were positioned within a 6 μm distance of their nominal positions. The bond force reached up to 2000cN. Tools heated up to 200°C were used in this process. Throughput at 3 μm accuracy is specified at >120 units per hour. At 10 μm , the process delivers up to >1,500 units per hour. In both cases, the bond time of 500ms is included. The end user's measurements are shown in **Figure 3**.

Measurement results of a 370 x 470mm application

Another fan-out process at a different user's facility was laid out as a 370 x 470mm application, with ample space left for eventually working with even larger panels of up to 650 x 830mm. This is a good example of Amicra's present capabilities – with enough space left for accommodating larger panels, even up to 650 x 830mm.

The actual requirement was: bonding a non-contacting foil on glass wafers and boards, plus the processing of flipped and not-flipped die, measuring from 1 x 1mm up to 20 x 20mm. Substrate sizes ranged from 8" to 12" wafers, as well as 370 x 470mm boards; also required was being able to provide an extremely large working area of up to 600 x 600mm.

In terms of process accuracy, the application required a 3 μm machine capability, and 10 μm in terms of real processed parts. All of these were to be measured and confirmed by the user. At 3 μm accuracy, the throughput

expectation was >1200 UPH; at 10 μm it was 2000 UPH, both for 8" wafers. The actual results came out very close to these conditions: for the 8" application with real parts, the processed accuracy across the entire board area came very close to the specified 3 μm machine capability. In a 370 x 470mm board application, accuracy was better than 10 μm .

Both final measurements were taken by the end user. With large panels, there is still room for accuracy improvement: the target is 5 μm . The system uses just four reference "production" chips placed in the four corners of a board and then subsequently, aligning all other chips across the board relative to these four exposed locations. The concept, as opposed to other schemes deploying reference chips every 10cm, is aptly termed "relative placement."

As for die thickness, the application was tested to work down to 50 μm for die measuring 5 x 5mm, with UV tape of a very low stickiness. On the system used for this end user evaluation, the integrated flux unit was used.

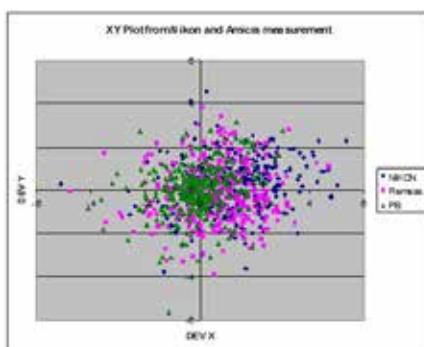


Figure 4: XY plot for a 12" wafer application taken by the end user on Nikon equipment and repeated by Amicra. Source: Amicra

Figure 4 shows an XY plot based on Nikon's measurement at the end user's premises and by Amicra. The results: C_{pk} for the 10 μm specification on a 12" wafer yielded an X of 2.0, and a Y of 2.6. For the 370 x 470mm board application with 10 μm accuracy specifications, the results were: X = 0.97 and Y= 1.03, in this case based on Mitutoyo measurement equipment and processes. All indications so far point in the direction of achieving improvements to a C_{pk} value of 2.0 (10 μm spec) and a C_{pk} of 1.0 (at a 5 μm spec). This would also pertain to very large boards.

At present, we are working with two end users in the indicated application areas. The first wants to place just two reference die. These are actually productive die and are used for further adaptations of the system in other processes at the fab. After placing these first two reference die, they are remeasured in terms of their alignment and a map of the exact locations of the other die is developed. The measurement of the reference die is then repeated at appropriate time intervals, as is the map calculation. This is to counter the effects of temperature drift in the system relating to the X/Y and phi results. These reference die are also used for accommodating other types of die to be placed. They also allow for the interruption of the placement process at any time. In this manner, a time lapse of several months until finishing the placement is possible without any loss of accuracy.

The second end user has expanded its application to use four reference die. This enables not just a drift compensation in terms of X/Y and phi, but it also allows for a compensation of thermal and mechanical board expansion. The calculated reference map is scaled accordingly.

Biography

Johann Weinhaendler holds a degree in electrical engineering, an MBA from Open U. Business School (UK), and a doctoral degree in marketing from Trinity College (Dublin, Ireland); he is Managing Director of Amicra Microtechnologies GmbH; email: johann.weinhaendler@amicra.com

Precision epoxy dispensing combined with traceability

By Willibald Konrath, Klaus Scholl, Haiko Schmelcher [*TESAT Spacecom GmbH & Co. KG*] and Cyriac Devasia, Ravi Balasubramanian [*MRSI Systems, LLC*]

Demand of satellite communication systems has been growing rapidly during the last few years. Delivery time, manufacturing quality level, first-pass yield, and finally, price, are getting more and more important today. To meet these demands, RF components require ever-increasing levels of integration, culminating in the RF system-in-package (RF-SiP) platform. It is important, however, that regardless of the integration scheme, RF performance characteristics are not degraded. Additionally, with each level of integration comes a more complex thermal management scheme that involves the whole satellite sub-system and the microwave modules.

Driven by the requirements discussed above, and based on existing operator-less ghost-shift capability over night [4], TESAT's microwave assembly technology experts have the concept of "hi-rel production documentation." This capability is especially important in order to provide end users a detailed view inside applied manufacturing processes, especially if the product is already hermetically sealed and has been anonymously pre-produced (i.e., pre-produced independent from a customer purchase order, or a dedicated customer to stock). In this manner, the complete assembly line including epoxy dispense, pick and place, cure, plasma cleaning, wire-bonding, automatic optical inspection and electrical test, is setup and operated. For the epoxy dispense process, we had to consider how to introduce an adequate inline adhesive volume measurement and determined which data should be archived. The initial goal is to replace two of four quality inspector eyes. The medium- to long-term goal is to eliminate manual visual inspection completely.

Inline volumetric scan

The MRSI-175Ag epoxy dispensers already contain height sensing in order to control the clearance of the pump nozzle above the substrate (30µm); typically, the sensor is a triangulation sensor. The implementation of the right confocal height sensor has two major advantages vs. the triangulation type: 1) Height sensing can be performed very close to obstacles e.g., hybrid components, substrate stacks, or housing walls, where a triangulation sensor system fails; 2) The same confocal light sensor can be applied in dual use for high-speed inline volumetric scan of the adhesive pattern.

An inline volumetric scan can be performed either pattern by pattern, or at the end of the dispense process. We prefer the pattern by pattern approach where the applied adhesive pattern is scanned immediately after dispense at up to a 10 inches per second robot gantry speed. The dispense system uses measurement algorithm processes that gather sensor data and calculate applied adhesive volume in nanoliters. This volume is stored within a traceability data file.

A comparison of volume results has been performed among the MRSI software algorithm, volume extraction by a capability of the 3D visualization software, and an off-line topography laser measurement system providing a sub-micron height sensing resolution. Volume results are within a <3% variation (**Table 1**).

MRSI-175Ag software	20.8nl
3D visualization software	20.7nl
NanoScan laser system	21.2nl

Table 1: Adhesive volume result comparison.

Overall reduced process speed, including volumetric measurement, might occur as a drawback for the

moment (depending on application), but future sensors with increased sampling rates will improve this.

Pattern picture storage

The MRSI-175Ag Dispenser is equipped with two cameras (high and low magnification) in order to capture photographs of applied epoxy dispense pattern. The low magnification camera has a field of view (FOV) for pattern up to approximately a length of 4.5mm.

Traceability file data addresses the photograph of die/pattern N20 (which is GaAs-MMIC 2100700-116; as an example, see **Figure 1**).

A file name numbering scheme takes multi-picture patterns (patterns larger than a low magnification camera field of view), as well as product tray-schemes or multi-ups (several substrates or hybrids on one boat) into account. Stored pattern pictures can either be evaluated manually for low production volume, or be processed automatically using the vision tools of the applied automatic optical inspection system. Multi-colored LED light helps to achieve the right contrast for automated picture evaluation.

Traceability data file

Up to now, a traceability data file for an epoxy dispense process has often been neglected or was not even used in manufacturing. The new system provides a class of traceability file including the following production data: 1) Production order number; 2) Adhesive lot number; 3) Datamatrix product serial number; 4) Adhesive pattern volumes; 5) XYZ-cloud file names; and 6) Pattern picture file names.

Jet valve technology

Hi-reliability production documentation features as discussed above are very helpful for initial dispense process

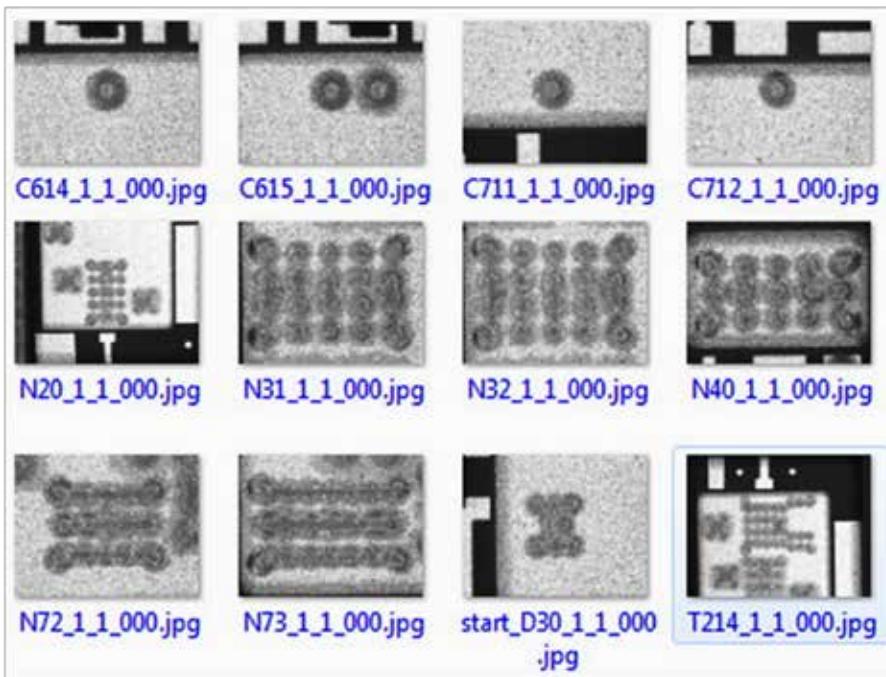


Figure 1: Picture documentation of adhesive pattern.

development in order to characterize various choices of valves that may be integrated, as well as their dispense results (**Figure 2**). Selectable choices are: 1) auger pump technology; 2) jet valve technology; and 3) precision time/pressure system. The choice of pump is dependent upon the application, including epoxy characteristics (viscosity, grain size, etc.), substrate flatness, dispense height (packaged walls verses flat substrates), desired speed, and volumetric control.

Adhesive volume tolerance

A drift of inline measured adhesive volume against set-point can be controlled by programmable tolerance limits (e.g., $\pm 10\%$).

Outlook for pick and place

Confocal height sensor and related software can also be installed on MRSI-705 pick and place machines as a feature. Detailed software capability will be developed in close cooperation with the TESAT hybrid group. Inline high speed height profiling of placed die can be performed in a similar fashion to epoxy dispense technology with respect to the following results:



Figure 2: Jet valve on MRSI-175Ag dispense machine at the left, auger pump at the right.

particles on top of the die, such as chip debris transferred from the die package by the pick tool. Chip-outs at die edges could also be identified. **Figure 3** depicts a 3D visualization of performed height profiling (same software as on MRSI-175Ag).

Summary

We have pushed ultra low-volume microwave epoxy dispense into a new performance class over the years [1-3]. Features such as high-speed inline

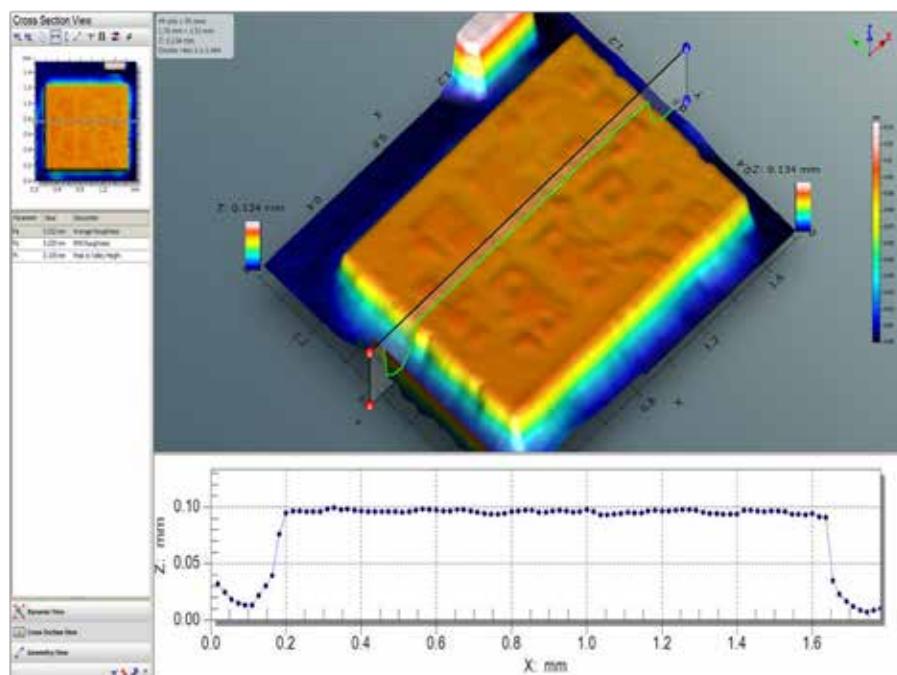


Figure 3: Height profile of placed die on MRSI-705.

volumetric scan provide a new level of process control and production documentation that supports high-reliability (hi-rel) operator-less manufacturing as required for medical, defense and space applications.

Acknowledgment

TESAT thanks MRSI Systems for its support in bringing the machine up to that level. Many thanks also to VERMES for providing the latest generation jet valve to TESAT for beta test.

Biographies

Willibald Konrath received his diploma degree in Microwave Engineering at the U. of Applied Sciences in Koblenz, Germany and is Head of the Microwave Factory at TESAT Spacecom GmbH & Co. KG; email: willibald.konrath@tesat.de

Klaus Scholl received his diploma degree in Physics at the Technical U. of Aachen, Germany and is Senior Expert on adhesives and qualification of materials at TESAT Spacecom GmbH & Co. KG.

Haiko Schmelcher is Senior Technician for epoxy dispense, pick and place, wire bonding and automatic optical inspection (AOI) at TESAT Spacecom GmbH & Co. KG.

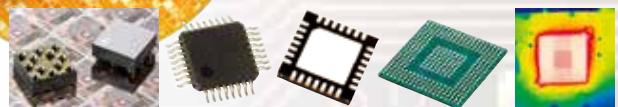
Ravi Balasubramanian received his Master's degree in Electrical Engineering from the Indian Institute of Technology, Chennai, India, and a Master's Degree in Bio-Medical Engineering from the U. of Connecticut. He is a Staff Software Engineer at MRSI Systems LLC.

Cyriac Devasia received his undergraduate degree in Mechanical Engineering from the Indian Institute of Technology, Bombay, a graduate degree in Mechanical/Systems Engineering from the U. of Toledo, Ohio, and a graduate degree in Business Administration from Boston U.; he is VP of Engineering at MRSI Systems LLC.

References

1. W. Konrath, K. Scholl, U. Müller, H. Schmelcher, "Ultra low-volume epoxy dispense technology for microwave hybrids used in fixed wireless access systems," Publication for MRSI in Billerica/USA, distribution at exhibitions.
2. W. Konrath, K. Scholl, U. Müller, H. Schmelcher; "Ultra low-volume epoxy dispensing," OnBoard Technology," Oct. 2005.
3. W. Konrath, B. Haeussermann, K. Scholl, H. Schmelcher, R. Schmitt, T. Weigle, "Highly reliable epoxy dispense technology for microwave hybrids suited for future space communication systems," Microwave Engineering Europe, Sep. 2009.
4. W. Konrath, "High-volume series production of microwave hybrid transceiver modules in man-less ghost-shift using LTCC-multilayer technology," German IMAPS Conf., Munich, October 2009.

Johnstech®



Wafer & Package Final Test



- **High Performance, Low Force Probe Array & Test Contactors**
- **Characterization, Production Floor, and Test Cell Integration Services**

Johnstech®

www.johnstech.com/connected

Find out more and win an iPad

PROFILE



Innovation for industry

Chip Scale Review staff interviews Laurent Malier, CEO of CEA-Leti



Laurent Malier, PhD

As Leti's CEO, Laurent Malier directs the activities of one of Europe's largest micro- and nanotechnologies research institutes, which employs more than 1,700 people and has a portfolio of 2,200 patents. He joined Leti in 2005 as vice president of strategy and programs and was named to the chief executive post in October 2006. Under his leadership, Leti has increased its technology transfers to industry, emphasized the institute's focus on creating startups and expanded international awareness of its offer through close collaborations with Caltech, IBM and several Japanese companies.

In 2013, Malier also became president of the Association of Carnot Institutes (AiCarnot), a network of 34 French research organizations working with companies, promoting innovation and developing technology transfers. He also is president of the steering committee of the Institute of Technology Research Technology (IRT) in Nanoelectronics, and a member of the steering committee of the Association for European Nanoelectronics Activities (AENEAS).

Malier graduated from Ecole Polytechnique and received his doctorate degree in solid-state physics in 1994.

About

Leti is an institute of CEA, a French research-and-technology organization with activities in energy, IT, healthcare, defense and security.



Minatec innovation campus – Grenoble, France

Leti is focused on creating value and innovation through technology transfer to its industrial partners. It specializes in nanotechnologies and their applications, from wireless devices and systems, to biology, healthcare and photonics. NEMS and MEMS are at the core of its activities. In addition to Leti's 1,700 employees, there are more than 250 students involved in research activities, which makes Leti a mainspring of innovation expertise. Leti's portfolio of 1,880 families of patents helps strengthen the competitiveness of its industrial partners.

CEA is a French government-funded technological research organization. A prominent player in the European Research Area, it is involved in setting up collaborative projects with many partners around the world.

Given the state of the semiconductor packaging industry - including all the technical and

financial challenges associated with R&D for advances - what are the top one or two issues the industry must tackle over the next 18-24 months and why? Do you have proposed solutions for these challenges?

Packaging roadmaps remain very close to those of silicon components; however, they must also account for the functionalization and diversification of electronic systems. The main technical challenges are related to miniaturization (interconnect density, 2.5D and 3D integration, eWLB, etc.), to integration density (thermal management, testability, reliability, etc.) and functionalization (bandwidth, operating frequency, isolation and electrical losses). Whether for monolithic integration or based on the assembly of different chips — the main evolution in 2.5D and 3D packaging — the fan-out eWLB package and TSVs do not solve all problems. Indeed, smart system integration and the emergence of new application areas have led to the emergence of new technical challenges, such as: 1) Packaging suitable for heat

dissipation of LEDs; 2) Optical coupling for photonic interposers; and 3) The use of GaN for power packaging.

Similarly, the economic challenges must take into account: 1) Lower costs; 2) The use of a flexible manufacturing chain; 3) Variable market sizes (high volume, niche market, etc.); and 4) Substrates of different sizes (200mm, 300mm) and varied types (silicon, glass, organic).

Monolithic 3D integration (3D IC), 2.5D and 3D interposers, and fan-out eWLB are gradually becoming industrialized. These methods are complementary; they can cover many applications and different types of markets. However, the reliability of these processes must be improved and we should be able to test the entire chip during the process without difficulty. Also, the manufacturing costs and time-to-market must be quickly known to be able to make choices. For now, there is no complete model and the standards are still inadequate.

■ How will CEA-Leti participate in addressing the issues you raised in question #1?

CEA-Leti mainly uses silicon for these packaging technologies. It develops technological processes in 3D integration (3D IC, 3D TSV), silicon interposers (2.5D), and also wafer-level packaging for MEMS. This broad domain of expertise allows us to use (and take advantage of) processes and compatible equipment throughout the entire chain of production of electronic components (or MEMS) and associated packaging. The Leti approach on interposers aims to develop — in the near future — commercial off-the-shelf concepts adapted to systems on silicon. It offers a complete line on 200mm and 300mm to meet the different needs of the market. For each new product, a cost study and market analysis is conducted directly with the industrial partner as soon as the packaging technology has been identified.

■ How do you see the packaging industry's roadmap playing out over the next 5 years? What are the major milestones? What steps is CEA-Leti taking to meet this next group of challenges?

For a long time, the evolution of the transistor size has allowed us to measure the evolution of electronic components. With the evolution of packaging towards 3D, we are now able to push the limits of integration even further, reduce the length of interconnects and limit electrical losses. While meeting specific criteria directly related to the application of this general trend, this evolution is expected to continue by:

- Increasing the functionality and the communication efficiency
- Providing faster and HD interconnect networks (photonics, fiber coupling)
- Power management and improving the thermal dissipation
- Providing more autonomy and energy efficiency
- Size reduction and controlling manufacturing costs.

The impact at the packaging level is great, and for many years we have continued to address these multiple developments. Some examples are:

- Electrical interconnects (high temperature, high density, Cu/Cu bonding, TSVs)
- Integration of optical function in silicon
- Electrical/optical coupling on-chip, integrated photonics on silicon
- Active interposers with tunable filter
- Thin-film packaging at the MEMS scale (integrated vacuum, optical, etc.)
- Optimization of interfaces and thermal interface material (TIM) to improve heat dissipation.

■ How is CEA-Leti's participation in standards activities and/or research consortia activities helping to meet the technology challenges that lie ahead in the next 2-5 years?

Leti participates in most networks involving the semiconductor packaging industry. Several Leti experts participate in working groups of the ITRS (assembly and packaging, MEMS, interconnects, etc.) and the iNEMI. In Europe, Leti is a member of several committees (Euripides, CATRENE, Eniac) and is active in numerous European projects.

■ What other comments would you like to share with the *Chip Scale Review* audience?

Leti has a unique packaging platform that can manage the entire value chain from design to final test. It has two back-end lines (200mm and 300mm) compatible with 3D integration and wafer-level packaging microsystems. Our ability to innovate in extremely diverse fields has enabled us to acquire a very wide range of expertise and be at the forefront of innovation.

Leti has defined different approaches in its manufacturing capabilities: 1) An R&D approach or innovative proof-of-concept in close collaboration with semiconductor manufacturers; 2) A prototyping approach where industrial end-user customers must rapidly assess the real benefits of technological solutions before production.

Contact Information

CEA-Leti
17 rue des Martyrs
38054 Grenoble cedex 9
France

Phone: +33 (0)4 38 78 44 00
E-mail: leti@cea.fr
www.leti.fr

INDUSTRY NEWS

3D TSV ICs: "We are ready!"

By Werner Schulz [[PLUS/VDI Nachrichten](#)], Yann Guillou [[SEMI](#)]

"**A**pplication ready" was an apt denomination of the second "European 3D TSV Summit" held January 20 to 22 on the Minatec Campus of CEA-Leti in Grenoble, France.



Conference amphitheater.

With 332 attendees, 24 presenters drawn from a valid cross section of leading companies in the field, three keynotes, two panel discussions, and 50 attendees taking the chance of visiting Leti's TSV cleanroom, the 2014 Summit was a clear success and a well-rounded repeat performance of last year's inauguration event. A total of 26 table-top exhibitors were accommodated - a few more wanting to participate had to be turned back for lack of space.



Busy show floor during a morning break.

Raj Pendse, VP and Chief Marketing Officer of STATS ChipPAC, made it a point to add a bit more of definition to the Summit agenda. "We are ready. But the application is not ready." A clear call to arms for system designers to adopt a



Raj Pendse, VP and CMO, STATS ChipPAC.

more forward looking position on using and implementing 3D TSV ICs in their upcoming projects.

In the near term, this year and next, "economic concerns may limit TSV ramping", Mark Stromberg of market research house Gartner stated in his market outlook. But he indicated that the unexpected stall would likely be resolved by the beginning of 2015. Another impediment is not likely to go away soon: high capital cost for equipping TSV lines for volume production - which "may limit the number of companies willing and able to implement this promising IC technology." But, Stromberg said, after moving beyond the 10nm node "TSV will become a required technology for system design."

A similar stance was taken by Eric Mounier of Yole Developpement in his outlook on "3D Packaging Market Trends and Applications." More specific: the middle end, Mounier predicts, will be a "strategic area", because it is "where foundries, OSATs and IDMs are going to compete." Mounier said "3D ICs will come in a great variety of forms and configurations." TSV/WLP processing already is a reality in camera image sensors. TSV for MEMS already is further along on the road to adoption on a large scale. And, last not least, TSVs are an important enabling technology for future photonic systems.

Speaking from a position of industry leadership in regard to its high-end FPGA

process for Xilinx, Mei Kei Ieong of TSMC Europe elevated 3D TSV to the new paradigm for high-density logic besides classical planar scaling guided by Moore's Law: "We are at the leading edge of system scaling." TSMC's CoWoS technology, he says, has the advantage of tightly integrating a multiplicity of chips. "Homogeneous CoWoS is now in production." Heterogeneous setups are at the demonstration stage. A test chip with Wide I/O-1 DRAM has been implemented, the memory interface reaching up to 380MHz. Daisy-chain HBM with six top die on full reticle has been realized as a test vehicle in 2013. For 2014, TSMC plans to tape out and validate a HBM function on CoWoS. "Ultimately we are moving to true 3D stacking with memory on top of logic." When? "This year or next."

"Enabling 2.5D Technology for Commercialization" was the topic of Michael Thiele's (GlobalFoundries) presentation. With a TSV line installed at the fab in Malta, New York, characterized for 20nm and 14nm next in line, and a bump and test facility under construction there, another volume bump and test facility (for SnAg C4 and Cu pillars) already in operation in Dresden, Germany, and a 300mm TSV line for interposer processing installed in Singapore. With these facilities, the company appears to be well positioned for 3D TSV – yet strictly focusing on the front side: "We have no plans at the moment for backside processing," Thiele said. "3D integration is a foundry process. We do via middle and will build the necessary capacity for two prospective customers."

Applied Materials was represented at the 2014 TSV Summit by Sesh Ramaswami of the Silicon Systems Group – with a rather optimistic and confident outlook on 3D TSV ICs: "We develop technology platforms to enable TSV and interposers in fan-out extensions for multi-chip integration and panels for lower cost."

The fundamental question, according to Ramaswami: "When, specifically with DRAMs, will HVM start delivering ROI to all the members in the supply chain?" Now that the major technology issues have been mostly resolved, Ramaswami said, "the attention is on defects, yields and reliability. This is indicative of a more stable ecosystem and application readiness."

"What is driving 3D Applications" was the timely question posed by Martin Henry of STMicroelectronics. The answer: imaging, as evidenced by a camera with 2.5D TSV wafer level components in production since 2008. Form factor is the key, he said, with a surface gain of 33 percent and a thickness gain of 50 percent since then. Electronics-to-photonics integration is next. This requires, as Henry stated, TSVs with high aspect ratios and large passive interposers with embedded thermo-mechanical stress sensors in an innovative assembly flow. Advanced logic integration with memory on application processor with via middle was demonstrated in 2012 on 65nm logic and recently on 28nm FDSOI with no impact on BEOL and yield.

Eric Beyne, Program Director 3D Systems Integration at Imec, Belgium, presented a detailed cost analysis of 2.5D and 3D system integration. "Wafer thinning, TSV and backside processing are unlike any other processing done before." Key challenge for volume application, Beyne said, is to understand the cost structure and the impact of the various process steps on total cost, and then reduce the cost of integration. Currently, the unfavorable cost situation is exacerbated by the fact that there is no high-volume manufacturing ongoing, which, over time, would involve a cost depression pattern. So the focus has to be on incremental cost improvements as achieved by incremental technology improvements in all areas.

A comparison of "2.1D" and 2.5D technologies – and their future market potentials – was provided by Ron Huemoeller of Amkor. "2.1D" works without interposer on a dual or highly integrated organic interposer, offering an RDL focus of 2 – 6 μ m, with 25 – 30 μ m pads and 10 – 20 μ m vias. In his view, both will have their own evolutionary paths and applications in consumer and mobile

devices, as well as in high-end graphics processing and servers. Special advantage of organic interposers, according to Huemoeller, is their embedding of passive components and the reduction of assembly steps, while enlarging interposer size.

"Orthogonal Scaling" was the overarching view and sweeping tour d'horizon outlining IBM's "future path for denser and more efficient systems" as presented by Thomas Brunschwiller from IBM Research in Zurich, Switzerland. Three developments, in IBM's view, will define the future of electronic circuits and systems: big data and cognitive computing, the end of classical scaling and materials with their unfavourable energy costs, leading to "orthogonal scaling," with high density provided by TSV connectivity, and circuit proximity provided by stacked memory structures ("hybrid memory cube"). Liquid cooling will enable true volumetric scaling and distributed power delivery, while Si-photonics will provide off-stack communications.

Finally, a brief review of the presentation given by Patrick Leduc of CEA-Leti, on "novel architectures for imaging and high-performance energy-efficient computing devices." Leduc: "We are in the Zettabyte (10^{21} bytes) era." In 2014 data center traffic will reach more than 4 Zettabytes, and the race for more operations per second is pointing towards the Exaflop age. Power supply and heat dissipation in data centers are touching their limits. This, says Leduc, calls for novel interconnect solutions in parallel multi-core computing architectures. They will require appropriate interposer technologies, in other words: active Si interposers with active and passive photonic components integrated in them.

Proceedings of the event are available and can be purchased online. A photo gallery is online. For any inquiries, contact Yann Guillou (yguillou@semi.org), European 3D TSV Summit event manager.



Sockets, Contactors & Adapters for Prototype Development & Test

- Compatible with virtually any footprint
- Probe-pin & Elastomer solutions
- Pitch range from 0.30mm to 2.54mm
- Pin counts up to 2000
- Bandwidth to 40GHz
- SMT, thru-hole & solderless options
- Several socket closure styles available
- Custom requirements are welcome
- Competitive pricing
- Expedited delivery

For further information visit www.e-tec.com

or contact us directly for immediate attention
E-Tec Interconnect Ltd, USA Marketing & Sales
E-mail: info-US@E-tec.com, Telephone: +1 408.746.2800




The only event
that encompasses
the diverse world
of integrated
systems packaging!



May 27-30, 2014

**The Walt Disney World
Swan & Dolphin Resort
Lake Buena Vista
Florida, USA**

For more
information, visit:
www.ectc.net

Don't miss out on the industry's premier event!

ECTC 2014

**The 64th Electronic Components
and Technology Conference**

**MORE THAN 300
TECHNICAL PAPERS COVERING:**

- 3D/TSV
- Advanced Packaging
- Modeling & Simulation
- Optoelectronics
- Interconnections
- Materials & Processing
- Applied Reliability
- Assembly & Manufacturing Technology
- Electronic Components & RF
- Emerging Technologies

Conference Sponsors:



HIGHLIGHTS

- 41 Technical Sessions including:
 - 5 Interactive Presentation Sessions, including one featuring student presenters
- 18 CEU-approved Professional Development Courses
- Technology Corner Exhibits, featuring more than 95 industry-leading vendors
- 5 Special Invited Sessions
- Several evening receptions
- Wednesday luncheon keynote speaker
 - Peter L. Bocko, CTO, Corning Glass Technologies
- Multiple opportunities for networking
- Great location

ADVERTISER INDEX

Amkor www.amkor.com	1, OBC
Amicra Microtechnologies GmbH www.amicra.com	37
CSC Pure Technologies www.cscptech.com	12
DL Technology www.dltechnology.com	31
ECTC www.ectc.net	64
Emulation Technology www.emulation.com	55
Essai www.essai.com	IFC
E-tec Interconnect www.e-tec.com	63
EV Group www.evgroup.com	49
GPD Global www.gpd-global.com	25
Hanmi Semiconductor www.hannismsemi.com	9
Honeywell www.honeywell-radio.com	7
Incal www.incal.com	10
Indium Corporation www.indium.us/E036	51
Ironwood Electronics www.ironwoodelectronics.com	11
JF Microtechnology www.jftech.com.my	17
Johnstech www.johnstech.com/connected	59
KYEC www.kyec.com	23
Kyzen www.kyzen.com	19
Leeno www.leeno.com	2
Loomis Industries www.loomisinc.com	4
Micro Control www.microcontrol.com	27
Nanium www.nanium.com	36
Nordson Asymtek www.nordsonasymtek.com/s2	47
Plasma Etch www.plasmaetch.com	34
Quik-Pak www.quikicpak.com	33
SEMI www.semirexpos.org	53
Sensata www.qinex.com	15
Smiths Connectors IDI www.idinet.com	IBC
SSP Inc www.sspinc.co.kr	8
Winway Technology www.winwayglobal.com	13

ADVERTISING SALES

USA West, USA-North Central

Kim Newman

P.O. Box 9522 San Jose, CA 95157-0522
T: 408.429.8585 F: 408.429.8605
ads@chipscalereview.com

USA-East, USA-South Central

Ron Molnar

13801 S. 32nd Place Phoenix, AZ 85044
T: 480.215.2654 F: 480.496.9451
rmolnar@chipscalereview.com

International

Lawrence Michaels

2259 Putter Court
Brentwood, CA 94513
T: 408.800.9243 F: 408.429.8605
lxm@chipscalereview.com

Korea

Young J. Baek

407 Jinyang Sangga, 120-3 Chungmuro 4 ga
Chung-ku, Seoul, Korea 100-863
T: +82.2.2273.4818
ymedia@chol.com



Introducing Our Advanced

QFN TEST SOLUTIONS

The leading provider of high performance test sockets has expanded its offering to include two new QFN testing solutions. Archimedes for peripheral test and the patented Celsius for tri-temp peripheral package test are both examples of what you have come to expect from Smiths Connectors | IDI, great value and leading edge technology. By combining proven scrubbing contact technology with our global manufacturing and distribution capabilities, testing QFN devices is now more affordable than ever.

Our renowned quality and reliability make Smiths Connectors | IDI your worldwide partner for the next generation of test solutions.

Phones & Tablets

Technology Leadership in
Copper Pillar, 3D and Wirebond Stacking



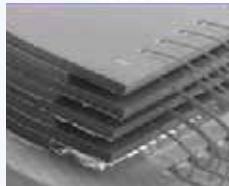
Keeping It Thin!

Enabling Technologies

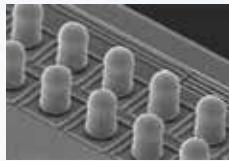


TMV® PoP or fcCSP
Application Processor
Baseband
Combo Chip
Memory
PMIC
RF

Stacked NAND



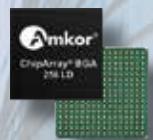
Copper Pillar



FC^MBGA
Graphic
Processor



WLCSP
PMIC
Audio Codec
Power Amplifier
Compass



CABGA/FBGA
PMIC
Audio Codec
Baseband
Camera Module
RF

Sensor Packages



Cavity MEMS



LGA



MLF®

Microphone, Pressure, Humidity/Temperature, Gyroscope,
Accelerometer, Fingerprint, Light, Infrared and Fusion Sensors



Visit Amkor Technology online for the most current product information and locations.

www.amkor.com