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The International Magazine for the Semiconductor Packaging Industry

Volume 17, Number 2

March - April 2013

Cover Feature

**From Unit Processes to Smart Process Flows –
New Integration Schemes for 2.5D Interposers**

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International Directory of IC Packaging Foundries

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- Fan-Out Wafer-Level Packaging
- Testing of Automotive Components
- Speeding 3D-IC to Commercialization
- Interposers: What's Different This Time Around?
- Market Forces Drive the Greening of Our Industry & Foster Innovation



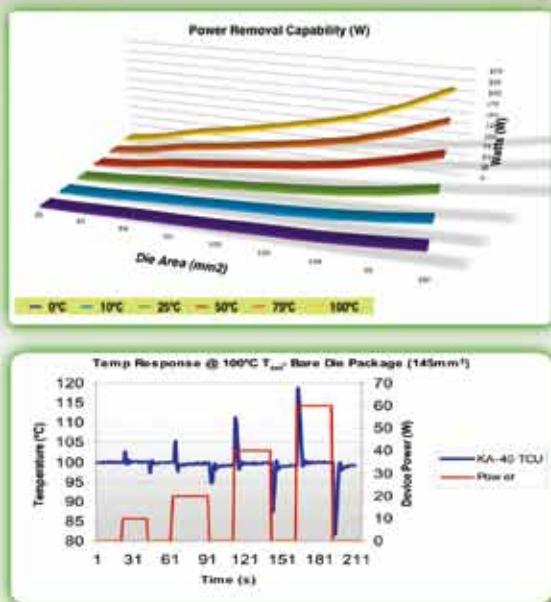
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Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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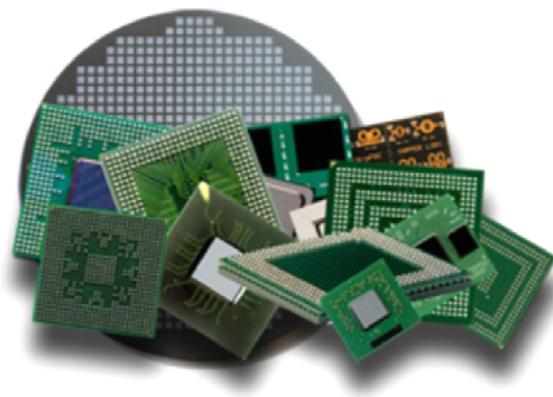
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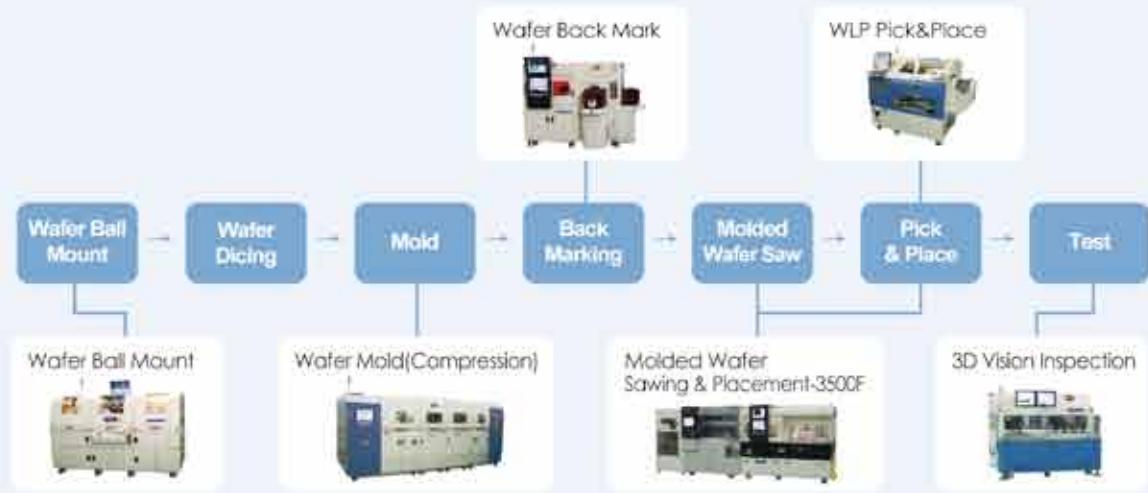
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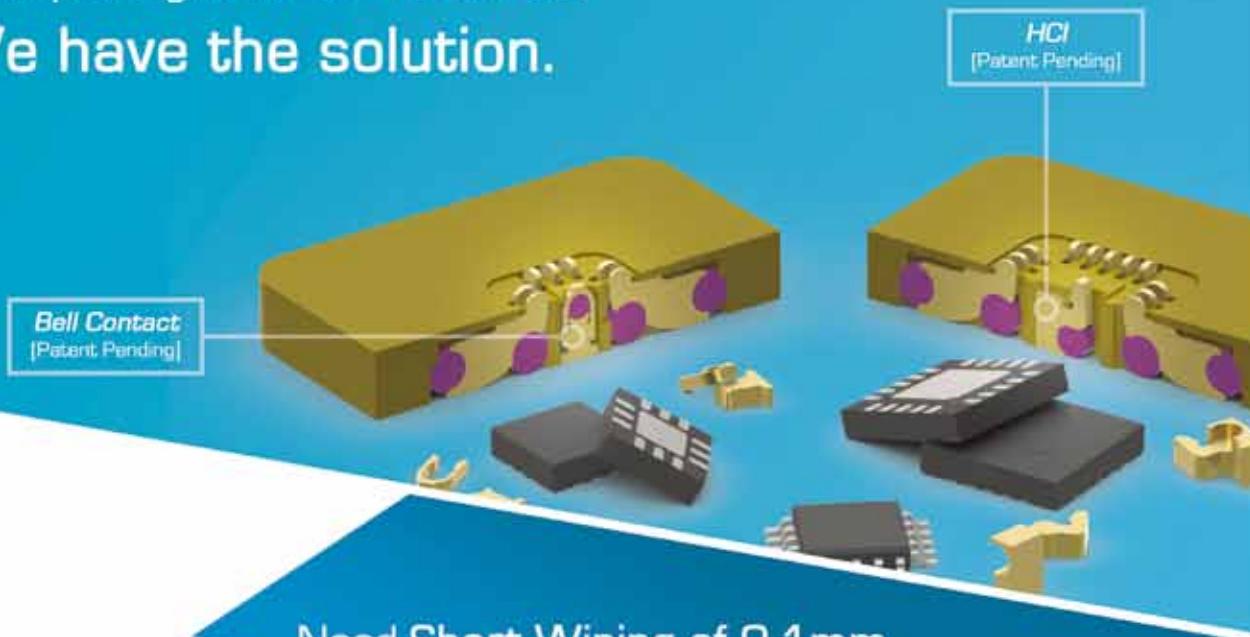




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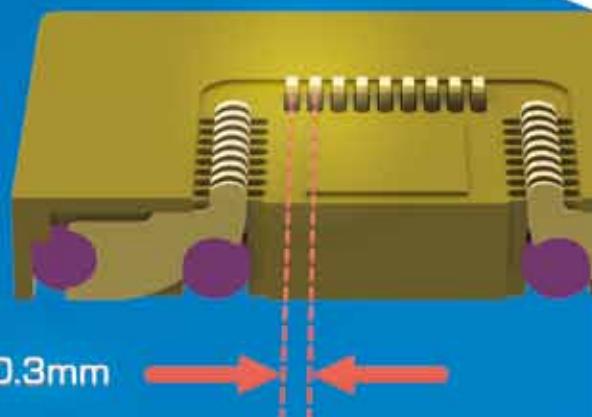
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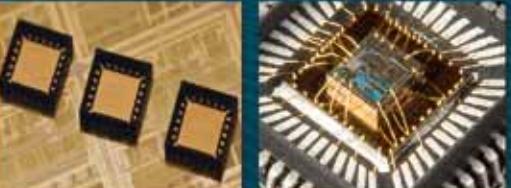


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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$100 per year to Canada or \$115 per year to other countries. In the U.S. subscriptions by first class mail are \$95 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January–February, March–April, May–June, July–August, September–October and November–December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

FROM THE PUBLISHER



OSATS: Executives' Perspectives

Today's OSATS (Outsourced Semiconductor Assembly and Test Services) leaders are capable of delivering innovative solutions to integrated device manufacturers in every segment of the supply chain.

These services include comprehensive support for package design, wafer bumping, probing, sorting, thinning, dicing, wire and flip-chip bonding, 3D/stacked packaging, package-in-package (PiP) and package-on package (PoP). In the following commentary, I wanted to offer recent viewpoints directly from the top management of the OSATS providers. The following executive comments are recently extracted from their respective quarterly and annual reports to their shareholders.

Ken Joyce, Amkor's President & CEO noted the following in his report: "Looking ahead to the first quarter 2013, we are seeing seasonal demand patterns and we are currently planning capital additions of around \$450 million for 2013 primarily to support the growth opportunities we see in mobile communications."

ASE Group Chairman and CEO Jason Chang noted in his company's report that "ASE's continued execution to expand operations and deliver growth resulted in setting a new record for the company in 2012 particularly as we embrace this era of mobile communications and optimize our business activities accordingly." Chang added, "The macroeconomic climate and the cyclic nature of our industry will always impact our bottom line, however, our global strategy – expanding regional capabilities, manufacturing capacity, and product portfolio – is proving the right long-term strategy for our ongoing success. Clearly, semiconductor is at the center of huge technology transitions worldwide."

Tan Lay Koon, President & CEO of STATS ChipPAC, commented in part, "Based on current visibility, we expect net revenues in the first quarter of 2013 to be decreased compared to the prior quarter as the revenue outlook for first quarter of 2013 is impacted by seasonality."

John Chia Sin Tet, Group Managing Director of Unisem (M) Berhad, commenting in the company's report said, "The operating environment remains challenging due to global economic uncertainties. We expect a soft first quarter due to continued inventory adjustments in the industry."

In this issue, we cover the top ten OSATS WLP assemblers, fan-out wafer-level packaging, new integration schemes for 2.5D interposers, as well as what's different this time around in a market outlook for interposers, and how the industry can leverage SEMI standards to speed 3D-IC to commercialization and finally, we round out the issue with articles that discuss the market forces that are driving the greening of our industry while fostering innovation and the testing of automotive components.

Once again, CSR delivers the pertinent and carefully crafted articles to provide our readers the foundation to maintain a solid understanding of current trends and technologies, whether in-house or outsourced.

Kim Newman

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Director of Operations



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MARKET TRENDS

Interposers: What's Different This Time Around?

By Linda C. Matthew [[TechSearch International, Inc.](#)]

Silicon interposers are a technology with a history of multiple incarnations over more than 20 years. Today, interposers with TSVs are considered an alternative to 3D IC structures where the die are stacked on top of each other using TSVs. Applications for interposers with TSVs include ASICs for networking applications and FPGAs. Some companies are also examining the potential for interposers with GPU/CPU and mobile computing. The drivers are mainly partitioning large die, integrating single chips into a module, reducing die size where substrate density is the constraint, and minimizing the stress on large die that are fabricated with extra-low-k (ELK) dielectrics. Most of today's interposers are silicon, but research is also underway on glass interposers. Some companies are even investigating the possibility of laminate substrates as interposers.

Old vs. New Interposers: A History Lesson

One question that sometimes arises is how today's silicon interposers differ from the thin-film on silicon (MCM-D) of the past. Through most of the 1990s, silicon substrate work was underway at various companies as part of the multi-chip module (MCM) movement. Thin-film-on-silicon MCM-D, where D stood for "deposited," was one substrate choice competing with laminate (MCM-L) and ceramic (MCM-C) substrates. The benefits of silicon would have combined to give a denser, higher-performance module than laminate substrates could. But ultimately, the technology did not penetrate the high-volume commercial market and lost the battle to conventional

FR-4 because of cost and logistics. The competing laminate substrates were less dense because of the rough topography of the FR-4, but had much lower cost. And from a logistics standpoint, the higher density of the silicon substrate could not be fully utilized because the large number of high lead-count die that it could support created a package that was extremely difficult to test and had low yields. A technology that could not find a large market in 1995 is generating a different response today because packaging and integration have evolved substantially.

Advantages of Silicon Interposers

The interposers in production today are silicon with redistribution layers on each side. Today, multiple chips are mounted side-by-side on the interposer, but future versions show the possibility of stacked die with TSVs mounted on the interposer. Most of today's interposers are passive structures, but the incorporation of passives has been demonstrated.

The advantages of 2.5D (die connected to silicon interposers with TSVs) result from the combination of the silicon material properties and multi-chip packaging. Advantages include: 1) High wiring density due to the very flat substrate; 2) Efficiency of wiring layers on each chip because the global wiring is on the interposer; 3) Efficiency of active area on each chip because there is no keep-out area for the TSV; 4) TCE matched to the silicon die; 5) Lower cost of active devices due to partitioning large die with improved performance; 6) Lower cost of active devices due to smaller flip-chip bump pitch; 7) Lower power requirements than equivalent single-chip packages due to multiple chips combined on one

substrate; 8) Possibility of integrating passives into the substrate; and 9) More efficient heat dissipation than a 3D stack using a thermal lid.

Silicon Interposer: Planned and in Production

Silicon interposers are used as LED sub-mounts, substrates with integrated passives for transceiver/receiver applications, substrates for multi-chip modules, and interposers with through-silicon vias will increasingly be used for 2.5D applications. Network system and server makers, including Cisco, Ericsson, Fujitsu, Huawei, IBM, and Juniper Networks, show silicon interposers on their product roadmaps.

Silicon interposers are used for RF modules, where they offer the benefit of integrated passives. NXP's spin-off, IPDiA, manufactures silicon interposers for RF modules and hundreds of millions of units have been produced. STMicroelectronics has internal production on thin-film-on-glass and thin-film-on-silicon and produces transceiver/receiver modules internally. STATS ChipPAC supplies silicon interposers with integrated passives for RF module applications; the company described some of its developments in silicon interposers using Cu pillar and AgSn micro bumps for silicon interposer applications [1]. Test chips with a 5mm x 5mm outline were fabricated with 10,000 micro bumps on a 40 or 50µm pitch.

IBM's work with silicon interposers dates back to the late 1980s. Recently, the company has developed multiple technologies for TSV applications, including a program to fabricate silicon interposers. IBM has evaluated the thermal cycling reliability of

low-volume solder joints for the configuration of a silicon chip on silicon interposer on organic substrate [2]. Results show that the significant CTE mismatch between the silicon and organic substrate causes large stresses in the low volume solder joints.

IBM supplies a silicon interposer with TSVs to Semtech Corporation for a mixed signal application. The module integrates a high-performance data converter with a DSP and includes deep trench capacitors in the interposer. The interposer enables mixed IC technologies and solves density, power, and bandwidth issues. Applications include receivers for fiber optic telecommunications, high-performance RF sampling and filtering, test equipment and instrumentation, and sub-array processing for phased array radar systems.

IBM has also described its work on a silicon interposer in an optical transceiver module [3]. This is the first demonstration of the Terabus optoelectronic (OE) module using a TSV silicon interposer for the dense 24 TX + 24 RX transceiver. The interposer enables integration of CMOS and optoelectronic devices. It supports four flip-chip devices: two optoelectronic arrays (VCSELs and photodiodes) and two CMOS ICs with receivers and laser drivers. IBM refers to the entire interposer sub-assembly as an Optochip.

Xilinx's Virtex-7 2000T Field Programmable Gate Array (FPGA) uses a silicon interposer with TSVs. Xilinx reports that the 2000T is the world's highest-capacity FPGA, using 6.8 billion transistors, 2 million logic cells, and the equivalent of 20 million ASIC gates for system integration, ASIC replacement, and ASIC prototyping and emulation. The key to the performance gains is the partitioning of an FPGA die into four "slices" that are mounted on a silicon interposer or what Xilinx calls its "Stacked Silicon Interconnect" technology. Using internal design

capability, Xilinx has been able to partition its die into slices that are smaller than a conventional large FPGA die. The slices are fabricated in 28nm silicon technology. TSMC fabricates the passive silicon interposer in 65nm node silicon technology. TSVs in the interposer have an aspect ratio of 10:1.

In March 2012, Altera and TSMC jointly announced the world's first heterogeneous 3D-IC test vehicle manufactured with TSMC's Chip-on-Wafer-on-Substrate (CoWoS™) process [4]. CoWoS is TSMC's entry into the contract assembly world, and uses chip-on-wafer bonding to assemble die to a silicon interposer. The interposer is then attached to the substrate to form the final component. By attaching the device silicon to the thick interposer before it finishes fabrication, the process avoids manufacturing-induced warping.

Suppliers

Silicon interposer research activities, prototype development, and shipments are taking place at a number of companies including ALLVIA, ASE, Dai Nippon Printing, Ibiden, IBM, IMT, IPDiA (formerly NXP), NEPES, Shinko Electric, Silex Microsystems, SPIL, STATS ChipPAC, Teledyne Dalsa, Tezzaron and its Novati subsidiary (formerly SVTC's Austin, Texas facility), TSMC, and UMC. **Figure 1** shows the chip-to-chip (C2C) assembly with Tezzaron's interposer on the bottom; the interposer was developed with IME in Singapore. While many companies have contemplated the design

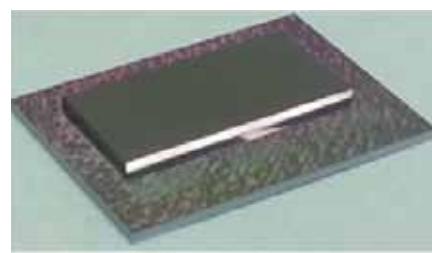


Figure 1: C2C with Tezzaron's interposer on the bottom. SOURCES: Tezzaron, IME

of structures with silicon interposers, the industry infrastructure and supply base for the widespread adoption of the technology has been a concern. The **Table 1** shows specifications of silicon interposers under evaluation. 

| Property | Value |
|---------------------------------------|----------------|
| Substrate length, width (mm) | 5.5 - 55 |
| Substrate thickness (μm) | 100 - 250, 400 |
| Via metal | Cu |
| RDL (number of layers) | 1 - 5 |
| Via diameter (μm) | 10 - 75 |
| Via pitch (μm) | 35 - 200 |

Table 1: Specifications of silicon interposers under evaluation. Source: TechSearch International, Inc.

References

1. S.W. Yoon, D. Shariff, J.H. Ku, P.C. Marimuthum, F. Carson, "3D TSV Interposer Technology with Cu/SnAg Microbump Interconnection," 6th International IMAPS Conference and Exhibition on Device Packaging, March 2010.
2. K. Sakuma, K. Sueoka, S. Kohara, K. Matsumoto, H. Noma, T. Aoki, et al., "IMC Bonding for 3D Interconnection," Electronic Components and Technology Conference, June 2010, pp. 864-871.
3. F. Doany, B. Lee, C. Schow, C. Tsang, C. Baks, Y. Kwark, et al., "Terabit/s-Class 24-Channel Bidirectional Optical Transceiver Module Based on TSV Si Carrier for Board-Level Interconnects," Electronic Components and Technology Conference, June 2010, pp. 58-65.
4. "Altera and TSMC Jointly Develop World's First 3D IC Heterogeneous Test Vehicle Using CoWoS™ Process," Altera Press Release, March 22, 2012.

Biography

Linda C. Matthew received her BS and MS degrees in materials science and engineering from MIT; she is a Senior Analyst at TechSearch International, Inc.; email tsi@techsearchinc.com

INDUSTRY NEWS

Imec and Qualcomm Extend R&D Collaboration

Imec and Qualcomm Technologies, Inc., a wholly owned subsidiary of Qualcomm Incorporated, announced an extended collaboration agreement to accelerate scaling technologies for logic and memory devices. The first fabless integrated circuit company to become a core partner of imec, Qualcomm Technologies will gain comprehensive insight into all advanced process technologies under investigation at imec to help shape future product roadmaps. By gaining early information on CMOS advancements, the product design community in IDMs, fabless, fab-lite and system-design companies can better anticipate the future impact and potential of new technologies to shape development efforts.

"We have collaborated with imec on the 3D stacking program for the last four years and we look forward to expanding our engagement with imec to include CMOS research and the new MRAM program," said Jim Thompson, EVP, Engineering at Qualcomm Technologies Inc. "Early engagement on new microelectronic technologies with imec enables Qualcomm to deepen the co-optimization of product architecture and technology while mitigating new technology risk in collaboration with our supply partners."

Leti Targets European Silicon Photonics Supply Chain

CEA-Leti has announced that it will coordinate a four-year project aimed at building a European-based supply chain in silicon photonics and speeding industrialization of the technology. The PLAT4M (Photonic Libraries And Technology for Manufacturing) project will focus on bringing the existing silicon photonics research platform to a level that enables seamless transition to industry, suitable for different application fields and levels of production volume.

PLAT4M, which is funded by a European Commission grant of 10.2 million euros, includes 15 leading European R&D institutes and CMOS companies, key industrial and research organizations in design and packaging, as well as end users in different application fields to build the complete supply chain.

"Silicon with its mature integration platform has brought electronic circuits to mass-market applications – our vision is that silicon photonics will follow this evolution," said Laurent Fulbert, Integrated Photonics Program Manager at CEA-Leti, coordinator of PLAT4M. "Upgrading existing platforms to become compatible with industrialization is now essential and this requires streamlining and stabilizing the design and process flows by taking into account design robustness, process variability and integration constraints. The PLAT4M partners bring a critical combination of expertise to the challenge of building a complete supply chain for commercializing silicon photonics in Europe."

According to CEA-Leti, a surge in output of silicon photonics research in recent years has significantly boosted the potential for commercial exploitation of the technology. However, most of this R&D has been devoted to developing elementary building blocks, rather than fabricating complete photonic integrated circuits that are needed to support large potential markets.

CEA-Leti further announced that the PLAT4M consortium will make technologies and tools mature by building a coherent design flow, demonstrating manufacturability of elementary devices and process integration and developing a packaging toolkit. The project will validate the complete supply chain through application-driven test vehicles representing various application fields, such as telecom and datacom, gas sensing and light detection and ranging

(LiDAR) and vibrometry. It also will focus on preparing the next-generation platform by setting up a roadmap for performance evolution and assessing scalability to high-volume production.

The supply chain will be based on technology platforms of Leti, imec and STMicroelectronics, supported by a unified design environment. The project is expected to have multiple benefits for the European photonic industry including:

- 1) Preparing the supply chain for silicon photonics technology, from chip-level technology to packaged circuits;
- 2) Making integration technologies accessible to a broad circle of users in a fabless model;
- 3) Contributing to the development of a design environment that facilitates photonics/electronics convergence;
- 4) Moving the emphasis from the component to the architecture, and thus concentrate efforts on new products or new functionalities rather than the technology level;
- 5) Aggregating competencies in photonics/electronics design and fabrication; and
- 6) Retaining the key added value in components in Europe through optoelectronic integration, with little added value in offshore assembly.

Among the members of the consortium, in addition to CEA-Leti, are: imec, the University of Paris-Sud, III-V Lab, TNO, Mentor Graphics, PhoeniX BV, Si2, STMicroelectronics, Tyndall-UCC, Aifotec, Polytec, Thales Research & Technology, and NXP.

Yole: BioMEMS Market to Almost Triple in Size Over Next 5 Years

Yole Développement released its latest market forecast for BioMEMS. According to the market analysis and research firm, the BioMEMS market is expected to grow rapidly, from \$1.9B in 2012 to \$6.6B in 2018 ([Figure 1](#)). This growth is almost a tripling in size, with mobile care applications contributing significantly.

Benjamin Roussel, Technology &

BioMEMS and microsystems for life science market (in \$M)

Including: pressure sensors, silicon microphones, accelerometers, gyroscopes, optical MEMS and image sensors, microfluidic chips, microdispensers for drug delivery, flow meters, infrared temperature sensors, emerging MEMS (RFID, strain sensors, energy harvesting)

(Source: BIOMEMS report, Yole Développement, February 2013)

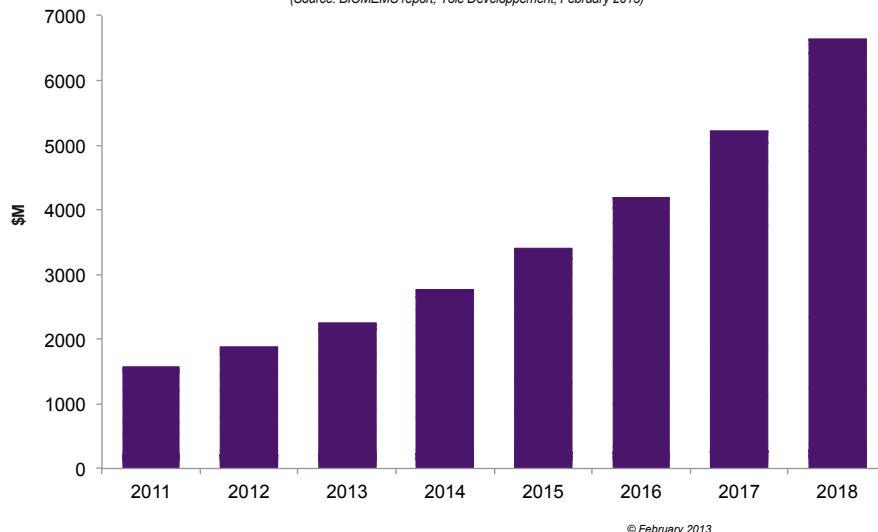


Figure 1: BioMEMS and Microsystems for Life Science Market (in \$M). SOURCE: Yole Développement.

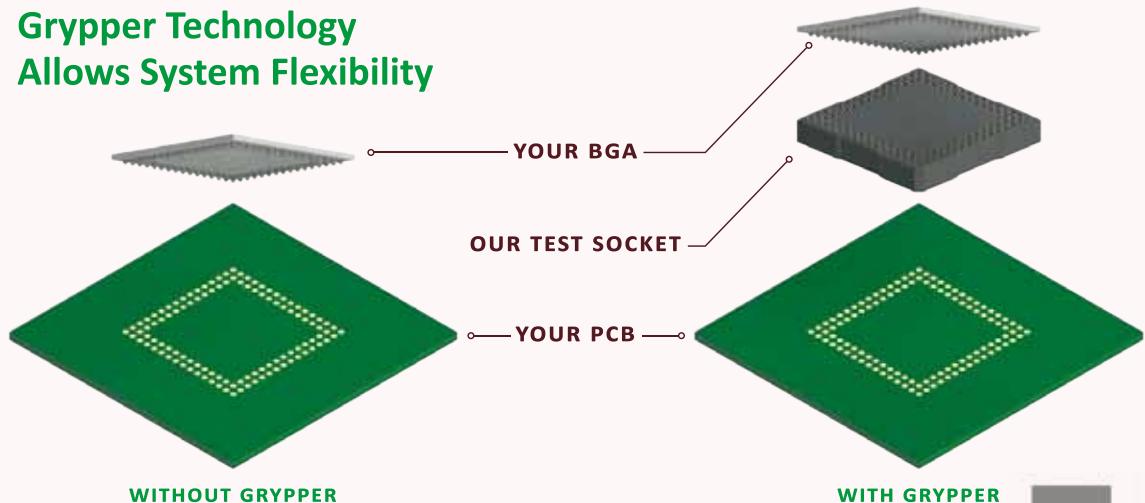
Market Analyst at Yole, also pointed out that microsystems integration is fast becoming a key added-value for system manufacturers.

Microsystem devices have become increasingly visible in the healthcare market by serving as solutions adapted to the requirements of various applications. The usefulness of these devices is two-fold: for one, they improve medical device performance for the patient; and secondly, they offer competitive advantages to system manufacturers. For example, the introduction of accelerometers in pacemakers has revolutionized the treatment of cardiac diseases.

In related news, Yole also released data crediting STMicroelectronics for capitalizing on the booming demand for MEMS in mobile devices by shipping 58% more MEMS units in 2012 to

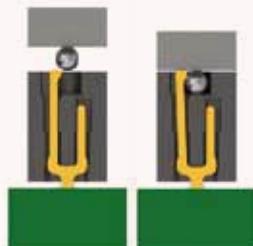
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|---|--|



2010-2012 MEMS revenue evolution for Top 3 MEMS companies

(February 2013, Yole Développement)

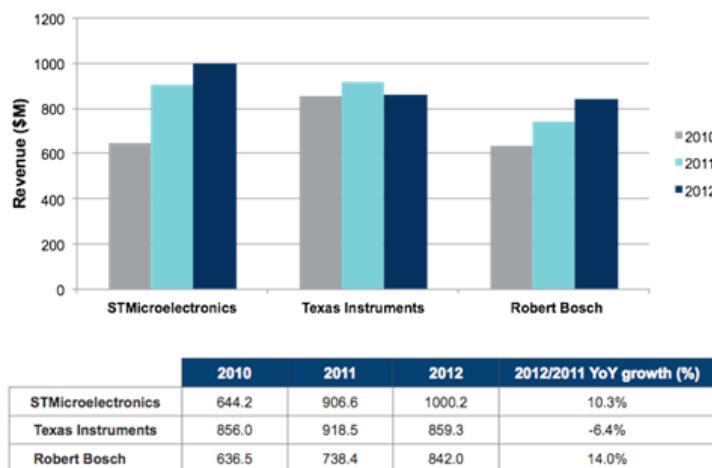


Figure 2: 2010-2012 MEMS Revenue Evolution for Top 3 MEMS Companies. SOURCE: Yole Développement

become the first company to reach \$1 billion in MEMS sales (Figure 2). That was in a year when the average prices of accelerometers and gyroscopes that are its core MEMS products dropped by 20%-30%, noted the research firm.

"The company [STMicroelectronics] was there and ready with its 8-inch fab when the volume demand started, as well as a large portfolio of products and low prices," said Laurent Robin, Activity Leader, Inertial MEMS Devices & Technologies at Yole Développement. "They could use a feed-the-fab-strategy to build volumes, and discounts for buyers of multiple devices, to meet the price demands of the cell phone makers."

A*STAR's IME's Latest Collaboration Leverages Packaging Capability

A*STAR's Institute of Microelectronics has signed an agreement to collaborate with Petroleum Geo-Services (OSE:PGS), a focused geophysical company headquartered in Oslo, Norway, to develop a high performance microelectromechanical systems (MEMS) based sensor for deep

sea seismic oil and gas exploration. The collaboration leverages IME's experience in designing high-performance MEMS sensors, MEMS process platforms and in-house packaging capabilities, and PGS's expertise in seismic exploration. The project will demonstrate a MEMS sensor and provide guidelines for the packaging and integration with ASIC in the next phase.

The MEMS sensor is targeted for

incorporation into a PGS commercial streamer system to acquire more precise seismic data during seismic surveys to locate and estimate the size of offshore oil and gas reserves.

ESCATEC Celebrates Ten Years of Operation at Its Heerbrugg Factory

ESCATEC is celebrating the tenth anniversary of the opening of its Heerbrugg facility (Figure 3) with a special event for customers. "The theme of our event is Building Bridges," explained Christophe Albin, Executive Chairman of the Board of Directors and founder of ESCATEC. "Heerbrugg's central European location in Switzerland enables ESCATEC to build bridges for rapid communication and support for our customers all over the EU. From Heerbrugg we provide contract product design services and manufacturing from prototypes to low volume, high mix assembly. We also act as a bridge to our factories in Asia that combine our Swiss quality and reliability standards with low labor costs for high-volume production."

Yole: Flip-Chip Market Reinvigorated by Cu Pillar and Micro-Bumping

Yole Développement projects that over the next five years, a 3x wafer



Figure 3: ESCATEC's Heerbrugg Factory.

growth is expected for the flip-chip platform, reaching 40M+ of 12" eq wspy by 2018. Despite its high 19% CAGR, flip-chip is not a new technology, noted the marketing consulting firm — having been first introduced by IBM over 30 years ago. Flip-chip is keeping up with the times and new bumping solutions are being developed to serve the most advanced technologies, like 3DIC and 2.5D.

Yole further observed that in 2012, bumping technologies accounted for 81% of the total installed capacity in the middle end area, representing 14M+ 12" eq wafers — and fab loading rates are high as well, especially for the Cu pillar platform (88%).

Yole also reported that in 2012, flip-chip was a \$20B market (making it the biggest market in the middle-end area), and the research firm expects it to continue growing at a 9% clip, ultimately reaching \$35B by 2018. Flip-chip capacity is expected to grow over the next five years to meet large demand from three main areas: 1) CMOS 28nm IC, including new applications like APE and BB; 2) The next-generation of DDR Memory; and 3) 3DIC/2.5D interposer using micro-bumping. Driven by these applications, Cu pillar is on its way to becoming the interconnect of choice for flip-chip.

Peter Chiang Joins IPC as VP of IPC China

IPC announced the appointment of Peter Chiang as its new Vice President of IPC China. He will also serve as IPC's chief representative for Taiwan. Within his role of VP of IPC China, Chiang will work in conjunction with IPC China President Phil Carmichael to lead the organization's China operations and staff. As chief representative for Taiwan, he will have responsibility for providing standards development activity support, raising awareness of IPC and its programs, making company visits and establishing relationships with prospective distributors in the region.

"Peter is an experienced business professional with more than two decades experience in sales and marketing, training, finance, and management and service to multi-national companies," says Phil Carmichael, president, IPC China. "His market analysis skills and proven performance record of stellar client service made him the ideal candidate to work with IPC China staff to build IPC's presence in China, increase Taiwanese OEM membership and assist IPC members in achieving their business goals."

Prior to IPC, Chiang held key positions at Lexmark Asia Pacific Corp., Silicon Graphics/CRAY RESEARCH, Wang Industrial Co. Ltd., and China Management System Corporation. He holds a Bachelor of Science degree in computer science from National Taipei Commercial College in Taiwan and is fluent in Mandarin, English and Taiwanese. He works from IPC's China headquarters office in Shanghai

Triton Micro Technologies to Develop Via-Fill Technology

Tokyo-based Asahi Glass Co., Ltd. (AGC) and nMode Solutions Inc. of Tucson, Arizona, have invested \$2.1 million to co-found a subsidiary business, called Triton Micro Technologies (www.tritonmicrotech.com), to develop via-fill technology for interposers, enabling next-generation semiconductor packaging solutions using ultra-thin glass. The new company, headquartered in Tucson with a manufacturing facility planned in California, will combine nMode's interposer technology for electrically connecting semiconductor devices with AGC's materials technology and micro-hole drilling techniques to produce 2.5-dimensional (2.5D) and three-dimensional (3D) through-glass-via (TGV) interposers needed for advanced semiconductor devices.

To achieve the next-generation in high-density semiconductor packaging, interposer technologies are needed

to form the high number of electrical connections between a silicon chip and a printed circuit board. Interposers allow high packaging integration in the smallest available form factors.

Triton Micro Technologies will manufacture ultra-thin glass interposers using a high-efficiency continuous process that lowers costs and helps to commercialize the widespread use of interposers. The company will draw upon nMode's intellectual property and AGC's proven carrier-glass technology and via-hole drilling methodologies to fabricate its interposers. Triton then will apply its proprietary technology to fill the high-aspect-ratio via holes with a copper paste that has the same coefficient of thermal expansion as glass. This reduces the potentially damaging effects of thermal stress during manufacturing and long-term use. Triton's process creates high-quality electrodes within the interposer to provide the electrical interface capable of accommodating advanced, high-density ICs.

Triton's interposers are compatible with wafers having diameters from 100mm to 300mm and thicknesses of 0.7mm and below. The company also can design and manufacture customized solutions for unique applications.

"The global semiconductor industry recognizes that silicon is approaching its performance limits as an interposer material, but the need remains to create smaller, more efficient packages for today's and tomorrow's high-performance ICs," said Tim Mobley, CEO at Triton. "Our technology allows us to achieve known-good-die testing at the highest levels of packaging integration, faster cycle times and the lowest cost per unit in the market."

Here We Come!

The premier international packaging, components, and microelectronics systems technology conference, the Electronic Components and Technology Conference (ECTC), will be upon us

shortly. The 63rd ECTC will be held at the Cosmopolitan of Las Vegas, Las Vegas, Nevada, USA from May 28 - May 31, 2013.

This year's conference will have about 40 technical sessions (oral presentations, interactive presentations, and student posters), 16 professional development courses, a panel discussion, a plenary session, a CPMT Seminar, and a technology corner for exhibitors. The line-up of sessions includes: Advanced Packaging, Electronic Components & RF, Emerging Technologies, Interconnections, Assembly & Manufacturing Technology, Materials & Processing, Modeling & Simulation, Optoelectronics, and Applied Reliability.

Much can be learned at this annual conference. Information on two of the topics covered at the conference is

presented below.

Through-Via Interconnection

The topic of through silicon vias (TSVs) incorporates both 2.5-D and 3-D technology. 3-D interconnection involves stacking ICs vertically, and routing each of the die to the substrate below by incorporating vias that go through the bulk silicon of the die beneath it to carry the electrical signal to the substrate below. In 2.5-D, chips are partitioned and placed side by side on an interposer with through-vias to a substrate below.

The identified potential markets for through-via technology have a combined unit potential of 39 billion units, which will expand to 60 billion units in 2016. The forecast for through-via technology is for this new technology to be less than 1% of the total available identified markets through 2016, but growing each year.

Fan-Out or Reconfigured WLP

Reconfigured or fan-out wafer-level packages were introduced in 2006. After devices are manufactured on a wafer, the devices are sawn and transferred on a carrier to another larger wafer that has gaps between die, which are filled with over mold material that also coats the back side of the devices for protection. This allows for a larger surface on which to extend a redistribution layer, thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a printed circuit board.

Units of fan-out WLPs are growing at a CAGR of 11.6% for the years 2011 through 2016. These packages are between 8 and 9% of the total WLP population output.



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From Unit Processes to Smart Process Flows – New Integration Schemes for 2.5D Interposers

By Thorsten Matthias, Markus Wimplinger, Paul Lindner [EV Group]

A hot topic in the packaging world right now is the 2.5D interposer. An interposer allows inter-chip communication between multiple chips with intra-chip interconnects, thereby enabling unmatched bandwidth, reduced power consumption, and very good heat spreading. Interposers also enable a modular design and manufacturing architecture by die partitioning. Finally, 2.5D interposers allow the implementation of a large part of the promise of 3D ICs without the need to make through-silicon vias (TSVs) into the chips.

While the technical attractiveness of interposers has been acknowledged by the industry, cost is still prohibitive for many applications. At the IEEE Global Interposer Technology (GIT) Workshop in November 2012, a cost target of 1cent/mm² for consumer electronic applications was discussed. Interposer dies are very large, which results in a large cut-off area. Assuming that 80% of the wafer can be used for manufacturing, the 1cent/mm² equates to \$543USD/wafer total cost-of-ownership, which is an ambitious target.

There are multiple approaches to reduce the cost of interposers. **Figure 1** shows the basic concept of an interposer with RDL (redistribution layer) and microbumps on one side, TSVs through the interposer, and C4 bumps on the other side. One cost reduction approach is to replace the single crystal silicon wafer by cheaper materials like glass or polycrystalline silicon. Another approach is to reduce manufacturing cost

by increasing substrate size: LCD size panels for glass and poly-Si, and 450mm wafers for single-crystalline silicon. Lithography is another important area. The established patterning technologies from laminates are probably not sufficient for many applications, whereas front end lithography with line/space dimensions of 1μm/1μm is probably not necessary for many applications. There is a trade-off between resolution and cost. At the GIT Workshop, several speakers opined that 3-4μm L/S might be the sweet spot enabling high performance interposers at a reasonable price.

Via manufacturing, however, is also a significant cost contributor. From the electrical performance point of view, 10x100 vias seem sufficient for many applications. However, via manufacturing costs are positively correlated with the via depth and the via aspect ratio. The cost for creating a 10x100 via is more than twice the cost for a 10x50 via, which again costs more than twice as much as a 10x25 via. So from the cost reduction point of view, it would make sense to reduce the interposer thickness. The problem is that reducing the interposer thickness magnifies the problems with die handling and assembly. In the remainder of the article we will discuss how thin interposer handling can be avoided by smart process integration.

Interposer Manufacturing Flows

Up until now, interposer manufacturing flows have been envisioned as follows: the interposer die, as well as the dies to be stacked on the interposer, are individually manufactured (front-and backside of the thin dies including bumps on both sides). In the end, the thin dies are stacked on the thin interposer. This process flow allows that both active dies, as well as the interposer, can be tested prior to stacking. More important, it fits

the established manufacturing supply chain, where foundries would produce the interposer wafer and OSATs would take care of chip stacking, assembly and packaging. While this process sequence intuitively seems an obvious choice, it creates many difficulties from the manufacturing point of view, as delineated below.

- a) Bow and warpage of the thin interposer is a serious issue. While thin-wafer processing is well established by the usage of a temporary carrier, there is no good solution for handling of thin dies, especially if bumps are already on both sides. Not only are the thin dies fragile, but the internal stress creates die bow and warpage, which magnifies the difficulties. A die, which is flat at room temperature, most likely will be bent at elevated temperature. Precision alignment and bonding are difficult under such circumstances.
- b) The dies are bonded to the interposer with microbumps and a thermo-compression bond process. For high-density TSV applications, a solder-less bonding approach like Cu-Cu bonding might be necessary. The thermo-compression bond process prefers elevated temperatures up to 350°C. But if C4 bumps are already on the other side of the interposer die, then the thermo-compression bond temperature has to be reduced in order not to melt the C4 bumps. This results in reduced bond contact quality and increased cycle time.
- c) Thermo-compression bonding requires quite high bond forces of several hundred Newtons per die. The C4 bumps on the bottom side



Figure 1: Schematic cross section of a 2.5D interposer: C4 bumps on the bottom side, microbumps on the top side of the interposer; multiple redistribution layers (RDL) on top and bottom side.

of the interposer are spherical, which means that they form point contacts to a planar surface, which would result in immediate deformation of the bumps.

A New Process Flow

Breaking with the goal of stacking completely processed thin dies allows the creation of easier, smarter and more elegant process flows. One potential process flow for 2.5D interposers (EVG patent pending) with C4 bumps on the frontside, microbumps on the backside, and multiple RDL layers, would be as follows (Figure 2 shows the entire process flow):

Manufacturing of Thin Interposer Wafer. The interposer wafer after frontside processing is temporarily bonded to a carrier wafer for thinning and backside processing (Figure 2). The recent advances in thin-wafer processing by temporary bonding and debonding have been reviewed in the literature [1]. Within this process flow, “frontside” of the interposer refers to the side with C4 bumps. These C4 bumps could be created prior to temporary bonding or at a later point in the manufacturing line (bump-last processes).

Chip-to-wafer Integration. Multiple chips are stacked onto the interposer next to each other. Note that one chip itself could be a 3D stack, e.g., a memory cube. The entire chip stacking happens while the thin interposer wafer is still bonded to the carrier wafer (Figure 3). This has the advantage that the carrier wafer compensates and absorbs all the internal stress and keeps the interposer wafer flat. In the case where the C4 bumps are already present on the frontside of the interposer, they are safely embedded in the adhesive. It is important that the adhesive is rigid at the bonding temperature.

The chip-to-wafer stacking can be performed as sequential or parallel chip stacking. The more chips to be bonded, the more advantageous is the parallel chip-to-wafer bonding, called advanced chip-to-wafer (AC2W) bonding (Figure 4). Typically, the bonding is performed in a dedicated bond chamber with thermo-

compression bonding, as the bow/warp of the thin dies usually prevents massive reflow processes.

One of the attractive ideas behind 2.5D interposers is the modular integration approach, where companies can combine their ASICs with off-the-shelf chips. However, as long as there are no standards for die thickness, it has to be assumed that the dies will have different thicknesses. This means that the bonding

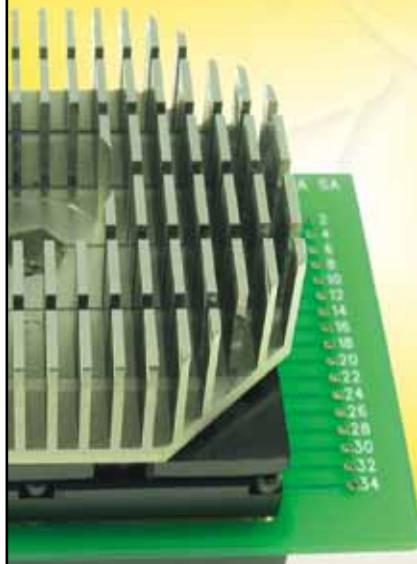
system has to be able to deal with such thickness variations.

Overmolding of dies on interposer (interposer still on carrier). After chip stacking, the entire wafer is overmolded while the thin interposer wafer is still bonded to the carrier wafer (Figure 5). This overmolding prior to debonding is the key integration concept. The overmolding compound creates a rigid film on top of the thin interposer wafer.

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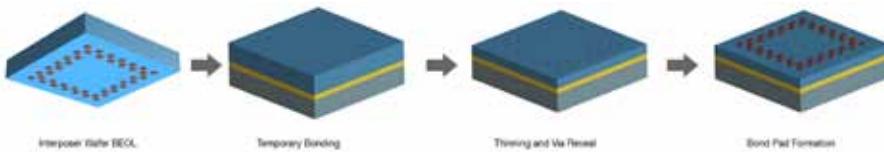


Figure 2: The interposer wafer is temporarily bonded to a carrier wafer for thinning, via reveal and bond pad formation.

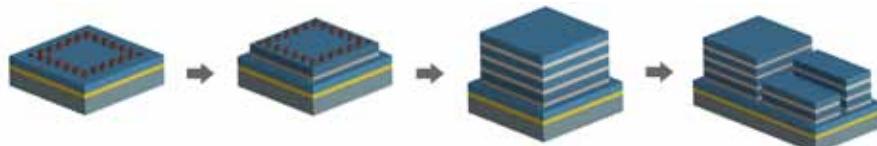


Figure 3: Chip-to-wafer stacking: The interposer wafer is still bonded to the carrier, which avoids any issues with bow/warp of the large interposer dies during thermo-compression bonding. Multiple chips can be stacked on top of each other. The individual chip stacks on the interposer can have different heights.

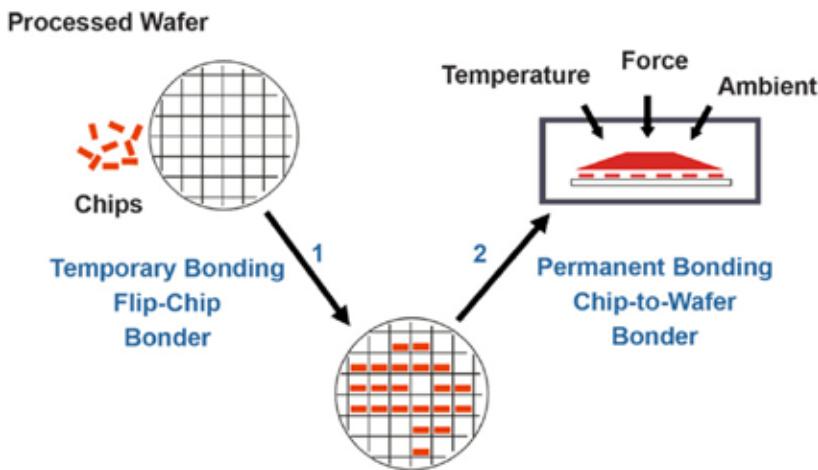


Figure 4: Process flow for the advanced chip-to-wafer (AC2W) bonding concept; The individual chips are temporarily bonded to the processed wafer using a volatile adhesive. The partially or fully populated wafer is then transferred to a bond chamber, where the permanent bond is established by applying force and temperature in an inert or reducing environment.

Polishing and thin film processing. The mold compound can be ground and polished. As a result, the entire stack of interposer+stacked dies+overmolding again resembles a standard round wafer with a flat, polished surface, which can be processed in standard wafer-level equipment. There is a lot of conceptual similarity to reconfigured wafers in fan-out wafer-level packaging (FO-WLP) from the manufacturing point of view

(e.g., heat spreader and heat sinks can be manufactured now).

Debonding. Finally, the thin interposer wafer is debonded from the carrier. However, because of this special process sequence, the thin interposer wafer is no longer fragile. Technically, overmolding in this process sequence is a kind of carrier swap technique. The mold compound acts as a rigid carrier after debonding – so it eliminates

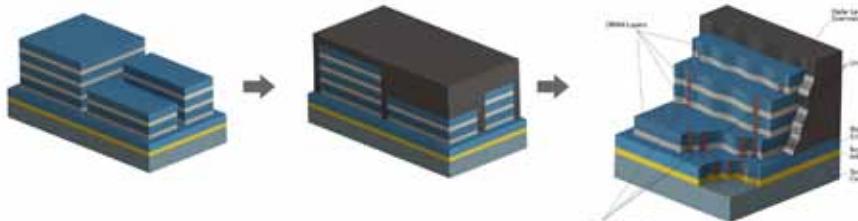


Figure 5: Left: After chip stacking, the entire wafer is overmolded while the thin interposer wafer is still bonded to the carrier wafer. Right: Cross section of the interposer after chip stacking and overmolding; in this example, a memory cube consisting of 4 DRAM dies is stacked on the interposer.

the need to deal with thin dies after debonding. Usually after debonding, a thin wafer is mounted on dicing tape on the film frame. But a thin wafer on a film frame cannot be processed with standard equipment. Typically, the next step would be dicing. However, within this process flow, the thin interposer is now “mounted” on the “mold compound wafer,” which means it is not necessary to use dicing tape. Additional thin film processing steps can be performed on the interposer frontside.

C4 bumps created on the interposer (“bump last” process flow). One highlight of this process flow is that the C4 bumps are created after debonding as one of the last process steps ([Figure 6](#)). As such, this process removes one of the most difficult manufacturing challenges from thin wafer processing – there is literally no bump damage at all, as bumps are created after debonding. Creating the C4 bumps in the end also has the advantage that it increases the process window for thin-wafer processing. Usually, the temperature during all backside process steps has to stay below the reflow temperature of the C4 bumps. However, if the bumps are produced after backside processing, then backside processing can be performed at higher temperature.

Interposer Thickness Control

There is one highly important aspect of creating the C4 bumps in the end – precise interposer thickness control. Usually the C4 bumps would have to be embedded in the temporary adhesive. Thick films are expensive and show poor thermal conductance, but most importantly, they have poor total thickness variation (TTV). It is of the

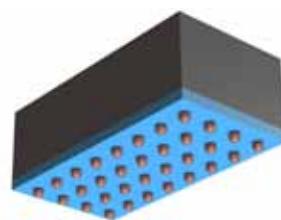


Figure 6: After debonding, the mold compound acts as a carrier wafer providing mechanical stability for wafer-level processing. This allows the creation of the C4 bumps at the very end of the process flow

highest importance that the interposer wafer has a uniform thickness after thinning. For via-first/via-middle integration schemes, the uniform thickness ensures a smooth TSV reveal process. Poor TTV of the thin interposer wafer would result in either grinding into the TSV or wafer areas that are too thick for the TSV reveal process. For via-last integration schemes, a poor TTV would increase the risk that the TSV does not electrically connect to the frontside metallization layers.

Backgrinding achieves co-planarity between the backside of the carrier wafer and the backside of the device wafer. The carrier wafer and the device wafer themselves should have a TTV of less than 1 μm each. The potentially largest contribution to thin-wafer TTV stems from the adhesive layer. The adhesive layer TTV is impacted by the adhesive properties, the adhesive film thickness and the coating, baking and bonding processes. The TTV contribution from coating and baking depends on the film thickness. **Table 1** shows the common thickness regimes for thin-wafer processing. The topography on the frontside of the device wafer, which needs to be embedded in the adhesive film, determines the thickness of the adhesive film. An 80 μm bump requires an adhesive film thickness of 100 μm . On the other hand, if the C4 bump is created in the end, a very thin adhesive film of 20 μm can be chosen.

Coating, especially of thick films, can result in center high or low spots, and in edge bead. The baking process can even increase the edge bead. There are multiple sophisticated technologies available to mitigate the TTV-like dynamic dispense, area dispense, multiple film coating and spray coating. The TTV contribution from the bonding process on the other hand is, within first order, not dependent on the adhesive film thickness and can even improve the TTV. On the EVG850TB temporary bonding system, we are using a setup with a rigid pressure plate, which allows planarization of the edge bead, as well as, center high spots. **Table 2** shows achieved TTV results today and the

| Topography | Interconnect | Application | Adhesive T |
|-------------------------|------------------------|--|----------------------|
| < 10 μm | Bonding Pads | Die to Die Various | 20 μm |
| ~30 to 40 μm | Microbumps, Cu-pillars | Die to Die Die to Interposer | 40-50 μm |
| ~80 to 90 μm | Bumps | Die to Substrate Interposer to Substrate | 90-100 μm |

Table 1: The topography on the frontside of the device wafer, which needs to be embedded in the adhesive film, determines the thickness of the adhesive film.

roadmap for 2013. It is important to note that TTV is very much dependent on the adhesive properties. The table shows the results achieved with selected adhesives.

| Bondline thickness | TTV Achievement 2012 | TTV Roadmap 2013 |
|--------------------|----------------------|------------------|
| 20 μm | 1 μm | 1 μm |
| 50 μm | 2 μm | 2 μm |
| 100 μm | 3 μm | 3 μm |

Table 2: Achieved results and roadmap for selected materials; TTV data are based on full wafer mapping with a 3mm edge exclusion zone.

Group; T.Matthias@EVGroup.com

Markus Wimplinger received his electrical engineering degree from HTL Braunau in Austria and is Director of Corporate Technology Development and IP at EV Group.

Paul Lindner received his electrical engineering degree from HTL Braunau in Austria and is Executive Technology Director at EV Group.

Summary

3D IC manufacturing is entering a new era. Today, the individual unit processes of TSV manufacturing and chip stacking are mature enough to allow smart process flows. In this article, a process flow for interposer was described that addresses improved interposer TTV, increased bump yield, and the ability to implement heat spreaders as a wafer-level process. A holistic manufacturing approach that includes the entire package has the potential to reduce the manufacturing complexity, while at the same time increasing yields and reducing costs.

Reference

1. T. Matthias et al., "The Material Breakthrough Towards Standardized Thin Wafer Processing," Chip Scale Review, Vol. 16, Nr. 2, March/April 2012.

Biographies

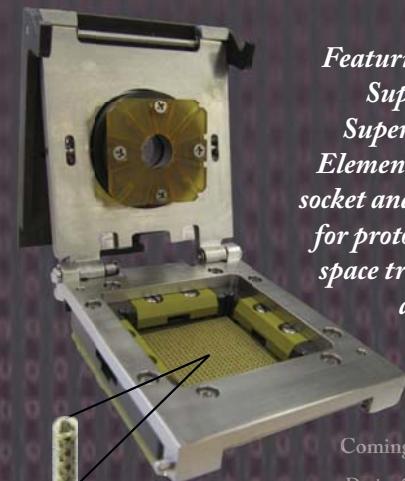
Thorsten Matthias received his doctorate from Vienna U. of Technology with a thesis in solid-state physics; he is Director of Business Development at EV



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Testing of Automotive Components

By Davide Appello [STMicroelectronics]

The automotive market demands a variety of components that are pervasively deployed in modern cars. Engine control, transmission, body, dashboard, passive and active safety, infotainment – all are examples of applications. Each of these application segments is characterized by a specific mission profile: the time for which the component is supposed to be operative during its lifecycle and the temperature conditions under which it is operated. Typical life durations are between 7 and 14 years, while operating temperature conditions are generally between -45°C and +150°C (ambient). The achievement of having very low defective parts in the field puts severe requirements on the testing flow. The tests must be accurate enough to screen all defects present at time-zero, but also capable of screening all those parts that may contain so-called early failures. Combining very high coverage tests with reliability-sensitive tests is the objective for the testing of automotive electronics components.

Test

As a regular practice, parts can be tested several times prior to shipment to the end user (see **Figure 1**). At wafer level, the main focus is usually to screen for gross defects and provide early feedback to the fab. Probe technology offers interesting capabilities to achieve high multisite testing, especially for digital products. This is possible thanks to design-for-test (DFT), which allows a limit on the number of contacted pads with respect to the whole pad interface of the device. Nonetheless, there are other limitations at probe test, for example, the achievement of high accuracy measurement of analog parameters. These limitations

are usually not present at package test where it is usually possible to obtain the maximum coverage. Similarly, multi-temperature testing is targeted at the package level.

Often full coverage testing is applied at final test and hence its duration could be a critical factor to manage. For example, microcontrollers usually need a very long test time because of the inherent requirements of flash intellectual property (IP). Unfortunately, at final test, more constraints limit the ability to achieve very high parallel test implementation. There are two main categories of limitations: electrical and mechanical. Electrical limitations are introduced by ATEs. For example, when testing power devices, ATE resource availability and device interface board complexity are the limiting factors. For other products such as microcontrollers, the main limiting factors are mechanical in nature: the physical space available for contactors is limited on device interface board (DIB), and large package sizes of 24x24 or more can constrain the maximum parallelism to a single digit. Much higher parallelism is currently applied at the burn-in stage, where other limitations are present.

Burn-In and Reliability Testing

Burn-in happens to be the most controversial test. It is usually intended

to screen for so-called early failures, and is achieved through the electrical stimulation of parts while they are heated. In this way, the high temperature simulates an acceleration of device aging, thereby anticipating failures of weak devices. The acceleration rules are related to the concept of activation energy as used in Arrhenius' laws [1,2], which describe the relation between temperatures, electrical fields and aging. Despite accelerating the aging process, the overall burn-in duration may last for several hours. This aspect is very critical in the setup of manufacturing flow, since it has a direct negative impact on cycle time and testing capacity allocation. Moreover, it also correlates with a high utilization of rapidly-degrading hardware such as the burn-in-boards (BIBs). BIBs are actually mounting sockets that hold devices and are loaded into thermal chambers (ovens) where thermal conditioning is applied. Extended burn-in cycles are not just aging parts under test, but are also deteriorating the BIB performance, which must be re-generated from time to time.

The cost sensitivity of the burn-in process is indirectly observable from several works present in literature [3,4]. The industry has tried to identify alternatives to it, while still preserving the final quality. To date, however, no effective methods have been found

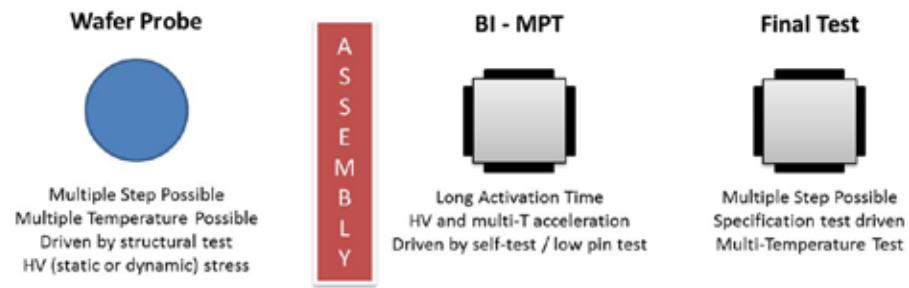


Figure 1: Test flow for automotive devices.

Semiconductor Assembly MATERIALS

to actually substitute for the burn-in concept. Nonetheless, several positive effects have been introduced by these efforts, which have resulted in improved product quality. Design for manufacturability concepts [5-7] for example, highlight methods and tools capable of protecting potentially weak structures and making them more robust. Electrical stress testing (high voltage, static or dynamic) combined with high-accuracy post-stress tests have shown reliability defect-screening capabilities. Finally, outlier detection through data mining of test results has also demonstrated screening capabilities. For example, part average testing (PAT) is an outlier detection methodology widely known and utilized in the industry [8].

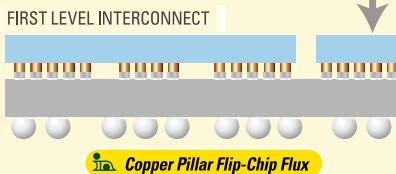
It is important to highlight two major trends associated with the burn-in process. These trends are pushing to achieve testing capabilities during burn-in so as to reduce the duration of FT on ATE, and/or, to implement additional tests to increase the quality of the testing process. The second initiative concerns data collection, which is used to optimize the entire process and enable reliability-learning. As a consequence, the burn-in equipment is likely to become a special kind of ATE. This kind of special ATE would necessarily feature a very low-cost per site and will very likely not allow exhaustive testing of all device characteristics. Additionally, it will have to match DFT and self-testing capabilities of products. To do this, the complexity of the logic interface must be realistically reduced, and must also take into account self-test features. At the same time, the requirements on power performance and reducing the power supply voltage are pushing the need for higher accuracy power supply units.

If one goal of burn-in is to provide screening for early failures (or extrinsic defects), it is also very relevant for monitoring the quality of intrinsic behavior – also referred to as quality excursion monitoring. With respect to such monitoring, there is a broad range of experimental implementation, which aims to assess the behavior of the fundamental parameters for the given device or technology. Several of these experiments exploit legacies and so-called “lessons-learned” cases. There are, however, few documents that aim to define procedures and criteria for reliability studies of automotive-grade products. A de-facto reference are the various AEC Q100 procedures [9], which are the most widely adopted methods for reliability assessment.

Test Program

As the reader may guess at this point, one key characteristic of the testing of automotive components is about the number of testing steps that a part undergoes from out of the fab to shipment (wafer sort, burn-in, final test). As a consequence, not infrequently, several test programs must be developed and optimized. Electronic design automation tools (EDA) have greatly helped to automate some fundamental parts of test programs like automatic test pattern generation (ATPG) to test logic, and built-in-self-test (BIST) engines to test memories [10]. In this way, a majority of functional testing has been removed from modern test programs while still achieving an

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improved screening of defects inserted during processing at the fab.

Unfortunately, EDA has not helped to achieve automated testing of analog IPs. Moreover, the multitude of ATEs available on the market are not sharing languages, tools and architectures, making test program development a highly customized activity. Re-use and structured test interfaces are, by default, the instruments allowing the reduction of the complexity of test, and possibly the next-generation ATE might be designed to directly exploit these properties [11,12].

Concurrently, standards have been developed to simplify the access (control and observation) to embedded IPs. As a consequence, this leads to a more generic identification of the testing requirements independently from IP characteristics [13].

Testing of Special Features

In recent years, automotive products have driven several innovations. Safety is now a pervasive requirement for

applications such as braking and airbags and is expanding into active safety applications for assisted driving and anti-collision mechanisms.

The stringent safety requirements imposed on automotive applications not only emphasize the demand for very high quality and reliable products, these requirements are actually adding new objectives for testing. In a nutshell, safety requirements [14] not only demand that hard defects are screened away, they actually require that "softer" defects do not manifest themselves at the margins and outside of normal operating conditions, thereby preventing a device from going into unsafe states. The direct consequence is the introduction of pseudo-functional tests, which on top of structural tests, ensure that complex failure modes are addressed and weak/marginal parts are screened out.

Besides innovations in safety, automotive applications are also driving demand for more secure devices.

Intellectual property protection, including software, is needed to allow multiple players in the application development supply chain to share platforms and combine respective potentials

From a testing view point, security features usually involve the full traceability of a single part. Additionally, security features are used to selectively enable or disable access to certain functionalities, depending on the life cycle. Once again, this has impact on the test program, which should recognize the specific configuration and verify the integrity of the device.

Automotive electronics applications are also pushing strongly to integrate newer and more powerful functionalities. There are at least two interesting trends that could become relevant drivers for testing. These are known good die (KGD) applications, whose main objectives are the small size and high-temperature capabilities. KGD will be the driver for the development of wafer-level reliability testing methods



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and tools. Another relevant segment concerns the RF applications for radar. Assisted driving and vision are pushing for ever greater sophisticated solutions requiring multi-gigahertz testing capabilities.

Summary

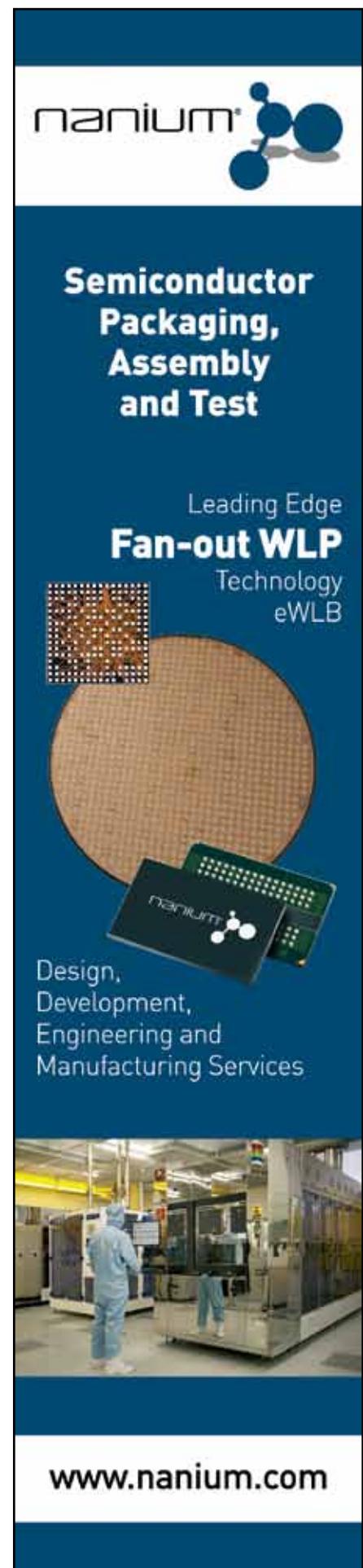
While both consumer and mobile semiconductor applications are pushing toward increased performance by adopting ever smaller pitch lithography, automotive products are often exploiting less advanced technology platforms. The test technology for automotive electronics, however, pushes the envelope much harder to new limits. The goals of achieving extremely high quality and screening out unreliable parts demands that high temperature and long testing times be used to effectively activate (expose) defects. Many of the concepts discussed above may become common requirements in the near future for a broader class of products, which makes testing for automotive products an interesting look-ahead experience. 

References

1. A. Birolini, "Reliability Engineering: Theory and Practice," Springer, 2010.
2. D. Appello, P. Bernardi, R. Cagliesi, M. Giancarlini, M. Grosso, "An Innovative and Low-Cost Industrial Flow for Reliability Characterization of SoCs," IEEE European Test Symp., 2008.
3. A. Nahar, R. Daasch, S. Subramaniam, "Burn-in Reduction Using Principal Component Analysis," IEEE Int'l. Test Conf., 2005.
4. O. Semenov, A. Vassighi, M. Sachdev, A. Keshavarzi, C.F. Hawkins, "Burn-In Temperature Projections for Deep Sub-Micron Technologies," IEEE Int'l. Test Conf., 2003.
5. K. Preston White, R. N. Athay, W. J. Trybula, "Applying DFM in the Semiconductor Industry," IEEE CPMT Int'l. Electronics Manufacturing Technology Symp., 1995.
6. D. James, "Design-for-Manufacturing Features in Nanometer Logic Processes – A Reverse Engineering Perspective," IEEE Custom Integrated Circuits Conf. (CICC), 2009.
7. S. S. Sabade, D. M. Walker, "Evaluation of Effectiveness of Median of Absolute Deviations Outlier Rejection-based IDDq Testing for Burn-in Reduction," Proc. of the 20th IEEE VLSI Test Symp., 2002.
8. P. Buxton, P. Tabor, "Outlier Detection for DPPM Reduction," IEEE Int'l. Test Conf., 2003.
9. <http://www.aecouncil.com/AECDocuments.html>
10. M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital Systems Testing & Testable Design," J. Wiley & Sons, New Jersey, 1990.
11. D. Appello, P. Bernardi, M. Bruno, R. Cagliesi, M. Giancarlini, M. Grosso, et al., "An Automatic Functional Stress Pattern Generation Technique Suitable for SoC Reliability Characterization," 2nd IEEE Int'l. Workshop on Automated Test Equipment: Vision ATE 2020, Santa Clara (CA), USA, October 30-31, 2008.
12. L. Ciganda, F. Abate, P. Bernardi, M. Bruno, M.S. Reorda, "An Enhanced FPGA-based Low-cost Tester Platform Exploiting Effective Test Data Compression for SoCs," 12th Int'l. Symp. on Design and Diagnostics of Electronic Circuits & Systems, 2009.
13. IEEE: <http://grouper.ieee.org/groups/1149/7/>
14. ISO 26262 http://www.iso.org/iso/catalogue_detail?csnumber=54591

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WLPs in an OSAT World; The Top Ten OSAT WLP Assemblers

By Sandra L. Winkler [New Venture Research]

Wafer-level packages (WLPs) are formed on the die while they are still on the uncut wafer. The process can be thought of as an extension of front-end manufacturing in that it involves the entire wafer, but is more similar to bumping for flip chip and tape automated bonding (TAB) operations, as benzocyclobutene (BCB) layers are involved. Being assembled in a batch process, WLPs are also low cost. The result is that the final packaged product is truly die sized, more so than "chip scale." Singulation of the device occurs after the device is fully packaged, unlike traditional forms of packaging.

Because of the low-cost nature of the WLPs, interest in this package solution is increasing the total percentage of WLPs of the total IC units from 4.9% in 2011 to 6.6% in 2016. This is from the total of all ICs, which includes bare die. Given the small size of the device, WLPs are ideal in handheld electronic devices such as cell phones, tablets, digital cameras, and more.

Devices that utilize WLPs as a package solution include: 1) DRAM, 2) SRAM, 3) Flash, 4) EEPROM/Other, 5) Standard Logic, 6) Sp Logic-Communications, 7) Sp Logic-Automotive, 8) Sp Logic-Other, 9) Analog-Amplifiers and Comparators, 10) Analog-Interface, 11) Analog-Regulators and References, 12) Analog-Data Converters, 13) Analog-Consumer, 14) Analog-Computer, 15) Analog-Communications, and 16) Analog-Industrial/Other.

Because WLPs are die sized, the package is limited to low I/O count devices, in which all the I/O can fit

underneath the package. This paradigm has been challenged by the introduction of the fan-out WLP, thus allowing these expanded WLPs to enter into the realm of higher I/O count devices.

Fan-Out WLPs

Reconfigured or fan-out wafer-level packages were introduced in 2006. After devices are manufactured on a wafer, the devices are sawn and transferred on a carrier to another larger wafer that has gaps between die, which are filled with overmold material that also coats the backside of the devices for protection. This allows for a larger surface on which to extend a redistribution layer (RDL), thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a printed circuit board. A small number of companies offer a reconfigured wafer-level package, while others assemble a licensed package.

Markets for WLPs

Products for WLPs include: cell phones, melody chips, sound chips, PDAs, tuner, watches, RF, automobiles, baseband processors, tablets, EMF filtering, ESD protection devices, and any electronic device.

WLP technology is sometimes used for discrete and passive semiconductors, which are smaller and can therefore take better advantage of the benefits of wafer-level packaging. Voltage regulators, which are in essentially all electronic products, are the largest market for WLPs, followed by amplifiers and comparators.

The Growth of WLPs for ICs and the Role of the OSATs

The worldwide market for WLPs used for IC units is growing at a compound annual growth rate (CAGR) of 13.9% through 2016. The OSAT (outsourced assembly and test) companies are gaining share—the CAGR for those companies is 15.4% for WLPs that house ICs.

The Outlook for Fan-Out WLPs

Units of fan-out WLPs are growing at a CAGR of 11.6% for the years 2011 through 2016. These packages are between 8 and 9% of the total WLP population output. Fan-out WLPs are utilized in package transceivers, baseband processors, RF and analog, power management, and analog and logic ASICs, including application processors, power amplifiers, and within multi-chip modules (MCMs) to create a radio-in-package (RiP) device. More applications will be found for these packages subsequently.

The OSATs That Assemble WLPs

A number of OSAT companies assemble WLPs, and fan-out WLPs. These companies in order of units, are listed below.

Amkor Technology. Amkor offers wafer-level chip-scale packaging (WLCSP) to form solder bumps on device I/O pads or to add a copper redistribution layer and route from I/O pads to solder bumps on JEDEC/EIAJ standard pitches.

The CSPn1 bump on repassivation (BoR) option provides a reliable, cost-effective, true chip-scale package on devices not requiring redistribution.

The BoR option utilizes a polyimide repassivation layer with excellent electrical/mechanical properties. A nickel-based or copper under bump metallurgy (UBM) is added, and solder bumps are then placed directly over die I/O pads. The technology used for CSPn1 results in robust packages that do not require underfill in their applications. CSPn1 is designed to utilize industry-standard surface mount assembly and reflow techniques.

The CSPn1 bump on redistribution (RDL) option adds a plated copper redistribution layer to route I/O pads to JEDEC/EIAJ standard pitches, avoiding the need to redesign legacy parts for CSP applications. Nickel-based or copper UBM is offered, along with polyimide or PBO repassivation. CSPn1 with RDL utilizes industry-standard surface mount assembly and reflow techniques, and does not require underfill.

CSPn3 utilizes one layer of copper for both redistribution and UBM. This simplified process flow reduces cost and cycle time. CSPn3 has been in production since 2009, and current output exceeds 500M units/year. This WLCSP option utilizes industry-standard surface mount assembly and reflow techniques, and does not require underfill.

Amkor provides wafer bumping, wafer-level test, back grind, dicing, and packaging in tape and reel to support a full turn-key WLCSP solution. In addition, Amkor is able to integrate its wafer bumping products into high-performance packaging options, such as flip-chip CSP (fcCSP) and system-in-package (SiP). The company has developed the capability to produce both single-die and multi-die wafer-level fan out (WLFO) packages, including 3D configurations.

FlipChip International, LLC. FlipChip International is the leading provider of merchant wafer-level packaging (WLP) and flip-chip bumping to the semiconductor market through its Phoenix, Arizona, facility, its joint venture in China, FCMS (Shanghai), and nine licensees globally.

Services provided include standard flip-chip (SFC, formally known as Flex-on-Cap™), redistributed SFC, Wafer UltraCSPTM, Spheron™ (high-frequency RF packaging), and EliteCSPTM (a low-cost electroless nickel-bumped WLP). FCI offers both sputtered and plated UBM alternatives, in the industry's broadest portfolio of bump technology options. FlipChip provides turnkey wafer-bumping services from engineering prototypes to high-volume manufacturing and is at the leading edge of emerging 3D and embedded die technologies.

NANIUM S.A. Licensing Infineon's eWLP and in a joint development with Infineon, NANIUM has extended this reconstituted technology to 300mm (12-inch) wafers. It has also extended the technology to create side-by-side and stacked SiP solutions. In a joint development with 3D Plus that is currently in prototypes and qualification samples, NANIUM is stacking the wafers for DDR3 DRAM applications [1].

This fan-out WLP currently has a single-layer RDL, with multiple RDLs and double-sided RDLs for PoP applications under development. The package thickness is 0.7mm, with a bump height of 0.25mm and a pitch of 0.5mm. Bump height of 0.1mm and a pitch of 0.2mm is in development [1].

STATS ChipPAC, Ltd. STATS ChipPAC offers both a fan-in and fan-out WLP. The company licenses the eWLB, which is a fan-out packaging approach with inherently lower stress, larger pad pitch, and redistribution layer (RDL), that allows higher integration and routing density in less metal layers in an fcBGA substrate. The fine line width and spacing capabilities of eWLB provides more flexibility in the package routing design and offers superior electrical performance, enabling the number of layers in the organic substrate of a standard fcBGA device to be reduced.

This package solution provides a versatile platform for the semiconductor




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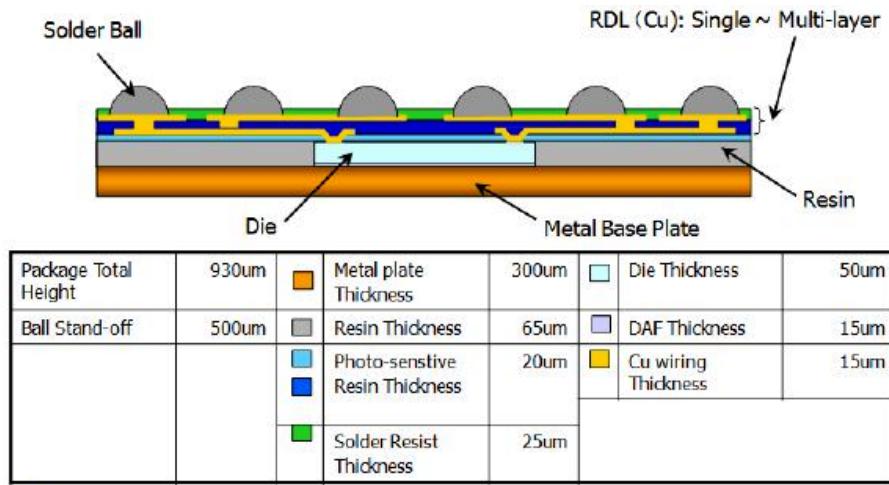


Figure 1: A wafer fan-out package. SOURCE: J-Devices Corporation

industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D system-in-package (SiP) configurations.

ASE, Inc. ASE, Inc.'s Advanced Wafer-Level Package (aWLP™) is a fan-out WLP that can be extended into 2D and 3D solutions. This package fans out the electrical traces over an overmold material that enlarges the package size beyond the size of the actual die. This differentiates the package from the company's acSP™, which is a WLP, but remains the same size as the size of the die. Applications for this package include Bluetooth, Wi-Fi, GPS, FM radio, analog devices, microcontrollers, integrated passives, EEPROM, power and voltage regulators, power amplifiers, and RF devices. End applications include cell phones, PDAs, and system boards.

Hana Micron. Hana Micron offers both a fan-in WLP, and fan-out WLP. The company offers wafer test and packaging process (wafer thinning, protection tape coating, wafer singulation and tape and reel.)

Siliconware Precision Industries Co., Ltd. (SPIL). A new high-performance fan-out wafer-level package (sWLP) was developed by SPIL, with an emphasis placed on the fabrication process and material selection. To overcome warpage challenges, a lamination process with dry film was employed to embed the die

and ensure that it adhered to the silicon wafer on the back side, thus achieving ultra-low warpage of 40 μm [2].

The lamination process with dry film reduces the bump pad stress, copper trace stress, and thus warpage. The maximum bump stress is located around the bump edge. The bump pitch to the PCB is 0.4mm, but is moving to 0.3mm pitch. The die has a lithography of 65nm, which is moving to 0.45nm [2]. The resulting package height is only 0.65mm, with 80 I/Os and a 5.5 \times 5.5mm package size. The sWLP is designed for mobile applications, with thinner die [2].

Unisem. Unisem offers a wafer-level CSP low cost solution that enables direct connectivity at the substrate or board level. To help provide this service the company is equipped with the latest state-of-the art Laser Mark, Laser Groove, Camtek, and Rudolph Wafer 2D/3D inspection stations and high speed Muhlbauer Die Sorter. The company also offers a full turnkey solution for wafer-level CSP from wafer bumping, packaging, test solution (probing) and full wafer map integration to handle die size from 0.2mm² to 36mm².

United Test and Assembly Center, Ltd. UTAC Group (UTAC Holdings and subsidiaries) offers a WLP in addition to other wafer-related services, such as providing redistribution layer (RDL) and bumping services.

J-Devices Corporation

The wafer fan-out package (WFOP) offered by J-Devices Corporation is processed on panels, not wafers, and is therefore very cost effective. The WFOP (see **Figure 1**) is a replacement packaging solution for flip-chip BGA. This simple structure offers low stress, and EMI shielding because of the grounded baseplate. The package offers a direct heat path from the backside of the package. Chip stacking is possible without TSVs when using this technology, and the WFOP can achieve similar electrical performance as a chip stack with TSVs. The package has a ball pitch of 40 μm in mass production, with 20 μm for the company's chip-on-chip.

Acknowledgment

More information on this topic and more can be found in New Venture Research's *Advanced IC Packaging Markets, Materials, and Technologies, 2012 Edition*; <http://www.newventureresearch.com/wp-content/uploads/2012/12/ap12bro.pdf>

References

1. J. Campos, "New Applications for Fan-Out Wafer-Level Packaging Technology," Presented at IW LPC, Santa Clara, California, October 5, 2011.
2. H. S. Hsu, D. Chang, K. Liu, N. Kao, M. Liao, S. Chiu, "Innovative Fan-Out Wafer-Level Package Using Lamination Process and Adhered Silicon Wafer on the Back Side," Presented at the Electronic Components Tech. Conf. (ECTC), San Diego, California, June 1, 2012.

Biography

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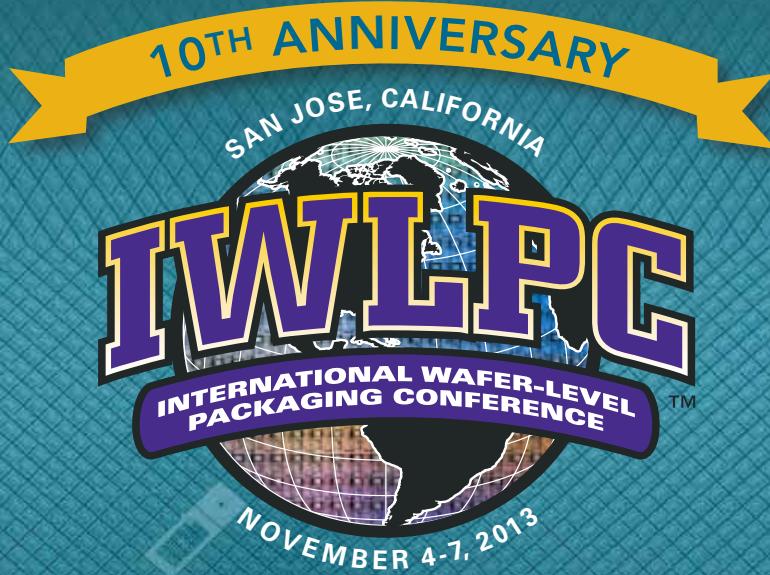
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Fan-Out Wafer-Level Packaging: Extending the Platform

By Eoin O'Toole [Nanium]

Fan-in wafer-level packaging, often known as wafer-level chip-scale packaging (WLCSP), usually involves creation of a redistribution layer (RDL) and ball grid array (BGA) on the surface of the original semiconductor die. This type of packaging has been gaining popularity for a number of years leveraged by electrical/thermal performance improvements and significant cost reduction when compared with laminate substrate-based packaging.

The RDL process is performed on standard front end semiconductor equipment allowing a large number of dies to be processed in parallel. As functionality built into the silicon die increases, the number of I/Os increases; at the same time, die area reduces for the same functionality because of technology node related die shrinkage. As a result, less die space is available to accommodate all of the I/Os on the die surface.

The solution to this dilemma was found with the development of fan-out wafer-level packaging (FOWLP). This technology involves spreading the useful surface of the die beyond the extent of the original front end die. The package extension is usually achieved by filling the necessary extra space with a highly filled epoxy mold compound; the repassivation dielectric, redistribution layer, and the solder mask dielectric – all extend to the surface of the mold compound providing the space required to form a BGA with similar pitch and ball pad opening to that of a standard FBGA package. The thermal and electrical performance of fan-out packaging has been compared favorably with VQFN, TSLP FCFBGA, and WLCSP.

Based upon a typical fan-out high-level process flow for a fan-out process, this article will provide an overview of contemporary wafer-level fan-out technologies including a comparison of the technology used for each of the crucial process steps.

This comparison is not meant to be exhaustive, but will provide a meaningful insight to the world of fan-out wafer-level processes. A number of other innovative and interesting solutions based on silicon/glass interposer technology are not included due to limitations of space and timeline.

At Nanium, the fan-out wafer-level technology is the embedded wafer level ball grid array (eWLB). In addition to the fan-out wafer-level

technology overview, the need for an extension to the eWLB technology platform in the form of double-layer redistribution for enhanced application adaptability and matching to the next front end technology nodes will be discussed. Details of the technology development enabling the double-layer redistribution process with process and reliability assessment we did will also be presented.

Technology Comparison

The bare bones process flow of most wafer-level fan-out technologies is shown in **Figure 1** and a technology comparison overview is provided in **Table 1**. Detailed discussion is provided below.

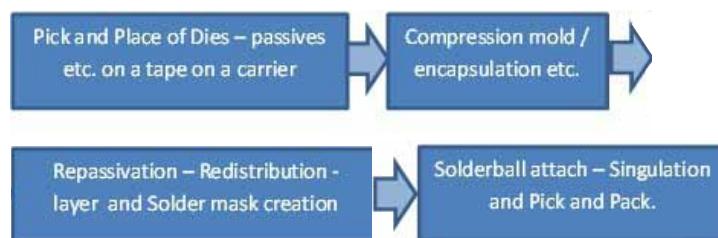


Figure 1: Bare-bones fan-out process flow.

| Nomenclature | Institute / Company-Technology Owner | Mold | Dielectric | Patterning | Copper thk | Comments | Refs |
|--------------|---|------------------------------|-------------------------------|----------------------------------|---------------------------------|----------------------------|-----------------------|
| eWLB | Infineon Technologies-Intel Mobile Communications | Compression | WPR or Polyimide or PBO | Photolithography | 5-10um | First Wafer Level Fanout | Ref 1 |
| RCP | Freescale | Film Encapsulation | Not specified | Photolithography | Not specified | | Ref 2 |
| WLFO | Amkor | Compression | ajinomoto build up film (ABF) | Photolithography | 3-20um | | Ref 3 |
| PWLB | ADL Engineering | Not specified | Not specified | Photolithography | Not specified | | |
| WFOP | J-Devices Corporation | No Mold | Unspecified Resin | Photolithography | Not specified | RDL on metal plate support | Ref 4 |
| M-Series | DECA Technologies | Encapsulant Film/Compression | Dry Film | Laser Ablation/ Photolithography | Not specified | | |
| SWLP | Siliconware Precision Industries Co. Ltd/Spil | None-lamination | Not specified | Photolithography | Not specified | no mold, silicon support | Ref 5 |
| EMWLP | Institute of Microelectronics-Singapore | Transfer Molding | Dry Film | Photolithography | Copper pillars 20-200um | | Ref 6 |
| SIWLP | Renesas Electronics | Powder Compression | Polyimide | Photolithography | Not specified Copper pillars | RDL first process | Ref 7 |

Table 1: Comparison of some of the main fan-out wafer-level technologies.

Pick and Place Process. Performed on high-accuracy pick and place equipment onto some type of bonding film – either temporary – to be subsequently removed, typically by thermal release, or to be used as the re-passivation first dielectric layer.

Mold/Encapsulation Process. This process encompasses either compression mold-based on either liquid mold compound, or powder mold compound. The use of alternatives such as encapsulant films/transfer molding is becoming more widespread. Renesas' SiWLP RDL first process uses a flip-chip die bond onto the RDL structure and overmold/underfill of the dies.

Dielectric Materials. A variety of different dielectrics, including low-temperature cure epoxy dielectrics, low-temperature polyimides, PolyBenzOxazole-based dielectric, and customized dielectrics, are available depending upon the requirements of the final application. All of the main fan-out technologies shown in Table 1 can

now boast reliability results rivaling traditional lead frame and laminate substrate packages.

Dielectric Patterning. Patterning of the dielectric material is not clearly specified in all cases but is expected to be performed by photolithography in all but the Amkor WLFO technology, where it is performed using UV laser ablation. DECA Technologies uses both laser ablation and its Adaptive Patterning process.

Copper RDL Thickness. The copper thickness used in the different technologies varies significantly, but most are in the 3-20 μm range. Technologically, there is no apparent strict limitation to values provided, some development, however, may be required.

In absolute terms, it is difficult to give an overall rating of the different technologies. Front end die dimension, pad pitch, TV opening, and packaging requirements in terms of electrical/thermal performance, reliability performance, process cycle time from

silicon delivery to shipment, assembly yield, and of course cost, must all be considered.

Market Share Comparison

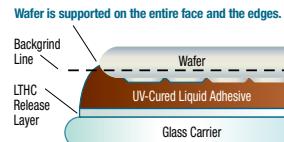
The fan-out wafer-level market is currently dominated by the applications based on eWLB technology mainly due to Infineon Technologies' driving of the technology (**Figure 2**). The vast majority of the eWLB packages in high volume have been cost and yield optimized, and are consequently based on a relatively relaxed set of design rules. Typically, they have one layer of copper redistribution layer based on a 20 μm line minimum width and spacing, and solder ball pitch from 400-500 μm for enhanced reliability.

One of the well-known challenges of eWLB fan-out wafer-level packaging is related to die shift. Unlike a normal silicon wafer, in a reconstituted wafer (after overmold), the individual die position will depend on a number of dependent and independent variables

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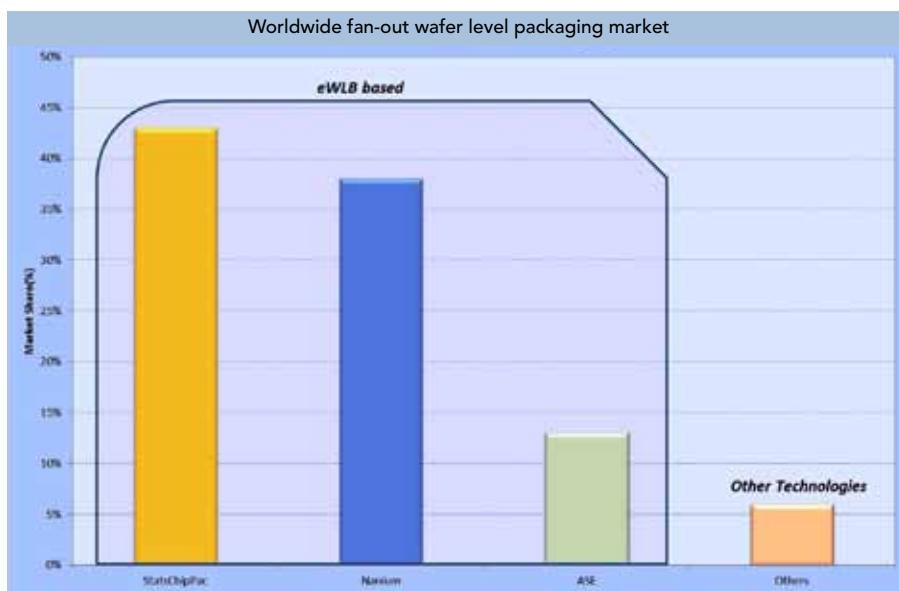


Figure 2: Worldwide fan-out wafer-level packaging market.

from coefficients of thermal expansion, temperature variations within equipments, chemical shrinkage of the epoxy mold compound and die slippage due to mold filling related to the fan-out process. It is possible through a combination of theoretical modeling and empirical fast feedback to establish and control a tight specification on die shift, however some tolerance is always required to guarantee correct pattern overlay in the redistribution layer process.

With technology-related shrink (**Figure 3**), bond pad pitch and TV opening is decreasing rapidly, more functionality is being included in the front end die and the number of I/Os is rapidly increasing per mm².

The most cost effective and yield optimized design no longer has sufficient space to allow for contact and redistribution trace routing; where necessary, the flexibility provided by two redistribution layers is required. Also where required, a double-layer RDL allows routing to the ball pads even with the tightest pad pitch and TV opening. A double redistribution layer allows for the incorporation of a ground plane and facilitates the incorporation of passive devices created in the redistribution layer.

In an effort to assess the processability, reliability, as well as to have an indication of volume yield performance when transitioning from single- to multiple-

layer RDL, a design of experiments (DoE) was performed to simulate the conditions expected to be applied in a productive double-layer RDL design. The DoE was performed on silicon die with a passivation layer/single AlCuSi pad metallization with an oxide nitride passivation. The pad pitch was 80µm and the TV opening was 60µm. An overview of the experiment is displayed in **Table 2**.

Different combinations of the dimensions listed below were verified as an effort to assess the best processability in the production line and resulting reliability:

a) Opening in the first dielectric layer

(DW1) of 20µm is typical for a robust eWLB design for a front end die with a TV opening of 50µm and a pad pitch of ~60µm allowing for a die shift + dielectric opening overlay tolerance of +/-15µm.

b) Land pad in the first redistribution layer (RD1): A land pad of dimension equal to the dielectric opening +/-10µm is needed to guarantee 100% to the dielectric opening.

c) Opening in the second dielectric layer (DW2), either greater or smaller than the RD1 land pad dimension: In order to guarantee a maximized contact area between the land pad in the first redistribution layer and the via in the second dielectric window to the second redistribution layer (RD2), it may be necessary to use an opening in the second dielectric layer superior to the first redistribution layer land pad dimension.

d) Where possible, an offset in the alignment from the via in the first dielectric layer to the via in the second dielectric layer is expected to give an improved reliability performance.

There is one standard variant that is often included in eWLB packages we design, but which was not possible to include in this assessment because of limitations of the silicon test die used. This variant is the condition of the first dielectric opening greater than the chip pad TV opening. The silicon test die had too small a chip pad pitch to allow for a

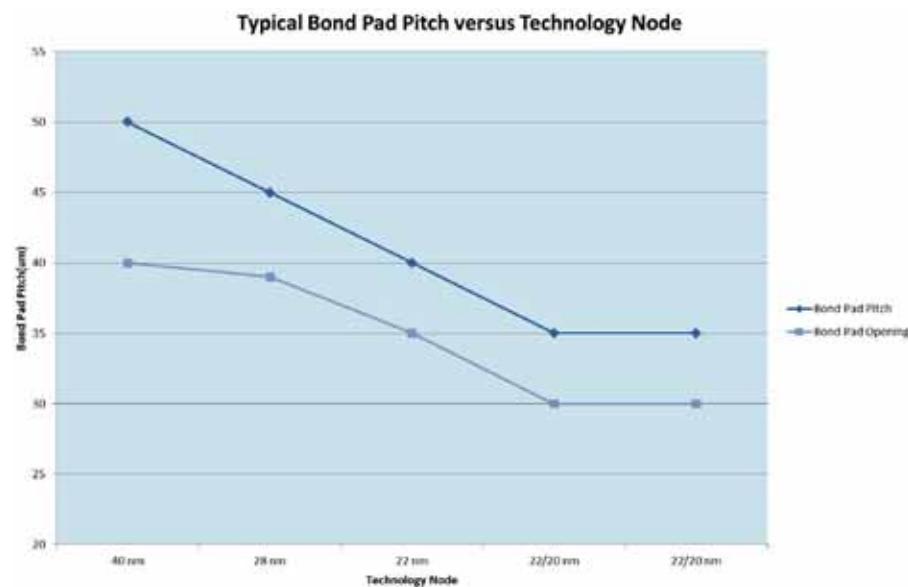


Figure 3: Bond pad pitch by technology node.

condition of dielectric layer 1 via > TV opening. This condition is particularly

popular for packages that have made the transition from flip-chip, where a small

TV opening and large pad pitch are common, thereby allowing a seamless transition without modification to the front end's dies' structure. The resulting design was enhanced to maximize the number of interlayer transitions to more effectively evaluate the reliability of the package; examples are shown in Figures 4 and 5.

| RUN | Via1 | | Via2 | | Via Alignment (X/Y) |
|-----|------|-----|------|-----|------------------------|
| | DW1 | RD1 | DW2 | RD2 | |
| A | 20 | 40 | 20 | 50 | 0 |
| B | 20 | 40 | 20 | 50 | 75/75 |
| C | 20 | 40 | 70 | 110 | 75/75 |
| D | 20 | 40 | 70 | 110 | 0 |
| E | 30 | 50 | 20 | 50 | 75/75 |
| F | 30 | 50 | 20 | 50 | 0 |
| G | 30 | 50 | 70 | 110 | 0 |
| H | 30 | 50 | 70 | 110 | 75/75 |

Table 2 : Via 1 and Via 2 dimensions (all dimensions are in μm).



Figure 4 : Design features - design A (see Table 2).

Results

The first output of the experiment was the alignment of the silicon dies with the subsequent dielectric and redistribution layers. This output was assessed by inspection using a brightfield optical microscope.

Aluminum Pad to DW1 Alignment + RD1 to DW1 alignment (Via 1). Examples of aluminum pad to DW1 opening to RD1 landing can be seen in Figure 6. A sample inspection on 8 positions – from the center to the edge of several 300mm wafers – was performed. Since this is the same as a single redistribution layer design and

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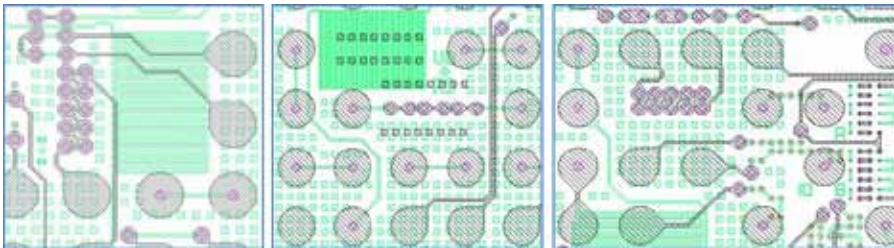


Figure 5 : Design features: design H (see Table 2).

within the advanced design rules we provide, the result was not surprising. A 100% yield for aluminum pad to DW1 opening and RD1 landing to DW1 opening was achieved.

RD1 to DW2 Alignment + RD2 to DW2 alignment (Via 2). One of the limitations of the double redistribution structure in eWLB is the lack of the option of 100% automated optical inspection. This is because of the small variations in alignment between the respective layers. Examples of the alignment achieved RD2 to DW2 to RD1 for each of the individual configurations are as follows: In sample inspection, 8 positions (on each wafer) – from the center to the edge of several 300mm wafers – resulted in a 100% yield for the contact RD2 to DW2 to RD1. Examples of several of the via chain structures from RD2 to RD1 to the aluminum pad are shown in **Figure 7**.

The second output of the experiment was the quality of the electrical contact achieved at each of the metal to metal interfaces. The quality was assessed by using a 4-point measurement of the via contact resistance. The results are as follows:

a) Via 1 Al (chip pad) to RDL1: The contact resistance of a 20 μ m via and of a 30 μ m via was measured (shown in **Figure 8a**); and b) Via 2 RDL1 to RDL2 (copper to copper) (shown in **Figure 8b**). The contact resistance of a 20 μ m via and of a 30 μ m via was measured; a small amount of dispersion was observed within the wafers. All values are well within our internal specification.

Another concern for a double redistribution layer is leakage current from the first to the second redistribution layer; the measurement of this leakage was the third output of the experiment. The leakage current was measured

between an RDL1 meander and an RDL2 ball pad. In a standard leakage current measurement, all of the values



Figure 6: Images from sample inspection.

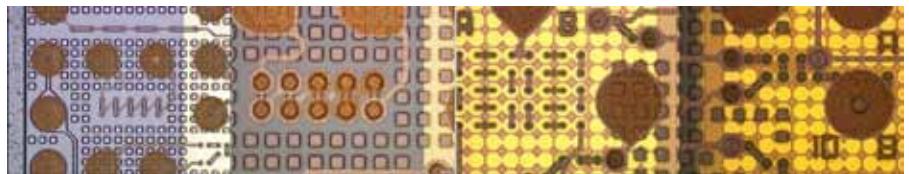


Figure 7: RD1 to RD2 via chain based on configurations A, H, D and G.

were well below the specification limit.

Reliability Testing and Results

A wide range of reliability testing was performed (**Table 3**) on a loose component level, including unbiased highly-accelerated stress testing, high-temperature storage testing, preconditioning under moisture

sensitivity level 1 conditions, followed by thermal cycling; second level, assembled on board testing (including on board thermal cycling and drop testing) was also performed. The readouts used in the reliability assessment of the tests include online electrical continuity testing for many of the tests, scanning acoustic microscopy (SAM) to verify the package integrity, and finally, mechanical cross section with ion mill polishing for physical failure analysis.



All reliability testing was performed in our in-house fully accredited laboratory. All of the reliability results available to date show the robustness of the package and the corresponding process.

Summary

The need for fan-out wafer-level packaging is becoming increasingly

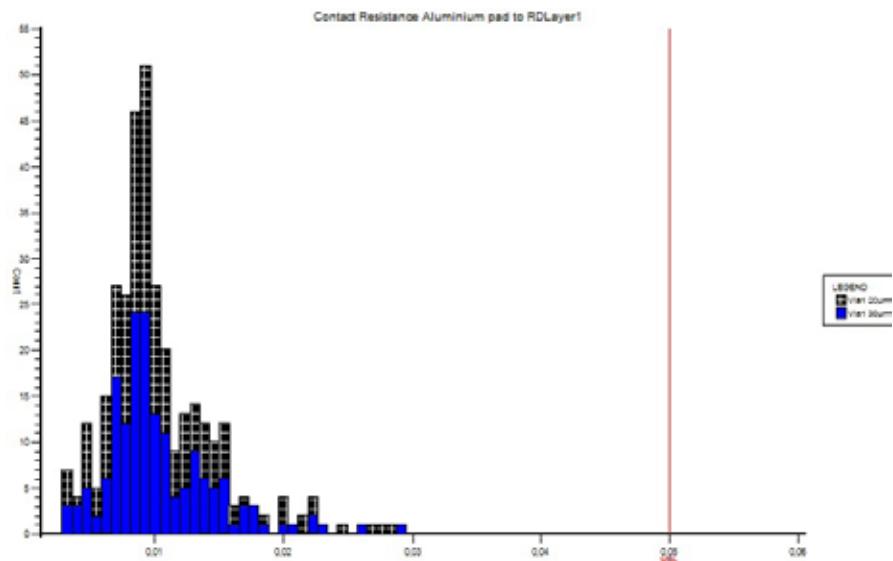


Figure 8a: Contact resistance results for a) Via 1 Al to RDL1.

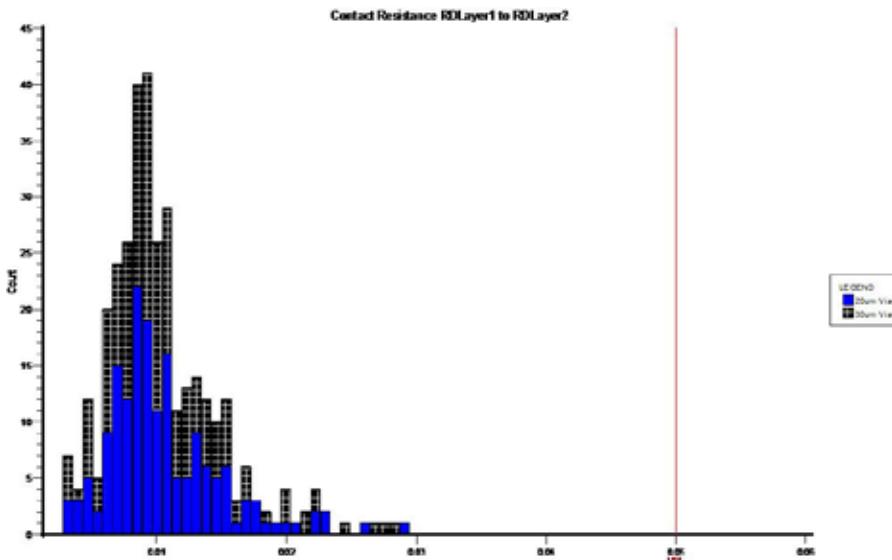


Figure 8b: Contact resistance results for b) Via 2 RDL1 to RDL2.

apparent in a wide range of applications. The choice of available fan-out technologies that offer flexibility, depending upon individual application needs, is also growing. To further extend the adaptability of eWLB, and to guarantee continuity for subsequent technology nodes, it is necessary to provide the option of multiple redistribution layers. The development of a multiple redistribution layer process in 300mm fan-out wafer-level packaging has been described and several conclusions may be drawn:

- 1) When required, we can successfully produce 2 layer RDL in 300mm eWLB;
- 2) Small differences in the reliability performance and cross section appearance give preference to conditions B and E, however none of the conditions were completely excluded if necessary;
- 3) A double layer redistribution layer structure is preferably avoided because of cost, yield, and complexity, not least of which is the incapability to perform a 100% automated optical inspection; and
- 4) No significant yield detractors were observed, however, final yield

| Reliability Test | Standard/Spec | Pass Criteria | Final Assessment (Pass/Fail) |
|-------------------------------------|--|-------------------------|------------------------------|
| Moisture Sensitivity Level (MSL) | EIA/J-STD-0200(Level1) | MSL 1 | Pass |
| High Temperature Storage (HTS) | JESD22-A103 (Cond. C: Ta:175°C) | 200hrs | Pass |
| Temperature Cycling (TC) | JESD22-A104 (-55°C/+125°C/2cy/hr) Precond. L1;Tr:260°C | 500x | Pass |
| Temperature Cycling (TC) | JESD22-A104 (-40°C/125°C/2cy/hr) Precond. L1;Tr:260°C | 850x | Ongoing |
| Temperature Cycling on Board (TCoB) | IPC 97-01 (-25°C/+100°C/1cy/h) | 1000x | Pass |
| Temperature Cycling on Board (TCoB) | IPC 97-01 (-40°C/+125°C/1cy/h) | FF>500x | Pass |
| Drop Test (DT) | JESD22-B111 | FF<10% fails @ 20 drops | Pass |

Table 3: Reliability testing results.

assessment can only be attained by volume production. 

References

1. M. Brunnbauer, T. Meyer, G. Ofner, K. Mueller, R. Hagen, “Embedded Wafer-Level Ball Grid Array (eWLB),” Electronic Manufacturing Tech. Symp. (IEMT), 2008 33rd IEEE/CPMT International; pp. 1-6.
2. B. Keser, et al., “The Redistributed Chip Package: A Breakthrough for Advanced Packaging,” Electronic Components and Tech. Conf., 2007. Proc. 57th, pp. 286-291.
3. S-J. Lee, et al., “Electrical Characterization of Wafer-level Fan-out (WLFO) Using Film Substrate for Low Cost Millimeter Wave,” Electronic Components and Tech. Conf. (ECTC), 2010 Proc. 60th, pp. 1461-1467.
4. N. Hayashi, et al., “A Novel Wafer-Level Fan-out Package (WFOPTM) Applicable to 50µm Pad Pitch Interconnects,” Electronics Packaging Tech. Conf. (EPTC), 2011 IEEE 13th, pp. 730-733.
5. H.S. Hau, et al., “Innovative Fan-Out Wafer-Level Package Process and Adhered Si Wafer on the Backside,” Electronic Components and Tech. Conf. (ECTC), 2012 IEEE 62nd, pp. 1384-1387.
6. V. Kripesh, et al., “Design and Development of a Multi-Die Embedded Micro Wafer-Level Package,” Electronic Components and Tech. Conf., ECTC 2008. 58th, pp. 1544-1549.
7. E.O'Toole, et al., “Reliability, Processability, and Yield in 2-Layer RDL eWLB Packaging,” Advanced Packaging Conf. Semicon Europa 2012. Speaker 11, pp. 1-17.

Biography

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Market Forces Drive the Greening of Our Industry and Foster Innovation

By Osvaldo Gonzalez [CH2M Hill]

Healthy rivers, toxic-free cities, and semiconductor manufacturing processes are not three topics most people would generally combine into one conversation. Nevertheless, the inextricable link between these three topics is at the center of a growing discourse within the industry that promises a new emphasis on innovation—one that takes the long-term perspective on a traditionally fast-paced market. The social and environmental forces that impact the industry today have shifted the conversation about environmental performance away from mere regulatory compliance towards a more opportunity-focused attitude that addresses everything from resource optimization and operational cost control, to corporate social responsibility. By taking a look at what is driving these changes in the marketplace and exploring what they mean to how we do business, we can better understand how wafer packaging, assembly and testing will contribute to improving our industry while simultaneously improving the health of the planet and our communities. The following is a primer for why the trend toward “green” is happening and what we can expect to come from it.

Market Drivers

Today's marketplace is defined by the portability and connectivity enabled by the age of information (that thing the semiconductor industry coincidentally resides at the center of). The amount of information at our disposal today is unparalleled, as is our motivation to use it. One of the results of our access to and global sharing of information is the increased transparency it has created. The trend toward transparency is impacting many aspects of our

society; from our personal relationships, to how we do business. One of the latest trends in the information age marketplace is the dominance of verifiable performance data over third party certifications. When it comes to knowing just how “green” a company may be, never mind all the certificates of achievement that are on the lobby wall—the facts are all we need. Consumers not only want to know what your policies are, but they want to see proof you are working towards them. Today, consumer demand for transparency is putting pressure on the industry to employ quantitative metrics for reporting how manufacturers are impacting economies, communities, and ecosystems; and the more information the better.

Transparency and the demand for performance data have also shifted the public's expectations for corporate responsibility. A company is no longer just expected to make quality products while turning a profit and complying with the legal requirements associated with its business. Companies are expected to do more (and prove it). The number of jobs created and revenues generated are still important metrics, but now we also want to know how much carbon you emitted into the atmosphere, how many tons of waste you diverted from the landfill, and whether or not your products are polluting the aquifers. Although the emphasis is predominantly still on impacts to people, a synergy has been forged between economic viability, community vitality, and the larger environmental considerations that force a company's overall value proposition to include an analysis of economic, social, and environmental attributes—the Triple Bottom Line (**Figure 1**). The leaders within our industry have

taken a proactive stance on this matter by engaging in voluntary reporting programs and third party certifications. Companies have shown a willingness to ‘open their books’ and allow outsiders to evaluate their policies, products, buildings, operations, and/or their impact to the environment by way of greenhouse gas emissions or other impacts to living systems. The companies that participate in these programs do so for sound business reasons; and below are the three major reasons why.



Figure 1: The three components of the triple bottom line: Economy, Environment, and Society

The semiconductor manufacturing industry requires high quantities of natural resources. It is no secret that the resources available on this planet are limited; it is the reason why wastefulness is not a good long-term strategy. Few people, however, think about the amount of resources it takes to make the chips that reside inside the devices we use every day. It takes a lot of water, energy, minerals, chemicals, and human ingenuity to make semiconductors. According to a 2010 survey including 44 different facilities from 18 of the largest manufacturing companies in the world, wafer starts consume, on average, approximately 1.7kWh of electricity, 4.3 gallons of water (not including ultrapure water, or UPW), and generate 0.06

pounds of waste for every cm² of wafer output from the fabrication plants [1]. When you consider that 25.7 million square inches of silicon per day are projected to be produced in 2013 [2], it is easy to imagine the immensity of this impact worldwide. For semiconductor manufacturing companies, securing a steady supply of high-quality, well-priced, natural resources is more than good business policy – it is part and parcel of a responsible environmental policy.

The costs of energy, water, and material resources are volatile and represent a significant risk to profit margins. The cost of supplying energy, water, and raw materials to a manufacturing process takes up the lion's share of operating expenses in a wafer manufacturing plant. When the prices of these resources vary so greatly from one country to the other (**Figure 2**) and fluctuate over time, profitability suffers [3]. One thing that is quite clear about energy in the future is that prices and demand are on the rise. Researchers predict that despite a projected 15% increase in energy prices by 2035, the global demand on energy resources will grow by 60% [4]. As for water resources, global freshwater use for energy production alone is expected to increase by 20% in that same time frame [5]. Global water scarcity issues and competing uses such as sanitation, energy production, and food production, make quality and access a more pressing concern than price volatility. With the prospect of 9 billion people inhabiting Earth by 2050 and the increasing water demands that come with it, securing access to water resources can be a delicate topic for wafer manufacturers.

The volatile price of energy and the scarcity of fresh water incentivizes manufacturers to implement effective resource management initiatives within their organizations and develop ways to do more with less—a basic tenet of both economies and ecologies. To eliminate the risk to profitability, companies engage in strategic negotiations to establish predictable pricing structures on their utility services and engage in demand reduction projects that

modify the production process and/or plant operations in a way that reduces the amount of resources consumed. The more aggressive companies go as far as producing some part of the energy and water resources needed for production themselves. While all of these measures have risk mitigation and long-term profitability as their primary motivations, the proactive approaches align well with principles of environmental sustainability and result in reduced carbon emissions, less waste, and can even improve a region's access to fresh water resources [6].

Better resource management requires better monitoring of resource use. As the adage goes, “you cannot manage what you do not measure.” At the end of the day, greening up (regardless of the industry) is about

managing your resources in the most informed way possible. Tracking operational characteristics depends on a robust monitoring program capable of both extracting meaningful data from a process as well as applying it to making the process more resource-efficient. This is not a new concept to the industry; what is new is the diversity of disciplines included in the criteria. The goal of implementing comprehensive monitoring programs is still the same: to inform strategic improvements to the manufacturing process.

For as much as we strive to get quality information, one critical aspect to our information gathering efforts resides in comparability—we must be able to compare against a reference baseline. Comparable operational data derived from actual manufacturing plants is the

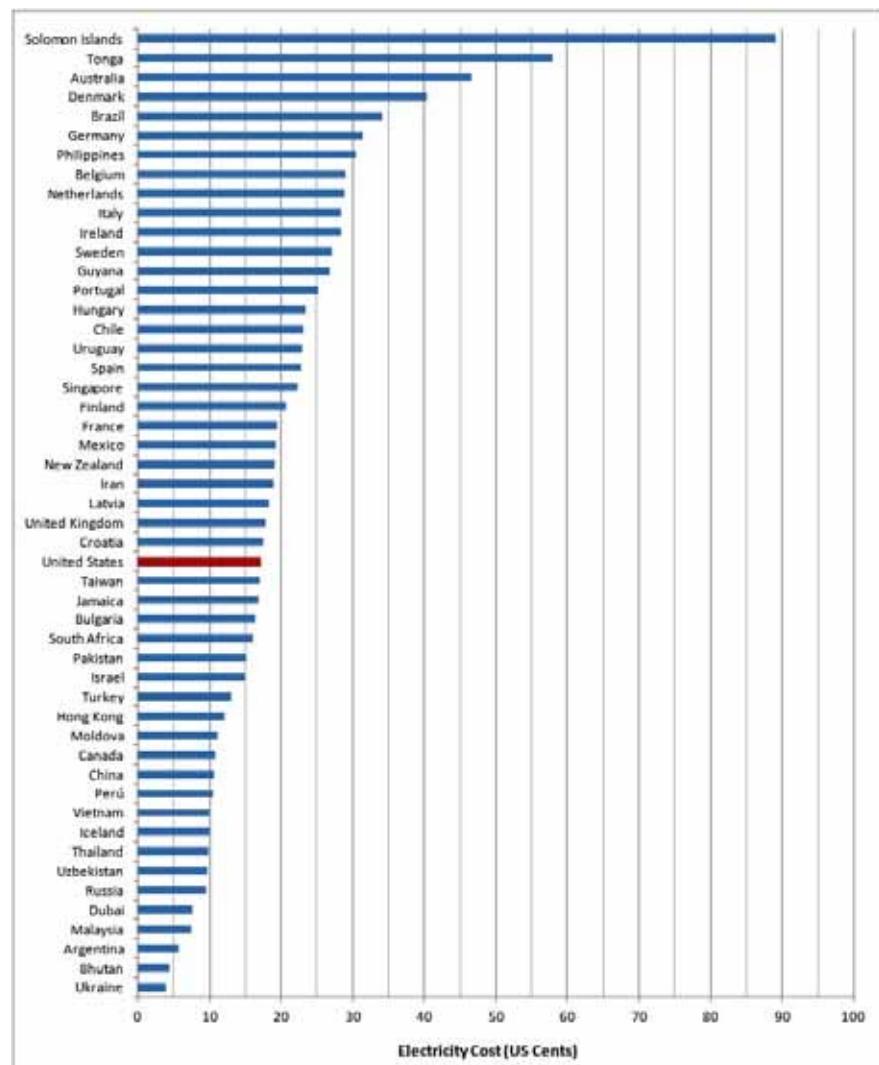


Figure 2: Electricity costs by country [3].

best way to evaluate how effectively energy, water, and chemical resources are utilized. This lets companies see priority initiatives by highlighting situations where performance is far from the industry norm. An additional benefit to comparable data sets is the context that it provides for feasibility. When many other plants are able to achieve a targeted level of performance, it is reasonable to determine that the improvement you seek is achievable. This is why it is essential that every step in the wafer production, testing, and packaging process be effectively monitored and evaluated for performance. We all have a role in reducing the resource demands of wafer production; below are some examples of how this is being done in the marketplace.

Scrutinizing Packaging/Assembly/Testing Processes

The growing awareness of natural resource-related risks has brought the matter of sustainability into the boardroom and incentivized companies to move swiftly towards aggressive resource management policies. Now more than ever, this shift is perceived as necessary to secure a company's short- and long-term viability. Semiconductor manufacturers are scrutinizing resource use and reducing operating costs by breaking down the process step by step and looking for ways to eliminate waste and improve resource efficiency throughout the manufacturing process. But what does this all mean for the packaging, assembly, and testing side of operations?

Simply put, it is time to get involved in the conversation. As significant contributors to the overall footprint of resource use, it is important that people involved in packaging, assembly, and testing understand the potential risks and benefits their work represents to their clients and the industry as a whole and work to improve their environmental, social, and economic performance in measurable ways.

There are many opportunities for improvement in the production, assembly, testing, and transport side of the equation, but it all begins with clear objectives. Set performance

goals and develop a plan with specific priorities for the first stage. Once you identify where resource utilization can be improved, work collaboratively to achieve it. An example of such a collaborative effort is the use of waste heat. Using waste heat from boilers to pre-condition outside air can be a useful strategy for reducing operating costs while lowering the total greenhouse gas emissions. By knowing what the overall environmental objectives for the company include and having a common language for discussing proposed interventions, those involved in any step of the production process can support the sustainability objectives.

The key metrics used to evaluate environmental performance include looking at performance as a function of wafer output or as a function of plant floor area. Whether for reducing greenhouse gas emissions, water use, energy use, or material utilization, there is a lot of potential for improvement in the way in which company funds are applied toward procurement of goods and services. A strong procurement policy that looks upstream to identify resource risks as well as looks downstream to evaluate ways to extend the useful life and recyclability of manufactured products is a fundamental part of the global shift toward the greening of industries.

Down the Road

There is no telling what new innovations will come out of a quest to eliminate all waste from the semiconductor industry, but such a bold endeavor is nothing more than a prerequisite to accomplishing the goal of this globally accelerating trend toward green. "Sustainability" is the new "quality" and corporate programs to

implement sustainability programs parallel the adoption of total quality management (**Figure 3**) [7]. Based on that experience, we can expect to see increasingly aggressive monitoring and reporting requirements as well as ongoing waste reduction and resource optimization programs. We will also see a shift away from the distinction between capital and operational expenses, which favor a lowest first cost solution while ignoring the operational side of ownership. Combined funding mechanisms between capital expenses and operations will allow companies to realize process improvements based on life cycle savings. As the market acclimates to evaluating decisions based on total cost-of-ownership, life cycle analysis will not only impact what your company buys from others, but also what it sells. Research is already underway to develop biodegradable semiconductors for short-term applications. Durable substrates will be designed for adaptability to multiple configurations with the intent of extending their useful life through repurposing. We have a long way to go in making our industry entirely sustainable, but if the last ten years have shown us anything, it is that what might have seemed impossible just a short time ago, can be commonplace today.

One Step at a Time

So with all the hubbub of sustainability and the opportunities it promises, where does one begin? The answer is very simple: a plan. Begin defining your key performance indicators and creating a monitoring plan to measure them. Develop and implement your monitoring plan and make sure to include system-wide metering as well as sub-metering at the specific system(s) or equipment level. This allows you to manage your

| STAGE | TOTAL QUALITY MANAGEMENT | SUSTAINABILITY INITIATIVES |
|--------------|--|---|
| Early | Treated solely as a cost, and an additional step at the end of manufacturing processes. | Treated solely as a risk, or as a response to regulations that require compliance. |
| Intermediate | Inspections integrated throughout processes. Some process-improvement and other cost-reduction opportunities identified. | Treated as both a risk and an opportunity. Program extended into multiple corporate functions. |
| Advanced | Expanded beyond product lifecycle into workforce behaviors. Also extended beyond organization to trading partners. Used as a competitive differentiator. | Expanded beyond organization to entire "sustainability supply chain." Opportunities include talent management benefits. Used as a competitive differentiator. |

Figure 3: Total quality management principles and sustainability initiatives.

various loads separately as well as obtain overall data for a building or a campus that can be compared against other plants. This brings me to my next point: benchmarking. Benchmarking your operations against another like facility (whether inside your company or industry-wide) is a first step toward finding the greatest opportunities for improvements. By taking these initial steps of setting goals, tracking progress, and comparing against others, you will be well on your way toward improving your triple bottom line and bringing about positive change for the industry.

Summary

The steady shift towards sustainability (a euphemism for the social, environmental and market forces affecting all businesses today) has created a powerful gravitational epicenter for business policy and long-term strategic planning. When it comes to the “greening” of the semiconductor manufacturing industry, the possibilities—as well as the risks—are daunting. We have amazing tools at our disposal now to collect, process, and share data that enables tremendous advances in resource management to take place. It is high time we use them. Through the effective management of human, natural, and economic resources, our industry stands to make a lasting positive impact to the health of our planet and our communities. 

References

1. Mohler, Nixon, & Williams; “Environmental Metrics Program, 2010 Annual Survey Data Set,” April 20, 2011.
2. SEMI annual silicon shipment forecast for the semiconductor industry, October 2012; www.emsnow.com/npps/story.cfm?id=49671; accessed 12/18/2012.
3. United States Energy Information Administration; www.eia.gov/countries/; accessed 12/19/2012.
4. World Energy Outlook, 2012 Report Fact Sheet; www.worldenergyoutlook.org/publications/; accessed 12/20/2012.
5. World Water Assessment Programme; The United Nations World Water Development Report 3: Water in a Changing World. Paris: UNESCO, 2009.
6. K. Freas, A. Munévar, “CH2M Hill’s Systems Thinking: Sustainable Water in a Changing Climate,” Live Better Magazine, April 2, 2012.
7. S. F. Fust, L.L. Walker, “Corporate Sustainability Initiatives: The Next

TQM?” Korn/Ferry International, Executive Insight, 2007.

Biography

Osvaldo “ozzie” Gonzalez received his Bachelor’s degree in environmental science from Humboldt State U., his Masters in architecture from Cal Poly Pomona, and is a Sustainable Design Technologist at IDC Architects, a subsidiary of CH2M Hill; email osvaldo.gonzalez@ch2m.com

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GUEST EDITORIAL



Speeding 3D-IC to Commercialization: Update on SEMI Standards

By James Amano *[SEMI]*

The industry is poised to jump from concept to commercialization with 3-D technologies. Given their potential for increased performance, smaller footprint, and reduced cost and power consumption, 3D-IC technologies are now on the leading edge of innovation. 3D integration using through-silicon vias (TSVs) promise a fundamental shift for current multi-chip integration and packaging approaches. But cost-effective, high-volume manufacturing will be difficult to achieve without standardized equipment, materials, and processes, especially because 3D-ICs' design and mechanical complexity can lead to increased manufacturing defects, as well as thermal management issues and signal interference.

Multiple manufacturing challenges must be resolved to move forward. Focusing on 3D-IC technology and the manufacturing process will help reduce costs through increased throughput, improved product quality, better yields, and lower maintenance and operational expenses. No single company can fully realize these benefits without working closely with their suppliers and their competitors. Highly automated and advanced manufacturing systems comprise multiple equipment types, technologies and supporting products from best-in-class suppliers from around the world; enabling these different processes, products and technologies to work seamlessly and cost-effectively together requires diverse, well-informed and effective industry standards.

Understanding the essential role of standards in enabling low-cost, high-quality manufacturing, SEMI first

charged its International Standards group with exploring the challenges of 3D-IC manufacturing issues in spring 2010. The first 3DS-IC (where the "S" stands for "stacked") SEMI Standards Technical Committee was formed in North America in late 2010, with a counterpart in Taiwan created in July 2011. In early fall 2012, the Japan Packaging Committee authorized the formation of a 3D-IC Study Group with plans to explore and ultimately engage in the activities in North America and Taiwan (**Figure 1**).

TSV Geometrical Metrology

The 3DS-IC SEMI Standards committee's first accomplishment was *SEMI 3D1, Terminology for Through Silicon Via Geometrical Metrology*. SEMI 3D1 provided a starting point for standardization of geometrical metrology for selected dimensions of

through-silicon vias (TSVs). Although different technologies measured various geometrical parameters of an individual TSV, or of an array of TSVs — such as pitch, top diameter, top area, depth, taper (or sidewall angle), bottom area, and bottom diameter — it was difficult to compare results from the various measurement technologies as parameters are often described by similar names, but actually represent different aspects of the TSV geometry. The Inspection & Metrology Task Force recognized the need for such a standard. SEMI 3D1 is an important first step in promoting common understanding and precise communication between stakeholders in the 3D-IC manufacturing supply chain.

Glass Carrier Wafer Specs

Recently at the North America (NA) Standards Fall 2012 meetings, the NA 3DS-IC Committee approved SEMI

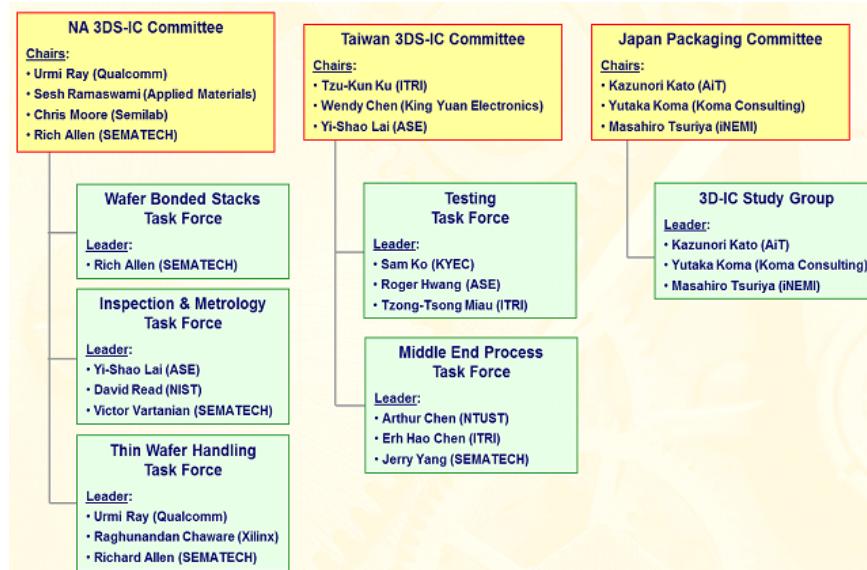


Figure 1. SEMI International Standards organization charts.

Draft Document 5482, *New Standard: Specification for Glass Carrier Wafers for 3DS-IC Applications*. Developed by the Bonded Wafer Stacks Task Force, this specification addresses the needs of the industry by providing the tools needed to procure pristine glass carrier wafers for use in 3DS-IC processes.

SEMI Draft Document 5482 describes dimensional, thermal, and wafer preparation characteristics for the glass starting material that will be used as carrier wafers in a temporary bonded state. This specification also describes glass carrier wafers with nominal diameters of 200 and 300mm, and a thickness of 700nm, although the wafer diameter and thickness required may vary due to process and functional variation. Such variations need clarification in the purchasing order or in the contract. Methods of measurements suitable for determining the characteristics in the specifications are also indicated (**Figure 2**). Document 5482 is on track to be published as SEMI 3D2 in early 2013.

SEMI 3DS-IC Standardization Activities Continue

The NA Three-dimensional Stacked Integrated Circuits (3DS-IC) Committee and its associated task forces met in conjunction with the NA Standards Fall 2012 meetings in San Jose, California in July. Summaries of task force activities are presented below:

Bonded Wafer Stacks Task Force. In addition to the development of SEMI Draft Document 5482, the Bonded Wafer Stacks Task Force will continue development of SEMI Draft Document 5173B, *New Standard: Guide for Describing Materials Properties and Test Methods for a 300mm 3DS-IC Wafer Stack*, which failed technical committee review based on inputs received from the Cycle 6 voting period. The task force plans to reballot this document as 5173C for the Cycle 1, 2013 voting period. The task force will also continue to work on the SEMI

New Activity Report Form (SNARF #5174, *New Standard: Specification for Identification and Marking for Bonded Wafer Stacks*).

Inspection & Metrology Task Force. The Inspection & Metrology Task Force received committee approval to develop

a new test method for measuring warp bow, and TTV on silicon and glass wafers as SNARF #5506.

Current metrology strategies have evolved from methods used to characterize smaller, lower aspect ratio geometries. Conventionally, three-point



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Taiwan 3DS-IC Activities

The Middle End Process Task Force formalized its standardization efforts via SNARF #5473 (*New Standard: Guide for Alignment Mark for 3DS-IC Process*) and SNARF #5474 (*New Standard: Guide for CMP and Micro-bump Processes for Frontside TSV Integration*). The task force plans to submit SEMI Draft Document 5474 for balloting in early 2013. The Testing Task Force also received approval to begin work on a new guide for *Incoming/Outgoing Quality Control and Testing Flow for 3DS-IC Products* as SNARF #5485. (For more information about Taiwan 3DS-IC activities, please contact Ms. Catherine Chang (cchang@semi.org) at SEMI.)

Ballots for the above activities will be issued throughout 2013, and are just the beginning of this global, industry-wide effort. Over 160 technologists from industry, research institutes, and academia around the world have already joined the SEMI 3DS-IC Standards Committee and are at work on these critical standards.

Pre-competitive collaboration is difficult, and involves hard work by industry experts, but it creates significant benefits for the industry as a whole, for companies participating, and for individuals involved in the process. If you or your company is not yet involved in these efforts to shape the future of 3D-IC, learn more about SEMI Standards by visiting www.semi.org/en/Standards. Note that participation in the SEMI Standards Program is free, but requires registration. To learn more, contact jamano@semi.org or register at: www.semi.org/standardsmembership.

Biography

James Amano received his BA from the U. of Colorado at Boulder, and is the Senior Director of International Standards at SEMI; email jamano@semi.org

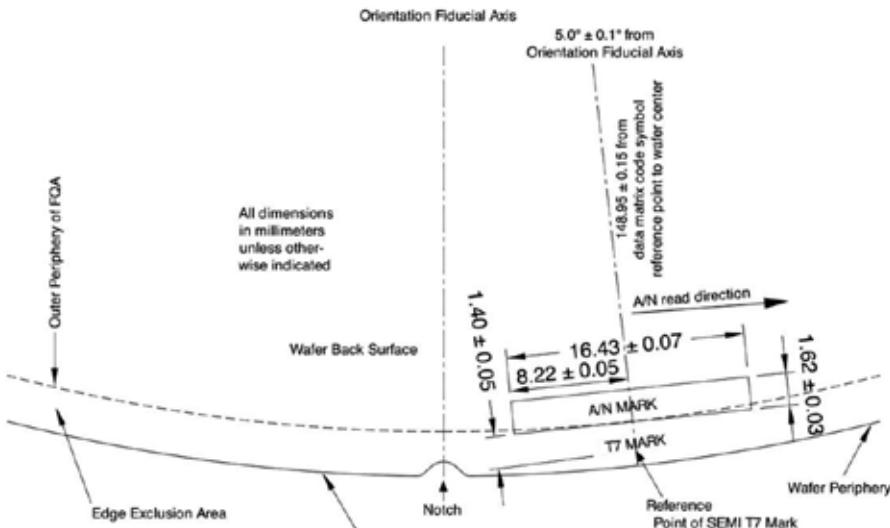


Figure 2. Optional A/N code field location on back surface of 200mm and 300mm diameter glass wafers.
SOURCE: SEMI 3D2-0113

mounts have been used to measure flatness/warp of wafers along with the gravity compensation. For instance, 3DS-IC applications use larger and thinner wafers than conventional applications. Large, thin wafers have inherently low stiffness, leading to large deflections, which make compensation more challenging. Ball mounts cause large deflections, four-point and ring supports have redundant support and are sensitive to how parts are placed on the mount.

The industry benefits from identifying an alternate test method that better reflects the application usage of these wafers. One approach used in the industry is a similar set up to Sori with a wire mount and a non-contact scanning method that allows depicting a complete picture of the wafer's shape and dimensional parameters.

SNARF #5506 will lead to the development of a new test method that accurately and reliably depicts the dimensional shape of single silicon and glass wafers that are $\geq 300\text{mm}$ in diameter and $\leq 775\mu\text{m}$ in thickness and that uses a wire mount and laser scanning interferometry. This method will recommend that the wafer is characterized in a position that allows for a free state profile measurement

on a flat surface. The document will include applicable ranges for valid measurements where possible.

The Inspection & Metrology Task Force will also continue its work on the following standardization activities:

- New Standard: Guide for Measuring Voids in Bonded Wafer Stacks (SNARF #5270)
- New Standard: Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures (SNARF #5410)
- New Standard: Terminology for Measured Geometrical Parameters of Through-Glass Vias (TGVs) in 3DS-IC Structures (SNARF #5447)

SEMI Draft Document 5410 is scheduled to be submitted for the Cycle 1, 2013 voting period, which occurs January 3–February 15.

Thin Wafer Handling Task Force. The Thin Wafer Handling Task Force is nearing completion in its development of SEMI Draft Document 5175, *New Standard: Guide for Multi-Wafer Transport and Storage Containers for 300mm, Thin Silicon Wafers on Tape Frames*. Ballot 5175 is scheduled to be submitted for the

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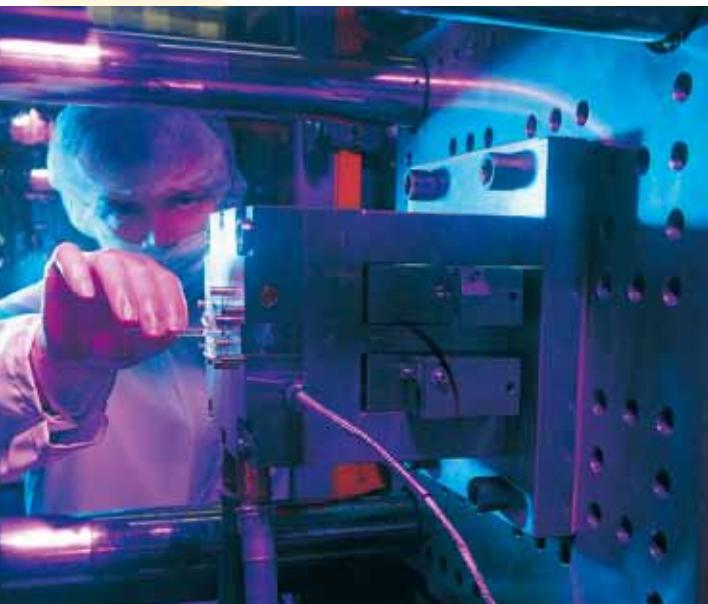
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IWLPC Announces 2013 Event Sponsors

Chip Scale Review & the SMTA are pleased to announce plans for the 10th Annual International Wafer-Level Packaging Conference (IWLPC) & Tabletop Exhibition scheduled for November 4-7, 2013 at the DoubleTree Hotel in San Jose, California are well underway. This premier industry event explores leading-edge design, material, and process technologies being applied to wafer-level packaging applications. There will be special emphasis on numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand WLP solutions for integration, cost, and performance requirements. In addition to professional development courses, the conference includes three tracks with two days of technical paper presentations covering: Wafer-Level Packaging; 3D (Stacked) Packaging; and MEMS Packaging.

Call for Papers Extended

The IWLPC Technical Committee invites all those interested to submit an abstract for this program.

Contact a technical committee member or visit the website and submit your abstract to http://www.iwlpc.com/call_for_papers.cfm

The call for papers deadline has been extended to April 19.

Sponsorship Opportunities

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This event would not be possible without the support of the event sponsors. This year's Platinum sponsors are Deca Technologies, Invensas Corporation, Stats ChipPAC and SUSS MicroTec.



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Stats ChipPAC is a leading provider of packaging and test solutions for the communications, digital consumer and computing markets. STATS ChipPAC offers advanced wafer level packaging, flip chip interconnect, TSV, 2.5D and 3D integration to support next generation mobile devices requiring higher levels of performance, increased functionality and compact sizes.



With more than 60 years of engineering experience SUSS MicroTec is a leading supplier of process equipment for microstructuring in the semiconductor industry and related markets. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Nanoimprint Lithography as well as key processes for WLP, MEMS and LED manufacturing.

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This year's Gold Sponsors are EV Group, Nanium and Pac Tech.



EV Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices, and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, EV Group services and supports an elaborate network of global customers and partners all over the world. More

information about EVG is available at www.EVGroup.com.



Nanium is a world-class provider of semiconductor assembly, packaging and test engineering and manufacturing services, and a leader in 300mm wafer-level packaging (WLP). The company offers in-house capabilities for the entire development chain, from design to multiple packaging technologies, and the flexibility to tailor solutions that respond to the most specific and demanding customer requirements. The company is based near Porto, Portugal, and has an office in Dresden, Germany.



Pac Tech Packaging Technologies is a provider of both WLP services and equipment. The company has over 15 years of experience in the industry and has manufacturing sites all around the world, including Germany, United States, Japan, and Malaysia. These sites can supply both engineering and prototyping services, as well as high volume production. Additionally, Pac Tech is structured to provide a single source for all contract bumping services.



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In addition to Platinum, Gold and Silver sponsorship opportunities, there are many ways to become a sponsor for IWLPC. New to 2013 is the hotel key card sponsorship. The key card sponsor's company logo will be imprinted on all attendees hotel keycards. The cost is \$1750 and there is only one key card sponsorship! Sign up today for the remaining Silver, Reception, Lunch, WiFi or Refreshment sponsorships. Visit

<http://www.iwlpc.com/sponsorinfo.cfm> for more information. Email info@chipscalereview.com or contact Ron Molnar at rmolnar@chipscalereview.com or call him at 480-215-2654.

Exhibitor Opportunities

Tabletop exhibits at IWLPC are \$1250 for an 8'x10' or 8'x8' exhibit space inclusive of one keynote dinner ticket, electronic attendee list, directory listing, lunch each day, company sign, IWLPC proceedings and one conference pass. Booth reservations are being taken up now. Visit the exhibitor tab at the website to retrieve the application and pick your booth off the floorplan also located on the website. Space is limited. Be sure to contact your CSR representative or Seana Wall at SMTA seana@smta.org today to get a premium booth location while they last.

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BiTS Takes a Byte Out of Test

By Ron Molnar [[Chip Scale Review](#)]

Attendees of the 14th annual Burn-in and Test Strategies (BiTS) Workshop held in Mesa, AZ on March 3-6, 2013 were once again treated to a variety of excellent programs focused on the burn-in and test of integrated circuits. Attendance continued to be strong. There were 361 total participants, which included conference attendees, exhibitor staff, and exhibits-only visitors.

The event kicked off with a 3-hour Tech Talk titled “Thermal and Mechanical Challenges for Test Handlers” by Jerry Tustaniwskyj, PhD, Director of Technology Development at Delta Design, Inc. It was followed by a 3-hour Tutorial titled “Package Test is a Dirty Business” by Jerry Broz, PhD from International Test Solutions describing socket cleaning strategies to reduce the cost of test and improve the overall equipment effectiveness. The first day drew to a close with the Socket Market Report by Fred Taber of Taber Consulting.

Fred Taber, the General Chair and Test Technology Consultant, and his distinguished organizing committee have diligently worked to improve this event year after year. This year they video recorded all of the presentations and made the slides and audio available to the registered attendees as a supplement to the published technical papers.

The second day opened with the Keynote Address titled “The Dramatic Restructuring of the Integrated Circuit Industry” by Bill McClean, President of IC Insights, Inc. McClean described their new “tops down” forecasting model for the semiconductor industry

which is now tied closely to the growth in global Gross Domestic Product (GDP). After emerging from a lackluster 2.0% growth rate during 2007 – 2012, he expects the IC industry CAGR to more than triple to 7.4% in



Bill McClean of IC Insights delivering the Keynote Address. *Photograph: courtesy of BiTS Workshop, LLC*

the next 5-year period.

Attendees enjoyed 29 technical presentations from test industry leaders organized in 7 sessions over 2-1/2 days, including a poster session and a panel discussion titled “Interconnectology: Inspiring a Paradigm Shift” hosted by Francoise von Trapp, the Founder of 3D InCites. The panelists were Scott Jewler of Advanced Nanotechnology Solutions, Chris Scanlan of Deca Technologies, Dr. Sitaram Arkalgud of Invensas, and Ira Feldman of Feldman Engineering.

Many new products and services were on display and described by representatives from the 52 companies in the Exhibit Hall over the course of two days. Principal sponsors were Test Tooling Solutions, Teradyne, Interconnect Devices, R&D Circuits, Sensata Technologies, and Chip Scale



Talking Points ‘talk show’, hosted by (right) Francoise von Trapp (of 3D InCites & Impress Labs), with guests (L to R) Scott Jewler (Senior VP, Advanced Nanotechnology Solutions, Inc.), Sitaram Arkalgud (Director of 3D Technologies, Invensas Corp.), Chris Scanlan (VP Product Development, Deca Technologies). Not Shown is guest Ira Feldman (President & CEO, Feldman Engineering Corp.) *Photograph: courtesy of BiTS Workshop, LLC*

Review. Networking was encouraged amongst the international crowd during the breaks, receptions, and the western-theme “Wrangler Roundup” dinner.

Fred Taber summarized it best, “BiTS 2013 was a very successful workshop, with a strong technical program highlighted by the Keynote Address delivered by Bill McClean of IC Insights



Carol McCuen (center) of R&D Circuits receives the Attendee Choice award from (left) Fred Taber, BiTS Workshop General Chairman and Mike Noel of Freescale BiTS Workshop Technical Program Chair.

Photograph: courtesy of BiTS Workshop, LLC



BiTS EXPO, Multitest booth. L to R: Jim Brandes, Kim Barrett, Tony DeRosa, Bob Chartrand (all of Multitest) *Photograph: courtesy of BiTS Workshop, LLC*



BiTS EXPO, IDI booth. L to R: Jeff Tamasi, Kim Hause, Jon Diller, Tim Dowdle, (all of Interconnect Devices Inc.) *Photograph: Chip Scale Review*

and the Talking Points ‘talk show’ hosted by Francoise von Trapp of 3D InCites, plus the EXPO was sold out and then expanded to accommodate additional exhibitors.” Planning has already begun for the next BiTS Workshop to be held on March 9 – 12, 2014.



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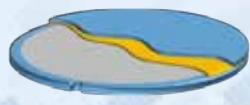
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Product News

EV Group Developing Room Temp Covalent Bonding Technology

EV Group (EVG) is developing equipment and process technology to enable covalent bonds at room temperature. The technology will be available on a new equipment platform, called EVG580® ComBond®, which will include process modules that are designed to perform surface preparation processes on both semiconductor materials and metals. The process enables treated surfaces to form strong bonds at room temperature instantaneously without the need for annealing.

"In response to market needs for more sophisticated integration processes for combining materials with different coefficients of thermal expansion, we have developed a process technology that enables the formation of bond interfaces between heterogeneous materials at room temperature," stated Markus Wimplinger, Corporate Technology Development and IP Director for EV Group. He also noted that the new technology will enable different variants of the new process according to the requirements of different substrate materials and applications.

The new process solutions will enable covalent combinations of compound semiconductors, other engineered substrates and heterogeneous materials integration for applications such as silicon photonics, high mobility transistors, high-performance/low-power logic devices and novel RF devices. The process technology and equipment that enables this room temperature covalent wafer bonding will be applied to EVG's wafer bonding solutions for MEMS wafer-level packaging, as well as to the integration of MEMS and CMOS devices.

Equipment systems based on a 200mm modular platform, tailored for the specific needs of the new processes, will be available in 2013.

ACE Unveils LTS 300 Automated Hot Dip Lead Tinning System

ACE Production Technologies has announced the introduction

and availability of the LTS 300, an automated molten hot dip solder lead tinning system for reconditioning all T/Hole, SMT and QFP components, and to ensure their compliance with RoHS and hi-rel requirements.

"The new LTS 300 actually combines three (3) essential tinning processes in one machine; it performs a Dip process for through-hole components, a Drag process for chips and LCCs, and is equipped with a vacuum-articulated spindle for tinning QFP leads," said Alan Cable, President of ACE.

These applications include



LTS 300

refurbishing legacy components (removing the oxidized (plated) lead finish and replacing with a fused intermetallic Sn/Pb finish); gold embrittlement mitigation, i.e., removing the gold from the component leads by "solubilizing" in molten Sn/Pb solder; tin whisker mitigation (replacing tin plating with fused alloy); converting RoHS components to Sn/Pb and vice-versa; solderability testing (IPC/EIA J-STD-001 and ANSI-GEIA-STD-0006); and BGA cleansing, i.e., removing excess solder from extracted BGAs without wicking or solder suckers.

The LTS 300 employs a "dip" process for T/H components, using a flat wave solder nozzle, working in conjunction with pallets that hold the components in position through the process. Under program control, a pallet of components moves to the flux station followed by preheating, then to the first solder

pot (scavenging pot) to remove the existing coating. While immersed in the solder, a side to side motion provides a "scrubbing" action to help in dissolving the unwanted plating into the "scavenging" alloy. The pallet returns to the flux station where the leads are once again fluxed then conveyed to the second solder pot for the final homogenous intermetallic coating.

The LTS 300 also employs a "drag" process for chips, LCCs, and MELFs using a cascading solder nozzle. Components are pulled through a solder wave in a programmed and controlled manner, and as they escape the wave, the downward flow of solder draws off excess solder, leaving the pads on LCCs co-planer and chip terminations within dimensional specifications.

The QFP tinning process for fine pitch QFPs employs a side wave solder nozzle in a configuration that immerses the leads into a side wave to dissolve and remove the initial coating and then provide a final alloy coating.

Thermal Interface Material Enables Enhanced Thermal Conductivity for Modules

Infineon Technologies AG has incorporated a thermal interface material (TIM) solution from Henkel Electronic Materials that makes available a heat conducting compound optimized specifically for the architecture of power semiconductors in modules.

The companies jointly noted that power electronics are experiencing a continuous rise in their power densities. As a consequence, thermal management for today's power semiconductors must be integrated as early as their design phase. Only then can reliable cooling be safeguarded over the long term noted the company. A particularly important role is assigned to thermal conduction at

the link between the component and the heat sink. In these cases, materials are often used that cannot meet the growing requirements. The new TIM material was developed to address these challenges.

The TIM greatly reduces the contact resistance between the metal areas on the power semiconductor and the heat sink. On the EconoPACKTM+ of the new D Series, the contact resistance between the module and heat sink drops by 20%. With a high filler content, the material reliably applies its improved properties of thermal contact resistance from the first moment the module is switched on. There is no need for a separate burn in cycle usual on many comparable materials with phase change properties.

The development of the new heat conducting material focused on ease of processing in the form of honeycombs stencil-printed on modules. This prevents air from becoming trapped in

the link to the heat sink. Also, the heat conducting material does not contain any substances harmful to health, meeting the requirements under the Directive 2002/95/EC (RoHS). In addition, the TIM is free of silicone and does not conduct electricity.

Dr. Martin Schulz, responsible Manager for the qualification at the Application Engineering of Infineon Technologies AG, noted that, "The paste simplifies the link between the module and the heat sink, optimizes heat transfer, and so extends both the service life and the reliability of the modules." The TIM was developed for use on Infineon modules and is now available for the IGBT EconoPACKTM+ module series.

TESEC/FocusTest Partnership Produces Next-Generation MEMS Handler

TESEC Corporation announced the

development and sales of the ULTRA MEMS Handler - designed jointly by TESEC and FocusTest Inc. - targeting inertial (accelerometer, gyroscope and magnetometer) MEMS devices. The new handler is a carrier-based system with parallel test capabilities for 16, 32, 64 and 96 devices. The system will be available for demonstration and shipment mid-2013. TESEC noted that the overall MEMS market is the fastest growing portion of the semiconductor market, with 2012 revenues of \$11.5B and an expected growth rate exceeding 10% for the next several years.

The handler provides MEMS device suppliers with a significant throughput enhancement, as a significant portion of devices are being tested today on systems that provide only four to sixteen parallel processing. In addition to significantly higher parallel performance, the handler offers state-



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of-the-art features aimed at higher performance and lower test time. With ±360 degree, 3 axis rotation it is capable of providing stimulus for accelerometers and gyroscopes. A Magnetic Stimulus Unit adds magnetometer test capability, making it a 9 DOF (degrees of freedom) capable system. Future versions of the ULTRA are planned to expand coverage to address pressure sensor and high G MEMS devices.

TESEC will provide world-wide sales/distribution, manufacturing and support for the ULTRA. FocusTest will provide MEMS and test cell specific engineering and applications.

ECD Debuts Factory-Wide Humidity Monitoring System

ECD launched its latest product designed to reduce the risk of MSD- and ESD-related defects. The system, called SensorWATCH™, is a factory-wide humidity and temperature monitoring system that provides customer audit

protection, delivers 24/7/365 access to factory conditions worldwide, and eliminates time-consuming manual record keeping.

"As devices get smaller and densities tighter, the impact of moisture on electronics manufacturing is greater than ever before," explained ECD's Todd Clifton, VP of Sales and Marketing. "Moisture can adversely affect almost everything in an

electronics manufacturing environment and cause corrosion, poor solder paste performance, as well as delamination and internal cracking at the component level. Measuring and recording temperature and humidity is critical to complying with standards developed to prevent MSD- and ESD-related defects."

The product will be commercially available in April 2013. ■



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