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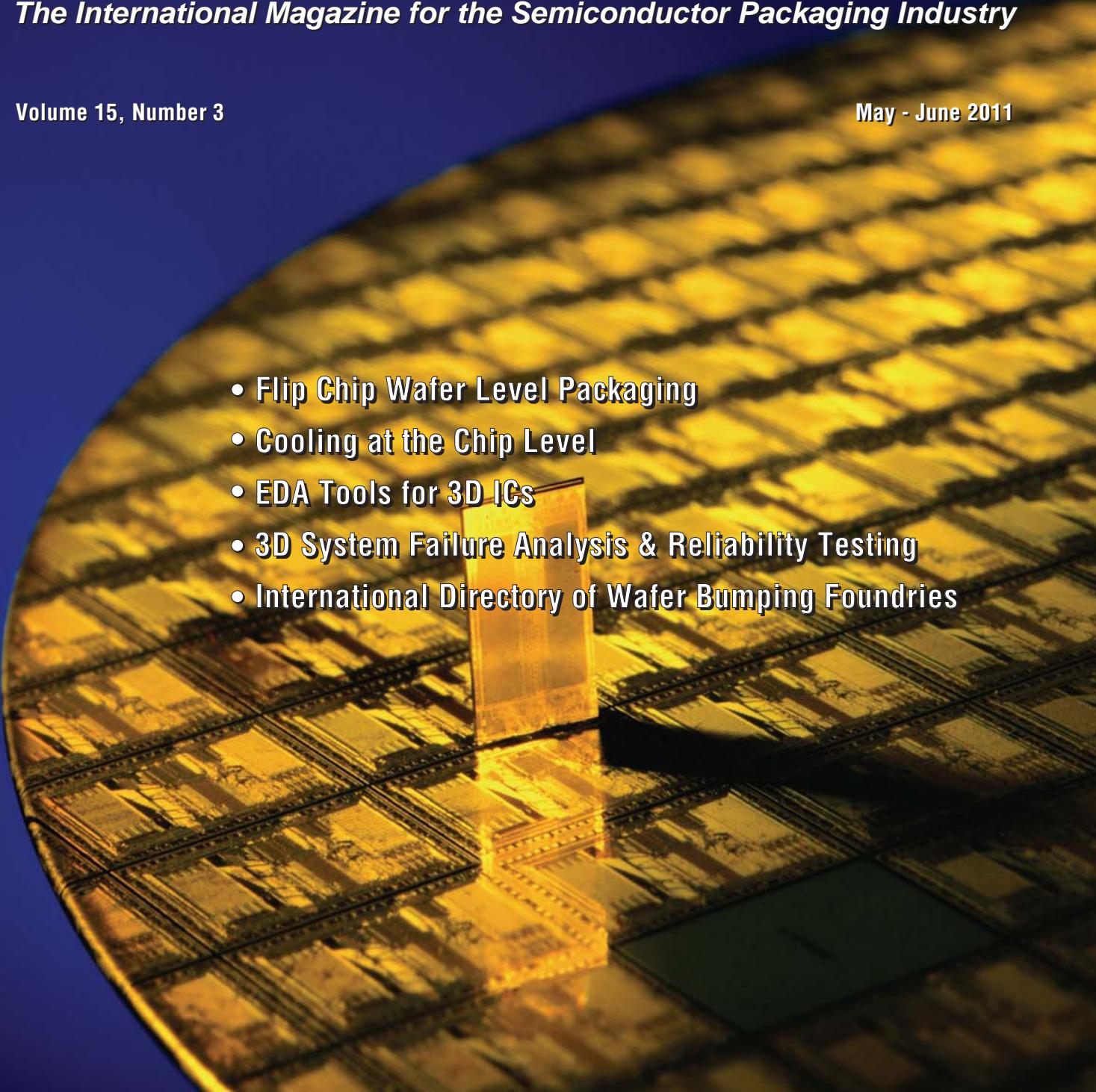
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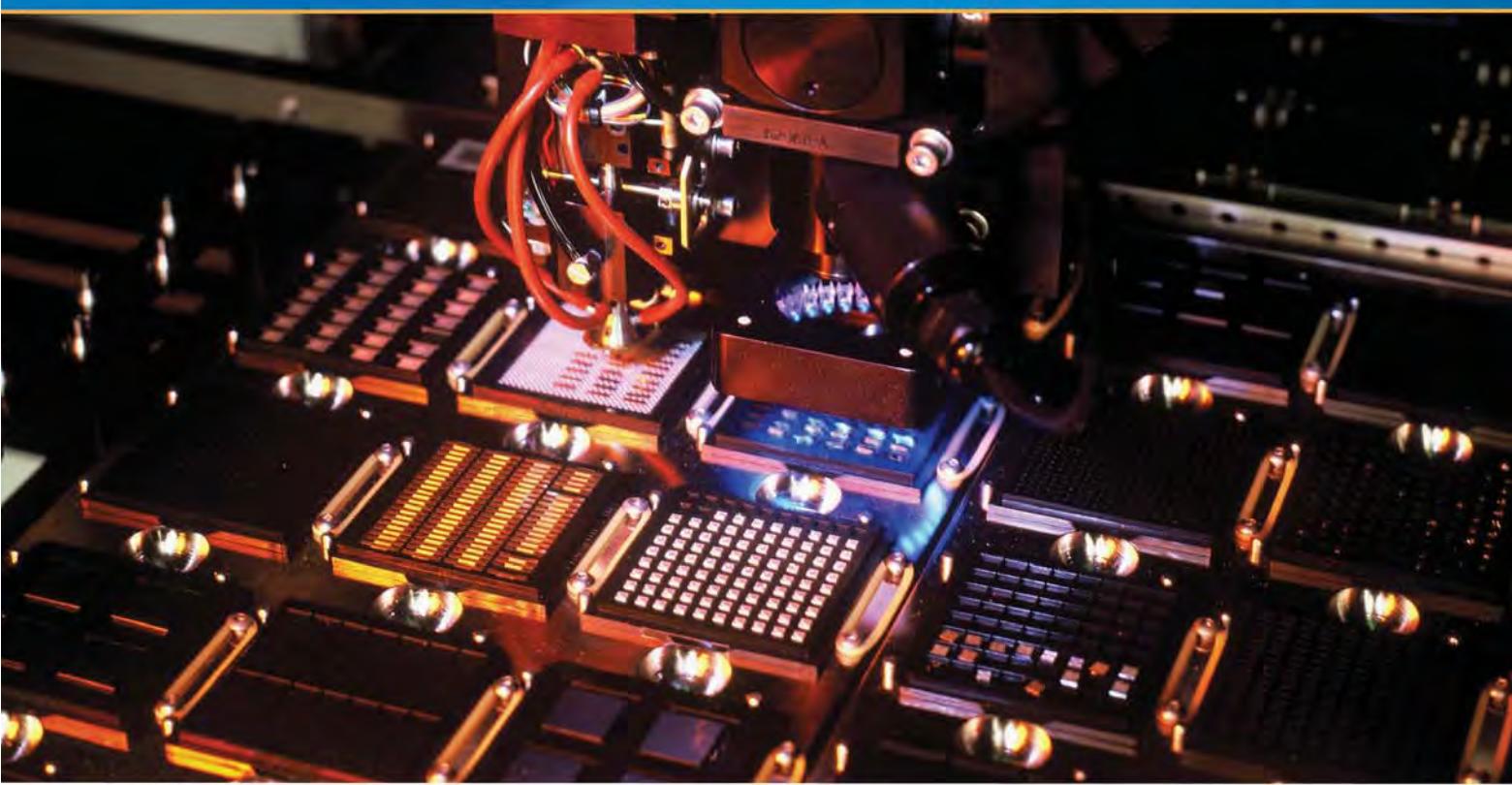
REVIEW®

*The International Magazine for the Semiconductor Packaging Industry*

Volume 15, Number 3

May - June 2011

- 
- Flip Chip Wafer Level Packaging
  - Cooling at the Chip Level
  - EDA Tools for 3D ICs
  - 3D System Failure Analysis & Reliability Testing
  - International Directory of Wafer Bumping Foundries



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**May-June 2011**

**Volume 15, Number 3**



As the demand for 'smart' devices grows, more applications will require wafer level packages (WLP) and 3D WLP to meet functionality demands. As a result, wafer-level chip scale packages (WLCSP), such as the one depicted in this photo shot by Jess Alford, are experiencing an industry growth spurt. In this issue, Dan Baldwin, of Engent Inc, writes about low-cost, 3D WLCSP technology that leverages the existing infrastructures of WLP and high-volume flip chip assembly as a stepping stone to 3D integration.

## Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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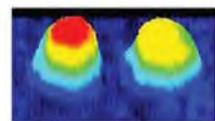
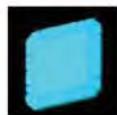
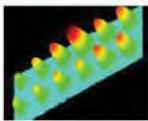
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# FROM THE PUBLISHER



## Just Showing Up

A colleague of mine was recently attending her daughter's National Honor Society induction, and told me that the Mayor of the city who gave the guest keynote divulged a bit of wisdom he had realized over the years through his experiences as a business consultant and also in public office. It's this: half of the secret to success is just showing up. It seemed pretty basic until I realized how much this applies to *Chip Scale Review*'s continued success as the semiconductor industry publication. We just keep showing up.

I'm not just talking about copies of the magazine being present at major and minor industry events; we show up in person, and it makes a difference in our awareness of what's happening in the industry, both from a technical and business perspective. What's more, we bring all that information back to our readers through event coverage and analysis by staff writers in the print publication and more recently, in *CSR Tech Monthly*, our e-Newsletter. In the past few months, you might have bumped into me; Francoise von Trapp, our contributing editor; or Ron Friedman and Ron Molnar, our sales representatives at events such as the BiTS Workshop, the GSA Memory Conference, SEMI-Therm, and MEPTEC's Heat is On! conference, and others.

Because we've realized how important these events are to our readers, we've introduced a new department in the magazine, Industry Happenings. It's not just a standard event calendar. On these pages you'll find coverage of the SEMITherm event by Ron Molnar. You'll also find previews of upcoming industry events such as SEMICON West and the IW LPC 2011.

My colleague never divulged what the Mayor said made up the other 50% of the secret to success; but I'd like to suggest that it's more than just showing up; it's getting involved. We've certainly discovered the benefits of partnering with industry organizations to help promote their events and becoming media sponsors. This issue of *Chip Scale Review* will be blanketing ECTC 2011, May 31-June 2 in Orlando, Florida, as CSR is for the first time, the official media sponsor for that event. *Chip Scale Review* staff will also be bouncing around the sessions and exhibits — so you may find your photo or some words about your company showing up in the July - August issue (you can read all about it while you're sitting at your exhibit at SEMICON West.) See you out there!

*Kim Newman*

Publisher

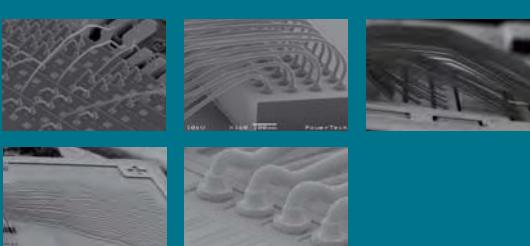
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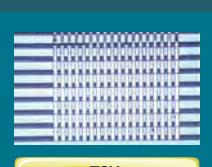
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# EDITOR'S OUTLOOK



## Getting the Cooling to Where it's Needed

By Ron Edgar [Technical Editor, *Chip Scale Review*]

Not long before the demise of Digital Equipment Corporation (DEC), they spent a fortune developing an ill-fated water-cooled system, Aquarius. The loss, reputed to be in the order of \$2B, no doubt contributed to their fall. However, it highlighted the well-known fact that one of the most serious problems facing system designers, and especially chip designers, is the reality of handling heat production. All but the most exotic of hardware has been, until recently, air cooled. Now, even my computer is water cooled. But standard techniques are not enough for tomorrow's needs — they are not getting close enough to dissipate heat where it is produced. Hot spots are part of the problem, 3D stacking is another. Clock rates continue to climb and higher levels of integration are contemplated. So what are we doing about it?

IBM has been getting a lot of press coverage on their efforts to improve cooling. Back in '09, they announced their Aquasar hot-water-cooled supercomputer. This joint IBM and ETH Zurich venture cooled the processors with warm water and extracted the surplus heat with heat exchangers. The harvested heat was then used to heat the building, reducing overall power consumption. At CeBIT 2011 in Hanover, Germany, IBM talked about their program and their test chips — 3D stacks with cooling channels between layers.

CMOSAIC is a four-year project between IBM Research, ETH Zurich, and École Polytechnique Federale de Lausanne (EPFL), which examines cooling techniques needed to support 3D chip architectures. Says Professor John Thome, CMOSAIC project coordinator,

"The CMOSAIC project is a genuine opportunity to contribute to the realisation of arguably the most complicated system that mankind has ever assembled: a 3D stack of computer chips with a functionality per unit volume that nearly parallels the functional density of a human brain."

Cooling between the layers is not the only way to go. In a paper (Bakir MS, Huang G, Sekar D, King C. 3D Integrated Circuits: Liquid Cooling and Power Delivery. IETE Tech Rev 2009;26:407-16) authored by researchers at Georgia Institute of Technology, Intel, and SanDisk, they discussed fluidic through-silicon vias (F-TSVs), which circulates fluid through the stack using special TSVs. This paper characterized their approach as, "Unlike prior work on microfluidic cooling of ICs that require millimeter-sized and bulky fluidic inlets/outlets to the microchannel heat sink, the proposed micropipe I/Os are microscale, wafer-level batch fabricated, area-array distributed, flip-chip compatible and mechanically compliant." Read the full article at <http://tr.ietejournals.org/text.asp?2009/26/6/407/57826>.

In a recent article in Journal of Low Power Electronics, Vol. 7, 1-12, 2011, Cyber-Physical Thermal Management of 3D Multi-Core Cache-Processor System with Microfluidic Cooling, Qian et al. not only used microfluidic channels, but coupled this with "a thermal management that can actively control the flow-rate of microfluidic channels to maintain the system temperature within certain temperature range." By dynamically changing the flow rate to different parts of the system according to predictive

software, it "... attains a more even temperature distribution with lower pumping power overhead. The total flow-rate, which is a direct reflection of pumping power, has been reduced by up to 72.1% with a fine grained flow-rate control." Yes, another outstanding read.

There are many other areas being looked at to help with heat removal. One such is the concept of very thin, liquid-cooled heat sinks. This would allow board pitch to shrink. Another is in the area of thermal interface materials (TIMs). Because TIMs account for up to 50% of the thermal resistance, there is keen interest in this area. Hierarchical nested surface channels (HNCs) need to be optimized and are a tradeoff between reduced bondline thickness and increasing resistance with smaller HNC cell sizes. For 3D stacks, underfill was originally used to reduce mechanical stress. Now, thermal properties are also important. Epoxy containing dielectric particles such as  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$ , conventionally applied by capillary forces result in poor thermal properties, typically worse than most TIMs. However, a technique called sequential underfilling filters the underfill as it exits the stack and loads the space between the dice with much more dielectric material than the conventional method. This allows much better thermal flow by putting the particles in closer contact with the dice and each other.

Much of the material here comes from IBM — thank you. And what are others doing? Lots! Intel, AMD, and a host of research facilities are hard at work hoping to keep Moore's Law alive by getting the cooling to where it's needed. ☺



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# GUEST EDITORIAL

## 3D: Progressing Past the Powerpoint

By Françoise von Trapp, Contributing Editor [*3D InCites*]

We've been hearing it a lot in the past year: when will 3D through silicon via (TSV) stacking move past the powerpoint to actual production? The implication that 3D integration using TSVs looks good in theory, but won't ever make it to market adoption has been one of the ongoing debated topics. But it's been a valid concern. As many reasons as there are to move to 3D integration, there have historically been just as many arguments against it. Mostly, I'm compelled to surround myself with fellow Kool-aid drinkers; those of us who see the elegance and beauty in the 3D solution and don't want to see the roadblocks because they're merely nuisances to those of us who truly believe. 3D just makes sense, and sooner or later everyone's going to have to see what we see. And then those darn realists poke pins in that bubble. It costs too much; there's too much needed to motivate the changes to the existing infrastructure; it doesn't matter if it WORKS, it will sit on the shelf forever until there's just no other way to do it. In my darkest moments of pure skepticism, I've even voiced my theory that there are those high-level decision makers in the industry who prefer to coast along to their retirement with existing technologies rather than rock the boat with something disruptive.

But in the past few months, things are happening. The pessimists are coming around. They're willing to take the first step towards adoption in the form of 2.5D silicon interposer technologies (**Figure 1**). The 3D

evangelists are also coming to the same conclusions; they know their time will come and at least 2.5D is a step in the right dimension (pun intended). And suddenly, we're there; moving beyond the powerpoint presentations to what Jan Vardaman, president and CEO of TechSearch International called "real engineering work." She talked about this progress in her presentation at the IMAPS Global Business Council, March 8, 2011. Vardaman pointed to progress in design tool developments; process improvements such as via fill, wafer thinning and handling, and singulation; new inspection and failure analysis technology; reliability data; and standards establishment. Still needing work is design software, thermal management, test, and reliability data.

### The Killer "Killer App"

It's well known that MEMS and CMOS image sensors (CIS) opened the manufacturing door for via-last TSVs — the first applications for TSVs in 2.5D. For a while it was thought that DRAM memory stacks would be the next step in realizing 3D IC stacks with TSVs. Samsung and Elpida both announced prototypes and Elpida went so far as to suggest production dates. Those well-known images became part of every 3D powerpoint as proof of 3D ICs potential. It was expected that memory on logic stacks would follow. And then somehow, the memory+logic application leapfrogged past DRAM as wide I/O DRAM on Logic was announced as the "killer app" for 3D IC.

At the GSA Memory Conference: 3D Architecture with Logic & Memory Integrated Solutions, March 31, 2011, I asked the experts why; what happened to DRAM being the next "killer app" despite all the roadmap declarations? According to Dr. John Lau, Fellow of Industrial Technology Research Institute (ITRI) everyone predicted that DRAM TSV stacks would happen before passive silicon interposers. "But everyone was WRONG! Passive interposers will be in production before the memory chip," He noted. "Whoever published that roadmap was 99% wrong." He noted that since Elpida made its announcements, nothing has shipped. Moreover, he said Elpida didn't even have a pilot line for stacking memory chips. Cost, he says, is always most important.

Kyowin Jin VP, Product Planning, Worldwide Marketing & Sales, Hynix Semiconductor, Inc. explained further that while using TSVs in DRAM memory is motivated by the technology benefits rather than cost, the benefits to DRAM stacks alone are not compelling enough. However, when you add in the benefits of stacking that DRAM cube on a logic stack, it becomes a worthwhile value proposition. Improving yield of "logic + stacked DRAM combined" becomes more important than improving "DRAM only yield", he explained. According to Yuan Xie, Pennsylvania State University, for 3D IC to be adopted, it has to both enable novel architectures as well as identify a killer app. 3D IC enables novel architectures such as latency (fast interlayer interconnect), bandwidth (high number of connections between layers), heterogeneous integration, and a cost benefit. "Killer apps" include high-capacity memory, multi/many-core processors, and exascale computing. Specifically, Xie noted that wide I/O DRAM demonstrates the bandwidth benefits of 3D for future quad High-Definition TV (HDTV) applications.

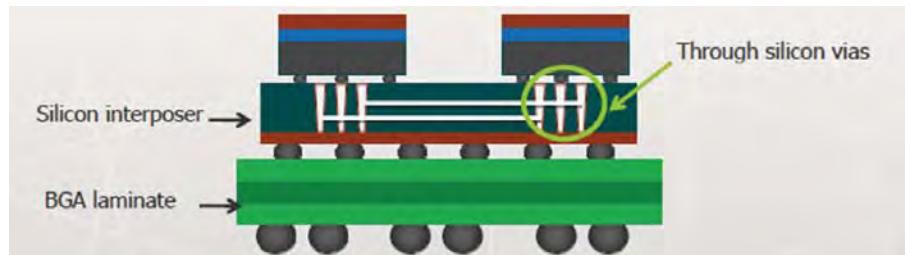


Figure 1. 2.5D-IC moves existing chips and design methodologies into the third dimension with interposers or flip chips. (Source: Mentor Graphics)

## What's Now and What's Next

Supporters of Si interposer technology have been voicing the benefits of 2.5D for quite some time, but it wasn't until Xilinx introduced its stacked silicon technology about six months ago that technologists began talking about it as not an alternative but a first step towards achieving full 3D. Lau differentiates between 3D silicon integration and 3D IC Integrations. 3D Si integration is the furthest away from market adoption, and involves very high aspect ratio TSVs in ultra thin wafers without bumping. He divides 3D IC integration into 3D TSV memory stacks, active interposers for stacking DRAM on logic, and passive interposers in 2.5 and 3D configurations. Due to its ability to leverage existing infrastructure, Lau predicts that passive interposer technology will be used the most in the next ten years while the kinks are worked out of "true" 3D IC integration. Active interposers with TSVs need an ecosystem, EDA tools and business models. Ultimately, the way to go to compete with Moore's law will be 3D SI integration (**Figure 2**), and that the industry should strike to make this happen. Realistically, we're looking at 10 years before it's in production. 

## Conclusion

Signs of movement beyond the powerpoint are everywhere. Foundries and packaging houses are gearing up to add what has been dubbed "mid-end" processes for silicon interposer and 3D processes. Amkor has been working with Xilinx and TSMC to assemble its stacked silicon FPGA. ASE is also promoting its 2.5D processes. On April 11 2011, TSMC threw its hat in

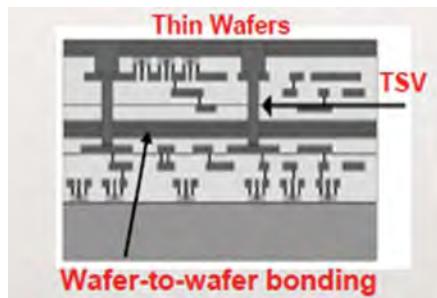


Figure 2. 3D si integration involves very short wiring with TSVs between bonded ultrathin wafers without bumps. (Source: ITRI)

the mid-end process ring, announcing it would expand its wafer bumping and wafer level packaging offerings, and begin focusing on silicon interposer processes. On April 19, 2011, STATS ChipPAC announced the addition of a 300mm "mid-end" process flow to support the advanced

manufacturing requirements of 2.5D and 3D TSV as well as wafer level packaging, flip chip and embedded die technology. Before we know it, these technologies will be referenced in powerpoints only for historical reference. In its place, look for developments of 3D Si integration. 

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# INDUSTRY NEWS

## IHS iSuppli Ranks Semiconductor Suppliers; Samsung closing in on Intel

In its recently released market research report for 2010, IHS iSuppli reports that the #2 ranked semiconductor manufacturer, Samsung, is closing the gap between it and Intel with a 9.2% market share of global chip revenue, up from 7.6% in 2009. This puts the company only 4.1 percentage points behind Intel. Even more interesting is the shift for companies like Renesas, Micron and Broadcom, who leapt several places ahead to put them in the top 10 at 5, 8, and 10 respectively. ST Microelectronics slipped back from 5th to 7th place, and Qualcomm also dropped back from 6th to 9th place. The most dramatic increase of revenue was Renesas, with a 130% increase from \$5153 to \$11,893.

"The rise of Samsung is one of the biggest stories of the last decade in the worldwide semiconductor market," said IHS analyst Dale Ford. "When experts discuss competition for Intel, they almost always focus on Advanced Micro Devices Inc. (AMD). While it is true that AMD is Intel's major competitor in the microprocessing unit (MPU) market, Samsung is the primary rival of Intel for overall semiconductor market share. And although they are mainly indirect competitors in the marketplace, Intel and Samsung have been ranked No. 1 and No. 2, respectively, for a number of years." In 2001 Intel's market share at 14.9% was more than three times that of Samsung at 3.9%; Samsung ranked fifth then.

IHS iSuppli analysts attribute Samsung's growth to the surging IC memory market and its position as the top supplier of DRAM and NAND. Additionally, The memory boom has also moved other major memory suppliers up the market share rankings and charts. Micron Technology, Hynix Semiconductor and Elpida Memory expanded their share of the total market by 1.1%, 0.7% and 0.4%, respectively.

Renesas' impressive rise in revenue was largely due to its merger with NEC

2009 Rank	2010 Rank	Company Name	2009 Revenue	2010 Revenue	Percent Change	Percent of Total	Cumulative Percent
1	1	Intel	32,187	40,394	25.5%	13.3%	13.3%
2	2	Samsung Electronics	17,496	27,834	59.1%	9.2%	22.4%
3	3	Toshiba	10,319	13,010	26.1%	4.3%	26.7%
4	4	Texas Instruments	9,671	12,994	34.4%	4.3%	31.0%
9	5	Renesas Electronics Corp.	5,153	11,893	130.8%	3.9%	34.9%
7	6	Hynix	6,246	10,380	66.2%	3.4%	38.3%
5	7	STMicroelectronics	8,510	10,346	21.6%	3.4%	41.7%
13	8	Micron Technology	4,293	8,876	106.8%	2.9%	44.6%
6	9	Qualcomm	6,409	7,204	12.4%	2.4%	47.0%
14	10	Broadcom	4,278	6,682	56.2%	2.2%	49.2%
15	11	Elpida Memory	3,948	6,446	63.3%	2.1%	51.3%
8	12	Advanced Micro Devices	5,207	6,345	21.9%	2.1%	53.4%
11	13	Infineon Technologies	4,456	6,319	41.8%	2.1%	55.5%
10	14	Sony	4,468	5,224	16.9%	1.7%	57.2%
18	15	Panasonic Corporation	3,243	4,946	52.5%	1.6%	58.8%
17	16	Freescale Semiconductor	3,402	4,357	28.1%	1.4%	60.3%
19	17	NXP	3,240	4,028	24.3%	1.3%	61.6%
23	18	Marvell Technology Group	2,572	3,633	41.3%	1.2%	62.8%
16	19	MediaTek	3,551	3,553	0.1%	1.2%	64.0%
20	20	nVidia	2,826	3,196	13.1%	1.1%	65.0%
21	21	ROHM Semiconductor	2,586	3,118	20.6%	1.0%	66.0%
22	22	Fujitsu Semiconductor Ltd.	2,574	3,090	20.0%	1.0%	67.0%
24	23	Analog Devices	2,091	2,862	36.9%	0.9%	68.0%
30	24	Maxim Integrated Products	1,657	2,367	42.8%	0.8%	68.8%
29	25	Xilinx	1,699	2,311	36.0%	0.8%	69.5%
		All Others	78,11	92,667	18.6%	30.5%	
		Total Semiconductor	230,194	304,075	32.1%	100.0%	

Table 1. IHS iSuppli Table: Final Worldwide Revenue Ranking for the Top-25 Semiconductor Suppliers in 2010 (Ranking by Revenue in Millions of U.S. Dollars)

Electronics. The two companies, which had combined revenues in 2009 of \$9.5B, grew 24.7%, less than the overall market, to \$11.9B in 2010.

## Japanese Earthquake Hits Supply of Cell Phone Image Sensors

According to market research company IHS iSuppli, the March 11 earthquake in Japan is impacting the production of CMOS image sensors (CIS) at Toshiba's Iwate image sensor fab, which was shut down, as well as delaying delivery of CIS from Sony to cell phone OEMs. Together, the companies accounted for 19.2% of the 2010 global handset digital camera image sensor revenue.

"With their low cost and easy integration with other electronics, CMOS has long been the technology of choice for cell phone cameras," said Pamela Tufegdzic, analyst for consumer electronics at IHS. "The Japan earthquake and subsequent logistical challenges have

disrupted a portion of the supply of this key component."

While CIS production and distribution has been impacted, supplies of the major alternative image sensor technology — CCDs — appear to be unaffected in the near term. Because of their higher image quality, CCDs are commonly used in digital still cameras. In contrast, CIS are predominately used in cell phones and often in other devices where the camera is secondary to other functions. The global CCD market is dominated by Japanese suppliers including Sony, Panasonic Corp., Fujifilm, Sharp Corp. and Toshiba.

## CEA-Leti to Implement Multiple EV Group Systems on its 300mm 3D Line

CEA-Leti has installed multiple EVG tools in its 300mm cleanroom dedicated to R&D and prototyping for 3D integration applications. Although this state-of-the-art facility is focused on R&D and prototyping, EVG's equipment will



Figure 1. EVG850 production bonding system for direct wafer bonding installed in Leti's 300mm 3D line (Courtesy of Leti)

reportedly be used in 3D technology demonstrations for Leti's global customer base, as well as low-volume pilot production on 300mm wafers with the end goal of transferring the processes to their industrial partners' high-volume manufacturing environments.

The EVG systems to be deployed on CEA-Leti's new 300mm 3D line include an IQ Aligner production mask alignment system, a SmartView NT highest precision bond alignment system, an EVG560 production wafer bonding system and an EVG850 production bonding system for direct wafer bonding (**Figure 1**). CEA-Leti intends to tap EVG's process know-how in 3D integration and through-silicon via (TSV) manufacturing, as the institute's 3D offerings include TSVs along with advanced capabilities in alignment, bonding, thinning and interconnects.

"These new tools offer important new capabilities to Leti and our partners," noted CEA-Leti CEO Laurent Malier. "Together we will demonstrate 3D and heterogeneous integration technologies on 300mm wafers."

### SEMI CEO and President, Stan Myers, to Step Down from Executive Leadership

SEMI has announced the impending retirement of CEO Stanley T. Myers, who has informed the SEMI International Board of Directors of his intention to step back from executive leadership this year. Myers has participated for more than 50 years in the semiconductor industry, including 24 years as a SEMI



board member, 15 years as president and CEO of the association, as well as chairman of the SEMI International Board in 1994.

"Stan is a driving force at the helm of our industry association," said Rick Wallace, CEO of KLA-Tencor Corporation and Chairman of SEMI's BOD. "Under his leadership, SEMI has grown and diversified to meet the changing needs of member companies that participate in one of the world's most complex and sophisticated high-tech industries. As Stan anticipates the next chapter of his life, we appreciate his thoughtful and deliberate framework for a succession plan."

In consideration of Myers' announcement, Wallace appointed a Board search committee to evaluate candidate successors for the role that Myers will be vacating. Tim O'Shea, with the executive search firm Heidrick & Struggles, will conduct the search for SEMI. Myers plans to continue supporting the association when a new president and CEO is named.

### Crane Aerospace & Electronics appoints John P DiStasio, Senior Director of Business Development, Microwave Solutions

Crane Aerospace & Electronics announced the appointment of John P. DiStasio, Senior Director of Business Development for Electronics Group Microwave Solutions. DiStasio will lead the Microwave Solutions business development team, which includes

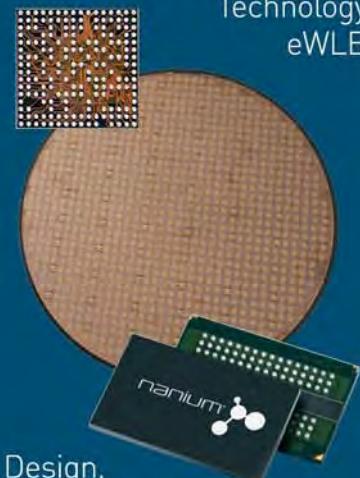
sites in Beverly, MA; Chandler, AZ; West Caldwell, NJ; and San Jose, Costa Rica. Prior to his appointment, DiStasio held the position of Director of Field Sales at Cobham — M/A-COM, managing the worldwide field sales organization. DiStasio holds a BS in Electrical Engineering from Northeastern University.



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# Partnering to Enable Volume Manufacturing for 3D IC Stacks with TSVs

**Collaboration between suppliers and semiconductor manufacturers is vital to help ensure that cost-effective processes are built into the R&D effort at the beginning.**

By Sitaram Arkalgud, Director of 3D Interconnect [[SEMATECH](#)]

**3**D through silicon via (TSV) technology offers the benefits of functionality/performance enhancement and power/cost reduction for future semiconductor products. However, it demonstrates a classic example of the entry-level hurdles facing the introduction of a new technology. TSV is not a single technology element but spans all aspects of the industry. To successfully enter high volume manufacturing (HVM), it requires broad collaboration among IDMs, equipment and materials suppliers, fabless and fab-lite manufacturers, and test, packaging and assembly companies. To address the various implementation scenarios for 3D TSV, leading-edge processes, integration approaches, metrology technologies, and tool sets must be developed to deliver cost-effective 3D interconnect processes.

SEMATECH traditionally focuses on developing materials and equipment solutions to reduce cost-of-ownership (CoO). This is accomplished by working to extend current technologies as long as possible and by preparing for transitions to next-generation technology. Its track record in preparing new technologies for manufacturing include the industry's 300mm wafer size transition, 193nm immersion, and high-*k* and low-*k* materials. SEMATECH's TSV research and development is the successor to almost ten years of work the consortium has undertaken to develop robust copper/low-*k* interconnect technology. SEMATECH's program on 3D integration focuses on a via-mid approach, with Cu—Cu bonding covering both die-to-wafer (D2W) and wafer-to-wafer (W2W) integrations. It partners with leading-edge equipment and materials suppliers and leverages their

expertise to deliver innovative, manufacturable process solutions.

Although SEMATECH has significantly broadened its charter to explore cutting-edge technologies and future-oriented manufacturing strategies, its approach to R&D is still rooted in the twin legacy of pulling important university research into the commercialization pipeline and working with equipment and materials suppliers to ensure that the solutions it develops are both manufacturable and affordable.

Today, especially given the increasing role suppliers are playing in technology development for the industry, SEMATECH encourages a new level of partnership in which suppliers join as program members in areas of specific expertise and interest, share ideas and resources, and take advantage of expanded opportunities to develop and test their tools and materials. Specifically, with new equipment and materials suppliers now on board in its 3D interconnect program, including NEXX Systems, Atotech, Tokyo Electron Ltd., and Lasertec, SEMATECH researchers are able to work on early development challenges including cost modeling, technology option narrowing, and technology development and benchmarking, while also building industry consensus on 3D.

## 3D Infrastructure Value Chain

3D infrastructure and supply chain readiness is the biggest concern for the broad adoption of 3D ICs. A primary concern is that the traditional front-end and assembly roles are being questioned, resulting in questions regarding ownership, liability, and value proposition. In addition, there are various strategic technology choices and different process steps that need to be determined before the implementation of 3D TSV interconnects is realized.

These include a lack of electronic design automation (EDA) tools, the need for cost-effective manufacturing equipment and processes, insufficient yield and reliability data involving thermal issues, electromigration and thermo-mechanical reliability, and compounded yield losses. Given the disruptive nature of TSVs, its successful implementation will require an unprecedented level of cooperation within the supply chain.

Issues that have restricted 3D interconnects from entering HVM encompass the front-end, assembly and packaging, and design and test. Timely availability of advanced equipment is a key enabler of 3D development. SEMATECH is working jointly with chipmakers, equipment and materials suppliers, and universities on device interactions for fabrication at the 65nm node for planar and future scaling to 30nm for planar and non-planar CMOS technologies. The result is a proven 3D TSV infrastructure from materials through integration.

A major supply chain question is where in the production line will TSVs be created—as part of wafer fabrication, or at the end, as part of packaging? The answer affects both via processes and via locations. It also determines who in the supply chain does the job, wafer suppliers or packaging houses. Partnering with suppliers has allowed SEMATECH to address these and other industry concerns. For example, SEMATECH has made considerable investment in a complete 300mm 3D IC pilot line, with capabilities in equipment, processing, and metrology to advance 3D integration technologies. SEMATECH members are now able to evaluate tools, process modules, and even integration sequences within a state-of-the-art CMOS environment.

One of the keys to fabricating many 3D chip structures is the development of high-yield, low-cost copper electroplating solutions that will enable high-density 3D TSVs. The technology of copper electroplating provides a void-free fill for all feature sizes while minimizing interconnect overburden and topography at the same time. There is a variety of products that may have different optimal fill conditions and working with suppliers can help researchers eliminate the various challenges associated with cost, new materials, and technical questions such as copper pumping and overall reliability.

### Tool Partners

NEXX Systems, which manufacturers process equipment for advanced wafer-level packaging (WLP), collaborates with SEMATECH on innovative electrodeposition technology in the area of advanced WLP items and their participation in SEMATECH's 3D program provides valuable expertise on developing robust, low-cost electroplating solutions. One advantage of the NEXX platform is the versatility of

the tool, which allows the investigation of various methods and chemistries to achieve a reliable, consistent electrochemical deposition for wafer plating. Furthermore, the NEXX Stratus system (**Figure 1**) commonly used in the packaging arena, is now being developed as a tool suitable for front-end cleanrooms. The inset (of **Figure 1**) shows the cross-section of copper filled TSVs plated using the NEXX Stratus.

As a market leader in PCB and IC substrates industries, Atotech's participation in SEMATECH's 3D program has been very valuable for SEMATECH engineers as they develop process technologies for both D2W and W2W 3D applications. Atotech contributes to the R&D with cost-competitive, innovative chemistries and plating know-how. The partnership has provided cost-effective processes for industry-wide implementation of copper electroplating solutions to enable void-free bottom-up filling of high density 3D TSVs (**Figure 3**). Specifically, the electrical characterization data and early reliability data generated



**Figure 1.** The NEXX Stratus system commonly used in the packaging arena is now being developed as a tool suitable for front-end cleanrooms. Inset shows the cross-section of copper filled TSVs plated using the NEXX Stratus

for the experiments enable the R&D teams to analyze results and improve the process for best TSV performance.

In addition to via size and shape, researchers must consider different chemistries to form the vias potentially requiring new etch chemistries. As SEMATECH's first associate member of its 3D program, Tokyo Electron Limited (TEL) has provided their experience in deep silicon etching. TEL's 300 mm Telius™ SP UD, the latest generation TSV etch tool, has allowed SEMATECH researchers to investigate various

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Figure 2. Tokyo Electron's Telius™ SP UD, and inset shows the details of a 5x50 micron TSV

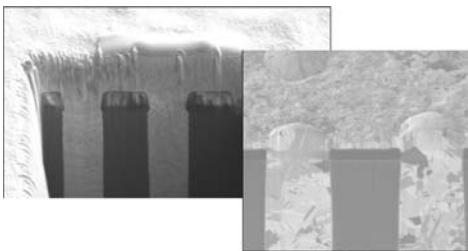


Figure 3. Atotech's and SEMATECH's partnership enables cost-effective processes for industry-wide implementation of copper electroplating solutions to enable void-free bottom-up filling of high density 3D through-silicon-vias (TSVs)

chemistries to etch vias ranging from sub 1 $\mu\text{m}$  to > 10 $\mu\text{m}$  in diameter, using a non-Bosch etch. Furthermore, the integration of TEL's 3D tools has enabled SEMATECH to explore different etch chemistries and develop an optimized etch process for TSVs. **Figure 2** shows Tokyo Electron's Telius™ SP UD, and inset shows the cross section of a 5x50 $\mu\text{m}$  TSV.

The partnership is a twofold benefit — refining TSV etch development processes and providing useful data to SEMATECH members as well as TEL's customers, and has expanded from TSV etch development to developing new technologies used elsewhere in TSV processing.

To effectively explore innovative metrology capabilities that will make 3D TSVs commercially viable, researchers from SEMATECH are exploring 3D metrology techniques to complement bonding tool development. The key steps towards bridging high-volume manufacturing readiness gaps for an integrated 3D TSV tool platform and developing metrology techniques that will accelerate adoption of 3D integration is to partner with suppliers who help develop robust, cost-effective process metrology solutions.

In 2010, Lasertec joined SEMATECH to further investigate and compare 3D TSV depth metrology schemes—critical work necessary not only for TSV RIE process control, but also for providing critical feed forward data for wafer thinning and TSV expose processes.

To facilitate this work, Lasertec placed a 300mm TSV infrared (IR) etch metrology tool (**Figure 4**) in SEMATECH's 3D R&D center, providing advanced measurement capabilities that have enabled accurate, repeatable TSV depth measurements over a range of TSV dimensions (**Figure 5**).

## Standards

Although supplier engagement is important to deliver 3D TSV solutions for HVM, bringing in all players from across the entire industry—fabless, fab-lite and IDM companies, outsourced assembly and test suppliers, and tool vendors—is equally important to drive industry consensus on integration approaches, process architectures, tool sets, creating a roadmap, and for standards.

3D must accommodate the wide range of process parameters demanded by competing companies trying to establish their own proprietary process flows. Standards will be needed to ensure common interfaces from different suppliers. Heterogeneous stacking will require integrating processes from different manufacturers.

SEMATECH is playing a strategic role in working with the industry to drive manufacturability and forge consensus on technology options, standards, and cost modeling. SEMATECH, the SIA, and SRC established the 3D Enablement Center targeting standards in inspection, metrology, microbumping, bonding, and thin wafer and die handling.

The center aims to solve key industry infrastructure gaps including developing uniform standards and a better understanding of key manufacturing parameters, which would identify the key areas for developing design tools to be transitioned to mainstream high-volume production.

## Conclusion

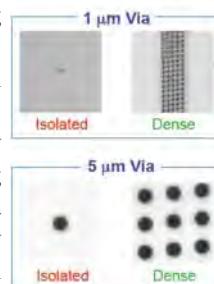
The technology roadmap requires intense collaboration throughout the industry supply chain. Design enablement companies, equipment and materials suppliers, fabless, fab-lite, and assembly and packaging companies must join with vertically integrated chipmakers to develop system-wide solutions.

Since 3D TSVs are destined to play such a significant role in the products that apply them, partnering with the right supplier can make the difference between success and obsolescence. The benefit with the SEMATECH/supplier partnerships is having ready and early access to advanced technology and the expertise in material research, design, bonding, packaging and testing. The result is a proven 3D TSV infrastructure from design to tested package and the key to building the products that shape the market.



Figure 4. Lasertec's WASVI series TSV300-IR provides advanced measurement capabilities that have enabled accurate, repeatable TSV depth measurements over a range of TSV dimensions

## Static repeatability



Achieved a good repeatability for high aspect ratio via of 1 $\mu\text{m}$  and 5 $\mu\text{m}$ .  
Figure 5. The data in the graph above, from Lasertec's WASVI TSV300-IR tool, shows the repeatability of depth measurements made on 1 and 5 micron wide, dense and isolated TSVs

# Chip-Level Spot Cooling

By Kaveh Azar, Ph.D. [Advanced Thermal Solutions, Inc.]

**A**s device densities and clock frequencies continue to increase, the switching currents carried by the power and ground networks increase as well, leading to a power density increase. This increase, along with the lower power supply voltages and thinner wires, can adversely affect the robustness of an IC. Power distribution systems are designed to provide needed voltages and currents to the transistors that perform the logic functions of a chip. The supply voltages are assumed to be constant across a chip, and are expected to operate reliably over the chip's lifetime. The complexity of power distribution systems and their subsequent spot heating have a significant impact on chip performance. If IC designers do not consider such matters, they will have a difficult time producing a robust system since the chip may fail in the field after it is embedded in a system.

This issue is acutely highlighted by the International Technology Roadmap for Semiconductors (ITRS). **Table 1** shows their predicted trends in electronics packaging for the coming years.

As observed by Lin, et al., the projected allowable maximum power density (shown in **Table 1**) is approaching

Year of Production	2013	2016	2019
Supply Voltage (V)	0.9	0.8	0.7
<sup>1</sup> Transistor (M)	4424	8848	17696
<sup>2</sup> Size (mm <sup>2</sup> )	310	310	310
<sup>3</sup> Lg (nm)	13	9	6
<sup>4</sup> I <sub>d,sat</sub> (uA/um)	2220	2713	2744
<sup>5</sup> I <sub>sd</sub> , leakage (uA/um)	0.11	0.11	0.11
<sup>6</sup> Intrinsic Delay, $\tau$ (ps)	0.25	0.15	0.10
<sup>7</sup> Switching Energy (fJ)	0.0198	0.0091	0.0036
<sup>8</sup> Max. P.D.(W/cm <sup>2</sup> )	63.87	63.87	63.87

**Table 1.** High Performance Double Gate Logic Technology Trend Targets. [1]

<sup>1</sup>Functions per chip at production (million transistors)

<sup>2</sup>Chip size at production (mm<sup>2</sup>)

<sup>3</sup>Physical gate length (nm)

<sup>4</sup>Effective saturation drive current (uA/um)

<sup>5</sup>Source/drain sub-threshold off-state leakage current (uA/um)

<sup>6</sup>Intrinsic transistor delay for NMOS devices at 25°C (ps)

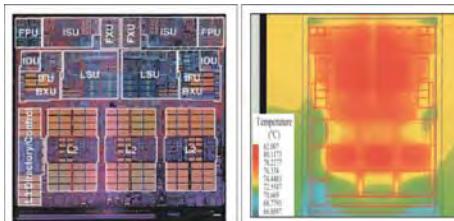
<sup>7</sup>Energy per device switching transition with dimensions W/Lg=3 (fJ/device)

<sup>8</sup>Maximum allowable average power density (W/cm<sup>2</sup>)

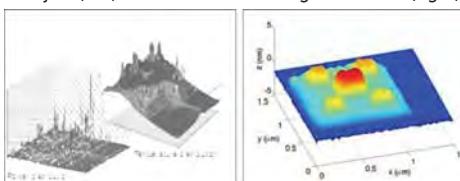
saturation in the next few years due to the limited capability for system level heat removal.<sup>1</sup> While increasing the chip size can reduce the overall heat flux, the desire to place more circuitry on the same silicon will negate the notion of a larger chip. As noted by Taur, thermal problems are amplified because the leakage current (power at the transistor level) forms the major portion of the total power dissipated by the chip.<sup>3</sup> Seeing as this leakage is undesirable from the thermal standpoint, it has become the primary factor in limiting the scaling of CMOS devices.

Due to the increase in power dissipation across chips, local hot spots have become a challenge for device designers and thermal engineers. From the combination of small device features and passage of electrical current in such locations, local heat flux densities have risen dramatically while posing a significant challenge for cooling thermal spikes on the chip. **Figure 1** shows one such effect where there is significant power and subsequently temperature distribution on the chip.<sup>4</sup>

The power profile over the chip has peaks and valleys. The peaks represent the highest power concentration (largest heat flux, W/mm<sup>2</sup>) and highest



**Figure 1.** Map of FET Junction Temperature for a 115 W Packaged Power 4 Chip Derived from Chip Power Analysis (left) and Thermal Modeling Simulation (right).<sup>4</sup>



**Figure 2.** Power and Temperature Distributions at the CPU Junction.<sup>5</sup>

temperature levels on the chip. This is depicted in **Figure 2** for a CPU. These peaks have a proportionally higher temperature than the rest of the chip and represent the potential for a chip's malfunction or its catastrophic failure. Once we translate this to a PCB, some of the components are of high to average power and some are of low to average power. Consequently, the PCB has the same power and thermal response as the chips on the components forming the PCB. This impacts the thermal response of the components residing on it, i.e., change of boundary conditions. The thermal management at both levels of packaging: chip (component) and PCB are huge bottlenecks in the successful launch of an application. They become even more prevalent as the heat flux density increases.

Despite significant advances in component packaging and material design, the industry continues to struggle with this issue. The solution for the spot cooling has two broad forms — at the silicon level and at the packaging level.

## Silicon Level

Many solutions have been explored at the silicon level. Among these is the deployment of micro-channel heat exchangers (MCHEs), thin-film thermo electric coolers (TECs), micro heat pipes, and localized copper bumps to improve heat spreading on a larger surface area, or in the case of an MCHE, transporting it to a different location. **Figure 3** shows a stacked MCHE that is used for cooling a silicon substrate.

The success of these techniques (except for a handful of highly customized applications, such as larger scale computers) has been weak and unsatisfactory. TECs, bumps, micro heat pipes, etc, have had moderate success in dampening the peaks observed as a result of the power density variation. Often, because of the aspect ratio or the area, the heat flux exceeds 400-500 W/

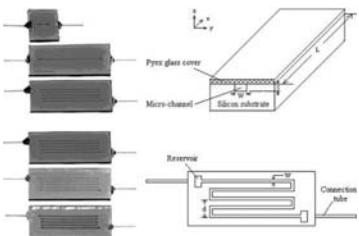


Figure 3. Stacked Micro-Channel Heat Exchanger for Substrate Cooling.<sup>6</sup>

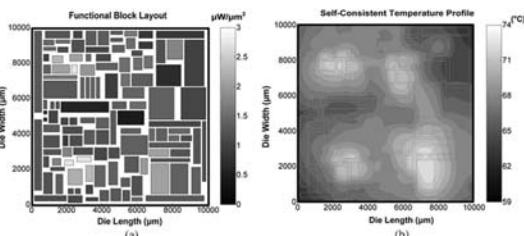


Figure 4. Block Diagram and the Topical Temperature Measurement of a 10 x 10 mm Test Chip, respectively.<sup>12</sup>

cm<sup>2</sup>. In some high-power applications, it exceeds 1-2 kW/cm<sup>2</sup>. With such high heat fluxes, one can appreciate the limits of the aforementioned technologies.

A notable approach to this problem has been the electrical control of the chip. Dynamic thermal management(DTM) has been examined as a technique for controlling CPU power dissipation. DTM refers to a range of possible hardware and software strategies that work dynamically, at run-time, to control a chip's operating temperature.<sup>7</sup>

Traditionally, the packaging and fans for a CPU or computer system are designed to maintain a safe operating temperature even when the chip is dissipating the maximum power possible for a sustained period of time, and therefore generating the highest amount of thermal energy. This worst-case thermal scenario is highly unlikely, however, and thus such worst-case packaging is often expensive overkill. DTM allows packaging engineers to design systems for a target sustained thermal value that is much closer to average-case for-real benchmarks. If a particular workload operates above this point for sustained periods, a DTM response will work to reduce chip temperature. In essence, DTM allows designers to focus on average thermal conditions in their designs, rather than worst-case conditions.

The key goals of DTM can be stated as follows:

1. to provide inexpensive hardware or software responses,
2. to reliably reduce power and,
3. to impact performance as little as possible.

To better understand the process, the maximum power dissipation occurs when all of the structures within the processor are active with maximum switching activity. In reality, the maximum power

dissipation is constrained by the software program that can maximize the usage and switching activity of the hardware. Special max-power benchmarks can be written to maximize the switching activity of the processor. These benchmarks are often quite esoteric, perform no meaningful computation, and dissipate higher power than 'real' programs. Thus, DTM techniques could be used solely to target power levels seen in maximum power benchmarks and would rarely be invoked during the course of typical applications.<sup>8</sup>

### Package Level

At the package level, cooling solutions can be applied to the top of the silicon, or alternatively the component is immersed in some sort of heat transfer fluid. The goal of these approaches is to rapidly remove the heat from the device or to provide a medium that can effectively absorb the thermal peaks by improved thermal spreading. A number of techniques have been explored by many researchers in the field with varied success.<sup>9</sup> **Table 2** presents such techniques and their respective characteristics.

Technology	Advantages	Disadvantages
Fan sinks with heat pipe (hybrid)	Compact, versatile	Reliability, space, limited to ambient temperature
Thermoelectric	Spot cooling	Reliability, low capacity
Liquid cooling	High surface heat transfer	Sealing, cost, maintenance, packaging
Direct immersion	High capacity	Cost, sealing, packaging
Refrigeration	Sub-ambient	Cost, power, space, packaging
Cryogenics	Super cooling	Cost, power, packaging

Table 2. Thermal and Deployment Characteristics of Select Cooling Options.<sup>9</sup>

Other cooling solutions have been deployed or exist at university or company laboratories.<sup>10,11</sup> One paper by Lin and Banerjee demonstrates the impact of global and local cooling solutions applied to hot spots on dies specifically designed for such study.<sup>12</sup>

**Figures 4a** and **4b** show the functional block layout of a test chip showing the power density associated with each block. Nominal total power consumption is 90 W. **Figure 4b** shows four hot-spots on the topical substrate temperature profile of the test chip. In this case, the highest temperature is around 73 °C.

**Figures 5a** and **5b** show the topical substrate temperature profile of the test chip for global and spot cooling respectively. The substrate temperature profile shows several hot spots, and the highest junction temperature is around 73°C. Although the results shown here are specific to the aforementioned IC, the conclusions drawn are more generic.

**Figure 5** shows the effect of applying global and localized cooling strategies on hot spot management. As shown in **Figure 5a**, a lower junction-to-ambient thermal resistance ( $\theta_{ja}$ ) obtained by applying global cooling (through better interface material, higher cooling efficiency, etc.) reduces the maximum junction temperature. However, on-chip hot spots and thermal gradients still remain. On the other hand, localized cooling solutions such as local spray cooling and thin-film thermoelectric coolers can be applied to eliminate the hot spots. For example, if a thin-film thermoelectric cooler is placed on the backside of the wafer below the location of the bottom-right hot spot, it can effectively eliminate the targeted hot spot as shown in **Figure 5b**.

### Summary

The power profile over the chip has peaks and valleys. The peaks represent the highest power concentration (largest heat flux, W/mm<sup>2</sup>) and highest temperature levels on the chip. Thermal management of these hot spots has become a unique challenge for device designers and thermal engineers alike. Through the combination of smaller device features and the passage of

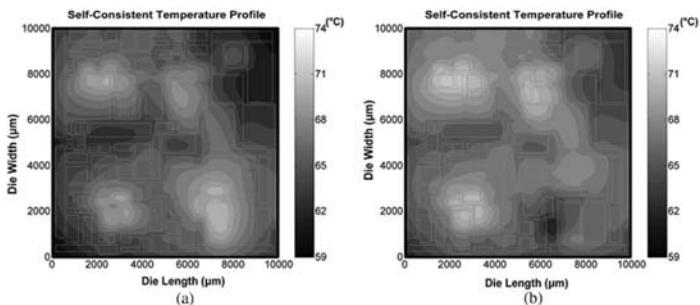


Figure 5. Topical Temperature Difference for Global (5a) and Spot Cooling (5b) of a 10 x 10 mm Test Chip.<sup>12</sup>

electrical current in such locations, local heat flux densities have risen dramatically. They pose a significant challenge for cooling thermal spikes on the chip.

It is clear that topical or spot approaches for the thermal management of these hot spots are not sufficient. To successfully develop such products, it is essential for thermal management and logic-flow to be considered concurrently, and for a system level approach to be taken.<sup>12</sup>

## References

1. International Technology Roadmap for Semiconductors (ITRS). [www.itrs.net](http://www.itrs.net).
2. Lin, S. and Banerjee, K., Cool Chips: Opportunities and Implications for Power and Thermal Management, IEEE Transactions On Electron Devices, Vol. 55, No. 1, January 2008.
3. Taur, Y., CMOS Design Near the Limit of Scaling, IBM J. Res. Develop., Vol. 46, No. 2/3, 2002.
4. Warnock, J., Keaty, J., Petrovick, J., Clabes, J., Kircher, C., Krauter, B., Restle, P., Zoric, B. and Anderson, C., The Circuit and Physical Design of the POWER4 Microprocessor, IBM Journal of Research and Development, Vol. 46, No. 1, 2002.
5. Wei, J., Thermal Management of Fujitsu's High-Performance Servers, Fujitsu Sci. Tech. J., 43, January 2007.
6. Web Reference: [http://plaza.ufl.edu/rxiong/research/STflow\\_files/micro-channels.JPG](http://plaza.ufl.edu/rxiong/research/STflow_files/micro-channels.JPG)
7. 8. Brooks, D. and Martonosi, M., Dynamic Thermal Management for High-Performance Microprocessors, Proceedings of the 7th International Symposium on High-Performance Computer Architecture, Monterrey, Mexico, January 2001.
9. Azar, K., Advanced Cooling Concepts and Their Challenges, Presented at the Int. Workshop Thermal Investigations ICs and Systems (THERMINIC), Madrid, Spain, 2002.
10. Rodgers, P., Eveloy, V., and Pecht, M., Limits of Air-Cooling: Status and Challenges, Proc. SEMI-THERM, 2005.
11. Prasher, R., Chang, J., Sauciuc, I., Narasimhan, S., Chau, D., Chrysler, G., Myers, A., Prstic, S., and Hu, C., Nano and Micro Technology-Based Next-Generation Package-Level Cooling Solutions, Intel Technol. J., Vol. 9, No. 4, November 2005.
12. Lin, S. and Banerjee, K., IEEE Transactions on Electron Devices, Vol. 55, No. 1, January 2008.

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# 3D Wafer Level Chip Scale Packaging: A Stepping Stone to Full 3D Integration

By Daniel F. Baldwin, Ph.D., Paul Houston, Brian Lewis, Tim Sparks, Fei Xie [ENGENT, Inc.]

**B**ack-end-of-line (BEOL) assembly involving 3D integration at the wafer level has received increasing exposure in electronics literature. Development efforts for 3D wafer-level integration are underway worldwide, with the promise that this elegant integration technique will enable a long-term solution to the industry's expanding computational power and memory requirements. In the short term, however, a need exists for achieving many of 3D integration's benefits without requiring a vertically integrated production infrastructure typically needed for the full 3D wafer-level integration solution.

For emerging applications, there is a 3D integration technology that provides many of the 3D wafer-level integration benefits and leverages existing high volume BEOL production infrastructure. An initial stepping stone for 3D integration is 3D die-to-wafer (D2W) or die-to-die (D2D) integration. 3D integration at the die level offers key features like very high levels of integration, very small form factor packages (often chip scale in size), very low profile packages, low weight packages, and improved digital and RF performance.

3D D2W integration can be achieved via face-to-face bonding of fine-pitch flip chip components and low-profile passives onto a redistribution layer of another silicon component - a wafer level chip scale package (WLCSP). In this manner, a flip chip driver can be mounted directly onto a CSP memory component, ASIC, etc. Wafer level packaging (WLP) provides a highly functional platform from which to implement a new package technology incorporating 3D D2W integration. Moreover, such a packaging architecture provides a cost-effective, rapid time-to-market alternative to emerging 3D wafer-level integration technologies.

This article summarizes this low-cost, 3D WLCSP technology that leverages the

existing infrastructures of WLP and high-volume flip chip assembly. It will briefly review 3D integration technologies, present implementation strategies for 3D die level integration packaging, and present examples of 3D die level integrated packaging solutions. Additionally, the assembly advancements associated with and implemented to produce the 3D face-to-face flip-chip-on-wafer (F2FFCoW) package will be explained.

## 3D Die Level Integration

3D die level integration is a device-level integration scheme wherein multiple layers of planar devices are stacked and interconnected in the Z-direction using various combinations of flip chip interconnect, direct die bonding, and through die vias. 3D die stacking is achieved by producing devices of a specific function (i.e., embedded processors, DSPs, SRAM, DRAM, embedded wireless networks, etc.) that are bonded together in singulated or tile form. Singulated known good die (KGD) are then vertically interconnected to create an integrated functional device.

3D die level integration represents a unique opportunity to gain the performance and form factor advantages of 3D wafer level integration without the drawbacks. 3D die level integration does not suffer from high yield loss due to good die being bonded to bad die during wafer integration, and does not require full-scale wafer processing. 3D wafer-level integration requires both, resulting in prohibitively high costs for integrated packaging solutions for high-performance applications. In these applications, 3D wafer bonding is supplanted by D2W or D2D bonding because of its ability to assemble only probed good die, to support easier alignment tolerances, to interconnect die of dissimilar sizes, to interconnect die from dissimilar size wafers, and to interconnect die of dissimilar base semi-conductor materials — i.e., heterogeneous integration.

## Implementation strategies for 3D Die-Level Integration

There are a number of techniques that can be used to implement 3D die-level integration. These include D2D integration, D2W integration, die to interposer integration, and combinations thereof. The key to implementing high performance and high reliability 3D integrated die packages is to leverage existing domestic infrastructure, interconnect structures that have a proven reliability track record, and well-characterized packaging architectures. Fundamental building blocks to 3D integrated die packages are multi-layer, wafer-level redistribution technology, integrated passive structures, embedded IC structures, very fine pitch flip chip/direct die bonding, through silicon/substrate vias, wafer/die thinning, and warpage compensation of thin die and substrates.

In most instances, die-level integration leverages industry-proven wafer-level redistribution technologies for which there is a strong domestic manufacturing infrastructure. This follows since most ICs are designed for wirebonding and to a lesser extent flip chip, and the former does not lend itself well to 3D integration.

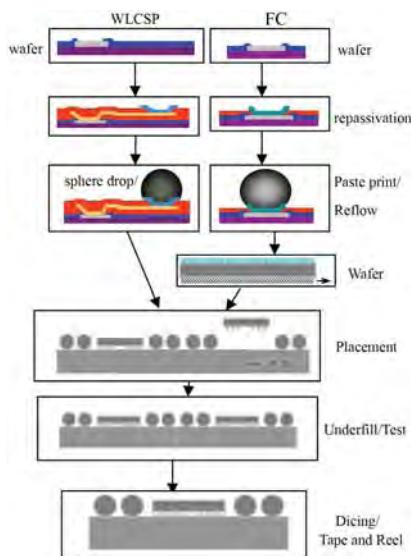


Figure 1. 3D WLCSP and FC Process Flow [6]

BEOL redistribution processing provides the interconnect structure which ensures a compatible I/O pad structure between the ICs during 3D bonding. **Figure 1** shows an example of one such 3D die level implementation using redistribution technology.

Proven techniques for interconnecting 3D die stacks include wirebonding and bump bonding such as solder flip chip, thermosonic bonding, thermocompression bonding, and low-temperature compression bonding. Additional, more involved, techniques for 3D die interconnect include silicon fusion bonding, polymer bonding, metal-to-metal fusion (e.g., Cu to Cu) bonding, direct bond interconnect™ (DBI), and eutectic bonding. These later techniques are more common in wafer bonding applications but can be used for D2W and D2D bonding. The choice of which interconnect structure or combination of interconnect structures depends on semiconductor type, form factor requirements, and electrical performance requirements. The good news is that 3D die-level integration can accommodate many interconnect variations within a package giving the designer flexibility in the cost/performance tradeoff.

When thickness profile is less of a constraint, interconnect interposers with and without through silicon vias (TSVs) can be implemented. Often the interposers are Si-based, taking advantage of the widely available, domestic 150mm and 200mm silicon foundry infrastructure. This infrastructure is finding new life in producing very high density and cost effective 2D and 3D interposers.

**Figure 2** shows a highly integrated, chip-size, four-die module based on D2D integration and wafer-level redistribution technology with a maximum package thickness of 0.8mm. **Figure 2b** shows the package stack-up and **Figure 2a** shows the 4 die module without the high density multilayer substrate. Die 1 is a large memory device that serves as the base die for 3D integration. It is redistributed to incorporate a multilayer, polymer dielectric/Cu interconnect structure to receive Die 2, 3, and 4 in a flip chip configuration. A high-density, microvia substrate is precision bonded to the top sides of Die 2, 3 and 4. Au wire ball bonding is then used to interconnect the high-density substrate to the redistribution pads of Die 1 (**Figure 2e**).

Next the package is encapsulated and the high density substrate CSP pads are solder balled to complete the package assembly (**Figure 2d**).

Die-to-interposer integration is another innovative way to achieve 3D D2D/D2W. **Figure 3** shows a cross-section of a high-speed RF module with eight heterogeneous die (4 GaAs, 2 SiGe, 2 Si) flip chip bonded to an integrated TSV Si interposer substrate. Three different flip chip interconnects are

used at the first level including copper column-solder interconnects, noble metal, plated stud-solder interconnects, and controlled collapse solder interconnects.

**Figure 3** illustrates a copper column-solder flip chip interconnect between a high speed GaAs RF device and TSV interposer as well as the solder flip chip interconnect between the TSV interposer and the high density organic substrate. This module includes flip chip pitches down to 150mm, high-density

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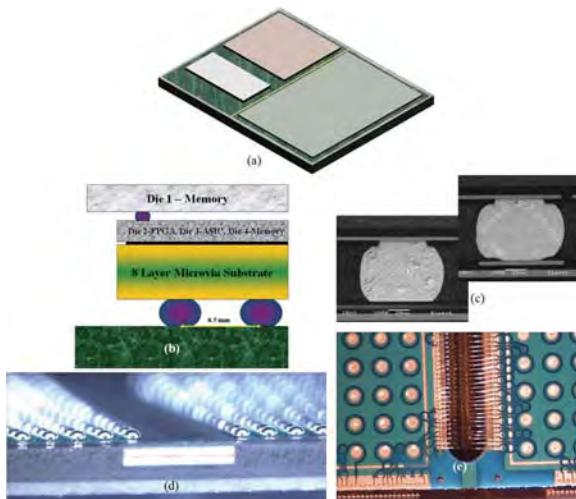


Figure 2. High Speed Digital Module with Die to Die Integration "C 2 Processors and ASIC to Memory

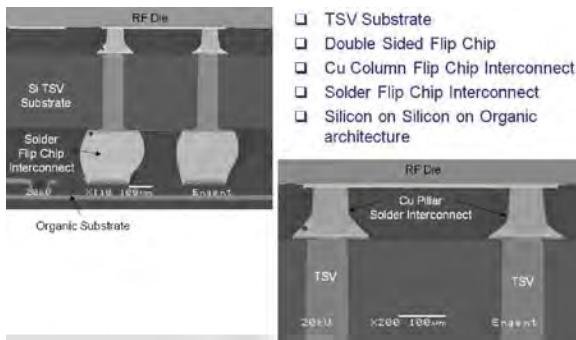


Figure 3. High Speed RF Module with Die to Interposer Integration "C 2 RF Devices and 2 Processors to TSV Interposer

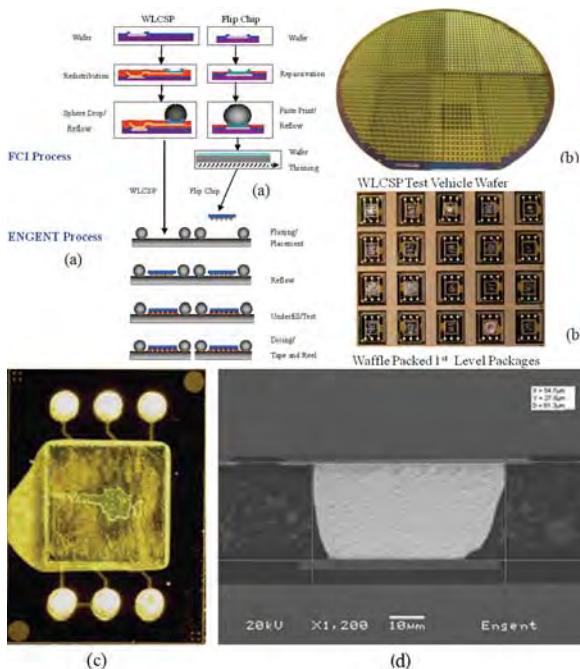


Figure 4. 3D Wafer Level CSP technology (a) Flip Chip Process Flow, (b) Wafer Level Assembly and Singulated 3D-WLCSPs. (c) ACT Die Flip Chip Mounted to PA Wafer, (d) ACT to PA Flip Chip Interconnect

wafer-level redistribution interconnects on the interposer, thinned GaAs die down to 100mm thick, surface mount passives, thin-film passives, 100mm underfill keep-out areas, and 200mm spacing between die requiring precision underfill processing.

**Figure 4** shows an example of a qualified 3D D2W integration technology utilizing very-fine-pitch flip chip, wafer-level redistribution, and wafer-level balling technologies. This packaging scheme involves mounting a flip chip component to the active surface of a WLCSP, enabling 3D die-level integration. This packaging scheme has been successfully demonstrated in an assortment of applications including the MEMS-ASIC combination highlighted in reference 5.

This implementation of 3D die-level integration is realized by face-to-face bonding of fine-pitch flip chip components down to 80 $\mu\text{m}$  pitch (ACT die) onto a redistribution layer of the base WLCSP (PA wafer). In this manner for example, a flip chip driver can be mounted directly onto a memory component, ASIC, driver chip, etc. This new low-cost 3D WLCSP technology leverages the existing infrastructures of WLP and high volume flip chip assembly. WLP provides a highly functional platform from which to implement the new package technology incorporating 3D D2W integration. Moreover, such a packaging architecture provides a cost-effective, rapid time-to-market alternative to emerging 3D wafer-level integration technologies.

The 3D-WLCSP is a qualified package (first and second level interconnects) in volume production. Efforts have focused on wafer level processing and very-fine pitch flip chip placement forming the 3D-WLCSP and the associated challenges that this type of packaging and assembly includes. Key aspects of wafer level processing have been explored including wafer level redistribution, ball drop, wafer thinning, dicing thinned wafers, and flip chip bumping. Moreover, flip chip pitch and bump size has been varied, as well as key assembly materials (including fluxes and underfills) used to attach the flip chip to the WLCSP. Process solutions for flip chip fluxing methods for very-fine-pitch (down to 80 $\mu\text{m}$ ), small bump sizes (down to 50 $\mu\text{m}$ ), vision recognition of the chip and substrate during assembly, reflowing of the flip chips on a wafer, and underfilling a bumped wafer with chip components in close proximity have been established. Initial reliability results are presented in references 8 and 9, which highlight that even though the flip chip is mounted silicon-to-silicon, the pitch and bump size make it so that the underfill selection has a large impact on the reliability of the assembly. Various aspects of the D2W assembly process have been explored, including scaling issues with high-volume assembly, utilization of low-cost underfill approaches such as no-flow underfills, wafer-applied underfills, and underfill encroachment on the WLCSP balls. Finally, data on 2nd level reliability of the 3D-WLCSP has been established, indicating robust reliability of the 3D-WLCSP assemblies mounted on conventional printed circuit boards.<sup>8,9</sup>

Further density opportunities are emerging in the wafer-level 3D packaging space as TSVs ramp in production. **Figure 5** shows a 3D-WLCSP incorporating TSVs in the base wafer (PA) and flip chip die (ACTs) mounted on the back side of the silicon. In this case, the base wafer requires thin-film wiring or redistribution interconnect on the top side of the wafer routed to capture the TSVs as well as the flip chip ACTs. Using this 3D-WLCSP architecture, the entire base die area can be utilized for ACT die bonding, the inter-die interconnect lengths can be minimized improving performance, and the ACT and PA die can be probe tested to minimize the yield loss.

## Summary

As the move to higher performance and smaller form factor electronics continues, 3D die level integration has moved to the forefront as an

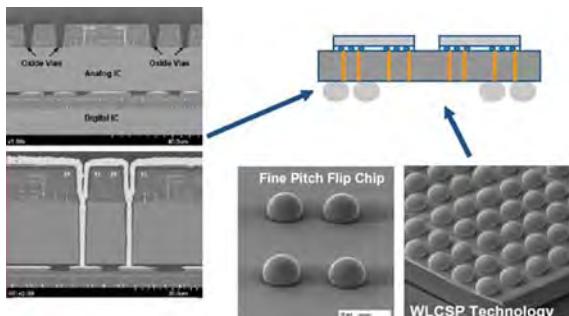


Figure 5. Routing on multiple grids application solution platform. While current 3D packaging solutions involving a combination of high density circuit boards with wirebonded stacked ICs can satisfy some of the performance and form factor requirements, 3D die level integration is proving to be the solution-of-choice for many mission critical, high-reliability applications. The key features of the technology are very high levels of integration, very small form factor packages often chip scale in size, very low profile packages, low weight packages, and improved digital and RF performance. This paper has reviewed 3D integration

technologies, presented implementation strategies for 3D die level integration for chip size packaging, and presented examples of 3D die level integrated packaging solutions.

6. Stout, G. A., Tessier, T.G., Clark, D. Houston, P., Baldwin, D. F. Li, Z., "3D-WLCSP Package Technology: Technology and Design Considerations," Proceedings of the International Wafer Level Packaging Conference, San Jose, CA, Oct. 13-16, 2008.

1. Garrou, P. "Posturing & Positioning in 3-D ICs," Semiconductor International Magazine, April 1, 2007.
2. Garrou, P. "Wafer-Level 3-D Integration Moving Forward," Semiconductor International Magazine, October 1, 2006.
3. Hopkins, J., et al. "Through-wafer Via Etching," Advanced Packaging, April, 2005.
4. T. G. Tessier, D. Scott, D. McComb and R. Forcier, "Mobile Handsets Dictate Flip Chip and Wafer Level Packaging Trends", Semicon West, July 2008.
5. "Chip-On-MEMS Heterogeneous Integration of MEMS and Circuits", [www.vti.fi/en/products/technology/com/](http://www.vti.fi/en/products/technology/com/)

# Taking the Fear and Pain out of 3D Migration

By Lisa McIlrath, [R<sup>3</sup>Logic, Inc.]

**3**D Integration is touted as being the solution to the end of scaling, but the fact remains that there are still many hurdles to overcome in both the design and manufacturing arenas. Cost is one of the major factors in the decision to migrate to 3D technologies or not, and the ability to leverage tried-and-true IP libraries developed at different process nodes can represent a significant savings in both design and manufacturing costs. 3D EDA tools must allow designers to rapidly assess the benefits of a particular stacked configuration including the package and possibly interposer layers, while maintaining existing 2D design flows and methodologies.

## Elements of Fear

The only thing wrong with 3D integration is that the supply chain is uncertain; we don't have good device models (thermal, mechanical, or electrical), and we don't know how to test the die in the stack. Otherwise, it's really great.

It takes a lot of pain to push a multi-hundred billion dollar industry to change its ways, and a lot of reward from any new technology to keep it changed. 3D Integration is exciting, but is it worth the risk to my business to chase after uncertain benefits? What are the real cost and/or performance gains that can be achieved? How can I quantify these and justify the risk?

In the 2D world, designers have the benefit of well-studied models that can be relied upon to closely approximate system behavior under a range of conditions. This frees them to focus on design at the abstract, or system level. In 3D, such models are incomplete or virtually nonexistent as far as fabless companies are concerned. Consequently, there is no choice but to descend into the physical implementation of the stack to ensure that performance criteria can be met. To date, however, few design tools have been available to permit true-3D analysis, spanning multiple die and multiple

technologies. Why not? What is so special about 3D that makes 2D tools inadequate?

We want to answer these questions, define exactly what a true-3D tool is and describe what functions are needed to make 3D design decisions with confidence.

## 3D Design Tools to the Rescue

Designing in three dimensions looks a lot easier than it actually is. Most people who have done it will attest to the fact that one can design 3D systems by patching current 2D tools with scripts and various hacks, but in the words of one veteran 3D designer, it is like "repairing your car with chewing gum and scotch tape".

Given that the objective is to reduce designer pain rather than to increase it, let's briefly state the bare minimum requirements of a true-3D EDA tool:

- Use of independent technology file for 3D rules and configuration
- Ability to use existing 2D PDKs and standard cell libraries without change
- Ability to maintain the integrity of 3D multi-tier cells while editing 2D views (and vice-versa)
- Plug-and-play compatibility with existing flows

There are so many possibilities for configuring a 3D stack (with or without interposer, face-to-face, face-to-back, etc.) and so many ways of combining different die technologies (Figure 1) that the need for 3D technology independence should be self-evident. It should be equally obvious that the designer should not change any portions of existing 2D PDK's or libraries—even if someone already wrote automated scripts to perform this task.

A TSV is the simplest example of a 3D cell (Figure 2), in which different components of the cell reside on different dies. If one part of the

TSV is moved or deleted, the rest of it must be moved or deleted as well.

Plug-and-play compatibility is essential because the fact is that existing tools can already almost do the job. The role of the true-3D EDA tool is to gracefully fill the gaps not covered by current 2D tools. To do this well and thoroughly, it must work within an open standards framework for passing file information to and from the existing toolset. For example, a 3D floorplanner should provide the partitioned netlists and pre-placed TSV positions for each tier to a 2D place-and-route tool. After placement and routing of each tier, the 3D structure must then be recoverable so that electrical and design rule verification can occur across the tiers. In other words, the 3D connectivity and placement information must survive the passage through the 2D design flow, and any changes made to the individual tier designs that affect the 3D structure, for instance moving part of a TSV cell, must be reflected back to the 3D database.

## Maximizing 3D Performance

Until there are a number of successful 3D demonstrators and a body of knowledge of 3D design best practices has evolved, there will remain a great deal of fear and reluctance to betting the farm on this new technology. The afore-mentioned

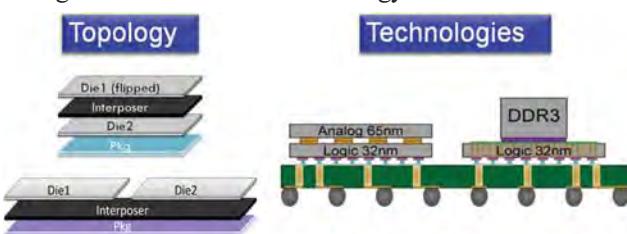


Figure 1. Stack topology and die technologies are specified in a distinct 3D technology file

## A TSV is a 3D cell

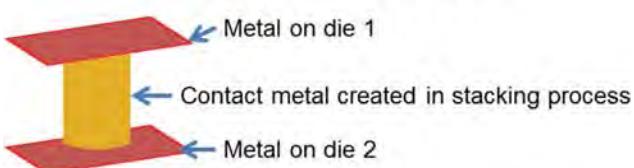


Figure 2. A TSV seen as a 3D cell

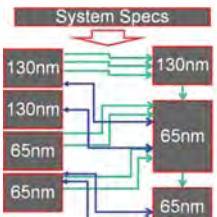


Figure 3. System partitioning alternatives

basic features of a true-3D tool are only just that — basic. To really show convincingly that there is a true cost and/or performance benefit to 3D chip implementation, a 3D pathfinding tool has to be able to dive deep enough into the physical design of the stack so that one can have confidence that the performance parameters it predicts are meaningful.

In addition to the baseline features that must exist in any 3D EDA tool, we identify four essential capabilities needed for efficient design space exploration (aka pathfinding) to rapidly find the sweet spots for 3D.

#### **1. Ease of IP re-use and re-configuration**

If nothing else, being able to use existing, proven IP libraries for the majority of the stack, as opposed to re-characterizing everything in an SoC for a new technology node, represents a huge cost savings in and of itself. It remains to show that there is a concomitant performance or cost benefit exceeding that of going to the next technology node. The only way to do this with any level of confidence is through trial placement of the hard macro blocks called for in the architectural design, followed by routability and signal integrity analysis. This implies that the designer must have full flexibility to choose both the tier placement and the IP library for each block, and that the 3D tool should partition the netlist accordingly (**Figure 3**).

#### **2. TSV planning and assignment**

In the early days of 3D adoption, one has to expect that to minimize cost and risk, the initial 3D stack architectures — at least those produced commercially — will be little more than stacked versions of 2D systems. This being said, there are significant cost savings and performance improvements that can be achieved by introducing interposers with TSVs just to facilitate routing and increase bandwidth. A prominent example is the Xilinx 4-Virtex-on-interposer system announced in October

2010. These 2.5-D systems, as they are often called, are vital to establishing the supply chain for 3D manufacturing. The demand for interposer-based stacks will provide the impetus for developing robust TSV processes, which are needed before widespread 3D fabrication and commercialization can occur.

TSV planning and assignment is crucial in a 3D pathfinding tool because even slight changes in functional block placement on one tier can lead to significant cost increases due to their impact on other tiers. Take for example the configuration shown in **Figure 4**. The left-hand image shows signal flight-lines for a 2-die system flipped directly onto a BGA. The die are arranged diagonally to

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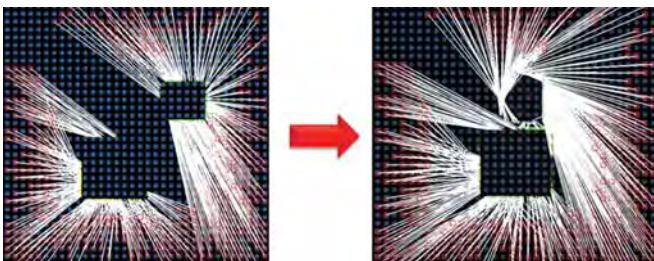


Figure 4. Impact of interposer on package design

minimize cross-over, but still two metal layers are required to route the traces on

the package. The legitimate question is then: "Can we do better with a 2.5D (3D) arrangement?" Is it possible to improve signal delay between the two die, not change the package footprint or pinout — because that impacts the entire product line — and decrease the

cost of the package by removing a routing layer?

Since the interposer area is one cost element, we move the two die as close together as possible. Suddenly the flight-line crossover is much worse — now what? The 3D pathfinding tool has to step in to find the solution by helping to generate a TSV arrangement that can achieve the best compromise for routing both the interposer and the package. In the case at hand (**Figure 5**) it was

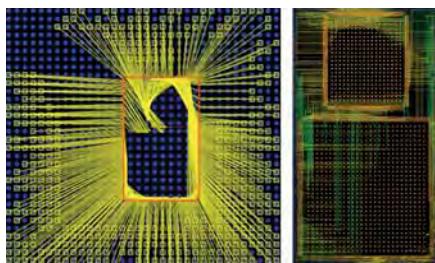


Figure 5. TSV placement and assignment to minimize cost and maximize routability

possible to find a solution that reduced the packaging cost (by removing a routing layer) and improved signal integrity and bandwidth between the two die. Signal crossover was handled on the passive Si interposer where the cost of using three metal routing layers was significantly less than using two on the package.

### **3. Multi-grid routing**

An important point of the previous example is that the package substrate was modeled in the 3D pathfinding tool as just another tier — a perfectly logical consequence of the fact that any 2D technology, including that of the package, can be specified in the 3D technology file. The use of multiple disparate technologies also implies multiple disparate manufacturing grids and hence, for true inter-tier co-design to take place, multiple routing strategies are needed as well. Contrast for example the package-to-TSV routing in **Figure 6** with that of the interposer-to-TSV routing on the right-hand side of **Figure 5**.

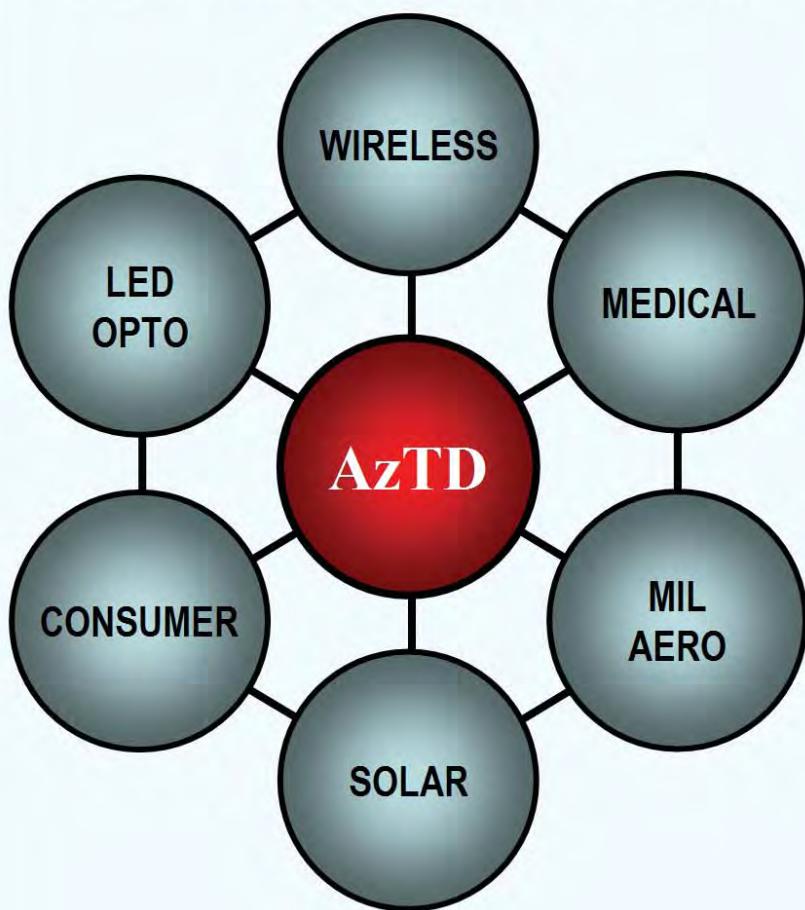
### **4. Signal / power integrity and IR drop analysis**

Being able to place and assign TSVs and perform trial routing is critical for 3D pathfinding if the goal is to verify that 3D

*(continued on Page 48)*



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# Site-specific Analysis for Failure Analysis and Reliability of 3D Systems

By Richard J. Young, [\[FEI Company\]](#)

## Bio for Richard Young, FEI Company

Richard Young is Technologist in the Electronics Market Division at FEI, focused on SEM, FIB and DualBeam systems used for failure analysis and characterization. He joined FEI in 1991. Richard holds a Ph.D. in Physics from the University of Cambridge, where his research included the application of focused ion beams for TEM sample preparation and gas chemistry. Richard holds several US patents and has published widely on FIB, SEM and DualBeam technology and applications.

**D**evelopment and failure analysis (FA) labs operate outside the fab and provide characterization and analysis results to a wide variety of internal and external customers. A fundamental capability is providing site-specific, root-cause analysis and data that support development, yield improvement, and field returns. These techniques rely on a number of electron and ion beam technologies for sample preparation and analysis including focused ion beam (FIB), scanning electron microscopy (SEM), dual-beam (a system combining both FIB and SEM), and transmission electron microscopy (TEM). Particularly for sample preparation, FIB has become invaluable due to its ability to create highly site-specific cross-sections and TEM samples, and to perform gate-level circuit re-wire and debug.<sup>1</sup> With sectioning, the FIB can make localized openings through widely differing material types, enabling analysis on areas that would not be possible by mechanical polishing due to both the localization required (e.g. a 20 nm thick TEM sample must be located to within a few nanometers of the correct location), and due to sample preparation challenges, such as material smearing/tearing due to hardness differences. The localized nature of the milling also means that multiple sections (in different orientations if needed) can be achieved even in close proximity to each other, and that the rest of the device can remain intact for other analyses. Development and reliability activities supported by FA labs generally focus on

the development and yield of the fab process for the devices themselves. However, with more complex packaging and three-dimensional (3D) integration activities, the number of packaging-related sample requests into the labs is increasing. This is because new packaging technologies — such as through-silicon-via (TSV), redistribution layer (RDL) fan-in and fan-out, wafer-to-wafer (W2W) and multi-chip stacks—require site-specific sectioning as part of process development, reliability testing, and FA. An additional constraint for this work is that access to the area of interest is becoming more complex (e.g. due to 3D stacking) with larger volumes of material requiring removal. Just as with the gate-level analysis, site-specific FIB methodologies are desirable for packaging technologies too, but as we'll discuss next, FIB has historically been considered too slow for many applications. This has limited the numbers of such time-expensive samples being run, with other jobs being turned away, or not even getting the work request in the first place. However, the situation is changing with the availability of new FIB techniques and technologies that significantly speed up the sample preparation process.

## Site-specific Sectioning using FIB

FIB systems, whether single-beam FIB or in the dualbeam SEM/FIB combination, generally use a gallium liquid metal ion source (Ga-LMIS), providing a typical beam current range from 1 pA to 10s of nA. This corresponds to a maximum

material removal rate by sputtering of  $\sim 103 \mu\text{m}^3/\text{min}$  for silicon at 60 nA of beam current, which enables volumes of a few 10s of  $\mu\text{m}$  on a side (e.g. for transistor cross-section or TEM sample) to be removed in a reasonable time. However, many 3D packaging samples require much larger volume material removal than is the case with traditional FIB applications (e.g. milled volumes in the order of  $100 \times 100 \times 100 = 106 \mu\text{m}^3$  and larger), so they are often seen as being prohibitively time consuming for the FIB approach. Without new sample preparation techniques, focused on throughput and efficiency, these trends could force an almost exponential growth in the needs for system time and lab resources dedicated to packaging related issues.

The challenge therefore is to get the desired FIB benefits (namely: localized, site-specific sectioning), but at faster volume removal rates than has been possible by previous FIB approaches. Despite other techniques, such as broad-ion milling and laser ablation that have larger volumetric removal rates, the value of site-specific FIB is well appreciated and labs sometimes use existing FIB tools with 20nA capabilities for these jobs. However, they are only running a limited number of samples using mill times with the FIB.

## Going Faster — High-Speed Silicon Removal

There are several approaches for improving throughput of larger volume sample preparations. These include using enhanced etch gases in combination with the ion beam, as well as technology improvements that increase the useful FIB current available for sectioning applications. In addition, progress has been made in beam scanning strategies for increasing the milling rate for a given beam current, and in the use of automation routines that allow unattended milling to

occur; perhaps overnight while the tool would otherwise be unused.

Using a reactive gas (typically halogen based: e.g. I<sub>2</sub>, XeF<sub>2</sub>, Cl<sub>2</sub>) in addition to the FIB usually enhances the etch rate from 1-15X, but with the combination of XeF<sub>2</sub> gas and a silicon substrate the enhancement can be over 1000X. This is due to the spontaneous reactivity of the gas with Si that enables access trenches to be drilled even through a full-thickness silicon device for circuit edit applications. Such an enhancement makes removing large volumes of Si more practical even with the typical upper end of FIB currents of 20-60 nA. This high-speed silicon etching approach has been applied to full-thickness silicon trenching for W2W bonding process development<sup>2</sup> and to TSV sectioning<sup>3</sup>.

In the W2W example, a FIB system equipped with an IR microscope and CAD navigation was used (CAD navigation allows patterns from the original design database, e.g. GDS-II format data, to be used for aligning and navigating around the sample based on FIB, SEM, or, as in this case, IR images). The IR/CAD combination was used to locate the buried interconnect features at the W2W interface through the full thickness (750-800 μm) of the upper wafer. Fast trenching opened up a window down to the area of interest (Figure 1a), after which the interface could be inspected by direct FIB sectioning and imaging. To enable a more detailed investigation, regions of interest were extracted from the trench and prepared for TEM analysis (region

thinned to < 100 nm), (Figure 1b). The TEM and other analytical data indicated that some Cu grain growth had taken place during the bonding/annealing process, with grains now spanning across the line of the original interface. This was contrasted with the other metal-via interface, where there is a distinct horizontal interface at the barrier interface. In addition, no voids were observed at the bond interface on any of the samples run.

## Larger Beam Currents and New Source Technology

Silicon with XeF<sub>2</sub> is certainly a special case with no other known combination of gases and materials approaching 1000X enhancement over pure sputtering. Therefore, for other materials, the need for faster volume removal rates drives the need for more ion beam current. The challenge for the LMIS-based FIB is that the beam performance becomes degraded, due to the ion optical properties of the source and focusing lenses, above several 10s of nA of ion beam current. Therefore, careful column design is required to produce good performance in this range. For many years, 20nA was the typical maximum beam current. More recently though, systems with good sectioning performance even at currents as high as 65nA have become available. In addition, when the 3X increase in beam current is combined with more optimized scanning strategies during the sectioning, the

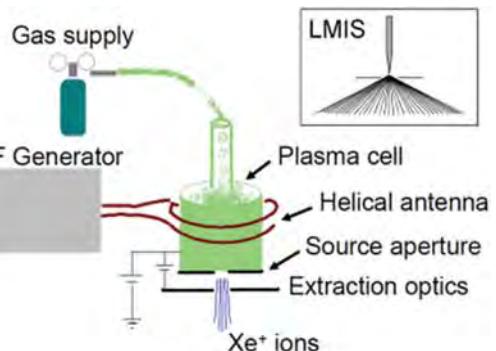


Figure 2. Schematic of ICP source used in xenon Plasma-FIB system. Inset image is LMIS source. See text for more details

improvement over traditional FIB sectioning can be >6X. While this is less than the 1000X seen in the Si-XeF<sub>2</sub> case, it is still highly valuable, enabling times for jobs to be reduced from a full day to a more manageable 4hrs, or from 6hrs to less than one.

To go beyond this level of performance requires new ion source technology, such as the inductively-coupled plasma (ICP) source.<sup>4-6</sup> The LMIS-type of source can be characterized as a point source with high brightness but relatively low angular intensity due to a cone-shaped emission pattern from the source (Figure 2 inset). The small virtual source size provides good beam resolution at low beam current (e.g. < 5nm at 1pA), but as the beam current increases into the 10s of nA regime, the effects of spherical aberration dominate the beam performance due to the large aperture opening angle required to supply the needed beam current from the source. In contrast, the ICP source is broader, but with much higher angular intensity as the beam emerges from the source in a more collimated fashion (Figure 2). The “brightness” (a key performance metric of a source) of the ICP source is lower than the LMIS, but it is still 5-10X the brightness of the duoplasmatron type of plasma source often used in sputtering application.<sup>4</sup> The ICP design is also superior to such DC plasma source types in terms of lifetime. The ICP source uses an external RF antenna to couple energy into the plasma, thereby avoiding internal cathode erosion, which severely limits the lifetime of other plasma ion beam source types.

These ICP source attributes enable it to have superior beam performance over the LMIS at very high beam currents, enabling

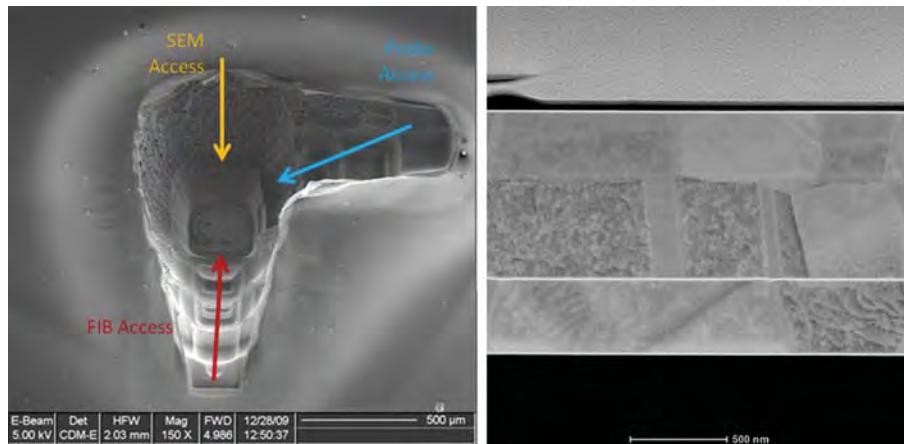


Figure 1. Site specific TEM sample from W2W bonded test vehicle. The side trenches in 1a are to facilitate the subsequent sample preparation steps needed to extract the sample for use in the TEM (1b). Sample courtesy of SEMATECH

up to several  $\mu\text{A}$  of ion beam current for fast material removal. The cross-over in beam spot performance between the LMIS and ICP source is around 50nA, above which the ICP source offers better performance. At lower current, the LMIS outperforms the ICP source, but imaging resolution below 30nm has been demonstrated with ICP based systems. In addition, the ICP source allows a wide range of possible ion species; with Xe currently being used as the milling species of choice due to its high mass and favorable ion source performance parameters. Using a 1 $\mu\text{A}$  Xe beam will have an overall milling rate for silicon some 20X higher than a Ga beam operating at 65nA.

### Plasma-FIB Applications in Packaging Reliability

ICP-source based plasma-FIB systems are now being applied to 3D-packaging challenges. At the IMAPS Device Packaging Conference (March 2011,

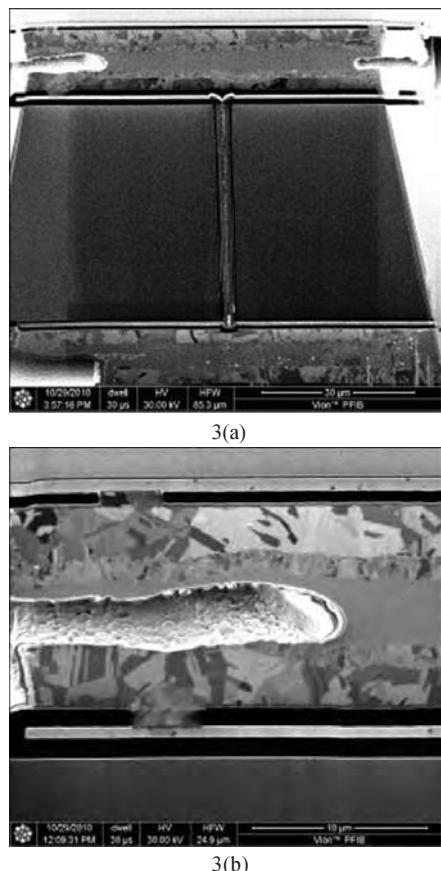


Figure 3. Plasma-FIB section and image of 3D-integration test chip. The three chip stack is connected using TSV. In 3b the details of the IMC in the chip-chip bond are visible. Sample and images courtesy of Fraunhofer EMFT

Scottsdale, Arizona) Peter Ramm of Fraunhofer EMFT in Munich described the use of such a plasma-FIB for reliability studies on a 3D-integration test chip.<sup>7</sup> This device consisted of a three-level stack using a silicon-interposer with TSVs as the middle layer connecting the top and bottom devices (Figure 3). The plasma-FIB was used

to section and image through different regions of the device to investigate both the TSV interconnections and the intermetallic compounds (IMCs) produced at the bonding interfaces between the chips. It should be noted that like the Ga-LMIS based FIB, that Xe-ICP images

(continued on Page 40)

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Casio Micronics Co., Ltd. 10-6, Imai 3-chome, Ome-shi Tokyo, 198-8555 Japan Tel: +81-428-32-1551 www.casio-micronics.co.jp	Ball Drop	BP: > 150 WD: 125, 150, 200, 300 UBM: TiNiCu, NiAu Electroless, Sputtered UBM	SEU, SHL, SLF
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ChipMOS Taiwan No. 1, R&D Rd. 1, Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C. Tel: +886-3-577-0055 www.chipmos.com	Electro Plate	BP: CM WD: 150, 200 UBM: TiW+Au Sputtered UBM	AU
CV Inc. 850 S. Greenville, Suite 108 Richardson, TX 75081 Tel: +1-214-557-1568 www.covinc.com	Electro Plate	BP: > 36 WD: 200, 300, Partial, Die UBM: Cu, Ni+Au, Ni+Pd+Au Electroless UBM	CP SEU, SHL, SLF Other
Flip Chip International 3701 E. University Drive Phoenix, AZ 85034 Tel: +1-602-431-6020 www.flipchip.com	Ball Drop Electroless Stencil Print	BP: > 35 WD: 150, 200, 300 UBM: NiAu, Al/NiV/Cu Electroless, Sputtered UBM	CP SEU, SHL, SLF
Fujitsu Semiconductor Ltd. Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome, Kohoku-ku Yokohama Kanagawa 222-0033 Japan Tel: +81-45-415-5858 http://jp.fujitsu.com/fsl/en/	Electro Plate	BP: > 50 WD: 150, 200, 300, Die UBM: TiCu+Ni, Ni Electroless, Sputtered UBM	SEU, SHL, SLF



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IC Interconnect 1025 Elkton Drive Colorado Springs, CO 80907 Tel: +1-719-533-1030 www.icinterconnect.com	Ball Drop Stencil Print	BP: > 200 WD: 75 - 200 UBM: Ni+Au Electroless UBM	SEU, SHL, SLF
<b>IMI</b> <b>International Micro Industries (IMI)</b> 1951 Old Cuthbert Road, Bldg. 404 Cherry Hill, NJ 08034 Tel: +1-856-616-0051 www.imi-corp.com	Electro Plate	BP: > 5 - 10 WD: 100, 125, 150, 200, 300 UBM: Au, Cu, CM Sputtered UBM	AU CP SEU, SHL, SLF Other (In, Ni, Ag, AuSn)
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KSW Microtec Manfred-von-Ardenne-Ring 12 D-01099 Dresden, Germany Tel: +49-351-88960-10 www.ksw-microtec.de	Electroless Electro Plate Stencil Print	BP: > 20 WD: 100, 150, 200 UBM: Ni+Au Electroless UBM	AU SEU, SLF Other (Ni+Au, Pd)
Minami Co., Ltd. EMS Tsukuba Factory 38-32, 5-Chome Minami-Cho, Fuchu-Shi Tokyo 183-0026, Japan Tel: +81-42-368-8311 www.ho-minami.co.jp	Ball Drop Stencil Print	BP: > 80 WD: 100, 125, 150, 200, 300 UBM: Au, Cu	SEU, SHL, SLF
 <b>NANIUM S.A.</b> Avenida 1º de Maio 801 4485-629 Vila do Conde, Portugal Tel: +351-252-246-000 www.nanium.com	Ball Drop Electro Plate Stencil Print	BP: CM WD: 150, 200, 300 UBM: CM	AU CP SEU, SHL, SLF

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# INDUSTRY HAPPENINGS

## SEMICO Research Summit: An Executive Perspective on the New Frontier for Semiconductors

Painting a bright future for the electronics industry driven by smart technologies, a varied assortment of industry executives from across the semiconductor supply chain offered insight at the SEMICO Research Summit, May 1-3, 2011. The theme of the two day event was "The New Frontier," which is being paved largely by the opportunities afforded by the recent wave of smart technology: phones, tablets, homes, etc. Taking advantage of these opportunities will require a new approach pretty much across the supply chain.

Offering a snapshot of SEMICO's industry analysis, Jim Feldhan, CEO, opened up the proceedings. He talked about global economics, giving a country-by-country breakdown, stressing how we really need to pay attention to the world environment. The US is gridlocked, causing deficit phobia, decimating educational investments, and the infrastructure is being ignored while other countries are investing heavily. He also touched on the aftermath of the earthquake/tsunami/nuclear disaster in Japan; noting that while it will take Japan 3 years to rebuild, the world-wide effect will be short-lived. He predicted that electronics supply chain shortages will be over by September, and spot shortages will actually result in pent-up demand and stimulate growth in 2012. One lesson learned is that there needs to be a global balance in the supply chain so that sources aren't limited to one geographical region, in case of natural disasters.

Feldhan also set the stage for the remainder of the summit, calling the explosion in smart phones the "Promised

Land" with lots of leading-edge chips for baseband and applications and processors and memory. And the market for MEMS and sensors is expected to grow 58% in 2011. Adapting to the speed and product drivers of this New Frontier will, more than anything, require changes in the way things are done.

As Danny Biran, Sr. V.P. of Marketing, noted, historical definitions are becoming meaningless. With regard to the previously clearly defined purposes of ASICs, FBGAs, ASSPs, and μP/DSP, those lines are now blurring. With improved process technologies and design techniques, more functions can be implemented on the same die. With these converging platforms, Biran says that semiconductor companies must create new types of products to succeed. "Rethink priorities, needs, your development organization, and skill sets," he advises. "Let the product drive the structure of organization and design methodologies. Engage with platform vendors early on in the process — don't make assumptions of what can or can't be done." This way, he says you can ensure you get the best combination of flexibility, time to market, performance, and cost.

The importance of open communication and collaboration going forward was another underlying sentiment voiced by many of the speakers. Gregg Bartlett, SVP of Technology and R&D, GLOBALFOUNDRIES, said the mobile electronics experience is enabled by silicon innovation. At 20nm and beyond, he says packaging integration is no longer an afterthought, but rather a dominating contributor to the value chain because it

offers opportunities to lower cost and accelerate time to volume. 2.5D and 3D processes give system level designers another knob to allow for repartitioning products.

Bartlett says that this calls for a collaborative environment, where foundries work together with OSATS to jointly develop IP solutions for customers. He proposed a new global model for collaboration calling for advanced research and early engagement across the customer base. Likewise, involving the EDA and packaging communities early on is vital. It's important to establish design rules that can be substantiated in technology, and to foster a multi-sourced, geographically dispersed supply chain. Aart De Geus, founder of Synopsys, concurred, saying that for future technology generations, software development needs to take place along with hardware development, rather than waiting for the hardware to be ready to go before developing software.

Perhaps Moshe Gavrielov, President & CEO, Xilinx, Inc. voiced best what is needed when he quoted Charles Darwin as saying "It's not the strongest of the species or smartest that survive, but the one most accepting of change." In addressing skepticism about making progress in semiconductors below 30nm, Joe Sawicki VP and GM, Design-to-Silicon, Division Mentor Graphics succinctly summed up what applies for all moving forward. "The only one rational approach to looking forward is with WILLFUL OPTIMISM, and continue to deliver on what is possible; even if it's thought to be unachievable."

## SEMI-THERM 27 Attendance Underscores the Importance of Thermal Management



The 27th annual IEEE Semiconductor Thermal Measurement, Modeling and Management (SEMI-THERM) Symposium was held March 20-24, 2011, in San Jose, CA. This marked the first year that MEPTEC co-located its annual one-day thermal packaging workshop with the



SEMI-THERM event.

The 5-day event showed increases in attendance and course offerings across the board over 2010. It attracted 198

symposium attendees (up 43%) to 44 short courses (up 83%) and 486 total registered attendees (up 66% over 2010). There were 38 exhibitors (up 31% over 2010), reported Tom Tarter, Exhibitor and Conference Manager, and President of Package Science Services, LLC.

"SEMI-THERM 27 demonstrated, through increased symposium and exhibition attendance, that the electronics industry is recovering from the downturn over the last several years and that the



## SEMICON® West 2011

thermal management aspects of the industry remain of high importance. The recovery also led to a significant increase in the number of exhibitors, maintaining SEMI-THERM as the premier venue for displaying and introducing new electronics thermal management products and services.” noted Bernie Siegal, President of Thermal Engineering Associates, Inc, and Steering Committee Operations Chair,

Keynote speaker, William Chen of ASE Group, kicked-off the event with a provocative presentation titled, “Engineering the Packaging Revolution.” Jim Wilson of Raytheon was honored with the prestigious 2011 THERMI Award for his contributions to the field, and Dirk Schweitzer of Infineon Technologies AG received the Harvey Rosten Award for Excellence for his paper.

“The conference had an impressive turnout of attendees from various parts of the world e.g. North America, Asia (Hong Kong, Taiwan, China, Japan, Korea, and India) and Europe (Russia, Poland, Germany, Turkey, Belgium, Hungary, and the Netherlands).” remarked General Chair, Sai Ankireddi, PhD., Sr. Principal Engineer at Intersil Corp., “The participation by these engineers, technologists and scientists from all over at this annual symposium is testament to SEMI-THERM’s truly international stature, and to its position as the de-facto forum for practical knowledge and experience sharing in the areas of thermal measurement, management and modeling.”

### SEMICON West 3D and Advanced Packaging Program: Having Cake and Eating It Too

This year’s 3D integration and Advanced Packaging Programs at SEMICON West, July 12-14, 2011, in San Francisco, CA, are shaping up to be

real crowd pleasers. The SEMI Advanced Packaging Committee, chaired by Bill Chen, ASE Fellow, has been hard at work making sure all bases are covered in this expanding market sector from 3D integration, heterogeneous integration of MEMS and sensors to the latest in ‘contemporary’ packaging and wafer-level packaging (WLP) processes. In fact, so much ground to cover called for the expansion of the original time slots.

Divided on three different stages over two days, this year’s programs will follow a keynote/panel discussion format with representatives from across the supply chain assembled to discuss challenges and solutions for each focus area.

### Heterogeneous Integration with MEMS & Sensors

With double-digit growth forecast for the MEMS industry, more MEMS devices and sensors are finding applications in the global market place. Smart phones, handheld gaming devices and consoles, and automotive applications are leading the charge. With devices on the market ranging from pressure sensors, RF-MEMs, accelerometers and gyroscopes, to microphones, micro-actuators, compasses, CMOS image sensors, chemical sensors, microfluidics, and mirrors and displays, there’s no doubt that MEMS are growing fast. To paraphrase ITRS, the intersection of Market and Technology is calling for “More MEMS and More Than MEMS”. This session will focus on key players in the system, device manufacturer, OSAT and consortia segments of MEMS.

Chaired by Klaus-Dieter Lang, Fraunhofer - IZM Director, keynote speeches for this session will be delivered by an industry visionary (TBD) and market analyst, Jan Vardaman, president, TechSearch International. At press time, confirmed panelists include M. Juergen Wolf, Fraunhofer IZM, Yoshiaki Sugizaki, Toshiba Corp, and Gilles Poupon, CEA-Leti, They will be joined by several other

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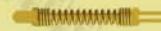
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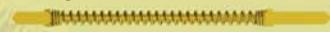
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## UPCOMING EVENTS

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representatives from across the MEMS and packaging ecosystem from academia through the supply chain.

### 3D in the Deep Submicron Era

3D is about much more than 3D-IC and Moore's Law Scaling. The drive for 3DIC has spawned a whole ecosystem for TSV technologies ranging from industry, academia, and research institutes to equipment and materials suppliers. Silicon interposers based upon TSV — thus inspiring the term 2.5D — have become critical in the first wave of 3D implementation. From high-performance network systems and servers to laptops, tablets, mobile systems and game consoles, the silicon interposer represents a solid fork in the highway for 3D implementation, thus raising the questions: What is the silicon interposer ecosystem? Is the industry infrastructure in place for high-volume cost-efficient 3D implementation? What will the next step be? In the world of “More Moore and More Than Moore”, 3D silicon interposer technology enables the industry “to have its cake and eat it too”.

Session chairs Jie Xue, Cisco, and Gamal Refai-Ahmed, AMD, are organizing a group of experts on these topics to address these specific questions and concerns. Divided into two sub-sessions, the first will address 2.5D integration using silicon interposer technology, and will kick off with a keynote address from industry visionary, Vincent Tong, Senior VP at Xilinx, followed by a panel discussion moderated by Sitaram Arkalgud, 3D IC program director at SEMATECH. Confirmed panelists include Rao Tummala, of Georgia Tech's 3D Packaging Center; Ron Huemoeller, Senior VP, Advanced 3D interconnects, Amkor; Jon Greenwood, Senior Member of Technical Staff, Technology & Integration GLOBALFOUNDRIES, and others.

The second session will feature a keynote by well-known market and technology analyst, Jean-Marc Yannou, of Yole Développement. The ensuing panel discussion, 3D Packaging Technology and Ecosystem, will examine the state of the 3D market and its

remaining hurdles. Confirmed panelists now include Bill Bottoms Chairman and CEO Third Millennium Test Solutions, Inc. (3MTS); Rozalia Beica Global Director of 3D Interconnect Technology Transfer and Integration of Applied Materials; and Calvin Cheung VP of Engineering, ASE U.S.

### Contemporary Package Challenges and Solutions for 40nm and Beyond

Much has been written about emerging technologies for the 40nm fab node (and beyond), such as CU pillar FC, ELK compatibility and 3D TSV. However, product-level applications for these technologies tend to focus on performance-driven market segments; markets that are better-able to fund technology development and can accept higher initial risk. But what about market segments that account for up to 70% of our industry and are driven largely by low-cost and low-risk? Are cost-effective IC package solutions available for market segments such as handheld, consumer and automotive as they migrate to smaller silicon lithographies in search of cost reduction?

When faced with the decision to use an advanced fab node, will these companies:

- Change package interconnect technology?
- Change package and PCB technologies?
- Change system architecture?
- Adopt new technologies such as FO-WLP and TSV?
- Continue to use the existing fab node
- Do something else?

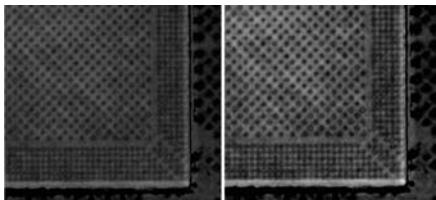
Co-Chaired by Tom Gregorich of MediaTek and Rich Rice of ASE, one of two keynotes will be delivered by Jim Walker, Research V.P. Panelists include Doug Yu, Sr. Director of Interconnect and Packaging, TSMC; Andreas Knoblauch, Director Package Development Automotive, Infineon Technologies; Mike Ma, V.P., R&D, Siliconware Precision Industries Co., Ltd (SPIL); and Fernando Chen, Senior Director, Laminate Products & Technology Marketing, STATS ChipPAC.

(continued on Page 44)

# WHAT'S NEW!

## Molded Flip Chip Imaging Enhancement

Molded Flip Chip Imaging (MFCI) enhancement from Sonix was designed to improve image quality and defect detection in molded flip chips and packages with polyimide (PI) layers by reducing the impact of the scattering and attenuation effects of filler particles in mold compounds and PI layers. Filler particles increase scattering of ultrasonic signals, causing shadows in



the images, and in some cases completely obscure solder bumps and Cu pillars, resulting in reduced image quality and inaccurate defect detection. Also, the polyimide materials (PI) used to improve the thermal properties of thinner dielectric layers attenuate the ultrasonic signal, further degrading image quality and defect detection. Configured through Sonix WinIC™, Sonix MFCI improves the spatial resolution, contrast and edge definition when inspecting samples containing materials that scatter or attenuate ultrasonic signals. Sonix MFCI is available as an option on all Echo™, Echo Pro™ and AutoWafer™ tools, and as a field upgrade on all Sonix Fusion™ and Vision™ tools. [\[sonix.com\]](http://sonix.com)

## Triple Stacked Spring Pin Socket

Ironwood Electronics' triple stacked BGA socket (CBT-BGA-7007) addresses high performance requirements for testing processor and memory simultaneously along with a memory probe. Two different spring pin technologies were utilized in the design—0.5mm pitch stamped spring pins,

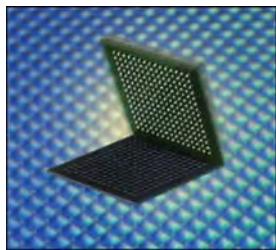


which have 26 gram actuation force per ball and cycle life of 500,000 insertions; and 0.4mm pitch etched spring pins, which have 4 gram actuation force per ball and cycle life of 500,000 insertions. The stamped spring pins are used in between memory and memory probe as well as between memory probe and processor top. The etched spring pins are used in between processor bottom and target PCB. Socket temperature range is -55C to +180C. The socket also features a floating guide for precise ball to pin alignment.

The CBT-BGA-7007 was designed specifically for testing processor BGA, 12x12mm, 0.4mm pitch, 520 position, 29x29 ball array in the bottom socket and a memory BGA, 12x12mm, 0.5mm pitch, 168 position, 23x23 ball array in the top socket. The socket is mounted using supplied hardware on the target PCB with no soldering, and uses the smallest footprint in the industry, allowing inductors, resistors and decoupling capacitors to be placed very close to the device for impedance tuning. [\[ironwood.com\]](http://ironwood.com)

## Reballing Preforms for Wafer Level Package

EZReball™ from BEST Inc. are said to be the finest pitch, smallest ball diameter reballing preforms worldwide. Now available in ball sizes down to 8 mils (0.20mm), these preforms



accommodate devices down to 0.4mm pitch sizes. Solder sphere alloys are available in lead-free, tin-lead and high temperature alloys. The preforms are suited to leading-edge users who need to reball wafer-level components down to 0.4 and 0.5 pitches. Additionally, they can be used to help diagnose and troubleshoot component problems. EZReball™ preforms are available in packages of (15) preforms and come with a QC stencil in the package. [\[www.solder.net\]](http://www.solder.net)

## Advanced Macro Inspection Module

The F30™ Advanced Macro Inspection Module, introduced by Rudolph Technologies, is said to further



extend the capabilities of the Explorer® Inspection Cluster product line. Foundries and IDMs that have installed the module report improved throughput over the entire sensitivity range when compared to previous generation tools. The hardware platform is capable of supporting 450mm development, and is designed to accommodate future customer requirements and capabilities. The F30 Module features a flexible blend of throughput and detection sensitivity, resulting in a lower CoO. It combines automated setup, intelligent software and robust capability staged on a flexible platform designed to accommodate additional capability as defined by customer requirements. [\[rudolphtech.com\]](http://rudolphtech.com)

## Reworkable Edgebond Adhesive

Zymet Inc.'s UA-2605 is a reworkable edgebond adhesive that is said to improve thermal cycle performance of CBGAs and plastic BGAs. According to the company, in one trial, UA-2605 tripled the 0°C to +100°C performance of a CBGA, to nearly 2500 cycles. Previously, an underfill was needed to achieve this level of performance.

This edgebond adhesive is reportedly easier to process than an underfill. With UA-2605, only one bead of adhesive at each corner is required. There is no need to preheat the board, wait for underfill flow, or multiple dispensing passes. Additionally, BGA rework is



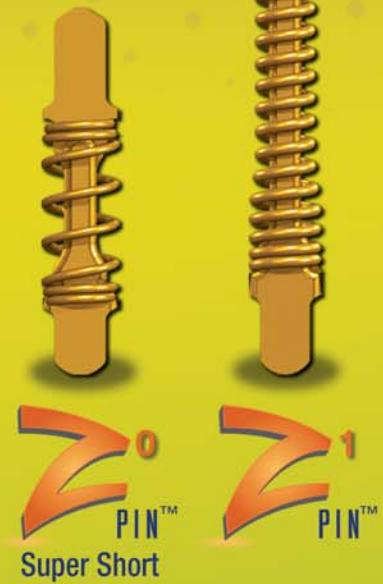
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and interfaces, substantial developments in 3D interconnections, new material composition, and increasing component density while reducing critical dimensions,” says Mario Pacheco, Staff R&D Engineer at Intel. “These trends and developments translate into challenges for defect isolation and characterization that are outpacing traditional failure analysis techniques. Xradia’s developments in throughput and resolution address crucial gaps in failure analysis with a faster, non-destructive technique enabling high resolution characterization of *intact* packages.” [\[Xradia.com\]](#)

### High Resolution 3D X-ray Microscope

The *VersaXRM-500* from Xradia is a 3D X-ray microscope featuring a versatile combination of reportedly world-leading resolution and contrast, sample flexibility, and the large working distance required to address emerging research challenges in many market segments including the semiconductor industry.

The *VersaXRM* family builds on the resolution, contrast and versatility inherent in Xradia platforms, including true submicron spatial resolution, even when positioned only millimeters from the source. The system features flexibility for correlative microscopy with multi-length scale imaging using the *VersaXRM* in conjunction with the *UltraXRM* or other microscopy techniques. The combination of better working distance and imaging flexibility extends the value of microCT, improves throughput. Additionally, it offers the only non-destructive submicron resolution tomographic capability, able to visualize buried features without de-packing, cutting, or otherwise destroying the device, a process that can potentially introduce physical artifacts. This can also prevent the loss of critical information about the root cause of the failure as a result of destructive imaging methods.

“The package assembly roadmap calls for an increasing number of stacked dice

### Conductive Die Attach Film

With the introduction of a novel material formulation, Ablestik C100 series conductive die attach films from Henkel enable leadframe package manufacturers to realize the advantages of film-based solutions formerly only available for non-conductive processes. Established benefits over traditional paste die attach reportedly include the elimination of die tilt, ability to process thinner die, and greater bondline control.



These die attach materials are said to provide a high degree of manufacturing latitude. Workability has been established on die sizes ranging from 1mm x 1mm up to 6mm x 6mm for a variety of package types including both QFNs and QFPs. Additionally, the materials’ better wetting ability with lower bonding temperature provides stable adhesion strength for robust adhesion against moisture and MSL Level 2 performance on all leadframe surface finishes. [\[Henkel.com/electronics\]](#)



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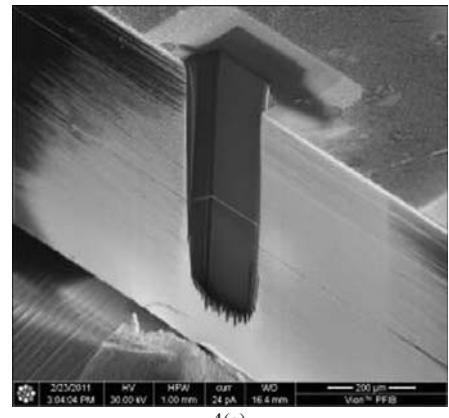
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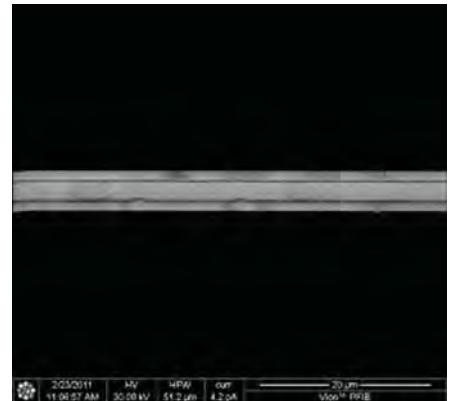
(continued from Page 29)

show strong grain contrast in many metallic samples due to “ion channeling” contrast in the secondary electron image. This makes the ion beam an excellent tool for not only sectioning, but also imaging such interconnect and IMC samples.

In a second paper at IMAPS, the plasma-FIB was also applied to an investigation of W2W bonding using an anisotropic conductive adhesive.<sup>8</sup> This bonding was achieved using metal-coated polymer spheres (4μm in diameter) in a benzocyclobutene polymer matrix. Figure 4 shows a section through the interface region where the interconnecting spheres



4(a)



4(b)

Figure 4. Plasma-FIB section and image through W2W bonded interface. 4b shows a detailed view of the bond, including two of the interconnecting spheres. Sample and images courtesy of SINTEF

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have been precisely sectioned. The authors reported a good correlation between the contact area size and resistance, indicating a satisfactory insulation between bonded areas, and noted that “a well controlled stand-off height was observed in FIB inspection of diced cross-sections.”

#### Conclusion

3D packaging integration continues to increase in complexity, which is driving more samples into FA labs for development support, reliability studies, and failure analysis. FIB and dualbeam FIB/SEM provide key capabilities to support these activities, notably the ability to provide site-specific sectioning and analysis. In addition to the increase in sample numbers, there is also a need for larger removal volumes for many of the jobs, compounding the increased need for tool time and resources to meet the demand. To address this, a number of system and technology developments are improving the throughput of the FIB technique; these include enhancements via

FIB-induced beam chemistry and the use of higher current ion sources, notably the recent introduction of FIBs based on the inductively coupled plasma ion source.<sup>5b</sup>

## Acknowledgements

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- A part of the work has been performed in the project JEMSiP\_3D, which is funded by the Public Authorities in France, Germany, Hungary, The Netherlands, Norway and Sweden, as well as by the ENIAC Joint Undertaking.

## References

- [1] For an overview on FIB techniques see, for example, Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques, and Practice, eds. L.A. Giannuzzi and F.A. Stevie, Springer, New York, 2005.
- [2] W.H. Teh, C. Deeb, J. Burggraf, M. Wimplinger, T. Matthias, R. Young, C. Senowitz, and A. Buxbaum: "Recent Advances in Submicron Alignment 300mm Copper-Copper Thermocompressive Face-to-Face W2W Bonding and Integrated Infrared, High-Speed FIB Metrology", Proceedings of 13th IEEE International Interconnect Technology Conference, 2010.
- [3] P. Gouet, M. Mercier, D. Serre, and C. Rue,: "Failure Analysis of Through-Silicon-Vias Aided by High-Speed FIB Silicon Removal", Proceedings of 16th IPFA, Suzhou, China, 2009, pp. 94-99.
- [4] N.S. Smith, W.P. Skoczylas, S.M. Kellogg, D.E. Kinion, P.P. Tesch, O. Sutherland, A. Aanesland, and R.W. Boswell: "High Brightness Inductively Coupled Plasma Source for High Current Focused Ion Beam Applications", J. Vac. Sci. Technol., 2006, B24(6), pp. 2902-2906
- [5] S. M. Kellogg, A. Graupera, R. Hoelle, T. Miller, S. Zhang, D. Laur, and A. Dirriwachter: "A System for Massive, Rapid Material Removal for Device Analysis in Monolithic 3D Integrated Circuits", Presented at 53rd International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication, Florida, May 2009
- [6] S.M. Kellogg, R. Schamper, S.Y. Zhang, A.A. Graupera, T. Miller, W.D. Laur, and A.B. Dirriwachter, "High Throughput Sample Preparation and Analysis using an Inductively Coupled Plasma (ICP) Focused Ion Beam Source", Microsc. Microanal., 2010, 16 (Suppl 2), pp. 222-223.
- [7] P. Ramm, A. Klumpp, G. Franz, and L. Kwakman: "Failure Analysis and Reliability of 3D Integrated Systems", Proc. IMAPS Device Packaging Conf., Scottsdale, Arizona, 2011
- [8] M.M.V. Taklo, T. Bakke, H.R. Tofteberg, L.G.W. Tvedt and H. Kristiansen: "Anisotropic Conductive Adhesive for W2W Bonding", Proc. IMAPS Device Packaging Conf., Scottsdale, Arizona, 2011

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# Full Speed-Ahead for Flip Chips

By Jean-Marc Yannou, [Yole Développement]



Jean-Marc Yannou is in charge of advanced packaging analysis at Yole Développement, including wafer-level packaging and 3D system integration. His 15 years of experience in the semiconductor industry include serving as innovation manager for system-in-package (SiP) technologies at Philips/NXP Semiconductors, and years at Texas Instruments.

The worldwide flip chip market reached \$16B in 2010, and is now poised for extreme growth as the technology continues to evolve and loses its reputation as a costly packaging solution (**Figure 1**). Although

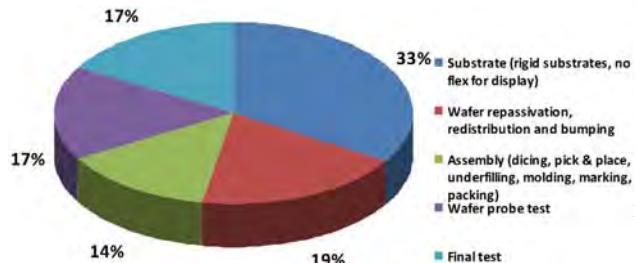


Figure 1. 2010 Total Flip Chip Market Value split by cost-of-ownership supply chain segments (substrates for LCD drivers excluded, service margin included) Total = \$16B

the flip chip market is large and well established, it isn't considered mature yet. In 2010, it accounted for 29% of the total IC packaging market — involving more than 17B flip chip ICs.

A serious growth phase is currently underway, with an expected compound annual growth rate (CAGR) for wafer bumping in flip chip in package at 10.5% during 2010 to 2016, which is 2 points higher than the CAGR forecasted for the average semiconductor industry. 2011 will be the first year to exceed 10M bumped wafer starts for flip chip, and fab utilization is also greater than 95%.

## Why flip chip, Why now?

Flip chip technology isn't new. But its recent evolution toward copper pillar bumping is rapidly being adopted for consumer, telecom, and industrial applications as a leading alternative to

solder in the rush to meet RoHS lead-free interconnect requirements by 2014. More importantly, while it was previously driven mainly by performance (and by the I/O interconnect gap resulting from the relentless Moore's law), it's now increasingly being driven by cost concerns. Additionally, new underfilling technologies and materials are enabling lower-cost flip chip assembly flows with good reliability.

Historically, flip chip technology has been considered excessively costly. As such, the main driver for adopting flip chip technology has never been low cost; it's always been electrical and thermal performance for high-speed processors or for RF power amplifiers. It's also performance driven — a different sort of performance — because it's about light efficiency for high-power LEDs; and for CMOS image sensors and SAW filters, it's size or hermeticity, respectively.

We may actually see flip chip prices drop significantly as volumes keep on increasing. Flip chip costs are expected to decrease slowly and progressively, but it is already very competitive with a number of packaging platforms that use wire bonding. It's important to note here that the increasing price of gold isn't one of the primary factors behind the demand for flip chip, because copper wire bonding is now widely used across all applications.

## Copper pillar bumps

A significant evolution in flip chip technology, the copper pillar bump's fast growth is quite surprising; as is the fact that a new technology could help with lowering costs in the packaging domain very quickly, and at an industrial scale. This is fairly rare in the packaging domain. Typically, new technologies equate to higher cost. In this case, it appears that it will actually help decrease costs.

One of the key reasons the copper pillar bump is so wildly successful is that it allows for much finer pitches and, at the same time, offers superior reliability and costs less.

Finer pitches are possible because copper can be plated with aspect ratios higher than 1, whereas the alternative solder tends to collapse after reflow. To achieve good reliability, a minimum bump height is necessary. Copper pillar bumps can be fine-pitch and high at the same time. The height, which is the space between the substrate and the IC, helps with ease of flow of the underfill. This means faster flow underfill techniques and lower cost, thanks to copper pillars. In particular, "molded underfill" or "MUF" goes hand in hand with copper pillars and offers significant assembly flow simplifications. Finer pitches also decrease the complexity of routing the substrates by enabling peripheral bumping and "bump on leads" (**Figure 2**). So down the road we'll need fewer

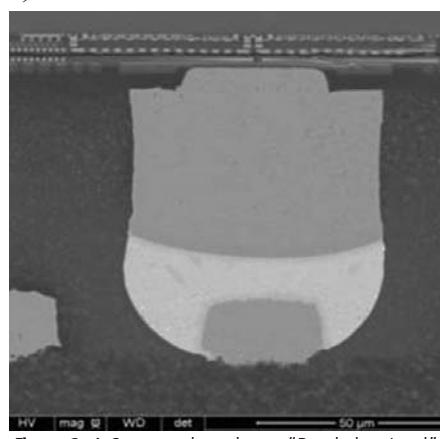


Figure 2. A Copper column bump "Bonded on Lead" (Courtesy of StatsChipPac)



Figure 3. Intel's copper pillar bumped packages

substrate layers, which will also decrease cost. This is incredibly significant when you consider that more than 50% of the cost of a flip chip package is its substrate.

Intel began producing copper pillars in 2007 (**Figure 3**), while the next announcement to come from another company about adopting copper pillars wasn't until 2010 when Texas Instruments and Amkor unveiled a partnership. Others, however, have been using copper pillars more discreetly, to package RF power amplifiers or high side switches.

We expect copper pillars to account for nearly 50% of the flip chip wafer bumping count in 2016 — with the total more than double than that of solder bumping wafer count. The overall flip chip market has a CAGR of 8%. This may seem low, but it's because some applications grow fast while others remain flat. Our forecast for copper pillar bumping for 2010 to 2016 is at a CAGR of 20%. When you think that flip chip (and semiconductor) world leader, Intel, switched to copper pillar bumps years ago, a 20% compound annual growth rate is quite impressive. Copper pillar bumping will overtake the #1 position in bumping technologies by 2013. Currently, gold-plated bumps for LCD driver ICs are #1, but are expected to remain flat in the coming years.

### Supply chain restructuring underway

TSMC is making massive investments in wafer bumping for flip chip and is now in position to vie with outsourced semiconductor assembly and test (OSAT) providers to provide this service. How

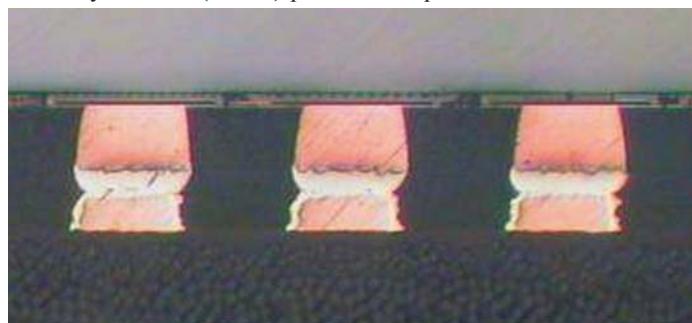


Figure 4. Cross section picture of Copper pillar bumps, (Courtesy of Amkor Technology)

might OSATs react? A smart way to retaliate is to focus on R&D—because no packaging R&D is done without the OSATs. They lead most materials and process flow innovations. And right now, Amkor (**Figure 4**) and STATSChipPAC are getting lots of publicity about their copper pillar bumping, which is something TSMC doesn't have yet. Concurrently, a new business model—that of the “wafer bumping houses” specializing in wafer bumping services—has emerged as a significant player type in this market. All of this equates to some rather serious changes going on in the supply chain at the moment.



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But, during the next 3 years, we're likely to see foundries gain the upper hand with wafer bumping. The OSATs, however, will more than likely maintain their strong positions in both wafer bumping and assembly. Their business model enables them to control the supply chain well, because they provide the complete set of flip chip services, including package design and qualification, wafer bumping, substrate in-sourcing, assembly, and final test.

So it would be exaggerating to say that value flows from the traditional back-end players to the front-end foundries. To some extent, this is true, but in the end, it seems that everyone has something to earn from this market growth, except maybe for the substrate manufacturers, who will need to invest into new technologies like lower CTE or thinner substrates while being able to keep track of customers' requested cost-down roadmaps.

By largely contributing to the consolidation of the "mid-end" wafer-level packaging infrastructure, flip chip favors the fast growth of 3D wafer-level packaging with TSVs (they require similar infrastructures) and will benefit from it through the fast growth of silicon to silicon microbumping, and emergence of silicon and glass interposers in flip chip packages. This is another serious threat to high end IC substrate manufacturers: silicon and glass interposers are a direct threat, and as ICs go 3D, substrate-consuming technologies such as package-on-package will be phased out. Fast-growing substrateless fan-out wafer-level packaging technologies (such as Infineon/Intel's eWLB) are fueling this paradigm shift.

## Extreme growth ahead

Flip chips are everywhere. They can be found in virtually every hot portable handheld device and gadget, application processors, transceiver ICs, power amplifiers, power management units, CMOS image sensors, telecom infrastructure applications, automotive headlights and general lighting appliances.

The flip chip market essentially started from scratch about 15 years ago and has reached a remarkable \$16B in that time. As the technology evolves, matures, and its cost decreases, flip chip growth should only continue to soar. 

*(continued from Page 37)*

*Editor's Note: This agenda is subject to change, and more speakers will be announced as they are confirmed. Stay tuned for program updates on 3D InCites ([www.3dincites.com](http://www.3dincites.com)) and in the July issue of **CSR Tech Monthly**. Details can also be found at [www.semiconwest.org](http://www.semiconwest.org).*

## Sneak preview of MEMS programs at SEMICON West

This year's main MEMS program at SEMICON West gathers some sector leaders on Tuesday morning, July 12, to discuss the future of the industry as more of its output moves from a niche business into high volume markets. Speakers include:

- Rakesh Kumar, Director, MEMS, Global Foundries, will talk about applying learnings from the CMOS industry to MEMS foundry production.
- Jean-Christophe Eloy, CEO, Yole Développement, presents the MEMS technology roadmap, and how new processes and industrial infrastructure will enable new applications.
- Claude Jean, EVP and GM, Foundry, Teledyne Dalsa, will address specialty foundry issues and new technologies.
- Jo De Boeck, SVP Smart systems & Energy Technology, IMEC, will report on MEMS platform opportunities and SiGe options.
- Gary O'Brien, Director Advanced MEMS Design, Robert Bosch, will discuss new developments coming out of the labs.
- Matt Crowley, VP Corporate Development and Founder, Sand9, will update attendees on developments in packaging technology and oscillators for wireless.

## 2011 IW LPC Sponsor Update

Sponsorships continue to roll in for this year's 2011 International Wafer Level Packaging Conference. The SMTA and Chip Scale Review are

pleased to announce an additional Platinum Sponsor, NEXX Systems; as well as several Gold Sponsors including NANIUM, Europe's largest outsource semiconductor assembly and test service (OSAT) provider; STATS ChipPAC, one of the top 5 OSATS worldwide, and packaging equipment manufacturer, Pac Tech.

### Platinum Sponsor

NEXX Systems, Inc. manufactures semiconductor equipment designed expressly for wafer level packaging processing (WLP), addressing the demanding economic and process flexibility

requirements of the semiconductor packaging industry. The Company has two product lines: Stratus, an electrodeposition system offering breakthrough technology that combines the process advantages of vertical wafer orientation with the economic advantages of parallel processing; and Apollo and Nimbus, sputter deposition systems designed to provide high throughput and productivity, with low consumables cost.

### Gold Sponsors

NANIUM provides design, development, engineering, and small to high volume manufacturing services for semiconductor



packaging, assembly and test, operating namely in WLP and in traditional substrate and leadframe based packages. NANIUM was one of the first companies worldwide offering high volume manufacturing for fan-out WLP on 12" wafer, based on Infineon Technologies' eWLB technology. The company is continuously developing new solutions, like System-in-Package (SiP) at the wafer level, to stay at the leading edge of this technology. Thanks to 15 years' experience in the semiconductor business (as former Siemens Semiconductors, Infineon Technologies, and most recently Qimonda Portugal), NANIUM has a highly qualified and competent team and state-of-the-art equipment and facilities, ready to provide services beyond its



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STATS ChipPAC Ltd. is a leading service provider of semiconductor packaging design, bump, probe, assembly, test and distribution solutions. The company has the scale to provide a comprehensive range of semiconductor packaging and test solutions to a diversified global customer base servicing the computing, communications and consumer markets.

Pac Tech Packaging Technologies is a worldwide leader in WLP services and equipment. Pac Tech has over 15 years of experience in



the industry and has manufacturing sites all around the world, including: Germany, United States, Japan, and Malaysia. These sites can supply both engineering and prototyping services, as well as high volume production. Pac Tech is structured to provide a single source for all contract bumping services, as well as providing turn-key WLP Equipment.

*There are still 2 silver level sponsorships available, as well as coffee break, reception, lunch, and WiFi sponsorships. Contact Kim Newman at [knewman@chipscalereview.com](mailto:knewman@chipscalereview.com).*

## 2011 IWLPC Program Takes Shape

The technical committee has been hard at work recruiting keynote speakers and organizing panels to make certain the 2011 International Wafer Level Packaging Conference (IWLPC), October 3-6, 2011 is the best it's ever been. Confirmed keynote speakers include Matt Nowak of Qualcomm and Bill Bottoms, of 3rd Millennium Test Solutions. Additionally, each conference day (Oct. 5 and 6) will feature a panel discussion, one titled The Effect of Infrastructure on Technology Adoption, and the other Will 2.5D and 3D Compete or Coexist?

The four day event begins with two full days of Process and Six Sigma Certification workshops. Exhibits and tech sessions comprise the remainder of the two conference days, offering full technology tracks on 3D, Wafer Level Packaging, and MEMS and many exhibitors showcasing their products and services that support these market sectors.

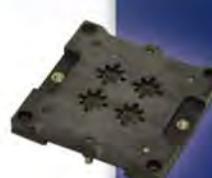
## 3D Panel Will 2.5D and 3D Compete or Coexist?

The introduction of 2.5D silicon interposer solutions to meet the performance, size and cost requirements of next generation consumer electronics has the industry questioning whether this is an interim solution while 'true' 3D addresses remaining limitations of thermal, supply chain infrastructure and cost of test issues; a complementary solution for 3D systems, or an alternative avenue to 3D TSV altogether? In other words, will 2.5D and 3D compete or coexist? This panel will discuss the motivations of these scenarios from the perspective of their core competencies. Confirmed 3D panelists include Ron Hoemueller Sr. Vice President of Adv 3DIC, Scott Jewler, Chief Engineering, Sales and Marketing Officer at Powertech Technology; and Phil Marcoux, of PPM Associates, consultant for TSV technologies. Additional panelists will include experts in thermal management,



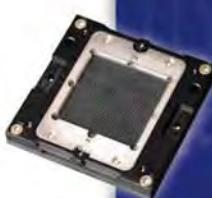
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design, test, and an end user, and will be announced as their participation is confirmed.

## WLP Panel: The Effect of Infrastructure on Technology Adoption

The adoption of any new semiconductor technology depends heavily on the state of the existing technology infrastructure. The IC-packaging industry is no exception. Established relationships and physical structures represent challenging obstacles, and enabling advantages, for new semiconductor technologies. This panel will discuss and evaluate the existing industry infrastructure and the technological momentum driving, and regulating, adoption. It will also discuss the role of infrastructure in determining technological progress. Panelists will include packaging experts drawn from top analyst firms, key trade media and leading industry innovators, and will be announced as participation is confirmed.

## MEPTEC/SMTA Medical Electronics Symposium Call for Papers

SMTA and MEPTEC will once again be joining forces to present the Medical Electronics Symposium, September 27-28, 2011. The two-day technical program titled "Medical Electronics-Vital Technologies for Health" will be held September 27-28, 2011 at Arizona State University in Tempe, AZ. ASU's School of Biological and Health Systems Engineering will co-sponsor this event.

This symposium will focus on medical

electronics and medical device applications. The technical committee is soliciting abstracts from within the medical community that will share the most up to date information about company electronics expertise, practices, technology and applications as it relates to the symposium topics. Deadline for abstracts is June 1, 2011.

Session topics include:

- Market Trends & Forecasts in Medical Electronics
- MEMS Technologies for the Medical Industry
- Manufacturing Technologies and Standards
- Latest Developments in Implantable Products and Applications
- System Level Products and Applications-instrumentation (defibrillators, etc.)
- Materials and Design
- Systems Manufacturing (i.e. PWB/PCB assembly, stacked packages)
- Reliability/Safety/Regulatory/Testing

The abstract and presentation must be non-commercial in nature and emphasize the medical technology and not the company portfolio. Please include your contact information (address, phone number, email address) and a presentation title with your abstract submission. Please provide an abstract of 300 words minimum on any of the topics above by email to [bcooper@meptec.org](mailto:bcooper@meptec.org) (for first four topics) or [patti@smta.org](mailto:patti@smta.org) (for last four topics). There is no technical paper requirement for this symposium. Presentations are due on August 30, 2011.

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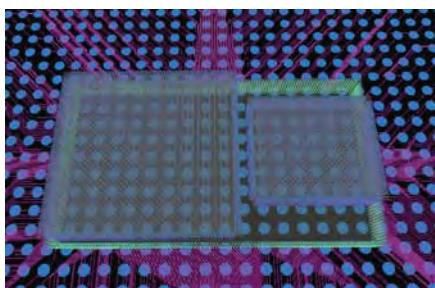


Figure 6. TSV placement and assignment to minimize cost and maximize routability

stacking can improve system performance and not break the bank. However, it's not enough to show that the system is routable, but that the physical layout can support the required data speeds. The ability to verify signal and power integrity over the complete 3D stack is thus the final essential component of the 3D pathfinding tool. A true-3D tool, which has all the connectivity and electrical information for the TSVs and 3D interconnects in place, is the ideal engine for extracting the full parasitic

network of the 3D structure. In pathfinding mode, approximate algorithms are sufficient to provide confidence in performance estimates; however, the same engine can be used to provide the inputs to more detailed analyses as needed later on in the flow.

## Conclusion

By choosing as an example a very basic 2.5D design case to illustrate how a true-3D pathfinding tool can identify cost savings while re-using existing components, we wanted to show that it's not necessary to start from scratch and re-architect entirely new systems to reap the benefits of 3D integration. This being said, one can only imagine how much more can be achieved by pushing the analysis to a finer level.

The pain of 3D design comes largely from the need to perform multiple different types of operations — partitioning, routing, extraction, etc —

that heretofore required different tools, each having different file formats, and that were not designed to support multiple technologies. A single true-3D pathfinding tool, such as presented here, which does communicate gracefully with the rest of the flow, is what is required to remove this pain.

The fear of 3D design — at least that part which is due to uncertainty in cost and performance benefits — comes from having to take a leap of faith on inexact models at the front end of the design flow, not knowing if these will hold up by the time it reaches the end. It is absolutely vital to have a tool that can dive into the physical design space at an early stage to validate the performance predictions and to provide accurate data for cost modeling. With such a tool in hand, there is absolutely nothing left to stop anyone from seeing how they can profit from 3D integration. 

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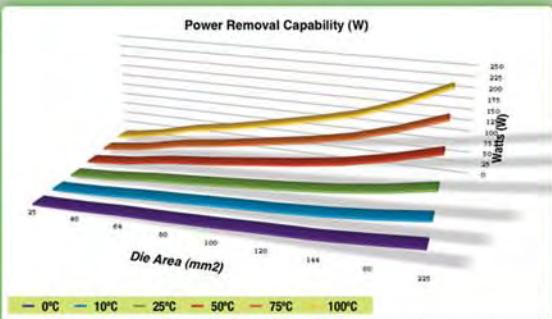
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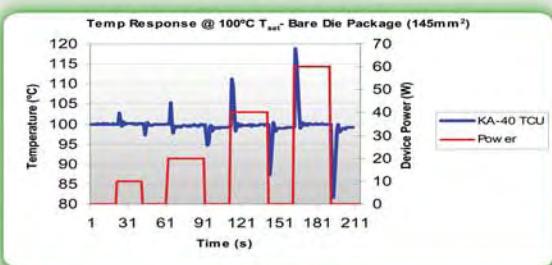
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