

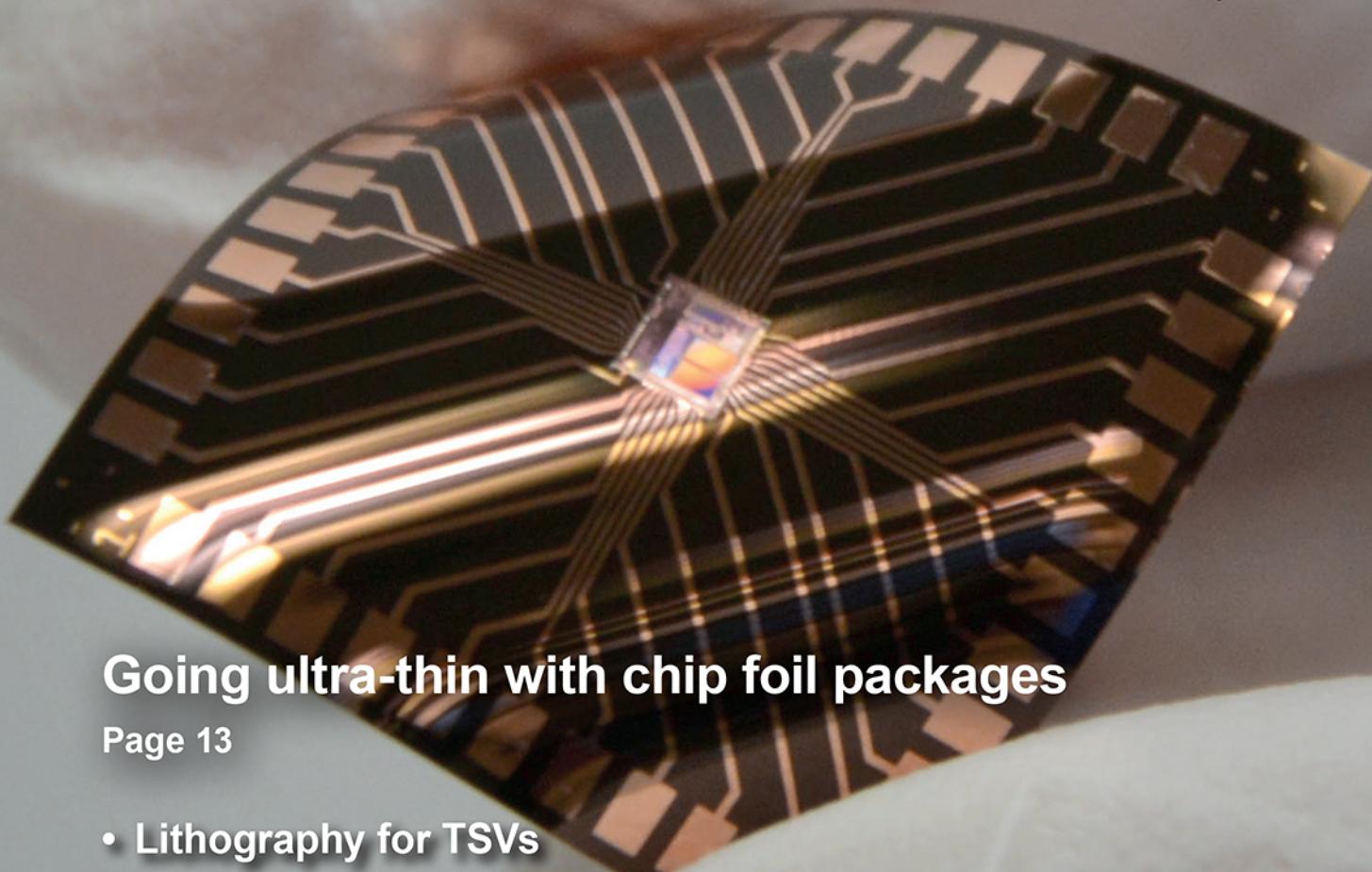
# Chip Scale Review®

ChipScaleReview.com

*The Future of Semiconductor Packaging*

Volume 20, Number 2

March • April 2016



## Going ultra-thin with chip foil packages

Page 13

- Lithography for TSVs
- IoT and MEMS packaging
- Heterogeneous integration
- Packaging of high-power devices
- 3D packaging and WLP processes
- Next-generation Cu pillar plating technologies





invent

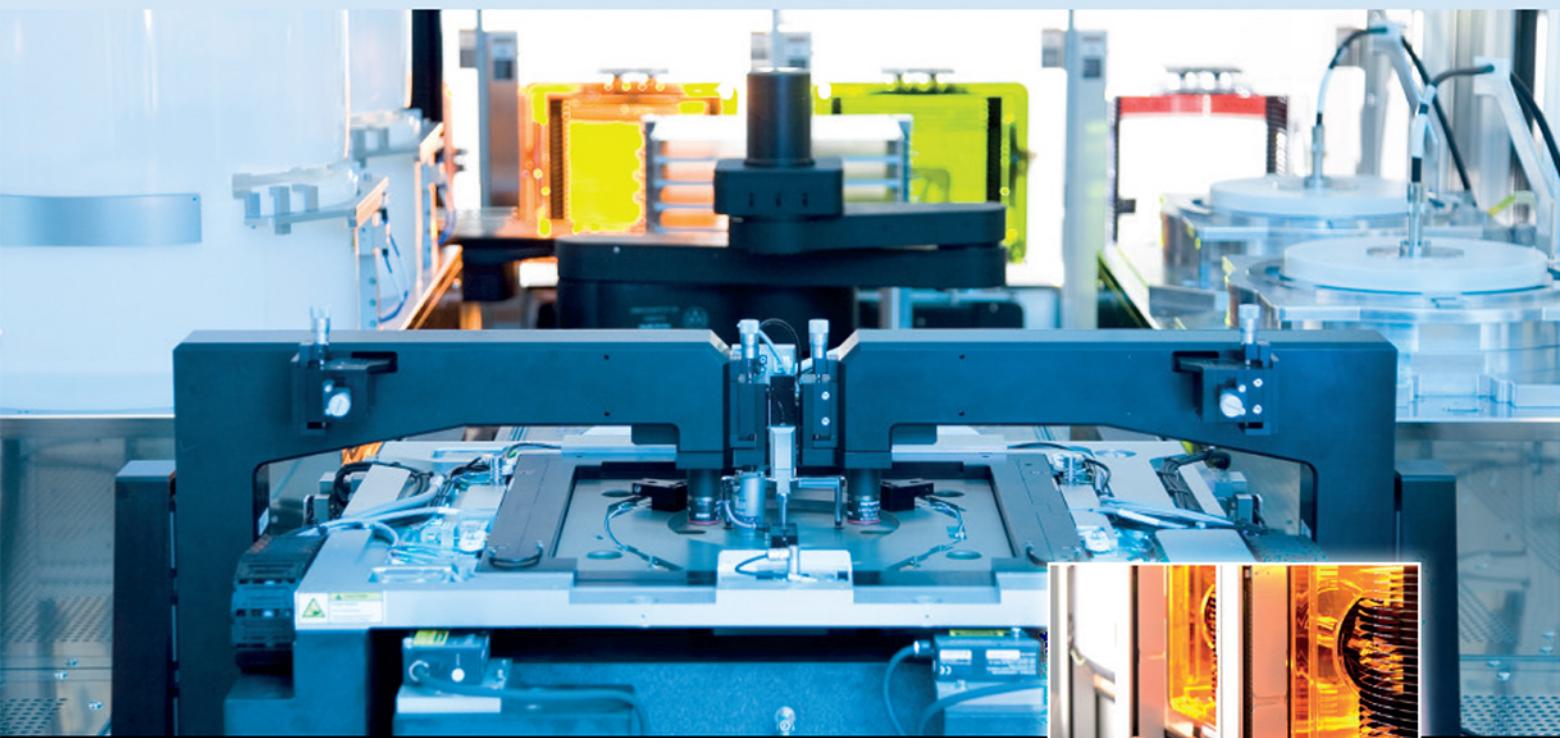
innovate

implement

[www.EVGroup.com](http://www.EVGroup.com)

## Solutions for 3D Integration and Advanced Packaging

- ▶ Fusion & hybrid bonding for 3D wafer stacking
- ▶ Temporary bonding and debonding for thin wafer processing
- ▶ Lithography for advanced packaging



**GET IN TOUCH** to discuss your manufacturing needs  
[www.EVGroup.com](http://www.EVGroup.com)

# CONTENTS

March • April 2016  
Volume 20, Number 2



In the thin chip foil package, ultra-thin dies are placed in a cavity of a film laminate, which results in a bendable fan-out chip package with the fragile IC securely embedded in the center layer. The capability to bend flat chip packages and mount them onto curved surfaces will enable new sensing applications in production environments, healthcare, robotics and potentially any aspect of our daily life.

Photo courtesy of Fraunhofer EMFT

## DEPARTMENTS

<b>In Memoriam</b>	Eugene R. Selven	2
<b>Market Update</b>	3D packaging and WLP processes Mark Thirsk <i>Linx Consulting</i>	5
<b>Guest Editorial</b>	Public/private partnerships drive National Photonics Initiative Alan Willner <i>National Photonics Initiative</i>	8
<b>Industry News</b>	BiTS 2016: Exploring the impact of IoT and Big Data	54



**Connecting People and Technology**

As one of the world's largest suppliers of outsourced semiconductor packaging design, assembly and test services, Amkor helps make "next generation" products a reality.

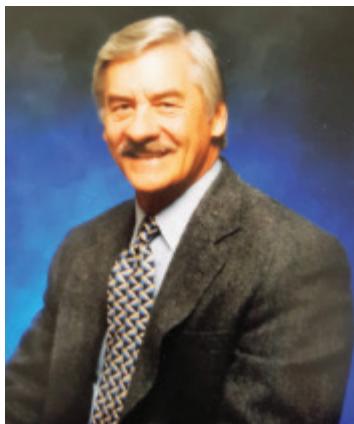
Our continuous path of innovation, improvement and growth has led us to be a strategic and trusted packaging partner for many of the world's leading semiconductor companies.

As industry moves aggressively toward new and more complex technologies, our unique expertise in high-volume manufacturing techniques and the ability to solve technological challenges are among our greatest strengths.

Customers also benefit from our extensive and expanding global footprint, enabling us to easily handle large orders and offer quick turnaround times. Amkor is positioned to deliver end-to-end solutions that meet the requirements for a broad range of product designs today, and in the future.

[www.amkor.com](http://www.amkor.com)

# IN MEMORIAM



A LEGEND, AND A LIFE WELL LIVED

## *Eugene Ronald Selven*

Publisher, *Chip Scale Review*  
1999-2008

1932 – 2016

**T**hose who were fortunate to have known Gene Selven recall a passionate, remarkable person in both business and leisure. His presence would fill a room—there was no escaping it. He was also passionate in everything he did. If you are new to the industry and didn't know Gene, there are many still around from the "good old" days that worked with him. "Gene was a terrific icon in the electronics industry," notes Mary Ann Olsson, an industry analyst who was introduced to Gene through industry colleagues. "One of my first bosses always told me to call Gene for the right answers. He was always sweet and helpful to me during the early years of my electronics research. He was a good soul!"

Born in Chicago, Illinois, Gene received his Bachelor of Science degree in Electrical Engineering from the University of Illinois in 1954, and then served in the U.S. Army from 1954-1956, stationed in Japan. Beginning his early career at IBM, he moved out of state to California as Manager of Product Marketing at Texas Instruments in the Semiconductor Division. In 1969, he moved his residence to beautiful Portola Valley in Northern California where he began working as the Director of Product Marketing at Fairchild. In 1971, he joined the Semiconductor Division of Raytheon as Director of Marketing.

In 1976, Gene successfully started and grew his own company and expanded into publishing—purchasing the magazine *Chip Scale Review* from Tessera in 1999. His daughter, Kim, continues that legacy today. An early admirer of Gene, Tom Di Stefano of Centipede Systems remembers Gene as always generous and considerate. "Gene Selven built several publications into industry standards in his lifetime," said Di Stefano. "In his most recent endeavor, he grew *Chip Scale Review* to a leading position in the semiconductor industry. As an advisor to the magazine, I was always delighted by Gene's wisdom and insight in handling the many challenges that arose."

Gene will be remembered as a true gentleman who kept his cool and resolve at all times—a true leader. Andrea Roberts of AR Marketing, says, "He was a wonderful man—and so passionate about the industry and communicating about it. I would always brighten up when I'd see him at a trade show. He was an institution in the industry, and although he was away from the industry for a number of years, he will be missed."

Having traveled the world several times, Gene was an international traveler both in business and his personal life. An avid fisherman, he loved to fish on Lake Tulloch, and often traveled to Alaska over the years to catch halibut and salmon. Golf was another passion. The San Francisco 49ers and Giants were his favorite teams and he was a season ticket holder of both for many years. Having grown up with the Chicago White Sox, however, it bears "special mention" that he also considered that team to be his roots.

Gene is survived by his two daughters, Kimberly Newman of Campbell, California, and Karen Williams of San Jose, California, grandson James Newman of Campbell, and his sister, Shirley Jensen of Lawton, Michigan. Services were held on March 30th. Donations can be made in Gene's honor on the Alzheimer's website on the (donate) tribute page under Gene Selven ([www.alz.org](http://www.alz.org)).

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

## STAFF

**Kim Newman** Publisher  
knewman@chipscalereview.com  
**Lawrence Michaels** Managing Director/Editor  
lxm@chipscalereview.com  
**Debra Vogler** Senior Technical Editor  
dvogler@chipscalereview.com

## CONTRIBUTING EDITORS

**Roger H. Grace** Contributing Editor - MEMS  
rgrace@rgrace.com  
**Jason Mirabito** Contributing Editor - Legal  
jason@isusip.com  
**Dr. Ephraim Suhir** Contributing - Editor - Reliability  
suhire@aol.com

## EDITORIAL ADVISORS

**Dr. Andy Mackie (Chair)** Indium Corporation  
**Dr. Rolf Aschenbrenner** Fraunhofer Institute  
**Joseph Fjelstad** Verdant Electronics  
**Dr. Arun Gowda** GE Global Research  
**Dr. John Lau** ASM Pacific Technology  
**Dr. Leon Lin Tingyu** National Center for Advanced Packaging (NCAP China)

## SUBSCRIPTION--INQUIRIES

Chip Scale Review  
All subscription changes, additions, deletions to any and all subscriptions should be made by email only to  
subs@chipscalereview.com

Advertising Production Inquiries:

**Kim Newman**  
knewman@chipscalereview.com

Copyright © 2016 Haley Publishing Inc.  
Chip Scale Review (ISSN 1526-1344) is a registered trademark of Haley Publishing Inc. All rights reserved.

Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. In the U.S. subscriptions by first class mail are \$125 per year. Subscriptions outside of the United States are \$225 per year to other countries.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January–February, March–April, May–June, July–August, September–October and November–December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

## FEATURE ARTICLES

<b>Thin chip foil packaging: An enabling technology for ultra-thin packages</b> Christof Landesberger, Nagarajan Palavesam, Andreas Drost, Waltraud Hell, Robert Faul, Christoph Kutter <i>Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT</i>	13
<b>Through-silicon via-last lithography for 3D packaging</b> Warren Flack, Rezwan Lateef <i>Ultratech, Inc.</i>	16
<b>Next-generation copper pillar plating technologies</b> Cassandra Melvin, Bernd Roelfs <i>Atotech Deutschland GmbH</i>	20
<b>The X-ray metrology of TSVs</b> David Bernard, John Tingay, Philip Moyse, Will Heeley <i>Nordson DAGE</i>	25
<b>The Internet of Things and MEMS packaging</b> Vik Chaudhry, Adrian Arcedera <i>Amkor Technology, Inc.</i>	32
<b>Die-to-wafer stacking enables the future of 3D integration</b> Teng Wang <i>imec</i>	36
<b>Power module packaging: the “Promised Land”</b> Coralie Le Bret <i>Yole Développement</i>	38
<b>Fine-pitch stacking on a carrier wafer</b> Chen Hong Ciou, Hsiao Chun Huang, Hsien Wen Chen, Stephen Chen, Mike Ma <i>Siliconware Precision Industries Co., Ltd. (SPIL)</i>	43
<b>Avoiding low-cycle fatigue in solder materials using inhomogeneous column grid array (CGA) design</b> Ephraim Suhir <i>Portland State University</i>	46

## QUALITY IS EVERYTHING

Your yield. Your profitability. Your reputation depends on 100% quality assurance for every wafer, device and package.

Sonix is the leader in ultrasonic technology and expertise for inspecting wafer bonds, device interconnects and package integrity.

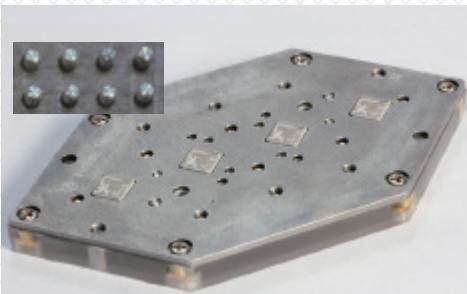
Find smaller defects faster, at any layer. Learn more and request a free sample analysis at [Sonix.com](http://Sonix.com).

**sonix™**

© 2016 Sonix, Inc. All rights reserved.

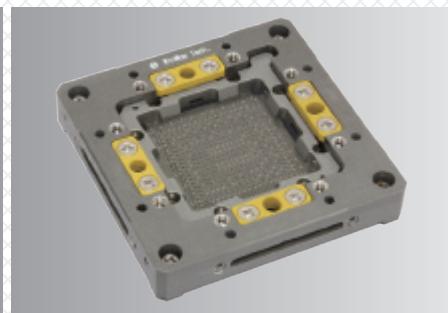
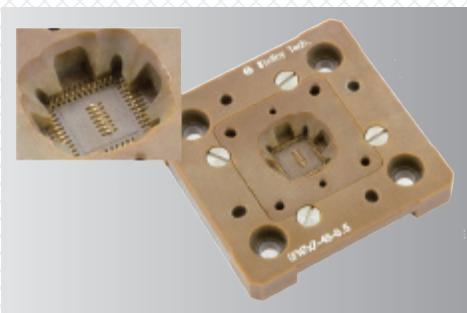
# YOUR TRUSTED PARTNER IN IC TEST

**WLCSP**



**Vertical  
Probe Card**

**W-Pin**



**High Speed  
Brownie Socket**

## Semiconductor Test Engineering Center



## Thermal Control System



ATC Controller

Plunger

Thermal Head

Manual Lid

High Performance  
Contact Solution

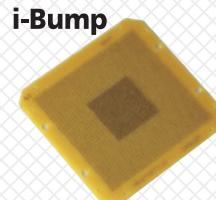
Spring  
Probe



W-Pin



i-Bump



PCR®



# MARKET UPDATE



## 3D packaging and WLP processes

By Mark Thirsk [[Linx Consulting](#)]

In recent years, through-silicon via (TSV) processes have been promoted as one solution to high-density 3D chip-scale packaging. Simultaneously, however, multiple proprietary packages have been developed that achieve some level of chip-scale packaging requirements, but that do not go all the way to meeting the definition of being true 3D technologies. Here, we look beyond the long list of proprietary package types to make some sense of the manufacturing processes used in these 3D and wafer-level packages, the equipment needed, and the bill of materials to achieve success. We will also highlight the differences and commonality in the process approaches and cost assumptions for each technology.

Market size estimates for the value of the module market by ASE are on the order of \$60Bn for 2015, with a CAGR of better than 10% through 2018. Packaged modules are close to the size of the chips being packaged, and include hybrid systems that include ICs and passives. Advanced packaging technologies can be seen as enabling the Internet of Things (IoT), and extending the scaling of advanced devices. As packaged modules are developed for various applications, manufacturers strive to meet the performance, power, and cost (PPC) requirements set by the system designer. Different package types meet the needs for different system types for segments such as mobile or computing, and each competitor in the market attempts to develop proprietary packaging technologies and designs that leapfrog competitors, result in a dizzying list of package types being introduced to the market. This article attempts to develop a coherent view of the segmentation of these package types through the analysis of the manufacturing technologies and materials used to create the final package.

### Wafer-based TSV-packaged devices

For much of the last decade, discussion of 3D packaging using TSV technology has been the center of an approach to develop very high-density hybrid or stacked device packages. The TSV package raises many concerns in implementation, however. Among these is the requirement for a known good die (KGD) approach to packaging that precludes a full wafer approach. In addition, the design and engineering required to apply TSV I/O to either similar or hybrid device stacks is significant, and only lends itself to runs of large numbers of units. For these reasons, TSV technology has found applications primarily in DRAM dual inline memory module (DIMM) packages.

### Alternative wafer-based packages

A reevaluation of the basic expectations of packaging technology supports the conclusion that multiple alternative packages may be a more effective approach to addressing packaging challenges. Each package has to optimize a list of properties consistent with the system design and the device type. These properties include: 1) Package footprint; 2) Package cost; 3) Package height; 4) Board-level bump pitch; 5) Device types required in the package; 6) Interconnect redistribution between silicon device and pitch, and output bump pitch; 7) Passive devices required for package function; 8) Heat removal requirements; and 9) 2D, 2.5D or 3D.

Package designers have approached these challenges with the introduction of interposers that can achieve much of the interconnect redistribution requirements, as well as supporting the mounting of multiple devices in one package, either side-by-side in a single layer, or in a vertical stack of two or

more devices with wire bond, or more advanced interconnect approaches. The required package functionality is tightly constrained by the overall package cost. Packages that are too costly for the applications they are meant to address will not be accepted by final customers.

Until recently, silicon scaling has outpaced package integration complexity, enabling advanced devices to be integrated primarily on silicon. The effective slowing of scaling is countering this trend because the rising cost of integrating system components into complex silicon designs in the most advanced technologies (system-on-chip) is not offering expected cost savings. Advanced packages can mitigate this by combining multiple lower cost devices into an acceptable package form factor to deliver product functionality; this is commonly designated as a system-in-package (SiP).

A secondary concern in package design is that of time-to-market. Integrated device manufacturers with extremely high unit sales are able to design packages in parallel with device development, and make the required layout compromises to develop highly integrated package designs such as stacked 3D TSV packages. For smaller production runs that are constrained to very tight market windows, however, standard packaging solutions tend to be preferred as they enable faster design turnaround.

### Redistributed integrated silicon packages (RISP)

Approaches to meeting the challenges of providing silicon packages that integrate one or more silicon devices, with appropriate interconnect redistribution, can be termed redistributed integrated silicon packages (RISP). The greatest challenge in the integration of RISPs is in developing the appropriate processes for wafer-level interconnect redistribution.



**LD microprecision sdn bhd**

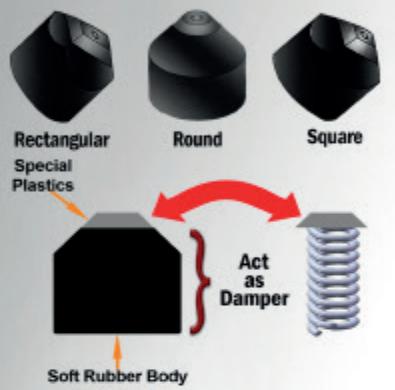
## Does Die YIELD LOSS Matter To You?

### Hybrid Rubber™ Tips

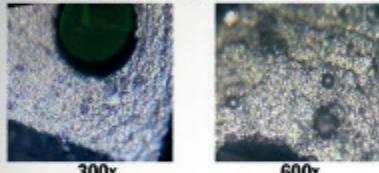
Patent No: PI 2014702292 & PCT/MY2015/050036

#### Solve:

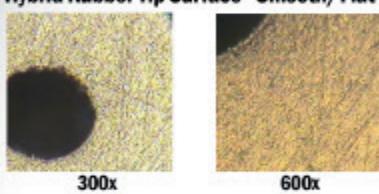
- Crack die
- Sticky tips surface
- Missing die
- Uneven tips surface
- Stack die
- Shorter tips life span
- Low temperature
- Foreign particles on die



#### Current Rubber Tip Surface - Pimples



#### Hybrid Rubber Tip Surface - Smooth/Flat



#### Other Products



YOUR GLOBAL SEMICONDUCTOR / LED  
PACKAGING SOLUTIONS PROVIDER

[www.ldmicroprecision.com](http://www.ldmicroprecision.com)  
[sales@ld-micro.com](mailto:sales@ld-micro.com)

RISPs use a combination of technologies that have various pitch capabilities. Each technology is best suited to one or more regimes of production as shown in **Figure 1**.

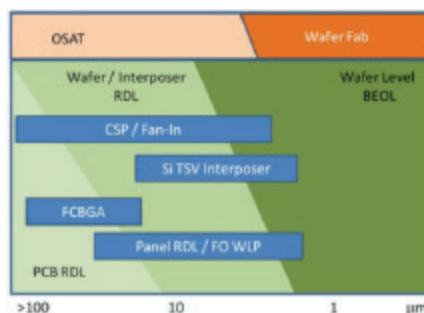


Figure 1: RISP production technologies.

### Wafer-based packaging

Since the mid-80s polymer stress buffer (PSB) techniques have been used to interface bonding pad technologies to the package interconnect. In PSB, the solder ball sits directly over the bond pads. These technologies, still in use today, have been the precursor for the redistribution layer (RDL)/fan-in technology. Processing uses liquid dielectrics such as, polyimide (PI), polybenzoxizole (PBO), and BCB, as well as sputtering technologies to deposit seed metal layers. In some cases, CVD dielectric deposition may replace liquid polymers. Equipment sets are repurposed fab tools with stepper-based lithography. This approach employs wafer-fab technology that results in relatively high equipment depreciation costs and material costs, but high interconnect densities. Package sizes are kept to the size of the silicon die.

Through-silicon via (TSV) approaches use front-end technologies to prepare the wafer for advanced frontside or backside redistribution layer (RDL) technology. Most wafer-based TSV approaches require an interposer to interface with the chip, but true 3D packages have been commercialized by Micron and Samsung in DRAM packages.

Materials and processes required for a TSV process include: 1) Wafer bonding; 2) Photoresists; 3) Plasma via etching; 4) Chemical vapor deposition (CVD) or atomic layer deposition (ALD) isolation oxide; 5) Physical vapor deposition (PVD) barrier and seed; 6) Electrochemical deposition (ECD) copper via fill; 7) Copper CMP; 8) Barrier CMP; 9) Wafer backgrinding/thinning; 10) Via reveal/silicon etch; 11) Oxide CVD and CMP; 12) Wafer debonding; and 13) Cleaning.

Required equipment sets need to be wafer fab compatible and thus, as with fab-based fan-in technology, process costs and equipment depreciation are consistent with other fab processes, and are relatively high with CMP tools averaging \$4M, and plating systems approximately \$1-2M.

### Reconstructed wafer technologies

In response to the very high costs and slow cycle time of wafer-level TSV technologies, reconstructed wafer technology supporting wafer-level fan-out, including multiple chips, stacked, and hybrid packages, can take advantage of packaging multiple known good die. Substrates can be inorganic, such as silicon wafer or glass-based, or organic, such as overmolded polymer films. Generally, the substrates support redistribution layer (RDL) processing, and devices can be placed before or after interconnect processing. After placement, devices are overmolded

Substrate Type	Type	RDL Pitch	Equipment Type	Materials	Typical Production Type
Wafer	PSB	10 - 100	Wafer Fab / BEOL	PVD seed liquid dielectric Plated metal	Wafer Fab
	RDL / Fan-in	1-100	Wafer Fab / BEOL	PVD seed liquid dielectric Plated metal	Wafer Fab
	TSV	>10	Wafer Fab / BEOL	PVD seed CVD dielectric Plated metal	Wafer Fab OSAT
Reconstructed Substrate (Wafer or panel)	FO WLP Inorganic Substrate	1 - 100	OSAT	PVD seed liquid dielectric Plated metal	OSAT
	FO WLP Organic Substrate	10 - 100	OSAT	Liquid seed Film dielectric Plated metal	OSAT
Interposer	Si based TSV	1 - 100	OSAT	PVD seed Liquid dielectric Plated metal	OSAT
	Glass	1 - 100	OSAT	PVD seed liquid dielectric Plated metal	OSAT
	Organic	10 - 100	OSAT	Liquid seed Film dielectric Plated metal	OSAT

Table 1: Summary of signal redistribution layers by segment.

with organic resins to provide support and protection.

RDL processes can generally be run with sputter deposited, plated metals, and either film dielectric, or liquid dielectric, although thermal budgets for organic reconstituted substrates to not allow high-temperature liquid dielectric use.

Packaging technology is consistent with interposer or board-level manufacturing, using lower-cost tooling, and high-throughput steppers or contact lithography with liquid or dry film. This provides relatively low-cost processing, although when implemented at an outsourced semiconductor and test (OSAT) supplier, almost all processing equipment may need to be purchased solely for this process. In the most advanced processes, interconnect pitches can be as low as 1 to 2 $\mu$ m, allowing complex redistribution.

In many cases, reconstituted wafer-level packaging does still require an interposer substrate. Sometimes, TSV silicon is used for the interposer, and recently, Amkor has proposed defining the RDL on a sacrificial silicon substrate that is removed before bumping, resulting in a silicon-less package (SLIM).

There are many similarities between panel RDL processing and early-generation display manufacture. Some panel manufacturing may be carried out using FPD (flat panel display) processing tools. Package processes for reconstituted substrates include: 1) Placed chips on substrate film; 2) Overmolded resin; 3) Dielectric deposition – liquid or CVD; 4) Via lithography, and dielectric etch – liquid or plasma; 5) Seed deposition – liquid or PVD; 6) Interconnect lithography; 7) Copper plating of interconnect; 8) Resist strip, and etch seed; 9) Pillar formation; and 10) Substrate film removal, and back grinding. Drawing from this analysis we can summarize that signal redistribution layers can be segmented as shown in **Table 1**.

## Summary

We anticipate that RISP development will continue and will become more important in meeting market expectations. RISP devices will offer higher levels of integration with smaller footprints to meet the design requirements of advanced mobile and computing systems. Additionally, the high functionality offered by RISP modules will lead to increasing value according to the packaging operations.

The continued optimization of package cost may drive the migration of some

signal redistribution to the fab back-end-of-line (BEOL) to ensure cost-effective implementation. Manufacturers will have to seek the best balance of high-cost wafer fab processing and OSAT processing to meet required package functionality at the lowest economic cost.

## Biography

Mark Thirsk received his BSc in Metallurgy at the U. of Birmingham and is a Managing Partner at Linx Consulting; email mthirsk@linx-consulting.com



**GEORGIA TECH INVITES MATERIAL, TOOL, SEMICONDUCTOR, PACKAGE, ASSEMBLY, TIER 1, TIER 2 AND OEMS TO JOIN ITS INDUSTRY CONSORTIUM**

**NEW ERA OF AUTOMOTIVE ELECTRONICS (NAE)**

*Georgia Tech to Launch Large Scale, Comprehensive and Leading-edge System Integration R&D and Supply-chain Industry Consortium in New Era of Automotive Electronics (NAE)*

New Era of Automotive Electronics (NAE) is expected to account for about a third of the total cost of each car, about \$10,000, potentially creating a market of \$1T within a decade.

The Southeast USA, with Atlanta as a global hub for European, Japanese, Korean and US car and component Tier 1 and 2 companies, presents Georgia Tech, as the top-tier University in this region, with a unique opportunity to contribute to NAE. The challenges in addressing these needs are more complex than any electronic product to date and include both hardware and software.

Georgia Tech is launching the NAE Industry consortium with focus in three areas:

1. Device and package technologies leading to highly miniaturized, low cost and highly-reliable autonomous and all-electric automotive systems
2. Partnership with Tier 1 and Tier 2 global supply-chain companies for R&D in integrated components; and car makers to develop road maps, supply-chain management and standards
3. Education of large number of highly-interdisciplinary engineers who are well prepared for the NAE industry.

Georgia Tech has world-class faculty expertise and infrastructure for the most leading-edge:

- Devices such as SiGe, GaN, photonic, and image sensors
- Highly integrated and highly-miniaturized packaging such as glass-based packaging; high bandwidth digital, RF (5G) and photonics; high-power and high-temperature materials; cameras, radar, and lidar.

Georgia Tech is planning the NAE program launch for May 2016.

For information, contact Prof. Rao Tummala at [rao.tummala@ece.gatech.edu](mailto:rao.tummala@ece.gatech.edu)

Georgia Institute of Technology | 813 First Drive, NW | Atlanta, GA USA 30332  
+1 404 894 9097 | [www.prc.gatech.edu](http://www.prc.gatech.edu)



## Public/private partnerships drive National Photonics Initiative

By Alan Willner [*National Photonics Initiative*]

**L**ook around you — your phone, computer, TV — all modern-day technologies enabled in large part by photonics. Optics and photonics relate to the science and application of light. Specifically, photonics detects, generates and harnesses light to advance manufacturing, health care and medicine, defense and national security, communications, energy and many other industries. Simply put, photonics is lighting our future by addressing and solving the challenges of the modern world. It enhances our quality of life; protects our health, safety and security; and helps drive economic growth, job creation and global competitiveness.

A 1998 National Research Council report, “Harnessing Light,” presented a comprehensive view of the potential impact of optics and photonics on health care, manufacturing, defense, communication and many other industries. Since that report’s release, many countries have significantly increased their national commitments to the optics and photonics industries. For example, in 2011, Germany committed nearly €1 billion (\$1.3 billion in USD) to photonics R&D over 10 years; China began funding several programs targeting photonics supply chains; and the European Commission, as part of its new Horizon 2020 program, has directed €1.6 billion (over \$2 billion in USD) to photonics-related R&D over the next seven years, and has designated photonics as one of only five key enabling technologies for future prosperity.

In 2012, the U.S. National Research Council released a sequel to Harnessing Light, entitled “Optics and Photonics: Essential Technologies for Our Nation,” that called for a National Photonics Initiative (NPI) to increase collaboration and coordination among US industry, government and academia.

Such a collaboration is intended to identify and further advance areas of photonics critical to US competitiveness and maintaining national security. Historically, the United States had been the world leader in deploying photonics research to power cutting-edge technologies, but global competition was threatening this leadership position, causing a substantial loss of global market share to overseas competitors as well as thousands of US jobs.

Heeding the report’s call, the Optical Society (OSA) and the international society for optics and photonics (i.e., SPIE) – two of the nation’s largest premier photonics societies – joined forces to formally launch the NPI in May 2013. OSA and SPIE launched the NPI with the support of the American Physical Society (APS), the IEEE Photonics Society (IPS) and the Laser Institute of America (LIA), as well as backing from industry and academia within the broad-reaching photonics community.

For nearly three years, the NPI has successfully served as an advocate for photonics in Washington, DC and around the country. The NPI is committed to working with the federal government to position the United States as a leader in photonics research and development (R&D) by driving funding and investment in the areas of photonics that are critical to maintaining US competitiveness and national security, as well as to developing federal programs that encourage stronger partnerships between US industry, academia and government labs. A recent example of this collaboration is best demonstrated by the NPI’s work with federal agencies, congressional leaders,

industry and academia on the recently announced Integrated Photonics Institute for Manufacturing Innovation (IP-IMI) – now known as the American Institute for Manufacturing Integrated Photonics (AIM Photonics).

On July 27, 2015, Vice President Joe Biden announced that a consortium led by New York-based SUNY Polytechnic won the competition to be the country’s first photonics IMI (**Figure 1**). More than \$110 million federal investment and \$500 million in non-federal funds make AIM Photonics the largest investment to



**Figure 1:** On July 27, 2015, Vice President Joe Biden announced that a New York-based consortium led by SUNY Polytechnic is the winning location for the country’s first Integrated Photonics Institute for Manufacturing Innovation (IP-IMI).

date in President Barack Obama’s National Network of Manufacturing Institutes (NNMI).

AIM Photonics’ winning proposal was selected by the Department of Defense (DOD) from three finalists. AIM will focus on developing an end-to-end photonics “ecosystem” in the United States, including domestic foundry access, integrated design tools, automated packaging, assembly and testing, and workforce development. It will serve as a hub, bridging the gap between applied research and product

40+ years of  
perfect  
pitch.



And now, the perfect name



**Qi-nex** [kuh-nekts] 1. Over 40 years of reliable burn-in and custom connections; 2. Quality interconnects for **nex**-gen solutions.

Introducing Qinex, the brand name for superior interconnection solutions from Sensata Technologies. Qinex, the new word in perfect pitch.

**QUALITY.** High-value interconnection solutions since 1970.

- ✓ 24/7 global engineering
- ✓ 24/7 global support teams
- ✓ Local engineering and sales
- ✓ Six Sigma quality management
- ✓ Proven, reliable high-volume manufacturing
- ✓ Expert molding, design, and customization

**INNOVATION.** More I/O choices, smaller form factors, superior performance in less time.

- ✓ Latest 3D design tools
- ✓ On-site model shops
- ✓ Rapid prototyping
- ✓ Advanced thermal analysis
- ✓ Design on demand
- ✓ Broad range of innovative contact designs



**PARTNERSHIP.** In a fierce global market, only Qinex reliably supports the innovation, reputation and competitiveness of your business. We'll work with you to get it right, the first time.

Learn more by contacting the experts in perfect pitch:

WEB [www.Qinex.com](http://www.Qinex.com)

EMAIL [QinexCSR@sensata.com](mailto:QinexCSR@sensata.com)

CALL 1-480-682-6148

development by bringing together companies, universities and other academic and training institutions, and federal agencies to co-invest in key technology areas that encourage investment and production in the United States.

AIM Photonics also serves as a “teaching factory” that provides a unique opportunity for the education and training of students and workers at all levels, while providing the shared assets to help companies – most importantly, small manufacturers – access the cutting-edge capabilities and equipment to design, test and pilot new products and manufacturing processes.

Private and public sector investment in optics and photonics does not end with the establishment of AIM Photonics. With current demand exceeding the supply of a trained workforce and the forecast calling for an increased demand for optics and photonics research, technologies and its commercial applications, the NPI identifies a need for, and an opportunity, to invigorate technical, hands-on learning in the United States.

Additionally, advanced optics and photonics research and technology underpin many large-scale technological challenges, such as mapping neurons in the brain, monitoring energy and the environment, and developing next-generation high-performance computing. The NPI encourages collaboration between government and the optics and photonics industries to identify and strive for joint goals that ensure development of critical technologies and lead to commercialization.

At the core of its advocacy efforts, the NPI is pursuing opportunities both in Congress and the administration to establish an education-to-workforce pipeline with increased industry internship opportunities for optics and photonics technicians in community colleges, and modernized educational laboratories for optics and photonics in four-year universities (**Figure 2**). The NPI is also working to collaborate

with government to develop photonics technology road maps to advance common interests and goals between public and private institutions.

The NPI has had particular success in helping to develop a roadmap in support of President Obama’s Brain Research through Advancing Innovative Neurotechnologies (BRAIN) Initiative. The BRAIN Initiative was established in April 2013 by the Obama administration as a bold new Grand Challenge to cultivate innovative technologies that can create a dynamic understanding of brain function and ultimately help researchers find new ways to treat, cure and even prevent brain disorders such as Alzheimer’s disease, epilepsy and traumatic brain injury. Towards this end, the NPI founded in 2014 an innovative multidisciplinary industry cohort, the Photonics Industry Neuroscience Group, to work collaboratively with the research community and federal government on next-generation imaging technologies in support of the BRAIN Initiative. Consisting of top US industry leaders in optics and photonics including Accumetra, LLC, Agilent, Applied Scientific Instrumentation, Coherent, Hamamatsu, Inscopix, Inc., Spectra-Physics and THORLABS, the group committed upwards of \$30 million in existing

and future R&D spending over the next three years to advance optics and photonics technology in support of the BRAIN Initiative. Further, the NPI Photonics Industry Neuroscience Group offered to the administration a roadmap for federal, private and joint funding opportunities in key optics and photonics areas where advances in technology and training would significantly accelerate progress toward achieving the BRAIN initiative goals of mapping neurons and circuits. Delivery of this road map to the White House Office of Science and Technology (OSTP) has established a strong dialogue between the administration and the NPI on opportunities to advance BRAIN Initiative goals through optics and photonics.

While the NPI is greatly encouraged by the level of collaboration between government and the optics and photonics industry that has been established since its inception, there is always more to be done. In the year ahead, the NPI will continue to identify and strive for joint technology goals that ensure development of critical technologies and lead to commercialization. For example, the NPI believes that there is a compelling need to accelerate US high-performance computing (HPC) R&D, which is essential to national security, defense



**Figure 2:** Constituents from Florida meet with Rep. John Mica (R-FL) in his Washington, DC office during the annual Congressional Visits Day organized by the National Photonics Initiative and member societies.

# Precision Dispensing Systems

and commercial applications.

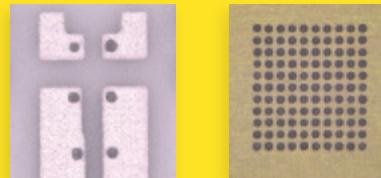
Congressionally, the NPI has been supportive of the reauthorization of the America Creating Opportunities to Meaningfully Promote Excellence in Technology, Education and Science Act, also known as America COMPETES. Reauthorization of the America COMPETES Act will help bolster US national competitiveness in science and technology in the years to come. Further, inclusion of authorization language that encourages partnership between the federal government, industry and academia will spearhead pivotal R&D investments in photonics, ensuring tomorrow's jobs and talent stay in the United States.

Now is the time for the United States to make photonics a national priority. On December 20, 2013, the United Nations General Assembly 68th Session proclaimed 2015 as the International Year of Light and Light-based Technologies (IYL 2015). Much of the world has long recognized the promise of light and many countries have significantly increased their national commitments to the optics and photonics industries. By uniting the public and private sectors to develop critical technology roadmaps, and by creating educational opportunities that will inspire a more skilled workforce, our nation can strengthen its leadership position in this critical, enabling technology and help grow international economies.

## Biography

Alan E. Willner received his PhD in Electrical Engineering from Columbia U., was co-chair of the US National Academies' study, "Optics and Photonics: Essential Technologies for our Nation," is a fellow of OSA and SPIE, is a member of the U.S. National Academy of Engineering and is chair of the National Photonics Initiative ([www.lightourfuture.org](http://www.lightourfuture.org)). He is the Steven and Kathryn Sample Chair in Engineering at the U. of Southern California; [willner@usc.edu](mailto:willner@usc.edu).

## 01005 Dispensing



- NEW Precision Auger Pump developments for repeatable 01005 Dispensing
- Dispense solder paste at 150 µm diameter
- Coupled with Real Time Process Control (FPC) to ensure a perfect process

## Real Time Process Control



### Fluid Pressure Control (FPC) is Real Time Process Control

- Automated adjustments in Real Time
- Delivers a constant supply of fluid to pump regardless of fluid level
- Maximizes pump dispense capabilities
- Enhances Repeatability



A wide range of dispense pumps is also available.

Supplying a full range of  
precision dispense products.

**GPD Global**  
Precision Dispensing Systems

+1.970.245.0408 • [request@gpd-global.com](mailto:request@gpd-global.com) • [www.gpd-global.com](http://www.gpd-global.com)



## Your Standard in Precision Automation™

Die Bond and Dispense Solutions



### Typical Applications

#### Semiconductor Packaging

- Medical Imaging
- Multichip Modules
- 3D / 2.5D Packaging
- Wafer Scale Packaging
- RF / Microwave Modules

#### Photonic Packaging

- Optical Engines
- LED Assemblies
- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

#### MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

# Thin chip foil packaging: An enabling technology for ultra-thin packages

By Christof Landesberger, Nagarajan Palavesam, Andreas Drost, Waltraud Hell, Robert Faul, Christoph Kutter *[Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT]*

**R**educed height for chip packages is a dominant requirement for electronic components for mobile and wearable applications. Furthermore, the capability to bend and mount chip packages onto curved surfaces or into application-specific formed housings would allow the distribution of electronic and sensing systems in industrial production environments as well as in potentially any object of our daily life (e.g., Internet of Things [IoT]). These applications will require a technology platform for the interconnection and packaging of several IC components such as, a sensor element, a microcontroller IC for data acquisition and transceiver functionality, and some kind of micro-energy supply. Low-cost manufacture of such internet-compatible sensor nodes will be the key for bringing such products to high-volume applications. Foil-based systems are among the most highly rated candidates to achieve these requirements for the following reasons: 1) Electrical wiring layers on film substrates can be prepared at very high resolution, which allows for direct electrical interconnection of IC devices; and 2) By using web substrates, the whole process chain for device assembly, packaging and testing can be realized by continuous roll-to-roll manufacture.

## Mechanical robustness of ultra-thin silicon

The mechanical flexibility of ultra-thin silicon devices thinner than 30 $\mu\text{m}$  is well known. Optimum mechanical stability can be achieved by advanced grinding and subsequent stress-relief processes such as chemical mechanical polishing (CMP), or wet or dry chemical etching. Besides the backside thinning techniques, the die separation technique has a major influence on the mechanical strength of the ultra-thin silicon devices [1]. Among the various existing dicing techniques, plasma dicing shows the best results in terms of

robustness, and in the case of ultra-thin devices, it also is best in terms of cost. Advanced thinning and dicing techniques result in nearly damage-free chip rear side and side walls. Nevertheless, the ultra-thin single crystal silicon chip is very fragile in terms of mechanical handling forces and can be broken during assembly. Therefore, any packaging technology for ultra-thin dies must ensure mechanical robustness.

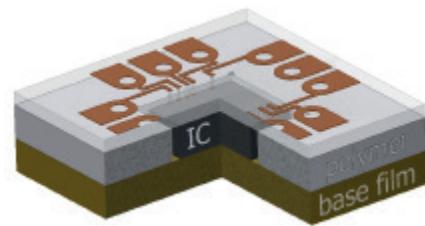
In order to verify the influence of a film package on the fracture behavior of thin silicon samples, we ran a series of experiments using three-point bending tests. The thickness of silicon samples was varied in three steps: 130 $\mu\text{m}$ , 65 $\mu\text{m}$  and 30 $\mu\text{m}$ . We compared the breaking tests for bare silicon and silicon embedded between two polyimide film layers. In the case of 130 $\mu\text{m}$  thick samples, embedding did not influence the breaking test results. However, in the case of ultra-thin samples (30 $\mu\text{m}$ ) the fracture force was increased by a factor of nearly three when chips were laminated between two film layers [2]. It was also found that the mean displacement at the instance of breaking of the silicon samples was increased by a factor of two. These results clearly confirm the improvement of mechanical robustness of thin silicon due to embedding in film laminates. The expected benefits of thin chip foil packages are the availability of extremely thin and mechanically bendable IC packages that are sufficiently robust to withstand further fast running assembly steps, and that also enable new applications for sensors and electronics on curved surfaces.

## Technological concept for flexible chip foil packages

Fraunhofer EMFT has set up a technological concept that is based on a three-layer embedding technology by which the fragile IC is located in the center of the laminate structure. **Figure 1** illustrates this set-up. By a first processing

step, thin or ultra-thin microelectronic devices are bonded onto a film substrate in a face-up orientation. Then, devices are embedded in a planar polymer layer that can be structured by a photolithographic process. After opening of vias above the IC contact pads, a thin-film metal deposition and patterning process is carried out that results in a fan-out routing for the I/O contact pads. Finally, the top wiring layer can be covered by a polymer film layer. The concept results in a chip foil package whereby fragile ICs are embedded in a plane-parallel polymer laminate of an overall thickness between 80 $\mu\text{m}$  and 150 $\mu\text{m}$ . This new package is five to ten times thinner than state-of-the-art chip packages.

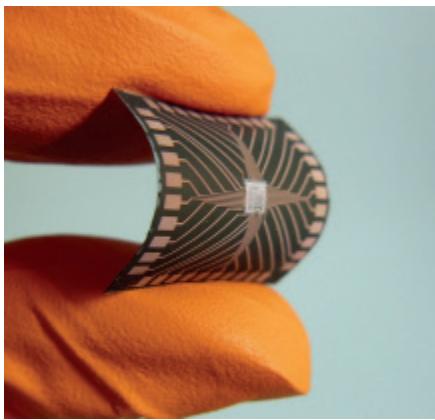
Electrical interconnects are processed by sputtering of metal directly onto the aluminum contact pads of IC devices. Metal deposition at the sidewall of a contact via and top metal layer are done in one step ("one step interconnect"). Such an approach is highly beneficial when two or even more ICs and subsequent components have to be electrically interconnected in one film chip module. It also renders additional bumping processes unnecessary. In some applications, the low thickness of only sputtered metal films is not sufficient for low-resistance interconnects. In such cases, electroplating of copper wiring layer can be easily introduced to the process flow.



**Figure 1:** Technical concept for face-up chip embedding in film substrates with electrical interconnection and fan-out wiring scheme.

## Technological results

We prepared several 25 $\mu\text{m}$  thin microcontroller ICs (Microchip PIC, 16 bit, 40 I/O contacts) according to the well-known dicing-by-thinning concept. We used a wafer saw for preparation of front side grooves on the controller IC wafer. For the first technological demonstration, we used polyimide film substrates that had a thickness of 50 $\mu\text{m}$ . We cut a round area 150mm in diameter and bonded it temporarily onto a standard silicon carrier wafer (150mm diameter). Because of this “film-on-carrier” configuration, it was possible to apply standard photomask lithography for patterning of via and metal interconnects. Lastly, the polyimide film stack with embedded chip components was removed from the carrier and cut into individual chip foil packages. **Figure 2** shows the flexibility of the fan-out film package of the embedded ultra-thin microcontroller. Electrical testing showed high yield for electrical interconnects.



**Figure 2:** Functional technology demonstrator of flexible thin chip foil packages prepared at Fraunhofer EMFT.

Indeed, it would be desirable to replace mechanical sawing by plasma trench etching for the die separation process. However, this generally requires slight changes in the design of dicing streets before wafer manufacture. This topic will require further discussions with IC design and manufacture companies. Nonetheless, the ultra-thin dies in their final film packages did not show any cracks or damages. This confirms the increased robustness on account of the embedding process.

## Outlook: Roll-to-roll chip embedding

The technological concept of this thin chip foil package offers the chance to develop a continuous roll-to-roll process for chip embedding in film substrates. Such a process would enable extremely thin and flexible packages for any type of functional IC devices in high volume and at low cost. To achieve this, two process steps need to be considered: highly accurate die bonding, and lithographic patterning. Both are available today for roll-to-roll (“R2R”) manufacture.

From an economic perspective, lithographic patterning represents a rather costly process. However, these costs are minimized when many chip interconnect patterns can be processed in parallel. In order to realize massively parallel roll-to-roll (R2R) lithography on polymeric substrates, patterns for 1) via formation and 2) fan-out wiring need to be aligned with respect to I/O contact pads of embedded dies. Preferred processing techniques are: 1) laser direct imaging and 2) R2R stepper lithography. Pattern alignment and the UV exposure step are expected to be carried out for a large set of dies in one step. The following example shows the potential benefit of parallel processing: In the case of a 2.4mm by 2.4mm large IC with 40 I/O contact pads, the single chip foil package might show a size of 3.5 x 3.5mm<sup>2</sup>. A lithographic exposure field of 5cm x 5cm will then cover some 170 chip packages. It should be mentioned that the time required to analyze the true chip positions, which has to be done before UV exposure, does not increase the overall processing time because it can be done simultaneously at successive processing steps. Altogether, this may lead to a highly accurate, adaptive and continuous lithography process at very high throughput.

Our next target is to realize an industrial oriented application of thin chip foil packages. We are looking for a partner consortium that will include an IC manufacturer, equipment suppliers (e. g., for roll-to-roll lithography), and companies who need thin or flexible chip packages for their specific future products. A second focus of development work will be targeted towards the investigation of all relevant reliability aspects of chip foil packages under mechanical bending and different climate conditions.

## Acknowledgements

This work was funded by the Bavarian Government under contract no. VI/3-3622/452/3, and the European Commission under the grant agreement PITN-GA-2012-317488-CONTEST.

## References

1. C. Landesberger, et al., “Backside Thinning and Stress-Relief Techniques for Thin Silicon Wafers,” Handbook of 3D Integration, Vol. 3, Wiley-VCH, 2014, (ISBN 978-3-527-33466-7).
2. N. Palavesam, et al., “Investigations of the fracture strength of thin silicon dies embedded in flexible foil substrates,” SIITME 2014, Bucharest, Romania.

## Biographies

Christof Landesberger received his diploma degree in Physics from Ludwig-Maximilians U. München. He is currently a group manager at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT; email Christof.landesberger@emft.fraunhofer.de

Nagarajan Palavesam received his Joint Master degree in Micro and Nanotechnologies for Integrated Systems from Polytechnic U. of Turin, INP Grenoble and EPFL. He is a doctoral candidate at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT.

Andreas Drost received his diploma degree in Physics from Technische U. München. He is a Research Scientist at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT.

Waltraud Hell received her diploma degree in Chemistry from Technische U. Hannover. She is a Research Scientist at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT.

Robert Faul received his diploma degree in Electrical Engineering from Technische U. München. He is a Design Engineer at Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT.

Christoph Kutter received his PhD in Physics from U. of Constance, Germany. He is a Professor at the Faculty of Electrical Engineering and Informatics at U. der Bundeswehr München and he is the Director of Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT.

# MultiPlate

An innovative plating system for next generation packaging technologies



Through hole  
filling



Single and double  
side plating



High speed  
pillar plating



Redistribution  
layer plating

## Compatible with:

- 150, 200, 300 mm wafers and panel
- Thin Taiko wafers

## Learn more:



# Through-silicon via-last lithography for 3D packaging

By Warren Flack, Rezwan Lateef [Ultratech, Inc.]

**S**caling the diameter of the through-silicon via (TSV) is a major driver for improving system performance and cost. In addition, reducing the size of via landing pads provides significant advantages for device design and final chip size. Current via-last diameters are approximately 30 $\mu\text{m}$  and are being scaled to 5 $\mu\text{m}$  and beyond.

With smaller TSV diameters, back-to-front overlay becomes a critical parameter because via landing pads on the first metal level must be large enough to include both the TSV critical dimension (CD) and overlay variations. This article discusses back-to-front side wafer lithography characterization and optimization for next-generation TSV scaling.

## Lithography as a critical factor

Foundry customers and makers of leading-edge devices are evaluating TSVs for next-generation three-dimensional (3D) packaging. Common TSV methods include via-first, via-middle and via-last process flows. Via-last is a wafer backside approach that provides extensive flexibility because the process can be implemented at either the foundry or an outsourced semiconductor assembly and test (OSAT) site. TSV-last processing is similar to TSV-middle in that a larger via is formed that requires the deposition of a liner and barrier followed by complete filling and planarization. However, TSV-last processing removes potential interference of large TSVs with back-end-of-line (BEOL) processing. Additionally, the TSV-last approach complements ongoing scaling for non-TSV process flow elements, such as wafer-to-wafer bonding accuracy.

Lithography is one of the critical factors affecting overall device performance and yield for via-last TSV fabrication. Scaling the TSV diameter is a major driver for enabling system performance and cost improvements. Current via-last diameters – approximately 30 $\mu\text{m}$  – are being scaled to 5 $\mu\text{m}$  and may further decrease to less than 2 $\mu\text{m}$ . A unique lithography requirement for via-last patterning is back-to-front-side wafer alignment. With smaller TSV diameters, the back-to-front overlay becomes

a critical parameter because via landing pads on the first metal level must be large enough to include both TSV critical dimension (CD) and overlay variations. Reducing via landing pad size provides significant advantages for both device design and final chip size.

The manufacturing approach utilizing 3D TSV technology alleviates interconnect delay considerations by reducing global interconnect wiring lengths. In addition, TSV technology enables superior bandwidth performance, improves power management and addresses device latency issues. Many companies have research activities in 3D TSV technology, and numerous demonstration vehicles have been developed [1]. Some of these TSV process sequences require the need for back-to-front alignment solutions during the lithography process step.

Interposers for packaging also require TSV technology. Devices under consideration for use with interposers include graphics processors, high-end application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs). The drivers are mainly partitioning large die, integrating single chips into a module, reducing die size where substrate density is the constraint, and using the interposer to minimize the stress on large die fabricated with extra-low-k dielectrics (ELKs).

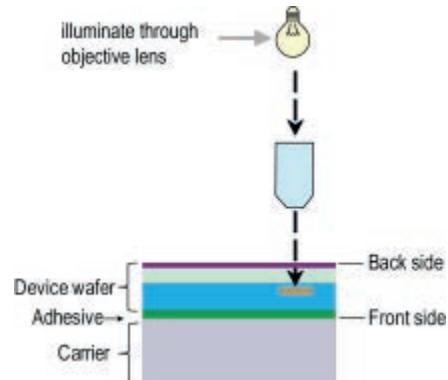
Image sensors have utilized TSV technology in mass production over the last few years, and DRAM manufacturers are expected to begin utilizing TSV packaging technology as well. Adoption of this technology by memory companies can play a significant role in driving the technology forward. However, the requirements for memory manufacturers are much more stringent and require developing improved back-to-front alignment capability.

## Alignment system

The naming convention adopted here is the wafer device side is the front side and the silicon side is the back side. The side facing up on the lithography tool is the back side of the TSV wafer (see **Figure 1**). The method of top

infrared (IR) illumination provides practical advantages for integration with stepper lithography. Because the illumination and imaging are directed from the top, this method does not interfere with the design of the wafer chuck, and does not constrain alignment target positioning on the wafer [2].

The top IR alignment method illuminates the alignment target from the back side using an IR wavelength that can transmit through silicon (light green in **Figure 1**) and the process films (blue). For this configuration, the embedded target (orange) needs to be made from an IR-reflective material, such as metal, in order to achieve the best contrast. The alignment



**Figure 1:** Off-axis alignment configuration with infrared illumination and imaging from above the wafer. This configuration is extremely flexible, providing access to the entire wafer for target alignment.

sequence requires that the wafer move in the Z direction to shift the alignment focus from the wafer surface to the embedded target.

The lithography system used has a top IR alignment system that supports back-to-front side alignment applications. The TSV-last application requires alignment to embedded metal targets below silicon, and the off-axis IR alignment system was designed to achieve back-to-front-side overlay of less than 1 $\mu\text{m}$  ( $\text{mean} + 3\sigma$ ) over a full 300mm wafer. However, a large portion of this budget is consumed by the error uncertainty of the back-to-front overlay metrology.

# Advanced Automated Bondtesting

## The Nordson DAGE 4800 bondtester with camera assist automation

The Nordson DAGE 4800 brings the latest developments in automated wafer testing technology to users testing wafers from 200mm to 450mm in diameter

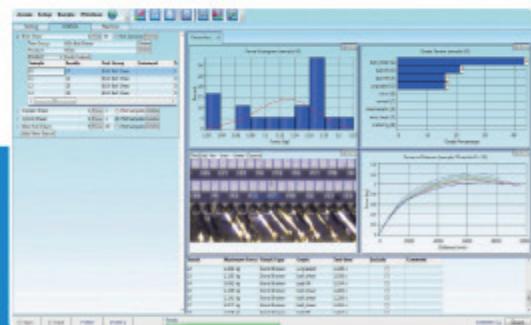
### Key Features:

- Flexible wafer map creation tool enables quick and precise test set-up
- KLARF data import to identify defective bonds
- Automatic smart chuck with unique edge lift system
- Multiple camera options for image and video collection
- Multi-function cartridge (MFC) allows automated application changing



Intelligent Software - Paragon™ is the latest generation software and is at the heart of the 4000Plus, Optima and 4800 series bondtesters. In addition to the intuitive manual testing options, camera assist automation allows for fully automatic test options:

- Multiple camera options aid set-up and allow the use of automation patterns and routines
- Fiducial recognition aligns samples and allows for both linear and angular correction
- Automated testing adds repeatability and reproducibility to your results by removing operator input
- When combined with an integrated wafer handling device the system can test multiple wafers consecutively



**Paragon™ - Automated Bondtesting Software**



## Metrology

To eliminate the inherent restrictions in topside planar metrology, a direct, back-to-front-side registration metrology package was developed to run on the lithography system, utilizing the off-axis IR alignment system. A dedicated software option was developed to capture both reference patterns and TSV patterns at pre-programmed locations inside the die, and on all dies of the wafer. The metrology package is called dual side alignment stepper self metrology (DSA-SSM).

As shown in **Figure 2**, the reference Metal 1 feature (outlined by the blue ring) and the resist target feature (outlined by the red ring) are not in the same focal plane. For a silicon thickness of 50 $\mu\text{m}$ , focusing on one feature will render the other feature out of focus. Therefore, each feature must have its own focus offset to be programmed in the metrology measurement recipe. The image capture system then identifies the relative location of both features to determine possible offsets. When the wafer lot is completely measured, the metrology

software will analyze the offsets and use an industry standard stepper overlay model to determine stepper correctable offsets.

The concept of tool-induced shift (TIS) provides a method to compensate for systematic measurement errors. The basic concept is that two measurements taken at 0 and 180 degree wafer orientations can be represented as two components of error: a TIS error component that is independent of orientation, and a characteristic or “actual” measurement that rotates with the wafer [3]. Because tilt between the wafer and metrology tool is a source of TIS, the extent and composition of films in the optical path can modulate TIS, and in practice, the measured TIS error may have a process dependency. However, for well-controlled processes with consistent TIS measurements, the TIS concept provides an effective method for data correction.

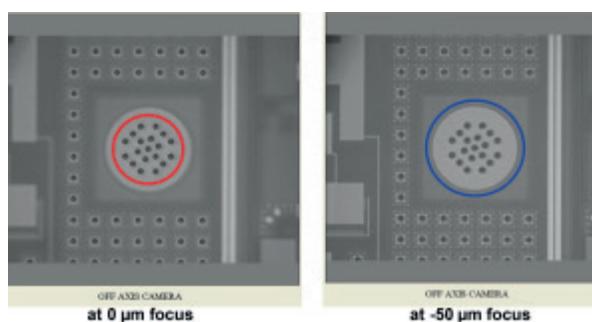
To test the DSA-SSM, a TSV-last test vehicle was created with a damascene Metal 1 process, temporary bonding to a carrier, back grinding, and a final surface finish by CMP [4]. The TSV diameter is 5 $\mu\text{m}$  and the silicon thickness is 50 $\mu\text{m}$ . The alignment requirement is that the TSV etching will land completely on Metal 1 pads. The test lot consists of ten 300mm wafers.

## Metrology repeatability

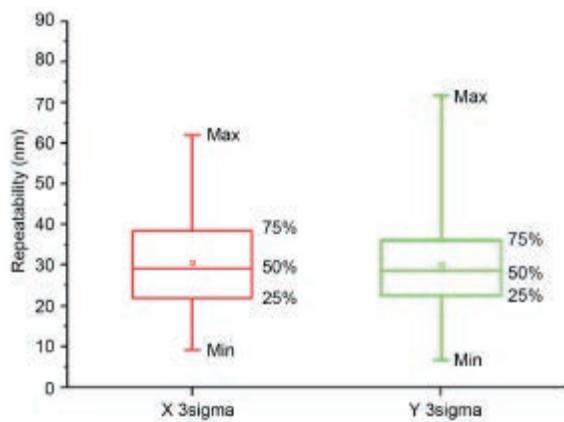
A 300mm wafer from the TSV-last test vehicle lot was used to characterize the repeatability of the DSA-SSM. Each of the 115 die on the wafer was measured five separate times. The repeatability is shown in **Figure 3**. The average 3 $\sigma$  is 30nm in X and Y. This is within the requirements for 750nm overlay performance of this 5 $\mu\text{m}$  TSV last process.

## Calculation of TIS

TIS was characterized by using the DSA-SSM to measure overlay on the TSV last test vehicle lot at 0 and 180 degree orientations and then analyzing the data. The sum of offsets for the two orientations divided by 2 gives the TIS estimate. **Figure 4** shows a vector plot

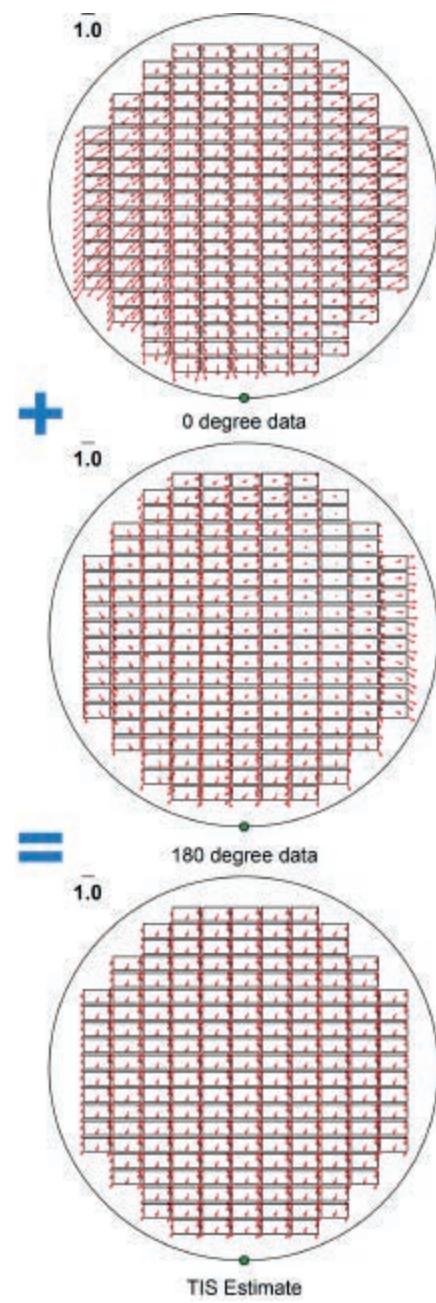


**Figure 2:** The left-hand image shows the resist target in focus (the ring outlined in red). These are on the top surface (focus at 0 $\mu\text{m}$ ). The right-hand image shows the circle of METAL1 in focus at -50 $\mu\text{m}$  (the ring outlined by the blue). The height difference between the two features is larger than the focal depth of the alignment camera so always one of the two is out of focus.



**Figure 3:** Repeatability of DSA-SSM measurement for a single wafer measured multiple times at 115 points. Each point on the wafer is measured 5 times to calculate 3 $\sigma$  for each point. Average 3 $\sigma$  is 30nm in X and Y.

example of 0 and 180 degree measurements of the same wafer. The average TIS offset is -155nm for X and -453nm for Y. For ease of visual comparison, both sets of measurements are plotted on the original 0 degree orientation. The TIS vector plot is shown at the bottom of **Figure 4**. It is apparent that the TIS estimate is uniform across the wafer, and the corrected data has



**Figure 4:** Calculation of the TIS estimate from 0 degree and 180 degree measurements of the same wafer. For ease of visual comparison, both sets of measurements are plotted on the original 0 degree layout map. The TIS is the sum of the offsets from both orientations divided by 2.

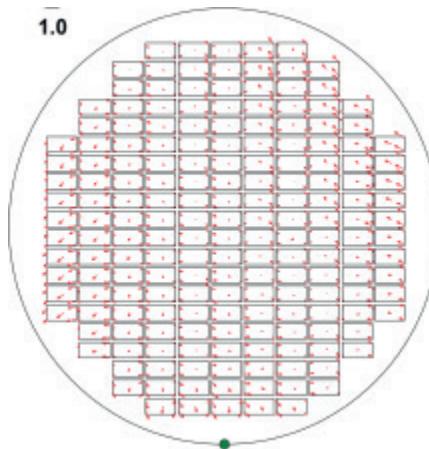
a smooth variation consistent with physical error sources. Because the TIS values are consistent, a single TIS mean correction can be used to correct the means for the 0 degree overlay measurements.

## Lot overlay measurement

A dense 920-point sampling plan that measures 184 steps per wafer was used for lot characterization. This sampling plan provides detailed information that can be used to characterize interfield linear and higher-order terms. A total of five sites per field were measured to characterize intrafield modeling terms. Individual recipes with specific metrology structures, product layouts, and sampling plans can be saved on the lithography stepper.

## Overlay optimization

The DSA-SSM measurements were used to optimize the TSV overlay for the TSV test vehicle lot. Direct referencing of the TSV image to the embedded metal pattern allowed for identification of critical interfield and intrafield parameters. For specific process optimization, linear corrections are available at the job level. Optimization for these parameters is common for frontside overlay, and as DSA overlay approaches similar performance, it is not surprising that detailed optimization is required for DSA alignment as well. For each of these activities, DSA-SSM provides feedback to identify error components and estimate offsets to minimize their effects. To simulate production operation, the ten wafer DSA test vehicle lot was run on the stepper, and then analyzed using DSA-SSM. The overlay results for a sample

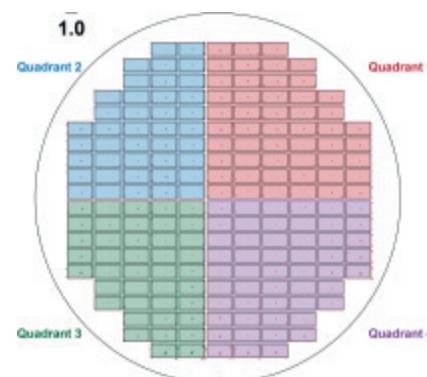


**Figure 5:** The overlay results after TIS correction for a wafer from the TSV test vehicle lot. For this wafer, the  $3\sigma$  is 658nm in X, and 515nm in Y.

wafer after TIS correction is shown in **Figure 5**. For this wafer the  $3\sigma$  is 658nm in X and 515nm in Y.

An analysis of the larger  $3\sigma$  in X revealed a nonlinear error source that originated from a process step outside of the lithography module. Nonlinear effects can be approached in various ways depending on the stability of the signature. For thinned substrates, significant distortions may come from processing steps other than lithography. Therefore, the initial lithography matching may need to be supplemented with methods to address process specific higher-order errors. Subdividing the wafer map into multiple alignment zones provides a flexible method to account for nonlinear effects because it allows for independent mapping and optimization of each zone [5]. The multi-zone approach can track errors that are not repeatable over time. The repeatable component of error can be addressed using nonlinear offsets.

To investigate the effectiveness of multiple alignment zones, the same ten-wafer TSV test vehicle lot was processed through lithography again using a four-quadrant mapping for each wafer as shown in **Figure 6**. Each of the four quadrants can be independently mapped and optimized with linear stepper offsets.



**Figure 6:** A per-quadrant residuals plot of one TSV test vehicle wafer processed on the stepper with four-quadrant mapping.

The mapping method gave significant overlay gains by optimizing the per-wafer or per-quadrant offsets, and the use of per-quadrant offsets provides a better fit to the nonlinear errors [4].

## Summary

Scaling of TSVs in the TSV-last process requires tighter overlay specifications. This

means that overlay correction methods commonly used for front-side stepper lithography will become increasingly important for TSV lithography. Direct verification of TSV lithography to the embedded reference layer is enabled by using the DSA-SSM. For this study, the DSA overlay performance is better than 750nm and exceeds the requirements for 5 $\mu$ m diameter TSVs.

## Acknowledgment

Elements of this article appeared in the paper “Optimization of through-Si via-last lithography for 3D packaging,” originally distributed at the International Wafer-Level Packaging Conference at San Jose, California, October 13-15, 2015.

## References

1. J. Vardaman, et al., “TechSearch International: 3D TSV Markets: Applications, Issues and Alternatives,” Aug. 2012.
2. W. Flack, et al., “Verification of back-to-front side alignment for advanced packaging,” International Wafer-Level Packaging Conf., Santa Clara, CA, Nov. 2012.
3. D. Coleman, et al., “On the accuracy of overlay measurements: Tools and mark asymmetry effects,” Integrated Circuit Metrology, Inspection, and Process Control IV Proc., SPIE 1261 (1990).
4. W. Flack et al., “Optimization of through-Si via-last lithography for 3D packaging,” Inter. Wafer-Level Packaging Conf., San Jose, CA, Oct. 2015.
5. W. Flack, et al., “Lithography technique to reduce the alignment errors from die placement in fan-out wafer-level packaging applications,” The 61st Elect. Comp. and Tech. Conf. Proc., Lake Buena Vista, FL, June 2011.

## Biographies

Warren Flack received his BS and MS degrees in Chemical Engineering from the Georgia Institute of Technology and his PhD in Chemical Engineering from the U. of California at Berkeley; he is the Senior Director of Global Applications at Ultratech, Inc.; email wflack@ultratech.com

Rezwan Lateef received his BS and MS degrees in Electrical Engineering from the U. of Illinois at Urbana-Champaign and is the GM and VP of Litho Products at Ultratech, Inc.

# Next-generation copper pillar plating technologies

By Cassandra Melvin, Bernd Roelfs [Atotech Deutschland GmbH]

**A**s the industry moves towards smaller, faster devices, there is mounting pressure on all members of the supply chain to enable higher performance at lower cost. The limitations of Moore's Law are becoming more evident as advanced technology nodes are no longer providing a significant cost benefit. R&D investments in next-generation sub-10nm node lithography tools are becoming increasingly expensive and perhaps are no longer the viable solution for improving cost effectiveness. As a result, the industry has shifted its focus to advanced packaging as a means for providing better performance and lowering costs, following the so-called "More than Moore" approach. There are three primary drivers for this shift: improved performance, more functionality, and cost reduction. This article will discuss how these three drivers have led to the emergence of flip-chip packaging using pillars and the current and future challenges for Cu pillar technology.

Various packaging technologies have been tested for their ability to provide substantial technical advantages while reducing the overall production flow and minimizing manufacturing costs. Currently, the preferred packaging technology for sub-45nm node technologies is flip-chip because of its ability to offer a significantly improved I/O density and minimized footprint compared to standard wire bonding, as well as better thermal and electrical performance. Flip-chip technology is relatively inexpensive compared to other emerging packaging technologies and currently accounts for approximately 16% of the 200mm packaging market, according to industry reports. Many of the key players in the packaging industry already utilize flip-chip in high-volume manufacturing and the five-year forecast is promising, showing steady growth

for flip-chip across all market segments with the most substantial growth in the consumer electronics sector.

During the flip-chip process, the die is flipped over and connected to the substrate prior to being packaged. Connection is possible by various applications but the primary two are soldering or using pillars. Flip-chip ball grid array (BGA), which used SnAg solder balls to connect the chip to the substrate, has been the preferred method in the past but is slowly being surpassed by Cu pillar. The two methods of soldering, paste printing and micro ball placement, have their own set of limitations, namely the resolution of the printing equipment and the slow and costly micro ball placement process. For the most advanced technology nodes, Cu pillar is the preferred application for the first layer interconnect process and will account for the majority of future growth in the flip-chip market segment.

## Copper pillar plating process and requirements

During the plating process, the die is connected to the IC package by two layers of Cu pillars – the first layer interconnect on the die side and the second layer interconnect on the substrate side. To further increase the I/O count, an optional redistribution layer (RDL) may be plated on the die side. The Cu pillar is electrolytically plated according to the application requirements for height and diameter, usually followed by a thin Ni diffusion barrier (up to 3µm), and finally a Sn or SnAg cap.

The critical requirements for pillar plating – high throughput, exceptional reliability performance, and high yield – can be optimized using a high-speed plating process that can achieve superior uniformity and voiding performance.

Throughput is directly correlated to the deposition speed (as well as

the design of the plating tool) and therefore, applying higher current densities will, in most cases, result in an increased throughput. High-speed pillar plating, however, generally has a negative impact on the voiding performance and uniformity. Excess voiding is a common problem when plating at higher current densities and especially in the absence of a Ni diffusion barrier on top of the Cu. Furthermore, using standard Cu plating chemistries and while plating at current densities of 10+ ampere per square decimeter (ASD) it is difficult to satisfy the industry's requirements of <5% for nonuniformity. Both voiding and nonuniformity impact the electrical performance, which is a measure of reliability, as well as the yield.

Furthermore, the purity of the bath – and specifically the level of additive incorporation – has a direct impact on the voiding performance, as a less pure or "dirty" plating bath with significant additive incorporation results in more voids. This problem can be overcome by optimizing the additive suite utilized during the plating process. Typically, three additive suites are used in Cu plating, including accelerators, which selectively speed up the deposition, suppressors that selectively slow the deposition, and levelers that support a uniform thickness distribution.

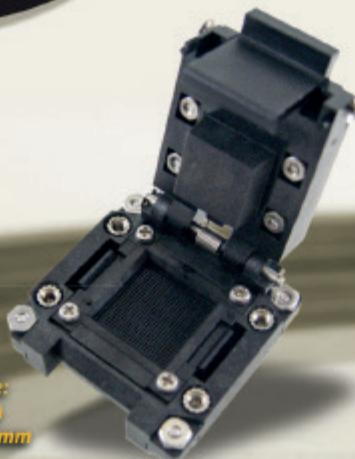
The plating mechanism at work is determined by the additive suite and contributes to the voiding performance and uniformity of the deposited Cu. The plating chemistries, therefore, are what determine how the plating process will perform and impact throughput, reliability, and yield, as well as the quality of the deposited Cu. Therefore throughput, reliability and yield can be optimized by improving the existing plating chemistries so that uniformity and voiding performance

# Socket to me, Baby!

## M SERIES H-PIN SOCKET

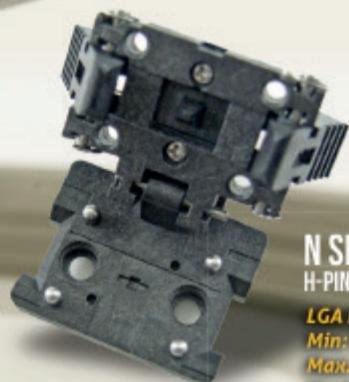
BGA Package size:  
Min: 2mm x 2mm  
Max: 12mm x 12mm

Pin Count:  
576 max



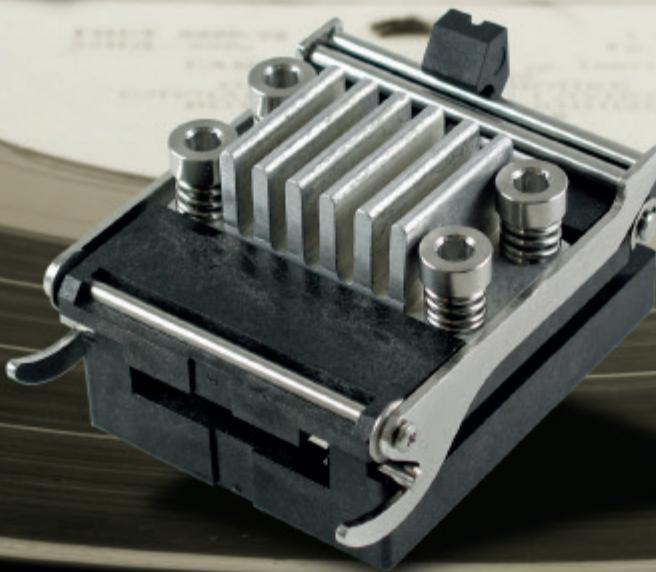
## N SERIES H-PIN SOCKET

LGA Package size:  
Min: 0.50mm x 0.50mm  
Max: 4.0mm x 4.0mm  
Pin Count:  
64 max



## Q SERIES H-PIN SOCKET

BGA Package size:  
Min: 20.0mm x 20.0mm  
Max: 32.0mm x 32.0mm  
Pin Count:  
1521 max - 0.80mm  
961 max - 1.00mm



## CHART-TOPPING PERFORMANCE, NOW FROM THREE NEW SOCKET DESIGNS.

Check out these brand-new additions to the Plastronics' line of high performance burn-in sockets. They feature SNAP-FIT designs and H-PIN contact technology to give you high performance at burn-in costs. Plastronics has the widest offering of burn-in socket platforms to fit your product specifications, no matter how large or small. Package sizes range from 0.50mm x 0.50mm to 60mm x 60mm and pitch sizes as small as 0.30mm. For everything else, we offer fast customization and delivery. Take our sockets for a spin – we know you'll become a big fan.

are not compromised with higher current density plating.

For future requirements of even higher throughput – and therefore significantly faster deposition rates along with further improved yield – completely new technologies are needed. Standard electrochemical deposition (ECD) tools and chemistries will reach their technical limitations, so new solutions with vastly different technologies must be developed to enable high-speed pillar plating with the best reliability performance.

To address the current and future process requirements for pillar plating, we have expanded our semiconductor product portfolio with the next-generation of Spherolyte Cu pillar plating chemistries, as well as an electrochemical deposition tool designed for high-speed pillar plating. The next sections will highlight the performance of these new technologies compared to their previous, industry accepted pillar plating process.

## Spherolyte RDL/pillar UF2 and UF3 processes

As throughput is directly correlated to deposition speed, the development of new electrolytes with faster deposition rates is paramount to satisfying the industry requirements for high throughput. The improvement of the Cu deposition rate beyond the industry standard of 1-2 $\mu\text{m}/\text{min}$  is critical for next-generation packaging technologies; however, uniformity must not be compromised as a consequence. Uniformity of Cu pillars is a prerequisite for a regular soldering process without any opens between the pillar on the die and its counterpart on the IC substrate. Usually, uniformities, or to be precise, nonuniformities are calculated and expressed as shown in **Figure 1**. Most pillar plating applications require a nonuniformity rate of 5% for within-wafer (WIW) and within-die (WID), with a profile (WIP) variation of less than 2 $\mu\text{m}$ .

Key to the development of a new additive suite is the leveler. This is a specific N-containing additive molecule that interacts with the other additives, namely the accelerators, usually SPS, Bis-(sodium sulfopropyl)-disulfide containing. The combination of accelerator and SPS controls the property of the Cu deposit, including: 1) Physical properties like hardness, resistivity, etc.; 2) Grain size;

3) Roughness; and 4) Uniformity and profile.

Profile and uniformity are linked to each other. Profile requirements may vary according to the specific application requirements for shape and form. Standard pillars are rectangular in shape, however oval and rounded pillars are not uncommon, and some pillars are placed on top of a recess structure known as pillar on pad. Therefore, different electrolyte systems are needed to comply with the varying requirements.

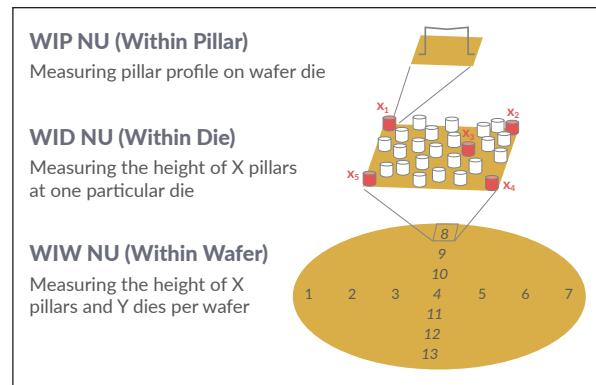
## High-speed systems for conformal plating

The first electrolytic system to be discussed is the second-generation of electrolytes for Cu pillar plating. It is a purely conformal plating process, meaning that the Cu deposition exactly follows the given underlying shape, i.e., a flat surface will result in a flat Cu surface and a waved surface will result in a waved Cu surface. The benefit of such an electrolyte system is that Cu deposits are usually perfectly flat and smooth as long as the underlying pad structure is as well. In this case, the pillar shapes are flat without any doming or dishing (see **Figure 2a**).

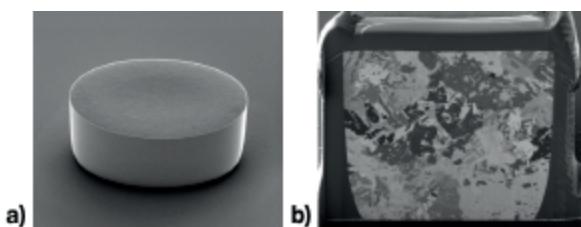
This example has been plated with Spherolyte RDL/pillar UF2 at 3.8 $\mu\text{m}/\text{min}$ . These electrolytes can be used for much higher deposition speeds, up to 4.4 $\mu\text{m}/\text{min}$ , as shown in **Table 1**. It should be noted that the uniformity is also a function of the layout. Generally, standard layouts can be plated with higher current densities.

## Limitations of conformal plating

While the ability to create a perfectly flat (uniform) pillar shape is



**Figure 1:** Nonuniformity calculations for Cu pillar plating. The example shown is for WIW with 13 dies.

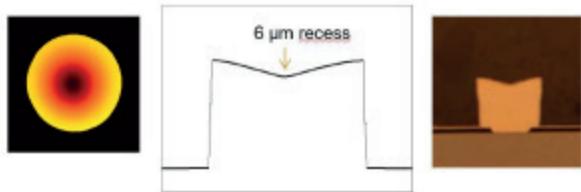


**Figure 2:** a) (left) Example of a 20 $\mu\text{m}$  oval Cu pillar plated with a conformally deposited electrolyte at 3.8 $\mu\text{m}/\text{min}$ . b) (right) An FIB cut through the Cu pillar.

Speed	3.3 $\mu\text{m}/\text{min}$	3.9 $\mu\text{m}/\text{min}$	4.4 $\mu\text{m}/\text{min}$
Non uniformity	15 ASD	17.5 ASD	20 ASD
WIW	2.5 %	3.0 %	4.6 %
WID	2.2 %	2.4 %	4.5 %
Profile	1.5 %	1.7 %	2.3 %

$\text{Non-uniformity \%} = \frac{100}{2} \frac{(Z_{\max} - Z_{\min})}{Z_{\text{ave}}}$

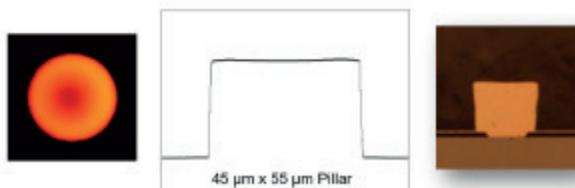
**Table 1:** Example of nonuniform plated Cu pillars at different deposition speeds using the Spherolyte RDL/pillar UF2 process. Numbers given are for test wafers plated in a fountain type plater. The pillar height is 27 $\mu\text{m}$  in a 42 $\mu\text{m}$  thick resist.



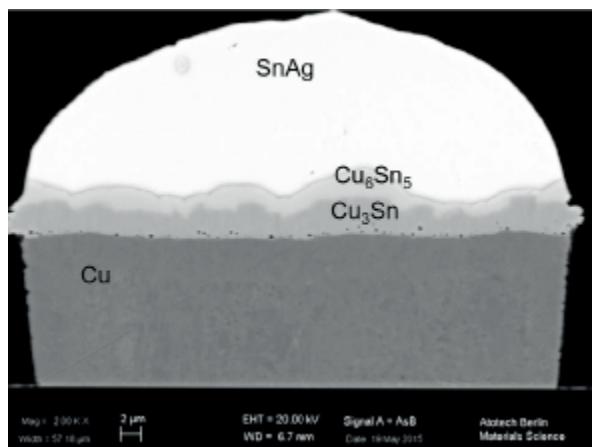
**Figure 3:** A Cu pillar plated on top of a  $\mu$ -via with a conformally plated electrolyte (Spherolyte RDL/pillar UF2) with a pillar height of 45 $\mu\text{m}$  and a pillar diameter of 55 $\mu\text{m}$ .

advantageous, it also has limited use for pillar in pad applications, wherein the Cu pillars are built on top of a  $\mu$ -via as shown in **Figure 3b**.

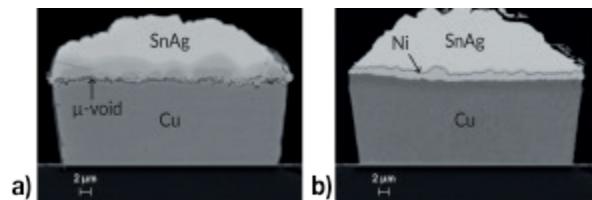
The remaining recess after plating



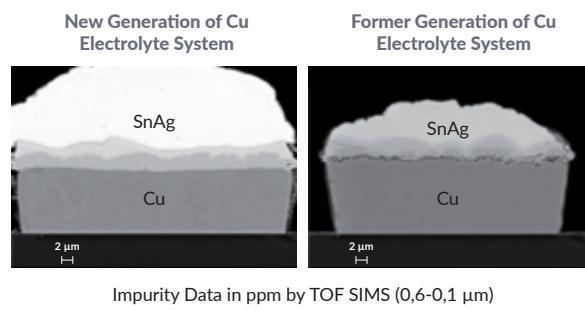
**Figure 4:** The same Cu pillar type (over  $\mu$ -via) as in **Figure 3**, plated with a new generation of electrolyte (Spherolyte RDL/ Pillar UF3). The pillar height is 45 $\mu$ m, and the diameter is 55 $\mu$ m. The plating was at a deposition speed of 3.3 $\mu$ m/min with a 1 $\mu$ m recess. Within-die and within-wafer nonuniformity are <3%.



**Figure 5:** Void formation in the intermetallic phase between Cu and SnAg. Voids appear as small black spots.



**Figure 6:** Example of void appearance and its suppression: a) (left) Void formation for a Cu-Sn interface after 250 hours of storage at 150°C; a chain of voids is visible; b) (right) There are no voids for the same Cu pillar with a 3 $\mu$ m Ni diffusion barrier between 20 $\mu$ m Cu and 15 $\mu$ m SnAg. Plated in a Fountain type plater at a deposition rate of 2.2 $\mu$ m/minute.



**Figure 7:** Cu-SnAg pillars after 250 hours of storage at 150°C: a) (left) The resulting pillar plated with the latest generation of Cu pillar electrolytes (Spherolyte RDL/pillar UF3) in a fountain plater without an intermediate Ni barrier; b) (right) The reference system is the Spherolyte RDL/pillar UF2. Both samples were plated at 2.2 $\mu$ m/min in a fountain plater.

such pillar types usually mirrors the exact depth of the  $\mu$ -via underneath. Such recesses can be used for placing solder material on top of the pillar, however, most packaging companies prefer perfectly flat surfaces. This in turn requires a completely different additive system, one with a different filling capability.

### Copper pillar plating for pillar in pad apps

Next-generation electrolytic systems are comprised of altogether different additives. The main role of these additives is to level out every recess while maintaining a flat surface on flat wafers (**Figure 4**). This requirement is a contradiction in itself for an electrolytic system. Therefore, these additives systems do not give perfectly flat pillar surfaces on flat substrates but rather slightly convex-shaped pillars. Nevertheless, the degree of this convex shape needs to be in-line with the usual requirement of 5% nonuniformity.

### Voiding in the intermetallic phases

It is a well-known fact that intermetallic phases between solder and Cu are prone to void formation [1,3]. These voids appear only after a certain heat treatment (reflow), and not directly after plating. An example for such a void formation is given in **Figure 5**.

The voids (black spots in **Figure 5**) appear after storing the wafer at 150°C for 250 hours, predominantly in the Cu-rich intermetallic  $\text{Cu}_3\text{Sn}$ . Voids appear

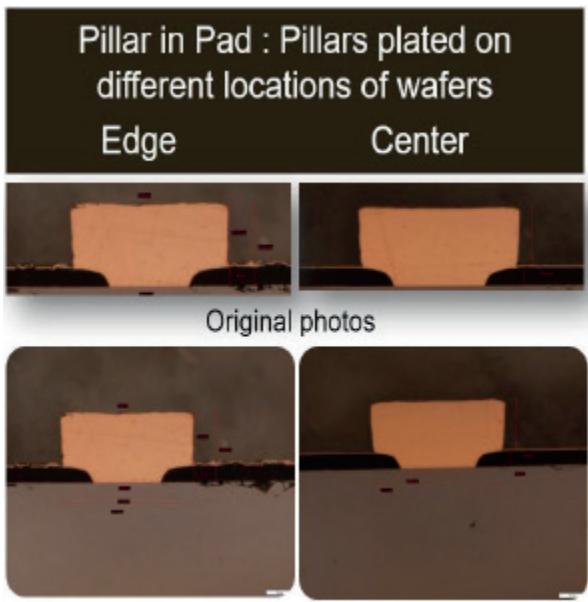
both with SnAg and Sn solders on Cu pillars. According to [1], such voids are caused by the electrolyte system itself, mainly by a complex formed out of leveler and accelerator (SPS) in the Cu process. Some accelerator/leveler complexes are significantly incorporated during the plating process and can lead to small crystallization failures. Cu and Sn are known to interdiffuse quickly into each other and so do the crystallization failures. The latter can accumulate at the boundary of Cu and  $\text{Cu}_3\text{Sn}$ . Severe voiding can lead to disintegration of the solder joint and result in electrical failures.

One strategy to avoid such voids is the use of a diffusion barrier between Cu and Sn, while another option is to use modified electrolyte additives that are less incorporated. The industry standard is to plate a thin Ni layer as a diffusion barrier. **Figure 6** shows the interface of such a metal stack (Cu-Ni-Sn) after heat treatment. There are no voids visible. The main disadvantages when using a Ni diffusion barrier are the additional process steps and the blocking of plating cells in the single-wafer tools, thereby reducing the overall throughput of the tools.

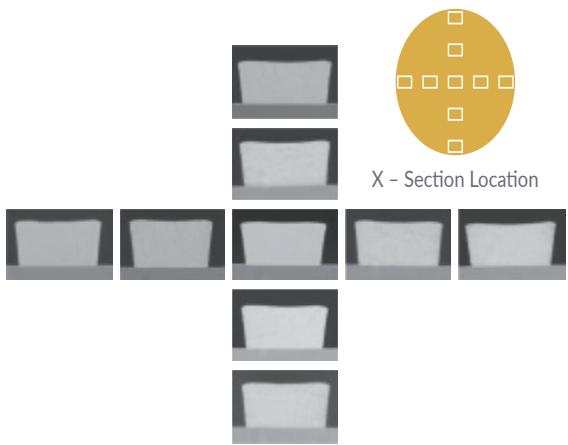
The new generation of Cu additives overcome the problem discussed above. These electrolytes show significantly reduced incorporation levels of additives into the plating bath. This has been proven by secondary ion mass spectrometry (SIMS). **Figure 7** compares the new generation of Cu pillar additives with the older generation. The resulting SIMS data show that the amount of examined incorporated impurities in the Cu pillar is significantly reduced. Impurities have been measured in a layer thickness of 0.6-1.0 $\mu$ m. As a consequence, the level of void formation is reduced to an acceptable amount.

### A new solution for copper pillar plating

The Spherolyte RDL/Pillar UF3 process is a solution that satisfies all performance requirements for Cu pillar plating. The main features of our new process are a pure Cu deposit due to low incorporation of additives, a nonuniformity of <5%, no voiding in the intermetallic phase prior to



**Figure 8:** Cu pillar in pad technology.



**Figure 9:** Example of profile uniformity of Cu pillars plated with Spherolyte chemistries at 20 ASD on MultiPlate. The cross sections were taken at nine different locations on a 300mm wafer.

reflow, faster plating at 15+ ASD (up to 4.4 $\mu\text{m}/\text{min}$ ), and the elimination of the Ni diffusion barrier typically required to prohibit migration and voiding in the intermetallic phase. Additionally, this next-generation electrolyte system is suitable for both standard pillar plating, as well as pillar in pad applications (Figure 8). Using this new process, plating of Cu pillar in pads is optimized and dishing is minimized.

### A new technology for high-speed pillar plating

While the new Cu electrolyte system has shown satisfactory results at standard current densities, as

requirements for high-speed pillar plating go well beyond 10 ASD, new technologies must be considered for optimal plating performance. In order to achieve successful plating at very high current densities (20+ ASD), completely new technologies are needed as the chemistries alone are no longer capable of optimum performance on standard fountain plating tools. Therefore, there is a need for new equipment that is capable of high-speed pillar plating at 20 ASD and beyond. The requirements for a tool capable of 20+ ASD must include systems and mechanisms for enabling optimized uniformity, low impurity incorporation and therefore, void-free plating, and highest possible throughput.

Our solution for enabling high-speed pillar plating is MultiPlate (Figure 9)—a tool for electrochemical deposition in advanced packaging technologies.

### Solutions for enhanced uniformity

The new system utilizes a reverse pulse system for optimal uniformity (no doming or dishing) in

high-speed pillar plating, made possible by an integrated multipurpose rectifier. A copper dissolving unit is implemented for monitoring and replenishing the Cu concentration via an external unit. This has a direct impact on the additive incorporation and purity of the bath, and therefore the uniformity and voiding performance of the deposited Cu.

Dimensionally stable inert anodes are used in a segmented design with two and three segments for 150, 200 and 300mm wafers or panels, respectively. The segmented anodes enable an adjustable current distribution throughout the entire wafer surface, allowing an optimized within-wafer

uniformity. An advanced fluid system is used for optimizing electrolyte flow distribution by means of a short distance from the cathode (wafer) to the segmented anode. This provides a direct flow to the wafer and improved agitation, both of which are required for high-speed pillar plating and a uniform thickness distribution.

And finally, a free programmable mechanical agitation mechanism enables the movement of the wafer holder within a mere 35mm from anode to cathode, thereby eliminating the risk of spray and flow patterns and consequently improving the overall uniformity.

### Summary

In summary, the Spherolyte UF3 process fulfills all requirements for Cu pillar plating; pure Cu is deposited using a high-speed pillar plating process, without compromising the voiding performance or uniformity. For next-generation requirements for pillar plating, at current densities beyond 15 ASD, MultiPlate is a solution for optimized performance; high-current density plating of pure Cu, with improved uniformity and voiding performance.

### References

1. Y. Yu, et al., "Effects of residual S on Kirkendall void formation at Cu/Sn-3.5 Ag solder joints," *Acta Materialia* 56, 5514-5523, 2008.
2. L. Yin, et al., "Controlling Cu electroplating to prevent sporadic voiding in Cu<sub>3</sub>Sn," *Electr. Comp. and Tech. Conf.*, 406-414, 2009.
3. S. Kumar, et al., "Microvoid formation at solder-copper interfaces during annealing: a systematic study of the root cause," *Jour. of Electr. Materials*, Vol. 40 No. 12, 2415-2424, 2011.

### Biographies

Cassandra Melvin received her BS in Business Management at Rensselaer Polytechnic Institute and is Global Product Manager for Advanced Packaging at Atotech Deutschland GmbH; email Cassandra.Melvin@atotech.com

Bernd Roelfs received his PhD in Surface Science and Electrochemistry at Free U. Berlin and is Global Product Manager for Advanced Packaging at Atotech Deutschland GmbH.

# The X-ray metrology of TSVs

By David Bernard, John Tingay, Philip Moyse, Will Heeley [Nordson DAGE]

Originally distributed at the International Wafer-Level Packaging Conference, San Jose, CA Oct. 13-15, 2015

**T**he emergence, development and use of through-silicon vias (TSVs) requires the availability of new inspection and measurement tools to validate the TSV manufacturing processes, to ensure and optimize TSV production yields, and to provide high quality QA data. The areas where this need is most acute is in the measurement of the level of voiding and other critical dimensions associated with TSV fill, recognized as one of the major causes of poor yield in the TSV manufacturing process. With TSV production most likely to be undertaken during the middle-end-of-line (MEOL) or back-end-of-line (BEOL) process flow, optical or infrared techniques cannot provide this void data. Therefore, the use of X-rays offers a valuable, fast and nondestructive method of inspecting and measuring TSVs, not just for voiding, but also for a range of other critical dimensions.

X-ray inspection/measurement has not been available for use in the applications noted above in the past owing to the limitations of X-ray tube resolution for the features of interest and the limited quantity of X-rays (or flux) that has been available to give fast data acquisition. However, this paper will present the results of nondestructive, on-wafer measurements on TSVs including their voids, with size and location within the TSV depth, as well as other critical dimensions using a new, production-ready X-ray metrology tool.

## The rise of HVM TSV manufacturing

The use of TSVs in “real products” has, until now, been limited to specialized field-programmable gate array (FPGA) devices that only have a tiny volume requirement. However, more recently, the use of TSVs has been announced for high-performance memory, providing improved operation and lower power consumption aimed at the enterprise server market [1, 2]. In addition, there have been further announcements to use these new memory configurations for new GPU applications [3] where the high-

performance memory assists and improves the overall GPU capabilities. As a result, the steady rise of TSV-based packages towards high-volume manufacturing appears to have legitimately started. TSVs are used in these devices as the connections through each of the stacked die in the package, as well as part of the interconnection between the dies. As the manufacturing volumes are stepped up, there is a vital need to optimize the manufacturing yield. In particular, this is necessary so as to mitigate the already more expensive cost of the die for 3D use owing to the larger silicon area required per die to locate the TSVs, and which cannot be utilized for transistors. In the typical TSV manufacturing process for these devices, the TSVs are created after metallization but before final packaging – the so called middle-end-of-line (MEOL).

When the empty TSV is initially produced in the die, in principle it is possible to see down the empty TSV optically so as to judge the quality of this manufacturing step. However, this is not easy to do because of the high aspect ratio of TSV features that limits the amount of light that can be reflected back to the optical detector from the bottom of the hole. At present, typical aspect ratios of TSVs in memory devices are in the 10:1 range with indicative sizes of around 5 x 50 $\mu\text{m}$  to 10 x 100 $\mu\text{m}$ . Once the TSV is subsequently filled with the conducting metallization (typically tungsten or copper) however, then there is no way optically, or by infrared techniques, that the quality of the fill process, and in particular the presence and location of voids that may have been caused in the TSV during the fill process, can be measured. It appears that using an increased fill speed to improve throughput is counterbalanced against an increased probability of voiding. Therefore, a compromise must be struck in production so as to optimize throughput but minimize/remove voids. If voids are not removed, then the presence of a trapped volume within a constrained plug of material in the

wafer/die has the potential to cause stress and other issues in the TSV/die, as the wafer will undergo other high-temperature processing steps in the subsequent manufacturing flow before ending up in the final package. As the status of the filled TSV cannot be seen optically, then the opportunity to evaluate and measure if voiding has occurred after fill has not existed so far. This analysis is required, not just in terms of potential cross-wafer variation caused by manufacturing variations, but there is also a need to understand at what depth it occurs within the via such that correctional activity can be applied, quickly, to the manufacturing process. At present, there is the real potential for defective TSVs to be created but not able to be measured, analyzed and identified as failures until much later in the production process, such as when connections are more readily available for external testing. Not only does this potentially delay the time until the faults are identified, together with the continuing production of additional quantities of defect material in the meanwhile, but there are also the substantial additional costs that will accrue for the many processing steps necessary to get to the point after TSV fill where the die can actually be tested.

Traditionally, the only available method that could be used in production to check the fill within a TSV, after the filling process is completed, is to use a focused ion beam scanning electron microscope (FIB-SEM) tool. Here, an individual TSV on a wafer can be excavated by etching away the surrounding silicon material before etching and micro-sectioning through the TSV to present the fill quality as a series of SEM images. Such a procedure can typically take hours to complete, can only be undertaken on a single TSV and that TSV is then destroyed in the process. The results for this single TSV has then to be assumed to extrapolate to many, or all, other TSVs on the rest of the wafer. A wafer may contain many hundreds of

thousands of TSVs, or more, in number. Furthermore, should warpage within the wafer exist, then the fitness of this single result as representative of everything on the wafer will be further called into question. This is why Nordson DAGE has developed an entirely new X-ray metrology tool (XM8000) to provide the opportunity to investigate and automatically analyze TSVs on a wafer, in a fast production-efficient manner, for the quality of voiding and other critical dimensions following fill – and to do this entirely nondestructively.

This approach is different from the use of X-rays that may be more familiar within the wafer foundry where X-rays are used for diffraction (XRD) and fluorescence (XRF) measurements. In this tool, X-rays are used in transmission mode. This is achieved by using recent developments in X-ray technology that have been developed specifically for the electronics industry [4, 5] together with the use of novel 2D and 3D X-ray analysis techniques [6]. This new tool provides automatic, nondestructive measurements of voiding and other critical dimensions on the smallest of TSVs, allowing better quality assurance much earlier in the TSV manufacturing process. This new tool has already been successfully applied to automatically analyzing voiding and critical dimensions of wafer bumps and solder bumps on copper pillars, whose feature size can be below 20 $\mu\text{m}$  in diameter.

## 2D X-ray analysis

The Nordson DAGE XM8000 X-ray Metrology system can be configured to provide measurements using both 2D and 3D X-ray techniques. The 2D X-ray methodology, most commonly used for the measurement and defect review on wafer bumps and solder bumps on copper pillars, takes an image of a field of view (FOV) on the wafer and automatically analyzes the image in real time to provide void measurement, critical dimensions and defect review (e.g., missing bumps, etc.), with all the data correctly assigned to the specific bump in the specific die on the (up to) 300mm wafer. 2D metrology only requires a single “top-down” image to be analyzed. Operational throughput for 2D analysis is, therefore, based on the minimum size of the flaw(s) that is to be detected to a high confidence level in a specific feature (e.g., void size in the bump). This criterion then defines a FOV (or image magnification) that must be used to achieve this aim. Each FOV takes a finite time to complete as it

must include the time to create a suitably clear X-ray image for automatic analysis, as well as the time to make the analysis and to move the sample manipulator precisely to the next FOV. The size and pitch of the features to be analyzed will determine the quantity of features that can be analyzed in a single FOV. Overall throughput, therefore, will be a multiplication of the number of FOV needed to cover the desired analytical regime and the time taken per FOV (ignoring wafer load/unload).

The suitable tool magnification is set by the user. It needs to provide sufficient pixels in the image to cover the minimum void size that is to be captured and identified in the bump to the required level of confidence. This is true, whether it is a single void or multiple voids in the same bump. In this way, any void that is equal to, or greater than, the minimum desired void (in the bump) will be identified in a single analysis pass. Should a user demand that a smaller minimum void needs to be identified in each bump, it requires that a higher magnification X-ray image is used. Therefore, the FOV will be smaller, with fewer features analyzed per FOV, and so requires more FOV to cover the same number of features on the wafer, thereby reducing throughput. Conversely, accepting a larger minimum-detectable void allows a lower magnification X-ray image to be used, thereby providing a larger FOV for each image, and so allows increased throughput.

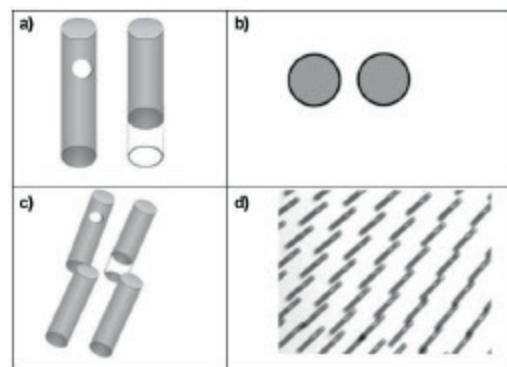
## 2D X-ray approach for TSVs?

It would be hoped that the 2D X-ray techniques successfully applied to wafer bump metrology could also be used for TSV analysis. Unfortunately, this is not the case. A top-down 2D X-ray image cannot be used to identify and measure voids and critical dimensions for TSVs. This is because of two main reasons. The first is the density, or lack thereof, of the material in the filled TSV. The second reason is caused by the effects of what is called projection distortion.

With filled TSVs able to be less than 10 $\mu\text{m}$  in thickness, it can make it very difficult to see in the image the lower absorption of the X-rays as they pass through the less dense regions caused by the voids (or partial fill) when compared to the relative density of a “fully-filled” TSV. This will be even more difficult to do if the minimum void to be

detected is also small (see **Figure 1a, 1b**). As a result of this situation, a top-down view cannot be used to inspect the TSV. It might be considered however, that for the human eye, an oblique angle view X-ray image could be used for the analysis instead. Unfortunately, such an approach is the second reason for the inability to use the 2D view for TSV analysis. Although the oblique-angle X-ray view does indeed indicate the presence, or absence, of voiding down the length of the TSVs (see **Figure 1d**), the effects of projection distortion on the image (**Figure 1c**) makes automatic analysis from these types of images difficult to do and reduces the precision of the measurement. Projection distortion is a phenomenon caused by the effects of having a point source of X-rays passing through the sample and then being detected on a large-area, flat detector (**Figure 1c**).

Projection distortion, sometimes called gun-barrel distortion, causes objects located towards the edges of the FOV to have an angle of view that is greater than the angle of view at the center of the FOV (see **Figures 1c** and **1d**). This causes high aspect ratio features, such as TSVs, to overlap each other as you go towards the edge of the image. This effect is accentuated, and is seen closer towards the center of the FOV, as the pitch of the features reduces. While this effect can be discerned, and somewhat discounted, using the human eye (see **Figure 1d**), it does not provide a reliable method for automated image analysis. This is because even a very slight angular variation of the detector capturing the X-ray image will cause a great deal of change in which features are overlapped, and by how much, making it



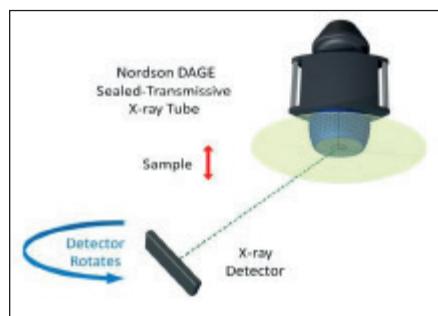
**Figure 1:** Issues of using a 2D-only X-ray approach for automatic TSV metrology: a) TSVs containing voids or a partial fill; b) Top-down 2D view of TSVs. The presence of voids or a partial fill cannot be distinguished in the X-ray image against the background density down the TSV; c) The effects of projection distortion on X-ray images; d) Oblique X-ray image of 10 x 100 $\mu\text{m}$  TSVs containing voids.

very difficult to automatically define where one TSV ends and the next starts. Therefore, fully automated analysis cannot practically use this oblique-angled 2D approach. Instead, a 3D X-ray approach has to be used for automated TSV analysis.

### 3D technique for TSV analysis

The 3D X-ray that is used for TSV analysis is a partial computer tomography, or PCT, technique. This has similarities to the computer tomography (or CT or CAT) techniques that are used in hospitals for diagnostic imaging. It should not be confused with what can be called a full  $\mu$ CT technique, as this is usually much more time consuming to undertake and is limited to only analyzing very small samples in the sufficient resolution required to detect typical failures. See reference [6] for more details.

In the PCT 3D X-ray technique, many 2D X-ray images are taken of the same sample FOV with the detector at a fixed oblique angle rather than from the “top-down” position. Images are taken from  $360^\circ$  around the FOV. In the XM8000 tool this is achieved by the detector being rotated around the X-ray tube – to – wafer axis (**Figure 2**). This movement geometry not only captures the necessary oblique view X-ray images, but also ensures that the wafer does not need to be moved away



**Figure 2:** Schematic of PCT (3D) X-ray methodology.

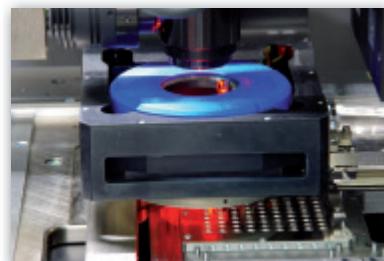
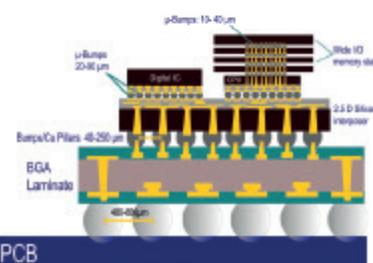
from its proximity to the X-ray source. If the wafer was tilted to achieve the oblique view, as an alternative approach say, then the necessary movement of the wafer away from the tube to prevent collision would result in a greater separation between tube and sample and that directly affects the geometric magnification that the system can apply. With such small features as TSVs to be

analyzed, the loss of any magnification would compromise the detail in the 2D images and therefore limit the resolution in the final 3D model [5, 6].

Once all the 2D oblique-view X-ray images have been acquired, a 3D model of the density variations (TSV features) within the FOV can be mathematically/computationally reconstructed from them by using appropriate CT algorithms. This generates a 3D model

comprising voxels, or volume pixels. It is this 3D model that can then be visualized, virtually sliced and diced in any plane, and therefore analyzed to provide the required measurement data on the TSVs. For example, the 3D model can be cut in any horizontal plane down the z depth of the TSV into the wafer, like a virtual cross section, to provide the presence, or absence, of voiding and critical dimensions at

## Sub Micron Die Attach Solutions



### Ultra Precision Die Placement & FC Bonders for Advanced Semiconductor & Opto/AOC Packaging

#### Features

- Down to  $\pm 0.5 \mu\text{m}$  @  $3\sigma$  Die Placement Accuracy
- Highest Speed at Ultra Precision Placement Accuracy
- Unique Dynamic Alignment System
- Eutectic Die Attach via a Unique Laser Soldering System
- Integrated Heated Bond Tool and Pulse Heater Option
- Up to 600 mm x 600 mm Bonding Area
- Active Bond Force Control
- Quantitative Parallelism using an Autocollimator
- UV Dispense and UV Cure for In-situ Lens Attach
- Process Ultra Small Die Sizes  $< 100\mu\text{m} \times 100\mu\text{m}$

#### Markets

- SiPhotonics
- Laser Bar
- 3D/2.5D IC
- TSV / TCB
- Fan In/Out
- eWLP



NOVA<sup>Plus</sup>



AFC<sup>Plus</sup>



**Learn More:** [www.amicra.com](http://www.amicra.com)

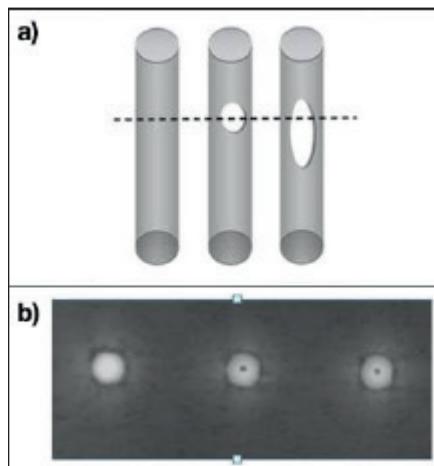
Upcoming trade shows:

ECTC - Las Vegas, NV; June 1-2, Booth: 214

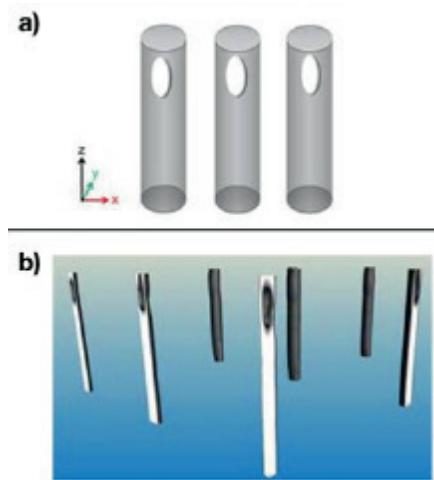
SEMICON West - San Francisco, CA; July 12-14, Booth: 6173

IWLPC - San Jose, CA; October 18-20, Booth: 14

that particular depth (**Figure 3**). These are not the original 2D X-ray images, but reconstructed 2D images that can be obtained from any plane in the 3D model. Additionally, vertical planes can be taken and analyzed through the model to provide, with additional 3D rendering of the CT model, an appreciation of the whole TSV (**Figure 4**), which may be saved in the event of a flaw being detected.



**Figure 3:** Use of a 3D, or PCT technique, to generate a 3D model from which measurements can be taken from 2D reconstructed slices; a) 3D diagram model of TSVs. The dotted line indicates the selected plane of the 2D reconstructed image seen in **Figure 3b**; b) A 2D reconstructed X-ray image from a 3D model at the plane shown. The size and the location of the voids and other critical dimensions in this plane can be seen and measured.



**Figure 4:** 3D visualization of a 3D model of TSVs showing the presence and position of voids; a) A 3D diagram model of TSVs with voids; b) A 3D visualization of a reconstructed 3D model showing cut-planes exposing the voiding within the TSVs and indicating their location down the TSV.

This 3D approach allows the XM8000 tool to automatically measure the majority of TSVs seen in the whole FOV under analysis, as they will all be reconstructed in the 3D model, so each has its own volume of voxels for analysis. Furthermore, any effects of overlaps between TSVs, caused by the projection distortion in the individual original 2D X-ray images, is completely removed in the 3D model. In this way, together with the fast and highly precise wafer vacuum chuck movement, the XM8000 can measure, nondestructively, automatically and in real time the following TSV data:

- Length of TSV and percentage of partial fill;
- Total void volume in the entire TSV;
- Single largest void in the TSV (by horizontal cross-sectional area in percentage);
- TSV depth profile – for example, to check for any cross-sectional diameter variation down the TSV; and
- TSV orthogonality – the offset of the TSV from being perpendicular to the direction through the wafer.

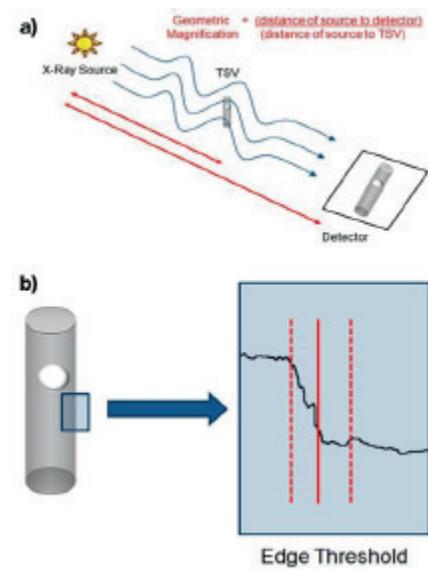
The results are available and identifiable for each specific TSV/die/wafer. Historically, even if simpler, off-line X-ray tools were used just to visualize the filled TSVs using oblique views as a simple inspection check, these systems did not have the manipulator precision to allow for the identity of the TSVs seen to be explicitly identified and therefore, repeated inspection, let alone measurement, could not be guaranteed to apply to the same features.

Throughput for TSV metrology will depend, as for bumps, on the minimum level of voiding that is to be detected, subject to the limitations of low overall material density that exists with such tiny features when viewed in X-ray. It is understood that FIB-SEM analysis of a single TSV can typically take many tens of minutes to hours to achieve. In contrast, using the XM8000 at a setting where a typical FOV used to identify a 1 $\mu\text{m}$  diameter void in a 5 $\mu\text{m}$  diameter TSV and which contains ~30 TSVs, this then works out that sample movement, imaging and real time nondestructive analysis takes ~1s/TSV, with all the data available for each TSV analyzed.

## Measurement bias and causes of error

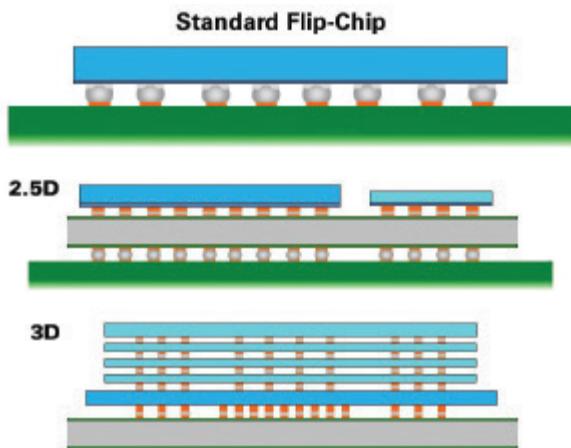
As with all metrology techniques, the cause of error and bias, where equivalent measurements can be made, must be considered. This is especially true for this novel use of X-ray metrology, when comparing with optical and other techniques that are more familiar within the wafer foundry, as well as for having confidence in the results. The sources of error within X-ray metrology mainly can come from the geometric magnification used in the image and the edge detection threshold applied. This ignores the errors associated with the conversion of measurements from images, as this will be common to other optical and infrared techniques.

As the TSV fill material absorbs proportionally more X-rays than the surrounding silicon material, it creates a contrasting image on the X-ray detector. As has been discussed, the 3D volume used for measurement is built up from a reconstruction of multiple 2D X-ray images (see **Figure 5a**). When using X-ray imaging, if there are small errors in the TSV to source distance, then this will vary the magnification in each image (i.e., compared with if the source to detector distance remains the same). Therefore, if the system manipulation is not as precise as it can be, then it could result in the TSV size being reported differently in each image that creates the 3D model (see **Figure 5a**).



**Figure 5:** Sources of potential error in X-ray metrology; a) X-ray imaging of a TSV from absorption variation and the effects of geometric magnification; b) Edge thresholding error.

# Ultra-Low Residue No-Clean Flip-Chip Fluxes



Eliminates the cost of cleaning away flux residues. Prevents damage due to die and joint.

- Flip-Chip Flux NC-26-A
- Flip-Chip Flux NC-26S
- Flip-Chip Flux NC-699

*Learn more:*  
[www.indium.us/E042](http://www.indium.us/E042)

From One  
Engineer  
To Another®

[www.indium.com](http://www.indium.com)  
[askus@indium.com](mailto:askus@indium.com)

ASIA • CHINA • EUROPE • USA



©2016 Indium Corporation

To make the 3D model, or measure directly from the 2D X-ray image, it requires that a suitable edge detection threshold level is set in the software. As the X-ray spot size is larger than optical techniques and the absorption of X-rays is not linear, the threshold must be such that it is able to identify the TSV to a sufficiently high confidence level. Therefore, the X-ray image will see the fill material but not the low density barrier layers, and so the reported size of the TSV may be smaller than for other metrology equipment. The same is also true for negative structures, such as voiding, within the TSV. With very high uniformity of X-ray measurements across the wafer, a limited number of FIB-SEM results would allow calibration/validation of this threshold. It is crucial that the edge threshold used for measurements remains consistent in the tool in order to provide good repeatable data over time (see **Figure 5b**).

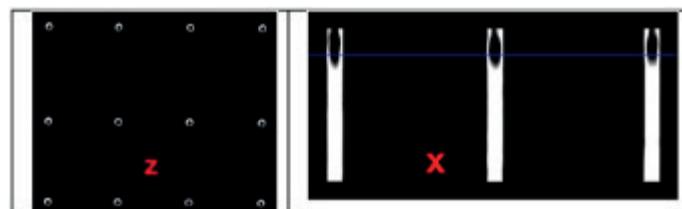
## Experimental

The authors gratefully acknowledge the Fraunhofer IZM-ASSID, Dresden, who have supplied Nordson DAGE with a special TSV wafer manufactured with deliberate void defects to analyze on the XM8000 tool. The tool settings used were as follows:

- X-ray tube power = 3.0W
- X-ray tube accelerating voltage = 40kV
- Image resolution 0.25µm/pixel to 0.20µm/pixel
- Image averaging = 24fps/integration time of 1s
- 12 images per FOV to make a 3D model
- Class-1/ISO-3 above-wafer cleanliness
- Vacuum chuck can handle up to 3.0mm of warpage
- 642 TSVs analyzed in every die of the wafer
- 115 dies/wafer in 12 rows x 12 columns
- 73,892 TSVs analyzed in total on the 300mm wafer
- Nominal TSV diameter ~10µm
- Nominal TSV length ~100µm

## Results

The output of the tool is data on each TSV measured, which is achieved by analyzing the 3D model of each TSV. A view of the 2D reconstructed visualization of some example TSVs is shown in **Figure 6**. These images are from TSVs with a nominal diameter of 5µm and a nominal length of 50µm, but similar images are available from the larger sized TSVs in the IZM-ASSID test wafer.



**Figure 6:** Nominal 5 x 50µm TSVs containing voids: reconstructed 2D views in x and z planes from the 3D model.

**Figure 7** shows selected results from the test wafer. **Figure 7a** shows the total missing material (i.e., total of all voiding in the whole TSV) in the worst measured TSV for each die. This is then used to create a wafer map of the defect levels. The

# Cohu

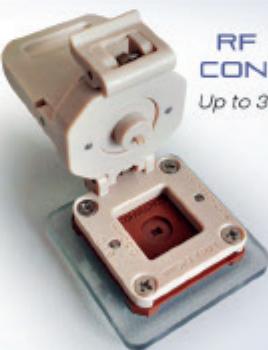
## INTEGRATED TEST SOLUTIONS



for Turret, Gravity,  
Pick & Place and  
Test-In-Strip Handlers

with applications available for RF, High Power,  
MEMS sensors, Bare Die, Digital and Analog ICs  
and LED test

**NEW!**



**RF SCRUB  
CONTACTOR**

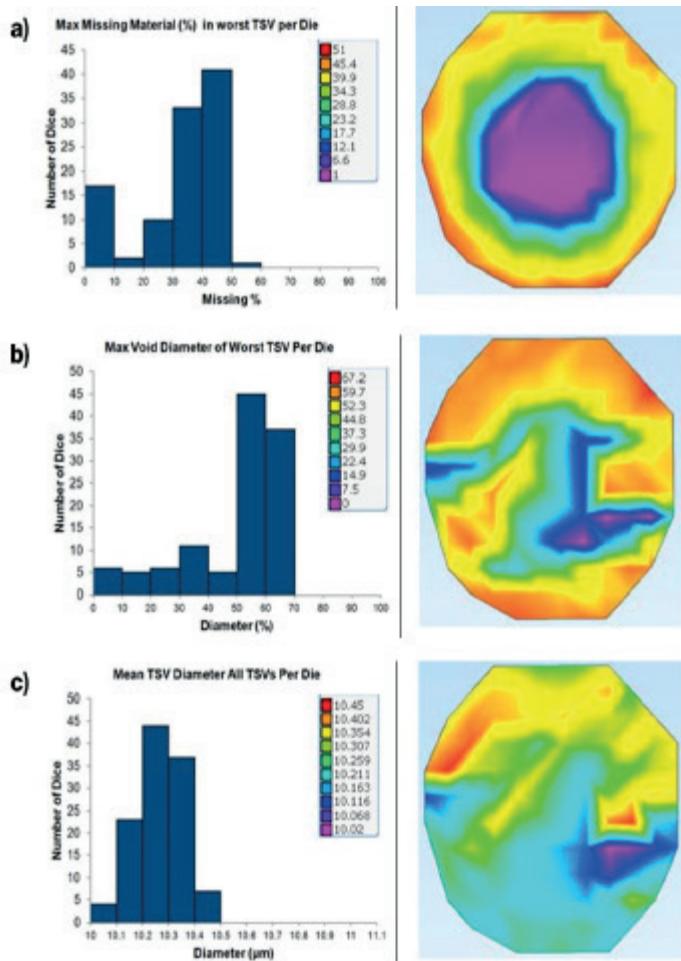
Up to 33 GHz @ -1dB

### NOW OFFERING:

*Spring Pins, RF and  
Cantilever Kelvin Contactors*

- Excellent performance
- Worldwide engineering and service support
- Continuous innovation for new applications

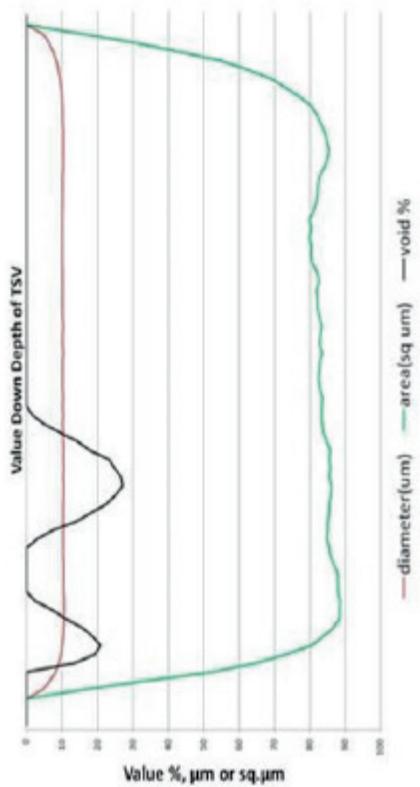
[cohu.com/products/contactors](http://cohu.com/products/contactors)  
Contact: [ITSinfo@cohu.com](mailto:ITSinfo@cohu.com)



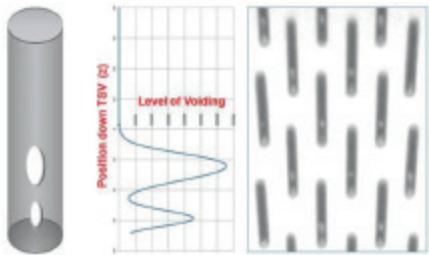
**Figure 7:** Results from the test wafer with wafer map variation: a) Maximum missing material in the worst TSV per die; b) Maximum void % diameter at any point in the depth for the worst TSV per die; c) Mean TSV diameter of all measured TSVs per die.

wafer is not shown as circular in the map as an artifact of the relatively few die on this particular wafer. **Figure 7b** shows the maximum void % by area at any point in the length of the worst TSV for each die. **Figure 7c** shows the average of the diameter measurements along the length of each TSV for all TSVs measured per die, indicating that the XM8000 can provide critical dimension data by depth in addition to voiding information.

The results, shown in **Figure 7**, have been simplified to indicate, in essence, the worst situation from the worst TSV measured per die. However, it must be remembered that underlying this data is the result for each and every TSV measured, such as that shown in **Figure 8**. All this data is available in a readily-manipulable format such that additional useful information can be extracted from the dataset as the X-ray tool opens up new measurement paradigms and opportunities in the production area. For example, **Figure 9** shows an aggregate result for the level of voiding in all the TSVs measured on the wafer. The positions in z, on average, of two distinct voiding areas in the TSVs on this test wafer are clearly visible and are backed up by the 2D oblique view X-ray image.



**Figure 8:** Results of TSV diameter, fill area and void percentage of area as the 3D model is analyzed down the depth of a single TSV.



**Figure 9:** Average of all void data by position in the z direction down the TSV from all TSVs measured in the test wafer.

## Summary

A new method for TSV metrology on wafer has been described that includes the ability to accurately measure voiding and other critical dimensions, as well as their values in the z-depth of the TSV. The throughput of measurement for TSV analysis will be slower than that for wafer bump metrology owing to the need for more 2D images to be taken to produce an accurate 3D model from which the data is extracted. Therefore, nondestructive TSV metrology on this tool may still be limited to a sampling regime per wafer rather than the 100% inspection that is a realistic opportunity

for wafer bumps. However, it does represent an opportunity to make multiple, nondestructive measurements on TSVs across a wafer that will be many thousands of times faster than would be required to test, and also destroy, a single TSV using an FIB-SEM tool.

## Acknowledgments

The authors would like to thank the entire Nordson DAGE Team for all their great help with this paper. We should also like to acknowledge Fraunhofer IZM-ASSID, Dresden, for supplying the test wafer.

## References

1. “Samsung starts mass producing industry’s first 3D TSV technology based DDR4 modules for enterprise servers,” Samsung press release, 28 Aug., 2014.
2. “TSV-based memory going to volume production: the era of 3DIC finally begins,” Yole Développement press release, 1 Dec., 2014.
3. “Nvidia’s 2016 roadmap shows huge performance gains from

upcoming Pascal architecture,” [www.extremetech.com](http://www.extremetech.com), 17 Mar., 2015.

4. D. Bernard, K. Bryant, “The implications of recent technology advances for X-ray inspection in electronics,” Proc. of the SMTA Inter. Conf., Fort Worth, TX, 16-20 Oct., 2011.
5. D. Bernard, “Selection criteria for X-ray inspection systems for BGA and CSP solder joint analysis,” Proc. of Nepcon Shanghai, 2003.
6. D. Bernard, D. Golubovic, E. Krastev, “3D board-level X-ray inspection via limited angle computer tomography,” Proc. of the SMTA Inter. Conf., Orlando, FL, 14–28 Oct., 2012.

## Contact author

David Bernard is Business Manager Automated X-ray Systems at Nordson DAGE; email [david.bernard@nordsondage.com](mailto:david.bernard@nordsondage.com)

Visit us on our website  
**www.e-tec.com**

**E-tec** Interconnect

**NEW**  
**in the Test Socket World:**

**E-tec Interconnect is pleased to present its new Clamshell Open Top Socket**

- **High reliability** up to 500k insertion cycles
- **High frequency** up to 27 GHz in pogo pin (up to 40GHz validated, with Elastomeric contact technology)
- Thru-hole technology, SMT, Solderless Type  
Also pluggable into adapter MiniGridSocket series (see E-tec catalog TS01)
- All kinds of packages, even your latest special custom packages

Flat Pack
PGA
LGA
Ceramic spatial
LCC
BGA
QFN / Power QFN
Custom

**E-tec Interconnect AG**, Mr. Bud Kundich, Los Altos CA 94024, USA  
Phone : +1 408.746.2800, E-mail : [info-us@e-tec.com](mailto:info-us@e-tec.com)

EP Patents 0897655, 1385011, 0829188, US Patents 6249440, 6190181, 6390826 and Patents in other countries

# The Internet of Things and MEMS packaging

By Vik Chaudhry, Adrian Arcedera [Amkor Technology, Inc.]

**M**any experts regard the Internet of Things (IoT) as the third wave of technology. The personal computer (PC) created the first wave in the late 80s and early 90s. The cell phone initiated the second wave. It is widely believed that the IoT will be the third wave of technology where engineers use the experience and infrastructure of the first two waves to make day-to-day chores more connected for increased comfort, convenience and safety.

The transition of PCs from large desktop items with large under-the-desk boxes to highly portable laptops, and the transition from brick-sized, single-function cell phones to pocket-sized, multifunction smartphones resulted from an equally dramatic, but not as visible, transition from discrete packaged semiconductors to complex flip-chip integrated circuits (ICs) and multi-chip modules. Similarly, the IoT will require substantial IC packaging changes to achieve its expected growth potential.

## Background on IoT growth and pervasiveness

“Smart” is a term commonly associated with products targeting the IoT. Any smart system is built with some basic building blocks. The most commonly used building blocks in an IoT system are: 1) Sensors and actuators; 2) Analog and mixed-signal translators; 3) Microcontrollers or embedded processors; 4) RF connectivity; and 5) Power management.

Sensors provide the changes in environment or status to a microcontroller or embedded processor, that in turn performs necessary calculations or makes decisions. This information is communicated through RF connectivity to the cloud or a local network, and once the necessary actions are determined, the response

can be communicated back to a receiving node where an actuator can take appropriate actions. This initial IoT implementation is becoming smarter in terms of taking actions once a threshold is observed. In applications where action is required, greater capabilities can be found both on the sensor, as well as on the actuator side.

Microelectromechanical systems (MEMS) sensors play a significant role in the IoT. The other aspects include embedded processors and RF connectivity. MEMS sensors with other IC technologies are rapidly becoming highly integrated sensing nodes that process the sensor data and then communicate it to a local or remote location either directly, or through the IoT. While the embedded processors and RF connectivity have been adopted over time, MEMS is relatively new. However, the MEMS adoption rate is quite high and as a result, system designers expect the cost reductions to be high. Based on the use of MEMS technology, sensors for the IoT are projected to reach a trillion units in the next decade [1]. However, lack of standardization (i.e., one product – one ASIC – one package – one test system) will delay this monumental growth.

## Packaging issues

While people are increasingly aware of the IoT and the promise of connecting billions of things together, many system designers are not aware of the packaging changes that are required to achieve this growth. On the other hand, the semiconductor industry is well known for meeting the packaging needs of innovative new products based on available package technologies, and then optimizing the packaging to achieve cost reductions. This trend is also occurring in the IoT area.

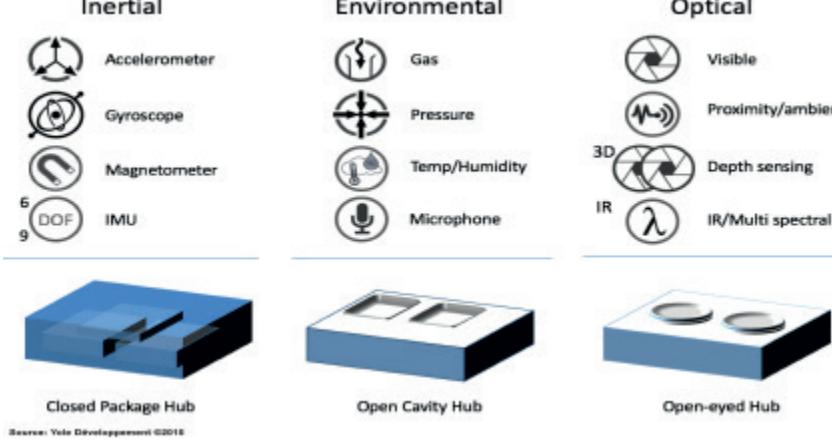
Today’s designs must transition to more advanced solutions that combine more and more functionality into a single

semiconductor package. With the high level of integration, concerns for EMI, package stress, and testing complexity are just a few of the issues that arise. Historically, packaging has always been the last, or among the last issues that is addressed in system design. In many cases, packaging has been an afterthought. While this has been changing, progress still needs to be made in many design circles to provide optimum system design advantages.

Solving the packaging issues for consumer products is difficult enough, but providing industrial packaging solutions means even more challenges. While designers working on the IoT are well aware of the building blocks, they usually are not prepared to address the challenges that result when these building blocks are packaged together in a single IC-style package. Common requirements for an IoT package are low cost, low power dissipation for silicon, and very good power dissipation characteristics for the package, and good RF shielding in packages that support multiple RF standards including Bluetooth® Low Energy (BLE), Wi-Fi, or ZigBee®, and others. With MEMS sensors in the IoT package, stimulus delivery is another important aspect, therefore cavity-based solutions are popular. Another requirement is a production-ready package to meet market timing. Waiting for a new custom package is usually not an option. A small footprint, whether it is a discrete solution or an integrated solution, is necessary in any case.

## Today’s packaging solutions

Market analysts at Yole Développement have identified three sensor clusters that exist in today’s smartphones—the sensors clusters include a closed package, an open package and optical clusters. They expect these clusters to have increased integration in the future with system-in-package (SiP) technology as the primary means of achieving the increased integration. As shown in [Figure 1](#), the different clusters target different



**Figure 1:** Integrated sensor clusters in smartphones vary based on sense parameters.

SOURCE: Yole Développement.

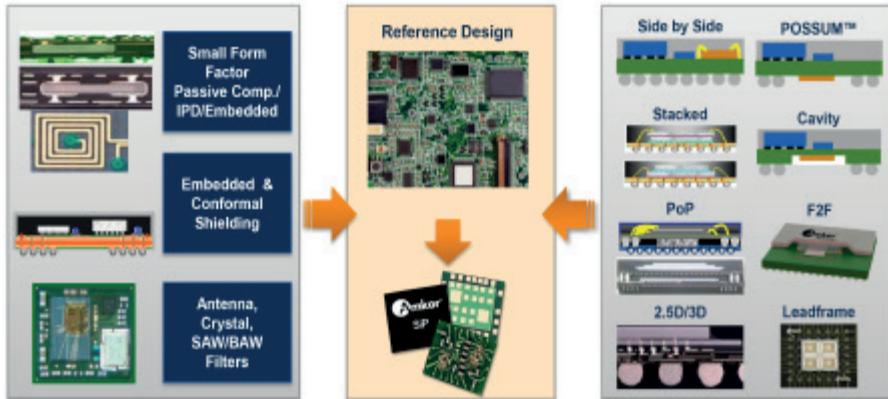
sensing requirements. The closed package isolates inertial measurement unit (IMU) sensors from the environmental impact of torsion and humidity. These are typically overmolded plastic packages.

In contrast, the open-cavity cluster requires access to the environment for measurements such as pressure, humidity, gas, and more. The optical or open-eyed cluster also requires access to the external world and, in fact, a line of sight. Each of the packages in these clusters has unique design requirements.

SiPs are an ideal way to combine sensors, embedded processors, and RF connectivity together in a small form factor that meets both footprint and height constraints. With this packaging approach, manufacturers can combine different technologies very quickly without spending a lot of money on new mask sets.

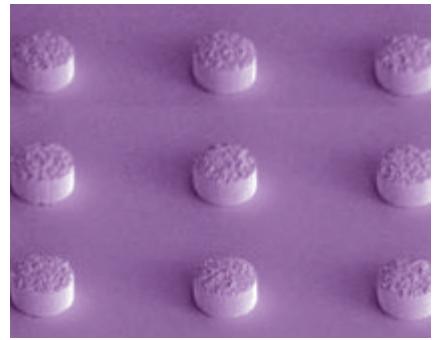
In addition to quick time-to-market, a SiP allows manufacturers to use off-the-shelf components to build a system solution. Because all the building blocks are already in product form, it is relatively easy for packaging engineers to rearrange them to get optimal performance in terms of antenna location, power dissipation, and other critical design criteria.

As **Figure 2** shows, a SiP can be a combination of several technologies including wafer-level packages, 2.5D or 3D structures, wire bonding, package-on-package (PoP), and more. SiPs can also include embedded passives, conformal shielding, filters and antennas. Combining all these technologies or components into a single package can be very beneficial for wearables where space and size are critical, as well as smart home and other smart applications, where space and size are also important.



**Figure 2:** SiP module design options take many forms.

While using some of the same foundry processes as CMOS devices, MEMS devices are different in many ways. For a MEMS sensor to interact with the environment, the package needs to deliver the stimulus to the chip. The stimulus can be in the form of vibration, humidity, pressure, light and more. Because the MEMS device is a mechanical structure with very small features, environmental contact must address particulates and the possibility of foreign matter



**QUALITY SILICON WAFER  
PROCESSING  
SINCE 1995**



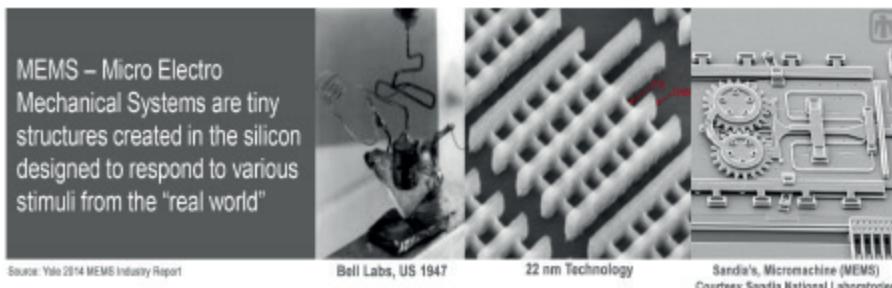
IMAT specializes in Thermal Oxidation and PVD Metal Deposition of silicon wafers. IMAT also provides custom patterned photoresist for a variety of applications on 8" and 12" wafers.

Ask us about how we can help streamline your tasks.

**IN-HOUSE PROCESSING**  
**THERMAL OXIDATION**  
**METAL SPUTTERING**  
**METAL EVAPORATION**  
**THICK RESIST PATTERN**  
**CUSTOM PHOTORESIST PATTERNING**  
**FORMING GAS ANNEAL**  
**25MM-450MM**



[www.imatinc.com](http://www.imatinc.com)

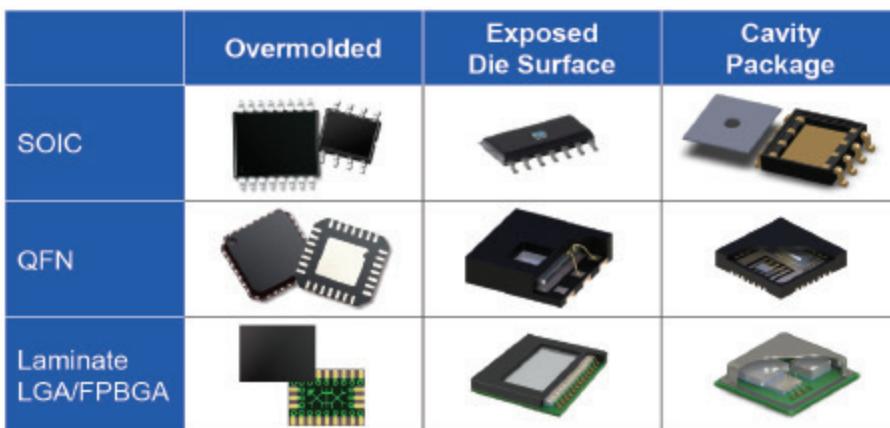


**Figure 3:** The packaging challenge: stimulus delivery. SOURCE: Yole Développement, 2014 MEMS Industry Report.

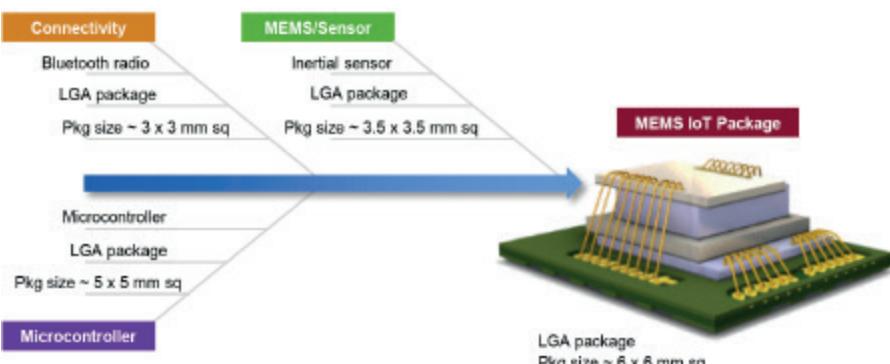
	Connectivity	Memory	Power Management	Microprocessor & Microcontroller	MEMS & Sensor
SOIC/TSSOP		✓		✓	✓*
QFN/TQFP	✓		✓	✓	✓*
Laminate CSP	✓	✓	✓	✓	✓*
WLCS	✓		✓	✓	✓*

\*Limited Compatibility

**Figure 4:** Current discrete (single-technology) packaging for the IoT.



**Figure 5:** Evolution towards standardization for MEMS/sensor packaging.



© Copyright Amkor Technology, reprinted with permission.

**Figure 6:** Adding IoT blocks to a MEMS/sensor package.

contacting the structure. **Figure 3** helps to visualize the challenges.

MEMS devices do not scale in the way CMOS devices scale with different processes. This means that there are no roadmaps for the MEMS process nodes. As a result, planning and packaging pose even greater challenges for MEMS devices.

**Figure 4** shows standard packages that exist today for IoT applications. Note that MEMS and sensor packages are typically modified versions of packages used for other technologies and the modifications are not standardized. Packaging designers tend to use the same packages, but the changes are typically not compatible for a given application. This situation increases packaging cost.

SiP design methodology and standardization are among the approaches for cost reduction. If the package is standardized, cost is reduced by spreading development, assembly and testing costs over higher volumes with economies of scale, rather than each company using a custom packaging design.

Standardizing the packages for MEMS sensors not only helps lower the cost, but also helps increase the adoption of MEMS solutions in the market. Standards build manufacturers' confidence to enter the market with the reliability data that allows them to stand behind their products. When the forms of packages are fragmented, the reliability or field experience data is limited and it delays the adoption by manufacturers. **Figure 5** shows different package types that could be used, or at least proposed as goals for standardized packaging that match the three cluster classifications identified previously.

The size of an IoT design can be reduced through package-level integration as shown in **Figure 6**. The initial IoT solution was more than 10mm<sup>2</sup> in area using discrete packages - a separate package for each technology. With the integrated package solution, the final size is about 6mm<sup>2</sup>. This reduction of 40% does not include the space saving in routing the signals. Expanded design capability to combine traditional layout expertise with digital and RF circuit design and system modeling is essential to achieve this advanced package-level integration.

## Evolving packaging solutions and issues

The packaging for MEMS devices is transitioning from quad flat no-leads (QFN) packages to laminate-based packages. Packaging alternatives include cavity-based packages or hybrid cavity packages with half of the package molded and the other half with a cavity for the MEMS device (**Figure 7**). While the molded part is more robust and can handle harsh application conditions, many of the sensors need the

cavity to interact with the environment as noted earlier.

Several advanced packaging design techniques will be involved in achieving the appropriate highly integrated, self-powered MEMS sensor node that senses, computes and communicates with the IoT. The 3D approach shown in **Figure 6** will evolve based on PoP, chip-on-substrate, chip-on-wafer, advanced interconnects including interposers and thru-mold via (TMV®), advanced materials including inter-layer dielectric (ILD) materials, film-over wire (FOW), conformal shielding, and other techniques that are either being developed or being used for one of the other technologies today.

Conformal shielding provides an excellent example of a system-level solution for combining technologies, while avoiding electromagnetic radiation effects among electronic components within a SiP and with the surrounding environment. Using a sputtering shielding technology to replace bulky metal shielding has zero impact on package size and weight, with excellent electrical and magnetic shielding performances.

Other package-level issues that must be solved for an advanced multi-technology IoT device to pass rigorous quality testing include: chip-package interaction, warpage of thin high-density packages, delamination, and more.

When multiple-die in a single package are pushed to their highest performance capabilities, thermal stress is always a major consideration. Thermal enhancement options to ensure that each die operates within its thermal limits may require: 1) Thermal vias; 2) Stacked Cu-filled via structures; 3) Direct-to-metal die attach pad structure; 4) Enhanced thermal die attach compound; 5) Enhanced thermal mold compound; 6) Detailed mechanical test and simulations for mechanical SiP integrity including: warpage improvement, solder joint reliability, die strength and stress, flip-chip bump fatigue, substrate trace cracking, temperature cycling, and more.

## System-level packaging technology

Similar to previous technology waves, the IoT will dramatically change people's lives in the 21st century and beyond. However, today's approach to system-level technology must change. Silicon design must take into account packaging capabilities, limitations and requirements from the beginning. When several ICs are mounted on a substrate, it is more important than ever that the interaction among the various signals and noise aspects are considered early in the design process.

To bring down system cost, achieve a more robust design and avoid some of the difficulties that others have encountered, packaging experts must be involved soon enough in

	Cavity Package	Hybrid Cavity Package
SOIC	A standard surface-mount package with a rectangular body and four pins at the bottom.	A hybrid cavity package with a larger, more complex body and multiple pins and leads extending from the top and sides.
QFN	A square package with a flat top and four pins at the bottom.	A hybrid cavity package for QFN, featuring a larger body with internal components visible through windows and multiple pins.
Laminate LGA/FPBGA	A package with a large, complex base and a smaller top component.	A hybrid cavity package for laminate LGA/FPBGA, showing a multi-layered structure with internal components.

**Figure 7:** Alternatives for adding IoT blocks to MEMS/sensor package.

the design integration process to address increasing packaging/system complexity in IoT-related applications and, in fact, most of the advanced systems that are expected to be developed in the future. Standardization for packaging and other aspects promises to play an important role in achieving design goals.

## Reference

1. <http://www.tsensorssummit.org/Resources/TSensors%20Roadmap%20v1.pdf>, Stanford U., Oct. 23-25, 2013.

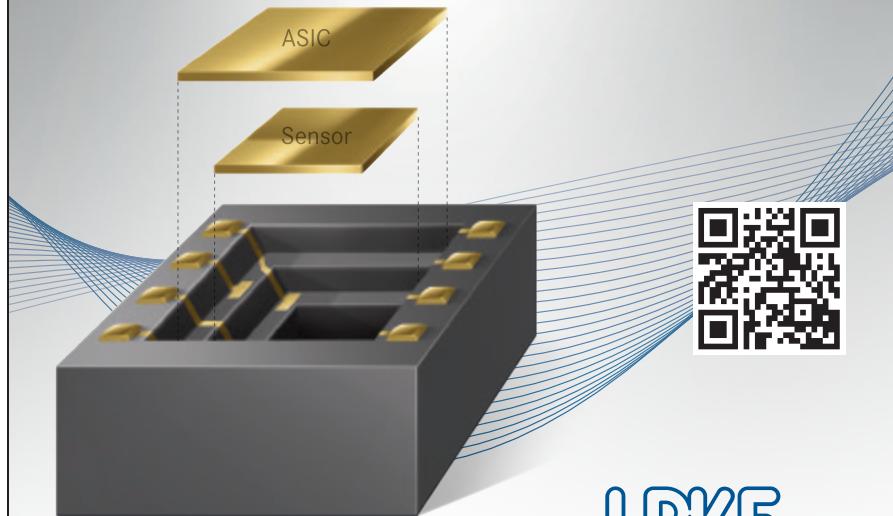
## Biographies

Vik Chaudhry received his MS and MBA degrees from Arizona State U. in Tempe and is Sr. Director, Product Marketing and Business Development, Advanced Products, at Amkor Technology; email: [Vikrant.Chaudhry@amkor.com](mailto:Vikrant.Chaudhry@amkor.com)

Adrian Arcedera received his degree in Chemical Engineering from the U. of the Philippines and is VP, MEMS/Sensors, Standard Products, at Amkor Technology.

## Easy Stacking for MEMS Packaging

New three-dimensional MEMS packaging with LPKF LDS technology simplifies the stacking of dies and eliminates manufacturing steps. Plated through-holes, no bumping process, three-dimensional circuitry, easy stacking. Find out more: [www.lpkf.com/mems](http://www.lpkf.com/mems)



LPKF Laser & Electronics AG  
Phone +49 (0) 5131-7095-0

**LPKF**  
Laser & Electronics

# Die-to-wafer stacking enables the future of 3D integration

By Teng Wang *[imec]*

**O**ne of the challenges in making 3D chip manufacturing an industrial reality is the development of a high-throughput process flow for narrow-pitch, high-accuracy stacking and bonding of dies. Today's most widely-used bonding process in the industry involves thermal compression bonding (TCB). However, the conventional approaches to TCB suffer from cycle times of more than one minute per die, making them unpractical for stacking on 300mm wafers. This article explains some key aspects to develop a fast and effective solution for accurate die-to-wafer stacking.

## Comparing stacking strategies with test vehicles

To compare the merits of the most promising assembly and stacking processes, and to work towards a fast, automated process, imec and its partners have recently experimented with a 300mm test design and implementation. The setup of the test vehicle allows for multi-layer stacking and subsequent electrical measurement of connections between all stacked layers.

The test chips are manufactured in imec's standard 65nm CMOS back-end-of-line (BEOL) process with  $5 \times 50\mu\text{m}$  via-middle TSV technology (through-silicon via). On the front side of the wafers, on top of the interconnect layers, Cu microbumps in  $20\mu\text{m}$  pitch are fabricated. The wafers with the top chips are thinned on a carrier wafer, revealing the TSVs. For Cu-to-Cu direct bonding, these TSV nails can be directly used to connect to the Cu bumps on the chip one level below. To test solder-based bonding, an additional bumping process must be applied to add CuNiSn microbumps to the TSVs. The wafers with the bottom chip of the stacks are processed without making TSVs but with the necessary BEOL layers to enable connecting and measuring the test structures on the stacks.

The  $50\mu\text{m}$  thick wafers with the top chips are then diced to be ready for die-to-wafer bonding. In die to wafer bonding, singulated dies are stacked onto bottom dies that are still part of a fully intact 300mm

wafer. Compared to wafer-to-wafer bonding, this allows testing for good top dies, and bonding top dies with another dimension than the bottom chips.

To assemble the chip layers, we chose thermal compression bonding. TCB is the most promising bonding method when it comes to bonding interconnects with an ultra-fine pitch. Another attractive advantage is that it allows stacking and flattening thinned chip that show some amount of warpage. And last – important for our R&D – TCB can be used with various joint metallurgies and underfill strategies.

## Joining the microbumps

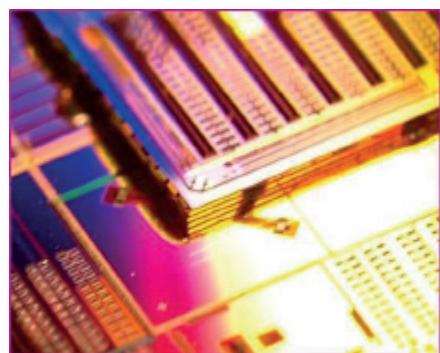
We experimented with different bonding metallurgies, solder-based methods and Cu-to-Cu direct bonding (**Figure 1**). For solder-based bonding, an additional bumping process was applied to our wafers for the top chips to form CuNiSn microbumps. When subsequently these bumps are joined with the Cu bumps on the lower chip, Cu-Sn intermetallic compounds are formed. We observed some underfill getting trapped into the soldered joints, but measurements proved that all joints were electrically connected. In addition, we are also exploring non-conventional bumping metallurgies, e.g., those based on Co, aiming at improving the reliability of such tiny bump joints.

A particularly interesting bonding metallurgy for 3D stacking is Cu-to-Cu direct bonding. Here, the revealed TSV nails on the back side of the top chips can

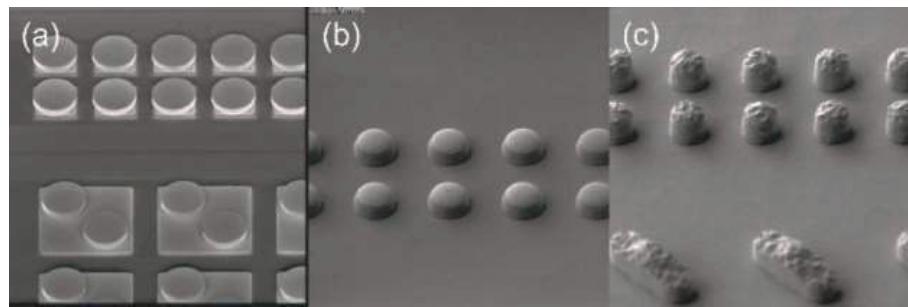
be directly used to connect to the Cu bumps on the chip one level below (**Figure 2**). The advantage is that the extra bumping step is eliminated, which greatly reduces the process complexity and cost. A constraint, however, is that direct bonding allows no backside redistribution. In addition, the post-bonding alignment accuracy should be tightly controlled (below  $3\mu\text{m}$  in our work).

## An efficient underfill

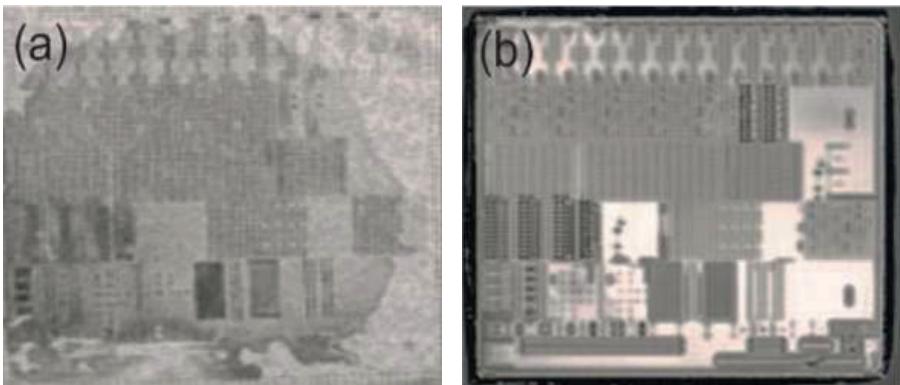
Another important benefit of using TCB for 3D chip stacking is its possibility to use a pre-applied underfill. That underfill is a polymer-based composite material that fills the gaps between the bonded dies. A pre-applied underfill is deposited on the top or bottom surface before bonding. It is the logical choice for the shrinking inter-chip



**Figure 1:** A 6-layer 3D stack, bonded by Cu-Cu direct bonding with pre-applied underfill. The continuity of TSV and microbump connections can be measured through all the layers.



**Figure 2:** Scanning electron microscopy (SEM) images of the structures for inter-chip in-terconnection: a) Cu microbumps on the front side; b) Revealed TSV nails on the back side; c) CuNiSn microbumps on the back side.



**Figure 3:** Scanning acoustic microscopy (SAM) images of N=2 stacks with irregular bump distribution. a) A stack bonded with NUF using a standard dispensing pattern. Nonuniform underfill flow and voids at the corners can be clearly observed. b) A stack bonded with WLUF showing void-free filling.

gaps going sub-10µm. These prove difficult to fill with conventional capillary underfill (CUF) or molded underfill (MUF).

We compared two types of pre-applied underfill materials, namely no-flow underfill (NUF) and wafer-level underfill (WLUF) (**Figure 3**). NUF, as a dispensable material, is always deposited onto the bottom chip or wafer, meaning that to stack N layers of chips, N-1 dispensing steps need to be inserted between the bonding steps. WLUF, in contrast, can be applied on the backside of the top wafer before dicing, by a lamination or spin-coating process. Therefore, the bonding cycles do not need to be interrupted with repeating dispensing steps. This important feature of WLUF makes it a favorable choice for building multi-layer 3D ICs. In addition, our test proved that WLUF has superior filling results that are independent of the layout of the microbumps and the inter-chip gaps. A potential issue with the underfill on the thin top die could be additional warpage. But our tests indicate that the slight additional warpage can easily be handled by the thermal compression bonder, which will effectively flatten the stacked thin chip.

### Collective bonding and faster tools

One major concern of using TCB for 3D assembly is its low throughput: upwards of one minute per die. To make TCB practical for multilayer stacking on 300mm wafers, we followed two paths. One was developing an innovative way of vertical collective bonding. And a second path was the collaboration with a tool supplier partner to deploy a considerable faster bonding process.

In our collective bonding sequence, every die to be stacked is first aligned and placed onto its bottom chip using a short TCB cycle with a low peak temperature. This only partly cures the WLUF—just enough to keep the stacked chips together. Afterwards,

when the topmost chip is added, a complete TCB profile with higher temperature over a long time period is applied. This completely cures all the bonds. For multi-die stacks, this collective bonding scheme offers significant process time savings compared to conventional sequential bonding with a full TCB cycle applied for every added die.

In collaboration with Besi, a supplier of die bonding tools, we've also developed a process solution using their newest tool at maximum efficiency.

Besi's Datacon 8800 TC tool uses two bond heads, enabling the bonding of dies in parallel. The tool also shortens the bonding cycles because of its extremely short heating (200°C/s) and cooling (100°C/s) ramps. The placement accuracy of the tool is rated at +/- 2µm @3sigma. And using the tool and other optimizations such as WLUF, we arrive at a bonding time of under 10 seconds, which is a considerable improvement.

### 3 D moving forward

More and more, stacking chips in 3D packages is seen as the way forward to building more powerful systems.

Furthermore, it's a way to compensate for the laws of physics that threaten to push chip makers off the path of Moore's Law, but also a way to combine heterogeneous designs into smart, tightly coupled packages.

As an emerging technology, however, 3D stacking still has many open options and technical details that have to be worked out and standardized. R&D efforts such as imec's 3D Integration Program are narrowing down the choices to what is most practicable, economic, and efficient in view of the applications that will most profit from 3D integration. With these experiments and test vehicles, imec and its partners have contributed to a path for a high-throughput flow for a highly accurate stacking and bonding of dies with dense, narrow-pitched inter-chip connections.

### Biography

Teng Wang received his BEng from Tongji U., China, MSc and PhD from Chalmers U. of Technology, Sweden, and is a Sr. R&D Engineer at imec; email [teng.wang@imec.be](mailto:teng.wang@imec.be)

# PLASMA ETCH

PROGRESS THROUGH INNOVATION

## INTRODUCING THE PE-25-JW

The Plasma Etch, Inc. PE-25-JW is a fully automated plasma cleaning system.

Surface energy modification with plasma treatment yields improved markability, adhesion and ease of assembly with a low environmental impact.

Removes organics and improves bonds.

LOW STARTING PRICE  
\$ 5,900 USD



TO LEARN MORE, VISIT [www.PLASMAETCH.COM](http://www.PLASMAETCH.COM)  
OR CALL US TODAY AT 775-883-1336

# Power module packaging: the “Promised Land”

By Coralie Le Bret *[Yole Développement]*

**A**t the beginning of 2015, after two years of stagnation, Yole Développement (Yole) reported growth in the power electronics market [1]. The power devices market reached \$11.5 billion in 2014, with 8.4% year-to-year growth [1]. Green technologies, energy management and government policies, especially in China, are driving this growth. Even within this favorable climate, the power module market, especially at the packaging level, stands out (**Figure 1**). Our analysts reported that the power module market reached \$2.6 billion in 2014, with 30% of that dedicated to the materials for packaging segment. By 2020, the power module market is expected to reach \$6.7 billion [2].

How can power module packaging improve to ensure the optimization of

the whole power electronics device? What are the technical challenges facing the industrial players? And what breakthroughs, such as wide band gap (WBG) technologies or embedded die packaging technologies, are needed by the industry? This article summarizes the growing power module market. The expansion of this sector is being driven largely by the increase in electric vehicle/hybrid electric vehicle (EV/HEV) and renewable energy market segments and the penetration of WBG technologies.

Two main packages are used to assemble devices for power electronics: discrete components and power modules. The packaging is selected depending on the final product and its application according to the following parameters: power, voltage, current and form factor. The technical evolution of power electronics devices is currently focusing on miniaturization, power density, efficiency and increased reliability.

Power modules - mostly developed for high power range applications - are a combination of active devices, such as insulated gate bipolar transistors (IGBT) devices, and diodes, all with different designs. Within this sector, more than 70% of the modules are based on a baseplate manufacturing technology. Direct bond copper (DBC) packaging is the most widely used.

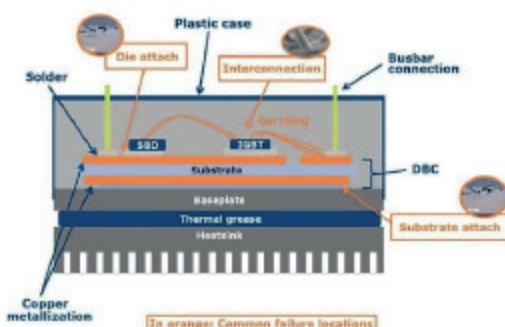
Today, power module devices clearly dominate the power electronics market in terms of value. In 2014, IGBT-based power modules represented 78% of the \$3.5 billion IGBT market, with the remaining 22% being discrete IGBT components (**Figure 2**) [3]. Component choice is dependent on the application and required power density. The manufacturing cost

is determined by the material selected. For example, if silicon is used, 50% of the unit price is determined by the component, 30% by other materials, and 20% by assembly costs and margins.

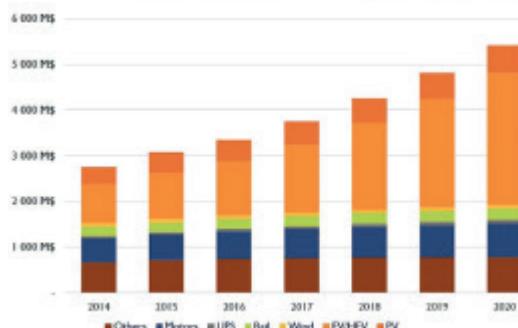
## EV/HEV and renewable energy: driving growth

According to Yole's estimates, the renewable energy market segment, including wind and photovoltaics applications, will roughly double between 2014 and 2020, reaching 16.2 million power module units. Pushed by the decentralization of energy production, the market for solar energy production systems will continue to grow. This will be especially noticeable in China where the players, supported by the Chinese government, are very active and gaining a better market position than European and North American companies [4]. The wind turbine market is developing differently. After a significant drop in 2013, that market should now be stable for several years. Our latest power electronics analysis, focusing on power electronics for renewable energy applications, predicts a 60GW market by 2024, with a small increase compared to 2015's wind capacity [5]. Meanwhile, inverters based on WBG power modules, mostly silicon carbide-based, could enter the wind market in the next couple of years.

Alongside these developments, the EV/HEV sector is expected to show the strongest growth during the period 2014-2020. It will expand from 7.1 million to 34.4 million units [6]. The automotive sector's development of EV/HEV is leading to new standards and opportunities. In our analysis, we have highlighted the rapid evolution of this market segment and the widespread demand for innovative technologies. Car design, inverter type, power module packaging and the use of WBG solutions are part of this growth. Higher power density and better thermal management



**Figure 1:** Standard power module packaging design. SOURCE: [6]



**Figure 2:** IGBT modules market forecasts to 2020 split by application, in value - in US\$ Million. SOURCE: [3]

are the two main drivers of this industry. We have also identified other applications such as grid, motors, uninterruptible power supply (UPS) and rail, which all play a part in the development of the power module market.

From a technology perspective, IGBT modules represent the main part of the power module market with 17.8 million units in 2014. WBG solutions, including gallium nitride (GaN) and SiC, were still a minor market segment in 2014 but according to our analysts, they could achieve a higher penetration rate in future. The forecast WBG compound annual growth rate (CAGR) between 2014 and 2020 reaches 22% for SiC. During the same period GaN's CAGR has been estimated at 95% by our analysts. In addition, we have highlighted emerging devices like high-speed silicon IGBTs and silicon-based super-junction metal-oxide-semiconductor field-effect transistors (SJMOSFETs) spreading through the power module marketplace.

### The “Promised Land:” the power module market segment

Today, most power electronics players, whatever their market positioning along the supply chain, want to expand their activities towards the power module market segment. This trend is creating very tough competition within the sector. Power electronics companies are looking for more business opportunities and executives would like to increase the value of their companies.

Against this background, we have identified several strategies in play. The approach differs from one continent to another as described below.

**Asia.** In Asia, most companies occupy every part of the supply chain. The main players are Mitsubishi Electric, Fuji Electric, Toyota, and BYD. Only one Europe-based player is involved all along the supply chain: ABB, which is developing power electronics devices and power modules, as well as inverters.

**North America.** In North America, companies such as International Rectifier, acquired by Infineon Technologies one year ago [7], Microsemi, and Fairchild Semiconductor focus on one area. For some of them it's discrete power devices, for others power modules. At the beginning of 2016, Yole is tracking the battle between Chinese investors

and ON Semiconductor for Fairchild Semiconductor's control. This acquisition could significantly change the power module market landscape.

**United States.** The US is also home to inverter makers such as Emerson and General Electric.

**Europe.** In Europe, the power electronics market is diversified, although inverter and pure device makers are present. This group includes Infineon Technologies,

Schneider, Siemens and Valeo. In addition, some European companies are strongly positioning themselves on device and power module activities or power module and inverter activities.

### Packaging as a key enabler

Packaging is a key step in the power module supply chain: in a power module, the costs of materials for packaging reached almost 30% of

**Ready... Set... Jet!**

**Nordson ASYMTEK's new 2-piece ReadiSet™ Jet Cartridge is quickly and easily removed, cleaned, inspected, and re-installed without tools, maximizing equipment utilization and up-time.**

**You can rely on our award-winning support network. Contact us now to find out more.**

<b>USA:</b>	info@nordsonasymtek.com Tel: 1.800.ASYMTEK or +1.760.431.1919
<b>China:</b>	info-china@nordsonasymtek.com Beijing: +8610.8453.6388 Guangzhou: +8620.8654.0092 Shanghai: +8621.3866.9166
<b>Europe:</b>	cs.europe@nordson.com +31.43.352.4466
<b>Japan:</b>	info-jp@nordsonasymtek.com +81.3.5762.2901
<b>Korea:</b>	info-kr@nordsonasymtek.com +82.31.765.8337
<b>India:</b>	info@nordsonasymtek.com +91.44.4353.9024
<b>Singapore:</b>	info@nordsonasymtek.com +65.6796.9515
<b>Taiwan:</b>	info@nordsonasymtek.com +886.229.02.1860

[nordsonasymtek.com/nexjet](http://nordsonasymtek.com/nexjet)

total power device costs in 2014 [8]. This share, including raw materials for packaging only, represented a \$787 million market.

Globally, in response to the growing threat coming from device and inverter makers, “pure” power module companies must develop their knowledge and increase their expertise. This is especially important at the packaging level, to enable development of higher added-value solutions and keep their leading market positioning. However this group includes only two main companies, Semikron and Danfoss. Such companies favor vertical integration to acquire new packaging competencies.

Within the power module supply chain, design and die manufacturing companies would also like to expand their activities into packaging. Rohm Semiconductor can be listed as an example. Initially involved in the development of SiC-based IGBT devices, today the company offers new power module solutions, including AC/DC converters, DC/DC converters, and LED drivers, and plans to expand these activities in the near future.

This movement all along the power electronics supply chain is very significant. Within the dynamic power module sector, we have highlighted the diversity of business models. In the future, most business models will be centered on power module activities with the specialties listed below.

**Materials.** Many companies are developing not only one, but several materials for power module packaging.

**Encapsulation and thermal interface materials.** Both of these parts of the power module are mostly developed by chemical companies. We highlight the solutions offered by ShinEtsu, Dow Corning, Wacker, and Momentive.

**Substrate and die attach.** These entities are also produced by chemical players. Specifically, our analysts name Heraeus and Dowa. These companies are part of a group of key power electronics leaders.

**Baseplate.** Companies involved in this sector have a distinct business model. Therefore, they are only implicated in baseplate development and are not active in other sections of the power module supply chain.

## WBG technologies: dream or reality?

A WBG component unit price is more expensive than traditional silicon technologies, reaching as much as 65% of the total module manufacturing cost according to 2014 estimates [9]. Even if WBG power devices represent a niche market today with fewer than 400,000 units in 2014, they have clear benefits for power electronics companies. For example, in a 50kW photovoltaic inverter, SiC technology allows a 40% reduction in weight.

Because of the increasing demand coming from rail, wind and photovoltaics sectors, power module manufacturers are increasingly looking for innovative solutions to package WBG-based devices. There are no standard packages for WBG technologies. These modules need specific packages adapted to high WBG voltage and frequency.

In parallel, the automotive sector has already announced new solutions using WBG technologies. This year, Toyota confirmed they are working towards high-volume production before 2020. One of the key power electronics leaders, Cree, has also announced a power device module last September. This product was developed by Cree’s Power and RF division, newly named Wolfspeed [10]. According to our latest analysis, WBG technologies represent a real opportunity to increase power device performance and answer the needs of the market.

## The bright future of power electronics modules

A standard power module is a complex assembly of materials and active devices. Its common failures mainly occur at the die attach and die interconnection levels. Packaging technology evolution is therefore focused on the development of innovative materials. Yole expects power modules to benefit from the invention of new materials by 2020 (Figure 3).

Analysts identified the following developments:

- Companies are developing new materials to improve die attach lifetime. They are especially considering new technologies for die attach using sintering processes. Their aim is to be able to handle operating at high temperature inside the module and so increase the reliability.
- Material suppliers are also working on new gels for filling that could be used with WBG technologies and ensure the temperature stability of the whole power module.
- At the substrate attach level, power module players are developing new solutions to remove layers and decrease power module dimensions.
- Within substrates, the challenge is mainly focused on the type of ceramics selected, especially for high-temperature operation, and their thickness to ensure the most appropriate electric insulation.

High-voltage applications are also a critical point for power module packaging technologies. Since the end of 2014, leading power module makers have released new solutions, with high-voltage applications for rail and grid. They include: Hitachi (1,700-6,500V), Infineon Technologies (3,300-6,500V), Mitsubishi Electric (3,300, 4,500 and 6,500V) and ABB (1,700-6,500V). Some companies are considering pure advanced packaging technologies such as wafer-level packaging (WLP) and embedded-die, especially for discrete components [11].

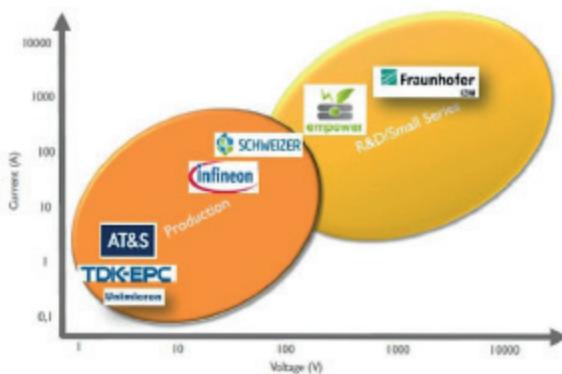


Figure 3: Technology roadmap for embedded die; power electronics roadmap. SOURCE: [11]

In the low-power range, companies are mostly considering discrete components. Such power devices are characterized by their small size. They are easy to integrate because of their small size and the maturity of the technology, but their thermal management is not optimized. Companies are investing a lot in new technologies, but innovative solutions are still under development today.

Schweizer Electronic has developed a silicon-based power module based on embedded-die technology, although it costs much more than standard packaging. GaN Systems also chose embedded-die packaging technology for its power modules. According to System Plus Consulting, a sister company of Yole, GaN Systems has released a 650V high-voltage GaN transistor embedded in an optimized thin package from AT&S [12]. The combination of GaN Systems' components and AT&S' embedded-die technology enables optimized heat management, package thickness, and high-power performance at high frequency. In parallel, EPC

Power has also developed a new 400-450V GaN-based solution. The company is using WLP technology to package its component.

The power module market, especially at the packaging level, is an attractive industry. The standard module is evolving daily with many companies working on the optimization of each part of the module. This results in the emergence of new manufacturing and packaging processes. Alongside these developments, discrete devices are still represented in the power electronics market. Their technologies are mature. However, companies are still waiting for innovation at the packaging level to ensure better performance and facilitate their integration. WBG technologies play a key role within this evolution as well. Indeed, they serve as a real opportunity for the power module players to answer the requirements of high-voltage applications. Companies are concerned, however, with specific packaging, which remains a non-negligible challenge.

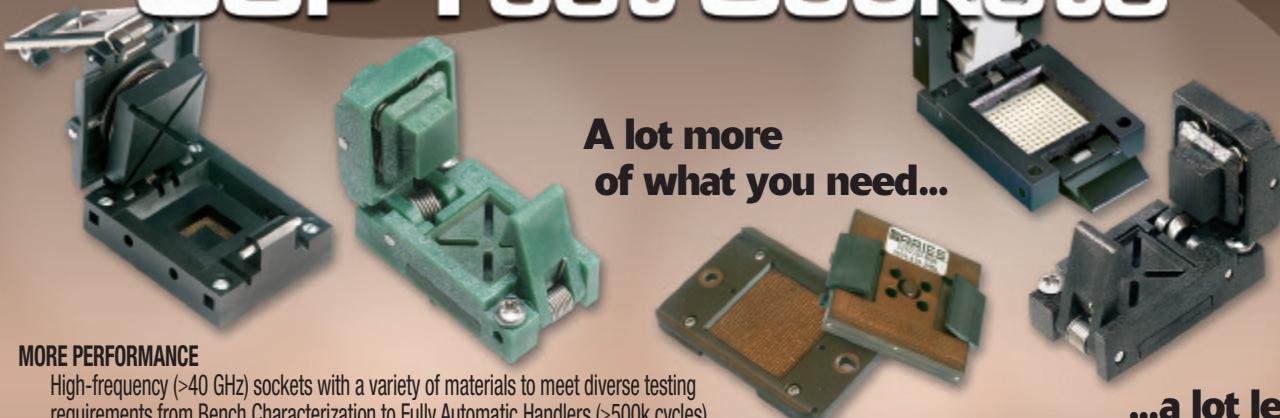
## Acknowledgments

This article was written in collaboration with Hong Lin, PhD, Mattin Grao Txapartegi, and Milan Rosina, PhD - all Technology & Market Analysts at Yole Développement, as well as Pierrick Gueguen, PhD, Business Unit Manager at Yole.

## References

1. "Status of the Power Electronics Industry report," [www.i-micronews.com/component/hikashop/product/status-of-power-electronics-industry-2015.html](http://www.i-micronews.com/component/hikashop/product/status-of-power-electronics-industry-2015.html); Yole Développement, Feb. 2015.
2. "Power Packaging Technology Trends and Market Expectations report," [www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html](http://www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html); Yole Développement, Mar. 2015.
3. "IGBT Market & Technology Trends report," [www.i-micronews.com/component/hikashop/](http://www.i-micronews.com/component/hikashop/)

# CSP Test Sockets



**A lot more of what you need...**

**MORE PERFORMANCE**  
High-frequency (>40 GHz) sockets with a variety of materials to meet diverse testing requirements from Bench Characterization to Fully Automatic Handlers (>500k cycles) delivering what you need.

**MORE CHOICES**  
Industry's widest available DUT interfaces – Spring Probes, Microstrip™ Contacts and two types of Conductive Elastomers.

**LESS COST**  
All DUT interface materials available in off-the-shelf molded plastic for a fraction of other's machined housing cost.

**LESS WAIT**  
Aries can deliver the exact sockets you need in four weeks or less! So why settle?

**...a lot less of what you don't!**

**ARIES® ELECTRONICS, INC.**  
Bristol, PA 19007-6810  
Tel 215-781-9956 • Fax 215-781-9845  
Email: [info@arieselec.com](mailto:info@arieselec.com)  
[www.AriesElec.com](http://www.AriesElec.com)

*The Evolution of Interconnect Innovation*

- product/igbt-market-and-technology-trends.html?Itemid=0; Yole Développement, Jul. 2015.
4. "Status of the Chinese Power Electronics Industry report," [www.i-micronews.com/component/hikashop/product/status-of-the-chinese-power-electronics-industry-2015.html](http://www.i-micronews.com/component/hikashop/product/status-of-the-chinese-power-electronics-industry-2015.html); Yole Développement, Nov. 2015.
  5. "Opportunities for Power Electronics in Renewable Electricity Generation report," <http://www.i-micronews.com/component/hikashop/product/opportunities-for-power-electronics-in-renewable-electricity-generation.html?Itemid=0>; Yole Développement, Jan. 2016.
  6. "Power Packaging Technology Trends and Market Expectations report," [www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0](http://www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0); Yole Développement, Mar. 2015.
  7. "Infineon Technologies AG successfully acquires International Rectifier" on [www.i-micronews.com/power-electronics/5018-infineon-technologies-ag-successfully-acquires-international-rectifier.html](http://www.i-micronews.com/power-electronics/5018-infineon-technologies-ag-successfully-acquires-international-rectifier.html)
  8. "Power Packaging Technology Trends and Market Expectations report," [www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0](http://www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0); Yole Développement, Mar. 2015.
  9. "CREE 1700V SiC module - first 1700V SiC MOSFET with Z-Rec SiC diode report," System Plus Consulting, [www.i-micronews.com/component/hikashop/product/cree-1700v-sic-mosfet-with-z-rec-sic-diode.html](http://www.i-micronews.com/component/hikashop/product/cree-1700v-sic-mosfet-with-z-rec-sic-diode.html), Yole Développement, Mar. 2015.
  10. "Cree Announces Wolfspeed – the New Name for the Power and RF Business" on [www.cree.com/News-and-Events/Cree-News/Press-Releases/2015/September/Cree-Power-and-RF-is-now-Wolfspeed](http://www.cree.com/News-and-Events/Cree-News/Press-Releases/2015/September/Cree-Power-and-RF-is-now-Wolfspeed)
  11. "Fan-out and embedded die technologies and market trends report;" [www.i-micronews.com/component/hikashop/product/fan-out-and-embedded-die-technologies-market-trends.html](http://www.i-micronews.com/component/hikashop/product/fan-out-and-embedded-die-technologies-market-trends.html); Yole Développement, Feb. 2015.
  12. "GaN systems 650V GaN on silicon HEMT AT&S ECP embedded power die package report," [www.i-micronews.com/component/hikashop/product/gan-systems-650v-gan-on-silicon-hemt-at-s-ecp-embedded-power-die-package.html](http://www.i-micronews.com/component/hikashop/product/gan-systems-650v-gan-on-silicon-hemt-at-s-ecp-embedded-power-die-package.html), System Plus Consulting, Jan. 2015

## Our Point Is... DL Technology Needles Work Precisely For Any Application.



DL Technology needles are designed and crafted to dispense material accurately, efficiently and to provide for better material release. Our needles are constructed in a variety of sizes, configurations, and patterns to meet your needs for any application.

**EZ-FLO** needles available in footed and non-footed surface mount, encapsulation, luer, and cone. Designed to provide precise, repeatable volumes. Stainless steel and ceramic needles available.

**Easy Release Luer-lok dispense needles** available in stainless steel and plastic. Used for applications such as epoxy, solder paste, solder mask and a variety of other materials.



**Custom Needles** can be designed according to unique requirements and specifications.

DL Technology has been the leader in micro dispensing technology for over 15 years. For more information, or for size or specifications on our line of needles, pumps or valves, visit [www.dltechnology.com](http://www.dltechnology.com).

### DL Technology

216 River Street, Haverhill, MA 01832  
P: 978.374.6451 | F: 978.372.4889  
[sales@dltechnology.com](mailto:sales@dltechnology.com)



report," [www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html](http://www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html); Yole Développement, Mar. 2015.

7. "Infineon Technologies AG successfully acquires International Rectifier" on [www.i-micronews.com/power-electronics/5018-infineon-technologies-ag-successfully-acquires-international-rectifier.html](http://www.i-micronews.com/power-electronics/5018-infineon-technologies-ag-successfully-acquires-international-rectifier.html)
8. "Power Packaging Technology Trends and Market Expectations report," [www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0](http://www.i-micronews.com/component/hikashop/product/power-packaging-technology-trends-and-market-expectations.html?Itemid=0); Yole Développement, Mar. 2015.
9. "CREE 1700V SiC module - first 1700V SiC MOSFET with Z-Rec SiC diode report," System Plus Consulting, [www.i-micronews.com/component/hikashop/product/cree-1700v-sic-mosfet-with-z-rec-sic-diode.html](http://www.i-micronews.com/component/hikashop/product/cree-1700v-sic-mosfet-with-z-rec-sic-diode.html), Yole Développement, Mar. 2015.
10. "Cree Announces Wolfspeed – the New Name for the Power and RF Business" on [www.cree.com/News-and-Events/Cree-News/Press-Releases/2015/September/Cree-Power-and-RF-is-now-Wolfspeed](http://www.cree.com/News-and-Events/Cree-News/Press-Releases/2015/September/Cree-Power-and-RF-is-now-Wolfspeed)
11. "Fan-out and embedded die technologies and market trends report;" [www.i-micronews.com/component/hikashop/product/fan-out-and-embedded-die-technologies-market-trends.html](http://www.i-micronews.com/component/hikashop/product/fan-out-and-embedded-die-technologies-market-trends.html); Yole Développement, Feb. 2015.
12. "GaN systems 650V GaN on silicon HEMT AT&S ECP embedded power die package report," [www.i-micronews.com/component/hikashop/product/gan-systems-650v-gan-on-silicon-hemt-at-s-ecp-embedded-power-die-package.html](http://www.i-micronews.com/component/hikashop/product/gan-systems-650v-gan-on-silicon-hemt-at-s-ecp-embedded-power-die-package.html), System Plus Consulting, Jan. 2015

### Biography

Coralie Le Bret received her Engineering degree in Material Sciences at INSA Lyon, France, and is a Technology & Market Analyst at Yole Développement; email [lebret@yole.fr](mailto:lebret@yole.fr).

# Fine-pitch stacking on a carrier wafer

By Chen Hong Ciou, Hsiao Chun Huang, Hsien Wen Chen, Stephen Chen, Mike Ma [Siliconware Precision Industries Co., Ltd. (SPIL)]

## I

In recent years, there is growing interest in applying glass as an interposer for fine-pitch 2.5D/3D substrates as shown in **Figure 1**. Silicon interposers were the first substrates used for 2.5D integration of logic and memory ICs [1-2]. However, the high cost and electrical loss of wafer back-end-of-line (BEOL) silicon interposers has fueled the need for glass interposers. The advantages of using a glass substrate include material properties such as the ability to adjust the coefficient of thermal expansion (CTE) to improve reliability, electrical performance, as well as the cost effectiveness that glass-based solutions provide over other approaches [3]. Furthermore, the fine-pitch re-distribution layer (RDL) also plays an important role for the next-generation of semiconductor packages; resolution requirements are not only in the sub-micron range, but the single-digit micron range, and the L/S requirement of  $2\mu\text{m}$  is a logical choice for fine-pitch RDL applications. The optical characteristics of suitable lithography systems should offer a numerical aperture (NA) of about 0.16 in order to meet the line/space (L/S) resolution requirement while also preserving a reasonable depth of focus (DoF). In addition to lithography systems, photoresist (PR) and surface roughness also contribute significantly to the DoF [3].

This paper focuses on material selection and warpage. Polymeric dielectrics represent a wide range of material classes that can be used for wafer-level packaging (WLP), such as epoxy, polyimide, silicone, polybenzoxazole, fluorinated polymer and polynorbornene. Warpage is one of the major concerns for WLP. No component can expand or shrink freely on account of differences in chemical shrinkage and the coefficient of thermal expansion (CTE) of the components. The result is warpage that combines with the differences in dimensional change. In a typical array package, warpage is seen in either a concave or a convex shape. In this study, we tested many thin-film polymers and tried to determine a direction for the warpage and planarization of the passivation (PSV) layer.

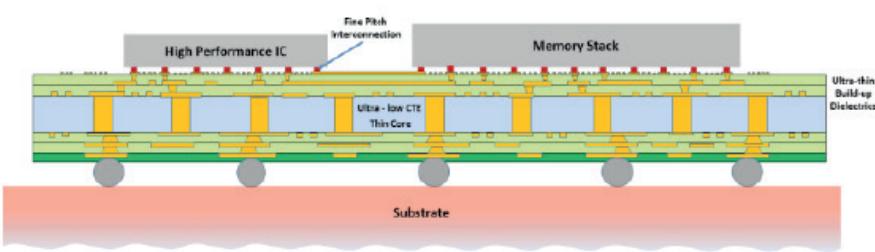


Figure 1: Example of a fine-pitch 2.5D package [4].

	Item	Unit	Polymer A	Polymer B	Polymer C	Polymer D
Mechanical property	Cure conditions	T <sub>c</sub>	200	230	200	230
	Film thickness	$\mu\text{m}$	3~10	7~24	4~15	7.5~14.5
	Shrinkage	%	S+20	S+30	S	S+10
	Young's Modulus	GPa	Y	Y+1.5	Y+0.4	Y+2.8
	CTE	$\text{ppm}/\text{K}$	C+28	C+18	C+12	C

Table 1: Characteristics of polymers.

## Experimental

For every material characterization shown in **Table 1**, such as Young's modulus, the coefficient of thermal expansion (CTE), and chemical properties like shrinkage during the cure process can help to predict a polymer's behavior under mechanical stresses such as CTE mismatch and shrinkage of the layer in a multi-layer stack.

The steps for creating the PSV layer include: 1) PR coating, 2. Exposure, 3. Development, 4. Post-development bake (Polymer B), 5. Hard bake, and 6. Plasma treatment (Polymer B). In the RDL process, liquid photoresist is coated on the dielectric layer and patterned with a lithography tool. Exposure is performed on a stepper with a 0.16 NA lens. The system used in this study has the capability to select i-line, g-line, and ghi-line wavelengths. The tool functions include a wafer edge exposure (WEE) unit for exposing the wafer edge, and a wafer edge protection (WEP) unit for protecting the outer edge of the wafer. The WEE function

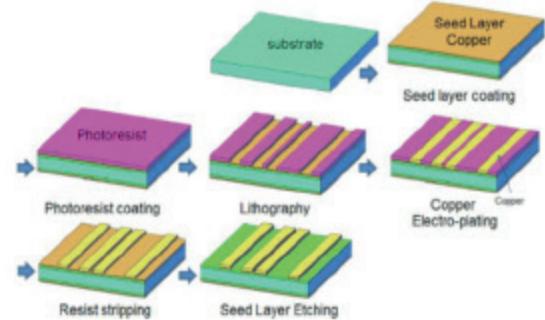


Figure 2: Process flow of an RDL on polymer [5].

can remove PR from the outer edge and create a contact ring for electroplating. The WEP can be used to leave PR on a thin ring inside the WEE creating a protective seal ring to prevent leakage of solution during the electroplating step [6].

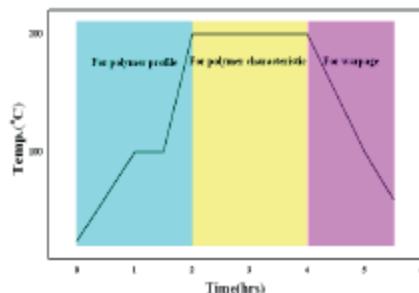
After exposure, copper lines are metallized by sputtering a Ti-Cu seed layer and electrolytic copper plating until the copper height reaches the required amount. The last steps are removal of the photoresist and wet chemical etching of the seed layer; the process flow is shown in **Figure 2**. RDL can perform on various substrates; in this study, the RDL process

was formed on a glass substrate. **Table 2** shows glass characteristics.

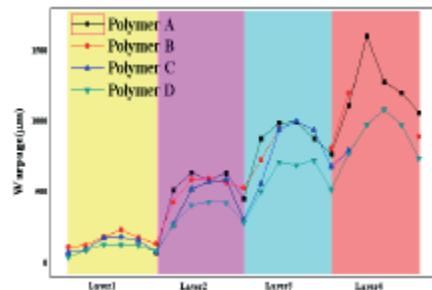
Hard cure is necessary to achieve the necessary polymer properties. The curing temperature is changed for different polymers using a cyclone oven in a N<sub>2</sub> atmosphere. **Figure 3** shows the standard polymer's cure temperature.

	Item	Unit	Glass A	Polymer A	Polymer B	Polymer C	Polymer D
Mechanical property	Cure conditions	°C		200	230	200	230
	Film thickness	μm		3~10	7~24	4~15	7.5~14.5
	Shrinkage	%		S+20	S+30	S	S+10
	Young's Modulus	GPa		Y+66.94	Y	Y+1.5	Y+0.4
	CTE	ppm/K		C	C+74.33	C+64.33	C+58.33

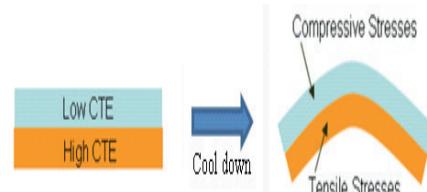
**Table 2:** Glass characteristics.



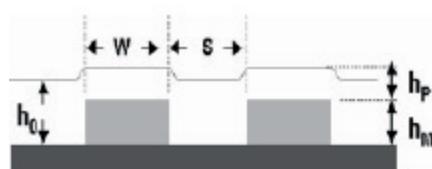
**Figure 3:** Standard polymer cure temperature profile.



**Figure 4:** Warpage profile.



**Figure 5:** Schematic of deformation.



**Figure 6:** Model and parameters comprising DoP.

## Result and discussion

**Warpage behavior.** Structure warpage was measured stage by stage and the focus was on the passivation (PSV) as shown in **Figure 4**. In the results, Polymer D has a smaller warpage than the others. Stress between layers is not only a result of the CTE mismatch, but also due to shrinkage of the layers [7]; the Young's modulus of the polymer is also a key factor. Warpage considerations are: 1) CTE mismatch of the layers; 2) Young's modulus for the material; and 3) Shrinkage of the polymer.

High shrinkage means more photosensitizer had evaporated, which led to a large stress produced during the curing process. After considering the combined effects on the structure, it was determined that the CTE mismatch of layers is the most influential factor; the CTE of the polymer accounts for the most warpage in the fine-pitch stacking structure. **Figure 5** shows the warpage behavior when there are two or more layers in the heterojunction structure. Deformation caused by stress tends to be in the direction of the high CTE surface.

**Planarization.** Planarization of the top of the stacking is important for fine-pitch structures. Additionally, a formula could calculate the degree of planarization. The parameters and model are described in **Figure 6** [5] and as follows:

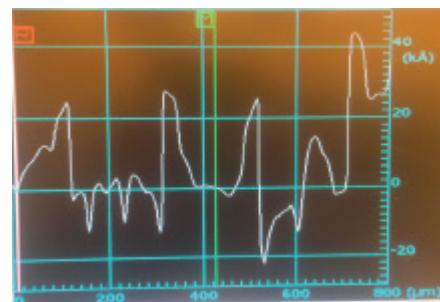
$$\begin{aligned} h_0 &: \text{PSV height on substrate} \\ h_p &: \text{PSV height on metal} \\ h_m &: \text{Metal height} \end{aligned}$$

Step height was measured (i.e., depth of cavity) after plating and the difference is about 8 μm. For copper wiring with a large pitch such as, 10 μm, the DoF of the exposure process is sufficient for an 8 μm cavity, but if the line/space is 2 μm, the DoF is smaller than L/S 10 μm. First, polymer C and polymer D were used to test the planarization; the result is shown in **Table 3**.

From **Table 3**, it can be seen that polymer D is better than polymer C for planarization. We believe that the key for planarization could be two conditions, one is viscosity,

Characteristic of polymer		
	Polymer C	Polymer D
Viscosity (cp)	250	4000
Shrinkage (%)	20	30
Depth between Cu wire (μm)		
Before coating, $h_m$	8.5	8.3
After coating, $(h_p + h_m) - h_s$	5.8	4.2

**Table 3:** Depth between  $h_m$ .



**Figure 7:** Step height resulting from the gap on the top of the stack.

and the other is shrinkage [8]. High viscosity means that there is more photoresist in the cavity during photoresist coating. On the other hand, for the case of a low viscosity photoresist, there is less photoresist in the cavity. Second, a high shrinkage means the thicker photoresist will lose more of its volume during the curing process, which will lead to poor planarization.

Polymer D was used for multi-layer stacking, and this structure is measured by its step height. **Figure 7** shows the gap is about 6 μm, so the DoF of exposure must be larger than the gap to avoid breakage of the copper wiring.

## Summary

In summary, this paper presents a direction for accomplishing fine-pitch on multi-layer stacks. Warpage and planarization are important for DoF of the exposure. With respect to warpage of the structure, we expect that a model can help us understand warpage of the polymer without testing. For planarization on top of stacking, liquid photoresist has some weak points like shrinkage and the type of photoresist, which we need to overcome. So far, dry film seems a solution for planarization. Fine pitch is expected to enable the use of high-density 2.5D interposers for cost-sensitive, smart mobile, and emerging wearable electronics applications.

## References

1. P. Sun, V. C.-K. Leung, B. Xie, V. W. Ma, D. X.-Q. Shi, "Warpage reduction of package-on-package (PoP) module by material selection and process optimization," Proc. Electr. Comp. and Tech. Conf. (ECTC), Shanghai, 2008, pp. 1-6.
2. M. Topper, T. Fischer, T. Baumgartner, H. Reichl, "A comparison of thin-film polymers for wafer-level packaging," Proc. Electr. Comp. and Tech. Conf. (ECTC), Las Vegas, NV, 2010, pp. 769-776.
3. S. R. McCann, V. Sundaram, R. R. Tummala, S. K. Sitaraman, "Flip-chip on glass (FCOG) package for low warpage," Elec. Comp. and Tech. Conf. (ECTC), 2014 IEEE 64th, 2014, pp. 2189-2193.
4. M. Ishihara, et al., "A dual face package using a post with wire component: novel structure for PoP, wafer-level CSP and compact image sensor packages," Proc. 58th Elec. Comp. and Tech. Conf., 2008, pp. 1093-1098.
5. K. Zoschke, J. Wolf, O. Ehrmann, M. Töpper, H. Reichl, "Copper/benzocyclobutene multi-layer wiring – a flexible base technology for wafer-level integration of passive components," Proc. 9th Elec. Packaging Tech. Conf. (EPTC), 2007.
6. N. Shimizu, "Development of organic multi-chip package for high-performance application," Inter. Microelec. Assy and Packaging. Soc. (IMAPS), Orlando, FL, Sep. 30-Oct. 3, 2013.
7. Y. Suzuki, R. Furuya, V. Sundaram, R. R. Tummala, "Demonstration of 10µm micro vias in thin dry-film polymer dielectrics for high-density interposers," IEEE Trans. Comp. Packaging Tech., 2015, 194-200.
8. K. Oi, S. Otake, N. Shimizu, S. Watanabe, Y. Kunimoto, T. Kurihara, et al., "Development of a new 2.5D package with novel integrated organic interposer substrate with ultra-fine wiring and high-density bumps," Elec. Comp. and Tech. Conf. (ECTC), 2014 IEEE 64th, 2014, pp. 348-353.

## Biographies

Chen Hong Ciou received a Masters degree from the National Taiwan U. of

Science and Technology, NTUST, and is an Engineer at Siliconware Precision Industries Co., Ltd. (SPIL); email mikeqiu@spil.com.tw

HSiao Chun Huang received a Masters degree from the National Yunlin U. of Science and Technology, NYUST, and is a Senior Engineer at Siliconware Precision Industries Co., Ltd. (SPIL).

Hsieh Wen Chen received a Masters degree from Chung Yuan Christian U.,

CYCU, and is a Department Manager at Siliconware Precision Industries Co., Ltd. (SPIL).

Stephen Chen received his Master's degree from Chung Yuan Christian U. (CYCU) and is a Director at Siliconware Precision Industries Co., Ltd. (SPIL).

Mike Ma received his PhD from North Carolina State U. (NCSU) and is a VP at Siliconware Precision Industries Co., Ltd. (SPIL).

# GHz Bandwidth Sockets for BGA & QFN

## Industry's Smallest Footprint

- Pitch - 0.3mm to 1.27mm - BGA, QFN (MLF)
- Bandwidth to 40+ GHz
- Six different lid options
- Optional 500,000 insertions
- Heatsinking to 100 watts



**Ironwood**  
ELECTRONICS  
[www.ironwoodelectronics.com](http://www.ironwoodelectronics.com)

1-800-404-0204

# Avoiding low-cycle fatigue in solder materials using inhomogeneous column grid array (CGA) design

By Ephraim Suhir [Portland State University]

**N**umerous semi-empirical inverse power law relationships of the Coffin-Manson type have been suggested during the last decades to predict the fatigue lifetime of solder materials in IC devices. The predictions are based on an assumption that these materials are always stressed above their yield point and, hence, experience low-cycle fatigue condition during accelerated testing and actual operation. But could this condition be avoided by a proper design of the solder system? If this is possible, the elastic fatigue conditions will take place, and even if the induced stresses are above the fatigue limit (but still below the material's yield stress), the solder material's lifetime will increase dramatically, and the Palmgren-Miner rule of linear accumulation of elastic fatigue damages could be used instead of the Coffin-Manson models to predict it.

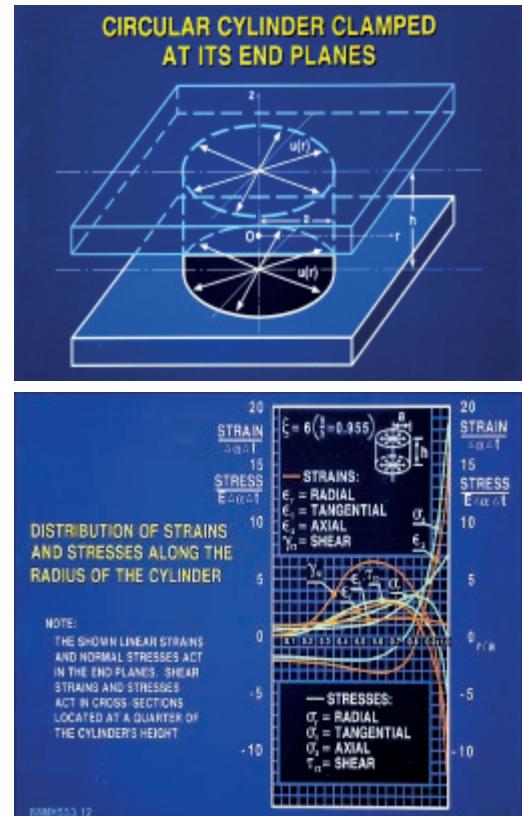
In the outline that follows, some recent findings associated with the use of inhomogeneous ball grid array (BGA) and column grid array (CGA) technologies for lower thermally-induced stresses in the solder material are addressed. In many cases, if the yield stress is high enough (e.g., in lead-free solders) and the predicted stress relief is significant, no inelastic strains could be expected. The findings are based mostly on the application of the analytical stress modeling using structural analysis and theory of elasticity methods.

## Inhomogeneous BGA and CGA technologies

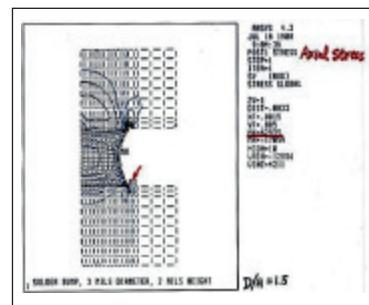
The first attempt to model solder joint interconnections as short cylinders was undertaken back in 1989 [1] in connection with the Bell Labs Si-on-Si technology and addressed local thermally-induced stresses caused by the coefficient of thermal expansion

(CTE) mismatch between the Si and the solder (**Figure 1**). The analytical solution obtained using modified Bessel functions was in good agreement with finite element analysis (FEA) computations (**Figure 2**, left) and was used to select the appropriate (low stress) aspect ratio of the solder joints (**Figure 2**, right). Joints configured as short cylinders provide elevated interfacial compliance, act as effective strain buffers and, owing to that, are able to relieve the interfacial stresses [2, 3].

BGA soldering technology (**Figure 3a**) is currently widely used as an effective second-level (package to PCB) interconnection technique. It enables one to permanently surface mount electronic components on a printed circuit board (PCB) with high mounting density (high pin count). In addition, this technology leads to a short signal delay. The reliability of BGA interconnections is, however, the bottleneck of BGA designs. This is due primarily to the lack of compliance of the BGA solder balls. They do not flex the way the longer leads of the previous generations of the second-level



**Figure 1:** Solder joint modeled as a short circular cylinder ("column") clamped at its end planes and experiencing axisymmetric elastic deformations caused by local mismatch [1]. The highest ("peeling") stresses and strains act in the axial direction although the "external" local mismatch strains  $\Delta\alpha\Delta\tau$  are in-plane ones.



**Figure 2:** Solder joint modeled as a short circular cylinder ("column") clamped at its end planes and experiencing axisymmetric elastic deformations caused by local mismatch [1]. The FEA data show the meniscus in the cylindrical solder joint at low temperature conditions (the CTE of the solder material is substantially higher than the CTE of the Si chip and the Si substrate).

interconnections were and are unable therefore to effectively relieve stresses in the joints. Higher mechanical flexibility of the interconnections can be achieved by employing joints configured as short cylinders with large (compared to conventional joints) stand-off heights, such as, e.g., CGA (**Figure 3b**).

Ceramic CGA were addressed by Banks and Gerke [4], Master, Cole, Martin and Caron [5] and Sinha, Isaacs and Tofil [6] about twenty years ago. It has been experimentally demonstrated that the application of the CGA technology could lead to a substantially longer lifetime of the joints. Recently, Fleisher and Willing [7] provided a study for space systems, in which high reliability is particularly important.

A short beam with clamped and offset ends was considered [8] as a possible improvement of the BGA design. The developed model is a modification of the classical Timoshenko short-beam theory. While this theory, typically applied to a cantilever beam, seeks the beam's deflections caused by the combined bending and shear deformations for the given loading, an inverse problem, having in mind electronic packaging application, was addressed here: the lateral force was sought for the given ends offset of a beam clamped at its ends. In short beams this force is larger than in long beams, because the sought force has to overcome both bending and shear resistance of the beam in order to achieve the given ends offset. It has been pointed out that short beams could adequately mimic the state of stress in solder joint interconnections with large—compared to conventional BGA joints—stand-offs. It has been indicated that by employing beam-like solder joints, one can even manage to avoid inelastic deformations in them, thereby dramatically increasing their fatigue lifetime. It has been determined that the maximum shearing stress is inversely proportional to the square root of the stand-off height of the joint in the extreme case of disk-like (very small stand-off height) joints and is inversely proportional to the cube of the stand-off height in the opposite extreme case of a beam-like (significant stand-off height) joint (see **Figure 2**). The peeling stress at the joint ends has

been found to be inversely proportional to the stand-off height of the joint in the case of a disk-like joint and is next to zero in the case of a beam-like joint.

While employing beam-like solder joints of the CGA type is an effective means to increase the interfacial compliance of the bonding system and, owing to that, to reduce the interfacial stresses in the bonding material, employment of inhomogeneous

bonds is another powerful and flexible means for relieving the interfacial stresses. Inhomogeneous bonds are characterized by different physical properties (Young's modulus, CTE, the application/fabrication temperature) at different segments of the bond. Inhomogeneous piece-wise continuous bonds were considered in connection with and in application to holographic memory devices [9,10], and applied



**PacTech**

member of nagase group

# Your Partner for Advanced Packaging

## Our Services

### Wafer Bumping

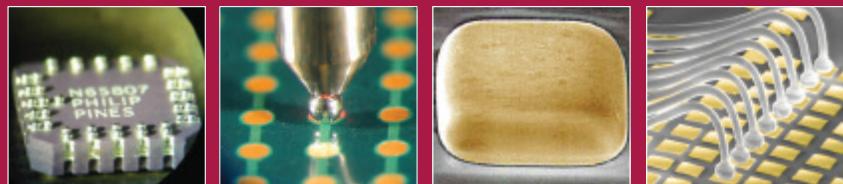
- UBM & OPM Plating, e.g.  
  eless NiAu & NiPdAu,  
  e-plate Cu & Au
- NiFe Plating for MEMS
- Solder Ball Attach /  
  Solder Jetting
- Wafer Level RDL (Low  
  Volume)
- CSP & BGA Ball Rework

### Wafer Backside Metallization

- Wafer Thinning
- Single Wafer Etch
- TiNiAg & TiNiAu Evaporation

### Backend & Die Sort

- Laser Marking, Sawing,
- Electrical Test
- Tape & Reel
- FC-Assembly

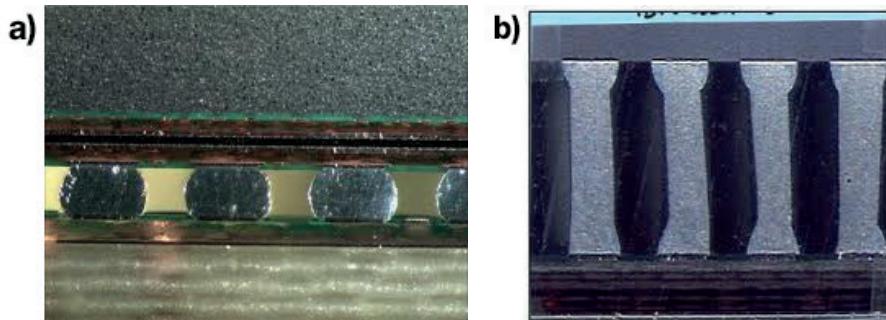


ISO 9001  
ISOTS 16949



[www.pactech.de](http://www.pactech.de)

[sales@pactech.de](mailto:sales@pactech.de)



**Figure 3:** Ball grid array (a) and column grid array (b) solder joint interconnections.

later on as an effective stress relieving technology in electronics and photonics packages (e.g., [11]).

Because the interfacial stresses in assemblies comprised of dissimilar materials concentrate at the assembly ends, the application of low-modulus bonding material at the peripheral portions of the assembly can result in a significant stress relief, so that even bonding materials with a low-yield stress might not experience inelastic strains. It is advisable that the length of the possible inelastic region at the end of a soldered assembly with a

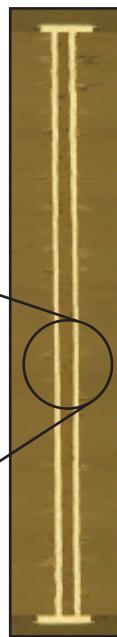
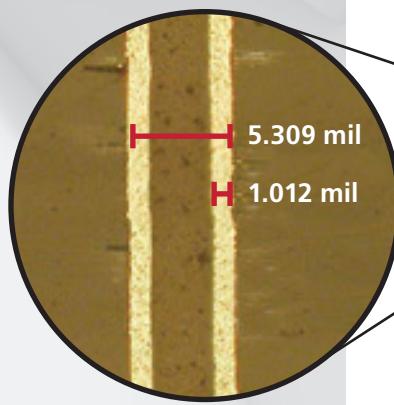
low-yield stress is evaluated first [12]. It is the ratio of this length to the half of the assembly length that can be used as a suitable figure of merit of a particular low-yield-stress bonding material. In the analysis [12] this material was considered linearly elastic at the strain level below the yield point and ideally plastic at the higher strains. Clearly, the stress-strain diagram for actual elasto-plastic solders will be restricted by the two extreme easy to model cases: the ideally elastic/ideally plastic case considered in this analysis and the linearly elastic case addressed earlier (e.g., [3]).

The BGA and CGA interconnections are obviously inhomogeneous, but are not piece-wise continuous either: because of the gaps between the joints, they could be rather identified as bonds comprised of an array of separate (independent) supports. Intuitively it is felt that if the distances between these supports are small, a relatively simple predictive stress model developed for continuous bonding layers (e.g., [13]), whether homogeneous or inhomogeneous, can still be used for the evaluation of the stresses and strains in BGA and CGA systems. But how “small” is small? A rather general analytical stress model that enables one to evaluate the thermally-induced stresses in bonded assemblies with gaps between the supports (joints) has been developed in [14] to answer this question. It has been concluded that the model developed for a continuous bond can be used for the BGA and CGA systems as well, if the ratio  $s = \frac{p}{2l}$  of the pitch  $p$  (the distance between the joint centers) to the joint widths  $2l$  is below 5, and the product  $kl$  of the parameter  $k$  of the interfacial shearing stress (this parameter can be computed as a square

# CONQUER COMPLEXITY

## High Aspect Ratio Load Board Drilling & Plating

- 0.4mm pitch
- 4.75mm thick
- 37:1 Aspect Ratio
- 1 mil plating



**CONTACT US |** [cse@rdaltanova.com](mailto:cse@rdaltanova.com)

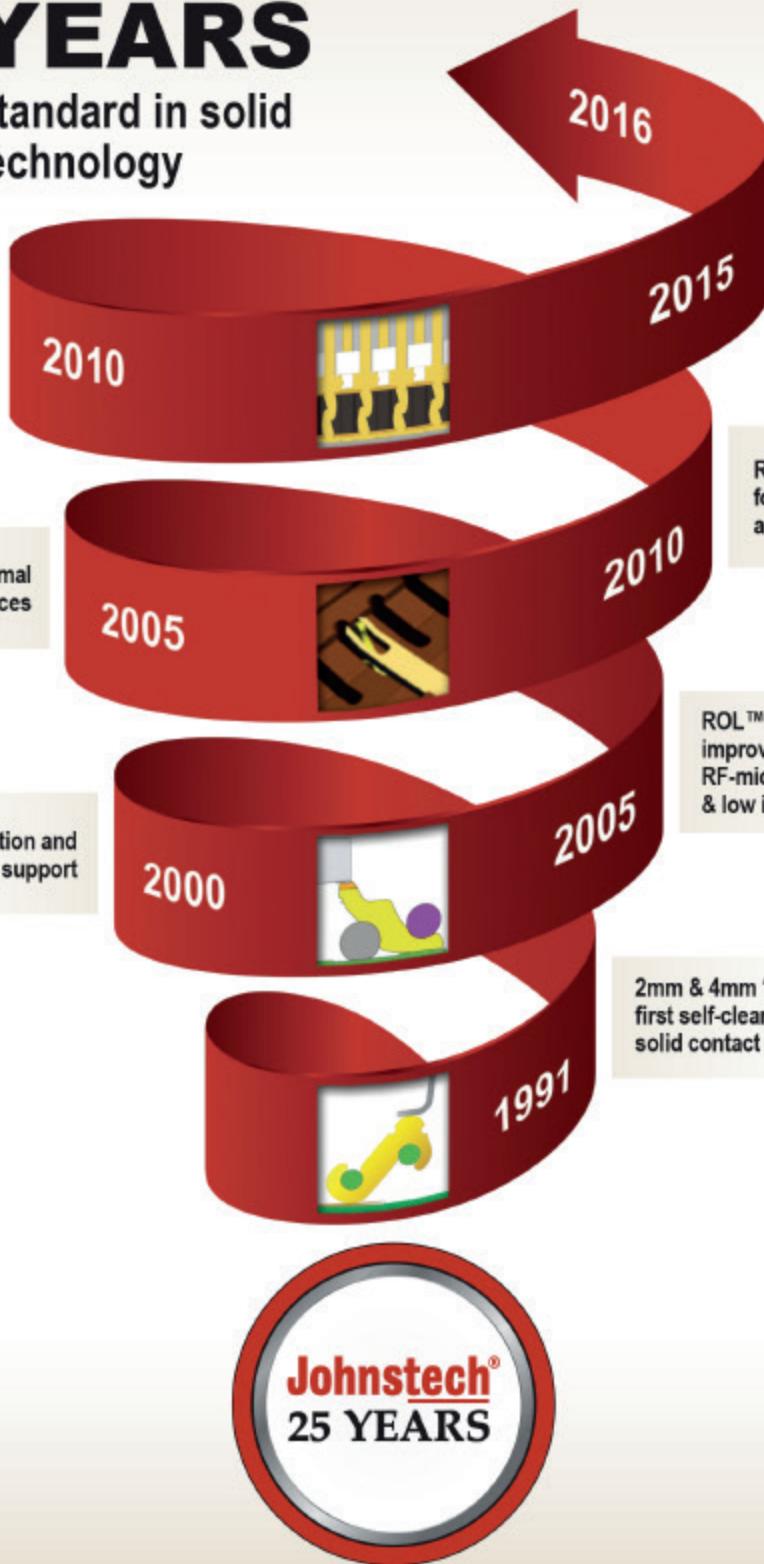
R&D Altanova 3601 So. Clinton Ave. South Plainfield, NJ 07080  
[rdaltanova.com](http://rdaltanova.com)

**R&D**   
**Altanova**®

# A BENCHMARK OF THE INDUSTRY FOR 25 YEARS

Still the standard in solid contact technology

Verticon® 100 BGA and  
ROL 100A Performance Plus  
20-80 GHz,  
(including mm-wave)



IQtouch™ Micro  
WLCSP probe arrays

root of the ratio of the axial compliance of the assembly to its interfacial shearing compliance) and half the assembly length  $l$  in the equivalent homogeneously bonded assembly is above 2.5. This is indeed the case in actual BGA and CGA systems. FEA carried out for a BGA assembly [15] has confirmed this conclusion: the FEA data obtained for the actual BGA assembly turned out to be the same as the data obtained for an assembly with no gaps between the joints. The BGA material was considered in this analysis, as it has been in [12], linearly elastic at the strains level below the yield point in shear, and ideally plastic above the yield strain. The numerical example carried out for a 30mm long surface-mount package and a 200 $\mu\text{m}$  thick lead-free solder indicated that, in the case of a high expansion PCB substrate, about 7.5% of the interface's length experienced inelastic strains, while no inelastic strains occurred in the case of a low-expansion ceramic substrate. The latter result indicates particularly that the use of a low-expansion substrate can lead to inelastic strain-free conditions in the solder material, i.e., to avoid its low cycle fatigue performance. Application of BGA joints with elevated stand-offs are advisable in this case, and the need for a significant "leap" to a CGA design might not be even necessary.

Thus, there are two effective means to reduce the thermally-induced interfacial stresses in bonded assemblies: application of the joints with elevated stand-offs (not even necessarily of the CGA type) and the use of inhomogeneous bonds, in which the peripheral portions of the assembly have different physical properties than the major mid-portion of the assembly. There is an obvious incentive for combining these two means in the same design. Accordingly, a BGA or a CGA with a low modulus solder or an epoxy material at the peripheral portions of the assembly was addressed [14-19]. The following sequence of actions has been undertaken when developing the analytical predictive models discussed below.

**First step.** The mid-portion of the assembly subjected to the given temperature change and to thus far unknown thermomechanical forces acting in a symmetric fashion at the boundaries between the mid-portion and the peripheral portions was considered, and the expression for the interfacial displacements at this boundary was obtained.

**Second step.** The peripheral portion of the assembly subjected to the given

temperature change (not necessarily the same as that for the mid-portion: the peripheral material could be applied at a lower temperature than the bonding material at the mid-portion) and to thus far unknown, but the same thermomechanical forces as those applied to the mid-portion. These forces act, however, in an asymmetric fashion, because the outer ends of the peripheral portions are stress-free.

**Third step.** The condition of the compatibility of the interfacial displacements of the mid-portion and the peripheral portion at their boundary was used to evaluate the thermomechanical forces at this boundary.

**Fourth step.** The expressions for the distributed forces acting in the cross sections of the mid-portion and the peripheral portions of the assembly were obtained, using the expression for the force at their boundary.

**Fifth step.** The interfacial shearing stresses were evaluated by differentiating the expressions for the distributed forces. As a result of using this technique, the obtained distribution of the interfacial shearing stresses along the assembly was such that the stress in its mid-portion increases from zero at the mid cross section of the assembly to a certain high value at its boundary with the peripheral portions. Then, the stress drops to a low value at the inner ends of the peripheral portions, i.e., at their boundary with the mid-portion, and then increases again at the outer end of the assembly. The maxima of these stresses at the outer ends of the mid-portion and the peripheral portions can be made rather low by the appropriate use of bonding materials properties, the application temperature of the peripheral portions, and the lengths of the peripheral portions, significantly lower than the stress at the ends of a homogeneously bonded assembly. The references [16-19] contain numerical examples of how the stress computations should be carried out.

## Summary

The induced stresses in solder joints can be brought down considerably by employing beam-like (CGA) joints. It is imperative, of course, that if such joints are employed for lower stresses, the joint ends should be reliably anchored, and that there is still enough interfacial real estate so that the joints' bonding strength is not compromised. On the other hand, owing to a lower stress level in solder systems with elevated stand-off heights, assurance of their strength is less of a challenge than in the case of

conventional BGA joints. By employing beam-like solder joints one might even be able to avoid inelastic deformations in them, thereby dramatically increasing the lifetime of the material. The numerical example carried out for a CGA assembly with a low modulus and low fabrication temperature bonding material at the assembly ends has indicated that stress relief as high as 34.3% can be achieved compared to the assembly with a homogeneous bond. The stand-off of a beam-like joint characterized by the inelastic strain-free state-of-stress should be significant enough to make the shearing stress low compared to the bending stress. This will take place for height-to-diameter ratios of about 12-13. The further increase in the stand-off height, even if it is technologically achievable, is not advisable, because it will lead to undesirable elevated bending stresses. Future work should include, but might not be limited to, the FEA computations and experimental evaluations (e.g., shear-off testing and/or temperature cycling) of the induced stresses in, and the fatigue lifetime of, typical BGA and CGA assemblies.

## References

1. E. Suhir, "Axisymmetric elastic deformations of a finite circular cylinder with application to low-temperature strains and stresses in solder joints," ASME Jour. of Appl. Mech., vol. 56, No. 2, 1989.
2. E. Suhir, "Calculated thermally-induced stresses in adhesively bonded and soldered assemblies," Proc. of the Int. Symp. on Microelec., ISHM, 1986, Atlanta, GA, Oct. 1986.
3. E. Suhir, "Stresses in bi-metal thermostats," ASME J. Appl. Mech., vol. 53, No. 3, Sept. 1986.
4. D. R. Banks, R. D. Gerke, "Assembly and reliability of ceramic column grid array," Surface Mount Inter. Conf. & Expo., San Jose, CA, 1994.
5. R. N. Master, M. Cole, G. B. Martin, A. Caron, "Ceramic column grid array for flip-chip applications," ECTC, Hopewell Junction, NY, 1995.
6. A. Sinha, P. Isaacs, T. Tofil, "Mechanical reliability analysis of ceramic column grid array solder joints," IBM Jour. of Res. and Dev., Apr. 1997.
7. J. Fleisher, W. Willing, "Study of CGA components for space systems," Rel. and Maint. Symp. (RAMS), 2012.
8. E. Suhir, "Analysis of a short beam with application to solder joints:



13th International Wafer-Level Packaging Conference

October 18–20, 2016 | San Jose, California

## Exhibitor & Sponsorship Opportunities

### WHAT IS THE COST TO EXHIBIT?

	Member	Non-Member
<b>One Booth (8' x 10')</b>	\$1,300	\$1,500
<b>One Table (6')</b>	\$900	\$1,100

EARLY BIRD PRICING ENDS JULY 8<sup>TH</sup>

### WHAT IS INCLUDED?

- 8' x 10' Pipe & Drape Booth **OR** 6' Table-Top
- Standard Electric Included
- Booth Staff Lunches Each Day
- One Conference Pass (including proceedings)
- Electronic Attendee List
- Show Directory Listing
- Company Sign
- Networking Reception

### LOOKING FOR AN ALTERNATIVE SPONSORSHIP OPTION THAT YOU DON'T SEE LISTED?

Contact one of the representatives to reserve your booth or create a customized sponsorship package for your company!

Questions on the Conference or Exhibition

Jenny Ng

jenny@smta.org | 952-920-7682

Questions on Sponsorships and Exhibition

Kim Newman

knewman@chipscalereview.com | 408-429-8585

[www.iwlpc.com](http://www.iwlpc.com)

### SPONSORSHIP OPPORTUNITIES

Command the attention of the IC Packaging Industry!

#### PREMIUM SPONSORSHIP LEVELS

Platinum Sponsor (Limit 4) <b>(2 Left!)</b>	\$5,800
Gold Sponsor (Limit 4) <b>(1 Left!)</b>	\$4,700
Silver Sponsor (Limit 2)	\$3,800 <b>SOLD!</b>

#### ADDITIONAL SPONSORSHIP OPPORTUNITIES

All Sponsorships require an exhibit booth reservation.

Reception Sponsor (Limit 2)	\$2,500
Keynote Sponsor Day 1 or 2 (Limit 2)	\$2,000
Lanyard Sponsor	\$3,300 <b>SOLD!</b>
Lunch Day 1 or 2 Sponsor (Limit 2)	\$1,950
Refreshment Day 1 or 2 Sponsor <b>(1 Left!)</b>	\$1,000
Charging Station Sponsor (Limit 1)	\$2,200 <b>SOLD!</b>
Luggage Tag Sponsor (Limit 1)	\$1,800 <b>SOLD!</b>
Tote Bag Sponsor (Limit 1)	\$2,800 <b>SOLD!</b>
Notepad & Pen Sponsor (Limit 1)	\$2,200
Wi-Fi Sponsor (Limit 1)	\$3,000 <b>SOLD!</b>
Raffle Drawing Sponsor	\$200
Show Directory Advertising Options:	
Full Page, Color, Front Inside Cover	\$750 <b>SOLD!</b>
Full Page, Color, Back Inside Cover	\$750 <b>SOLD!</b>
Full Page, B&W, Throughout Directory Unlimited Spaces	\$500



**SMTA**  
Surface Mount Technology Association

**Chip Scale Review**  
The Future of Semiconductor Packaging

are proud to present the leading industry event for designers, users, and suppliers of 2.5D & 3D integration, flip chip, and wafer-level packaging equipment, materials, and services.

- could larger stand-off heights relieve stress?," Eur. Phys. Jour. of Appl. Phys. (EPJAP), vol. 71, 2015.
9. E. Suhir, "Adhesively bonded assemblies with identical nondeformable adherends and inhomogeneous adhesive layer: predicted thermal stresses in the adhesive," J. Reinforced Plas. and Comp., vol.17, No.14, 1998.
  10. E. Suhir, "Adhesively bonded assemblies with identical nondeformable adherends and piecewise continuous adhesive layer: predicted thermal stresses and displacements in the adhesive," Int. J. Solids and Struc., vol. 37, 2000.
  11. E. Suhir, "Thermal stress in an adhesively bonded joint with a low modulus adhesive layer at the ends," Jour. of Appl. Phys., Apr. 2003.
  12. E. Suhir, "Interfacial thermal stresses in a bi-material assembly with a low-yield-stress bonding layer," Modeling and Simulation in Materials Science and Eng., vol. 14, 2006.
  13. E. Suhir, R. Ghaffarian, L. Bechou, J. Nicolics, "Column-Grid-Array (CGA) technology could lead to a highly reliable package design," Paper #2006, IEEE Aerospace Conf., Big Sky, MT, Mar. 2016.
  14. E. Suhir, R. Ghaffarian, J. Nicolics, "Could thermal stresses in an inhomogeneous BGA/CGA system be predicted using a model for a homogeneously bonded assembly?," Jour. of Mat. Science: Materials in Elec., published online 28 Oct. 2015.
  15. E. Suhir, L. Bechou, B. Levrier, "Predicted size of an inelastic zone in a ball grid array assembly," ASME J. Appl. Mech., vol. 80, Mar. 2013.
  16. E. Suhir, R. Ghaffarian, J. Nicolics, "Could application of column grid array technology result in inelastic strain-free state-of-stress in solder material?," Jour. of Mat. Science: Mat. in Elec., accepted Aug. 25, published online Sept. 4, 2015.
  17. E. Suhir, R. Ghaffarian, "Predicted stresses in a ball grid array (BGA)/ column grid array (CGA) assembly with a low modulus solder at its ends," Jour. of Mat. Science: Mat. in Elec., published online Sept. 4, 2015.

## Biography

Ephraim Suhir received his MS from the Polytechnic Institute, Odessa, Ukraine, and PhD from Moscow State U. He is a Fellow of the American Physical Society (APS), the Institute of Physics (IoP), UK, Institute of Electrical and Electronics Engineers (IEEE), and the International Microelectronics and Packaging Society (IMAPS). He is on the faculties of Portland State U., Portland, OR USA, and Technical U., Vienna, Austria. He is also CEO of ERS Co., Los Altos, CA USA; email suhire@aol.com

## High Speed / Low Cost Development, Test & Burn-In Sockets

### Compression, SMT, & Thru-Hole PCB Mounting

Lead pitches as low as 0.4mm, up to 125,000 insertions.



Quick  
On/Off Lid



Easy Screw - Lid  
removed to show detail.

### Multi-Cavity Sockets

Significantly reduce your socket & labor costs with these multiple IC test and burn-in solutions.



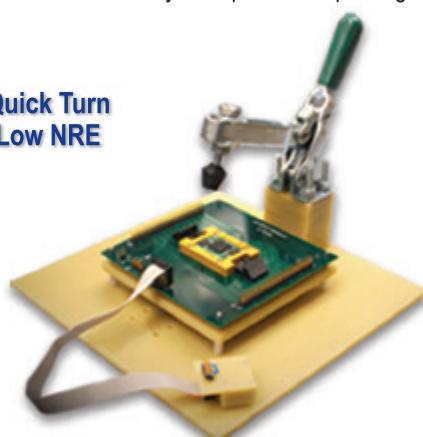
Easy Knob  
configuration



### Custom Test Fixtures

Fully automated or manually operated solutions to test any lead pitch & IC package

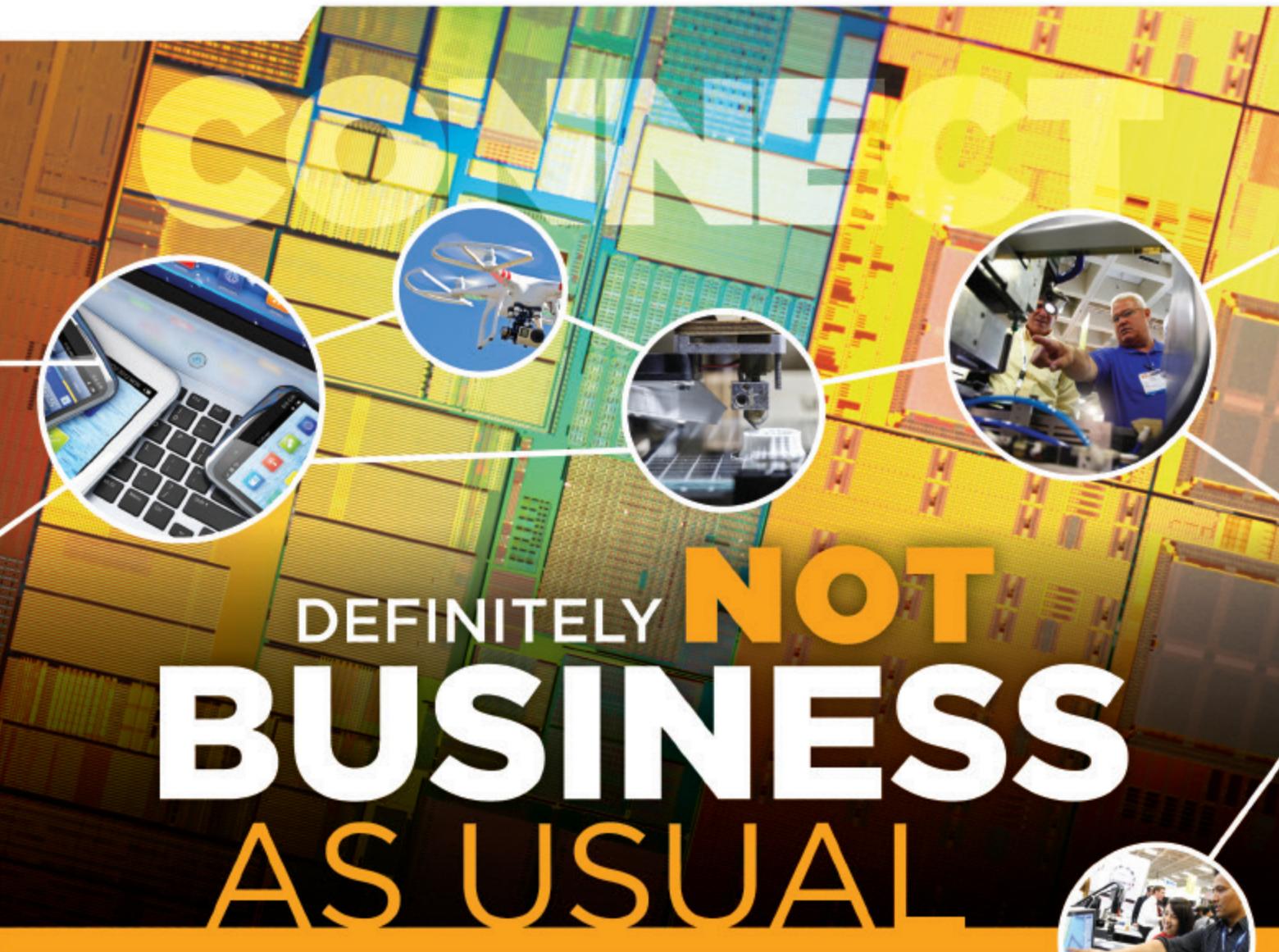
Quick Turn  
Low NRE



**ET®** **EMULATION  
TECHNOLOGY, INC**

1-800-232-7837

[www.emulation.com](http://www.emulation.com)



**Consolidation happened.** An unprecedented \$100 billion in M&As was announced in 2015. Where does that leave you? Find out at SEMICON West 2016—now completely re-engineered, **bringing together the full electronics supply chain** to help you find your place in today's "anything but usual" semiconductor market.



## The industry changed. SEMICON West did, too.

**SEMICON<sup>®</sup>  
WEST**

700+ Exhibitors | IC Design Summit | CONNECT Executive Summit | Future Innovators Seminar | Innovation Village | World of IoT Showcase | Silicon Innovation Forum Advanced Manufacturing Forum | 3D Printing/Additive Manufacturing Pavilion "Get CONNECTED" Opening Reception | Regional Pavilions | Community Networking Mixers | Compound Semiconductor Pavilion | and more...

Register Today—[WWW.SEMICONWEST.ORG](http://WWW.SEMICONWEST.ORG)

# INDUSTRY NEWS



## BiTS 2016: Exploring the impact of IoT and Big Data

The Burn-in and Test Strategies (BiTS) Workshop held its 17th annual North American event March 6-9 in Mesa, AZ (Figure 1). The event was attended by more than 200 test engineers and managers from around the world, representing more than 100 companies including top foundries, fabless and integrated device manufacturers. Also represented were outsourced subassembly and test suppliers, and suppliers of equipment and consumables to the semiconductor industry. More than 350 people participated in this year's event. Attendees provided very positive feedback regarding the opportunities to meet, network, and explore current test ideas and challenges with other professionals who are focused on emerging test challenges.



Figure 1: Main session at BiTS 2016.

Thirty technical presentations were delivered by suppliers, end users and engineering professionals. The presentations underscored the event's themes: the Internet of Things (which included the Internet of Vehicles), and Big Data and its impact on the semiconductor industry. A poster



Figure 2: A poster session at BiTS 2016.

session (Figure 2) reinforced the theme and highlighted related and contemporary topics. The event's notable keynote presentation, given by Dale Ohmart of Texas Instruments, and distinguished talk, delivered by Risto Puhakka of VLSI Research, were well received by attendees. In addition, BiTS 2016 featured a

**sensors**  
expo & conference

Sensing Technologies Driving Tomorrow's Solutions

June 21-23, 2016  
Exhibition Dates: June 22-23  
McEnery Convention Center | San Jose, California  
NEW LOCATION in the Heart of Silicon Valley!

Over 5,000 highly qualified engineering professionals are planning to attend. **Will you be there?**

**Sensors Expo & Conference is North America's premier event focused exclusively on sensors and sensor-integrated systems, and is widely known as the world's largest and most important gathering of engineers involved in sensor systems.**

**New** **Tracks and Focused Education.** With new and updated tracks, all new Pre-Conference Symposia, and over 55+ Technical Sessions at the 2016 event, you're sure to find the best in sensing technologies and innovative ideas to drive the future.

**New** **Embedded Systems Pavilion.** The Technology Pavilions on the Expo Floor showcase elite exhibitors that have the technologies and solutions you've been looking for. New for 2016 is the Embedded Systems Pavilion that is joining the ranks of the MEMS Pavilion, IoT & Wireless Pavilion, and Energy Harvesting Pavilion.

**Plus** **Networking, Visionary Keynotes, and more!** Register today and you'll gain access to hours of networking onsite, two visionary Keynotes (open to all), over 250+ top exhibitors, and free education on the Expo Floor in the Sensors Live Theater.

[www.sensorsexpo.com](http://www.sensorsexpo.com) #Sensors16 [f SensorsExpo](#) [@SensorsExpo](#) [in Sensors Expo & Conference](#) [@SensorsExpo](#)

\*Discount is off currently published rates. Cannot be combined with other offers or applied to previous registrations.



**Figure 3:** The BiTS EXPO.



**Figure 4:** The BiTS Technical Committee: Front row (L to R) - Ila Pal, Ira Feldman, John Hartstein, Ashok Kabadi; Back Rows (L to R) - Morten Jensen, Owen Prillaman, Marc Moessinger, Paul Boyce, Susan Kinne, Jeff Roehr, David Peterson, Jason Mroczkowski, Fred Taber, Valts Treibergs; Not shown: Debora Ahlgren, Rafiq Hussain. Company affiliations are listed at [bitsworkshop.org/committee.php](http://bitsworkshop.org/committee.php)



**Figure 5:** Tom Yin, CEO of TwinSolution Technology Ltd, the Premier Sponsor and Ira Feldman, General Chairman of BiTS 2016.

tutorial delivered by Jeffrey Roehr of Texas Instruments.

The ever popular BiTS EXPO ([Figure 3](#)) provided an opportunity for forty-seven companies to provide invaluable information to both attendees and visitors from the local technology community. An Executive Forum, seeking to solicit input regarding emerging trends and challenges in the industry from executives of participating companies and sponsors, was

facilitated by Rick Nelson, Executive Editor of Evaluation Engineering.

The BiTS technical program and exhibition are dedicated to providing a forum for sharing of the latest information on a broad range of test topics including final/packaged part test, wafer sort, and burn-in. The BiTS technical committee ([Figure 4](#)) comprises volunteers from across the industry and around the world, representing companies who are interested in helping to shape the conference and the industry.

TwinSolution Technology ([Figure 5](#)), which was celebrating its 10th anniversary, was the event's Premier sponsor, while Test Tooling Solutions Group continued its support as the Emeritus sponsor. "The strong on-going presence of an international group of professionals



**Figure 6:** Ira Feldman presents the Best Presentation award for the presentation, "Magnetically shielded test-cell for an integrated fluxgate sensor," to Gert Hansel of Texas Instruments and Loren Hillukka of Johnstech International Ltd.



**Figure 7:** General Chairman Ira Feldman presents the Best Presentation Tutorial In Nature award to Noureen Saji and Jeff Sherry of Johnstech International Ltd., for "Device packaging and how it affects RF performance."

visiting BiTS underscores the strength of the workshop's program," said Ira Feldman, General Chairman of the Burn-in and Test Strategies workshop. "This year, over 34% of participants were international visitors to Mesa, Arizona. And, both professional and overall participation are up 10% over 2014. We believe this portends a very strong BiTS China event in Suzhou this September."

In other news from the event, the Best Presentation award was given to Gert Hansel of Texas Instruments ([Figure 6](#)) for his paper entitled: "Magnetically shielded test-cell for an integrated fluxgate sensor." The Best Presentation Tutorial (in nature) was given to Noureen Saji and Jeff Sherry of Johnstech International Ltd. ([Figure 7](#)).

## Chip Scale Review®

ChipScaleReview.com

*The Future of Semiconductor Packaging*

**Advertise Now  
for**

**SEMICON®  
WEST**

**Show Edition  
May June**

**Ad Space Close May 20  
Ad Materials Close May 27**

**Contact:  
[ads@chipscalereview.com](mailto:ads@chipscalereview.com)**

Chip Scale Review is once again a proud Media Partner of SEMI for 2016

**May 31- June 3, 2016**  
*The Cosmopolitan of Las Vegas • Las Vegas, Nevada*

# ECTC 2016

The 66th Electronic Components  
and Technology Conference

**Don't Miss Out  
on the Industry's  
Premier Event!**

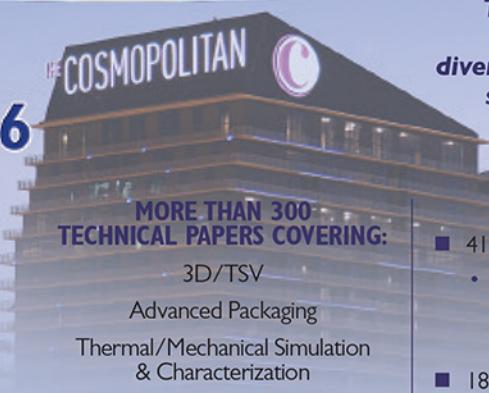
For more information, visit

**www.ectc.net**

Conference Sponsors:



Official Media Sponsor:



**MORE THAN 300  
TECHNICAL PAPERS COVERING:**

- 3D/TSV
- Advanced Packaging
- Thermal/Mechanical Simulation & Characterization
- Optoelectronics
- Interconnections
- Materials & Processing
- Applied Reliability
- Assembly & Manufacturing Technology
- High-Speed, Wireless & Components
- Emerging Technologies

**The only event that  
encompasses the  
diverse world of integrated  
systems packaging.**

**HIGHLIGHTS**

- 41 technical sessions including:
  - 5 interactive presentation sessions, including one featuring student presenters
- 18 CEU-approved Professional Development Courses
- Technology Corner Exhibits, featuring more than 100 industry-leading vendors
- 6 special invited sessions
- Several evening receptions
- 3 conference luncheons
- Multiple opportunities for networking
- Great location

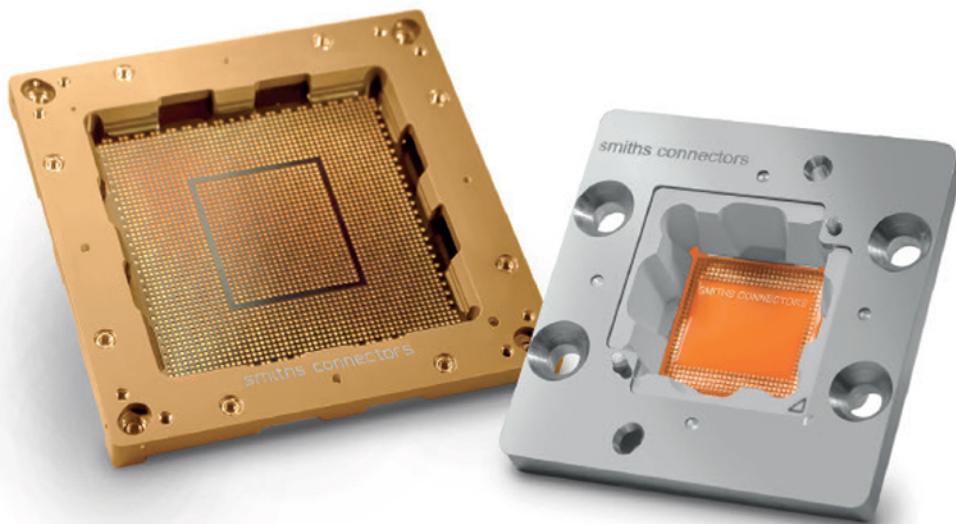
## ADVERTISER INDEX

Amicra Microtechnologies	<a href="http://www.amicra.com">www.amicra.com</a>	27	Johnstech	<a href="http://www.johnstech.com/industrybenchmark">www.johnstech.com/industrybenchmark</a>	49
Amkor Technology	<a href="http://www.amkor.com">www.amkor.com</a>	1	LD microprecision	<a href="http://www.ld-micro.com">www.ld-micro.com</a>	6
Aries Electronics	<a href="http://www.arieselec.com">www.arieselec.com</a>	41	LPKF Laser & Electronics AG	<a href="http://www.lpkf.com/mems">www.lpkf.com/mems</a>	35
Atotech	<a href="http://www.atotech.com/products/semiconductor-technology">www.atotech.com/products/semiconductor-technology</a>	15	MRSI Systems	<a href="http://www.mrsisystems.com">www.mrsisystems.com</a>	12
Chip Scale Review	<a href="http://www.chipscalereview.com">www.chipscalereview.com</a>	55	Nordson ASYMTEK	<a href="http://www.nordsonasymtek.com/nexjet">www.nordsonasymtek.com/nexjet</a>	39
Cohu, Inc.	<a href="http://www.cohu.com/products/contactors">www.cohu.com/products/contactors</a>	30	Nordson DAGE	<a href="http://www.nordsondage.com">www.nordsondage.com</a>	17
DL Technology	<a href="http://www.dltechnology.com">www.dltechnology.com</a>	42	PacTech	<a href="http://www.pactech.de">www.pactech.de</a>	47
E-tec Interconnect	<a href="http://www.e-tec.com">www.e-tec.com</a>	31	Plasma Etch	<a href="http://www.plasmaetch.com">www.plasmaetch.com</a>	37
ECTC	<a href="http://www.ectc.net">www.ectc.net</a>	56	Plastronics	<a href="http://www.plastronics.com">www.plastronics.com</a>	21
Emulation Technology	<a href="http://www.emulation.com">www.emulation.com</a>	52	R&D Altanova	<a href="http://www.rdaltnova.com">www.rdaltnova.com</a>	48
EV Group	<a href="http://www.evgroup.com">www.evgroup.com</a>	IFC	SEMI	<a href="http://www.semiconwest.org">www.semiconwest.org</a>	53
Georgia Institute of Technology	<a href="http://www.prc.gatech.edu">www.prc.gatech.edu</a>	7	Sensata Technologies	<a href="http://www.qinex.com">www.qinex.com</a>	9
GPD Global	<a href="http://www.gpd-global.com">www.gpd-global.com</a>	11	Sensors Expo	<a href="http://www.sensorsexpo.com">www.sensorsexpo.com</a>	54
IMAT Inc.	<a href="http://www.imatinc.com">www.imatinc.com</a>	33	Smiths Connectors	<a href="http://www.smithsconnectors.com">www.smithsconnectors.com</a>	IBC
Indium Corporation	<a href="http://www.indium.us/E042">www.indium.us/E042</a>	29	Sonix	<a href="http://www.sonix.com">www.sonix.com</a>	3
Ironwood Electronics	<a href="http://www.ironwoodelectronics.com">www.ironwoodelectronics.com</a>	45	SPIL	<a href="http://www.spil.com.tw">www.spil.com.tw</a>	OBC
IWLPC	<a href="http://www.iwlpc.com">www.iwlpc.com</a>	51	Winway Technology	<a href="http://www.winwayglobal.com">www.winwayglobal.com</a>	4

**smiths connectors**

*Introducing the new*

## **Silmat® Test Socket**



***Uniting the unparalleled attributes of Silmat®  
Elastomeric Contacts with the best-in-class engineering  
and test development practices of Smiths Connectors***

---

Smiths Connectors, a leading supplier of high reliability test solutions, is introducing the Silmat® elastomeric contact to our technology portfolio. The patented, low profile contact is engineered specifically to provide electrical and mechanical advantages in the Digital High Speed and PoP Top segments of the Semiconductor Test industry.

Dedicated to ☺

***Being your preferred solution provider***



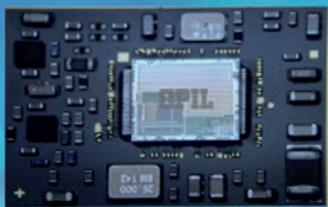
**Advanced Wire Bond**



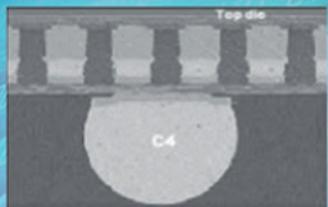
**Large Flip Chip Package**



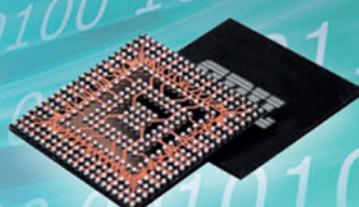
**mWLCSP**



**SiP**



**2.5D/INTI**



**FOWLP**

## **SPIL New Plant**

- Big Area**

*More than 5 years capacity growth*

- Turnkey Service**

*Bumping, Assembly & Testing*

- Advance Package Line**

*3DIC, FOWLP...etc*

