

# Chip Scale Review®

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*The Future of Semiconductor Packaging*

Volume 19, Number 3

May • June 2015

**Dispensing technologies in semiconductor packaging**

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- FOWLP
- Packaging for IoT
- Projection lithography
- Focused beam ellipsometry
- Challenges in advanced 3D integration
- 3D thermal simulation in the IC design flow
- Advanced bumping technology in mainland China





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The DispenseJet 9500 jets underfill for flip-chips that are attached to an organic substrate strip in an array layout. Using non-contact jetting, the fluid is able to be dispensed close enough to the edge of the device to minimize keep-out zones. Capillary force causes the underfill to flow underneath the die, thereby filling the spaces between the bumps on the die and the substrate.

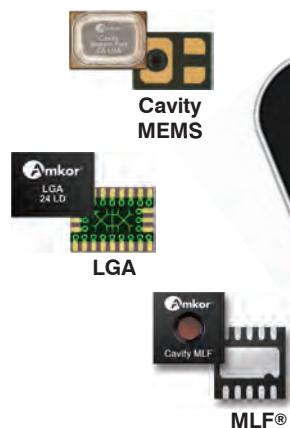
Photo courtesy of Nordson ASYMTEK.

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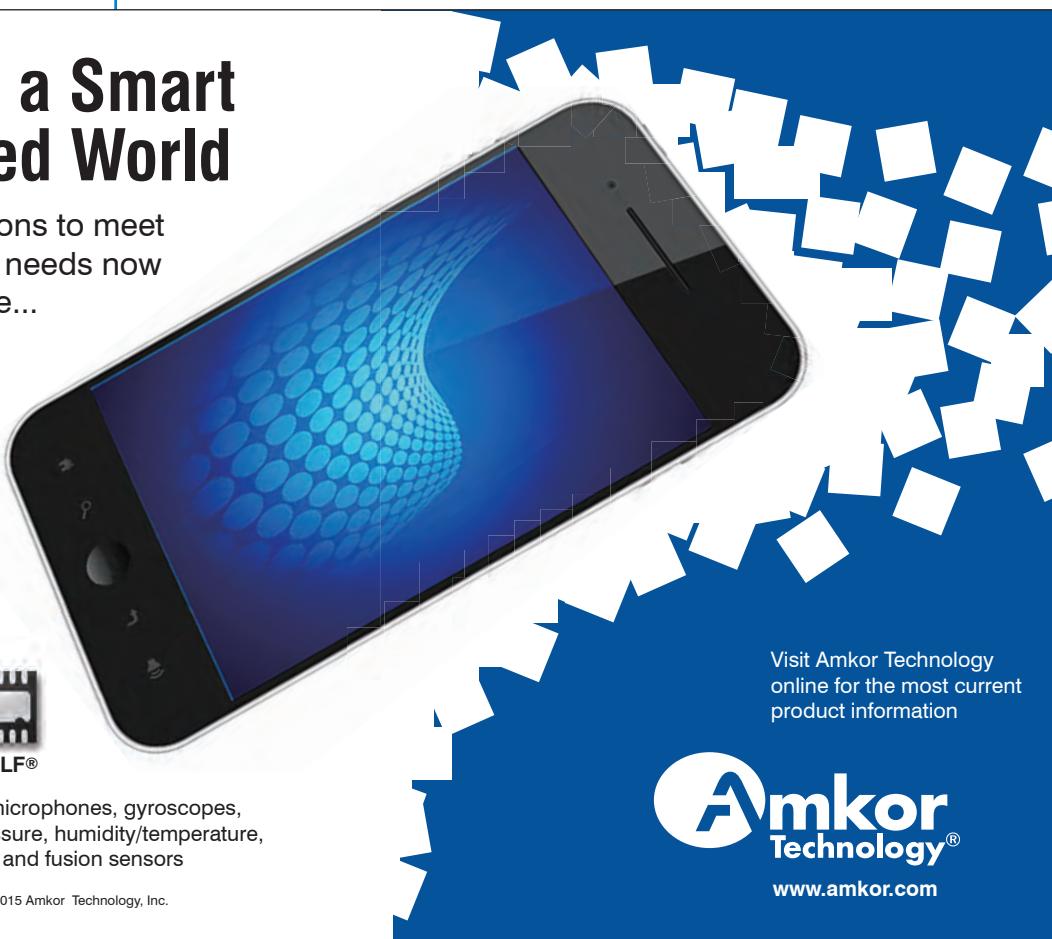
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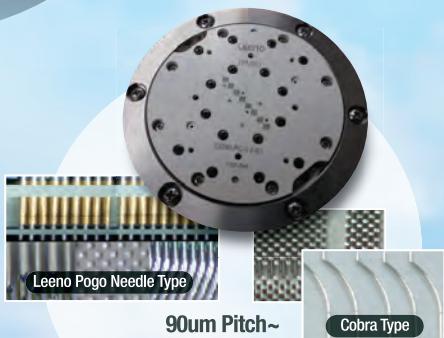
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**Wafer Level CSP Probe Card**



**Probe Head**



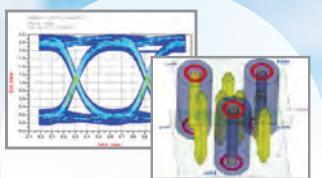
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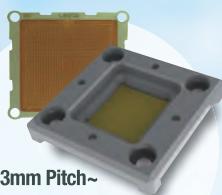


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# MARKET UPDATE



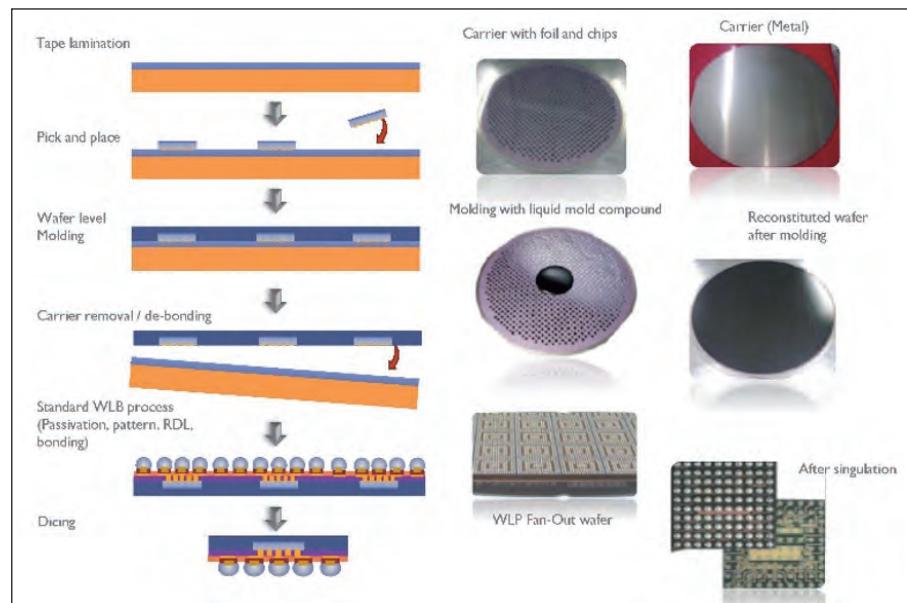
## Fan-out packaging: what can explain such a great potential?

By Jérôme Azémar, Phil Garrou [Yole Développement]

**W**afer-level packaging (WLP) has proven to be a high-performance, low-cost option for many applications such as consumer mobile products. We believe that at a given pitch, WLP is limited in the I/O it can provide since all the I/O pads have to fit within the area of the die. Fan-out packaging was developed to supply an increased number of I/O for such cases. Fan-out packaging is usable for single-chip, multi-chip, and system-in-package (SiP) assembly and can easily be extended to support package-on-package (PoP) configurations. Furthermore, we expect a \$200M fan-out WLP market in 2015 with 30% CAGR in the coming years. What can explain such a great potential [1]?

Fan-out WLPs (FOWLP) are typically “re-configured” by placing known good ICs active face down on a foil and over-molding them. The foil is then removed and the resultant plastic wafers are flipped and processed in a wafer fab. Front-end isolation and metallization redistribution layer (RDL) processing is then used to fan out the interconnections to the surrounding area with lithography and patterning wafer-level processes. Next, solder balls are applied and testing is performed on-wafer. The reconstituted wafer is then sawn into individual units, which are packed and shipped. As a WLP, fan-out wafer-level packaging (FOWLP) eliminates the printed circuit board (PCB) substrate as well as the need to use wire bonding or flip-chip bumps to establish electrical contacts. Without a PCB, the package is inherently thinner, which is a feature in great demand for today’s mobile products (**Figure 1**).

With the fan-in WLP approach, the number of interconnects and their pitch must be adapted to the chip’s size. FOWLP, by contrast, supports a fan-out area that is adaptable and which has no restriction on ball pitch. The FOWLP approach, not constrained by die size, can provide design flexibility to accommodate an unlimited number of



**Figure 1:** Process flow for standard Infineon eWLB fan-out packaging. SOURCE: Fan-Out and Embedded Die: Technologies & Market Trends Report – Feb. 2015

interconnects between the package and the board for maximum connection density, finer line/spacing, improved electrical and thermal performance, and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

### Development of fan-out wafer-level packaging

The Infineon e-WLB (embedded wafer-level BGA) technology [2] was commercialized in volume, in early 2009. Infineon’s chip was a wireless baseband SoC with multiple integrated functions (GPS, FM radio, BT, etc.). LGE, Samsung (baseband modem), and Nokia (baseband modem and RF transceiver) have used Infineon’s eWLB in their cell phone products. The Infineon eWLB wireless business was acquired by Intel in 2011 [3].

The Infineon technology was subsequently licensed to OSATS NANIUM [4], STATS ChipPAC [5] and ASE [6] which created a supply chain infrastructure with multi-

sourcing capability. While STATS ChipPAC and NANIUM have been steady, consistent suppliers since their licensing and subsequent scale-up, ASE dropped production a few years ago and recently has resumed production with the Infineon-based technology as well as in-house developed fan-out technologies.

Freescale’s redistributed chip package (RCP) process [7], is a similar technology that has been licensed to Nepes, who to date has very limited production with that technology [8].

FOWLP technologies are also being developed by TSMC [9], SPIL [10], J-Devices [11] and others. None are currently in HVM and will initially lack the multi-sourcing available with eWLB. TSMC recently purchased a plant in Taiwan from Qualcomm and reportedly is turning it into a facility devoted to the development of their advanced integrated fan-out wafer-level packaging (InFO-WLP) technology. TSMC reports manufacturing will commence in 2016 depending on “customer demand” [12].

SPIL has discussed its efforts to commercialize a panel fan-out package concept

|  | WFOP™                        | eWLB  |
|--|------------------------------|---|
| Package structure                              |                              |   |
| RDL (Redistribution Line) formation technology | PCB semi-additive technology | Semiconductor photolithography  |
| Manufacturing work size                        | Panel (Large size)           | Wafer (200 mm Ø / 300 mm Ø)   |
| Minimum device pad pitch                       | 50µm                         | 70µm<br>Influence of die shift problem caused by mold resin shrinkage |

**Figure 2:** Comparison of J-Devices' WFOP™ to the Infineon eWLB.  
SOURCE: Yole Développement.

by combining PCB, semiconductor backend, semiconductor WLP and LCD Gen 2.5 glass (370X470mm) processing technologies [9]. This effort requires high-accuracy die bonding and die shift compensation at film lamination, lower warpage sheet form film lamination, good copper trace plating uniformity control at large panel area, and also precise photolithographic technique. Known good die are reconstructed on the LCD Gen 2.5 glass carrier with adhesive temporary bonding material. Processing issues are identified as warpage, die shift "coordinates compensation at lithography" and Cu plating uniformity.

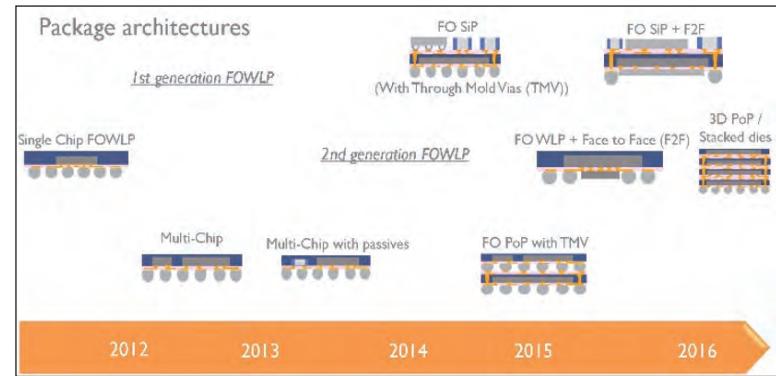
J-Devices is also attempting to develop panel based processing for low-cost fan-out packaging technology [11,13]. The J-Devices wafer fan-out package (WFOP) is compared to the eWLB in the following table (**Figure 2**). The metal plate serves to minimize warpage and decrease thermal issues. Greater than 1000hrs of package and board-level reliability have been achieved. It should be stated that such J-Devices' panel production is not yet in high-volume manufacturing (HVM).

### Second-generation FOWLP

The second-generation of FOWLP are multi-chip structures including familiar PoP and SiP architectures and the incorporation of passives. Double-sided and stacked solutions are created by through-mold vias (TMV). These new multi-die solutions are also available from STATS ChipPAC, ASE and NANUM. Such packages are generating increased interest in this packaging technology (**Figure 3**).

### The FOWLP market

Yole's analysts estimate that the 2014 market for FOWLP is ~\$174MM with



**Figure 3:** Second-generation FOWLP packaging options. SOURCE: Fan-Out and Embedded Die: Technologies & Market Trends Report – Feb. 2015.

STATS ChipPAC having the largest share at 59% of the market (**Figure 4**). With several new suppliers coming on line, we see the market growing at a 30% CAGR to >\$600MM by 2020.

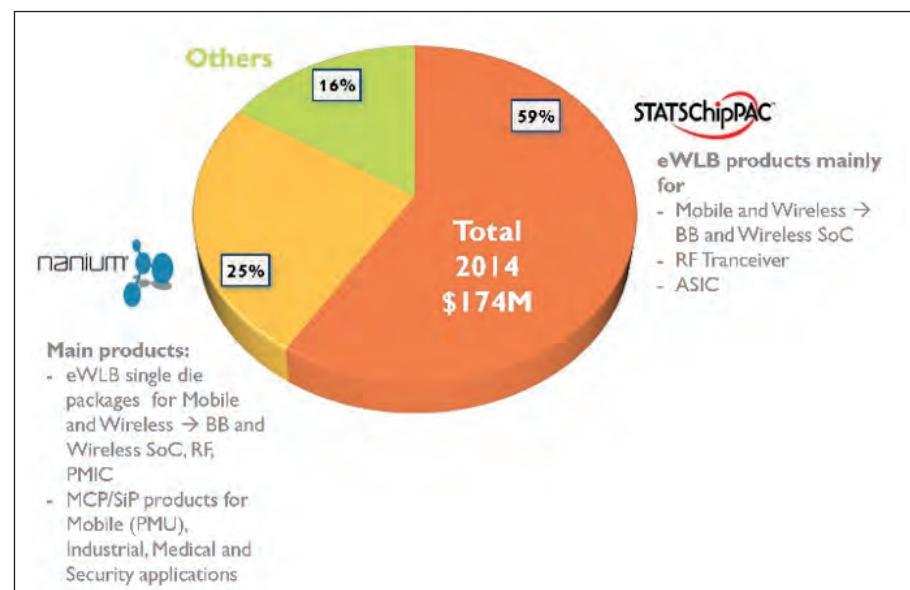
### FOWLP challenges

Despite its many positive attributes, challenges remain for FOWLP that impede its widespread adoption. IME has initiated a High-Density FOWLP Consortium that includes Amkor, NANUM, STATS ChipPAC, NXP, GLOBALFOUNDRIES, K&S, Applied Materials, TOK, KLA-Tencor, SPTS, and others [13]. Their compilation of challenges and proposed solutions is shown in **Figure 5**.

The two main challenges of fan-out

packaging are die shift and warpage of the molded wafer. Die shift impacts the alignment of the RDL on the die pad. Changes in die positions are caused by thermal expansion of the carrier during molding and shrinking of the mold compound upon cooling. Warpage impacts equipment handling. Processing equipment will not accept the molded wafer if warpage is too high. Proper selection of the mold compound and optimizing molding process conditions are therefore needed to minimize warpage of the molded wafer.

Finding the proper RDL insulator with a low-temperature cure has been a lingering problem. Typical materials with cure temperatures > 250C cannot be used because they exceed the  $T_g$  of the molding resins.



**Figure 4:** 2014 FOWLP revenue (\$MM). SOURCE: Fan-Out and Embedded Die: Technologies & Market Trends Report – Feb. 2015.

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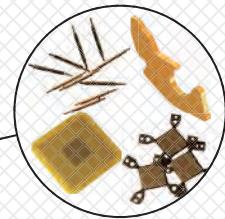


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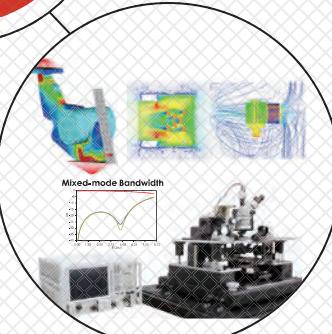
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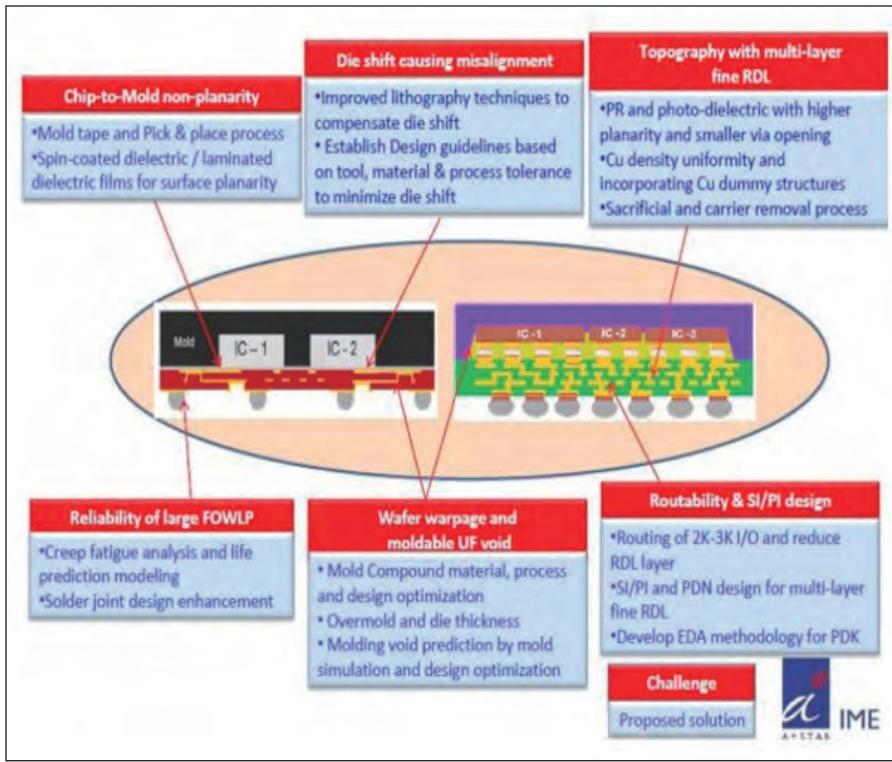


Figure 5: FOWLP challenges and proposed solutions. Courtesy A\*Star IME.

Polymer dielectric suppliers have been working on low-temp cure variations of the typical PI and PBOs to meet such FOWLP requirements.

In addition: 1) FOWLP is often perceived as too expensive; this issue should be alleviated as the new suppliers reach HVM; 2) FOWLP imposes a specific re-design vs. flip-chip solutions are much more flexible and mature cost-wise; and 3) The window of application for FOWLP is restricted to die that need an I/O pitch larger than the chip dimensions can accommodate, otherwise fan-in or other solutions will meet the requirements.

It is expected that the mobile industry will remain the main driver for FOWLP demand in the future because of its superior RF performance and its good form factor. The new FOWLP solutions such as SiP and PoP will soon allow it to penetrate the industrial, automotive, and medical markets.

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## Biographies

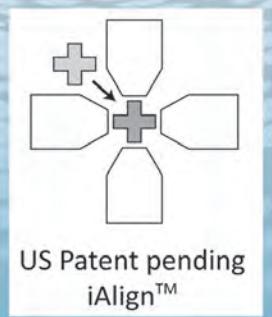
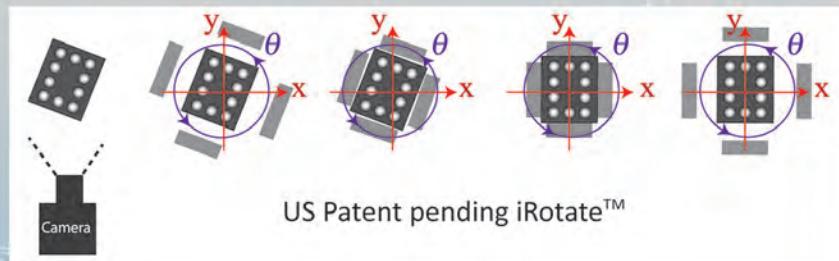
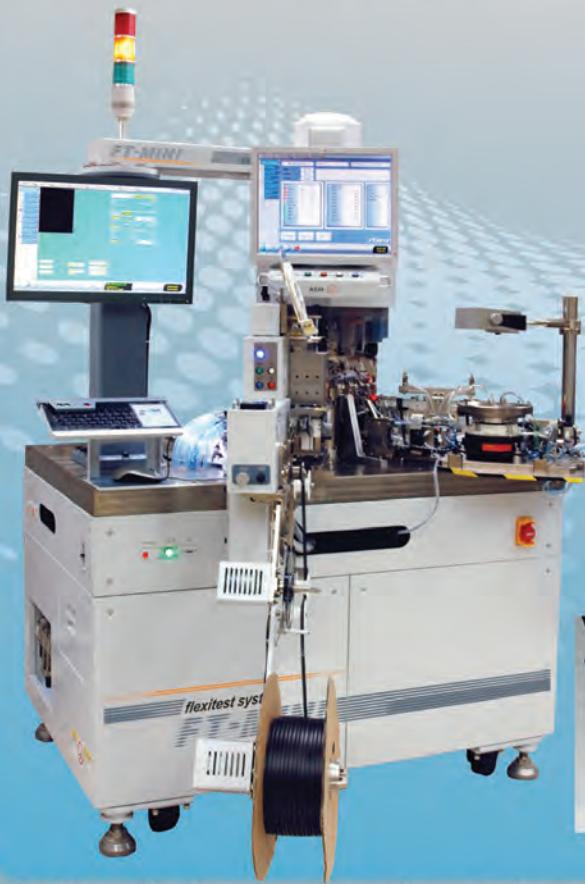
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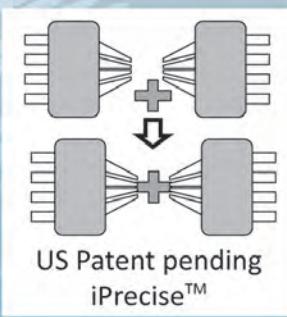
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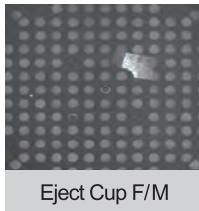
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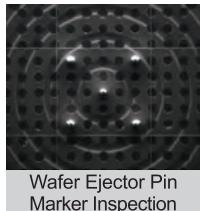
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|              | CHIP ROTATION        | ±0.05 °@ 3σ                   |
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# GUEST EDITORIAL



## Advanced bumping technology and solutions development in mainland China

By Lin (Leon) Tingyu [National Centre for Advanced Packaging (NCAP)]

**S**mart mobile, tablets, wearable products, and the Internet of Things (IoT) continue to drive packaging and interconnect technologies to achieve a balance among fine-pitch, small die size, advanced performance, and low cost. Additionally, the development of 2.5D/3D ICs are pushing the formation of middle-end processes (Figure 1). Bumping/Cu pillar are becoming key technology enablers of cost-effective middle-end supply chain processes. This is the reason that foundries and outsource assembly and test service (OSATS) providers are forming joint ventures with customer approval. For example, JCET and SMIC are working on middle-end processes, and a similar collaboration happened with ASE and Inotera. In addition, in China, Fujitsu and Tian Shui Hua Tian Technology Co., Ltd. are exploring their own middle-end process flow and building up their bumping capability.

Wafer-level packages are widely using “middle-end” technologies that are found in the overlap areas between the IDMs or CMOS foundries’ back-end-of-line (BEOL) wafer fabs and the back-end wafer bumping assembly facilities of OSATS and wafer bumping houses. Figure 2 illustrates the formation of “middle-end” technologies [1]. Middle-end processes are driving a new supply chain (Figure 3).

Based on mainstream bumping technologies, bumping interconnect and board-level assembly have three main categories; flip-chip mass reflow, thermocompression (TCB) bonding, and low-temperature Cu-Cu bonding (Table 1).

As advanced packaging technology nodes shrink to less than 65nm, chip/package interaction (CPI) issues pose challenges for middle-end processes. In particular, Cu and low-k (LK) dielectric materials have been adopted

to reduce propagation delay, crosstalk noise, and power dissipation because of RC (resistance capacitance) issues [3]. Existing extreme low-k dielectric materials have lower hardness and mechanical modulus that results in a major reduction of the material strength of the ELK material. That, in turn, could induce delamination of the ELK at board-level assembly. In addition, compared with lead-free solder, Cu pillar and substrate bonding will have a much higher stiffness that will increase mechanical stress on the ELK material. Therefore, a CPI margin and design rules are necessary; study results have been given with details [3-6].

There are some additional challenges associated with bumping technologies, for example, the bumping process, which has encountered undercut issues [7], bumping height uniformity, etc. The substrate is facing fine line/space, small via diameter, warpage/flatness and low CTE core and solder mask material issues. Additionally, nonconductive paste/nonconductive film (NCP/NCF) has to be balanced with  $T_g$  and Young’s modulus to fully protect the bump and low-k material, flowability with proper penetration around a 20 $\mu\text{m}$  gap and smaller filler size, as well as the requisite lower viscosity. In another aspect, the smaller under bump metallization (UBM) diameter may

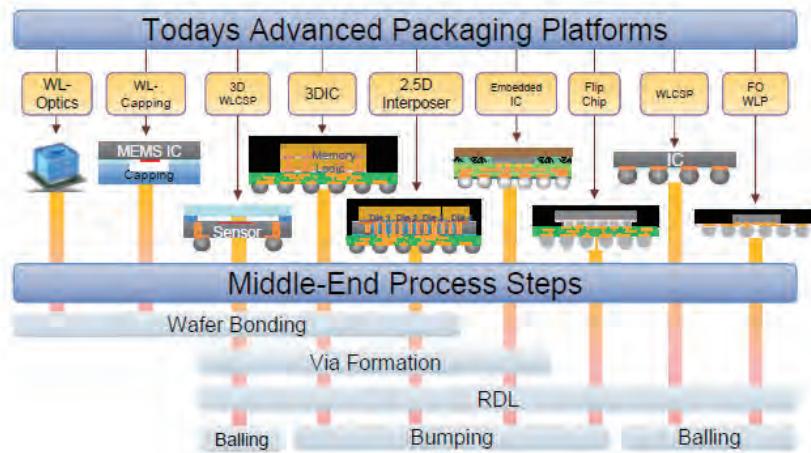


Figure 1: The roles of bumping/Cu pillar in today's advanced packaging platforms. SOURCE: Yole Développement [1]

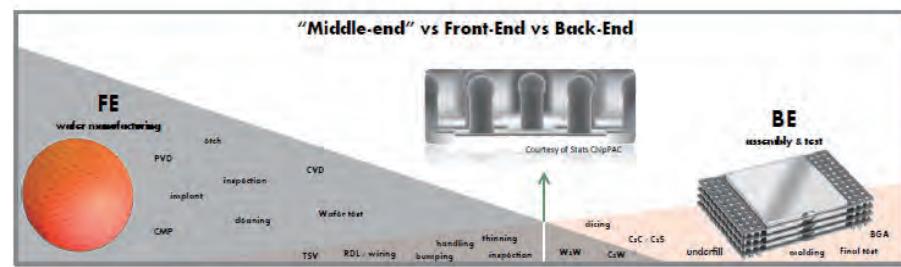


Figure 2: WLP middle-end technologies and market formation [1].



Figure 3: Middle-end process supply chain and market scale [2].

| Methodologies       | Bump diameter ( $\mu\text{m}$ ) | Bump pitch ( $\mu\text{m}$ ) | Bump metal           | Challenges   |
|---------------------|---------------------------------|------------------------------|----------------------|--|
| Cu pillar bump      | >15                             | >40 or <40 (micro-bump)      | Cu/Ni/Sn; Cu/Ni/SnAg | Warpage and flatness (silicon and substrate); low CTE substrate          |
| Solder bump (print) | 200                             | 400                          | SAC305               | High throughput, high yield, and low CTE substrate, warpage of substrate |
| Solder bump (mount) | 100-150                         | 150-300                      | As customer requests | High throughput, high yield, and warpage, and low CTE of substrate       |

Table 1: Bumping technology and challenges summary.

increase stress on the low-k material that could induce reliability issues. IMC cracks are caused by void creation and subsequently induce a crack along the whole bump [7].

From a bumping production capacity perspective, JCET (Jiangsu Changjiang Elect. Tech, HuaTian and Fujitsu – three major OSATS in China – are more or less ready for facing the challenges discussed above and have robust solutions available. In general, the production capacity is much higher than expected and can meet most of the customers' requests. For example, JCET/SMIC, a joint venture between these two companies, executed factory

expansion in 2015; the bumping capacity has improved greatly and can meet customer requests beyond 100k pieces per month (12" wafer). Additionally, Hua Tian Technology Co. Ltd. has a capacity >5000pcs per month for copper pillar and solder bump processes, respectively; their products are mainly for CIS, MEMS, Touch finger, PMU and interposer.

### Summary

Chinese OSATS have technical solutions for Cu pillar (pitch >40 $\mu\text{m}$ ) and solder bumping. Currently, they put more effort on improving

yield for middle-end processes, and continue to explore 2.5D/3D IC packaging and interconnect applications. In the next few years, TCB and low-temperature Cu-Cu bonding will be the main business focus. There are no mature technology enablers for TCB, and Cu-Cu bonding and emerging technologies are being built up with the goals of high throughput, low cost and high-reliability.

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### Biography

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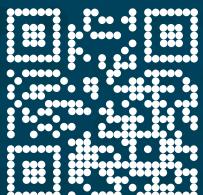
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# Dispensing technologies in semiconductor packaging

By Akira Morita, Garrett Wong, Dan Ashley [Nordson ASYMTEK]

**F**luid dispensing is used in the manufacture of semiconductor packages that comprise a wide variety of products. Specific techniques and equipment are required for each application and several options are available for each. Because these dispensing applications generally deal with microelectronics, to get the quality, reliability, precision, and accuracy that are required, process controls become an important manufacturing consideration. This article explores the role that dispensing plays in semiconductor packaging and the types of equipment and processes needed for success.

The main semiconductor packaging dispensing applications are underfill, flux, thermal interface material (TIM), and solder seating lines for flip-chip assembly, wafer-level packaging, and lid assembly. A lot of the equipment and techniques that have been used to accurately dispense fluid have been around and tested for many years. The difference is that now some of the equipment and fluids have been refined to accommodate the chips being used in today's applications. These chips can be allocated much more densely, placed closer together, stacked, and/or thinner.

## Flip-chip underfill

Underfill is a popular and proven technology for flip-chip assembly. The most important reason for applying underfill is the mismatch of coefficients of thermal expansion (CTE) between silicon die and the organic substrate. Without underfill, because of rapid thermal cycling, the mismatch can cause significant stress on the interconnections or bumps between the die and substrate, resulting in their fatigue and cracking. One of the key trends found in denser packaging is that bump stand-off (bump height) is shrinking: from 100 $\mu\text{m}$  to 80 $\mu\text{m}$  and 40 $\mu\text{m}$ . This lower bump stand-off induces more stress on the bumps, giving further importance to underfilling.

The equation established to define this phenomenon is the strain and modified Coffin-Manson equation. It is based on the principle that different thermal expansion rates of the die and substrate result in relative displacements that induce shear and axial strains in the interconnection. As the bumps get smaller ( $h$ ), displacement is the same; therefore, the stress

gets larger. **Figure 1** is a schematic of one-half of a typical flip-chip attached to a substrate.

The modified Coffin-Manson equation relates strain to fatigue life. Fatigue life is the number of cycles the bump can endure before cracking to failure. The equation says that the number of cycles to failure is proportional to 1 over the strain squared. As an example, a 50 $\mu\text{m}$  bump has twice the strain of a 100 $\mu\text{m}$  bump; therefore, the 50 $\mu\text{m}$  bump design will fail 4 times sooner under the same conditions.

Capillary underfill has been the most popular underfill dispensing technology since flip-chips emerged (**Figure 2**). Therefore, experience with that technology enables it to support a wide variety of flip-chip devices. Capillary underfill works very simply: when underfill material is dispensed next to the flip-chip, it will spread under the die with capillary force caused by the narrow gaps among the die, bumps, and substrate. Because of this capillary principal, the underfill material needs to be at a low enough viscosity to flow smoothly under the die.

To lower the viscosity, the underfill dispensing system applies heat to the substrate (usually during the dispensing process) to decrease the viscosity, maintaining the fluid at a constant temperature of about 80-100°C. Rather than contact heating or radiation heating, impingement heat (convective heating) is the most reliable way to heat

a board. Because the backside of the substrate sometimes is populated with components or rough structures, and backside circuits cause different heat absorption because of reflections, impingement heating has become the most popular technology.

Underfill material should be dispensed close to the die edge because the underfill fillet

## Strain & Modified Coffin-Manson Equation

- Different expansion rates of die and substrate result in relative displacements that induce shear and axial strains in the interconnection
- As the bumps get smaller( $h$ ), displacement is the same, therefore stress gets larger.

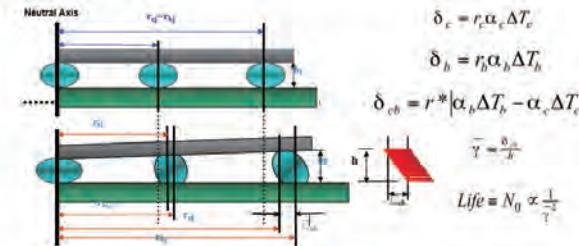


Figure 1: Strain and modified Coffin-Manson equation.

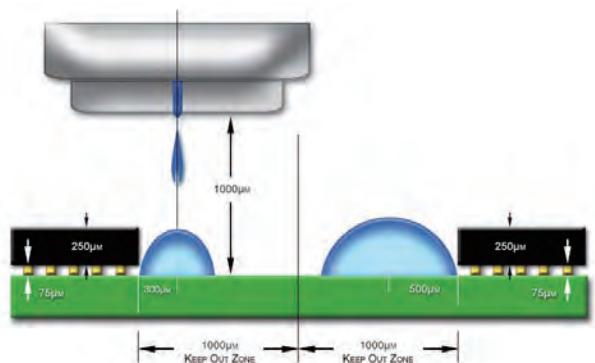


Figure 2: Jetting underfill.



Figure 3: Dispensing examples: a) Needle dispensing showing retraction; b) Jet dispensing a drop.

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should be as small as possible. The dispensing system has to be able to maintain a very tight keep-out zone (KOZ). The KOZ is quite critical because of denser component layouts; therefore, jet dispensing is the standard technology for this application (**Figure 3**). It is non-contact dispensing, shooting small fluid dots from the dispenser tip, which does not touch the device. As the dispensing head passes over the device, dots of fluid are shot next to the die. This is one of the most distinguishing differences between jetting and needle dispensing. Furthermore, jet dispensing is 3 to 5 times faster than needle dispensing because in needle dispensing, the needle has to move up to break the fluid. In jetting, the tip doesn't have to retract before or after it dispenses the fluid, eliminating z-axis motion. This time savings is extremely significant when producing millions of units.

Recently some trials have been conducted in the market using a tilted jet for dispensing underfill (**Figure 4**). The aim is to dispense dots at the corner between the die bottom and substrate. This might decrease the KOZ because the fluid is moved to the die's side.



**Figure 4:** Jetting underfill using a tilt and rotate head.

Another benefit is that tilted shooting has more tolerance in x-y accuracy than right-vertical shooting. When right-vertical shooting comes too close to the die edge without precise location accuracy, it could shoot dots on top of the die. Tilted-shooting has a greater margin of safety in location accuracy, thereby avoiding shooting dots on top of the die.

Process controls that are built into the dispensing equipment also enable a more reliable, predictable, dispensing process. Because the amount dispensed changes over time due to changes in fluid viscosity, the closed-loop process control of the dispense amount proves to be significantly beneficial. There are several process control systems available to regulate this amount: calibrated process jetting (CPJ), calibrated process jetting plus (CPJ+), and mass flow calibration (MFC) (**Figure 5**).

CPJ uses a scale inside the dispensing equipment to measure the average dispense weight per dot before actually dispensing on the device. The dispenser can determine the number of dots needed for each device by using dispense weight data that is input by an operator. The fluid or underfill material's viscosity will change in the syringe over time. This viscosity change will cause an average weight change per dot. The dispenser periodically checks the average weight, then adjusts the number of dots. For example, if one flip-chip needs 30mg of underfill and one dot weight has 30 $\mu$ g, then 1,000 dots would be dispensed for the die. If the dot weight changes to 40 $\mu$ g over time, the dispenser will adjust the number of dots to 750.

CPJ+ also measures the average dot weight by using a scale inside the dispenser, but the method of making the adjustment is different. It changes the weight to maintain the original dot weight per dot rather than changing the number of dots. In other words, in the above example, the weight of the dot would change from 40 $\mu$ g to 30 $\mu$ g. This adjustment is very useful when there is a smaller number of dots because a one dot difference is a large percent of the entire dispensing weight per device. Changing the number of dots wouldn't result in altering the weight very much.

MFC is basically the same methodology as CPJ, but it is applied mainly to time pressure

or needle or augur valves. Other calibration methods have been adopted in the market—for example, dispensing a dot on paper and measuring its diameter rather than weighing it. However, measuring diameter is not very convenient in terms of automatic calibration when compared to measuring weight. Therefore, the use of CPJ, CPJ+, and MFC is more popular. These closed-loop processes are important because without them, if the fluid properties change, you have no way of knowing. These processes do, however, require specific hardware and software.

### Flux jetting

Flux is another important process for flip-chip assembly (**Figure 6**). It removes the oxidized layer that's on the circuit pads and the bumps' surface for better solder wetting and reliable solder bonding. Before flip-chip bonding, flux must be applied on the bumps of the flip-chip or the substrate surface. Many die bonders have a flux dipping capability. The bumps of flip-chip are dipped into a thin flux coating just before flip-chip attachment to the substrate. This method has two challenges: 1) Too much flux tends to be applied, and 2) Bump height variation causes the flux to be applied non-uniformly. The viscosity of the flux used for dipping is higher than for spraying, so the flux sometimes climbs up the die edge to the backside of the die, resulting in too much flux and contamination to the top of the die. The extra flux residue can cause device failure. In addition, because the flux isn't applied uniformly, some bumps do not get fluxed.

A better method of applying flux is to use a dedicated system designed to apply the flux with a spray in a thin and uniform coat onto the substrate surface. The thinner the flux the better, not only because only a small amount of flux is needed to remove the oxidized layer, but also because too much flux leaves a residue that can prevent underfill from filling the gap between the die and substrate, causing the device to fail. Spraying the flux over the substrate ensures a more uniform application than applying it to the bump side of the die. These systems can spray a wide array of patterns and geometries while maintaining good edge definition (0.5 to 1.0mm) and minimizing overspray. Because of the volatile and hazardous nature of the flux, getting a fully-enclosed, vented system is recommended. Many high-volume production sites use dedicated flux spraying machines.

### Thermal interface material

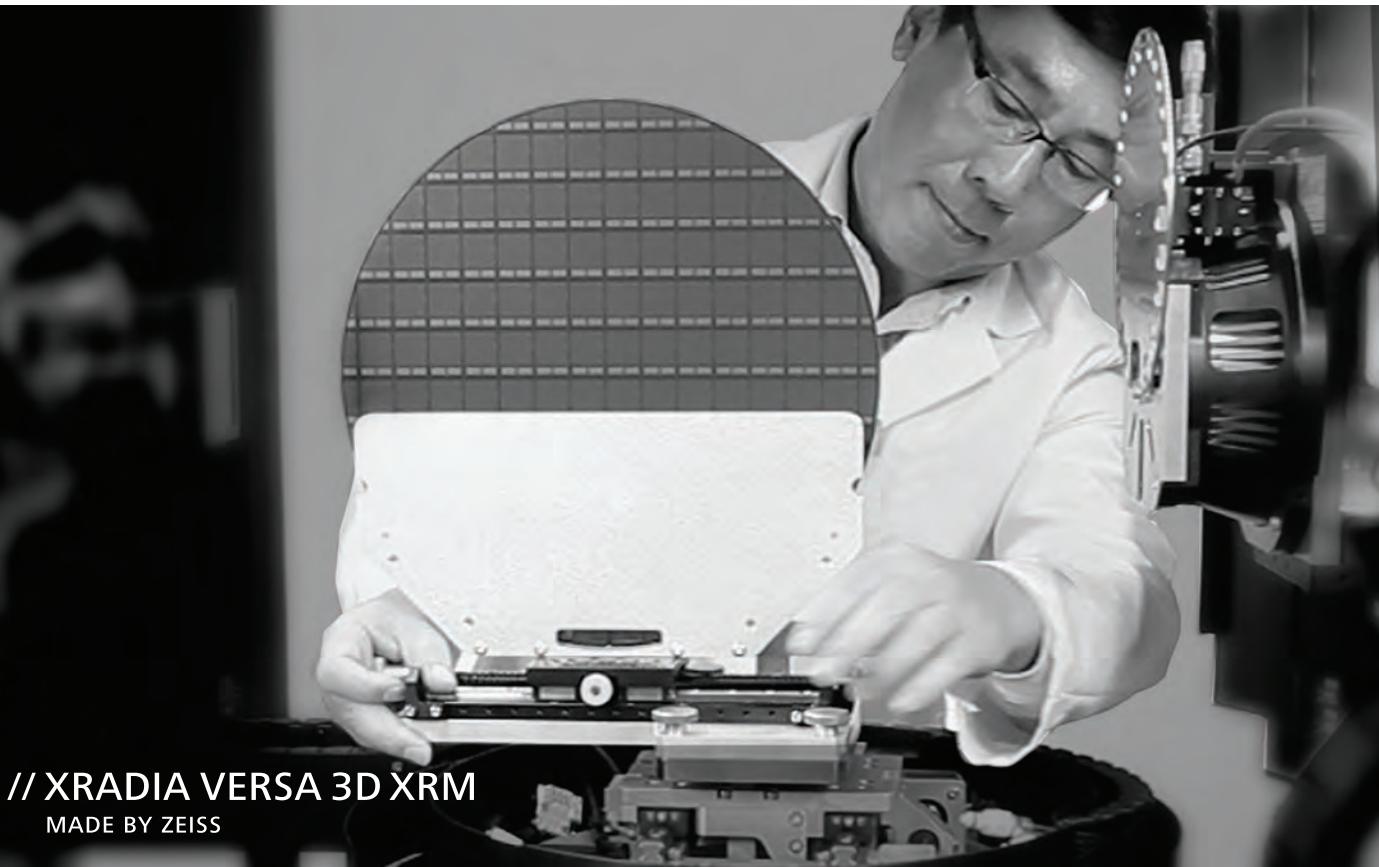
Lids are attached to the top of die used in logic devices to dissipate the heat the dies generate during their use (**Figure 7**). Thermal interface material (TIM) is dispensed on the



**Figure 5:** Dispensing weight adjustment with CPJ.

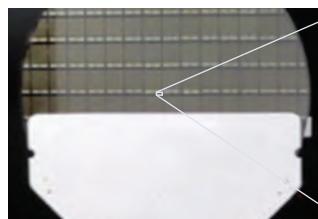
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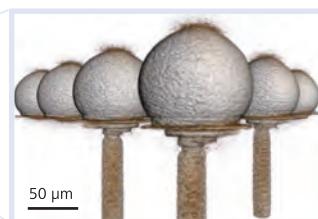


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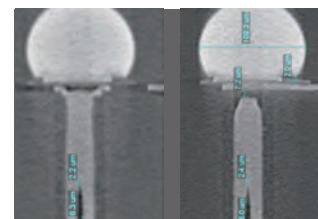
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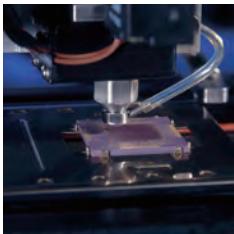


Figure 6: Applying flux.

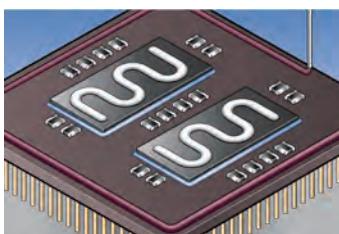


Figure 7: Lid sealing.

top of the die, filling the gap between the top of the die and the lid. The cut edge of the lid is attached to the substrate surface with a solder paste sealing line that forms an adhesion between the lid and the substrate.

Dispensing TIM is a very exacting process. If there is too little fluid dispensed or it's not dispensed accurately, a gap can be created between the die and the lid and the heat won't dissipate adequately. If too much TIM is dispensed on top of the die, it creates a mess inside the lid and the lid might tilt, resulting in lid attachment failure. Many TIMs are made of a silicone base, so its sticky characteristics make it difficult to break off during dispensing. Therefore, maintaining volume control during dispensing is a major challenge. Along with calibrated process jetting, some systems provide mass flow calibration. Working in tandem, they provide automatic calibration to consistently deliver user-specified amounts of fluid, minimizing setup-to-setup and line-to-line variations, while completely eliminating the need for operator interaction. MFC and CPJ automatically compensate for both fluid viscosity changes over time as well as batch-to-batch variations.

### Solder paste sealing lines

Solder paste sealing lines (Figure 8) are applied to attach the lids in semiconductor packaging in a process very similar to MEMS and printed circuit board (PCB) assembly. However, unlike MEMS cap sealing, the semiconductor lid attachment is most commonly used for heat spreading from the semiconductor chip to a larger heat sink. Although the purpose of the lid is different, many of the challenges in solder paste dispensing are the same between these applications.

As package sizes are reduced and board densities increased, these sealing lines become thinner to accommodate smaller package sizes. Yet, there is constant pressure

to increase the dispenser's productivity by moving to higher line speeds to dispense the solder paste and to use multiple valve systems to increase productivity.

Sealing lines need to form a complete seal around a device, so the lines are usually dispensed in a continuous line around all four sides of the device. Increasing the line speed creates challenges because as the speed increases, it's more difficult for the dispense platform to hold a consistent, straight line to mate well with the lid, which is applied downstream from the dispenser. As the line widths decrease, contact area with the lid decreases and any waviness in a line, particularly after rounding a corner, can result in incomplete contact around the lid and device yield loss or premature reliability failure. When increasing speed, maintaining tight control over the dispensed line path becomes increasingly important.

Achieving small, thin line widths also is more difficult when dispensing with multiple valves. To achieve very thin lines of solder paste, the auger valve needle must be placed very close to the substrate surface. Using a high-accuracy height sensor and precision Z-axis controls to correctly position each valve needle tip relative to the surface height is critical. With multiple valves riding on a single gantry, the ability to independently control the Z-height of each valve is also critical for dealing with warpage or height variations in the substrate. Multiple valves increase the number of height sensing measurements that must be performed to adjust the individual height of each valve. The extra time for such increased height sensing reduces some of the time savings derived from implementing a multiple valve set-up. However, height sense times are a very small portion of the

overall solder paste dispensing process time, so using multiple valves in an auger system still increases the overall throughput of the dispenser.

As a result of these challenges, a number of companies have explored using jetting technology to dispense solder paste,

as it may enable higher line speeds and smaller, thinner lines. Traditionally, due to its high viscosity and solder ball content, solder paste has been dispensed with auger or time-pressure valves.

Early attempts at jetting solder paste often resulted in individual solder balls coining from the contact between the ball and seat of the jet, leading to clogging of the jet nozzle. Coining is the process by which the round solder ball material is flattened by a vertical imposed force, essentially flattening out the ball (and making it wider)—the same process used for minting coins. Since then, a collaboration between solder paste suppliers and dispensing equipment companies to alter the jet mechanics and formulate solder pastes with higher flux content has resulted in successful jetting of smaller, more consistent solder ball sizes, but these are different solder paste formulations than standard pastes historically have been. The technology is still in its infancy and only a small sub-segment of the larger solder paste dispensing market. Costs for these specially formulated solder pastes are higher, so adoption is slow. As such, many of these sealing line applications are still done using auger valves for dispensing, while trying to increase line speeds and use multiple simultaneous valve set-ups to increase equipment productivity.

### Other applications

Additional dispensing applications include ball grid array (BGA) solder ball reinforcement, dam and fill, chip attachment, cavity fill, die attach, non-conductive paste, no flow underfill, and 3D packaging. These applications require dispensing systems that are extremely accurate, reliable, precise, and that can dispense very small amounts, in very tight places, at extremely high speeds. As products and technologies change, causing manufacturing and assembly processes to become more challenging, more collaboration is needed between the designer, the fluid formulators, the dispensing equipment manufacturers, and everyone involved in the manufacturing process to ensure that the systems are available to enable future products and technology.

### Biographies

**Akira Morita** received his BS and MS in Physics at Ritsumeikan U., and MBA at Rensselaer Polytechnic Institute, and is Business Development Manager at Nordson ASYMTEK; email [Akira.morita@nordsonasymtek.com](mailto:Akira.morita@nordsonasymtek.com)

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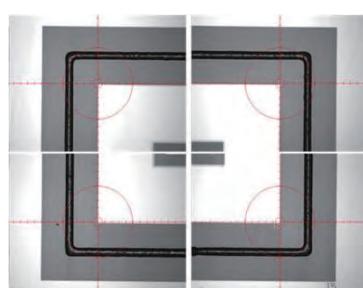


Figure 8: Solder paste sealing lines.

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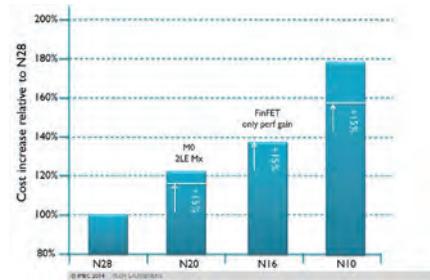
# Next-generation 3D FPGAs

By Xin Wu, Woon-Seong Kwon, Suresh Ramalingam /Xilinx/

Over the past 50 years, semiconductor technology has advanced dramatically, keeping incredible pace with Moore's Law's doubling of capacity every 22 months, while enabling greater functionality, performance and power efficiencies. In recent years, however, this progress has been facing an increasing number of technical and cost challenges. An ingenious way companies are overcoming these challenges today is by employing 3D IC technologies that place multiple dies stacked side-by-side on a silicon interposer, or stacked on top of one another. By doing so, companies can create devices that exceed the capacity pace of Moore's Law. For example, in 2011 we brought 3D IC technology into actual volume production with the Virtex®-7 2000T. At 6.8 billion transistors and 2 million logic cells, the 28nm 3D IC was almost 40% greater capacity than the largest FPGA implemented in a traditional monolithic 28nm process [1-3]. 3D IC development continued to mature with the introduction of our 20nm UltraScale™ family that includes the use of the "Xinterposer" on the Virtex UltraScale VU440T FPGA [1, 4]. Creating these 3D IC devices came with its share of challenges.

Over the last decade, semiconductor companies have had to look for more innovative ways to maintain the increase in capacity, performance and power efficiency of devices, while keeping costs reasonably low. In particular, transistor leakage has become a worsening problem in planar semiconductor processes, and becomes untenable below 20nm. To address these challenges, in recent years semiconductor manufacturers have devised a number of innovations such as high-k/metal gates (HK/MG), double-patterning, M0 structures, FinFETs, and uni-directional back-end-of-line (BEOL). These innovations address the technical challenges, but they are more complex, so they also increase the cost of building devices.

**Figure 1** shows imec's estimation of the cost of recent technology nodes. Although each company and its



**Figure 1:** Imec's estimation of technology cost in different nodes. Courtesy of imec.

technology costs are not the same, this graph nevertheless indicates a troubling trend. With all the challenges mentioned above, the rate of adopting newer technology nodes has slowed.

## 3D IC: capabilities for integration and growth

Over the past several years, 3D IC technology developments have made significant progress [5-9]—not only increasing capacity, but also increasing the performance, reducing power consumption, and lowering total cost per gate of the ICs. Unlike today's Si technology, which has a fairly uniform direction of development, 3D ICs offer a variety of development opportunities.

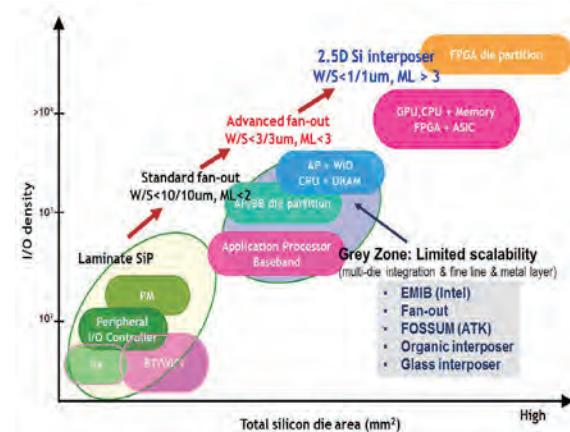
**Figure 2** shows the many categories of passive 3D (both multi-chip modules [MCMs] and ICs) technologies and their connectivity capability (I/O density) vs. their contents capacity (Si die area).

The lower-left corner of **Figure 2** shows a group often referred to as MCMs, which are a relatively mature, lower-cost 3D technology in which devices are connected on a package or tiny printed

circuit board (PCB) that is, in turn, bonded to a system PCB. MCMs mostly utilize existing packaging technologies with I/O counts in the range of a few hundreds and a connection line width/spacing larger than 10µm.

The middle group (see **Figure 2**), which has an I/O count in the one to several thousands range, is mostly used for chip-to-chip connections. The technologies here are fan-out, or EMIB (Intel), or various kinds of interposers, etc. The connection line width/spacing is for the most part in the range between 10µm/10µm to 1µm/1µm. Their cost will typically be higher than those in the MCM group.

The top-right group (see **Figure 2**), which has connectivity ranging from tens of thousands to several hundreds of thousands, is utilizing uBump (micro-bump) through-silicon via (TSV) and

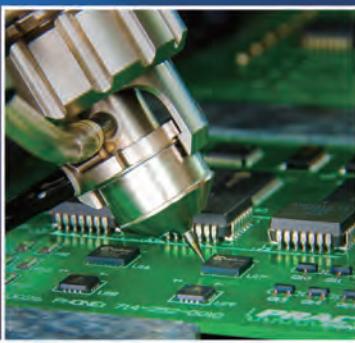


**Figure 2:** Connectivity capability (I/O density) vs. contents capacity (Si area) of various passive 3D IC technologies, as of today.

Si fab technologies. The interconnect of devices in this group can have sub-micron to even state-of-the-art BEOL technologies. These technologies allow die partitioning (i.e., connection without going through I/Os). Therefore, they not only offer higher content integration, but also can save a large amount of power, which reduces

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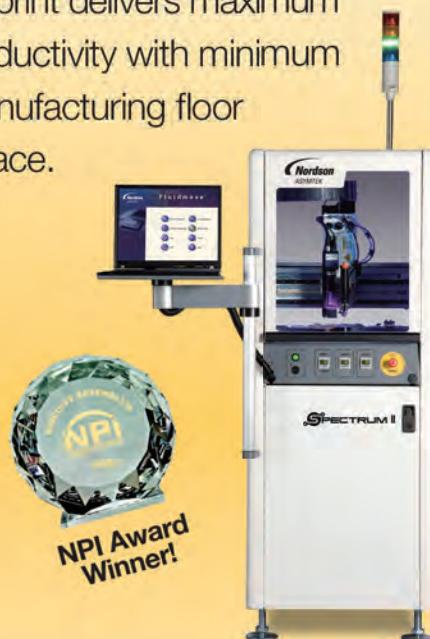
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the number of connections required for I/O or bridges. Xilinx' Stacked-Silicon Interconnect (SSI) technology and TSMC's CoWoS (Chip-on-Wafer-on-Substrate) belong to this category.

Up to this point, we've discussed passive 3D ICs, where the interposer or other media connecting two or more active chips do not contain transistors. There is an additional category of 3D ICs known as active-on-active 3D IC (i.e., active 3D IC) in which each component, except the package substrate, all have some amount of transistors. **Figure 3** shows various examples of active 3D ICs.

In **Figure 3**, the active 3D ICs are categorized by 3D integration formats. The chip-level integration active 3D ICs are mainly memory devices interconnected through uBumps and TSVs. The wafer-to-

technologies, some passive and some active, are in production, while many more are in the development stage. If one is considering implementing a design in a 3D IC, one must ensure the method being used meets time-to-market and cost requirements, as some 3D IC technologies (especially the newest ones) may take time to ramp and qualify. Some may not end up working at all.

**Product and planning.** While all 3D IC technologies provide capabilities far beyond planar ICs, they typically incur more cost. One needs to ensure a device will truly benefit from 3D and will be able to justify the higher cost.

**Architecture.** A 3D IC will most likely need a different architecture than that of a conventional monolithic IC. It might be less an issue in low connectivity, low

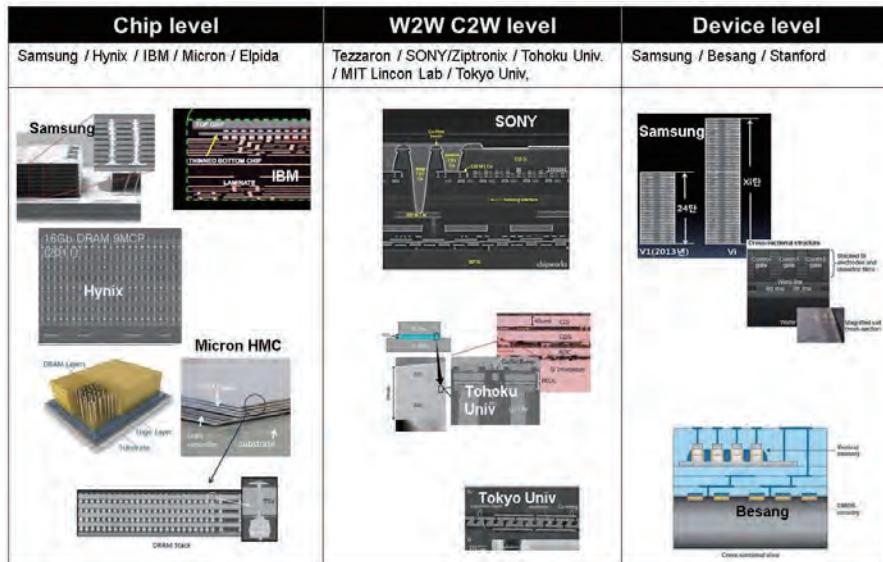
**Third-party IP and industrial protocols.** Industrial protocols for 3D ICs are in the very early stage of development. Some, such as the HBM standard, are here today, but many others are not yet available. If one needs intellectual property (IP) from third-party vendors, and if the connection protocols in between IPs or devices are not available, one needs to work with third-party IP providers to establish one between parties.

**Test, DFT (design-for-test) and KGD (known-good-dies).** Among all costs associated with 3D IC technologies, perhaps the most important one, especially at an early stage, is yield loss. Assume there are four dies in a 3D IC: the total yield is equal to  $Y_1 \times Y_2 \times Y_3 \times Y_4$ . If one of the dies is defective (found after assembly), the other three good dies won't work properly in the design. Therefore, KGD is a major issue. One might have to build in extra DFT capability in order to improve KGD.

**Supply chain.** Last, but definitely not least, the 3D IC manufacturing supply chain can become far more complicated than that of a conventional monolithic IC. For example, besides conventional Si wafer fab and assembly suppliers, there might be a 3D IC integration provider and/or third-party chip provider(s) from the same or different Si wafer fabs. Package substrate providers also play more significant roles because of their interaction with 3D ICs mechanically, electrically, and in terms of thermal management. Financial liability between suppliers becomes more complicated. Sometimes intellectual property concerns might prevent one Si wafer fab from shipping to another Si wafer fab for fear it might help their competitor become a 3D IC integration provider. One will need to plan and manage the supply chain more carefully.

## The evolution of 3D IC FPGAs

For well over a decade, our engineers have been researching 3D IC architectures, leveraging the fact that Xilinx FPGAs have relatively regular and repetitive structures, which lends them to being partitioned relatively easily (**Figure 4**). Nevertheless, the connectivity requirements of partitioned dies are much higher than normal package technology. Package technology can have interconnect counts around 1000 and line width/spacing of  $10\mu\text{m}/10\mu\text{m}$  or above. In comparison, a good FPGA partitioned die connection needs interconnect counts in the range of hundreds of thousands and



**Figure 3:** Various active 3D ICs, courtesy of various publications by Samsung, Hynix, IBM, Micron, Elpida, Tessaron, Sony, Ziptronix, Tohoku U., MIT, Tokyo U., Besang, and Stanford U.

wafer (W2W) and chip-to-wafer (C2W) devices allow finer connections (therefore higher connectivity) and the device-level integration is performed during the silicon fab process. An example of this is the multi-stacking gates Flash memory from Samsung. Of all these, only memory devices from chip-level, active 3D ICs are in early production, while other more sophisticated integration technologies are in development.

## Considerations for 3D IC products

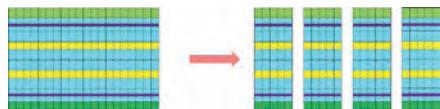
Before taking the leap into 3D IC design, companies need to consider the following:

**Technology availability and risk.** As of today, only a few 3D IC manufacturing

content 3D IC products where the chip-to-chip connection is still through I/Os. In more sophisticated 3D ICs, such as chip partitioning or active 3D IC, the right architecture is one of the keys to success.

**Design enablement.** Designs require multiple chip simulation, placement and routing of libraries from different technologies, as well as verification across chip boundaries. In recent years, EDA tool vendors have begun to provide tools with some of these capabilities, but one needs to be prepared and plan that the tools' EDA vendors are providing may be immature, or even incomplete. In-house solutions may have to be developed and interoperability considered.

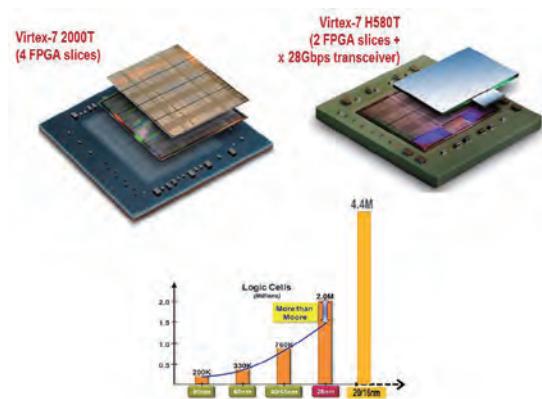
line width/spacing must be in the sub-micron range. **Figure 4** is an illustration of partitioning die in an FPGA.



**Figure 4:** An illustration of Xilinx FPGA die partitioning. Different colors of blocks represent different logic functional blocks (green blocks are giga-bit transceivers, yellow are I/Os, blue are programmable logic dies, and purple are DSPs, etc.).

When TSV and uBump technologies appeared on the horizon circa 2005, we realized that 3D IC architectures could be used for our devices. At the end of 2008, Xilinx began product development (the technology development started in 2006). We had to not only create the chip architecture and design it, but we also had to create new EDA tools to help with the design and verification of the 3D ICs (many of these are available now from commercial EDA vendors). The company also had to create a supply chain to manufacture the dies and interposer, test them, package and assemble them together, and then test the assembled parts. After overcoming all these challenges, the company introduced the 28nm 7 series SSI technology (i.e., passive 3D IC) products in 2011. These devices were shipped and qualified in volume production in 2012 and early 2013, respectively. The Virtex-7 2000T, using 3D technology, has 6.8 billion transistors and the logic capability is 40% larger than a monolithic device can be done in the same 28nm node.

**Figure 5** shows both homogeneous integrated and heterogeneous integrated



**Figure 5:** Xilinx' 28nm 7 series FPGA products using SSI (Stack-Silicon-Interconnect) technology (i.e., passive 3D IC), including both homogeneous and heterogeneous integrated dies. The logic capacity trend chart indicates that 3D IC increases logic capacity more than "regular" node-to-node scaling of Moore's Law.

SSI Technology 7 series products, as well as a logic capacity trend chart for several technology nodes.

## Design attributes for next-generation FPGAs

3D IC technology was applied to a higher percentage of devices in the 20nm UltraScale and 16nm UltraScale+ FPGA families than was the case in the 7 series FPGA family. These next-generation 3D ICs use the company's "Xinterposer," which is a more resilient second-generation interposer. It is actually larger than the optical lithography tool reticle size (33mm x 26mm) and requires photo stitching to manufacture it. We worked closely with TSMC to develop it and to improve its mechanical strength and reliability.

The 20nm VU440 has 4.4 million logic cells (more than double the previous node's largest FPGA), approximately 600,000 uBumps, and 19 billion transistors. It is in 50mm x 50mm and 55mm x 55mm packages, having 2,377 and 2,892 BGA balls, respectively. **Figure 6** shows an UltraScale 3D FPGA VU440.



**Figure 6:** An UltraScale 3D FPGA VU440.

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## Biographies

Xin Wu received his PhD from the U. of California, Berkeley, and is VP at Xilinx; email [xin@xilinx.com](mailto:xin@xilinx.com)

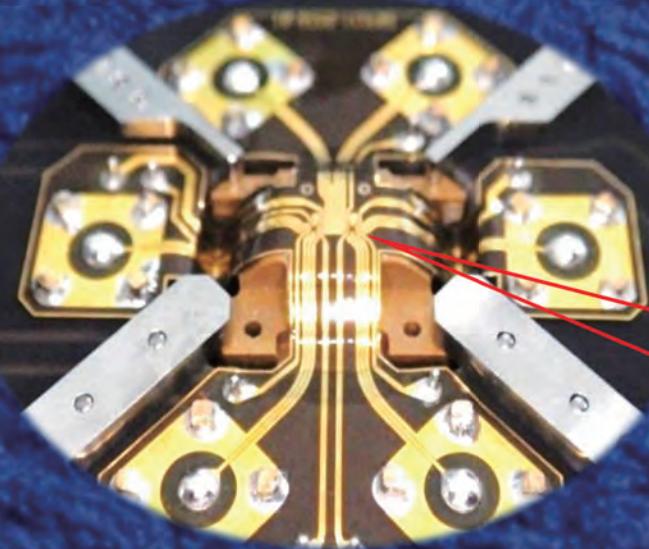
Woon-Seong Kwon received his PhD from Korea Advanced Institute of Science and Technology (KAIST) and is a Principal Engineer at Xilinx.

Suresh Ramalingam received his PhD from the Massachusetts Institute of Technology (MIT) and is a Fellow at Xilinx.

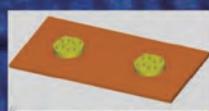
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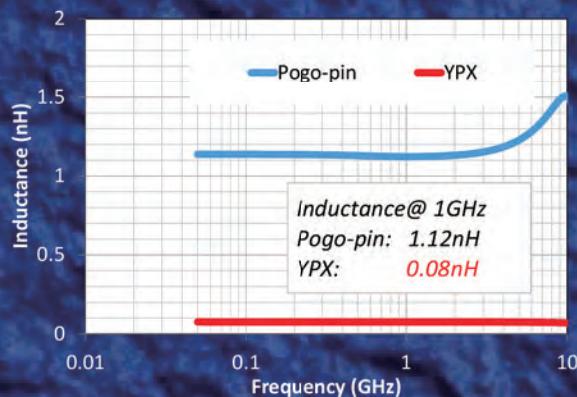
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# Semiconductors and packaging for the Internet of Things

By John H. Lau [ASM Pacific Technology Ltd.]

**M**ost people think that the next big thing after smartphones is the Internet of Things (IoT). The IoT connects devices for applications such as wearables, car, home, health, etc., with other devices to form a global integrated network and is anticipated to create the next technological revolution. In this article, we discuss the key semiconductor devices and their packaging technologies for IoT applications. Emphasis is placed on the 3D CMOS image sensor (CIS) and IC integration and 3D microelectromechanical systems (MEMS) and IC integration for system-in-package (SiP) devices. Trends for these applications will also be presented.

**Figure 1** shows a schematic of IoT devices. It can be seen that these devices connect everything. Not only are there many devices, they are also connected to other things such as wearable electronics, which can be connected to health monitors and to smartphones, which can be

go to creating the “things” (hardware), while 90% go the software connecting these “things” to the internet (e.g., Big Data and cloud computing).

## Semiconductor and packaging for IoT applications

Some of the potential semiconductor applications for IoT devices are as follows:

- 1) Sensors,
- 2) Microcontroller units (MCU),
- 3) Power management ICs (PMIC),
- 4) CMOS image sensors (CIS),
- 5) Memory/embedded flash,
- 6) Microelectromechanical systems (MEMS),
- 7) Fingerprint identification sensors (FIS),
- 8) Radio-frequency identification (RFID)/ RFICs,
- 9) Microprocessors to control the devices,
- 10) Global positioning system (GPS) ICs,
- 11) Wireless (e.g., Bluetooth® and Wi-Fi) connectivity ICs,
- 12) Near-field communication (NFC) connectivity ICs,
- 13) Security for authentication and anti-counterfeiting ICs.

Key drivers for semiconductors for IoT applications are:

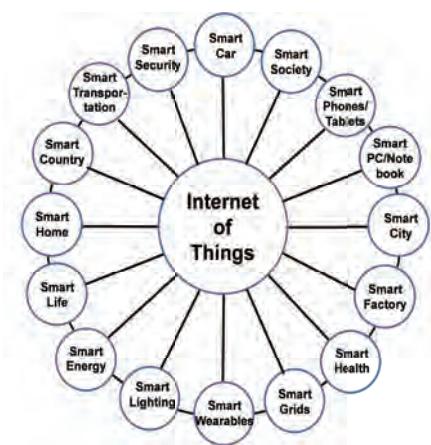
- 1) Cost, cost, cost,
- 2) Ultra low-power (long battery life),
- 3) Small form factor (miniaturization),
- 4) Security and privacy, and
- 5) Low heat dissipation for wearables (touch to the skin).

Most semiconductor products for IoT applications don't need 12" wafers — 8" wafers are more than enough! Also, unlike for smartphones, the process technologies of most semiconductors for IoT applications don't need to go down to 14nm or even 45nm, and even 0.18μm (at most 65nm) is adequate. Furthermore, unlike personal computers, notebooks, smartphones, and tablets that have a very simple product platform and very large manufacturing volumes, the products associated with IoT applications will have more platforms, but smaller manufacturing volumes.

What does this anticipated growth mean to the semiconductor and packaging industry? Most people think that only 10% of the predicted growth (dollar value) will

(miniaturization) system-on-chip (SoC) and SiP. For examples, 1) Broadcom integrated the NFC, Bluetooth®, Wi-Fi, and frequency modulation (FM) into a single connectivity chip; 2) Powerchip Technology integrated the embedded flash memory and ARM-based processor into a single chip; and 3) Intel integrated its 32-bitx86 processor with 80kB static random-access memory (SRAM) and 384kB flash in its Quark SE SoC. On the other hand, Infineon integrated the MCU, a wireless module, a host interface, and the OPTIGA Trust authentication chip into a SiP. (The OPTIGA™ Trust authentication chip is the core of the company's “iBadge” solution for IoT applications. When integrated into smart heating or lighting systems or surveillance cameras, this security chip is used to authenticate those devices that are authorized to access the network.) Also, Apple integrated the application processor, NAND flash, wireless connectivity chip, PMIC, sensors, and some special-purpose chips into a SiP (called S1) for its Apple Watch. Furthermore, Intel integrated the Quark SE SoC MCU, low power DSP, Bluetooth® low energy wireless connectivity, PMIC, and a 6-axes combo sensor with accelerometer and gyroscope MEMS into an SiP (called Curie module) for wearable applications.

In this study, SiPs such as the 3D CIS/IC integration (**Figure 2**) and 3D MEMS/IC integration (**Figure 3**) for IoT applications will be discussed. For 3D CIS/IC integration SiPs, two cases will be considered; 1) the CIS wafer is stacked on top of the logic/processor wafer by wafer-to-wafer (W2W) bonding and connected through TSVs (through-silicon vias) [1-4], and 2) the logic/processor chip is chip-to-wafer (C2W) bonded on the CIS wafer with TSVs. For 3D MEMS/IC integration SiPs, three cases will be considered: 1) the MEMS wafer is bonded on the cap wafer (W2W) with TSVs, 2) the MEMS chip is bonded onto a TSV-interposer wafer (C2W), and 3) the MEMS wafer is bonded on the cap wafer with circuits and TSVs (W2W bonding). It should be pointed out that some SiPs for IoT applications are very simple and can be assembled by surface mount technology and/or wire bonding chip-on-board technology, which are out of the scope of the present study.



**Figure 1:** Internet of Things (IoT).

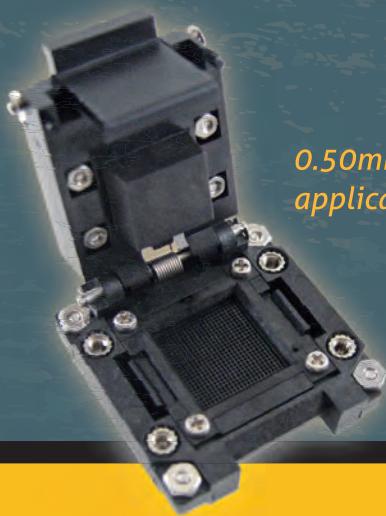
connected to a home network or computer. With 10 billion devices connected today, and 50 billion projected by 2020 according to Cisco Systems, the global IoT market will see an explosive growth. IDC predicts that the global IoT market will grow at a rate of 17.5%, from \$1.9 trillion in 2013, to \$7.1 trillion in 2020.

What does this anticipated growth mean to the semiconductor and packaging industry? Most people think that only 10% of the predicted growth (dollar value) will

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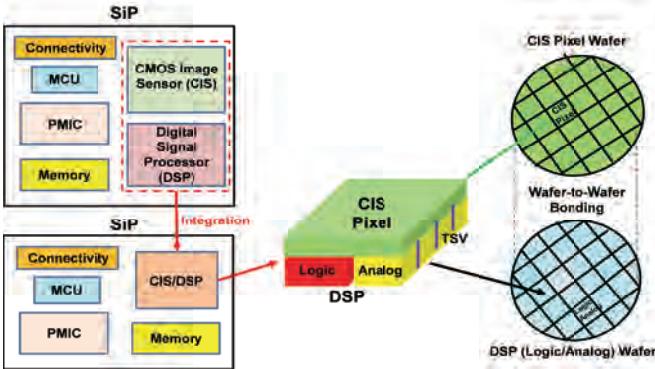


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**Figure 2:** SiP integration of BI-CIS and logic/analog DSP.

### 3D CIS and IC integration SiPs for IoT applications

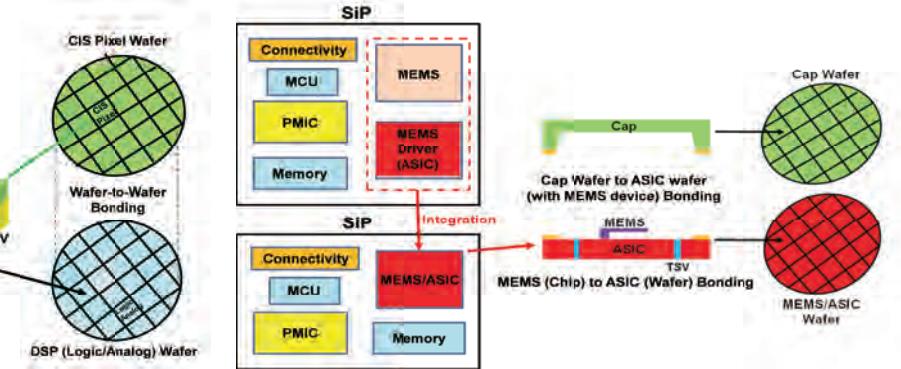
The basic function of a CIS device is to convert light (photons) into electronic signals (electrons). CIS has a huge market with portable, mobile, wearable, and automotive product applications and is a key element of the IoT segment. For example, smartphones and tablets use CISs for cameras, and automobiles use CISs for machine vision. In general, a CIS consists of a matrix of micro lenses, transistors and metal wiring, and a photodiode (PD) [1, 5–10].

There are two different kinds of CIS, namely front-illuminated (FI) CIS and back-illuminated (BI) CIS. For FI-CIS, the matrix of micro lenses is at the front, transistors and metal wiring at the middle, and a PD is at the deep bottom (back) of the wafer surface. The transistors and metal wiring at the surface of the Si substrate reflect some of the light and therefore, the PD can only receive the remainder of the incoming light.

A BI-CIS contains the same elements as an FI-CIS, but instead orients the transistors and metal wiring behind the PD layer by flipping the silicon wafer during manufacturing and then thinning its reverse side so that light can strike the PD layer without passing through the transistors and metal wiring layer.

Compared to FI-CIS, BI-CIS can improve the chance of an input photon captured from about 60% to over 90% [10].

**3D CIS wafer and IC wafer stacking with TSVs.** **Figure 4** shows the 3D stacked BI-CIS device [7]. It consists of two chips, the CIS pixel chip, and the logic circuit chip, and they are vertically connected through TSVs around their edges. The



**Figure 3:** SiP integration of MEMS and an ASIC driver.

advantages of this design are that 1) more pixels can be placed on the same CIS pixel chip size (or a smaller chip size can be used for the same amount of pixels), and 2) the CIS pixel chip and logic chip can be fabricated separately with different process technologies. As a result, the CIS chip size is reduced by 30% and the scaling of the logic circuit chip is increased from 500k gates to 2400k gates [7].

The number of TSVs is on the order of thousands, including vias for signals, power supplies, and grounds. There is no TSV in the pixel array area. The column TSVs are placed in between the comparators on the pixel CIS chip and the counters of the logic circuit chip. The row TSVs are placed in between the row drivers of the CIS chip and the row decoders of the logic chip (**Figure 4**). This arrangement of TSVs can reduce the influence of noise and make it easy to manufacture the CIS chip. For example, to reduce the influence of noise, comparators are arranged on the pixel CIS chip, which can be manufactured by using Sony's mature process technology, rather than on the logic circuit chip.

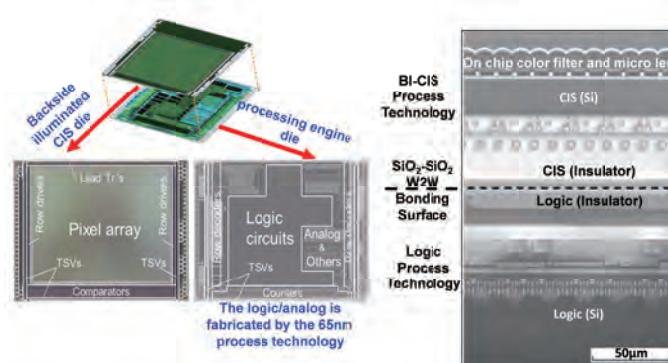
The CIS pixel chip is fabricated using Sony's conventional 1P4M BI-CIS (90nm) process technology. The logic chip is fabricated by the mature 65nm 1P7M logic process technology. The size of the pixel

chip and the logic chip is about the same. The CIS Si-insulator of the CIS wafer is bonded to the logic Si-insulator of the logic wafer ( $\text{SiO}_2$ -to- $\text{SiO}_2$  W2W bonding). The TSVs are then formed and Cu filled after the bonding of the wafers.

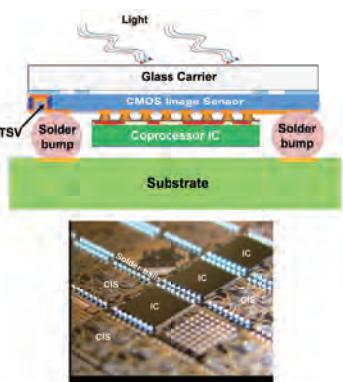
### 3D CIS wafer and IC chip integration.

**Figure 5** shows the 3D CIS and IC integration presented in [9]. It consists of the CIS, coprocessor IC, and glass carrier. The I/O count of the CIS is 80 and that of the IC is 164. The size of the CIS and the coprocessor is not the same and thus W2W bonding is almost impossible. The dimensions of the CIS are  $5 \times 4.4\text{mm}$ , and dimensions of the IC are  $3.4 \times 3.5\text{mm}$ . The IC and the CIS are bonded face-to-back as shown in **Figure 5**. The interconnects of the CIS and IC are Cu-pillar with a SnAg solder cap. The TSVs are in the CIS wafer, which are connected to the substrate with solder bumps. Redistribution layers (RDLs) are in both the CIS and coprocessor IC.

There are at least two ways to perform the final assembly. One is to stack up the coprocessor IC chip to the CIS wafer (C2W) first, and then do the ball mounting of the CIS wafer. The other is to perform the ball mounting on the CIS wafer first, and then perform the IC chip to CIS wafer (C2W) bonding. **Figure 5** shows the 3D prototypes during the assembly process (solder balls



**Figure 4:** Sony's BI-CIS:  $\text{SiO}_2$ -to- $\text{SiO}_2$  W2W bonding of the pixel wafer and logic/analog wafer.



**Figure 5:** STMicroelectronics/Leti's logic chip to CIS wafer (with TSVs) bonding.

done first): mounted IC coprocessors and untreated sites.

#### Trends in 3D CIS and IC integration

**SiP.** The  $\text{SiO}_2\text{-SiO}_2$  (W2W) bonding of the pixel wafer and the logic/analog wafer, then fabrication of TSVs and Cu filling around the chip edges for interconnects (as shown in **Figure 4** and the middle of **Figure 6**) are very high-throughput assembly processes. Recently, W2W hybrid bonding (i.e., when Cu-Cu and  $\text{SiO}_2\text{-SiO}_2$  happen at the same time) as shown at the bottom of **Figure 6** has attracted some attention. The challenge is that for Cu-Cu W2W bonding, the TSV

is usually made before bonding, while for  $\text{SiO}_2\text{-SiO}_2$  W2W bonding, the TSV is usually made after bonding.

#### 3D MEMS and IC integration SiP for IoT applications

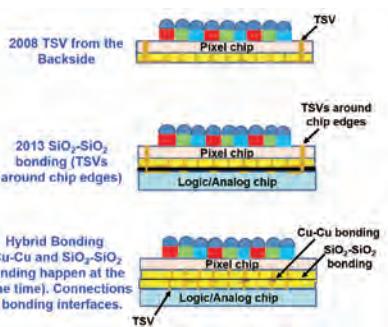
The IoT phenomenon has been called a machine-to-machine (M2M) revolution, and MEMS [4, 11-16] is one of the important groups of machines that will play an essential role in expansion of the boom. For example, MEMS sensors allow equipment to gather and digitize real-world data that can be shared on the internet. IoT application devices promote a major new growth opportunity for the MEMS market.

**RF-MEMS wafer bonded on a cap wafer (W2W) with TSVs.** **Figure 7** schematically shows the zero-level packaging for an RF-MEMS device [13]. It comprises the RF-MEMS, HR-Si substrate with RDLs, and Cu-Sn-Cu for sealing ring and bonding pads, the HR-Si cap with TSVs and RDLs, and the solder bump. One of the main objectives of [13] is to study the bonding characteristics (sealing ring and interconnect bumps) of the MEMS wafer and the cap wafer.

After the fabrication of the sealing ring and interconnect bumps on the cap wafer

in [13], it was found that the average height of the interconnect bump is taller than the sealing ring by  $1\mu\text{m}$ . This uneven height can be planarized by the fly cutting (of the Sn layer) method. First, the cap wafer is coated with a resist layer. Then, a diamond cutting bit moves over the wafer performing a milling type operation, removing all materials with which it comes in contact. The surface flatness can be significantly improved (the average height difference has been reduced to  $0.1\mu\text{m}$ ) and becomes smooth after fly cutting. For the characterization of the MEMS package, please see [13].

**MEMS chip bonded on a TSV-interposer wafer (C2W).** **Figure 8** schematically shows a MEMS package based on an interposer wafer [14]. It can be seen that the MEMS device is bonded to a Si-interposer wafer with Cu-filled TSVs and RDLs (C2W) and is hermetically sealed with a cap wafer with a cavity. This is a 2.5D MEMS/IC integration. A typical cross section image of the final assembly is shown in **Figure 8**. It can be seen that all the key elements of the MEMS package, such as the MEMS device, Si interposer, TSV, microbump, and sealing ring, are in proper position.

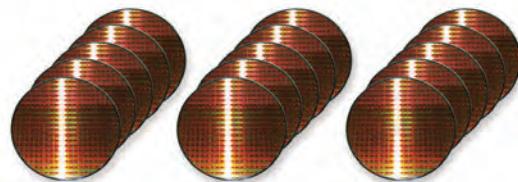


**Figure 6:** Trends in the Bi-CIS semiconductor and packaging assembly process.

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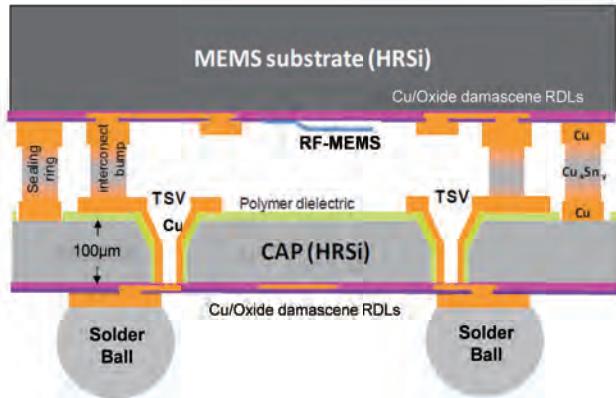
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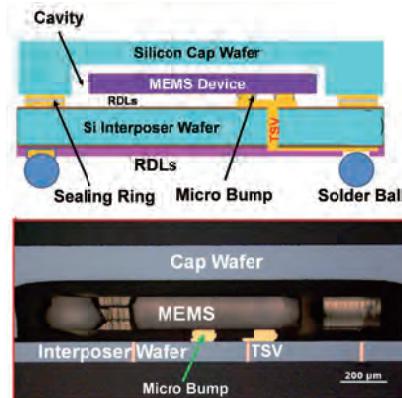
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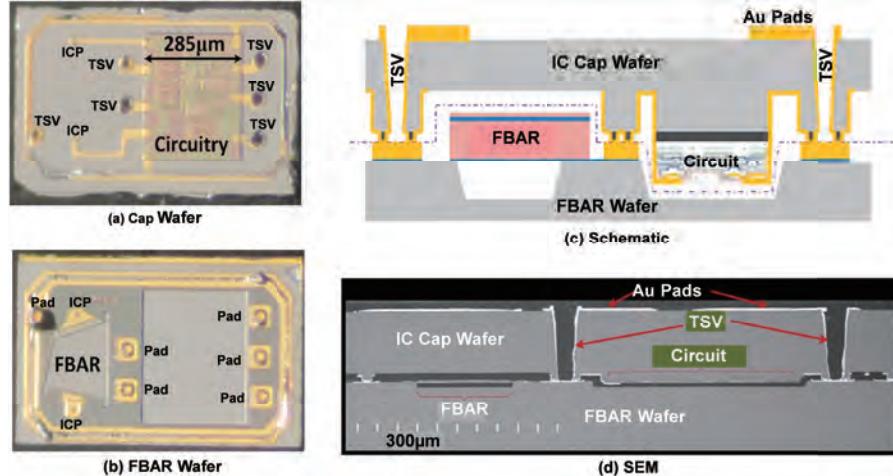
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**Figure 7:** Imec's cap wafer with TSVs to MEMS wafer bonding.



**Figure 8:** IZM's MEMS device (chip) to TSV interposer wafer bonding.



**Figure 9:** Avago's cap wafer with circuits and TSVs to FBAR (MEMS) wafer bonding.

For the characterization of the MEMS package, please see [14].

**MEMS wafer bonded on the cap wafer with circuits and TSVs (W2W).** **Figure 9** shows the wafer-scale packaging for film bulk acoustic resonator (FBAR)-based oscillators [15, 16]. **Figure 9a** shows the cap wafer (upper part) of the package. It can be seen that there is an IC device ( $330\mu\text{m} \times 285\mu\text{m}$ ), six TSVs for external connection, two internal connections (ICP), and a small cavity for the FBAR. **Figure 9b** shows the FBAR wafer (lower part) of the package. It can be seen that there is an FBAR, six external pads (for those six TSVs), two internal connections (from the cap electronics to the FBAR), and a cavity (for the IC device). This is a real 3D MEMS and IC integration (very similar to Case 10 of Figure 11 in [11, 12]). Both the FBAR and cap wafers are high-impedance Si to minimize cross talk and capacitive losses.

The Au-Au diffusion bonding of the cap wafer with the IC device and TSVs and the FBAR wafer is schematically shown at the top of **Figure 9c**. The cross section

SEM (scanning electron microscope) image of the bonded package is shown in the bottom of **Figure 9d**. It can be seen that all the key elements such as the FBAR, IC device TSVs, cap, sealing ring, and pad, are in proper position. For detailed characterization and mechanical and electrical performances, please read [16].

**Trends in 3D MEMS and IC integration SiP.** Avago's MEMS wafer bonded on the cap wafer with IC and TSVs is a real 3D MEMS and IC integration SiP, and is the right way to go. However, it only works for a vertically integrated company, which has the MEMS device and the IC cap. On the other hand, the 3D IC MEMS and IC integration SiP shown in **Figure 3** can be a next-to-the-best candidate. In that case, someone can buy the MEMS device and bond it to the ASIC wafer with TSVs (C2W) followed by W2W bonding of the cap wafer to the ASIC wafer with the MEMS device. Of course, in the latter case, the MEMS and ASIC can be integrated onto an SoC wafer, which can be W2W bonded onto the cap wafer. Again, the drawback is losing the flexibility.

## Summary

Semiconductor and packaging for IoT devices have been presented in this study. Some important results and recommendations are as follows:

- 1) A list of potential semiconductors for IoT applications has been provided. Some of the drivers of semiconductor technologies for IoT applications have also been given;

- 2) The process technology for most semiconductors for IoT applications doesn't need to be very advanced—65nm is adequate. Also, the wafer size doesn't need to be 12"–8" is enough;

- 3) Unlike personal computers and smartphones, the product platform of most IoT devices is more and its volume is less;

- 4) The key innovation of semiconductor and packaging for IoT devices is to integrate some of the semiconductors into miniaturized SoCs and SiPs;

- 5)  $\text{SiO}_2\text{-SiO}_2$  (W2W) bonding of the pixel wafer and the logic/analog wafer, then TSV fabrication and Cu filling along the chip edges for 3D CIS and IC integration SiP is a very high-throughput assembly process;

- 6) More R&D activities should be done on hybrid bonding for 3D CIS and IC integration SiP, especially on making the TSVs, because most TSVs are made before Cu-Cu bonding and after  $\text{SiO}_2\text{-SiO}_2$  bonding; and

- 7) A MEMS wafer bonded onto the cap wafer with an IC and TSVs is a real 3D MEMS and IC integration SiP and is the right way to go. Unfortunately, this only happens in a vertically integrated company. The next best thing is to bond the MEMS device to the ASIC wafer with TSVs, and then bond the ASIC wafer with the MEMS device to the cap wafer as suggested, for example, in **Figure 3** and [11, 12].

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# GaN-on-Si CSP LEDs

By Zainul Fiteri [Plessey Semiconductors]

The next wave in solid-state lighting will be realized with LEDs that are distinctly different from the majority of LEDs shipping today. The technologies driving this change will be a shift in the die technology to a GaN LED structure grown on Si substrates, and then exploiting that Si interface in new formats based on the chip-scale package (CSP) and wafer-level packaging (WLP) techniques commonly used in today's semiconductor IC industries. This article explains our approach to CSP LEDs, the resulting benefits, and some of the challenges ahead in these developments.

## Background

Today the majority of LEDs are supplied in surface-mount plastic leadless chip carrier (PLCC) packages. A multi-billion piece per year supply chain has grown rapidly over the past few years that has driven down the cost and increased the market penetration of LEDs. From being mainly used in backlighting applications (TV, monitors, mobile phones), PLCC LEDs are now common-place in all sorts of consumer and industrial lighting applications. The PLCC packages are commonly named by their footprint: 3020, 5630 and 3030 are three of the most common standards. For example, the 3020 version relates to a 3.0 x 2.0mm footprint. This convention has enabled a level of standardization across the industry, allowing customers to easily switch between vendors without any printed circuit board (PCB) re-design. This level of commoditization has been an essential part of the volume growth for LEDs and has to be repeated if CSP is to become the future standard for high-volume LED supply.

## The problem with PLCC

As with most first-generation surface-mount packages, the principal issue is the real estate utilization, expressed as the ratio of the active die size to PCB footprint. This ratio for typical LED PLCC products today is at the level of just 2%. With the introduction

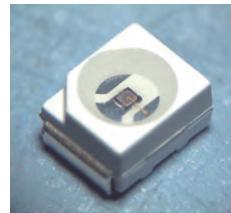
of first-generation CSP, this utilization will leap to the 30% level, opening up a host of new application design opportunities.

At first sight, LED PLCC packages appear to be similar to low cost discrete semiconductor packages, but in fact, there is more to them than meets the eye. The internal construction of PLCC packages includes a shaped cavity that acts as a reflector that directs the light upwards through the phosphor/silicone. This construction is needed as the vast majority of LED die are manufactured using sapphire substrates, and as sapphire is transparent, the light is scattered in all directions and the PLCC-type package age is required.

**Figure 1** shows a PLCC package.

## The GaN-on-Si factor

Plessey LED die utilize the company's GaN-on-Si technology platform. The migration of LEDs from high-cost sapphire substrates to large diameter, low-cost silicon substrates is well-documented elsewhere, but a few aspects and benefits related to the CSP perspective need to be restated to highlight its main advantages.



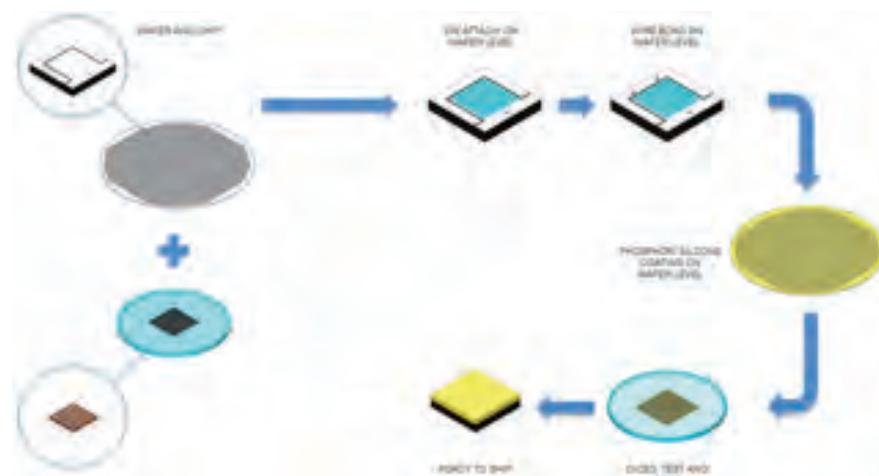
**Figure 1:** A PLCC package.

The principal difference between silicon and sapphire are the optical properties: silicon is opaque, whereas sapphire is transparent in the visible spectrum. This means that, for a GaN-on-sapphire LED, the light is scattered in all directions, but a GaN-on-Si LED produces a single-surface emitter. Therefore, GaN-on-Si LEDs do not require a special reflector package to redirect the scattered light, the single-surface emission properties thereby being ideally suited to minimal packaging, such as CSP concepts.

## CSP: first-generation concept, construction

Our approach to CSP was to find a format that would be a best fit to supplement the inherent benefits of the existing GaN-on-Si LED die design. There are three key aspects to consider going from die to a complete CSP LED product: 1) Mounting, 2) The cathode contact, and 3) Phosphor coating. **Figure 2** shows the first-generation CSP construction flow.

For the mounting, the aim is to deliver a solution that provides good thermal conductivity, at low cost, that also meets the expectation for an operating life measured in decades. For this, we need look no further than silicon itself. To state the obvious, we know there will be no thermal mismatch



**Figure 2:** First-generation CSP construction flow.

between the GaN-on-Si die and the Si mounting, and as a material, it is fully understood following over fifty years of use in the semiconductor industry. To optimize the electrical connectivity, the construction uses copper through-silicon/wafer vias (TSV or TWV). From a purely academic perspective, we concede that this construction makes few claims in terms of innovation, but for exacting cost and reliability requirements a “proudly invented elsewhere” approach is often the best chance for commercial success.

Although the mount and via solution does not break new academic ground, it does represent considered engineering in the selection of materials, design and implementation. The benefits of mounting Si to Si have to be preserved in the interfaces and attach method. For the best electrical performance, the vias used will be 100 $\mu\text{m}$  in diameter and Cu-filled. As Si is also a conducting material, the vias are isolated from the bulk mount with a SiO<sub>2</sub> passivation. At present, the CSP LEDs are only single-junction variants so the level of voltage isolation is not exacting. In the construction of the vias, the size and depth of the via is more of a manufacturing challenge: 300 $\mu\text{m}$  from top to bottom through the Si mount. At each end of the via there is a deposited 20 $\mu\text{m}$  Cu bond pad, with a 3 $\mu\text{m}$  Ni-Au plating. The active LED die is connected to the Si mount using conductive epoxy. This selection of materials and design makes no compromise on the zero hour performance of the LED, and also provides a balanced construction that maintains this level of performance through the many hours of operation and thermal cycling that the LED will experience over decades of operating life.

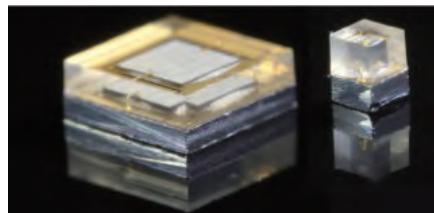
Our existing GaN-on-Si die are of a vertical design: cathode top contact and anode bottom contact. To apply this die design to CSP, we need to make a contact from the top surface cathode bond pad to the mount linking to the TSV for a bottom contact in the finished LED. In the first-generation this contact will be made with a standard wire bond.

Finally, the phosphor or silicone coating is applied. For general lighting applications, LEDs are usually white in color. The most efficient white light is produced by phosphor conversion of blue light emitted from an LED die. Phosphor deposition is the last LED process to become automated and in the last few years, various techniques of producing repeatable and stable phosphor on die (PoD) have been realized. Our

CSP LEDs will take advantage of such a technique to make a flat finish phosphor coating to produce an LED with a near Lambertian light distribution.

The smallest version CSP, which is 0.55 x 0.55mm, will require a reduced diameter TSV in the Si mount. These new vias will be 60 $\mu\text{m}$  in diameter, and will also have a complete Cu fill. It is expected that making a reliable and repeatable 300 $\mu\text{m}$  x 60 $\mu\text{m}$  vias in high-volume production will present a few sleepless nights for the manufacturing line, but nothing more than that!

The first two examples of products manufactured with this process flow will be a 350mA LED with a 2.0 x 2.0mm footprint, and a 20mA version with a 0.55 x 0.55mm footprint. These LEDs will have an active die to footprint ratio of 30%, or an increase in brightness (cd/m<sup>2</sup>) of 10x when compared like-for-like with a PLCC equivalent. **Figure 3** shows CSP prototypes of 2mm X 2mm and 0.55mm X 0.5mm. Although



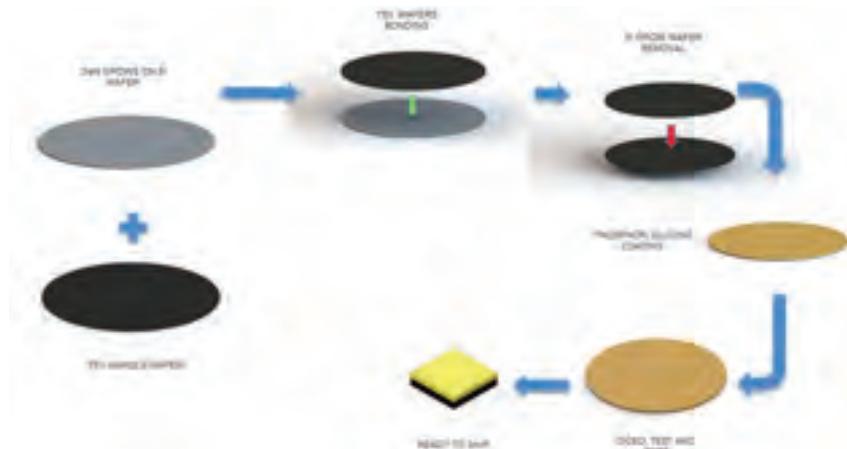
**Figure 3:** CSP prototypes of 2mm X 2mm and 0.55mm X 0.5mm.

this will trigger a major change in how LEDs are experienced from the customer perspective, the technical challenges from the supplier perspective are within reach. The next phases will see little change in the external appearance, but involve considerably more effort in development.

## Next-generation CSP: to 95% footprint utilization

The removal of the cathode contact bond wire is the key element in driving the footprint utilization to something approaching the ideal 100%. As mentioned previously, GaN-on-Si die have a vertical structure, with the die substrate forming the live anode contact and a top surface bond pad for the cathode. To achieve a bond wire-free, true CSP LED product or WLCSP, the GaN architecture design has to go through a fundamental change in the structure to one with two lateral contacts. This change in structure will be realized with TWVs. This technique has been achieved, but for an LED structure, this still represents a significant challenge to achieve while keeping the key performance parameters for the LED intact. One major obstacle will be the change in the bulk Si substrate from being a single anode contact to a distributed anode and cathode contact by utilizing a TSV wafer. Simulation results predict we can achieve this with negligible impact to the electrical or thermal performance. The design options are identified and the process development phase will continue through 2015 with the goal of establishing a process that delivers in terms of performance, yield and cost.

The implementation of TWVs in GaN-on-Si with two bottom contacts will enable true CSP (WLCSP) with a significant reduction in assembly process steps in conjunction with increased throughput. This will remove the need for any additional real estate on the Si mount and, in principle, lead to the ideal footprint utilization. In practice, for mechanical handling and optimum phosphor coverage, the maximum achieved in commercial products for a single LED will likely be 95%.



**Figure 4:** Next-generation CSP construction flow.

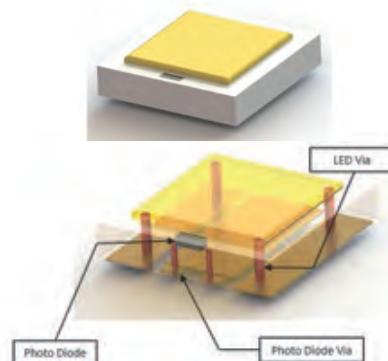
Finally, a wafer-on-wafer attach will be explored, whereby the GaN-on-Si LED wafer will be attached directly to the Si mounting wafer. This technique would remove one of the singulation stages and lead to something of an end game for the optimum construction for LEDs sold in billions of pieces per month. This also is one of the major advantages of GaN-on-Si with its surface emitting characteristic over volume emitting. For a surface emitting chip, wafer-level assembly can be achieved throughout the process steps. Volume emitting has to go through a lengthy process to prevent blue light leakage from the chip side walls after being singulated. **Figure 4** shows the next-generation of CSP construction flow.

#### From CSP to WLP and future integration

Another reason for not having a full footprint utilization is to develop functional integration into a CSP LED product. In this phase of development, the Si mount wafer progresses from a simple means of making electrical and thermal contact, to a “value add” addition to a simple LED. At the lowest level, the “value add” could be the integration of a protection diode or photo-diode. Additionally, the integration possibilities using a Si mount are endless—it could well lead to the integration of control and drive circuitry. With this kind of functional integration, it is easy to see how a simple CSP LED then evolves into a chip-on-wafer (CoW) product with few technical hurdles. **Figure 5** shows construction of an integrated CSP.

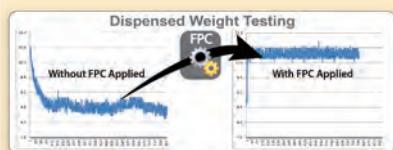
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**Figure 5:** Construction of an integrated CSP.

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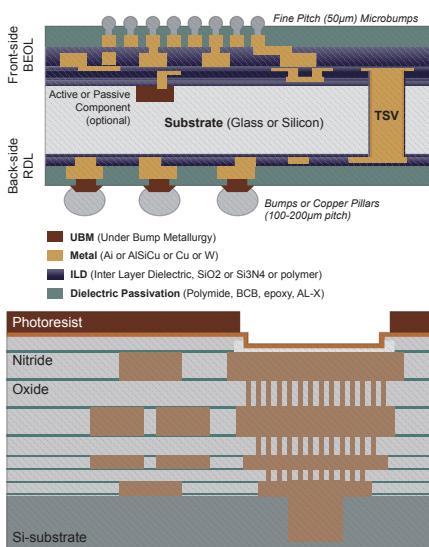
# In-line process monitoring of advanced packaging processes using focused beam ellipsometry

By Jay Chen, Jian Ding [Rudolph Technologies, Inc.] and Parker Huang [SPIL]

Demand for small form factor devices with a high level of integrated computing power and reduced power consumption continues to drive the consumer electronics market. Meeting this demand requires short, high-density interconnections between high-capacity memory chips and microprocessor units. Advanced packaging schemes during design and development need to take into consideration both the device and the package to create synergy between the two in performance, cost and reliability. Silicon interposers for 2.5D and 3D IC stacking have gained traction as a viable solution for higher interconnect density, smaller form factor, reduced power consumption, and increased bandwidth.

2.5D interposers are evolving in two distinct categories depending on their source of fabrication. The finer pitched high-density versions have traditionally been manufactured by foundries using dual damascene technologies, while those with lower density and coarser features were manufactured by the assembly houses using their redistribution layer (RDL) technology (Figure 1). Recently, outsourced semiconductor assembly and test providers (OSATs) have acquired the capability to process some of these high-density interposers and are able to accept wafers from multiple sources, fabricate interposers, and perform assembly and test.

With the increasing complexity of the process and tighter specifications come the need for better process characterization and control. OSATs have traditionally relied on manual table-top systems or semi-automated tools, such as reflectometry, for process characterization. They have also used cross section microscopy in select cases to verify the accuracy of the measurements. More accurate characterization of these films, including the measurement of thicknesses and optical constants on single and multi-layer stacks on blanket and product wafers, requires an automated metrology solution. In addition to film thickness, the ability to simultaneously measure film stress and wafer bow on a single



**Figure 1:** Schematic of a) Interposer technology, b) Photoresist patterning to define UBM area. Focused beam ellipsometry measures photoresists, ILD layers, and dielectric passivation layers at various process steps. Sources: Yole, IME.

platform can provide critical information regarding the mechanical integrity of a package as the devices are stacked [1-4].

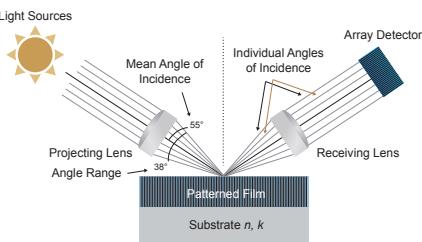
Here, we discuss the adoption of Rudolph's fully-automated focused beam ellipsometry (FBE) system to meet current 2.5 and 3D IC metrology needs and to enable a seamless transfer to high-volume production. We now use this technology routinely to measure dielectric layers of oxide/nitride stacks, thick photoresists, and polymers on glass substrates at post-deposition, post-etch, pre-and post-CMP process during redistribution layer (RDL), under bump metallization (UBM), and micro bump formation. We show here selected examples from various process steps.

We also discuss feed-forward metrology, a concept that has gained widespread attention and acceptance in front-end semiconductor manufacturing for improving measurement accuracy in complex multi-layer, multi-parameter film stacks. We demonstrate the application of this concept for multi-layer dielectric stack

measurements and its potential advantage during both R&D and in-line monitoring.

## Focused beam ellipsometry

Focused beam ellipsometry (FBE) provides a simultaneous measurement of ellipsometric parameters, Delta and Psi, within a range of incidence angles from 45 to 65 degrees, at a discrete set of wavelengths: 633nm, 784nm, and 923nm. Simultaneous, multi-angle measurement is achieved by focusing a collimated beam to a 15µm spot onto the sample using a projecting lens and collecting reflected light with the similar lens focused at the same spot. **Figure 2** shows the FBE implementation. Deep ultraviolet



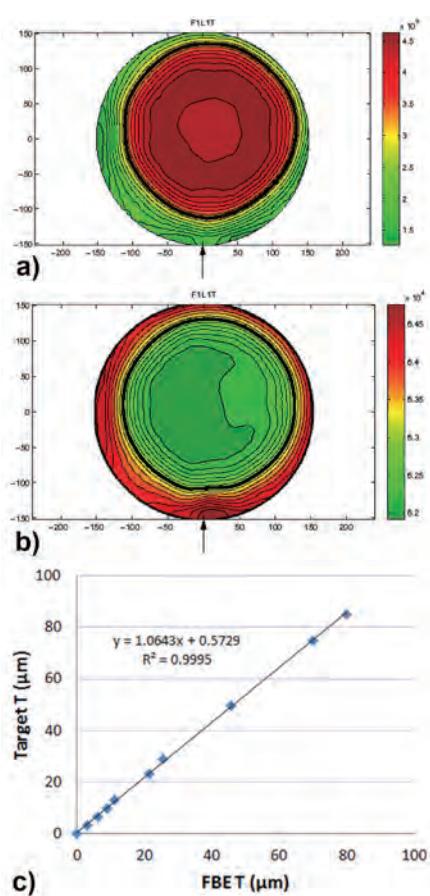
**Figure 2:** Schematic representation of the FBE system. Deep UV reflectometer and visible reflectometer options are not shown.

(193nm-400nm) and visible (400nm-900nm) reflectometry are available options and are particularly useful in characterizing multi-layer films and when optical constants are required at lithographic wavelengths. Depending on the film and parameter of interest, any combination of these technologies can be used.

## Characterization of thick photoresist

Improving package reliability requires high aspect ratio interconnects to provide higher stand-off between the chip and the substrate, hence the need for thick photoresists. Thick photoresists are used to define the size and location of the bond for advanced packaging. They also help realize high-density metal structures for applications such as copper pillars and bump plating. Spin-on deposition of the resists, before process optimization, results in significant thickness variation

across the wafer. Characterizing thickness uniformity across the wafer (to 3mm edge exclusion) allows for process optimization. We measured films ranging in thickness from 5 $\mu\text{m}$ - 90 $\mu\text{m}$ . Within-wafer uniformity profiles from 45 $\mu\text{m}$  and 6 $\mu\text{m}$  films are shown in **Figure 3**, and **Table 1** summarizes the statistics. Also, **Figure 3c** shows the linear correlation obtained between the FBE measurements and target thickness. Repeatability ( $3\sigma$ ) of the measurements is typically  $<0.15\%$ . Measurements are rapid and take less than 2s per site, delivering full wafer maps and line scan measurements in minutes to provide complete information.



**Figure 3:** 49pt within-wafer uniformity profiles are shown for a) 45 $\mu\text{m}$  and b) 6 $\mu\text{m}$  resist wafer; c) Correlation between reference metrology thickness and FBE thickness across the process range.

### Characterization of polymers on glass

Thin polymer films find applications as permanent dielectrics, in which case they remain in components and serve as insulators and as release layers. During the temporary bonding process, the polymer acts as a release layer to bond with the adhesive of the silicon substrate. Monitoring the thickness uniformity

of the polymer on glass substrate is a critical process in the fab. A polymeric film with poor thickness uniformity will lead to issues during subsequent processing. Prior to the use of FBE, there were no other methods available in the fab to robustly measure

|                                | 6 $\mu\text{m}$ resist film | 45 $\mu\text{m}$ resist film |
|--------------------------------|-----------------------------|------------------------------|
| Wafer Center ( $\mu\text{m}$ ) | 45.7                        | 6.2                          |
| Range ( $\mu\text{m}$ )        | 28.4                        | 0.2                          |
| 1 Sigma Std Dev (%)            | 35                          | 1.65                         |

**Table 1:** Within-wafer range and standard deviation are shown for a 6 $\mu\text{m}$  resist film. Within-wafer non-uniformity is  $\sim 1.65\%$ . Within-wafer range and standard deviation are shown for a 45 $\mu\text{m}$  resist film. For thicker films, the non-uniformity (35%) is significant. Having the thickness information for the whole wafer allows for process optimization and validating improvements.

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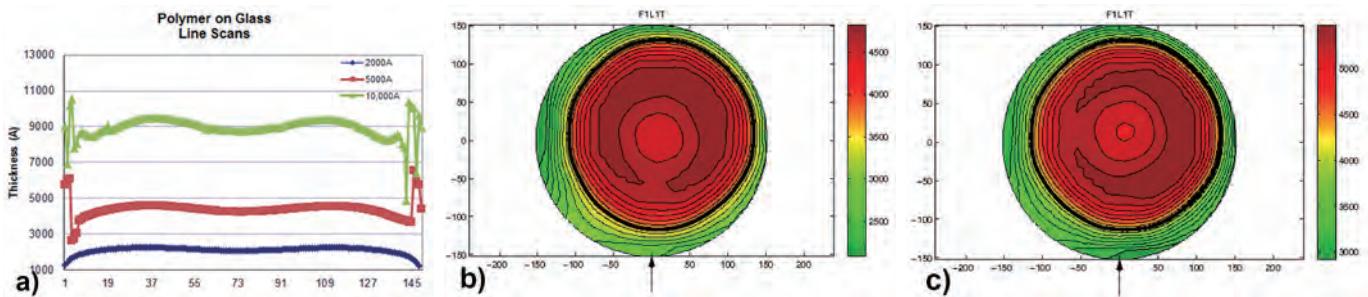
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**Figure 4:** a) High-resolution line scans across the polymer films (2000Å-1μm) on glass substrates. Profiles show the within-wafer thickness variations, especially at the edge of the wafers on some of the films; b) and c) Within-wafer uniformity profiles of a 5000Å film on glass and silicon, substrates, respectively.

these films. **Figure 4** shows high-resolution line scans of films ranging in thickness from 2000Å to 1μm. As the films get thicker, more variation is apparent at the very edges of the wafer. **Figure 4b and c** show 49-point within-wafer uniformity profiles of a 5000Å film on glass and silicon substrates, respectively. The profiles are very similar and the within-wafer range is ~2200Å.

#### Characterization of oxide/nitride/oxide stacks

As discussed earlier, the growing complexity of the devices and the increasing

requirement of high-density routing and fine-pitch interconnections have led to investigations in the RDL and passivation layers [4]. Fine-pitch RDL can be realized in two ways, either as a damascene integration similar to what is used in front-end fabs during BEOL processing, or the conventional RDL integration that is used in packaging houses. The damascene approach is an attractive option as it allows access to sub-micron line/space widths and is now possible at OSATs. Using this approach, we have achieved high-density interposers (1μm L/S, 10μm TSV). To evaluate the capability of the

FBE tool in these applications we looked at dielectric film stacks of oxide/nitride/oxide/nitride/oxide/nitride/oxide. In the following paragraphs, we describe two different approaches that are available for measuring these types of stacks.

The first approach is a feed-forward approach (**Figure 5a**), where the wafer, using LOT and wafer ID is tracked through the process flow and measured at every step. During runtime, thickness measured from the previous process step can be either retrieved from the tool (tool-centric solution) or obtained from a server (server-centric solution, shown in

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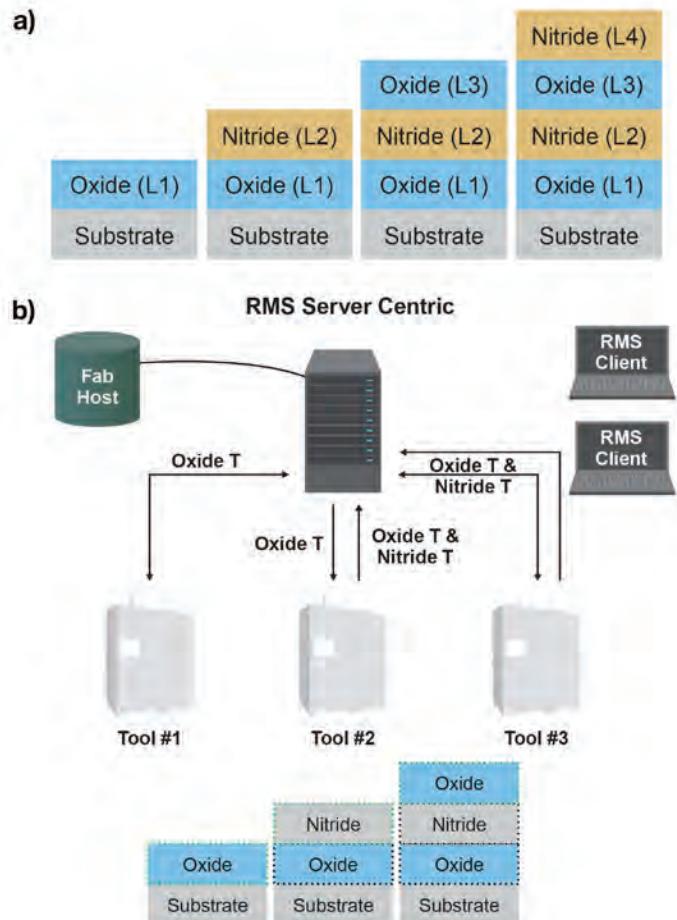
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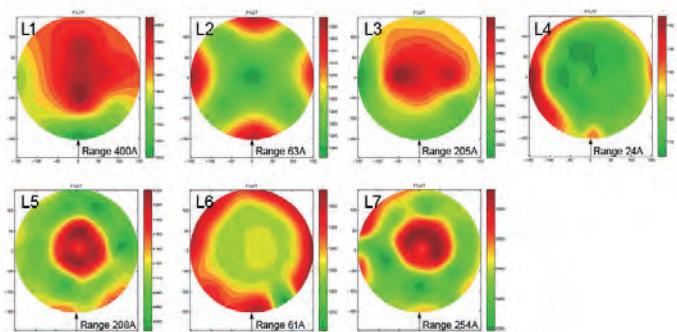
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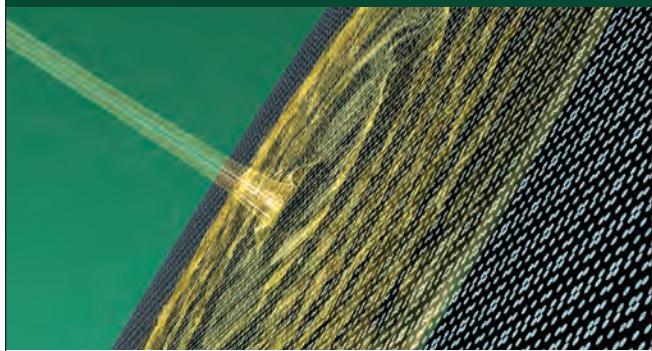
**Figure 5:** a). Schematic sketch of the multi-layer stack for feed-forward metrology; b). Illustration of a host-centric solution for a fleet of tools in high-volume manufacturing.

**Figure 5b).** **Figure 5a** shows part of the process flow for an ONONONO stack. For example, during measurement of the nitride layer (L2), thickness of oxide (L1) is downloaded from the server, and this input is used by the modeling engine. This approach is more robust than using an assumed value for the layer based on the target thickness, as it represents the actual thickness variation of the oxide, and the nitride thickness calculated in this manner is more accurate. An additional advantage of the feed-forward approach is that the measurement accuracy and repeatability are comparable to single-layer performance.

**Figure 6** shows the wafer uniformity profiles obtained using a feed-forward approach. The FBE tools, by virtue of the technology and the



**Figure 6:** Within-wafer uniformity profiles of ONONONO stack using the feed-forward approach.



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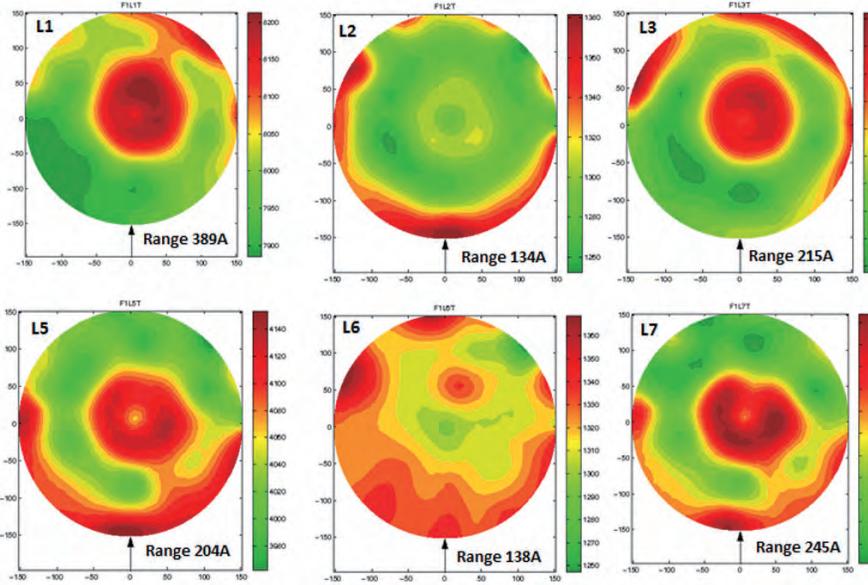
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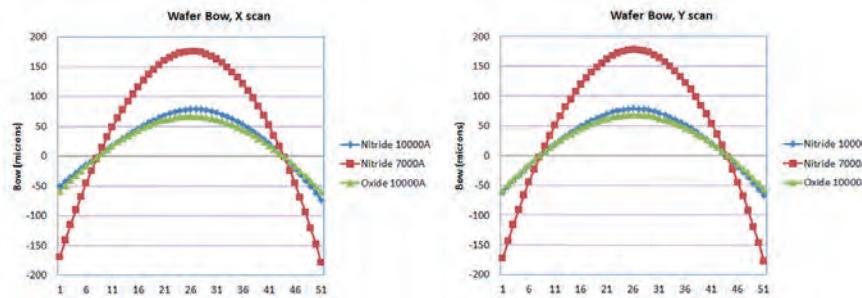
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**Figure 7:** Within-wafer uniformity profiles of ONONONO stack. Thickness is reported from all layers, except layer 4 (thinner nitride), which was fixed in the model.



**Figure 8:** X scan and Y scan profiles showing the wafer bow on nitride and oxide single-layer blanket wafers.

|         | Thickness (Å) | Stress (MPa) |
|---------|---------------|--------------|
| Nitride | 9897          | -198.18      |
| Nitride | 7396          | -685.26      |
| Oxide   | 10068         | -177.01      |

**Table 2:** Wafer thickness and stress calculated on the nitride and oxide single-layer blanket wafers.

stable laser light source, lend themselves to excellent intrinsic matching. In a high-volume manufacturing facility, this allows the wafer to be routed to any of the available tools in the fleet, without requiring wafers to be sent to the same tool.

A second approach to film stack measurement, which measures all the layers simultaneously, is appropriate for processes where it is not possible to measure after every deposition. Because of the nature of the materials involved, we report the thickness of six of the layers in the seven-layer stack (**Figure 7**). No attempt is made to compare the profiles directly as the wafers

were different. Comparison of within-wafer range is shown so the reader can appreciate the difference between the approaches. Thickness range from within-wafer profiles, in general, is slightly worse compared to the feed-forward approach, and also one of the layers (layer 4, 700 Å nitride) is fixed in the model to improve the accuracy of the other layers. Depending on the process flow, tolerances and requirements, either one of these approaches can be easily adopted.

### Characterization of wafer bow

Interlayer dielectric film stress measurement results, summarized in **Figure 8** and **Table 2**, help OSATs monitor the mechanical integrity of the process during development and ensure yield at volume manufacturing. Oxide and nitride film thickness and bow were determined

by performing line scans in both x and y directions, which were subsequently used in the stress calculation.

### Summary

Development of advanced packaging techniques at OSATs and the growing complexity of the process require more automated and advanced metrology techniques. FBE is used extensively in film characterization in both front-end-of-line (FEOL) and back-end-of-line (BEOL) in wafer fabs and foundries. This paper has described the adoption of this technology for measurements of dielectric films during various stages of process development and optimization in advanced packaging. The fully automated measurements are non-contact, nondestructive and provide the ability to characterize the full wafer at production-worthy throughputs. The small spot enables measurements on product wafers and is suitable for in-line monitoring. We introduce the feed-forward concept as a viable option for characterizing multi-layer film stacks on account of its intrinsic matching capabilities for the fleet.

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# 3D thermal simulation in the IC design flow

By John Parry [Mentor Graphics Corporation]

**D**esigning a large high-power die, such as a system-on-chip (SoC), without considering how to get the heat out is likely to lead to a packaging solution that doesn't have optimal cost, size, weight, and performance. In the past, IC designers have treated the die temperature as if it was uniform. But heating caused by current leakage, which is temperature dependent, is making power dissipation less uniform, and the use of thinner die, now well below 50 $\mu$ m, has reduced the heat spreading capability of the die.

When designing stacked 3D ICs, the die cannot be designed independently because of their electrical and thermal interaction. Through-silicon vias (TSVs) that act as inter-die interconnections can help remove heat from the die stack. Because they reduce hot spots, their placement relative to high-power regions on the die can affect overall thermal performance.

This kind of work is best done within the IC design flow, which means that co-designing – mechanically, electrically, and thermally – is essential. Today's IC design and thermal simulation tools allow fast and accurate thermal simulation of dies and interposers for 3D ICs to be done concurrently while designing the IC package (**Figure 1**).

The solution described in this article uses die power map files that can be generated by power analysis tools and enables creation of thermal maps that can be used for thermal design and for checking against thermal constraints. The advantage to this method is that more accurate thermal models of dies that take into account the metallization, such as interconnects and TSV in the dies, can be created and used in thermal simulation. Additionally, a 3D IC thermal model can be created for further thermal simulation at the system level.

## IC thermal design starts with the package

The package construction must be included in the thermal model to obtain the correct temperature distribution inside the die. It should be represented as mounted on a typical PCB and a heat sink solution represented if needed, so that the effects of heat spreading in the board and into the heat sink are accounted for in the predicted package temperature distribution. For correctly predicting the way the package interacts thermally with its environment

## Thermal design early for optimal performance

The best opportunity for optimizing the chip-package architecture is in early design and before the detailed IC design starts. At this stage, the number of die, as well as the intended size and budgeted power for each die, are known. This information can be used to create a 3D thermal conduction model of the candidate packages, or package variants, which can be used to explore the package design space. It could also include convection and radiation if the package style includes an internal cavity. The model also provides the thermal environment that will allow temperature data to be back-annotated to the IC design flow.

The thermal model of the candidate packages can be used to investigate the influence on the thermal performance of different die arrangements, package size, and packaging materials, such as the amount of copper in the substrate for a ball grid array package.

At the early design stage, there is a high degree of freedom and opportunity to explore different package options

and their design. Based on an initial estimate for the size of the die, design parameters that can be investigated to determine their influence on the die temperature rise and variation for a given package style may include: 1) The influence of the number and possible layout of TSVs; 2) Influence of the size, shape, and material choices for an interposer; 3) Effect of interfacial resistances (glue layers); 4) Pyramid vs. overhang stack arrangements (if wire bonded); 5) Cooling solutions internal to the package, for example, die edge cooling, internal heat slugs, etc.; 6) Influence of external cooling solutions, for example, solder pads, underfill options etc.

Features that have the greatest effect on die temperature rise and variation need to be modeled in greater detail and optimized for thermal performance. Temperature ranges across the die are likely to be too

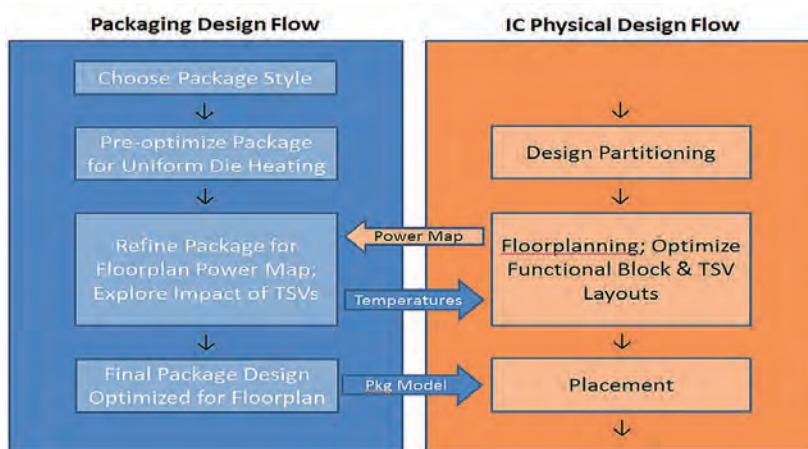


Figure 1: Opportunity for parallel package and IC physical design flows [1].

and the correct temperature distribution within the package, 3D computational fluid dynamics (CFD) simulation is needed.

Simply applying a constant thermal resistance value to each surface of the die to represent the heat flow path to the ambient is insufficient to use as a boundary condition. A high resistance to the ambient does not capture any local heat spreading effects because of the presence of high thermal conductivity materials in close thermal contact with the die. These tend to hold the die temperature uniform without contributing significantly to the total thermal resistance to the ambient. Using a single thermal resistance value may lead to overdesigning and possibly incorrect decisions.

high to assume a single thermal conductivity value, so temperature-dependent thermal conductivities are necessary to accurately predict hot spots on the die. For transient calculations, the material density and specific heat capacity need to be included.

### Creating a model for the thermally active layers

To create a model for thermally active layers, one needs to use a 3D representation of the active layers of the die (metallization and polysilicon) with an isotropic block ~0.5 to 1.0 $\mu$ m thick. Silicon dioxide ( $\text{SiO}_2$ ) and silicate glass are typically used as dielectric materials to separate metal wires on the active surface of the die and have thermal conductivities on the order of 1W/mK. This value is around two orders of magnitude less than the metal they isolate, which historically has been aluminum or copper.

Wires on different levels run in different directions so the material behavior is locally orthotropic. However, the high level of interconnection between the levels, combined with metal running in different directions, causes the heat to smear. For early design activities outside the main IC design flow, the bulk behavior can be approximated with an isotropic material with all the active surface layers captured within the thickness of one mesh cell in the package-level model.

The IC process and design technology files contain information about metal width and spacing as well as the preferential routing directions. It can be used to calculate

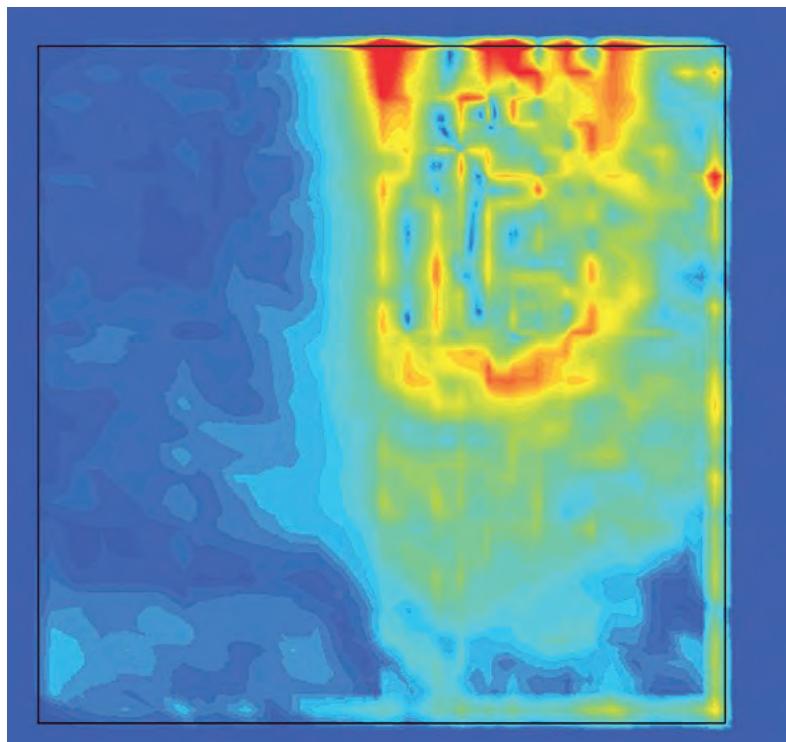
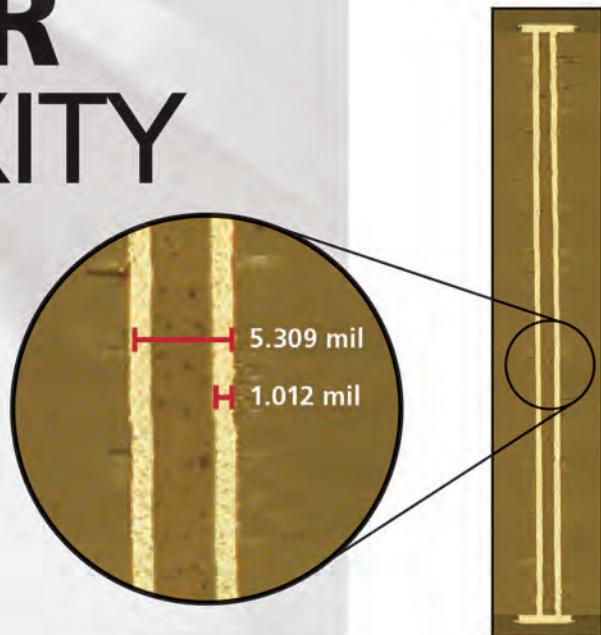


Figure 2: Die temperature distribution from a detailed non-uniform power map.

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the overall thickness and an isotropic averaged material property for this thermally active layer.

Up to this stage of the modeling process, heat should be distributed uniformly over the die. This will not be the case in practice, and the model should be refined to remove this assumption as soon as more detailed information is available from the IC design team. The benefit of using this assumption at the outset is that it gives an indication of the inter-die temperature variation that arises from the package's limited ability to hold the bulk die temperature uniform.

### Assisting floor planning

Providing the IC design team with information about the average die temperature and temperature variation for each die before the IC design process starts can greatly help floor-planning [2]. Floor planning is critical to the quality of the design because decisions made during this activity can either alleviate or exacerbate this temperature variation.

Once floor planning starts, a high-level power map from the IC design team can be imported into the thermal model of the package (Figure 2). The simulation model will often only take a matter of minutes to run, indicating where TSVs should be located to improve the thermal performance or where design changes are needed. For example, it may be important to ensure that two or more different functional blocks operate at similar temperatures to eliminate timing issues.

For logic-on-logic 3D ICs, the location of TSVs should be accounted for when partitioning the design among the various dies and during inter-die and intra-die floor planning, requiring power map information for each die. At this stage, opportunities exist to move the functional blocks in both x and y directions (xy expansion), keeping their relative positions the same but adjusting the gaps (white space) between them into which TSVs can be inserted to examine their effect on die hot spots. Knowing the TSV size and pitch, which scale with die thickness, blocks of higher through-plane thermal conductivity can be superimposed over the die thickness in these white space regions in the CFD simulation software to locally override the properties of silicon.

In early floor planning, extremes can be investigated to inform the IC design team of the extent to which hot spots can be controlled using TSVs, thereby placing boundaries on the problem. Optimizing both functional block and TSV layouts during floor planning needs to be done as part of the IC design flow.

As floor planning progresses, the thermal design effort needs to focus on the detail of the thermal interaction between die as the design is further elaborated. The power map for the die becomes much more detailed, and in the case of a 3D IC, the number and location of TSVs need to be defined as part of the electrical design.

### Thermal simulation inside the IC design flow

Thermal simulation work is best done within the IC design flow itself. To this end, the Mentor Graphics 3D CFD thermal simulation software FloTHERM is embedded into the Calibre IC design suite. TSMC created a thermal analysis flow based on FloTHERM and Calibre DESIGNrev and RVE, an industrial standard physical verification results viewing environment (Figure 3) [3]. This solution provides thermal simulation on

dies and interposers of 3D ICs, enabled by an automatic gridding capability that uses a localized grid in critical model areas such as the dies.

The flow described above takes die power map files that can be generated by power analysis tools and creates thermal maps that can be used for thermal design and for checking against thermal constraints. The thermal results can also be displayed as a histogram in Calibre RVE, and the thermal hotspots highlighted onto the design in Calibre DESIGNrev. In transient analysis,



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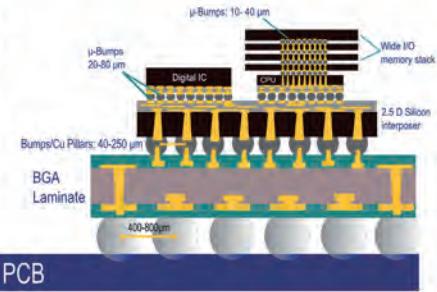
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## 3DIC Reference Flow – Mentor Track

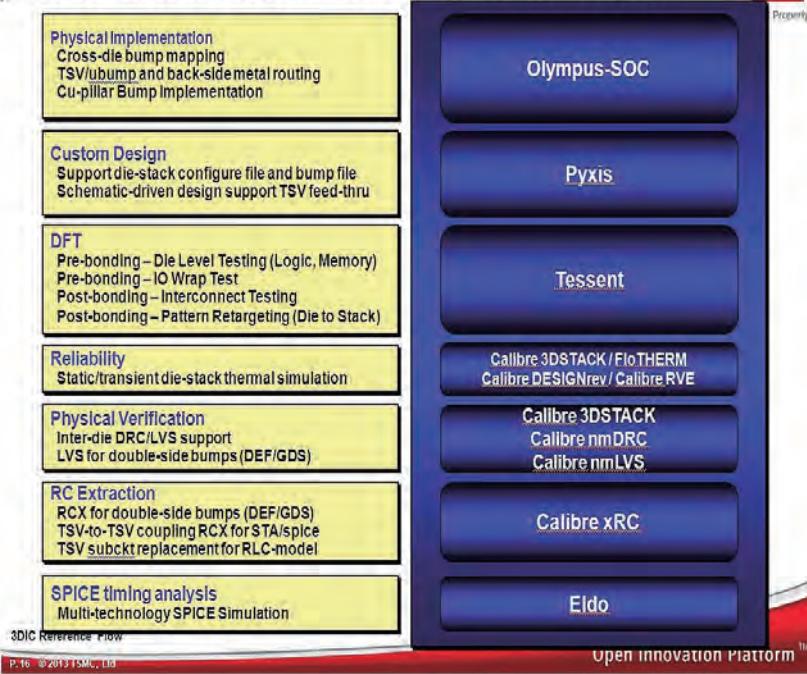


Figure 3: TSMC 3D IC reference flow 2013 [3].

temperature vs. time graphs can be displayed using Mentor Graphics EZwave graphical waveform environment.

More accurate thermal models of dies that take into account the metallization, such as interconnects and TSV in the dies, can be created and used in thermal simulation. A 3D IC thermal model can be created to allow the 3D IC package to be imported into a larger system, for further thermal simulation at the system level.

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### Biography

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# Critical challenges in advanced 3D integration: a metallization overview

By Thierry Mourier [CEA-Leti]

**M**ost major players in the semiconductor industry consider 3D integration to be a mandatory pathway to next-generation devices. This technology clearly has evolved beyond the feasibility phase and now is in increasingly common use in the so-called maturation phase.

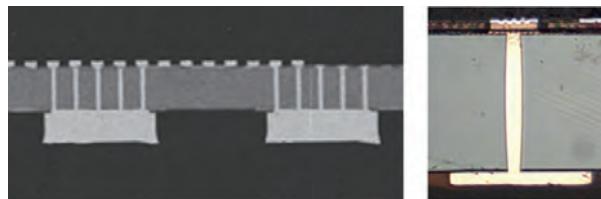
The type of integration selected varies from mid-process integration to a TSV-last approach, depending on the product and who does the integration: IDMs, outsourced semiconductor assembly and test suppliers (OSATs), or foundries. Several generic integration flows were evaluated in recent years to develop the requested process steps and integration modules to a sufficient maturity level to further investigate mass-volume production. The introduction of 3D integration for mass volume, however, has been delayed for several reasons. For one thing, the cost of this technology remains too high to clearly justify switching to it. For another, the targeted applications are moving to large circuits (interposers) and requirements for higher connection density, which will have a significant impact on the availability of the processes to be integrated.

Among the processes that will reach their limits, metallization appears to be critical. This article presents an overview of two of the most important processes required for advanced 3D integration. Through-silicon via (TSV), the connection between both sides of the circuit to allow vertical stacking, is the most challenging process. The barrier and seed layer deposition, as well as the copper filling or lining processes, face some limitations when performed using ionized physical vapor deposition (IPVD), because of the well-known poor step coverage of this technique. Alternative solutions must be quickly evaluated with regard to performance, as well as cost, to be transferable to manufacturing. The evaluation of the material properties and the associated characterizations are also critical points because most analysis methods are

defined for surface or horizontal parts of the device, whereas the most important interfaces of the TSV are the vertical ones. Specific sampling and preparation methods must be developed and will be discussed. Considering external connections, a higher density is required, which would lead to the fast decrease in the diameter of these solder connections. The integration and reliability behavior of the targeted dimensions are not known today.

## TSV challenges

Two types of TSV integration are possible depending on when they are performed and they lead to different morphology and specifications. The TSV can be processed between front-end-of-line (FEOL) and back-end-of-line (BEOL). In this case, it is called mid-process TSV. It is important to note that this configuration is also generally used for the realization of silicon interposers for which there can be no FEOL. These TSVs are generally in the range of 10 $\mu\text{m}$  diameter and the etched silicon depth is determined by the ability to handle the wafer after carrier removal. This depth is generally in the range of 80-100 $\mu\text{m}$ , resulting in a TSV aspect ratio of 10:1. These are the geometries that are actually considered (**Figure 1**) [1,2]. However, new projects and their specifications target higher aspect ratios for different reasons. The first one



**Figure 1:** Integration of 10x100 $\mu\text{m}$  TSV on a silicon interposer (left) and 6x55 $\mu\text{m}$  TSV in a memory on logic device stack (right).

is related to the development of silicon interposers. The die size of early products was in the millimeter range and a silicon thickness of 80 to 100 $\mu\text{m}$  was sufficient to overcome the bowing generated during the

integration. Today, the use of thick silicon-on-insulator (SOI) substrates, as well as the increase of interposer size, results in an increased deformation of the silicon substrate during both the phase when the device is exposed to thermal stress, and the flip-chip mounting process. Large bowing leads to bad soldering between the chip and the interposer.

To overcome this issue, dynamic thermo-mechanical study of the dielectric stack used on both front and back sides can be done [3], but this approach appears limited. The most efficient solution is to increase the silicon thickness. However, this increase leads to a critical state of metal deposition processes and specifically barrier and seed layer. The actual target is to increase the silicon thickness up to 150 $\mu\text{m}$  or even 200 $\mu\text{m}$  leading to a 15 to 20:1 aspect ratio, while 10:1 already appears as close to the metallization process limits.

The second motivation to increase the aspect ratio is driven by 3D IC activities. For these products, the silicon surface remains a critical aspect. Introducing TSV technology raises the notion of a keep-out zone (KoZ), which could be defined as the region around the TSV where no device can be placed due to the stress generated by the TSV on the silicon substrate [4]. One solution to overcome this limitation is to decrease the TSV diameter. Again, the ability to handle the wafer after debonding will fix the minimal aspect ratio. Fifty to 60 $\mu\text{m}$  appears to be the limit for wafer thickness. The TSV diameter is targeted at 3-5 $\mu\text{m}$ , thus increasing the aspect ratio to more than 15:1. As mentioned above, moving to high-

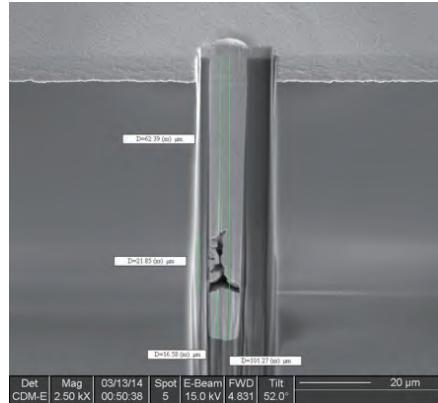
aspect ratio structures will exceed the limits of the standard barrier and seed deposition processes. As for the larger TSVs described before, the ionized PVD is the reference process, but is

known for providing limited step coverage. **Figure 2** shows the incomplete filling of a TSV because of a discontinuous seed layer at the bottom sidewall. Progress can be made on new IPVD systems, but the step coverage of such processes will stay in the range of a few percent, creating a need for a very thick deposit that will increase the cost and the internal stresses.

Alternative solutions have to be evaluated. For barrier material, the choice

of metal-organic chemical vapor deposition (MOCVD) TiN was considered by Leti as the primary choice. In order to build a very polyvalent process considering the need of low temperature for via-last integration, the choice was made for a precursor allowing a 200°C process. A collaboration with SPTS integrated this material initially on a 8:1 aspect ratio TSV with excellent electrical results [5]. Barrier efficiency to copper diffusion of the material is excellent and

5nm are sufficient to pass a 500°C, 10 hours thermal budget. Evaluation is now underway on the extension of this material to a much higher aspect ratio. **Figure 3** shows the step coverage of MOCVD TiN on 10x200μm. The results give almost 30% minimum step coverage in these aggressive structures, showing that the MOCVD TiN is a very good candidate for next-generation barrier layers.



**Figure 2:** Voids in a TSV filling because of a seed layer discontinuity.

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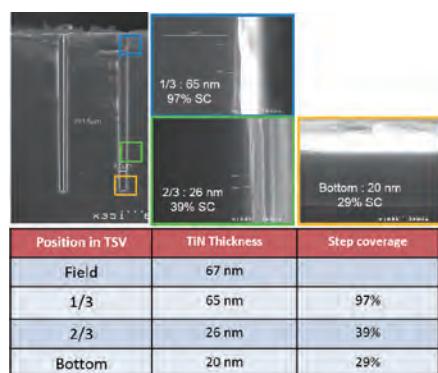


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Two processes are under evaluation for the seed layer. An MOCVD Cu seed is the most likely process to be used with an MOCVD barrier and is being developed based on the experience Leti has had with this material for damascene and TSV. MOCVD shows excellent step coverage. Additionally, G. Pares has reported the successful integration of 10x100μm TSV filled with copper using full CVD TiN barrier followed by a CVD copper seed layer, thereby confirming the excellent extendibility of CVD copper seed to very aggressive aspect ratios [6]. CVD copper seed, however, often suffers from adhesion difficulties related to the use of a fluorine-based precursor (Cupraselect). Work is

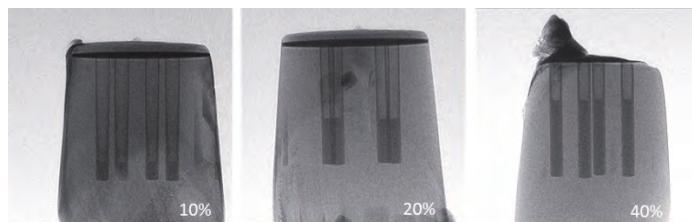


**Figure 3:** Step coverage of MOCVD TiN in a 10x200μm TSV (20:1 AR).

underway with SPTS to find the proper precursor to obtain a robust, full CVD process.

Another alternative to address iPVD's lack of step coverage is an electrochemical process. For that, Leti is collaborating with Alchimer on eGseed material. This process is based on the electrografting of copper seed. The process has been reported by Alchimer in several publications and is being evaluated on MOCVD TiN. **Figures 5b** and **5c** show void-free filling 10x120 $\mu\text{m}$  and 2x15 $\mu\text{m}$  TSVs using the same combination of MOCVD TiN, electrochemical seeding, and new-generation electroplating electrolyte.

Electrochemical plating of the structure is also becoming challenging because of the increase in step coverage. During introduction of mid-process TSV, a new generation of electrolyte was developed, combined with adapted process reactors. Considering the hardware, particular focus was put on the optimization of ionic transport to the bottom of the TSV by adding specific motions in the reactor. On the plating-chemistry side, a new electrolyte was developed to promote a pure bottom-up filling instead of the super-fill mechanism of the standard electrolytes used for filling the damascene structures (**Figure 4**). However, when moving to a higher aspect ratio, the design of the additives in the so-



**Figure 4:** Xray tomography of a partial filling of TSV showing pure bottom-up fill.

called Gen III electrolytes that provide the requested mechanism has to be adapted to the more aggressive geometries. Gen IV materials are being released and studies to evaluate their extendibility to high-aspect ratio structures is ongoing.

**Figure 5** shows a 10x120 $\mu\text{m}$  TSV filled with a) Gen III, and b) Gen IV electrolytes. We can clearly see that a bottom-up mechanism was not generated for Gen III chemistry, resulting in excessive lateral growth and pinching at the top of geometries. For the Gen IV chemistry, the bottom growth allowed void-free filling of the TSV before lateral growth created the void.

In the case of TSV-last integration, via dimensions are much higher (in the 50 $\mu\text{m}$  range) and complete fill with copper is replaced by a liner. The plating mechanism has to be monitored to provide a conformal growth in the geometry to ensure constant current density in the whole TSV. Specific plating chemistry and process conditions are again required to ensure a fast plating rate for throughput considerations, while ensuring the renewing of copper species in a very deep feature. **Figure 6** shows the effect of copper-concentration decrease at the bottom of a 60x200 $\mu\text{m}$  TSV. Because of higher consumption of cupric ions than mass transport can handle, a much slower growth is generated deep in the feature, leading to the thin final copper layer. In the center image, the process was tuned to increase the bottom copper thickness, but that led to significant overplating on the top third. The right image shows an optimal development with 100% step coverage obtained in the whole TSV.

These examples (in the previous images) show that the application – the integration scheme – will lead to specific process, material and hardware development to find the appropriate solution.

Characterization is one of the most critical challenges that accompany TSV integration. Most semiconductor characterization methods are made



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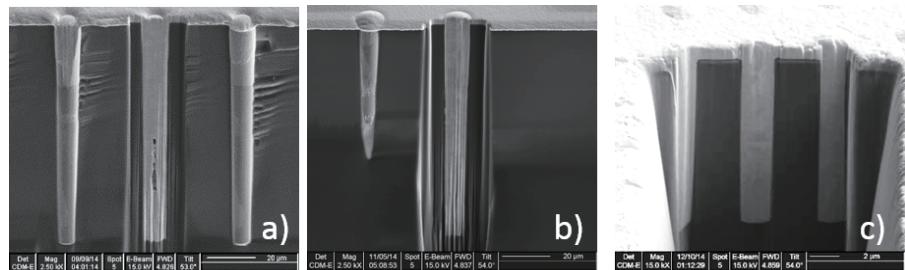
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to analyze planar surfaces. Or, in the case of the TSV, the vertical part of the structure is very long and is the active area with the desired properties. New techniques are being developed to overcome these issues, but specific sample preparation can allow the use of existing techniques [7]. For example, barrier properties to copper diffusion can be characterized as shown in **Figure 7**. A specific plasma-focused ion beam (p-FIB) preparation is performed to extract a square TSV and remove the silicon parallel to the sidewall, until the dielectric liner is reached. This configuration allows analysis by time-of-flight secondary ion mass spectrometry (TOF-SIMS) profile to evaluate copper diffusion through the barrier material along the TSV sidewalls. The results confirm the excellent barrier properties of the MOCVD TiN, as no copper is detected in the oxide after a 400°C thermal treatment. The same sample preparation can be applied to allow the existing characterization method to meet the TSV integration requirements.

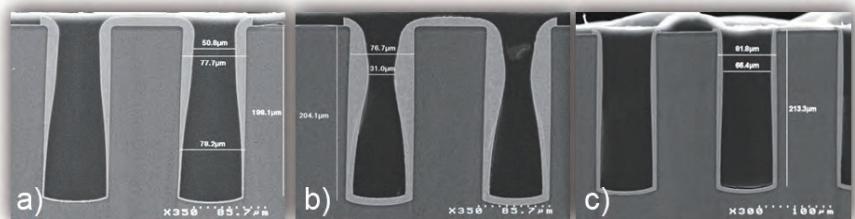
## The external connections challenges

As for the TSV density, chip-to-chip connection density must be increased significantly, while the diameter of solder bumps must be reduced. The actual size of the smallest microbump is around 20 $\mu\text{m}$ , but a 5 $\mu\text{m}$  diameter is targeted for next-generation assembly. Today, the standard copper pillar technology, based on the electrochemical deposition of copper and tin-silver material, is the reference process, but its extendibility to much smaller diameters is not known. The main issues are related to the down-scaling effect on the formation of the intermetallic compound and control of the defects, such as Kirkendall voids. The final reliability, both for mechanical strength and electromigration, will be strongly dependent on these properties.

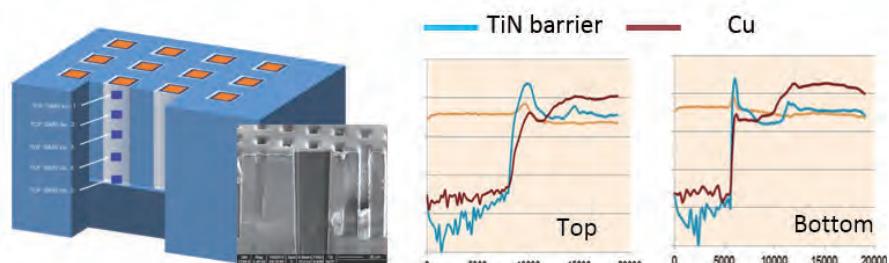
As diameter decreases, the amount of tin available to form the intermetallic Cu<sub>6</sub>Sn<sub>5</sub>, known to provide the good mechanical properties, decreases. This will lead to a faster formation of the Cu<sub>3</sub>Sn phase, known to promote generation of micro-voiding during the multiple reflows required for the 3D integration. **Figure 8** shows the intermetallic compound (IMC) formation on actual 20 $\mu\text{m}$  bumps (left) and on a 5 $\mu\text{m}$  one (right). After the first reflow – and because of the reduction of the tin thickness from 10 $\mu\text{m}$  to 4 $\mu\text{m}$  – almost all the tin is consumed to create the IMC. The two images on the right show the interface between copper and the IMC after one and five reflows. We can notice a significant increase in the amount of voids, which could lead to very poor mechanical properties in the connection.



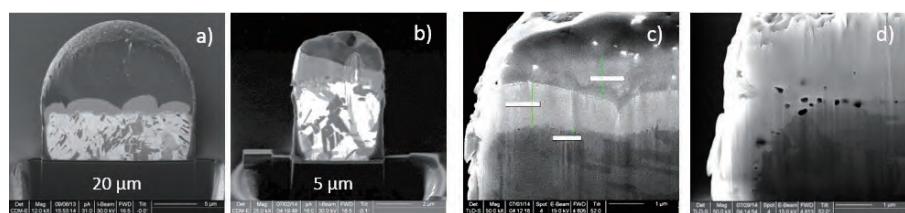
**Figure 5:** Filling of 10x120 $\mu\text{m}$  TSVs with a) Gen III, and b) Gen IV, and c) a 2x15 $\mu\text{m}$  TSV with Gen IV chemistries using MOCVD TiN and an electrochemical seed layer.



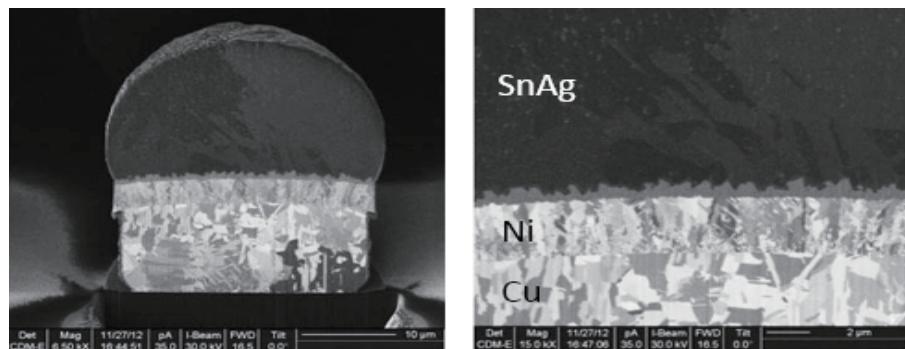
**Figure 6:** Effect of ECD process tuning on the morphological behavior of plating chemistry in a 60x200 $\mu\text{m}$  TSV - last structure: a) DC plating, b) Pulse plating and high current density, and c) Pulse plating and low current density.



**Figure 7:** PFIB sample preparation and TOF SIMS profiles showing excellent barrier properties of MOCVD TiN in 10x80 $\mu\text{m}$  TSVs.



**Figure 8:** IMC growth on a) 20 $\mu\text{m}$  and b) 5 $\mu\text{m}$  microbumps, c) 1 reflow, and d) 5 reflows on a 5 $\mu\text{m}$  microbump.



**Figure 9:** IMC growth on a 20 $\mu\text{m}$  bump using a CuNiSnAg solder bump.

Process conditions are being optimized, but the copper-tin system appears difficult to handle for fine-pitch solder bumps. The nickel-tin system appears to be a solution. It can be obtained by plating a nickel layer between the copper stud and the tin-silver layer.  $\text{Ni}_3\text{Sn}_4$  phase appears to be the unique formed phase and its growth is much slower than the  $\text{Cu}_6\text{Sn}_5$  phase, leading to the formation of fewer voids. **Figure 9** shows the same bump processed on the left with CuSnAg plating, while CuNiSnAg is used on the right. The IMC is confirmed to be much thinner with the use of nickel. Reliability comparison between these two systems is still ongoing.

## Summary

Today, the demand for 3D integration is seeing a trend toward increasing the density, thereby decreasing the feature size of the geometry to be processed. For both TSV and solder bumps, the actual metallization technologies are reaching limitations and new solutions must be introduced in the areas of both materials and deposition techniques. Particular care must be taken to limit their cost, which appears clearly as a barrier to further mass-volume 3D manufacturing. Some of the evaluated solutions appear very attractive, but much development is still required to advance them to a sufficient maturity level.

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## Biography

Thierry Mourier received an engineering degree with a specialty in electrochemistry from the Conservatoire National des Arts et Métiers in Grenoble, France. He is currently in charge of development of deposition processes for 3D and WLP technologies at CEA-Leti; email: thierry.mourier@cea.fr

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# Projection lithography performance using full-field exposure technology

By Ralph Zoberbier [*SÜSS MicroTec Lithography GmbH*]

**F**or decades, photolithography has been a fundamental process used in the fabrication and packaging of microelectronic devices. A key component of any photolithography process is the exposure tool, which uses light in the ultraviolet wavelength range to pattern a photosensitive resist or polymer. The exposure tool must be able to create the desired feature in the photo resist, precisely aligned to previously fabricated structures in underlying layers. Several types of exposure technologies exist today: proximity or contact printing, laser direct imaging and projection lithography. These technologies and the equipment toolsets differ mainly in terms of technical capabilities such as optical resolution, overlay performance and effective throughput. They also have a major impact on the costs related to the exposure process.

Looking at the main drivers and trends in the semiconductor industry clearly shows that on the one hand, innovation and performance improvements of microelectronic devices are required to meet future end user trends. For example, consumer electronic devices like tablets and smartphones are getting thinner and thinner and at the same time have to have higher computing power with increasing data storage and communication capabilities. On the other hand, manufacturing costs become more and more important for companies as a means of maintaining or improving their market position in a global and highly competitive environment. As photolithography is a key manufacturing process and cost contributor, the careful selection of the right exposure solution is mandatory to achieve the best possible cost structure in today's industrial lithography applications. Mask aligner technology is by far the lowest cost exposure solution in the market that provides excellent patterning capability coupled with highest possible throughput. Emerging applications in the semiconductor industry, however, require increased resolution and overlay

performances that are beyond the physical capabilities of a mask aligner. Up to now, the industry's only option was to switch to stepper technology. With the newly available scanning lithography technology on the DSC300 Gen2, engineers have an alternative selection of an exposure technology that uses the advantages of full-field lithography well-known from mask aligners. Furthermore, these capabilities are extended by the provision of projection scan lithography performance at a lower cost point than from UV steppers. The right selection of exposure technology requires a deep understanding of the pros and cons of each technology, plus a good understanding of the application requirements.

## Trends in advanced packaging applications

A wide variety of advanced packaging technologies exist today to meet the requirements of the semiconductor industry. The leading advanced packages, including chip-on-chip, wafer-level packages, chip-on-chip stacking, and embedded IC, all have a need to structure thin substrates, redistribution layers and other package components, such as high-resolution interconnects. The consumer's constant push for higher functionality on smaller and thinner end devices – like smartphones or tablets – drives the need for next-generation packages with finer features at increasing reliability of the package. In addition, cost considerations become more and more important in order to survive in the competitive landscape for all parties within the supply chain, from chip manufacturer, foundry, assembly and test suppliers, to the device manufacturer. Therefore, the industry desperately strives for innovative approaches to lower manufacturing costs coupled with enabling technologies that meet the challenging technical requirements.

A very good example of this trend is flip-chip technology. While solder bumping and single RDL layer technologies were

mainstream several years back, Cu pillar interconnects and multi-layer RDL are considered as one of the main growing application segments for the future. Cu pillar technology enables fine-pitch interconnects needed for the adoption of wafer-level packaging technology for leading edge devices with high I/O counts. However, the high number of interconnects limited to the chip-scale area requires photolithography of thick resist with almost vertical sidewalls and very good overlay of the pillar opening to underlying metal pads. Again, technical requirements of the lithography process define the required exposure technology, but careful selection is mandatory to also achieve the lowest possible manufacturing costs.

## Review of exposure technologies

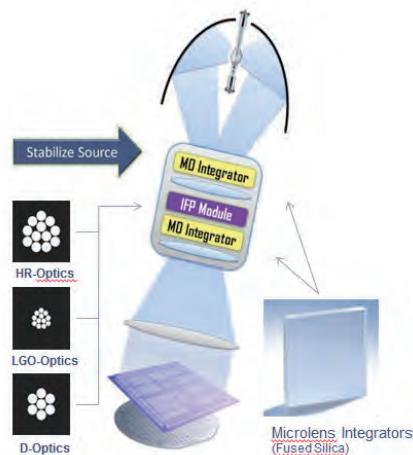
Full-field proximity printing and step-and-repeat projection lithography are the traditional exposure technologies of the electronic industry in applications fields such as wafer-level packaging, MEMS, LED, and displays.

**Mask aligners.** Mask aligners (also known as proximity or contact printers) are used for transferring a geometric pattern of microstructures from a full-field photomask to a light-sensitive photoresist, coated on a wafer or substrate, by exposing with collimated ultraviolet light. The mask and the wafer are aligned to each other and are in close contact or proximity. A mask aligner typically includes an illumination system, a mask stage for aligning the mask and a wafer stage for aligning the wafer.

In theory, contact lithography offers the highest resolution down to the sub-micron range, on the order of the wavelength of the illumination light. However, practical problems, such as mask contamination, make this process difficult to use for mass production. Proximity lithography, where the photomask and the wafer are physically separated by a typical proximity gap

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**Figure 1:** Conceptual drawing of SÜSS MO Exposure Optics® with exchangeable illumination filter plates.

of 20 to 50 microns, is well-suited for mass production and can achieve resolution down to 3µm on a 300mm wafer.

The exposure technology with by far the highest throughput available on the market is the mask aligner because one wafer is exposed in a single shot. At the same time, these exposure systems are available at the lowest capital costs on account of low equipment complexity compared to projection lithography and UV stepper tools. This low complexity results in the lowest level cost-of-ownership.

Latest developments for mask aligners allow the optimization of exposure performance. As an example, illumination systems based on microlens Köhler integrators, illustrated in **Figure 1**, allow the use of front-end-like lithography techniques, such as illumination shaping, and the use of assist features on the photo mask to provide the best possible result. Limitations, however, can still arise in cases when thick resist processes require very straight resist sidewalls and when practical overlay requirements reach a level of 1-2 microns or below on 300mm wafers.

#### Step-and-repeat projection systems.

These systems, also known in the industry as UV steppers, have been selected by users whenever they reached the process limitations or yield requirements of mask aligners. The type of UV stepper is typically defined by the optical layout used. In semiconductor back-end applications today, steppers are typically built with 1X catadioptric or 2X demagnification optics coupled with a corresponding stepping stage. Depending on the available field size of the optics, the system exposes a certain area of the wafer at a time, and performs a step-and-repeat process to cover the whole wafer. The main advantages of using a stepper lie in its overlay capability and, when 2X demagnification systems are used, in its enhanced resolution. A 2µm resolution capability with 0.5µm overlay performance is state-of-the-art technology. However, this performance is usually not required for the majority of wafer-level packaging applications, and is bound with higher equipment costs, typically an increase of 3-4x compared to 300mm mask aligner systems.

Another limitation of a step-and-repeat system is the limitation of the field size. The maximum die or package size that can be exposed is limited by the lens design itself. The larger the lens design, the higher the cost of the lens, and the more complex the optical aberrations correction design becomes. The field size that is usable is limited to be a multiple of a die size, to allow for step-and-repeat. With the limited usable field size, these systems typically require 80 or more exposure steps to pattern a complete 300mm wafer with the corresponding sacrifice in throughput. Furthermore, step-and-repeat systems cannot expose non-repeated features on a wafer or substrate. For example, flip-chip or redistribution layers (RDL) require the exposure of the wafer edge to enable electrical connection of electrodes for the subsequent plating processes. To overcome this limitation, UV steppers

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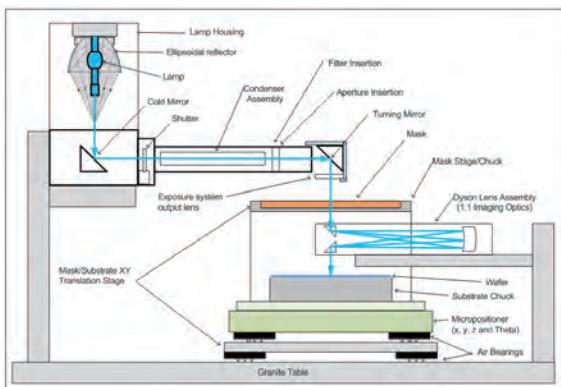
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**Figure 2:** Full-field scan exposure setup.

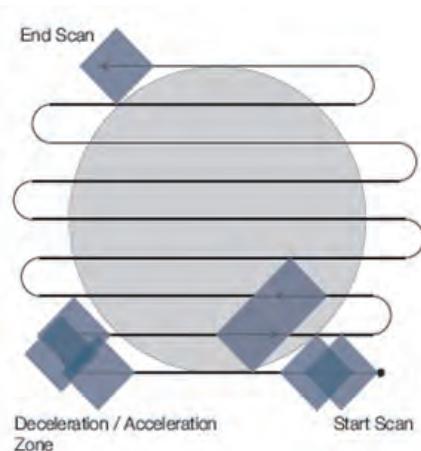
use either an edge exposure function on the pre-alignment station that further reduces the effective throughput of the exposure tool itself, or require additional edge exposure equipment that adds capex and complexity to the manufacturing line.

**Full-field projection scanning technology.** This new technology holds the promise of being the missing piece that offers projection lithography performance, coupled with the advantages of a full-field exposure tool at a lower cost point,

compared to a traditional UV stepper. This newly designed exposure concept meets the majority of process requirements and is built on a low complex projection lens design without the requirement of a highly sophisticated step-and-repeat stage. **Figure 2** shows a full-field scan exposure setup.

The projection scanner uses a 1X catadioptric lens design with a field size of ~30x30mm. This area is used to image the features from a full-field mask onto the wafer in a continuous scan process (**Figure 3**).

The complete wafer layout including non-repeated features, like the edge exposure ring, can be implemented into the mask design. The alignment of the mask to wafer is performed either through on-axis (TTL=through the lens) alignment or by off-axis alignment, depending on the process conditions. Thermal management of the mask itself has to be considered when operating a



**Figure 3:** Continuous scan operation for the exposure of an entire 300mm wafer.

14" soda lime mask to process 300mm wafers.

It is important to understand that mask contamination or intensive mask cleaning is not a requirement or limitation for this full-field exposure technology, as mask and wafer are operated with a large separation of about 200mm (shown in **Figure 2**).

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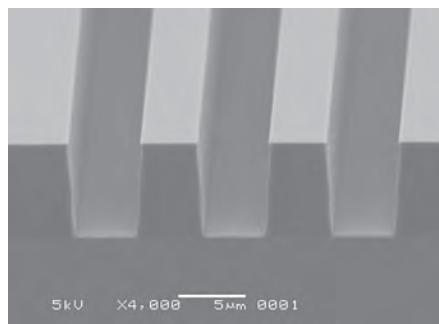
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## Requirements for advanced packaging applications

The processing of thick resists is very common in advanced packaging applications. As mentioned, today's emerging bump applications often require straight sidewalls to enable a high pin count. However, this requires a high depth-of-focus (DOF) of the projection exposure tool. The projection scanner technology provides the optimal combination of high DOF and resolution performance at a reasonable cost level. A flexible and interchangeable NA setting of the systems allows the ideal combination of resolution and DOF. In addition, as one of the key process parameters, focus adjustments can be used to adjust sidewall performance to meet application requirements (**Figure 4**).



**Figure 4:** DSC300 performance using TOK TMMR P-W1000T: 5µm L/S, 7µm thick.

The DOF of the exposure tool also defines the process window when processing highly warped substrates. Wafer bow and warpage become more and more of an issue when the substrate contains different types of materials each with a different coefficient of thermal expansion (CTE). New packaging concepts such as fan-out wafer-level packaging (FOWLP) use artificial wafer substrates based on compound materials. The trend to thinner packages and wafers can result in significant warpage, up to several mm. Currently, the effective exposure of these substrates requires pulling the substrate as flat as possible to stay inside the DOF of the systems. Only then is the expectation of acceptable resolution and CD uniformity of the exposure process achieved.

Latest developments and improvements show that, as an example, embedded wafer-level ball grid array

(eWLB) (FOWLP) wafers with an initial 5mm bow can be pulled flat down to a remaining high-low variation of <20µm on the exposure station, which is well inside the DOF for targeted features sizes of around 5-10µm.

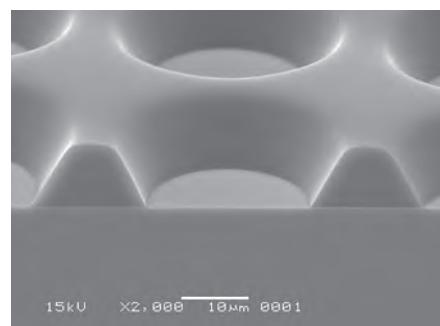
Finally, thermal control of the exposure mask during the process is a key requirement for full-field exposure systems. The exposure of a 300mm wafer requires a 14" photomask that is typically made of soda lime to maintain reasonable pricing, while UV steppers use 6" reticles made of quartz. As soda lime has a much different CTE compared to the typical silicon substrate, temperature changes result in a run-out effect between mask and wafer. Run-out is a magnification mismatch between the mask and the wafer that would lead to overlay inaccuracies. Adjustments and tight control of the mask temperature are needed to maintain a minimum runout and high overlay performance (**Figure 5**).

The final overlay performance including closed-loop run-out control of a full-field projection scanner for a

typical high exposure dose lithography process is in the range of 1-2µm, which meets typical market requirements.

## Cost-of-ownership considerations

The reduction of manufacturing costs and optimization of the equipment park is a key topic in every modern fab for semiconductor devices and packaging services. Therefore, cost-effective equipment that meets the technical requirements but is not over-engineered is the key to profit margin maintenance. Depending on



**Figure 5:** DSC300 performance using HD PBO 8820, 20µm via, 10µm thick.

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The advertisement features the company name "PRECISION CONTACTS" in a stylized blue font. Below it, there are four small images of various precision contact components: a blue Kelvin test socket, a silver leadless chip carrier (LCC), a yellow QFN package, and an orange leadless chip carrier (LCC). At the bottom, the website "PrecisionContacts.com" is written in a large, bold, orange font.



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| Cost per wafer                 | Mask Aligner | UV Scanner | UV Stepper |
|--------------------------------|--------------|------------|------------|
| <b>CAPEX</b>                   | \$1.3M       | \$1.8M     | \$3.0M     |
| <b>Throughput (WPH)</b>        | 65           | 39         | 35         |
| <b>Depreciation</b>            | \$0.87       | \$1.47     | \$2.75     |
| <b>Mask costs</b>              | \$0.96       | \$0.42     | \$0.19     |
| <b>Service and maintenance</b> | \$0.22       | \$0.37     | \$0.69     |
| <b>Consumables</b>             | \$0.16       | \$0.70     | \$0.84     |
| <b>Labor</b>                   | \$0.02       | \$0.03     | \$0.04     |
| <b>Cost per exposure</b>       | \$2.23       | \$2.98     | \$4.51     |
| <b>CoO comparison</b>          | 75%          | 100%       | 150%       |

**Table 1:** Cost-of-ownership comparison of exposure technologies based on a typical WLP process (1500mJ/cm<sup>2</sup> dose).

the process requirements, a careful selection of the exposure technology helps improve the cost structure of a lithography manufacturing line. A cost-of-ownership (CoO) comparison between the different selections should help to demonstrate the cost impact that comes along with each of the technologies (industry example shown in **Table 1**).

Obviously, the mask aligner technology provides the best CoO because of the low capex required and high throughput. The projection scanner still offers a ~50% cost advantage over a traditional UV stepper. This additional alternative helps users to lower their manufacturing costs for the majority of today's processes and ensures

availability of UV steppers for more critical layers.

## Summary

With projection scanning technology, an alternative exposure solution became available that provides projection lithography performance coupled with the advantages of a full-field exposure system. The system is designed to address the unique challenges of emerging packaging applications at a competitive CoO within the projection lithography equipment market.

## Biography

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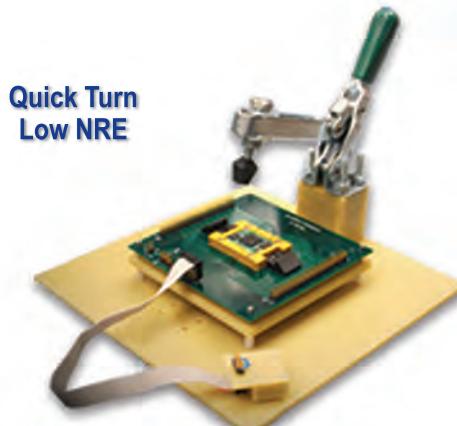


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# Advanced wafer-level technology: enabling innovations in mobile, IoT and wearable electronics

By Seung Wook Yoon, Boris Petrov, Kai Liu [STATS ChipPAC]

New and emerging applications in the consumer and mobile space, the growing impact of the Internet of Things (IoT) and wearable electronics (WE), and the complexities in sustaining Moore's Law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on density scaling and system level integration to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost.

This paradigm shift from chip scaling to system-level scaling is and will continue to reinvent microelectronics packaging, drive increased system bandwidth and performance, and help sustain Moore's Law. Demand for maximum functional integration in the smallest and thinnest package will continue to grow with an order-of-magnitude requirement for lower cost and power consumption. The challenge for the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals.

The Internet of Things (IoT) is emerging as a third, and ultimately bigger, wave in the development of the Internet, following the rise of the fixed Internet in the 1990s and the mobile Internet in the 2000s. While the fixed Internet connected 1 billion users via personal computers and the mobile Internet connected 2 billion users via computers, smartphones and tablets (on its way to 6 billion), the IoT is expected to connect up to 18 billion "things" to the Internet by 2018 (Figure 1). With the rapidly growing range of IoT applications, the number of "things" connected to the Internet could reach as high as 28 billion devices by 2020 [1]. There are many reports examining the implications of the IoT wave across multiple sectors within the electronics industry, particularly in the communication and semiconductor domains.

## Next-generation packaging requirements

Semiconductor packaging has a significant impact on the overall device performance. Traditional packaging technologies

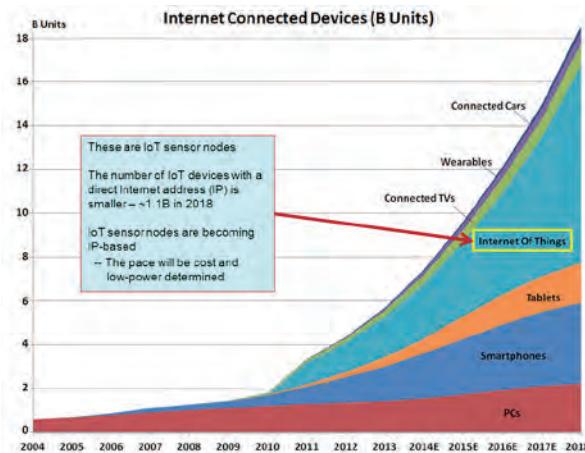


Figure 1: Estimated number of internet connected devices.

Source: BI Intelligence

are reaching their limits in terms of the performance, size and scalability required to meet the needs of emerging applications. Current and future demands of microelectronic systems in terms of performance, power consumption and reliability at a required cost are met by developing advanced silicon process technology, innovative packaging solutions based on chip and package system co-design, low cost materials, reliable interconnect technologies, and advanced assembly and test.

For IoT devices, there are four interrelated requirements for an effective packaging solution: 1) Cost effectiveness, 2) Thinner and smaller form factor, 3) High performance, and 4) Integration. For IoT and WE devices, three types of integrated circuits (ICs) will be the primary drivers of semiconductor growth: 1) Specialized low-power microcontrollers (MCUs, embedded processors with non-volatile memory (NVM) and power management functions); 2) Connectivity (Wi-Fi, Bluetooth®, GPS, cellular, ZigBee®, etc.); 3) Sensors and actuators (MEMS, image sensors, others).

The applications listed above and ICs require different process technology nodes and different process technologies—MCU (digital + mixed-signal + non-volatile memory), connectivity (RF + analog + antenna/security) and sensors (MEMS and non-MEMS). System-on-chip (SoC) could be an attractive

solution if different functions can be placed in the same wafer fab solution. However, achieving such an all-in-one SoC solution can be quite difficult and often very costly. An alternative approach is to balance silicon-level and package-level integration, as evidenced by rapid expansion of system-in-package (SiP) modules. SiP modules provide the ability to not only integrate multiple technologies, but also additional components such as passives, antennas, etc., to create fully functional sub-systems. To illustrate the

potential for miniaturization by use of SiP modules, Xiaomi's low-cost, high-performance MI3 smartphone, for example, contained approximately 850 electronic components, including ~22 filters, ceramic crystals, oscillators, ~103 diodes and small transistors, and ~670 passives.

## Advanced wafer-level technology

As a small, lightweight, high performance semiconductor package, wafer-level chip-scale packaging (WLCSP) has been a popular solution for space constrained mobile devices and is a compelling solution for new IoT and WE applications. WLCSP was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin-film metals and solder bumps applied directly on the surface of the die with no additional packaging [2]. The WLCSP provides the smallest possible package size—the final package is no larger than the die itself. The volume of WLCSP used in the industry has experienced steady growth – driven by the small form factor and high-performance requirements of mobile consumer products.

For emerging applications requiring significantly higher performance and bandwidth, a transition from fan-in WLCSP to fan-out wafer-level packaging (FOWLP) is often required to achieve maximum connection density, improved electrical and

thermal performance and small package dimensions. FOWLP, also known as embedded wafer-level ball grid array (eWLB), is a versatile interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements. Unlike fan-in wafer-level packaging, eWLB is not constrained by the semiconductor die size.

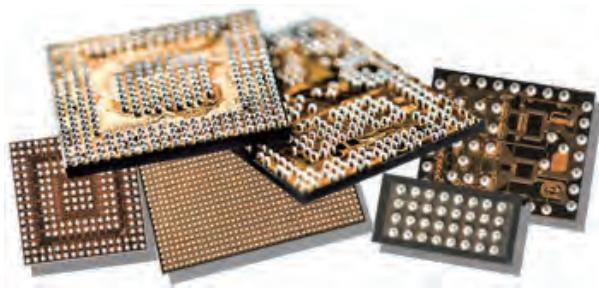
eWLB technology addresses a wide range of factors for mobile, IoT and WE applications. At one end of the spectrum is the need for a significant increase in input/output (I/O) density, a particular challenge as packages become progressively smaller and thinner. eWLB achieves fine line width and spacing as well as superior electrical performance, providing more design flexibility and a significant reduction in size than is possible with printed circuit board (PCB) technology. eWLB also provides the ability to integrate different active and passive elements, embedded very close to each other as an SiP. Complex thermal issues related to power consumption and device's electrical performance (including electrical parasitic and operating frequency) are successfully addressed by eWLB technology [3].

On the other side of the spectrum is the need to reduce assembly and test costs to meet consumer requirements for mobile, IoT and WE. The manufacturing process for eWLB is well established and lends itself to the use of large wafer and panel sizes, which provides compelling cost reductions over conventional wafer-level processing. The advantages of the unique manufacturing process are covered later in this article.

### eWLB for mobile applications

As demonstrated by the evolution of cellular phones, product differentiation today is driven by ever-expanding functionality, feature sets, and faster communications. At the same time, consumers have made clear their desires for feature-rich products in compact form factors for portability. eWLB provides the smallest possible yet highest performing semiconductors. Currently all leading mobile products as well as some consumer electronics contain eWLB packages that are baseband processors, RF transceivers, connectivity devices, near field communication (NFC), security devices, MCUs, memory, memory controllers, RF MEMS and power management ICs (PMICs) (Figure 2). There have been new opportunities and accelerated customer adoption in areas such as logic processors, MEMS, audio devices, fingerprint sensors and automotive devices.

In a number of cases, eWLB achieved a 20~40% reduction in package size as compared to other packaging solutions and over 50% volume reduction because of its slim and smaller form factor. For RF and high-frequency devices, eWLB showed less parasitic electrical performance, therefore, it also significantly improved overall device performance. In one example, a 77GHz SiGe mixer packaged as an eWLB achieved excellent high-frequency electrical



**Figure 2:** eWLB products found in various mobile and consumer electronics.

performance because of the small contact dimensions and short signal pathways that decreased parasitic effects. Higher power efficiency was found in eWLB solutions for PMIC devices compared to other package solutions. In terms of advanced silicon (Si) nodes, eWLB solutions are in high-volume production on 28nm and starting to ramp on 20nm devices.

### eWLB results

There are a number of cases where eWLB has helped semiconductor companies achieve very specific and measurable results. Following are some examples:

**RF eWLB.** Redistribution layers (RDL) in eWLB are utilized for higher electrical performance and complex routing to meet electrical requirements (Figure 3a). RDL also can provide embedded passives (R, L, C) using a multi-layer structure. Excellent performance of transmission lines was reported in manufacturing eWLB (insertion loss 0.1dB/mm @ 10GHz, 0.25dB/mm @ 60GHz) [4]. Inductors in eWLB offer significantly better performance compared to inductors in standard on-chip technologies. Further improvement of the quality factor of the integrated inductor and capacitors by using low-loss thin-film dielectrics and molding compound in eWLB was reported as well.

**SiP eWLB.** FOWLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in wearable electronics as a way

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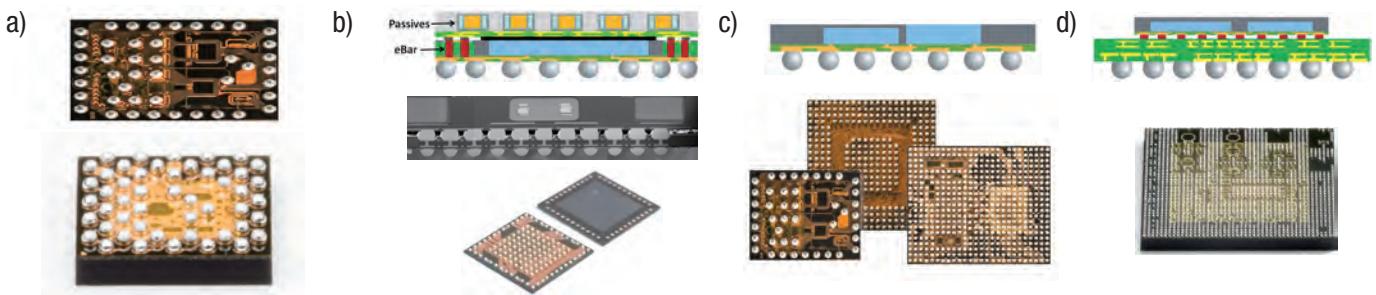
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**Figure 3:** Examples of eWLB for IoT devices: a) RF eWLB, b) SiP-eWLB, c) Multi-die eWLB, and d) 2.5D eWLB.

to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor. **Figure 3b** shows an example of SiP eWLB that has a number of discretes in the top package and is pre-stacked on the bottom eWLB to form a 3D SiP module with a thin profile. Discretes are removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. Discretes are also more effective when they are close to the device, which significantly improves the overall performance as well as provides a power saving advantage. This SiP eWLB has demonstrated more attractive power efficiency performance compared to conventional

packaging and it is representative of a significantly smaller packaging solution that is well-suited for IoT or WE devices.

**Multi-die eWLB.** Side-by-side multi-chip packaging can provide more design flexibility for SiP applications because a chip designer has more freedom in pad location, as well as circuit block allocation, as shown in **Figure 3c**. The 2.5D eWLB technology utilizes very fine-pitch metal line width and spacing as well as multi-layer RDL processing, providing better technical solutions for multi-chip packaging. Multi-die eWLB has already been in high-volume manufacturing for the last three years in applications such as RF, SoC, PMIC, and memory devices. Discrete multi-layer ceramic chip (MLCC) capacitors

and integrated passive embedding have also been successfully demonstrated and qualified.

#### Future 2.5D/3D applications with eWLB.

To enable higher interconnection density and signal routing, packages with multi-layer RDL and fine line/width spacing are fabricated and implemented on the eWLB platform. There are a number of development activities focused on further enhancements to highly integrated eWLB packaging solutions including finer line/space widths down to  $2/2\mu\text{m}$ , ultra-thin package profiles (currently qualified for 0.3mm including solder ball) and multi-layer RLD (above 3 layers). Innovative structure optimization of 2.5D/3D eWLB provides dual advantages of both height reduction and enhanced package reliability. Successful reliability characterization results on 3D eWLB-PoP package configurations demonstrate the capabilities of eWLB as an enabling technology for highly integrated miniaturized, low profile, and cost-effective solutions.

#### Cost-effective manufacturing process

The commercial availability of new packaging technology is driven by economies of scale and return-on-investment (ROI). While there are multiple variants of fan-out packaging in development in the industry, eWLB is the only FOWLP solution in the market today that has been in high-volume manufacturing for several years. The eWLB manufacturing process has continued to evolve to the FlexLine manufacturing flow, which is in volume production today. The FlexLine manufacturing method is wafer size agnostic, so one manufacturing module can produce fan-in (FI), fan-out (FO), and 3D fan-out products regardless of the incoming wafer size as illustrated in **Figure 4**. The same bill of materials, manufacturing method and manufacturing location can produce wafer-level packages from any silicon wafer size. Because the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm incoming wafers does not adversely affect the manufacturing utilization.

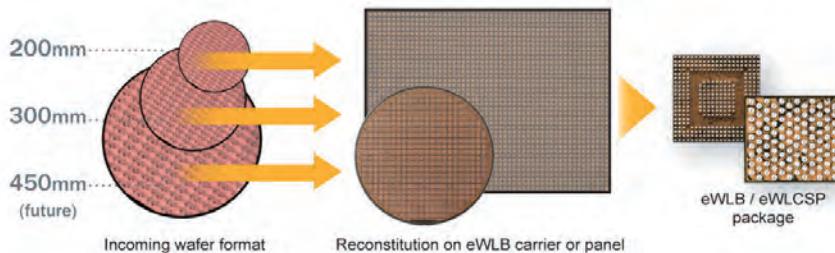
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**Figure 4:** The FlexLine approach can process multiple silicon wafer diameters on the same manufacturing line to produce both fan-in and fan-out packages.

FlexLine provides the ability to scale a device to larger panel sizes for a compelling cost reduction compared to conventional wafer-level packaging methods. A cost-effective manufacturing process is critical for the introduction of new products, such as wearable devices. The FlexLine process has been proven for advanced silicon nodes down to 28nm, ball pitches down to 0.35mm, and body sizes ranging from 2.0x2.0mm to over 10.0x10.0mm.

## Summary

Rapid growth of emerging mobile, IoT and WE devices will be enabled only by more compact and low-cost semiconductor packages with increased performance and packaging complexity. Wafer-level technology effectively accommodates new lithography nodes and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher bandwidth, ultra high-density, embedded capabilities, and improved thermal dissipation in a small, thin package format, advanced wafer-level packaging is an alternative for small flip-chip and large QFN packages and is quickly becoming a package of choice in the evolving mobile, IoT and WE markets. Fan-out wafer-level technology also provides the ability to tightly manage the co-design process and achieve silicon optimization, which is increasingly important in ultra cost-sensitive markets.

Advanced packaging plays a crucial role in delivering higher performance, lower power, lower cost, and a smaller form factor. There are many challenges that have been, and are being resolved in the application of cost-effective materials and processes for various reliability and security requirements for new and emerging mobile, IoT and WE applications. The industry requires innovation in packaging technology and a cost-effective high-volume manufacturing process that is able to meet current and forecasted market demands.

eWLB technology is an important wafer-level packaging solution that will enable the next-generation of mobile, IoT and wearable applications. The advantages of standard

fan-in WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound, and achieve 3D vertical interconnections for new SiP and 2.5D/3D packaging solutions. Next-generation eWLB technology will play an important role in the new wave of mobile, IoT and wearable devices today, and in the near future.

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## Biographies

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# GUEST EDITORIAL



## MEMS packaging: heading towards convergence

By Doug Sparks [[Hanking Electronics Ltd.](#)]

**M**icroelectromechanical systems' (MEMS) chip size and package size have decreased dramatically in the last 20 years. This shrink has accelerated with the heavy use of MEMS in consumer applications such as smartphones, gaming systems and tablets. Originally, MEMS packaging technologies, like process technologies, were unique among manufacturers, devices, and applications, and had only slight similarities with IC packaging. There was a shift from MEMS ceramic packages to plastic, and then to chip-scale packages (CSP) for decades beginning in the automotive marketplace, and continuing on to the consumer applications. Even sensors and MEMS chips with fluid interfaces have decreased in size as is illustrated in **Figure 1**. Wafer-to-wafer bonded differential or gauge pressure sensor chips were thick in order to decouple package-induced thermomechanical stress. Prior generations of automotive pressure sensors, and even current industrial MEMS pressure sensors use thick (1.5mm-3mm) sodium-doped glass or silicon wafers bonded to the silicon diaphragm wafer. The

wafer bond was either anodic, for glass substrates, or reflowed glass for silicon substrates. The fluid was exposed to the backside of the silicon diaphragm, avoiding corrosion of the frontside metallization.

For slightly corrosive or humid MEMS packaging applications, the top circuit side of the silicon chip is often protected with parylene and/or a silicone gel coating. For aggressive industrial applications, MEMS pressure sensor chips are immersed in gas-free silicone oil using a welded corrugated stainless steel diaphragm.

Now, MEMS pressure sensors use silicon-to-silicon direct wafer bonding followed by chemical mechanical polishing (CMP) for thinning or chemical vapor deposition (CVD) sealing to form a reference vacuum cavity or diaphragm. This process flow results in extremely thin MEMS chips. These small, thin MEMS chips are used in automotive, medical and consumer applications. For smartphones, that package must conform to the same size requirement of similar MEMS motion sensors and ICs. This new MEMS wafer bond process is comparable to that used in making CMOS image sensors (CIS), in which the CMOS array wafer is

silicon direct-bonded to a carrier wafer prior to thinning by CMP. One can see how CIS has borrowed the wafer-to-wafer bonding and thinning processes developed for MEMS and silicon-on-insulator (SOI) wafers. The MEMS pressure sensors and CIS chips are generally under 100-500 $\mu$ m's thick, as opposed to 2-4mm thick found in older generation of MEMS pressure sensors.

Temporary, or adhesive wafer-to-wafer bonding, is being employed in both MEMS and ICs for wafer thinning and handling of thinned wafers for consumer applications, as well as via-last TSV processing. Once the associated back-end processes are complete, there are three temporary processes employed for separation of the device wafer or chips from the carrier wafer: thermal, chemical and mechanical. For thermal separation, the wafer stack is heated and then slid apart. For the chemical separation process, the carrier wafer, often glass wafer, has drilled holes that allow for a quick separation of the wafers after solvent soaking. For mechanical separation, the edge of the wafer or chip is pried from the carrier wafer, which had a release layer sprayed on it prior to adhesive dispense.

Back-end processing of such small MEMS devices as pressure sensors and microphones is also adopting the latest chip singulation methods that have been applied to ICs. Laser dicing is being used by many of the thinner, high-volume MEMS wafer manufacturers. Deep reactive ion etching (DRIE) was developed and applied to many MEMS devices and is now starting to be used for ICs and MEMS wafers for chip singulation in the back-end or packaging facilities. DRIE or plasma singulation of

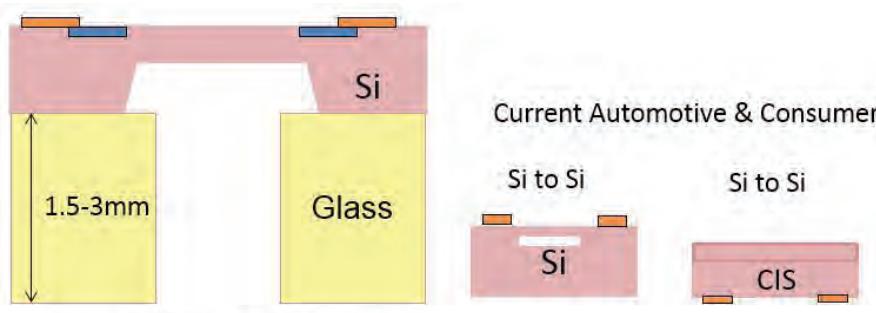
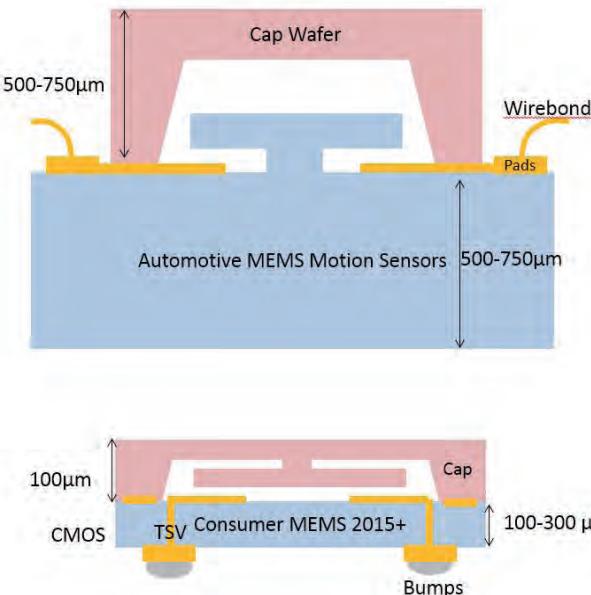


Figure 1: MEMS pressure sensor chip size change.



**Figure 2:** MEMS motion sensor CSP size and technology change (not drawn to scale).

silicon wafers provides a smaller “saw” street resulting in more chips per wafer, and it can eliminate sharp corners and silicon slurry or laser slag particle contamination. These small die are most often next placed on a circuit board panel or interposer, and in many cases, calibrated at the same time in parallel prior to panel singulation.

Chip-scale packaged (CSP) MEMS motion sensors have seen a similar shrink over the last 10 years as illustrated in **Figure 2**. The first high-volume MEMS accelerometers and gyroscopes were applied to vehicles in the late 1990s. These utilized wafer-to-wafer bonding for a small CSP to both protect the moving MEMS elements from mechanical damage, but also to control the damping and element gas pressure. Wafers (at full thickness) were bonded together, most often using reflowed glass wafer-to-wafer bonding. This reflowed glass provided a hermetic seal that was electrically insulating, however a wide sealing surface was required because of the spread of the glass when reflowed. To shrink the sealing surface area, and in some cases lower the wafer bonding

temperature, metallic wafer-to-wafer bonding methods were developed.

The metallic wafer bonding methods discussed above borrowed metallurgies and processes developed for bumping and circuit board component attachment. Solder or eutectic wafer bonding generally is used for lower temperature wafer bonding in which the grain structure of an electroplated or polycrystalline element would change at higher bond temperatures.

It is also used for IR and optical sensors in which coatings can degrade at high temperatures. Gold-tin, gold-indium, copper-tin, aluminum-germanium and gold-silicon are common examples of eutectics or solders employed with MEMS wafer bonding. To minimize sealing area, a metallic thermocompressive bond is employed without the formation of a eutectic liquid phase. Examples of thermocompressive bond metals include gold-gold and copper-copper. In addition to these new types of metallic wafer bonding, through-silicon vias (TSV) have been adopted by many MEMS device manufacturers. TSVs have been included in both the top capping wafers and the lower device or CMOS wafer.

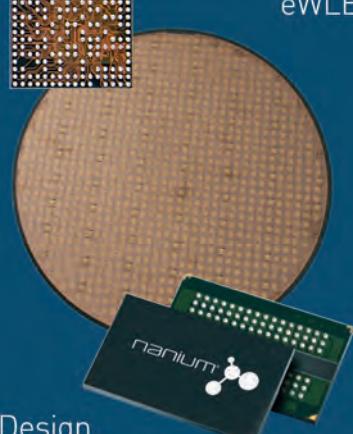
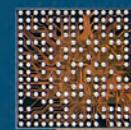
Wafer-level packaging of high-Q resonators, such as gyroscopes and RF devices, have had problems with desorbed gas molecules. These water vapor and air molecules desorb from the wafer surfaces during the relatively high temperature (250–500°C) wafer bonding process after hermetic sealing of the individual sensing or actuating elements.



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The trapped gas molecules raise the pressure and therefore, lower the Q, and can then be absorbed by the microcavity surfaces that are at low temperatures (-40-0°C) and then desorbed at higher temperatures (85°-150°C) during operation, resulting in degraded performance. To permanently trap the residual gas molecules, thin-film getters were developed and integrated into the WLP process flow. Improved degas baking of the wafers and CVD sealing have also been used recently to reduce the trapped gases in MEMS CSP and enhance long-term reliability of the hermetic CSP.

For many years, MEMS chips have been stacked on top of a CMOS application-specific IC (ASIC) and with other MEMS chips to form combo packages, electrically interconnected with wire bonding. These have resulted in 3-axes acceleration, 3-axes gyroscopes, e-compasses and ASICs in the same over-molded package. As is illustrated in **Figure 2**, MEMS wafers and CMOS wafers are increasingly being bonded together, using a metallic bond, which also has metallic electrical interconnects between wafers and to the TSVs. This structure enables a further shrink to MEMS CSPs through a bumped electrical interface. The top capping wafer can be a pure MEMS device, or the CMOS wafer can contain moving MEMS elements, released by an anhydrous oxide undercut process. The change over from 200mm MEMS wafers to 300mm wafers may be driven by WLP needs not MEMS fab capacity. MEMS-CMOS wafers are also being fabricated in which the silicon element is released by an anhydrous HF process and then sealed in a vacuum using a CVD process. It is easy to draw the parallel between the MEMS wafer/chip stack that combines metallic interconnects and TSVs and the same electrical structures used in 3D-ICs. The DRIE processes developed for trench dielectric isolation and MEMS devices in the 1980s and 1990s are now being used for TSVs in silicon interposers and 3D ICs. The convergence of the MEMS wafer processes and wafer-level packaging techniques is now evident for MEMS, CIS and 3D ICs.

### Summary

Thanks to the requirements of consumer markets, MEMS back-end processing and package designs are converging with each other, as well as those of CMOS imaging sensors and 3D ICs. Wafer processes developed for MEMS devices such as DRIE and wafer bonding, are now being adopted by back-end facilities to package MEMS, CIS and 3D ICs. This trend is likely to progress with 3D IC, with MEMS sensors the likely outcome.

### Biography

Doug Sparks received his PhD in Material Science from Purdue U. and is the EVP at Hanking Electronics; email [sparksdr@hanking.com](mailto:sparksdr@hanking.com).



## KLA-Tencor leverages front-end technologies for packaging inspection and metrology

By Debra Vogler, Sr. Technical Editor

**K**LA-Tencor recently announced two new systems that support advanced semiconductor packaging technologies. One of them – the CIRCL-AP™ – enables all-surface wafer defect inspection, and review and metrology at high throughput, which is achieved by the use of multiple modules that utilize parallel data collection for process control.

Prashant Aji, Sr. Director, Head of Marketing SWIFT, at KLA-Tencor, told *Chip Scale Review* that the traditional packaging flow in which a wafer is processed at the front-end before going to an outsourced assembly and test (OSAT) house for packaging, has been changing. “For the last 5-6 years, wafer-level packaging has been growing significantly because the industry has been driving more towards the use of through-silicon vias (TSVs), redistribution layers (RDLs), and bumping, giving rise to the middle-end market,” said Aji. “Sometimes, this middle-end is at an IDM house or foundry, or it’s at an OSAT packaging facility.”

The company is responding to what it views as multiple inflection points in the packaging industry driven by the shrinking size of packages to meet the mobile market, the emergence of wafer-level packaging (WLP), a shift to OSATS, and the adoption of front-end processes, such as CMP, electroplating, and Cu seeding, to the back-end. For the back-end portfolio, the company has leveraged its experience in front-end technologies along with its expertise in advanced optics, advanced illumination, and algorithms. “These technologies provide sensitivity at high throughput, which are required for the changing middle-end-of-line market,” explained Aji.

Other packaging market drivers detailed by Aji include: 1) Decreasing bump size for wafer-level chip-scale packaging (WLCSP), as well as for fan-out packages; 2) The switch from solder bumps to Cu pillars; and 3) With respect to fan-out packaging, the line spacing of RDLs is decreasing. About the latter, Aji told CSR that now, line spacing is around 10µm, but it will be dropping down to 5µm, and then to 2µm in late 2016 as it goes into production. “Our tool is qualified to run those 2µm line spacing inspections,” said Aji. “Customers are also adding TSVs to the wafer and typically, the aspect ratio for TSVs is 10:1. Our tool, because of its high sensitivity, is well-positioned to inspect in that space for RDLs, TSVs, and Cu pillars. Those are the



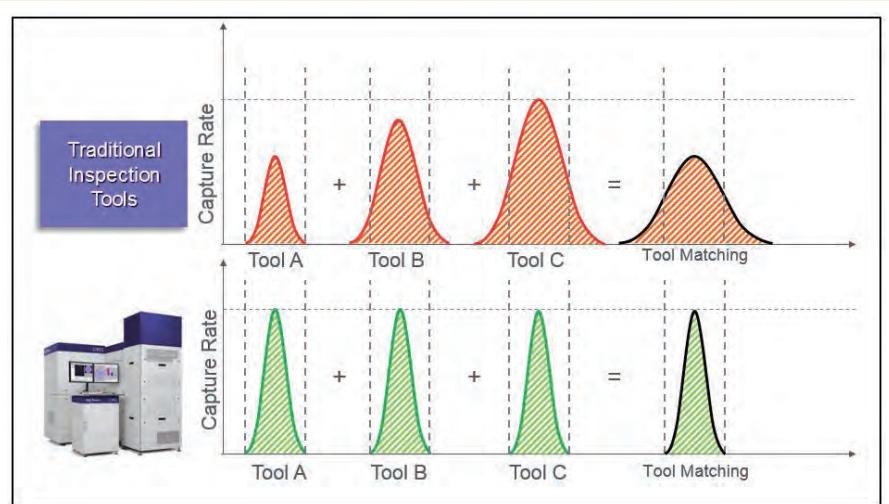
Prashant Aji, Senior Director, Head of Marketing SWIFT, at KLA-Tencor.

three main applications we’re focusing on. For process flows, we’re focusing on 2.5D and 3D fan-out packaging, and high-end WLCSP.”

The CIRCL-AP comprises three modules plus a handler. The 8-Series module provides front-side defect inspection and metrology capabilities, and couples LED scanning technology with automated defect binning. The CV350i module, based on the company’s VisEdge® technology, enables detection, binning and automated review of wafer edge defects and metrology for critical edge trim and bonding steps in the TSV process flow. The Micro300 module enables high-precision 2D and 3D metrology required for these advanced processes.

Aji told *Chip Scale Review* that the CV350i module is a key differentiator for the tool. “One of the biggest costs for advanced WLP that is preventing the industry from taking 3D ICs to high-volume manufacturing (HVM) is the bonding process,” said Aji. This module enables the monitoring of the device-to-carrier bonding process, thereby enabling rework to be done if needed. “By improving the yield of the bonding process, the overall costs for packaging are reduced.”

Also a key enabler is the use of high-brightness LEDs (HBLEDs) in the frontside inspection module. The company has been using HBLEDs in its front-end equipment since 2008. “The long life and stability of these devices translates to reduced consumable costs for the users,” said Aji. “When customers buy multiple tools, they can do tool matching in a robust way without compromising sensitivity (**Figure 1**).” According to Aji, this ability comes not only from the design of the hardware itself, but in the very tight control of the optics and optical components, as well as how the LEDs are sourced.



**Figure 1:** CIRCL-AP™ tool matching. LED illumination and advanced custom optics enable tool-to-tool matching with higher defect capture rate.

# INDUSTRY NEWS

## ECTC 2015 continues its tradition of excellence

By Eric Perfecto [\[IBM Corporation\]](#)

The 65th annual Electronic, Components and Technology Conference (ECTC) sponsored by IEEE/CPMT convened at the Sheraton Hotel & Marina in San Diego, CA on May 26-29, 2015. By all measures, the event, considered by many to be the premier international conference on IC packaging, components, and microelectronic systems technology, was an outstanding success. This year, the ECTC General Chair was Beth Keser from Qualcomm; Henning Braunisch of Intel, was the Technical Chair.

There were many broken records at this year's ECTC, including the highest attendance ever: 1,559 attendees from 32 different countries; 106 Technology Corner exhibitors, including 22 new exhibitors; and an overall increase of corporate sponsors. This year the conference introduced a very popular "app" that enabled the scheduling of activities and allowed for full communication among conference attendees. The conference also held the first CPMT Women's panel with the focus on the topic of "Own Your Own Personal Success – What You Should Do," chaired by the ECTC General Chair, Beth Keser.

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(Left to right): Alan Huffman/RTI International, Vice General Chair; Sam Karikal/Broadcom, Assistant Program Chair; ECTC Keynote Speaker, Matthew Grob, Qualcomm CTO; Beth Keser/Qualcomm, 65th ECTC General Chair, and Henning Braunisch/Intel, Program Chair.



This year the 2015 IEEE Components, Packaging and Manufacturing Technology Field Award was given to Nasser Bozorg-Grayeli of Intel. Steve Bezuk of Qualcomm (on the left) received the 2015 CPMT Electronics Manufacturing Award. Also in the picture is Jie Xue of Cisco, IEEE CPMT Society President.

The conference consisted of 361 technical papers, presented in 36 oral and 5 interactive presentation sessions, including a student poster session. This year the ECTC abstract acceptance rate was 62%, with submission divided between corporations (48%), universities (42%) and institutes (10%). The number of papers accepted were primarily from the US, Japan, Taiwan, China, and Germany (in that order).



Gail and Paul Wesling received an ECTC contribution award from Beth Keser, Qualcomm, 65th ECTC General Chair, for the many years of publishing the ECTC proceedings.



John Knickerbocker, IBM Research, assembles a cheeseburger at the outdoor ECTC Gala Reception. This year's ECTC Gold Gala sponsors were: Amkor, DOW Electronic Materials, NANUM, SPTS, SPIL, and Deca Technologies.

Vardaman of TechSearch International, Inc., had the highest attendance (225 people)—the highest of the 6 special sessions.

#### Mark your calendar for the 66th ECTC

Planning is already underway for the 66th ECTC, which will be held

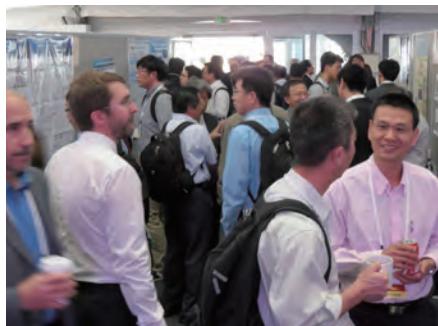
May 31–June 3, 2016, at the Cosmopolitan Hotel in Las Vegas. The first call-for-papers has been issued and abstracts must be received by October 12, 2015. For more information visit <http://www.ectc.net>.



Bill Chen/ASE, Kyung-Wook Paik/KAIST, and Jean Trehewella/GLOBALFOUNDRIES, enjoy the ECTC Gala Reception.



E. Jan Vardaman, TechSearch International, chaired the ECTC Plenary Session on the Internet of Things. The four panelists to her left are Subramanian Iyer, UCLA/IBM, Ilyas Mohammed/Jawbone, Jerry Tzou/TSMC, and Li Li/Cisco.



All five interactive presentations – designed to allow technical exchange in a friendly environment – were very well attended.

While the topic of 3D still dominated in the number of sessions with 12 in total, other alternate packaging structures, such as wafer-level packaging (WLP), fan-in and fan-out got the highest attendance. In particular, the sessions that dealt with the implementation of micro-pillars with WLP. The Wednesday Plenary Session on The Internet of Things and the Future of Interconnected Electronics, chaired by E. Jan

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## Must See Events at IWLPC 2015!



### Keynote Address

#### High Density Fan-Out: Evolution or Revolution

Rama Alapati, Director, Package Architecture & Customer Technology (PACT), GLOBALFOUNDRIES



### Panels

#### Fan-Out WLP Panel Processing

Moderated by: E. Jan Vardaman, President, TechSearch International, Inc.



#### Interposers, 3D TSVs, and Alternatives:

#### What are the Options and Where do They Fit?

Moderated by: Françoise von Trapp, Queen of 3D, 3D InCites

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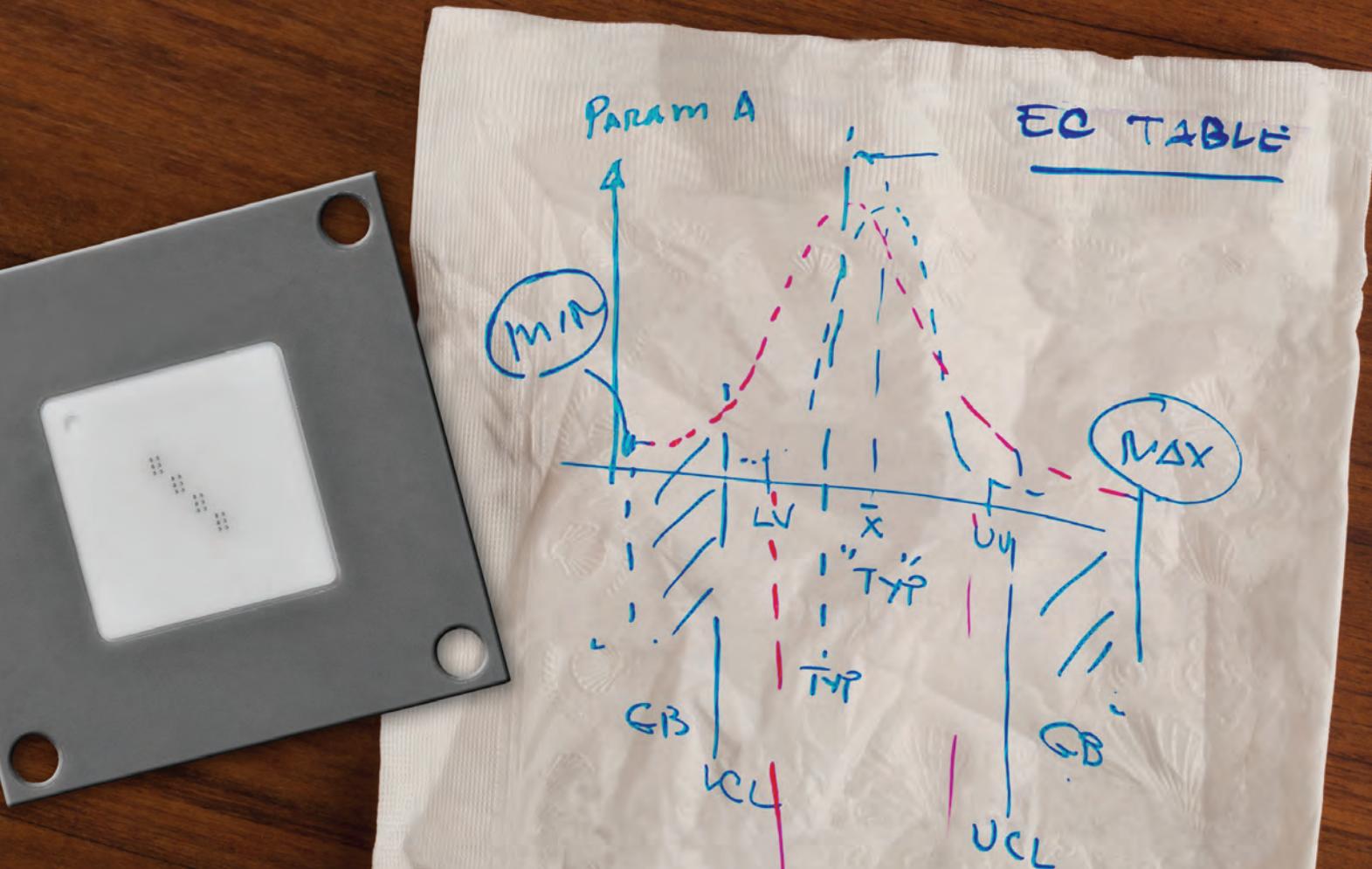
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