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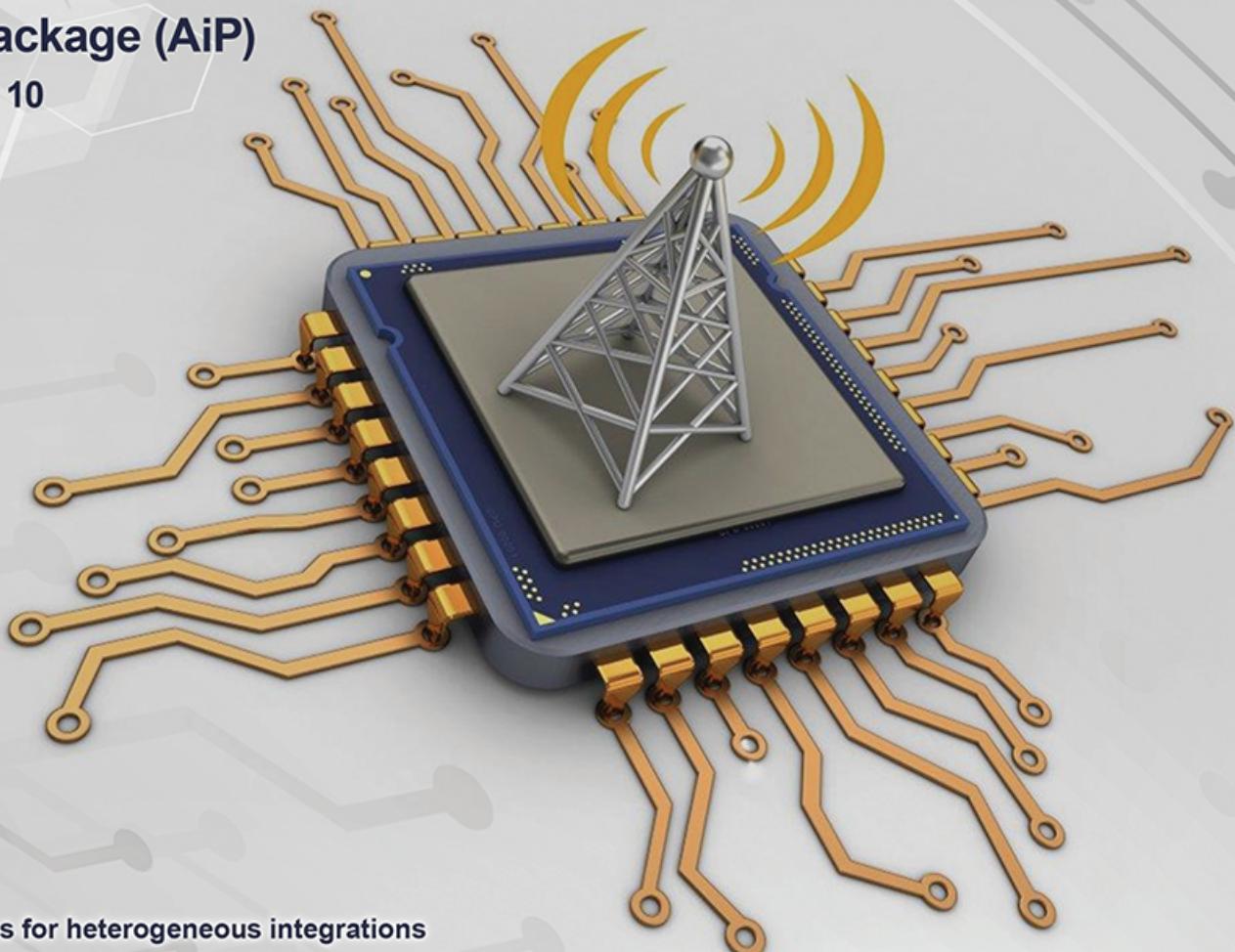
The Future of Semiconductor Packaging

Volume 23, Number 1

January • February 2019

Production test interface solutions for mmWave and antenna in package (AiP)

Page 10



- RDLS for heterogeneous integrations
- Moore's Law for Packaging to replace Moore's Law for ICs
- New test methodologies for 5G wafer high-volume production
- Temporary bonding and the challenge of cleaning post-debond
- Air jetting debonding for thin-wafer/panel and FOWLP processing
- Discontinuities drive innovations in 3D-IC package design & verification



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CONTENTS

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The emergence of next-generation 5G, WiFi protocols, and automotive radar have pushed ICs into extreme frequency bands. High-volume 6GHz production test cells are being modified to up-convert, mix, down-convert, source, and measure for both cmWave (3GHz to 30GHz) and mmWave (30GHz to >100GHz) frequencies. Test interface hardware has now become a key differentiator for bringing these next-generation applications to market, with relatively few solutions available.

Cover image courtesy of Cohu

DEPARTMENTS

Technology Trends

- Discontinuities are driving innovation in 3D-IC package design and verification** 7
Wally Rhines *Mentor, a Siemens Business*

- CEA-Leti's extended 300mm line to enable disruptive technologies** 41
Emilie Viasnoff, Christophe Maleville *CEA-Leti*

Industry News

43

FEATURE ARTICLES

- Production test interface solutions for mmWave and antenna in package (AiP)** 10
Jason Mroczkowski, Dan Campion *Cohu*

- New test methodologies for 5G wafer high-volume production** 14
Daniel Bock, Jeff Damm *FormFactor, Inc.*

- Redistribution layers for heterogeneous integrations** 20
John H. Lau *ASM Pacific Technology, Ltd.*

- Temporary bonding and the challenge of cleaning post-debond** 26
Phillip Tyler, Kenji Nulman *Veeco Instruments - Precision Surface Processing*
Michelle Fowler, Seth Molenhour *Brewer Science, Inc.*

- Moore's Law for Packaging to replace Moore's Law for ICs** 31
Rao R. Tummala *Georgia Institute of Technology*

- Air jetting debonding for thin-wafer/panel and fan-out wafer-level package processing** 37
Hao Tang, My Nguyen, Joshua Huffaker, Anastasia Banner *Micro Materials Inc.*

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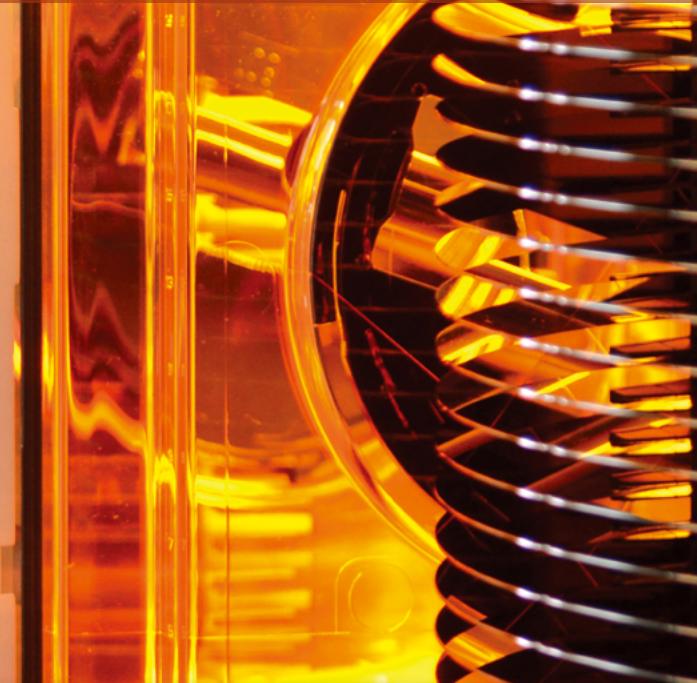
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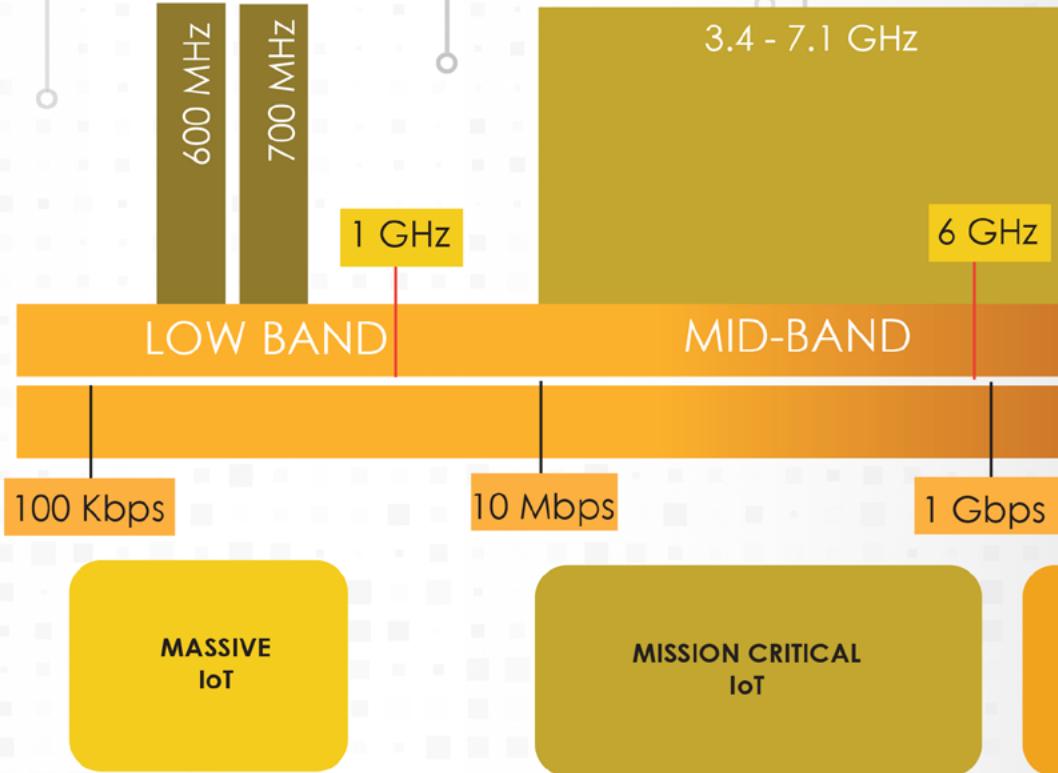
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Discontinuities are driving innovation in 3D-IC package design and verification

By Wally Rhines *[Mentor, a Siemens Business]*

Disruption and discontinuity are often the hallmarks of progress. Rarely does an industry experience progress without turmoil, no matter how much we plan and prepare. Roles and responsibilities change, familiar processes vanish, and even the tools we use change. However, as anyone who has ever been a part of a merger knows, some of the biggest challenges arise when two groups, each with their own well-established practices and processes, are tasked with finding new ways to work together to bring about a new blended entity. Organizational structures magnify the conflict and separation between these groups because they often have their own, separate metrics for success.

Multi-chip packages (MCPs) have existed for quite some time now, and the outsourced semiconductor assembly and test (OSAT) industry has been manufacturing them for years. However, traditional 2D layout and packaging approaches are increasingly stressed to meet performance and form factor needs. Three-dimensional integrated circuit (3D-IC) designs increase both data throughput and the amount of functionality in a given footprint. By going to 3D, the connections between any two given points can be made shorter with lower parasitic resistance and capacitance values compared to traditional packaging approaches. This increases bandwidth and allows smaller drivers for inter-chip communication, which reduces power dissipation significantly.

Both the IC industry and the packaging industry have well-established processes for design and verification, so the amalgamation of the two shouldn't take that much work. Right? Of course it isn't that easy. While each packaging era brought disruptive change to the industry, the last time we saw this much upheaval was when the industry transitioned from lead frames and the use of mechanical computer-assisted design (MCAD) tools to plastic ball grid array (PBGA) and package-on-package (PoP) technologies, which heralded the development of electronic design automation (EDA) tools for packaging.

However, the advent of 3D-ICs could be considered a case study for merging disparate technologies. 3D packaging allows designers to combine chips using different technologies (e.g., different process nodes, or types) into a single multi-chip package with similar performance and footprint (heterogeneous technology integration). What does that mean in the real world? With 3D-ICs, we have different design components supplied by unrelated design teams and/or companies. Each component is designed using different tools, for different processes, with different database formats and vastly different layout styles.

Why does design of a component with different tools as described above matter? Individual ICs and intellectual property (IP) are designed in compliance with well-established and proven design rules encapsulated in a qualified process design kit (PDK) supplied by a given foundry, and supported by automated flows and tools from the electronic design automation (EDA) industry. Designs are built using Manhattan shapes and silicon redistribution layers (RDLs). Before designs are sent to the foundry, physical verification such as design rule checking (DRC), litho-friendly design (LFD) simulation, and design for manufacturing (DFM) optimization ensures physical manufacturing success. All of this verification is targeted to (and qualified for) a specific process node at a specific foundry. With a 3D-IC package containing multiple die, that means multiple PDKs, each of which will be significantly different from the others. There is traditionally no PDK that can converge across these individual die processes while also capturing the package-specific process impacts.

An IC-style layout also brings with it assumptions about layer depths. In an IC design, everything drawn on a given layer/data type is to represent the same vertical depth (i.e., metall1 vs. metall2). This assumption breaks down when there are multiple IC components that may happen to have objects on the same graphic database system (GDS) layering, but at different depths. This discrepancy

also causes grief for connection models. IC designers are used to metal stacking (e.g., metall1 to metall2 through a via), but what happens when they connect die tops to an interposer? One die top metal may be metall6, and the other die top metal may be metall12.

Of course, it's not just physical layout that is impacted. What about design intent? In the IC space, designers generate Verilog code from the register-transfer level (RTL) abstraction, or they generate a schematic represented as SPICE input. To verify connectivity, the layout vs. schematic (LVS) process relies on active device pins. Other circuit verification, including parasitic extraction (PEX) and electrical rule checking (ERC), ensures that the circuitry implements the design's intended performance and reliability targets.

But at least the ICs have formal and automated verification! Because most package designs are still assembled manually by OSAT companies, package guidelines tend to be far less detailed and standardized, and far more flexible as far as physical implementation goes. A package design rule manual consists primarily of textual documents that describe the design intent, but there are no formalized PDKs, or design rule decks, or even layer maps/assignments. These design intent specifications are unique to each package, and are applied within each package design database, before the package assembly. In addition, OSATS typically have their choice of substrate vendors, who have their own process-specific components that must be taken into consideration. Substrate materials (laminates vs. silicon) can impact package design flow ([Figure 1](#)).

Package designers also rely primarily on manually-compiled spreadsheets to represent their circuitry. Because package design tools do not deal with data down to the transistor level, file formats such as AIF are used to represent the connections from the pins of one die to its surroundings. With no true devices, a traditional LVS tool relying on a SPICE-style netlist has nothing to check. Even the failure mechanisms to

be checked may vary, and impacts at the package assembly level, such as stress and thermal conditions, can ultimately impact the original die behaviors.

Wow, the scenario described above is pretty scary! With all these challenges and disparities, how will 3D-IC succeed? I'm sure many are thinking we need an entirely new design flow. But what would a heterogeneous package planning and design system look like? There are two primary requirements to ensure the success of heterogeneous packages:

- Designers must be able to identify and verify the connectivity between components; and
- Designers must have an original source netlist that describes the intended circuitry, and the ability to extract the package circuitry and verify it matches the design intent.

One thing the industry has learned to date—we are much better off augmenting existing IC and package flows to enable the smooth transfer of data between the disparate domains than we are trying to force all functions into a single tool environment. By building a bridge between the two domains, we enable all teams to continue to work with as little disruption to their traditional experience and workflows as possible. That means developing new methodology for physical verification that understands the different package components, their locations and transformations, and their specific process dependencies.

Preserving design intent also requires extensions of existing tools. Typical IC verification includes LVS, which requires a trusted, pre-defined source netlist. That netlist is generated from RTL with pre-characterized cell data. IC LVS requires components to connect, and forces the insertion of dummy devices where needed. But how do you communicate design intent across different substrates and databases? With spreadsheets as the primary exchange mechanism, how will designers communicate all the different types of data/information? How will it scale with increasing complexity and pin counts? What will the interaction look like between geographically diverse teams or external suppliers? What kind of cycle time will teams achieve for feedback?

Any solution the industry introduces must automate the communication of each design-specific choice of assembly structure, and be able to read and process

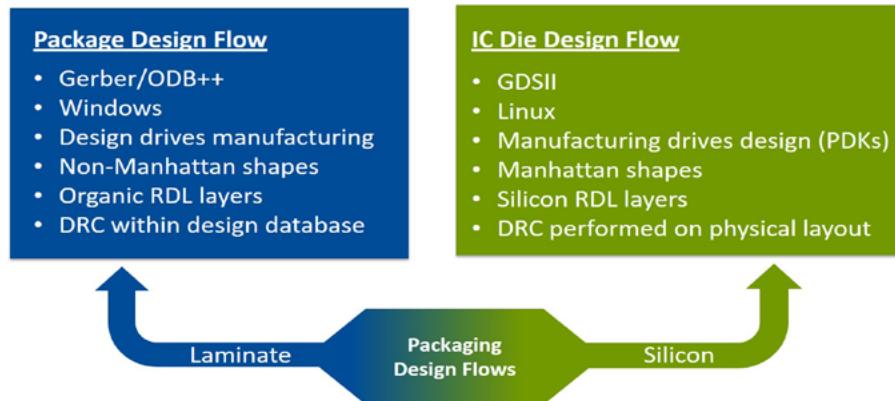


Figure 1: Substrate materials impact design flows.

data formats from both domain sets. Independent in-process verification must address the rapidly changing and complex rules of advanced packaging by supporting both physical and electrical checks, and automating checking of new or nonstandard rules. A powerful geometry processing engine combined with field solver technology is needed to process built-in checks for electromagnetic interference, signal integrity, and power integrity, as well as user-definable custom rules. The ultimate goal is to implement an automated solution that robustly handles the issues of translating to a sign-off format and checks appropriately, without requiring designers to become familiar with the different underlying formats, while also making it easy to use, fast, and accurate.

Fortunately, solutions for all of the challenges listed above are coming online. EDA companies are introducing new and enhanced tools and processes that enable 3D-IC package designers to continue using their existing toolsets while adding the functionality they need to perform such processes as package DRC, LVS, and PEX. For example, the Mentor Xpedition® SI substrate integration tool can generate system-level connectivity information in multiple formats (e.g., a spreadsheet-like netlist for package LVS, or a system-level Verilog netlist for downstream analysis like static timing analysis (STA)). The Calibre® 3DSTACK tool enables package physical verification (DRC, LVS, and LVL). To allow designers to run LVS on the package in stand-alone mode, connections from die-to-die or die-to-BGA through the package are extracted. This extracted netlist can then be compared to the netlist from the Xpedition SI tool, and used to drive parasitic extraction or other circuit analysis.

The physical connections through a passive interposer or package-level RDL can be verified for shorts or opens to the pin labels to which they connect in the layout. The Calibre xACT™ IC parasitic extraction tool can read in the required inputs from the Calibre 3DSTACK tool natively. It also provides options that can be used to prevent double-counting of parasitics. In the STA flow, the Calibre 3DSTACK tool automates the interface assembly creation (including connectivity annotation), the interface technology data creation, and the interface RC rules/models calibration as one step (i.e., one Calibre 3DSTACK run).

To further support this growth, foundries and OSATS are creating the first assembly design kits (ADKs)—the package equivalent of the IC PDK. These ADKs augment the foundry process-specific PDKs for the ICs, enabling validated design flows across a number of different targeted tools, covering issues associated with the package, the dies in the package, and the combination of the two. This formalized guidance enables the final package design, with all its components, to be validated independently from both the original design tool and any proprietary data formats before sending the package for manufacturing. The introduction of foundry-qualified ADKs for sign-off physical verification of packages, combined with new and enhanced tools that operate in both the IC and package domains, provide standardized rules, qualified tool flows, interface formats, input/output formats—all tested, qualified, and proven to produce working products. The availability of qualified ADKs will enable customers to produce higher-quality incoming designs with optimized die/package performance, while reducing overall cycle times.

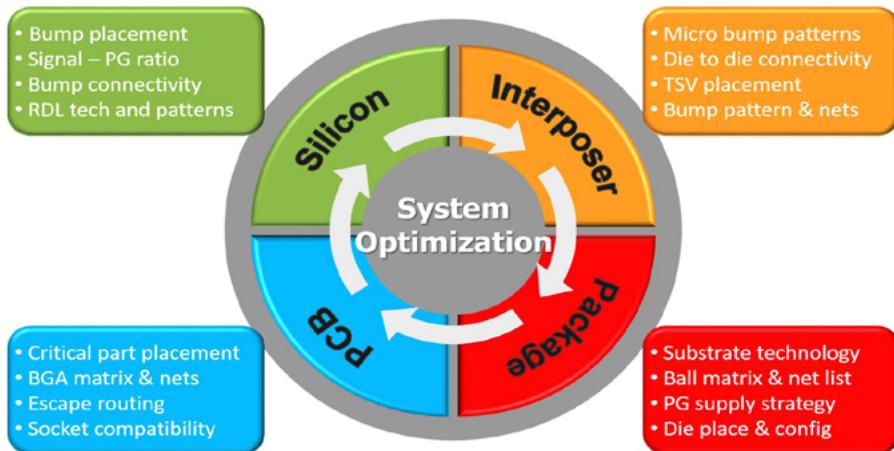


Figure 2: Heterogeneous package planning and design interdependencies drive the need for blended functionalities that support the needs of all design teams.

This blending of tool functionalities, combined with the support provided by an ADK, enables both IC and package designers to quickly and confidently adopt new package design

and verification technologies within their existing tool flows and processes (**Figure 2**). By minimizing the impact on workflows, this approach supports a faster ramp of 3D-IC products.

Summary

3D-IC packages are a fast-growing segment of the semiconductor industry. Simplifying and speeding up package verification, while ensuring full coverage and accurate results, supports and encourages the growth of existing and emerging package technologies, and the new and innovative products they can deliver.

Biography

Walden C. Rhines is CEO Emeritus of Mentor, a Siemens business. He was previously CEO of Mentor Graphics for 25 years and COB for 17 years. Prior to Mentor, Dr. Rhines was EVP, Semiconductor Group, responsible for TI's worldwide semiconductor business. He holds a BS degree in Engineering from the U. of Michigan, an MS and PhD in Materials Science and Engineering from Stanford U., an MBA from Southern Methodist U., and Honorary Doctor of Technology degrees from the U. of Florida and Nottingham Trent U.

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Production test interface solutions for mmWave and antenna in package (AiP)

By Jason Mroczkowski, Dan Campion [Cohu]

Incredibly, the number of transistors in integrated circuits (ICs) has tracked Moore's Law, doubling every two years. Equally amazing is the recent jump in IC device operating frequency into the mmWave spectrum. The emergence of 5G, next-generation WiFi protocols, and automotive radar have pushed ICs into these extreme frequency bands to take advantage of the additional available bandwidth. The need for instantaneous data transfer has driven the increasing demand for these new mmWave devices, whether for safety concerns in automotive radar, enormous data networks for 5G cellphone backhaul, or simply the expectation to instantaneously stream 4K video from your tablet to your flat screen. Historically, 6GHz was the high end of the frequency band for the majority of ICs. Operating frequencies have jumped to 30, 40, 60, and 80GHz to get the necessary bandwidth for next-generation 5G, WiFi, and automotive devices. This equates not to a doubling in frequency, but to a gigantic leap that in some cases is greater than an order of magnitude. An additional test challenge beyond the rapid growth in operating frequencies is caused by 5G applications driving an emerging need for production over the air (OTA) test of antenna in package (AiP) devices (**Figure 1**).

Today, commercially-available ICs already exist that require bandwidth in the GHz range for early 5G applications in various mmWave frequency bands from 30GHz to nearly 100GHz. However, for years many of these devices were only engineering samples confined to a characterization lab for in-depth analysis and debug. Recently, mmWave devices, initially from the automotive industry, are moving quickly into the production environments where high-volume testing is required. The quick transition from concept to production has created a bottleneck as device test plans

and interface hardware were previously not yet fully defined. The high-volume production test cells used for 6GHz devices were modified to up-convert, mix, down-convert, and measure mmWave frequencies. This resulted in a very complex and custom interface for each mmWave application.

Interface hardware has now become the critical path for mmWave IC testing. What historically was considered a high-speed load board and spring pin socket no longer provides sufficient performance for this new generation of ICs. Now, the interface must be considered holistically, including all the mechanics of connecting the IC to the tester/handler and the impact the environment has on the transfer of data at incredible speeds. In the mmWave frequency bands, minuscule changes in the environment wreak havoc on the electrical performance. Stack-up tolerances and temperature fluctuations in handler kits, docking hardware, connectors, cabling, etc., all impact electrical performance and the ability to get 100% test coverage of mmWave devices.

load board from TX to RX, or IC designers included mixing and couplers at the die level to sample the mmWave signals without interface to the outside world. Although these methods circumvent the need for a mmWave test system, it either becomes too tedious to debug or consumes valuable real estate and adds complexity to the die, thereby delaying time to market and/or pushing the IC cost upwards. Furthermore, the accuracy and reliability of the test results are not completely understood.

Testers now have first-generation up-conversion, mixing, and down-conversion add-on modules that allow a more traditional automatic test equipment (ATE) test plan. These bolt-on modules extend the frequency capability of the 6GHz tester to the mmWave region. The typical maximum bandwidth of these add-on modules is around 10GHz so they are considered banded solutions. Interface hardware can be built to be broadband, but components in the mmWave region are typically band limited, which drives custom hardware for different frequency bands.

A 5G module designed for 28-39GHz, a WiFi module designed for 56GHz to 64GHz, or an automotive radar module designed for 76-81GHz require a different add-on module for the tester. Besides being banded, these solutions are typically scalar rather than vector to keep costs down. They can measure gain or output power, but not phase. The full vector solution (a vector network analyzer (VNA) in a tester) systems exist, but the increasing radio frequency (RF) channel count of the new

devices are making full vector systems prohibitively expensive.

Although most current generation testers now have instrument options that can supply at-speed signals to the device under test (DUT), their calibration plane ends with a power meter at the test head. That means

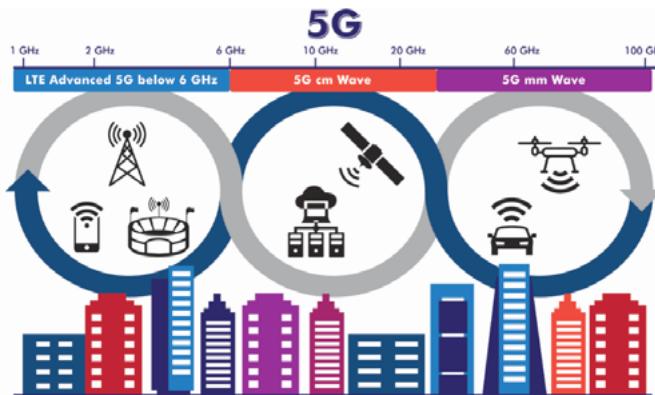


Figure 1: Diverse 5G applications span the cmWave and mmWave bands.

Early on the expectation was to bring mmWave devices to production with the assistance of either loopback on the load board or built-in self test (BIST) in the device. Because tester resources for mmWave frequencies were unavailable, test engineers included loopback traces on the

the losses associated with any hardware between the test head and the DUT must be understood, limited and calibrated out. The challenge of mmWave production test is getting sufficient electrical performance at the DUT while maintaining a reliable contact in an environment with significant and unknown stack-up tolerances. When you add the stack-ups of the test environment (docking hardware, stiffener frames, PCBs, contactors, change kits, etc.) it becomes obvious why a compliant interconnect mechanism is required. To maintain reliable contact to the DUT, the interface must include a compliant transmission line without adding significant additional loss to the system.

Traditional ATE interface hardware for 6GHz applications had enough performance overhead that a standard spring pin and high-frequency load board PCB dielectric was sufficient. Regardless of how these components were put together, the parts could be tested with reasonable yield, however, at mmWave frequencies this is no longer the case. Every component and transition must be optimized for minimal loss and best impedance match. At mmWave frequencies, testers can source +5 to +10dBm output power and must put the DUTs into saturation for 100% test coverage. DUTs in the mmWave range require approximately -5dBm input power so a 10dB loss through the system is the threshold. Furthermore, it becomes difficult to calibrate with higher than 10dB loss in the interface. The losses mask the difference between calibration standards and limit the accuracy of the calibration.

Loss adds up quickly at 80GHz. Transitions from one component to the next are a big factor. Even linear loss from traditional load board PCB architecture can quickly overcome the 10dB threshold. High frequency dielectrics have up to a 3dB per inch loss at 80Ghz. Traditional spring pin socket loss above 40Ghz quickly degrades to higher than 10dB and resonances change from insertion to insertion making an unreliable interconnect. Finally, SMA connectors are mode limited to around 27GHz so cable sourcing may need to change.

At mmWave frequencies, an electrically transparent interconnect is difficult to achieve, but with some creative design practices it is possible to get sufficient electrical and mechanical performance to test beyond 100GHz. Thinking outside the box of the traditional PCB and socket

structure is required. Minimizing the number of impedance discontinuities is a priority. Bypassing the PCB and directly interfacing with the compliant interconnect eliminates the launch into and out of the PCB. Although the PCB is a great interface for high-density low-frequency and power signals, the dense environment extends line lengths and limits optimization at mmWave frequencies. Furthermore, the standard spring pin socket is not a reliable option at mmWave frequencies. For the high-speed signals, a single-piece compliant interconnect, such as Cohu's xWave technology (**Figure 2**), is a better option as it eliminates resonances created by the length of the pogo pin and inconsistencies on account of the changing interaction between the probe components. Combining the socket and PCB into one single compliant transmission line provides a low-loss, well-matched interface from the tester to the DUT with minimal discontinuities.

The 5G revolution also includes AiP devices that require OTA test solutions at these mmWave frequencies. OTA test setups are complicated further by application

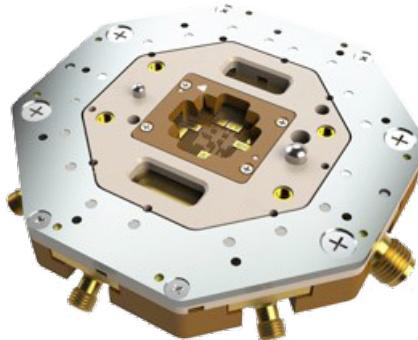


Figure 2: Cohu xWave contactor/probe head for production test to 100GHz.

variables, such as near field/far field, antenna integration level, and radiation orientation. The position of the test interface antennae from the device in the test setup could vary between a few millimeters to tens of centimeters depending on whether it is near/far field and the center frequency. These antennae can be integrated at the die, package, or module level. The radiation direction of the antennae can also be oriented to come out of the ball/pad, lid, or side of the device or module. These variables drive the test cell configuration beyond the norm and blur boundaries between the tester, contactor/probe head, and handler/prober to meet the test requirements.

mmWave test interface solutions

Package and wafer test interface solutions exist today for mmWave devices. The front runners of these solutions are membrane, conductive elastomer, and hybrid lead frame based. Because mmWave devices are just now reaching production volumes, the mmWave interface solutions are only now being exercised in production environments. In-depth comparisons on longevity, maintainability and performance are being done today. Each available solution has advantages and disadvantages.

Conductive elastomer solution. Conductive elastomers minimize the inductance of the socket with extremely short interconnects, but they still require a PCB interface for the mmWave signals. They are typically combined with small daughter cards to provide sufficient electrical performance for mmWave frequencies. Elastomers have limited compliance, a relatively short lifetime (typically less than a couple hundred thousand test cycles), and their characteristics vary widely with temperature. These limitations inhibit the technology from being used in production environments where temperature fluctuations and stack-up tolerances can stress the elastomer.

Membrane solution. A membrane solution includes an impedance-controlled flex circuit. The mmWave signals bypass the PCB and transition from the flex circuit into a semirigid coaxial cable and/or an RF connector. The low frequency and power signals transition from the flex circuit into a traditional PCB. Membrane solutions create an impedance-controlled path from the test equipment to the DUT, but they are fragile and have limited compliance, which can lead to reduced lifetime. Membrane solutions are often used in wafer test applications where tolerance stack-ups are reduced and precise prober automation reduces the wear and tear on the interface.

Hybrid solutions. When considering the harsh production environment of test, a lead frame and spring pin hybrid solution, such as Cohu's xWave technology (**Figure 2**), offers electrical and mechanical advantages. The xWave contactor or probe head utilizes patented hybrid contacting technology to optimize RF performance and provide robustness for production testing of the most challenging cmWave and mmWave devices. An impedance-controlled lead frame connects the mmWave signals while standard spring pins connect low-frequency and power connections. The

hybrid solution embeds coplanar waveguide lead frame structures in the socket with coaxial waveguide connections to the test equipment. The traditional spring pin socket and PCB remains for the low frequency, control and power signals. This approach combines the robustness of the traditional spring pin/PCB interface while eliminating the discontinuities for the mmWave signals. The result is an interface solution that can withstand tri-temp high-volume production environments and last greater than 1.5 million cycles on a handler or greater than 3 million cycles on a wafer prober. The hybrid nature of the xWave technology has also enabled the integration of patch or horn antennas into the contactor

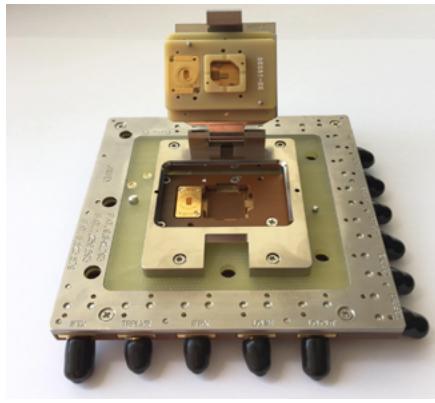


Figure 3: Cohu xWave contactor for OTA testing of a 60GHz UltraGig single-chip integrated antenna in package (AiP).

(**Figure 3**) either above, below, or beside the DUT depending on the radiation direction(s). Cohu's entire test cell domain knowledge also allows for the seamless integration of these solutions into the tester or handler as needed to provide optimized solutions (**Figure 4**).

Interface design

Regardless of the interface technology applied, a system-level approach to interface design is required. The socket/contactor cannot be considered alone. Interactions with the PCB, probe card, connectors, cables, waveguides, etc., have an impact on performance that cannot be ignored. Applying rule of thumb RF design practices is insufficient when designing mmWave interfaces at 80+GHz. Complex

interactions create unforeseen resonances that cannot be predicted without 3D electromagnetic simulation (**Figure 5**). The best approach is simulation of the entire path from the tester to the DUT to confirm electrical performance before fabrication. Mechanical tolerances must also be considered. Building worst-case tolerances into the simulation models provides the most conservative result and provides the best probability of first-pass success. Electrical and mechanical engineering co-design is required and needs to consider mechanical feasibility and the impact on mmWave performance. Without this approach, there is little chance to meet the window of opportunity to bring these ICs to market.

handler ↔ contactor ↔ tester

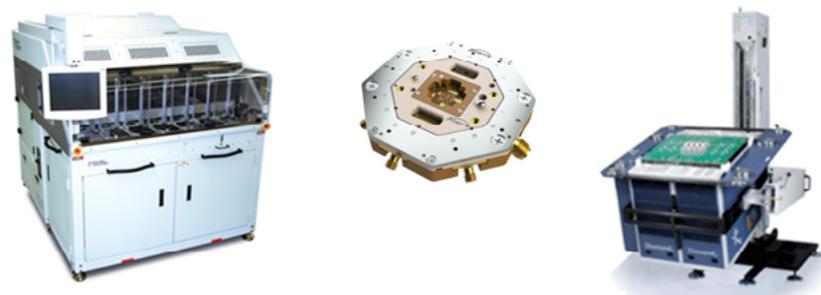


Figure 4: Cohu enables seamlessly integrated solutions for the most challenging 5G applications.

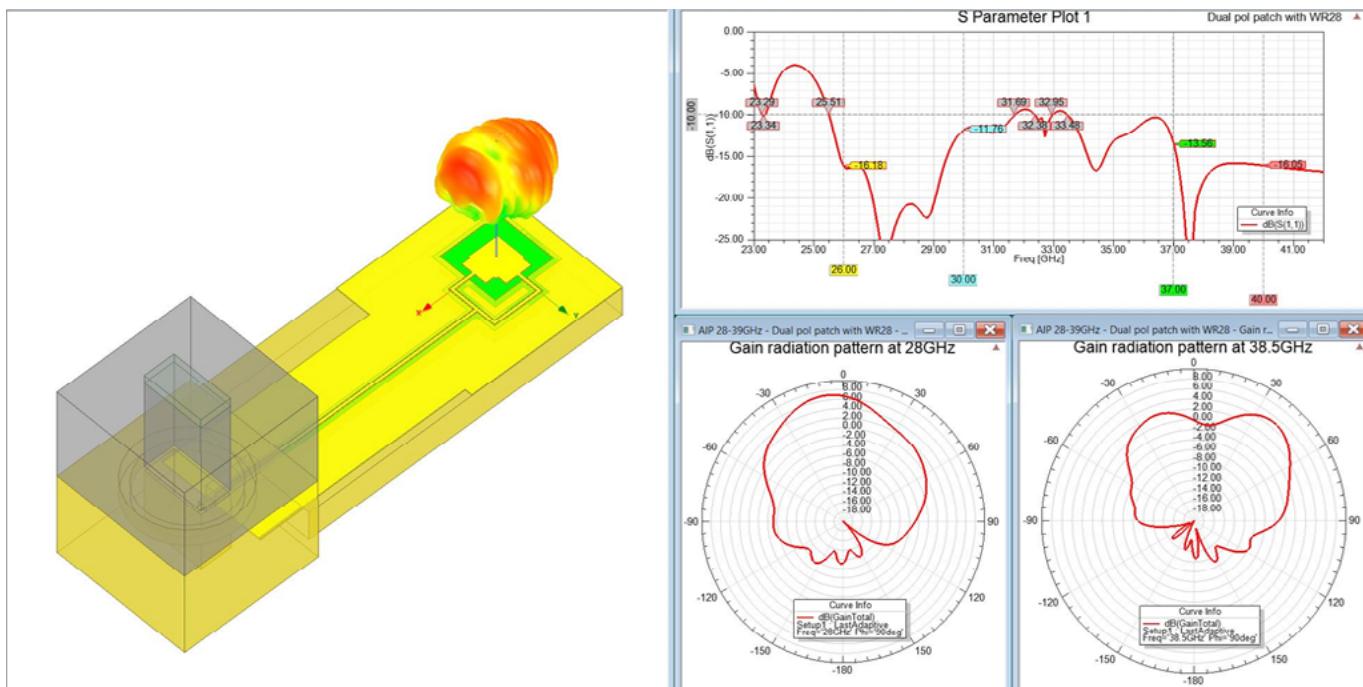


Figure 5: Cohu xWave OTA dual-band dual-polarization patch antenna 3D electromagnetic simulation.

Summary

Moving forward, the challenge will be lowering the cost of test for mmWave devices. Today it is conceivable that the cost of test is 80% the cost of the IC for first-generation 5G devices. This situation cannot be sustained. As volumes of mmWave devices increase, there will be some natural economies of scale that drive down costs. More efficiently designed test cells and interface hardware will need to complement the economies of scale to bring the cost of test down to palatable percentages within the coming years.

Contacted production test at mmWave frequencies is the norm today. Metal transmission lines connect the tester to the DUT for up to 80GHz testing. Ultimately, these mmWave devices are connected to an antenna module that communicates wirelessly to the outside world. However, space constraints and cost are pushing vendors to integrate antenna arrays directly into the semiconductor package or substrate. The emergence of antenna in package (AiP) is changing the landscape of test. AiP requires an over the air (OTA) mmWave interface to the DUT. Embedding a wireless interface in the ATE environment is nontrivial. Test vendors, such as Cohu, are embedding horn antennae and patch antennae into the contactor, test head and/or the handler interface.

As more devices move into the mmWave frequency bands, test infrastructure may morph into very different form factors. Although a few devices incorporate mmWave components, today the trend toward the connected world will continue to push the limits of existing speeds and bandwidths. This trend will require new technologies in test to confirm functionality and reliability of these devices. Traditional transmission line topologies will be obsolete. Waveguides will replace cabling and PCB traces, and antennas will replace contacted interfaces. It is foreseeable that semiconductor devices will no longer incorporate physical contacts to provide power or to communicate with the external environment. What will the ATE test environment look like then?



Biographies

Jason Mroczkowski is Director RF Product Development and Marketing in the High Performance Contactor – Interface Solutions Group at Cohu. He graduated from the U. of Minnesota with a BSEE and holds an MBA from the U. of St. Thomas. He began his career in Research & Development where he developed high-frequency interconnects and earned multiple patents for mmWave applications.

Dan Campion is the General Manager of the High Performance Contactor – Interface Solutions Group at Cohu.

He has 18 years experience within the semiconductor industry in test engineering, program management, and business leadership. Dan has both BSEE and MBA degrees from the U. of Minnesota.

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New test methodologies for 5G wafer high-volume production

By Daniel Bock, Jeff Damm [FormFactor, Inc.]

Companies developing 5G technologies are racing to develop the first chipsets in order to set the standard of deployment and be the leader. While initial standards for 5G were set at the end of 2017 [1], and there are ideas about the applications of 5G (Figure 1), it is still unclear how exactly it will all come together. This uncertainty demands unprecedented levels of collaboration and partnership. This article explores the challenges and changes in test methodology of 5G devices, and showcases the results of a collaboration with Intel [2].

5G brings three technical improvements/enhancements when compared to the current deployed, 4G standard:

1. Greater available bandwidth, increasing to more than 4GB per connection per month from today's less than 1.5GB per device [4].
2. Lower latency, for critical applications to be more responsive [5].
3. The ability for up to 1 million devices (such as sensors and smart devices, per square kilometer [6]) to be connected to the network.

Some of the resultant solutions to meet these requirements for 5G include:

- The opening of millimeter wave (mmW) frequencies: ~30GHz and above;
- The increase in the number of mobile sites to allow for more devices [7]; and
- The deployment of edge cloud nodes so that data doesn't always need to go back to the central node.

Because of all of these changes, the full network infrastructure will need to be upgraded. Prior to 5G, the upgrades were primarily around changing from analog to digital in the first few generations, as

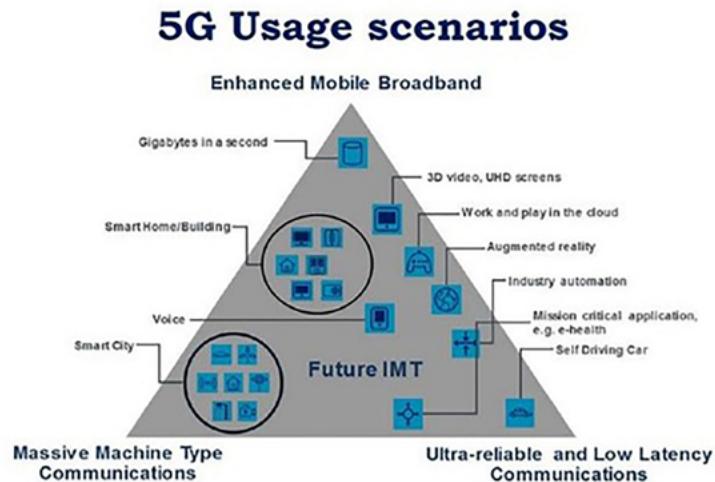


Figure 1: Usage scenarios for 5G [3].

well as improving modulation techniques [8]. "So the scale of 5G when compared to previous upgrades to the infrastructure is much larger than seen in the past because of the technology extensions. However, as Scott Fulton points out, "5G is a capital improvement project the size of the entire planet, replacing one wireless architecture created this century with another one that aims to lower energy consumption and maintenance costs [9]."

In order to provide the chips required for this change in the landscape, there will be a large number of changing requirements in wafer test that come out of these architectural requirements. FormFactor partnered with Intel to investigate these changes, and tested one such example of a new test methodology [2].

The history of mmW testing

Historically, millimeter wave testing of wafers was relegated to labs and low-volume production for defense, aerospace and other somewhat-exotic applications. This is because of the low transmission range, high cost of generating RF signals with IC

chips, and low data rates that were required. Therefore, wafer high-volume manufacturing (HVM) production floors topped out at 6GHz because mobile phones were the devices using a majority of the RF ICs.

Millimeter wave testing, however, has been moving into high-volume production because of automotive radar and high-speed digital parts that require the increased performance gained with higher frequencies. That is either with more accurate resolution of a nearby vehicle or obstacle, or more data being moved in data centers and over fiber connections. Some of the challenges identified in automotive test [10] include:

1. Power accuracy;
2. Maintaining RF calibration of the test equipment (and final RF signal path);
3. Setting appropriate test limits at these higher frequencies;
4. Millimeter "anything" is just more expensive; and
5. Test engineering is not familiar with mmW testing.

Following the path laid by automotive radar applications, 5G is going to be pushing semiconductor test developments and will expand them because of the unique challenges with higher channel counts and good signal integrity. This article provides what manufacturers—and in particular, test engineers—need to know about changes in testing for mmW wafers used in 5G. It reviews some of the changes that will be required to support wafer testing in the bands starting at 26GHz and all the way up to the 67GHz range in HVM, and will discuss the advancements in probe card technology that enable multi-site production-level testing.

Test protocols that are going to be developed for 5G will need to handle multi-site calibration and testing with minimum cross talk, as well as handle the large number of RF channels due to phased-array antennas for beam forming. Essentially, testing needs to be designed specifically for multi-site production tests with the limited number of tester channels that are available. In short, production testing of these parts has just gotten dramatically more expensive, with costs easily increasing by a factor of 2 (or more).

The new challenges for 5G production-level test

The emergence of 5G is changing the landscape for RF production compared to what we saw over the past 30-40 years. We explore the major requirements below.

Higher frequencies with more channels per device. The first big shift that is affecting the test cell is the new, higher speed channels operating up to almost 70GHz. Traditional HVM wafer testers are capable up to 6GHz, which covered all of the bands being used by 4G. In addition, these testers could be extended to higher frequency with custom extenders, adding 1-2 channels at these frequencies. The 5G devices that are being developed will include up to 64 RF channels per device under test (DUT) in the highest channel count. This means that a traditional tester is not the best solution because of the frequency limitations. Semiconductor manufacturers are requesting new testers with more channels that are more capable than current off-the-shelf testers. While this is a possible solution, it should also be noted that any tester that is developed cannot be too expensive as production test will become economically unviable. Adding higher

frequencies with the large channel counts could feasibly increase tester cost more than 10x.

Increased parallelism. Increased parallelism also leads to the need to perform multi-site RF test. Currently, mobile RF system-on-chips (SoCs) are tested at x4 multi-site wafer test, with a desire to get to x8 fully parallel test when possible. This still holds true with 5G devices. However, the x8 parallelism pushes the total channel count upward to more than 256 RF channels on many of the devices being developed today. Making a tester that could connect to this number of RF channels is not feasible for two reasons: 1) cost, and 2) space limitations within the test floor. Without increasing the channel count in the tester, there are alternative methods to increase the total channels that can be tested. These methods include using baluns, power combiners, switches, and loopback test, to name a few.

Verifying signal accuracy. The last requirement for 5G parts is accurate RF test in the test cell. This is not only to validate RF performance, but to prevent packaging bad devices. With most of the current advanced packaging technologies that can support RF being quite expensive, yield of more than 95% is required from a wafer where it would be economically viable to not do wafer RF test and only do final package test.

However, the high-speed signals in 5G mean that it is more sensitive to process variation, especially in the initial stages of technology development. That means that yield will be well below 95% for a period of time, therefore making it impossible to remove wafer RF test.

In order to support high signal integrity, measurement errors—such as impedance mismatch, cable loss, and RF source variation over time—that might be considered insignificant at lower frequencies can become important at millimeter wavelengths. Using a simultaneous multi-site calibration during multi-DUT testing provides the highest electrical accuracy because all the DUT RF channels are in a known and controlled state.

RF calibration is used to move the measurement reference plane from the

tester to the device in order to obtain the best device measurement and to remove the effects of the test fixture. This is done by measuring RF on a calibration substrate (**Figure 2**). In order to accurately measure the effects of the test fixture, the calibration substrate should mirror the multi-site layout of the probe card.

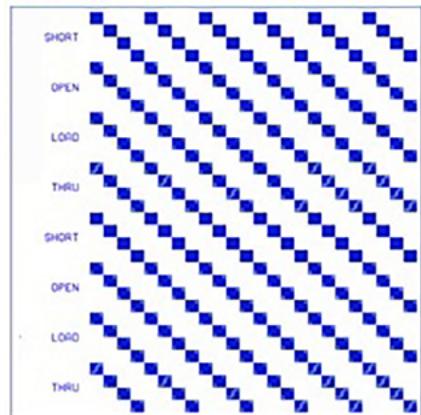


Figure 2: Example of a custom multi-DUT calibration substrate for SOLT.

For RF calibration, there are a number of options that use a combination of RF standards (**Table 1**). For lower frequencies, short-open-load-thru (SOLT) is a standard calibration technique. For highest

Test Method	Wafer Test Cost	Functional Test Coverage	Full RF Bandwidth Test	Probe Card Complexity
No Wafer Test	● / ●	●	●	●
DC Test	●	●	●	●
Full Channel	●	●	●	●
Loopback	●	●	●	●
Baluns, Switches, Combiners	●	●	●	●
Antenna Coupling	●	●	●	●

Legend: Green = Best, Yellow = Acceptable, and Red = Unacceptable.

Table 1: Comparison of six different wafer test methods.

accuracy, SOLT requires good definitions of all of the standards. It is possible to use short-open-load-reciprocal (SOLR) as an alternative as long as channel-to-channel cross talk is less than 20dB. That is because when the cross talk reaches the level of less than 20dB, the SOLR algorithm gets confused and will not be able to properly calculate the thru length. Therefore, in such cases, it is best to go back to SOLT.

As the frequencies get higher, an alternative model—multi-line reflect thru (mTRL)—is used. mTRL was developed by NIST, and is considered to be the gold standard in RF calibration. However, it is difficult to use with probe cards because of the fixed distance separation between the probe tips.

Another thing to consider in RF calibration is that when there is a lot of “noise” in the post-calibration verification, it could be from cross talk as well. In order to reduce this, it has proven useful to use sweep averaging and a reduced intermediate frequency (IF) bandwidth (BW) on a vector network analyzer (VNA). This reduces the effects of the cross talk signals, narrowing the acceptable signal being measured. This brings the measurement into a +/-0.1dB of 0 in a post-calibration verification, which is an acceptable level in production test.

Production test methods for 5G

In order to evaluate the deficiencies of current methods for use in a 5G production wafer test floor, we considered four primary metrics of a test method:

1. Wafer test cost;
2. The comprehensiveness of the functional test coverage for the DUT, requiring all channels to get back to the tester;
3. The ability to do full bandwidth test, where the signals do not need to get back to a tester channel; and
4. The complexity of the probe card, which then results in an increased cost for the consumable.

We then looked at six possible test methods (**Table 1**). As can be seen, no single method is fully capable today and requires some amount of compromise. All methods were evaluated using FormFactor’s Pyramid Probe probe card technology.

All of the methods listed above are fairly well understood and have been used for years. The only method that is new for wafer test is antenna coupling. Antenna coupling demonstrates the ability to do power combining at a large bandwidth (much larger than most combiners and baluns) and requiring less area and no power, like a switch. This results in a lower cost of test impact when compared to the other methods, which all have at least one red column. The following

sections will go over the antenna coupling method, including a technical description on how the method works, as well as test structures being evaluated, and then finally with a test that was done with Intel.

OTA testing using antenna coupling

When using antennas, it should be noted that there are different regions of what the electromagnetic field looks like in relationship to the distance that it is away from the antenna (**Figure 3**). Traditional over-the-air (OTA) testing is done in package test, where test engineers place a horn antenna into the tester at the far-field region of the antenna, and where electromagnetic radiation is the dominant type of energy transfer. However, the use of the antenna coupling method for wafer test places the antenna much closer, in the near-field reactive region at a distance of <100μm, where non-radiative energy transfer is the dominant type of energy transfer.

Although the antenna is not forming a true antenna beam pattern on account of the closeness of the antenna to the DUT, it does provide some benefits. For one thing, most antennas operate in a narrow band, with a fractional bandwidth (BW) of maybe 10-20%. Operating in the reactive region allows for the BW of performance to be much larger, closer to 80%, or more. In addition, the advantage of placing the antenna in the membrane is that it can be used also for antenna power combining with several channels, and arbitrary antenna designs can easily be designed within the membrane.

In order to evaluate the capability of the Pyramid Probe for OTA testing, a test Pyramid Probe was designed with two different types of antennas: a ring antenna and a dipole antenna (**Figure 4**). In addition, there were two different sizes made of each type, to evaluate how the performance changes with size. In order to simulate the DUT, a calibration substrate was

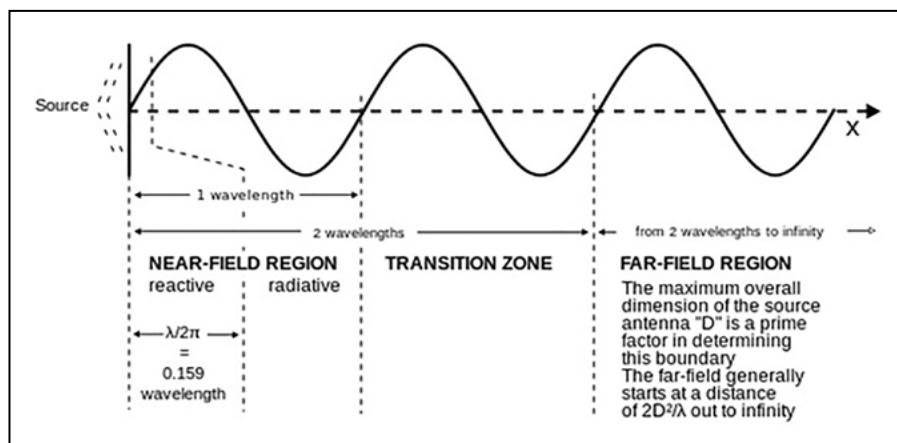


Figure 3: The relationship of distance to the type of field measurements that are done using an antenna. The wafer test antenna coupling method sits in the near-field, reactive region [11].

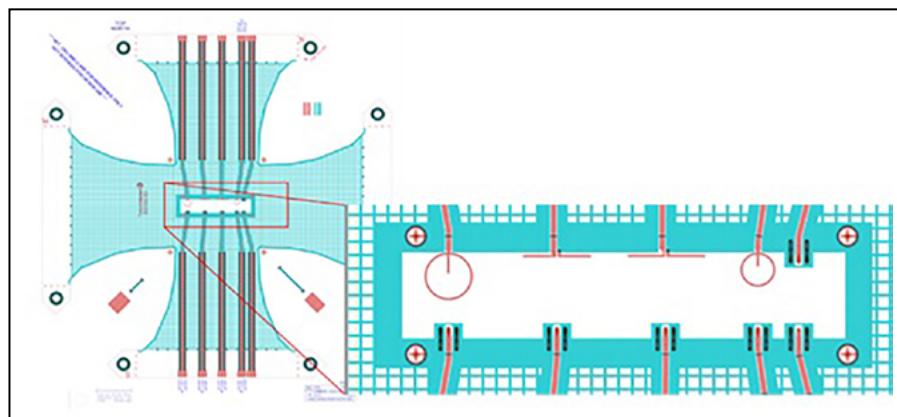
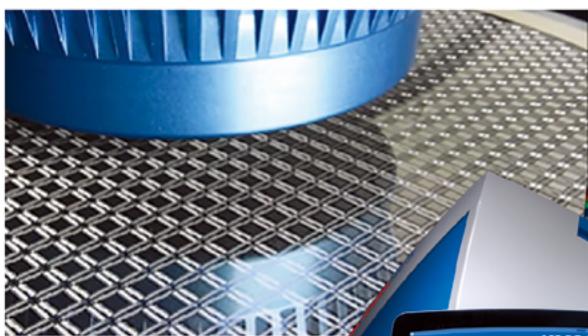
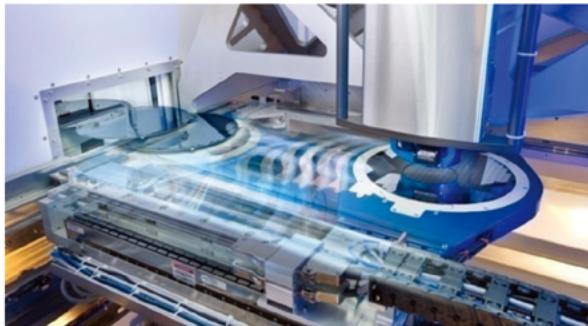


Figure 4: The test membrane designed by FormFactor for evaluation of in-membrane antennas. It included two different types of antennas (dipole and ring), with each having a large size and a small size.

XM8000

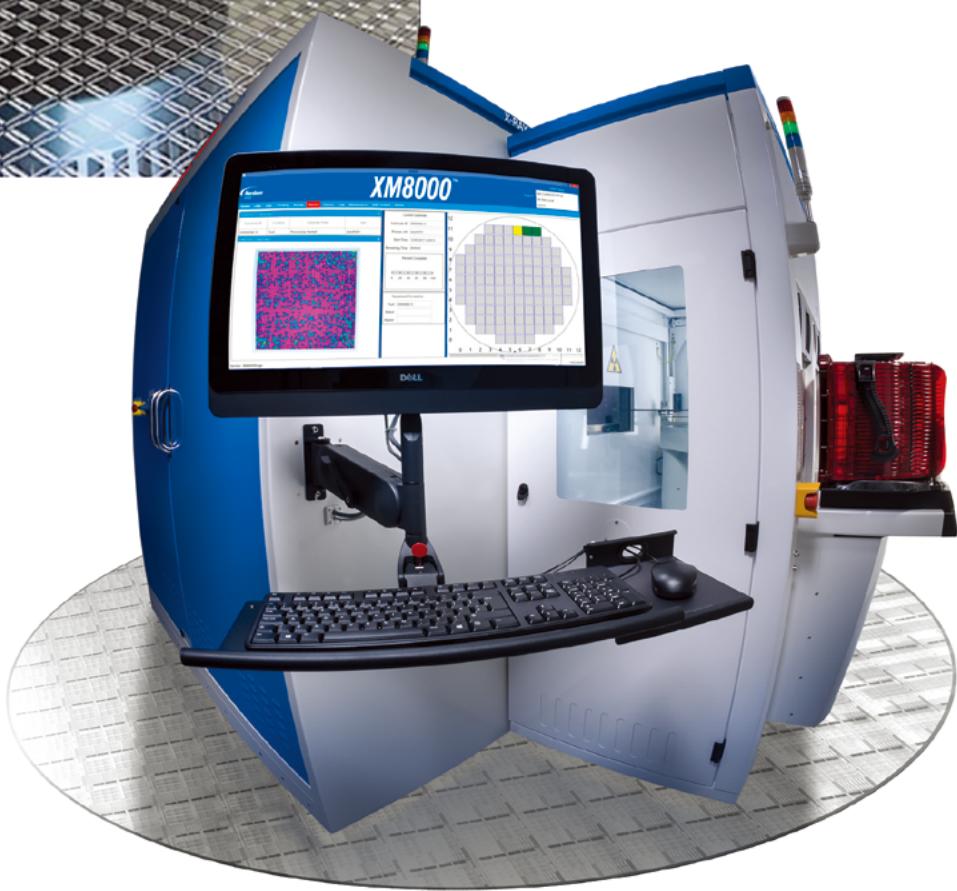
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designed with the same antennas on it. The results (**Figure 5** and **6**) demonstrate that the antennas have good signal-to-noise ratio, as well as operating ranges from about 5GHz to 50GHz with flat performance.

Another test was to use the ring antenna in the membrane, but place a pad on the calibration substrate and see if a pad on the DUT could provide a large enough signal to be detected (i.e., does the DUT need to have an antenna on it for measurement, or can a pad be used without any additional structures). The results (**Figure 7**) indicate that it is possible to receive a signal, but the response is not as flat as with the antennas on the calibration substrate.

OTA testing with 5G devices

In a joint collaboration with Intel to develop a test methodology for their 5G RF-SoC devices, OTA testing was explored because it could provide simpler power combining in the dense RF-SoC

Probe touchdown	Transmit Power from Same DIE (dBm)		
	1/4λ to Ring Antenna	Ring Antenna only	Fully Conducted Path
1	-63.27	-86.67	-38.593
2	-63.169	-85.95	-38.594
3	-63.8	-86.68	-38.588
4	-63.825	-86.62	-38.589
5	-63.636	-85.63	-38.59
6	-63.687	-85.51	-38.597
7	-63.793	-86.62	-38.602
8	-64.043	-86.23	-38.61
9	-64.728	-85.14	-38.616
10	-64.673	-85.98	-38.615
11	-64.955	-86.69	-38.634
12	-64.866	-85.43	-38.649
13	-65.111	-85.95	-38.648
14	-65.785	-84.65	-38.698
15	-65.826	-84.25	-38.711
16	-65.854	-84.13	-38.757
17	-65.748	-84.32	-38.762
18	-65.831	-84.61	-38.766
19	-65.696	-84.21	-38.753
20	-65.692	-84.74	-38.778

Table 2: OTA testing for 5G devices using three different methods.

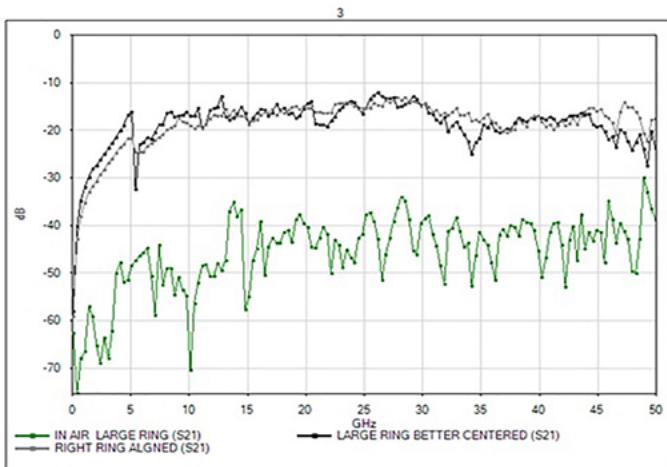


Figure 5: Measurements of the antenna coupling of the ring antenna. The green line denotes the noise floor of the test system.

device layouts [2]. A test device was selected by Intel, and a membrane was designed for this device that then included three different measurement paths:

1. Standard conduction – direct electrical connection of the DUT to the tester;
2. One-quarter wave antenna in the membrane that connected to the solder ball, which transmitted to a ring antenna in the membrane, which then took the signal to the tester; and
3. Ring antenna directly above a BGA solder ball.

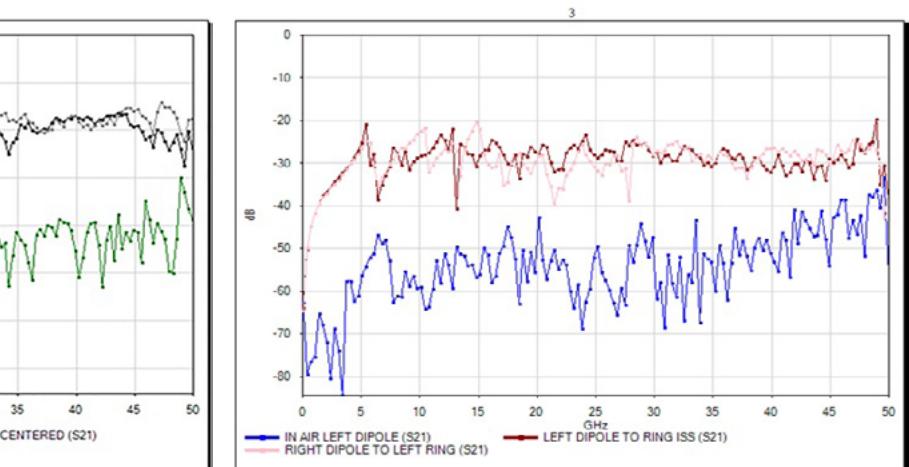


Figure 6: Measurements of the antenna coupling of the dipole antenna. The green line denotes the noise floor of the test system.

In order to show repeatability, each method was done with 20 touchdowns on the same DUT. Each method showed a high amount of repeatability (**Table 2**). Although the power level is lower in the quarter wave to ring antenna method (as well as solder ball method to ring antenna) when compared to the traditional conduction method, the ability to power combine multiple channels provides some benefits in reducing the complexity of the active circuitry and cost of the test setup while still providing a good signal for known good die testing. In

addition, a measurement of a single tone going through the system showed both a clean, unmodified signal, as well as high repeatability from the first to last touchdown (**Figure 8**).

The final test evaluation of the antenna test method was then to look at the signal during a 12-tone, linearity measurement to check for harmonic distortions. The signal was shown to have no cross-mode effect, with a highly linear response across the full band, as well as a signal that was exceptionally clean (**Figure 9**).

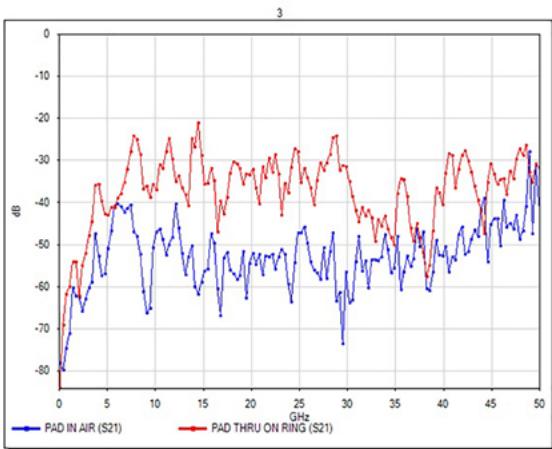


Figure 7: Measurement using a ring antenna to receive a signal from a pad on the ceramic substrate. The blue line is the noise floor.

Summary

The development of 5G is requiring a paradigm shift in test methodology with a tight relationship between the device manufacturers and test hardware manufacturers. Millimeter wave testing and OTA have increased challenges and a corresponding impact on yield. An exponential increase in RF channels is driving the collaborative development of production test methodologies in order to establish 5G deployment standards. Our collaboration with Intel to develop a new test methodology for 5G exemplifies a path that semiconductor manufacturers could pursue in full production.

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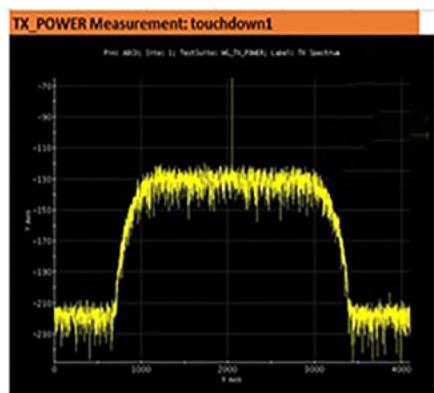


Figure 8: Single-tone measurement of the antenna method showing repeatability. The measurement on the top was on the first touchdown, while the one on the bottom is on the 20th touchdown, on the same device.

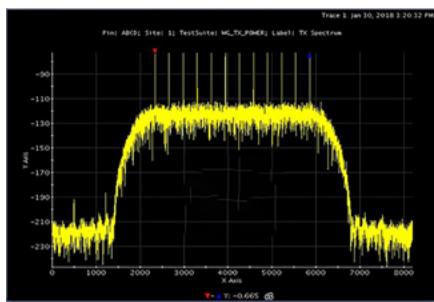


Figure 9: Evaluation of a 12-tone linearity measurement.



Biographies

Daniel Bock is an RF Applications Specialist at FormFactor, Inc. He received his PhD in Physics at Carnegie Mellon U. in 2006. He went to work in 2007 with Physical Optics Corp. in Torrance, CA, where he was awarded more than \$4M in SBIR research grants from the Department of Defense, developing innovative high-power tunable filters. Since he joined FormFactor (then Cascade Microtech) in June of 2012, he has been focusing on mmW RF test solutions including RF Calibration in a HVM environment, RF design of structures, and the requirements for automotive radar and 5G; email Daniel.bock@formfactor.com

Jeff Damm is a Senior Product Applications Engineer at FormFactor working with mmWave probe technology. He began his career in research and development at Dexcel, Inc., working with GaAsFET waveguide low-noise amplifiers. He next joined Tektronix GaAs research group, and then co-founded Triquint Semiconductor focusing on GaAs/pHEMT/HBT RFIC product design and development group. Prior to joining FormFactor, Jeff worked in the development of mesh-network wireless instrumentation at Lizard Monitoring, a developer of temperature sensing network systems for retail food chains. He graduated from Oregon State U. with a BS in Electrical & Computer Engineering.

Redistribution layers for heterogeneous integrations

By John H. Lau [ASM Pacific Technology, Ltd.]

Heterogeneous integration uses packaging technology to integrate dissimilar chips with different functions from different fabless houses, foundries, wafer sizes, and feature sizes into a system or subsystem. This situation differs from solutions such as system-on-chip (SoC), in which most functions are integrated into a single chip using a finer feature size. For the next few years, we will see more of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, and/or cost [1]. How should these dissimilar chips talk to each other, however? The answer is redistribution layers (RDLs). In this study, the fabrications of RDLs for heterogeneous integrations are presented. Emphasis is placed on the RDLs for heterogeneous integration on: A) organic substrates, B) silicon substrates (through-silicon via (TSV)-interposers), C) silicon substrates (bridges), and D) fan-out substrates. Some recommendations will be provided. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance. The subsections below follow the alphabetic labels above.

A: RDLs for heterogeneous integration on organic substrates

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of conventional low-cost high-density substrates and build-up organic package substrates by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up layer, shrinking the dimensions of the metal line width and spacing, and reducing the pad size and pitch.

A1: IBM's SLC technology. More than 25 years ago, IBM in Japan at Yasu invented the surface laminar circuit (SLC) technology (Figure 1 [2-4]). SLC formed the basis of today's very popular low-cost organic package substrates with build-up layers vertically connected through microvias [5] to support heterogeneous integrations such as flip chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo-sensitive epoxy and the conductor plane of copper plating, i.e., using a semi-additive process (SAP). In general, a package substrate with twelve

layers [e.g., two core layers and ten build-up layers (5-2-5)] and a 10 μm line width and spacing are more than adequate to support most of the chips.

A2: Shinko's build-up with thin-film layer. In 2013 and 2014, Shinko proposed making thin-film layers (down to 2 μm) on top of the build-up layer of a package substrate and called it "i-THOP" substrate [6,7] intended for high-performance applications. (See [8] for more details.)

A3: Cisco's organic interposer. Figure 2 shows a 3D heterogeneous integration designed and manufactured with a large organic interposer with fine-pitch and fine-line interconnections by Cisco [9]. The organic interposer has a size of 38mm x 30mm x 0.4mm. The minimum line width, spacing, and thickness of the front side and back side of the organic interposer are the same and are, respectively, 6 μm , 6 μm , and 10 μm . It is a 10-layer high-density organic interposer (substrate) and the via size is 20 μm . The major manufacturing steps for making the organic interposer are the same as those for the organic build-up package substrate. These include [9]: a) plating through-hole (PTH) generation and

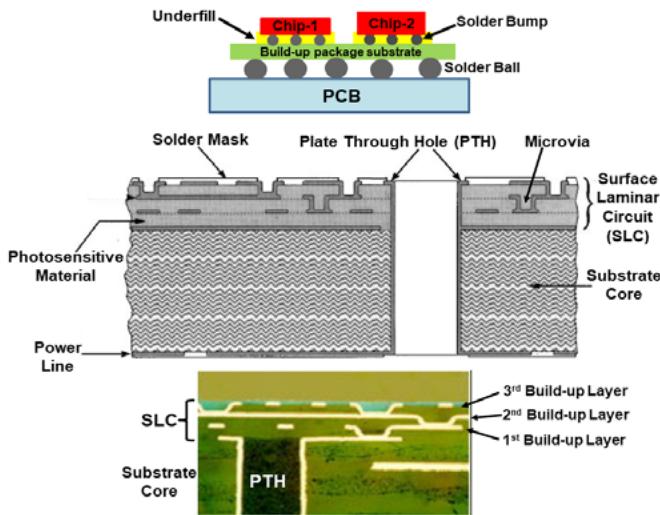


Figure 1: Heterogeneous integration on organic substrate (IBM SLC).

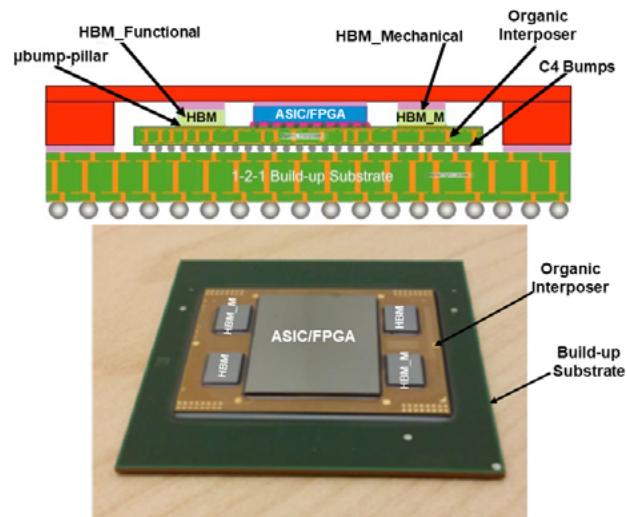


Figure 2: Heterogeneous integration on organic substrate (Cisco organic interposer).

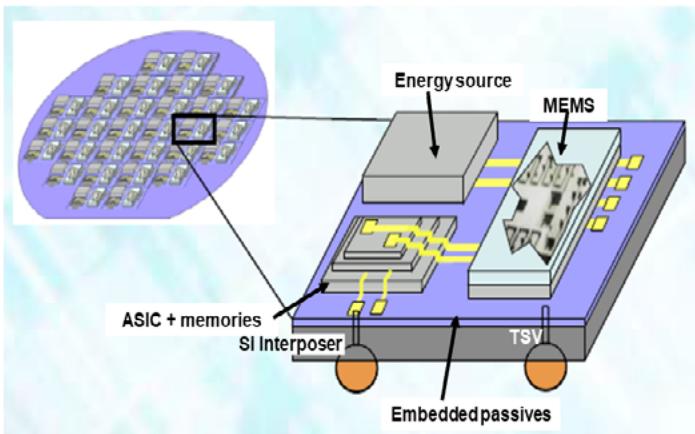


Figure 3: Leti's system-on-wafer (SoW).

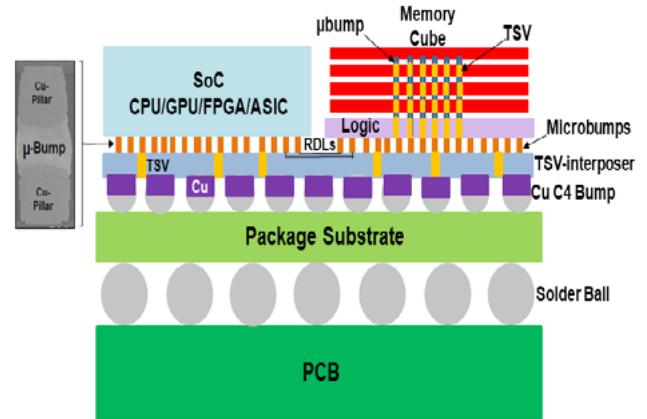
filling for the core layer, b) circuitization of the core layer, and c) building Cu wiring layers on two sides of the core layer with SAP. A high-performance application-specific IC (ASIC) die measured at 19.1mm x 24mm x 0.75mm is attached on top of the organic interposer along with four high-bandwidth memory (HBM) dynamic random access memory (DRAM) die stacks. The 3D HBM die stack with a size of 5.5mm x 7.7mm x 0.48mm includes one base buffer die and four DRAM core dice that are interconnected with TSVs and fine-pitch micro-pillars with solder-cap bumps. The pad size and pitch of the front side of the organic interposer are 30 μ m and 55 μ m, respectively.

B: RDLs for heterogeneous integration on silicon substrates (TSV-interposers)

Heterogeneous integrations on silicon substrates are for multi-chips on silicon wafer or system-on-wafer (SoW). The assembly methods are usually flip-chips-on-wafers with TSVs with mass reflow (Figure 24a of [10]) for pitch \geq 50 μ m or with thermocompression bonding (Figures 24b, 24c, and 24d of [10]) for very fine pitches ($<50\mu$ m). In general, the RDLs for heterogeneous integration on silicon substrates are for ultrafine line width and spacing (down to submicron) applications.

B1: Leti's SoW. One of the early applications of SoW is given by Leti [11,12] as shown in **Figure 3**. It can be seen that a system of chips such as ASIC and memories, power management ICs (PMICs) and microelectromechanical systems (MEMS) are on a silicon wafer with TSVs. After dicing, the individual unit becomes a heterogeneous integration system or subsystem on a silicon substrate with RDLs and TSVs (which is called a TSV-interposer) and can be attached on an organic substrate, or stand alone.

B2: TSMC's CoWoS and CoWoS-2. Later, TSMC put SoW into production and called it chip-on-wafer-on-substrate (CoWoS) for the TSV-interposer size = 800mm² [13-15] and CoWoS-2 for the TSV-interposer size = 1200mm² [16] as shown in **Figure 4**. It can be seen that the TSV-interposer with RDLs is supporting the SoC and the HBM cube and is attached to an organic package substrate. **Figure 5a** shows the TSMC/Xilinx sliced field-programmable gate array (FPGA) CoWoS [13-15]. It can be seen that the TSV (10 μ m diameter) interposer (100 μ m deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between the sliced FPGA chips are connected mainly by the 0.4 μ m pitch (minimum) RDLs of the interposer. **Figure 5b** shows Nvidia's



Underfills are applied:

- Between the TSV-interposer and SoC/Logic
- Between the TSV interposer and package substrate

Figure 4: TSMC's CoWoS-2 structure.

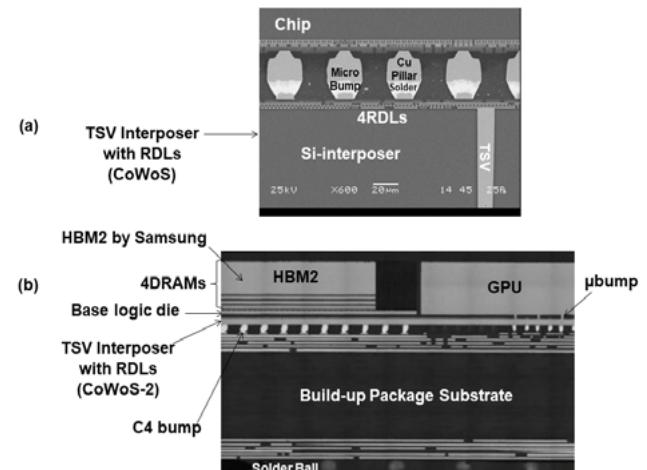


Figure 5: a) TSMC/Xilinx CoWoS structure; and b) TSMC/Nvidia CoWoS-2 structure.

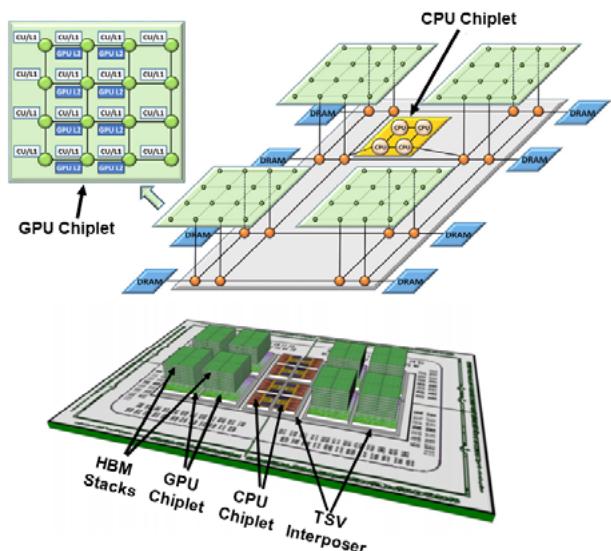


Figure 6: UCSB/AMD GPU chiplets, CPU chiplet, and HBMs on TSV-interposers.

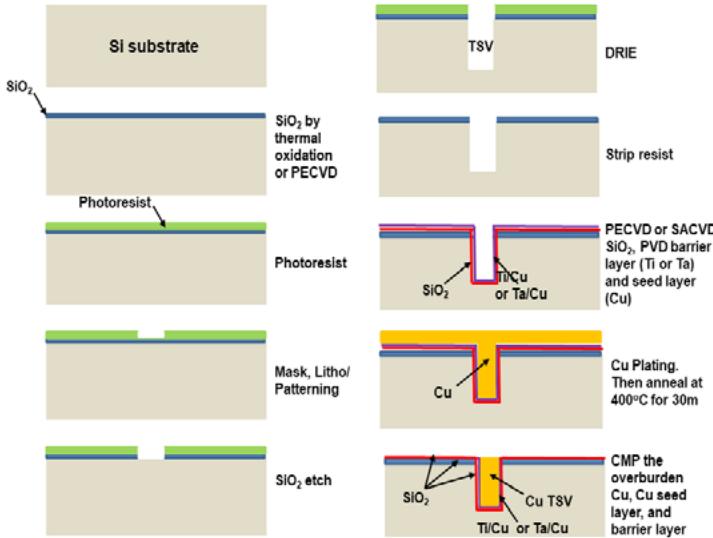


Figure 7: Key process steps in fabricating a TSV.

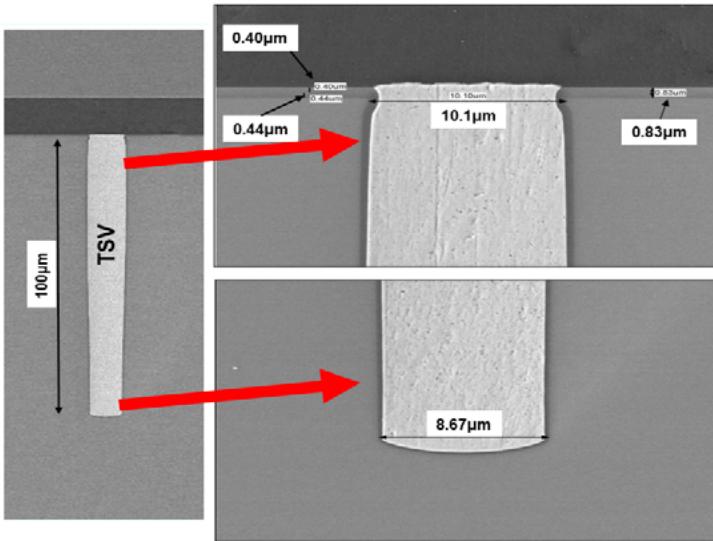


Figure 8: A fabricated TSV.

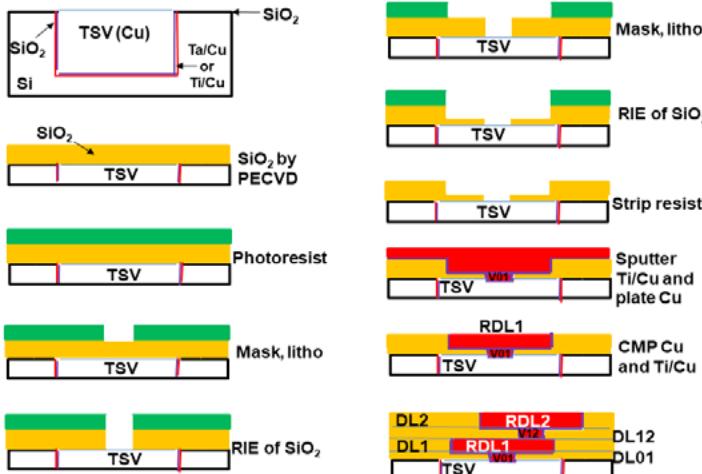


Figure 9: Key process steps in fabricating RDLs from a TSV.

Pascal 100 graphic processor unit (GPU) [17,18], which is built on TSMC's 16nm process technology and is supported by four HBM2 memories (16GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with Cu-pillar and solder-cap bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are on top of a TSV-interposer (1200mm^2), i.e., CoWoS-2, which is fabricated by TSMC with a 64nm process technology. The TSV-interposer is attached to a 5-2-5 organic package substrate with controlled collapse chip connection (C4) bumps.

B3: UCSB/AMD's chiplets on TSV-interposers. Excited by the Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS), UCSB and AMD [19] proposed a future very high-performance system shown in [Figure 6](#). This system comprises a central processor unit (CPU) chiplet and several GPU chiplets, as well as HBMs on a passive TSV-interposer and/or on an active TSV-interposer with RDLs.

B4: Fabrication of TSVs. [Figure 7](#) shows the key process steps in making a TSV [20,21]. It starts with a $\text{SiN}_x/\text{SiO}_x$ insulation layer by either thermal oxidation or plasma-enhanced chemical vapor deposition (PECVD). After photoresist and TSV lithography, the TSV is etched into the Si substrate by a Bosch-type deep reactive ion etch (DRIE) to form a high-aspect ratio (10.5) via structure. The etched TSV structure is then processed with a SiO_2 liner by sub-atmosphere chemical vapor deposition (SACVD), a Ta barrier layer and a Cu seed layer by physical vapor deposition (PVD). Cu electro-chemical deposition (ECD) is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10 μm in diameter and a depth of about 105 μm , which give an aspect ratio of 10.5. In such a high-aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness at the field. The scanning electron microscopy (SEM) cross-section images are shown in [Figure 8](#). It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from the etching process point of view. The Cu thickness at the field is <5 μm . The post-plating anneal is at 400°C for 30 minutes. To complete the TSV process, excess Cu at the field is removed by chemical mechanical polishing (CMP).

B5: RDLs by dual Cu-damascene process. [Figure 9](#) shows the key process steps in making the RDLs from the TSV of an interposer. First, the SiO_2 layer is fabricated by PECVD. The step is followed by applying photoresist and mask or stepper, then using photolithography techniques (align and expose) to open vias on the SiO_2 . Then, reactive ion etch (RIE) of the SiO_2 is accomplished. Next, apply mask or stepper, and then use photolithography techniques to open the redistribution trace locations. Then, use RIE to etch off more of the SiO_2 , strip off the photoresist, and sputter Ti and Cu. Then use ECD to deposit Cu over the entire wafer. Those steps are followed by CMP of

the Cu and Ti/Cu, which then results in RDL1 being obtained. Repeat all the above steps to obtain V_{12} (the via connecting the RDL1 to RDL2) and RDL2, and any additional layers. **Figure 10** shows the image of the cross section of the fabricated RDLs on a TSV of an interposer [22]. It can be seen that there are three RDLs and these RDLs are called inorganic RDLs made by PECVD and dual Cu-damascene + CMP.

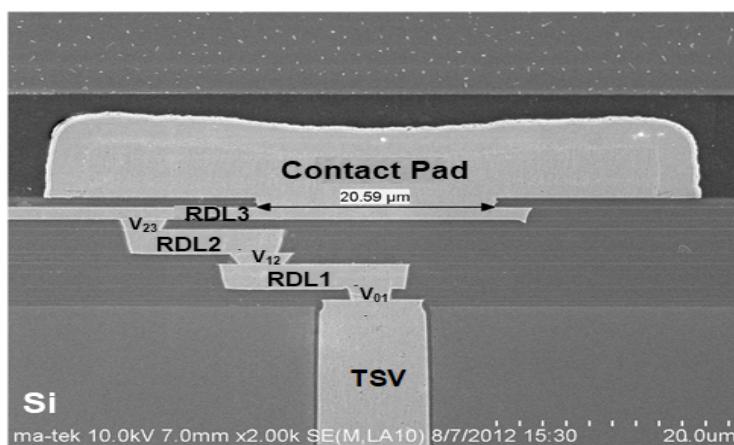


Figure 10: Fabricated RDLs on a TSV.

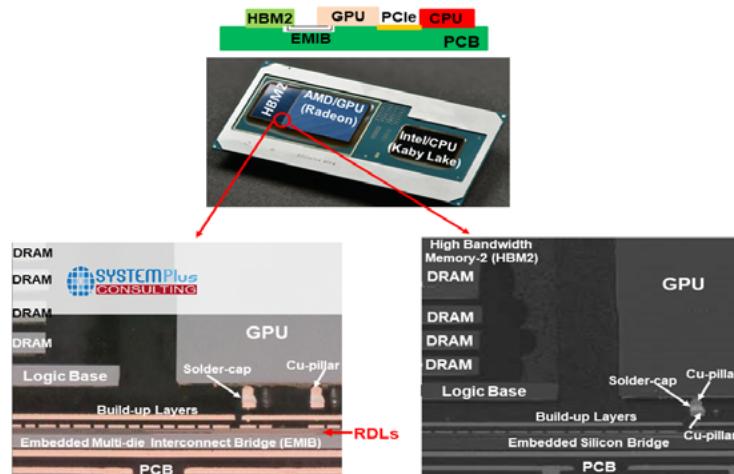


Figure 11: Heterogeneous integration of Intel's CPU, AMD's GPU, and HBM with EMIB.

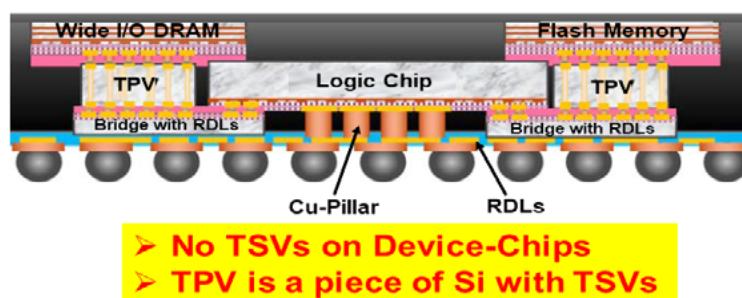


Figure 12: Imec's heterogeneous integration system with silicon bridges.

C: RDLs for heterogeneous integration on silicon substrates (bridges)

Basically, a bridge is a piece of dummy silicon with RDLs and contact pads, but without TSVs. Usually, the RDLs and contact pads are fabricated on a dummy silicon wafer and then diced into individual bridges.

C1: Intel's EMIB for heterogeneous integration. Intel proposed embedded multi-die interconnect bridge (EMIB) [23,24] RDLs to replace the TSV-interposer in heterogeneous integration systems. The lateral communication between the chips will be taken care of by the silicon embedded bridge with RDLs, and the power/ground and some signals will go through the organic package substrate (or PCB) as shown in **Figure 11**. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB. To make the EMIB, one must first build the RDLs (including the contact pads on a Si wafer, which will be discussed later). Finally, attach the non-RDL side of the Si wafer to a die-attach film (DAF), and then singulate the Si wafer into individual bridges. To make the organic substrate with an EMIB, first place the singulated EMIB with the DAF on top of the Cu foil in the cavity of the organic substrate. That step is followed by the standard organic package substrate build-up process all the way to the Cu-contact pads. The organic package substrate with the EMIB is ready for bonding of the chips such as the GPU and HBM cube, shown in **Figure 11**.

C2: Imec's bridges for heterogeneous integration. Ever since Intel's proposal of using EMIB to serve as the high-density interconnects between chips in a heterogeneous integration system was put forth, the "bridge" has been very popular. For example, recently, imec proposed [25] the use of the bridges + fan-out wafer-level packaging (FOWLP) technology to interconnect the logic chip, wide I/O DRAM, and the flash memory as shown in **Figure 12**. The objective is not to use TSVs for all the device chips.

C3: Fabrication of RDLs on a bridge from a Si wafer. The way to make the RDLs for the bridges on a dummy Si wafer depends on the line width and spacing of the conductive wiring of the RDLs, i.e., applications. For line width and spacing $\geq 2\mu\text{m}$, the organic RDLs (polymer and ECD Cu + etching) should be adequate. If the line width and spacing are $< 2\mu\text{m}$ or even in the submicron region, then inorganic RDLs (PECVD and dual Cu-damascene + CMP) should be used and the key process steps are shown in **Figure 13**. **Figure 14** shows a SEM image for the RDLs on the SiO_2 layer of a Si wafer. Finally, the wafer is diced into individual bridges with RDLs.

D: RDLs for heterogeneous integration on fan-out substrates

Recently, using the fan-out wafer/panel packaging technology to make RDLs (to eliminate the TSV-interposer) on substrates for heterogeneous integrations has been getting traction. There are at least two fan-out-wafer/panel packaging formations, namely chip-first and chip-last [26-36], which are discussed below.

D1: Chip-first process. STATS ChipPAC proposed [26,27] the use of the fan-out flip-chip embedded wafer-level ball grid array (FOFC-

eWLB) to make the RDLs for the chips to perform mostly lateral communications as shown in **Figure 15**. It can be seen that the TSV-interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated. ASE [37] proposed something similar by using the FOWLP technology to make the RDLs for the chips to perform mostly lateral communications (see **Figure 16**) and put it into production. It can be seen that the bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 bump process. ASE called this fan-out wafer-level chip-on-substrate (FOCoS) technology [37]. Recently, TSMC named this Info_oS (integrated fan-out on substrate) [38].

D2: Chip-last process. Recently, Samsung [39] proposed the use of chip-last or RDL-first FOWLP to eliminate the TSV-interposer (**Figure 17**) for high-performance computing heterogeneous integration applications. First of all, the RDLs are built on a bare glass – either in a wafer or a panel format. In parallel, wafer bumping of the logic and HBM chips will be done. Then, the following processes are done: fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfill dispensing and curing. Those steps are followed by epoxy molding compound (EMC) compression molding. Then, backgrinding the EMC, chips, and HBM cube and C4 wafer bumping are done. After those steps, one can attach the whole module on the package substrate. Finally, solder ball mounting and lid attachment are done. Samsung called the resulting structure a Si-less RDL interposer [39]. For a mobile application processor (AP) chipset, in contrast to the In-FO_PoP by TSMC/Apple [40], Samsung proposed the use of fan-out SiP side-by-side (SbS) for the AP chipset as shown in **Figure 18** [41]. The package profile of Samsung's solution should be thinner than that of TSMC/Apple's, however, the package size should be larger. Also, the cost of Samsung's process should be higher than that of TSMC's process.

Summary

Redistribution layers for heterogeneous integrations on organic substrates, silicon substrates (TSV-interposers), silicon substrates (bridges), and fan-out substrates have been presented. Some important results and recommendations are as follows:

- In general, for high-volume manufacturing (HVM), 70% of the RDLs for heterogeneous integrations should be on organic substrates and the metal line width and spacing are $\geq 10\mu\text{m}$. (Most of these heterogeneous integrations are actually SiP.) No more than 5% of the RDLs for heterogeneous integrations should be on organic substrates, and the metal line width and spacing are $< 10\mu\text{m}$. The i-THOP substrate (with $2\mu\text{m}$ line width and spacing) is facing challenges on yield losses.
- In general, for HVM, 25% of the RDLs for heterogeneous integrations would be on silicon substrates (either passive TSV-interposers or active TSV-interposers or both), silicon substrate (bridges), and fan-out substrate. The metal line width and spacing

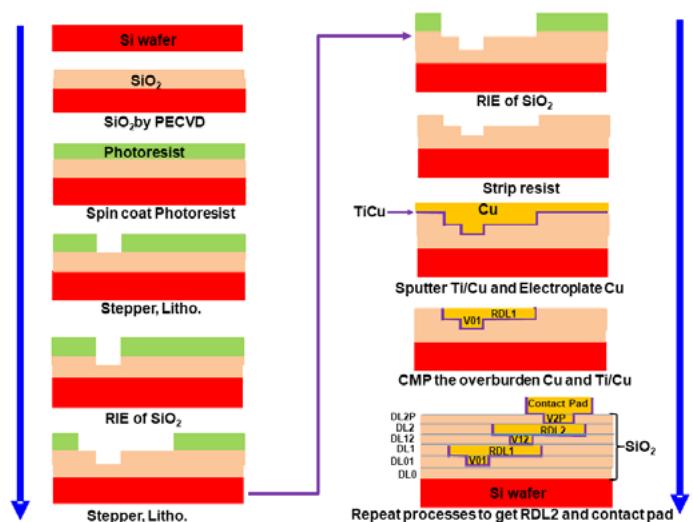


Figure 13: Key process steps in fabricating RDLs on a bridge from a silicon wafer.

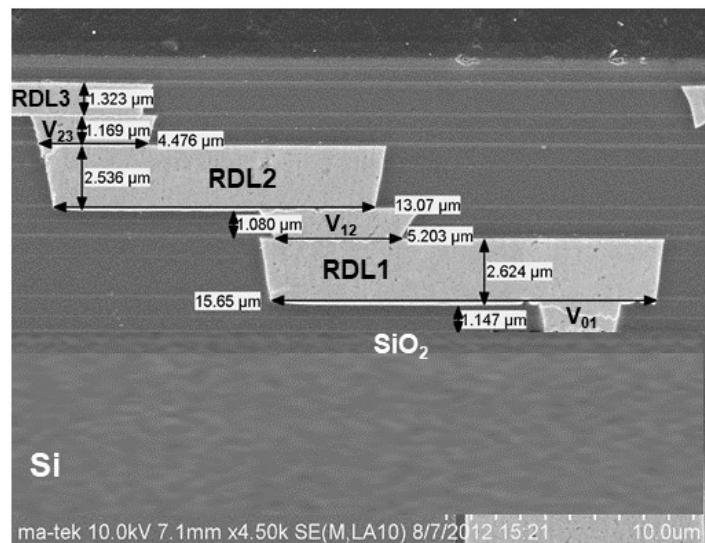


Figure 14: Fabricated RDLs on a silicon bridge with SiO_2 .

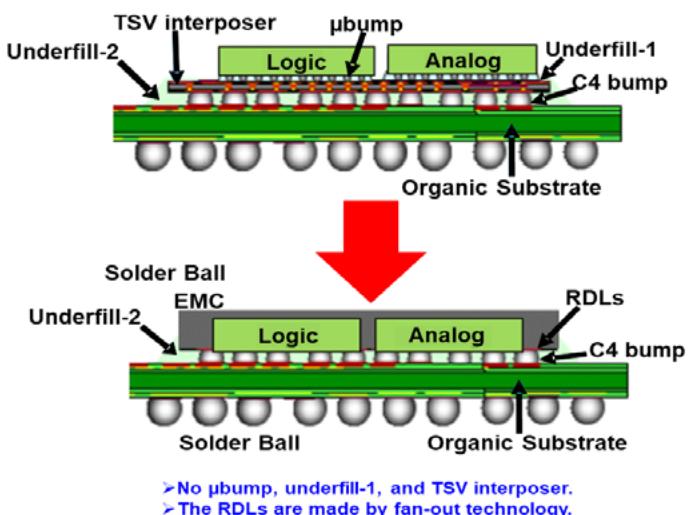


Figure 15: STATSChipPac's fan-out substrate (FOFC-eWLB).

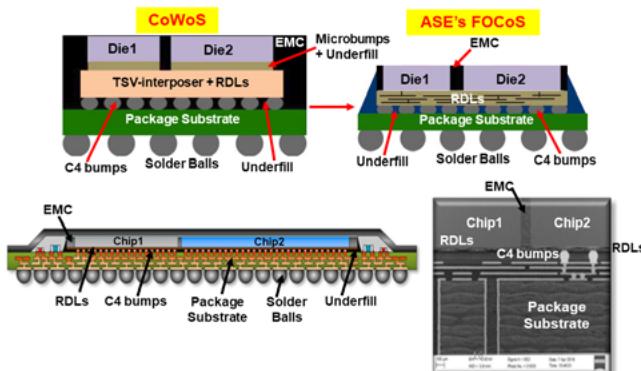


Figure 16: ASE's fan-out (chip-first) substrate (FOCoS).

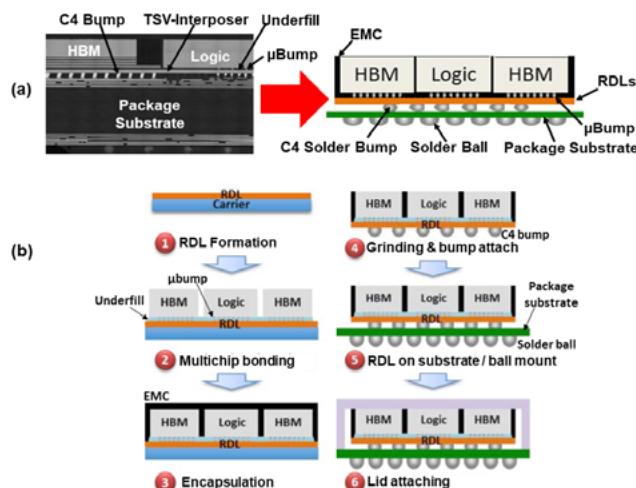


Figure 17: Samsung's fan-out (chip-last) substrate (Si-less RDL interposer).

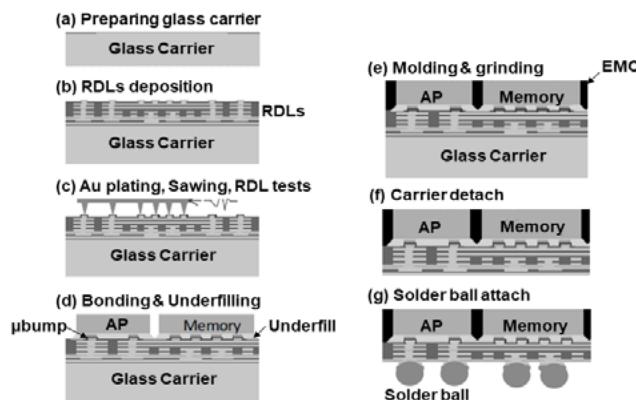


Figure 18: Samsung's fan-out substrate.



Biography

John H. Lau has been a Senior Technical Advisor of ASM Pacific Technology in Hong Kong since 2014 and a Senior Scientist at HP Labs/Agilent in California, U.S.A., for more than 25 years. He has published more than 470 peer-reviewed papers, has 30 issued and pending US patents, and 20 textbooks on flip-chip technologies, WLCSP, FOWLP, BGA, TSV for 3D integration, advanced MEMS packaging, lead-free solder and manufacturing, and reliability of 2D and 3D IC interconnections. John earned a PhD from the U. of Illinois – Urbana and is an ASME Fellow, IEEE Fellow, and IMAPS Fellow. Email john.lau@asmpt.com

of the RDLS are usually very small and can go down to submicron values.

- The fabrication process of RDLS for heterogeneous integrations on organic substrates is mainly SAP. Currently, two core layers and 12 build-up layers (6-2-6) with 10 μm metal line width and spacing are in HVM.
- The fabrication process of RDLS for heterogeneous integrations on silicon substrates (either passive TSV-interposers or active TSV-interposers) is by PECVD and Cu-damascene + CMP. Currently, there are at least four RDLS and their minimum pitch is 0.4 μm . The metal line width and spacing can go down to submicron values. This is called 2.5D IC integration technology. Among all the packaging technologies discussed in this article, this is the most expensive. However, this technology can be applied to very fine pitches, very high density, very high I/Os, and for very high performance applications.
- The fabrication process of RDLS for heterogeneous integration on silicon substrates (bridges) depends on the metal line width and spacing. If the line width and spacing are $\geq 2\mu\text{m}$, then polymer and ECD + etching are adequate. On the other hand, if the line width and spacing are $< 2\mu\text{m}$, then PECVD and Cu-damascene + CMP are needed.
- The fabrication process of RDLS for heterogeneous integration on fan-out (chip-first) substrates is by polymer and ECD + etching on a reconstituted wafer with embedded chips in the EMC. These RDLS will replace (eliminate) the μbumps, chip-to-wafer bonding, cleaning, underfill dispensing and curing, and the TSV-interposer. However, the metal line width and spacing cannot go down to $< 2\mu\text{m}$, and definitely not to a submicron value.
- The fabrication process of RDLS for heterogeneous integration on fan-out (chip-last) substrates is by polymer and ECD + etching on a temporary bare glass (wafer or panel) carrier. Those steps are followed by wafer bumping, fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfilling, EMC compression molding, etc. These RDLS will replace (eliminate) the TSV-interposer. However, the metal line width and spacing cannot go down to $< 2\mu\text{m}$ and definitely not to a submicron value. The advantages of fan-out chip-last over fan-out chip-first are: a) there is not a die-shift problem, and therefore a higher packaging assembly yield can be obtained, and b) one does not have to throw out known good dies (KGDs). The disadvantages are: a) higher cost, and b) more process steps, which lead to more chances to have packaging assembly yield loss.

References

Contact Publisher for references

Temporary bonding and the challenge of cleaning post-debond

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Michelle Fowler, Seth Molenhour [Brewer Science, Inc.]

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Temporary bonding is used for many applications in advanced packaging and microelectromechanical systems (MEMS). Device wafers are bonded to a carrier wafer with a temporary bonding material in order to perform subsequent backside processing without affecting the device side. After completing the fabrication steps, the wafer must be removed from the temporary carrier by a release mechanism appropriate to the type of temporary bonding material used. After debonding, the device wafer must be sufficiently clean in order to complete fabrication. If the device wafer was thinned, it will be debonded onto a film frame with ultraviolet (UV) tape. The cleaning process and chemistry need to be compatible with the tape and film frame structure.

Optimized cleaning is a result of selecting the most effective chemistry, equipment and process. The chemistry should dissolve the temporary bonding material while leaving the device wafer undamaged. The equipment needs to maintain process parameters, such as temperature and flow rates, while recirculating the chemical for reduced chemical consumption. The process determines the optimized parameters and sequence for the most effective cleaning at the lowest cost of ownership.

This paper describes the methodology and experimentation done to optimize the cleaning process for BrewerBOND® 305 bonding material. Parameters addressed included chemical purity, bath life and consumption, process temperature, dispense method, time, and process sequence. A design of experiment (DOE) methodology was performed to determine the impact of tool and chemical parameters that would yield residue-free wafers. In addition,

the effect of adhesive film thickness on process conditions was considered. Processes will be presented for both debonded wafers and wafers mounted onto film frames. The methodology provided an optimized cleaning process with lower cost using recirculated chemistry at ambient temperature.

The growing importance of TBDB

Wafer-level packaging (WLP) technologies continue to evolve and have been adopted for use in large-scale manufacturing. As demand for smaller, thinner packages has grown, temporary bonding and debonding (TBDB) has become an increasingly critical step in the fabrication process [1]. Consumer electronics, automotive and internet of things (IoT/5G)-based applications and services have been driving growth in the semiconductor industry. High performance, small form factor, and dense integration with low power consumption are requirements for today's advanced devices.

A critical requirement for advanced technology is the use of a temporary carrier wafer to support the device wafer that has been processed with temporary bonding and release material. Downstream fabrication processes include high-temperature thermal cycles, high-vacuum environments, and various chemical treatments that can damage an unsupported device wafer. Device damage due to bowing/warping induced from downstream processes can be prevented with the use of a temporary bonded carrier substrate.

In a standard TBDB process, a thermoplastic bonding material is spin-coated onto the front side of a device wafer then baked to remove excess solvent from the film. The carrier wafer, typically glass or silicon, is coated with a thin layer of release material used to facilitate debonding at the appropriate interface (**Figure 1**). The carrier and device wafers are then bonded together, under vacuum, using a bond temperature high enough for the bonding material to soften and become tacky.

Once the device wafer is supported by the carrier wafer, backside grinding or thinning using chemical mechanical planarization (CMP) can be performed. During this process, the device wafer is typically thinned to less than 100µm and in some instances, as thin as 30µm. The bonded pair then can undergo various backside processes, including high-temperature and vacuum exposure. Once

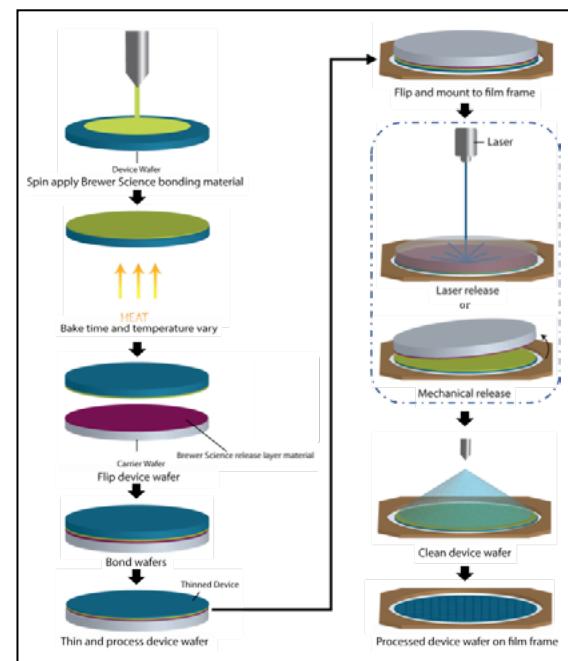


Figure 1: Illustration of wafer processing and handling flow.

backside processing is complete, the bonded pair can be mounted to a film frame and debonded using a variety of methods, including mechanical and laser release. Once the device wafer has been debonded from the carrier wafer, residual bonding material can be removed using a solvent cleaning process.

For this work, we will focus on the cleaning process and solvent removal of residual bonding material from the device wafer. Various solvent removal process parameters will be examined in combination with bonding material bake processes.

Processing

For this experiment, 200mm blank silicon test wafers were coated with two different film thicknesses (30 or 50 μm) of temporary bonding material and baked using a 3-step process of 60°C, 160°C and 220°C each for 3 minutes. After the initial coat and bake process, some of the test wafers were subjected to a simulated backside process using a high-temperature nitrogen oven bake of 250°C for 3 minutes. Once processed, six test wafers were mounted on film frames

using UV tape, which is then exposed to UV light to cure the tape for subsequent cleaning by liquid chemical processing.

Experimental setup

Removal of temporary bonding material from the silicon wafers was performed in a Veeco PSP WaferStorm® single-wafer tool. The solvent used to remove temporary bonding material was ultra-high purity (UHP) d-limonene and provided by Transene. Lower purity limonene was found to cause residues. Wafer rinsing was performed using isopropyl alcohol (IPA, J.T. Baker).

The first step in the cleaning process was to spray the wafer containing temporary bonding material with UHP d-limonene inside a concealed and exhausted process chamber (**Figure 2**). While the wafer was spinning, a high-pressure chemical (HPC) pump pushed d-limonene through a rectangular nozzle, providing a fan spray approximately 1.25" in width (**Figure 3**). The fan spray nozzle was attached to an arm that scanned linearly across the wafer surface for a pre-determined amount of time. The

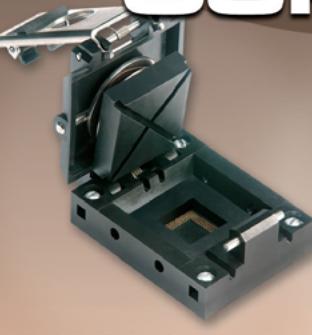


Figure 2: D-limonene dispensed through a high-pressure chemical fan spray.



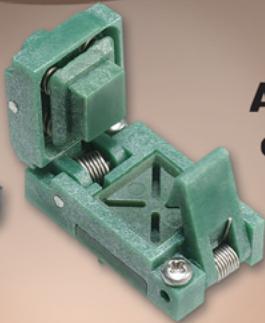
Figure 3: Macro photograph of a silicon wafer with the temporary bonding material.

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UHP d-limonene was either heated or dispensed at room temperature. After spraying the wafer, fresh UHP d-limonene supplied by a separate chemical tank was dispensed onto the wafer surface for 10s. Upon successful removal of the temporary bonding material, the wafer was rinsed with IPA for 20s and then spun dry at 1500rpm for 45s. IPA rinsing and spin drying were performed in a separate, clean chamber.

Definition of clean

The following sections discuss various elements of the cleaning process.

Before cleaning. Complete removal of the temporary bonding material was confirmed by visual observation and using a microscope. A layer of this material provided a uniform rainbow pattern across the wafer (**Figure 4**). The rainbow pattern was caused by light interactions with the temporary bonding material and

disappeared after processing. Observation of this material under a microscope showed a smooth and uniform layer except for the wafer edge. The material at the wafer edge was thicker on account of spin coating edge bead effects and made removal more challenging.

Nonconfocal (NCF) imaging was also utilized in determining if there was any residual temporary bonding material remaining on the wafer surface. Interference fringes were observed with this imaging technique and indicative of temporary bonding material.

After Cleaning. Once the temporary bonding material was successfully removed, a clean silicon surface was exposed. A color change and lack of topology indicated the material had been removed. The interference fringes observed in NCF mode were useful in determining if there was residual temporary bonding material. The lack of fringes (**Figure 4**) also indicated that complete removal of the material was achieved. Complete temporary bonding material removal, including the edge, was required for a process to be deemed successful.

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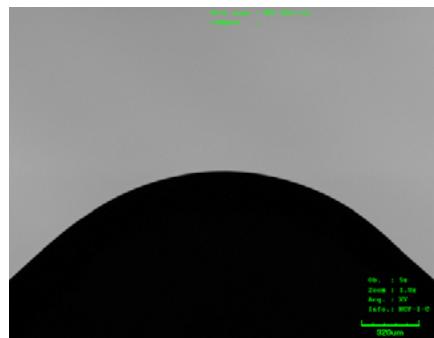


Figure 4: Optical micrograph (5X, NCF) of the temporary bonding material after removal.

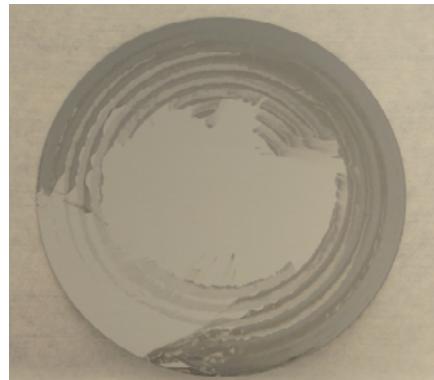


Figure 5: Macro photographs of significant incomplete temporary bonding material removal.

Incomplete removal. Residual temporary bonding material that was not removed with UHP d-limonene reacted with IPA to form a white residue indicative of incomplete removal. This white residue was the result of the temporary bonding material, which is nonpolar, being precipitated out by the polar IPA. If the process was not optimized, this residue could span the whole wafer (**Figure 5**) or be localized to the edge. Many of the failed experiments contained residual temporary bonding material at the wafer edge due to the edge bead effect during spin coating.

NCF mode showed clear fringes at the wafer's edge limited to 500µm from the edge and the remaining part of the wafer did not contain any fringes. To eliminate the remaining edge residues, we increased the process time from 60s to 120s.

Design of experiment

A design of experiment (DOE) was developed to investigate the impact of HPC fan spray pressure and UHP d-limonene temperature on the removal efficiency of temporary bonding material film. A wafer "passed" if there was no residue across the entire wafer surface. A wafer "failed" if there was residue on the wafer surface, including the edge. Experiments started with a 60s and 120s process time. If 60s or 120s was not long enough to remove the material, increments of 30s were added until complete removal was achieved.

One would expect a shorter process time and thereby cleaner wafer with higher pressure, higher temperature, lower film

thickness, and lower cure temperature. Wafer immersion in UHP d-limonene followed by a high-pressure fan spray was also investigated as a method to reduce overall process time, thereby increasing wafer throughput. One combination of variables that was investigated were the effects of cure temperatures of the temporary bonding film.

Results

The first DOE studied the effect of temperature (increasing it from 25 to 40°C) while keeping the pressure constant at 1500psi. D-limonene temperature had no observed impact on process time on a 30µm-thick temporary bonding material coating. Temperature was a critical parameter for thicker films, e.g., on a 50µm-thick temporary bonding material coating, the process time was able to be reduced by 33%.

The second DOE studied the effect of high-pressure spray while keeping the temperature constant using 40°C d-limonene. Minimum time required to achieve a clean wafer with a 30-µm-thick temporary bonding material coating and using a bake temperature of 220°C was 120s at either 500psi or 1500psi. No pressure effect was observed with a 30µm-thick temporary bonding material coating.

The minimum time required to achieve a clean wafer with a 50µm-thick temporary bonding material coating and using a bake temperature of 220°C was 180s at 500psi. Using a higher pressure

of 1500psi and keeping the temperature constant at 40°C, the process time can be reduced to 120s, therefore suggesting the high-pressure spray has a key impact on process performance.

The third DOE studied the impact of the cure temperature of the temporary bonding film. When polymers such as adhesives or photoresist are exposed to higher temperatures, it is more challenging to remove the material and longer process times are required. Yet again, a two-minute process time using 40°C UHP d-limonene and a fan spray pressure of 1500psi successfully cleaned both a 30µm- and 50µm-thick film of temporary bonding material. However, an additional minute was required to clean a 30µm-thick film if the lower temperature of d-limonene was used.

Discussion

The sections below discuss the various findings as a result of the experiments.

Wafer immersion. Immersing the wafers in a tank of UHP d-limonene prior to spraying was another technique that further improved process time. Adding an immersion time of 5min reduced the spray time from 120s to 60s using 40°C UHP d-limonene. Both 30µm- and 50µm-thick films of temporary bonding material and wafers exposed to a higher cure temperature were successfully cleaned with a five-minute soak and a 60s fan spray. Using technology that allows a unique combination of batch immersion with single-wafer spray, resulted in a 50% reduction of fan spray time, thereby increasing wafer throughput. A lower fan spray pressure of 500psi also achieved complete cleaning using a soak and spray approach.

Fresh UHP d-limonene. Ten seconds of fresh UHP dlimonene was required at the end of every process. Recirculated chemistry used during the fan spray removed the bulk of the temporary bonding material and 10s of fresh d-limonene guaranteed a pristine surface. Skipping this step yielded a white residue that covered the wafer surface (**Figure 6**). All fresh UHP d-limonene was diverted to the recirculated tank and reused to lower the cost of ownership.

Best known method. The best-known method (BKM) developed



Figure 6: Impact of using a fresh UHP d-limonene step.

from these experiments for removing temporary bonding material used 40°C UHP d-limonene and an HPC fan spray pressure of 1500psi. With these two settings, a process time of 120s removed both a 30µm- and 50µm-thick film of temporary bonding material, regardless of cure temperature. Process times under 120s resulted in wafers containing residual temporary bonding material at the wafer edge and yielded a failure. Complete wafer cleaning processes were also achieved using lower UHP d-limonene temperature and lower fan spray pressures. An immersion and spray approach were also demonstrated, which reduced the spray times from 120s to 60s if a five-minute soak was performed before spraying.

Effects of temperature and pressure. In most cases, solubility increases with temperature, and this trend held true with UHP d-limonene and the temporary bonding material. The BKM used a temperature of 40°C, but 25°C was also investigated. Process times did not change for a 30µm-thick layer using a lower temperature, but process times did increase using a 50µm-thick film or higher cure temperatures. In some instances, there may be sensitive features on the device wafer and a lower pressure could be required. The BKM used a fan spray pressure of 1500psi and any pressure below that could require longer process times. Similar to lowering the temperature, process times did not change for a 30µm-thick layer using lower pressure. However, process times did increase using a 50µm-thick film or higher cure temperatures at lower pressure.

The HPC fan spray pressure can be varied from 500psi to 3000psi. Only 500psi and 1500psi were explored in this experiment, but higher pressures could be utilized to clean more challenging wafers. Another benefit of a high-pressure fan spray is the ability to clean device wafers with significant topology. For example, a fan spray has a higher probability of cleaning an etched silicon trench than a soak-only or stream-only process.

Removal process. Complete removal of temporary bonding material was successfully achieved using UHP d-limonene and a high-pressure fan spray process. Two minutes of fan spray, with 40°C UHP d-limonene and 1500psi, removed both a 30µm- and 50µm-thick film, regardless of bake profiles. If needed, the temperature and pressure for the solvent clean process can be lowered, but will increase the process time. Utilizing immersion can further lower process time.

Cost of ownership – process time. Brewer Science's original temporary bonding material removal process involved alternating dispense/spin dry steps, with a final IPA rinse. Improvement was made to this method with the ability to collect/recirculate used chemistry, heat the solvent to increase solubility, and use a high-pressure fan spray. Brewer Science's previously recommended removal process takes 208s and the BKM developed in this paper takes 120s, or 60s if soaking is performed. For a cassette of 25 wafers, the temporary bonding material removal step is reduced from 87min using Brewer

Science's previous removal process, to 54min using the BKM developed here, or 34min if soaking can be utilized.

Cost of ownership – recirculated chemistry. Collecting and reusing UHP d-limonene is an important factor in lowering the cost of ownership. Used solvent passes through filtration to ensure debris is not redeposited onto the wafers. The recirculated solvent first passes through a 9µm stainless steel cartridge filter and then a 0.1µm fluoropolymer cartridge filter. Separate process chambers were used for the spraying removal step and the IPA rinse step to avoid contamination of the UHP d-limonene with IPA.

Summary

An optimized process was developed for completely removing the temporary bonding material. The use of a high-pressure fan spray at 1500psi and 40°C for two minutes results in a clean surface regardless of material thickness or bake temperature. This process is applicable to both debonded wafers and wafers on film frames. Recirculation of the solvent and performing the final rinse in a separate chamber significantly reduces the amount of solvent consumed and thereby reduces the cost of ownership for the cleaning process.

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Biographies

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Moore's Law for Packaging to replace Moore's Law for ICs

By Rao R. Tummala *[Georgia Institute of Technology]*

This article proposes Moore's Law for Packaging to replace Moore's Law for ICs, as this is seen as coming to an end. Moore's Law for ICs is about scaling transistors to ever smaller sizes, from node to node and interconnecting and integrating these to result in more transistors in smaller chips with higher performance at lower cost from 300mm wafers. As transistor scaling and integration comes to an end due to physical, material and electrical limitations, Moore's Law for Packaging can be viewed as interconnecting and integrating smaller chips with the highest transistor density and the highest performance at the lowest cost. Additionally, the proposed law can encompass smaller system components to form 2D, 2.5D and 3D multi-chip modules in the short term, and 3D system architectures in the long term for the entire system. Package or system scaling is proposed to be one and the same as the end goal of packaging is a system.

Just as Moore's Law for ICs has two components — number of transistors and cost of each transistor — I propose that Moore's Law for Packaging have two components as well: the number of interconnections or inputs/outputs (I/Os), and the cost of each I/O. This article lays the ground work for Moore's Law for Packaging by showing how I/Os have evolved from one package family node to the next, starting with <16 I/Os in the 1960s to the current silicon interposers with almost 200,000 I/Os. A variety of ways to extend Moore's Law by advances in Si interposers and beyond, using glass in panel embedding is also proposed. As Moore's Law for electronic packaging comes to its own end, this article proposes 3D opto-electronic packaging as the next Moore's Law for Packaging.

Introduction

Moore's law has been the driving force behind transistor scaling and integration

as well as reduction in cost of transistors during the last six decades. Electronic systems, however, such as smartphones, self-driving electric cars and machines mimicking human brains, are more than transistors and ICs. Moore's Law for ICs, which includes both increased transistor integration and cost reduction every two years, has brought electronics to more than a trillion-dollar industry. However, the prediction is that it will come to an end, at least in cost, if not in transistors. So what will take its place for electronics systems of the future? This article proposes Moore's Law for Packaging or Interconnections to replace Moore's Law for ICs, at least in terms of cost in the short term. Reducing transistor size — referred to as transistor scaling — along with their interconnections and integration to ever higher transistor density, was the basis of Moore's Law for ICs. Component size reduction for both active and passive system components, referred to as system scaling, along with their interconnections and integration to form modules in the short term and systems in the long term, can become Moore's Law for Packaging to form packaged systems.

Just as Moore's Law comprises doubling of transistors and a simultaneous cost reduction from node to node, every 18-24 months, Moore's Law for Packaging must do the same. Interconnections have been driven by computing systems, and within computing systems, between logic and memory. The new era of artificial intelligence, mimicking human brains, is yet another reason for Moore's Law for Packaging or Interconnections to come to the fore.

Currently, the most advanced Moore's Law for Packaging is with wafer-based silicon packaging. Silicon-based packaging, however, has many limitations at material, substrate or interconnect and system levels. At the material level, its electrical loss and its

dielectric constant are very high. At the interconnect level, its capacitance and resistance are very high, leading to so-called RC delays, slowing system performance from node to node. In addition, Si-based packaging doesn't conform to Moore's Law for cost. Cost, of course, is the basis for going away from Moore's Law for ICs. At the system level, Si interposers, while perfectly matched to ICs in terms of their thermal coefficient of expansion (TCE), they are totally mismatched to system boards, thereby requiring additional packaging, and subsequently making system-level interconnections even longer.

Moore's Law for ICs

Moore's Law states that the number of transistors on a silicon chip double approximately every two years [1], as shown in **Figure 1a**. Moore's Law has been proven to be accurate for six decades and is thus used to set R&D targets in the semiconductor industry. However, due to physical transistor scaling and leakage limitations [2,3], Moore's Law cannot be sustained forever. As the transistor size gets smaller, the distances between transistors also get smaller. The size of transistors would reach molecular dimensions eventually. At that point, the electrons would tunnel through the short distances, leading to short circuits [4,5]. Therefore, there is a limit beyond which Moore's Law for ICs is not possible — called the “beginning of the end of Moore's Law” — this is expected to be reached within the next decade. The second part of Moore's Law has to do with cost. Moore's Second Law states that the manufacturing cost must decrease as the number of transistors per unit area increase from node to node from a given size of wafer. The semiconductor industry has concluded, however, that beyond 14nm, there was minimal or no cost reduction as the next node was introduced [2] (see **Figure 1b**).

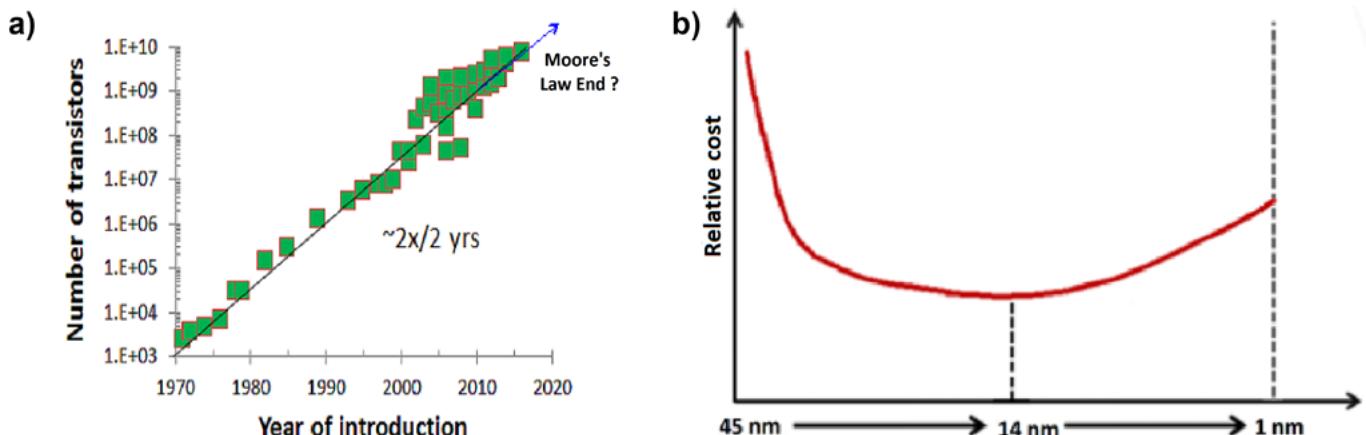


Figure 1: a) Moore's Law for ICs: The increase in the number of transistors as a function of time; b) Recent trend in the increased manufacturing cost per transistor.

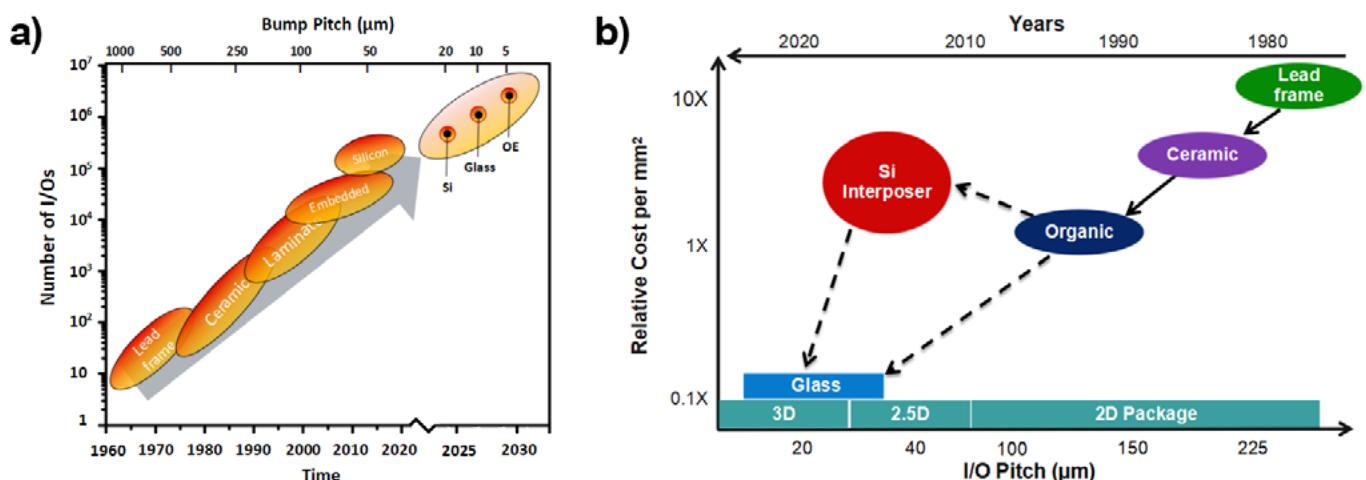


Figure 2: a) Moore's Law for Packaging (I/Os) during the last 6 decades; b) Moore's Law for Packaging: Cost reduction from one package family node to the next.

Moore's Law for Packaging: interconnections or I/Os

Figure 2a conveys the concept behind Moore's Law for Packaging. It started with dual in-line packages (DIPs) in the late 1960s with <16 I/Os leading to peripheral quad flat packages (QFPs) from 64 to 304 I/Os. This led to ceramic packages with increased I/Os up to about 1000 by the early 1990s. Ceramic packages are largely made of thick-film paste technologies of about 100 μm in line widths and vias, and are therefore limited in the number of I/Os they can achieve. They were also limited in performance on account of the high dielectric constant of ceramics and low electrical conductivity of co-fired metals such as W, Mo or Ag-Pd. So-called low-temperature co-fired ceramic (LTCC) addressed some of these limitations, particularly with RDL-like thin-film wiring on top that brought the number of I/Os >10,000. But organic laminate

packaging addressed both performance and cost limitations of ceramic and packaging moved on to build-up thin-film materials and process technologies providing I/Os in excess of 5000 and about 10x more with ultra-thin RDL-like wiring layers on top. The only way to achieve a dramatic increase in the number of I/Os is by wafer-based back-end-of-line (BEOL) RDL wiring on silicon packages up to 200,000 I/Os. Artificial intelligence, mimicking the human brain, and ultra-high bandwidth systems in excess of 50TB/s may need several orders of magnitude in I/Os at a continued-reduced cost per I/O.

Moore's Law for Packaging: cost

Just as with Moore's Law for ICs, cost should be an important factor for Moore's Law for Packaging. **Figure 2b** shows the relative cost reduction, as packaging moved from one package family node to the next. The only

exception seems to be silicon interposer, which is about 3-5X higher in cost per mm^2 than the predicted Moore's Law for Packaging trend. Glass packaging, being pioneered and developed by Georgia Tech and its partners, is expected to reverse the cost trend.

Lead frame package interconnections

Lead frame packages consist of etched metal structures to form leads (lead frame) to connect the die on one side and the board on the outside. The die is connected to the lead frame by fine wires using wire bonding. This assembly is then encapsulated in a molded polymer (typically epoxy) casing [6]. The DIP was the first package invented by Don Forbes, Rex Rice and Bryant Rogers at Fairchild in 1964. DIPs evolved into QFPs and small outline (SO) packages as shown in **Figure 3a** spanning I/Os from 16 to 308 [7-9].

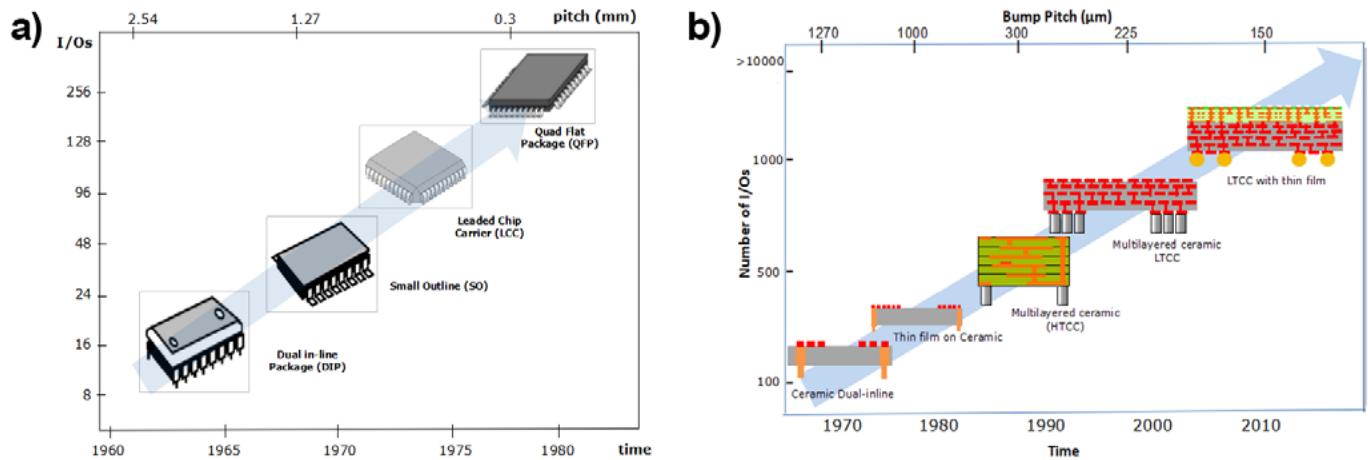


Figure 3: a) Evolution of lead frame package family in I/Os; b) Evolution of ceramic packaging in I/Os from 121 to >10,000 I/Os.

Ceramic package interconnections

Ceramic packaging started with alumina ceramic, the most abundant ceramic material available, as a byproduct of the production of aluminum metal. As such, alumina was the workhorse of the microelectronics industry in the 1970s and 1980s—developed by IBM, Kyocera, NTK in its early days (Figure 3b). It has been used in several substrate forms, from DIPs with 8–48 I/Os, to very sophisticated multilayer co-fired high-temperature ceramic (HTCC). Low-temperature co-fired ceramic packages (LTCC), as well as with thin-film wiring on LTCC, pioneered by IBM, were developed in the late 1980s [10–14]. LTCC substrates continue to be widely used for RF, high-temperature and high-reliability applications even today.

Laminate package interconnections

Organic laminate substrates with high density wiring were first introduced using surface laminar circuit (SLC) technology by IBM for its ThinkPad Laptop Computer

in the 1980s for three reasons: 1) Higher I/Os, 2) Higher electrical performance, and 3) Lower cost than previous ceramic generations. Laminate packages, shown with respect to their I/Os in Figure 4a, are typically fabricated in large panels by sequentially processing each layer with a layer of thin-film polymer dielectric and conductor using photolithographic processes. In contrast to ceramic substrates that required 800°C for LTCC and 1560°C for HTCC, organic substrates are processed at very low temperatures, typically <300°C. These accomplishments have led to significant advances in materials for the core and for the dielectric, as well as process advances in microvias and line lithography. The most advanced BT-epoxy laminate core today has a CTE of 3ppm/K, and a T_g of 300°C. It is fabricated using semi-additive processing with a smallest line width of 2μm and a via diameter of 10μm on a capture pad of 25μm diameter, providing a wiring density of 145 I/Os/mm²/layer [15–20].

Silicon package interconnections

Silicon packaging is the most advanced multi-chip packaging (Figure 4b), referred to as 2.5D with I/Os up to 200,000. This MCM concept is very much like the 100-chip multi-chip ceramic packages of IBM in the 1990s in terms of power distribution, signal transmission, thermal dissipation from the back of the chip, and flip-chip assembly. It has two unique technologies, however: 1) Through-silicon vias (TSVs), and 2) RDLs. The advances in the Bosch process for fabricating TSVs, as a result of manufacturing them in high-bandwidth memory products, have matured to a level of incorporating these cost effectively in silicon interposers. The RDL layers, however, were re-engineered from previous BEOL processing for ICs. The manufacturing infrastructure for BEOL is largely responsible for providing the highest I/Os in Si interposers, compared to organic or ceramic packages [21–25].

Si interposers are currently used at 2μm line widths by Intel in its EMIB [21],

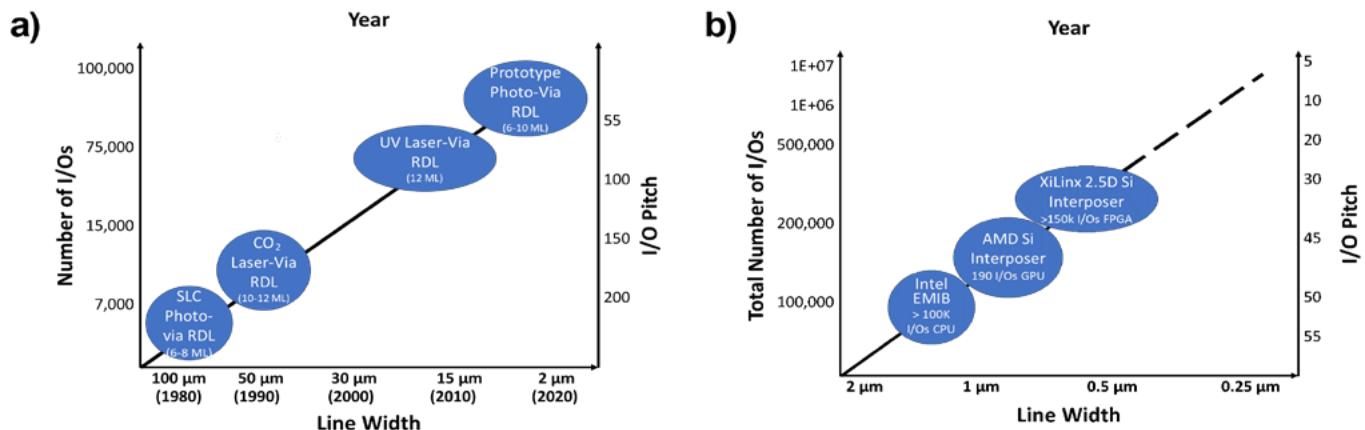


Figure 4: a) Evolution of laminate packaging in I/Os; b) Evolution of silicon interposers in I/Os.

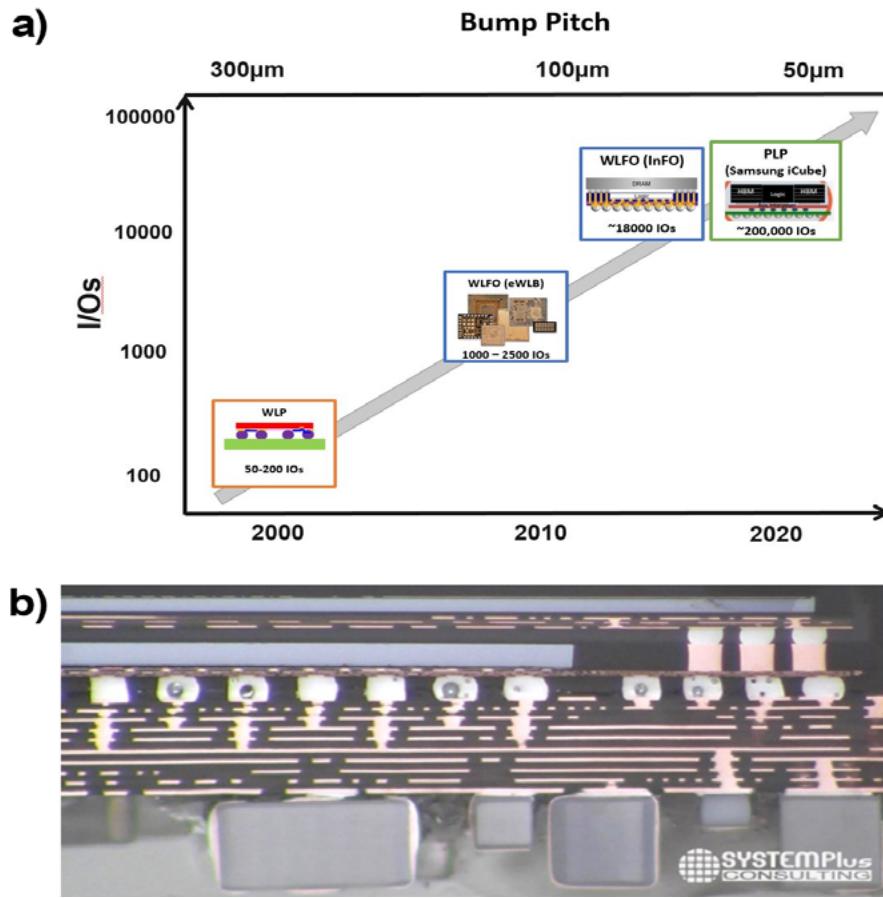


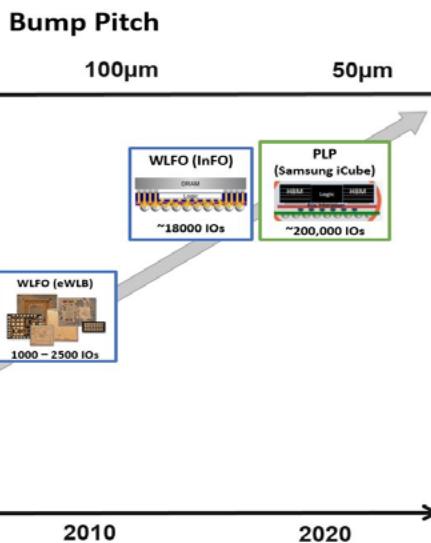
Figure 5: a) Evolution of wafer and panel embedding technology in I/Os; b) TSMC InFO - first high-volume WLFO technology. SOURCE: SYSTEMPlus Consulting

1µm by AMD in its GPU to HBM for bandwidth [22], and <0.5µm by Xilinx in its field-programmable gate array (FPGA) applications [23]. The actual number of I/Os for a 596mm² GPU die is around 190k, as published by AMD for its Radeon Fury device [22]. A similar number was published by Xilinx for its Virtex-7 2000T FPGA product [24].

Embedded package interconnections

Embedding means the chip is embedded or buried inside the package or board and the interconnections are made to and from these buried ICs using either wafer BEOL tools or package tools. Figure 5a shows the progression of embedding technology from wafer level, to wafer fan-out level to panel-level packaging (PLP) in I/Os.

Embedded wafer and panel fan-out packages are manufactured by reconstituting ICs into 200mm or 300mm round wafers and molding them with epoxy-based molding compounds before building RDLs on these molded wafers.



Panel fan-out (PFO) technology is being developed widely to address some of these issues noted above in both organic laminates and in inorganic laminates. Examples include Samsung's with organic panels and Georgia Tech with its glass panel embedding (GPE). Samsung's iCube, based on the RDL-first panel fan-out technology, achieves very high-density integration of logic and memory at lower cost than current WFO options, as shown in Figure 5a [29].

Future of Moore's Law for Package Interconnections

Referring to Figure 2a, there are many options to continue the proposed Moore's Law for packaging, such as:

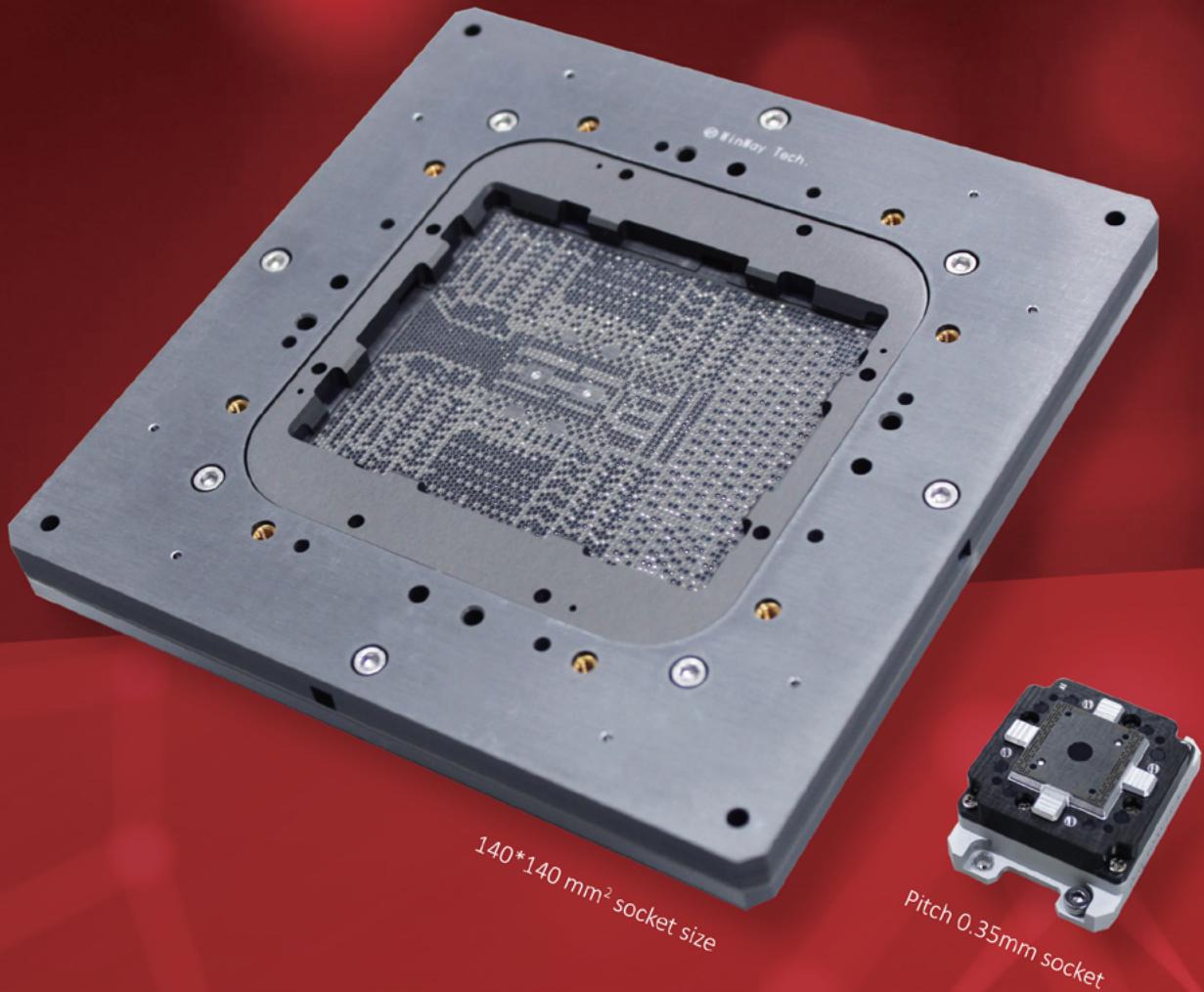
1. Extend silicon package interconnections.
2. Develop large-panel, low-C and low-R inorganic GPE packaging.
3. Develop other panel embedding technologies without molding compounds and assembly.
4. Move on to opto-electronic interconnections as electronic interconnections come to an end.

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Biography

Prof. Rao Tummala is a Distinguished and Endowed Chair Professor at Georgia Tech in the USA. He is well known as an industrial technologist, technology pioneer, and educator. Prior to joining Georgia Tech, he was an IBM Fellow and Director of Advanced Systems Packaging, pioneering such major technologies as the industry's first plasma display in the 1970s and the first and next two generations of 100-chip MCM package integration in the 1980s for servers, mainframes and supercomputers. He is the father of LTCC and the system-on-package (SoP) technologies. As an educator, Prof. Tummala was instrumental in setting up the largest Academic Center funded by NSF as its 1st NSF Engineering Research Center in Electronic Systems at Georgia Tech, pioneering an integrated approach to research, education and

industry collaborations with companies in the U.S., Europe, Japan, Korea, Taiwan and China. The Center, referred to as PRC, produced and supplied more than 1200 PhD and MS packaging engineers to the electronic industry. He has published about 800 technical papers and invented technologies that resulted in over 110 patents and inventions. He wrote the first modern handbook in packaging, *Microelectronics Packaging Handbook* (1988); then the first undergrad textbook, *Fundamentals of Microsystem Packaging* (2001); and the first book introducing the concept of SoP, *Introduction to System-on-Package* (2006). He received more than 50 industry, academic and professional society awards. He is a member of NAE and an IEEE Fellow, as well as President of the IEEE CPMT and IMAPS Societies. Email rao.tummala@ece.gatech.edu

Air jetting debonding for thin-wafer/panel and fan-out wafer-level package processing

By Hao Tang, My Nguyen, Joshua Huffaker, Anastasia Banner [Micro Materials Inc.]

Unlike mechanical debonding, which generates significant peel stress on a device's surface, air-jetting debonding (AirDebond[®]) injects air streams between the carrier and the device, pushing the carrier up from underneath while compressing the device down. As a result, this jetting technology allows a higher strength bonding adhesive at an elevated temperature, which is typically associated with excessive warpage control. Furthermore, the airflow produces the most uniform stress distribution, and the debonding is instant at room temperature—characteristics that are best suited for large-area debonding.

Air jetting debonding

This article describes the advancements in air jetting debonding and the material developments for high-temperature temporary support of thin-wafer fabrication, fan-out wafer-level packaging (FOWLP), and integrated circuit (IC) package assembly with a large thin substrate.

The fabrication of a thin IC wafer requires a temporary support for grinding, polishing, dry reactive ion etching, dielectric development, metal deposition, chemical etching, photoresist development and/or solvent soaking, plasma ashing, and wafer cleaning. Panel-level packaging also requires temporary support for redistribution layer (RDL) build-up, flip-chip bonding, fluxing cleaning, molding, and even the solder reflow process. After fabrication, the thin-wafer/panel requires debonding from its carrier. The bonding adhesive needs to be completely removed without any trace of residue contamination.

While a carrier and a device typically bond together under pressure in vacuum, debonding mechanisms to separate the carrier from the device vary with the adhesive. It is desirable to have the debonding done with the shortest cycle time, the minimum tensile stress exerted on the device surface, the elimination of heat damage on the device's structure, and easy cleaning with an environmentally friendly cleaner.

The concept of injecting air for carrier debonding was first introduced in 2016 for thin-wafer processing [1]. Unlike mechanical peeling, air jetting debonding introduces air streams to push the carrier up from underneath while compressing the device down (**Figure 1**). The structure and pattern of the device are being protected from the airflow. Furthermore, AirDebond[®] allows the carrier made by materials, such as silicon, ceramic and metal (as well as glass) to best match the coefficient of thermal expansion (CTE) of the device wafer for better warpage control at a high temperature.

Table 1 summarizes the application and materials with the air jetting technology.

Temporary bonding for a wafer process >400°C

The thermal stability of an adhesive often refers to its ability to resist decomposition and outgassing during high thermal processing. Z-coat 451 (Z451) is a single-layer bonding adhesive for up to a 400°C processing application. **Figure 2** illustrates a typical process flow with Z451. **Figure 3** shows the thermogravimetric (TGA) curve of Z451 under a constant heating rate of

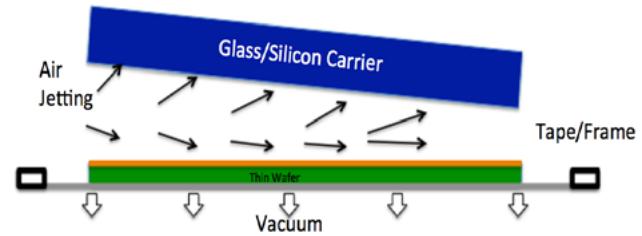


Figure 1: Illustration of the air jetting process.

	High thermal 400°C stability	RDL-first fan-out WLP	High chemical resistance debond with water wash	Water wash adhesive with 280°C stability
Protective coating, or sacrificial layer coating	N/A	Z-Coat 211	Z-Coat 100/122B	N/A
Bonding adhesive	Z-Coat 451	N/A	Brewer Bond 305/Z-Coat 008	Z-Coat 110
Bonding temperature	300°C	N/A	200°C	150°C
Thermal stability	400°C	350°C	280°C	280°C
Debonding method	AirDebond [®]	AirDebond [®]	AirDebond [®]	AirDebond [®]
Cleaning	Solvent	Peel or Cleaner	Water	Water
Pro and con	High temperature	Low cost	Easy debond/clean	Easy debond/clean

Table 1: Summary of the application and materials with AirDebond[®] technology.

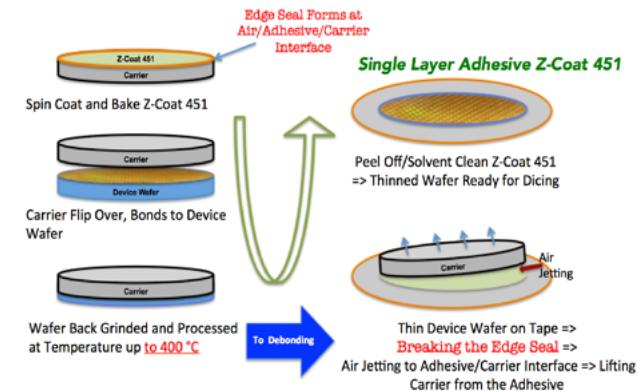


Figure 2: Typical process flow with Z451.

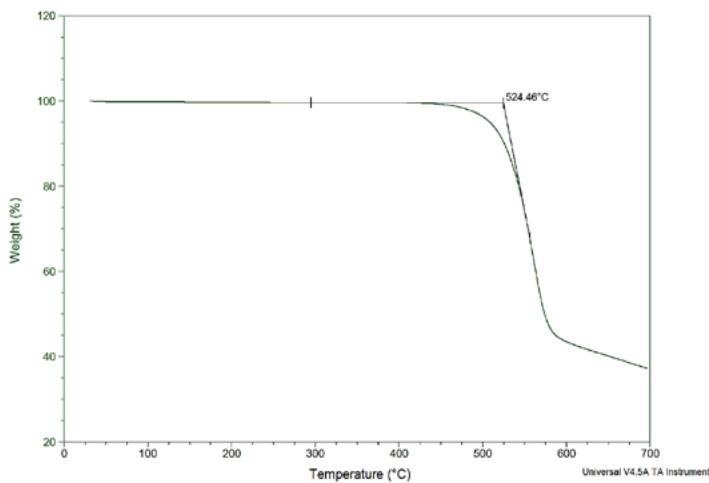


Figure 3: Thermogravimetric (TGA) curve of Z451 under a constant heating rate of 10°C/min to 700°C

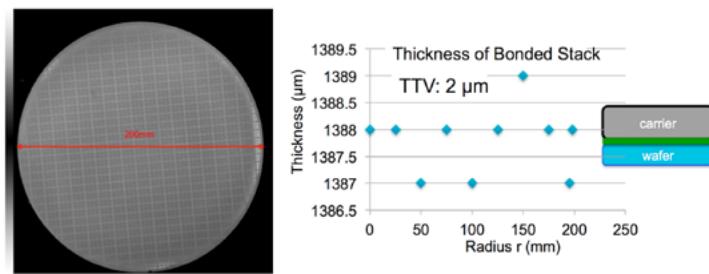


Figure 4: a) An acoustic image of a bonded wafer stack after backgrinding to 60µm; and b) A plot of the total thickness variation (TTV) measurement after grinding.

Chemicals	Test Condition	Result
PGMEA	25 C Soak 30 minutes	Weight Loss less than 1% surface keeps normal
0.045% KOH	25 C Soak 30 minutes	
Al Hydroxide	40 C Soak 60 minutes	
10% Oxalic Solution	47 C Soak 60 minutes	
TMHAH	25 C Soak 30 minutes	
Stripper	60 C Soak 60 minutes	
Hydrofluoric 6N	25 C Soak 30 minutes	
Acetic acid 6N	25 C Soak 30 minutes	
H ₂ O ₂ 30%	25 C Soak 30 minutes	
H ₂ SO ₄ 6N	25 C Soak 30 minutes	
HCl , Conc	25 C Soak 30 minutes	
H ₂ O:NH ₄ OH:H ₂ O ₂ (5:1:1)	25 C Soak 30 minutes	
H ₂ O:H ₂ SO ₄ :H ₂ O ₂ (8:1:1)	25 C Soak 30 minutes	
Isopropanol	25 C Soak 30 minutes	

Table 2: Summary of chemical resistance testing on Z451.

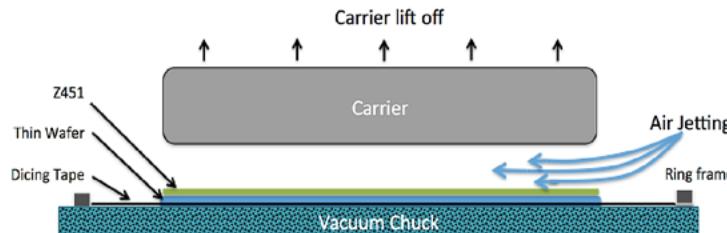


Figure 5: RDL-first FOWLP process flow with air jetting technology.

10°C/min to 700°C. We can see that the weight loss of the Z451 is highly stable up to 450°C. The decomposition temperature is around 500°C.

The bonded wafer stack is often backgrinded and then processed at the evaluated temperature with many types of chemicals. **Table 2** summarizes the chemical resistance testing on Z451. Good chemical resistance is needed for post-thinning chemical smoothing, surface roughing etching, photoresist stripping and via cleaning.

Figure 4a shows an acoustic image of a bonded wafer stack after backgrinding to 60µm, and **Figure 4b** plots the total thickness variation (TTV) measurement after grinding.

Before debonding, the wafer stack was laminated onto the UV tape with the dicing frame. The Z451 stayed with the device wafer after debonding. It was then removed from the device wafer without leaving any residue.

RDL-first FOWLP

In the RDL-first FOWLP process, a rigid carrier is used to support RDL build-up, die placement, and wafer molding for a finer length/spacing RDL structure with a better yield. It is commonly agreed upon that the RDL-first FOWLP approach is better suited for high-I/O-count, high-density, and high-value packages. **Figure 5** illustrates the RDL-first FOWLP process flow with the air jetting technology.

As described in **Figure 5**, a sacrificial layer coating on a rigid carrier is typically needed as the first process step prior to all other processing that follows. In general, the sacrificial layer must satisfy the following requirements: 1) Should be thermally stable at 300°C; 2) Should be resistant to all processing chemicals; 3) Should have good mechanical strength at a high temperature; 4) Should be tack free at 300°C; and 5) Can be easily removed from the molded wafer after carrier release.

Z-coat 211 (Z211) is a polyimide-based spin-on polymer designed as a sacrificial layer on a carrier. After spin coating, Z211 is step cured at temperatures up to 300°C to form a smooth, uniform, void-free yellowish dry film on the carrier. The TGA curve of Z211 at a constant heating rate of 10°C/min up to 600°C shows it is highly stable up to 425°C, with a decomposition temperature around 550°C. Z211 resists most processing chemicals in FOWLP fabrication. **Table 3** summarizes the Z211 chemical resistance testing results with various testing conditions.

In the demonstration testing, 200mm dummy silicon was used as the carrier. After a two-layer RDL build-up, flip-chip die placement, and wafer molding (granular epoxy), the carrier was released from the molded wafer with AirDebond®. It is worth noting that tape and frame are not required in debonding. Z211 stayed with the molded wafer and was cleaned by soaking in Z-clean 820C (Z820C) for 30min. It is noted that the molded wafer had an initial warpage of over 3mm with the silicon carrier. After the carrier was removed, the molded wafer exhibited no warpage.

Water cleaning after the 280°C wafer process

Z-coat 100 (Z100) is a water-soluble coating designed to protect the wafer surface and bump structure in wafer temporary support. It is applied

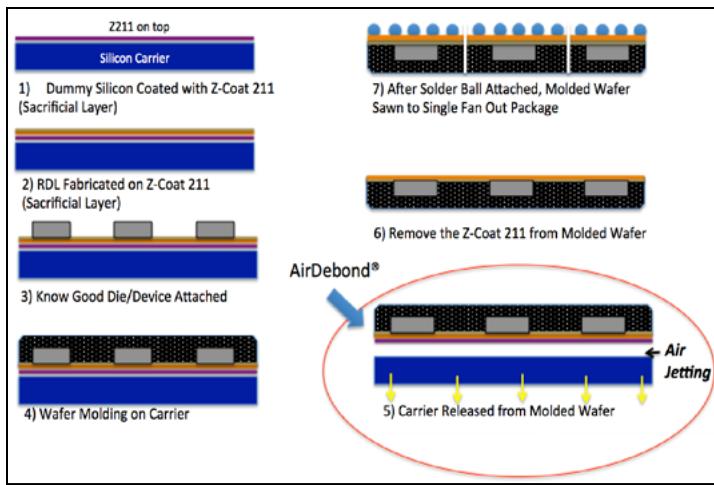


Figure 6: The processing flow with Z100 and BB305.

Z211 Dry Film Chemical Resistance TEST

Chemicals	TEST Conditions	Result
NMP	40 °C 60 minutes	Good/No Failure
2.38% TMAH	25 °C 30 minutes	Good/No Failure
DMAC	25 °C 60 minutes	Good/No Failure
DMSO	25 °C 60 minutes	Good/No Failure
Hydrofluoric Acid 6N	25 °C 30 minutes	Good/No Failure
Acetic Acid 6N	25 °C 60 minutes	Good/No Failure
AK 400 developer	25 °C 60 minutes	Good/No Failure
KOH 0.045%	25 °C 60 minutes	Good/No Failure
PGMEA	25 °C 60 minutes	Good/No Failure
Cyclopentanone	25 °C 60 minutes	Good/No Failure
Acetone	25 °C 60 minutes	Good/No Failure
Al Hydroxide	40 °C 60 minutes	Good/No Failure
10% Oxalic Solution	47 °C 60 minutes	Good/No Failure
Isopropanol	25 °C 60 minutes	Good/No Failure
H2O2: NH4OH	60 °C 60 minutes	Good/No Failure
H2O2 30%	25 °C 60 minutes	Good/No Failure
H2O (8):H2SO4 (1):H2O2 (1)	25 °C 60 minutes	Good/No Failure

Failure Modes: 1) Thickness reduction; 2) Patterns; 3) Discoloration; 4) Film Crack; 5) Surface Sticky/Tacky

Table 3: Summary of the Z211 chemical resistance testing results with various testing conditions.

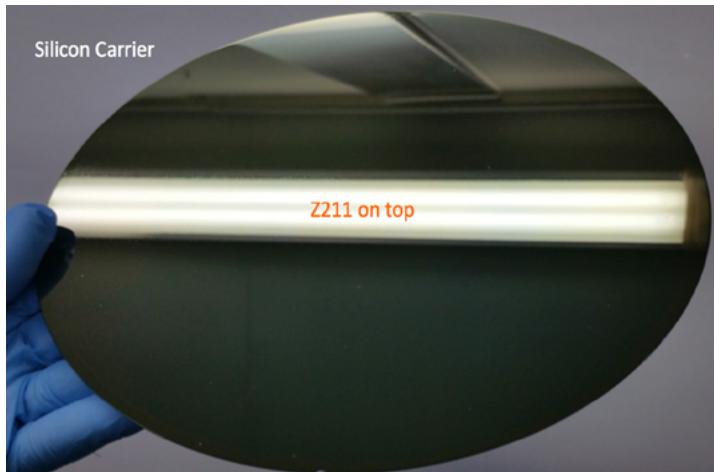


Figure 7: FTIR measurement on the wafer surface before and after the water rinse.

through either spin coating (for thickness <30μm) or stencil printing (for thickness >30μm). For a high topography or bump pattern, a thick Z100 coating fills in the space for surface topography planarization. The coating stays as a dry film after an initial bake and is thermally stable at 300°C.

BrewerBOND 305® (BB305) is an organic bonding adhesive manufactured by Brewer Science for processing up to 300°C. It has excellent chemical resistance. BB305 needs to be spin-coated directly onto the Z100 surface in order to bond the device wafer and the carrier. The BB305 coating completely covers the Z100 up from the wafer edge, including the bevel. The Z100 and BB305 combination is designed to have the wafer bonding stack able to withstand 280°C processing and resist chemical erosion. **Figure 6** shows the processing flow with Z100 and BB305.

Debonding occurs at the interface between Z100 and BB305 with AirDebond® at room temperature. Z100 stays as a dry coating on the device wafer and is completely removed with a deionized (DI) water rinse. **Figure 7** shows the Fourier-transform infrared (FTIR) spectroscopy measurement on the wafer surface before and after the water rinse: no trace of Z100 residue was found.

Water cleaning after IC package assembly with thin substrate

As the organic substrate becomes thinner and larger, it needs to temporarily bond to a rigid carrier for chip assembly and molding. **Figure 8** is the schematic diagram of the process flow for temporarily bonding and debonding for IC packaging with a large, thin panel organic substrate.

Z-coat 110 is a thermal plastic aqueous adhesive. Its rheology property is optimized for stencil printing or spin coating. After coating and soft bake, the adhesive is tack free at room temperature with the Tg around 100°C. **Figure 9** shows that the viscosity decreases

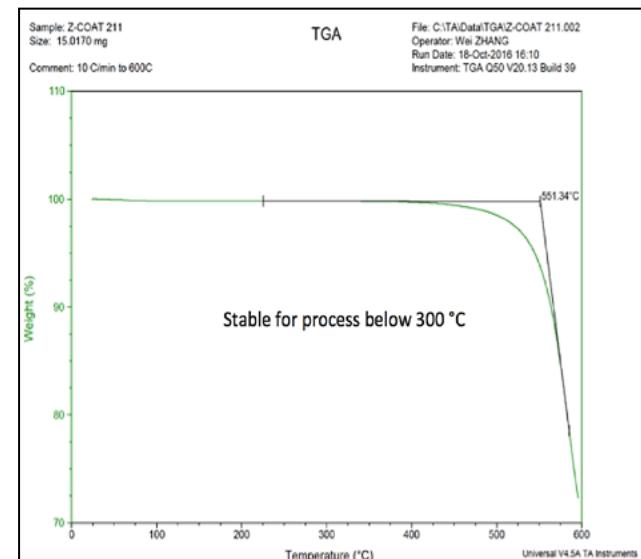


Figure 8: Schematic diagram of the process flow for temporarily bonding and debonding IC packaging with a large, thin panel organic substrate.

with a temperature increase, which is around 48,000cps at 200°C and 36,000cps at 230°C.

In the demo testing, the carrier is a 300mm x 300mm x 1mm thick glass, and the organic substrate is 296mm x 296mm in size and 0.1mm thin within a flip-chip assembly. The mold cap is a 0.4mm thick one block format. The bonding was done in 3min with thermal compression under an ~10Pa vacuum environment. With the substrate supported by the glass carrier, the flip chip was able to be assembled without any issue. After the flux residue was cleaned, the flip chip was over-molded.

The carrier was then released from the molded package with AirDebond®. The majority of the Z110 stayed with the glass carrier, but residue was observed on the side of the solder pad with the substrate. Both the glass carrier and the substrate were cleaned with a deionized water rinse. **Figure 10** compares the molded substrate: a) with the carrier before debonding, and b) after debonding from the carrier. The molded substrate exhibited severe warpage without a carrier.

Summary

A thin wafer/panel temporary support for high-temperature wafer processing emerges as a critical step in the fabrication of a thin, powerful package with maximum heat dissipation. Less expensive room-temperature mechanical debonding is sought after for its better throughput and higher yield. Also in demand are a nontoxic bonding adhesive and an environmentally-friendly cleaner to simplify the cleaning process.

In this paper, we presented AirDebond® as an advanced air-assisted mechanical debonding. It provides a more powerful separation force on the carrier with no tensile

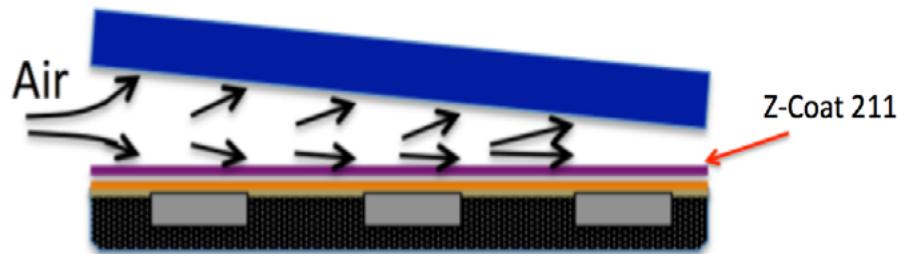


Figure 9: Schematic diagram of the air jetting process setup with the molded wafer on the carrier.

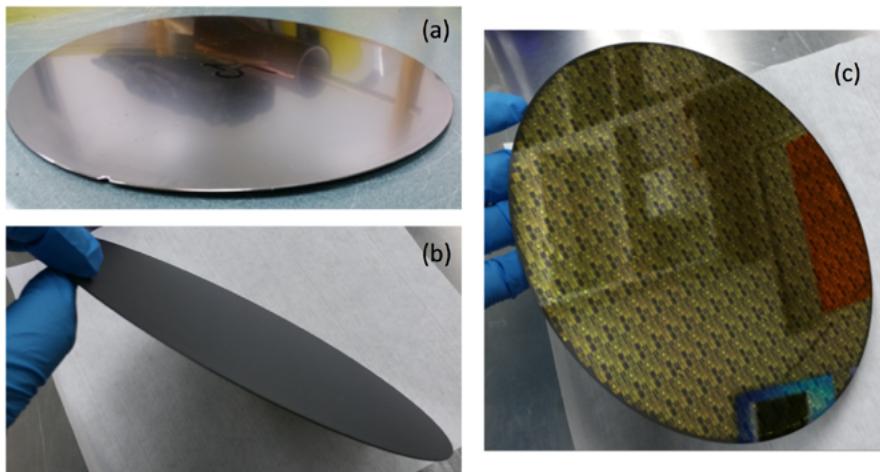


Figure 10: The molded wafer a) before debonding, b) after debonding, and c) after cleaning.

stress and no heat on the device surface. With this debonding, new wafer processing capabilities are being established with a series of temporary adhesives: 1) Z451 allows the wafer stack to be processed at 400°C for 60min; 2) Z211 enables low-cost RDL-first FOWLP with easy cleaning; 3) the combination of Z100 and BB305 allows wafer cleaning with water after temporary bonding for a 280°C processing temperature with harsh chemical soaking; and 4) Z110 enables the molded package to be cleaned with water after the flip-chip process with molded underfill assembly on a 0.1mm thin substrate.

The AirDebond® process is currently being optimized for different applications. With higher performance adhesives and a green cleaner, this technology is starting to prove its value for thin device packaging and assembly.

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Biographies

Hao Tang is the founder and CEO of Micro Materials Inc., Camarillo, CA. He previously worked at various engineering and management positions with Henkel Electronics (Irvine, CA) and Nantong Fujitsu (Nantong, China), focusing on material and process development for flip-chip packaging, fan-out WLP, WLCSP, MEMS packaging, 3D IC integration, and thin substrate assembly warpage control. He received his PhD in Mechanical Engineering from the State U. of New York at Binghamton, and Bachelor of Sciences degree in Engineering Mechanics from Tsinghua U., Beijing, China. Email hao.tang@micromaterials-inc.com

My Nguyen is the Director of Material Development at Micro Materials. He has an over 15-year record of success in developing and designing new materials for semiconductor fabrication and electronic packaging assembly, and has over 50 U.S. patents on formulations of adhesives, coatings, inks and pastes. He received his PhD in Chemical Engineering from Princeton U.

TECHNOLOGY TRENDS



CEA-Leti's extended 300mm line to enable disruptive technologies

Chip Scale Review asked CEA-Leti's Emilie Viasnoff, Deputy Head of its Silicon Component Division, and Christophe Maleville, EVP of Soitec's Digital Electronics Business Unit, to respond to questions that provide insights into the research organization's announcements in 2018 with respect to collaboration with Soitec on a 300mm wafer line that targets disruptive technologies. Such work will undoubtedly have implications for 3D ICs, stacked wafers/dies, and packaging technologies needed for photonics and quantum computing devices.

Introduction

In early December, 2018, CEA-Leti announced an extension of its 300mm silicon-based wafer line to open new R&D avenues for its industrial partners. The extension will allow innovative technological modules to be inserted in, or made compatible with, industrial flows up to completely pioneered technology routes that enable edge artificial intelligence (AI), high-performance computing (HPC), in-memory computing, photonics, power electronics, and other high-end applications.

Question: The news announcement in December highlighted disruptive technologies. What aspects of the development work are expected to be disruptive? What business models or technologies are expected to be disrupted by this work?

Answer: CEA-Leti and Soitec announced in July, 2018, a new phase of their long-standing collaboration, which launched a new 5-year collaboration agreement (2018–2022) focused on R&D for advanced

substrates. This agreement expands the partnership between CEA-Leti and Soitec as it includes the launch of a new prototyping world-class hub – named the Substrate Innovation Center (“Center”) – that will operate a pilot line to share skills between CEA-Leti and Soitec teams. This Center will promote the work of a whole ecosystem around engineered substrates by also opening access to its resources to foundries, fabless companies, equipment and material suppliers, and integrated device manufacturers (IDMs). Industrial partners interested in exploring the possible differentiation with advanced substrates will also be able to evaluate and prototype products in small series at the Center. While a typical manufacturing facility has limited flexibility to try new solutions and cannot take risks inherent with typical prototyping processes, the Center's mission is to become the global entity dedicated to the evaluation of technology choices and the design of substrate solutions to meet the future needs of the semiconductor industry.

With respect to the second part of

the question, there is a consensus that “bleeding edge” technologies, i.e., the continuation of Moore's Law whatever the cost of the technology, is bringing less and less return on investment for most players in the semiconductor industry. In this context there is a critical need for more innovations beyond traditional CMOS scaling. There are many opportunities for innovation in the value chain from semiconductor materials to devices to services, but the simplest yet most important one starts with substrates. Advanced engineered substrates, such as silicon-on-insulator (SOI), provide a key differentiator in achieving energy efficiency across many different applications such as 4G/5G connectivity. Radio-frequency SOI (RF-SOI) and fully-depleted SOI (FD-SOI) are great examples of how the industry is pushing substrate differentiation in developing new standards for RF communication, low-power computing, and AI. FD-SOI is considered today as the best technology platform for energy efficient AI at the edge, sensors and display, automotive,



Figure 1: Ecosystem targeted by the Substrate Innovation Center. SOURCES: CEA-Leti and Soitec

photronics, and edge computing. As this list continues to grow, so does the need for flexibility to continue to innovate and explore new applications made possible by substrates.

Q: What is the timeline for the work being planned?

A: **Figure 1** describes the ecosystem's intention of opening this Center. The facilities are now in place and are accessible to partners all along the semiconductor value chain. In addition, we continue working with equipment vendors to install the required equipment in response to the Center's needs.

Q: Are there any other technical aspects of the work being planned that you think are important and can be shared at this time?

A: Complementary to the Substrate Innovation Center, CEA-Leti and Soitec are active members of The SOI Industry Consortium, which is an industry non-profit organization representing the complete SOI-based microelectronics value chain: digital, RF, power, microelectromechanical systems (MEMS), etc. Its mission includes: 1) Promote and support SOI-based technologies; 2) Promote a comprehensive approach to SOI ecosystems; 3) Promote a market-application-technology-supply chain; 4) Promote a differentiated strategy for "More Moore" and "More than Moore;" 5) Promote innovation through application platforms; and 6) Challenge the SOI ecosystem to build up competitive platforms.

Acknowledgment

For more information about the SOI Industry Consortium, please visit www.soiconsortium.eu.

Biographies

Emilie Viasnoff is Deputy Head of the Silicon Component Division at CEA-Leti, Grenoble. She graduated from Ecole Normale Supérieure in Lyon, France and earned a PhD in Optoelectronics from the U. Paris-Sud, France. She joined CEA-Leti in 2009 after 5 years at Saint-Gobain Recherche working on thin-film processes.

Christophe Maleville has held the role of EVP of Soitec's Digital Electronics Business Unit since 2010. He joined Soitec in 1993 and was a driving force behind the company's joint research activities with CEA-Leti. He has a PhD in Microelectronics from the Grenoble Institute of Technology and obtained an executive MBA from France's Institut Européen d'Administration des Affaires.

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INDUSTRY NEWS



FormFactor adds second European service center

FormFactor, Inc. (NASDAQ: FORM), has announced the opening of a new service center in the key semiconductor manufacturing region of Grenoble, France. The facility will be run with a staff of applications engineers, service engineers, repair technicians, and account managers, and expands the capabilities of the company's existing European service center in Dresden, Germany. The company now has more than 25 service and repair centers globally. Additional service centers are under development for Pyeongtaek, South Korea; Clark, Philippines; and Dalian, China.

"The opening of our new service center coincides with the recent announcement that European Union leaders have pledged to invest €1.75 billion in microelectronics research and innovation," said Robert Selley, Global Senior Vice President, Sales and Service at FormFactor. (Ref.: <http://www.digitaljournal.com/tech-and-science/technology/european-union-invests-1-75-billion-in-microelectronics-research/article/539667>.) "As our customers expand their business, we are deeply committed to enabling their innovation and manufacturing success. We design and ship probe cards with more than 45 million MEMS probes annually to customer fabs around the globe. We've designed the unique capabilities of each service center to help us address customers' services requirements faster, more efficiently, and cost-effectively."

The new service center is located in Montbonnot-Saint Martin, in the greater Grenoble area, in close proximity to key semiconductor manufacturers. This allows the company to rapidly address customers' service and repair requirements for probe cards that serve various segments like automotive, system-on-chip (SoC), power, RF, and optical technologies such as vertical-cavity surface-emitting laser (VCSEL) and image sensors. In addition to multiple offices for local employees, the facility will include a cleanroom to perform probe card repair. This local repair capability significantly increases probe card uptime and profitability for customers.

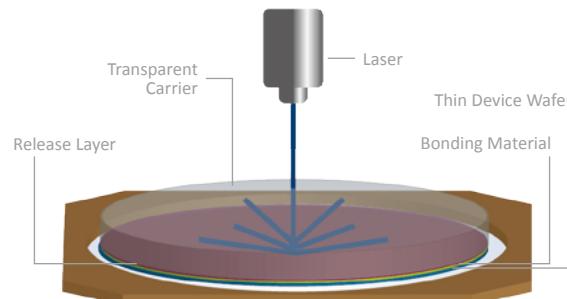


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Creating Safe Environments

Laser Release System

In the laser release system, the device wafer is bonded to a transparent glass carrier using a bonding material and a release material. Once processing is completed, the pair is separated by exposing the release material with an excimer laser or solid-state laser. Low-stress separation coupled with high throughput make the laser release system suitable for all production environments.



Laser Release System Benefits:

- Highest-throughput system available with a release time of less than 30 seconds
- Ultraviolet laser does not heat or penetrate the bulk bonded structure
- Low-stress processing through use of CTE-matched carrier and room temperature separation

Compatible with:

308 nm

343 nm

355 nm

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Senior-level promotions at Indium Corporation

Indium Corporation announced the promotion of three employees to high-level positions in their respective departments.

Scott Pringle has been promoted to Business Unit Vice President. Pringle will continue to be a member of the Management Team, with his new position bringing a focus on aligning the Global Account Sales and the China Field Sales organizations, as well as serving as leader and coordinator of the Asia Sales Leadership Team. Throughout his more than a decade at Indium Corporation, he has distinguished himself as an industry expert and built a strong global sales organization. He has broad and extensive international experience developing business in Europe, the Americas, and Asia.

Chris Bastecki has been promoted to the position of Director of Americas Sales and Global PCBA Marketing. Bastecki, who joined Indium Corporation in 2012, will now lead both the Americas sales and service organization, and the global PCBA product groups to create and execute successful sales strategies and sustained growth. He has more than 25 years of experience in electronics materials marketing, sales, and business management.

Chris has a bachelor's degree in metallurgical engineering from the University of Pittsburgh and an MBA from Carnegie Mellon University. He has participated in numerous leadership development programs at Harvard University and other institutions, as well as Six Sigma training.



From left to right: Scott Pringle, Business Unit Vice President; Chris Bastecki, Director of Americas Sales and Global PCBA Marketing; and Jonas Sjoberg, Associate Director of Global Technical Service and Application Engineering.

Jonas Sjoberg has been promoted to Associate Director of Global Technical Service and Application Engineering. He provides direct management of the Asia Technical team, focusing on promoting career development among his team members through trade show participation and creation of papers for industry publications. Sjoberg also coordinates global technical initiatives with the other technical teams in Europe and the Americas. He joined Indium Corporation in 2014 and has more than 20 years of technical experience in the electronics industry, establishing himself as an industry expert.

Indium Corporation is a materials manufacturer and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

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IWLPIC Technical Committee announces Best Presentation & Papers Awards for 2018

The IWLPIC Technical Committee has announced the Best of Conference, Best Presentation & Best Papers in the WLP, 3D, and Advanced Manufacturing and Test tracks as chosen by the technical committee and attendees. Selections are based on technical merit, relevance, originality, knowledge of subject, quality of material, and quality of presentation.

About IWLPIC

IWLPIC brings together the semiconductor industry's most respected authorities addressing all aspects of wafer-level, 3D, TSV, and integrated system packaging.

Going into its 16th year, the IWLPIC is co-produced by *Chip Scale Review*, the leading international magazine addressing the semiconductor packaging industry, and SMTA, the distinguished global association representing electronic assembly and manufacturing professionals.

The conference comprises three parallel technical tracks with two full days of presentations on wafer-level packaging, 3D integration, and advanced manufacturing and test. Professional development courses, keynote speakers, and panel discussions are offered by world-class experts and enable attendees to broaden their technical knowledge. The technical program includes a two-day expo where 75 exhibitors showcase their latest technologies and products. The conference provides a collective network of over 800 industry professionals, including vendors from leading semiconductor companies, foundries, and OSATS, as well as key technology, equipment, and materials suppliers in the exhibit area. Attendees will be inspired by the quantity and quality of the featured new developments and emerging technologies. The 16th Annual Conference will be held October 22-24, 2019 in San Jose, CA. For more information visit: www.iwlpc.com

	Best Presentation of Conference Robert Hubbard, PhD, Lambda Technologies, Inc. "Failure Relief in FOWLP Polymer Layers"
	Best Paper of Conference Best 3D Track Paper Arnita Podpod, imec "High Density and High Bandwidth Chip-to-Chip Connections with 20µm Pitch Flip-Chip on Fan-Out Wafer-Level Package"
	Best WLP Track Paper Jae Cho, PhD, GLOBALFOUNDRIES "Chip Board Interaction Analysis of 22-NM Depleted Silicon on Insulator (FD-SOI) Technology in Wafer Level Packaging (WLP)"
	Best Advanced Manufacturing Track Paper Habib Hichri, PhD, SÜSS MicroTec Inc. "Fine RDL Formation Using Alternative Patterning Solution for Advanced Packaging"



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Imec's 300mm wafer platform for MOSFET devices with 2D materials

At the 2018 IEEE International Electron Devices Meeting (IEDM) in December 2018, imec presented a 300mm wafer platform for MOSFET devices with 2D materials. Such materials could provide the path towards extreme device-dimension scaling as they are atomically precise and suffer little from short channel effects. Other possible applications of 2D materials could come from using them as switches in the back-end-of-line (BEOL), which puts an upper limit on the allowed temperature budget in the integration flow.

The imec platform integrates as a transistor channel WS2, a 2D material that holds promise for higher "on" current

compared to most other 2D materials and good chemical stability (Figure 1). Imec reported on the metal-organic chemical vapor deposition (MOCVD) growth of WS2 on 300mm wafers, a key process step for device fabrication. The MOCVD synthesis approach results in thickness control with monolayer precision over the full 300mm wafer, and also in potentially the highest mobility material. The benefits of the MOCVD growth come at the price of a high temperature while growing the material.

To build a device integration flow that could be compatible with BEOL requirements, the transfer of the channel material from a growth substrate to a device wafer is crucial. Imec has demonstrated a

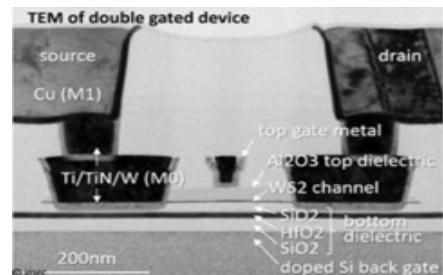


Figure 1: Transmission electron microscope (TEM) image of a double-gated device (WS2). SOURCE: imec

full 300mm monolayer 2D material transfer, which is very challenging on its own because of the low adhesion of 2D materials to the device wafer and to the extreme thinness of the material transferred: 0.7nm. The transfer process was developed together with SUSS MicroTec and Brewer Science using temporary bonding and debonding technologies. WS2 wafers are temporarily bonded to glass carrier wafers using a specially formulated material (Brewer Science). Next, the WS2 monolayer is mechanically debonded from the growth wafer and bonded again in vacuum to the device wafer. The carrier wafer is removed using laser debonding. This debonding technique is a key enabler for the controlled transfer of 2D materials.

Iuliana Radu, Beyond CMOS Program Director at imec, noted that, "Building the 300mm platform for MOSFET device study with 2D materials and developing the process step ecosystem speeds-up the technological adoption of these materials. Several challenges are still to be resolved and are the subject of ongoing research and development." Major challenges include scaling the equivalent oxide thickness (EOT) of gate dielectric for 2D materials, and reducing channel defectivity to boost mobility.

Imec's research into advanced logic scaling is performed in cooperation with its key CMOS program partners including GLOBALFOUNDRIES, Huawei, Intel, Micron, Qualcomm, Samsung, SK Hynix, Sony Semiconductor Solutions, TOSHIBA Memory, TSMC, and Western Digital.

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- 41 technical sessions including:
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- Several evening receptions
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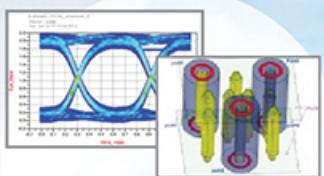
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Cobra Type

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Eye Diagram
4Port VNA Test



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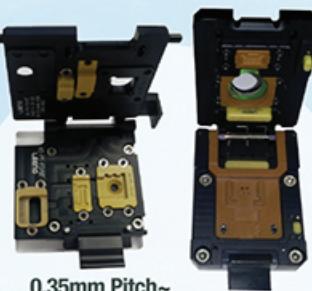
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SLT Socket

0.35mm Pitch~

Compact Camera Module Test Socket



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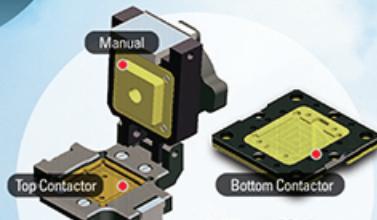
0.35mm Pitch~

Logic Test Socket



0.35mm Pitch~

Memory Socket



0.35mm Pitch~

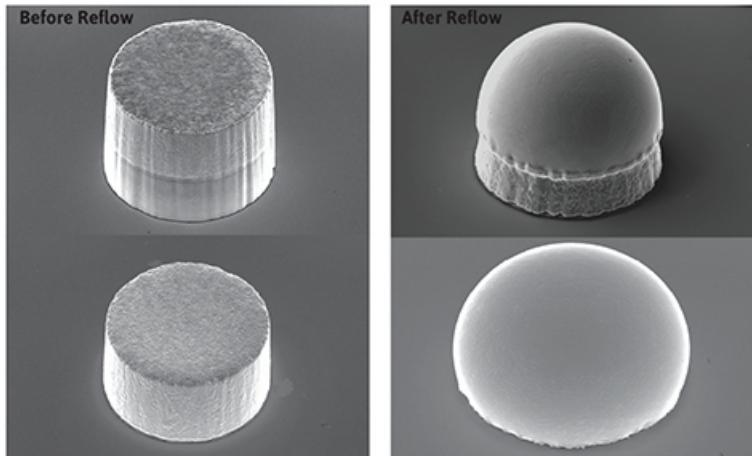
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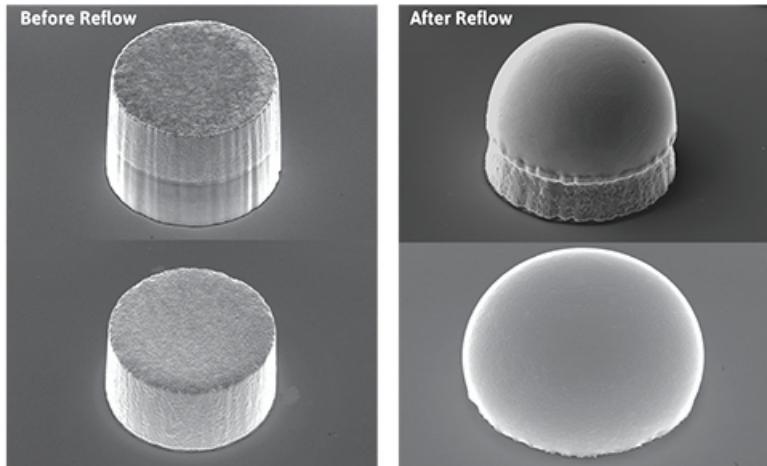
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