

# ChipScale

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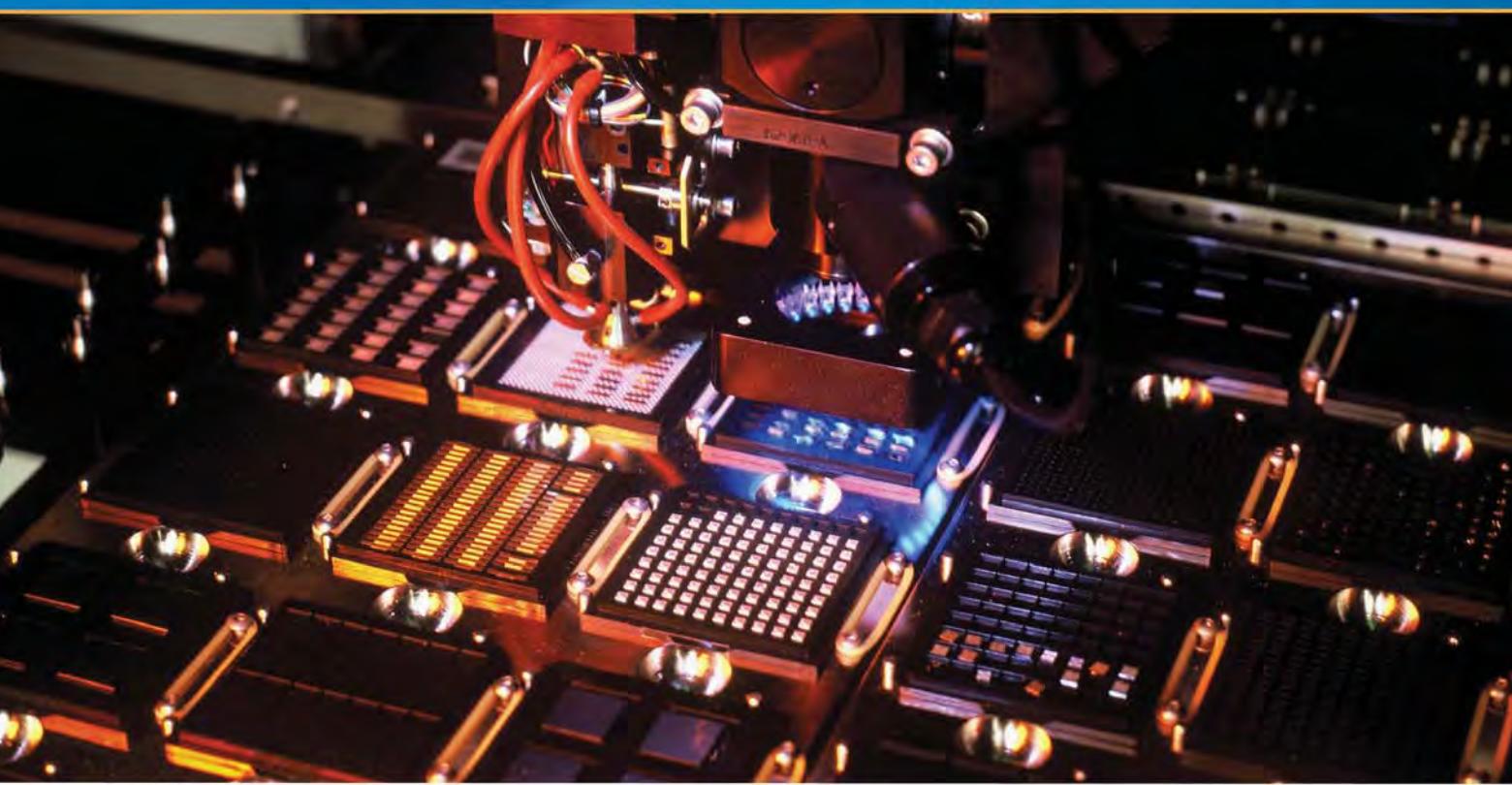
R E V I E W®

*The International Magazine for the Semiconductor Packaging Industry*

Volume 15, Number 1

January-February 2011

- 
- HDI for Flip Chip
  - Copper Bond Test Challenges
  - Relating Spring Probes to Signal Integrity
  - Single Sided Wafer Thinning and Handling
  - International Directory of Test & Burn-In Socket Suppliers



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**January–February 2011**

**Volume 15, Number 1**



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## Chip Scale REVIEW™

*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging  
Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS,  
MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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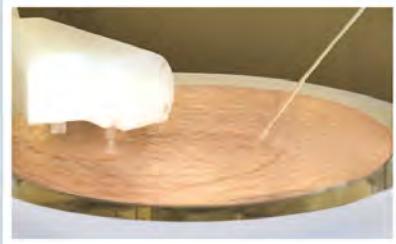


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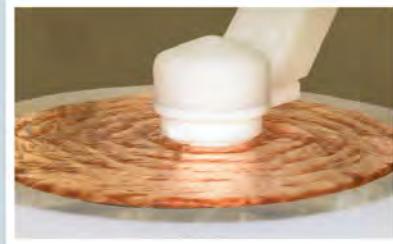


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## STAFF

**Kim Newman** Publisher  
[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)  
**Lawrence Michaels** Managing Director  
[lkm@chipscalereview.com](mailto:lkm@chipscalereview.com)  
**Ron Edgar** Technical Editor  
[redgar@chipscalereview.com](mailto:redgar@chipscalereview.com)  
**Françoise von Trapp** Contributing Editor  
[francoise@3dincites.com](mailto:francoise@3dincites.com)  
**Sandra Winkler** Contributing Editor  
[swinkler@newventureresearch.com](mailto:swinkler@newventureresearch.com)  
**Dr. Tom Di Stefano** Contributing Editor  
[tom@centipedesystems.com](mailto:tom@centipedesystems.com)  
**Paul M. Sakamoto** Contributing Editor Test  
[paul.sakamoto@dftmicrosystems.com](mailto:paul.sakamoto@dftmicrosystems.com)  
**Jason Mirabito** Contributing Legal Editor  
[mirabito@mintz.com](mailto:mirabito@mintz.com)  
**Carol Peters** Contributing Legal Editor  
[cpeters@mintz.com](mailto:cpeters@mintz.com)

## SUBSCRIPTION INQUIRIES

Chip Scale Review  
T 408-429-8585  
F 408-429-8605  
[subs@chipscalereview.com](mailto:subs@chipscalereview.com)

Advertising Production Inquiries:  
**Kim Newman**  
[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)

## EDITORIAL ADVISORS

**Dr. Thomas Di Stefano** Centipede Systems  
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Subscriptions in the U.S. are available without charge to qualified individuals in the electronics industry. Subscriptions outside of the U.S. (6 issues) by airmail are \$85 per year to Canada or \$95 per year to other countries. In the U.S. subscriptions by first class mail are \$75 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a year with issues in January–February, March–April, May–June, July–August, September–October and November–December. Periodical postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

# FROM THE PUBLISHER



## 2011: A Year of Promise

It's that time of year again — when all the forecasters get out their crystal balls and make predictions for the coming year. For the semiconductor device manufacturing industry, 2010 turned out to be a banner year exceeding forecaster's original predictions (32% growth), in part due to an over-correction of 2009's economic decline, as well as the overwhelming success of Apple's iPad and other electronic tablets and smart phones. For 2011, the predictions for growth are conservative, held back by an overcapacity in memory and PCs, yet kept in the positive numbers by enough application growth to offset it. Then again, as I write this, Verizon just announced they will carry the iPhone 4 beginning in February. Will the marriage of what claims to be "the world's fastest network" with the "phone that changed everything" fuel the market more than originally predicted? If iSuppli is correct in their prediction of a 25% increase in iPhone sales, it could very well affect overall growth.

In any case, from where we sit in the world of semiconductor device packaging, we're ready for a year full of promise ahead, with game-changing technologies on the verge of commercialization (3D TSVs, and silicon interposers, to name a few.) We're excited about bringing our readers the most up-to-date technology features from all aspects of packaging. To bring you even more quality content, we've launched *CSR Tech Monthly*, a technology focused eJournal bringing you the latest in packaging processes each month. Don't miss the February issue focused on Wafer Bumping and the March issue focused on Sockets, just in time for the 12<sup>th</sup> annual BiTS Workshop. In addition to expanded editorial opportunities, *CSR Tech Monthly* also gives our advertisers another vehicle for showcasing their expertise and products.

Also underway are plans for the 2011 IWLPC, you'll find the call for papers in this issue. We'd like to thank Luu Nguyen of National Semiconductor for putting on the Tech Chair hat. Andy Strandjord of Pac Tech USA is General Chair for the second year in a row. Other new committee members bringing fresh insight to the event include Ravi Chilukuri, Amkor Technology, and Maaika M Visser Taklo, SINTEF ICT, for the WLP track; Peter Ramm, Fraunhofer, and Herb Reiter, eda2asic Consulting have joined the 3D track with Roger Grace, of Roger Grace Associates joining the MEMS track.

Happy New Year to all! Thanks for helping Chip Scale Review grow and continue to be the go-to publication for the semiconductor packaging industry. ☺

*Kim Newman*

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# EDITOR'S OUTLOOK



## Are Plasmons Living up to the Hype?

By Ron Edgar [[redgar@chipscalereview.com](mailto:redgar@chipscalereview.com)]

Plasmons have been around for a while. There is a ton of research on the subject, but what have they found that might affect us? One end of the spectrum seems to offer hope of solving a number of real-world problems (got my attention) while at the other the pundits are offering “invisibility cloaks” and “perfect lenses.” It seems the possibilities for plasmons are almost endless. At the recent Nanometa Conference at the Seefeld Ski Resort in the Austrian Tirol, research paper after research paper explained the many facets of plasmonics. (<http://www.nanometa.org/>)

Before we go any further, for those who are not clear, what is a plasmon? A plasmon is the excited state of the electrons in a conductive material. When a force displaces electrons from their “normal” positions, the resultant positive forces try to attract electrons in an effort to balance the charges. The result is that the electrons oscillate. Depending on the physical constraints of the conductive material, the oscillation can have very defined wavelengths. Nanoparticles can have very discrete plasmonic modes whereas large structures, like thin metal films, can support a broad range of wavelengths. Many of these wavelengths are in the optical range.

Back in 2006, a group from Stanford (Rashid Zia, Jon A. Schuller, Anu Chandran, and Mark L. Brongersma) published a paper, “Plasmonics: the next chip-scale technology.” They explained that, “A tremendous synergy can be attained by integrating plasmonic, electronic, and conventional dielectric photonic devices on the same chip and

taking advantage of the strengths of each technology,” and the technology of plasmonics “... exploits the unique optical properties of metallic nanostructures to enable routing and manipulation of light at the nanoscale.” There have been, and continue to be, tremendous hurdles to overcome but this technology is ready to come out of the lab and is, in my opinion, a soon-to-be-mainstream technology.

Chips are becoming so hot and, with 3D stacking, the problem is exacerbated. With resistive metallic interconnects, the result is heat. If interconnects could be done optically, the result might be a cooler chip. However optics (photonics) do not scale well with the size of CMOS structures — but plasmonic ones do. A 2010 paper, “Towards Chip-Scale Plasmonic Interconnects,” (Wassel1, Tiwari1, Valamehr, Theogarajan, Dionne, Chong, and Sherwood from UC Santa Barbara and Stanford University) concluded, “... while pure plasmonics cannot provide a competitive energy efficient link, a hybrid plasmonic/photonics link provides the opportunity to replace short electrical links leading to latency and energy savings.” These interconnects cannot work as a universal solution but for critical high speed connections they may well fit the bill. They are being discussed for use as clock distribution or for interconnecting multiple cores, situations with high associated heat generation.

I hope you will take the time to look further. As for the “invisibility cloak,” I’m not holding my breath, but . . .

Once again we have a great spread of articles. Vern Solberg of Tessera, *HDI Solution for Very Fine Pitch Flip-Chip*

*Applications*, extols the virtues of “a truly novel approach for flip-chip substrate fabrication” where copper pillars improve control of the bump. *Copper Bond Testing Challenges* from Kamran Iqbal of Nordson DAGE discusses the First Bond Ball Pull test protocol and concludes that “The migration to copper from gold as an interconnect medium is set to continue . . .” *A Cost Comparison for Flip Chip, Wire Bond, and Wafer Level Packaging* by Chet Palesko of SavanSys Solutions, LLC, and E. Jan Vardaman of Techsearch International, Inc., is an insightful look at the strengths and weaknesses of each technology. If you are interested in “a novel chemical technology that thins wafers down to 50 $\mu$ m or less, with better uniformity, and at a lower cost than conventional thinning,” then be sure to read *Single Sided Wafer Thinning and Handling* by Ricardo I. Fuentes of Materials and Technologies, Corp. (MATECH). With RoHS came new challenges. This article by Kimberly D. Pollard, Allison Rector, and Michelle Wheeler of Dynaloy LLC., *Cleaning: The Forgotten Challenge*, characterizes “the cause of a common defect in lead-free electroplated solder formation — residual Cu . . .” *Copper Wire Interconnect has Arrived* by Flynn Carson, STATS ChipPAC, adds more information on why copper is overtaking gold.

From our own Paul Sakamoto we have, *Upgrading ATE Systems for Known Good Die Testing*, and Françoise von Trapp brings us up to date with 3D: *You’ve Come A Long Way, Baby!* All great reading, I trust you gain new insight from our offerings. 



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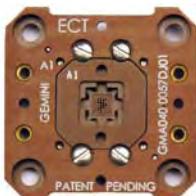
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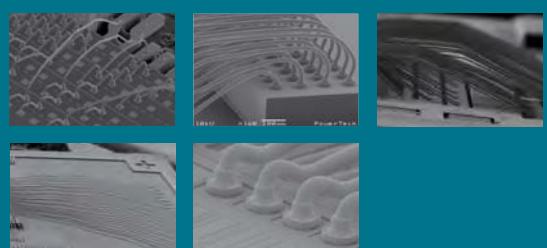
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# 3D: You've Come A Long Way, Baby!

By Françoise von Trapp, Contributing Editor [*3D InCites*]

**A** year ago, there were still skeptics in the room at the annual 3D Architectures for Semiconductor Integration and Packaging conference, sponsored by RTI's Tech Venture Forum. This year, not a single hand went up when Phil Garrou asked if anyone doubted that through silicon vias (TSVs) would be industrialized. It seemed everyone has reached a consensus: 3D ICs with TSVs are the way to go to achieve the performance, power, form factor and cost requirements of next generation semiconductor devices. But this consensus wasn't unique to this event, and it isn't just the R&D institutes that are banging the 3D drum. Major fabless, foundries, IDMs and packaging houses have all taken up the call to arms.

At SEMICON Taiwan, Nokia announced they will target a wide I/O single package 4 DRAM stack, combining the best of both worlds, wide I/O for performance, and TSVs for form factor (thin, multi-die stack). According to Klaus Hummler, Ph.D., senior principal engineer for the 3D interconnect division at SEMATECH, this is a perfect vehicle for Nokia to implement without over extending itself, because it doesn't require all the elements to be completely ready (e.g., true 3D co-design tools). Wide I/O DRAM on logic presents the lowest risk opportunity, he says. Hummler also noted that at 2010 IMAPS International Symposium in Raleigh, NC, the 3D panel discussion was particularly interesting, because of the "unusual degree of consensus" on how 3D will be implemented in high volume manufacturing (HVM), although there are still arguments about the timelines. Urmi

Ray, Ph.D. of Qualcomm said the company is on an aggressive timeline for implementation of 3D with TSVs, with commercial engagement foreseen in 2012. Nokia is targeting 2013 for HVM.

At IEDM 2010, in San Francisco, Kinam Kim, of Samsung Electronics, presented a talk entitled "From the Future of Si Technology Perspective: Challenges and Opportunities." Despite the still existing challenges of design, process and standardization, there's no question from Kim's perspective, "3D Si technology will have to be adopted in the technology roadmap," he said. He even offered a comparison between package-on-package (PoP) stacking and wide I/O TSVs that favored TSVs for package size, power consumption and bandwidth. In a technology presentation, TSMC's J.C. Lin talked about the company's investment into back-end-of line (BEOL) processes, and demonstrated that it has optimized TSV processes to its satisfaction.

## Why not CMOS Scaling?

In his pre-conference symposium presentation at the RTI event, Phil Garrou, Ph.D., of Microelectronic Consultants of NC, said that CMOS is "running out of gas", and driving the industry to 3D IC. Some technology 'brick walls' noted by Garrou include transistor gate delay, problems with low-k dielectrics; electrical performance issues such as copper resistivity, clock speed, and memory latency; and the cost of continuing traditional scaling.

As Subramian Iyer, IBM, noted, the industry has really been scaling through engineering, and that the role of memory

in processor and system performance is what got him involved in 3D. "3D integration is a logical extension of the holistic embedded memory roadmap and is a big deal for heterogeneous integration," noted Iyer. IBM is fully on board with 3D, as evidenced by their announcement of collaboration with Semtech Corp, supplier of analog and mixed signal semiconductors to develop a high-performance integrated ADC/DSP platform using 3D TSV technology.

Clearly, the message has shifted slightly. Last year, there was talk of the end of scaling and a shift to 3D integration as the solution. Now, we're hearing that 3D integration is a way to continue scaling. Either way, 3D integration seems to be the answer to the continuation of Moore's Law.

## Silicon Interposers: The First Step

In his presentation at the 3D Architectures conference, Jean-Marc Yannou, of Yole Développement remarked that this year's topic of the conference is interposers, whereas one or two years ago, interposers looked to be a remote dream technology that would act as a bridge to fill 3D ICs. Now it seems clear that interposers provide the logical first step to industrialization of 3D TSVs, and will be more than just a bridge technology.

"Ultimately we believe 3D is the best in performance and density — however you can't underestimate the potential and advantage of the interposers, they will always play an important role," noted Douglas Chen-Hua Yu, Senior Director of Integrated Interconnect and Packaging Division, TSMC, R&D Group. Silicon

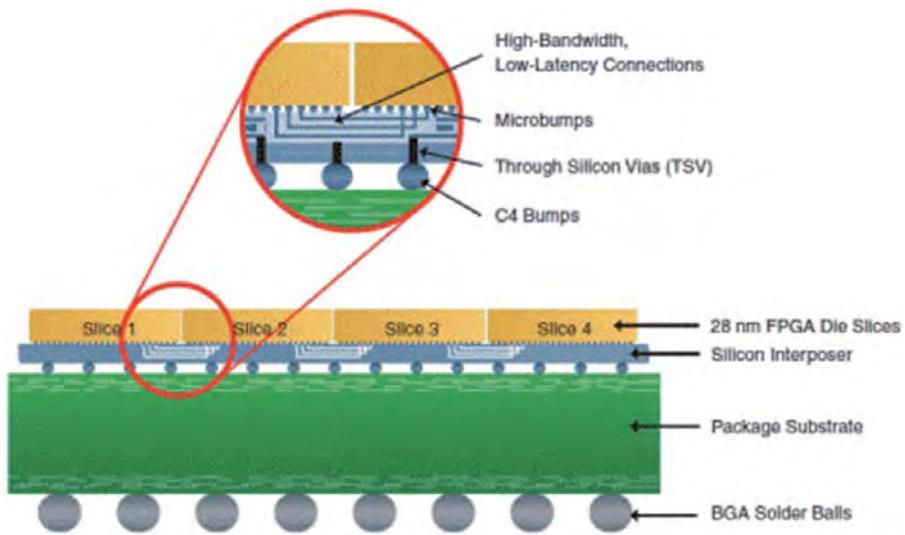


Figure 1. Xilinx silicon stacking technology.

interposer technology is also being leveraged by ASE to stack and assemble different technology chips from its foundries and customers. Calvin Cheung, VP of engineering at ASE Group said that the company sees many applications for interposer technology including integrating them into next-generation package-on-package (PoP) configurations due to requirements getting thinner with closer pitch requirements (100 $\mu$ m and 150 $\mu$ m) between silicon interposer and package substrates; and stacking logic/memory next to RF and MEMS devices on a silicon interposer in a heterogeneous configuration. "Silicon interposers aren't merely a stop-gap technology," noted Cheung. "We see long term value for silicon interposers."

Interposer technology makes sense because it leverages existing infrastructure; design tools are easily adapted to accommodate them; and as a result they will achieve a quicker time to market. As of early December, it was clear that 3D integration through the use of interposer technology was well on its way.

"What we heard this week is what we've been waiting for the last few years," said Garrou, referring to trilogy of 3D developments that include the aforementioned collaboration between IBM and Semtech; Samsung's development of an eight gigabyte (GB) registered dual inline memory module based on its

advanced Green DDR3 DRAM that incorporates 3D TSVs; and Xilinx's silicon stacking technology headed for production (**Figure 1**). All of these are expected to ramp into production in the 2011, 2012 time frame. Garrou added that similar announcements will start coming fast and furious, with silicon interposers leading the charge.

### Blasting through Remaining Roadblocks

Last year, there was little to report regarding progress in the design, test, and standards development areas; and all these were identified as limitations to market adoption. How things have changed.

At the 3D Architectures conference, Synopsys' Antun Domic and Cadence's Vassilios Gerousis presented their progress on design tools, Erik Volkerink of Verigy talked about the company's approach to 3D test, and there was a whole panel discussion devoted to the topic of standards.

According to Domic, Synopsys supports a phased approach and has proposed a "2.5D" IC implementation flow incorporating package, silicon interposer, and die co-design. He says this could be accomplished in a relatively small time frame. "The impact of 2.5D IC integration looks more affordable, all the necessary ingredients are at hand, and is a launch pad for 3D integration." He said, adding that the road has to be paved technically and

economically for all the players to be successful. Synopsis is working with its partners to make sure that all the EDA ingredients are timely available.

Gorousis concurs that it's not just a matter of optimizing chips, but the package and PCB as well. Cadence has been working with ST Microelectronics to develop a multi-platform design methodology that involves system architecture and partitioning. He reports that a complete ST/Cadence solution for TSV management exists.

From the test perspective, Volkerink says Verigy is taking a multidisciplinary approach for 3D that includes design, design for test, manufacturing, probing TSVs, wafer test, final test, test methodologies and test architectures. "It's about what defects and failures that you want to detect," he says, noting that 3D integration causes an exponential increase in interactions. Some of the answers might be in 3D adaptive test.

Cheung says ASE sees the 3D TSV interconnected dice stacks as an industry game changer, while emphasizing that work is needed industry-wide to enable cost-effective design and 3D IC manufacturing. Industry standards will play a major role to utilize economies of scale in production and shorten time-to-market for 3D IC design. Calvin also highlighted the need for new business models to clarify responsibilities and gains for the different players in the 3D IC eco-system.

### Conclusion

Several initiatives, work groups, and collaborative efforts have surfaced in the past few months focused on design tools, test methodologies, and standardization, supported by industry organizations like SEMI, the Global Semiconductor Alliance (GSA), IEEE, SEMATECH, Semiconductor Industry Association, and Semi Research Corp. Still even now, none of these so-called limitations are considered to be show stoppers to 3D integration. If all goes according to plan, 2011 could be the year it all comes together. Bring it on! 

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# DOE Relates Spring Probe Variables to Signal Integrity

By Ila Pal [Ironwood Electronics]

One of the modern world's driving engines is the semiconductor, also referred to as the integrated circuit (IC). These ICs are fabricated, assembled and tested in billions of units every year. The semiconductor industry is driven by the mantra "small, fast and cheap". Testing challenges increase due to smaller device size and faster performance (bandwidth). The socket industry that enables semiconductor device testing is heavily taxed by smaller and faster devices in addition to the other supporting segments of the semiconductor market. IC device manufacturers and test houses require reliable socket solutions for these high performance devices. Smaller and faster devices are typically more sensitive to changes in the electrical configurations used for testing, particularly in the case of AC performance or "signal integrity".

## Automatic Test Equipment System

A typical test system includes hardware and software to run different tests that validate IC performance. Test systems can be categorized as consisting of four distinct components — tester, load board, test socket, and handler. The test socket is mounted to the load board, which in turn is interfaced to the tester. A handler includes compartments for trays where devices under test (DUTs) are stored. A vacuum head/plunger inside the handler inserts the DUT into the test socket (bringing the IC contacts together with the test socket contactors) while the tester component performs the necessary tests. If we think of a test socket as the 'heart' of an automatic test equipment (ATE) system, then the spring probes are the 'arteries' that transfer the signal from the DUT to the tester through the load board. The health of these spring probes is essential to the performance of the test socket—but how do we test the spring probes or rate their health?

## Signal Integrity

Insertion loss of the spring probe is one of the first parameters verified by the

electrical test engineer. This determines whether the socket/interconnect system will pass the functional device test. There are seven principles for optimized insertion loss mentioned which are listed below.<sup>1</sup>

- Match the characteristic impedance of the socket to 50Ohms
- Keep the impedance constant through the socket
- Optimize (minimize) pad stack up capacitance
- Keep the socket contacts short
- The dielectric loss of the socket is not critical
- The conductor loss of the socket is not critical
- The contact resistance of the socket is not critical

Spring pins are a common interconnect medium used in the socket (**Figure 1**) and there is no established relation between critical spring probe parameters and their influence on signal integrity, other than keeping those contacts short. There is no baseline reference (or starting point) for spring probe design, which is an everyday need due to emerging new application requirements because of the varying functionality of IC devices. For example, an IC with a data rate of 5Gbit/s requires

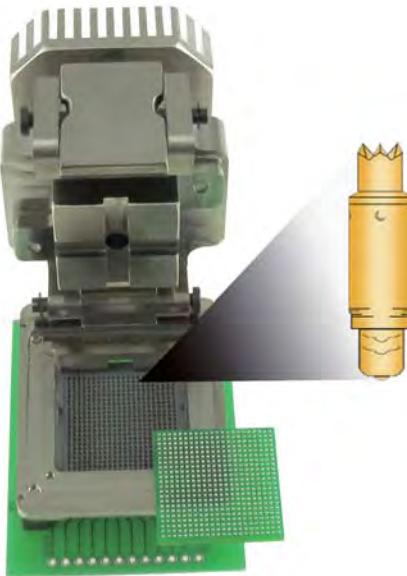


Figure 1. Spring pin socket showing features of spring probe contact.

a bandwidth of 2.5GHz. And when functions are extended to 3<sup>rd</sup> or 5<sup>th</sup> harmonics, depending upon the requirement, a corresponding bandwidth of 7.5GHz or 12.5GHz is needed. One way to accomplish this requirement is to over design a spring probe by making it extremely short, which means compromising mechanical features for electrical superiority. In addition to electrically testing the IC devices, the spring probes need to repeat the test for millions of IC devices. This can mean mechanical features become as critical as the electrical requirements. How can one strike a balance between electrical requirements and mechanical features?

## Design of Experiment

DOE (Design of Experiment) was used to demonstrate model development to identify the optimized frequency without compromising mechanical features. The first step was to design a set of experiments by identifying key input factors and output responses. In our experiment, we used spring pin length, width, and the ground pattern as input variables. We defined bandwidth as our output parameter for each experiment. Spring pin length was varied from 1mm to 4mm while spring pin diameter was varied from 0.25mm to 0.35mm. We used two ground patterns in our experiment. The first configuration was the typical 'G-S-G' and the second used ground pins surrounding the signal pins in all four directions. Pitch was kept constant at 0.5mm. Full factorial design with 2 levels for each factor resulted in 8 experimental runs. Blocks were not used, as the experiment is not dependent on the time factor. **Figure 2** shows run order, input variables, and the output variable.

## Statistical Model

After running experiments, results were analyzed using DOE software. The first step in analyzing the data was to identify which input variables and their interactions had significant influence on the output variable. Typically, half normal plot and

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Standard Order	Run Order	Block	Diameter (mm)	Length (mm)	Ground pattern	Bandwidth (GHz)
7	1	Block 1	0.25	4	C2	14
4	2	Block 1	0.35	4	C1	5.6
3	3	Block 1	0.25	4	C1	13.9
8	4	Block 1	0.35	4	C2	4
5	5	Block 1	0.25	1	C2	31
6	6	Block 1	0.35	1	C2	14.8
2	7	Block 1	0.35	1	C1	19
1	8	Block 1	0.25	1	C1	33

Figure 2. Design of Experiments table showing run order, input variables and the output variable.

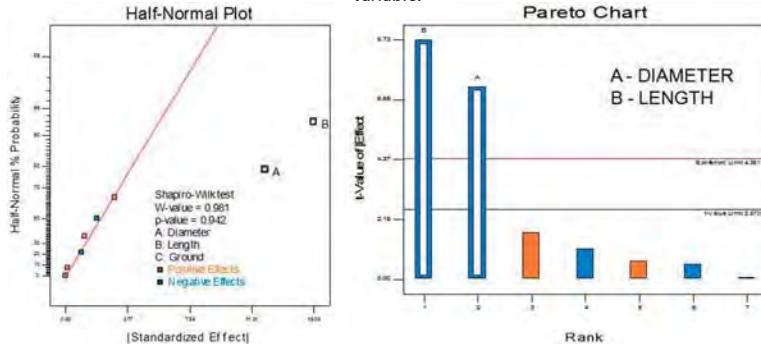


Figure 3. Half normal plot and Pareto charts showing the significant input factors from the insignificant ones.

pareto charts are used to separate the significant variables from the insignificant ones. From **Figure 3**, it can be seen clearly that spring pin length had the ultimate effect on bandwidth, followed by spring pin diameter. These are known as ‘main effects’. The ground pattern did not have any influence on the bandwidth and neither does the interaction of input variables. The next step was to generate an equation using these two input variables. DOE software presents this model through regression analysis. (Bandwidth =  $65.85 - 121.25 * \text{Diameter} - 5.025 * \text{Length}$ )

## Analysis of Variance

The above equation is valid within the limits used in our experiments (spring pin length from 1mm to 4mm and spring pin diameter from 0.25mm to 0.35mm). The next step is to verify the validity of the model using analysis of variance function (ANOVA) in the DOE software. The Model F-value of 62.78 generated by ANOVA implies the model is significant. There is always a question of error percentage. There is only a 0.03% chance that a “Model F-Value” this large could occur due to noise. “Prob > F” value is less than 0.05 which indicates that the

Values greater than 0.1 indicate the model terms are not significant (i.e. ground pattern and other interactions between input variables). Another factor used to validate the model is R-square (correlation factor). The maximum correlation is 1.00. In our case, the R-square value is 0.96 which means the model is very much coherent with the experimental data.

## Model Validation

After developing the model and determining the relationship of spring pin length and diameter to bandwidth, the next step was to verify the model through experimentation. The main objective was to maximize spring pin bandwidth. Once this criterion was set in the DOE software, many solutions were found. The selected solution for our experiment recommended 1mm long and 0.25mm diameter spring pins with the G-S-G pattern. The software also predicted the output bandwidth to be 30.5 GHz with a desirability of this outcome at 91%. The experiment was run using the selected solution variables and the results are shown in **Figure 4**.

From the graph, it can be seen that the insertion loss of -1dB = 30.9GHz. This frequency is within 1.3% of the predicted

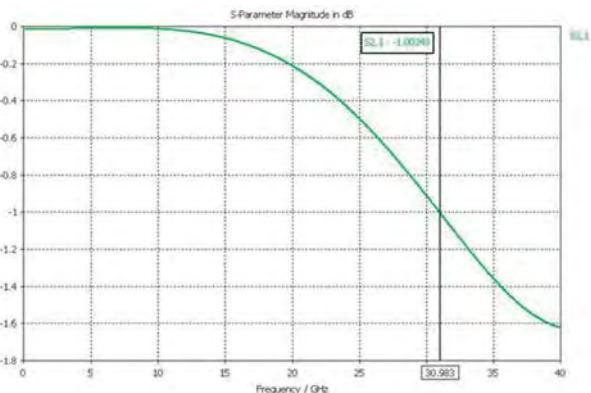


Figure 4. Maximum bandwidth criteria represented in frequency versus insertion loss graph.

model terms are significant with a 95% confidence interval criteria. In this case, spring pin length and diameter are significant model terms.

value of 30.5GHz. The verification experiment proved the model was valid.

To be certain, a second experiment was planned to verify the model. We chose two parameters optimization. In this case, the main objective was to maximize both spring pin bandwidth and spring pin length. Maximizing spring pin bandwidth and spring pin length gains a mechanical advantage without losing electrical requirements. Maximum pin length (and thus a maximum spring length) ensures proper contact force. This ‘must have’ feature in direct correlation to DC resistance also suits better interconnect compliance. Target PCBs need more compliance to accommodate coplanarity variations due to mask thickness or plating thickness variations. IC devices with warpage and ball height variation also need more compliance to engage all pins, leads, or balls. Once this maximum spring pin bandwidth and maximum spring pin length criterion was set in the DOE software, many solutions were found. The selected solution for our experiment recommended 0.25mm diameter and 3.64mm long spring pins with a ground pattern around all signal pins. The software also predicted the output bandwidth to be 17.25 GHz with a desirability of this outcome at only 63%. Then the experiment was run using the selected solution variables. The results are shown in **Figure 5**. From the graph, it can be seen that the insertion loss of -1dB = 15.2GHz. This frequency was within 12% of the predicted value of 17.25GHz. Since the model cautioned that the desirability was only 63%, the actual result has to be used with a proper safety margin. The second experimental run also proved the model was valid (with proper precautionary measures).

## Conclusion

This modeling technique can be extended with more input variables as well as output variables. The method allows one to choose which input variables will have significant influence on the output variables. This means insignificant variables need not be tightly controlled. This will make a significant difference in manufacturing and the yield can be improved to a higher sigma level—Design For Manufacturability. The model serves as a baseline reference and starting point for any spring probe design. By establishing relationships between critical spring probe parameters and their influence on signal integrity, the design cycle of new spring probes is reduced to coincide with a test process. Caution must be exercised when using the model with its boundary conditions and one must understand the desirability of

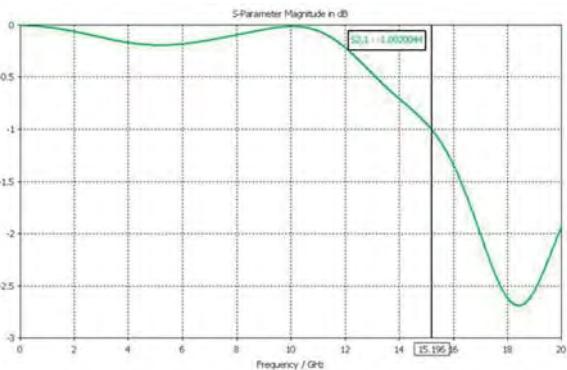


Figure 5. Maximum bandwidth and maximum length criteria represented in frequency versus insertion loss graph.

outcome. For example, spring pin length has to be between 1mm and 4mm and spring pin diameter has to be between 0.25mm and 0.35mm. By going through this statistical modeling, we identified that ‘keeping it short’ in addition to ‘keeping it skinny’ are must-have spring pin features for optimized frequency characteristics in semiconductor test applications. Future work will include more spring pin variables such as plating, tip geometry, spring force as input factors and include mechanical

life of spring probe in addition to electrical requirements as output factor. This will enable a mechanically and electrically optimized solution for semiconductor test applications.

## Author

Ila Pal is VP of Marketing at Ironwood Electronic, USA. He holds a MS degree in Mechanical Engineering from Iowa State University, Ames, USA. He holds a MBA degree from University of St. Thomas, Minneapolis, USA. He has six patents relating to high performance BGA socket design. He has presented many papers related to interconnection technology and published articles in reputed journals. He has spent more than 15 years developing new technologies in the Packaging and Interconnection field. He can be reached at [ila@ironwoodelectronics.com](mailto:ila@ironwoodelectronics.com).

## References

1. Eric Bogatin, *BiTS 2005 Signal Integrity of Test Sockets — Simplified*, page 32

# From One Engineer To Another

***“Are lead-containing alloys still allowed in applications for semiconductor and power semiconductor assembly?”***



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# INDUSTRY NEWS

## IWLPC Announces its Call for Papers

The SMTA and *Chip Scale Review* magazine are pleased to announce plans for the 8th Annual International Wafer-Level Packaging Conference and Tabletop Exhibition. This premier industry event explores leading-edge design, material, and process technologies being applied to Wafer-Level Packaging applications. There will be special emphasis on the numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand wafer level packaging solutions for integration, cost, and performance requirements.

The conference includes three tracks with two days of technical paper

presentations covering wafer level packaging, 3-D (stacked) packaging; and MEMS packaging.

The IWLPC Technical Committee, headed up this year by Technical Chair, Luu Nguyen of National Semiconductor, invites you to submit an abstract for this program. Deadline for submittal is April 22, 2011.

If you would like to present at this conference, please submit a 200-300 word abstract through the IWLPC website by April 22nd, 2011. Please include a title, author name, and contact information with your abstract. Authors will be notified of acceptance in late May/early June 2011. Note that technical papers are required and will be due in August 2011. For more information on the conference, or exhibit and sponsorship opportunities please contact Patti Hvidhyld at 952-920-7682 or send an email to [patti@smta.org](mailto:patti@smta.org).

## SEMI Honors Developers of Tessera Chip-Scale Packaging Technology

In recognition for contributions to the development and commercialization of Tessera's Micro Ball Grid Array ( $\mu$ BGA<sup>®</sup>) technology, SEMI awarded



Thomas Di Stefano, John W. Smith, Jr. and Michael Warner the 2010 SEMI Award for North America; the association's highest honor for technical contributions to the semiconductor industry. The award was presented during a banquet at the 2011 SEMI Industry Strategy Symposium (ISS) in Half Moon Bay, California.

"Our industry honors Tom Di Stefano, John Smith and Michael Warner for their combined efforts to commercialize  $\mu$ BGA<sup>®</sup> technology while at Tessera Technologies," said Stanley T. Myers, president and CEO of SEMI. "This critical packaging technology was an important development in the proliferation of smaller personal electronic devices that have spurred the market for semiconductor devices."

Di Stefano was the founding president of Tessera Technologies and a co-founder of *Chip Scale Review*, where he continues to be a regular contributor, and serve on the editorial advisory board. Di Stefano helped build Tessera into a world leader in miniaturized packaging. John W. Smith, Jr. joined Tessera in 1992 as its CEO where he served until his retirement in 2000. Michael Warner, a Tessera Fellow, joined the company in 1994 as the vice president responsible for developing products employing  $\mu$ BGA solutions for commercial applications.

"The introduction of chip scale packaging by Tessera enabled a decrease in package size and an increase in package frequency while reducing the total power required," said Bill Bottoms, chairman of the SEMI Award Advisory Committee. "This innovation is now the packaging solution of choice for most memory devices and a significant number of logic devices. It was initially adapted to meet performance requirements and the high-volume commercialization led to its widespread adoption as a lower-cost packaging alternative."

## Alchimer Appoints Chief Operating Officer

Industry veteran Erik C. Smith has been appointed chief operating officer of

Alchimer S.A., provider of nanometric deposition technology for through-silicon vias (TSVs), semiconductor interconnects and other electronic applications. Smith brings 25 years of semiconductor industry experience to this fast-growing start-up, including five years as president and COO of Qcept Technologies, a manufacturer of inspection systems for detecting non-visual defects (NVDs) on wafers. In addition to day-to-day operations, Smith was responsible for product development, applications, and sales and marketing.

"Erik's proven record as a COO, combined with his sales and marketing expertise and his in-depth experience in Japan, China, and other Asian markets, will help Alchimer capitalize on the momentum we have created around the globe," said Steve Lerner, CEO of Alchimer.

Prior to Qcept, Smith spent 12 years in a variety of management and senior executive positions at Ultratech Inc., including senior vice president of worldwide sales and marketing, helping the company achieve market shares of greater than 80% in the advanced packaging lithography business and greater than 90% for 300mm products at semiconductor IDMs. As managing director of Ultratech K.K., he helped launch Ultratech's Japanese operations. Smith will be based in Silicon Valley.

## STATS ChipPAC Reports Significant Growth in Flip Chip Business

STATS ChipPAC's strategic investments in its flip chip manufacturing operations have clearly paid off. With over 250M flip chip package units shipped last year, the semiconductor test and advanced packaging service provider reports that its flip chip business grew more than 50% in 2010 compared to 2009.

According to the company, the rapid expansion of its flip chip technology has been able to support the growth of its flip chip customers. STATS' flip chip portfolio ranges from large single die fcBGA packages with passive components used for graphics, CPU and ASIC devices to smaller fcFBGA packages including single die, multi-die

and stacked configurations that combine wire bond and flip chip technology within a single package.

Raj Pendse, Vice President of Advanced Product and Technology Marketing, STATS ChipPAC attributes the growth to the company's strong position in packaging for the mobile market, and increased market share in the computing and networking markets, as well as its diverse flip chip technology portfolio.

During 2010, the company continued to ramp production of its flagship bond-on-lead (BOL) interconnection technology. Additionally, to address a wider range of applications requiring higher I/O densities, STATS introduced copper column bump in conjunction with the BOL design for a cost effective, lead-free flip chip process that is scalable to very fine bump pitches. A number of process innovations in areas such as bumped wafer thinning, advanced molding technology, and die and substrate

handling were introduced to achieve thinner flip chip packages with higher yields.

These core enabling technologies are expected to provide a seamless migration path into more advanced solutions such as through silicon via (TSV), which require fine silicon-to-silicon and silicon-to-substrate interconnection. STATS ChipPAC's Singapore facility is already active in the development of TSV technology solutions.

"We have also expanded our foundry alliances to enable early development and qualification of flip chip packaging solutions for advanced silicon nodes. We are confident that these factors will provide us with a healthy growth trajectory going into 2011," said Pendse.

### Crane Aerospace & Electronics and Crane Electronics Inc. Awarded \$14.2M DOD Contract

Crane Aerospace & Electronics and Crane Electronics, Inc., Power Solutions

was awarded a \$14.2M contract by the U.S. Department of Defense for production of the Keltec Band 9/10 Transmitter High-Voltage Power Modules for the AN/ALQ-99 Tactical Jamming System. Under the contract, Power Solutions will work closely with the Navy Airborne Electronic Attack Systems Division in support of the ALQ-99 Pod.

"We are pleased to have been selected and are confident that with our clear focus on electronic warfare and radar systems, we can achieve the necessary results to sustain this platform," said Ed Fuhr, V.P. of Power Solutions for Crane Aerospace and Electronics.

These high-voltage modules are designed to drive multiple traveling wave tubes for jamming oncoming missile threats. The production is scheduled to begin January 2011 in Fort Walton Beach, Florida and is expected to be completed by June 2013.

(continued on Page 52)



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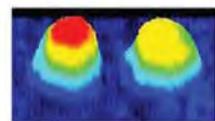
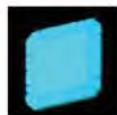
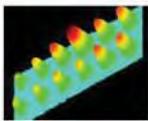
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# Cleaning: The Forgotten Challenge

## New Cleaning Technology Solutions for Lead-free Micro-Bumping Processes

By Kimberly D. Pollard, Allison Rector, Nichelle Wheeler [Dynaloy LLC]

For years, the semiconductor industry has followed a path of increasing performance by decreasing feature size and improving the cost per performance unit. This ultimately has led to the adoption of copper wires and chemical mechanical planarization (CMP), as well as replacing  $\text{SiO}_2$  with low- $k$  dielectric materials to improve performance and lower power loss at the interconnect level. Although the work continues, it is reaching natural limits, such as the cross-section of copper required to have sufficient conductivity even when coupled with ultra-low dielectric materials. Being at or near those limits for copper, the obligation is to provide more effective dielectric materials—with a dielectric constant approaching that of air ( $\epsilon=1$ ). This situation is very challenging and costly. With the industry aggressively calling for reduced energy consumption with smaller form factors, it's time to consider alternative approaches. One approach that has garnered a lot of attention is to re-engineer wafer level packaging (WLP) and develop processes for manufacturing stacked and vertically interconnected chips, connected by silicon or glass interposers. The goals are to improve density, reduce interconnect length and therefore transmission length, and thus reduce power consumption. This also leads to improved thermal management. The ultimate goal is to generate smaller, thinner, and more efficient mobile personal electronics and reduced power for server farms and data storage facilities.

Many traditional WLPs are simultaneously being combined with 3D technologies, providing a host of possible packaging schemes to meet a variety of final product needs and integration schemes. This has created opportunities for technology development in areas such as test procedures, materials sets, and processes.<sup>1</sup> This paper focuses on one of those

opportunities: lead-free compatible resist and post-etch residue cleaning solutions for high-density solder bumping, called microbumping ( $\mu$ -bumping).

In the world of 150 $\mu\text{m}$  pitch solder bumping, the introduction of RoHS rules for lead-free solder bump compositions (SnAg, SnAgCu) proceeded in the absence of an integrated process capable of defect-free surface preparation. It was relatively simple for solder bump compositions in many devices to be converted to lead-free alloys. However, new challenges have appeared in higher volume fabrication of SnAg micro-pillars ( $\mu$ -pillars) or copper, (Cu)  $\mu$ -pillars with lead-free solder caps as the bump pitch approaches 25 $\mu\text{m}$  with aspect ratios of 1:1 or 1.5:1. Individual processes involved in the total integration—including electroplating, thick photoresist application, thick photoresist removal, associated descum processes, and Cu seed metal etch step—have been challenged to meet the demands. New geometries, higher aspect ratios, and very dense solder bump arrays have created further challenges, stretching

the older 150 $\mu\text{m}$  technology beyond its capability. This article identifies a reliable route to defect-free Cu  $\mu$ -pillars with lead-free caps and lead-free solder plated  $\mu$ -bumps after photoresist removal in applications compatible with advanced packaging schemes and with improved yields and reliability.

One of the “most prevalent and most critical of all semiconductor manufacturing process steps is wafer cleaning. It has evolved to the point where not only most cleans must be specifically tailored to the preceding or subsequent fabrication steps, but to a level of sophistication that is better labeled as surface preparation or surface engineering”.

Previously, a problem commonly referred to as “white ring” in lead-free electroplating bumping applications was reported.<sup>3</sup> It is seen as a white residue on the Cu seed metal after photoresist removal and has been identified as a mixture of tin oxides.<sup>3</sup> Many process and chemistry-related variables have been linked to the creation of the residue, including electroplating solution metal

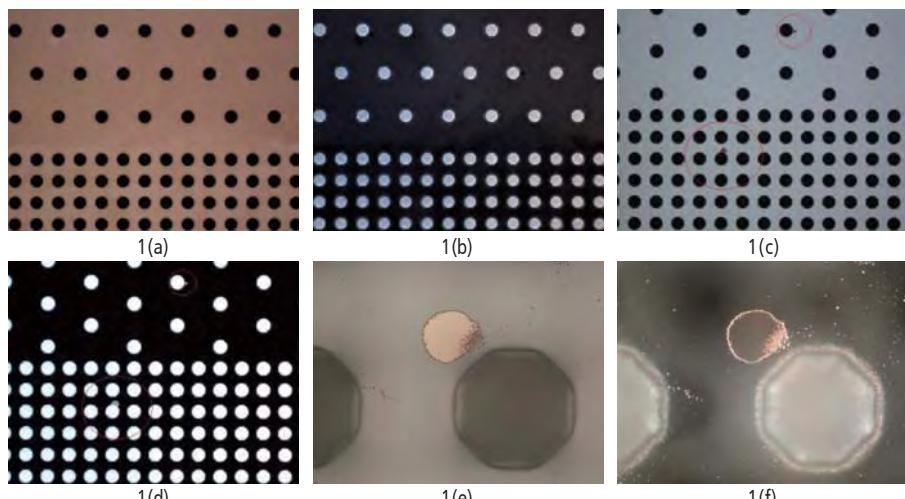


Figure 1. (a) Optical image: lead-free electroplated solder bumped wafer surface after cleaning showing complete photoresist removal, 50 x; (b) Corresponding dark field image, 50 x magnification; (c) Optical image: lead-free electroplated solder bumped wafer after Cu seed metal etch but before TiN etch, showing residual copper on the wafer surface; 50 x (d) dark field image of image in (c), 500 x; (e) optical image: copper residue defect; 500 x, (f) dark field image of image in (e), 500 x.

ion concentrations, electroplating current densities, photoresist processing conditions, photoresist removal, rinse steps for each process, pre-plating surface activation processes and post strip descum or back sputtering processes.

As solder bump pitches have decreased and solder bump aspect ratios have increased in both lead-free bump or Cu pillar, lead-free cap applications, this defect is more prevalent, but also more difficult to characterize. Although the general process flow has stayed approximately constant, many solutions for individual process steps have changed, substantially changing the outcome of the integration of those steps. For bump pitches in the range of 20 - 80 $\mu\text{m}$ , the wafer is free of photoresist after removal, and the Cu seed metal has a shiny non-oxidized appearance. However, despite the good visual appearance after the subsequent seed metal etch step, there still may be a yield-reducing defect found. It manifests itself as Cu residue left on the field after the seed metal etch step. The residue is randomly located and typically most prevalent in high-density solder areas.

To study the causes of Cu residue remaining on the wafer surface after the seed metal etch step, it is necessary to first characterize the residue. **Figure 1** shows optical images of the wafer surface after photoresist removal. The wafer is photoresist-free and the Cu field metal appears clean. Images of the wafer surface after seed metal etch are shown in **Figures 1c - f**. They highlight the random defect that is found occasionally when wafers like those imaged in **Figures 1a** and **1b** undergo Cu seed metal etch. The images show Cu residue remaining on the wafer surface, even though > 99% of the surrounding seed Cu has been cleared. The residual Cu after etch appears shiny and has been inhibited from etching. The Cu masking agent in the etch is optically transparent.

Due to the random nature of the residue and the increased probability that it will occur in bump areas with tighter pitches, several techniques were used to understand it. Given previous experience finding oxidized tin ( $\text{SnO}_x$ ) on the Cu surface, and the large volume of literature that discusses exchange reactions between Sn

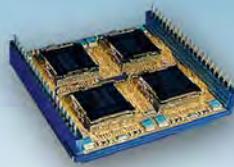
and Cu to form Sn metal films on Cu metal films, the hypothesis was that a thin layer of Sn was depositing on the Cu surface, inhibiting the etch process. Initially, energy dispersive analysis using X-rays (EDAX) was used for characterization. However, due to the depth of penetration into the surface and the thin residue, it was not possible to determine the residue composition.<sup>4</sup>

X-ray photoelectron spectroscopy (XPS) was the technique used next to

examine the surface, (see **Figure 2**). XPS collects oxidation state information from region scans of the elements in the sample. However, due to the close proximity of the bumps in the high density pattern area and the relatively large spot size of XPS, the tin found and shown in the spectrum could be due, at least in part, to contributions from tin in the solder bump.

To circumnavigate the spot size issue but remain surface sensitive, Auger Spectroscopy was used. A sample that had

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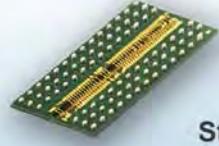
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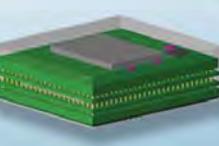
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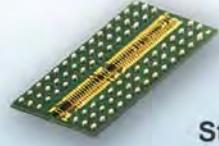
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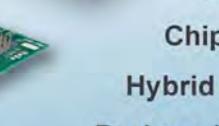
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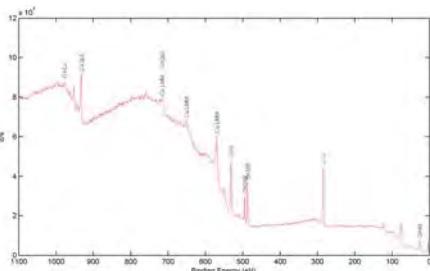


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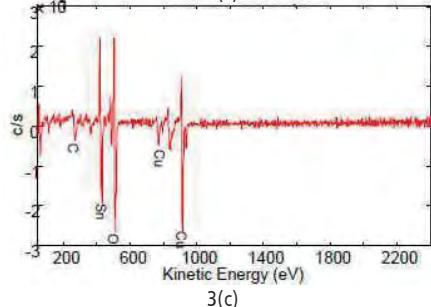
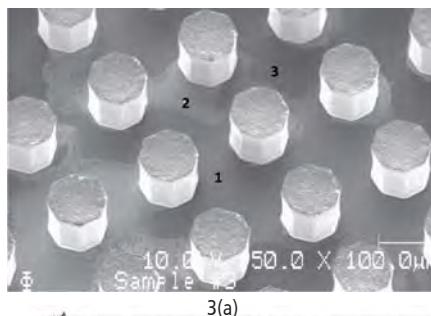


**Figure 2.** XPS survey spectrum of the Cu seed metal after photoresist removal and before seed metal etch. Sn is present, but with the tight pitch in the sample geometry, it was not possible to determine if it was from the solder bump or from Sn on the Cu surface.

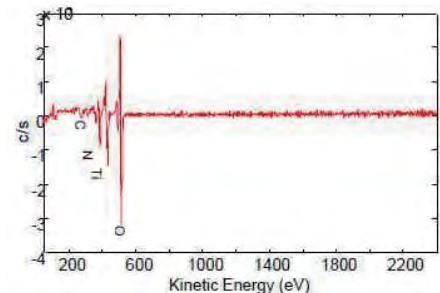
Cu residue after the Cu seed metal etch step was analyzed and results are shown in **Figure 3**. The Auger spectra are considered semi-quantitative. Although Auger spectroscopy can determine atomic concentrations, in this case it is more challenging due to peak overlap between the N and the primary Ti peak, with further complication when the layer is partially oxidized.

Three areas with distinctly different appearances in the same small area were examined (labeled (1), (2), and (3) in **Figure 3a**). Spot 1 has a hazy appearance; Spot 2 is a typical Cu containing residue; and Spot 3 has a dark colored surface. Auger survey scans indicate that Spot 1 contains titanium, (Ti), nitrogen, (N), and oxygen, (O). Since adventitious carbon, (C) is always found in analyses using high vacuum techniques, the C in the spectrum may not be present in the sample. It is probable that the spectrum is due to TiN, oxidized due to exposure with the atmosphere when the Cu was etched. Compositional analysis at Spot 2 indicates that the defect on the wafer surface that is inhibiting the Cu etch process is a Sn-containing film. Interestingly, Spot 3, although it has a very different appearance, is composed of Ti, N, and O, in only slightly different proportions than the analysis at Spot 1.

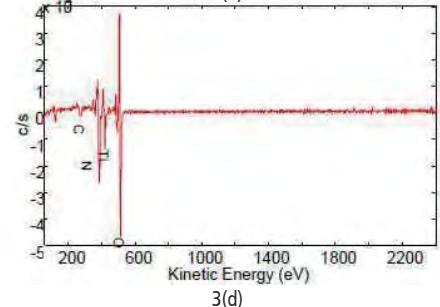
To estimate the thickness of the defect, the sample was sputtered with Ar to remove 50Å of film. The spectra in **Figure 4** for the same 3 points shown in **Figure 3a**, show that for Spots 1 and 3, the ratios of Ti:O and N:O increase, leading to the expected conclusion that the oxygen is incorporated due to exposure to the environment and is not part of the as-deposited TiN film. For



**3(a)**



**3(b)**



**3(c)**

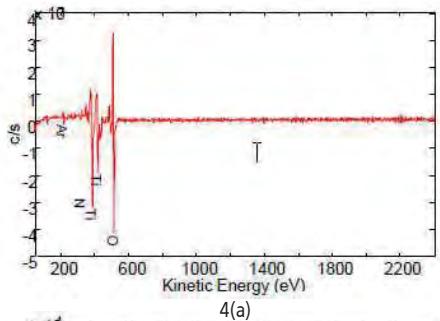
**3(d)**

**Figure 3.** (a) Scanning electron micrograph indicating the analysis points; (b) Auger survey spectrum for Spot (1) showing oxidized TiN; (c) Auger spectrum for Spot (2) showing the presence of Sn as the mask during Cu seed metal etch; (d) Auger spectrum for Spot (3), indicating oxidized TiN on the surface which is visually different from Spot (1).

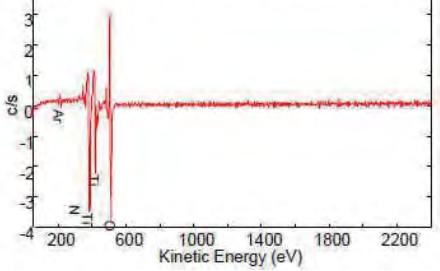
Spot 2, the spectrum shows that the relative amount of Sn on the surface appears to have decreased, suggesting that it is located on top of the Cu. This result is consistent with the observation that Sn is blocking the etch process. In this case the film is greater than 50Å thick. However, in other testing, the film thickness that can create the Cu defect has been 20 - 400Å. The Auger results do not clarify the oxidation state or coordination sphere of the Sn. Oxygen is present in the spectra, but how much is tin oxide and how much is oxidized titanium nitride is unknown.

The location of the often-transparent defect after seed metal etch was mapped to the same surface after photoresist removal, rinse, and dry, using shortened

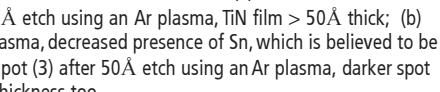
etch times to exaggerate the effect. The results for a two minute etch and a five minute etch in a dilute H<sub>3</sub>PO<sub>4</sub>-based etchant are shown in **Figure 5**. It is possible to map the surface appearance after photoresist removal to a defect if a short etch time is used, as shown in **Figure 5a** and **b**. By five minutes of etch time, the areas with the appearance of



**4(a)**



**4(b)**



**4(c)**

**Figure 4.** (a) Auger survey spectrum for Spot (1) after 50Å etch using an Ar plasma, TiN film > 50Å thick; (b) Auger spectrum for Spot (2) after 50Å etch using an Ar plasma, decreased presence of Sn, which is believed to be the mask in the Cu etch process; (c) Auger spectrum for Spot (3) after 50Å etch using an Ar plasma, darker spot of TiN > 50Å thickness too.

blemishes after photoresist removal have been completely cleared of Cu, as shown in **Figures 5c** and **d**. Since the appearance of the surface does not always predict defects, the cause of the defects is considered transparent.

When the randomly placed and transparent film that caused the residual Cu defect after the seed metal etch process was determined to contain Sn, many theories about the sources of Sn, as well as the mechanisms for deposition, were considered. Individual processes involved in building the solder bumped wafer include the electroplating process, thick photoresist application, photoresist removal, specialized rinse processes, descum or back-sputter processes, and Cu seed metal etch steps. Although photoresist removal is first suspected to cause the Sn defect, none of these processes have been left unaffected, as each may contribute to the availability of the Sn ion in solution for deposition onto the wafer surface. For example, wafers prepared at the same facility using the same resist and processing conditions, were split into two groups: one went into electroplating tool A, which held the wafers horizontally and contained an electroplating solution with higher Sn ion content; the second went into electroplating tool B, which held the wafers vertically and used an electroplating solution with lower Sn ion content. Multiple wafer pieces from multiple wafers were tested. In each case, the wafers from the second group that had gone into the electroplating tool using the electroplating solution with lower tin ion concentration had significantly fewer defects after cleaning and seed metal etch. Examples of typical differences in the outcome are shown in optical images in **Figure 6**.

Other variables such as the photoresist used, how it is processed, and the solder bump pitch on the wafer design can contribute to the ions available in solution for deposition onto the Cu.

Many variables in the photoresist removal process have also been attributed to affecting the mechanism for deposition of Sn on the Cu seed metal. For example, the temperature of the removal bath can give the solution enough energy to cause  $\text{SnO}_x$  to deposit on the Cu during the

process. The choice of rinse solvent has a large impact on the deposition of Sn/ $\text{SnO}_x$  on the Cu surface. It is known that use of water as a rinse solvent will increase the defect count, while the use of isopropyl alcohol (IPA) may decrease the defect count (**Figure 7**).

Since the defect is randomly and sporadically placed on the wafer surface,

testing carried out to determine the variables that most strongly affect the deposition of Sn must be repeated multiple times using multiple wafers to ensure that the results are the same for each sample and not just tested on an area of a wafer where the problem did not exist. Multiple tests with careful inspection have demonstrated that Sn

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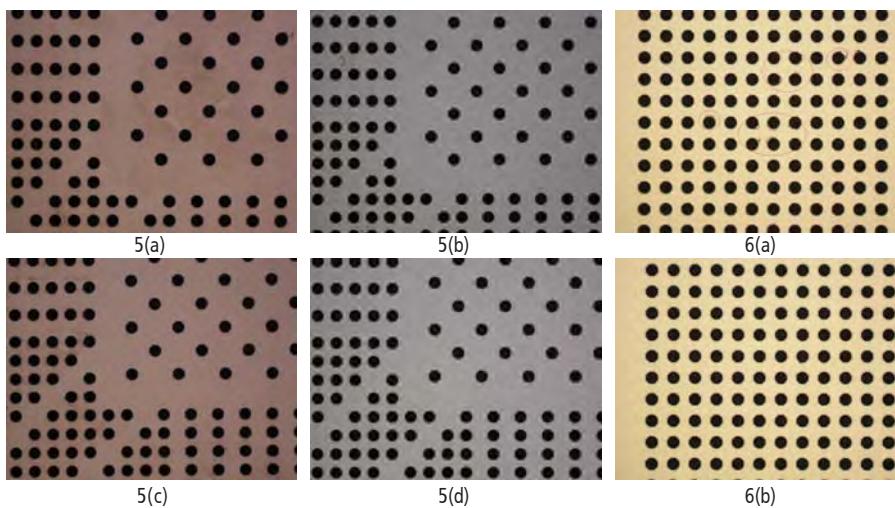
  
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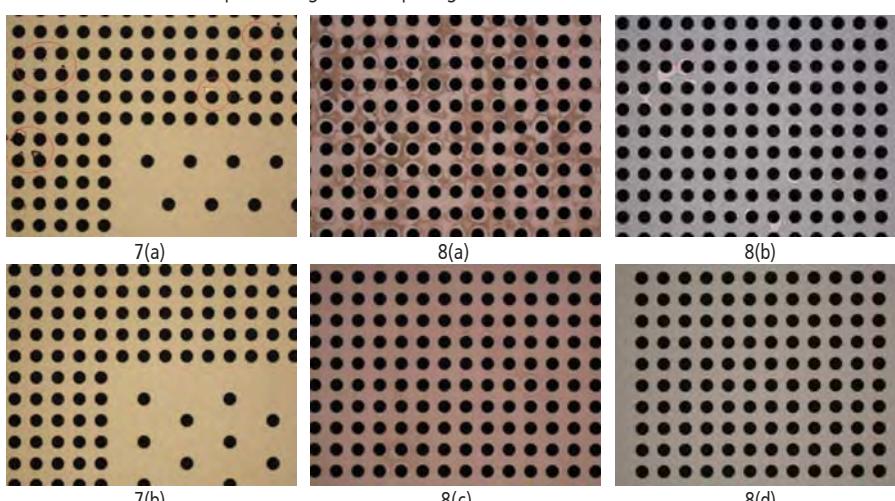
  
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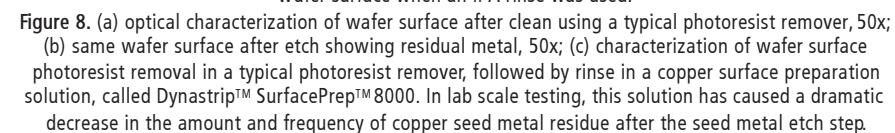
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**Figure 5.** (a) Optical image after clean, before seed metal etch, 50x; (b) Optical image, after 2 min seed metal etch, 50 x; (c) Optical image after clean, before seed metal etch, 50x; (d) Optical image, after 5 min. seed metal etch, 50x.



**Figure 6.** (a) Optical image of typical wafer surface after seed metal etch; (a) wafer electroplated in a horizontal electroplater using an electroplating solution with higher Sn ion content; (b) wafer electroplated in a vertical electroplater using an electroplating solution with lower Sn ion content.



**Figure 7.** (a) post-etch image of wafer surface when a water-based rinse w as used; (b) post-etch image of wafer surface when an IPA rinse was used.

**Figure 8.** (a) optical characterization of wafer surface after clean using a typical photoresist remover, 50x; (b) same wafer surface after etch showing residual metal, 50x; (c) characterization of wafer surface photoresist removal in a typical photoresist remover, followed by rinse in a copper surface preparation solution, called Dynastrip™ SurfacePrep™ 8000. In lab scale testing, this solution has caused a dramatic decrease in the amount and frequency of copper seed metal residue after the seed metal etch step.

must be removed from the surface of the seed Cu for a manufacturing process to be reliable. Since control of the defect and studies of its causes have not been straight forward and easily attributed or quantified, a solution for removing the Sn or  $\text{SnO}_x$  from the Cu surface was necessary.

There are many ways to approach the problem, including adding one or multiple descum or back-sputtering steps to remove any Cu surface contamination. However, due to efforts to continue cost-of-ownership reductions, the most preferable option is to remove the Sn

from the Cu surface as part of the post photoresist-removal rinse. Formulations to provide an engineered solution compatible with solvent-based photoresist removers, yet able to target Sn removal from the Cu surface and prepare it for the subsequent etch process, were developed. The solution was integrated into existing processes and has the added benefit of removing the Sn from the Cu seed metal immediately before even more difficult-to-remove intermetallics are formed. An intermetallic forms when the plating and the underplating (or substrate) inter-

diffuse. The materials mix and react chemically to form new compounds such as  $\text{Cu}_3\text{Sn}$  and  $\text{Cu}_6\text{Sn}_5$  for a Sn-Cu interface.<sup>5</sup> **Figure 8** illustrates the results of cleaning with and without the use of the specialized rinse solution.

## Conclusion

This paper has characterized the cause of a common defect in lead-free electroplated solder formation — residual Cu after the seed metal etch step in lead-free electroplated  $\mu$ -bumping applications. An approach that considers the surface preparation of the Cu seed metal after photoresist removal has been shown to eliminate the defect and improve the post seed metal etch result. Bench scale testing using a compatible post photoresist removal surface preparation solution in place of water or IPA has shown dramatic improvements. Currently the solution is undergoing large scale qualifications.

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# Cost Comparison for Flip Chip, Wire Bond, and Wafer Level Packaging

By Chet Palesko [SavanSys Solutions LLC] and E. Jan Vardaman [Techsearch International, Inc.]

**A**s semiconductor features sizes continue to shrink, the cost of packaging these leading-edge chips is a much greater percentage of the total system cost. It is critical that the designer choose the most cost-effective package for their application, or they risk delivering a non-competitive product. This decision is even more complex due to the variety of choices. This article compares the packaging costs of wire bond, flip chip, fan-in wafer level packaging (FI WLP), and fan-out wafer level packaging (FO WLP) using an activity based cost model of each technology. The scope of the cost models includes fabrication and assembly of the package, and the combination of characteristics that lead to the most cost-effective package for each technology is presented.

## Activity-Based Cost Modeling

Activity-based and parametric are the two dominant cost modeling methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model that matches as closely as possible. This “black box” approach, as an extrapolation based on historical data, is only appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities.

For reliable and dynamic trade-offs, activity-based cost modeling is the most accurate method because individual activities are characterized and analyzed. The total cost of any manufacturing process is calculated by dividing the process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity — both consumable and permanent material
- Any tooling cost

- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

Activity-based cost modeling is also well suited to comparing different technologies and manufacturing processes. The total cost of a product can be divided into direct manufacturing cost, allocated factory overhead, and profit margin.

The direct manufacturing cost is easy to quantify and reasonably consistent across the industry. However, factory overhead and profit margin vary significantly between different manufacturing sites and companies. By using activity based cost modeling, the specific differences in manufacturing cost can be determined by comparing the direct manufacturing costs. This “relative” cost modeling makes it much easier to understand the cost impacts — good or bad — of design decisions and technology tradeoffs.

The graph in **Figure 1** shows an example of an activity based cost graph for a wire bond substrate. Each activity contributes cost in at least one of the six categories shown. These categories are represented by the colored bars, and the running total is the line on the graph.

## Wire Bond Packaging

Wire bond packaging is a mature technology used to package billions of components. Given this maturity, manufacturing efficiency and yields are both quite high.

One of the primary purposes of any package is to convert the semiconductor I/O pad width and spacing into printed circuit board I/O pad width and spacing. Because the design rules are different, this conversion may be costly. For wire bond packaging, the conversion is done during the wire bonding process, which is relatively low-cost. The fine-pitch die I/O pads are connected to the substrate fingers at a larger pitch. This “spreads out” the I/Os and makes it easy to connect them from the substrate fingers through the substrate to the PCB. Consequently, wire bond substrates are simple and inexpensive to build since the wire bonding activity is spreading the I/Os, rather than requiring the substrate to handle fine-pitch semiconductor design rules. A two- or four-layer substrate with no high-density interconnect is usually adequate for most wire bond packages.

One of the current cost disadvantages of wire bonding is the cost of gold wire.

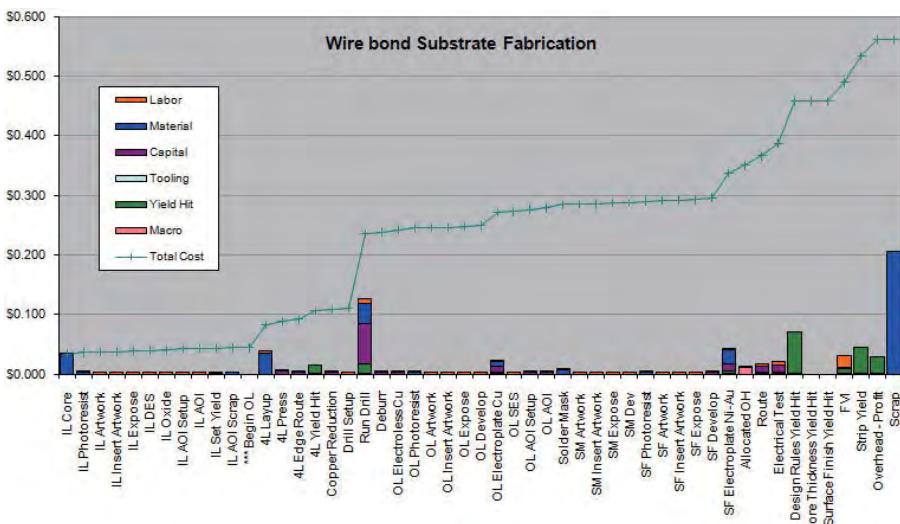


Figure 1. Sample activity-based cost results.

Using copper wire as an alternative to gold has become quite popular. However, today's assembly yield is lower and the wire bonding time is longer due to the stiffness of the copper wire. But even with the additional wire bonding time and slightly lower yields, copper wire bonding is usually less expensive than gold wire bonding with the price of gold at more than \$1,300 per ounce.

Wire bond packaging is generally the most cost-effective technology if a large package can be used relative to the I/O count and size of the die. Copper wire is the best choice, but in most cases, gold wire is also cost-effective.

## Flip Chip Packaging

Flip chip packaging using an area array solder bump or copper pillar configuration is rapidly becoming a popular alternative to wire bond packaging. This trend is largely due to thermal and electrical properties, declining cost, the ability to support high I/O count packages, and the ability to support smaller packages relative to the die size. As shown in **Figure 2**, the connection area required for flip chip is much smaller than that required for wire bonding because all the I/Os from the chip are connected through its bottom. Smaller packages in relation to die size can be achieved.

However, this smaller area comes at a cost. The two major cost drivers for flip chip packaging are both directly related to the act of bringing I/Os out under the die. The first major cost driver is wafer bumping. Die pads are designed in an area array format and the wafer is bumped for connection to the substrate. This bumping may be solder bumps or copper pillar, but either technology is a significant cost driver. The second major cost driver is the substrate. This high cost results from a combination

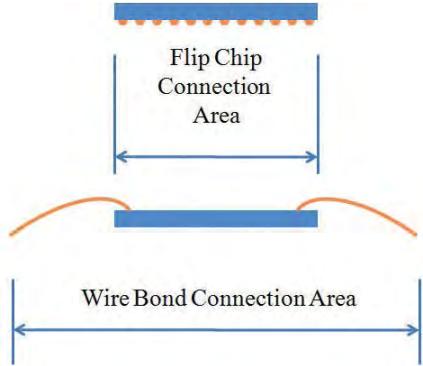


Figure 2. Wire bond vs. flip chip interconnection area.

of the high connection density, fine pitch design rules, and the fact that a significant number of build-up layers for escape routing are required to connect to the die.

Flip chip packaging is generally the most cost effective solution for high I/O count packages with a large die and size constraints. High I/O count packages are difficult and expensive for wire bonding, particularly if the package must be close to the same size as the die.

## Wafer Level Packaging

Traditional WLP is sometimes referred to as FI WLP. Once the semiconductor wafer is fabricated, the additional processing to complete WLP is straightforward and easily accomplished in the same factory. Therefore, WLP is usually a single manufacturing process that begins with a wafer and ends with a "ready-to-ship" packaged chip. In contrast, a chip packaged with wire bond or flip chip technology requires three different manufacturing processes: fabrication of the semiconductor, fabrication of the package substrate, and assembly of the die on the substrate. These processes are distinct and not suitable for completion in one factory.

In addition to the straight forward manufacturing process for FI WLP, another major advantage is package size. Since the package is fabricated directly on the wafer, the package and the die must be the same

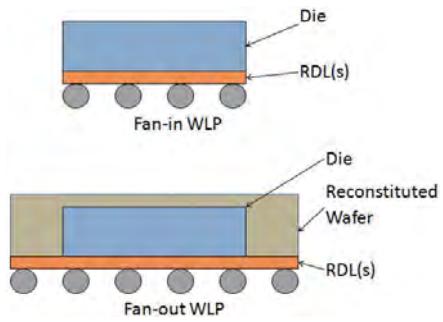


Figure 3. FO WLP compared to FI WLP.

size after singulation.

However, FI WLP presents a substantial disadvantage for any application requiring even a moderate number of I/Os. As discussed previously, one of the major roles of any semiconductor package is to convert the semiconductor I/O design rules into printed circuit board I/O design rules. Since the PCB I/O design rules are much looser than those for the semiconductor, the number of I/Os possible from the package is quite low compared to the number of I/Os possible from the die. Increasing the I/O count by growing the die or using fine pitch PCB design rules can significantly increase the cost.

One way to capture the benefits of WLP and overcome that I/O restriction is to use a FO WLP approach. Instead of directly fabricating the package on the semiconductor wafer, the wafer is diced and the individual dies are placed in a different substrate before the wafer level packaging steps are performed. This allows the FO WLP to be

## Package Cost Comparisons

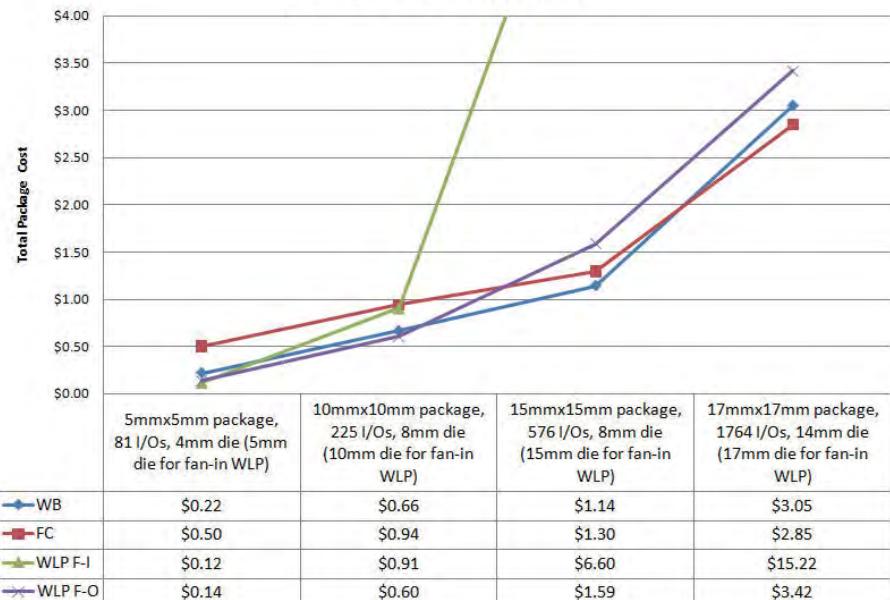


Figure 4. Package cost comparison.

larger than the die and therefore support a higher number of I/Os. The diagram in **Figure 3** shows the expanded I/O capacity of an FO WLP.

WLP and flip chip packaging are both good solutions for miniaturization. The advantages with WLP are that no wafer bumping is required, and it is much simpler to fabricate the package to match the semiconductor design rules of the die. The disadvantage is limited package size and I/O count (even with fan-out) due to the fact that a semiconductor process is used for everything. Large, high I/O count packages are more cost efficient if built using a 20x24" (approx. 508 x 610mm) PCB panel rather than a 200mm or 300mm round wafer.

#### Package Cost Comparisons

**Figure 4** shows the cost model results for wire bond, flip chip, FI WLP, and FO WLP for four different designs. Activity-based cost models were used for all four technologies and the manufacturing location is assumed to be Taiwan. A die size smaller than the package was used for FO WLP, wire bond , and flip chip packaging and a die size identical to the package size was used for FI WLP.

The 5mm x 5mm package with 81 I/Os is an ideal application for a FI WLP given the small die size and I/O count. However, as the package size is increased to 10mm x 10mm, the FI WLP option increases significantly in cost. This is primarily due to the cumulative yield loss of the semiconductor processes and the packaging processes. However, both FO WLP and wire bond packaging are cost effective since the die is diced and tested before packaging.

For the two large package examples, FI WLP is not a good option. Wire bond or flip chip packaging are the most cost effective choices for these packages. Wire bond packaging is a good option for the 15mm x 15mm package since the die size is only 8mm x 8mm and there is a lot of room for wire bonding. The 17mm x 17mm option is well suited for flip chip packaging given the high I/O count and large die size.

#### Summary and Conclusions

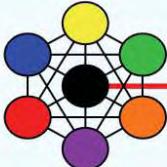
Based on the technology cost modeling analysis and cost drivers presented in this paper, we can draw the following general conclusions.

WLP — particularly FI WLP if the I/O count is small enough— can be the most cost-effective packaging solution for small packages, and should be considered as an option for packages up to approximately 10mm x 10mm.

Wire bond packaging is usually the most cost-effective solution for large packages if the I/O count is reasonable. It is extremely cost effective, but a substantial area is required for the wire bonding. Therefore

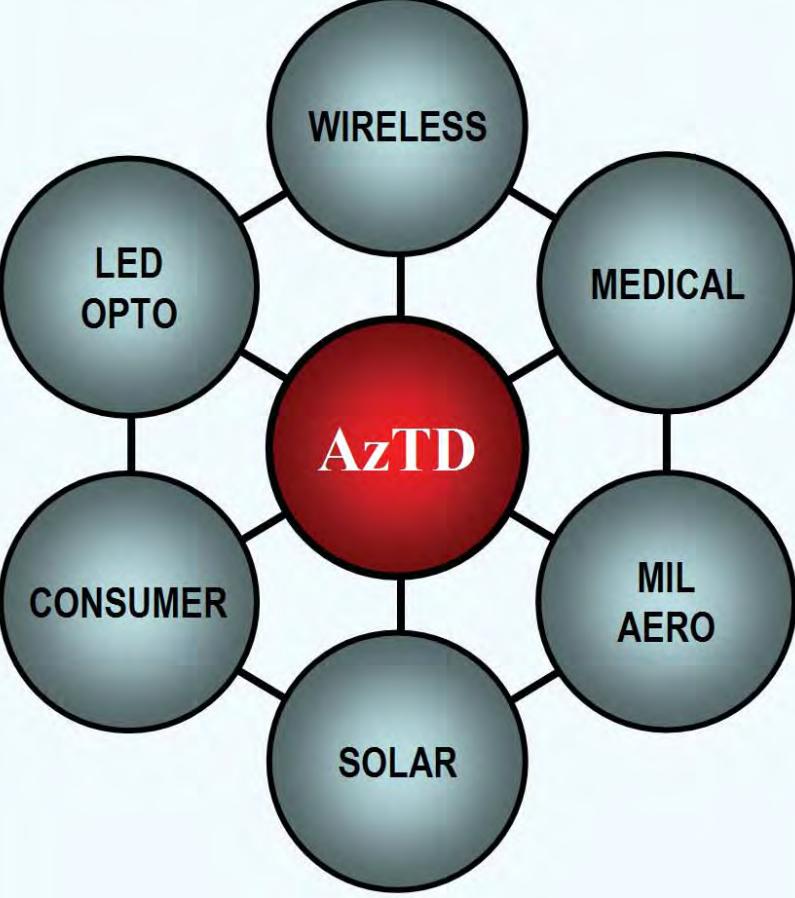
the number of I/Os must not be too large or there will not be enough room between the die and the edge of the package for the wire bonding.

Flip chip packaging is well suited for packages with high I/O counts and large dies. Wire bond connections are made one at a time and are done in many cases with expensive gold wire. However, all the I/Os from a flip chip die are made simultaneously when the die is bonded to the substrate. <sup>8</sup>



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# Copper Bond Testing Challenges

## A New Test Protocol Offers a Unique Industry Solution

By Kamran Iqbal [Nordson DAGE]

**C**opper has been under investigation as an alternative for gold interconnects for several years and is now one of the preferred materials for semiconductor and microelectronics. Copper's physical properties enable it to be used at smaller geometries providing similar performance to gold without the high material cost, which is one of the main driving factors behind this migration. Increasingly, copper is used for stud bumps, pillars, and also ball bonds. Larger geometry copper is also starting to replace aluminum interconnects for high-performance applications.

Testing the mechanical integrity of these interconnect bonds is an important part of manufacturing quality assurance and ultimately ensures product longevity. A common test method for interconnect bonds has been shear testing, where the bond is sheared off the bond pad. This is regarded a very accurate and reliable test to establish bond integrity. Another test method that can be introduced is tensile loading. In the case of copper bonding, this can be more representative of the loads to which the bonds would be subjected. This has not been a feasible option with gold, due to the high compliance of gold bonds, making it very difficult to grip and apply a given load successfully. A challenge of shear testing, which is becoming increasingly common as packages continue to shrink and contain complicated

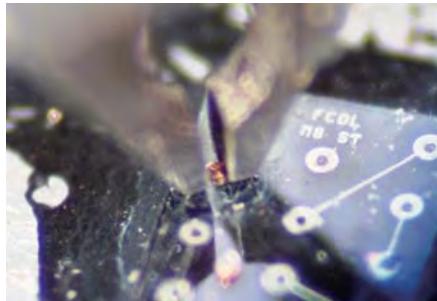


Figure 1. View of First Bond Ball Pull jaw closing over the copper ball bond prior to the pull testing taking place.

interconnect bond arrangements, is testing of densely populated packages, where the geometrical constraints can prevent successful shear testing (**Figure 1**).

### Material Differences

Copper has many physical advantages over gold for wire bonding including:

- Far superior electrical and thermal conductivity, opening up applications which were previously limited by the physical characteristics of gold.
- Better long term reliability due to less intermetallic growths allowing longer shelf life as well as longer operating life of products.
- Mechanically stiffer than gold, which is ideal for creating wire bond loops. With the growing complexity of device packages, copper wire is an ideal medium with which to manufacture more complex wire bond arrangements.

Although there are many advantages over gold, there are some disadvantages to the migration towards copper wire bonding:

- The bonding parameters must be kept under tight control, leading to more complex wire bonding machinery.
- An inert gas is required to reduce oxidation during ball formation. Poorly controlled environments would lead to oxidation and would render it unsuitable for bonding.
- There is lower bond strength in the second bond or stitch bond; this is due to oxidation in the copper.
- The mechanical hardness of copper wire generally requires higher heat, pressure, and ultrasonic energy to soften the ball, but this also softens the bond pad metallisation which can become inconsistent.
- The overall mechanical hardness of copper compared to gold leads to higher risk of cratering.

Although there are disadvantages in the shift from gold to copper wire bonding, a well-controlled wire bonding environment and strict controls of the bonding parameters limits these disadvantages, which are outweighed by the features and benefits copper presents, opening up a range of possible applications that were previously challenging with gold as an interconnect medium (**Figure 2**).

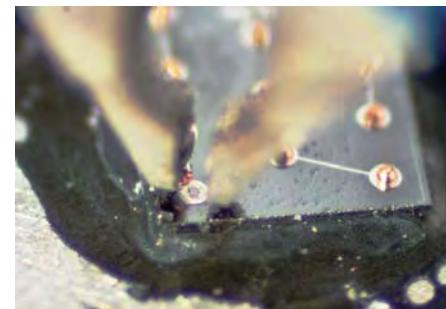


Figure 2. The First Bond Ball Pull jaw after the test.

With the migration towards copper as an interconnect medium, many challenges are highlighted for traditional bond test techniques.

### First Bond Ball Pull Test Protocol

The tough material nature of copper is an advantage for bond test techniques, as it can be gripped mechanically without the high risk of damaging the bond compared to a gold bond. A challenge is posed when trying to grip the bond successfully, with accurate and consistent pressure. Controlling the tool clamping pressure on a copper bond is important, as too much pressure could deform or break the jaw tool. This was not a major issue with more compliant materials such as gold, which reformed during clamping, posing less risk to the jaw tool. Any deformation in the jaw tool can lead to degraded and unreliable results. Too little pressure will lead to tool slippage potentially damaging both the tool as well rendering the results void (**Figure 3**).

The superior electrical and physical properties of copper compared to gold

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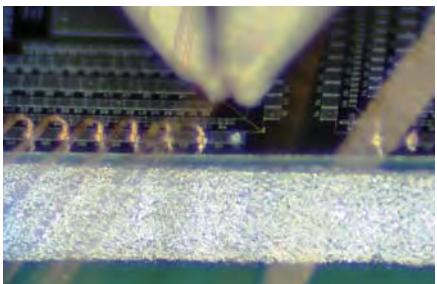


Figure 3. FBBP test complete with jaw at top of travel.

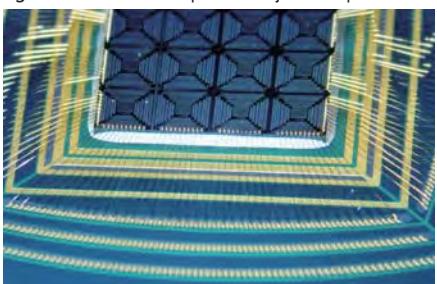


Figure 4. 25 micron copper wire bonding.

means that the wire bond geometries can be decreased. This decrease in size equates to an increase in bond density, finer pitch devices and more complex wire bond arrangements. The challenge this trend poses is successful positioning, alignment, and inspection techniques for bond test machines (**Figure 4**).

With the decreasing size of bonds, tooling techniques are of very high importance. The correct tooling technique, with correct material selection aids successful bond gripping as well as easier alignment in more densely populated test samples.

In anticipation of this shift in material choice, an advanced multipurpose bondtester<sup>1</sup> that caters to copper interconnect bond testing such as copper ball bond pull now exists and offers a novel industry unique solution. This system, coupled with the newly developed software<sup>2</sup> enables successful testing of copper interconnects providing unsurpassed accuracy and repeatability.

The new bond testing system enables software control of air pressure, allowing accurate gripping of the bond under test as well as spreading the load with selected clamp pressure. This consistent pressure is maintained during a FBBP test providing reliable clamp pressure in order not to deform the bond or let it slip during a test.

The system also provides high resolution control allowing the test specimen to be positioned accurately to

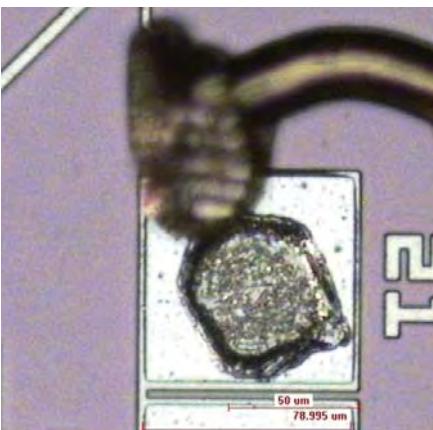


Figure 5. Bonding pad after FBBP test.

within microns. This makes it easier to test fine-pitch devices such as copper bonded interconnects. The bond testing system also provides advanced visual inspection via numerous options such as high magnification microscopes, imaging cameras or borescope, allowing detailed views of the test specimen (**Figure 5**).

Also developed is an ultra small geometry capability enabling the high precision testing of a range of interconnects such as copper ball bonds, studs, bumps and pillars. This advanced bond testing capability is further complimented with customized solutions such as user specified load tools.

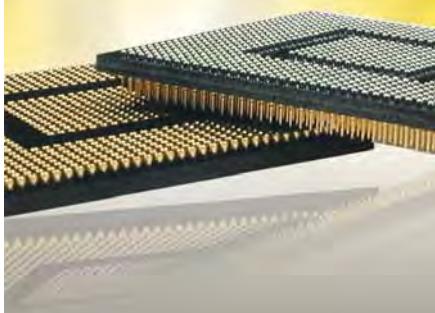
## Conclusion

The migration to copper from gold as an interconnect medium is set to continue with copper becoming one of the main materials of choice. With this anticipated trend, device manufacturers, test houses as well as research institutes need to be prepared with the appropriate equipment in order to fulfill challenging test requirements of this new shift in material choice. The FBBP test protocol in combination with an advanced multipurpose bondtester provides a complete solution to meet this industry demand.<sup>3</sup>

## References

1. 4000Plus. From Nordson DAGE
2. Paragon<sup>TM</sup>

Kamran Iqbal, B. Eng (Hons), M.S.c., Senior Applications Engineer, Nordson DAGE, may be contacted at [kamran.iqbal@nordsonnage.com](mailto:kamran.iqbal@nordsonnage.com). Tel: 011-44-1296-317800.



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# HDI Solution for Very Fine Pitch Flip-Chip Applications

By Vern Solberg [Tessera]

**A**lthough flip-chip assembly is widely accepted in the industry for a broad number of applications, the higher I/O and extremely fine-pitch contact spacing required for newer high-end processor semiconductors have increased assembly process yield challenges. A key concern is how to ensure consistent die-to-substrate interface; a critical barrier in achieving optimum assembly process yield. Historically, the perimeter bumped flip-chip process has served as the main interconnect method in direct-die flip-chip attachment. However, current generations of high density sub-micron wafer fabrication processes are enabling more functionality within the confines of a relatively small die. The smaller die outline forces the semiconductor company to further reduce wire-bond pitch, and it is not uncommon for these higher pin count die elements to be furnished with perimeter-located wire-bond site spacing less than 100 $\mu\text{m}$ .

## Contact Redistribution

To overcome flip-chip mounting and circuit routing difficulties, companies are relying more on contact redistribution. The redistribution process is performed while the semiconductor remains in the wafer level format and is quite complex. The wafer is prepared using a surface metallization process. A photo-imageable film is then applied and developed to define the circuit pattern for subsequent copper plating processes. When the plating is complete, the copper conductors connect the perimeter wire-bond features to the newly defined contact sites on the die face (typically arranged in a column and row configured array). After chemically etching away the remaining base metallization, the copper conductors are coated with a photo-imaged resist material. Only the array contact sites are left free of the resist coating to enable solder bumping or solder ball attachment. In regard to the solder bumping process, deposition of solder

paste at the die contact sites is a common practice, but the process is plagued with control variables. For example, the solder paste material, whether deposited or printed onto the wafer, comprises both solid alloy particles and flux. The ratio of solids to flux can vary somewhat, causing slight differences in the solder bump height when reflowed. Electroplating solder alloy on the contact sites offers significantly tighter tolerance control; however, electroplating is a slower process than printing and the plating thickness may not be uniform on all areas of the wafer. As a result, when reflowed to form the bump profile, the bump height can vary by several microns from one die to another.

Although the solder bumping process on the wafer is fairly uniform, precise control of the planarity (common height) of all contact features is not possible. Due to these surface irregularities and planarity issues, a reliable, defect free soldering process remains a viable challenge. The concern is the uneven profile height of solder bumped contact features. An non-uniform bump profile can compromise the integrity of solder interface between the die and substrate. This issue has become even more of a concern for larger die elements having several thousand contacts. Some companies have resorted to a more complex (and rather lengthy) proprietary wafer-level plating process that actually furnishes a raised solid copper post features at each contact site. Although the additive copper plating thickness will not be perfectly uniform across the wafers surface, the Cu post can be made planer by mechanical leveling. Examples for three common flip-chip contact variations noted are compared in **Figure 1**.

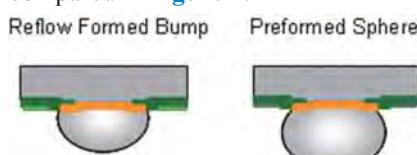


Figure 1. Comparing wafer level applied contact features developed for flip-chip die attachment.

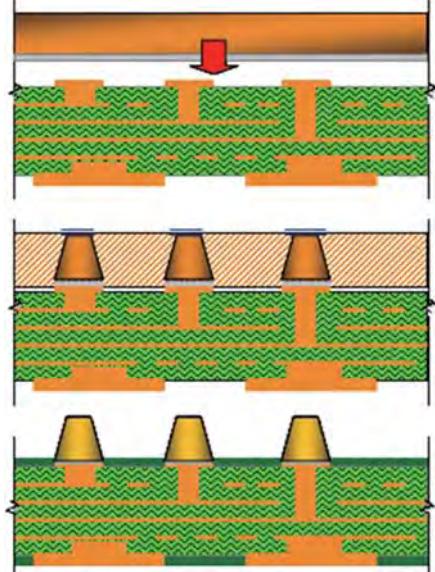


Figure 2. Basic HDI μPILR substrate fabrication sequence.

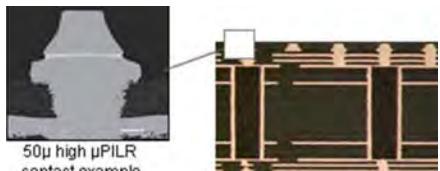
## HDI Substrate Development

The most common high density interconnect (HDI) substrate fabrication process used for facilitating high-pin-count direct flip-chip attachment begins with a high grade laminated glass reinforced epoxy-resin core structure. A number of dielectric and copper circuit layers are generally ‘built-up’ onto both sides of the ‘core’ structure using conventional lamination processes. In regard to substrate material, the majority of multi-layer substrates developed for flip-chip packaging rely on one of the commercial high-grade glass-reinforced epoxy compositions (FR-4, FR-5 and B-T). There are also a number of specialty dielectrics that may be required for specific

applications. Although developers of these HDI substrates make a strong effort to furnish a balanced structure, substrate warp during the

solder joining process continues to be a problem. To overcome the warping effects and other assembly related defects, substrate fabricators are working closely with their customers to explore viable solutions.

One solution gaining notice is the  $\mu$ PILR<sup>TM</sup>, a unique process developed by Tessera. This process furnishes a raised solid copper pillar-like feature at each contact site (**Figure 2**). The  $\mu$ PILR process requires only slight changes to the basic substrate build-up fabrication methodology. Following the normal sequential fabrication process, a single layer of rolled copper foil is thermally bonded onto the array pattern side of the substrate using standard laminate press systems and a proprietary Cu-Sn-Cu

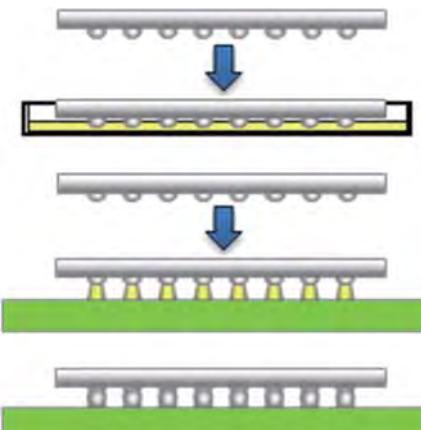


**Figure 3.** The 50mm-high  $\mu$ PILR contact joined to a very fine pitch land grid array on the HDI substrates top surface.

joining process. The example furnished in **Figure 3** is a cross-section showing the resulting metallic interface of the  $\mu$ PILR contact and land pattern on a HDI substrate interposer. After completing the bonding process, a photo-resist material is applied over the copper foil, exposed and developed to define the flip-chip array contact pattern. The uncoated copper is then removed using standard chemical etching. The remaining process steps include the application of the photo-imaged solder mask and subsequent Ni/Au plating of the exposed raised copper features to provide the flip-chip solder attachment methodology. The Ni/Au alloy combination has proven ideal for both eutectic and Pb-free solder attachment of the flip-chip die elements.

### Flip-Chip to $\mu$ PILR Assembly Process

During the package development phase of the flip-chip-on- $\mu$ PILR program, a test die and substrate vehicle was prepared to represent a model currently produced by a leading semiconductor company. The die-to-substrate assembly process begins with the transfer of the alloy



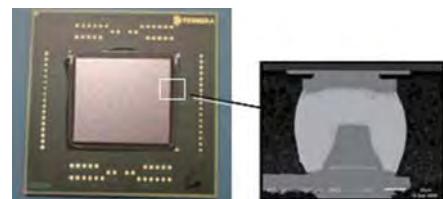
**Figure 4.** Flip-chip to  $\mu$ PILR assembly sequence.

bumped die element from its carrier tray or wafer carrier to a shallow flux reservoir. A precise level of the flux is maintained in the reservoir so that only the lower half of the bump contact is actually coated. Although standard die-attach systems can be used for die placement, there are also a number of commercial SMT assembly systems that have the accuracy needed for flip-chip placement. In anticipation of use for flip-chip assembly, these commercial SMT systems also furnish dip-tray stations between the semiconductor pick-up location and the substrate. **Figure 4** shows the basic assembly sequence for mounting the bumped flip-chip die onto a  $\mu$ PILR configured substrate. After mounting the flux-coated die, the substrate is transferred to a furnace system to complete the joining process. The temperature and thermal profile developed for reflow solder is dependent on the bump alloy selected. The solder alloy bump provided on the flip-chip test model was a SAC305 alloy composition. While the SnPb eutectic alloy may reach only 218°C the Pb-free SAC alloy generally requires a temperature of 235°C to 245°C to complete the joining process.

### Post Reflow Reinforcement

How to solve the physical stresses caused by the wide coefficient of thermal expansion (CTE), the mismatch between die (3 ppm/ $^{\circ}$ C) and package substrate (>16 ppm/ $^{\circ}$ C) is a primary challenge facing the packaging specialist. During various operating temperatures, the disparity between the die and the substrate can introduce physical stresses that can

compromise the integrity of the solder interface. Traditionally, underfill has been used to decrease the stresses caused by CTE mismatch and to improve solder joint reliability. However, due to the narrow stand-off height and often irregular solder bump profile, uneven flow and voiding in the underfill is common. On the other hand, the uniform stand-off height provided by the  $\mu$ PILR contact, enables unrestricted capillary flow of the underfill. Even though the ‘tacky flux’ material used for initially mounting the bumped die onto the  $\mu$ PILR contact site was rated as ‘no-clean’, a residue free surface on both die and substrate is vital so that the underfill material is able to flow smoothly and evenly between the surfaces. **Figure 5** shows a daisy-chain-



**Figure 5.** Post underfill example of a reflow soldered 10,132 I/O bumped flip-chip semiconductor mounted onto a  $\mu$ PILR substrate.

configured test die and substrate developed to replicate the physical outline and contact pattern of a functional semiconductor model. The vehicle developed for flip-chip-on- $\mu$ PILR evaluation included a face-down 20mm x 18mm x 1.75 mm thick, 10,132 I/O solder bumped die mounted onto a 40mm x 40mm x 1.25mm thick  $\mu$ PILR array configured substrate. Key concerns when selecting underfill products are the materials-glass transition temperature (Tg) and CTE after curing. In addition to the Tg and CTE issues, the underfill material selected needs to provide process uniformity and ensure end-product reliability.

### Final Assembly Process

Following the basic flip-chip assembly and underfill process, pre-formed solder alloy spheres are attached to the bottom side of the substrate. The process used for attaching the solder spheres to the bottom surface of the package begins with a stencil printing process that deposits a thin layer of ‘tacky flux’ at each contact site. Following solder ball placement, the flip-chip assembly is transferred once again to a reflow soldering system to

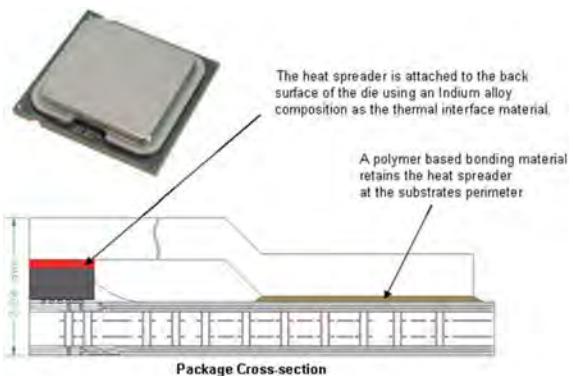


Figure 6. Heat spreader attachment.

complete the joining process. The systems commonly used for thermal reflow attachment of the solder spheres is a conveyor type, multiple zone convection oven. Time and temperature parameters for reflow soldering are closely monitored. The thermal profile developed for solder-ball attachment for the  $\mu$ PILR test model established an overall time duration of approximately 60 seconds above liquidus with a peak temperature of 240°C. The reflow procedure was followed by a

dynamic cleaning process using an alcohol/water solution to remove any surface residue. Following electrical testing, X-ray, and visual inspection, a coined copper alloy heat spreader was mounted onto the top surface of the package. The final assembly step was the bonding of a heat spreader to the semiconductor back surface and the substrates perimeter edge area (**Figure 6**). This was achieved using a relatively low melting temperature Indium alloy as the thermal interface material (TIM) and a low modulus polymer compound for edge sealant.

### Conclusion

The  $\mu$ PILR technology has proved to be a truly novel approach for flip-chip substrate fabrication. The raised contact format is proving to be a practical low-cost solution for the finer-pitch flip-chip applications because it overcomes most

of the assembly process yield concerns. This is due to the precise standoff height and the slightly tapered profile of the solid copper contacts. The small diameter contact profile not only enables finer contact pitch but it accommodates higher density circuit routing. Because the copper foil is furnished with a uniform thickness, a near perfect planer surface is retained for mounting the solder bumped flip-chip die. Soldering the flip-chip die onto the  $\mu$ PILR contact has also proven to furnish a physically stronger die-to-substrate interface and a more uniform standoff profile when compared to common bumped flip-chip-on-land and copper-post-on-die technologies. <sup>SR</sup>

### Acknowledgements

Key contributors in the preparation of this article included Tessera's Ilyas Mohammed, Ellis Chow and Laura Mirkarimi. Note:  $\mu$ PILR is a trademark of Tessera Inc. or its affiliated companies in the United States and other countries.

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# Copper Wire Interconnect Has Arrived

By Flynn Carson [STATS ChipPAC]

**C**ost and time-to-market are key variables to any product's success. As geometries and cost of the device fabrication process shrink, the device package cost becomes a larger component of the product cost. Value engineering to reduce this is a relentless and never-ending challenge. Cost reduction in packaging solutions and technology should also be easily implemented and transparent to end customers and users with respect to any impact to performance, quality, or reliability. Such cost saving technology can be introduced without impacting time-to-market and help the device manufacturer achieve or maintain a competitive edge in their respective markets. Copper (Cu) wire interconnect is a game changer for wire bond package solutions, replacing traditional Gold (Au) wire interconnect, and enabling lower cost without sacrificing performance, quality, and reliability.

Cu wire interconnect is not new and has, in fact, been used for many years in heavy wire bond applications such as low lead count power devices. It has many desirable characteristics that make it suitable for this application: excellent electrical and thermal properties, high fusing current, and low cost (**Table 1**). Since these types of devices are wedge bonded, the oxidation issue related to Cu wire could be more easily managed. Also, the hardness of Cu wire compared to aluminum (Al) or Au can be managed since these types of devices have quite robust bond pad structures. However, when trying to implement low-cost Cu

wire for the majority of wire bond package solutions that use a Au wire ball bonding process, the easily oxidized and harder Cu wire has faced a significant challenge. Thermo-sonic ball bonding allows for a much faster interconnect process compared to wedge bonding and is also compatible with advanced wafer fabrication nodes and bond pad structures with low-k dielectric and circuitry under the bond pads.

The first step of the ball bonding process is ball formation. This is done by applying a very large voltage to the tip of the wire extending slightly from the bond tool or capillary. During this electronic flame-off (EFO) of the wire to form the ball, oxidation can readily occur with Cu wire, as opposed to conventional Au wire. Such an oxide needs to be controlled as it will interfere with the Cu ball bond to the Al bond pad on the device. Thermo-sonic bonding of the ball to the bond pad is the second step in the ball bonding process. During this step, thermo-sonic energy is used to form the bond. Temperature, time, power, force, and ultrasonic energy are applied to the ball, deforming and bonding it to the bond pad. This is where the hardness, particularly the work hardness of Cu compared to Au, becomes an issue. Due to this increased hardness, Cu wire has a tendency to "scrub through" the thickness of the Al bond pad and displace all the Al (**Figure 1**). Hence, Cu wire must overcome these

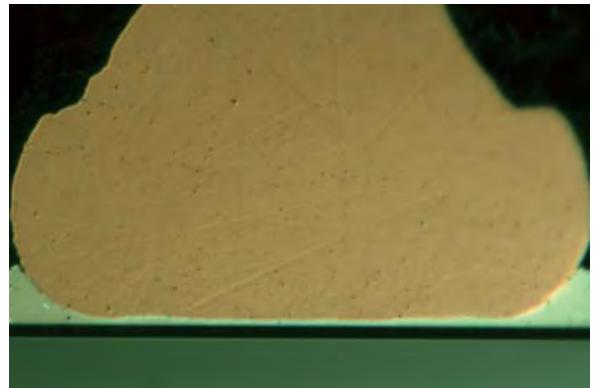


Figure 1. Cross-Section Cu Ball Bond on Al Pad.

challenges as well as demonstrate the same extremely high yields and reliability as Au wire to be considered a drop-in replacement.

## Ball Bonding Cu Wire

Advances in materials, equipment, and process have enabled Cu wire to prove itself comparable in yields and throughput to Au wire for most package applications. To address the issue of oxidation of the wire during the ball formation process, wire bonding equipment manufacturers have introduced kits that can be retrofitted to existing wire bonders or implemented on new bonders that allow the ball to be formed in an inert atmosphere. A flow of inert gas, such as forming gas (95%N<sub>2</sub>/5%H<sub>2</sub>), can be introduced where the ball is formed so that the newly formed Cu ball has no oxide on the surface and forms a symmetric ball. Forming gas or a blanket of N<sub>2</sub> gas is directed at the package surfaces to be bonded, the bond pad on the semiconductor device, and the bond finger or lead of the package substrate, so that the bond to each can be made without inducing oxidation that could interfere with wire-bond yield, quality, and reliability. Bonding wire manufacturers have also introduced Cu wire with very thin Palladium (Pd) coating or plating to reduce the wire's

Wire Material	Melting point (Deg. C)	Thermal Cond. (W/m-C)	Electrical Resistance (ohm-m)	Young's Modulus (Gpa)	Tensile Strength (MPa)	Hardness @ ball (Hv)
Gold	1064	315	2.33 x 10 <sup>-8</sup>	80	240	60-80
Copper	1083	393	1.72 x 10 <sup>-8</sup>	120	290	80-90
Pd Coated Copper	1083	393	1.80 x 10 <sup>-8</sup>	120	290	85-95

Table 1. Wire Material Properties.

sensitivity to oxidation and help it bond more readily to the bond pad and package terminal. Our studies have shown that yields and uptime of the wire bonder with Pd coated Cu wire is comparable to Au wire for both leadframe based and laminate substrate based wire-bond packages. All of the major bonding wire suppliers offer a Pd coated Cu wire product and are supporting this growing trend.

Bonding wire manufacturers have also played a pivotal role in introducing softer, more bondable, Cu wire. In tandem, the bonding tool/capillary makers and the equipment manufacturers have optimized products and software for Cu wire. The combination of softer wire, optimized tools, and Cu-wire-specific bonding parameters and looping profiles has allowed for Cu wire to be proven bondable on all but the most delicate bond pad structures used on the vast majority of devices in production today without damaging the bond pad structure or underlying dielectric and circuitry.

To assure and control the wire bond process and integrity, metrology and analytical techniques were developed to account for the unique properties and characteristics of the Cu wire bond compared to Au. Cu wire bond intermetallic is different than that of Au wire as the Cu to Al intermetallic compound (IMC) formation is much less than that of Au to Al during the bond process. Thus, whereas Au IMC post bond is measured by etching the Al bond pad on the device and measuring the IMC area, which is quite visible on the bottom of the Au ball, it is best to etch off the Cu wire and measure the less visible Cu IMC on the Al bond pad (**Figure 2**). Etching of the bond pad metal is still used for Cu wire to check for cratering, cracking, or damage of the bond pad structure. In addition, because of the Cu hardness, it is important to do a substantial amount of cross section analysis during the bonding characterization stage to make sure there is no subtle damage to the bond pad layers or stack. For this type of work, a very clean cross sectioning methodology is needed with clear and precise SEM analysis and images.

Cu wire has little issue passing the bond pull and ball shear test requirements

typically used to monitor Au wire bond integrity due to the higher mechanical strength of Cu, and Cu wire is also more resistant to wire sweep during the encapsulant molding process. However, Cu wire, being less dense than Au wire, is not as visible on the X-ray equipment used to monitor wire sweep, so new, more sensitive X-ray equipment must be implemented to inspect for wire sweep, especially for Cu wire less than 25 $\mu$ m in diameter.

As a result of all the improvements in materials, equipment, process, and methodology to assure the integrity and quality of the Cu wire bond, Cu ball bonding has been implemented in production with the same yield and quality as Au wire.

### Reliable Cu Wire Interconnect

Another important concern that has been overcome with Cu wire is proven reliability. Au wire ball bonding has a long history and reliability track record. Cu ball bonding cannot match this track record yet, but advancements in materials and production control has shown repeatable results. The maturity and confidence in Cu interconnect reliability is growing every day. There is a fundamental understanding of the variables that impact the reliability. The Cu ball bond is more sensitive to ionic impurity and the pH of the encapsulant molding compound (EMC). As a result, EMCs have been developed with guaranteed levels of ionic contamination, particularly Chlorine, of less than 30ppm and pH is controlled in the range of 4 to 6. Ionic contamination

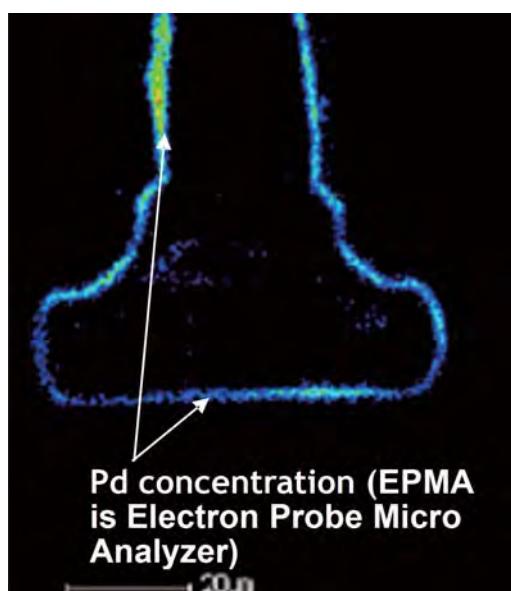


Figure 3. Pd at Ball Bond Interface.

can also come from the environment during the wire bonding process. This has driven the use of Class 1K clean room environment (Class 10K is the typical standard) and a more stringent housekeeping and gowning practice for production workers for Cu wire.

Another improvement that has been made for robust reliability and repeatability is the use of the aforementioned Pd-coated Cu wire. Our studies show the Pd, although dispersed during the ball formation, is present at the bond interface (**Figure 3**) and appears to make the bond less susceptible to failure during reliability test related to the bond cracking at the bond pad interface and related to corrosion or oxidation. Pd-coated Cu wire is recommended as it has demonstrated higher production yields and shown better reliability than bare Cu wire in several instances, especially with finer bond pad pitch and more advanced devices, which are less forgiving with respect to the process window and reliability.

More data and evidence of Cu wire interconnect reliability becomes available daily, increasing device manufacturer's confidence to apply Cu wire and realize the cost savings for ever more challenging applications and use requirements. Already

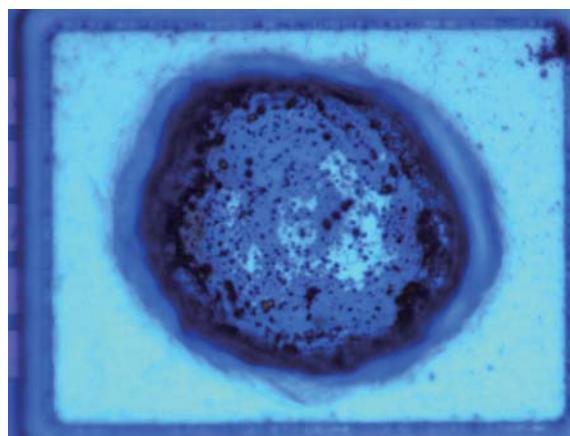


Figure 2. IMC Area of Cu Wire Bond (90% IMC).

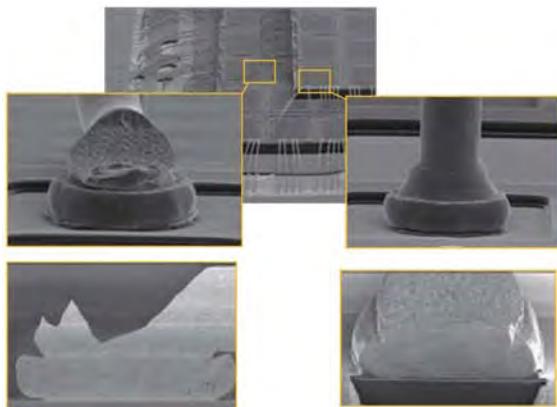


Figure 4. Die-to-Die Cu Wire Bonding.

most device manufacturers are rapidly converting to Cu wire for mobile and consumer applications, with those in computing and more demanding reliability and use requirements carefully considering or starting their due diligence.

#### Future Trends for Cu Wire Interconnect

Cu wire will continue to be applied to widespread applications and more

advanced silicon nodes. Die-to-die and reverse bonding (where a second bond or stitch bond is made on top of a ball bond) are actively being developed, qualified, and introduced into production (**Figure 4**). This will open the door for Cu wire to be used in stacked-die packages and side-by-side system in package (SiP) integration. Finer bond pitches below 45 $\mu$ m and less than 40 $\mu$ m bond pad opening will be in production soon, followed by even finer bond pad pitch and opening capability as the leading edged devices continue to shrink. Advanced wafer fab devices, beyond the current 40nm node with extra low- $k$  (ELK) dielectric and circuit under pad (CUP), will be characterized and proven for production. Advancements in materials, especially in terms of the wire itself (thinner diameters, softer wire), as well

as equipment will be needed to support these future needs. Wire bonders tailored for Cu wire can be more efficient and further reduce the cost of Cu wire interconnect.

#### Conclusions

Cu wire has arrived and is poised to displace the volatile priced Au wire on a large scale. Early adopters are already realizing the benefit of lower cost without sacrificing yield, quality, and reliability. Others in their respective markets will convert in order to be able to compete. As the confidence and maturity of Cu wire grows it will find its way into broader and more stringent applications. In the past, temporary spikes in the price of Au have never led to the maturation and widespread adoption of Cu wire, but the sustained high price of Au and focus on cost reduction has finally driven Cu wire across the finish line as a proven technology ready for widespread adoption — Cu wire is here to stay. 

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# Single Sided Wafer Thinning and Handling

By Ricardo I. Fuentes, Ph.D. [Materials and Technologies, Corp. (MATECH)]

Many excellent articles have been written on conventional grinding, polishing, and thinning techniques; as well as on the many methods for bonding a wafer to a carrier for handling, thinning or processing. This article focuses on something different—a novel chemical technology that thins wafers down to 50 $\mu\text{m}$  or less, with better uniformity, and at a lower cost than conventional thinning. Additionally, it will also discuss methods of handling thin wafers without carriers of any sort, thus dealing with the inherent issues of wafer distortion, warpage, and extreme fragility.

Wafer thinning can be performed in several ways: 1) by grinding the wafer down (usually to 100 to 150 $\mu\text{m}$ ), 2) by chemical mechanical polishing, which can bring the wafer thickness down to 50 $\mu\text{m}$  or less, 3) by chemical etching, which thins the wafer down and removes the subsurface damage left by grinding and polishing, and 4) by plasma etching. Usually a combination of grinding and one of the other methods is the most practical route to a cost effective thin die solution.

Most thin wafer handling is performed by bonding the wafer to a temporary carrier and thus handling the wafer in much the same way as a conventional thicker wafer. There are, however, applications where, for reasons of yield, economics, process flow, or device performance, it is preferable to handle the wafer without a carrier. It is this latter case that will be addressed here.

## Thinning and Stress Relief

Chemical thinning is a necessary step to eliminate the subsurface damage and relieve the stress that grinding and polishing leave behind. Chemical thinning is also an alternative to polishing (following grinding) as the method to make ultrathin wafers. It has the added benefit of completely eliminating damage or surface features that result in electrically active sites that other technologies may leave

behind, which are deleterious to device performance.<sup>1</sup>

Wet etching involves the interaction between a liquid and a solid substrate and it is often the fastest, most cost-effective way to remove material<sup>2</sup> selectively or across an entire surface, as required in packaging applications and many other steps of semiconductor fabrication.

The demand for denser, lower package heights, higher power requirements, tighter total thickness variation (TTV) specs, and the development of higher-functionality systems-in-a-package (SiP) or systems-in-a-foil (SiF) are driving the need for more robust, lower cost, higher yield thinning technologies with no end in sight.<sup>3,4,5</sup>

When the substrate may be wetted on both sides, immersion is a common choice for etching and thinning. If the substrate may only be exposed to etchants on one side, spin or spray become reasonable candidates, but each has its shortcomings — such as radial and transport-induced non-uniformities. Depending on the particular package or device requirements, improved uniformity (in terms of TTV) is often an important consideration; conventional technologies have clear limitations in terms of how much material they can remove while staying within the allowed TTV requirements. These technologies often result in undesirable exposure of the non-process side to residual liquid or vapors. This is of particular importance on freestanding wafers.

A novel etching technology\*, provides high uniformity as well as true single-sidedness on large ultrathin substrates. It addresses the main shortcomings of conventional wet processing by providing a consistent and uniform supply of chemicals throughout the liquid-solid interface while making available an orthogonal path for the byproducts, such as gases and vapors. Exposure of every surface element to the same chemical and transport environment makes the process

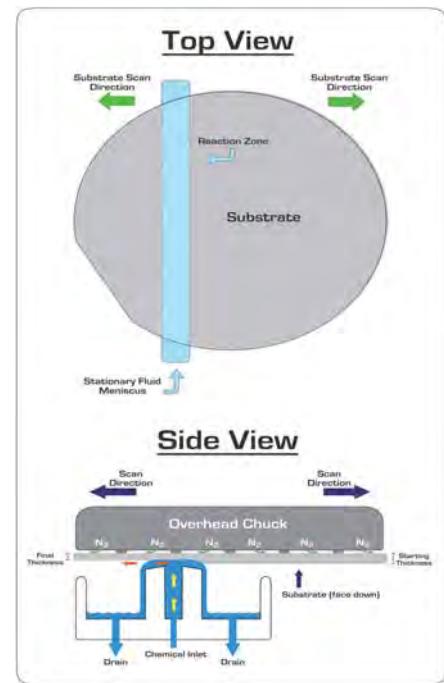


Figure 1. Schematic representation of the LinearScan process depicting the substrate material being removed by the etching process (held process side down), as well as the orthogonal paths of the reactants and the byproducts. The shaped flow of gas (DynamicConfinement), preventing the encroachment of fluid and vapors onto the non-process side (top), is also shown. Note the removal of material (etching) after the wafer has passed over the fluid meniscus and the different paths the reaction byproducts take to avoid interference with the supply of fresh reactants to the reaction zone. The top view illustrates the wafer being scanned repeatedly in alternating directions, as necessary, over the fluid meniscus showing the narrow reaction zone where thinning is in progress (wafer is being etched from below).

intrinsically uniform (**Figure 1**). The solid-liquid interface (boundary layer) is not subject to speed gradients, convection, or other transport-related gradients that may cause variations in its thickness and result in a large TTV. The system eliminates virtually all transport-related and centrosymmetrical non-uniformities that plague spin/spray and immersion processes. **Figure 2** shows the uniformity of 4", 6" and 8" wafers (as TTV) after the removal of 75 $\mu\text{m}$  with this proprietary tool. Substrates are held on their non-process side by a side-gripping or



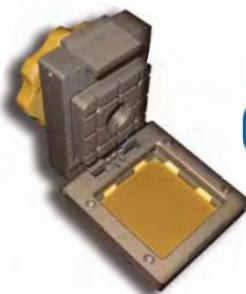
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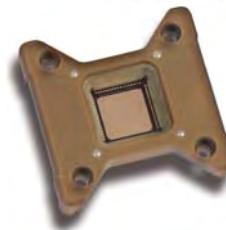
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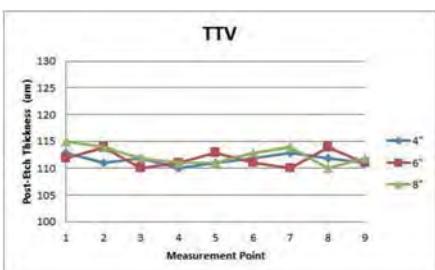


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**Figure 2.** The material removal uniformity (Total Thickness Variation or TTV) typical of the WaveEtch LinearScan thinning process is illustrated above. TTV ranges from  $\pm 1.5\mu\text{m}$  for 4" wafers to  $\pm 2.5$  for 8" wafers after the removal of 75 $\mu\text{m}$  to reach a final thickness, in this case, of 112 $\mu\text{m}$ .



**Figure 3.** Image of MATECH's side-contact chuck (CAT chuck). Notice the position of the fingers that have moved out of the way to avoid contact with the etching fluid while the remaining fingers stay in contact with the sides of the thin wafer keeping it within capture range of the fluid pool. The adaptive handling allows the chuck to manage ultrathin, severely distorted wafers while making no contact with the non-process side.

"caterpillar" non-contact chuck (or CAT chuck for its resemblance to the side motion of the namesake insect's legs), while being gently scanned over a narrow pool of etching chemicals. This novel chuck holds the ultrathin wafer by its edge and its legs retract sequentially out of the way as the wafer is scanned over the fluid meniscus, making no contact with the backside (non-process side) of the wafer, while still protecting it from vapor or liquid encroachment (**Figure 3**).

The reactants enter the reaction zone through the bottom of the pool, while the byproducts exit in a plane parallel to the substrate surface; this delays bath saturation, extends bath life, and ensures a consistent supply of fresh chemicals to the surface. The substrate is not immersed, but merely put in contact with the top of the pool's meniscus, as is also illustrated in **Figure 1**.

Chemicals and vapors are kept away from the non-process side by a proprietary gas sealing technology\*\* (**Figure 1**), which forms a gaseous O-ring around the periphery of the substrate to

prevent any liquid or vapor incursion. In this way, the non-process side is not subject to physical or chemical contact, thus eliminating the need for any kind of backside protection, such as resist or tape.

Wafer thinning and stress relief are native applications of this etching technology. Additionally, substrate assemblies — at any point in the packaging process, and of virtually any thickness, structure, and size — are all compatible with the process.

The final thickness for modern IC device substrates continues to decrease, with 50 $\mu\text{m}$  being the current state-of-the-art target for many modern devices.<sup>6</sup> Linear scan etching systems are particularly well suited to handle and process very thin substrates. The unique process is carried out with no violent spinning, no need for lateral confinement by pins or other hard devices that may damage the wafer's edge, and no dynamic loading due to high rotational speeds. In the absence of hydrodynamic edge effects, the edges of the wafers are free of sharpness and the formation of "teeth", or other features common in spin/spray etch systems that significantly weaken the substrates.<sup>7</sup>

The chemistries used in linear scan systems do not require surfactants and are used in smaller volumes at lower flow rates, allowing for more efficient chemical usage. Chemicals can be used to a process-dictated end-point without regard to surfactant depletion. Together, these features lower chemical usage and its associated purchase and disposal costs, as well as often easing environmental regulatory compliance resulting in overall production and costs-of-ownership reduction. Chemical usage reduction can range from approximately 20% to a factor of two or more, depending on the process, method, and tooling used to perform it.

Since all areas are exposed to the same chemical and transport environment, the size and shape of the substrate are largely irrelevant. A process developed for a given substrate geometry can be readily used for other substrate geometries, making product process migration effortless and cost effective. Linear scan etching systems naturally accommodate odd, noncircular, thick substrates, and structures larger than 300mm, as well as severely distorted wafers (up to 10 mm off-plane distortion).

For cleaning applications, such as those sometimes required for 3D stacks' low standoff height structures or to remove residual polymer, the chemical process and the rinse steps may be augmented by the application of megasonics. Megasonics alter the behavior of the boundary layer, promote transport to reach crevices in complex or high aspect ratio structures,<sup>8</sup> and speed up the process and rinse steps. The interfacial control allowed by this technology enables unprecedented manipulation of the liquid-solid interface.

Since there is no mechanical contact with the surface of the substrate, linear scan systems are well suited for thinning and stress relief after grinding operations for packaging applications of very thin wafers. The process offers superior uniformity (**Figure 2**) and thus the ability to tune grinding operations for optimum yield, picking up more chemical removal if necessary, while staying within the TTV budget and lowering the cost of the whole operation. The systems can handle the single-sided wet etching of ultrathin wafers ( $\leq 50\mu\text{m}$ ) avoiding the risk of punch through due to their uniformity. Intrinsic limits of grinding operations and downstream yield losses (from de-taping or debonding) usually prevent grinding to thicknesses below 150 $\mu\text{m}$ . The gentle and uniform nature of linear scan wet processing can easily thin well below 50 $\mu\text{m}$ .

## Ultra-thin Wafer Handling

Processes such as temporary bonding, back-grinding, metallization, etching, debonding, and dicing, all may involve some form of thin wafer handling. In general, all of these are carried out by bonding the device wafer to a temporary handle or carrier. The purpose of this operation is to handle the wafer throughout the process as a SEMI standard wafer would be handled, thus allowing use of existing equipment and facilities. To remove adhesive residue (usually by a wet process) and during packaging, the ultrathin wafers have to be detached from their carrier and handled freestanding. It is at this point that issues of breakage (i.e. yield) arise.

In these cases, thin wafers (as thin as 50 $\mu\text{m}$ ) have to be handled directly. Among the common wafer handling technologies — vacuum chucking, gripping, and

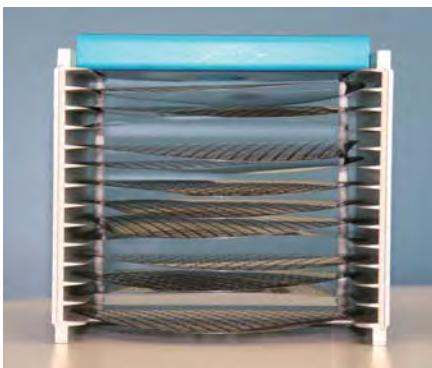


Figure 4. Image showing the large amount of out-of-plane distortion and warpage typical of unsupported ultrathin wafers. In this case approximately 10mm. Notice also the wide slots in the special cassette designed to accommodate said distortion.

Bernoulli — the latter is most suitable for ultrathin wafer handling between the cassette and the process station. The system is rugged, reliable and capable of a throughput of over 200wph.

There are two primary challenges in handling ultrathin wafers: distortion and breakage. The deflection of a wafer, in the

absence of added stress, is proportional to the square of its radius and inversely proportional to the third power of its thickness.

**Figure 4** shows the amount of distortion common in back end of the line (BEOL) freestanding ultrathin wafers. In this case, the distortion is approximately 10mm, compounded by the stress caused by additional layers deposited on them. Any method that will effectively hold and handle them must take this into account.

An end effector\*\*\* specifically designed to handle thin, distorted wafers was used (**Figure 5**). To planarize the wafer and confine its lateral motion, the end effector has a rim of very small fluoropolymer vacuum pads which make contact in the exclusion zone. This approach to lateral confinement is preferred to other contact methods which may chip or damage the edge of the wafer, resulting in reduced strength or breakage.



Figure 5. Bernoulli end effector effectively and consistently handles unsupported ultrathin wafers, down to 50 $\mu$ m thick. This image shows an 8" end effector used in conjunction with a WaveEtch system equipped with a side-contact CAT chuck. The etching system handles and processes freestanding 6" and 8" ultrathin wafers.

To assist in accommodating the extreme distortion, it is common for the cassette slots to be double-spaced as compared to standard wafer cassettes (**Figure 4**). Since the wafers can take a shape that is changing and unpredictable, the loaded cassette must be scanned before any wafer is moved out of it on into it. The cassette scanner measures the position of the edges

(continued on Page 53)

## Net-Zero

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-Carol McCuen, RF Engineer

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# Burn-In and Test Socket Manufacturing Technology, Markets and the Challenges in 2011

By Ron Molnar [Az Tech Direct LLC]

The requirements, design, and development of burn-in and test sockets continue to expand in complexity in direct relationship with device fabrication and packaging technologies. Over the years, based on corporate directives, it is now common for the Product Development Team — consisting of device, packaging, and test engineers, to design next generation product based on leading-edge capabilities in these areas. Modeling and simulation are playing an important role in product development, with the mechanical, electrical and thermal considerations taken into account at all levels. Keep in mind the socket is basically an interface between the packaged device on one side and some type of substrate or board on the other, connected to the testing system. This obviously adds to the complexity as socket manufacturers must meet requirements on the board/system side to optimize testing, for that particular device/package type. The impact of heating and cooling on the thermal properties of materials plays an even larger role in design for sockets utilized in hot/cold testing or for burn-in applications, with package geometries and materials also impacted by temperatures during the testing.

The socket supply chain has also grown in complexity, with focus on total cost-of-use or ownership (CoO), versus comparison of the socket selling price alone. Information related to contactor technology, material selection, socket manufacturing, and the customer data on contactor life and yield are all part of the cost model equation. Companies with burn-in and/or test systems, ranging from single facility to multinationals, are going beyond the cost model to define socket supplier relationships. Design and manufacturing locations, technical support and capability for prototype or volume production may be key factors.

To get a snapshot of where the socket industry is and what the next year will bring, executives from some of the world's leading socket manufactures were asked to weigh in with their thoughts in response to three (3) specific questions which is intended to initiate conversations with manufacturers on capabilities and product detail.

- 1) What is your competitive advantage?
- 2) What are the key markets you serve?
- 3) What are the challenges seen in 2011?

In a general overview of the responses, regardless of the socket technology, responses to the challenges for 2011 were by far the most interesting. For example, one respondent noted that WLP formats are beginning to blur the distinction between wafer probe cards and BGA sockets, driving the performance and reliability needed for wafer probe at a socket price point. The majority of challenges expressed were related to the increases in both the contact point "quantity and density", typically termed as the package lead, pad or ball "count and pitch". Higher performance, higher density, and faster speed at lower cost of ownership and faster time-to-market were an ongoing theme. Additionally, thermal and power challenges, and an increased need for device parallelism were mentioned. Only one company cited concern with the volatility of the semiconductor industry itself. It's interesting how some respondents' competitive advantages were identified as other challenges.

*An excerpt of this article has been formatted to coincide with the 2011 BiTS Workshop Guide & Directory.*

## Advanced Interconnections

Ann Cibelli

*Director of Communications*

**Competitive Advantage:** Compact size BGA sockets, same size as BGA to a few millimeters larger, with SMT design

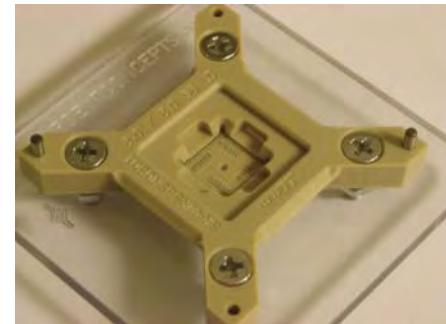
eliminating need for large keep-away areas or mounting holes and with soldering profiles often matching that of original device.

**Target Market:** BGA sockets for validation of chip sets, in applications including computer/server and automotive. Medical equipment, hand-held devices and military systems, where BGA's need to be removed or replaced in the field.

**Challenges seen in 2011:** Increasing signal speeds and finer pitches of less than 0.5mm. Research new insulator materials and applying screw-machined terminals, such as patented interstitial pin design, for lower profiles and shorter signal paths.

## Ardent Concepts

Stephen J. Cleveland  
*VP Business Development*



**Competitive Advantage:** Patented wire forms to reduce the cost of test and address the needs of high density, fine pitch applications.

**Target Market:** Technology optimized for AC performance and particularly well suited for test applications where signal integrity is of paramount importance.

**Challenges seen in 2011:** Meeting the needs of higher density applications, while aggressively reducing the cost of the consumables.

## Aries Electronics

Bill Sinclair  
*President*

**Competitive Advantage:** CSP test sockets using patented "Probe and Spring"

contact, that can be designed for devices with pitches as small as 0.2mm. Contact system consists of interposer set of two elements for short, reliable signal path.

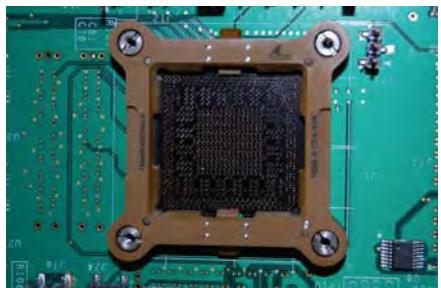
**Target Market:** CSP test sockets with pitches as small as 0.2 mm, for up to 500,000 cycles, at reasonable cost and minimal set-up fee. Adjustable pressure pads for force on CSP's, to ensure the connection for devices varying in thickness.

**Challenges seen in 2011:** Designing test and burn-in sockets that will work for smaller and smaller device pitches, in a variety of housing designs (clam shell, open top, etc.) at reasonable prices with minimal set-up fees will need to be addressed.

### Cascade Microtech

Randy Knudsen

*Test Engineer*



**Competitive Advantage:** Short electrical path designs provide a high-performance test solution for pad, lead and array applications. Worldwide sales and service team, with extensive knowledge and expertise, ensures our customer's success.

**Target Market:** RF and high-speed digital applications, from engineering test, characterization, failure analysis to automated test. Grypper is only solder-down, device-footprint test socket, allows BGA inserted without manual actuator.

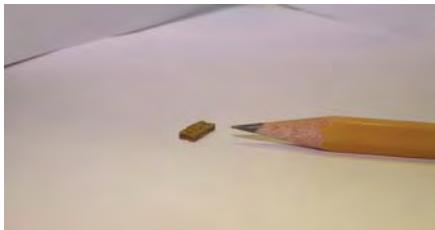
**Challenges seen in 2011:** Market demand, shorter lead times with added value. Higher performance and speed for hand-held devices and network products. Worldwide sales and service support to meet faster time-to-market and production up-times.

### Centipede Systems, Inc.

Thomas Di Stefano

*President*

**Competitive Advantages:** Replaceable contactor cartridges can be configured in arrays for parallel testing of devices in trays or strip formats, with high reliability



contactor arrays available at pitches to 0.4mm with extension down to 0.25mm.

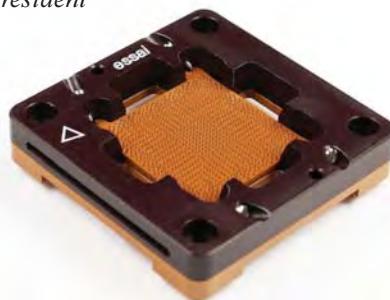
**Target Market:** Test and burn-in contactors for emerging Test-in-Tray back end applications that enable highly parallel handling.

**Challenges seen in 2011:** Achieve reliable, low maintenance contacts in high volume production . WLP formats begin to blur the distinction between wafer probe cards and BGA sockets, driving the performance and reliability needed for wafer probe at a socket price point.

### Essai

Nasser Barabi

*President*



**Competitive Advantage:** Functionality and reliability at competitive price points, derived from technology and infrastructure. Significant investment in research and development, advanced design, automated machining, state-of-the-art Material Lab.

**Target Market:** ATE, system level, and validation sockets, supporting advanced, high speed and high I/O packages. Processes support prototype and low volume manufacturing requirements that can scale to significant production volumes.

**Challenges seen in 2011:** Unpredictable nature of the last industry cycle showed ability to respond quickly to market changes is critical. Companies must be able to design, develop and deploy new solutions to address dynamic product landscapes.

### E-tec Interconnect

Chris Haffter

*Managing Director*

**Competitive Advantage:** The SMT, thru-hole and solderless (compression) mount sockets incorporating elastomer or probe-pin contact solutions and variety of closure types. Bandwidth to 30GHz. Pitch down to 0.30mm. Quick turn rush delivery.

**Target market:** Socket solutions for device prototyping, de-bugging, FPGA programming, pre-production and production test. as well as burn-in. Custom socket configurations for unique footprints and retrofit to the existing PCB layouts.

**Challenges seen in 2011:** Proliferation of higher pin counts, finer pitch, mixed pitch and non-symmetrical designs. Requirements for sockets with lower insertion loss, increased current ratings and high thermal dissipation, with high reliability.

### Interconnect Devices

Jon Diller

*Director of International Sales*

**Competitive Advantage:** Global and comprehensive manufacturer of final test sockets. With factories in the USA (Arizona/ Kansas) and China and also sales offices in Singapore and Europe, complete with test laboratories in our key facilities.

**Target Market:** Spring contact probes allows for durability and electrical transparency critical to high volume final test sockets for 0.4 and 0.5 mm pitch, ideal for WLCSP probing and the very dense wireless and networking BGA products.

**Challenges seen in 2011:** Robust solutions to reduce overall cost of ownership. The 0.3 mm pitch WLCSP's will arrive in force, creating demand for practical contactors, while managing the variable levels of demand as the economy stops and starts.

### Ironwood Electronics

Ila Pal

*VP of Marketing*

**Competitive Advantage:** Cost, lead time, socket size and six different contact technologies; embedded wire elastomer, spring pins, silver particle elastomer, diamond particle interposer, stamped/ etched spring pins and the silver ball matrix elastomer.

**Target Market:** Engineering and manufacturing of test and custom burn-in sockets, with delivery of custom

burn-in molded sockets for unorthodox packages in 3 weeks, less than conventional processes without compromising price.

**Challenges seen in 2011:** Technical challenges, as more packages have higher pin counts in the range of 1500 with 0.4mm pitch, meaning very high force needed in small area on socket. High strength materials and the new creative designs are a must.

### ISC

KS Lee

*Overseas Sales Mgr*

**Competitive Advantage:** Superior electrical performance in test speed/ frequency, quick turn capability with low cost per contact point. With S21 at  $-1\text{dB}$  at 40Ghz and 0.2nH, the conductive elastomer provides the performance below 0.4mm pitch.

**Target Market:** ISC has solutions for all the primary IC test applications from

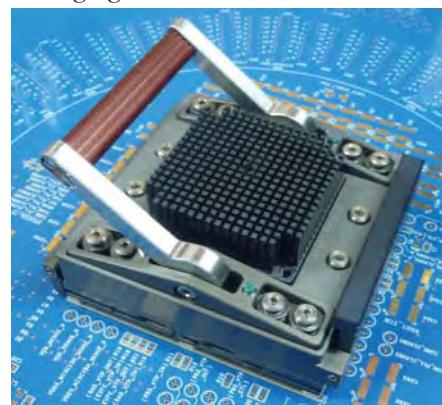
device bring-up and characterization to system level test, ATE and failure analysis.

**Challenges seen in 2011:** In 2011, ISC sees a continued march to lower costs, smaller lead pitches and greater device parallelism. We also are addressing increasing device speeds and functionality. Thermal and power challenges, higher test frequencies and physical demands like 3D packages and converging of wafer and package test. Coordination from development to end customer socket use at their global locations.

### Modus

Bruce Rogers

*Managing Partner*



**Competitive Advantage:** State-of-the-art technologies and low cost manufacturing provide cost effective test solutions, while leveraging a global sales and support team, Transcend Technologies assures seamless solution implementation and rollout.

**Target Market:** Automated production test, system level test, and device characterization sockets. Complete arsenal of materials and contact technologies, as each of these test regimes has unique requirements for the various package types.

**Challenges seen in 2011:** Thermal and power challenges, higher test frequencies and physical demands like 3D packages and converging of wafer and package test. Coordination from development to end customer socket use at their global locations.

### Multitest

Tony DeRosa

*Product Manager*

**Competitive Advantage:** Advanced contact technology, providing high volumes

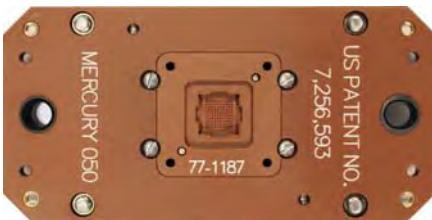
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using barrel-less or flat spring probe technology. Cantilevered beam technology offers advanced coatings to extend probe contact life and improve yields.

**Target Market:** Production test market, with range of contactor offerings for high end digital, automotive, high speed analog and communications. The Plug & Yield? Program minimizes integration risk and reduces overall lead time

**Challenges seen in 2011:** Total value, consisting of contact technology, short design cycles and hardware lead-times. In field, attention then turns to other cost factors of first pass yield, contact life, cleaning frequency and contact replacement cost.

### Plastronics

Steve Durrett

*Sales Manager*

**Competitive Advantage:** The H-pin Technology, offers high frequency, low resistance contact, 100% automated through the supply chain. Customers get better lead time, lower overall cost for volume production, down to the 0.4mm pitch.

**Target Market:** Burn-in sockets for high current or tough electrical specs. Design, tooling and molding of sockets or connectors in 250 to 25,000 volumes, withstands 180C+, for system level test, burn-in, automotive and military connectors.

**Challenges seen in 2011:** Although predicting a healthy semiconductor industry for at least the next 18 months, price erosion and nervous customer base impact forecasting, as uncertainty in debt level around the world impact the capital expenditures.

### Yamaichi Electronics

Nick Langston

*Business Development Manager*

**Competitive Advantage:** Technology with unique products allows superior solutions such as extending the contact

lifetimes, increasing yields on analog and mixed signal products, supporting extremely high data rates and bandwidth requirements.

**Target Market:** Testing and wafer probing product lines, with local and global engineering, manufacturing and sales support. Product design for sub 0.4mm pitch, data rates beyond 20 Gbps,

and contact life in excess of 1 million cycles.

**Challenges seen in 2011:** Quality! It is low quality — not high price — that will hurt business. Quality is the sum of how our people and product perform, existing in the relationship and product for all the electrical, mechanical and logistical need.

## New Horizons in Bond Testing

The Nordson DAGE 4000Plus is the most advanced bondtester on the market, representing the industry standard in bond testing.



### Data Integrity

Developed by the world leader in bond testing technology, the 4000Plus offers unsurpassed accuracy and repeatability of data providing complete confidence in results.

### Extensive Testing Capability

Load cartridges combined with standard and specialized fixtures perform shear tests up to 500kg, pull tests up to 100kg and push tests up to 50kg, covering all your test applications including new hot bump pull and fatigue applications.

### Ultimate Versatility

A range of XY stages, with a 160mm XY stage as standard, meets a wide range of requirements. The image capture system for advanced analysis is quick to set-up and in close proximity to the test head aiding faster testing.

### Intelligent Software

The 4000Plus utilizes Nordson DAGE's next generation Paragon™ software which boasts a highly configurable and intuitive interface as well as a wide variety of advanced functionality such as automatic GR&R calculation, built-in diagnostics, a unique database search engine wizard and superior reporting.

Learn more at  
[www.nordsondage.com/4000Plus](http://www.nordsondage.com/4000Plus)



[www.nordsondage.com](http://www.nordsondage.com) | [globalsales@nordsondage.com](mailto:globalsales@nordsondage.com)

# INTERNATIONAL DIRECTORY OF TEST & BURN-IN SOCKET SUPPLIERS

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COMPANY HEADQUARTERS	SOCKET TYPES	PACKAGE TYPES	SOCKET SPECIFICATIONS
Company Street Address City, State, Country Telephone Website	B = Burn-in D = Development P = Production T = Test Contactor  CM = Contact Mfgr.	BA = Ball Array BD = Bare Die LA = Leadless Array SM = Surface Mount TH = Through Hole	CP = Contact Pitch CL = Contact Life OT = Op. Temp. Range FQ = Frequency (Ins. Loss) CF = Contact Force / Pin CR = Current Rating / Pin
Advanced Interconnections Corporation 5 Energy Way West Warwick, RI 02893 Tel: +1-401-823-5200 www.bgasockets.com	D, P, T	BA, LA	CP > 0.5 mm CL > 200,000x OT = -40°C to +260°C FQ < 3.5 GHz @ -0.9 dB CF < 18 g CR < 2.8 A
AEM Holdings Ltd. 52 Serangoon North Ave. 4 Singapore 555853 Tel: +65-6483-1811 www.aem.com.sg	T	BA, LA, SM	CP > 0.4 mm CL > 50,000x OT = -50°C to +125°C FQ < 30 GHz CF & CR = CM
Andon Electronics Corporation 4 Court Drive Lincoln, RI 02865 Tel: +1-401-333-0388 www.andonelect.com	P	BA, LA, SM, TH	CP > 1.0 mm CL & FQ = CM OT = -65°C to +240°C CF = CM CR < 1.0 A
AQL Manufacturing Services 25599 SW 95th Avenue, Suite D Wilsonville, OR 97070 Tel: +1-503-682-3193 www.aqlmfg.com	T	BA, LA, SM, TH	CP > 0.5 mm FQ < (16 - 25) GHz CL, OT, CF & CR = CM
Ardent Concepts, Inc. 4 Merrill Industrial Drive Hampton Beach, NH 03842 Tel: +1-603-926-2517 www.ardentconcepts.com	D, T	BA, LA	CP > (0.3 - 0.6) mm CL > (100k - 500k)x OT = -40°C to +155°C FQ < (24 - 37) GHz @ -1dB CF < (11 - 30) g CR < 2.0 A
 Aries Electronics, Inc. 2609 Bartram Road Bristol, PA 19007 Tel: +1-215-781-9956 www.arieselec.com	B, D, P, T	BA, LA, SM, TH	CP > (0.3 - 0.5) mm CL > (10k - 500k)x OT = -55°C to +250°C FQ < (1 - 40) GHz @ -1dB CF < (15 - 110) g CR < (1.0 - 3.0) A
Azimuth Electronics, Inc. 2605 S. El Camino Real San Clemente, CA 92672 Tel: +1-949-492-6481 www.azimuth-electronics.com	D, T	BA, LA, SM	CP > 0.5 mm OT = -55°C to 155°C CL, FQ, CF & CR = CM
BeCe Pte. Ltd. Block 1, Yishun Street 23, # 01-09 Singapore 768441 Tel: +65-6257-2930 www.bece.com.sg	T	BA, LA	CP = CM CL = CM OT = CM FQ = CM CF = CM CR = CM
Bucklingbeam Solutions, LLC 16074 Central Commerce Drive, Suite A-102 Pflugerville, TX 78660 Tel: +1-512-670-3122 www.bucklingbeam.com	D, T	LA	CP > 0.15 mm CL, OT, FQ, CF & CR = CM
 Cascade Microtech, Inc. 2430 NW 206th Avenue Beaverton, OR 97006 Tel: +1-503-601-1000 www.cascademicrotech.com	D, P, T	BA, LA, SM	CP > (0.35 - 0.8) mm CL > (50 - 300,000)x OT = -45°C to +175°C FQ < (9.4 - 40.0) GHz CF < (15 - 55) g CR < (1.0 - 4.0) A



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Centipede Systems Inc. 41 Daggett Drive San Jose, CA 95134 Tel: +1-408-321-8201 www.centipedesystems.com	T	BA, LA, SM	CP > 0.3 mm CL > 500,000x OT < +160°C FQ = CM CF = CM CR < 2.0 A @ 150°C
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 Tel: +1-510-357-7900 www.contechsolutions.com	B, D, T	BA, LA, SM	CP > (0.2 - 0.5) mm CL > 500,000x OT = -55°C to +160°C FQ < (1.1-34.6) GHz @ -1dB CF < (19 - 39) g CR < (1.5 - 4.0) A
Custom Interconnects 2055 S. Raritan Street, Unit A Denver, CO 80223 Tel: +1-303-934-6600 www.custominterconnects.com	D, T	BA, LA, TH	CP > 0.5 mm CL > 500,000x OT = -60°C to +150°C FQ < 40 GHz CF = CM CR < 5.0 A
Emulation Technology, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-383-8480 www.emulation.com	B, D, T	BA, BD, LA, SM, TH	CP > (0.1 - 0.5) mm CL > (10k - 125k)x OT = -55°C to +130°C FQ < (3 - 30) GHz @ -1dB CF < (19 - 40) g CR < (0.05 - 4.0) A
Enplas Tesco, Inc. 765 N. Mary Avenue Sunnyvale, CA 94085 Tel: +1-408-749-8124 www.enplas-ets.com	B, D, T	BA, LA, SM	CP > 0.4 mm CL > (10k - 200k)x OT = -65°C to +150°C FQ = CM CF < (14 - 35) g CR < (0.5 - 1.0) A
 Essai, Inc. 45850 Kato Road Fremont, CA 94538 Tel: +1-510-580-1700 www.essai.com	T	BA, LA, SM, TH	CP > 0.3 mm CL > (20k - 250k)x OT = -40°C to +145°C FQ < 30 GHz @ -1dB CF < (15 - 40) g CR < (0.5 - 1.0) A
 E-tec Interconnect Ltd. Industrial Zone C Forel (Lavaux) CH-1072, Switzerland Tel: +41-21-781-0810 www.e-tec.com	D, P	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (100 - 10,000)x OT = -55°C to +125°C FQ < (17.7 - 38.3) GHz @ -1dB CF < 40 g CR < (0.5 - 3.0) A
Exatron, Inc. 2842 Aiello Drive San Jose, CA 95111 Tel: +1-408-629-7600 www.exatron.com	D, T	LA, SM	CP > 0.4 mm CL > (100k - 1,000k)x OT = -70°C to +200°C FQ < 40 GHz @ CM CF < (10 - 12) g CR = CM
Gold Technologies, Inc. 2360-F Qume Drive San Jose, CA 95131 Tel: +1-408-321-9568 www.goldtec.com	B, D, T	CM	CP > (0.4 - 0.5) mm CL > (20k - 1,000k)x OT = -55°C to +155°C FQ < (4.6 - 16.0) GHz @ -1dB CF & CR = CM
 High Connection Density, Inc. 820A Kifer Road Sunnyvale, CA 94086 Tel: +1-408-743-9700 www.hcdcorp.com	B, D, P, T	BA, LA	CP > (0.5 - 0.8) mm CL > (50k - 250k)x FQ < (4.4 - 10) GHz @ -1dB CF < (30 - 50) g OT & CR = CM

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High Performance Test 48531 Warm Springs Blvd., Suite 413 Fremont, CA 94539 Tel: +1-510-445-1182 www.hptestusa.com	B, D, T	BA, LA, SM	CP > 0.5 mm CL > (100k - 300k)x OT = -50°C to +150°C FQ < 3.0 GHz @ CM CF = CM CR < 5.0 A
 Interconnect Devices, Inc. 5101 Richland Avenue Kansas City, KS 66106 Tel: +1-913-342-5544 www.idinet.com/synergetix	D, T	BA, BD, LA, SM	CP > (0.4 - 0.5) mm CL > (250k - 500k)x OT = -55°C to +150°C FQ < (9.6 - 20) GHz @ -1dB CF < (17 - 85) g CR < (1.5 - 5.0) A
 Interconnect Systems, Inc. 759 Flynn Road Camarillo, CA 93012 Tel: +1-805-482-2870 www.isipkg.com	P	BA, LA	CP > 0.8 mm CR < 10 A CL, OT, FQ, CF = CM
 Ironwood Electronics 11351 Rupp Drive Burnsville, MN 55337 Tel: +1-952-229-8200 www.ironwoodelectronics.com	B, D, T	BA, LA, SM	CP > (0.25 - 0.4) mm CL > (2k - 500k)x OT = -70°C to +200°C FQ < (6 - 40) GHz @ -1dB CF < 50 g CR < (2.0 - 8.0) A
ISC Technology Co., Ltd. Keumkang Penterium IT-Tower F6 333-7 Sangdaewon-Dong, Jungwon-Ku Seungnam-City, Kyunggi-Do, Korea Tel: +82-31-777-7675 www.isctech.co.kr	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 200,000x OT = +150°C Max. FQ < 40 GHz CF < 50 g CR < 2.0 A
J2M Test Solutions, Inc. 13225 Gregg Street Poway, CA 92064 Tel: +1-571-333-0291 www.j2mtest.com	D, T	BA, BD, LA, SM	CP > 0.2 mm CL > 500,000x OT = -55°C to +150°C FQ < 17 GHz @ CM CF < 13 g CR = CM
Johnstech International Corporation 1210 New Brighton Blvd. Minneapolis, MN 55413 Tel: +1-612-378-2020 www.johnstech.com	D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (300k - 1,000K)x OT = -40°C to +155°C FQ < (3.0 - 40) GHz @ -1dB CF < (20 - 150) g CR < (0.8 - 6.7) A
Loranger International Corp. 303 Brokaw Road Santa Clara, CA 95050 Tel: +1-408-727-4234 www.loranger.com	B, D, T	BA, LA, SM, TH	CP > (0.25 - 0.4) mm CL = CM OT = CM FQ = CM CF = CM CR = CM
M&M Specialties 1145 W. Fairmont Drive Tempe, AZ 85282 Tel: +1-480-858-0393 www.mmspec.com	D, T	BA, LA, SM	CP > 0.3 mm CL > 500,000x FQ < 25 GHz @ -1dB OT, CF & CR = CM
Micronics Japan Co., Ltd. 2-6-8 Kichijoji Hon-cho, Musashino-shi Tokyo 180-8508, Japan Tel: +81-422-21-2665 www.mjco.jp	B, D, T	BA, SM	CP > 0.2 mm FQ < 40 GHz @ -1dB CL, OT, CF & CR = CM



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Mill-Max Manufacturing Corp. 190 Pine Hollow Road, P.O. Box 300 Oyster Bay, NY 11771 Tel: +1-516-922-6000 www.mill-max.com	P	SM, TH	CP > (1.27 - 2.54) mm CL > (100 - 1,000)x OT = -55°C to +125°C FQ = CM CF < (25 - 50) g CR < (1.0 - 3.0) A
Modus Test Pte. Ltd. 52 Ubi Avenue 3, # 03-29/30 Frontier Building Singapore 408867 Tel: +65-6748-9178 www.modustest.com	D, T	BA, LA, SM, TH	CP > 0.3 mm CL > 1,000,000x OT = +200°C Max. FQ < 20 GHz @ CM CF < 35 g CR < 5.0 A
 Multitest Elektronische Systeme GmbH Aeussere Oberaustrasse 4 D-83026 Rosenheim, Germany Tel: +49-8031-4060 www.multitest.com	D, T	BA, LA, SM	CP > (0.25 - 0.5) mm CL > (500k - 1,000k)x OT = -60°C to +200°C FQ < (0.5 - 40) GHz @ CM CF < (26 - 55) g CR < (1.8 - 4.6) A
OKins Electronics Co. Ltd. 6F, Byucksan-Sunyoung Technopia 196-5, Ojeon-dong, Uiwang-si Gyeonggi-do 437-821, Korea Tel: +82-31-460-3500 / 3535 www.okins.co.kr	B, D, T	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (10k - 100k)x OT = -55°C to +150°C FQ < (7.0 - 12.4) GHz @ -1dB CF < (7 - 15) g CR < (0.5 - 1.0) A
Paricon Technologies Corporation 421 Currant Road Fall River, MA 02720 Tel: +1-508-676-6888 www.paricon-tech.com	B, D, P, T	BA, LA	CP > (0.1 - 0.4) mm CL > 1,000,000x OT < 150°C FQ < 40 GHz @ -1dB CF & CR = CM
Phoenix Test Arrays 3105 S. Potter Drive Tempe, AZ 85282 Tel: +1-602-518-5799 www.phxtest.com	D, T	BA, LA, SM	CP > 0.4 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < 25 g CR < 3.5 A
 Plastronics Socket Company 2601 Texas Drive Irving, TX 75062 Tel: +1-972-258-2580 www.plastronics.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (5k - 20k)x OT = -65°C to +150°C FQ < 15 GHz @ -1dB CF < (7 - 50) g CR < (0.4 - 1.2) A
ProFab Technology Inc. 41817 Albrae Street Fremont, CA 94538 Tel: +1-925-600-0770 www.profabtechnology.com	D, T	BA, LA	CP > (0.26 - 0.45) mm CR < 7.0 A CL, OT, FQ & CF = CM
 Protos Electronics 1040 Di Giulio Avenue, Ste. 100 Santa Clara, CA 95050 Tel: +1-408-492-9228 www.protoelectronics.com	D, T	BA, LA, SM	CP = CM CL > 300,000x OT = -55°C to +135°C FQ < 22.3 GHz @ -1dB CF < 20.8 g CR < 4.0 A
Qualmax, Inc. IT Castle, 1-dong, 1101-ho 550-1 Gasan-dong, Geumcheong-gu Seoul, Korea 153-768 Tel: +82-2-2082-6770 www.qualmax.com	D, T	BA, LA, SM	CP < (0.4 - 0.5) mm CL < (200k - 500k)x OT = CM FQ < (9 - 25) GHz @ -1dB CF < (18.5 - 40) g CR < (1.0 - 4.0) A



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Rika Denshi Co., Ltd. 1-18-17, Omori-Minami, Ota-Ku Tokyo 143-8522, Japan Tel: +81-3-3745-3811 www.rdk.co.jp	D, T	BA, LA, SM	CL > (500k - 1,000k)x OT = -40°C to +160°C FQ < 36 GHz @ -1dB CF < (15 - 30) g CP & CR = CM
Robson Technologies Inc. 135 E. Main Avenue, Suite 130 Morgan Hill, CA 95037 Tel: +1-408-779-8008 www.testfixtures.com	B, D, P, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > 25,000x OT = -50°C to +150°C FQ < 30 GHz @ -1dB CF = CM CR < 3.0 A
RS Tech Inc. 2222 W. Parkside Lane, Suite 117-118 Phoenix, AZ 85027 Tel: +1-623-879-6690 www.rstechinc.com	B, D, T	BA, LA, SM, TH	CP > 0.35 mm OT = -55°C to +150°C FQ < (9 - 10) GHz @ CM CR < (1.0 - 15.0) A CL & CF = CM
Sanyu Electric, Inc. 6475 Camden Avenue, Suite 100 San Jose, CA 95120 Tel: +1-408-269-2800 www.sanyu-usa.com	CM	CM	CP > 0.2 mm CL = CM OT = -40°C to +150°C FQ < 40 GHz @ -1dB CF < (15 - 25) g CR < (4.0 - 5.0) A
 Sensata Technologies, Inc. 529 Pleasant Street, P.O. Box 2964 Attleboro, MA 02703 Tel: +1-508-236-3800 www.sensata.com	B	BA, LA, SM	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (10 - 25) g CR < 1.0 A
S.E.R. Corporation 1-14-8 Kita-Shinagawa Shinagawa-Ku Tokyo 140-0001, Japan Tel: +81-3-5796-0120 www.ser.co.jp	B, D, T	BA, LA, SM, TH	CP > (0.3 - 0.4) mm CL > (20k - 500k)x OT = -40°C to +150°C FQ < (5 - 20) GHz @ CM CF & CR = CM
Test Tooling Solutions Group Plot 234, Lebuh Kampung Jawa, FTZ Phase 3 Bayan Lepas, Penang 11900, Malaysia Tel: +60-4-646-6966 www.tts-grp.com	D, T	BA, LA, SM, TH	CP > 0.2 mm CL > 1,000,000x OT = -40°C to +150°C FQ < 20 GHz @ -1dB CF & CR = CM
3M, Electronics Solutions Division 3M Austin Center 6801 River Place Blvd. Austin, TX 78726 Tel: +1-512-984-1800 www.3mconnector.com	B, D, P	BA, LA, SM, TH	CP > (0.65 - 2.54) mm CL > 10,000x OT = -55°C to +150°C FQ = CM CF < (8.5 - 80) g CR < (0.5 - 1.0) A
Unitechno Inc. #2 Maekawa Shibaura Bldg., 13-9 2-Chome Shibaura, Minato-ku Tokyo 108-0023, Japan Tel: +81-3-5476-5661 www.unitechno.com	D, T	SM	CP > 0.4 mm OT = -40°C to +150°C FQ < (6 - 8) GHz @ CM CL, CF & CR = CM
Wells-CTI 2102 W. Quail Avenue, Ste. 2 Phoenix, AZ 85027 Tel: +1-480-682-6100 www.wellscti.com	B	BA, LA, SM, TH	CP > (0.4 - 0.5) mm CL > (3,000 - 10,000)x OT = -55°C to +150°C FQ = CM CF < (8 - 80) g CR < (0.5 - 2.0) A



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WinWay Technology Co. Ltd. 2F, No. 315, Minghua Road, Gushan District Kaohsiung 804, Taiwan Tel: +886-7-552-4599 www.winway.com.tw	B, D, T	BA, LA, SM	CP > (0.3 - 0.4) mm CL > (50k - 500k)x OT = -50°C to +150°C FQ < (0.2 - 14) GHz @ -1dB CF < (10 - 41.3) g CR < (1.5 - 3.0) A
 <b>YAMAICHI ELECTRONICS</b> Yamaichi Electronics Co., Ltd. 3-28-7 Nakamagome, Ota-Ku Tokyo 143-8515, Japan Tel: +81-3-3778-6111 www.yamaichi.co.jp	B, D, P, T	BA, BD, LA, SM, TH	CP > 0.4 mm CL = CM OT = -65°C to +150°C FQ < (2.7 - 6.9) GHz @ -1dB CF < (13 - 30) g CR < (0.5 - 1.0) A
Yokowo Co. Ltd. 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 www.yokowo.com	B, D, T	BA, LA, SM	CP > 0.3 mm OT = -55°C to +150°C FQ < 16 GHz @ -1dB CL, CF & CR = CM



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# INDUSTRY NEWS

(continued from Page 19)

## The 61st ECTC Increases Its Focus on 3D/TSV Technology

Each year, the Electronic Components and Technology Conference (ECTC) strives to offer its attendees an outstanding array of packaging technology information. This year's conference promises to be just as exciting this year as last year. It will be held in Lake Buena Vista, FL from May 31- June 3 at the Walt Disney World Swan and Dolphin Resort. Situated on 87 acres of beautiful lake front property, the resort is centrally located in Walt Disney World® Resort.

This year's program includes 41 technical sessions (eight of which are dedicated to 3D packaging and Si TSV fabrication, bonding, and reliability), 16 CEU-approved professional development courses, and a technology corner with more than 70 exhibitors. In addition to 3D, the conference has a high focus in embedded technologies and chip-package-interactions. All in all, more than 300 technical papers will be presented covering advanced packaging, modeling & simulation, optoelectronics, interconnections, materials & processing, applied reliability,

assembly and manufacturing technology, electronic components & RF, and emerging technologies. Special papers presented at the ECTC will be awarded the Intel Best Student Paper Award and best and outstanding paper awards.

## China WLCSP Names Senior VP of Strategic Development; Opens R&D Center in CA

It's been a busy month for China WLCSP Co. Ltd, provider of wafer level miniaturization technologies. In early January, the company opened an R&D center in Sunnyvale, CA to support the company's regional activities with OEMs and industry partners in the growing mobile handset market. And more recently, Vage Oganesian was named senior VP, Strategic Development.

"The US is a strategic market, which is experiencing solid growth in the high end mobile device market," said Wang Wei, CEO of China WLCSP. "We have several important customers and partners in this country, where we plan to play a leading role over the next few years."

Wangwei says Oganesian brings a global perspective and a history of successful technology advancement from previous positions including Tessera Technologies, where he was V.P. of R&D since 2005, and Shellcase Technologies.

"There is a definite synergy between China WLCSP's focus on the development and delivery of innovative technology and my own philosophy that strategic thinking, customer focus, and deployment of appropriate R&D resources can help a company realize the full potential of its vision for the future," said Vage Oganesian.

Oganesian will report to China WLCSP's CEO, Wangwei, and be responsible for the company's business and technology vision and direction for its continuing innovation in, and development of, miniaturization technologies for wireless, consumer and computing electronic devices. He will also help set the corporate strategy and develop the technology roadmap.

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## CEA-Leti Ramps up 300mm Line Dedicated to 3D-Integration

Grenoble-based research institute, CEA-Leti, officially ramped one of Europe's first 300mm lines dedicated to 3D-integration applications in a ceremony on January 18, 2011. By adding this technology to its existing 300mm CMOS R&D line, Leti now can offer heterogeneous integration technologies to customers on both 200mm and 300mm wafers.

The new line, dedicated to R&D and prototyping, includes 3D-oriented lithography, deep etching, dielectric deposition, metallization, wet etching and packaging tools that will be available for Leti's customers and partners around the world. It will allow Leti to apply its 3D-integration generic processes on 300mm wafers.

"This extension offers important new capabilities to equipment manufacturers and other Leti partners," said Laurent Malier, CEO of Leti. "Together we will demonstrate 3D and heterogeneous integration technologies on 300mm wafers."

(continued from Page 41)

of each wafer and provides the data for the wafer handling robot end effector.

Similarly, the aligner, which has a Bernoulli movable chuck, makes no contact with the wafer surface. To prevent the wafers from shifting positions after alignment, the aligner chuck and the end effector perform a "handshake" whereas the vacuum hold from the chuck is not released until the hold from the end effector is in place.

## Conclusion

The combination of Bernoulli and CAT non-contact chucks along with linear scan wet etching makes an excellent combination for wet processing and handling ultrathin freestanding wafers. The ability to use virtually any chemistry to interact with any substrate material enables the systems to process most materials of interest, all while retaining the ability to handle ultrathin wafers with severe warpage or distortion. In addition to packaging applications, the systems are being used to etch or thin InP, Ge, GaAs, Si, polysilicon, glass, and quartz, among others. Substrates of odd shapes and within a large range of size and thickness can also be processed. These methods provide a new way to wet thin and handle ultrathin wafers in a more precise, efficient, and environmentally friendly manner. <sup>Sp</sup>

## Acknowledgements

\*WaveEtch™, LinearScan™, CAT™ Chuck and \*\*DynamicConfinement™ are trademarks of Materials and Technologies Corp. (MATECH)

\*\*\*Mechatronic Bernoulli End Effector  
Ricardo Fuentes is the founder and president of Materials and Technologies Corp., (MATECH), 641 Sheafe Road, Poughkeepsie, NY 12601, United States; phone (845) 463-2799, e-mail [info@motech.com](mailto:info@motech.com).  
The author is thankful to Mechatronic Systemtechnik GmbH, Tiroler Strasse 80, 9500 Villach, Austria, for kindly providing some of the images in this paper.

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Laurent Malier and Susumu Kaminaga, President of SPP and chairman of SPTS. Mr Kaminaga gave Laurent Malier a present to thank him for their collaboration on the 300mm Line.

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# TEST PATTERNS



## Upgrading ATE Systems for Known Good Die Testing

By Paul Sakamoto, Contributing Editor [*DFT Microsystems*]

**O**ne of the great “unsung heroes” of Moore’s Law is the ever-shrinking package around the die. After all, it’s hard to have tiny, hand-held digital devices if the silicon is packaged in FPGA packages. Today, that package has been reduced to the point that it is becoming a coating and some bumps on the die. Sometimes, it is a stack of these die that are connected with TSVs (Through Silicon Vias). In all cases, it is now a requirement that full-performance be guaranteed during wafer level test. This need may bring rise to many challenges for some companies. The one that we will address in this article is the need to upgrade the ATE used in the wafer test area.

A common practice over the years has been to partition device testing for SoC (System on Chip) devices so that older, lower-performance ATE is used for wafer test and newer, high-performance equipment is used for post-assembly test. This was largely because wafer tests, particularly speed and analog tests, were executed below specification to allow for the difficulties of creating a high-fidelity probe contact to the die. Slow gains in wafer test performance were made over the years to help eliminate waste at the post-assembly, final test level. Today, many of these older ATE systems are still able to test most of the device parameters, particularly the bulk of the digital pins for wireless applications, but they fall way short in the areas of HSIO (High Speed I/O), RF and lower speed analog. You can newer products, upgrading old wafer test systems with OEM help is seldom an option. On the other hand, many new consumer devices have such a low cost structure that buying a new high-end system to test them is out

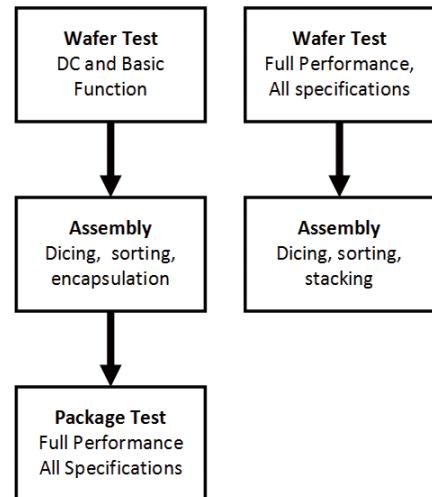
of the question. A possible solution is to add an after-market upgrade.

Do-it-yourself upgrading of ATE has been happening ever since the first systems were shipped over 40 years ago. The popularity of this activity has not been all that broad, however, due to the lack of sufficient economic pressure. In the past, speed of development and throughput for chip test was the lead factor above test cost. Today the focus is changing somewhat to cost of acquisition of the equipment taking a much bigger role.

To illustrate the difference in approach between then and now, consider the following hypothetical conversation. The Boss says, “Bill, do we have to buy the new Blartfast 2000 ATE system to test the new part? It costs \$2 million! Can’t you just modify the old Blartfast 1990?” Bill than responds, “Sure. Just give me \$1M, five engineers and about a year. It’ll be fun. The instrument sales guy will like it too.” Of course, the Boss than says, “Never mind. Write up the Blartfast 2k requisition.” Today, the conversation would be more like, “Bill, you have two months and \$200k to get the new parts ready to test. If you can’t get it done, your job goes to India.” Faced with this, Bill is now ready to begin home remodeling of his ATE.

So, what are some typical applications for DIY (Do It Yourself) ATE upgrades? SerDes I/O pins are a good target. Many new mobile devices use the MIPI protocol to communicate between cameras and the rest of the phone using just a few wires to send a lot of data. Other SerDes test challenges include HDMI, DP (display port), USB 3.0, PCIe, MDDI, and SATA. What makes these great candidates for the addition of a discrete instrument? They

### Legacy Test Flow      Known Good Die (KGD) Test Flow



all consume relatively few device pins, have very high-speed requirements (GHz) and are often co-located on devices where the fundamental data rate of the other few hundred pins is <<200MHz. There is usually no viable OEM upgrade available (if there is, you should consider it). The other factor is to look at what the savings amount to, and in most of these cases it's the difference between a \$100k instrument or a \$1.5M tester with options.

Some will argue that this kind of tester upgrade has poor throughput, but I would suggest that this is “old-school” thinking and that modern instrumentation is often very competitive in speed of analysis. For many analog tests, it’s actually superior due to its ability to locally process captured test data.

For all of you test engineers that are frustrated designers and system integrators, rejoice! Your time has come to be the hero, or at least keep your job, and make your old testers new again with home-brew testing.

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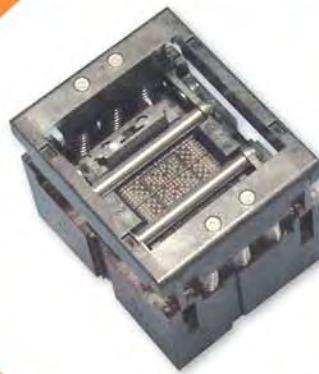
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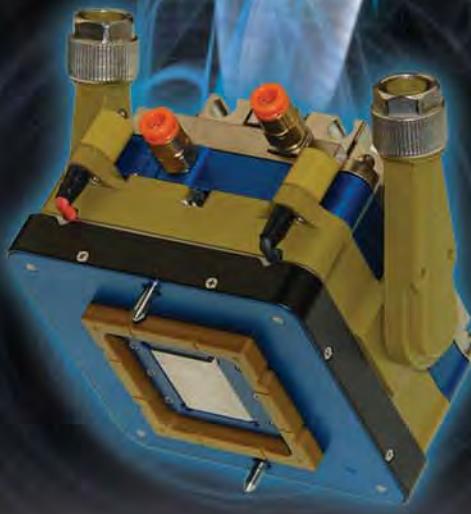


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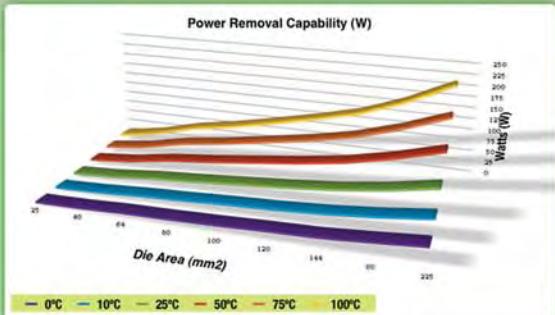
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