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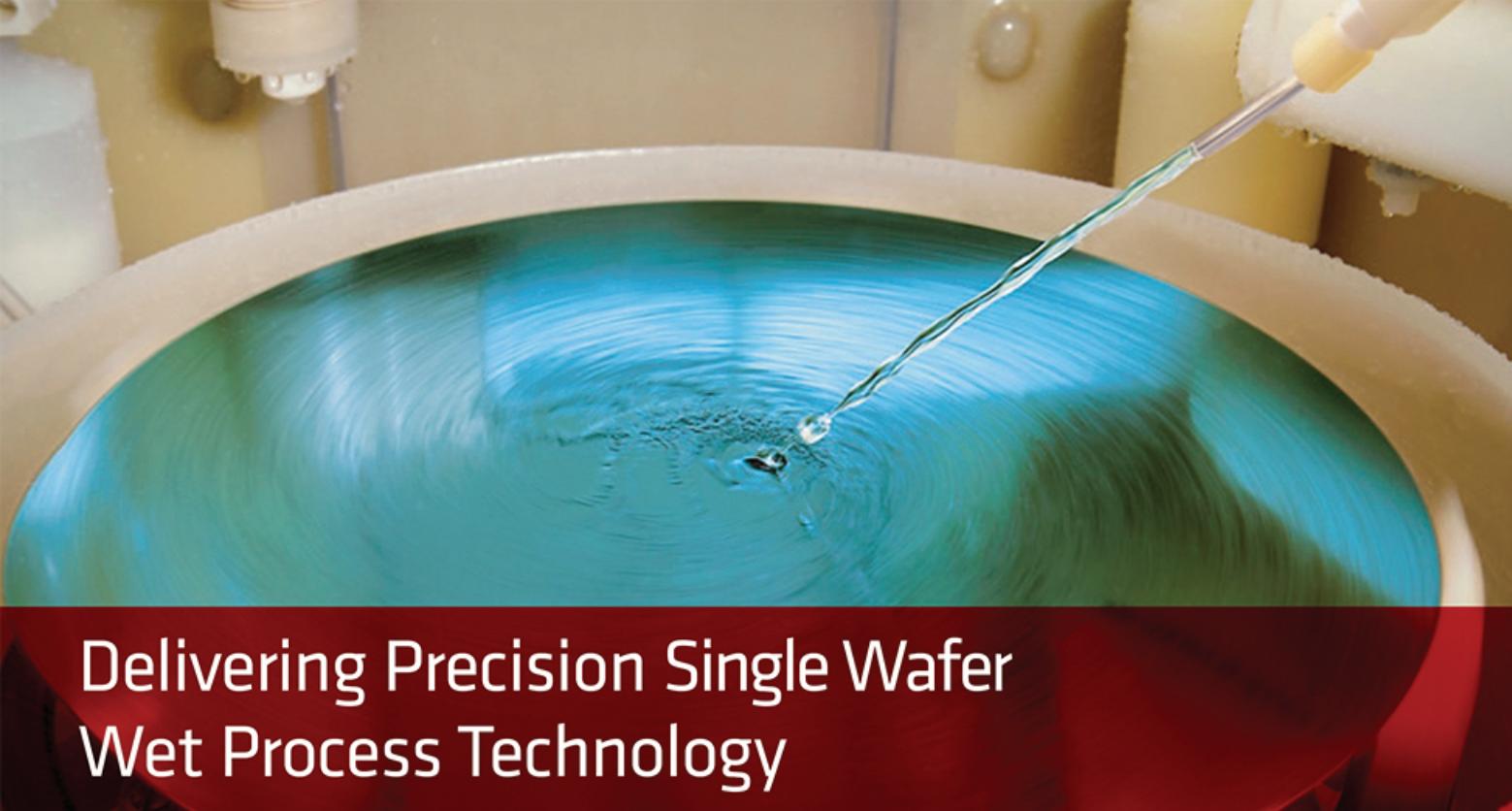
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- Interferometry for metrology applications
- Contactor and package design effects on crosstalk
- Non destructive 3D X-ray imaging for failure analysis





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The photo shows a close-up side-view of the ablation area inside SUSS MicroTec's ELP300 Excimer Laser Stepper. A polyimide-coated silicon wafer is positioned beneath a stationary projection lens (not visible). Bright ablation plumes are visible on the wafer's surface as polyimide is directly removed by the projected mask pattern and with sub-micron depth accuracy. Excimer laser ablation is a technology enabler and an attractive alternative to photolithography.

Cover photograph courtesy of SUSS MicroTec SE.

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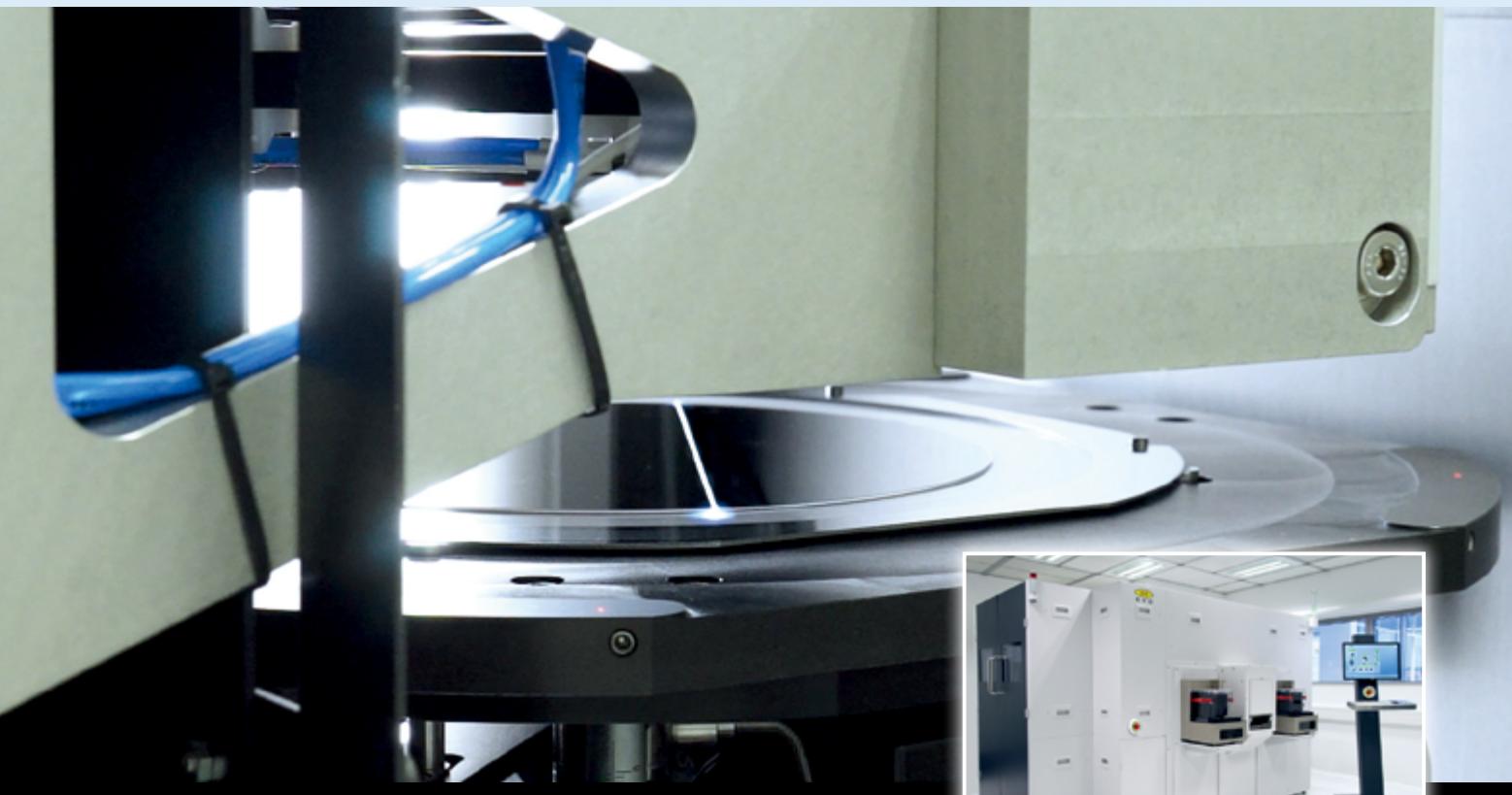
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STAFF

Kim Newman Publisher

knewman@chipscalereview.com

Lawrence Michaels Managing Director/Editor

lmichaels@chipscalereview.com

Debra Vogler Senior Technical Editor

dvogler@chipscalereview.com

CONTRIBUTING EDITORS

Roger H. Grace - MEMS

rgrace@rgrace.com

Dr. Ephraim Suhir - Reliability

suhire@aol.com

Steffen Kröhner - Advanced Packaging

Steffen.Kroehnert@nanium.com

EDITORIAL ADVISORS

Dr. Andy Mackie (Chair) Indium Corporation

Dr. Rolf Aschenbrenner Fraunhofer Institute

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Dr. Arun Gowda GE Global Research

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Advertising Production Inquiries:

Lawrence Michaels

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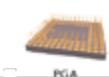
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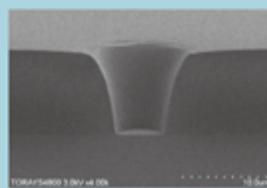
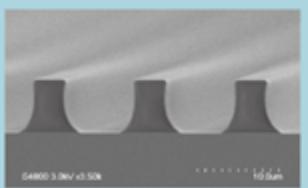
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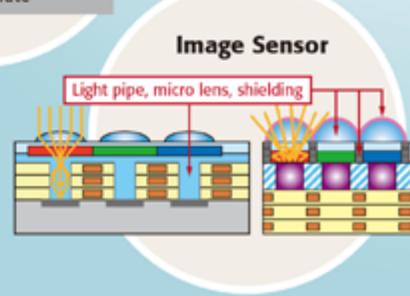
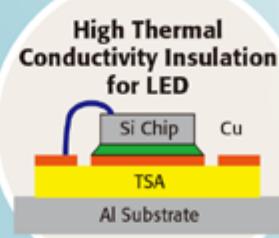
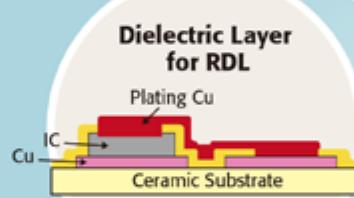
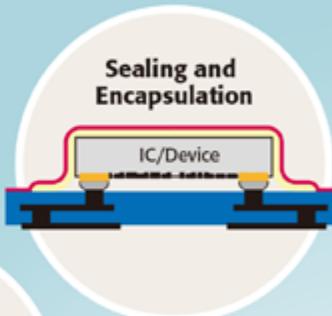
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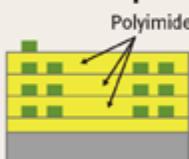
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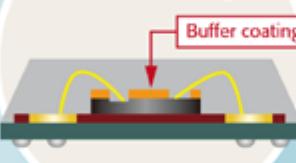
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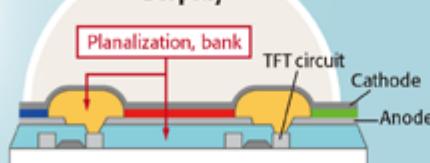
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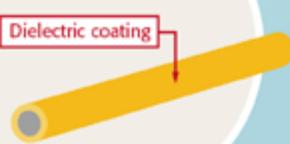
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Photonic packaging: moving from component- to wafer-level packaging

By Peter O'Brien [[Tyndall National Institute](#)]

Packaging of integrated photonics or photonic integrated circuits (PICs) is evolving. This evolution is driven by the emergence of new applications in markets that have extremely high-volume requirements, typically millions of components per year. Applications include, high-speed communications for data centers, sensors for automotive such as LIDAR, medical, and point-of-care diagnostics, and the growth of the Internet of Things (IoT).

There have been significant developments to realize cost-effective PIC device fabrication processes [1], but there now exists a packaging bottleneck that is impeding the growth of these markets. Key challenges to be overcome include low-cost optical fiber and micro-optical packaging processes that provide high coupling efficiencies (e.g., <1dB loss per optical interface), the ability to package large numbers of optical channels per chip (e.g., >100 channels per optical interface), the integration of different PIC platforms (e.g., Si, InP and SiN), and the hybrid and heterogeneous integration of photonic and electronic devices in a common package. Challenges also remain in providing high-speed electrical packaging as required for communication systems with bandwidth requirements of >100G. In addition, the drive to develop highly integrated photonic and electronic components in a single package adds to the difficulty of efficiently managing thermal loads. Critically, the technologies developed to overcome all these challenges must be implemented in high-volume manufacturing environments, using cost-effective materials and packaged using equipment that operates using automated machine vision (passive) alignment processes.

Existing photonic packaging processes typically rely on component-level packaging, where optical and electrical connections are assembled after the photonic device has already been placed in a mechanical package, as seen in **Figure 1**. This serial

type process flow has limited throughput, and scale-up in manufacturing depends directly on the number of packaging machines. Historically, such serial process flows have been acceptable for low-volume

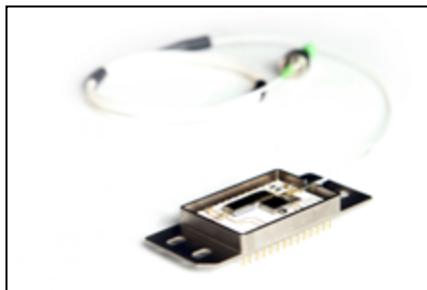


Figure 1: Existing photonic packages rely on component-level serial processes, with relatively long process times that are difficult to scale (e.g., optical fiber attachment). There is a need to move to wafer-level parallel packaging processes that can offer 10–100 times reduction in process times.

high-value applications, such as fiber optic telecommunication that requires extremely high reliability and long lifetimes. The typical packaging for such a telecom component involves: 1) The photonic device assembled in the package; 2) Electrical connection using gold ribbon wire bonding; 3) Active alignment of the optical fiber to minimize insertion loss; and 4) Hermetic sealing of the mechanical housing in an inert atmosphere. This serial packaging approach, however, cannot meet the cost and volume demands of emerging mass markets in photonics.

The advent of the PIC is helping to address the packaging bottleneck. For example, silicon-based PICs offer many technological advantages, combining high levels of functionality in a single chip that can be applied across multiple markets, from communications to medical diagnostics and sensing [2]. The high refractive index of the silicon optical waveguide results in a highly compact optical system, with dimensions on the order of 1cm² or less. Although a separate light source has to be integrated into the Si-PIC, as silicon is an indirect

band gap semiconductor and does not emit light, integrated Si-PICs can now perform the essential functions for a complete photonic system, namely, light generation, transmission, modulation and detection. Critically, using silicon for photonics enables us to benefit from the well-established process flows and manufacturing equipment developed by the CMOS semiconductor industry. It is possible to use CMOS wafer-scale assembly and packaging processes to overcome the throughput limits of existing packaging processes, ensuring photonic systems meet the demands of emerging mass markets.

Optical packaging

Optical packaging typically involves bonding of optical fibers to the photonic device, where single or fiber arrays can be used. The conventional packaging process uses an active alignment procedure where the coupled optical power is continuously measured and maximized, and the fiber is fixed in position using a laser welding or UV epoxy curing process—sub-micro alignment tolerances are required. This process is performed at the component or package level, and suffers from significant throughput limitations, with cycle times on the order of minutes to tens of minutes per package, depending on the complexity of the photonic device to the assembled. Wafer-level packaging has the ability to overcome these limitations, where parallel alignment processes can achieve significantly higher throughputs: seconds per device. Eliminating the need to bond fibers to the photonic chip through the use of micro-optics assembled on-wafer offers one solution. At the Tyndall Institute, we have developed a process to assemble micro-optics on the Si-PIC, where the sub-micron alignment and bonding processes can be performed at wafer level, with devices singulated after micro-optic assembly. The Si-PIC chip incorporates surface grating couplers, which direct light into the optical waveguide, and

when micro-optics are bonded over these gratings, light can be precisely focused to the grating region to achieve high coupling efficiency. This style of optical interconnect is ideal for low-cost photonic packages, such as pluggable transceivers for data centers or disposable biosensors for medical diagnostics. This type of high-volume and low-cost interconnect will become a viable alternative to the dominant fixed-fiber design.

Though fiber attachment is expected to remain a key optical packaging process, it must be modified to reduce cycle time and make it more cost-effective. One approach is to use evanescent coupling. In this design, light is coupled between the optical fiber and PIC waveguide via an optical interposer, much like an electrical interposer is used to interface between adjacent electronic devices. Structuring the PIC at the wafer level to include an evanescent coupling element is relatively straightforward, and when bonded on top of the optical interposer via a flip-chip process, enables light to efficiently transfer between the PIC and interposer waveguides. An added advantage of the evanescent technique is the ability to form an optical connection at any point on the PIC surface, rather than at the PIC edge or facet, as with standard fiber coupling. Optical interposers can be fabricated in glass, with embedded waveguides interfacing between the optical fibers and PIC. Although at a relatively early stage of development, both micro-optics and evanescent coupling indicate the benefits of using wafer-level processes to ease the burden of optical packaging.

Electrical packaging

Electrical packaging for photonics is often overlooked, but can be the largest contributor to material costs within the package. As the demand for higher operating frequencies rises, there is a need to integrate the electronics closer to the PIC. In some cases, electronic and photonic functionality can be integrated in the same device, although hybrid integration using 2.5 and 3D integration processes tend to be the preferred technology (see **Figure 2**). A number of photonic foundries now offer copper pillar processes, enabling electronic ICs, such as modulators and amplifier chips,

to be directly integrated into the PIC. This close integration supports extremely high-frequency operation of the photonic-electronic system. However, unlike an electronic system, photonic devices can

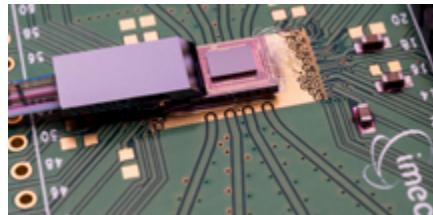


Figure 2: 3D integration of an electronic IC (e.g., modulator driver) on a silicon PIC. Copper pillars with solder caps enable flip-chip integration of the electronic IC on the PIC. Also shown is a planar optical fiber array bonded to the PIC.

be severely impacted from heat generated by the electronic chip, especially if the photonic device has wavelength-sensitive functions such as switches, multiplexer and demultiplexer elements. 2.5D integration can alleviate this problem because it can thermally isolate devices. They also offer the potential to combine both optical and electrical functionality in the same interposer. If a glass interposer is used, optical waveguides can be defined in the glass substrate using processes such as femto-second laser inscription or ion diffusion to modify the local refractive index. This type of dual functioning interposer is under development by a number of academic and industrial research groups, and is expected to become a commonly used technology for PICs that have complex electrical and optical functionality.

PIXAPP: photonic packaging pilot line

Integrated photonics is recognized to be a strategically important technology, much like integrated electronics was 40 years ago. The technology is at an early stage of development and requires support from governments and publicly funded agencies. Initiatives such as Pilot Lines in Europe and AIM Photonics in the United States have been established to support the growth of the integrated photonics ecosystem. These initiatives support the development of supply chains, help prepare technology roadmaps,

offer advanced training for the future workforce, and provide low-to-medium volume manufacturing services.

The European Union, through its Horizon2020 programme, has funded a number of photonic pilot lines, including a photonic packaging pilot line coordinated by the Tyndall Institute. Called PIXAPP, the packaging pilot line provides users with a range of advanced photonic and electronic packaging capabilities, with the ability to scale manufacturing to medium volumes [3]. Target markets include communications, biomedical devices, and sensors. PIXAPP is strongly focused on offering standardized packaging technologies, and is working with its global partners to establish a detailed set of packaging design rules and technology roadmaps. Design rules, when implemented at an early stage of product development, deliver cost-effective manufacturing processes, avoiding the need to customize. Another objective of PIXAPP is to provide hands-on training, with the first course set for January 2018, offering a unique opportunity to engage in practical photonic packaging processes. PIXAPP is strongly focused on offering standardized packaging technologies, and is working with its global partners to establish a detailed set of packaging design rules and standards. As in the electronics industry, the photonics industry needs to move to design standards if it is to capture the opportunities of large and growing markets.

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Biography

Peter O'Brien received his BAMod (Physics) and PhD from Trinity College Dublin, and U. College Cork, respectively; he is Director of the PIXAPP Pilot Line and Head of Packaging Research at Tyndall National Institute; email peter.obrien@tyndall.ie

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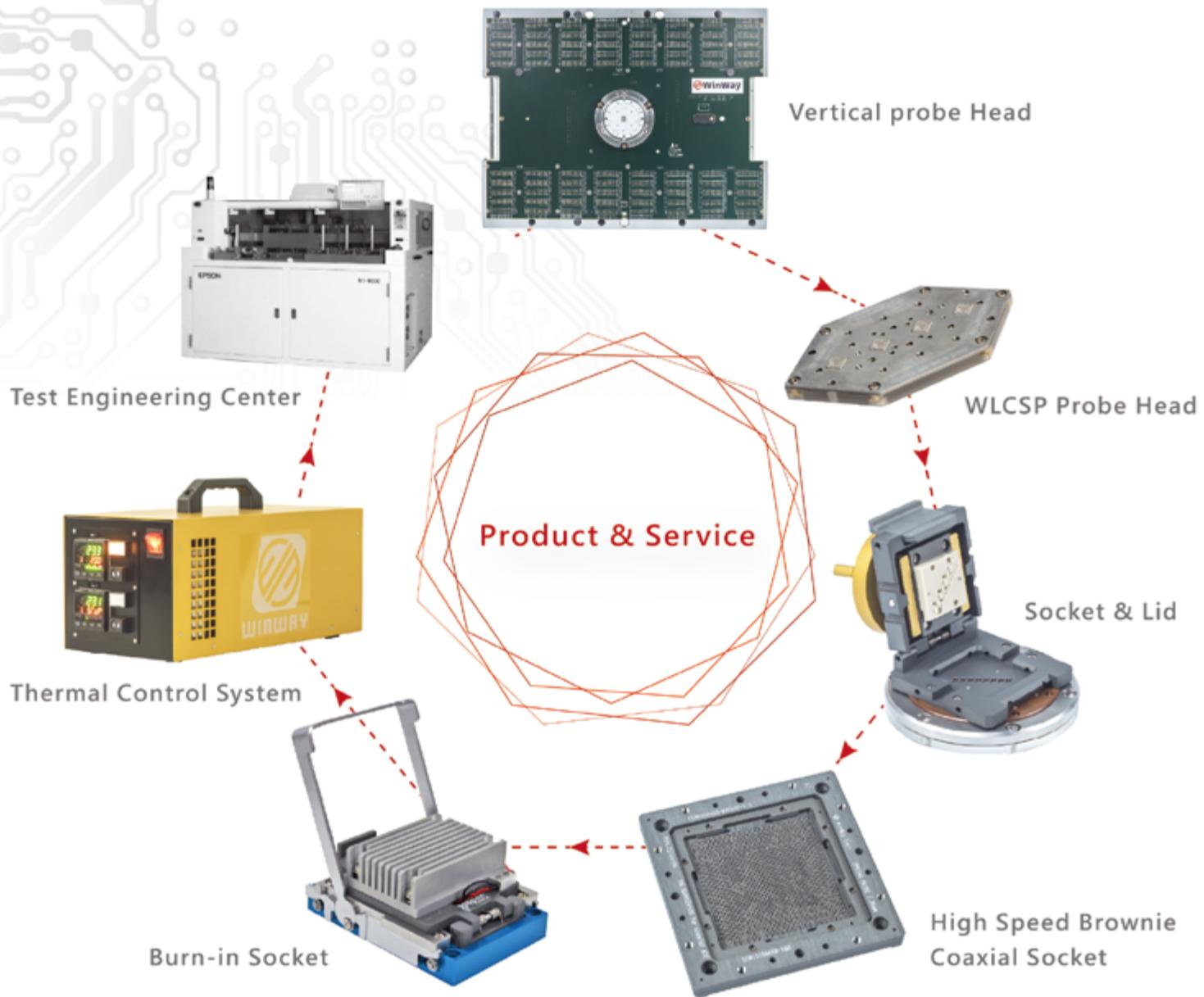
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Excimer laser ablation for microvia and fine RDL routings for advanced packaging

By Habib Hichri, Markus Arendt [*SUSS MicroTec Photonic Systems, Inc.*]

Excimer laser ablation is a direct etching process using high-energy pulses at short wavelengths that allows patterning of most polymers at minimal thermal impact through bond breaking. Metal layers of $>1\mu\text{m}$ in thickness serve as a stop layer, so underlying circuits are not affected by the excimer laser ablation. With this type of patterning technology, the advanced packaging industry gets access to materials that do not require photo patterning and allow a wider range of options for coefficient of thermal expansion (CTE) matching in the package. A tool, consisting of a high-power excimer laser source, a reticle-sized laser mask, and reduction projection optics on top of a state-of-the-art wafer stepping stage enables the accurate and cost-effective replication and placement of high-resolution circuit patterns. We will explain the excimer laser technology and its application for drilling microvias and trenches that are used in different packaging applications.

The high-density structuring challenge

Every type of advanced package, including chip-on-chip, wafer-level packages (WLP; e.g., 2.5D), chip-on-chip stacking, and embedded IC, all have a need to structure thin substrates, redistribution layers, and other package components at high resolution with smaller features sizes and tighter pitches. A very common example is drilling vias down to contact pads for applications like fan-in or fan-out WLP (FOWLP). Another emerging example is trenching to form embedded connectors in thin substrates or interposers. When using organic dielectrics, these structures are usually created by photolithography, using an ultraviolet (UV) light source with a photomask, or by laser direct imaging (LDI). These photoimageable materials, such as polyimides (PIs), polybenzoxazoles (PBOs) and epoxies, face CTE mismatch,

and pattern integrity control through developing and curing. This causes stress damage between these materials and the chips, resulting in higher warpage, and finally, impacting the reliability of the package. Furthermore, these materials have limitations in the resolution and via wall angle that they can support. In the case of vias for example, this limits the minimum achievable diameter and interconnect density, as well as their practical aspect ratios to values <1.5 . Devices that are already seeing an impact are those involving larger dies, higher I/O densities, thinner Si chips and substrates, and, obviously, any high heat load applications. Other challenges in this multi-step process involving developers and other wet chemicals are the increasing cost-of-ownership (CoO) associated with these chemicals, as well as their safe handling and disposal to support a greener process. A very attractive alternative to photolithography would be a technique that can directly structure PIs, PBOs and epoxies at even higher resolution than today's bleeding edge packages, and allows a wider material selection to contain the CTE issue, at reduced cost. Excimer laser ablation now provides that alternative.

Excimer laser ablation process

The laser ablation of thin film polymers is in principle not a new technology for wafer-level packaging. The laser ablation of polymers was first reported by Srinivasan, et al. [1] in 1982. Low speed and high cost were the major barrier for further developments thirty years ago. But the lithographic approach of excimer laser systems using quartz masks on stepping/scanning platforms has improved this technology to overcome the limited throughput.

Excimer laser ablation is a one-step, dry-etch patterning process that differs from solid-state laser ablation in that the excimer process is based on photo-chemical (photolytic) bond breaking; the solid-state

process relies on heat (pyrolytic), melting and evaporation to ablate polymers [2-3]. This "cold ablation" allows material removal without damaging surrounding areas, and no cracks or heat-affected zones are observed.

When a high-energy laser pulse is focused onto a material so that the intensity (which is measured as the fluence) is above a material-dependent threshold value, the high-energy ultraviolet photons directly excite electrons and break interatomic bonds. This threshold is quite important because it can be used to structure polymers on top of inorganic materials like metal without destroying the metal underneath because the threshold of metals is mostly very different to the threshold of dielectric materials. Along with the subsequent shock wave, this causes material to be ejected at high velocity in the form of mostly gaseous organic byproducts, and sometimes as fine powder. Because a typical excimer laser pulse duration is around 30ns, the interaction with the material occurs very rapidly resulting in little time for thermal transfer in the material.

Post-ablation cleaning

Excimer ablation of polymers produces little (to no) heat affected zone (HAZ), and $>90\%$ of the ablated material evaporates. The remaining portion results in the generation of carbonaceous debris that will be landing back on the surface of the dielectric. For these, a cleaning process is essential to eliminate any interference of the debris with the subsequent process steps such as seed layer deposition and plating.

The most common and recommended cleaning process post ablation is cleaning with O_2 plasma or desmear. **Figure 1** shows post-ablation and post- O_2 plasma cleaning for a via patterned by excimer laser. Another alternative to O_2 plasma cleaning post ablation is the use of a protective layer (or sacrificial layer) that will be coated in a thin film ($1-2\mu\text{m}$) on top of the dielectric prior to ablation. The sacrificial layer is a UV-

absorbent material that is water soluble. The ablation process will ablate the sacrificial layer and the dielectric and any debris generated during the ablation process will be recast on top of the sacrificial layer. After ablation, the wafer is subject to water spray that dissolves the sacrificial layer and the debris will be carried away with the water. **Figure 2** shows the results of using a sacrificial layer as a way to remove debris.

Material structuring with excimer laser ablation

Excimer laser ablation is a dry-etch process that removes material with each pulse applied. The amount of material removed – or etch rate – is dependent on the material and the fluence (energy), and can vary from 50nm per pulse for low fluences of 100mJ/cm^2 up to over 1000nm per pulse for high fluences of $>1000\text{mJ/cm}^2$ (**Figure 3**). The ablation rate is nearly constant for different geometry sizes and is not affected by the depth of the structure (**Figure 4**), which can vary from 1 μm up to more than 100 μm . This allows precise depth control and enables the creation of staggered features or blind holes. The fluence can be selected for process optimization and determines the desired sidewall angle for an application, which ranges from around 50deg for lower fluences up to 83deg with the highest possible fluence of around 1300mJ/cm^2 .

Excimer laser ablation is suitable for patterning a wide variety of materials, such as polymers, dielectrics, thin-metal layers on top of polymer (<600nm), epoxies, epoxy mold compound (EMC), nitrides and other materials. It allows using non-photosensitive materials, some of which offer better thermal and mechanical properties (i.e., lower CTE and residual stresses, higher Tg and thermal stability). With the use of excimer laser ablation, inorganics such as SiN and thin metals with layer thicknesses <600nm on top of a polymer can be structured. When ablating thin metal, the photochemical process happens in the top layer of the underlying polymer, and the created shock wave causes the metal layer on top to be ejected. Ablating metals can be used for seed layer removal in a very fast and cost-efficient way of up to 100WPH because only one pulse is needed. In contrast, a metal layer of $>1\mu\text{m}$ thickness serves as a stop layer for the excimer pulses, and the shock wave that is created is absorbed in the metal layer.

Excimer lasers are available with 5-10 times higher power (300W) than solid-state

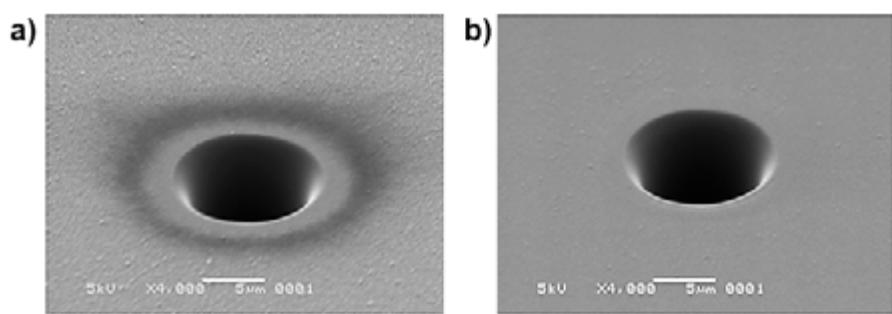


Figure 1: Post-ablation cleaning using O_2 plasma a) post ablation, and b) post- O_2 plasma cleaning. Material is HD4100 (HD Micro).

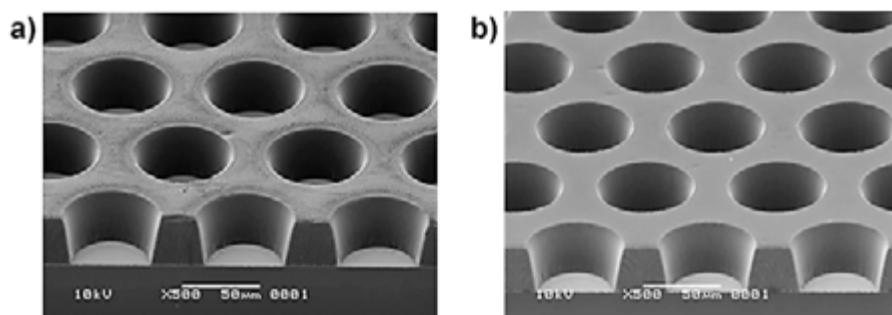


Figure 2: Post-ablation cleaning using a sacrificial layer coated prior to ablation and removed by water spray post ablation: a) top surface post ablation, and b) top surface post water spray. Material is FCPI2100 (FujiFilm).

laser systems, and therefore are capable of forming a large rectangular area beam. This has the advantage of being compatible with the use of standard photomask reticles (usually in 7" size, at similar prices as conventional UV stepper reticles), and to operate the system in a step-and-scan or step-and-repeat mode like any other UV stepper. For the light blocking metal on the reticle, Al is most suitable on account of it is a very high threshold level that makes the mask stable for a long production cycle time. For high resolution, the system uses a projection lens with reduction optics to project the image of the photomask on the wafer (2.0X, 2.5X, and 5X are available). The schematic of the excimer laser stepper is shown in **Figure 5**.

The ablation field size and shape is usually customer specific and based on the available power from the laser, the die or package size, and the required fluence. The reduction projection lens amplifies the energy from the beam delivery system by the square of the reduction factor (i.e., 6.25 for a

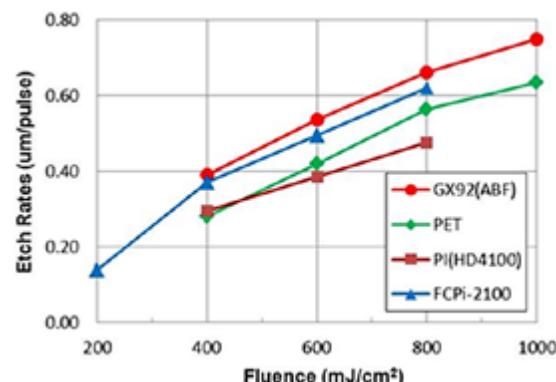


Figure 3: Example of ablation rates in ABF (GX92), PET, PI (HD4100) and FCPI-2100 (Fuji film) as a function of fluences.

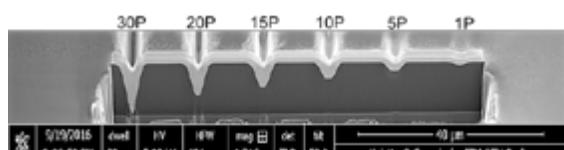


Figure 4: Ablation profile in low-temperature polyimide vs. number of pulses [4].

2.5X reduction optics) to achieve the higher fluence level required to ablate the material at the substrate plane. The throughput for such a system is mostly defined by the thickness of the material that determines the number of pulses required. Furthermore, the etch

rate of a specific material, the fluence, the power of the laser system, and the selected reduction factor influence the throughput. Like any mask-based system, the throughput is independent of the number of features ablated in a specific field, and therefore much higher compared to a printed circuit board (PCB) drilling system with solid-state lasers.

Excimer laser ablation results

The main requirement for a successful ablation is the absorption of the UV light of the laser system by the polymer. Multiple materials were coated on SiO_2 wafers either by spin coating or lamination processes, and exposed to an excimer laser using a mask with different features' sizes and shapes (vias or trenches). The following figures demonstrate the capability of an excimer laser to ablate vias and trenches in different materials. **Figure 6** [4] shows a via with a 5 μm diameter ablated in 15 μm thick BCB with an aspect ratio of 3:1.

Figure 7 shows the excimer laser resolution capability to achieve 2/2 μm L/S in dielectric material. The material used for resolution is a photosensitive material from HD Microsystems. **Figure 8** shows the capability of using the excimer laser ablation to generate vias and RDLs without any intermediate process steps by just exchanging the mask pattern. With the reduced number of process steps, the cost-of-ownership (CoO) can be significantly improved. **Figure 9** shows a trench formed by excimer laser, plated, and planarized using the chemical mechanical planarization (CMP) process. The CMP process was landed on the seed layer, which was later removed using an excimer laser.

Electrical and reliability test

The electrical performance and reliability of the structures created by excimer laser ablation was validated in various test series. In one of the yield evaluations, a daisy chain design was used [4]. The linewidth in the design is 5 μm and the via diameter is also 5 μm . Each chain contains 960 vias. The average resistance of a complete chain is in the range of 150 Ohms.

Figure 10 shows a yield map of a 200mm wafer where the daisy chains were ablated in a low-temperature cured (230°C) polyimide (LTC9320, Fuji Film), which is commonly used for RDL generation on temperature-sensitive reconfigured wafers. Each green

mark is a functional chain and a red mark indicates an open circuit in the chain. The higher numbers of defective chains at the edge are related to the edge bead removal of the polymer.

Another reliability test involved excimer laser structuring of non-photo dry film Ajinomoto Build-up Film (ABF). Data was collected for microvia (8 μm) and trenches (5/5 μm line/space) in ABF material patterned by an excimer laser on a glass panel [5]. The microvia successfully passed the thermal cycling (4300 cycles at -55°C [15mins] to 125°C [15mins]) and bHAST test (130°C, 85%RH, 5.0V) for two pitches of 20 and 40 μm (**Figure 11**). The 10/10 μm line/space traces enabled by the excimer laser were also able to pass the thermal shock test (-55°C [1min] to 125°C [1min]) for 1000 cycles. **Figure 12** shows the reliability results for 1000 cycles of thermal shock for daisy chain structures with pitches ranging from 20-40 μm . The results are comparable to photo-definable polyimide.

Today's use in advanced packaging

Excimer laser ablation systems have been around more than 30 years, and more than 100 systems have been installed since then. More and more companies in advanced packaging from both industry and research, use excimer laser ablation; among them are IBM, Fraunhofer IZM, and Georgia Tech. Qualification for high-volume manufacturing (HVM) has been successfully completed by an industrial customer. Various material suppliers have developed mostly non-photosensitive resists that show high ablation rates with almost no debris, to provide users access to the cost and reliability advantages of excimer laser ablation.

One of the major drivers to investigate excimer laser ablation is a reduced number of process steps compared to photolithography, where post-exposure develop and UV curing can be eliminated. In comparison to solid-state laser ablation, there is a significant throughput advantage through mask-based ablation, while the laser source itself comes at a comparable cost level of around \$2,000 per Watt.

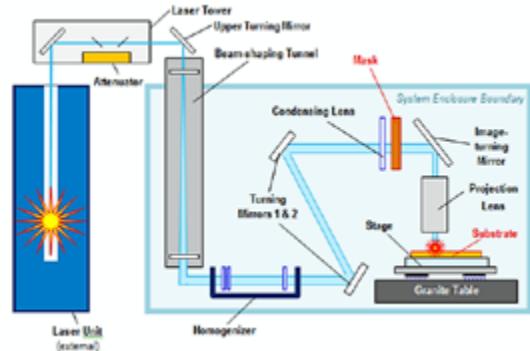


Figure 5: Schematic of the excimer laser stepper setting.

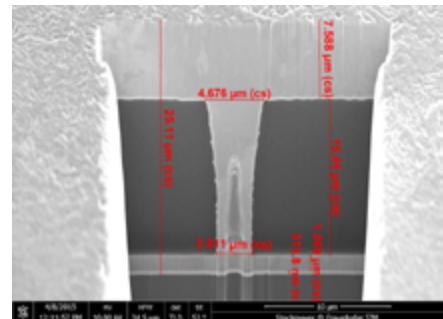


Figure 6: SEM image of a 5 μm via ablated in BCB material showing an aspect ratio of 3:1 [4].

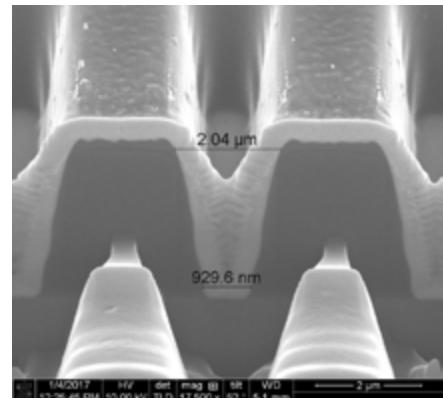


Figure 7: SEM image of the resolution capability of excimer laser ablation for 2/2 μm in HD4100.

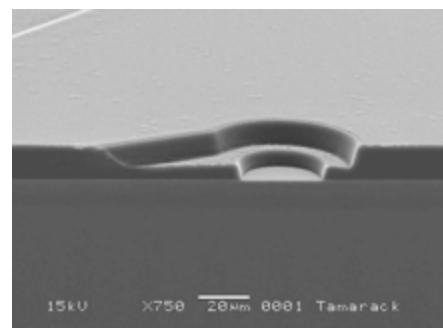


Figure 8: SEM image of an embedded RDL and via formed by excimer laser ablation in PBO film (HD8930, 13 μm thick).

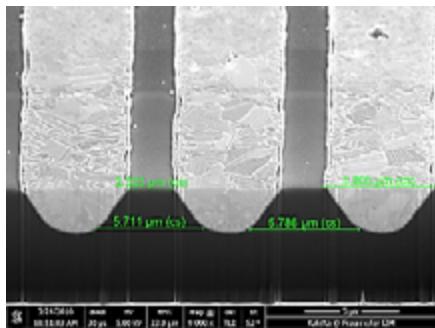


Figure 9: Cross section of an ablated RDL trench post-CMP. The seed layer was removed using an additional excimer laser processing step [4].

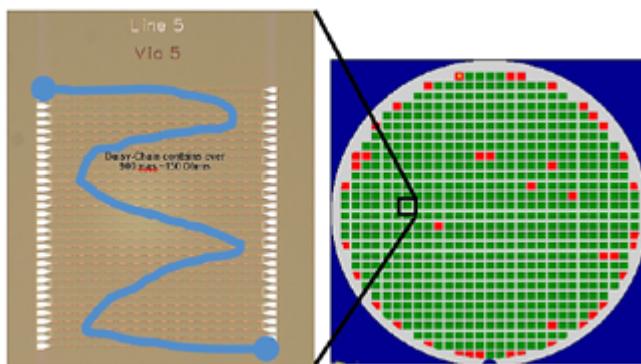


Figure 10: Daisy-chain yield over a 200mm wafer [4].

Excimer Laser Micro-via Reliability

– Build-up + excimer +Eless seed SAP –

GT-PRC team: Yuya

- 8μm diameter, 20/40μm pitch micro-vias in 10μm build-up layer with excimer laser
- Coupon number: 6 coupons in one panel
- 8 daisy-chain lines in a coupon for 40μm pitch, 6 lines for 20μm pitch

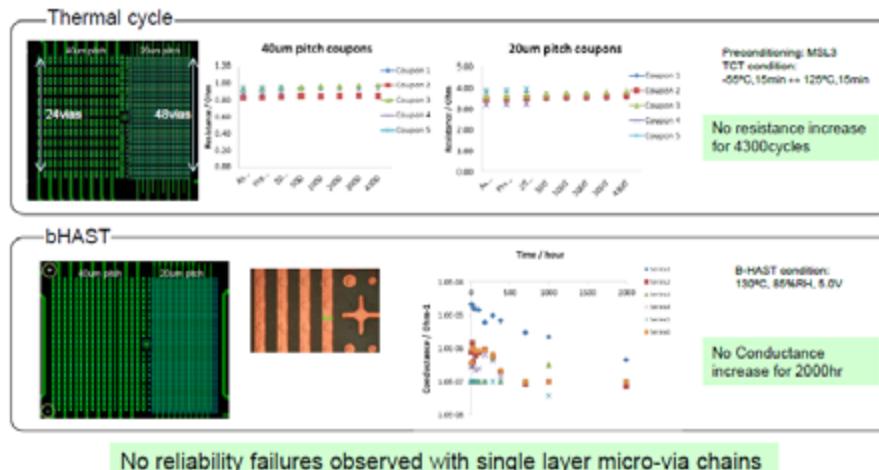


Figure 11: Reliability for an 8μm excimer laser-ablated microvia in ABF (thermal cycle: -55°C (15mins) to 125°C (15mins) [5].

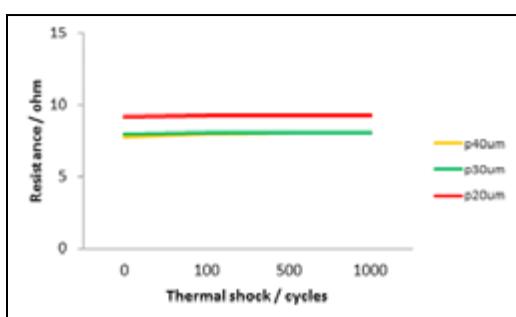


Figure 12: Reliability for a 10μm trench fabricated by an excimer laser in ABF (thermal shock: -55°C (1min) to 125°C (1min) [5].

Summary

The application of the PCB-like laser ablation technology on a mask-based lithographic process using a stepper platform allows the fabrication of ultra-fine structures with high throughput.

Feature sizes of 5μm and below for both vias and RDLs are demonstrated and show an excellent yield. There are many benefits from using an excimer laser compared to a common photolithography approach: 1) elimination of many process steps and consumables from the integration flow; 2) the pattern integrity of the structuring (“what you see is what you get”); 3) the ability to pattern ultra-fine vias and RDLs; 4) overcoming the obstacle to remove the seed layer in fine RDL trenches; and 5) the use of non-photo-definable materials that enable a wider option for CTE matching and are often cheaper. With a reduced number of process steps, high throughput using a

mask-based stepper system, and laser cost at a similar level to solid-state lasers, excimer laser ablation presents a cost-efficient method to enable users to reach the requirements for advanced packaging platforms where dense routing in combination with multi-layer build-ups are needed.

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Biographies

Habib Hichri received a BS degree from the National School of Engineering of Gabes, Gabes, Tunisia, an MBA from the State U. of New York at Buffalo, Buffalo, NY, USA, and Master’s and PhD degrees in Chemical Engineering from Claude Bernard U. at Lyon, Lyon, France. He is Director of Applications Engineering at SUSS MicroTec Photonic Systems, Inc.; Habib.Hichri@Suss.com

Markus Arendt received his Diploma in Industrial Engineering from the U. of Karlsruhe, Germany, and his PhD in Economical Engineering from the U. of Heidelberg, Germany. He is President at SUSS MicroTec Photonic Systems, Inc.

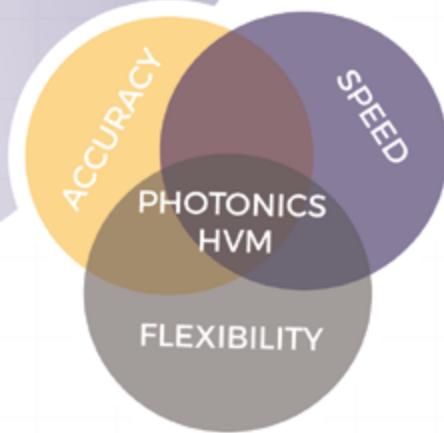
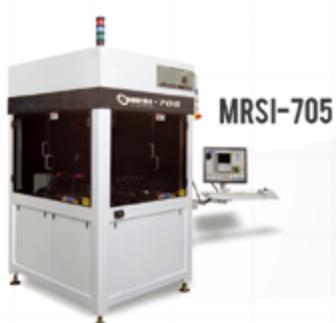
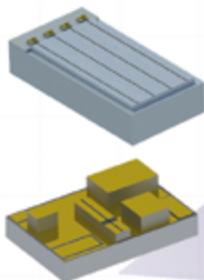


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Photonic modules for data centers require cutting-edge technologies

By Stéphane Bernabé, Olivier Castany, Bertrand Szelag, Benoît Charbonnier [[CEA-Leti within IRT-Nanoelec](#)], and Marc Epitaux [[SAMTEC Inc., within IRT-Nanoelec](#)]

The continuous increase of worldwide internet traffic has led to the development of mega data centers to manage the huge amount of information to be stored, processed, and routed. This has resulted in the mass adoption of optoelectronic devices at every level of the global network. This is particularly true in the aforementioned data centers, in which parallel optics vertical cavity surface emitting laser (VCSEL)-based transceivers operating at 25Gbps per channel are now commonly used to connect switches racks at distances of several hundreds of meters.

The next-generation of data centers, exhibiting dimensions equivalent to that of several soccer fields, will have to manage ever increasing aggregated data rates over distances measured in kilometers. This requires new optical components to be developed with long-range single-mode optical fiber transmission, and likely the adoption of wavelength division multiplexing (WDM) techniques to increase the overall bandwidth carried on a single fiber. These last two characteristics are not manageable by VCSEL modules even though they have the capability to be directly modulated at data rates as high as 25Gbps and carry advanced modulation like PAM4. Indeed, 850nm wavelength VCSEL modules are limited to multimode fiber links that are challenged by modal dispersion in long ranges and by WDM filtering packaging implementation.

As a result of the situation described above, two integrated photonics technologies are now competing to share the market of next-generation hyper-scale data centers, as well as data center clusters that are separated by several dozen kilometers: InP-based circuit devices, and silicon photonics devices (using silicon-on-insulator [SOI] wafers as substrates). The latter emerged at the turn of the century and the multiplication of industrial players in the last five years (Intel, Cisco, Mellanox, and others) making it a more mainstream technology. This trend will be accelerated in the coming years by the requirement for integrated photonics to

provide terabit per second optical transmission to electrical switches, which are expected to offer ever increasing bandwidth: 400Gbps for the next Ethernet interconnect link standards, to 25.6Tbps data rate in the next 10 years.

Challenges for Si photonics

To address these challenges, silicon photonics integrated circuits (Si-PICs) possess several advantages. First, using a sub-micrometric silicon waveguide allows integrating miniature optical structures, like light modulators, WDM filters, and photodiodes when additional epitaxial germanium is used. This makes silicon photonics capable of providing densely integrated complex circuits, like multi-channel transceivers, high radix optical switches, and so on, on a few square millimeters of a chip. As an example, a 16-channel integrated multiplexer (whose typical size is around 3cm using glass technologies) has a maximum dimension of 1mm when using integrated Si-PICs that use sub-micron, high refractive index contrast waveguides. On top of that, silicon photonics leverages the CMOS industry foundry fabrication lines, as the aforementioned optical functions can be processed on a 300mm wafer using deep ultraviolet (DUV) lithography. As a result, silicon photonics is particularly well suited for mass production with high yields leading to a substantial economy of scale.

Beside the chip fabrication itself, a reduction of the cost related to the circuit testing is also obtained by wafer-level testing capabilities of the silicon photonics circuits. For example, CEA Leti performed the functional testing of circuits as complex as QPSK (a high-level transmission standard used in long-haul fiber telecommunication network) transmitters using a reconfigurable probe test station from Cascade with embedded test equipment from Keysight.

Because silicon photonics is an emerging technology, several industrialization challenges remain to be addressed. The first one is design automation. Photonics circuits

do not follow the same design rules as those from the CMOS industry. As a result, electronic design automation (EDA) tools need to be updated to integrate the specific design rules, providing photonics-friendly design rule check (DRC) procedures. In addition, SPICE-like models of the devices need to be developed for photonic building blocks to aid circuit designers working to optimize their circuits for a given technology platform (i.e., process design kits, or PDKs). IRT Nanoelec is a French government-funded consortium gathering industrial companies (ST, Mentor Graphics, SAMTEC), a R&D research lab (CEA Leti), and academics (CNRS) to build the necessary libraries to support this activity. IRT Nanoelec has invested a great deal in this activity, and these libraries will be made available in Mentor Graphics' Pyxis environment, as well as to customers through multi-wafer projects offered at CMP (a French wafer broker company).

The second challenge is the laser integration: for this topic, IRT Nanoelec is developing a technique whereby III-V material is bonded over the SOI wafer, and then post-processed with CMOS-compatible technology in order to define heterogeneous single-mode lasers.

Finally, the last goal of IRT Nanoelec is to develop a novel packaging platform for silicon photonics optical engines that can be placed closely to a host chip and facilitate optical fiber connection. Typical links of 200 or 400Gbps are targeted to provide a total bandwidth of 6.4Tbps for a host chip like an Ethernet switch or a field-programmable gate array (FPGA) device. Challenges to overcome will be long manufacturing cycle time, high bill of material (BOM) costs (which will decrease as the technology is adopted), and scalable methods of packaging photonic modules.

This new generation of optical module, sometimes referred to as "mid-board optical modules" (MBOM), requires several advanced packaging techniques to be used for the Si-PIC integration. This is directly due to the electronic/photonics integration, fiber optic coupling, and high number of I/Os to be

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routed. For this, standard solutions do not exist in the legacy optoelectronic modules, as they typically consider single-channel devices, or parallel optical devices with data rates of 28Gbps maximum. Therefore, techniques like copper micro-pillars in combination with flip-chip assembly, as well as passive alignment techniques for single-mode fiber are required and are being developed within the framework of IRT Nanoelec's photonics program. Most of these techniques directly rely on packaging technologies from the semiconductor industry. Recently, results on these three topics have been separately demonstrated by companies and labs such as Finisar [1], IBM [2] and PETRA [3], mixing chip stacking techniques and silicon MEMS micro-machining.

In the meantime, IRT Nanoelec has also successfully demonstrated results at several international conferences such as IEDM, OIC, ECTC and ESTC. First, a 50 μ m pitch copper micro-pillar assembly of an EIC driver

circuit flip-chip mounted on the top of the Si-PIC has led to a demonstration of a 100Gbps photoreceiver (4-channel 25Gbps) using an integrated photonic circuit as small as 5x5mm² [4].

A close view of the electronic-photonic core of the module can be seen in **Figure 1a**. It uses a chip-on-board (COB) architecture, and the fiber connection is obtained by actively aligning a fiber ribbon placed in a glass v-groove array as is typically done in commercial products. **Figure 1b** shows the 25Gbps eye diagrams obtained at the electrical outputs of the four receiver channels.

Progress achieved within the EU-funded PLAT4M project has also demonstrated 56Gbps (28Gbaud) PAM-4 modulation capabilities of silicon photonics modulators. This feature will be used in a further evolution of such optical modules with four channels, doubling the transmission capacity to 200Gbps. A corresponding multilevel eye diagram can be seen in **Figure 2**.

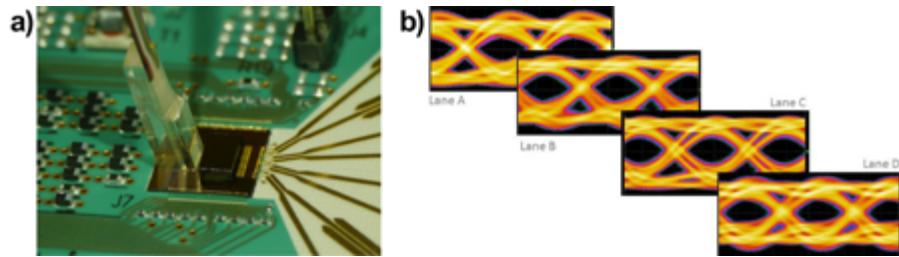


Figure 1: 100Gbps silicon photonics receiver: a) Close-up view of the module, showing the photonic integrated circuit, flip-chipped transimpedance amplifier, and connected fiber array; and b) 25Gbps OOK eye diagram as measured at each electrical output of the module.

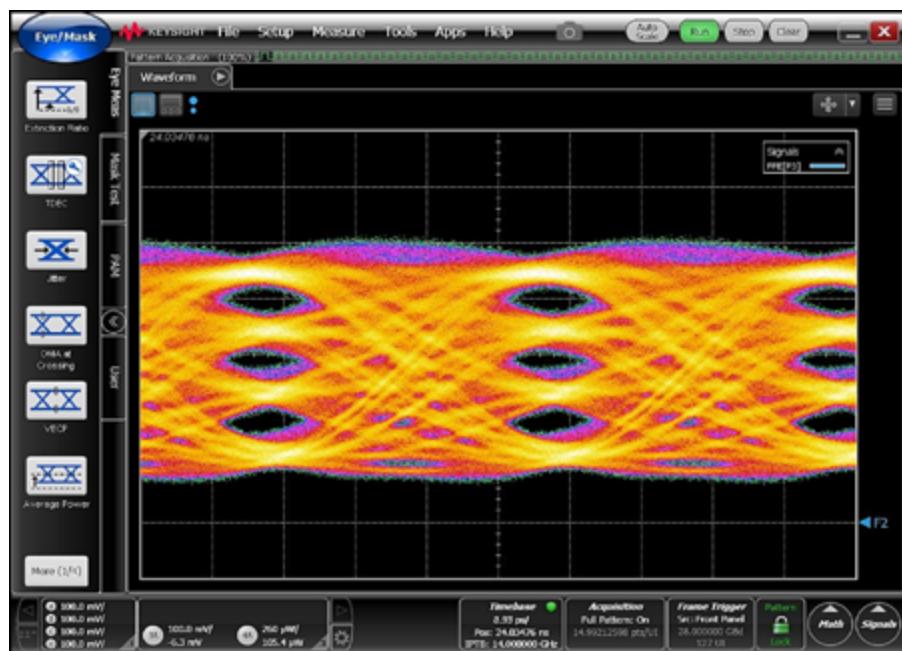


Figure 2: PAM-4 eye diagram obtained at the optical output of a silicon Mach-Zehnder modulator.

IRT Nanoelec micromodules

Next-generation modules in the IRT project combine a small form factor architecture with passive alignment of a single-mode optical fiber array in order to build a 200Gbps transceiver with 4 channels for transmission and 4 channels for reception. For this first demonstration, we packaged a Si-PIC into an extended version of the SAMTEC FireFly™ interconnect solution, sharing the same organic substrate technology [5]. In this architecture, the “photonic engine” (i.e., the assembly of the Si-PIC and its driving electronic circuits) is flip-chipped onto the substrate by using ball grid array (BGA) solder reflow. The organic board is then connected to the host board using SAMTEC’s UEC5 edge connectors. The optical coupling is achieved by a passive alignment approach. The optical train consists of a two-stage lens system to relax the alignment tolerance between a first array of micro-lenses (backside lens) and a fiber coupler. Both optical elements are made of glass to best match the coefficient of thermal expansion (CTE) of the Si-PIC and are micro-machined using MEMS-like technology at the wafer level. Sub-micron accuracy in the fabrication of those optical components is required to guarantee the passive alignment tolerances. To be efficient, this optical layout requires the backside lens array to be accurately positioned on the Si-PIC side facing the fibers. SAMTEC and CEA Leti have developed two alignment methods to reach sub-micron accuracy placement of those micro-lenses, using either vision-assisted assembly with a high-precision die-bonder, or a self-alignment [6] method relying on solder reflow using low-resolution flip-chip equipment. Both processes have been demonstrated and have shown placement accuracy of micro-lenses better than 1 μ m. In both cases those assembly methods use standard manufacturing equipment and are capable of high throughput in production. **Figure 3a** shows the DragonFly packaging platform, and **Figure 3b** is a schematic of the related optical ray tracing.

In the packaging platform architecture shown in **Figure 3**, the fiber coupler holds the fibers in V-grooves, turns the transmitted and received light by nearly 90 degrees, and shapes the optical beams to interface with the backside lens. The enlarged beam between the backside lens and the coupler is nearly collimated, which allows relaxed alignment tolerances, compatible with simple mechanical clamping. This optical element consists of ultra-precise mechanical and optical features that have been etched out

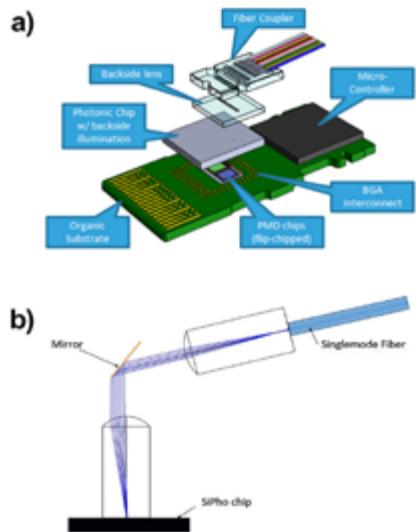


Figure 3: Mid-board optical module, as developed within the IRT-Nanoelec Photonic Program: a) View of the module architecture; and b) Optical ray tracing of the two-lenses architecture.

from a glass wafer. Fiber V-grooves, turning mirrors and micro-lenses have been micro-machined precisely relatively to each other to enable, as stated above, the passive alignment carried out in this packaging platform. **Figure 4** shows the resulting prototypes of the assembled modules.

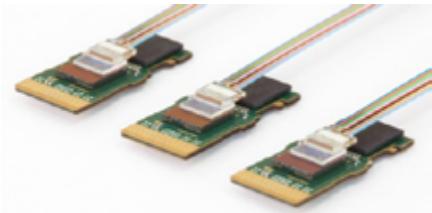


Figure 4: Prototypes of the “Dragonfly” module, using the SAMTEC platform.

Photonics meet 3D packaging

We have seen that several advanced techniques related to packaging technologies helped Si-PICs to be integrated into compact, high-performances modules. This trend should not stop here. The next step after integrating Si-PICs in mid-board optical modules will be the intimate co-integration of the optical transceiver with the “host chip,” e.g., an electronic chip or an FPGA, sharing the same interposer. For this, 3D packaging architectures should be applied, using through-silicon vias (TSVs) in the Si-PIC. These architectures are currently being investigated at several labs, notably IME A*STAR [7] and CEA Leti with STMicroelectronics [8-9]. One of them is depicted in **Figure 5**, and shows a common BGA laminate shared by a host chip

and its photonic transceiver, made of a SOI chip with TSVs.

With this system-in-package (SiP) approach, future electronic devices will be provided with huge optical communication capabilities, exceeding several terabits per second per module. In parallel, these architectures will enable the development of future photonic-based high-performance computers (HPCs).

After years of maturation in R&D labs and industrial companies, silicon photonics is close

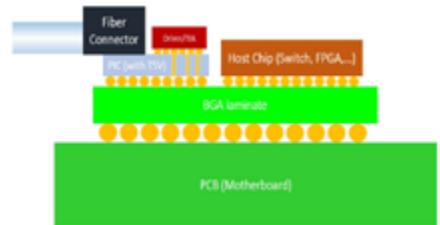


Figure 5: Typical architecture of a co-integrated host chip (switch, FPGA or microprocessor) with a silicon photonic transceiver, sharing the same package.

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to reaching the needed maturity to be fully deployed in large-scale data centers, filling the gap created by the tremendous growth of bandwidth needs. Remaining challenges, mostly related to device integration and packaging, are being tackled by several R&D organizations such as French IRT-Nanoelec. There is no doubt that, combined with advanced packaging technology, silicon photonics circuits will help data centers and HPCs to enter a new era, coping with the challenges of lower power consumption, lower latency, and higher speeds.

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Biographies

Stéphane Bernabé received his MSc in Physics and Photonics Engineering from U. Louis Pasteur/ENSPS, Strasbourg, France and is Project Leader at CEA-Leti, email stephane.bernabe@cea.fr

Olivier Castany graduated from Ecole Nationale Supérieure, Paris, France, and received his PhD in Engineering Science from Bretagne U., France and is a Research Engineer at CEA-Leti.

Bertrand Szelag received his PhD degree in Microelectronics from the Grenoble Institute of Technology, Grenoble, France, and is a Project Leader and Process Engineer at CEA-Leti.

Benoît Charbonnier is IRT Photonics Program Manager at CEA-Leti.

Marc Epitaux received his Master Degree from the Swiss Federal Institute of Technologies in Lausanne, Switzerland and is Chief Architect at Samtec Optical Group, Samtec Inc.

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Interferometry for advanced packaging metrology applications

By Julia Brueckner [Quantum Analytics]

The dramatically increasing cost per mm² in the front end combined with the need for higher I/O counts have caused the wafer-level packaging industry to experience tremendous development. The exponential growth in customer demand for complex and high-density devices drives the need for new packaging solutions because further die shrinking is complicated and expensive. These solutions enable increased functionality and offer higher levels of integration while continuing to reduce package size. The diverse market environment employs a large range of new integrated circuit (IC) packaging types to meet specific applications, i.e., integration of memory, accelerated processing unit (APU), modem and analog – all packed into one thin package [1].

However, there is a corresponding need to implement innovative control processes [2]. This is due to the need to meet the quality and throughput expectations of the market while ensuring every known good die from the final customer ends up in a well working package. The gains in packaging process control provide assurance that the interconnection from the IC to the circuit board is good. Moreover, this improved process control helps ensure the desired heat dissipation, mechanical/environmental protection, and the device's long-term reliability and performance specifications are met. An accurate and near real-time metrology loop becomes essential. In this case, process control is based on optical, non-contact, nondestructive, high-throughput interferometry technologies. Spectral coherence interferometry (SCI) is utilized to measure film thickness, as well total thickness variation (TTV) and warpage [3,4]. White light interferometry (WLI) measurements provide 3D topography information, including step heights, critical dimensions (CD) and roughness [5]. Those measurements are not straight forward and require nonstandard sensors due to

the large amount of height variation and material properties that come along with epoxy mold compound (EMC) processing in wafer-level packaging.

Most wafer-level packaging approaches (especially the fan-out types) require EMC. This can either be in the form of a full wafer coating in fan-in processes, which provide great cost benefits in embedded wafer-level chip-scale packaging (WLCSP). Additionally, it can be in the form of a reconstituted wafer, e.g., embedded wafer-level ball grid array (eWLB) technology [6]. The latter has a number of advantages, including the realization of ICs with a high number of interconnects while maintaining excellent electrical and thermal properties all on a small silicon acreage. In general, fan-out wafer-level packaging (FOWLP) offers an efficient solution providing high I/O count, a thin package with short development times and good yield rates for a WLP because it only uses known good dies. However, the visual inspection is restricted and reconstituted wafers can reveal a high number of surface irregularities and height deviations. The mold material creates many challenges for the process control loop due to its low reflectivity and strong internal scattering. Conventional optical thickness metrology methods fail to deliver data. Therefore, what is used today are contact-based

approaches (not permitted for product wafers), or are not accurate enough on warped wafers (such as back-pressure probes). Other techniques require the destruction (cross cut) of the wafer, such as scanning electron microscopy (SEM).

In the first part of this article, we will explore how an SCI-based sensor with a high numerical aperture is utilized to measure layers and surfaces of mold materials despite measurement constraints: high roughness values, high internal scattering, and severe wafer warpage. Different strategies are demonstrated using specifically designed sensors to investigate this challenging molding material on the same metrology platform. By combining different sensors into the same module, it is possible to monitor not only the thickness of several layers, but also the total thickness, TTV and surface warpage simultaneously.

Spectral coherence interferometry (SCI)

Wafer-level EMC deposition is hard to control and can lead to a very inhomogeneous thickness distribution across the wafer. The high variation of the surface structure and layer thickness emphasize the need for an accurate process inspection metrology. If the sample looks like the left illustration of **Figure 1**, the results of the measurements are easy

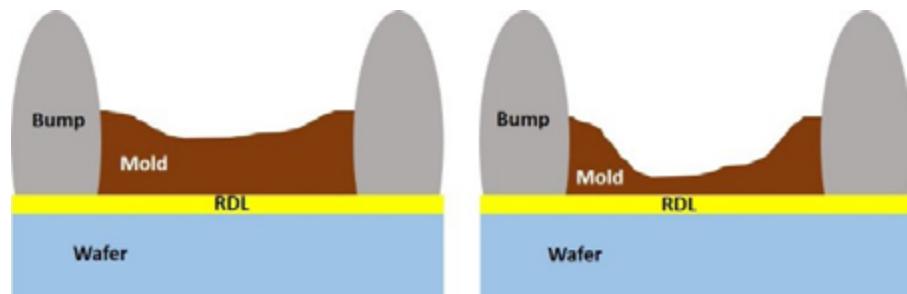


Figure 1: Sketch of sample composition. The two images represent the sample conditions at two different locations. This huge mold thickness variation on structures at different locations (compare **Figure 1a** (left) vs. **1b** (right) mold thickness distribution) makes optical inspection very challenging.

to interpret because the surface signal of the mold and the signal intensity of silicon reflection do not vary by much. However, if the sample shows a signature like the illustration in **Figure 1b**, interpretation becomes difficult due to changing signal intensities and peak positions. The height difference of the mold could change by a factor of two from one position to the other. A sensor was developed with a much larger numerical

aperture (NA) of 0.2 to face these challenges, and reflection signals – even at steep locations – could be detected and analyzed accordingly. **Figure 2** represents a measurement of 4 bumps in a WLCSP process that are surrounded by the mold compound. The top of this figure (**Figure 2a**) shows a 3D representation of the bumps and the bottom a cross section between two of

them. The height difference between the bumps and the mold surface is about 133 μ m. Additionally, the mold thickness in the center of those bumps was measured using the same sensor. The layer thickness distribution ranges from 20 to 75 μ m depending on the position on the wafer.

As can be seen in **Figure 3**, different sensors were deployed for specific applications. The StraDex f4-300 manufactured by Sentronics Metrology (Mannheim, Germany) with a NA of 0.2 is used for mold thickness and warpage of the surface as a single top sensor. It can be used in conjunction with a StraDex f22-95, which has a NA of 0.12 to measure total layer thickness. This f22-95 is also capable of measuring the tape glue and RDL thickness simultaneously. A StraDex f24-300 with a low NA of 0.05 can penetrate the thick silicon layer. A microscope/camera from the back visualizes the measurement position to avoid the bumps.

The setup presented in **Figure 3** allows for measurements of the mold compound thickness using the StraDex f4-300 sensor with a NA of 0.2. This sensor can also monitor the surface mold material; and together, with the surface signal from the bottom StraDex f22-95 sensor, the total thickness of the stack is captured. This StraDex f22-95 sensor can be mounted at the bottom, and its NA of 0.12 makes it possible to look through rough tape material. The multi-layer stack of tape, glue, RDL and total layer thickness can be measured simultaneously. A sensor with a small NA (0.05) is required to measure the thick silicon die thickness. A combination of those sensors integrated into one SemDex metrology system (either configured to be fully-automated for HVM or as a semi-automated manual loaded system for R&D purposes) provides many solutions for a reduced cost-of-ownership (CoO) and footprint, and enable mold wafer metrology that is not possible with the built-in grinder IR probe. In addition, it is also possible to integrate sensors using different technologies into this platform. For example, reflectometry for thin-film thickness or WLI for 3D topography. Next, we'll explore how WLI can be used to achieve fast and accurate measurements of step heights, CDs of pads, and under bump metallization (UBM) features on wafers with high nonuniformity.

White light interferometry (WLI)

The RDL process flow requires a full lithography and plating cycle. To ensure a reliable product, all process

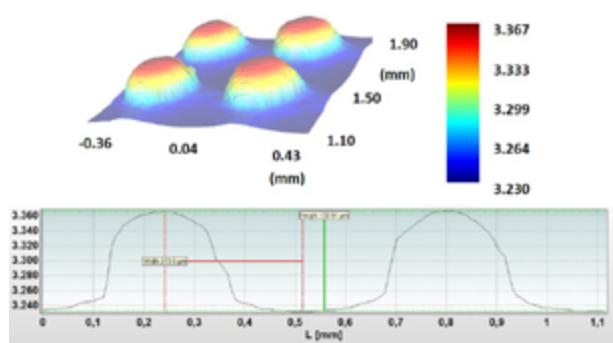


Figure 2: Bump height measurement: a) (top) 3D surface image, and b) (bottom) line analysis through two of the bumps to determine the height difference of bumps to mold surface.

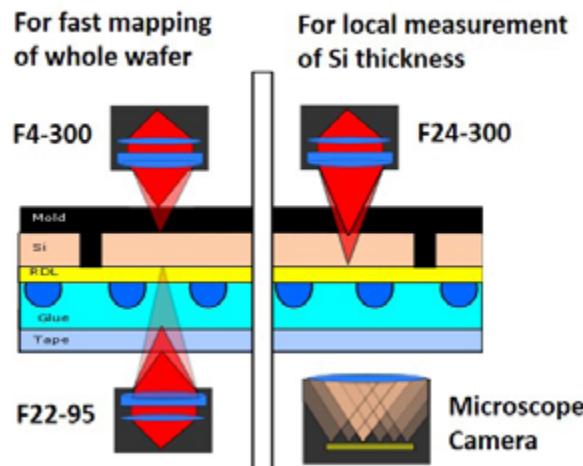


Figure 3: Sketch of the sample consisting of a molding compound, silicon wafer, RDL, solder bumps, glue and tape layers.

aperture (NA) of 0.2 to face these challenges, and reflection signals – even at steep locations – could be detected and analyzed accordingly. **Figure 2** represents a measurement of 4 bumps in a WLCSP process that are surrounded by the mold compound. The top of this figure (**Figure 2a**) shows a 3D representation of the bumps and the bottom a cross section between two of

different sensors and measurement configurations provides a high amount of flexibility and allows for monitoring multiple process steps. **Figure 3** presents a sketch of the sample composition together with different sensors, and their ability to measure single layers, multi-layers and total layer thickness in specific configurations.

steps need to be tightly monitored and controlled. One of the challenges here is how to measure step height of pads or UBM features on structures that are not completely flat and show height variations. We can solve this challenge by introducing a stable algorithm to evaluate those features automatically.

Most methods only measure the step height of a feature at one particular location from a 2D scan. This is only valid if the underlying structure is completely flat and the local height variation is small compared to the global distribution. For most FOWLP processes, this is not the case because the RDL is built on the reconstituted wafer (eWLB wafers) or it is a multi-layer RDL process in which the height variations from the lower level will automatically be translated to the upper level. With a typical surface scan approach using a point source, it can be difficult to measure the height of a nonuniform pad. This can be the case for pads located between the die and the mold fan-out area. It is part of the normal process variation to have a

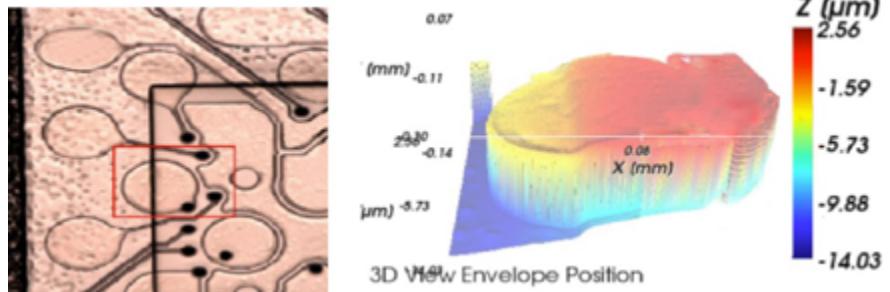


Figure 4: RDL structure on molded wafers, as a) an AOI picture (left) and b) as a WLI 3D false color image (right).

step of a few microns from the die to the mold. Once the pad is placed, there will be a step on the pad itself (see **Figure 4b**, right). By using a point source on one location it is impossible to monitor the step height variations around the pad.

The StraDex a3-50 WLI sensor delivers a full 3D image with lateral and vertical resolution and range capable of seeing the entire pad or UBM of interest [7]. In the first step, an HD camera searches for the exact fiducial location for each die to be measured. The WLI measures

a specific feature and after finding the exact center its CD is calculated. With the known radius, the actual step height can be calculated from the 3D profile. The process engineer can define two ring positions (inner and outer level) and width with respect to the feature edge. The area is divided into segments (usually 360) and each segment is evaluated for minimum, maximum and median values. The step height is calculated from the outer and inner segment height difference and statistics are computed on those step heights to

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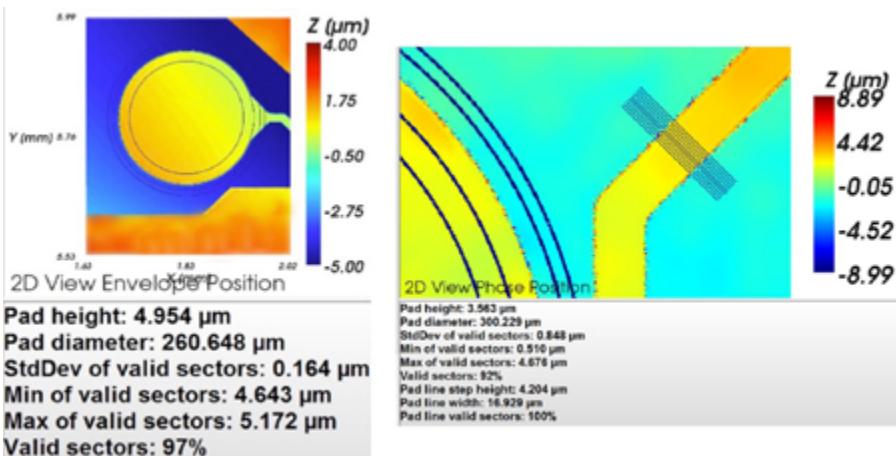


Figure 5: Automatic a) (left) pad height and b) (right) copper trace height evaluation using a StraDex a3-50 WLI sensor.

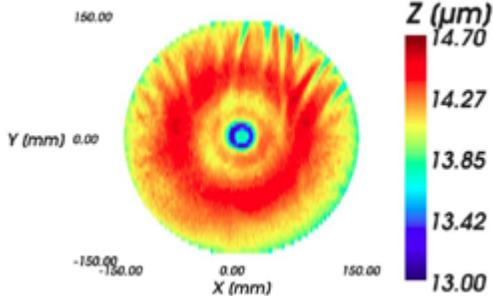


Figure 6: High-resolution full-wafer map for PR coating with multiple thousand data points.

get a figure of the planarity of the pad (see **Figure 5a**, left).

Once the pad center has been found, it is straightforward to evaluate the attached copper line because both are manufactured in a tight tolerance lithography step. The algorithm will ignore the area directly around the edge due to the WLI inherent overshoot problems. The width is calculated from a smoothed 3D profile averaged over many lines across the copper trace (see **Figure 5b**, right).

Summary

With the growing demand for thinner packages that consist of multiple devices, the need for an accurate metrology loop to control the process flow is essential. The integration of memory, APU, modem and analog all into one package requires that each layer thickness has to be exact to specification. Controlling wafer thickness helps to improve process flows, and thereby increases yield. The creation of full wafer maps with orders

of magnitude more data points is an important step to reveal areas of low yield. SCI provides an optical, non-destructive, high-throughput solution to measure a single-layer, multi-layer thickness, total layer thickness and surface warpage simultaneously at a 4kHz rate. **Figure 6** presents a full 300mm wafer map with multiple thousand points of a 15µm photo resist coating achieved with a HVM-compatible cycle time of 1 minute. This high-speed method can finely map the thickness distribution in order to improve the coating process.

Combining many StraDex f sensors with different optics and NAs enables a variety of applications. Using a sensor with a high NA can overcome the challenge of measuring mold materials despite high roughness, high internal scattering and severe wafer warpage. The height difference between bumps and the mold surface, as well as the mold layer thickness itself can be measured with high throughput. Adding an additional bottom sensor of a different optical design enables multi-layer thickness, total layer thickness, and variation data.

A WLI-based method is used to automatically measure and evaluate key features in RDL manufacturing. This technique is independent of the pad shape and other nonuniformities across the measurement area. The step height data is captured for the entire pad structure and evaluated in different segments, which enables the analysis of the pad planarity.

All presented applications can be realized using one SemDex metrology platform equipped with different sensors based on optical interferometry. Each system can be equipped with up to eight different sensors and microscopes/cameras to cover a variety of applications. This not only reduces CoO, but also saves expensive cleanroom space.

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Biography

Julia Brueckner received her PhD in Physical Chemistry at the U. of Heidelberg, Germany. She is an Applications Scientist for optical metrology equipment at Quantum Analytics; email jbrueckner@lqa.com

Nondestructive 3D X-ray imaging for advanced packaging failure analysis

By Cheryl Hartfield [Zeiss Semiconductor Manufacturing Technology], and Daniel Nuez [Xilinx, Inc.]

Packaging of integrated circuits is growing more and more complex – and housing multiple die in a single package is just one challenge chipmakers face. Typically, these die are connected in complex ways, and chipmakers must contend with shrinking feature sizes and interconnects, escalating device density and package size, thinner layers, and a widening variety of materials.

As a result, failure analysis (FA) on advanced packages is becoming increasingly difficult. The goal of FA is to isolate where the failure is located, and then figure out what it is and why it happened – its root cause. Visualization of defects aids determination of the root cause. Packages are essentially opaque boxes containing electrical connections. Often, to visualize a defect in the electrical path, physical failure analysis (PFA) is applied.

Maintaining integrity of the defect site is critical. If a sample is cut or reduced in size, further electrical analysis may not be possible, and the structure may be disrupted by introducing artifacts or changing the stress profile from that of an intact sample. Conventional nondestructive methods have become less effective at visualizing defects in many of today's packages, creating a significant need for new nondestructive approaches such as 3D X-ray microscopy (XRM).

Benefits of X-ray microscopy

In the typical board- and package-level FA lab workflow, failures are evaluated nondestructively prior to destructive analysis (Figure 1). The most common nondestructive PFA techniques for isolating and visualizing defects are optical inspection, 2D X-ray, and scanning

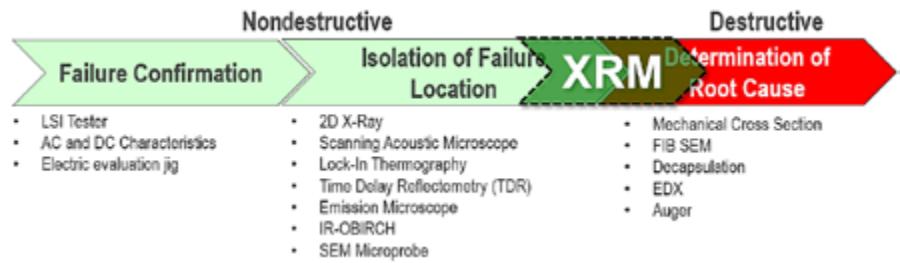


Figure 1: Acceptance of 3D X-ray microscopy is growing for failure analysis.

acoustic microscopy (SAM). Due to increased package complexity, these imaging techniques are becoming less effective.

XRM, a relatively new FA technique, uniquely provides a high-resolution, nondestructive method to find and image defects in 3D. It thereby provides critical knowledge to guide next steps. Application of XRM typically fits between fault isolation and root cause determination (Figure 1).

Once the fault location is isolated, traditionally, a next step is a visit to the “coroner's office” – that is, PFA techniques that destroy the sample are used to investigate the root cause of the failure. The techniques cited on the far right side in Figure 1 all involve physically cutting, drilling or otherwise altering the sample in some way. If the fault is not properly located, there is no second chance to find it unless another package is sacrificed.

Providing 3D intelligence ahead of destructive analysis is a key benefit of XRM. It enables higher success rates in cross-sectioning and finding root causes. Visualization of defects by 3D XRM can even eliminate the need to perform PFA, saving time and resources. The case study included in this article illustrates the effectiveness of 3D XRM in the FA workflow.

Visualizing defects nondestructively with virtual cross sections

The power of 3D tomography comes from its ability to provide virtual cross sections, revealing the details inside structures. Figure 2 provides a simplified overview of the XRM tomography process. Figure 2a shows that data is acquired by collecting 2D projection images from a rotating sample positioned between an X-ray source and a detector (the yellow dot in Figure 2a). The XRM detector is composed of scintillator-coupled optical microscope objectives combined with a charge-coupled device (CCD) camera. The X-rays pass through the sample and hit the scintillator mounted on the objective lens. The scintillator converts the pattern resulting from X-rays transmitted through the sample into the optical image captured on the right (Figure 2b). The sample is then rotated slightly, the image captured again, and this process is repeated through up to 360 degrees of rotation. The resulting group of projections – typically, between 1,000 and 2,000 – are then processed by algorithms to mathematically reconstruct the 3D volume (Figure 2c).

The time required for the entire process is variable – typically ranging between 30 minutes and 8 hours – depending on the number of projections and how much time

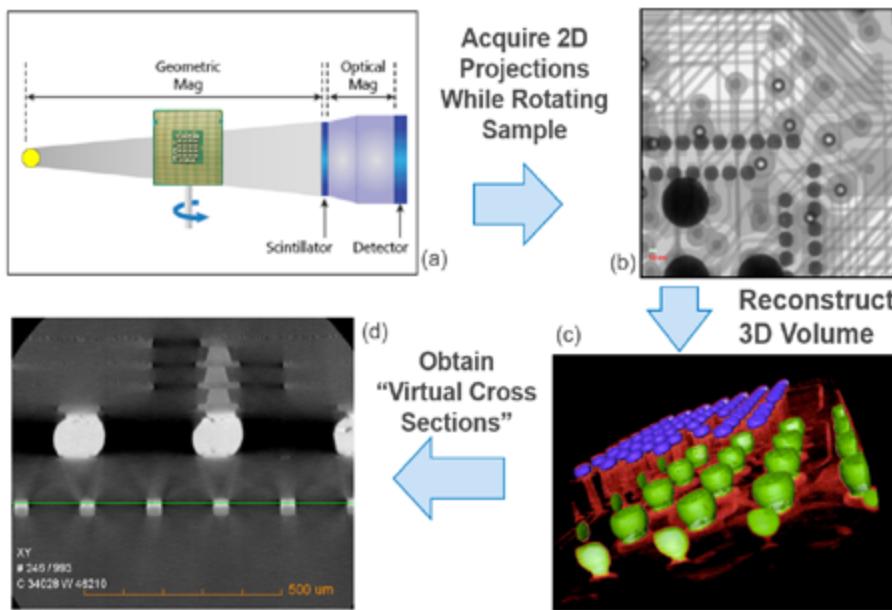


Figure 2: XRM 3D tomography yields highly informative visual information about failures, nondestructively.

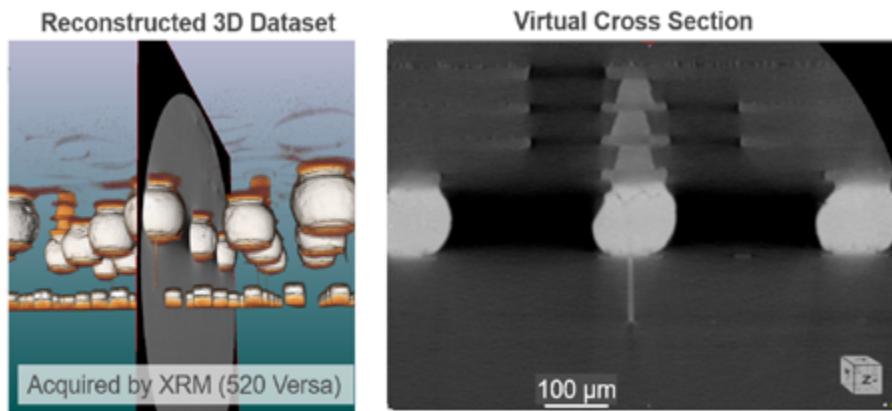


Figure 3: Using XRM, any plane through the 3D data may be viewed as a virtual cross section.

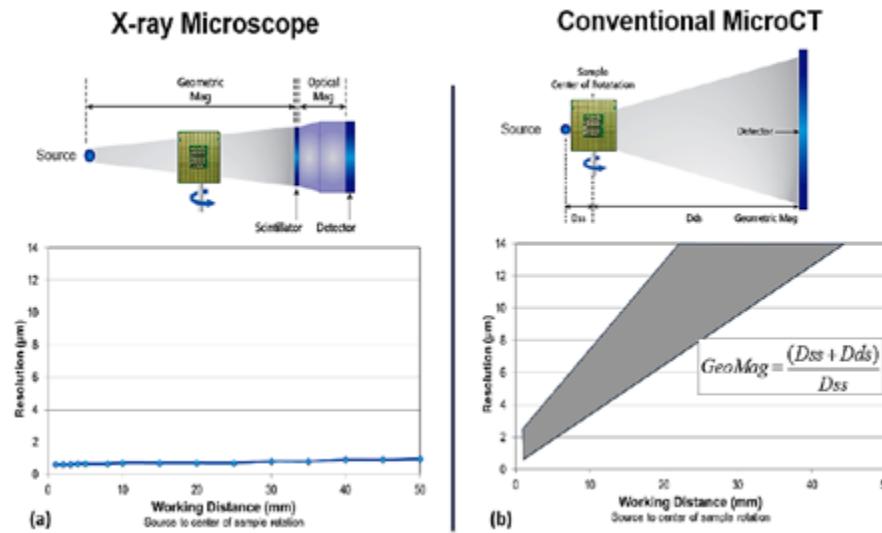


Figure 4: XRM is well-suited for package FA because it maintains resolution regardless of package size.

is spent per projection. From the resulting 3D volume, one can view any number of horizontal or vertical cross sections through the sample (**Figure 2d**) – essentially, isolating any desired sliver of the 3D volume. Therefore, details of fault locations can be visualized without destroying the sample. As an example, **Figure 2d** shows a virtual cross section of a 2.5D interposer stack.

The virtual cross-section plane can be moved interactively through the 3D dataset in any of the three orthogonal directions (x, y, z). This allows localization of defects to specific areas, such as the substrate-side or chip-side of a flip-chip bump, and aids understanding of the failure mechanism. **Figure 3** provides another look at how a virtual cross section is obtained from the reconstructed 3D dataset.

XRM vs. micro-CT

Micro computed tomography, or micro-CT, is another approach to obtaining 3D images. However, as **Figure 4** illustrates, XRM offers significant resolution advantages compared to micro-CT. To achieve high resolution in micro-CT systems, high-geometric magnification is required. This involves placing the sample very close to the source (**Figure 4b**) and moving the detector as far away as possible – this ratio determines the magnification and, thus, the resolution of the image. With micro-CT, large samples are challenging to image at high resolution. As samples become larger, they must be moved further away from the source so they can be rotated without colliding with it. As the sample is moved away, there is a linear reduction in the magnification, which, in turn, lowers the resolution (**Figure 4b**).

The advantage of XRM is that high-resolution images can be obtained from fully intact large samples that are positioned further away from the source (**Figure 4a**). The scintillator-coupled microscope objectives provide the magnification necessary to retain resolution versus depending upon geometric magnification alone. With XRM, resolution remains relatively independent of the package size, and high resolution can be maintained with

large sample sizes. This capability represents the core value of XRM vs. micro-CT technology.

Increasing the success rates of PFA

The following case study demonstrates the benefits that 3D XRM offers to chipmakers. In this instance, a 2.5D interposer test chip with micro-bumps was used for packaging development and process optimization. In the center of [Figure 5](#) is the package computer-aided design (CAD) layout, showing micro-bumps and larger C4 bumps. A short has been isolated to the spot depicted in the green box at left. At right is the 2D X-ray image – the three micro-bumps are visible inside the C4 bump, in the same orientation, but it's impossible to see where the short is actually located.

The red dotted line in the middle image indicates the direction of the physical cut performed with PFA in an effort to visualize the short. As the orange line labeled "solder extrusion" shows – and as was later determined using XRM – the short from one micro-bump to another exists at an angle. XRM also revealed that the size and mass of the short was below the detection limits of the 2D X-ray system.

The failure analyst repeatedly cut and polished the sample to get as close as possible to the failure site. An anomaly in the form of solder extrusion was observed (see [Figure 6](#)) and suspected to be the cause of the short. An optical image is on the left, and a SEM image is on the right. Visual evidence of a short across adjacent bumps is missing in both optical and SEM images. The analyst continued to polish about 10 microns further, and as [Figure 7](#) shows, polished through evidence of the short. Although the electrical data pointed to the short's general location, more precise information was needed to successfully confirm the short by destructive PFA.

3D XRM can reveal details of a solder bridge (location, size and orientation) prior to destructive analysis. This information can then guide and enable successful execution of a precise cut into the solder bridge. As [Figure 7](#) shows (right image), there was evidence of solder extrusions in

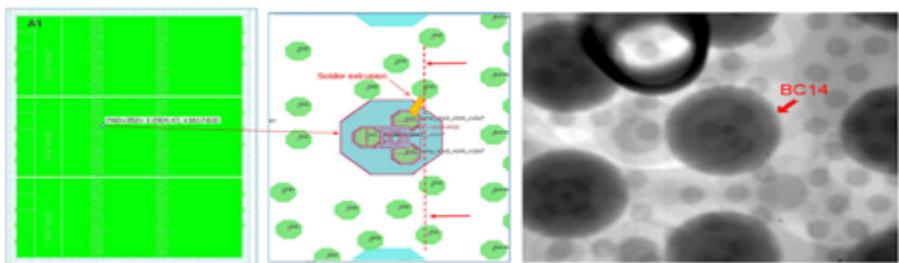


Figure 5: In a sample 2.5D interposer chip, an electrical failure was found at pin BC14, but 2D X-ray inspection failed to show any structural anomaly.

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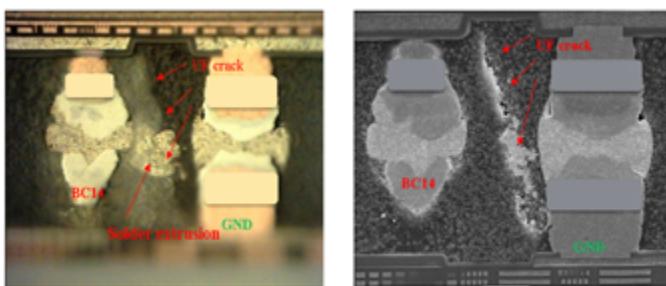


Figure 6: The first cut using PFA revealed the solder extrusion, but not the bump-to-bump connection, requiring further cutting and polishing.

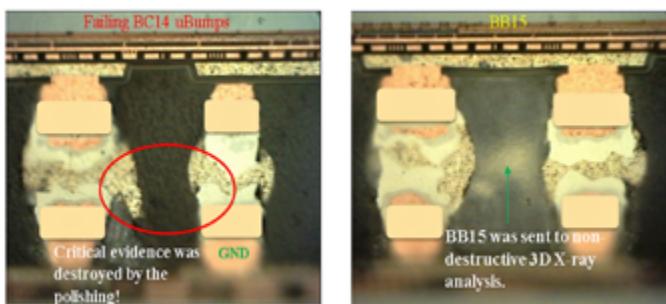


Figure 7: The second polish destroyed the physical evidence of a micro-bump short on pin BC14. Nondestructive 3D XRM tomographic imaging was performed on adjacent bump BB15 due to evidence of solder extrusion in the cross section's optical image.

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adjacent bumps. Before attacking the sample further with continued polishing, a defective area was imaged by 3D XRM using sub-micron voxels.

The 3D rendering in **Figure 8** shows the exact location and orientation of the short, which guided the subsequent destructive cross-sectioning angle and resulted in a successful FA report.

Failed Pin	BC14	BB15
3D XRM integrated FA		XRM clearly visualized the solder bridge defects without cutting or downsizing the sample
Conventional FA	1 st cut revealed solder extrusion, but evidence of solder bridging was not obtained in further polishing due either to removal of evidence or to analysis in the wrong plane	Further X-section is possible, guided by 3D XRM data

Figure 8: 3D XRM data confirmed the defect with no destruction of the chip sample.

Summary

Package technology is growing in complexity and the FA workflow needs to adapt to the new requirements. Conventional FA involves cutting into samples and polishing the edge to the approximate location of the failure. Then SEM and/or optical micrographs are used to capture high-resolution 2D images in order to help determine the failure's root cause. While valuable for some applications, this approach is destructive – it provides a single chance to choose the right cutting orientation that will expose the failure for imaging. Moreover, the process may introduce artifacts from cutting and polishing that can hinder root cause determination. Defects may be missed, leading the failure analyst to conclude that no defect could be found.

With its high-resolution and nondestructive properties, 3D XRM imaging and analysis has become increasingly commonplace in FA workflows, particularly for advanced 2.5D and 3D packaging architectures. By providing detailed 3D images of failure locations, it is a valuable precursor to – and in some cases, can completely replace – physical cross-sectioning.

Biographies

Cheryl Hartfield received her MA and BS in Microbiology from UT Southwestern Medical Center and Texas A&M, respectively. She is Solutions Manager for X-ray microscopy at Zeiss Semiconductor Manufacturing Technology; email cheryl.hartfield@zeiss.com

Daniel Nuez received his BS in Information Systems from U. of San Francisco and is a Senior Device Analysis Engineer at Xilinx, Inc.

Contactor and package design effects on crosstalk

By Noureen Sajid [Johnstech International]

Increasing data rates and shrinking package sizes in the chip test industry result in challenges with noise due to close spacing of high-frequency lines. Crosstalk, a measure of how much noise in a signal line is induced from nearby signal lines, quantifies the noise in a test system. Interference effects can range from signal degradation to the damage of the components (e.g., sensors).

With limited real estate on devices, it is not always feasible to employ strategies to make packages more immune to noise. Providing sufficient grounding to protect a signal line could mean adding more I/Os than a device can accommodate, which is not always possible. Trying to keep the locations of signal lines as far away as needed can also prove difficult when there is tight spacing.

In this paper, a brief definition of crosstalk is provided, including an explanation of the ways of evaluating it (near end, far end), and the components that are involved in the evaluation (aggressor, victim). Then, the ways in which crosstalk is affected by package parameters such as layout of the signal lines, grounding and inductance, are discussed.

Strategies for improving the noise immunity of test systems using the features within a contactor are also introduced. This would show that the combination of package and contactor features can provide a test system that is much more immune to electromagnetic noise than the individual components of the test system.

Definition of crosstalk

Crosstalk is a form of electromagnetic interference (EMI). When current travels down a signal line, the electrons in the conductor get excited and tend to start traveling at the surface of the conductor. This phenomenon is known as the skin effect. As the skin effect increases, the electromagnetic field grows to

affect adjacent conductors causing a loss of signal in the original conductor (termed “aggressor”) and creating an interference on another conductor line (termed “victim”).

The process of quantifying is mainly through a logarithmic scale as shown in the example depicted in **Figure 1**. It is always preferred that the crosstalk is more negative on the Y-axis, which indicates that there is less coupling between the two conductors. The -20dB

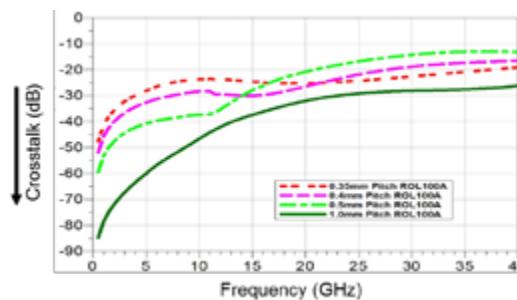


Figure 1: Crosstalk variations resulting from different pitches.

point on this scale is the spec at which 1/100th of the signal from the aggressor has crossed over to the victim line and is usually the industry standard for crosstalk maximum in a test system.

We can consider a 4-port system, where port 1 and port 3 are the inputs to transmission lines 1 and 2, respectively, and port 2 and port 4 are the outputs to transmission lines 1 and 2, respectively. We can consider near end crosstalk would be S31 or S42 and the far end crosstalk would be S41 and S23. This system is illustrated in **Figure 2**. For the

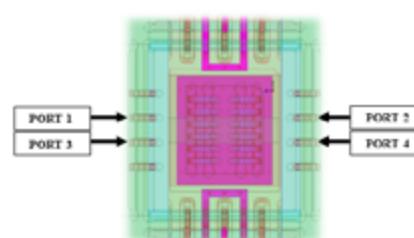


Figure 2: Contactor port definition.

purpose of this paper, we will only be focusing on far end crosstalk as that is the most concerning for test systems. In the proceeding discussions, crosstalk is measured on the victim line such that the input is at the load board and the output is on the device side on the victim line.

Isolation vs. crosstalk. Isolation is another term that is related to crosstalk, and it is important to understand the difference between the two terms. While isolation is measured on the same scale as crosstalk and has the same literal meaning, it differs from crosstalk as shown in **Figure 3**. The term crosstalk is used when the aggressor and the victim lines are adjacent to each other, or at least in the same vicinity. Isolation is defined as the measure of how immune a channel is to distant electromagnetic (EM) noise.

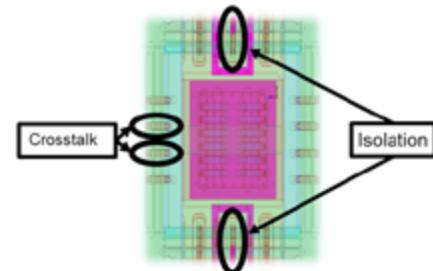


Figure 3: Difference between crosstalk and isolation.

Examples of crosstalk sources

To show the factors affecting crosstalk, we have modeled one common package type and performed simulations. The modeled package style is the quad flat with no leads (QFN) as described in detail below.

For the simulation, we chose a 5mm x 5mm package and varied the following parameters to observe the subsequent changes in crosstalk:

- Pitch varied from 0.35mm to 1.0mm;
- Load board thickness varied from 5 mils to 10 mils; and
- Conductive housing vs. nonconductive housing.

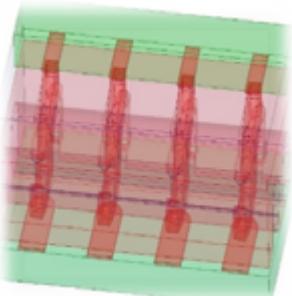


Figure 4: 1.0mm pitch HFSS model.

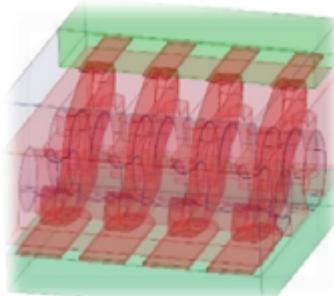


Figure 5: 0.5mm pitch HFSS model.

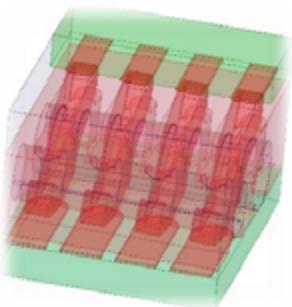


Figure 6: 0.4mm pitch HFSS model.

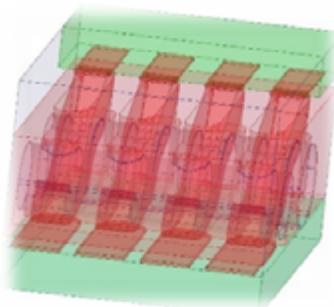


Figure 7: 0.35mm pitch HFSS model.

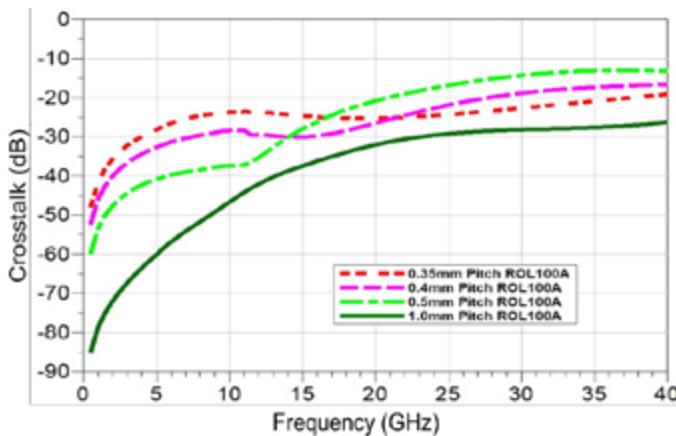


Figure 8: Crosstalk vs. device/contactor pitch.

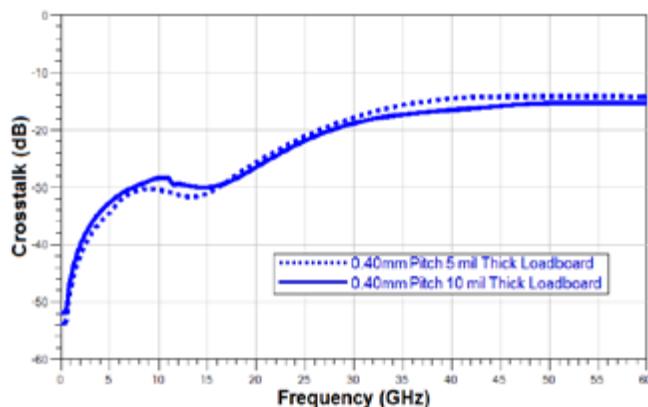


Figure 9: Crosstalk vs. board thickness.

In each case, all other geometrical aspects of the device were maintained at nominal.

Pitch varied from 0.35mm to 1.0mm. To perform this simulation, a row of four contacts was selected as shown in [Figures 4-7](#). In each scenario, the only change made was the distance between the contacts, which was varied between 0.35mm, 0.40mm, 0.50mm and 1.00mm. The simulations shown here include device pads, contactor and load board pads.

The results of the simulation are shown through the graph in [Figure 8](#). The dark green solid line on the graph clearly shows that the crosstalk is lowest when the contacts are furthest apart at 1.00mm pitch. This shows that increasing the distance between adjacent channels decreases crosstalk with respect to the decrease in capacitance between the two channels. This reduction in capacitance decreases the coupling between the channels and makes it more difficult for the signals to cross over to the adjacent line.

One can observe a similar trend for the other pitch configurations up to 13GHz. With the increase in pitch from 0.35mm to 0.50mm, crosstalk decreases. However, after 13GHz, this trend changes for the 0.35mm to 0.50mm configurations. This demonstrates the importance of simulating a complete system across the full bandwidth of the device being tested. As the frequency increases, many other parasitics can influence the signal transmission, which they did not at a lower frequency. Board material dielectric constant and dissipation factor will define the trace width for optimal transmission, and the dissipation factor will determine signal loss between the source and device being tested.

Load board thickness varied from 5 mils to 10 mils. To determine the effect of load board ground on the crosstalk, we took the 5mm x 5mm QFN package with the 0.40mm lead pitch and varied the ground thickness of the load board between 5mils and 10 mils. The results of the simulation are shown in the graph in [Figure 9](#). Overall, the graph shows the impact of the load board thickness variation impacts crosstalk less than changes in pitch. However, at lower frequencies we observe that the 5mil thick load board shows lower crosstalk pertaining to the signals being able to couple to the ground plane more than on the 10mil-thick load board.

Conductive housing vs. nonconductive housing. In this scenario, we solved a customer problem and arrived at a solution that could be utilized when geometrical techniques are restrictive. For this scenario, we had a 5mm x 8mm QFN that needed significantly low crosstalk and isolation during test. The system (package and contactor) is shown in [Figure 10](#) and the simulation took device pads, contactor and load board pads into account, as labeled. This system (package and contactor) was simulated once with a nonconductive housing. The results of this simulation are shown in [Figure 11](#) with a graph that has both isolation and crosstalk plotted on it.

The isolation is plotted on the graph from outputs on ports 14 and 12 to the input shown as port 5. The crosstalk is observed on the output of port 5 from the input on port 3. The specification for this device was to keep the crosstalk and isolation under -40dB up till 10GHz. As can be observed from the graph in [Figure 11](#), this specification had been achieved for the isolation, but the crosstalk needed some more tuning. The distance between the channels could not be increased anymore due to real estate restrictions. Therefore, a solution was needed that went beyond geometrical enhancements.

To obtain a viable solution, we selected a shielding method for reducing crosstalk that worked to increase the grounding

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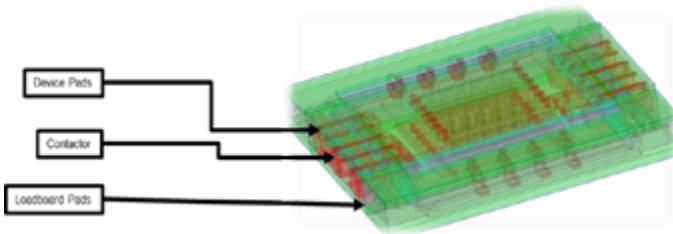


Figure 10: HFSS simulation model of a 5x5mm system (package and contactor).

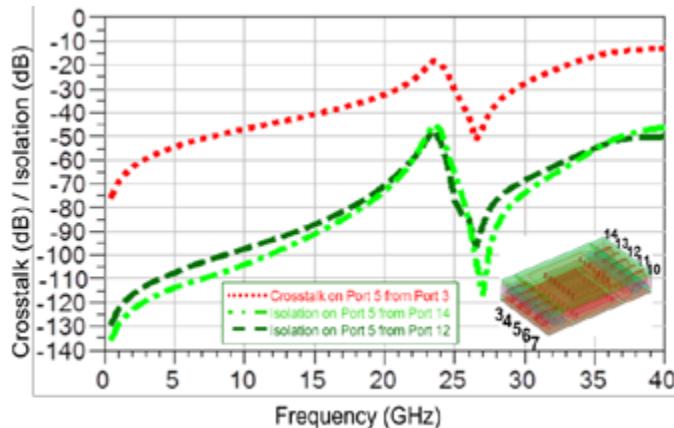


Figure 11: Crosstalk and isolation HFSS model for a 5x5mm system (package and contactor).

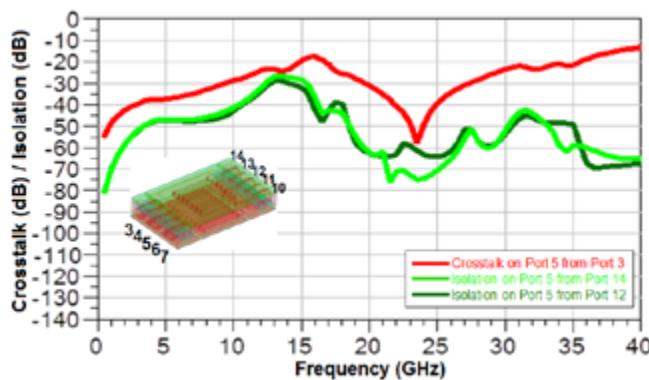


Figure 12: Crosstalk and Isolation performance for a 5x5mm system (package and contactor).

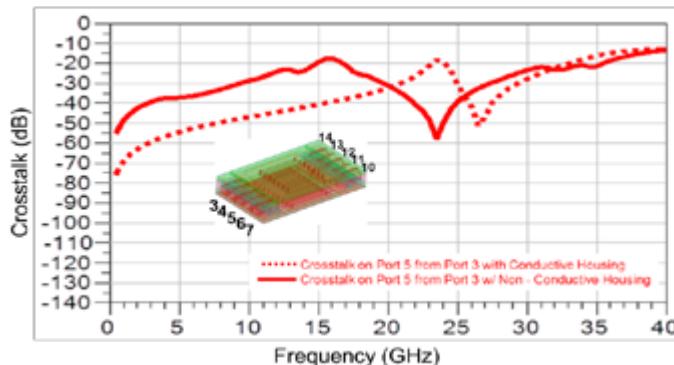
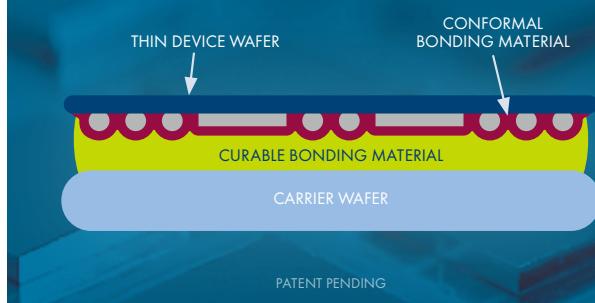


Figure 13: Crosstalk difference between a nonconductive and conductive housing.

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of the contactor, and therefore lower the inductance of the contactor. As mentioned before, the quantity of contacts and distance between the contacts were at their optimized geometry. In simulations, we tested the effect of the shielding by changing the contact material to a conductive metal housing. The signal contacts were encased in a coaxial like nonconductive insert while the housing material of the contactor was changed

to be conductive. This strategy creates a ground everywhere and lowers the inductance of the contactor a significant amount (almost 20% to 30%). The results of this simulation are shown in **Figure 12** and it can be observed that there is almost a 20dB drop in crosstalk and isolation from a nonconductive to a conductive housing. To observe the improvement in crosstalk, a comparative graph of the crosstalk is shown in **Figure 13**.

Immunization strategies for crosstalk

There are many more ways of lowering crosstalk and creating a well-shielded system. The importance of reducing crosstalk in test systems is to preserve the signal integrity of the test system and to restrict losses from aggressor lines that can add noise on victim lines. The immunization strategies that can be used to achieve this purpose are as follows:

- Pitch: Increasing the distance between adjacent signals reduces crosstalk by lowering the capacitance between the signal lines;
- Grounds: Increasing number of grounds between signals can create a shielding on the signal line and reduces the coupling of that line to other signal lines by reducing the inductance of the contactor. Conductive housings are a good example of extracting the benefit of this strategy to its optimized capacity.
- Quantity of grounds: Surrounding signals with grounds is another way to isolate signal lines and restrict them from coupling to other lines.
- Length of channels: Crosstalk increases as the length of two conductors travel adjacent to each other increases. Therefore, keeping the channels short will prevent the lines from coupling to each other by providing less capacitance between the lines.

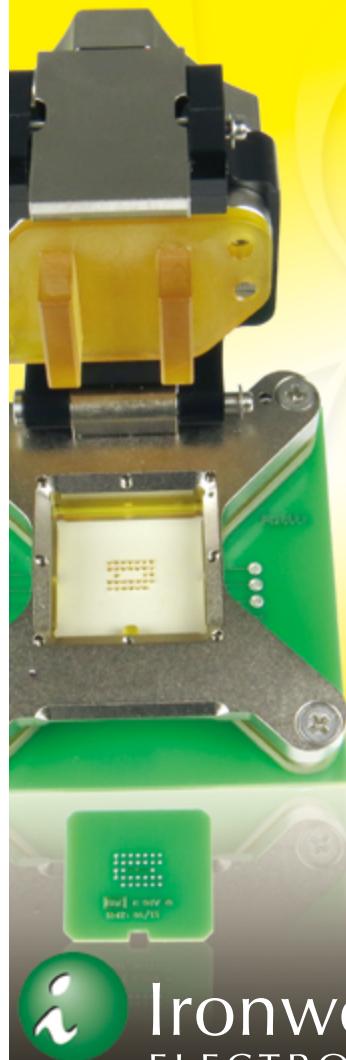
Many of the concepts and ideas touched upon in this article can be applied to other types of packages such as ball grid arrays (BGAs) and land grid arrays (LGAs). Overall, the most important point to note is that simulating packages with contactors and load board interfaces (full system) early in the design phase determines the expected test performance and enables us to find solutions faster, which in turn, lowers the cost-of-test (CoT) and increases the reliability of the test system.

Biography

Noureen Sajid received her BS in Computer Engineering from Bahria U., Pakistan, and her MS in Electrical Engineering from St. Cloud State U., MN; she is an Applications Engineer at Johnstech International; email nsajid@johnstech.com

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High-throughput via formation in solid-core glass for IC substrates

By Roman Ostholt, Norbert Ambrosius, Daniel Dunker, Jean-Pol Delrue [LPKF Laser & Electronics AG]

This article was edited from a paper presented at the 2017 MiNaPAD Conference, May 17-18, Grenoble, France.

Conventional laser ablation of glasses is prone to micro cracks, chipping and thermally-induced stresses that render it rather inappropriate for processing glasses on a micrometer scale [1]. Alternatively, selective laser etching (SLE) of glass can be used to generate arbitrary three-dimensional and micrometer scale features in glass [2]. However, the processing speed of SLE is not large enough to be an economical solution for a broader range of simple 2D or 2.5D processing tasks, such as through-glass vias (TGVs) for IC substrates. Typically, the glass section, which is modified with one laser pulse, has a length on the order of a few microns.

In contrast to SLE, laser-induced deep etching (LIDE) is making use of spatial and temporal beam shaping to create a significantly elongated interaction zone. The linear modification of the glass that can be induced with single laser pulses can reach up to several hundreds of micrometers. This offers the possibility to process the glass on the fly, which leads to a significantly higher processing speed. Spatially separated modifications turn into through- or blind-vias in the wet etching step. **Figure 1** shows the process flow of the LIDE technology for TGV formation that does not depend on a specific type of glass. Any silicate glass can be processed with LIDE,

although it might be necessary to adapt laser and etching parameters.

While single modification forms vias of various shapes, a continuous line of LIDE modification can be used to create cuts, simple or arbitrary shaped cavities in thin glass. **Figure 2** shows examples of glass cavities made by LIDE.

Glass thickness

As of today, glasses with a thickness of up to 500 μm can be processed in the described fashion. The surfaces of the glass sheets are typically unprotected during etching. Consequently, the thickness of the glass is also reduced by the etching process. The thickness reduction of the glass equals approximately the diameter of the TGVs.

Via diameter

The diameter of the via is determined by the etching time and the etch rate. In 50 μm -thin glasses, the minimum diameter accounts for 5 μm , while in 500 μm -thick glasses, the minimal TGV diameter is 50 μm . The maximum TGV diameter is unlimited in theory. However, due to practical limitations, TGVs with diameters well above 150 μm are typically not a domain for the LIDE technology. **Figure 3** shows a SEM picture of a TGV with a diameter of 20 μm in a 200 μm -thick borosilicate glass: Schott AF32eco.

Via shape and quality

If the glass is etched from both sides, the TGVs produced by LIDE technology have an hour-glass shape (**Figure 4**). The symmetrical taper angle is determined by the glass type and the etching conditions and is typically in amounts from 3° to 8°. By protecting one side of the modified glass from the etchant, v-shaped vias can be produced, which then feature the same taper angle through the entire glass. As

all recesses are cleared by a wet chemical etching step, all features are free of micro-cracks, chipping and thermally-induced stresses. This can be derived

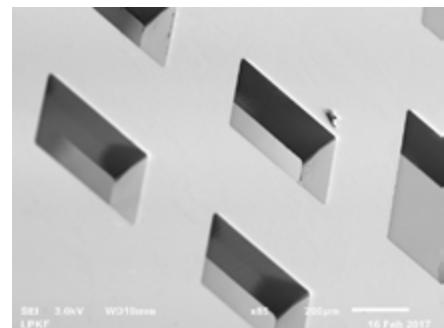


Figure 2: Scanning electron microscope (SEM) picture of rectangular glass cavities made by LIDE.

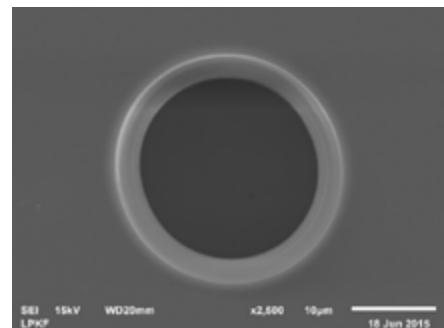


Figure 3: SEM picture: top view on a LIDE processed TGV.

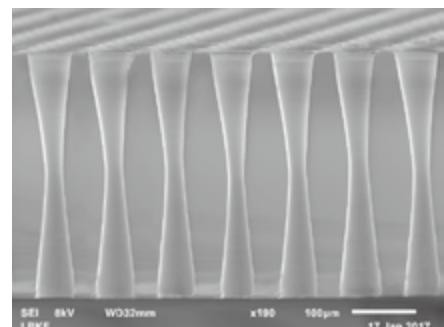


Figure 4: SEM picture of a cross section of LIDE-produced TGVs.



Figure 1: Laser-induced deep etching of through-glass vias.

from **Figure 5**, which shows an ultra-dense TGV array.

High-speed via formation with LIDE

The fundamental idea of the LIDE technology is the generation of continuous surface-to-surface modifications induced by single laser pulses. As a result, the laser head can be moved while the laser is pulsing on the fly without impairing the throughput or

accuracy of the processing tool. Laser processing speeds above 5000 TGV/s have been reported in [3].

Solid glass for advanced packaging

Glass is not a particularly new material in the field of electronics packaging. As an example, it has been found in the form of woven glass fabrics for decades. In this time frame, the average content of glass fibers in IC substrate materials has been continuously

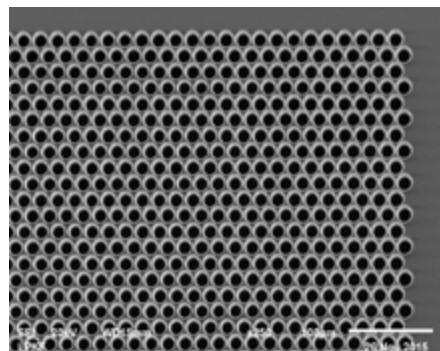


Figure 5: Ultra-dense TGV array in 200 μm -thick glass.

growing on account of the excellent RF and mechanical properties of glass.

Based on the above discussion, it's logical that many advanced packaging schemes rely on pure glass, and as such, also make use of some other benefits of solid thin glass, such as the small total thickness variation and low cost. Whether the glass is used in an interposer or as a solid glass core, the glass must feature micrometer-scaled high-precision and high-aspect ratios in such through-glass or in the cavities' recesses. On the other hand, glass is known as being difficult to process because any flaw induced by the processing leads to severe failures of the complete package. These problems of glass in advanced packaging are now resolved by LIDE.

Today's IC substrates typically have cores with a thickness of 400 to 800 μm . When changing to a solid glass core design, the intention is not to change the thickness of the core in the very same step, especially because handling of ultra-thin glass (200 μm) is more delicate than handling a reinforced woven glass.

Via formation in 500 μm -thick solid glass

To demonstrate the capabilities of LIDE and the Vitron 5000 laser tool to produce TGVs with the necessary properties for advanced packaging applications, a reference die pattern is processed and qualified. The laser tool is designed to process glasses up to 510x510mm² and 500 μm thickness.

The following tests were all conducted on aluminoborosilicate glass AF32eco from Schott with an initial thickness of 500 μm . The used reference die pattern as it is shown in **Figure 6** comprises 17,620 vias. The die has a size of 22.3 x 22.3mm² and the closest pitch in this pattern is 100 μm . The target hole diameter is 80 μm .

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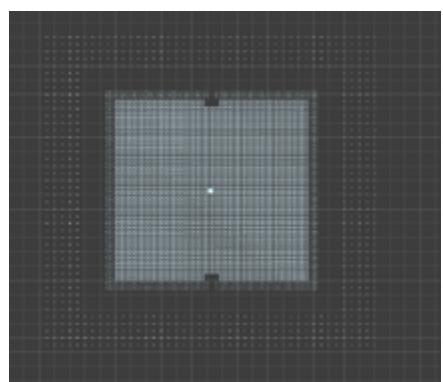


Figure 6: Reference pattern for one die.

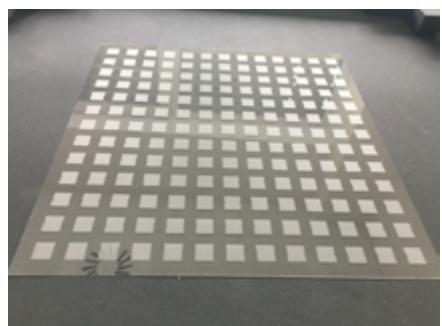


Figure 7: Glass panel with 13x13 dies.

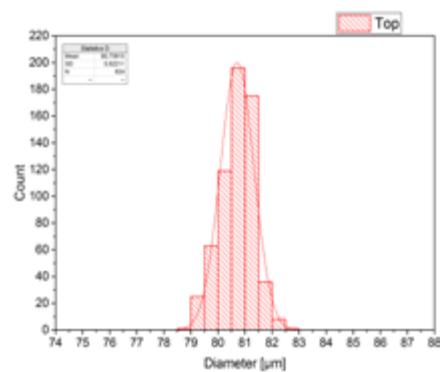


Figure 8: Via diameter distribution on the top side of the glass panel.

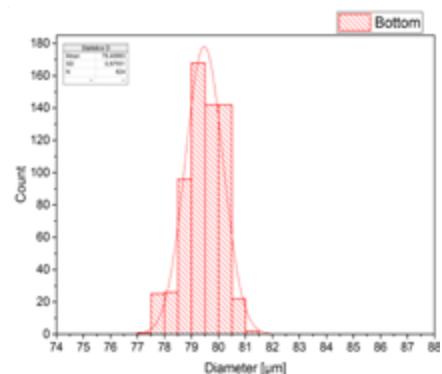


Figure 9: Via diameter distribution on the bottom side of the glass panel.

The reference die pattern is placed in 13 rows and 13 columns on a 300 x 300mm² panel resulting in total TGV counts of 2,977,780. The processed panel is shown in [Figure 7](#).

To check the capability of the LIDE process and the Vitron 5000, all the following measurements were done on a Werth Videocheck HA600 with an accuracy of 0.5μm + L/900 and a reproducibility of <1μm. A type 1 study of the Videocheck HA600 showed a standard deviation of the diameter measurement of 150 nm. On both sides of the glass, 624 TGVs were measured evenly distributed across the panel.

Diameter accuracy

As described above, the diameter of a TGV produced with LIDE is predominantly dependent on the etching conditions and time. For the panel shown in [Figure 7](#), the etching conditions and time were chosen to reach the targeted TGV diameter of 80μm.

The histograms of the diameter distribution of the panel are shown in [Figure 8](#) for the top side, and in [Figure 9](#) for the bottom side. The average top to bottom diameter variation is 1.9μm, and the standard deviation is 0.62μm on the top side, and

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0.67 μm on the bottom side of the panel.

Roundness

The roundness R of a via is dependent on the diameter D and its form tolerance FT, and can be derived from **Equation 1**.

$$\text{R} = (\text{D}-\text{FT})/\text{D} \quad \text{Eq. 1}$$

A histogram of the roundness of the 624 TGVs measured on the panel is shown in **Figure 10** (top side) and in **Figure 11** (bottom side).

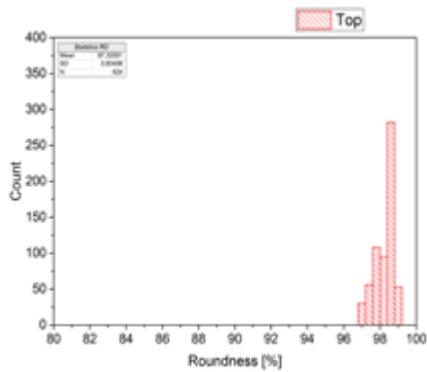


Figure 10: Via roundness distribution on the top side of the glass panel.

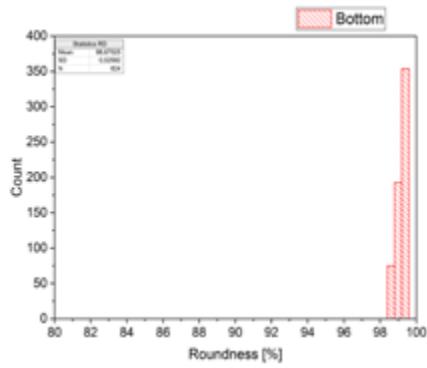


Figure 11: Via roundness distribution on the bottom side of the glass panel.

As the form tolerance is predominantly affected by the laser material interaction and only slightly influenced by the etching, the roundness values tend to become higher with the diameter, while the form tolerance remains stable.

Position accuracy

The histograms of the positional accuracy of the 624 TGVs are shown in **Figure 12** on both the x- and y-axes. The significantly higher standard deviation of the x-axis can be explained by the

machine kinematics of the Vitrion 5000. When processing a typical TGV pattern, one high-speed axis is traveling in the x-direction, while the axis in the y-direction is used for stepping forward, which is, of course, associated with a higher accuracy.

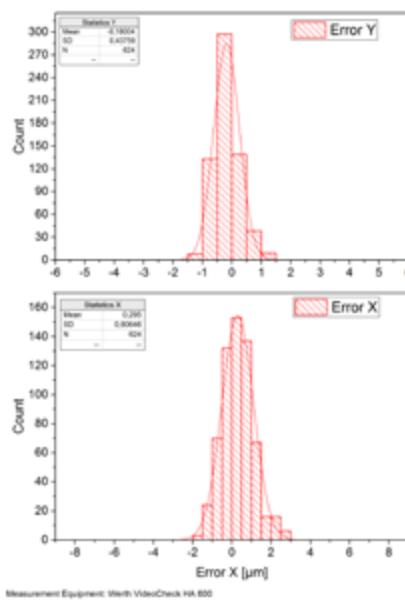


Figure 12: Accuracy distribution on the top side of the glass panel on both the x- and y-axes.

Throughput

The throughput of any TGV drilling technology depends on the used die pattern. The same applies, of course, to the TGV formation with LIDE. While the throughput of the Vitrion 5000 can theoretically reach values well above 5000 TGVs, some loose TGV patterns do not allow for these high numbers. Throughput values are only meaningful in conjunction with the die pattern with which these values are generated.

The panel shown in **Figure 7** features 2,977,780 TGVs and the laser processing was accomplished in 27.4 minutes. Thus, the throughput of the laser processing was 1,812 TGVs.

As etching is usually done in batches and the average processing time for the second processing step of one panel is strongly dependent on the batch size, etching tools, etching conditions and the targeted TGV diameter. Typical etching times are in the range of some tens of minutes.

Summary

Laser-induced deep etching is a new technology used to manufacture micrometer-scaled features of high-aspect ratio and utmost quality in thin glass sheets. It is demonstrated that TGVs produced with the Vitrion laser equipment and a TGV-rate of 1,812 TGV/s on a relevant die pattern fulfill all requirements of advanced packaging concepts relying on solid glass cores.

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Biographies

Roman Ostholt received his PhD in Mechanical Engineering at RWTH Aachen U. and is VP Technology Management at LPKF Laser & Electronics AG; email Roman.Ostholt@lpkf.com

Norbert Ambrosius received his Master in Mechanical Engineering at RWTH Aachen U. and is a Project Manager at LPKF Laser & Electronics AG.

Daniel Dunker received his PhD in Physics at TU Dortmund and is a Project Manager at LPKF Laser & Electronics AG.

Jean-Pol Delrue received his Executive MBA at HEC, Paris France, and completed a Post Doc. in Chemical Engineering at Stanford U., CA, USA, and his PhD in Physical Chemistry at UMH U., MONS, Belgium. He is the IC Packaging Business Development Manager at LPKF Laser & Electronics AG.

Lithography challenges for panel-level packaging

By Jack Mach *[Rudolph Technologies]*, and Ognian Dimov *[FujiFilm Electronic Materials, USA]*

The semiconductor industry developed around a technology based on creating devices on round silicon wafers. In recent years, device packaging technologies for these devices have become an important consideration in allowing the industry to continue to satisfy consumer demand for increasing performance in ever shrinking space. By default, many of these packaging technologies were developed for round, silicon wafer-like substrates, however there are significant advantages to be derived from using larger, rectangular substrates, commonly referred to as panels. Panel-level packaging (PLP) brings its own set of challenges, and its optimization requires the use of equipment and materials specifically designed to meet them.

Efficiency and throughput benefits

Square die do not fit well on round substrates. There is an inherent inefficiency near the wafer's edge, where squeezing as many die as possible onto the wafer inevitably results in part of the exposure field falling uselessly in the exclusion zone, or off the wafer entirely. On a rectangular substrate, the rectangular pattern from the mask can fit perfectly, ultimately increasing the average number of die per exposure and, by extension, the throughput of the exposure process.

Unlike silicon wafers, panels can be produced easily at almost any size. A larger substrate increases throughput by reducing the nonproductive time spent exchanging substrates. Moreover, the same considerations that have historically driven increases in wafer size also apply to non-round, non-wafer substrates, potentially providing substantial gains from using large panels throughout the manufacturing process.

A model designed to compare 300mm round substrates with 650mm

X 550mm panels [1] demonstrated significant benefits. The improved fit between die and substrate resulted in roughly 10% improvement in surface utilization. The larger size of the substrate and the improved fit between the mask and substrate reduce the transfer overhead by 5X. In this comparison, the panel-based process was estimated to reduce lithography cost per die by as much as 40%. Another study [2] estimated even greater cost reductions with further increases in panel size.

Challenges/solutions

Suppliers and device manufacturers, working to develop panel-based packaging processes that take advantage of panels' inherent benefits, face a variety of challenges, which can be grouped conveniently into two categories: equipment and materials.

Equipment. Advanced packaging (AP) lithography confronts a set of challenges that are unique to the application. Feature sizes range from micrometers to hundreds of micrometers and often require photoresist or dielectric layers much thicker than those found in front-end photolithography. The lithography system must be able to supply enough energy to activate the photosensitive material (e.g., resist, polyimide, dielectric, etc.), while maintaining focus throughout the thicker layers to precisely control critical dimensions (CD) and sidewall profiles. Some types of photosensitive materials emit significant amounts of gas during exposure that can contaminate optical elements located close to the wafer surface. A wide variety of substrates are used, including reconstituted wafers (in which separated die are embedded in a polymer compound), glass, and more. The substrates may exhibit several millimeters of warp, significant die-to-die displacement, and substantial inter- and intra-

die topography resulting from the embedding and bumping processes.

The exposure tool used in this study (JetStep® S3500, Rudolph Technologies) is specifically designed to address these challenges [3]. It has a large exposure field (52mm X 66mm) and provides a combination of resolution and depth of focus optimized for the feature sizes and resist thicknesses used in AP applications. A large working distance (between the objective and the substrate) greatly reduces the risk of contamination and the need for maintenance, and allows room for an on-the-fly autofocus system. The 2X optical reduction reduces the cost of masks. The optical design permits fast, easy adjustments of focus, alignment and magnification to accommodate warpage and other variations in substrate topography. The stage and substrate handler are specifically designed to transfer and flatten large panels.

The system is also designed to work within a feed-forward metrology loop that measures positioning errors of die on the substrate outside of the exposure tool. This approach eliminates the need to realign the exposure field within the stepper, which otherwise may account for as much as two thirds of an exposure cycle [4].

Materials. The warpage typical for large panels also presents several serious challenges for lithography processes from a materials perspective. For advanced applications, the requirements for higher resolution have driven film thicknesses down to ~5.0µm, with resolution requirements currently at 5.0 µm, and 2.0 µm performance expected to be required in the very near future. Suppressing the stress and warpage of panels requires dielectric materials with low curing temperatures (<200°C) and low curing shrinkage. Processing of such thin films on large format panels with different surface roughness and

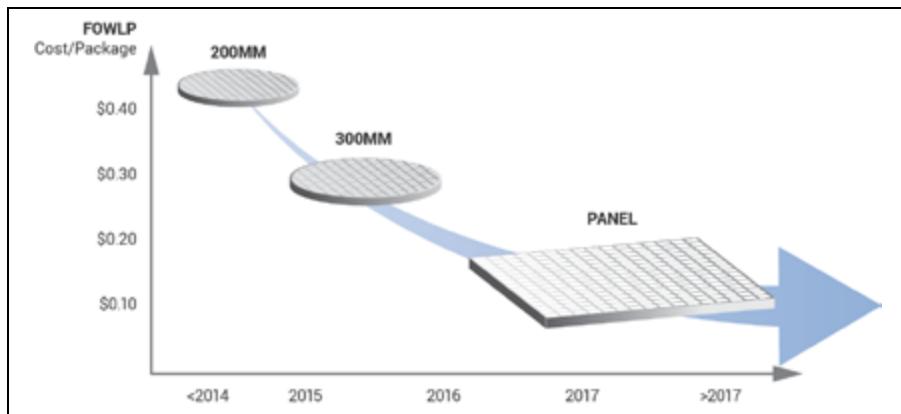


Figure 1: A Yole Développement study predicted significant cost reductions with panel-level packaging. The graph illustrates the example for 8x8mm packages with single-die embedding.

Performance Criteria	FCPi-2100
Thermal Film Shrinkage	170 – 200°C +1% RT – 200°C +4%
Maximum Bake Temperature Requirement	170 – 200°C
Dry Film Thickness (range)*	4-50µm
Elongation-to-break	60%
CTE	45 ppm/ ^o K (below Tg)
Modulus	1.8 GPa
Water Uptake (@ RH of 60%)	<1%
Chemical Resistance	OK
Dielectric Constant ε(k)	3.2 @ 1 GHz
Loss tan δ	0.015
Aspect Ratio (Resolution)	~ 2
Photospeed (BB & I-line Exposure)	<250 mJ/cm ² (at 5mm FT)

Table 1: Specifications of FCPi-2100 photo-imageable dielectric material.

properties is a challenge.

Other challenges include application method, stability (over longer job and queue times), and the ability to accommodate varying textures, and surface properties, such as, roughness, developer wettability, and reflectivity. A number of manufacturers are developing different technologies, so there is a lack of standardization. As a result, panels are being produced with different materials, formats, appearance, and surface properties. Glass panels are very smooth, while organic laminates and molded substrates may be very rough. Lithography materials and tools are expected to perform well on all these different types of panels, but the substrates can

create particular challenges during coating/lamination and exposure and development, including the following: 1) adhesion issues after lamination or development, 2) footing and residues after development, 3) loss of resolution due to scattering, 4) diffusion of aerial image at the interface with the panel, and more.

The spin coating process, which is typical for round wafers, is not applicable for large rectangular substrates. The alternatives for coating panels are spray/slitz coating or lamination with dry film. Among these options, slit coating and lamination of dry films are more mature and the equipment is available even for large panel formats. Both processes have challenges in advanced packaging applications where the films are becoming thinner as processes require higher resolution. Slit coating has difficulties in producing thin films with uniform thickness across the panel on warped substrates. There can also be issues with local uniformity around patterns from previous layers. The lamination of dry films has inherent advantages because it is a much simpler process with high throughput and efficient use of materials. Typically, a softbake or post-application bake after lamination is not needed, eliminating a process step and associated equipment from the line.

The material used in this work (FCPi-2100, Fuji) is a negative tone, photo-imageable dielectric material (PID) designed for advanced packaging applications. It is available as dry film and as a liquid dielectric material. Key performance data are shown in **Table 1**.

Results. To evaluate the performance of the exposure tool and the material, a focus-exposure matrix was created using a test reticle containing lines and vias of various sizes, a JetStep exposure system and dry film FCPi-2100. **Figures 2–5** summarize the results of the evaluation.

Summary

The lithographic challenges of panel-level processing can be met with a combination of equipment and materials that are designed for the

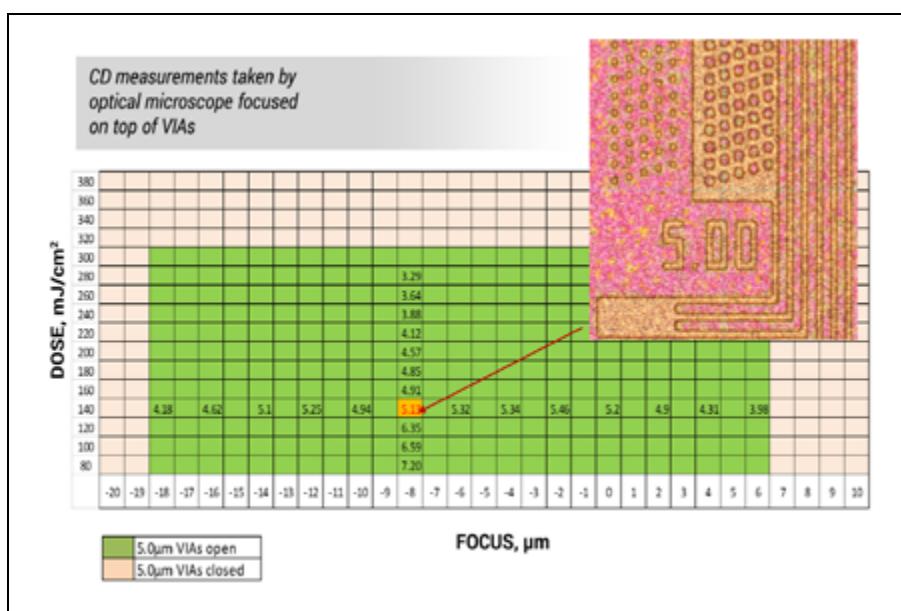


Figure 2: Focus exposure matrix overview of open 5µm vias using JetStep exposure tool and Fuji FCPi-2100.

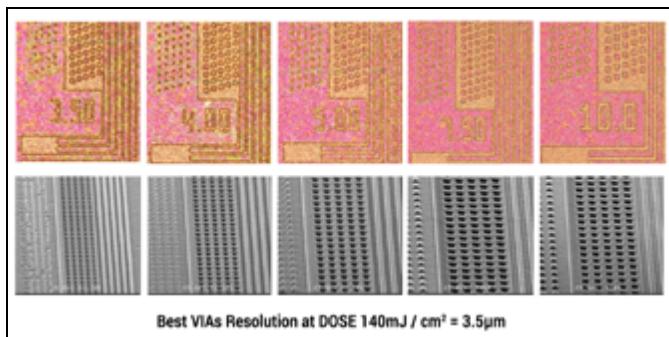


Figure 3: Images of open vias down to 3.5 μm diameter. The vias' resolution is at an exposure dose of 140mJ/cm 2 and F=-8 μm .

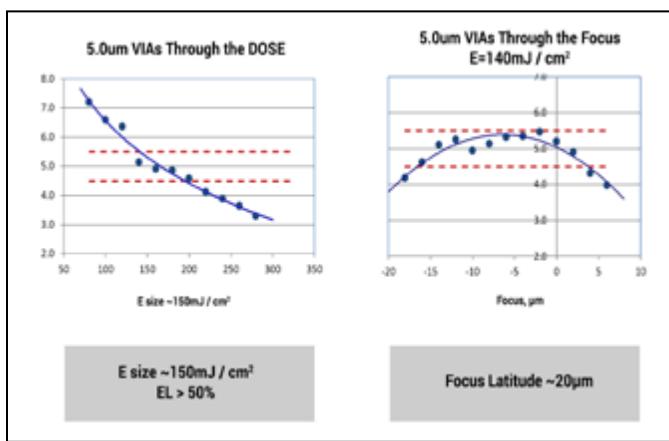


Figure 4: Exposure and focus latitude of 5 μm vias exposed by a JetStep 3500 system in FujiFilm FCPi-2100.

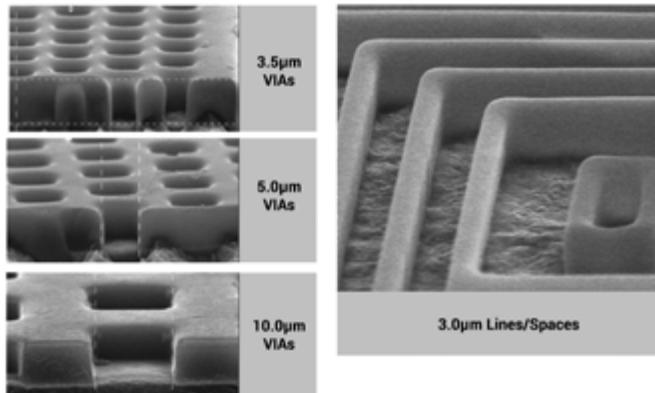


Figure 5: High-resolution images of vias and lines at E=140mJ/cm 2 , F=-8 μm .

application. The exposure tool needs a large field with an appropriate combination of resolution and depth of focus. It must also accommodate the rectangular shape, large size and varying topography of the substrate. The materials require low shrinkage, long queue time stability, and the ability to conform to the warped panels with large surface roughness and topography, in addition to fast exposure, high contrast, and fast development rate. A properly optimized material coupled with a suitable lithography system can result in more devices in a shorter amount of time, yielding greater productivity.

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Biographies

Jack Mach received his Bachelor of Electronic Engineering Technology degree from Wentworth Institute of Technology, and is an Applications Engineer at Rudolph Technologies; email jack.mach@rudolphtech.com.

Ognian Dimov received his Master of Science degree in Physics from Sofia U., Bulgaria, and is a Senior Associate Engineer at FujiFilm Electronic Materials, USA.

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Relieving stress in flip-chip solder joints

By Ephraim Suhir [Portland State University]

After flip-chip (FC) technology was suggested about fifty years ago, it rapidly became the architecture of choice because of the need to minimize the real estate occupied by an integrated circuit (IC) package. FC solder joints provide both electrical connection and mechanical support for IC chips, which makes FC designs mechanically vulnerable and prone to physical failures. Various measures (e.g., "dummy" solder joints) were suggested over the years to improve the situation. In particular, a variety of encapsulating, mostly "underfill" technologies (**Figure 1**)

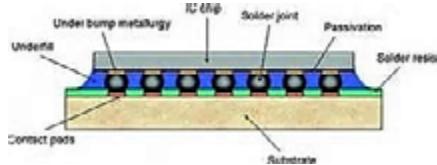


Figure 1: Flip-chip (FC) assembly.

1) were introduced. The published experimental and modeling investigations of the mechanical reliability of FC designs with underfills are numerous (e.g., [1, 2]).

It has been recently shown [3] that there exists an opportunity for avoiding inelastic strains in the second-level (package-to-PCB) solder joint interconnections in IC packages. This could often be achieved by employing joints with elevated stand-offs and/or by using inhomogeneous solder joint systems in which the solder material at the peripheral portions of the assembly has 1) a lower modulus, and/or 2) a higher yield stress, and/or 3) a lower melting temperature, than the solder material in its mid-portion, or 4) if an epoxy adhesive is employed at the assembly corners. If such an effort is successful, the inelastic strains in solder joints are avoided, and the fatigue strength of the material will improve dramatically. But what about the first level (chip-to-substrate) interconnections and particularly FC designs, and especially those with underfills? Are the findings and recommendations obtained for the second level of interconnections applicable to the

first level as well? What could possibly be done to relieve stresses in FC solder joints, and could this be done to an extent that inelastic strains are avoided, or, if this is impossible, could at least the sizes of the inelastic peripheral zones be established and minimized? Some answers to these questions obtained using analytical modeling [4] are set forth below.

FC assembly with underfill: could a bi-material model be used?

For about thirty years now, analytical thermal stress models for adhesively-bonded assemblies (refs. [5,6] have attracted over 500 citations) have been widely used and deemed effective. They are applicable if the bonding layer is much thinner than the bonded components and/or if its modulus is significantly lower than the moduli of the bonded materials. While the modulus and thickness of the adhesive layer are important, because they determine the interfacial compliance of the bond that acts as a strain buffer between the dissimilar materials of the assembly components, its coefficient of thermal expansion (CTE) is not. The "bond" in the FC assembly is, however, a complex composite structure comprising high-modulus solder joints (especially if lead-free solder is used) and an underfill. This "bond" is not thin (especially if joints with elevated stand-offs are considered [7]) and its effective modulus and CTE have a significant effect on the induced stresses. A trimaterial model [8] has to be used, therefore, to evaluate the induced stresses. In the example from [9], the highest shearing stress occurs at the chip-“bond” interface and are by a factor of 2.45 higher than the stress at the substrate-“bond” interface, but even the latter stress is about twice as high as the stress predicted using the bi-material model. As to the normal stresses acting in the cross sections of the assembly components, the tri-material model predicts that the highest stress occurs in the chip, and the lowest in the substrate. Furthermore, while the bi-material model simply assumes that the normal stresses in the “bond” are zero, the stresses in the cross

sections of the encapsulated solder are not low at all, rather, they are about 59% of the stresses in the chip. The normal stresses in the chip predicted by the bi-material model are only about 78% of the stress obtained using the tri-material model. The normal stresses in the substrate predicted by the bi-material model are, however, almost twice as high as the tri-material model predicts, but these stresses are low anyway.

Is it important that the entire under chip area is underfilled?

From the induced stresses standpoint, only the end portions of a bonded assembly should be securely bonded [10], and the lengths of these portions should not be below $L = \frac{s}{k}$ where k is the parameter of the interfacial shearing stress. This parameter is different in a bi- and in a tri-material assembly. The rationale behind this requirement is that the maximum interfacial shearing stress $\tau_{max} = kT \tanh kl$ can be evaluated as the product of the parameter k , the maximum force T in the mid-portion of a sufficiently long chip, when the stress at its interface with the “bond” is of interest, or the maximum force in the mid-portion of the substrate, when the shearing stress and the substrate-“bond” interface is sought, and l is half the encapsulated/“bonded” length.

Applying the above formula to the bonded peripheral portions, it can be seen that the maximum shearing stress will not change if the bonded length is sufficiently large, so that the hyperbolic tangent in this formula is close to 1.0, and this takes place if the condition $L = 2l \geq \frac{s}{k}$ is fulfilled. In the numerical example [11], $k = 3.0925 \text{ mm}^{-1}$, and the lengths of the peripheral encapsulated zones should not be smaller than $L = \frac{s}{k} = \frac{5}{3.0925} = 1.62 \text{ mm}$. Such a small length seems to be sufficient to cover and strengthen just the very extreme solder joints. The predicted maximum interfacial shearing stresses in this assembly are $\tau_{max} = 20.19 \text{ kg/mm}^2$ at the chip-“bond” interface and $\tau_{max} = -8.25 \text{ kg/mm}^2$ at the substrate-“bond” interface.

Thermal stress model for a typical FC package design

The architecture in **Figure 2** consists of a FC bonded to an organic substrate and covered by an organic lid. The lid is configured in such a way that its mid-portion is bonded to the back side of the chip using a thermal interface material (a heat sink is intended to be subsequently

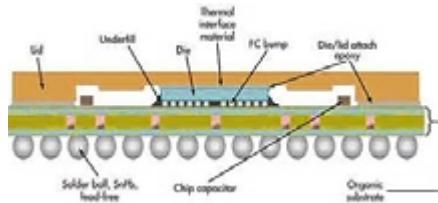


Figure 2: Typical FC package architectures.

mounted on the outer surface of the lid) and its peripheral portions are adhesively bonded around the lid's perimeter to the same substrate. The following sequence of actions [12] can be used to determine the induced stresses. First,

the mid-portion of the design is considered as a tri-material assembly that consists of the FC ("zero" component), the mid-portion of the organic substrate (component #1) located below the chip, and the mid-portion of the lid (component #2) located above the chip. The assembly is subjected to the combined action of the internal thermally-induced forces caused by the dissimilar materials of the assembly (the chip, the substrate and the lid), and by the so far unknown external forces applied to this assembly \hat{f} from the peripheral portions of the design. These peripheral portions of the design that consist of the thick peripheral portions of the lid and the peripheral portions of the substrate are considered at the second step of the effort. The external forces should be, of course, \hat{f} the same for the substrate and the lid of the tri-material assembly in the mid-portion, and for the substrate and the lid of the bi-material assemblies at the design's peripheral portions. The magnitude of the forces \hat{f} could be determined from the condition of the compatibility of the displacements at the extreme cross sections of the design's mid-portion and its peripheral portions. The numerical example [12] carried out for the temperature change of $\Delta t = 180^\circ\text{C}$, and here are some calculated data.

Forces acting in the mid-cross section of a long mid-portion of the assembly are as follows:

- 1) In the chip: $T^* = -7.052 \text{ kg/mm}$
- 2) In the substrate: $T_l^* = -4.611 \text{ kg/mm}$
- 3) In the lid: $T_o^* = -2.441 \text{ kg/mm}$

Forces acting in the mid-cross section of a long peripheral portion of the assembly are as follows:

- 1) In the lower portion of the lid:
 $T_o^* = -0.211 \text{ kg/mm}$,
- 2) In the substrate: $T_l^* = -0.632 \text{ kg/mm}$;
and
- 3) In the upper portion of the lid:
 $T_o^* = 0.421 \text{ kg/mm}$

Parameters of the interfacial shearing stress are as follows: for the assembly's mid-portion: $k = 0.916 \text{ mm}^{-1}$ and for the assembly's peripheral portions: $k = 1.256 \text{ mm}^{-1}$

The "external" force (between the mid-portion and the peripheral portions of the assembly) is: $\hat{f} = 1.552 \text{ kg/mm}$.

Normal stresses are as follows:

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- 1) In the chip $\sigma_0 = -14.104 \text{ kg/mm}^2$
- 2) In the mid-portion of the substrate:
 $\sigma_1 = 3.059 \text{ kg/mm}^2$
and
- 3) In the mid-portion of the lid:
 $\sigma_2 = 3.993 \text{ kg/mm}^2$

Maximum interfacial shearing stresses:

- 1) In the design's mid-portion at the chip-substrate interface are given by:
 $\tau_1 (\pm l_m) = \mp 5.647 \text{ kg/mm}^2$
- 2) In the design's mid-portion at the chip-lid interface $\tau_1 (\pm l_m) = \mp 3.993 \text{ kg/mm}^2$
- 3) In the design's peripheral portion at the chip-substrate interface at its boundary with the mid-portion $\tau_1 (l) = -1.156 \text{ kg/mm}^2$
- 4) In the design's peripheral portion at its free boundary $\tau_1 (-l) = -0.793 \text{ kg/mm}^2$
- 5) In the design peripheral portion at the chip-lid interface at its boundary with mid-portion $\tau_1 (l) = -2.478 \text{ kg/mm}^2$, and
- 6) In the design's peripheral portion at the chip-substrate interface and at its free boundary $\tau_2 (-l) = 0.529 \text{ kg/mm}^2$.

The assembly in the mid-portion of the design is identified here as a tri-material assembly, although it is comprised, in effect, of five materials. In addition to the three major components, it also contains materials that are two thin layers: an encapsulated solder joint layer, and a thermal interface layer. These two layers are thin and/or low modulus, so that they do not generate thermally-induced forces acting in their cross sections. These layers experience interfacial stresses only, and affect the magnitude and the distribution of these stresses. This is also true as far as the assemblies at the peripheral portions of the design are concerned: the adhesive bonds in them do not experience tension or compression, are subjected to shear deformations only, and therefore, do not have to be considered in the equilibrium conditions for the induced forces.

An inhomogeneous solder joint system for stress relief

Suggestions made for the second level of interconnections, as far as the application of an inhomogeneous solder joint system is concerned, are applicable also to the FC designs. Significant stress relief can be achieved by using solder joints with elevated stand-offs [13]. Such joints have elevated interfacial compliance and owing to that lead to lower interfacial stresses. One should have in mind, however, that systems with elevated stand-offs add weight to the structure, and if drop tests are considered, such systems are, for the same

drop height, more vulnerable than designs with conventional joints [14]. Inhomogeneous solder joint system designs, in which the solder materials at their peripheral portions have lower Young's moduli [15] and/or are applied at a lower reflow soldering temperature [16], or when epoxies are employed at the assembly ends [17] are as advisable as they are for the second-level interconnections. Here is how the induced shearing stresses can be minimized.

The shearing stresses in the mid-portion of an assembly with an inhomogeneous solder system increase from zero at the assembly's mid-cross section to its maximum values at the boundaries with the peripheral portions. At the inner boundaries of the peripheral portions, the stresses drop to low values, then increase again and reach their maxima at the free ends of the assembly. Optimized stress relief [18] can be achieved if the lengths of the low-modulus peripheral portions are established in such a way that the two stress maxima, at the boundary of the mid-portion with the peripheral portions and at the assembly ends, are made equal. In such a case, each of these maxima turn out considerably lower than the maximum stresses at the ends of the assembly with a homogeneous bond. Strange as it may sound, the lowest interfacial stresses can be achieved with stiffer mid-portions [19]. This is because such mid-portions result in low peripheral displacements and, hence, in lower interfacial stresses at the assembly's peripheral portions. It is this phenomenon that explains the stress relief in quad flat no-leads (QFN) assemblies [20]. If the inelastic strains in the peripheral solder joints cannot be avoided, then the lengths of the peripheral portions experiencing inelastic strains could and should be evaluated [21]. The number of the peripheral joints that experience inelastic strain is important, because the fatigue lifetime of the interconnection, whose peripheral joints experience low cycle fatigue conditions, is inversely proportional to the number of joints that are simultaneously subjected to inelastic strains.

Possible accelerated tests and next-generation of qual tests

The most widespread accelerated and qualification test procedures today are those for temperature cycling. Such testing is expensive, time- and labor-consuming, and its results might be misleading, because material properties are temperature-dependent and the elevated range of testing temperatures might trigger failure modes and mechanisms that will never occur in field conditions. Because of that, there are suggestions to replace temperature cycling with other types of loading, such as random vibrations (e.g., [22]). The highest thermal stresses occur at low-temperature conditions, and it is the combination of

low temperatures and repetitive dynamic loading that is able to dramatically accelerate propagation of fatigue cracks, whether elastic or inelastic. A modification of the recently suggested Boltzmann-Arrhenius-Zhurkov model [23] is developed and reduced to practice [24] for the evaluation of the fatigue lifetime of the second-level solder joint interconnections, but the approach is equally applicable to the FC interconnections. Random vibrations are considered as a white noise of the given $(\text{m/s}^2)^2/\text{Hz}$, which is the ratio of the acceleration amplitudes squared to the vibration frequency. If there is confidence that no inelastic deformations are possible, the probabilistic Palmgren-Miner rule [25] should be applied.

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Biography

Ephraim Suhir is on the faculty of the Portland State U., Portland, OR, USA, and Technical U., Vienna, Austria. He is also CEO of SBIR ERS Co. in Los Altos, CA, USA, and a Contributing Editor to *Chip Scale Review*; email suhire@aol.com



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Challenges in automotive package development

By Shaun Bowers [Amkor Technology, Inc.]

Automotive package development in outsourced semiconductor assembly and test suppliers (OSATS) is a natural extension of the market forces that established the OSAT market in the 20th century. The motivation to re-use technology, cross-pollinate approaches, standardization, and a lower barrier to entry for new package types all apply to automotive as well as standard OSAT packaging services. The trend to adopt new and varied package types to automotive applications is a direct response to the market forces that are increasing the semiconductor content in automobiles at an exponential rate. Whether a future car is considered a rolling smartphone, a rolling supercomputer, or a rolling artificial intelligence (AI)-enabled taxi, the quantity of integrated circuits per vehicle will continue to increase as carmakers rely on sensing, CMOS and solid-state devices for safety, performance, infotainment and vehicle autonomy functions.

Although the market forces outlined above push suppliers to adjust the way they approach automotive package development, the core objectives to address reliability and device performance have stayed static. Material selection, bond integrity, adhesion

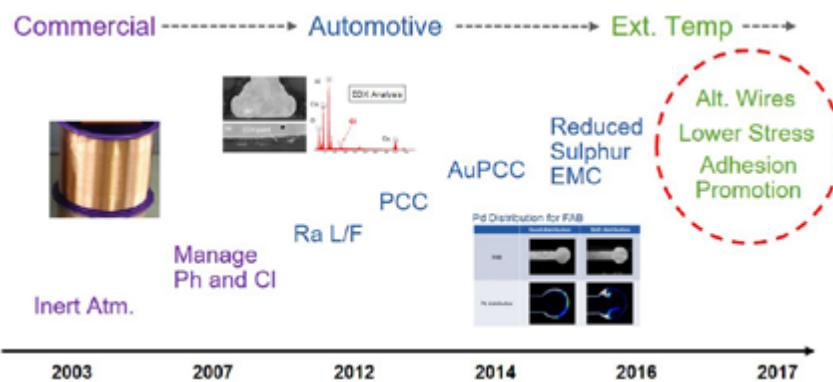


Figure 2: Evolution of Cu wire. SOURCE: Amkor Technology, Inc.

promotion and stress management remain the core of the package development objectives no matter the package format or function (Figure 1).

How package development activities are directed to address the market will greatly influence the ability to accelerate the adoption of new automotive packages. To become an automotive powerhouse, OSATS must change the way data is analyzed, adjust the test vehicle (TV) design and experimental approach, and dedicate resources specifically to automotive testing and analysis.

Automotive testing and test to failure

Failure mechanism (FM)-based testing is widely acknowledged as the accepted methodology to determine automotive fit for use. The use of the Automotive Electronics Council's (AEC's) AEC Q100, Q006 and Q101 specifications is common to evaluate new materials and semiconductor package types for automotive applications. Because copper (Cu) wire is mechanically more rigid, has low resistance, and is slower to develop intermetallics vs. gold (Au) wire, the use of Cu in automotive applications is ideal. The evolution of Cu wire bond has had many iterations (Figure 2), including how to form the bond, what

materials to use, and what environment in which to keep the device to ensure bond integrity.

As the survivable number of cycles (per AEC Q006 testing) is extended for Cu wire, key challenges in automotive package development start to be revealed. With a more capable material and an extended test spec, the amount of data on time to failure becomes rare due to the length of the test. It is not uncommon for some devices to exceed two or three times the defined envelope in AEC Q006, so failures in devices put into reliability testing nine months ago, have yet to occur.

In many ways, development and manufacturing groups are at odds for automotive applications. The manufacturing group does not want to see failures, but the development group needs to see them to learn, validate assumptions and make improvements. The only option seems to be to wait. This is in conflict with the market forces that want to adopt new packages quickly.

Automotive development groups have ways to adjust to this new reality, however. The long time to data dictates the adoption of aggressive test vehicles to force early failures in the testing of materials and designs. It necessitates the addition of purposeful variability to obtain meaningful A



Figure 1: Automotive development methodology.
SOURCE: Amkor Technology, Inc.

vs. B data from the experimentation (**Figure 3**). The benefit is that once success in aggressive testing schemes is achieved, it is easily adopted along a broad package envelope.

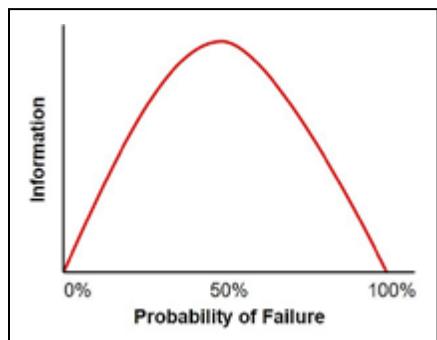


Figure 3: The use of purposeful variability for more meaningful data. SOURCE: "The Principles of Product Development Flow," Donald G. Reinertsen

Automotive design rules

The transition from Au to Cu wire in automotive products has also introduced the requirement for destructive analysis into the testing schedule (**Table 1**). Instead of merely

testing electrical response as in Q100, the Q006 test procedure requires destructive analysis of the devices after the environmental testing for devices with Cu wire.

Ensuring bond integrity after temperature cycling (TC), highly-accelerated stress

testing (HAST) and high-temperature storage (HTS) requires new design best practices (**Figure 4**). Ensuring that the device has no delamination in critical areas post-testing requires new materials best practices. Accepting that bond integrity,

	Read Point	Mold Compound Delamination Acceptance Criteria	Electrical
Qualification Requirements	T ₀	No delamination at first (ball) or second (stitch/wedge) bonds unless otherwise agreed between supplier and user.	All components passing production test
	Post MSL PC	No delamination at first (ball) or second (stitch/wedge) bonds unless otherwise agreed between supplier and user.	All components passing production test
	1X for AEC Q100 grade X or AEC Q101	No delamination at first (ball) bond. If any (stitch/wedge) bond delamination found – no heel cracks.	All components passing production test
	2X for AEC Q100 grade X or AEC Q101 (TC included if no BLR performed)	Evaluate the severity of any bond delamination found per Sections 5.2 and 5.3.	All components passing production test

Minimum CSAM sample size: EITHER the same 11 components per lot through each readpoint (preferable)
OR 22 random components per lot at each readpoint.

Table 1: AEC Q006 delamination criteria.

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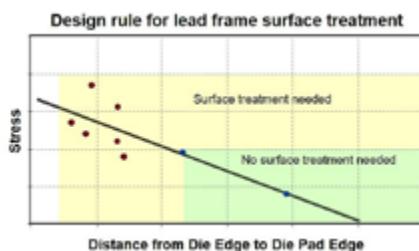


Figure 4: Automotive design rule example—roughened surface.

stress management and adhesion promotion all play roles in these best practices, then new design elements must be adopted early in the development process. The data gained from the aggressive test vehicles allows the validation of the new design elements. Determining when to use a certain technology or material can be tied directly to the results of the testing.

Automotive materials

With the aggressive TV and design-of-experiment (DOE) regimen established, it is now possible to perform A vs. B experiments on different materials. This allows the demonstration of the reliability response for items such as Au palladium-coated copper (AuPCC) vs. alloy wire selection, effect of ionic and/or corrosive materials within compounds, and the effect of roughened surfaces and mechanical design elements. The net result is that the findings enable confidence in material sets for devices specifically targeted to automotive applications.

The time elements of this testing remain lengthy and onerous. Although difficult, it is advantageous to develop accelerated testing to achieve results sooner. The industry has looked at increasing amplitude (temperature), frequency and order of operation to shorten

the time to data (**Figure 5**). All of these have merits and boundaries, but accelerated failure mechanism testing will shorten the time to data. If adopted and agreed upon, this will allow more development cycles in the given timeframe, and make iterative approaches easier to analyze.

New package types not covered by Q100 and Q006

As the automotive market matures, it will command the use of nontraditional form factors that are common in other, less rugged applications (**Figure 6**). In some cases, the specifications and documentation are lagging the technical capabilities. For example, it is possible for wafer-level

will be relied upon to bring these to market. Automobiles will continue to integrate functions dominated by sensing, CMOS and solid-state electronics applications like computing, communications, environmental/mechanical sensing and AI. As a result, a host of package types can be expected to be developed and deployed in automobiles such as WLCSP, flip-chip ball grid array (FCBGA) and embedded packaging along with more traditional laminate and lead frame packages.

Development activities will continue to be focused on bond integrity, adhesion promotion, materials and stress management. Whether the bonding approach uses copper pillar bumps (CuP),

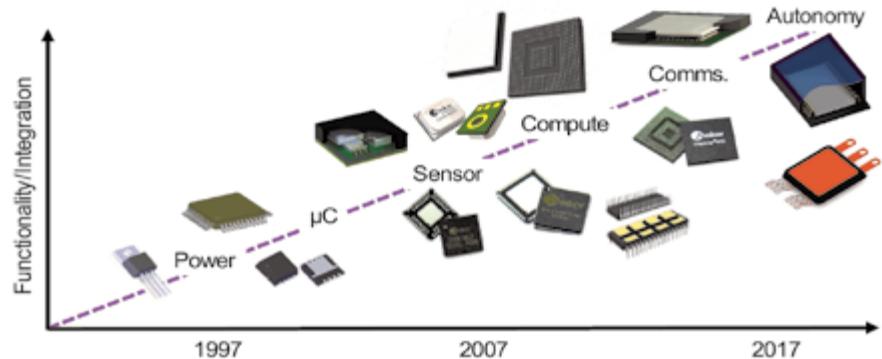


Figure 6: Adoption of package types over time in automotive applications.

chip-scale packaging (WLCSP) to pass AEC Q100 testing, as the testing schemes are directed towards showing failure modes common to traditional wire bond technology. However, passing Q100 does not necessarily mean that the package type is good for automotive applications. In WLCSP, it is rather easy to pass post-test delamination criteria because there is no mold interface. WLCSPs are commonly underfilled on a printed circuit board (PCB), thereby creating the interface in question. In this example, AEC testing is required to be done on the device (e.g., preconditioning +TC), but board-level reliability (BLR) testing might be more appropriate. This is one area where standards groups need to adapt to technology and consider different failure modes as a part of that effort.

alloy wire, hybrid wire, lead-free solder or other emerging techniques, bond integrity remains a key area of analysis. Testing requirements will involve destructive testing; therefore, adhesion promotion and stress management will be key to meeting the environmental reliability envelope of a vehicle application. Significant energy is expected to be spent to eliminate the failure-creating intermetallic compounds (IMCs) altogether, and to develop accelerated tests that enable more frequent cycles of learning. Development groups will need to adjust to keep up with the breadth and pace of automotive package development, and the OSAT community is uniquely positioned to create the required innovations.

Biography

Shaun Bowers received his BSME from Gonzaga U. and is VP, Mainstream Package Development and Technology Integration at Amkor Technology, Inc.; email shaun.bowers@amkor.com

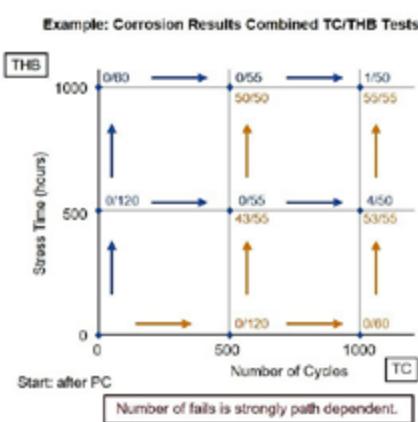


Figure 5: Graph of test order and effect on FM testing. SOURCE: Infineon Technologies

Future areas of interest/development for automotive applications

Looking forward to the future, two things are certain: 1) the automotive market will continue to grow and expand into new packaging types, and 2) the OSAT industry



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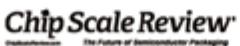
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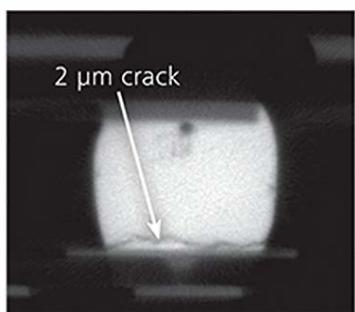
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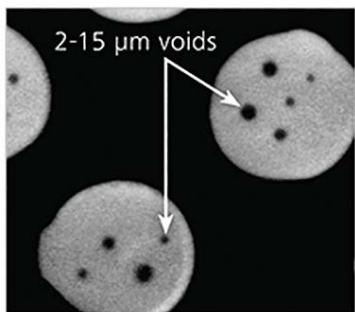
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