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R E V I E W

*The International Magazine for the Semiconductor Packaging Industry*

Volume 18, Number 3

May • June 2014

## Enabling a multiple processor SiP with 2.5D TSVs

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- 3D packaging for analog and power products
- Met-Via TSV interposer for CMOS biosensors
- Next-gen laser structuring for higher density packages
- Active interposer for high-performance C2C connections





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Open-Silicon, Inc.'s demo board showcases the benefits of 2.5D SiP technology with two SoCs powered by ARM Cortex™-A9 processors. The SoCs were manufactured on GLOBALFOUNDRIES' 28nm-SLP (Super Low Power) process technology. Amkor Technology, Inc. assembled the logic chips across a 65nm silicon interposer. The design enables high-bandwidth communication and demonstrates several advantages of 2.5D packaging.

Photo courtesy of Open-Silicon, Inc.

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REVIEW  
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*The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.*

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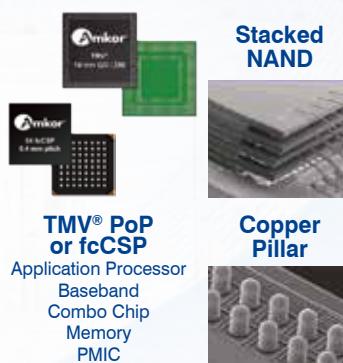
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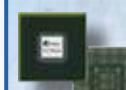
CABGA/FBGA  
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Audio Codec  
Baseband  
Camera Module  
RF



SCSP  
Memory  
Baseband  
RF



WLCSP  
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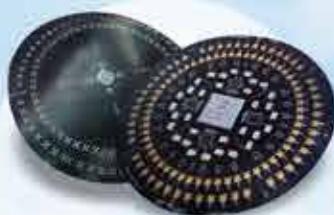
**Logic Test  
Socket**



**RF** Coaxial Spring  
Probe & Impedance  
Controlled Socket



**Probe Head**



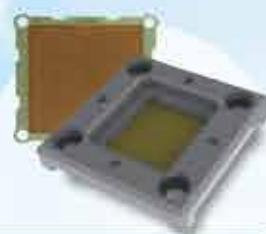
**Wafer Level CSP  
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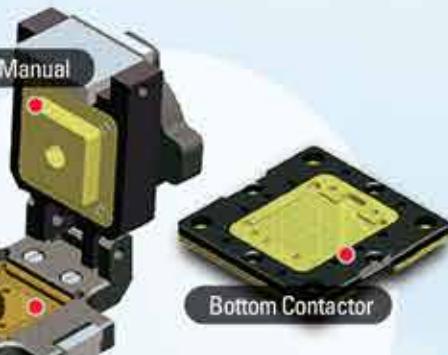
**Memory  
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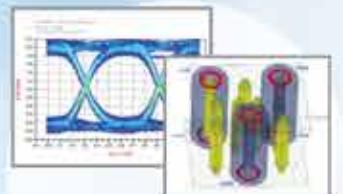
**Elastomer  
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**PoP Test  
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**Spring Contact  
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**Electrical Analysis**

CCC Test, HFSS, TDR  
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Subscriptions in the U.S. are available without charge to qualified  
 individuals in the electronics industry. Subscriptions outside of the  
 U.S. (6 issues) by airmail are \$100 per year to Canada or \$125 per  
 year to other countries. In the U.S. subscriptions by first class mail  
 are \$95 per year.

Chip Scale Review, (ISSN 1526-1344), is published six times a  
 year with issues in January-February, March-April, May-June, July-  
 August, September-October and November-December. Periodical  
 postage paid at Los Angeles, Calif., and additional offices.

POSTMASTER: Send address changes to Chip Scale Review  
 magazine, P.O. Box 9522, San Jose, CA 95157-0522

Printed in the United States

## FROM THE PUBLISHER

For those of you attending ECTC and SEMICON West this year, this expanded edition of Chip Scale Review brings 9 technical features and 4 columns on a broad array of topics that will give you plenty to think about as you plan your show visits. Also included is the first in a series of executive profiles. We also continue with another R&D Institute profile in a series that started earlier this year.

A technical focus of this issue is the results of a collaborative effort – represented by the exclusive cover design – by the team from Amkor Technology, GLOBALFOUNDRIES, and Open-Silicon. The article presents results on the design of a multiple processor SiP enabled by a 2.5D TSV. The goal was to produce a “first time right,” fully functional product demonstration to promote adoption of 2.5D SiP packaging for a broad range of leading-edge designs.

Enjoy this expanded ECTC and SEMICON West issue. At CSR, “we package the packaging industry!” If you have a leading story you want to bring to the industry’s attention in a future issue, contact us at [editor@chipscalereview.com](mailto:editor@chipscalereview.com)

**Kim Newman**  
 Publisher

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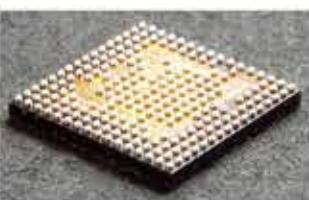
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MEMS



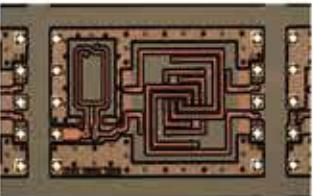
WLP



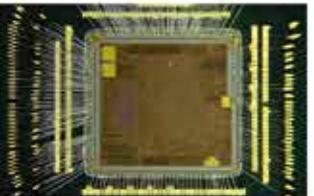
2.5D/3D/TSV



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# MARKET UPDATE



## FEOL materials creep into advanced packaging

By Mike Corbett, Mark Thirsk [Linx Consulting, LLC]

The migration of leading edge packaging away from chip on frame and wire bonding to 2.5D and 3D through-silicon via (TSV) packages that stack thinned die in chip-scale, all-silicon packages, is now well underway; and the hype around 3D is being dispelled by early product releases. TSV technology is being counted on to resolve latency issues while allowing for higher bandwidths, while delivering smaller form factors and low profile. Whereas many of these changes are being driven by the rapid growth and acceptance of smartphones and handheld tablets, many new packaging challenges and opportunities will also be driven by certain limits on front-end-of-the-line (FEOL) processing. For example, DRAM capacitors are reaching a point where it is unlikely that further scaling will be met through the introduction of new materials or from lithography-based solutions. As a result, DRAM producers are looking at TSV-based technologies with integrated logic to meet the density and performance scaling requirements in high-end server applications. Additionally, many logic producers are also looking at TSV technology to move on-chip memory closer to the core, add increasing amounts of memory, and free up space from the embedded DRAM to allow room for more, high-value add logic functions. Finally, the portioning of some

larger die also represents an excellent opportunity for TSV technology. Additionally, new materials developed for semiconductor wafer fabrication applications are increasingly being viewed as critical for advanced packaging applications. Examples can include low temperature deposition precursors used as dielectric liners, advanced barrier and seed enhancement layers such as Ru or Co for TSV copper, barrier and seed materials, and the use of other technologies such as plasma etch and CMP that are typically deployed for FEOL processing (see **Figure 1** for market data on advanced packaging materials).

The incorporation of new materials, into wafer-level packaging (WLP), flip-

chip and TSV (typically via-middle configuration) solutions, including wafer bonding, interconnect, underfilling, interposers, and molding compounds, etc., is driving new markets to meet these new applications. The advent of improved wafer-level packaging, novel fan-in and fan-out redistribution, added to the huge effort being expended in the emerging technology of TSV interconnect technologies is putting demands on existing materials and setting requirements for improvements and innovation of materials and processes within tight cost and reliability constraints.

In this review, we will focus on materials use and needed innovations in packaging challenges including TSV

### Advanced Packaging Materials (\$M)

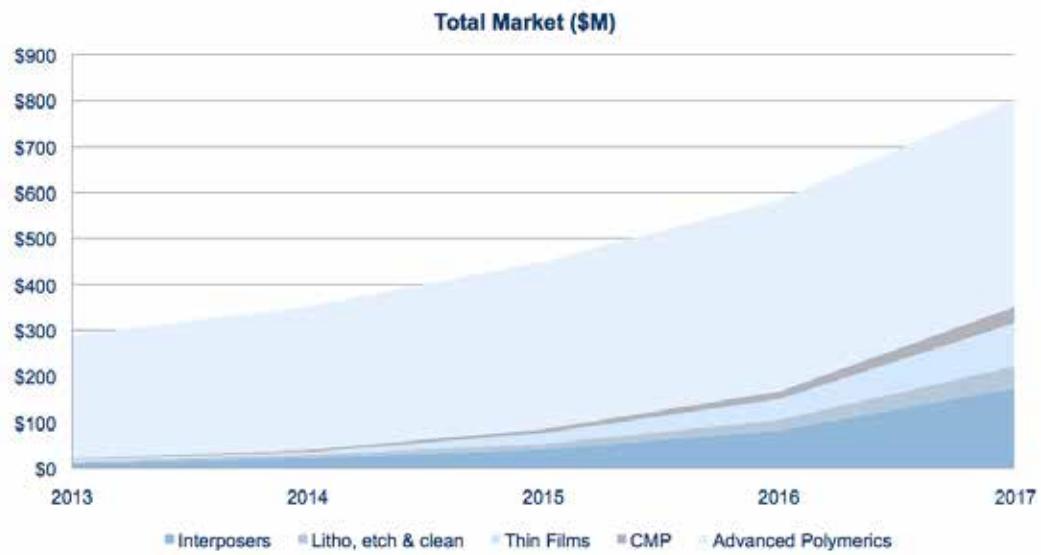


Figure 1: Advanced packaging materials (\$M).

liners, seed/barrier, plating chemistry, bump/pillar photoresists, temporary bonding adhesives, backside dielectrics, and underfills. In many cases these materials and processes are derived from the analogous front end wafer processes, and utilize the same equipment sets, as shown in **Figure 2**.

### TSV liners

The isolation oxide is a critical technology for TSV manufacturing as there is no alternative to a liner to achieve a functional device using TSV technology. All TSV developers have an isolation oxide technology in their process flow. The isolation layer is the protective or insulating layer that also serves to remove surface stresses from the silicon surface and to provide a surface for barrier deposition. As such, it must fill the high-aspect ratio vias and then endure a barrier and seed layer. Alternatives include spin-on dielectric oxides, chemical vapor deposition (CVD) oxides, as well as novel flowable CVD (FCVD) processes using advanced

precursors such as TSA. Atomic layer deposition (ALD) technology may also be an option for this film.

### Seed/barrier

PVD is an early favorite for barrier and seed deposition especially at larger nodes. A TaN or TiN barrier layer with an additional tie layer such as Ti or Ta can be used in initial configurations. This would be followed by a PVD layer for copper seeding. All of this is very similar to what is being implemented in interconnect processing for advanced logic and memory devices today. However, going forward with tighter pitches, there can be needs for advanced direct plate materials and seed enhancement layers, which may involve such new materials as cobalt and ruthenium.

### Plating chemistry

The technology to fill deep vias relies both on galvanic plating and modifications of the plating process through additive such as levelers,

and suppressors. These surface active chemicals aid the suppression of plating at the substrate surface and promoting deposition within the vias.

While the basic plating chemistry is borrowed from similar formulations to those used in dual damascene plating in the wafer back-end processing, the change in geometry offers new challenges. The >10:1 aspect ratios and larger via geometries drive modifications in the additive package and in the plating process, while fill times are orders of magnitude longer than those used to fill vias in trenches for interconnect. Process tuning reduces the overburden of copper on the wafer surface, and under specific conditions, processes that leave no added copper on the wafer surface with complete filling of the TSV structure have been demonstrated.

### Chemical mechanical planarization

Chemical mechanical planarization (CMP) will be a new entrant into the advanced packaging world. CMP

## TSV Via Middle Process is Most Familiar



### Via Middle

1. FEOL
2. TSV Litho
3. TSV Etch
4. TSV Isolation oxide
5. TSV PVD CuBS
6. TSV Copper Fill
7. TSV Copper CMP
8. TSV Barrier CMP
9. BEOL
10. TSV Wafer Bonding
11. TSV Wafer Thinning
12. TSV Via Reveal
13. TSV Oxide – Deposition and CMP
14. TSV Wafer Debonding



Tool	FEOL OEMS		Key Consumables
DRIE Etch	Lam Research	TEL	Fluorocarbons
PECVD Oxide	Applied Materials	Lam Research	TEOS, TSA, VDP
PVD	Applied Materials		Cu and Ta PVD, MOCVD
ECD	Lam Research	Applied Materials	ECD Copper
CMP	Applied Materials	Ebara	Slurries and pads
Aligner Bonder	TEL	N/A	Adhesives
Lapping	N/A	N/A	NA
Spin Track	TEL	DNS	SOD, Litho

Used in FEOL HVM by all memory and logic producers

**Figure 2:** TSV via-middle process is most familiar.

# Turret Test Handler



**FT2018**

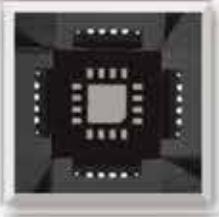
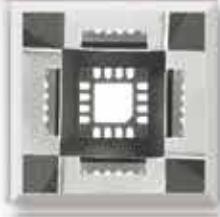
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  - ✓ Compensation for package thickness variation
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\*E.g. SOT23 with short test time



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requirements for copper barrier and seed applications will generally follow BEOL developments, although both the Applied Materials and Ebara tools will use slightly different configuration setups because of the much thicker films that will be employed. CMP can also be used for backside stress relief, post-thinning, as well as via reveal. These applications will require some advanced slurries and newly developed selectivities so as not to smear or remove the copper in the underlying films. Along with the CMP processing will be the use of low defectivity pads and also advanced cleaning chemistry to prepare the wafer surface for the next step, as well as prevent oxidation from occurring.

### Bump/pillar photoresists

To form the connections between wafers and interposers being packaged, front-to-front or front-to-back metal bumps, or pillars need to be formed. These are typically plated in vias patterned into thick resist. Whether mushroom shaped bumps that are plated thicker than the resist, and then reflowed, or cylindrical pillars that are plated within the vias, bump photoresists must achieve both good pattern fidelity, and plating solution resistance, as well as being easily removed after plating. Spinning the thick layers used for bumping is also a challenge, and novel resist formulations are in use to produce the high-aspect ratio, tight pitch patterns needed.

### Temporary bonding adhesives

Development of temporary bonding materials has been a difficult challenge. In a via-first or via-middle process, after the completion of front end processing, the bulk of the silicon must be removed from the back side of the wafer and the copper of the TSVs revealed. Following this aggressive process, the copper TSVs must be prepared for bonding – a process that can involve plasma or wet etching, oxide deposition, and CMP.

To accomplish bonding, a handle wafer is temporarily bonded to the front side of the device wafer to support it as it is thinned to 50 microns, or less, and prepared for the next bonding step. The

properties of the ideal bonding material are that the device and handle wafer be securely physically bonded together for processing, that the adhesive withstands aggressive chemistry and solvents, as well as high-temperature processing, and that it releases on demand, leaving no residue.

Multiple approaches have been developed to support the device wafer, and then allow separation by various physical or chemical changes in the bonding adhesive. Approaches include melting, polymer scission and dissolution. All of these approaches have limitations, but progress has been made, and functional materials are in use.

### Backside and RDL dielectrics

Backside and RDL dielectric materials are becoming increasingly important with increased bump densities and the move to WLP and the employment of WLP techniques for TSV. These materials are typically spin-on dielectric materials ranging from the venerable BCB to advanced PBO materials. There are still many challenges with these materials in terms of performance with regards to delamination, low stress, no moisture uptake, low temperature curing, and higher resolution.

### Underfills

Underfills supply physical support and environmental protection to the connection array, whether solder joints or bonded bumps. The underfill reduces the stress on the interconnect bumps and aids in reliability improvement. Liquid epoxy had been a dominant technology in capillary flow underfill, but this may not be universally acceptable for stacked packages. However, increasing problems with voiding around complex masks, as well as voiding associated with stacked chips, such as in TSVs, will continue to drive further development activities here. Molded underfills, vacuum underfills, and pre applied materials, such as non-conductive pastes and non-conductive films, will have to become more common in high-performance packages, and offer a path forward.

### Summary

The drive towards increased density and functionality of electronic devices is making a considerable impact on each stage in the value chain of the electronics industry. For semiconductor producers, development efforts include both device scaling and the designated optimum packaging technologies for the designated end application. Advanced packaging technologies and materials have been critical in driving the trend towards miniaturization over the last 10 years, with multiple novel approaches such as flip-chip, bump and pillar, and lead-free bonding, and will continue to be needed in delivering increased functionality per package.

As more FEOL processes and tool sets are required to deliver the next-generation packages, the expectation is that the more expensive FEOL materials will also make an appearance in advanced packaging. In many instances, these transplanted, advanced FEOL materials may not have the same purity and quality requirements of their back-end brethren. However, it is likely that the manufacturing infrastructure of the chemicals and materials supplier will already be set up to meet the FEOL requirements, so offering a lower cost version of some of the materials may be difficult. Therefore, scale will have to be the predominant cost driver. In addition, there will be many additional thermal, mechanical and moisture based requirements that the materials will have to meet, which will only up the ante on performance. As such, it is imaginable to have a future without so much segmentation between FEOL and BEOL for both materials and equipment suppliers.

### Biographies

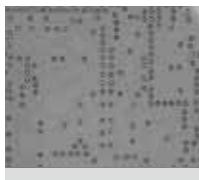
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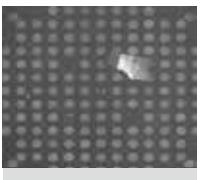
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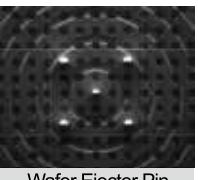
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- Auto Flatness Check Capability
- Wafer Map Shift Prevent Function
- Foreign Material Detect Inspection System
- Chip Out Detect Inspection System
- Lower Vibration Control System
- User Friendly MMI for Easy Operation
- Lower Temperature Control



Die Chipout Inspection



Eject Cup F/M



Wafer Ejector Pin Maker Inspection



FLIP CHIP BONDER - A110



FLIP CHIP BONDER - S100

### ■ General Specifications

SECTION		FLIP CHIP BONDER-A110	FLIP CHIP BONDER-S100
PRODUCTIVITY		15,000 (Based on Dry Run)	
ACCURACY	X-Y PLACEMENT	$\pm 6\mu\text{m}$ @ $3\sigma$	$\pm 15\mu\text{m}$ @ $3\sigma$
	CHIP ROTATION( $\theta$ )	$\pm 0.1^\circ$ @ $3\sigma$	
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)	
FOOTPRINT	DIMENSION (Wx Dx H)	1,600mm x 1,200mm x 1,500mm	
	WEIGHT	2,700 kg	



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# STANDARDS UPDATE



## Enabling 3DS IC manufacturing through SEMI Standards

By James Amano *[SEMI]*

**A**s the industry pushes current boundaries and explores new solutions to enable commercialization of 3D ICs, cost-effective high-volume manufacturing will be difficult to achieve without standardized equipment, materials, and processes, especially because 3D ICs' design and mechanical complexity can lead to increased manufacturing defects, as well as thermal management issues and signal interference.

Focusing on 3D IC technology and the manufacturing process will help reduce costs through increased throughput, improved product quality, better yields, and lower maintenance and operational expenses. No single company can fully realize these benefits without working closely with their suppliers and their competitors. Highly-automated and advanced manufacturing systems comprise multiple equipment types, technologies and supporting products from best-in-class suppliers from around the world. Enabling these different processes, products and technologies to work seamlessly and cost-effectively together requires diverse, well-informed and effective industry standards.

Understanding the essential role of standards in enabling low-cost, high-quality manufacturing, SEMI first charged its International Standards group with exploring the challenges of 3D IC manufacturing issues in spring 2010. The first 3DS-IC ("S" stands for "stacked") SEMI Standards Technical Committee was formed in North America in late 2010, with a counterpart in Taiwan created in July 2011. In early fall 2012, the Japan Packaging Committee authorized the formation

of a 3D-IC Study Group with plans to explore and ultimately engage in the activities in North America and Taiwan.

### TSV geometrical metrology

The SEMI 3DS-IC Standards committee's first accomplishment was SEMI 3D1, "Terminology for Through Silicon Via Geometrical Metrology." SEMI 3D1 provided a starting point for standardization of geometrical metrology for selected dimensions of through-silicon vias (TSVs). Although different technologies measured various geometrical parameters of an individual TSV, or of an array of TSVs — such as pitch, top diameter, top area, depth, taper (or sidewall angle), bottom area, and bottom diameter — it was difficult to compare results from the various measurement technologies because parameters are often described by similar names, but actually represent different aspects of the TSV geometry. The Inspection & Metrology Task Force

recognized the need for such a standard. SEMI 3D1 is an important first step in promoting common understanding and precise communication between stakeholders in the 3D IC manufacturing supply chain.

### Glass carrier wafer specs

Publication of SEMI 3D2, "Specification for Glass Carrier Wafers for 3DS-IC Applications" was approved in Fall 2012. Developed by the Bonded Wafer Stacks Task Force, this specification addresses the needs of the industry by providing the tools needed to procure pristine glass carrier wafers for use in 3DS IC processes.

SEMI 3D2 describes dimensional, thermal, and wafer preparation characteristics for the glass starting material that will be used as carrier wafers in a temporary bonded state. This specification also describes glass carrier wafers with nominal diameters of 200 and 300mm, and a thickness of

Part 2 Standardized Specifications for 200 mm and 300 mm Glass Wafers for 3DS-IC Applications

	Parameter	Grades A, B, C	Measurement Method
♦ 2-1.1	Glass Type	<input type="checkbox"/> Borosilicate or <input type="checkbox"/> Aluminosilicate	
♦ 2-1.2	Manufacturing Method	<input type="checkbox"/> Fusion, <input type="checkbox"/> Float, or <input type="checkbox"/> Drawn	
♦ 2-1.3	Surface Condition	<input type="checkbox"/> As-is (pristine) for fusion glass <input type="checkbox"/> Polished for float and drawn glass	
♦ 2-1.4	Nominal Ground Edge Exclusion	<input type="checkbox"/> None <input type="checkbox"/> Other: (specify) _____	
♦ 2-1.5	Wafer ID Marking	SEMI T7 (required) + optional alphanumeric, on back surface	
♦ 2-1.6	Notch Dimensions	<input type="checkbox"/> Notch Depth: 1.00 mm $\pm$ 2.50 mm $-0.00$ mm Notch Angle: 90.0 degrees $\pm$ 5 deg $-1$ deg <input type="checkbox"/> Other: (specify) _____	<input type="checkbox"/> SEMI MF1152 (Notch Dimensions) <input type="checkbox"/> Other: (specify) _____
♦ 2-1.7	Edge Surface Condition	<input type="checkbox"/> Polished	
2-1.8	Edge Chamfer	<input type="checkbox"/> 200 $\pm$ 50 $\mu\text{m}$ (for 300 mm glass wafers); <input type="checkbox"/> Other: (specify) _____ $\pm$ _____ $\mu\text{m}$	SEMI MF928: <input type="checkbox"/> Method A, <input type="checkbox"/> Method B <input type="checkbox"/> Other: (specify)
2-2.1	Diameter	<input type="checkbox"/> 200.0 $\pm$ 0.05 mm	<input type="checkbox"/> SEMI MF2074

Table 1: Requirements for standardized glass carrier wafers for temporary bonding. Note: table is an incomplete representation.

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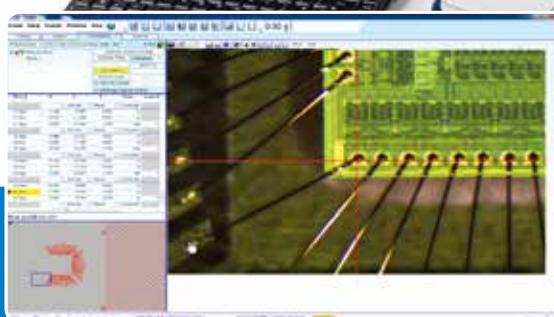


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700 $\mu$ m, although the wafer diameter and thickness required may vary due to process and functional variation. Such variations need clarification in the purchasing order or in the contract. Methods of measurements suitable for determining the characteristics in the specifications are also indicated (**Table 1**).

### Thin wafer transport and storage

In June 2013, SEMI published the 3D3 standard: "Guide for Multiwafer Transport and Storage Containers for 300mm, Thin Silicon Wafers on Tape Frames." Developed by the Thin Wafer Handling Task Force, SEMI 3D3 is intended to address the needs for choosing a method for shipping thin wafers on tape frames in such a way that they arrive undamaged at their final destination. It describes various methods of shipping thin wafers on tape frames. Examples of methods for shipping thin wafers on dicing frames are provided in **Figure 1**.

### Bonded wafer stacks and TSV metrology

At the heels of SEMI 3D3 publication, both SEMI 3D4 - "Guide

for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks" and SEMI 3D5 - "Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures" were released in mid-2013. Control of parameters, such as bonded wafer stack (BWS) thickness, total thickness variation (TTV), bow, warp/sori, and flatness metrology, is essential to successful implementation of a wafer bonding process. These parameters provide meaningful information about the quality of the wafer thinning process (if used), the uniformity of the bonding process, and the amount of deformation induced to the wafer stack by the bonding process. Developed by the Inspection & Metrology Task Force, SEMI 3D4 provides a description of tools that can be used to determine these key parameters before, during, and after the process steps involved in wafer bonding.

On the other hand, TSVs are critical elements in three-dimensional stacked integrated circuit (3DS-IC) packaging. Advanced TSV designs with higher

aspect ratios and smaller diameters may challenge TSV metrology techniques. SEMI 3D5 aims to assist in the selection and use of tools for performing measurements of geometrical parameters of an individual TSV, or of an array of TSVs.

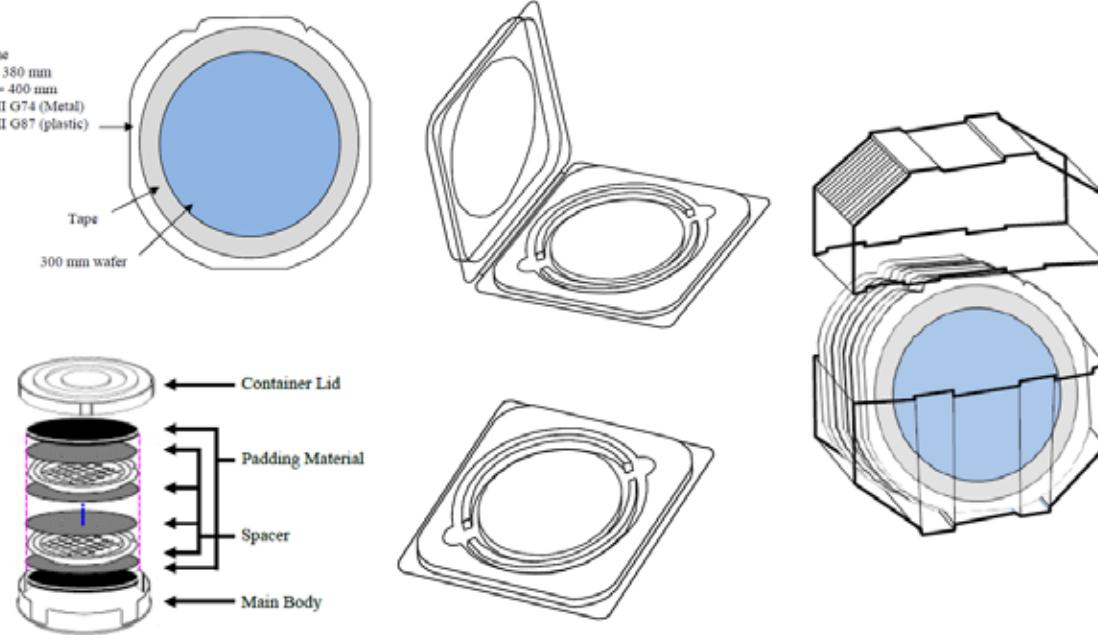
### The middle-end process

While the North America 3DS-IC Technical Committee (TC) led the first charge of SEMI 3DS-IC standards development (see the sidebar for a summary of its activities), the Taiwan TC Chapter's efforts came to fruition with Middle End Process Task Force publishing SEMI 3D6, "Guide for CMP and Micro-Bump Processes for Frontside TSV Integration" (Fall 2013) and SEMI 3D7, "Guide for Alignment Mark for 3DS-IC Process."

### Biography

James Amano received his BA from the U. of Colorado at Boulder and is a Senior Director of International Standards at SEMI ([www.semi.org](http://www.semi.org)); email [jamano@semi.org](mailto:jamano@semi.org)

*(SEMI 3DS-IC standardization activities continue on page 14)*

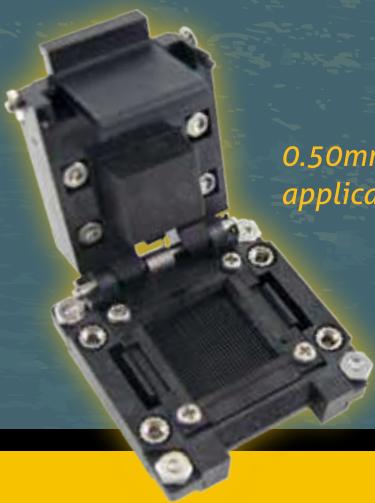


**Figure 1:** Methods for shipping thin wafers on dicing frames bonded wafer stacks and TSV metrology.

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# SEMI 3DS-IC standardization activities continue

## North America 3DS-IC Committee

- [Bonded Wafer Stacks Task Force](#) has divided the existing [5173](#) activity (*New Standard: Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack*) into smaller document development efforts:
  - New Standard: Guide for Describing Glass Wafers for Use as 300mm Carrier Wafers in a 3DS-IC Temporary Bond-Debond (TBDB) Process [Doc. [5692](#)]
  - New Standard: Guide for Describing Silicon Wafers for Use as 300mm Carrier Wafers in a 3DS-IC Temporary Bond-Debond (TBDB) Process [Doc. [5693](#)]
  - New Standard: Guide to Describing Materials Properties for 300mm Wafer Stacks [Doc. [5694](#)]
  - New Standard: Guide to Describing Materials Properties for Intermediate Wafers for Use in a 300mm 3DS-IC Wafer Stack [Doc. [5695](#)]. The task force submitted Documents 5173D, 5693, 5694, and 5695 for the [Cycle 2, 2014 voting period](#).
  - The task force is also continuing its work on SEMI Draft Document [5174](#), *New Standard: Specification for Identification and Marking for Bonded Wafer Stacks*.
- [Inspection & Metrology Task Force](#) is continuing its work on the following activities:
  - New Standard: Guide for Measuring Voids in Bonded Wafer Stacks [Doc. [5270](#)]
  - New Standard: Terminology for Measured Geometrical Parameters of Through-Glass Vias (TGVs) in 3DS-IC Structures [Doc. [5447](#)]
  - New Standard: Guide for Measuring Warp, Bow and TTV on Silicon and Glass Wafers Mounted on Wire Grids by Automated Non-Contact Scanning using Laser Scanning Interferometry [Doc. [5506](#)]
  - Revisions to SEMI 3D4 [Doc. [5616](#)] for clarification and additional improvements
  - The task force submitted Document 5447 for the Cycle 2, 2014 voting period.
- [Thin Wafer Handling Task Force](#) is considering possible standardization on dicing tape characterization and performance as well as unsupported thin wafer handling.

For more information about North America 3DS-IC activities, please contact Paul Trio ([ptrio@semi.org](mailto:ptrio@semi.org)) at SEMI.

## Taiwan 3DS-IC Activities

- [Middle End Process Task Force](#) recently initiated a new standards activity focused on overlay performance via Standards New Activity Report Form (SNARF) [5688](#): *New Standard: Guide for Overlay Performance Assessment for 3DS-IC Process*.
- [Testing Task Force](#) is continuing its work on Draft Document [5485](#), *New Standard: Guide for Incoming/Outgoing Quality Control and Testing Flow for 3DS-IC Products*.

For more information about Taiwan 3DS-IC activities, please contact Ms. Catherine Chang ([cchang@semi.org](mailto:cchang@semi.org)) at SEMI.

## Japan 3DS-IC Activities (under the Japan Packaging Committee)

- [Thin Chip \(Die\) Bending Strength Measurement Task Force](#) was chartered to develop a new test method for bending strength measurement under SNARF [5691](#): *New Standard: Test Method for Measurement of Chip (Die) Strength by Mean of Cantilever Bending*.
- **3D-IC Study Group.** The 3D-IC Study Group is considering possible standardization on bonded wafer handling, stacked wafer handling, and diced stacked dies handling.

For more information about Japan 3DS-IC activities, please contact Ms. Naoko Tejima ([ntejima@semi.org](mailto:ntejima@semi.org)) at SEMI.

Ballots for the above activities will be issued throughout 2014, and are reflective of the continued global, industry-wide effort. Over 100 technologists from industry, research institutes, and academia around the world have already joined the SEMI 3DS-IC Standards Committee and are at work on these critical standards.

Pre-competitive collaboration is difficult, and involves hard work by industry experts, but it creates significant benefits for the industry as a whole, for companies participating, and for individuals involved in the process. If you or your company is not yet involved in these efforts to shape the future of 3D-IC, learn more about SEMI Standards by visiting [www.semi.org/en/Standards](http://www.semi.org/en/Standards). Note that participation in the SEMI Standards Program is free, but requires registration. To learn more, contact [jamano@semi.org](mailto:jamano@semi.org) or register at: [www.semi.org/standardsmembership](http://www.semi.org/standardsmembership).



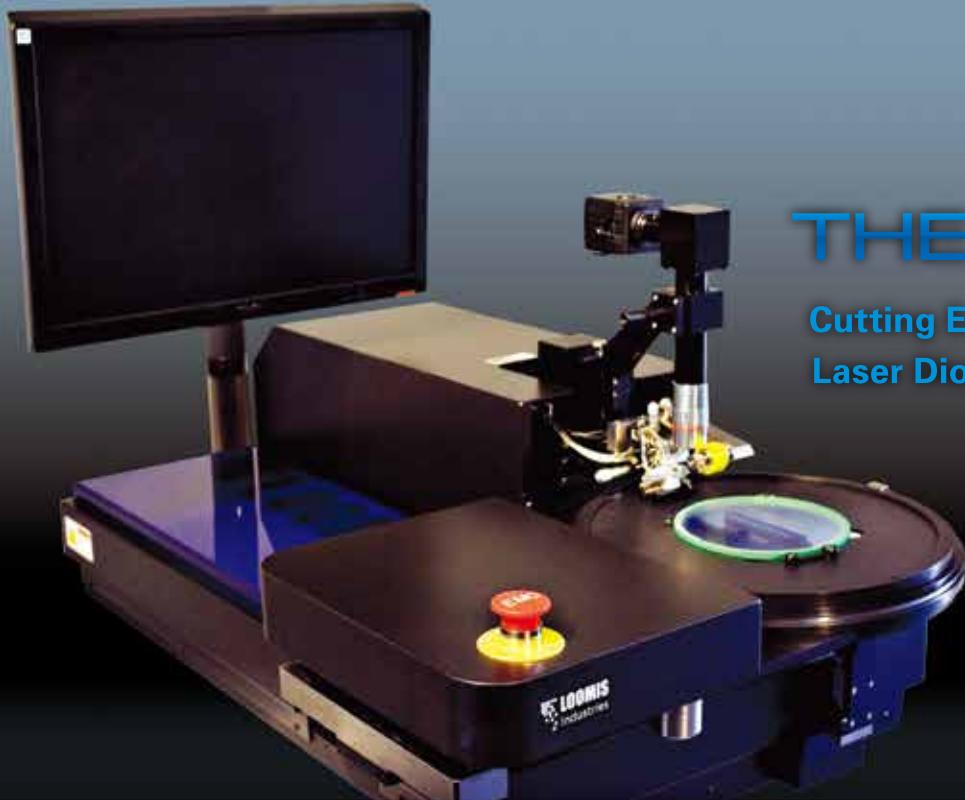
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# GUEST EDITORIAL

## A cost-effective platform for heterogeneous 2.5D ICs

By Guruprasad Katti, S.W. Ho, Liang Ding, Ka Fai Chang, Surya Bhattacharya [Institute of Microelectronics]

Heterogeneous integration of multiple chips on 2.5D interposers provides ample opportunities to optimize chips for next-generation mobile devices and data centers/servers to achieve lower power, higher performance, and smaller form factor. IC designers find that implementing systems using through-Si-interposer (TSI) based 2.5D IC technology provides the flexibility to choose the appropriate semiconductor process technology for each circuit building block function (e.g., CPU, memory, apps processor, transceiver, power management unit), and implement the system with better performance, lower power consumption and smaller form factor through the use of 2.5D IC technology. The cost of manufacturing Si interposers is a key challenge facing the high-volume ramp of 2.5D IC technology. In addition, TSI designers require a calibrated process design kit (PDK) to leverage the TSI-based 2.5D IC technology for prototyping system design. In this paper, we discuss recent developments that have been demonstrated at IME to reduce the cost of fabricating TSIs. We also present the available infrastructure at IME to support cost-effective prototyping of TSI-based 2.5D ICs.

The cost of fabricating 2.5D ICs on TSIs is impacted significantly by the costs of: a) fabricating interconnects on the front/back side of the interposer, b) formation of the TSV, c) temporary bonding and debonding, and d) thinning/backgrinding/TSV reveal. Depending on the application, we find that the cost of the 2.5D IC solution can be reduced by innovative approaches.

Today, Si interposers are made with a dual-damascene process that is dependent on the fabrication infrastructure, which is typical of

a foundry. We believe Cu-RDL interconnects that are insulated by polymer dielectrics can be extended to finer pitches, as well as to multi-level metals to support wiring on the front and back side of an interposer. In the case of traditional back-end-of-line (BEOL) processing, the fabrication of a 2.5D interposer is typically dependent on a foundry infrastructure. Polymer-based Cu-RDL interconnects, however, can be manufactured using outsourced semiconductor assembly and test services (OSATS) infrastructure, which leads to a cost reduction in infrastructure requirements. We demonstrate techniques to reduce the cost of 2.5D IC manufacturing by using less expensive front and back side interconnects, and by studying the opportunity to remove the need for using temporary bonding/debonding steps for certain applications. We also outline the infrastructure enabling the facilitation of the design, prototype, and manufacturing of 2.5D ICs for next-generation systems.

### Polymer-based Cu-RDL process flow

The fabrication of TSVs is the initial step toward manufacturing multilayer polymer-based Cu-RDL interconnects on 2.5D TSI. TSVs are manufactured using the traditional Bosch etch, sub-atmospheric chemical vapor deposition (SACVD) isolation oxide, physical vapor deposition (PVD) Ta barrier/PVD Cu seed, followed by electroplating Cu in sequence. The manufacturing of a three-metal layer polymer-based Cu-RDL process ( $W/S = 3/3\mu m$ ; thickness =  $3\mu m$ ; via size =  $5\mu m$ ) is detailed in Figure 1. Key challenges confronted during the process development are highlighted as well. After the seed layer deposition and photoresist patterning, Cu is electroplated to form the first Cu-RDL layer.  $Si_3N_4$  is deposited, patterned and etched before spin coating the polymer dielectric. The dielectric is further patterned using the via 1 mask, and the seed layer deposition and

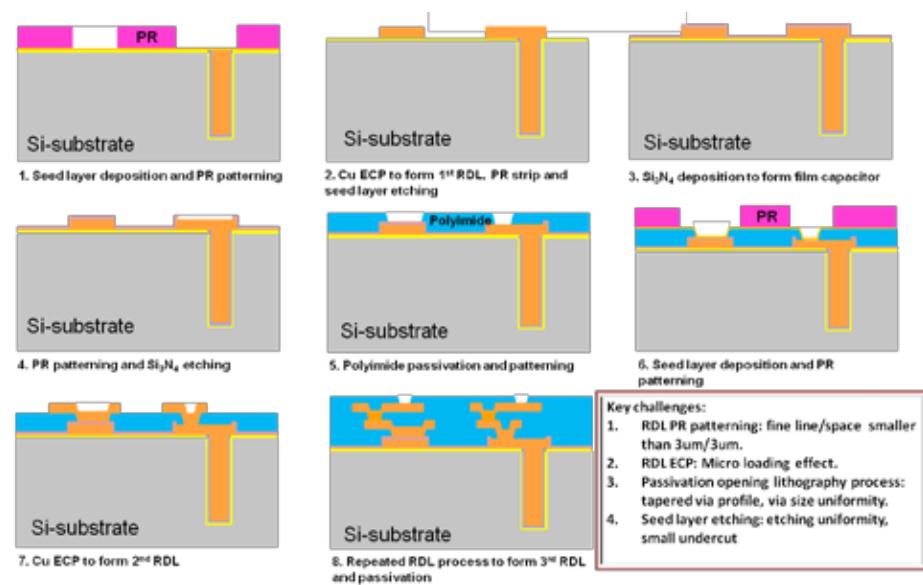
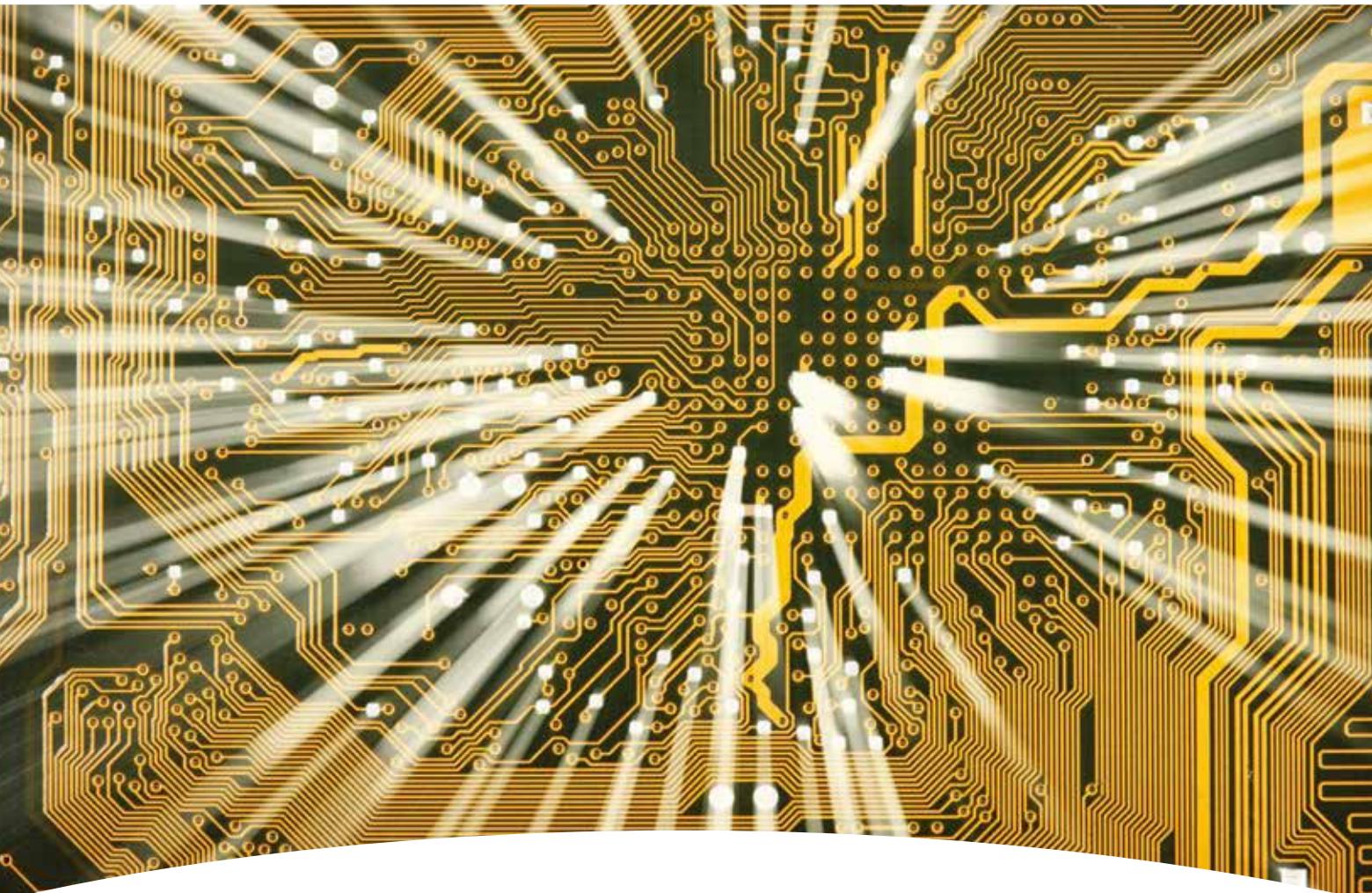


Figure 1: Process flow illustrating the manufacturing of a 3-layer polymer-based Cu-RDL process.

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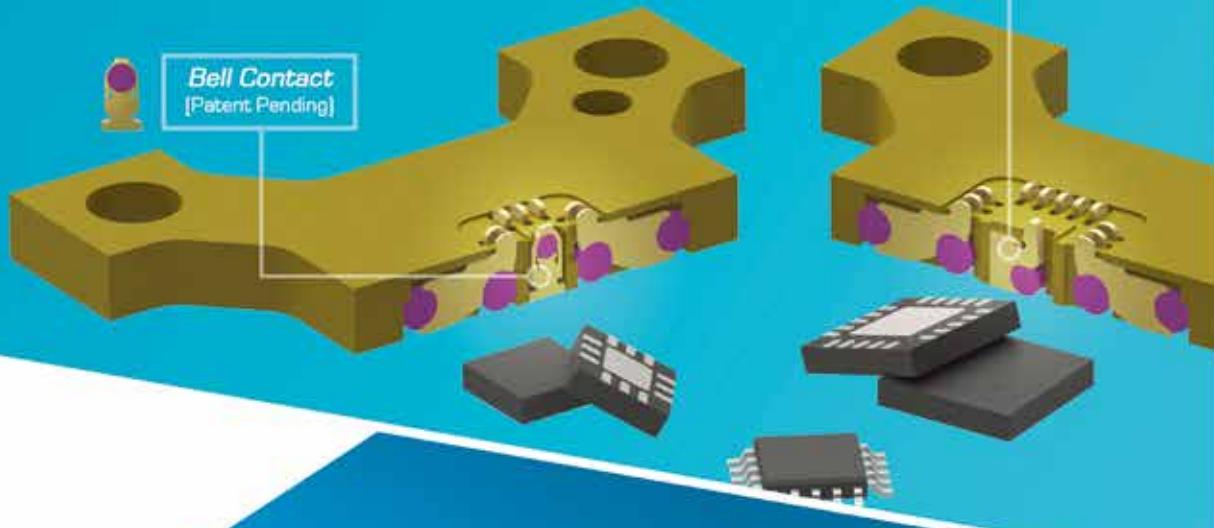
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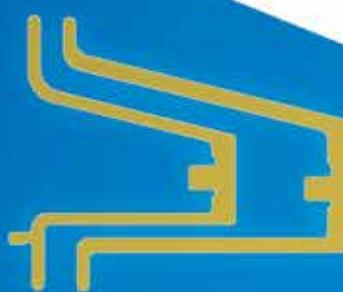
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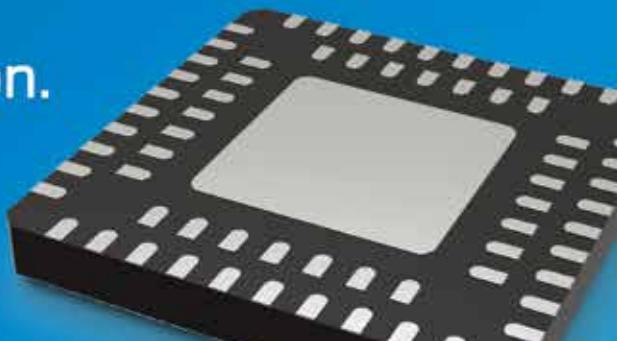
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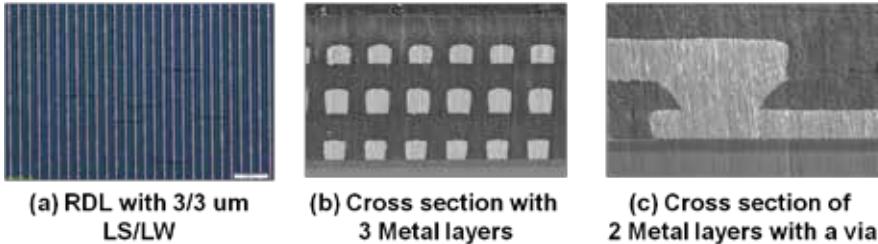
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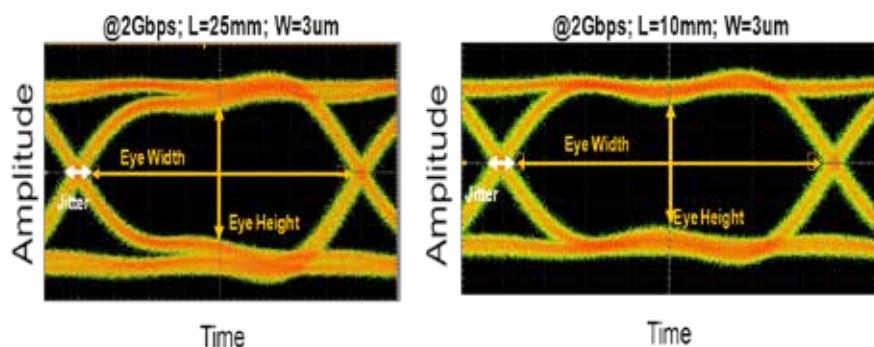


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**Figure 2:** Demonstration of 3-metal layer RDL technology (LW/LS = 3/3 $\mu$ m; Thickness = 3 $\mu$ m and via size = 5 $\mu$ m).



**Figure 3:** Measured eye diagram on Cu-RDL lines with LW = 3 $\mu$ m with varying lengths (25mm and 10mm).

photoresist patterning are accomplished to construct the via, as well as second Cu-RDL layer. The same procedure is replicated multiple times to construct all the Cu-RDL layers. The back side RDL interconnects can be manufactured with the similar process flow after the back side reveal of TSVs.

IME has been able to successfully achieve line width and spacing of LW/LS=3/3 $\mu$ m targeting a via size of 5 $\mu$ m. As a design rule, the 2.5 $\mu$ m enclosure is recommended on each side of the via such that the total via enclosure size of 10 x 10 $\mu$ m is much larger than the minimum line width of the Cu-RDL line. Additionally, the stacking of multiple vias on top of each other is not allowed and the stacked vias have to be spaced out as illustrated in step 8

of **Figure 1**. A realized patterned RDL with 3/3 $\mu$ m line width and spacing is illustrated in **Figure 2a**. A three-metal layer RDL cross section and cross section of two metal layers with via are illustrated in **Figures 2b** and **2c**, respectively.

The impact of varying lengths on polymer-based Cu-RDL lines with width = 3 $\mu$ m, thickness = 3 $\mu$ m and varying lengths (25mm and 10mm) is characterized through the eye diagram measurements performed at 2Gbps (**Figure 3**). The important statistics are listed in **Table 1**. It can be readily seen that for both lengths of 25mm and 10mm the eye diagram performance is satisfactory. However, because of lesser loss induced by the parasitic elements, the eye diagram with L = 10mm yields a

marginal better jitter, eye width and eye height performance compared to that with L = 25mm.

### Chip-2-wafer carrier-less assembly flow

Chip-2-chip (C2C) assembly suffers from lesser throughput issues and wafer-2-wafer (W2W) assembly flow is not a plausible alternative because of inherent 2.5D IC requirements (e.g., multiple die fabricated in various technology nodes with different sizes). Chip-2-wafer (C2W) assembly flow, therefore, is the most promising and sought after assembly option. Temporary bonding and debonding is one of the costliest processes to assemble 2.5D ICs; the use of C2W assembly and the carrier-less assembly flow shown in **Figure 4** illustrates how it is possible to achieve cost reduction of the process, by eliminating temporary bonding and debonding steps.

Once the guest dies are mounted on the 2.5D interposer and wafer-level over molding is achieved, the back side via revealing process to expose the TSVs and BGA ball drop is performed. This flow does not require the bonding and debonding to the temporary carrier wafer and should be preferred to achieve the low cost 2.5D IC assembly.

### Process design kit (PDK) and VLSI CAD flow

The PDK is quintessential to enable designers to leverage 2.5D IC technology. The design constraints encountered during the technology development are captured in the DRC rule decks. The LVS rules along with the process control monitored resistance and capacitance of interconnects forming the parasitic extraction rule decks are provided as well. In addition, the VLSI design CAD flow, illustrated in **Figure 5**, with the demonstration starting from design data entry, wiring density analysis, SI/PI analysis leading to .gds sign off to the manufacturing facility is provided. The chips designed using the PDK are manufactured as

	L = 25 mm	L = 10 mm
Eye Width [ps]	451.2	456.4
Eye Height [mV]	431.1	622.3
Jitter (peak-to-peak) [ps]	56.25	45.63

**Table 1:** Important eye diagram statistics measured @ 2Gbps for polymer-based Cu-RDL interconnects with LW = 3 $\mu$ m and lengths (25mm and 10mm).

MPW runs in IME's manufacturing facility as well.

## Summary

2.5D ICs offer flexibility to assemble

off-the-shelf components (onto 2.5D ICs) and are desirable for a plethora of applications on mobile communication as well as for data centers/servers. Fine-pitch ( $LW/LS = 3/3\mu m$ ; thickness =  $3\mu m$  and via size =  $5\mu m$ ) polymer-based Cu-RDL lines technology is realized to enable OSATS to manufacture the 2.5D ICs at lower costs. Eye diagram measurements at 2 Gbps on interconnect lines with a thickness of  $3\mu m$  and  $3/3\mu m$  line width and space confirm reliable communication with line lengths of 25mm and 10mm on 2.5D ICs. C2W carrier-less assembly eliminates the use of the carrier, as well as the temporary bonding and debonding processes, thereby leading to the reduction in manufacturing costs. IME offers silicon verified 2.5D IC PDK to participate in the MPW runs to manufacture functional 2.5D IC systems

## Biographies

Guruprasad Katti received his PhD from IMEC/KU Leuven - Belgium and is a Scientist at the Institute of Microelectronics; email: kattig@ime.a-star.edu.sg

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Liang Ding received his PhD from Nanyang Technological U., Singapore, and a BS from Huazhong U. of Science and Technology, China. He is a Scientist at the Institute of Microelectronics.

Ka Fai Chang received his PhD from The Chinese U. of Hong Kong, Hong Kong; he is a Scientist at the Institute of Microelectronics.

Surya Bhattacharya received his PhD from the U. of Texas at Austin and is Director of Industry Development at the Institute of Microelectronics.

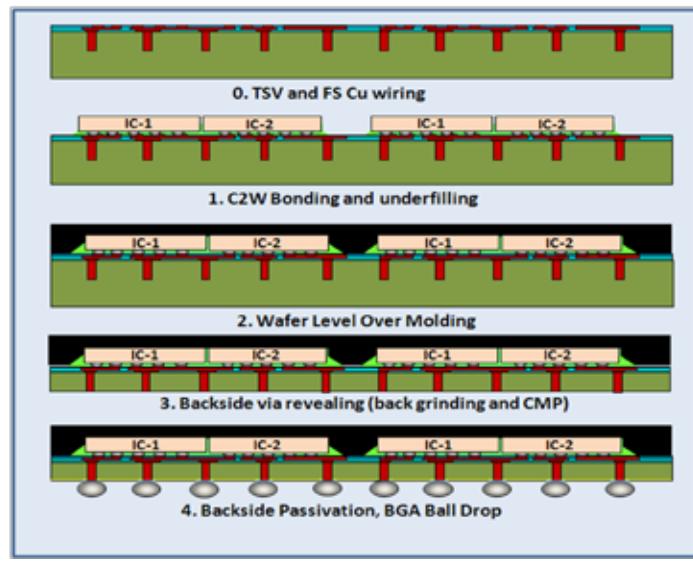


Figure 4: Cost-effective C2W carrier-less assembly flow.

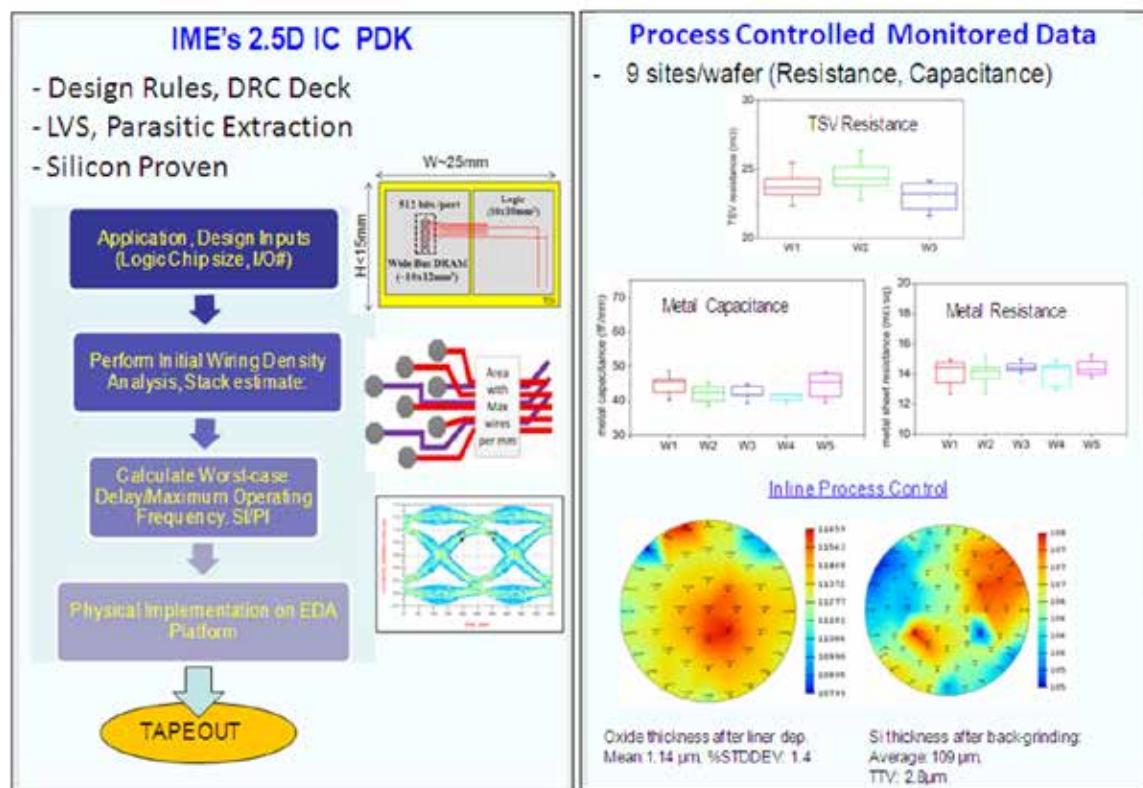


Figure 5: IME's 2.5D IC PDK encapsulating the process control monitored silicon data.



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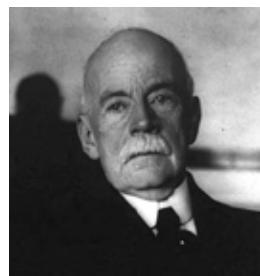


## TSV patents: new or old?

By Jason Mirabito [ISUS Intellectual Property PLLC]

**C**harles H. Duell, the Commissioner of Patents in the late 1890s, was supposed to have stated, "Everything that can be invented has been invented." While this certainly has proved to be untrue, in the world of patents, it is to some extent true that many purported new ideas in fact, originated many years ago. A good example of this may

be seen in patent activity in the field of so-called "through-silicon vias" or "TSVs" as they are popularly known. TSVs are one of the current "darlings" of attention and the subject of many technical



**Charles Holland Duell** (April 13, 1850 – January 29, 1920) Commissioner of the United States Patent and Trademark Office in 1898 to 1901

articles, studies and discussions, including patent studies.

A search of patent databases has reflected this popularity and interest. For example, a search on the US Patent Office database for the terms "TSV" and "through-silicon via" turns up hits that number, respectively, 1,807 and 1,175 issued patents. The number of published applications results in hits of 3,774 and 3,233 using those same terms. It is to be remembered that this is just the number of US patents and published applications, and does not include foreign counterparts. Using the Google patents database and restricting the search to just the term "TSV" turns up more than 600,000 hits, although this search term word would turn up any name or acronym including the letters TSV. One suspects the numbers

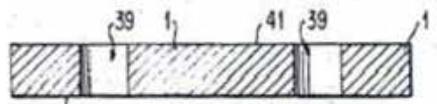
garnered from the US patent office database would be in fact larger if all the terms such as "3D IC" were also run through the database. All this just goes to show that there is a large amount of activity in companies seeking patents in this area of technology.

So, who are the companies that are being very busy in this area? They include, according to a 2013 analysis done by the Yole Développement market research firm, in terms of number of patent families from the largest to the smallest: IBM, Samsung, Micron, TSMC, Hynix, STATS ChipPAC, Intel, Amkor, Elpida and ITRI. According to the Yole report, somewhat more than 80% of the patents have been filed since 2006. The countries with the greatest amount of patent activity in this area, as can be gleaned from the list above, are the United States, Korea, Japan and Taiwan [1].

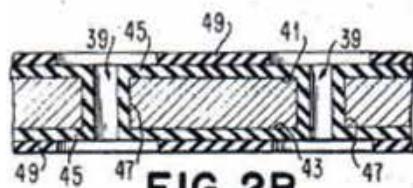
A perusal of the often accurate, and sometimes inaccurate, Wikipedia under the term "through-silicon via" covers a short article on the subject. In the article it is claimed that the technical concept of "through-silicon via" appeared in the late 1990s and that the term itself was coined in 1997. The main feature of the TSV is the "via" (which stands for vertical interconnect access) or, in other words, a technique to make electrical connections completely through silicon wafers to adjacent wafers stacked above and below.

Other than the name TSV, the technique, which now has become widespread, may have originated back in the early days of the 1960s. In 1964, two inventors, Merlin Smith and Emanuel Stern, both of IBM, filed a patent application for: "Methods of Making Thru - Connections in Semiconductor Wafers." Their application resulted in the issuance of

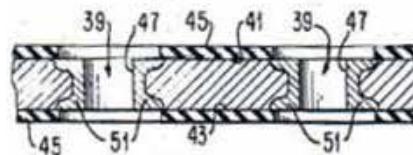
United States Patent 3,343,256 issued on September 26, 1967—it long ago expired. The object of the invention was said to "substantially reduce the space requirements of the total interconnection arrangement so as to achieve more compact arrangement of the circuit



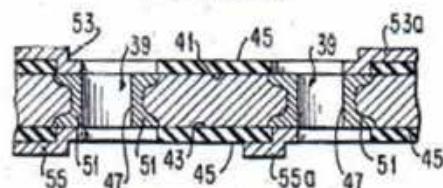
**FIG. 2A**



**FIG. 2B**



**FIG. 2C**



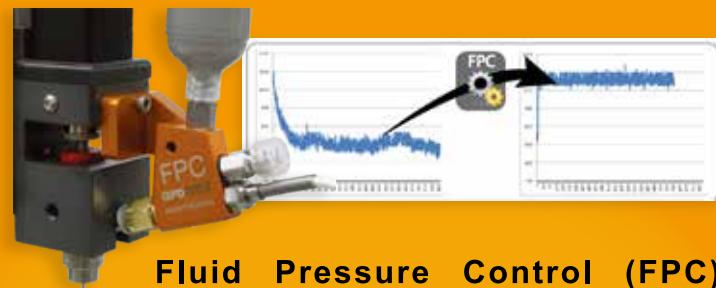
**FIG. 2D**

elements" and to do this by "providing thru-connections between major surfaces of the semiconductor wafer whereby the constituent conductor patterns can be distributed over both major surfaces of the semiconductor substrate."

**Figures 2a-d**, reprinted here, illustrate the process of making these connections. As can be seen in reference to **Figure 2a**, a wafer 1 includes a

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pattern of cylindrical holes 39 extending between two surfaces 41 and 43. Wafer 1 is then subjected to a thermal-oxidation process to grow an oxide layer 45 over the exposed surfaces 41 and 43 and also the walls 47 of the individual holes 39. Then, a layer of photoresist material 49 is formed over oxide layer 45 and exposed through a photographic mask plate so that photoresist material over narrow annular portions of major surfaces 41 and 43 adjacent the rims of holes 39 are unexposed. The layer of photoresist is then developed and cured, as shown in **Figure 2b** such that oxide layer 45 along walls 47 of each hole 39 and over the described portions of major and minor surfaces 41 and 43 are exposed. Referring now to **Figure 2c**, the exposed photoresist material 49 is removed by suitable solvents. As illustrated in **Figure 2d**, thin-film conductor patterns 53, 53a, 55 and 55a are deposited over oxide layer 45 on opposing major surfaces 41 and 43 of the wafer 1. As stated in the patent, conductor patterns 55 and 55a over major surface 43 of the wafer 1 correspond to required power and ground conductor patterns, respectively, in the integrated complex, and are connected along diffusions 51 and conductor pair 53 and 53a, respectively, to active circuit elements formed on major surface 41.

Thus, while Commissioner Duell may have been way “off base,” to some extent at least, it can be seen that perhaps the phrase “old wine in new bottles” is more accurate.

### Reference

1. Summary of “2.5D, 3DIC and TSV Interconnect Patent Investigation Report,” by Yole Développement, published in I-Micronews, 2013.

### Biography

Jason Mirabito received his Physics Engineering degree at New York U. and his law degree at American U. and Georgetown U.; he is a Member of ISUS Intellectual Property PLLC; email [jason@isusip.com](mailto:jason@isusip.com)

# EXECUTIVE PROFILE



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[www.EVGroup.com](http://www.EVGroup.com)



With 20 years experience in the semiconductor industry, Lindner's past work includes involvement in many aspects of semiconductor and MEMS equipment manufacturing.

Lindner began working at EV Group in 1988 as a mechanical design engineer. His responsibilities included the design of various semiconductor processing systems and tooling for custom applications, including innovative system designs pioneered in the first commercially available wafer bonders, silicon-on-insulator (SOI) bonding systems and precision alignment systems for 3D interconnect applications. Paul Lindner received his electrical engineering degree from HTL Braunaau in Austria.

Prior to his appointment as Executive Technology Director, Lindner established a product management department at EV Group. During that time he was involved in marketing, sales, manufacturing and on-site process support. Customer orientation throughout all steps of product development, innovation and implementation in a production environment are among the main goals of EV Group's technology groups headed by Lindner.

His current responsibilities include

## **invent – innovate – implement**

### **EV Group explores new techniques and serves next generation applications of micro- and nano-fabrication technologies**

*Chip Scale Review staff interviews Paul Lindner, Executive Technology Director*



**EVG headquarters in St. Florian am Inn, Austria.**

new technology development by heading R&D, product, and quality management, business development and process technology departments.

#### **■ How will EVG stay competitive with respect to continuing the development of thin-wafer handling technologies?**

EVG has a diversified product portfolio for thin-wafer handling, and pioneered the technology for power devices, compound semiconductors and mainstream memory and logic. This includes the capability to handle unsupported thinned wafers, temporary wafer bonding for subsequent chip stacking and permanent bonding for wafer stacking. Ongoing and early R&D investments in combination with close partnerships with end users enable us to innovate and implement thin-wafer handling technology in high-volume manufacturing.

#### **■ How are thin-wafer handling technologies evolving (e.g., development of advanced power devices, etc.)?**

No single solution fits all applications

today—this will remain the case as these technologies evolve. The material properties of temporary bonding adhesives carry distinct importance in defining a working solution, especially for thin-wafer handling. On the other hand, adhesives have to work hand in hand with the wafer bonding and debonding equipment, with a special focus on high-volume manufacturing. The challenge is to fit everything together. We are openly collaborating with our adhesive partners to leverage our solutions to support a wide variety of bonding applications and offer greater process flexibility for users. At this time, we have multiple established technologies in production, and several more are undergoing qualification now.

#### **■ How is EVG managing the financial challenges that come with its R&D roadmap schedule (e.g., internal R&D, external R&D, consortia activities, etc.)? Can you provide an update on some of these activities?**

EVG invests about 20% of its revenues into R&D for next-generation products. Additionally, we have partnerships with many leading

industrial research centers. For example, we launched a three-year common lab with CEA-Leti to optimize temporary- and permanent-bonding technologies related to 3D TSV integration and all direct bonding heterostructures. The lab, which continues more than 10 years of collaboration between the two organizations, is focused on hardware, software and process development.

**How do you see the bonding/debonding technology roadmap unfolding in the next 2-3 years? What about within the next 5 years? Are there any activities the industry needs to do a better job of evaluating or exploring or funding to meet the evolving needs of its (packaging) technology roadmap?**

We expect that cost pressure will drive a trend for monolithic integration (e.g., just DRAM dies stacked) at the wafer level. The elimination of dicing and subsequent stacking at the chip level will increase throughputs and enable greater scalability to smaller interconnect pitches. On the other hand, thin-wafer handling and processing will see consolidation to fewer working solutions. Special focus on thin-wafer processing will stem from more advanced packaging concepts, along with thin and highly integrated packages.

**Do you have any other comments or observations about the packaging industry you would like to share with our readers?**

Advanced packaging is the most rapidly developing field right now. Packaging will play a greater role in increasing system-in-package performance. At the same time, advanced packaging will be used to increase system-in-package functionality. In this sense, a trend that started in MEMS—namely, fusion of several chip functionalities in one package—will gain importance for other applications.

## About

EV Group (EVG) is a leader in wafer-processing solutions for semiconductor, MEMS and nanotechnology applications. Through close collaboration with customers, EVG implements a flexible manufacturing model to develop reliable, high-quality, low-cost-of-ownership systems that are easily integrated into fab lines. Key products include wafer bonding,



## Mission statement

EV Group's vision of exploring new techniques and serving next-generation applications of micro- and nano-fabrication technologies enables end users to successfully commercialize their new product ideas. The company's

Triple i-approach (invent - innovate - implement) is supported by a vertical integration, which allows EVG to respond quickly to new technology developments, apply the technology to manufacturing

challenges, and expedite device manufacturing in high volume.

A key aspect of the Triple i-approach is having comprehensive process knowledge built up over decades of experience. With state-of-the-art application labs and cleanrooms at its headquarters in Austria and in the U.S. and Japan, as well as in-house teams of process experts at its headquarters and all of its subsidiaries, the company is focused on delivering process expertise to its growing global customer base every step of the way—from initial development through final integration at the end user's site. Process development teams can provide equipment demonstrations, process development support and small-volume pilot-line production for custom applications, as well as independent research with partners to explore and develop baseline processes that open up new market opportunities.



**EVG is a leading supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets.**

lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems.

EV Group also holds a leading position in NIL and lithography for advanced packaging and MEMS. Leveraging a combination of industry-leading products and process expertise, EV Group helps end users to achieve cost-effective implementation of emerging semiconductor technologies such as through-silicon-via (TSV) processes for chip packaging and MEMS/sensors. Other target semiconductor-related markets include silicon-on-insulator (SOI), compound semiconductor, and silicon-based power-device solutions.

Founded in 1980, EVG is headquartered in St. Florian, Austria, and operates via a global customer support network, with subsidiaries in Tempe, AZ.; Albany, NY; Yokohama and Fukuoka, Japan; Seoul, Korea; Chung-Li, Taiwan and Shanghai, China.

# 2.5D TSV enablement of a multiple processor SiP

By Deborah Patterson, Mike Kelly, Rick Reed [[Amkor Technology, Inc.](#)]; Steve Eplett [[Open-Silicon, Inc.](#)] and Zafer Kutlu, Ramakanth Alapati [[GLOBALFOUNDRIES](#)][1]

The movement to 2.5D TSV package architecture has been a methodical undertaking. The skyrocketing cost of next-generation process node adoption has accelerated a shift in mindset away from the routine acceptance of transistor scaling for complex, new system-on-chip (SoC) designs and toward alternative options that maintain competitiveness. In addition, 2.5D TSV system-in-package (SiP) designs are also seeing interest in end use applications that may require the integration of components that are not yet defined well enough for SoC implementation. Interposer-based construction provides the speed, bandwidth, power efficiency and modularity that traditional multi-chip packages cannot implement. Cost reduction, faster time-to-market, yield improvement, component flexibility and re-use, and reduced program risk are additional expected benefits.

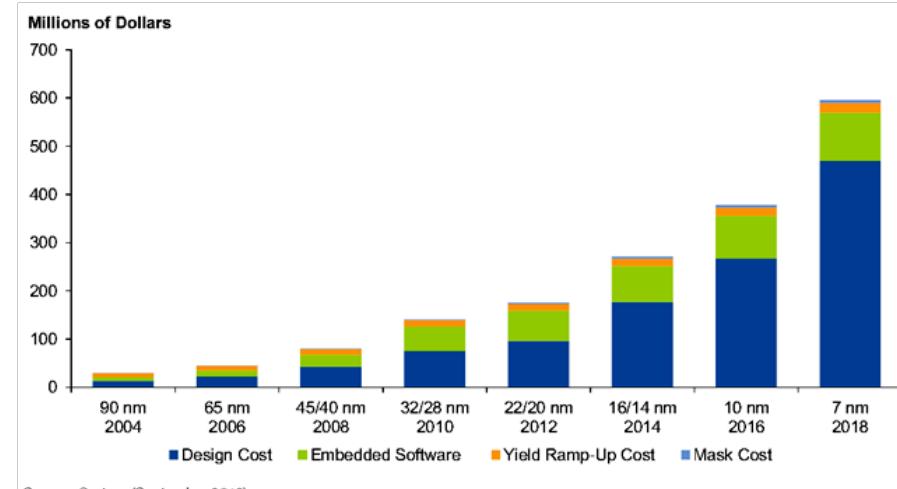
## Industry drivers for 2.5D through-silicon vias (TSVs)

System-on-chip design costs are forecast around \$300M as manufacturing moves into 16/14nm FinFET technologies. Although not as expensive, the adoption of updated tools to work with more sophisticated versions of older process nodes also contributes significantly to cost. Prudent use of existing IP, software, design and manufacturing tools, and other infrastructure can still run \$20M-\$50M per SoC design. The immense costs and longer timelines required to design and manufacture leading-edge SoCs have resulted in two significant changes: 1) Only the largest applications and markets are now targeted in order to recoup the considerable up-front investment; and 2) The number of

companies with resources to design next-generation technology nodes are rapidly shrinking.

For next-generation SoCs, lifetime revenue requirements now demand multi-billions of dollars in return to be economically feasible. **Figure 1** illustrates how “design costs for advanced SoCs have more than doubled, on average, for each node

improvements enabling new applications; 2) Smaller form factor; 3) Silicon layer count reduction for reduced cost and cycle time; 4) Employment of die utilizing the best technology node at the best price and performance (keeping foundry capex down); 5) Die partitioning and optimization for memory, analog, performance, power management, etc.;



Source: Gartner (September 2013)

**Figure 1:** Estimated design costs for next-generation SoCs. SOURCE: Gartner (September 2013)

during the last 10 years [2].”

Because of these trends, more cost effective alternatives such as 2.5D TSV SiP solutions are being evaluated prior to migrating to the next silicon process node. Advanced 2.5D SiP architectures can support leading edge system performance requirements while reducing time-to-market and lowering total cost-of-ownership as compared to new, packaged SoC platforms.

2.5D TSV architecture represents a viable approach to single package system design and allows for benefits such as: 1) Power and performance

6) Higher effective die yields obtained through die recovery; 7) Integration of memory technologies with clear downstream benefits for bandwidth and power; serving as replacements to eDRAM/eFlash; 8) Accelerated time-to-market; and 9) Risk reduction in the schedule.

Several of the benefits listed above offset the costs of an interposer and the more complex 2.5D assembly for an increasing range of applications. In addition, for customers with proven IP that is typically ported to each new process node, IP migration

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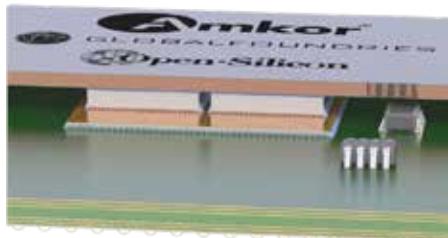


could be deferred. Third party design houses may choose to offer core IP as a shared resource across multiple users, amortizing development costs or applying the IP across multiple markets. The ability to extend core IP through re-use, or leverage it across multiple platforms, offsets the full NRE costs that individual companies would normally incur, thereby introducing a new IP usage model.

## Package design and functional results

The 2.5D TSV SiP integrated two 28nm SoC ARM dual core Cortex™-A9 processors to extend processor function and reduce product risk. As with

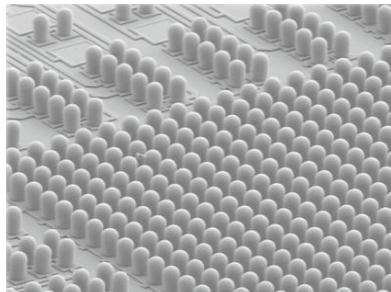
a)



repartitioned monolithic die, multiple independent ICs are similarly reliant on a silicon node or package interconnect density that can either preserve or limit inter-chip communication.

The silicon interposer was designed to provide a 16GB/sec full duplex data rate between these two devices. A 65nm process technology allowed for finer grain and lower power connectivity, reducing both form factor and overall power budgets. **Figure 2** illustrates the two side-by-side processors connected through the single silicon interposer. A view of the copper pillar bump array on the bottom side of the processors is also shown. **Table 1** defines basic structural elements of the package.

b)

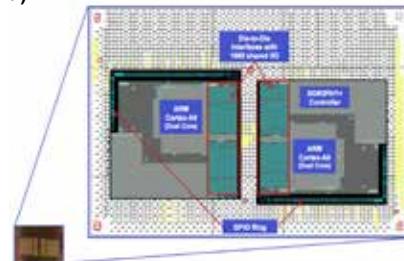


**Figure 2:** a) (left) Illustration of the two ARM Cortex™-A9 processors connected through b) (right) a silicon interposer by copper pillar micro-bumps. This SiP was designed for low power (although the lid could be employed as a heat spreader if thermal conditions necessitated this use).

Package					
Body Size	27.0 mm x 27.0 mm	Max. Thickness	2.78 mm	Ball Count	671
Processor					
Die Size	4.1 mm x 4.5 mm	Thickness	0.600 mm		
Bump Pitch (Cu Pillar)	40 µm	Bump Height (Cu Pillar)	40 µm		
Interposer					
Die Size	10.8 mm x 7.4 mm	Top Side Pad	NiAu	Bottom Side Solder Bump Height	80 µm
Thickness	~100 µm	Top Side Pad Pitch	40 µm	Bottom Side Solder Bump Pitch	170 µm

**Table 1:** 2.5D SiP package structure.

a)



b)



**Figure 3:** a) Outline of two ARM Cortex™-A9 dual core processors, connected through a 65nm silicon interposer; b) the interposer (shown at the lower left of 3a) with its TSVs and topside metallization.

## Interposer design

The most important consideration in joining the 28nm processors to the 65nm interposer was not just routing signals through copper pillar flip-chip interconnects and tight circuit geometries, although these structural elements do enable high performance electrical compliance. The fundamental understanding was that the single device architecture had to be modified to take full advantage of a 2.5D structure. From a functional level, the demonstration showcased how a multiple processor layout could be optimized in ways that would keep die-to-die I/O power low, reduce die-to-die I/O size (while maintaining adequate ESD protection), and optimize functional testing to highlight the competitive merit of multiple die systems.

Facilitating a low power design meant creating a pathway that would support the data rate across both processors through the silicon interposer. The interposer was comprised of four copper metal layers and an aluminum final metal layer with TSVs. The interposer construction used a 65nm back-end-of-line (BEOL) integration process flow at the foundry. The copper interconnection between the chips was designed with minimum 1µm line/space geometry.

The interposer connected 1,660 signals between the two processors. The spacing preserved a die-to-die distance of 0.5mm, though the interface was designed to support up to a 4mm maximum signal length between the die. After leaving the foundry, the interposer was thinned to 100µm to expose the 10µm diameter TSVs. **Figure 3** shows the layout of the two processors on the silicon interposer with a photo of the interposer displaying its topside pad metallization at the lower left.

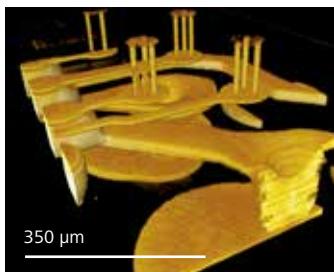
A single redistribution layer (RDL) on the backside of the interposer was used to connect the TSVs to lead-free solder bumps at a 170µm array pitch. These lead-free solder bumps joined the interposer to the 27mm x 27mm high-density build-up (HDBU) package substrate. The substrate comprised a 4-2-4 layer stack and 0.4mm thick core. **Figure 4** shows a cross section of the die/interposer/substrate construction and representative copper pillar and solder bump joints.

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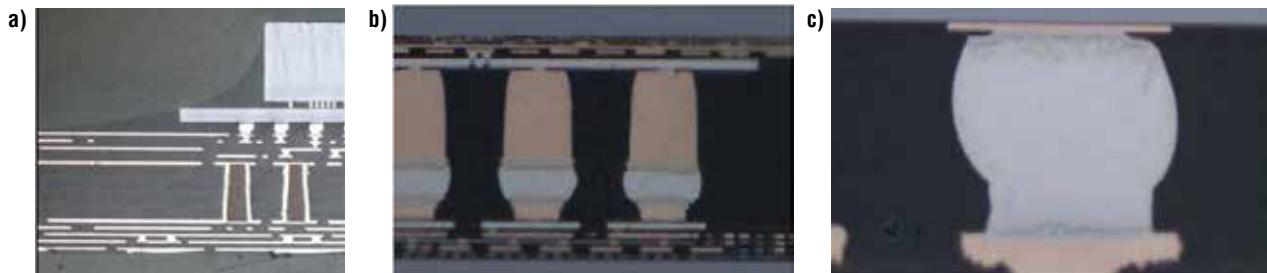
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**Figure 4:** a) Cross section of the 2.5D TSV SiP, b) representative Cu pillar micro-bumps at 40µm pitch, and c) representative SnAg flip-chip solder bump at 170µm pitch.



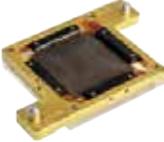
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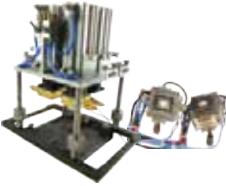
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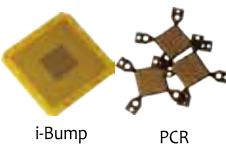
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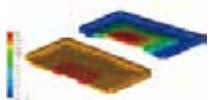
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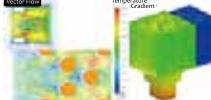
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### Concurrent IC and package design produces optimized systems

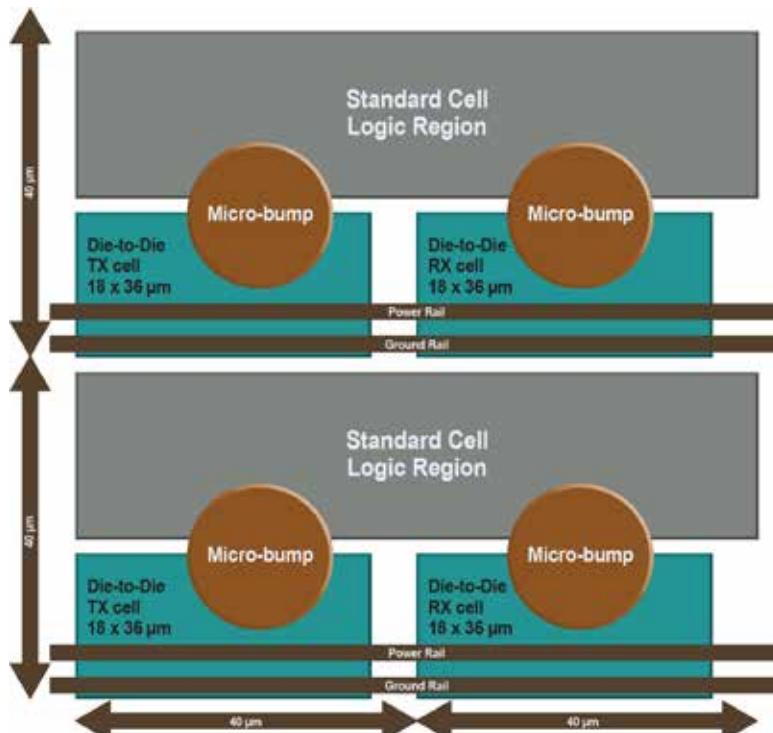
Whereas the interposer employs 65nm node technology, the processors were manufactured using a 28nm super low power (28nm-SLP) process. The goal was to design the processor as small as possible, reduce the power, and ensure that the distances between the I/O drivers were short.

**Driving power down, and speed up.** Power is costly to manage and limits performance. In mobile applications, a shutdown of the processor will occur if maximum skin temperature is reached. In computing, the power required to drive external memory reduces graphics and processor performance. In networking, over 50% of data center cost is due to cooling. At the device level, a junction temperature ( $T_j$ ) in excess of 80°C will increase the DRAM refresh rate, increasing both power and heat. Conversely, high-performance memory that uses massively parallel I/Os keeps power down, but requires very dense routing (that can also be provided in the form of interposer support). Therefore, demonstrating low signal I/O power was a fundamental requirement. Fortunately, it is also a feature that favors the 2.5D interposer system architecture, yielding performance advantages.

Besides the low power offering, the intra-die processor interconnect supports a very wide, higher speed data bus. A data bus is like a highway that connects the processor to the memory. The wider the bus (ex: 64-bit as compared to 32-bit), the more data that can be moved down the highway at the same time, allowing for faster access. To create a high-speed data bus between the two processors, copper pillar micro-bumps were positioned underneath the standard cell logic region of the processor interconnect at a 40µm pitch.

The custom placement of the copper

pillar micro-bumps produced several benefits. First, the system designer placed the output (TX/transmit) and input (RX/receive) cells within the logic region next to each other. The copper pillar micro-bumps were then positioned over each of these adjacent cells. This placement allowed for an efficient way to test the processor interconnects – not easy with over 1600 fine-pitch bumped I/Os. Because most wafer probe design-for-test (DFT) solutions reuse ASIC test methodology, wafer probe cards and ATE equipment suitable to test thousands of I/Os can be prohibitively expensive. Instead of a more traditional wafer probe solution, the chip designers embedded a test loopback capability into each of the adjacent input (RX) and output (TX) I/Os. This provided a way to test the wafer through electrical boundary scan. It allowed for nearly complete coverage at wafer probe using an extremely cost-effective probe card. **Figure 5** illustrates a top-down view of the logic area within the processor along with the concurrently designed copper pillar micro-bump layout.

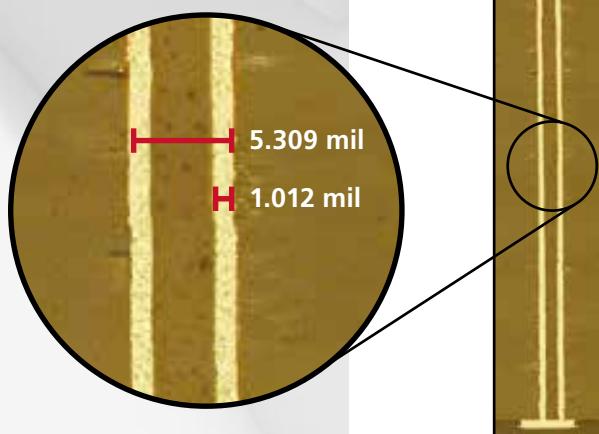


**Figure 5:** Top down view of a small region of the die-to-die interface (ref. Fig. 2). Relative positioning and size of the I/O cell layout with Cu pillar micro-bump placement for die-to-die interconnection through the 2.5D interposer.

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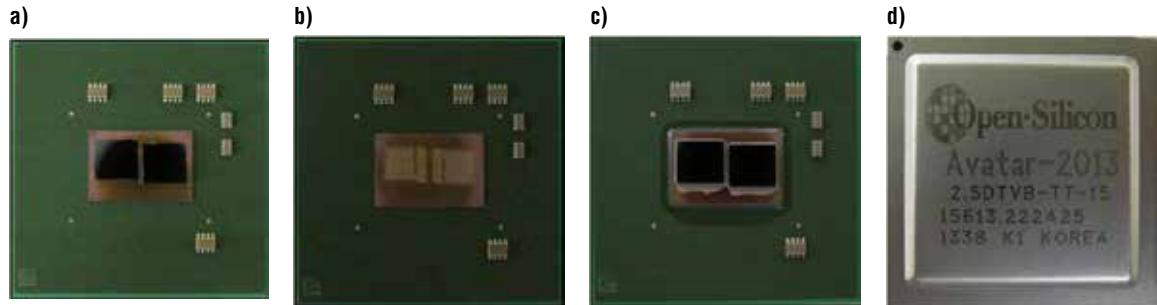
**The value-add of test.** The importance of test for 2.5D applications cannot be overstated. The sheer number of I/Os between die, interposer and substrate is unforgiving, and a cost-effective 2.5D solution must

produce high yields on final assembled parts. Wafer-level test provides full coverage and identifies known-good-die (KGD). The yielding components are then chosen for multi-die assembly to proactively address downstream fallout. For multiple integrated devices (SiP), independent access to each die is required and all interconnects are tested to confirm functional integration.

Once each die is characterized, it is possible to mix and match high and low leakage providing that both die are fully functional. Additionally, if architected into production chips, devices with failed sectors (akin to binning) could be offset against a functional mate with a net result of “recovering” die through test, providing a value-added service to this process (effectively raising yield).

**Shrinking the die area through effective supply chain collaboration.** A reduction in electrostatic discharge (ESD) protection for the die-to-die I/Os allowed for a reduction in I/O area. This is particularly significant when I/O counts increase into the thousands because area savings can now decrease proportionally. In addition, reducing ESD charge helps reduce capacitive loading, thereby increasing the line bandwidth for the data exchange between receiver and transmitter I/Os.

If a discharge occurs in the 2.5D assembly process, it would most likely arise when a bumped logic die first comes into contact with the metal bond pad of the interposer. Several different I/Os with varying ESD protection schemes were designed. Upon testing, it was found that the ESD requirement for the die-to-die I/Os could be relaxed while still doubling ESD protection targets. This contribution to a more efficient I/O design translated into improved data bandwidth, power, and area simultaneously.



**Figure 6:** (left to right) a) Interposer placement on the high-density build-up substrate, and b) the two processors mounted on the interposer, c) after underfill application, and d) after lid attach.

The I/O cell for die-to-die communication occupied an area of only  $18\mu\text{m} \times 36\mu\text{m}$  and fit handily within the  $40\mu\text{m}$  pitch of the copper pillar micro-bumps. I/O power was estimated to be 0.5-0.6 picojoule/bit. This low I/O power is a critical requirement for reaching higher bandwidths in products with tight overall power budgets. It is an example of a design element that directly translates into the interposer structure.

The adjacent input (RX) and output (TX) cells fitting under the individual  $40\mu\text{m}$  copper pillar interconnects resulted in a 78% area reduction as compared to general purpose I/O placement. The die-to-die bridge area was 50% smaller and fully characterized. The large number of I/Os supported by the interposer made for a robust power grid and provided for very low power per I/O.

Although a silicon interposer was chosen for this application, silicon interposers, organic interposers and fine grain substrates represent a continuum of price, performance and density. The right solution per SiP will shift as the capabilities of each improve over time. The design effectively combined the 28nm-SLP die with the 65nm interposer to support size and power reductions, efficient test methodology, and high speed and bandwidth design.

## Assembly

Final assembly utilized advanced TSV packaging technologies. Prior to assembly, both the processor dice and interposer go through the bumping process in wafer form. The processor wafers emerge with copper pillar micro-bumps and the interposer wafers have SnAg solder bumps.

The assembly flow is straightforward with the substrate going through an initial bake followed by chip capacitor attach. Interposer placement onto the substrate

through solder bump reflow follows. The processors are then placed on top of the interposer and undergo a mass reflow process to join the die to the interposer. Underfill is applied to both the copper pillar micro-bumps and the SnAg flip-chip solder bumps at the same time. Lid attach is then followed by laser marking and ball attach (BGA) as the final step in the assembly flow. **Figure 6** shows how small the interposer footprint actually is compared to the area required by the substrate to fan out the ball grid array. The substrate footprint is defined by the total solder ball count which, in this case, is  $27\text{mm} \times 27\text{mm}$  with depopulated corners for a total of 621 balls at a  $1.0\text{mm}$  pitch.

## SiP performance

The IC design and 2.5D TSV architecture enabled considerable bandwidth while maintaining high speed and low power operation. The system showcased 1GHz ARM dual core processor operation utilizing 28nm-SLP process technology, supporting memory (DDR3 at 1333Mbps), a boot-ROM (memory chip that allows a workstation to be booted from a server or other remote location), software that controlled die-to-die communication, general purpose input/output (GPIO) signaling, peripheral devices (i.e., on-board monitor), and an assortment of test functions. The functional die bridge that enabled high bandwidth communication between the processors was successfully characterized. During validation, the interface worked immediately at its (conservative) 500MHz design target. Dedicated I/O test structures were characterized and they appear capable of performance of at least 2GHz.

## Applications

One application segment for the Cortex™-A9 processor SiP includes

low power mobile devices and servers. Another application targets home gateways that require both low power and massive die-to-die bandwidth.

In general, perhaps the most common application for 2.5D packaging is SoC plus memory with half of all silicon IP targeting this area. Interposers support massive wide parallel buses between memory and logic devices, improving speed and significantly reducing power consumption. High-bandwidth memory (HBM) and Wide I/O memory are clear candidates for 2.5D integration.

The limitations of SoC are strongly seen in some general purpose ASIC designs with large serial memory interfaces that utilize external memory. Silicon node shrinks result in increasing SerDes data that is bumping up against die area constraints. By porting SerDes and large on-chip memories onto discrete die, “the need to move to the latest silicon node can be reserved for only the highest performance functions” [3], i.e. processors. 2.5D materials and designs for extraction models supporting a SerDes interface have since been

characterized. Efficient use of 2.5D SiP architecture can reduce die size, power usage, and cost.

High-performance products such as smart TVs, high-end cameras (DSC, SLR, video) and computers will benefit from this type of package construction by having very high speed CPUs connect to differentiated accelerator chips through (high bandwidth) silicon interposers – further reducing cost if a custom CPU die is not needed.

Other applications include SoC plus complex analog, RF, and high-speed interface for industrial, medical, testing, high-end commercial, and networking/telecom ASICs. SoC plus FPGA is a specialized application for fast time-to-market and customized requirements, while SoC plus other logic will enable IP re-use to reduce total cost-of-ownership.

### Summary

The program affirmed the collaborative business model and swift responsiveness of the supply channel. Investment in infrastructure and process

can take years to develop. The program defined and vetted the entire ecosystem from system designer, to foundry, to assembly and test provider. The emphasis on concurrent processor and interposer design optimized performance and design-for-cost advantages.

Foundry and system-level value adds included characterization of materials and validation of a process design kit (PDK). An enhanced EDA reference flow for 2.5D TSV design was created by the foundry to address top level interposer design and floor planning, TSV usage, front- and back-side interconnect and redistribution (routing). Software execution through a dual processor system included design-for-test (DFT) strategies that were shown to both validate performance and increase yields.

The program showcased a supply chain that came together to produce a “first time right” fully functional product demonstration. These competencies will help promote adoption of 2.5D SiP packaging for a broad range of leading edge designs.



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## Acknowledgements

The authors thank Abu Eghan and Abhishek Chhajer, responsible for substrate and interposer designs, respectively, at Open-Silicon. Acknowledgments also go to: Ravi Gutala on PDK support, Manjunath Prabhu's ESD design guidance. Jens Oswald, Christian Goetze, Samuel George, Juan Boon Tan, Wei Liu, Shun Qiang Gong, and Adam Beece from GLOBALFOUNDRIES, similarly contributed to the successful outcome of the program. The authors thank and acknowledge WonChul Do, EunHo Park, YoungRae Kim, DongHoon Han, and Yonglae Ko of the Amkor K1 R&D team located in Seoul, Korea, for their timely support and dedication. Recognition goes to David McCann, VP of Packaging Technology at GLOBALFOUNDRIES, and Ron Huemoeller, SVP of Advanced Product Development at Amkor Technology, for supporting this project.

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# The “active-interposer” concept for high-performance chip-to-chip connections

By Séverine Chéramy, Fabien Clermidy, Gilles Simon, Patrick Leduc [[CEA-Leti](#)]

**I**t is clear now that we are entering the era of zettabytes of information ( $10^{21}$  bytes). The combined capacity for data storage globally already passed the zettabyte threshold, while global internet traffic is expected to reach this threshold in 2015, and continue growing. High-definition video streaming, the consolidation of internet-based services, and the increasing number and capabilities of smartphones, tablets and other wireless devices contribute to the rapidly growing traffic. Data centers, the heart of the internet for data storage and processing, must be adapted to this growing market. As the internet is already responsible for more than 2% of global power consumption, power efficiency for these data center infrastructures becomes a serious challenge for society. For data centers, the zettabyte era will have to be a “green” computing era. Europe’s EUROSERVER initiative is addressing this challenge by developing a new generation of processing technology, based on low-power CMOS and 3D integration. Large processors are partitioned into small and low-power chiplets stacked on a large interposer. Using this technology, a 50x improvement of processor power efficiency is expected. Silicon interposers, and more particularly the performance of chip-to-chip connections on interposers, are key technologies to provide a cost- and power-effective solution. To go further, we propose in this paper to introduce the new concept of “active interposer,” a high-performance interposer that embeds some logic functions and power management.

## Architecture

To begin, let’s consider the concept of

chiplet and active interposer. The main idea is to design a chiplet, or duplicable computing unit. This chiplet is a high-performance computing dice realized in the most advanced technology node. It is a generic and modular tile and the interposer supports the chiplet. Thanks to its “active” behavior, it is used to customize the assembly for a dedicated application. The objectives of this interposer are to efficiently connect heterogeneous or homogeneous chiplets, support power management, provide test and debug features, and provide high-speed links between top-level chips and with the outside.

The main targeted advantages are: reduced non-recurring expenses (NRE) thanks to chiplet re-use in a large range of applications; increased yield through smaller die compared to classic large-size high-performance ASICs or ASSPs; and reduced cost thanks to integrated power management. All these advantages should be obtained without sacrificing performance. The domain of servers and micro-servers can benefit from such a technology, as modular and flexible performance is required, while maintaining the main computing tile.

As stated before, however, going 3D requires a modular approach, and thus the partitioning of existing multi-core architectures. With the multiplication of the number of cores, communication between cores and with internal and external memories becomes the main challenge (the so-called “memory wall”). Consequently, high bandwidth as well as low latency are required. To summarize: modular, flexible, high-bandwidth and low-latency 3D plug connections are required.

Asynchronous network-on-chip (ANoC) is an appealing solution for such a problem: thanks to its handshake-based protocol, it provides the required

flexibility (natural adaptation to heterogeneous technologies) and a low latency [1], while its topology can be adapted to the modularity demand. Being event-based, its power efficiency has already been proven with a 5x gain compared to synchronous solutions [2]. However, it also comes with a high number of signals, which is 2.5x the amount of data to be transmitted.

Let’s consider as an example a 64-bit, 16-core chiplet running at 2GHz. Each core comes with a 16KB instruction cache, a 16KB data cache (the full system embeds 256KB of L2 cache), and 4MB of L3 cache. In this example, the required input/output bandwidth is estimated at around 20GB/s. A typical ANoC configuration can reach a 1GHz equivalent frequency (i.e., 1ns total round-trip protocol). Thus, 160 data bits are needed, leading to 400 signals. At this targeted performance, only 2mm can be run between repeaters in a standard 28nm technology node. Consequently, buffers must be put on the interposer, which then becomes “active.” Thanks to such a solution, in/out data latency is limited to 2ns compared to a few tens of nanoseconds with serializer/deserializer solutions. Meanwhile, energy savings on data transmission reaches a 4x gain compared to low-power serial transmission schemes at less than 1pJ/bit [3].

To achieve further gains in integration and power efficiency, the second step should include a DC/DC converter on the active interposer. Here, the objective is to avoid external inductance and used capacitance-based DC/DC units. A single external power manager delivering 1.8V will then be necessary. Available area on the interposer or advanced technologies will be used to provide the required capacitances. A full-power scheme will then be provided

on the interposer, allowing selection of voltage domain as well as power cut-off per chiplet. **Figure 1** gives an overview of the active interposer concept.

### Challenging 3D process stages

The following design rules are expected from the architecture described above: an interposer size of about  $120\text{mm}^2$ , 65nm node and 6 top die of about  $20\text{mm}^2$ , and 28nm node. The 3D-IC stack leads to several key challenging process steps that will be described next.

**Chip-to-chip connections.** Chip-to-chip connections with a high density of interconnects ( $20\mu\text{m}$  pitch or lower) between chiplets and interposer are required to improve the global power efficiency of the system. Die-to-wafer is used for this 6-top die interposer.

Two types of interconnects can be tested: the first one uses direct Cu-to-Cu bonding, with no underfill; the second one uses copper-pillar technology, and therefore uses underfill to fill the gap between chips. Both types of interconnects can offer a  $20\mu\text{m}$  pitch interconnection, but with a very different

integration flow.

Cu-to-Cu bonding is a back-end compliant technology, in comparison with copper pillar, which is more a “packaging-like” technology. Both were evaluated as both have pros and cons in the industrialization scheme.

The mechanism of Cu-Cu direct bonding has been deeply analyzed and understood at CEA-Leti from the experience of wafer-to-wafer (WtW) bonding [4]. In addition, some excellent work on WtW reliability has shown promising results [5]. Transferring the process to die-to-wafer induces no major modification in the bonding mechanism itself [6], but an intensive work on characterization and reliability has been carried out in order to check any process-link behavior. Recent achievements released no major change on the daisy-chain resistance and similar reliability performance [7]. To reach such performance characteristics, a collective die surface preparation for direct bonding has been implemented to develop defect-free die direct bonding. An accurate pick-and-place tool was adapted to

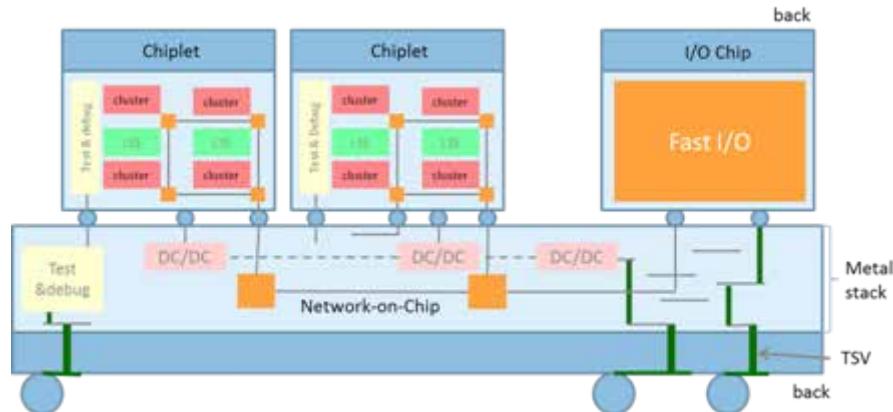
ensure a particle-free environment. After a damascene-like surface preparation, chips were bonded with less than  $1\mu\text{m}$  misalignment. The  $400^\circ\text{C}$  bonded daisy chains on the die-to-wafer structure are perfectly ohmic.

Whichever wafer-to-wafer or die-to-wafer strategy is chosen, or whether 200mm or 300mm wafers are used, the resistance of two bonded lines is equivalent to a simple line of double thickness after a  $200^\circ\text{C}$  thermal treatment. This main result proves that the bonding process has no impact on the resistance. After thermal aging, daisy-chain resistance showed absolutely no shift, proving the robustness of the bonding process (**Figure 2**). This process is therefore perfectly compliant with a  $20\mu\text{m}$  pitch integration, and can even easily be shrunk to less than a  $10\mu\text{m}$  pitch.

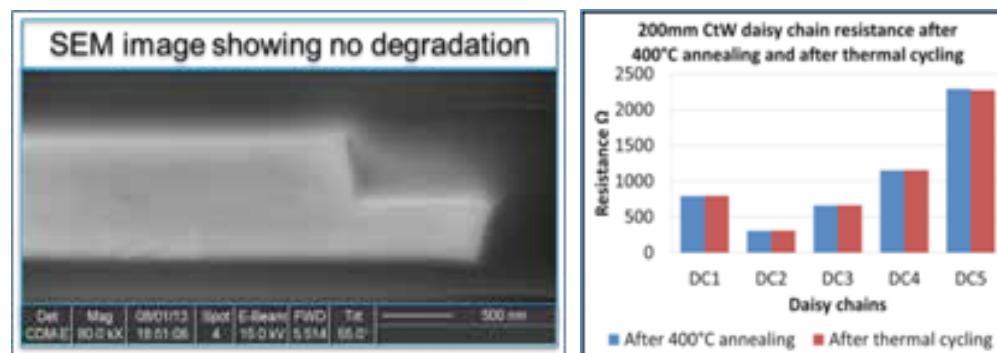
If this stacking is highly promising, especially for a very aggressive pitch, the shrink of copper pillar is also a possibility to consider (classic pitch today, used for wide I/O or passive interposer, for instance, is  $40\mu\text{m}$ ). Intermetallics grow under the influence of time and temperature. Therefore, the copper pillar (copper + solder) will not reach the same stability and reliability in comparison with Cu-Cu bonding, but its ease of manufacturing in an outsourced semiconductor assembly and test (OSAT) factory could bring other industrial advantages.

Classic process steps of copper pillar were developed with associated shrink—the height of the copper shrinks in the same manner as the diameter (keeping a similar aspect ratio). The interconnection density increase, associated with limited space between die (in z, and also x and y dimensions), leads to a modification in the underfill technology.

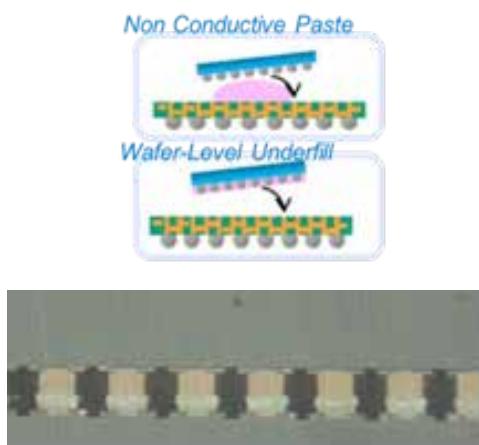
Use of a pre-applied underfill can advantageously replace classic capillary underfill (CUF) to fill the gap between chips. Leti has launched an intensive benchmark on both wafer-level underfill (WLUF) and non-conductive paste (NCP), and compared both approaches with capillary underfill [8]. Process work on daisy-chain wafers has been done on underfill deposition and stacking in order to achieve



**Figure 1:** Schematic view of the interposer concept.



**Figure 2:** Electrical data and cross section after thermal aging.



**Figure 3:** Daisy-chain resistance before and after JEDEC 3 pre-conditioning for wafer-level underfill, non-conductive paste and capillary underfill; and cross section of two die stacked with NCP.

a safe interconnection, without any polymer entrapment or voids in the polymer, which would cause a lack of reliability. We finally conclude that the non-conductive paste seems to be closer to being a mature technology.

**Figure 3** shows the principle of pre-applied underfill, a cross section after

stacking using non-conductive paste, and the resistance shift after JEDEC 3 preconditioning for both types of pre-applied underfill. More intense work is continuing on reliability with non-conductive paste as well as improvement of the wafer-level underfill process.

#### Through-silicon via (TSV) inside

**interposer.** The density required to take the signals out of the interposer is not as high as for the top-bottom interconnection. A TSV-middle approach, with a TSV of 10 $\mu\text{m}$  diameter, is used in a 65nm node device. This process already has been developed and is similar to the integration into wide I/O demonstrator done with STMicroelectronics and ST-Ericsson (Wioming) [9] (**Figure 4**).

**Temporary bonding with a polymer adhesive.** Temporary bonding with a polymer adhesive is used for interposer thinning and further back-side process. Well-known processes (ZoneBOND® or laser debonding), as previously developed and qualified into full demonstration, can be used with no major modification [10]. Nevertheless, limitation in temperature, especially for dielectric plasma-enhanced chemical vapor deposition (PECVD) (isolation silicon/copper redistribution layer), creates some reliability issues

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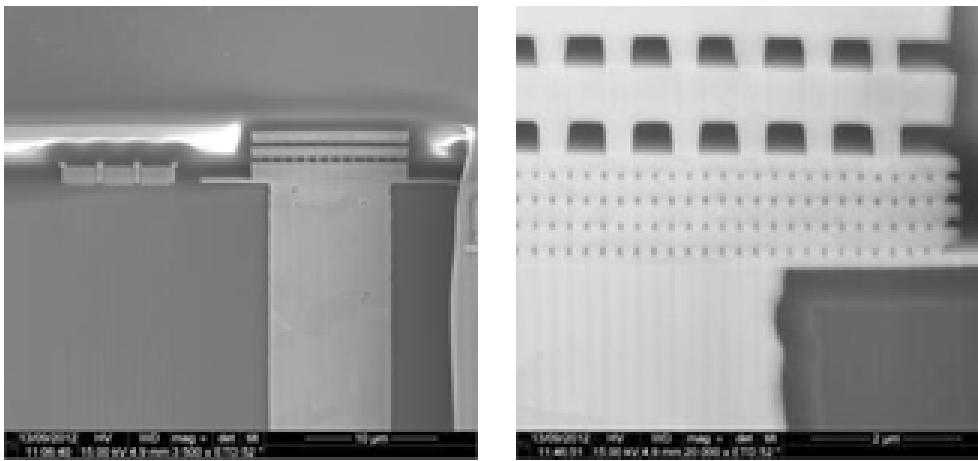
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Wafer Preparation

Dicing

Reticle Die Sorting

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**Figure 4:** TSV-middle integration into 7 metal layers c65nm (courtesy of STMicroelectronics).

and concern, for example, the coupling between Si substrate and package. Higher-temperature resistance of the temporary adhesive (classically, today  $<220^{\circ}\text{C}$  under plasma) is required and should be above  $300^{\circ}\text{C}$ . Work is in progress to reach such a temperature.

**Fine-pitch redistribution layer.** After a classic back-side process to reveal the TSV middle [9], a fine-pitch redistribution layer (line width of  $8\mu\text{m}$  for a  $8\mu\text{m}$  spacing) with aggressive angle ( $45^{\circ}$  was demonstrated), is processed to redirect the signal [11] (Figure 5). Those design rules facilitate

the back-side design of the layer and redistribution toward the BGA.

**Multi-die stacking is required.** If Cu-Cu direct bonding is done before the back-side process (called “stacking-first” integration), in case of fine-pitch copper pillar technology, the classic flow chart would be to stack the thin interposer on its BGA and then the top die on the interposer (“stacking last”). Nevertheless, stacking strategy is still a challenge, as the warp management of the interposer during the full stacking process, from ambient temperature to reflow temperature, is clearly a challenging point for large and thin interposers. If the size of the active interposer is kept reasonable in comparison to what is expected for a passive interposer, multi-die stacking is considered to be difficult.

Again, as for chip-to-chip

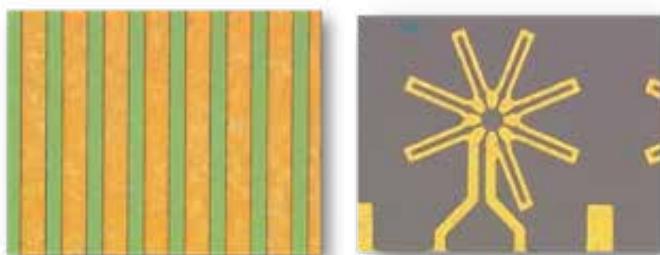
interconnection, work is done in parallel to compare two different approaches: the first is to keep the warp reasonable at die level from ambient temperature to reflow temperature, and the second is to facilitate the stacking with a stacking-first approach.

As said before, even if the active interposer size is kept reasonable, the warp monitoring is a key point that must be addressed during the whole fabrication of the interposer and die stacking. Furthermore, the warp management also will influence the final assembly on substrate, and the reliability during operation. We are working on complementary strategies to keep this warp reasonable from low temperature to reflow temperature; and in parallel, a mandatory study is also underway on a predictive and dynamic model, as well as material and integration characterization.

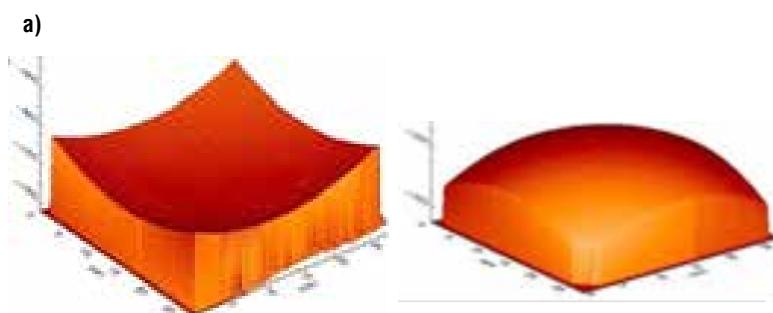
Due to the technological limitation for high-aspect ratio TSV metallization, it is commonly accepted that a maximum core silicon thickness of  $100\mu\text{m}$  is acceptable for the chips or the silicon interposer, compared to the several hundreds typically used. This implies a drastic sensitivity to dielectric-layer stress that induces bow deformation and, so, dedicated developments to limit the stress impact are mandatory.

Specific developments on PECVD silicon oxides and nitrides have been performed [12]. Mineral as well as polymer stress-compensation-layer integration schemes are now under development to balance both side stress and resulting warpage through the full application-temperature range.

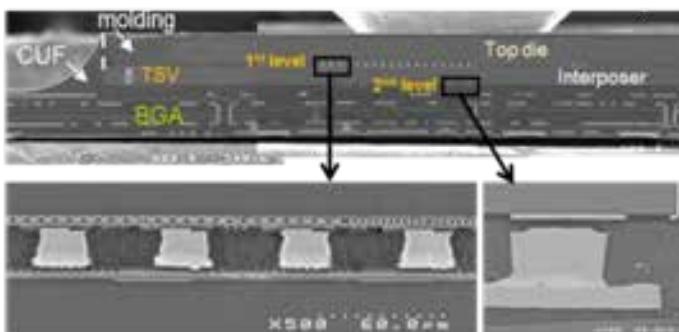
Fries Research & Technology's GmbH (FRT) confocal sensor, nanoindentation



**Figure 5:** Copper ultra-fine pitch redistribution layer (line  $8\mu\text{m}$ /space  $8\mu\text{m}$ ).



**Figure 6:** a) 3D reconstruction of chip topology profile; and b) TDM measurement during reflow.



**Figure 7:** A two-die stack on BGA, using inter-die material.

measurement, and topography and deformation measurement (TDM) permit finely characterized materials and processes involved in stress management (coefficient of thermal expansion, Young's modulus, and thermal dynamic bow) (**Figure 6**). Models and simulation for technology integration ensure a predictive tool through the targeted temperature range. Nevertheless, the first contributor to warp management is definitely the silicon thickness itself. Development of high-aspect ratio TSV, above AR15 and targeting AR20 (work currently under way at Leti), will ensure wider process assembly windows, as well as reliability during operating conditions. The thicker silicon substrate also will allow more comfortable and safe handling for final assembly operations.

In parallel, Leti has chosen to evaluate the stacking-first strategy to facilitate the stacking. As described in previous papers [13] [14], the stacking and underfill are done on a thick interposer, creating a thick topology (at least 100 $\mu$ m); there is no particular issue on this step. To reveal TSV from the back side, an inter-die material (IDM) is used to make the surface planar (**Figure 7**). Warp management and the compatibility of this IDM with subsequent back-side processing are closely monitored. The preliminary work done at Leti on this integration showed good results; the bow, after temporary bonding and interposer thinning at 200 $\mu$ m, while using a silicone-based material for the IDM, is finally lower than 250 $\mu$ m.

### Integration

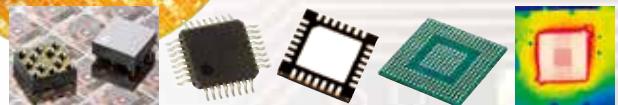
The use of active interposers faces more or less the same technical challenges during the full integration as the passive interposer. Some additional requirements, mainly based on face-to-face, high-density interconnections, are developed in parallel, on a “process bricks” scheme.

Leti has demonstrated in the past its capacity of full integration with its partners [15]. Recently, wide I/O demonstrators and passive interposer realizations (**Figure 8**) have been released and in some manner constitute the first steps towards realizing the active interposer, which will become a reality in 2015.

### Summary

This paper describes the “active” 65nm node interposer concept. Six top die processed in 28nm node will be stacked on this interposer with fine interconnect pitch. High-speed links, power management and test solution will be integrated inside the active interposer. This modular approach would significantly reduce the R&D cost for each design, as well as time-to-market. The technology developed for this integration can be considered as an evolution of the 2.5D interposer, including logic functions

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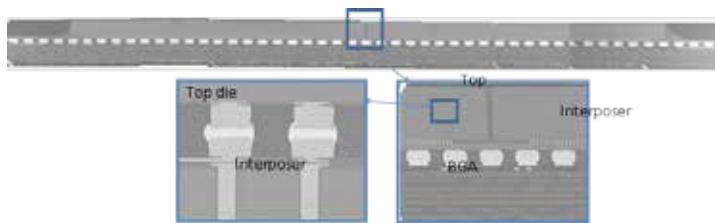


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**Figure 8:** 26 x 26mm x 80 $\mu$ m silicon passive interposer equipped with thick silicon die.

and denser interconnects. Using this technology for server and micro-server applications, 50x improvement of processor power efficiency is expected.

The active interposer is done in the frame of NanoElec Program; this initiative is open to external partners that can benefit from the current work, while bringing additional expertise to the consortium.

### Acknowledgments

This work has been done in close collaboration with our partners STMicroelectronics, SHINKO and Mentor Graphics.

Additionally, this work on active interposers is funded thanks to the French national program “Programme d’Investissements d’Avenir, IRT Nanoelec” ANR-10-AIRT-05.

Finally, the authors would like to thank Leti’s 3D-technology teams that were involved in this work.

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# Next-generation laser structuring method for higher density packages

By Matt Souter [[SÜSS MicroTec Photonic Systems Inc.](#)] and David Clark [[Coherent, Inc.](#)]

**P**hotolithography has long been the dependable standard for structuring organic materials used in advanced packaging. For several reasons, however, this multi-step process is beginning to limit package designs and performance. This article describes excimer laser ablation, a completely different approach to structuring organics that eliminates most of the drawbacks that our industry is now encountering with photolithography. Also discussed are key aspects of a turnkey stepper platform (the ELP300 from SÜSS MicroTec) that is optimized specifically for advanced packaging applications, and that has already enabled several packaging houses to implement excimer laser ablation into their pilot lines.

## The high-density structuring challenge

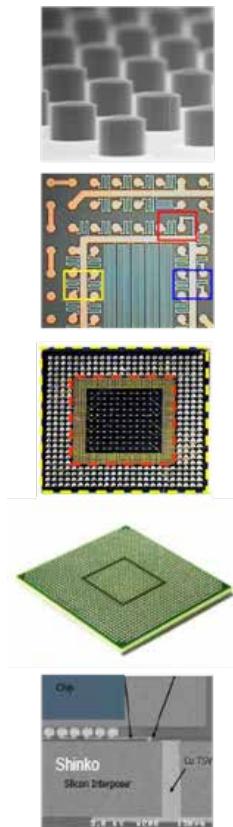
Every type of advanced package, including chip-on-chip, wafer-level packages (WLP; e.g., 2.5D), chip-on-chip stacking, and embedded IC, all have a need to structure thin substrates, redistribution layers, and other package components at high resolution (**Figure 1**). A very common example is drilling vias down to contact pads for applications like fan-in or fan-out WLP. Another emerging example is trenching to form embedded connectors in thin substrates or interposers. In the case of organic dielectrics, these structuring needs have usually been met by some type of lithography, using either a projection light source and photomask, or sometimes by laser direct imaging (LDI). The relentless, consumer-driven push for higher functionality from smaller products, however, is creating a fast-growing need for next-generation packages with smaller feature sizes and tighter pitches, which in turn means the

use of smaller structures (e.g., vias with diameters as small as  $5\mu\text{m}$ ). This situation is beginning to present several challenges for lithography.

Specifically, lithography requires the use of photo-imageable materials, such as polyimides (PIs), PBOs and epoxies. But there is a significant coefficient of thermal expansion (CTE) mismatch between these materials and the chips. Furthermore, higher density packages have bigger thermal loads, exacerbating this problem. As a result, this CTE mismatch can cause issues such as stress damage to low-k dielectrics and wiring layers, which are also getting thinner and, thus, are ever more sensitive to any thermomechanical stress. In addition, these photopolymers are limited in the resolution and via wall angle they can support. In the case of vias for example, this limits the minimum achievable diameter, and interconnect density, as well as their practical aspect ratios.

The magnitude of the problem is obviously package dependent. Devices that are already seeing an impact are those involving larger dies, higher I/O densities, thinner Si chips and substrates, and, obviously, any high heat load applications.

Moreover, lithography is a multi-step process involving developers and other wet chemicals making it increasingly unattractive for two reasons. First, there is the cost-of-ownership associated with these chemicals, and their safe handling



**Figure 1:** Some of the packaging applications that have a common need for via drilling and other structuring tasks.

and disposal. Second, like every other industry, advanced packaging is under pressure to use greener manufacturing that is more energy efficient and less polluting. Eliminating multi-step lithography and its associated chemicals would be very congruent with this goal.

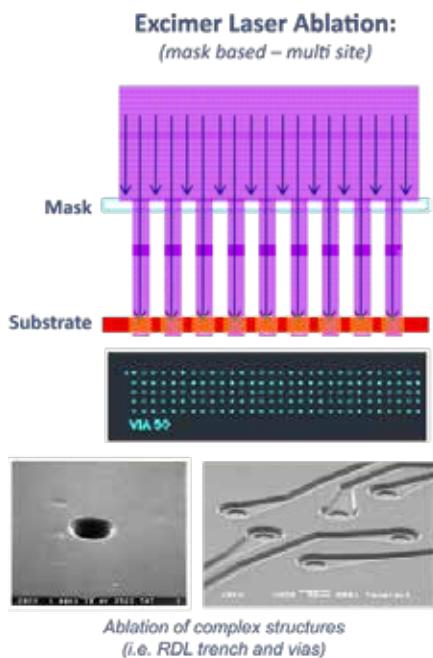
Clearly, a very attractive alternative to photolithography would be a technique that can directly structure PIs, PBOs and epoxies at even higher resolution than today's bleeding edge packages. Excimer laser ablation now provides that alternative while also delivering several other advantages.

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## Excimer UV ablation: a precision subtractive process

Direct ablation with an ultraviolet excimer laser is a dry, one-step technique that has been shown to successfully address the technical limitations discussed above. At a laser output wavelength of either 308 or 248nm, it can be used to pattern a wide variety of dielectrics and thin metal and SiN<sub>x</sub>. It is also particularly well-suited to direct via etching of PIs, PBOs and epoxies to metal contact pads (e.g., Cu, Al, etc.), eliminating the need for thermally inferior photo polymers, as well as the use of lithography chemicals.

What is excimer laser ablation? The excimer is a powerful, pulsed, ultraviolet laser that is well-proven in microlithography, as well as for low-temperature polysilicon annealing (LTPS) for the production of advanced high-resolution LCD and OLED displays. Microlithography uses high repetition rate lasers with low pulse energy, whereas LTPS requires very high pulse energy at modest repetition rates. It is the latter type that is proving well-suited to structuring polymers for advanced packages.



**Figure 2:** Excimer laser ablation is a dry single-step subtractive process where complex structures can be created as defined by a photomask.

(i.e., fluence) is above a material-dependent threshold value, then the high-energy ultraviolet photons directly excite electrons and break interatomic bonds. Along with the subsequent shock wave, this causes material to be ejected at high velocity in the form of a fine powder. Each pulse lasts a few nanoseconds and removes a thin layer of the target in a relatively cold process with almost no thermal effect on the surrounding substrate.

It is important to avoid any confusion and to distinguish excimer ablation from laser direct imaging (LDI). Excimer ablation is a direct and dry one-step subtractive process, whereas LDI is a multi-step photolytic process very similar to lithography except that a focused laser beam directly writes a pattern on a resist (**Figure 2**).



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## Advantages of excimer UV ablation for structuring

There are several advantageous facets of excimer ablation that merit discussion. Unlike most other laser types, the excimer produces a large-area beam that is usually rectangular in cross-section. This beam profile is very compatible with the use of photomasks. Specifically, the beam is used to fill a large-area mask typically fabricated from aluminum on quartz. The reflective aluminum is patterned as the inverse of the pattern to be structured on the actual substrate; the voids in the aluminum define the pattern that will be laser ablated. The photomask output is then reduced through a reduction lens onto the target – the targeted area depends on the laser power and the ablation threshold of the target material. For example, when using the Coherent LSX C300 with a pulse energy of 1.05 Joules, the typical target area in polyimides can be up to 50mm x 50mm.

With the type of photomask process described above, the throughput is very high (i.e., vias per second) and at higher pitches, the number of vias per second actually increases. The reason is that the amount of material removed with each laser pulse, i.e., the depth of any hole or trench, is dependent only on the pulse intensity and the specifics of the target material (Figure 3). So as the number of vias per area increases with the square

of the pitch, the number of through-vias that fit into the field will increase likewise. The parallel drilling rate (holes per second), therefore, actually increases with the square of the pitch size.

Because ablation directly breaks the interatomic bonds with minimal thermal effects, it results in excellent surface quality, no microcracking and no re-cast (melted) debris. The only post-processing cleaning required is a typical plasma/O<sub>2</sub> process. After this, the ablated vias, trenches and other features are perfect for metallization. Contrast this process with the multiple steps involved in photolithography.

Another advantage of excimer laser ablation is high resolution. The smallest feature (x-y axes) that can be imaged with a laser and photomask is related to the laser wavelength and optical resolution of the projection lens. With the standard ELP300 configuration, the system can easily create the 5μm diameter vias that represent the current state of the art for WLP applications.

Excimer laser ablation also provides precision depth (z-axis) control in two ways: either by hitting a hard stop naturally created by a material layer, or by pulsed dosing control (Figure 3). Specifically, the high pulse-to-pulse energy stability of the latest excimer lasers means that every pulse will remove an identical depth of material. So depth control is easily provided simply by programming a

fixed number of pulses at each stepper site location. In addition, excimer laser ablation even allows control of sidewall angle, by adjusting the laser intensity (fluence) and other means. A higher fluence produces a via or trench with steeper sidewalls, whereas a lower fluence results in a shallower sidewall.

Excimer laser ablation is also much more versatile than photolithography in terms of the variety of materials it can directly structure. This versatility enables it to be applied to other packaging tasks beyond via and trench creation. In addition to most organics, it can also pattern SiNx, epoxy mold compounds (EMC – filled and unfilled), as well as thin conductive materials on organic substrates, e.g., Cu, Au, ITO, IZO and CNT up to 0.6μm thick, defined by the photomask (Figure 4).

## Next-generation excimer stepper for packaging applications

SÜSS MicroTec's ELP300 Gen2 fully integrated platform is based on a platform first introduced in 1987. The ELP300 is a 200/300mm bridge tool, specifically designed to address the unique needs of the advanced packaging industry. It incorporates a high-power excimer laser (Coherent LSX C300) that generates pulse energies as high as 1.05 Joules at a repetition rate of 300Hz.

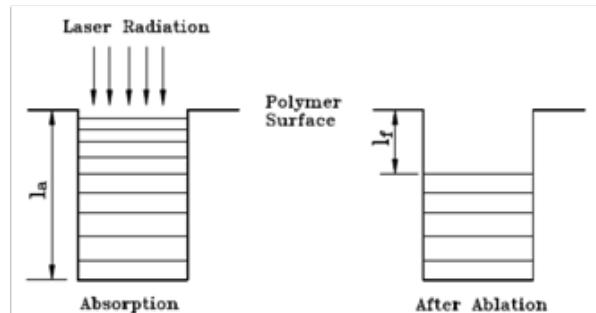
In terms of performance specifics, the system can generate via diameters as small as 1μm and traces as thin as

2.5μm. It includes an automated alignment system – global and site-to-site – with auto pattern recognition. Front side alignment precision is ±1μm. Wafer handling is fully automated and the system can accommodate wafer warpage up to 3mm.

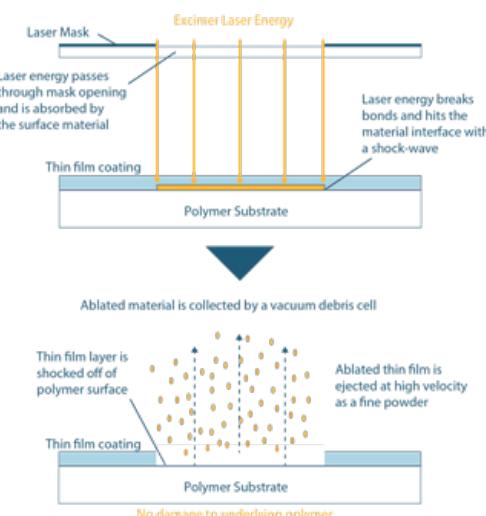
This laser ablation system is specifically designed for high throughput and 24/7 micro-patterning operations

### Depth Control - by No. of Pulses:

- Each pulse removes a certain amount of material
  - + Etch-rate = material removed/pulse
- With a known etch-rate – the number of pulses to reach a desired depth can be predicted and controlled



**Figure 3:** Precision depth control is straightforward with excimer laser ablation by first determining the etch rate per pulse, which is very reproducible, and then controlling the number of pulses.



**Figure 4:** Schematic illustration of how excimer laser pulses are used to remove thin films from a polymer substrate in a dry one-step patterning process.

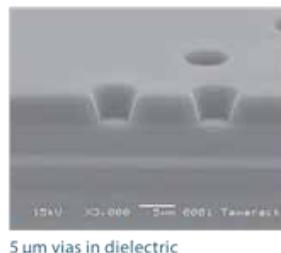
involving micron-sized features that require the highest degree of placement accuracy. The ELP300 Gen2's control system enables highly customized process automation to ensure optimal process capability, throughput, and cost-of-ownership (CoO) for a wide variety of structuring applications in advanced packaging. For example, this system can also be used for other WLP applications, including laser debonding for thin wafer handling, RDL/UBM seed layer removal, and RDL trenching.

### Some examples

**Figures 5-7** show vias and other structures patterned by excimer laser ablation. They all show the clean, debris-free edges and absence of cracking or any other type of thermal damage that are typical when using DPSS and CO<sub>2</sub> laser systems.

### Summary

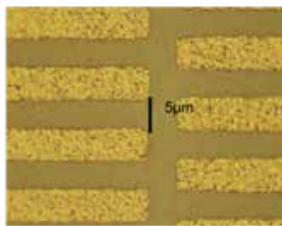
Current trends in advanced packaging mean that photolithography will no



5 μm vias in dielectric



1 μm vias in 25 μm thick PI



5 μm L/S in Au on PET

**Figure 5:** 5 micron vias in dielectric.

**Figure 6:** 1 micron exit vias in 25

thickness PI.

**Figure 7:** Patterning of metal films on polymer: 5 micron Au lines on PET.

longer be an optimum solution for creating vias and other two and three-dimensional structures in many package types. The need for an alternative method is now being met by excimer laser ablation, which eliminates the need to use photopolymers and their associated CTE mismatch, while delivering the required resolution and single-step process simplicity, and avoiding the use of wet etching and developing chemicals. Early adopters are already at the pilot stage and these authors expect production line deployment soon.

### Biographies

Matt Souter received his BS degree in Mechanical Engineering from CSULB, California, and is the Director of Global Laser Systems Global Sales and Product Manager at SÜSS MicroTec Photonic Systems Inc.; email matt.souter@suss.com

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# Effects of device configuration and grounding on test performance

By Jeff Sherry [Johnstech]

In the past, wafer probing was simplistic and commonly, only did enough testing to determine if the device on the wafer was operational to justify placing it in a package. With electronic devices getting smaller and with more functionality, as well as the necessity to operate at higher frequencies, more final testing is being done on the wafer. To reduce cost and space, these chips are assembled in the final system without any extra packaging. This article will outline the effects of ground placement relative to the RF signals in an array structure for a die on a wafer. Although the emphasis will be on wafer-level final testing, the principles of this article can be applied to any array device including packaged BGAs, WLCSP, etc. This article also will present data on how the test fixture or wafer probe used to test these devices (e.g., BGA or WLCSP) will be impacted by location and number of grounds. (e.g., GSG, GSSG).

Additionally, this article will highlight the effects of pitch and probe length on devices in terms of RF performance. Because the IC industry is moving to smaller pitches with more integrated devices and higher I/O counts, performance of the device on both the circuit board and during wafer probe final testing becomes a major factor.

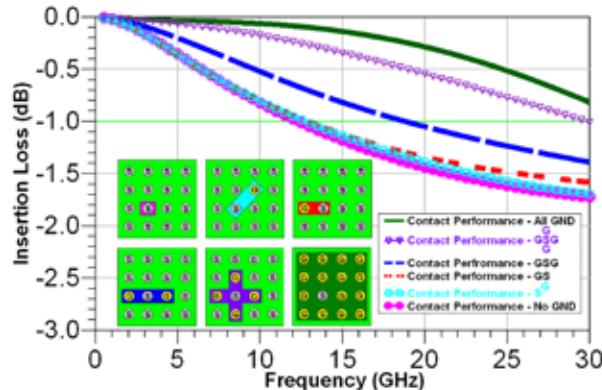
## Placement of ground/returns signals

The data and principles discussed in this paper can be applied to any type of testing including package and wafer testing. Many times, the package size and signal I/O count dictates the number and position of ground (GND) signals. However, this article will show using generated data from high-frequency structure simulator (HFSS) and Advanced Design Software (ADS) simulations that placement of

ground or returns signals becomes more critical for higher RF frequency, or with devices that have gains above 20dB. In general, the closer and more ground or return connections on the device, the lower the loss and the better the frequency response for the tested device. Furthermore, the probe array, socket, or test fixture has a big impact on the test frequency that can be supported by the length and inductance of the probes. The test fixture always will add inductance, and the shorter the probe lengths, the higher the frequency bandwidth.

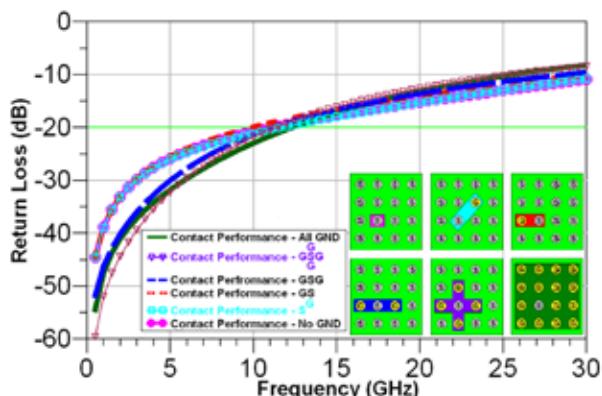
For one signal path through a probe array, the insertion loss is somewhat defined by the length of probe from the load board or probe card to the device. The probe's inductance and capacitance values are defined by the geometry of the probe and the pitch of the I/O. In the past, when devices had only a minimal number of signals because they were not integrated, it was easier to place grounds close to RF signals to get the desired performance. With more functionality being integrated into chips, and with I/O count and pitch defining size, there has been a movement over the years to choose the smallest device package possible. This has sometimes reduced the number of grounds or return signals on the device, or made the center of the device ground for all the signals, such as a quad flat no-leads (QFN) package. Because many fixture designers want to present data only with the best test results, there is a gap in test performance between what is possible and what is real. The rest of the article will explain this situation in more detail.

**Figure 1** shows the difference in insertion loss for different ground configurations on a 400 $\mu$ m pitch wafer-level chip-scale package (WLCSP) array. All simulations used the same 50 Ohms characteristic impedance matched HFSS model and the main signal is in the middle of the array. As expected, the solution with no grounds, or with grounds outside the model, shows the poorest insertion loss with a -1dB insertion loss of around 10GHz. As one ground gets closer to the RF



**Figure 1:** 400 $\mu$ m pitch IQTouch™ micro wafer probe with different ground configurations—insertion loss vs. frequency.

signal, the data improves slightly. When an additional ground is added, the performance improves and the -1dB insertion loss point improves by a factor of almost 2X – to over 18GHz. If the RF signal is surrounded by ground, the bandwidth improves to 39GHz. Surrounding the RF signals by ground effectively creates a coaxial connection and also is a very good shield for crosstalk or isolation measurements. Unfortunately, with I/Os at a premium, it is sometimes hard to justify adding extra grounds that take up chip real estate. However, many times it is cost effective to place multiple ground paths from chip to ground I/O because it reduces the need for extravagant ground

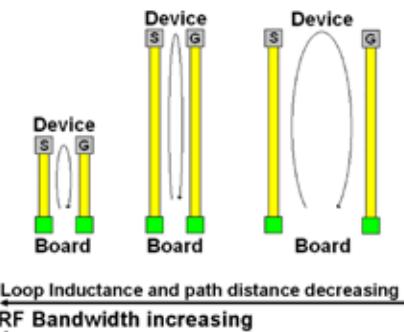


**Figure 2:** 400 $\mu$ m pitch IQTouch™ micro wafer probe with different ground configurations—return loss vs. frequency.

schemes on the board, which usually cost more for customers to implement than the cost of the additional wire bonds.

**Figure 2** shows the return loss performance of the different RF ground configurations for a 400 $\mu$ m WLCSP probe solution. It is interesting to note that the typical return loss specification is -20dB; the reflected signal is 1/100th of the input signal. In all configurations,

the return loss is better than -20dB past 30GHz; this is because the probe itself is very well matched to 50 Ohms due to probe construction, surrounding materials, and defined device pitch. As shown in the figure, the return loss for this probe has better than 10GHz performance for all types of grounding schemes, which indicates a well-designed probe that is matched to 50 Ohms. As more grounds surround the RF signal to create a coaxial connection,



**Figure 3:** RF performance vs. probe length and pitch.

the low frequency return loss does get slightly better. The figure shows data for 400 $\mu$ m pitch. For the same wafer probe contact at 500 $\mu$ m pitch, the return loss performance is better than 20dB out to 40GHz for the GND-SIG-GND configuration. The configuration with one signal in the middle followed by grounds surrounding the signal

on all sides on the rest of the array is sometimes done during testing of the probe to get optimum performance. This can be very unpractical, however, because array devices have more than one I/O and can't afford to place ground completely around the RF signals.

**Figure 3** depicts the effects of pitch on RF probe loop inductance and bandwidth. The shorter the path, the lower the inductance and the higher the bandwidth of the probes. If the return path is not close to the signal, there is an

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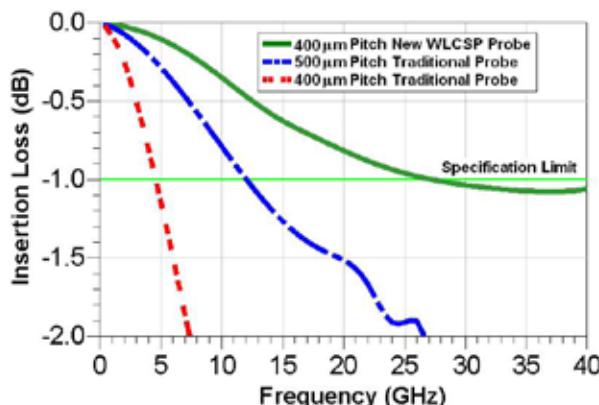
extra distance that needs to be traversed increasing the loop inductance and changing the RF bandwidth. The return loss of the probes is also dependent on the proximity to ground signals and the dielectric constant of the material between the signal and return or ground probe. Also, the longer the distance two signals are running side by side, the more crosstalk occurs. One way to reduce some of this noise is to run differential pairs so any ingress on lines can be factored out. One important factor that limits the probe length is compliance needed in probes to ensure they accurately make repeatable probe to the device under test. In large packaged devices, the variance between one side of the device and the other side might be fairly large, so more compliance may be needed. In wafer testing, the wafers are usually much flatter and the processes to fabricate them are much tighter, so compliance can be a lot less in many cases.

In **Figure 4**, the green WLCSP micro probe trace is a small wafer probe designed for high-frequency test. The other probes are a longer spring pin technology design at different pitches. The two different technology (spring pin) designs used the same spring pin. As probes get closer to each other, the S-parameters greatly change. All HFSS models used to generate the data used the same high-frequency load board material, traces and via structures for internal I/O optimized for 50 Ohms at each pitch, and a device designed for 50 Ohms with the same ball structure for each pitch. Each design was a 4x4 array and via structure for field or center connections and was optimized for 50 Ohm transitions at both load board and

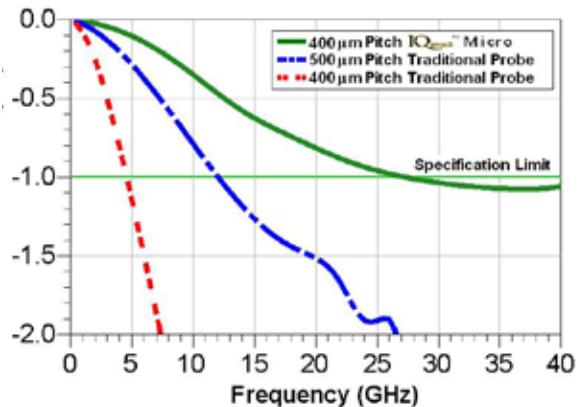
device interfaces. The light green line is the normal specification limit used by the majority of the industry that defines the bandwidth, although some competitors choose to publicize their 3dB insertion loss point, but this is half the power being lost, which is too much for many applications. From the graph, you can see that the smaller micro WLCSP probe has a bandwidth of 50% more because it is smaller by 40-50% depending on spring pin compression. Looking at the spring pin data, the smaller pitch greatly affects the performance. Going from 500 $\mu$ m pitch to 400 $\mu$ m pitch, the insertion loss bandwidth decreases by 3X. This is why it is harder to get good RF performance at smaller die pitches of 200 $\mu$ m and 300 $\mu$ m.

**Figure 5** shows the return loss data from the same three HFSS models described for **Figure 4**. Again, the smaller WLCSP micro probe has better return loss because it is smaller and better matched to 50 Ohms for 400 $\mu$ m pitch applications and has a very good -20dB return loss out to approximately 33GHz. The spring pin data, because it is taller and wider, shows degraded performance to 6GHz for 500 $\mu$ m pitch and 1.2GHz for 0.4mm pitch. The -20 dB bandwidth specification represents 1/100 of the signal being reflected back towards the source. All data was in GND-SIG-GND configuration with all adjacent probes defined as signals.

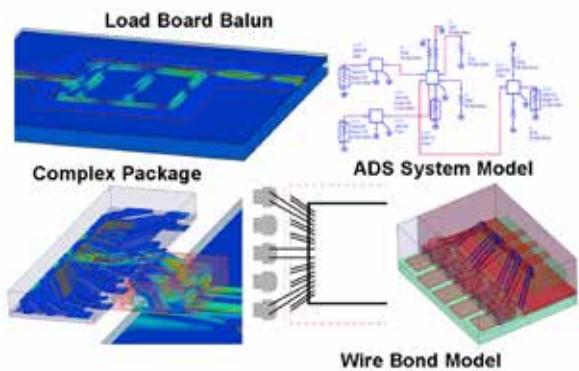
Notice that if a spring pin is specified for a -10dB return loss, its bandwidth is increased to 27.5GHz, which is close to the -20dB



**Figure 4:** Insertion loss performance vs. pitch and size of the probe contact.



**Figure 5:** Return loss performance vs. pitch and size of the probe contact.



**Figure 6:** Examples of other things in a test system that need to be included in the simulation.

specification for the WLCSP probe that has a bandwidth of 33GHz. A -10dB specification means that 1/10 of the power is reflected versus 1/100th for a -20dB return loss specification. If one of the grounds is removed from the GSG configuration, the performance will degrade even further as only one ground will be left for the return path – effectively doubling the return path inductance.

Because designs are getting more complex and are more affected by the surrounding load board or probe card and package or chip interface, it is important to model all parts of the system.

**Figure 6** shows that 3D designs, such as load board balun and package wire bonds, can be simulated in HFSS or equivalent 3D modeler and then merged into Agilent's Advanced Design Software (ADS) with other 3D simulations, or measured part performance such as a probe array to determine the overall system performance. In addition, simulation tweaks or matching can be performed

to correct or fix potential issues with the test design or even identify potential test issues such as oscillations that occur when ground inductance is insufficient to support test frequency or gain of the device.

## Summary

The RF performance of any system is dependent on a short return path. From the data presented in this article, the shorter the return path and the larger the number of close return connections can greatly affect the RF test performance. In many cases, the test data from test companies might not be the same configuration that is actually representative of the device under test. Many test companies provide the test data with grounds surrounding the RF signal providing a coax-like connection, so projected bandwidth is much higher than the actual bandwidth of the probe in the configuration being used. In most cases, modeling of the configuration being tested is the best way to get expected results. If material properties are accurate over frequency and the probe array or test fixture is simulated as built, the simulated results should be very close to the actual measured results. Many times, material suppliers don't provide the necessary electrical data needed for the materials in the fixturing or just provide it at 1 or 10MHz, which isn't accurate at higher frequencies, thereby resulting in fixture companies doing their own testing of the materials or sending them out to third party test houses.

Increasingly, devices are becoming more complicated, so better simulation is required on the whole system, from chip to tester, to determine effects of packaging, test fixture, load board layout, cable lengths to tester, etc. This article only focused on the effects of the device configuration on test probe array performance, as well as the test performance of a device in general, based on configuration. Without simulation results for the correct configuration, the impact of predicted test data based on data for the wrong device configuration can be catastrophic or result in incorrect test limits.

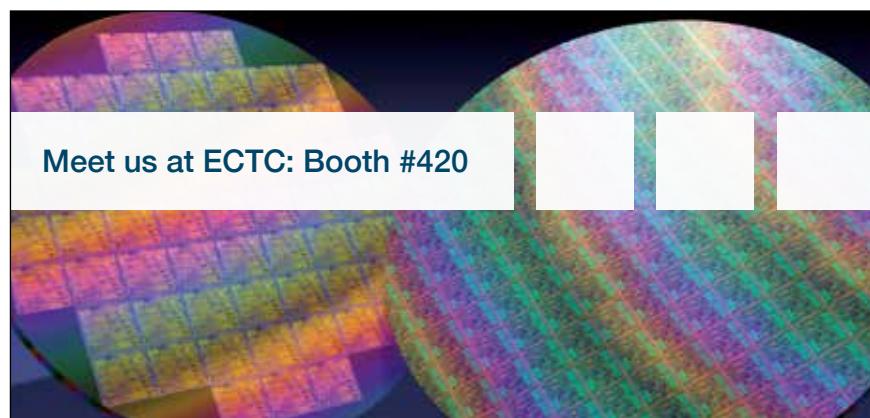
If the tools for these nonstandard simulations are not available from the test company providing the test fixture

or probe array, it could lead to delays of device to market caused by issues not associated with the chip design; issues such as the necessity to buy a different probe array, or relaying out load board or probe card, or even spending excessive time matching the device to the test environment for their device configuration. This is one reason why companies are working with test probe array or fixture companies early in the

design phase to prevent unexpected time-to-market production delays.

## Biography

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# 3D packaging for analog and power products

By Sreenivasan Koduri [[Texas Instruments](#)]

**W**hile Moore's law drove miniaturization in the silicon portion of the integrated circuit (IC) devices, there have been several parallel innovations in packaging. These innovations drove reduction of size and cost, along with increased functionality and performance. For the most part, a package was meant to provide protection to the IC die, and fanned out to interconnect from the die to the printed circuit board (PCB). Over time, that role of packaging has expanded to enable various functions and provide increased performance. Now, the package defines a large part of the devices' size, cost, reliability, as well as performance (thermal and electrical).

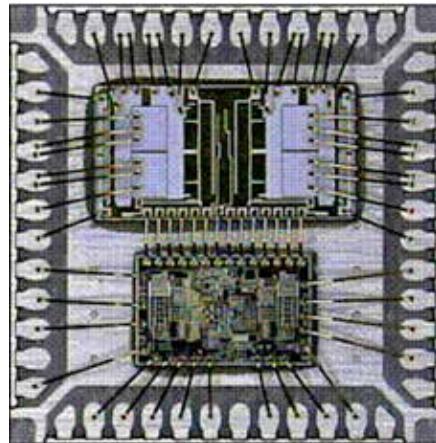
One of the trends increasing functionality is the ability to combine more than one Si die in a single package. Such multi-chip modules (MCMs) come in a large number of variations. Such combinations create several benefits. It can create subsystems with increased functionality. Sometimes it can also reduce the size and cost. Quite often, the dies combined are of different functionality, as well as of different Si nodes. Each of these nodes could be optimized for different types of circuits.

For example, it can have the digital portion of the circuits, memory, and analog portions implemented in different nodes that are best for the respective designs. With such partitions, local and global optimization can be achieved simultaneously, without having to create a super set of components in a single Si node. Creating such virtual Si nodes is a huge benefit for mixed-signal analog products. In this way, packaging serves as a mechanical interconnect and enables integration of functionality while reducing time-to-market and up front investments. From the user's point of view, such MCMs can hide the complexity with increased user friendliness.

In the early days, most of these dies

in MCMs were arranged side-by-side and interconnected through the substrate and wire bonds (**Figure 1**). Over time more creative arrangements have been developed in the industry. By combining components in the Z-dimension, some interesting 3D configurations have been created. More recently, there has been a lot of buzz about the 2.5D and 3D integrations with through-silicon vias (TSVs) and Si substrates for digital products. At the same time, the world of analog products has created a broad range of 3D packages.

Stacking multiple dies on top of each other (**Figure 2**) can help increase the



**Figure 1:** Two dies arranged side-by-side in a wire-bonded QFN package.

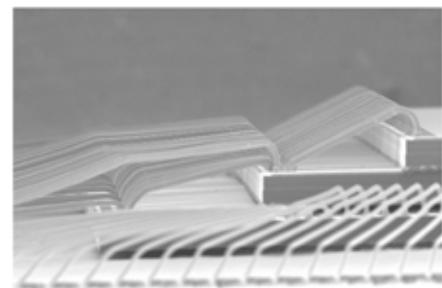
functional density quickly. In such stacking, the most common interconnect is wire bonding. There have been other interconnects such as face-to-face bonding and TSVs. In analog products, wire bond is still the dominate interconnect for single die as well as stacked die products.

Stacking dies can take on various configurations. In a pyramid or wedding cake type of configuration, the bottom die is larger than the top die. In this type of configuration, it is possible to make a direct wire bond interconnect between the dies. On the other hand, when two

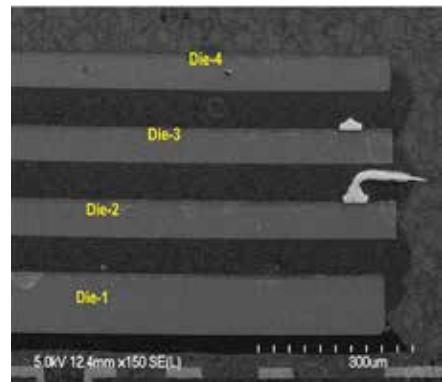
dies of the same size are stacked on top of one another, a direct interconnect becomes much more challenging. Typically, a spacer is used between the two dies.

There are some creative solutions such as wire-in-film where the adhesive material between the dies is thick and can accommodate wire bonds. With such creative ideas, stacking a large number of dies has been demonstrated successfully. Interestingly, with such stacking, it is possible for the area efficiency of the package to be more than 100%! That is, the total area of the dies can be higher than the area of the package (**Figure 3**).

Stacking in a 3D configuration is not limited to just ICs. Several integrations of the passives along with ICs have



**Figure 2:** Dies stacked on top of each other and interconnected with wire bonds.



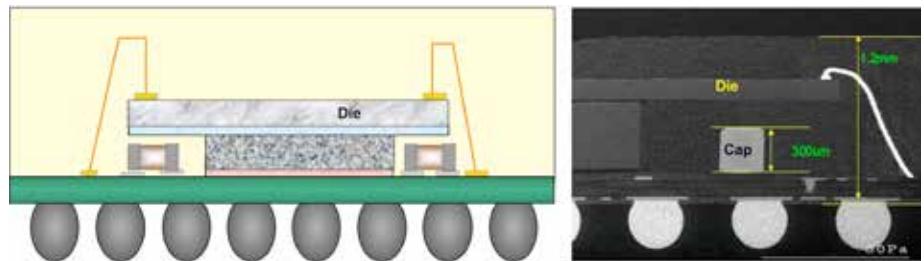
**Figure 3:** Four equal sized dies stacked and wire bonded in a wire-in-film configuration.

been demonstrated. **Figure 4** shows a case where a thin IC is overhanging on top of a discrete capacitor inside a package. The 3D arrangement in **Figure 4** is enabled to integrate a decoupling capacitor very close to the circuit. This scheme improves the device's performance significantly. Wire bonding on such a large cantilevered die without causing quality or reliability issues is a great challenge. The benefits, however, are well worth the development of 3D manufacturing technologies.

While stacked dies can increase functional density, the technology requires full pre-determination of the functions that need to be combined. Package-on-package (PoP) is a different configuration where two packages are stacked on top of each other with direct interconnections between the two packages (**Figure 5**). As shown in **Figure 6**, one or both of these packages can internally have stacked dies inside them. With such combinations, higher levels of 3D integrations are enabled. By using these PoP configurations, the top and bottom packages can have different functionality or performance to mix and match. Additionally, as the top package is directly connected to the bottom package, signals in between them do not have to go through the PCB on which this stack is assembled. This can be a big benefit when the parasitics of these interconnects is crucial. In some of the earlier analog products, large capacitors or other passive elements were stacked as the top package.

In power supply circuits, it is very common to use two field-effect transistors (FETs) to create a DC/DC converter. These FETs are switched in a controlled manner to efficiently convert the output DC voltage levels. Often, the two FETs are implemented as two discrete transistors in two different dies, and the switching circuit is implemented in a separate IC. Over time, these three dies are being combined in various fashions. One of the most efficient ways to combine these three dies is to stack the FETs and have the controller right next to the stack in the same package.

Typically, the efficiency of such voltage converters is going to depend on the  $R_{DS(on)}$  of the FETs, as well as the interconnect methods used in the package. While wire bonds provide a good amount of flexibility in interconnects, they require a large number of such bonds as the wires tend to be, relatively, of lower cross-sectional



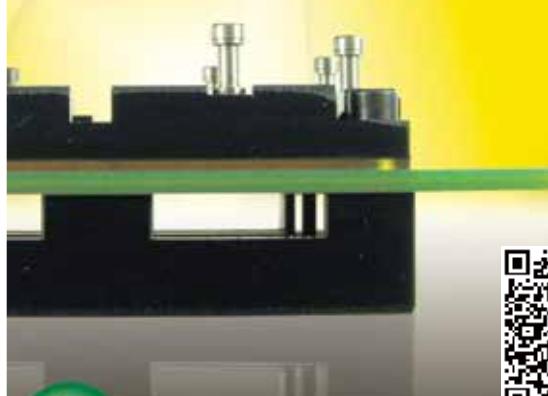
**Figure 4:** A die stacked on a spacer with a discrete capacitor under it.

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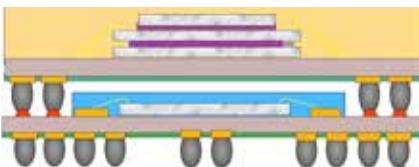
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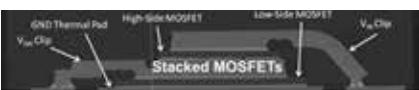
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**Figure 5:** Two BGA packages stacked as package-on-package.



**Figure 6:** A cross-sectional view of the package-on-package.

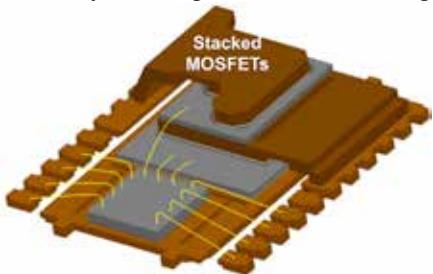


**Figure 7:** Two FETs, a lead frame, and two copper clips stacked in a 3D configuration.

area. One way to improve interconnect performance is to use Cu clips versus wire bonds.

**Figure 7** shows two FETs stacked on a lead frame with two copper clips in between the FETs. This type of stack is usually interconnected by solder in between the two FETs. In the above configuration, here is how the 3D stack is configured: lead frame + solder + FET + solder + clip + solder + FET + solder + clip. Current flows vertically through this full stack during power switching (voltage conversion).

A pair of FETs are switched by a controller (or gate driver) IC that is wire bonded to the FETs' gate pins. As shown in **Figure 8**, this controller IC can also be integrated into the package. A tightly coupled subsystem can be switched at very high speeds without exposing the package's complexity to the user. System designers can drop in this black box and expect the voltage conversions to be regulated very effectively without fully comprehending the internals. By vertically stacking and interconnecting



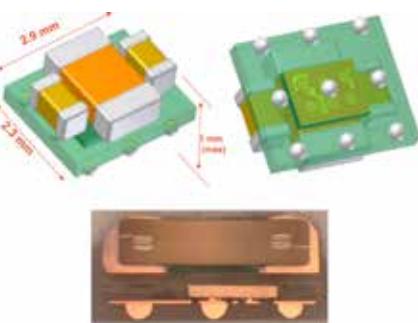
**Figure 8:** Two FETs, a lead frame, and two copper clips are stacked in a 3D configuration with a controller IC placed next to the stack inside the same package.

with clips, we get very high electrical efficiency along with good thermal performance. These heavy copper clips effectively can pull out the heat and dissipate it into the PCB. These 3D configurations are providing sufficient power densities to drive individual as well as large scale server farms.

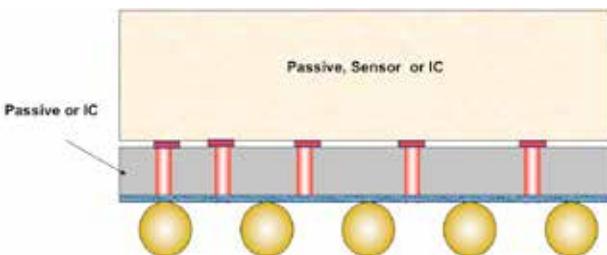
To further push the levels of integration, we have a MicroSiP™ package. In this package, along with an IC, passive components (capacitors and inductor) are combined into a single package. By doing this, the whole power supply circuit needed for a display or processor's power pin becomes a single drop-in solution.

In the MicroSiP package shown in **Figure 9**, the IC is embedded into the PCB substrate. It is invisible from the outside, while very efficiently coupled to the other components through the PCB's metal layers. With 3D stacking of ICs and passives, a range of products with various components can be mixed. The routing capability of the PCBs gives the additional flexibility.

A more subtle 3D integration is also happening at the wafer-level of processing. Some of the analog Si nodes are getting various types of bolt-on technologies added on top of the wafer. These additional wafer-level processes that happen outside the fab are commonplace with wafer chip-



**Figure 9:** A MicroSiP package with 3D integration of IC and passives.



**Figure 10:** TSV integration of two components.

scale packages (WCSPs). Similar processes are now expanding to provide a boost to the functionality that the fab is adding. These post-fab (pre-package assembly) processes can add simple things such as thick metal layers for power busing, or can create more complex structures. There have been several implementations of spiral coil inductors, and parallel plate capacitors that are layered on top of the wafer. These thin-film processes typically use polyamide-type of passivations with copper or gold-types of metal layers. By adding these on top of the wafer using a different set of materials and processes, uniquely differentiated components are generated. A high Q inductor with a very thick (10 to 20 microns) copper metal spiral can be very difficult to achieve in the fab processes. But, in a metal-top type of process, this can be more efficient. Similarly, a polyamide capacitor built up with layers of thick metals separated by the dielectric can give very high densities. Such capacitors are also used for high-voltage isolation solutions.

There is an increasing interest in adding various sensors on top of the wafer with post-fab processes. A humidity sensor, pressure sensor and magnetic flux detectors are examples of components that have been successfully demonstrated. By building these 3D structures on top of the wafer, very tight coupling of the components can be achieved with the circuit in the die. Also, by building these components across the wafer, large-scale integration is done in fewer manufacturing steps. Cost, size, and performance benefits offered by these built up layers will continue to expand the offering of this kind.

No discussion of 3D-packaging can be complete without mentioning TSVs. Even in analog products there are devices configured by integrating vertically with TSVs (**Figure 10**). While the digital products have pushed TSV

technologies to provide a large number of channels with very fine geometries, analog TSVs tend to be fewer and larger ones. A typical analog TSV can be as wide as 25 microns, 50 microns, or larger, in diameter. These copper-filled TSVs can provide

very low resistance interconnects needed for power, high Q inductors, or high-speed signals. These TSVs are combined with redistribution layers (RDLs) to add another layer of design flexibility. Such RDL layers make it easier to integrate dissimilar circuits with interconnect pads at different die locations.

## Summary

The examples provided give a glimpse into the wide range of 3D integrations happening in the analog and power semiconductor products. By no means are these a complete collection of 3D configurations. In analog and mixed-signal products, there have been a range of similar ideas that integrate ICs and passives as well as sensors. With ever-shrinking electronic gadgets, and the customer's demand for higher functional density, there is going to be an increasing trend to look at the Z-axis. With 3D integration, benefits are going to be multi-fold. Of course, such integrations are not simple. They bring a variety of challenges and new failure modes, which were not highlighted in this article. While some of these challenges are obvious from the constructions shown, there are a lot of things that are more subtle and difficult to address. However, the added benefits of 3D integrations can outweigh the challenges in a good number of cases. We will continue to see a lot more creative ideas and products in the future.

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# Met-Via TSV interposer as a TMV element of CMOS biosensors

By Thorbjörn Ebefors, Jessica Fredlund [*Silex Microsystems AB*] and Erik Jung, Tanja Braun [*Fraunhofer IZM*]

**A**n aging society and the raising of health standards in the more developed countries has caused healthcare costs per capita to increase much more rapidly than the gross domestic product (GDP) per capita. Presently, there is a clear driver toward prevention to reduce healthcare costs and to increase the quality of life. This philosophy demands technologies with functionalities beyond traditional diagnostic methodologies, namely on-the-spot or point-of-care (PoC) diagnostics instead of analysis in a centralized lab. In the CAJAL4EU consortium under the European ENIAC Joint undertaking initiative, the objective was to bridge this gap by novel and advanced technologies. The project, which was coordinated by NXP, Belgium, aimed at developing microelectronic-based diagnostic biosensor platforms, and enabling in vitro diagnostics for a variety of new multi-parameter test applications in a robust, user-friendly and cost-effective way. The technology is based on nanoelectronic modules, where microelectronic-based diagnostic detection platforms increase sensitivity, specificity and multiplex capability in human body fluid diagnostics. This technology enables prototype experiments that can be performed at the bedside, in the clinic, in an ambulance, in emergency rooms, or at home, depending on the particular diagnostic question [1].

The biosensors used in this evaluation consisted of a nanoelectronic-based CMOS transducer with an interface chemistry that makes the connection to the clinical sample to be analyzed. Subsequently, capturing of bio-targets can be detected by measuring capacitive/impedance changes in the electrical signal. With on-chip detection electronics, small electrical changes can be detected within milliseconds, enabling massively parallel real-time monitoring of bio-molecule binding events. Besides the transducers, interface chemistry and spotting technologies, microfluidics, software and hardware developments

(and their integration) have been developed by other CAJAL4EU partners to realize fully integrated biosensor systems and lab-on-chip devices. The detection principle for the biosensors is electrical detection (CMOS-based) by use of capacitive/impedance or electrochemical sensing strategies. These methods exhibit a high potential toward rapid, highly sensitive multiplexed detection of biomolecules, preferably label-free [2].

The focus for Silex Microsystems and Fraunhofer IZM within this CAJAL4EU project had been to develop an heterogeneous integration packaging technique between the active biosensor and the electrical connections. The metallized through-silicon via (TSV) interposer will establish the electrical connection between the microfluidics and the control unit. Because of the hermetic seal of the vias, a well-defined separation of the microfluidic from the electrical connection is realized. For this approach, dies with TSVs manufactured by Silex [3] were assembled at Fraunhofer IZM, together with the active biosensor. After compression molding, only the active biosensor and one side of the TSV dies are accessible for thin-film interconnection. Therefore, the redistribution of the over molded backside of the reconfigured wafer will be realized by using PCB-based redistribution technologies.

Future demands for ever smaller size and lower cost will inevitably lead to requirements on totally integrated sensor solutions that are much smaller than today's available technology. Heterogeneous integration will have a number of benefits, including less use of expensive Si material, yield improvements, and also the ability to integrate silicon dies fabricated in different technologies/fabs on different wafer dimensions. These benefits will contribute to a low cost end product. Vertical chip stacking, often used in heterogeneous integration, is realized by the metallized TSVs and is one alternative for decreasing the packaging

size and the costs, because the volume and weight of the package are reduced. The TSVs enable shorter redistribution layers (RDL), and the smaller size means better performance because the signal travels a shorter route and parasitic capacitances decrease (which also impacts system performance). Furthermore, the overall size and power consumption of the device are decreased [4]. Additional benefits from using metallized TSVs in Si-substrates are that high RF performance and improved signal integrity can be obtained. We have previously done work using metallized 50-90 $\mu$ m diameter rigid TSVs; the results showed high RF performance where the loss of a single coplanar TSV transition was less than 0.04dB at 5GHz. This loss is considered to be very small [5]. These miniaturized rigid TSV interposers with 50 $\mu$ m diameter vias allow for I/O densities above 35 I/Os per mm<sup>2</sup>.

The heterogeneous integration of the TSV interposer and the biosensor is achieved by reconfiguration wafer molding. There are two main approaches for embedded die technologies: wafer-level integration, where dies are embedded into polymer encapsulants, and 3D vertical integration, where dies are stacked on top of the substrate.

For wafer-level integration there are many technology options being pursued worldwide. The main drivers are the embedded wafer-level ball grid array (eWLB) by Infineon [6] and the redistributed chip package (RCP) by Freescale [7]. Amkor has focused on through-mold via (TMV) package-on-package (PoP) as the industry standard and achieved a via pitch of 400 $\mu$ m [8]. Singulated dies are assembled on an intermediate carrier and encapsulated by compression molding, forming a polymer wafer with embedded silicon dies. This "reconfigured" wafer is then released from the carrier. Using thin-film technology, an electrical redistribution layer is routed on the wafer. Finally, the wafer is singulated by sawing into single packages containing multiple embedded silicon dies. One trend in this

fan-out wafer level packaging (FOWLP) technology is at the moment a double-sided packaging with integration of vias through the encapsulants allowing electrical routing to the backside of the package [9].

Another concept for 3D integration of active components is the chip-in-polymer (CiP) technology, introduced by Fraunhofer IZM, TU Berlin and Wuerth [10]. It is based on embedding of ultra-thin dies into build-up layers of printed circuit boards (PCBs). The dies are bonded onto a core substrate using an adhesive; a resin coated copper (RCC) layer with thin Cu is used for the subsequent lamination. Interconnects are established by laser-drilled microvias ( $\mu$ -via) followed by a PCB-compatible Cu plating [10]. The combination of both concepts, embedding into polymer by molding and redistribution by PCB technologies, has the potential for highly integrated low cost packages [11, 12].

### Technical description

The following is a description of the metallized TSVs' fabrication process and the fan-out wafer-level packaging (FOWLP) technology used to combine and integrate the biosensor with the metallized TSVs.

**Manufacturing of biosensors.** The CMOS biosensor chip was designed by NXP Semiconductors in Belgium and the measurement principle is based on capacitive/impedance detection using metallic nanoelectrodes [13]. The biosensors were fabricated using a commercially available CMOS foundry process (at TSMC) on 300mm silicon substrates. Prior to CiP package processing, the CMOS biosensor wafers were thinned down to a 300 $\mu$ m thickness and singulated into dies by NXP Semiconductors, Germany.

**Manufacturing of the metallized through-silicon via interposer.** The metallized TSV is going to form the electrical connection between the microfluidics and the control unit located on different sides of the  $\mu$ -fluidic package. It is important that the metallized TSVs meet the requirements, such as low via resistance (<20m $\Omega$ ), low losses, and high yield (>90%) in order to meet performance and cost requirements of the end product. To minimize and reduce the risks of losses, the silicon substrate used was a 200mm diameter, 305 $\mu$ m thick silicon wafer (3-10k $\Omega$ -cm) from Okmetic, Finland. The use of rigid interposers (300-430 $\mu$ m thick) will eliminate the ultrathin wafer

handling requirements, such as bonding, debonding, and carrier handling steps [14].

The TSVs were designed to have 200 $\mu$ m diameter via holes (BS) with a 280  $\pm$  10 $\mu$ m depth, giving the aspect ratio (AR) of 1.5:1. The decision was made that there was no need to use smaller vias, with 50-90 $\mu$ m in diameter and with a pitch of 150 $\mu$ m, giving ~16-32 vias/mm<sup>2</sup>, which is available at Silex, because

the landing pads for the  $\mu$ -vias has to be as large as 100x100 $\mu$ m, due to potential die shift while assembling. Also, larger vias will ease the molding process and a higher yield is generally achieved, along with a lower cost-of-ownership.

The goal while deep reactive ion etching (DRIE) the BS via is to achieve vias with a straight or even a re-entrant wall profile to decrease the shadowing effect during the deposition of a

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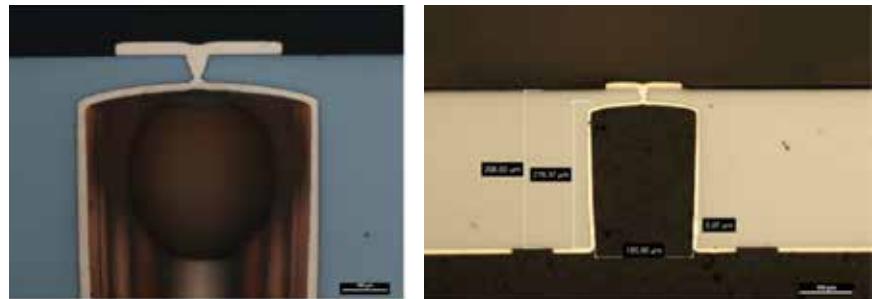
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conformal seed layer. To be able to close the via and create hermetically sealed vias, a tapered structure should meet the BS via from the front side (FS), with dimensions of  $25 \pm 10\mu\text{m}$  deep, surface opening  $25 \pm 5\mu\text{m}$  and bottom  $8 \pm 3\mu\text{m}$ . The X-shaped profile is also desired because it locks the structure and eases the complete void-free Cu filling of the FS via. The FS via requires two DRIE steps, where anisotropic and isotropic etches have been used. All the DRIE steps were done using Bosch-processes in a SPTS Pegasus or DS1 chamber. The chambers have different optimized etching parameters in order to obtain the desired profiles.

To obtain high-performance TSVs, an insulation layer is deposited after the DRIE etching; the layer comprises  $0.5\mu\text{m}$  thermal oxide and a  $0.12\mu\text{m}$  low pressure chemical vapor deposition (LPCVD) nitride. Before metallization could start, a  $0.5\mu\text{m}$  TiW adhesion/barrier layer was deposited with an Oerlikon/Unaxis LLS sputtering tool able to handle wafers with open through-holes, as well as a conductive  $0.5\mu\text{m}$  Cu seed layer on both sides of the wafers. That deposition gives enough seed layer coverage deep inside the via holes.

Early metallizing experiments were carried out on modified RENA and SemiTool Cu plating systems available at Silex's 8" MEMS foundry line. The Cu plating results, however, were not satisfying; instead, nonconformal plating was obtained, with voids present in the FS via. A specially designed plating tool, enabling cost effective simultaneous double-sided plating of the TSVs, was therefore set up. It was discovered that a double-sided plating was preferred because it minimized the risk of getting trapped air bubbles at the bottom of the BS via (where BS via meets FS via), due to the fact that the plating solution could flow through the via, until the FS hole is completely closed. The plating solution that was used was a Cu-line fill chemistry provided by DOW and Enthon. By proper mixing of the additives, a conformal film along the BS via and a void-free hermetic sealing of the small FS via hole were obtained. A line fill Cu-plating process is desired because Cu and Si have different coefficients of thermal expansion (CTE) and



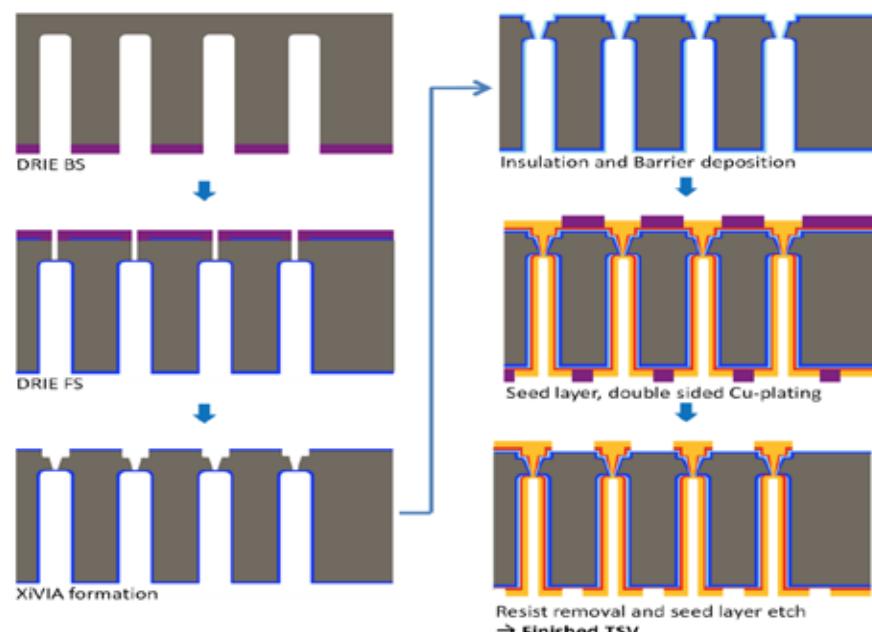
**Figure 1:** A cross section of the finished metallized TSVs. a) The left view shows a non-vacuum molded cross section where a void is obtained, while b) the right view shows a vacuum molded cross section.

also to limit the time-consuming Cu-plating. The plating time used to obtain controlled sealing and hermetically tight TSVs with the XiVIA™ feature is between 30-50 minutes. This plating time is a  $>20$ x reduction of the plating time used by Chen, et al. [15] for other similar TSV structures ( $300\mu\text{m}$  thick TSVs).

A thick dry-film resist ( $15\mu\text{m}$ ) was used as a plating mask for the interposer redistribution layers (RDLs), creating line dimensions with the smallest line/spacing of  $40\mu\text{m}$ . For integration purposes, in the subsequent processing of  $\mu$ -vias (see section "Manufacturing demonstration") the Cu layer must have a thickness in the range of  $15-20\mu\text{m}$  to allow laser drilled  $\mu$ -vias through the overmolded backside of the interposer dies. Also, a thick Cu film will provide a low resistivity and good signal properties.

The yield of conformal plated vias was further increased by optimizing the pre-wetting steps, thereby facilitating the wetting during plating. Also, the re-entrant wall profile of the BS and FS via will ease the wetting of the vias. Introduction of a quick Cu-etch step was necessary in order to remove copper oxide that may have formed, which would decrease the adhesion of the electroplated Cu. Evaluation of the plated vias was made by scanning electron microscopy (SEM), however the Cu is soft and is easily smeared during cross section preparation using dicing.

Because of the Cu smearing while dicing, a molded cross section was prepared by FhG-IZM on a small sample size. Analysis of the sample showed a void-free Cu-filling of the FS via as well as a conformal Cu film along the BS walls. It was stated, in order to



**Figure 2:** Established process flow of the metallized TSV at Silex.

obtain a void-free mold filling, vacuum molding was necessary (**Figure 1**). This knowledge was then an important input for the full wafer molding using multiple dies for fabrication of reconfigured wafers; see the section “Manufacturing demonstration” below.

The final step in manufacturing the metallized TSVs is to remove the conductive seed layer and the barrier layer to isolate the vias and create separated 3D connections between the BS and FS. This is preferably done by wet single- or double-sided etching. The established process flow is presented in **Figure 2**.

### TSV interposer layout

The interposer consists of 21 Met-Via® 200 TSVs with a staggered 500 $\mu\text{m}$  pitch layout. On the back side (large via hole side) each via is routed to a 300x300 $\mu\text{m}^2$  pad ( $\mu$ -via landing pad for the later polymer wafer fabrication) along the die edge for easy fan-out, and on the front side (small via hole side) each via is routed to a 200x200 $\mu\text{m}^2$  pad

( $\mu$ -via landing pad). The use of these large  $\mu$ -via landing pads was designed in order to have misalignment margins for the IZM laser drilling process. These large landing pads, however, could be reduced drastically in production environment processing, thereby allowing for higher TSV densities. Further, the relatively large pads also allow for certain die shifting during the epoxy molding because the pads are fully covered with molding compound and alignment can only be done by laser drilled vias from wafer front to backside used as fiducials. The routing on the back side is done with 100/75 $\mu\text{m}$  lines/spaces while the front side uses 55/65 $\mu\text{m}$  lines/spaces. The metallization for each via extends to a 75 $\mu\text{m}$  wide collar outside the via hole on the backside.

The resistance of the metallized TSVs was monitored by connecting the vias in a daisy chain where a series of 2-18 vias in an increment of two could be measured using low ohmic four-terminal measurements.

### Fan-out wafer-level packaging

The general process flow for the FOWLP approach with the metallized TSV interposers, the CMOS biosensor chip die, and PCB-based redistribution starts with the lamination of an adhesive film to a carrier. This special adhesive film has one pressure adhesive side and one thermo-release side, i.e., by heating up the tape above a certain temperature, the thermo-release side of the tape loses its adhesion strength. On this carrier-adhesive film, dies (the interposer TSV dies and the biosensor) are precisely placed, with the active side facing down toward the intermediate carrier. High accuracy is needed as die pads have to match with the redistribution layer. Molding is done by large area compression molding. For chip redistribution, low cost PCB-based technology with RCC has been selected. After lamination of the RCC film on both molded wafer sides in one step,  $\mu$ -vias are drilled to the die pads on both sides of the wafer. The next process steps are cleaning, palladium



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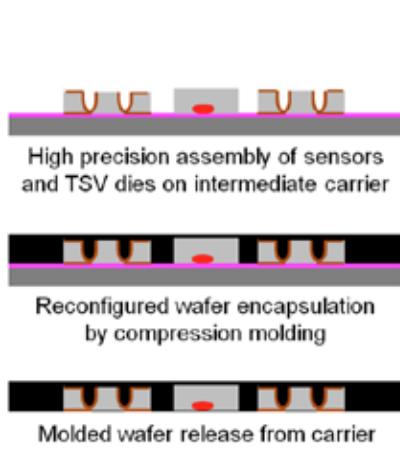
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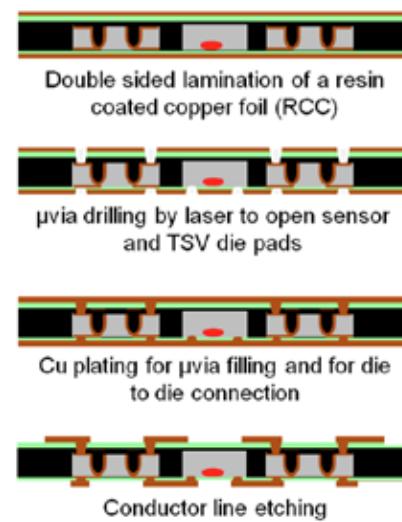


**Figure 3:** Process flow FOWLP with Met-Via TSV interposer dies for 3D electrical routing.

activation and copper plating. The die pad connection to the copper layers is achieved by using plating. Conductor line formation is accomplished by laser direct imaging (LDI) in combination with a dry film resist and copper etching. The process steps described above are summarized in **Figure 3**.

### Manufacturing demonstration

The general process flow described above was used for the fabrication of the CAJAL4EU biosensor package with electrical 3D routing obtained using silicon TSV interposers. Before die placement, a thermo-release film was laminated on a carrier. The release film was selected according to the required compression molding compound and the related molding temperature. A high-speed chip assembly machine, Siplace CA3, was used for chip assembly with an accuracy of  $\pm 15\mu\text{m}$ . Compression molding was done on a compression mold machine 120 t press from TOWA. For compression molding, a liquid epoxy molding compound was selected with fine filler particles to allow the void-free filling of the



**Figure 4:** Cross section of a part of the  $5 \times 3.5\text{mm}^2$  TSV interposer die embedded in a mold compound without any air entrapments present in the TSVs after the compression molding step, but before the  $\mu$ -via drilling and fan-out process steps.

compensation. The last process step was module singulation by dicing. **Figure 5** shows a singulated module from the top and bottom sides.

Furthermore, 2D X-ray and X-ray CT analyses were performed to analyze and show interconnection integrity as well as 3D electrical routing from the sensor's top side to the electrical connection on the bottom side. The x-ray CT image in **Figure 6** nicely demonstrates the 3D routing in the module.

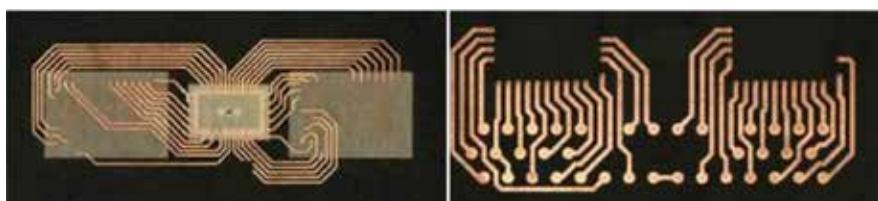
The 2D X-ray image of the TSV die shown in **Figure 7** demonstrates the three levels of 3D interconnections:  $\mu$ -vias for connection of the top side of the TSV die, TSVs through the silicon and  $\mu$ -vias for TSV backside connection through the molding compound.

Cross sections were also prepared to further analyze the 3D interconnection quality. **Figure 8** shows a detailed image of the cross section with the TSV die interconnection. The  $\mu$ -via connection through the molding compound for backside interconnections, as well as the  $\mu$ -vias to the top side, are well aligned to the die pads and show void-free metal connection to the die pads. The backside  $\mu$ -via diameter is  $100\mu\text{m}$  giving an aspect ratio of 1:1.

### Characterization

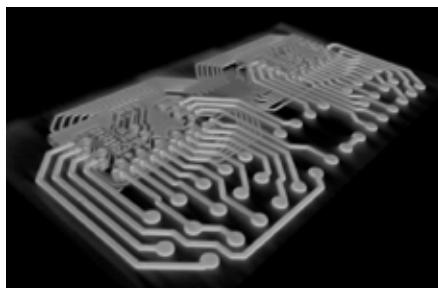
The following sections discuss electrical TSV measurement results and electrical measurements on singulated modules.

**Electrical TSV measurements.** As mentioned previously, a high yield is necessary in order to make a low cost product, therefore DC electrical measurements were conducted before sending the finished metallized TSV dies to Fraunhofer for molding. The via resistance was measured with an Agilent 34401A 6½ digit multimeter and a Karl SUSS PM5 single-side wafer probe station, using a low ohmic four-terminal, where PCM die with via daisy chains were characterized. During the electrical characterization,

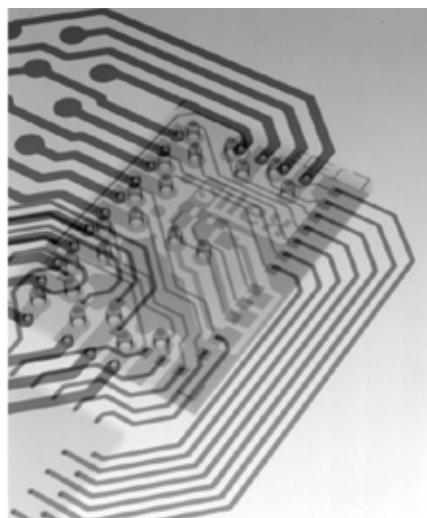


**Figure 5:** Top-view photo of a singular module after the fan-out process steps with 40 I/Os from the CMOS die to two TSV dies with 21 TSVs/die; a) (left) top side to microfluidic, b) (right) bottom side for electrical connection.

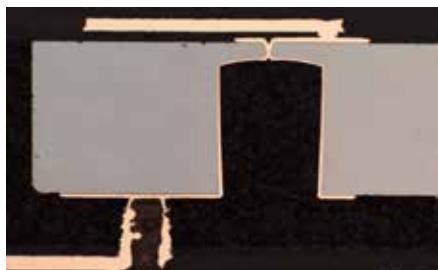
42 different PCM dies from 7 different 200mm Si-wafers were measured (6 PCM die from each Si-wafer). On each PCM die, 16 TSVs were characterized, which made a total of 672 TSVs. Only 3 out of the 672 TSVs showed short circuit or interruption, giving a yield of about 99.6 %. The same yield is expected for the sharp metallized TSV interposer dies. These interposers are therefore usable when embedded in the reconfigured polymer wafers allowing



**Figure 6:** X-ray CT image of a full module.



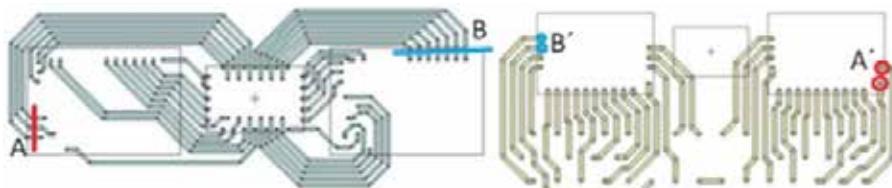
**Figure 7:** X-ray image of a connected TSV die.



**Figure 8:** Cross section through the TSV die with all levels of 3D interconnects (RDLs both on silicon and polymer levels). The depth of the  $\mu$ -via through backside over mold is approximately 100 $\mu$ m. The silicon thickness is 305 $\mu$ m and TSV diameter is 200 $\mu$ m.

high packaging yield. Using a double-sided wafer prober, a selection of only good TSV interposer dies could be accomplished, which would increase the overall packaging yield even further. That's the main advantage with the heterogeneous assembly approach—it allows for selection of only known good dies to be packaged and allows for a wider selection of choices of CMOS processes for the biosensors than if the TSVs had been integrated directly into the CMOS dies. The metallized TSVs were low ohmic with a resistance of  $11.2 \pm 4.2 \text{ m}\Omega/\text{TSV}$  ( $1-\sigma$ ).

#### Electrical measurements on



**Figure 9:** CAD layout of the fan-out layer on the singulated module; a) (left) Image illustrating the top side fan-out layer where the A and B lines indicate where the fan-out redistribution layer was shortened; and b) (right) Image showing the bottom side routing and the A' and B' rings indicate the location of the probe needles.

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Preliminary electrical results indicated a resistance of  $\sim 1\text{-}3\Omega$ , between the  $\mu$ -vias on the bottom side through the TSV die ( $\mu$ -vias landing pads and through the TSV) to the  $\mu$ -via on the top side and back again.

### Summary

The metallized TSV interposer was successfully manufactured and PCM test structures were electrically characterized, showing a mean resistance of  $11.2\text{m}\Omega/\text{Via}$  (with a  $\sigma$  of 4.2) and a yield of 99.6%. The TSV interposer die was assembled together with the NXP biosensor die, where the vacuum-assisted compression molding of a liquid epoxy molding compound with fine filler particles realized void-free filling of the TSV interposer die structure. Connections between the  $\mu$ -via landing pads on the TSV interposer die and the fan-out redistribution layer were realized by laser drilling  $\mu$ -vias and Cu-plating, after which, optical measurements of the potential die shift during the die assembly. The finished demonstrator module was optically inspected by X-ray CT, X-ray and SEM—all showing working connections. A preliminary electrical measurement also indicated that connections between the molded components with a resistance of  $\sim 1\text{-}3\Omega$  is possible to obtain.

The field of advanced package development, in recent years, has concentrated on heterogeneous IC packaging as a way of meeting the integration challenges of disparate technologies while simultaneously answering the needs of the market for smaller footprint and thinner packages that can deliver improvements in performance, size, and cost. Whether this has taken the form of 3D die stacking, 2.5D interposer technologies, functionally integrated LTCC substrates, package-on-package combinations, or (as in this paper), WL reconstruction of silicon dies embedded in polymer, all of these approaches aim to hit market points of size and performance at critical price points.

The development of commercially viable via alternatives has been a critical milestone in all of these packaging approaches. MEMS foundries such as Silex, whose base technology involves deep etching and filling of materials for novel micro machined structures, has found its capabilities leveraged into the packaging space – something Yole Développement coined in 2010 as the “emergence of the mid-end foundry” [16].

The dual combination of wafer-level reconstruction (WLR) and TMV, then, represents a way to circumvent the substantial engineering challenges of other, more direct, 3D IC approaches, and

offers an approach that can be immediately employed to advanced IC packaging without substantial R&D or time-to-market penalties.

It is foreseen that the use of FOWLP technology will increase in order to meet the increased packaging needs for rapid growth in smartphone shipments [17]. For FOWLP, future research will deal with up scaling of the processes presented to a larger scale moving from wafer-scale to panel-scale (fan-out panel-level packaging, or FOPLP) for economic reasons, where the major challenges are placement accuracy on large area, low cost encapsulation over a large area, and warpage control [18].

### Acknowledgments

The authors would like to acknowledge the support of the European Union [ENIAC JU 120215 Grant]. National Swedish funding is provided in part by VINNOVA, the Swedish Governmental Agency for Innovation Systems; and National German funding was provided by the German ministry for education and research [BMBF, SV16N10925] in the ENIAC CAJAL4EU Project.

Lucas Held at Silex is greatly acknowledged for design of the TSV interposer, the wafer-level interconnect design, and CAD support. Our thanks also go to the fab personnel at the Silex 8" fab for assisting with processing the TSV interposer wafers. Additionally, the authors want to thank Steve Voges, Tina Thomas, Ruben Kahle and Volker Bader at FhG for technical support.

Guido Albermann and Sven Reggelin at NXP, Hamburg-Germany, are greatly acknowledged for making biosensor dies from 12" CMOS wafers available for these packaging experiments.

The X-shaped locking TSV structure technology is licensed by Silex from ÅAC Microtec, Sweden. The XiViATM trademark is owned by ÅAC. Met-Via® is a registered trademark owned by Silex Microsystems AB.

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### Biographies

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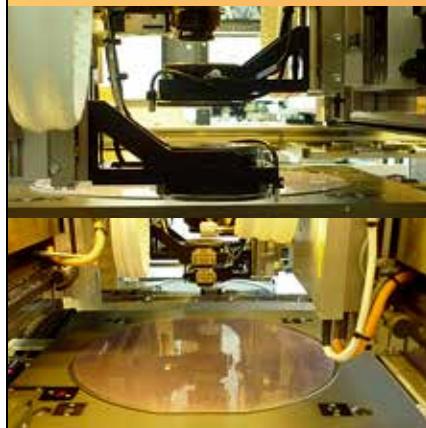
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# PROFILE



**Isabelle Guillaume**

Isabelle Guillaume has an engineering background (Telecommunication Engineer) as well as an MBA from Grenoble U. (IAE). Her career was spent with Schneider Electric, which provided a diverse business environment and enabled her to hold positions that included both marketing and general management. Her responsibilities included product marketing, project management, strategy and general management. She was also CEO of Easyplug, a technology start-up founded by Schneider and Thomson in 2000. During the last 5 years at Schneider, she was with the IT Business of Schneider Electric, in charge of the 3 Phase UPS Offer Management globally. She joined Minalogic in November 2013 as Chief Representative.

## Minalogic Backgrounder

Created in 2005, the Minalogic global competitive cluster in Grenoble brings together the Rhône-Alpes region's leading innovators in the field of smart miniaturized systems. By leveraging the Grenoble area's synergies between research, higher education and industry, it has achieved a global leadership position in smart embedded systems.

The foundation for Minalogic began in 1992, when STMicroelectronics, Léti-CEA and France Telecom R&D joined forces to ramp up research in submicronic technologies, with STMicroelectronics handling production. The microelectronics sector in the Grenoble area is extremely dynamic, as evidenced by the notable technological advances that local businesses and

## Minalogic cluster leads global competitive research and innovation in intelligent miniaturized products and solutions for industry

*Chip Scale Review staff surveys Minalogic with Isabelle Guillaume, Chief Representative of Minalogic*



**Minatec Campus** (upper left corner); **STMicroelectronics site in Crolles** (upper right corner); **clean room** (lower right corner); and **Soitec headquarters in Bernin** (lower left corner).

research labs have achieved. In the field of circuit miniaturization, Soitec, set the goal of achieving  $0.17\mu\text{m}$  etching on 300mm wafers and making energy-efficient components. Leti also has made advances in fluorescent micropoint screens. Local component manufacturers contributed additional expertise to the industry and provided key support for the technological advances made in and around Grenoble.

Additional expansion occurred in 2002, when Freescale Semiconductor (Motorola) linked up with the R&D division of NXP Semiconductors (Philips) and STMicroelectronics. The resulting joint facility, CrollesII, garnered investments of €2.8 billion—the largest industrial investment project in France in more than a decade.

Created at the initiative of CEA-Leti and Grenoble Institute of Technology, the Minatec center for innovation in micro- and nano-technologies is at the top of its field in Europe. The Grenoble area is one of the few places in the world that possesses the scientific, technological, and industrial resources required to achieve this level of recognition.

As a founder and partner of Silicon Europe, Minalogic is positioned as a global leader in intelligent miniaturized solutions—a unique hybrid of microelectronics, nanoelectronics and software that spans the range from fundamental research to technology transfer.

The technologies developed at the cluster are applicable to all business sectors, including more traditional



Public R&D laboratories at Minalogic for research and education at Grenoble facility.

industries. The aim of Minalogic is also to create a global business ecosystem in the field of smart miniaturized solutions based on leadership in research and innovation and on the leading role of major groups supporting the growth of SME.

Minalogic brings together major corporations, small and mid-sized businesses, government agencies, and organizations from the public and private sectors. The cluster's focus on innovation and its participatory governance model are designed with one objective in mind: to ensure efficient, results-oriented cooperation among cluster partners.

The cluster facilitates networking among innovators, manufacturers and investors to get new technologies to market quickly. Its public/private partnerships are dedicated to creating value for member companies through integration of hardware and software – a challenge facing many modern electronic systems that requires creative, interdisciplinary collaboration.

By supporting partnerships among universities, research centers and companies, Minalogic responds to the global high-tech community's need to identify new value-added technologies that can be integrated into existing products in healthcare, the environment, mobility, the media, the textile industry and other areas.

## Projects

The partnership's projects demonstrate a broad range of innovative linkage of software and hardware for current and future markets in five target markets: energy efficiency; connectivity and mobility; biology and healthcare; traditional industries; and imaging. Four of these projects are as follows:

### ■ Connectivity and mobility:

- Example: Delpix  
The Delpix project has enabled the creation of a full X-ray rapid-tomography system for quality inspection on the production line, overcoming the cost and quality issues that have long been barriers to using this modality in manufacturing. Partners in the project include Thales and Trixell (major companies), CyXplus, Digisens and Noesis (SMEs), and INP Grenoble and INSA Lyon (academy).

### • Example: EnergeTIC

The recently completed EnergeTIC project, certified by Minalogic, has developed technologies to optimize the efficiency of power-hungry data centers. The project has been implemented in two data centers: Bull's experimental Data Center, and the Eolas Green Data Center in Grenoble. The tests showed a 30 to 57% reduction in the data center's power consumption.

EnergeTIC brought together seven partners: Bull, Business & Decision Eolas, Schneider Electric, UXP, the Grenoble-based G2Elab, G-SCOP and the Joseph Fourier University/LIG.

### ■ Biology and healthcare:

- Example: FluMin3  
The FluMin3 project is developing a new generation of MEMS-based injection devices for single-dose medication that automatically adapts to intradermal, subcutaneous or intramuscular injection.

### ■ Traditional industries:

- Example: Printronics  
Printronics partners have developed technologies for printed electronics on flexible substrates using new polymer materials with conductor and semiconductor properties. These

technologies enable creation of intelligent and flexible products and open a large field of applications, including fitness, medicine, construction and sensors. The startup ISORG was launched by this project.

## Membership

Minalogic has more than 230 members, including:

- 189 companies (86% SMEs)
- 12 research centers and universities
- 15 local governments
- 13 economic development organizations
- 2 private investors

International companies that have an R&D presence in France can join Minalogic, which helps prospective members get established in France. The cluster's management is responsible for evaluating, accepting and guiding project proposals, and for securing financing for them from any of several government economic-development bodies. Since its launch, Minalogic has secured more than €726 million in financing for 259 research projects, whose total budgets are €1.9 billion.

The cluster also helps members secure financing to commercialize market-ready technologies at the completion of projects.

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# Optical technologies for TSV inspection

By Arun A. Aiyer [Frontier Semiconductor]

In the realm of 2.5D/3D packaging, a high-throughput, production-ready metrology tool with a single high-performance sensor that addresses multiple measurement needs throughout the process flow, i.e., from front-end-of-line (FEOL) to back-end-of-line (BEOL), can be very valuable in terms of yield improvement, cost-of-ownership reduction, and tools utilization. A metrology tool based on Virtual Interface Technology (VIT<sup>TM</sup>) has demonstrated its ability to be useful in the front end where the measurement features are only a few microns thick or deep, and in the back end where the measurement range spans from a few microns to several millimeters. This technology, therefore, provides tool-to-tool compatibility at different measurement points along a process line. Additionally, lattice stress in the vicinity of filled TSVs needs to be monitored and measured to avoid having active devices patterned in the keep-out-zone. A high-resolution  $\mu$ Raman capable of stress resolution at  $\sim 20$ MPa can monitor these stress zones.

## Measuring thickness

VIT<sup>TM</sup> is a Fourier domain technique that utilizes temporal phase shear of the measurement beam for thickness measurement of thick substrates. The sensor configuration enables creation of non-physical interfaces that enhance a tool's measurement capabilities in terms of measurement range, accuracy and repeatability. One example of how this technology is used in thick substrate measurement is demonstrated with the help of Figures 1-3. Sample illumination can be either from the front side or back side of the sample.

An examination of signal amplitudes in Figures 2 and 3 immediately reveals the effectiveness of the technology in

thickness measurement. When the technology is enabled, the signal pairs used in determining wafer thickness and thickness under the TSV are 5x or more stronger than the signal amplitudes without it. Stronger signals improve measurement accuracy and repeatability. Thickness of a 300mm wafer mapped using this approach is shown in Figure 4. The  $1\sigma$  standard deviation achieved by this technique is given in In Table 1. It is  $< 2$ nm, while the nominal  $1\sigma$  w/o VIT<sup>TM</sup> is  $\geq 100$ nm.

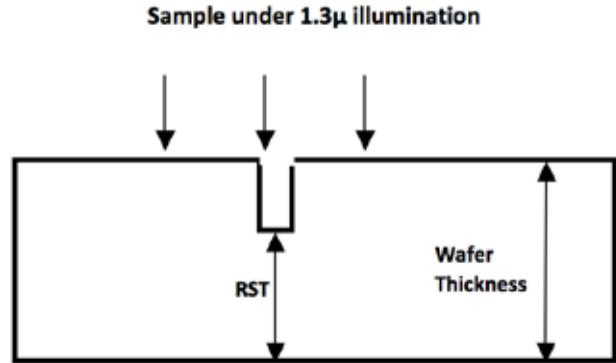


Figure 1: Schematic of TSV sample under illumination.

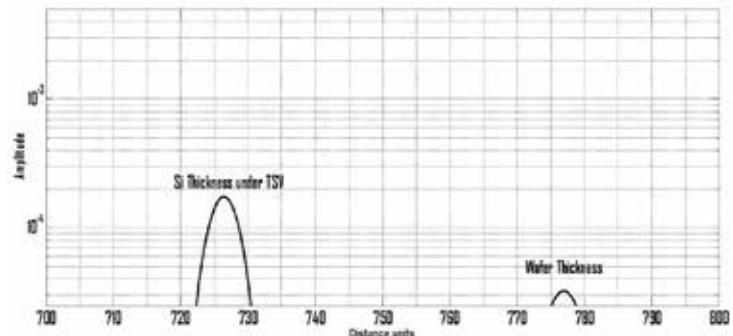


Figure 2: Thickness spectrum without enabling VIT<sup>TM</sup>.

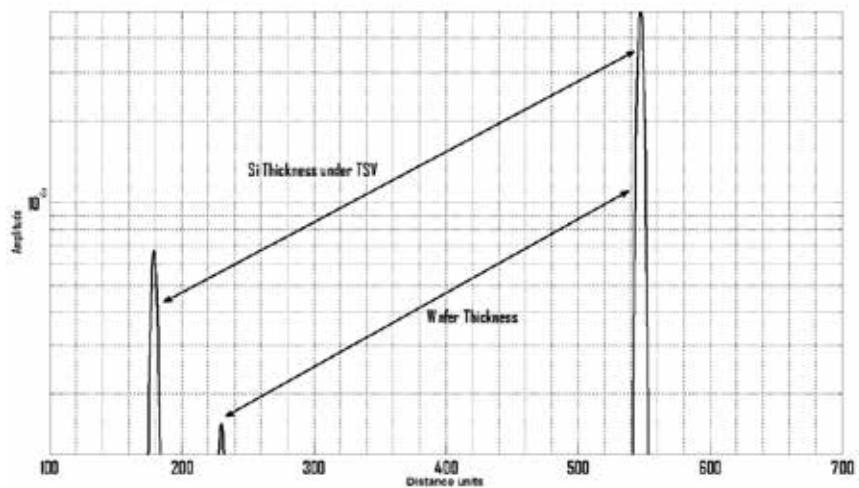
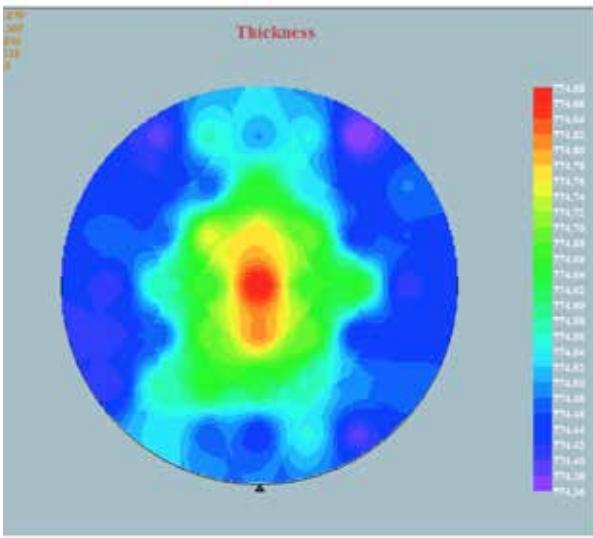


Figure 3: Thickness spectrum with VIT<sup>TM</sup> enabled.



**Figure 4:** Thickness map of a 300mm wafer (TTV 0.515μm).

Repeats	Wafer thickness (μm)
1	772.837
2	772.841
3	772.841
4	772.841
5	772.837
6	772.837
7	772.837
8	772.841
9	772.837
10	772.837
Average	772.838
1σ static repeatability	0.0018

**Table 1:** Thickness measurement repeatability.

Repeats	Depth in μm average of 10 measurements	1σ repeatability μm
1	49.629	~10 <sup>-3</sup>
2	49.626	~10 <sup>-3</sup>
3	49.629	~10 <sup>-3</sup>
4	49.630	~10 <sup>-3</sup>
5	49.629	~10 <sup>-3</sup>

**Table 2:** Depth and static repeatability of a 5x50 μm<sup>2</sup> TSV.

### Measuring TSV parameters and HAR trench depth

The parameters to be measured are top CD, bottom CD, side wall angle and bottom profile as described below.

**Depth.** The VIT™ enabled thickness spectrum is displayed in **Figure 5**. This spectral signature is typical from a sample like that shown in **Figure 1**.

Repeats	Depth μm
1	100.40
2	100.24
3	100.43
4	100.13
5	100.49
6	100.52
7	100.44
8	100.33
9	100.52
10	100.12
Average	100.367
Semi Dynamic 1σ Repeatability	0.15

**Table 3:** Depth and dynamic repeatability of 12x100 μm<sup>2</sup> TSV.

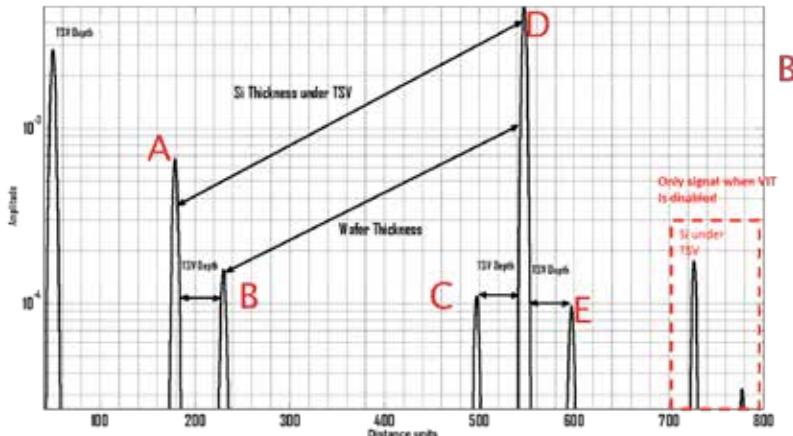
Peaks A, B, C, D and E appear only when the technology is enabled. It is important to note that the separation between peaks A/B, C/D, and D/E is the same as the TSV depth value, which is independently given by the first peak in the spectrum. The technology, therefore, has a self-checking mechanism built into it when measuring via depth. Via depth measured from a sample with 5μm x 50μm TSVs is given in **Table 2**. Depth value in each row corresponds to an average of 10 measurements and the corresponding 1σ standard deviation is shown in the third column. Depth measured with a 12μm x 100μm TSV sample is given in **Table 3**. In this case, between each measurement, the same via was moved in and out of the measurement beam by several millimeters to determine semi-dynamic

repeatability.

**TSV bottom CD.** Peak D in **Figure 5** results from virtual interfaces while peaks C and E are from the coherent interaction of the virtual interface with the interface defined by via bottom. TSV “optical” bottom CD (BCD) is calculated using the area under these peaks. This is not, therefore, a model-based approach. **Table 4** compares the computed BCD with that measured with an IR camera, which has a pixel resolution of 0.3μm/pixel. TCD in the table refers to via top diameter measured with the same IR camera. Knowing top and bottom CDs, the sidewall angle

(SWA) is determined. This is tabulated in the last column of **Table 4**. Similar measurements taken with the 12x100 μm<sup>2</sup> via sample are given in **Table 5**. From these two data sets, one can see that the 100μm deep via is tapered more near the bottom. The new technology can be engineered to measure TSV parameters either from wafer front side and/or back side. So a bottom probe may be used for profile measurement, even if the via is filled.

**Bottom profile in reveal CMP or etch.** For a Cu nail reveal process, it is important to know the via bottom profile, because after wafer-thinning grind, it is required to use CMP or etch the wafer far enough to expose the entire Cu nail rather than its tip. In Cu reveal, the time required from Cu tip exposure to complete via reveal can be several minutes and a priori knowledge



**Figure 5:** VIT™ enabled thickness spectrum that facilitates simultaneous measurement of thickness, depth, and via profile.

	TCD=5.2μm		
Repeats	BCD w/ VIT™ μm	BCD w/ IR Camera μm	SWA deg.
1	3.63	3.3	89.49
2	3.66	3.3	89.50
3	3.70	3.6	89.51
4	3.66	3.6	89.50
5	3.57	3.3	89.47
Average	3.65	3.42	89.49
Static 1σ	0.051		0.014

Table 4: Bottom CD and side wall angle of 5x50μm<sup>2</sup> TSV.

	TCD=11.8μm	
Repeats	BCD (μm)	SWA deg.
1	8.69	89.11
2	8.61	89.09
3	8.67	89.10
4	8.64	89.09
5	8.58	89.08
6	8.64	89.09
7	8.70	89.11
8	8.64	89.10
9	8.70	89.11
10	8.63	89.09
11	8.66	89.10
12	8.78	89.14
13	8.78	89.14
14	8.78	89.11
Average	8.67	0.017
Static 1σ	0.059	

Table 5: Bottom CD and SWA of 12x100μm<sup>2</sup> vias.

of parameter “b” can be valuable in controlling the reveal process. We have demonstrated the technology’s ability to measure bottom profile and the “b” parameter, and the result of one such measurement is shown in Figure 6. In calculating the “b” parameter it is assumed that the bottom profile can be represented by a prolate ellipsoid with the TSV diameter as its major axis, and “b” as its semi-minor axis.

**Depth measurement of the HAR trench.** Using the new technology, the depth of a 3μm wide trench with an aspect ratio of ~ 30 has been measured with good correlation to XSEM data as shown in Figure 7.

**C4 and micro bump measurement.** C4 and μBump arrays can also be measured with the new technology. The height map of C4 measurements is given in Figure 8.

	Thickness (μm)	1σ St.Dev. (μm)
Wfr8	4.35	0.058
Wfr12	3.32	0.051
Wfr13	3.96	0.062
Wfr14	3.36	0.064
Wfr15	3.92	0.037
Wfr24	4.09	0.064
Wfr25	4.14	0.038

Table 6: BSI-CIS wafer thickness.

thickness of 515.3 μm. Glass1 – identified as layer 4 – measured at 792.6 μm, while glass1 and glue form the fifth layer with a combined thickness of 962.2 μm. The total thickness of the stack labelled as layer 6 is 1307 μm.

Bonded Si wafer stacks with thinner individual layers that are tens of microns in thickness have also been measured using VIT™. Another example is the mapping of a warped bonded wafer stack, comprising a carrier wafer, Si layer, and embedding compound, for individual thickness.

**Measuring thickness of thinned wafers.** The technology has demonstrated its ability to measure highly thinned Si wafers, such as a BSI-

**Mapping the bonded wafer stack.** A glass wafer stack bonded with highly index matched glue, as shown in Figure 9, was measured. The thickness of various layers identified in there were parsed out with the new technology. Layer 1 is glue with a thickness of 170.8 μm. Layer 2 is glass2 with a thickness of 345.1 μm. Glass2 and glue form the third layer with a combined

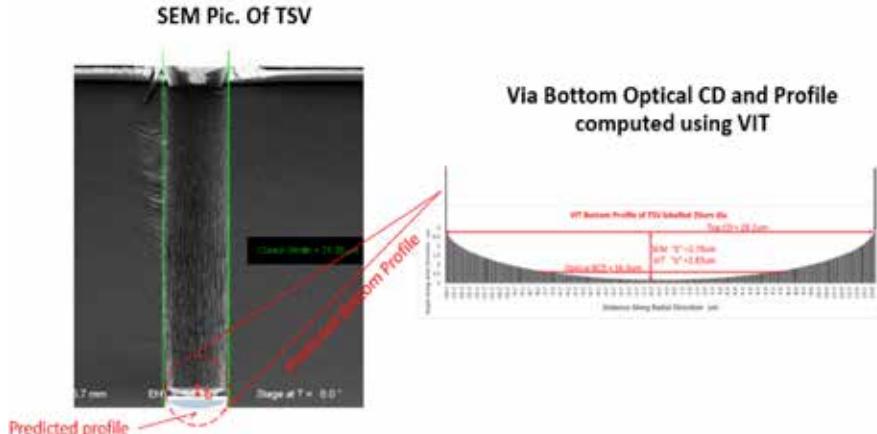


Figure 6: TSV bottom profile: “bSEM”=2.78μm, “b<sub>VIT</sub>”=2.83μm.

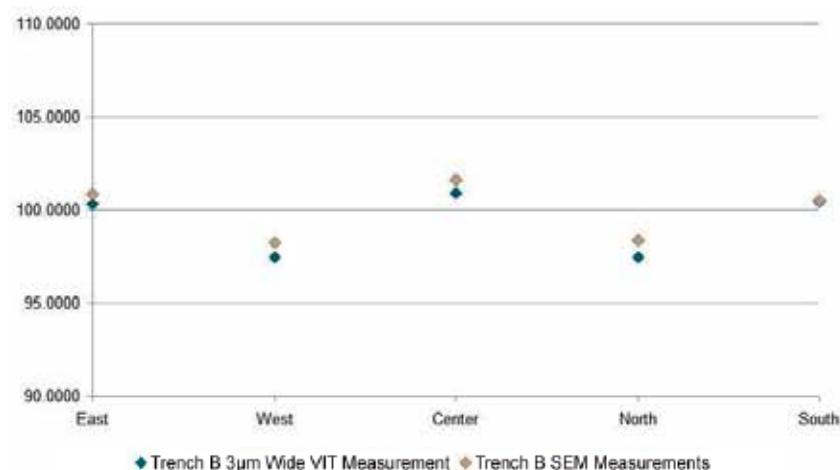
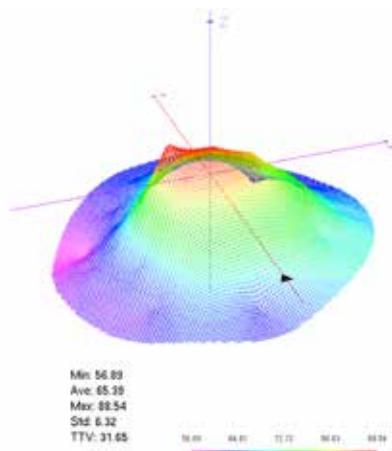


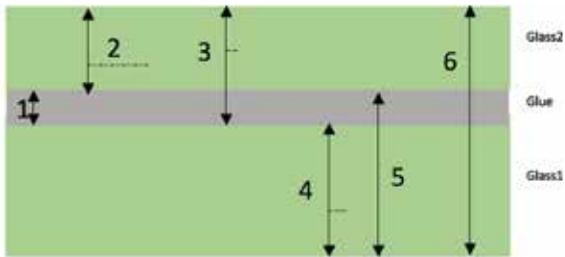
Figure 7: Depth comparison: VIT™ vs. SEM.



**Figure 8:** C4 bumps on an 88 $\mu\text{m}$  thick wafer and height map.



**Figure 9:** Bonded wafer stack (glue index matched to glass 1 and 2).



**Figure 9:** Bonded wafer stack (glue index matched to glass 1 and 2).

CIS wafer from the thinned Si side. Thicknesses measured on seven such samples are tabulated in **Table 6**.

#### **$\mu$ Raman for the TSV keep out zone**

We have also developed an automated high-resolution Raman spectrometer. Using this tool, we have demonstrated its capability to profile stress in the vicinity of metal filled TSVs. To measure the stress profile, the Raman shift in the stressed region is compared to that in

the unstressed region of the Si sample. The difference between the two shifts is used in calculating the induced stress.

**Figure 10a** shows part of a metal-filled TSV array that was used for measuring the keep-out-zone. The stress profile between two TSVs separated by 80 to 100 $\mu\text{m}$  was measured. **Figure 10b**

shows the stress profile before and after anneal. The significant change in stress profile measured by Raman makes  $\mu$ Raman an indispensable process-control-tool in 3D-IC HVM. It must be mentioned here that these measurements were taken on two different samples. The pre-annealed sample has TSVs at 80 $\mu\text{m}$  pitch, while that of the post-annealed sample has them at 100 $\mu\text{m}$  pitch.

#### **Summary**

The tool based on VIT™ has a depth/thickness measurement range spanning a few microns to a few mms. This makes the tool capable of monitoring several FEOL and BEOL processes in 3D packaging applications. These processes include: TSV depth and profile measurements; bonded wafer stacks measurement; thinned Si wafer measurement in RST and BSI-CIS applications; after reveal Cu nail coplanarity measurement; and C4,  $\mu$ Bumps and Cu pillar height measurements. The measurement range in Si spans from 4 $\mu\text{m}$  to 5mm. The technology's versatility 1) enables flexible utilization of tools in production, 2) provides full software compatibility, and 3) affords machine-to-machine matching. These factors in turn minimize cost incurred in operations and service training and lessens spare parts inventory. Consequently, tool downtime is reduced leading to better cost-of-ownership.

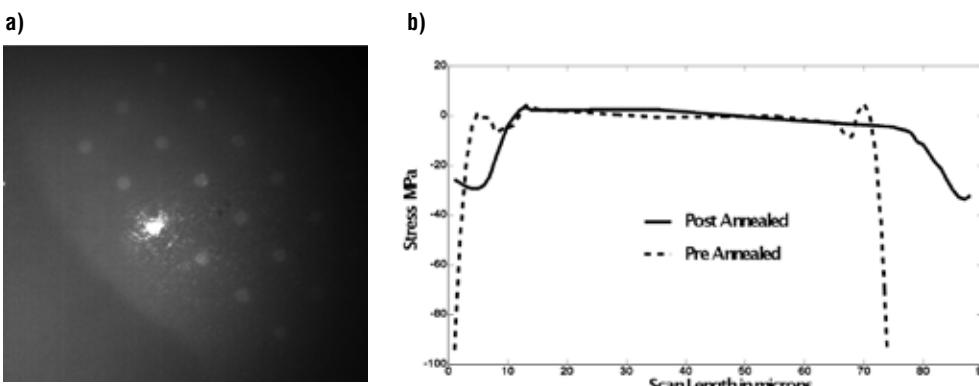
The  $\mu$ Raman tool has a spectral resolution of 0.05 $\text{cm}^{-1}$  and is therefore capable of measuring stress change as small as sub 25MPa. With this tool, we have demonstrated  $\mu$ Raman's ability to profile the keep-out-zone in TSV samples. Additionally, the significant reduction in stress values resulting from the anneal process is mapped by this tool.

#### **Acknowledgment**

The author would like to acknowledge the support given by Ann Koo, Loui Lau, Mihail Mihaylov, Jae Ryu, and Nikolai Maltsev during the development of this tool.

#### **Biography**

Arun A. Aiyer received his PhD in Applied Physics from the U. of Hull, in U.K., and his MS and BS in Physics from the U. of Kerala, in India. He is CTO at Frontier Semiconductor; email: aruna@frontiersemi.com



**Figure 10:** a) Metal filled 5 $\mu\text{m}$  diameter TSVs; b) Stress profiles of pre-annealed and post-annealed TSV samples.

# Advances in tweezer pull testing

By Bob Sykes *[XYZTEC BV]*

**M**easuring bond strength by pull testing is often the best way to get the failure mode in which you are interested. Additionally, and unlike a shear test, as the bond separates, the fracture surfaces are pulled away from each other, cleanly enabling accurate failure mode analysis. To pull a bond requires the substrate and interconnect to be gripped; because of size, shape and material properties, this can be difficult, particularly for the interconnection. In these cases, a set of accurately formed and aligned tweezer tips with precision control of their opening and closing is likely to make the difference between success and failure.

Preparation is the most important part of many things and this is certainly the case with tweezers pull testing. Preparation starts with “alignment,” here, the tweezer jaws are positioned to the sample. The next step is the “grip” where the jaws close onto the sample (**Figure 1**). Having completed the preparation we are

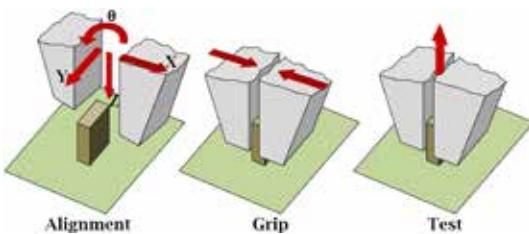
when the jaws are positioned toward the sample in readiness for the grip, but it also includes how the two jaws are aligned to each other. It is important that the tips and center lines of the jaws are in the same plane when they are open and as they close (**Figure 2**). For fine geometry applications this can mean only a few microns of misalignment will have detrimental effects. Before any of this can be done, we have to be able to see the sample and the jaws making illumination and magnification (when required) – an important part of the alignment setup.

Different applications also require different amounts of jaw opening. In the case of fine pitch, the opening must be as small as possible so the jaws do not interfere with adjacent bonds or wires. Alternatively, the bond positioning within the sample may be less precise and a wide jaw opening will reduce the required alignment precision, and less precise alignment can mean more tests per minute. During alignment, the

onto the substrate with a programmable force. The jaws then close while the landing force is maintained, ensuring they remain in contact with the substrate, and therefore, as low as possible. Alternatively, the test may require the grip to be performed at a set height above the substrate. In this case, a light landing force is used to detect the substrate surface, followed by a programmable “step back” to the grip height measured from the sensed initial contact point.

Having set up and completed the alignment, we are now ready for the grip. It may be obvious that the design of the tips that grip the sample is important, but there is much more to it than this alone. Nevertheless, tip design is a good starting point and it is as varied as the samples they have to grip. As shown in **Figure 3**, there are four generic types: plain, serrated, hook, and cavity. These basic forms are then adapted to suit the application. There are three generic modes in the way the tips can close:

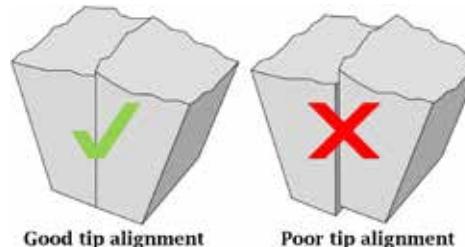
increasing force, constant force, and closing distance. With increasing force, the grip force increases in proportion to the pull force, which may be considered optimum because the grip gets stronger to resist an increasing pull force.



**Figure 1:** Alignment/grip/test.

then ready for the test. Although these two steps might sound simple, it will be shown that there is more to consider than might be immediately apparent. Typical of many activities, we tend to focus on the result, in this case the test, but preparation is where all the work is done and it is in this where success or failure is determined.

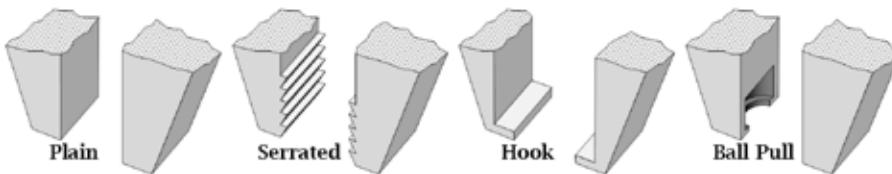
As previously noted, preparation is the “boring hard bit;” what we want is the result! But there is no getting away from it—we have to start at the beginning, in this case, alignment. Alignment occurs



**Figure 2:** Jaw alignment.

jaws are first positioned in the x, y and  $\theta$  (rotation) axes. This is almost always done manually, but it would also be possible to make it automatic. Following this maneuver, there is the vertical or z-axis alignment, which can, again, be manual, but a programmable position relative to the substrate is often useful. In ball pull applications, it is normally important to grip the ball as low as possible, keeping the jaw tips in contact with the substrate; this actually calls for a “landing force.” After initial alignment, and when the test is started, the jaws land

It is ideal when gripping hard samples, but when the sample is soft, the closing force can squash the sample causing it to fail in the jaws rather than at the bond. In cases such as these, the constant closing force method performs better—it is very well suited to gripping soft samples. With hard samples, the friction between the jaws and the sample produces the pull force, and so, increasing the grip increases the friction in line with the pull force required. Soft samples need to be reformed by the jaws to produce a “mechanical lock” between them,



**Figure 3:** Grip types.

and it is this “lock” that opposes the pull force. Examples of reforming are serrations “digging” into the sample, or a cavity reforming a ball into something like a mushroom shape. Reforming only requires a certain force—any more than this unnecessarily reduces the cross sectional area of the sample, reducing the maximum tensile load or pull force it can withstand, and thereby impart to the bond. As the load builds up though, the strain in the sample produces thinning, and this will relax the grip, thereby reducing the hold. It is therefore important that the grip force is held constant to maintain the required degree of interlocking between the jaws and the sample. To maintain this interlocking, the jaws must close as the test load builds up and the sample stretches. Another way of looking at this is, as the sample stretches, material flows out from between the jaws and they must continue to close through the test to compensate for this, maintaining the same grip. Some samples already have a feature under which jaws can hook and this is where constant closing force or a set closing distance can work well together with hook jaws.

Having optimized the alignment and grip on the sample, we are now ready to perform the pull test. As has already been said, this is now a simple task. There can be further complications, such as peel testing, that requires the movement of multiple axes, but in all cases, the sample is now pulled away from the substrate. Understanding the test result and failure mode is far from simple and requires a great deal of understanding, but this is not a topic we will venture into here.

Over the years, there have been many designs of tweezers tips and actuation methods that open and close them. Collectively, they cover all the requirements we have discussed with varying degrees of success and ease of use, but none of them include optimum provision for them all. It was with this intention XYZTEC developed its “USB” tweezers system. In addition to its many functions, the design had to be both

small, so it would fit into limited space applications, and light, so as not to affect the test results.

All tweezers are mounted onto a pull sensor that measures the test force and incorporates the  $\theta$  or rotational alignment axis. Like understanding the test result, the pull sensor is a topic in its own right, but here we are looking at the tweezers. Tweezer modules comprise two main elements: the jaws (tweezer tips), and the actuator that open and close them. To ensure precise alignment of the tips, the USB tweezers are like any set of hand tweezers in that the two halves that close onto each other are fixed together by a pair of spring arms. This design principle is proven to guide features in the jaws that can grip very small parts

by maintaining the alignment of the jaws with the required accuracy as they close. At the top where the two arms meet, there is a quick release mounting spigot for precise installation into the actuator. One screw secures the jaws allowing an easy change over for different applications.

The actuator incorporates a miniature motor, gearbox and positional encoder that drive a lead screw and cam arrangement to open and close a pair of



**Figure 4:** Section of tweezer module.

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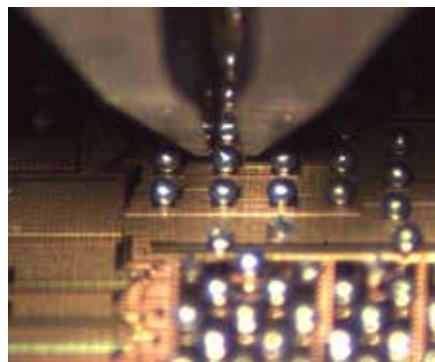
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tweezer actuation arms (**Figure 4**). The actuator arms also include a strain gauge load cell that is calibrated to measure the force at the tweezer tips. Just above the jaw mounting point, a high-intensity adjustable LED provides close and local illumination of the sample at the test point. The pull sensor can also be used in reverse as a push sensor and when required, it is this pull sensor that is used to provide a landing force. All these elements enable the jaw tip distance, opening and closing speed, grip force, landing force and illumination to be under programmable control using real units such as mm/s and kgf that meet all of the test requirements previously discussed. The module can be fitted onto a 100g, 1kg or 10kg pull sensor, and its range of adjustments make it suitable for applications within these ranges of pull force.

With the preparation done, we can start testing (**Figure 5**). The range of tweezer applications is too large to cover in its entirety, but we can look at a few of the more challenging and interesting examples. Gripping and pulling fine gold, copper or aluminium wire requires a precise opening position and constant closing force. Similar to a pair of pliers in miniature, jaws fitted with an integral diamond cutter positioned slightly above the tips of the jaws let the operator cut wire or ribbon so that only one bond can then be tested.

One of the most challenging tweezer tests is ball pull (**Figure 6**). This is often referred to as CBP which stands for cold ball pull or cold bump pull depending on any preference. The difficulty arises from the small geometries. Copper balls are relatively easy to test because they are



**Figure 6:** Cold ball pull test example.

quite hard and can withstand high grip forces without unacceptable deformation. Negligible, if any, reforming of the ball is required as the grip friction alone can be greater than the bond strength. Solder, and particularly gold, though, is more difficult and requires special cavities to be machined into the jaws to reform it, thereby allowing a suitable mechanical grip. To date, the limit on the ball size remains in the region of 50µm with the increase in volume of bumped wafers being a driving influence on continued development.

Tweezers are often used for peel tests. The example in **Figure 7** is of an aluminium bus bar being peeled from a solar cell wafer. This test has the added

complication that the wafer substrate is extremely fragile. To be able to peel the bus bar from it without it breaking requires the special clamping fixture shown below the tweezers. Ribbon peel on flex, or very thin substrates, can present similar difficulties that again require intricate clamping and support. Alternatively, when the substrate is rigid, the test is typically less complex.

Established tweezer solutions exist for the majority of applications. As previously noted, the ability to grip ball interconnects as they continue to shrink is a likely requirement. Another possible development would be a fully automated test, and this would be possible with a modern bond tester fitted with a suitable tweezer actuator. One capability that has not seen as much exploration is a means of clearing the tested parts out of the jaws, which is a particular problem for soft interconnects that get lodged into the complex features that reform the part – ball pull being a good example of this.

## Biography

Bob Sykes received an honors degree in Mechanical Engineering and is a Chartered Engineer; he is Chief Technical Officer at XYZTEC BV;



**Figure 7:** Peel test example.



**Figure 5:** Gold wire test.

# Improving tester area productivity through factory automation

By Shekar Krishnaswamy, David Hanny [[Applied Materials](#)]

The semiconductor test operation is the last step prior to customer shipment and therefore represents an important step in the overall order fulfillment process. Technological advances in the packaged products, as well as the fab production process, are driving more requirements for test, which in turn has increased the cost of testing. Factory automation methods developed in the fab segment have a proven track record in addressing these challenges effectively. They can help in significantly improving the overall equipment efficiency (OEE) of test equipment and the overall productivity of the test segment. In addition, test operations are faced with numerous challenges from a business perspective. These challenges include increasing product complexity, equipment diversity, technological evolution, product cost management, the industry migration from an integrated device manufacturer (IDM) to an outsourced assembly and test (OSAT) model, and supply chain requirements. These business-related challenges are significant and the impact is seen on the test operations at the factory level in the form of capacity imbalances, frequent setups and changeovers, prioritization issues resulting from product re-entrancy, managing large volumes of data, and management of large batch sizes. This paper will provide insight into the concepts and methods to address these manufacturing detractors and achieve the improvements necessary for a profitable test operation.

## The business challenges in test

The migration from “big box” communication and computing

equipment towards hand-held devices that boast high-speed, “always-on” connectivity with long battery life, and location-aware capabilities, have significantly changed the packaging landscape. This drive towards product miniaturization, low-power devices, higher functionality and lower costs has considerably increased the demands on test over the years. The penetration of electronics into the automobile and home segments have also added to the product and packaging complexity. While the business challenges are many, some of the important ones are discussed below.

**Product complexity.** Current assembly and test facilities are facing an explosion in part types compared to a few years ago. This part type explosion is also driving different types of testing leading to high degrees of factory complexity. In some cases, the same devices that are targeted for different markets, also drive different test policies. This product-driven complexity affects factory planning, factory efficiency, and factory monitoring and order fulfillment.

**Equipment diversity.** Currently, the typical test floor comprises many different types of testers – single device testers, parallel testers, single-headed testers and multi-headed testers. In addition, the test operation also requires other equipment resources such as handlers, load boards and sockets. While the determination and planning of all the required resources is a daunting task by itself, the high degree of variance driven by different equipment suppliers and different generations of equipment makes the task even more challenging. Maintaining high equipment utilization

is necessary to keep product costs low, but the diversity and dependency factors are major obstacles.

**Technological evolution.** In the past, the traditional lead frame based products made up nearly half of the products produced—today, it is less than 25%. Leading edge technologies such as flip-chip, chip-scale packaging (CSP), wafer-level packaging (WLP), stacked devices with through-silicon vias (TSVs), and numerous variants and combinations of the above, have made all aspects of the product lifecycle more challenging.

**Product cost management.** In a span of three years from 2008 to 2010, the cost of silicon declined as a result of the evolution of fab processing technologies. However, the cost of test has generally remained flat. The main reason this flatness has been the increase in the complexity of the testing process, the increase in the number of test passes for the product, and an increase in the cost of the overall test equipment suite, which is the combination of the tester, handler, load board, and sockets.

**IDM to OSAT model.** Cost-driven pressures have forced many of the integrated device manufacturers (IDMs) to spin-off or sell assembly and test factories. The assembly and test production volumes have migrated to outsourced services for assembly and test (OSAT). This migration comes at the cost of reduced flexibility and control, which consequently drives changes in enterprise resource planning (ERP), customer commitment management and logistics.

**Supply chain transformation.** Today, any portion of the fab, assembly or test operations can be in-sourced or

out-sourced. Any combination of the above can occur within the company, leading to significant supply chain challenges. In addition, contractual and customer satisfaction policies usually necessitate different levels of order prioritization that only add to the supply chain and order management complexity. If not properly managed, and necessary actions implemented during order execution, these challenges can severely impact customer deliveries leading to negative business consequences.

### Operational challenges in test

While the above business related challenges are significant, the impact is quickly transferred to the test operations at the factory level. The important challenges faced by test floor operations are discussed below.

**Capability and capacity imbalances.** Some of the key types of testers that may exist on the same floor are single device testers, parallel testers, single-headed testers and multi-headed testers. Many different tester alternatives may exist for testing a particular product, and a wrong tactical decision may have a negative impact on factory output and order fulfillment.

Testers that have similar capability may still display differences in reliability, testing speed, and quality of testing. This inherent imbalance in capability causes problems in tactical planning if not comprehended accurately. The next imperative is to execute to the plan at the shop floor level.

**Equipment setups.** The tester setup operation is complex, tedious, and iterative. Although the objective of factories is to achieve a successful first-pass setup, success often follows only after a few iterations. This constraint causes long setup durations (typically in hours) that require a significant amount of technician time.

Typically, the planning process assumes a certain number of setups per machine per week. What is commonly missed during the planning process is that certain setups are sequence-

dependent and will positively or negatively impact the productive time on the machine. As a result, the planned number of setups or the planned setup time is often exceeded. Product priority changes, quality problems, unscheduled equipment downtime, improper product routing, and so forth can cause more setups to the machines than the plan recommends. Such changes require two-way communication—manufacturing needs to know the setup quota from planning, and planning must be able to obtain feedback when this quota has been exceeded so that future plans can be adjusted accordingly.

**Product re-entrancy.** A few years back, single-pass testing was the norm and multi-pass testing was the exception. Today, it is very common to have multi-pass testing on most of the products in the factory. As mentioned earlier, increasing product complexity and increasing customer need for higher product quality have necessitated this change. While in many cases the multi-pass testing may be done at different temperatures requiring additional fixtures that drive setups, the operational complexity of tester/handler dedication, test time differences, and sometimes sampling policies, are sufficient to significantly stretch human decision-making capabilities.

**Data management.** Typically, data sources in manufacturing are diverse and include factory systems such as manufacturing execution systems (MES), engineering systems for product specifications and equipment capabilities, industrial engineering systems for processing times and equipment setup time, enterprise resource planning (ERP) systems for product demand and supply volumes, etc.

The test area has to comprehend and deal with very high volumes of data as it directly ties in at die-level volumes and encompasses a significant number of test parameters. With this large volume coupled with data diversity, it is becoming more challenging to quickly gather all needed data for timely decisions. Shortcuts include using stale

data or examining the output test data less frequently. Such shortcuts impact the ability to deliver the right quantity of product on time to customers.

**Batch size management.** While the automated test equipment (ATE) tests each device as a single unit or multiple devices in parallel, the input and output for the tester is the product lot. However, the burn-in operation prior to ATE can handle different lots, or may even have to handle subsets of a lot. In addition to large batch sizes, the burn-in times are long and on the order of many hours or even days. This gives rise to managing a different type of complexity—balancing cycle time without sacrificing equipment utilization or output.

**Segmented outsourcing.** In some instances, certain operations in test, like burn-in operation, may be outsourced to external companies. While this removes the batch size vs. equipment utilization problem, it adds complexity to the in-process logistics, product handling, product verification, and cycle time aspects.

**Factory dynamics.** The influence of factory dynamics cannot be understated. Even if good plans are developed, good execution mechanisms are in place, and data is aggregated from multiple sources, the process breaks when changes in assumptions are not understood and operational adjustments are not properly executed. Example scenarios include product holds, equipment downs, product priority changes, non-availability of peripheral resources such as load boards and sockets, and so forth.

### Role of planning, scheduling and dispatch

The complexities of test operations have increased significantly over the years; achieving high customer satisfaction with on-time delivery and cost-competitive products is a primary objective. Manufacturing scheduling and dispatching are proven systems that contribute towards meeting these objectives. However, current methodologies of manual planning and

execution will not achieve these goals. The effects of factory and customer dynamics are so large that manual methods characterized by data latency, human latency, human variability, and errors, cannot compete for long. Moreover, such manual methods do not scale in a cost efficient manner with changes in product mix, volume, technology, and factory sizes.

Solutions are therefore needed that enable factories to be nimble and to make decisions quickly. Solutions must not only be accurate, but must execute quickly and seamlessly. Obtaining real-time data aggregated from manufacturing, engineering, and planning systems is a necessity. In addition, solutions must easily capture business rules and provide useful information to all manufacturing stakeholders. Mission critical requirements are discussed below.

**Reporting and business rules representation.** A successful planning and scheduling solution must provide data management and data transformation functions so that planners can create weekly, daily, or even plans on a shift-by-shift basis. The data management functions must have access to real-time data so that operation changes can be made as needed.

**Dispatching and scheduling execution.** After a good plan is created, a mechanism to execute to plan must be provided. The solution's execution mechanism must be systematic and not prone to variability in human latency. This means that it must be integrated with factory MES transactions. The results of material processing decisions must align with the plan where the same business logic used to generate the plan is used in the dispatching and scheduling function. In addition, shop floor and equipment specific considerations must be incorporated so that overall factory objectives are balanced with practical operating constraints.

**Real-time data access and representation.** Because the factory floor is dynamic, real-time data must be used in the decision-making. The lack of real-time data renders decisions

ineffective and makes the planning and scheduling functions less credible. This lack of real-time data, therefore, promotes circumventing system logic by humans leading to higher manufacturing variability. In addition, real-time feedback is necessary to the ERP and planning functions for better planning.

**Change management.** A successful planning and scheduling solution must be implemented with minimal affect to business processes and shop floor end users. Many good systems fail because they are implemented as add-on functions to existing business processes. Other important aspects are managing changes in business logic and the availability of data sources. Such changes must be implemented with minimal reliance on complex coding and the expertise of additional IT personnel.

**Compliance monitoring.** A system is effective only to its degree of use. A planning and scheduling solution

must therefore enable usage to be monitored for effectiveness. This supports consistent system execution and reduction in variability. If operators don't follow dispatch decisions, it may indicate inherent flaws in business logic. Such measurement of operator compliance enables timely detection and correction.

### Deploying advanced planning, scheduling, and dispatch

Two cases that highlight the impact of planning, scheduling and execution via dispatch in test operations are detailed below. The two cases are highly disparate but represent the actual problems seen on the test floor. To help understand the cases, simple configurations were chosen and simulation modeling was chosen as the vehicle to demonstrate the coordinated working of planning, scheduling and dispatch execution.

**Case-1 (burn-in oven).** Two part



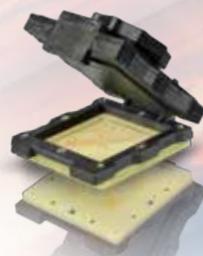
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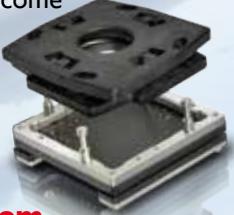


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types A and B are required to undergo the burn-in process. Product A has a 24 hour burn-in, while product B has a 36 hour burn-in. The maximum batch size of the burn-in oven is 1500 parts for both products. The lot size is 5000 parts for both products. There are 9 burn-in ovens. A key decision parameter is the operating batch size for the oven. There are two operating modes that have been modeled. One mode is to operate the oven at fixed batch sizes that makes it easy for shop floor operation. The other

has been formed to enable arriving lots to fill up to the maximum batch size, if possible. The simulations were performed for a 10 week period. The simulation tool used was the Applied Materials AutoSched AP (ASAP) system. The results of the simulation are given in **Table 1**.

Based on **Table 1**, it is clear that the intelligent batching approach provides better cycle time and on-time delivery results. The different levels of utilization represent the loading of the factory or

when to do the setup on the tester. There are two dispatch modes relating to the setup that have been modeled. One mode is to dispatch product on a first-in, first-out mode and let that policy dictate the setup. This procedure is used in many factories because of its simplicity. The other mode is to dispatch by batching lots that require the same setup. A setup change happens only when there are no lots using the same setup. The next setup to change is dictated by the lot due date and implemented via the critical ratio rule. Here again, the simulations were run for a 10 week period using the Applied Materials AutoSched AP simulation system. The results of the simulation are given in **Table 2**.

From the above discussion and **Table 2**, three important findings can be seen. First, the setup optimization policy clearly produces better results as evidenced from the setup percentages, cycle time, and the on-time-delivery (OTD) metrics. Second, it can be seen that even with setup optimization, OTD is affected at higher levels of utilization. This is true when the cycle times are higher and this effect is clearly seen. Third, at 40% utilization or below, setup optimization may not be necessary as there is enough tester capacity.

The above analysis further underscores the ability of good planning processes that determine the “sweet-spot” in which a company may want to operate. The “sweet spot” here is defined as the loading of the factory that is high enough to ensure profitable production while at the same time not affecting the on-time delivery performance of the product. This is a highly desirable factor, but also very complex to determine because of the factory and customer ordering dynamics. Simulation-based planning and RTD-based scheduling and dispatch work synergistically to give factories this leading-edge and differentiated capability.

## Summary

The business and operational challenges in test clearly highlight the need for more sophistication in decision making at the planning and shop floor level. As a result of advances

Batching Mode	Util	CT	OTD	Avg BS	Outs
Intelligent Batching	90%	54	87%	1396	730000
	84%	48	94%	1368	655000
	78%	43	98%	1340	615000
	69%	41	98%	1339	520000
	62%	39	99%	1316	495000
	54%	37	100%	1301	415000
Fixed Batching	89%	69	65	1400	720000
	83%	67	69	1370	645000
	77%	65	70	1340	605000
	69%	67	70	1340	510000
	61%	67	70	1320	485000
	54%	71	59	1300	410000

**Table 1:** Results of simulation for a burn-in oven.

mode is to operate with an intelligent policy that ensures a minimum batch size, yet tries to achieve the maximum when the work-in-process (WIP) exists. The intelligent batching policy also takes into account a waiting time period of 1 hour after the minimum batch size

the appropriate demand plans.

**Case-2 (ATE).** Two part types A and B are required to undergo the test process. Product A has a 2-pass test, while product B has a 3-pass test. There is a one hour setup between each test pass for product A, and a 1.5 hour setup

for each pass on product B. The test times vary from 1 to 2 seconds per part of product A, and 1.2 to 2 seconds per part of product B. The lot size is 5000 parts for both products. Eleven testers were assumed to be used for the two products. A key decision variable is

Setup Mode	Util	Setup	CT	OTD
With Setup Optimization	86%	2%	48	38%
	80%	2%	32	49%
	70%	3%	19	60%
	61%	4%	13	74%
	51%	6%	10	89%
	40%	7%	9	98%
No setup optimization	75%	14%	191	39
	74%	13%	96	37
	68%	12%	36	46
	59%	11%	22	57
	50%	10%	12	78
	40%	8%	9	95

**Table 2:** Results of simulation for a tester.

in decision and automation techniques, key planning and scheduling operating parameters can be monitored today at a much more advanced level. A systematic and consistent methodology is also necessary to implement at the shop floor level for execution to enforce the plans and schedules. While the benefits of simple cases have been presented, they are even more magnified in real-world cases. But, even in simple cases, it is not easy for humans to absorb, assimilate and use the different streams of data required for such sophisticated decision making. Applied's Factory Control and Automation systems provides the infrastructure, the technology and the business rules necessary to plan, schedule and execute, thereby enabling test operations to extract the maximum efficiencies from the factory.

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## Biographies

**Shekar Krishnaswamy** received his Bachelors degree in Mechanical Engineering from Anna U. in Madras, India and a Masters Degree in Industrial Engineering and Operations Research from the U. of Massachusetts at Amherst, and is a Senior Member of Technical Staff at Applied Materials-Automation Products; email Shekar\_Krishnaswamy@amat.com

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# INDUSTRY NEWS

## Corrections to page 36 of the article published in Chip Scale Review, March April 2014

NANIUM S.A. was omitted in the rankings presented in table 6 and 7 as previously published. The correct ranking is now accurately indicated.

## Ranking the top OSATs in IC packaging

Reconfigured FOWLPs were introduced in 2006. After devices are manufactured on a wafer, the devices are sawn and transferred on a carrier to another larger wafer that has gaps between die, which are filled with overmold material that also coats the back side of the devices for protection. This process allows for a larger surface on which to extend an RDL, thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a PCB. The leaders in FOWLPs are ranked in **Tables 6** and **7**.

FOWLP units (largest to smallest)
STATS ChipPAC
NANIUM S.A.
ChipMOS
Amkor
ASE

**Table 6:** FOWLP units (largest to smallest).

FOWLP revenue (largest to smallest)
STATS ChipPAC
NANIUM S.A.
ChipMOS
Amkor
ASE

**Table 7:** FOWLP revenue (largest to smallest).

South Korea-based STS Semiconductor & Telecommunications Co. Ltd., a leading semiconductor assembly and test solution provider specializing in mobile and communication devices, have entered into an agreement to validate high volume manufacturing capability for Invensas' Bond Via Array (BVA™) technology for next generation smartphone and tablet customers.

BVA is a proven advanced Package-on-Package (PoP) technology for System on Chip (SOC) and memory integration in mobile devices. Styled as a "Bridge Technology to 3DIC", it is a unique solution that utilizes established wire-bond assembly techniques to enable low power and high-bandwidth (1000 IO+) packaging in an ultra-small form factor, ideal for mobile devices.

STS's state of the art engineering and worldwide high-volume capabilities provide an ideal platform for high volume manufacturing of BVA.

"We are delighted to partner with Invensas on BVA," stated Chang-Bum Shim, Chief Operating Officer and Executive Vice President for STS. "STS understands the critical need to increase interconnect bandwidth for the growing Package-on-Package mobile SOC market, without increasing product size or the cost to the end user. Our engineering and manufacturing capabilities are ideally suited to the commercialization of BVA."

"STS is an ideal partner for BVA," said Simon McElrea, CTO of Tessera Technologies, Inc. and President of Invensas. "Their

continual investment in cutting-edge packaging technology and associated manufacturing capability, coupled with their growth model in mobile and communication devices, is perfectly aligned for BVA commercialization."

## Amicra welcomes newest Regional Sales Manager, Dave Halk

Amicra Microtechnologies GmbH announced that Dave Halk is the latest addition to its Regional Sales Management team, with a primary focus of serving the market of the USA

eastern region. Halk has an extensive technical background serving the advanced packaging market within the electronic assembly industry. Most recently, before starting at Amicra, Halk held the position



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## STS Semiconductor and Invensas to partner on high Bond Via Array (BVA) mobile solutions

Tessera Technologies, Inc. announced today that Invensas Corporation, its wholly owned subsidiary, and Seoul,

of Project Manager and Business Development Manager at SYNATEC GoA in Chattanooga, TN, where he organized and structured a new distribution channel for North America. Previous to that, he served as Business Manager at Siemens Electronic Assembly Systems & Co., located in Atlanta, where he managed and integrated several new products, including die bonders and inspection systems, into Siemens existing distribution channel. Halk has also held positions as General Manager, and Product Manager, correspondingly, for automated assembly equipment suppliers for the semiconductor industry, Besi/Datacon North America, and Kulicke & Soffa.

### **Deca Technologies ships 100-millionth wafer-level packaged component**

Deca Technologies, an electronic interconnect solutions provider to the semiconductor industry, announced that



it shipped its 100-millionth component. The company attributes this milestone to strong demand from portable electronics manufacturers for wafer-level chip scale packages (WLCSP) manufactured using Deca's integrated Autoline production platform, which is designed to achieve faster time-to-market at lower cost.

Leveraging advanced Autoline volume production technologies from SunPower Corp. (NASDAQ:SPWR), a leading solar technology and energy services provider, Deca quickly achieved this milestone by addressing cycle time and capital cost challenges that semiconductor device manufacturers have struggled with using the conventional approach to WLCSP manufacturing.

"As a customer of Deca Tech, Cypress has used the fast New Product Introduction capability of Deca to streamline its

back-end process and achieve cycle times of fewer than three days for full turnkey wafer-level packaging, test and singulation," said T.J. Rodgers, president and CEO of Cypress Semiconductor Corp. "We are even more pleased with Deca as our subsidiary," Rodgers continued. "The company's quick ramp to the 100-million-unit milestone is proof of the value proposition that we envisioned when we invested in this market."

### **Quik-Pak selected to provide enhanced molding and assembly services to wireless semiconductor and solar customers**

Quik-Pak has expanded its transfer molding and assembly capabilities to accommodate the increased demands of innovative companies in the wireless electronics and solar industries.

Quik-Pak's newly expanded manufacturing space, which is dedicated to its transfer molding operation, will be utilized to meet the volume demands of its customers. The company has also expanded its wafer preparation facility to accommodate new equipment capable of supporting high-volume wafer backgrinding and dicing operations.



"This expansion comes in response to our customers' demands for a reliable, US-based, mid-volume packaging and assembly provider," said Casey Krawiec, Global Sales and Marketing Manager. "Historically, Quik-Pak has been the go-to company for quick-turn and prototype builds. Our customers have increasingly asked us to provide packaging and assembly services in higher quantities. With this expansion and purchase of new equipment, we now have greater capability than ever before." The addition of an ISO class 8 molding room and the

expansion of the company's ISO class 7 dicing area allows it to provide volume manufacturing of saw-singulated air-cavity and over-molded QFN and DFN packages to customers, noted Steve Swendrowski, Quik-Pak General Manager.

### **NASA JPL enhances device fabrication capability with new Plasma-Therm system**

Plasma-Therm's VERSALINE® Deep Silicon Etch™ system was recently installed at NASA's Jet Propulsion Laboratory (JPL) to expand its silicon deep-etching resources. The new etching system targets silicon-based applications that include MEMS, sensors, and resonators. JPL's Microdevices Laboratory (MDL) serves users with many different requirements, and the system's mask selectivity, uniformity, vertical profiles,



sidewall smoothness, and silicon-on-insulator capabilities will be used to meet their device fabrication needs.

The new VERSALINE will complement JPL's existing suite of Plasma-Therm equipment, which has been used to make mission-critical components for NASA explorations. JPL scientists utilized Plasma-Therm systems to help fabricate sensors for the Planck and Hershel missions to map infrared and sub-millimeter cosmic radiation, and the spectrometer grating installed on the moon-mapper to detect water. Tunable diode lasers to sense methane and other metabolic products from possible past life forms, part of the planetary exploration project involving the Mars Rover, were also made with the assistance of Plasma-Therm technology.

A recent report describes new cosmic microwave background polarization

measurements, providing strong confirmation of the Big Bang theory and insight into the first moments of a rapidly expanding universe. The low-noise, superconducting and bolometer-based detectors were fabricated using Plasma-Therm systems that are part of the key process toolset at MDL.

"It is inspiring knowing that Plasma-Therm systems are used not only to develop sensors and optical devices for observing our terrestrial world, but also to contribute to the exploration of our solar system, other galaxies, and the early universe," said David Lishan, Plasma-Therm Principal Scientist and Director, Technical Marketing. "With the installation of this Deep Silicon Etch system, we look forward to expanding our partnership with JPL and providing another means to contribute to their exciting exploration missions."

### Dynaloy scientists highlight time and money-saving benefits of new single wafer cleaning technology for advanced packaging applications

Scientists from Dynaloy, LLC and EV Group explained a new, one-step cleaning process for removing negative dry film and negative spin-on film photoresist at the SEMATECH Surface Preparation and Cleaning Conference in Austin, Texas. Authors from Dynaloy include Technology Manager Kim Pollard, Chemist Travis Acra, and Chemical Engineer Richard Peters.

Known as CoatsClean™ technology, this approach to cleaning represents an improvement in process technology because it uses fewer chemicals, shortens process times, enables high wafer-to-wafer consistency, and offers process flexibility. All of these advantages come together in this process that has its own tool, the newly developed EVG-300RS.

During the presentation, researchers explained in detail how the CoatsClean™ technology process works. First, coat the wafer with a small amount of a specially formulated cleaner, then heat the formulation on the wafer, and finish with a rinse. Local point-of-use heating offers flexibility by allowing different wafer types to be cleaned with the same tool in the same bowl, eliminating the cost and time involved in setting up transitions. This process works on several different wafer types for both 200mm and 300mm wafers.

"Unlike spray processes that require large quantities of liquid for cleaning, CoatsClean™ technology is less expensive because it involves comparatively small amounts of cleaning solution. This factor creates a lower cost of ownership and a decrease in cost per clean, two important considerations within the industry," said Pollard.

The Power of [Integration]

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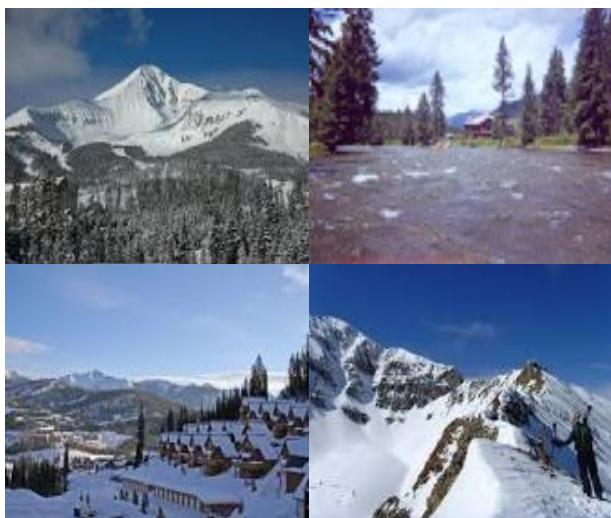
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## 2015 IEEE Aerospace Conference

Yellowstone Conference Center, Big Sky, Montana,

March 7-14, 2015

Track 11 "Diagnostics, Prognostics, and Health Management"

Session 11.12 "Probabilistic Design for Reliability of Aerospace Electronics and Photonics"

Co-chairs: E. Suhir, USA (suhire@aol.com) and L. Bechou, France (laurent.bechou@ims-bordeaux.fr)

## Call for Papers

300-500 word abstract due July 1, 2014, full-length paper (6-20 pp) due October 24, 2014

Peer-reviewed paper returned to author – November 14, 2014

**Final paper due date: January 5, 2015**

All submissions are electronic at: [www.aeroconf.org](http://www.aeroconf.org).  
Indicate session 11.12.

**Session's mission:** Probabilistic-design-for-reliability (PDfR) approach enables one to dramatically improve, in addition to diagnostics, prognostics and health monitoring (PHM) effort, the existing practices by quantifying, on the probabilistic basis, the operational reliability of aerospace electronic, opto-electronic and photonic materials, devices and systems. Major topics of the session include, but are not limited to, design for reliability (DfR), testability, and manufacturability; advanced electronic and photonic packaging; highly accelerated life testing (HALT) and failure oriented accelerated testing (FOAT); predictive modeling at all the stages of the product's lifetime; optimization studies and sensitivity analyses; missions success and safety; design for harsh and uncertain environments; human-in-the-loop related off-normal situations: could/should they be considered at the design stage?

**It is the 36-th annual week-long conference designed for aerospace experts, academics, military personnel, and industry leaders. The conference promotes interdisciplinary understanding of aerospace systems, their underlying science and technology. Attendees enjoy exceptional access to authors in a setting ideal for developing lasting relationships benefiting participants, their organizations, and the engineering and research communities.**

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