

# ChipScaleReview®

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*The Future of Semiconductor Packaging*

Volume 22, Number 4

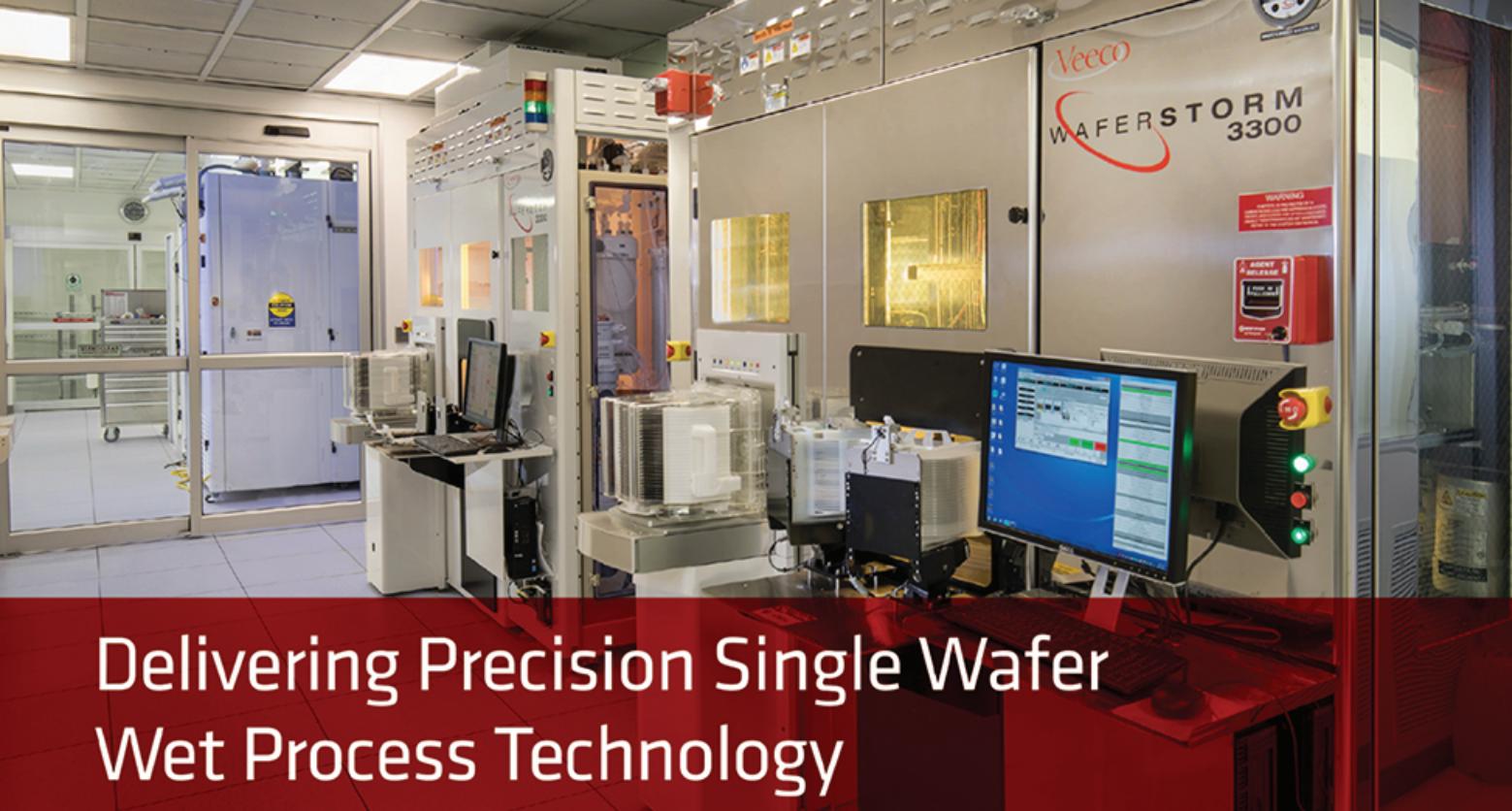
July • August 2018

## Advanced chip-package-board co-design

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- Coaxial socket technology
- Metal-based wafer-level and 3D-printed packaging
- Die-attach materials and LED functional performance
- Temporary bonding for high-temperature processing of thin glass

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Zuken's CR-8000 PCB and package layout design tools enable multiple chips, packages and boards to be assembled, viewed and edited on one canvas in either 2D- or 3D-mode. The image shows a three-die stack on a silicon interposer that is wire bonded to a package and placed on a board. A simple click into any one of these components in a hierarchy tree switches edit context to the selected part, including its specific technology, rules and layer stack-up.

Cover image courtesy of Zuken USA Inc.

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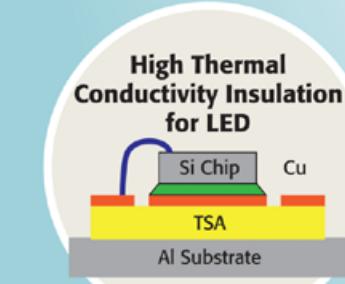
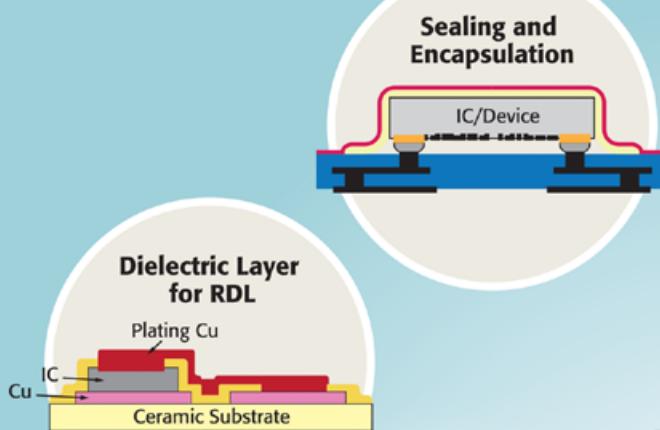
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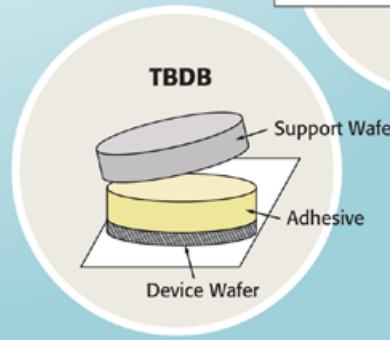
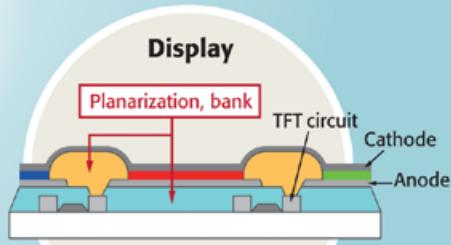
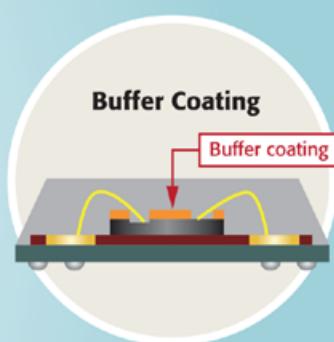
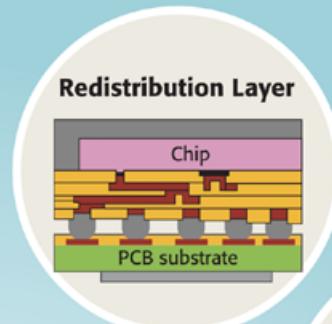
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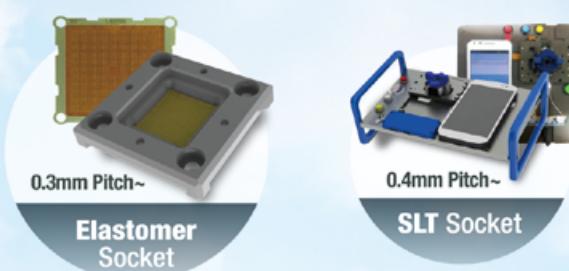
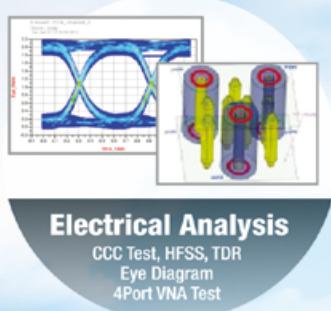
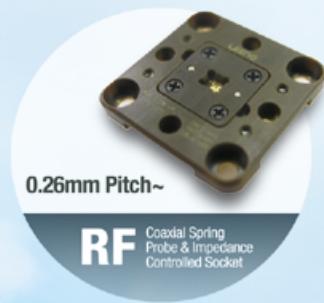
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# GUEST EDITORIAL



## Panel-level packaging shows great progress on large-area fan-out processing



By Tanja Braun and Michael Töpper [Fraunhofer Institute for Reliability and Microintegration]

The industry's march to reach ever decreasing on-chip dimensions is further exerting pressure on the interconnection to the mother board. The hype of Si-interposer technology is slowing down and has been commercialized for high-end applications, but has not proved to be a solution for consumer applications and other products. Conventional wafer-level packaging (WLP) (i.e., fan-in type) is actually a substrate-less package that is limited to a low number of I/Os due to the limited and steady decreasing area for the routing of each IC node. Any type of fan-out and miniaturized packages are therefore the optimal solutions to keep track of these developments. Fan-out wafer, and especially panel-level packaging are therefore two of the latest trends in microelectronics packaging. Simple upscaling of existing FOWLP technology, however, is not feasible and the use of equipment and materials from other market segments such as printed circuit board (PCB), liquid crystal display (LCD), or solar, also needs intensive development.

The Fraunhofer Institute for Reliability and Microintegration is spearheading this transition from fan-out wafer to fan-out panel-level packaging (FOPLP) with an initiative that is bringing together distinguished international partners – innovative small and medium-sized enterprises (SMEs) as well as global players. At the project's outset in December 2016, the project began with 17 international partners from industry (Amkor Technology, ASM Pacific Technology Ltd., Austria Technologie & Systemtechnik AG, Brewer Science,

Inc., Evatec AG, Hitachi Chemical Company, Ltd., Intel Corporation, Merck KGaA, Semsysco GmbH, Unimicron Technology Corp. and Ajinomoto Group, Atotech Deutschland GmbH, FUJIFILM Electronic Materials U.S.A., Meltex Inc., Mitsui Chemicals Tohcello, ShinEtsu Chemical, SUSS MicroTec SE). These partners worked to develop and evaluate materials, equipment and processes for panel-level packaging towards a reference flow ready for industrialization.

Eighteen months have passed since the kick-off meeting during which time the small- and medium-sized enterprises (SMEs) and global players have worked together on assembly strategy and dynamic layout adaptation, warpage control and solving die shift along with RDL on organic panels towards 2µm lines and spaces framed by a complex cost model. Over 100 different panels with over 100,000 embedded test chips have been manufactured to evaluate the influence of different materials and process steps. This level of effort also demonstrates the complexity of the topic and the need for multi-partner consortiums and projects. Besides the technical developments and progress, the topic of the missing standardization was intensively discussed and the group recognized this situation as one of the economic risks for panel-level packaging, especially for new equipment developments and handling infrastructure.

Together with SEMI, as a global industry association, the lack of standards has been identified as an important topic and a fan-out panel-level packaging task force was founded. This task force is now developing one or more standards focusing on panels for FOPLP applications, with an emphasis on parameters such as size, ID marking and orientation, edge exclusion or geometric parameters, such as total thickness variation (TTV), bow, warp, etc.

The main questions for the next 6 months of the project will be to find the sweet spot of PLP compared to production on wafers. This discussion, and also how to continue the project in 2019, will be tackled during IWLPC 2018 with a technical presentation at the conference on the challenges and advantages of PLP, an IZM-Panel Level Consortium booth at the exhibition, and a panel discussion on "What is the Sweet Spot for Large-Area (Panel) Packaging," with participation from major industry players.

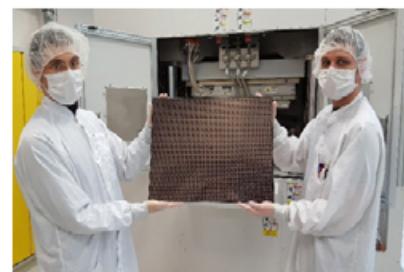
### Biography

Tanja Braun received her Dipl.-Ing. and Dr.-Ing. degrees from Technical U. Berlin and is heading a group on Assembly and Encapsulation Technologies, as well as the Panel Level Consortium at Fraunhofer Institute for Reliability and Microintegration; email tanja.braun@izm.fraunhofer.de

Michael Töpper has an MS degree in Chemistry and a PhD in Material Science. Since 1994 he has been with the Packaging Research Team at TU Berlin and Fraunhofer IZM, and since 2015 he has been a part of the business development team.



Large area 18"x24" panel-level compression molding for chip embedding



18"x24" fan-out panel with double-sided routing and through-mold vias



Jeroen Hoet



Stephen Hiebert

## Automotive apps are driving inspection requirements for advanced nodes

*Chip Scale Review asked KLA-Tencor experts Jeroen Hoet and Stephen Hiebert to respond to questions that provide insights into the defect reduction strategies needed for packaging of devices intended for automotive applications.*

**C**SR: How is the defect reduction strategy for packaging at outsourced semiconductor assembly and test suppliers (OSATS) or integrated device manufacturers (IDMs) different for the automotive industry compared to other industries such as consumer or mobile?

**KLA-Tencor:** At the final packaging assembly and test stages we see various trends for automotive that differ from consumer and mobile applications. Because of the push of the automotive industry for “Zero Defects,” increasing reliability is a higher priority than reducing package size for automotive applications. Therefore, well-proven packages dominate this market, for example, leaded-packages like quad-flat package (QFP) and also ball grid array (BGA), or quad-flat no-leads (QFN) packages.

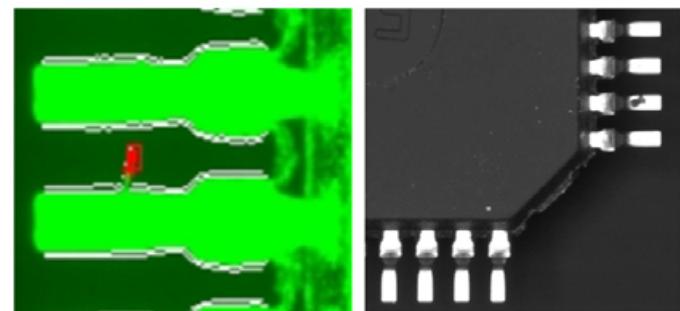
The most common package type in use today for automotive applications is the leaded-package. In the past, there was little economic incentive to focus on process control and defect traceability in the assembly lines. “Zero Defect” is changing this paradigm. A new focus on ensuring all contact points (wings for gull-wing leads) are within the dimensional tolerances will help to identify defects that create shorts or otherwise decrease the assembly quality. Each component that does not meet the tolerances will be sorted out of the production stream and will not make it to the customer. In addition to the increased inspection requirements, automotive customers are introducing additional package cleaning steps, with brush cleaning devices or CO<sub>2</sub> cleaning, to further reduce the number of failed packages that are shipped. Examples of burr and dirt-on-lead (DOL) defect images on leaded devices are in **Figure 1**. After defect detection, these parts can undergo a cleaning step to

remove the dirt from the leads and increase the yield.

As the market requirements have grown, the ICs packed inside the packages noted above have increased their memory content and clock speeds, resulting in increased complexity. For this reason, the share of BGA packages is growing faster than the leaded-components on account of the higher density of available contact points compared to gull-wing packages. Similar to the trend with leaded-packages, BGA components for automotive applications also have increased inspection requirements with tighter specifications for contact points’ (solder balls for BGA) dimensions, and newly introduced cleaning techniques at the end of the line.

Another trend is the increasing adoption of unique item level traceability (ULT), which guarantees that defects found at the end of the line are traced back to their origin. ULT allows a failure of a single IC inside a package to be traced back to the root cause of that failure at an earlier assembly step, or even at the wafer level. Reaching parts per billion reliability levels requires this kind of proactive defect reduction strategy that puts focus on all potential sources of failure.

**CSR:** How does the process control strategy at the packaging level change with the advent of system-on-chips (SoCs)/ICs in the 14nm and 10nm design rule range for automotive applications? What should the manufacturers at the packaging level do differently that they didn’t need to worry about with respect to design rules >65nm.



**Figure 1:** Examples of a) (left) burr and b) (right) dirt-on-lead (DOL) defect images.

**KLA-Tencor:** Even at the less advanced nodes, all automotive chip manufacturing process flows already contain significantly more inspection and metrology steps than found with consumer devices. These additional steps help recognize manufacturing excursions faster, improve the traceability of the source of the problem and keep non-conforming material out of the supply chain. This strategy requires automotive suppliers to focus on the wafer level and the packaged IC to find and eliminate defects at the source, as well as screen the production work in process (WIP) to prevent any defect excursions.

The process control strategies noted above have become even more stringent for design rules below 65nm. At the 1Xnm nodes, the transistor and metal layer dimensions have scaled down to such an extent that cross-talk and large on-chip interconnect parasitics (resistance, capacitance and inductance) have become significant issues. To resolve these undesirable characteristics, low-k SiO<sub>2</sub> doping is used to improve the performance of the interconnects to retain a high clock-speed, lower cross talk, reduce time delays and lower power consumption. However, because low-k dielectric material is more brittle than conventional oxides, there is an

increased risk of die cracking during the wafer dicing step (see **Figure 2**).

As a consequence of the increased risk of die cracking during the dicing step, manufacturers for the automotive industry are facing an increased need to add die crack inspection at the final die sorting step to guarantee cracked devices are removed from the line. The absence of e-test after dicing puts a priority on detection of these killer defect types through inspection techniques. Many of the side wall cracks capable of impacting the active area and destroying the device are also invisible to standard optical inspection. Infrared radiation (IR)-based technologies are currently being investigated to close the inspection gap. It is already demonstrated that an inspection with an IR camera directly above the device on the wafer does not provide the required sensitivity to detect the small side wall cracks. An innovative IR-based inspection solution has been developed to maintain sensitivity to all sides of the device. This new technology has already proven to provide zero slip-through in high-volume production. The key challenge is to maintain the required sensitivity at high-volume manufacturing (HVM) speeds of >8K dies/hour to guarantee an acceptable cost of ownership. Only limited suppliers are currently capable of offering zero underkill crack inspection at HVM-worthy speeds.

Many other changes in process control strategies can be found in wafer-level packaging. As 14nm and below semiconductor front-end technologies get deployed for automotive applications such as artificial intelligence (AI) and advanced driver assistance systems (ADAS), highly advanced packaging applications will also be utilized to enable very high bandwidth. Innovative 2.5D, 3D-IC, and high-density fan-out packaging technologies will be required for the electronics systems to process very large volumes of data in real time. Shrinking chip interconnect pitch and scaling redistribution layer (RDL) dimensions drive requirements for higher resolution inspection and high-accuracy metrology at the wafer

level. Resolution of inspection and accuracy of metrology will both be pushed to sub-micron levels. These advanced packaging technologies also have many more process steps than established automotive packaging technologies, and this process complexity drives significant inline inspection and metrology to achieve yield, quality, and reliability necessary for automotive deployment.

**CSR:** How do you foresee reaching parts-per-billion (ppb) automotive quality levels as the industry continues to need to provide ICs at ever smaller design rules? Another consideration could be that as the number of ICs being incorporated into autos continues to grow — that will also impact the level of reliability needed because the greater the number of ICs in a system, the higher the probability of failure unless the reliability of each IC can be improved.

**KLA-Tencor:** As the semiconductor content in luxury vehicles grows beyond 10,000 devices, the cumulative effect of semiconductor reliability is the top issue for the industry. Semiconductors have already become the #1 failure item in car quality, with the challenges continuing to grow. The difficulty in meeting ppb quality targets cannot be overstated. Leading automotive suppliers today can reach quality levels in the 1-10ppm range on mature devices that are built on well-characterized, larger design rule processes that have been in production for many years. Making the desired orders of magnitude improvements in quality cannot be accomplished by simply massaging the margins of these processes. Rather, it will require a fundamental rethinking of quality methods, business models and capital investment.

Compounding this reliability challenge is the rapid push of more advanced design rule devices into the automotive

## Side wall cracks at 65nm technology and below

Low-k material introduced at 65nm into the redistribution layer (RDL) is brittle due to low thermo-mechanical strength (10x worse than SiO<sub>2</sub>) — causing cracks during dicing

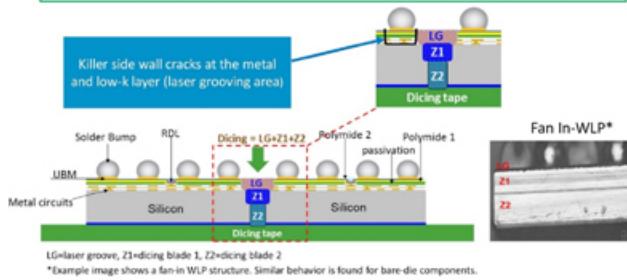


Figure 2: Side wall cracks at 65nm technology and below.

supply chain. Whether in AI chips for autonomous driving, domain controllers replacing traditional distributed electronic control units (ECUs), or advanced ADAS chips and sensors, the raw computational requirements are driving these advanced parts into cars. Car manufacturers will be faced with a significant reliability hurdle because these devices are more complex, far less mature, and difficult to test. Because reliability affects both warranty and liability, as well as the brand image of car manufacturers — and potentially the safety of their customers — process control in packaging, from wafer level to component, will increase significantly in the coming years to find and eliminate the sources of defects and screen for excursions. Manufacturers must seek every available opportunity for continuous improvement across the entirety of their manufacturing process to reach the goal.

## Biographies

Jeroen Hoet received his Executive MBA from Vlerick Business School, Belgium, his MBA from U. of Leuven, Belgium, and an MSc Engineering in Micro-electronics from Ghent U., Belgium. He is a Product Marketing Manager at KLA-Tencor; Jeroen.Hoet@kla-tencor.com

Stephen Hiebert received his BS in Mechanical Engineering from UCLA, an MS in Mechanical Engineering from Stanford U., and an MBA from UCLA Anderson School of Management. He is a Senior Director of Marketing at KLA-Tencor.

# Advanced chip-package-board co-design

By Tom Whipple, Narayanan TV [Zuken]

The proliferation of packaging designs that combine multiple chips into a single package is creating new challenges for package, printed circuit board (PCB) and integrated circuits (IC) designers. The common practice of designing the package, PCB and IC in stand-alone environments requires time-consuming manual processes that are error-prone and limit the potential for design reuse. What is needed are 3D co-design tools that integrate planning and final design implementation at the system level for PCBs, ICs, packages and mechanical enclosures. The ability to conduct system-level co-design makes it possible to optimize bump and ball placement, I/O placement and pin assignment to lower chip, package and PCB layer counts even in nontraditional structures with routing complexity in both vertical directions. The emerging IEEE 2401 design file format standard goes one step further by offering the potential to streamline the process of communicating design data with customers and partners using different electronic design automation (EDA) tools or with third-party software.

## New packaging architectures driving innovation

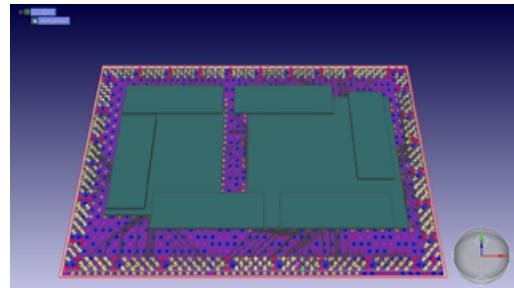
The continual increases in feature density that have driven innovation in the semiconductor industry for 50 years appear to be on the verge of slowing or coming to a halt. For example, Intel has suggested silicon transistors can only keep shrinking in accordance with Moore's Law for another five years [1]. As the potential for improvements in front-end processing slows, electronics original equipment manufacturers (OEMs) are seeking innovations in back-end processing, turning to a wide range of new packaging solutions to pack ICs ever more tightly together.

For example, package-on-package (PoP) architectures are increasingly used to

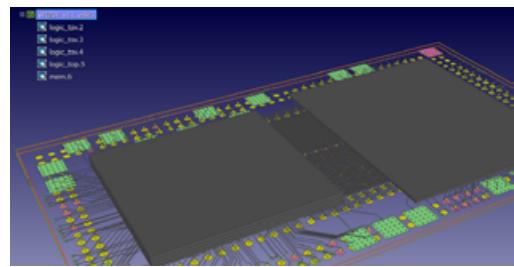
connect logic RAM ICs with short interconnects (**Figures 1, 2**). Higher density packaging methodologies such as system-in-package (SiP) integrate multiple chips into a single package, particularly in mixed digital and radio frequency applications. Even more complex packaging technologies utilize through-silicon vias (TSVs) to reduce interconnection distance in multi-chip package designs in order to increase performance and reduce power consumption. For example, fan-out wafer-level packaging (FOWLP) establishes die-to-die and die-to-ball grid array (BGA) connectivity directly through packaging redistribution layers (RDLs), eliminating the packaging substrate used in more established flip-chip (FC) and wafer-level chip-scale packages (WLCSPs). Samsung Electro-Mechanics' fan-out panel-level packaging (FoPLP) [2] places the chip on top of a panel board, eliminating the need to use PCBs for the package substrate, which reduces the cost of production.

## Challenges facing IC, PCB and package designers

The greater complexity of these and other new packaging solutions, combined with the increasing functionality of single package modules, is creating vast new challenges for not only package designers, but also IC and PCB designers who must integrate the package into their own work. Traditionally, the IC team creates the IC, the board team designs the PCB, and the package team is responsible for getting the PCB and IC teams talking to each other. The increasing functionality, tighter cost constraints, and the decreasing form factor of today's electronics products means that components need to be tightly coordinated with each other so that



**Figure 1:** A fan-out wafer-level two-ASIC package with a six-memory package on top designed using Zuken's IC package and PCB layout tool, CR-8000 Design Force.



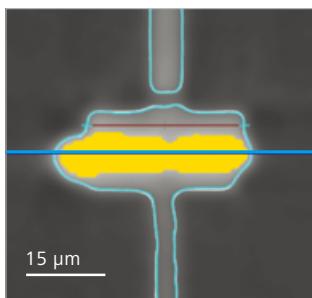
**Figure 2:** A 3D-IC stack side-by-side with a memory device in a package.

pin assignments can be optimized for small size and minimum layer count substrates.

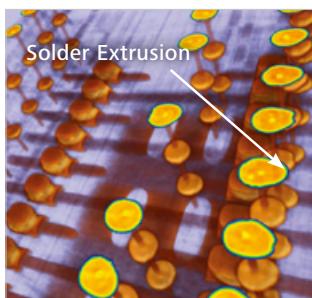
Package designers are typically responsible for determining the optimal number of packaging layers, routing the RDL on the IC side and the escape route on the PCB side. They must consider bump and ball placement, I/O placement and pin assignment to lower chip, package and PCB layer counts. This task is particularly difficult in non-traditional structures with routing complexity in both vertical directions such as PoP and SiP. With packaging density increasing at a rapid rate, packages are becoming increasingly difficult to route, which increases design time and, in some cases, has a negative impact on system performance. This raises the question of how to plan out pin assignments, component placement, escape routing, etc., for these complex designs.

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Some EDA vendors address the challenges noted above by offering feasibility or planning tools that don't generate mask-ready layouts. These tools, however, are often difficult to justify when users are already spending so much on implementation tools. It's also important to note that feasibility and planning requirements change – processes change, workflows change, roles change, etc. The use of two separate tools increases the difficulty of implementing change, especially when either the planning or implementation tool doesn't meet the new requirements. In addition, translating between feasibility tools and implementation tools is a lossy, error-prone process.

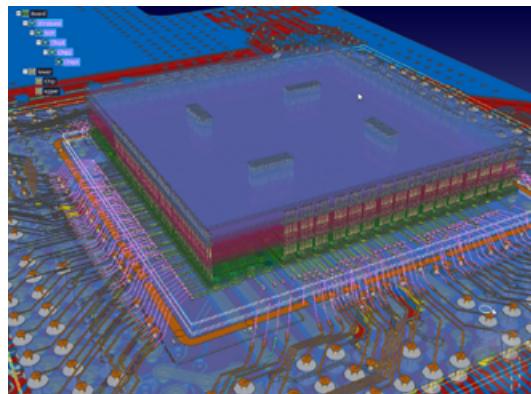
### New generation of co-design tools

A new generation of system-level 3D co-design tools addresses the challenge discussed above by providing an environment for system design that integrates planning, optimization, and implementation of all parts of the system: 1) chip-package-board; 2) physical design and analysis; 3) schematics and layout; 4) mechanical computer-aided design (MCAD) and electronic design. A hierarchical database enables each person working on the project to see his/her piece of the puzzle in context of the full product. Engineers can do system-level design, full package design, full PCB design, interposer design, and optimize the RDL routing and die bump placement for IC design in a single user interface (**Figure 3**).

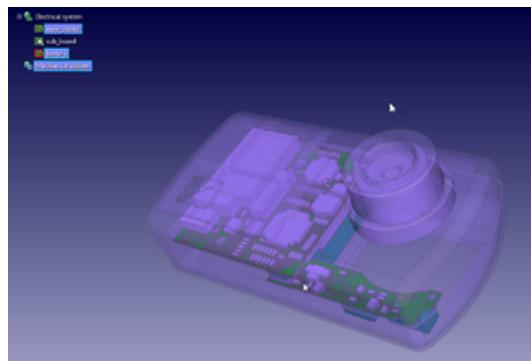
Push button integration with schematic and simulation tools ensures design data is transferred quickly and efficiently to achieve quick turnaround. The mechanical enclosure design is checkable against the final PCB, package, and IC dimensions to ensure fit and clearance (**Figure 4**). Layout versus schematic (LVS) verification software validates that a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design.

The need for the kind of co-design tools discussed above is best illustrated with the creation of a daisy chain test

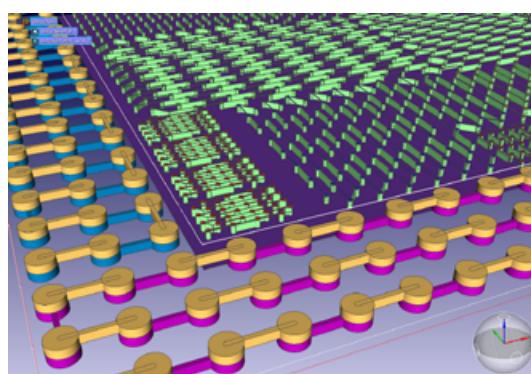
configuration between two packages and between a package and a die in a PoP design. A daisy chain test configuration is a stitching together of pins between two (or more) different components to provide a nearly zero-Ohm path between a set of pins. It is



**Figure 3:** Three-die stack with through-silicon-vias (TSVs) on an interposer in a package on a board using CR-8000 Design Force.



**Figure 4:** Three boards with 3D components and a 3D camera enclosure designed using CR-8000 Design Force.



**Figure 5:** 3D view of daisy chains across a chip-package and a PoP chip designed using CR-8000 Design Force.

used for a variety of tests to validate and improve the assembly process. These can include testing for voids,

characterizing solder bumps, measuring coefficient of thermal expansion, testing electrical continuity and electromigration reliability, among other things. **Figure 5** shows the 3D view of an example of daisy chains between two packages in a package-on-package configuration. It also shows several daisy chains between a flip-chip die and the bottom package.

Creating the full system-level netlist for this example is a tedious and error-prone process with most tools because it involves setting up proper net connections on the chip (or package) on one hand, and setting up a package on the other. This situation translates to not only maintaining the logic on the chip side and package, but also verifying the logic across the chip-package interface. This process can become particularly challenging when dealing with designs in silos and in a two-dimensional environment, wherein, while one can edit and visualize in the individual designs, visualizing the daisy chain across design boundaries is not possible. The user then has to ensure that the logic is implemented correctly from the start and that the proper verification is put in place.

However, when using a tool such as CR-8000 Design Force, which is naturally a 3D, hierarchical design system, the visualization is easily accomplished through an easy-to-use utility to create and visualize complex daisy chain configurations. The chain is created or modified by selecting a set of pins and running the command. The netlist for both sets of pins is created (or updated) and the routing for both substrates is created. The other need would be to provide a means for passing such information to other tools. For example, if one needed to pass the above daisy chain to an electrical simulation tool or a mechanical simulation tool, current process would need to rely on passing each of the individual designs separately, rather than as a system. This reinforces the need for an exchange format capable of passing 3D data across tools, which forms the focus of the next section.

## Increasing importance of data exchange

The integration of planning and implementation does not eliminate the need to interface with other tools. Even if a company focuses primarily on one vendor's EDA tools, inevitably, they have customers, third-party vendors, partners, etc., that use different sets of tools. Or the team uses one set of tools now, but in the past used a different tool. PCBs and ICs are still designed with different tools and this gap needs to be bridged. New design techniques such as FOPLP bring demands that current toolsets cannot meet. In other words, the increasing integration of EDA tools does not eliminate the need for data exchange.

Some EDA vendors have devoted minimal resources towards data exchange on account of perceived costs and risks. The primary benefits provided by the EDA vendor are in the algorithms and features of its tools. The design resources required to support data exchange take away from development of the core software. The development costs are required to support industry data exchange formats and maintenance expenses can be considerable because of frequent changes to these formats. The interpretation of data exchange formats can be difficult. For example, it's not uncommon for DEF files from one vendor to be unreadable by another vendor's tools. EDA vendors may also be concerned that if data can easily be exchanged between different tools then it will be easy for designers to move away from their tools. With users demanding the smooth flow of data between tools, however, it's clear that tools that can provide integrated chip-package-board flows along with implementation and seamless exchange of data will provide the greatest value to designers and be the most likely to succeed in the marketplace.

There are many de facto file formats that are used today to share data – spreadsheets, LEF/DEF, GDSII, ODB++, OpenAccess, etc. – but these tools are only supported for a subset of the whole design. In an ideal world we would have one standard format for all data exchange between different tool and design platforms. This format may already exist – the IEEE-2401 standard. The IEEE-2401 standard has the potential to provide all the information needed for design and simulation in much less time than

is required by current methods while being easy to implement because data is delivered in human readable, open formats such as XML and Verilog-HDL. The IEEE-2401 standard enables cross-discipline design teams to exchange system-level netlists, component information, design rules, etc., while avoiding the need to use error-prone formats such as spreadsheets. The IEEE-2401 standard format is constructed from six basic information types including Project Management (M-Format), Netlist (N-Format), Component (C-Format), Design Rule (R-Format), Geometry (G-Format) and Glossary.

## Summary

The increasing complexity and density of today's designs, combined with the proliferation of multi-chip packaging architectures has escalated the challenges involved in designing electronic products. Traditionally, three independent design processes have been required with point tools to design the chip, package and PCB. Today, an integrated chip/package/board co-design environment provides a holistic approach that makes it possible for designers working on the chip, package and board to view the complete system in their own environment and go from exploration to design implementation in a common environment. New industry standards such as IEEE-2401 go one step further by enabling the intelligent exchange of design information across the design team while making it possible to conduct signal and power integrity analysis concurrently, or interface to best-in-class simulation

and analysis tools from Ansys, Keysight, CST and Synopsys, to name a few.

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# Metal-based wafer-level and 3D-printed packaging

By Doug Sparks [\[Hanking Electronics\]](#)

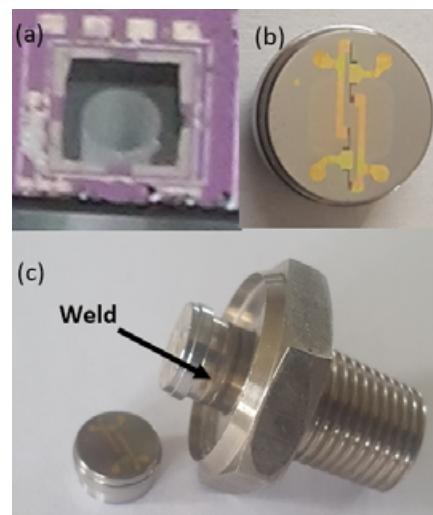
New technologies and materials are being incorporated into IC and sensor packaging each year. Wafer-level packaging (WLP) traditionally has utilized silicon, or perhaps glass substrates to form chip-scale packages (CSP). More extreme corrosive or high-temperature sensor applications as well as needs for better electromagnetic interference (EMI) shielding or perhaps cooling for high-power chips have pushed some packaging materials towards incorporating metals either in WLP and/or into the larger system-level package. This paper will discuss metal-based WLP of ICs and sensors as well as new developments in 3D-printed metal sensor, circuit and microfluidic packaging.

Adding circuits to metal substrates began in the 1980s with screen-printed hybrid technology using porcelainized steel [1]. This glass or glaze coated steel substrate material was seen as a lower cost option over alumina substrates and as a way of making large area, more complex substrate shapes and improving heat sinking for industrial applications. Thick-film piezoresistive pressure sensors were even demonstrated using coated steel substrates [2].

The first truly thin-film, IC-like device made on metal was an industrial pressure sensor. The driving force behind developing a sensor on steel was overcoming the poor fracture toughness of silicon. **Figure 1a** shows what happens to a differential silicon pressure sensor under overpressure conditions, the silicon diaphragm breaks like glass due to its low fracture toughness. Using a metal diaphragm instead of fragile silicon allows the sensor to be used in high-pressure applications without the worry of diaphragm breakage and release of the gas or liquid.

In the 1990s a “wafer” fab was constructed by Nagano Keiki [3,4], dedicated to only thin-film IC-type processing on stainless steel. The pressure sensors shown in **Figure 1b** are made using plasma-enhanced chemical

vapor deposition (PECVD) oxide, doped polysilicon and silicon nitride, as well as metal layers, all patterned with conventional photolithography techniques on stainless steel. These small steel sensor elements are first machined from rod stock, polished on one side and then fab-processed in trays. However, connected panels of the elements, more like a wafer or circuit board, with multiple sensors on a substrate, can also be used to run the metal parts through the dedicated fab [5]. After fabrication, the round sensing elements are welded to the threaded, hex nut pressure sensor package as shown in **Figure 1c**. The corrosive or hazardous liquid is only exposed to the bottom side of the stainless steel diaphragm, while the thin-film Wheatstone bridge circuit is safely located on the opposite, top steel surface. These steel sensors are still being fabricated in high volume for automotive and industrial applications. Other pressure sensor suppliers make competing products by attaching thinned single-crystal silicon strain gauges to steel diaphragms using reflowed glass and epoxy [6].



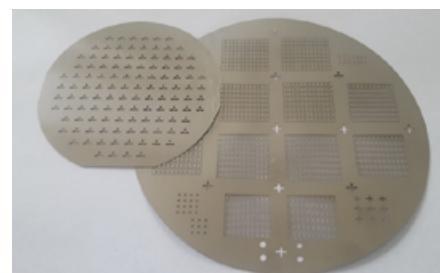
**Figure 1:** a) Ruptured silicon pressure sensor diaphragm; b) Thin-film stainless steel pressure sensor; c) Thin-film steel pressure sensor welded to the machined package with a threaded fluid connection.

Another metal MEMS technology developed in the 1990s and 2000s was LIGA, a German acronym for Lithographie, Galvanoformung, Abformung. LIGA involves the electrochemical plating of metal structures in a photoresist mold [7]. This 2D additive technology was used to grow nickel resonators for gyroscopes on CMOS wafers [8]. The CMOS integrated metal sensor was incorporated into a silicon to silicon wafer bonded stack to encapsulate the metallic sensor in a silicon CSP.

## Metal WLP

Grounded EMI shielding in the form of metal covers are often placed over silicon-based CSPs at the system board level. EMI shielding is one driving force for RF-MEMS, metal CSP applications. Metals like Kovar, stainless steel and titanium have been employed in microelectromechanical (MEMS) sensors and actuators. For over ten years, Professor McDonald's team at UCSB has developed titanium wafer fabrication processes and various devices, including metal RF-switches, using titanium wafers [9,10]. Ti fab processes such as deep reactive ion etching (DRIE), wafer-to-wafer bonding and more traditional film deposition and photolithography have been developed. The same photoresist spray coating processes that allow metal films, and hence, runners to be patterned over the 10- to 100-micron steps of a silicon MEMS cap wafer can be applied to a metal cap wafer.

**Figure 2** shows examples of metal wafers that have been patterned to form

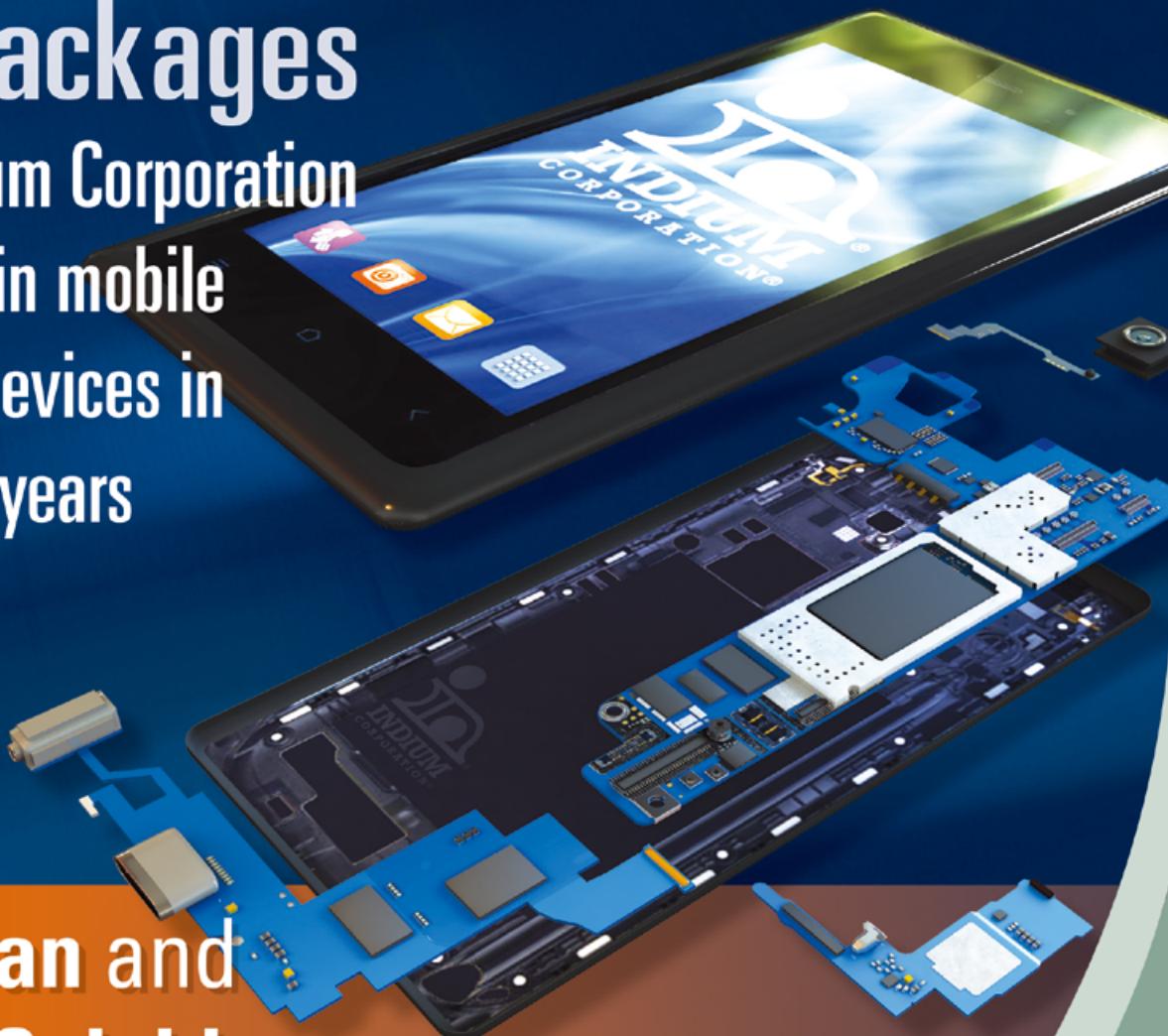


**Figure 2:** Metal wafers with patterned through via, bond pad opening, and fluid port.

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through-metal wafer vias (TMV), as well as fluid ports and bond pad openings for wire bonding of the CSP made using a metal multi-wafer stack. While many of the same wafer-to-wafer bonding methods developed for silicon wafers can, and have been applied to metal wafers, some practical limitation exists when mixing wafers of different materials in the stack. Differences in thermal coefficients of expansion (TCEs) between wafers, even when relatively small, can result in cracking or built-in stress after a higher temperature wafer bonding step. Kovar with a TCE of 5 to 6 ppm/ $^{\circ}\text{C}$  is often used with silicon (TCE 2.6 ppm/ $^{\circ}\text{C}$ ) as a hermetic package metal. However, anodically bonding large diameter Kovar wafers to borofloat glass (TCE 3 ppm/ $^{\circ}\text{C}$ ) can result in wafer bowing, and even cracking across the wafer-to-wafer bond interface, shearing off the majority of the glass wafer, as shown in **Figure 3**. Just a thin layer of glass is left, anodically bonded to the patterned metal wafer after this TCE related fracture. Like **Figure 1a**, **Figure 3** illustrates the impact of poor fracture toughness (glass and silicon) versus high-fracture toughness metals with regard to cracking and fracture at the wafer level during packaging. Care must be taken



**Figure 3:** Shear fracture of the glass wafer at the anodically-bonded metal to glass wafer interface.

when selecting the wafer bonding method when using metal substrates. Softer bonding materials like silicone or solder may be preferred for many applications where wafer TCEs don't closely match each other.

WLP using one or more metal wafers offers improved heat sinking of the CSP. For fluidic applications such as pressure sensors, active chip cooling and microfluidic sensors, a metal chip adds the ability to weld the CSP directly to metal tubing, as shown in **Figure 4**. In these applications silicon chips often use epoxy or silicone chip attachment material that degrades over time when used in liquid microfluidic applications.

On account of thermal shock cracking, welding is not an option for silicon, so the ability to weld a small diameter stainless tube or tubes to a metal chip offers some advantages in fluidic CSP applications.

CMOS wafer fab operators will not allow transition metals like those used in alloys such as stainless steel and Kovar, to be processed in their equipment due to potential contamination of silicon CMOS/BiCMOS wafers. Transition metals in silicon can cause high PN junction leakage currents, emitter-collector pipes, degraded minority carrier lifetimes and gate oxide, and are known to diffuse rapidly through silicon wafers [11]. Many traditional MEMS foundries, which do not process CMOS circuit wafers, will allow the processing of sodium containing borofloat glass and other substrates like titanium wafers. This substrate flexibility opens up the possibility of metal WLP devices. Metal wafers of 100mm, 150mm and 200mm are being processed in some MEMS fabs.

### 3D-printed metal packages

WLP for ICs and MEMS opens up many unique Internet of Things (IoT) applications. To avoid some of the complications of traditional WLP manufacturing like DRIE cavity, via etching and obtaining wafer-to-wafer bonded hermetic seals [12], one alternative that is being explored is using the 3D printing of metals to form the complex 3D structures found in many MEMS devices and packages. 3D printing can eliminate the need for CSP wafer bonding or welding in system-level packages. This new fabrication method can also directly merge the sensing elements with the larger system-level package using a single printing step.

Excellent metal electrical and thermal conductors like copper and aluminum, as well as corrosion resistant metals like stainless steel alloys and titanium can be 3D printed. Various types of 3D metal printing are available and include selective



**Figure 4:** Stainless steel tube welded to a metal microfluidic CSP.

laser melting (SLM) or direct metal laser sintering (DMLS) that use metal powder as a starting material. Electron-beam melting (EBM) is also used for 3D printing in which the raw material can be either metal powder, filaments, rod, or wire. These printing methods can be done under vacuum to reduce porosity, oxidation and other defects. Minimum printed feature sizes can range from 50 to 200 microns depending on the particle and beam size. The printing method and particle size also controls the surface roughness of the finished metal product. Post-print processing is often required to produce a polished finish.

3D metal printing has several advantages over traditional machining and wafer fabrication. It is often dramatically faster than processing wafers and the combination of machining and assembly. Material scrap is lower because it is a direct print additive process versus a subtractive machining or etching process. By printing a single piece instead of using assembly steps, the manufacturing process can be simplified. Metal and plastic 3D printing is ideal for fast prototyping and low-volume, high-cost products, or for the replacement of legacy products.

**Figure 5** shows a stainless steel, 3D-printed fiber optic pressure sensor that combines a reflective metal diaphragm along with the male threaded pipe fitting and hex nut portion of the final package into a single piece. 3D printing avoids

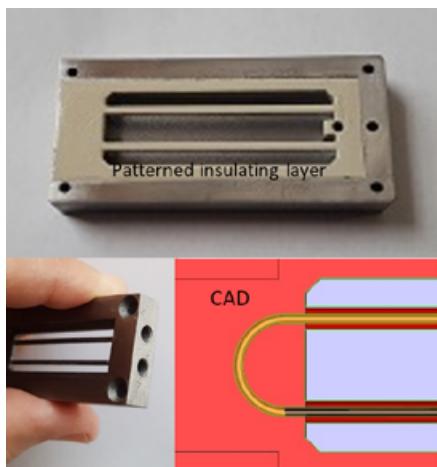


**Figure 5:** 3D-printed stainless steel optical pressure sensor prototype with a threaded metal package fluid port.

the welding step shown in **Figure 1c** for pressure sensors. The reflective finish of the stainless diaphragm requires polishing after 3D printing. This same smooth diaphragm surface is ideal for CVD dielectric deposition and patterning

of the metal, polysilicon and passivation layers shown in **Figure 1b**. Piezoresistive Wheatstone bridge strain gauges and pressure sensors can be made with 3D-printed stainless steel [13].

Industrial resonant Coriolis mass flow sensors are traditionally made from stainless steel or titanium pipe or tubing and require multiple welding steps to fully assemble the final product. 3D printing offers a method of making stainless or titanium tube-based sensors and packaging a wide array of micro size (mm long tubes) or larger macro size (meters long tubes) resonating flow sensors. **Figure 6** shows a small titanium 3D-printed mass flow and density sensor that combines the two resonating tubes with the package frame and M-5 female threaded fluid fittings (bottom left) in a single piece. 3D printing allows for buried channels [13] as shown in the CAD drawing (bottom right) in **Figure 6**. This type of embedded structure cannot be made using machining and would require photolithography, etching and wafer-to-wafer bonding steps if formed using MEMS substrates. The top surface of the sensor and package of this prototype is flat and polished after 3D printing to enable the deposition and patterning of circuit layers.



**Figure 6:** (Top) Single-piece, 3D-printed titanium resonant flow/density sensor and fluidic package. (Bottom right) CAD drawing of the embedded U channel.

The materials used for 3D printing are only limited by what metal or alloy can be either powdered or formed into wire. This opens up niche, low-volume industrial and aerospace applications that are currently too expensive to fabricate, or that use metals too hard to machine. With proper CAD design and processing to avoid warpage, 3D

printing can be used to fabricate panels and even complex metal wafers with cavities, vias, embedded channels, and other features of a variety of depths and sizes that cannot be practically fabricated with silicon or glass wafers. Post-3D metal print polishing, film deposition and patterning in a MEMS fab can enhance the utility of this new metal wafer fabrication process. Current 3D metal printing is limited to features with 50- to 200-micron resolution, which is comparable to traditional silicon cavities for MEMS capping wafers. Si DRIE features are much finer than those that can be 3D printed, however, just as thin-film layers can be deposited onto a planar, polished metal surface, it is possible to pattern and etch metals like titanium with MEMS fab equipment. The cost of 3D-printed prototypes, which can be fabricated in days, is now comparable to low-volume silicon MEMS prototypes that require a mask set and more than a month of wafer processing time. 3D printed MEMS wafers with more complex geometries and thin-film electrical components is a future possibility and would open up some new material opportunities in wafer-level packaging.

## Summary

Thin-film circuits, as well as many sensing and actuating elements, can be applied to and made from metal substrates, which enable metal-based CSPs. Patterned thin films like CVD silicon dioxide, silicon nitride, polysilicon, aluminum, gold and other metals have all been developed and used in production on metals like stainless steel and titanium. WLP using metal wafers in MEMS fabs is now an option for applications requiring improved heat sinking, EMI protection, as well as corrosion-resistant microfluidic materials. 3D metal printing is also under development for combining multiple sensing and packaging components together into a single piece to save assembly time, reduce material costs, and offer new packaging capabilities.

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## Biography

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# Temporary bonding for high-temperature processing of thin glass

By Robert A. Bellman, Prantik Mazumder, Robert G. Manley, Kaveh Adib, Shiwen Liu, Leena Sahoo [Corning Research and Development Corporation]

**T**hin glass substrates offer low dielectric constant and high-temperature process capability for faster, thinner packages, but handling is challenging on account of the flexibility of the substrate. Polymeric and tape wafer bonding solutions are available, but only for low-temperature processes. This paper describes Advanced Lift-off Technology (ALOT), a temporary wafer bonding method for thin glass that permits processing up to 580°C. Fluorocarbon plasmas are shown to modify the surface energetics of a glass continually from that of a clean “glass-like” surface (high surface energy) to that of a “Teflon™-like” surface (low surface energy) permitting controllable van der Waals bonding between a thin glass and a glass carrier at room temperature. This modification can withstand the vacuum, thermal, wet-processing steps of back-end-of-line (BEOL) processing. However, the bond energy between the pair remains low enough after the thermal processing steps that render the pair fully detachable.

## Introduction

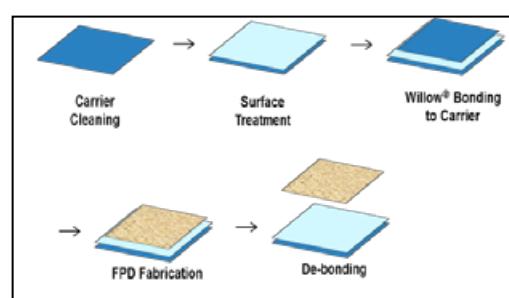
Ultra-thin glass offers the promise of cheaper devices using roll-to-roll processing, and the potential to make thinner, lighter, more flexible and durable displays. However, the technology, equipment, and processes required for roll-to-roll processing of high quality displays are not yet fully developed. Because panel makers have already heavily invested in toolsets to process large sheets of glass, laminating flexible thin glass to a glass carrier and making

display devices by a sheet-to-sheet process offers a shorter term solution to develop the value proposition of thinner, lighter, and more flexible displays. While displays have been demonstrated on polymer sheets such as polyethylene naphthalate (PEN) laminated to a glass-glass carrier, the upper temperature limit (usually less than 200°C) of the PEN limits the process capability and in turn, device quality, not to mention the high permeability of the polymer substrate leading to environmental degradation of organic light-emitting diode (OLED) devices. There is, therefore, much value in inventing a material/process combination that would allow temporary bonding of thin glass to a rigid, transparent and high-temperature glass carrier substrate, such as glass, and de-bond the thin glass from the glass carrier after the flat panel display (FPD) processing steps (**Figure 1**). This realization nucleated ALOT technology, which could be summarized as the following problem statement: a) the thin glass must bond spontaneously with a glass carrier at room temperature with sufficient bond or adhesion energy; b) the bonded pair must withstand the thermal, chemical, vacuum and wet processing steps of FPD fabrication; c) the outgassing and/or contamination during the

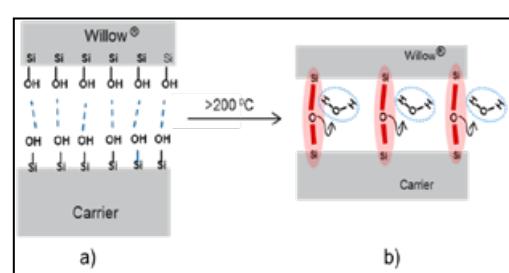
thermal processing should be as low as possible; and d) at the end of the high-temperature steps, one should be able to separate the thin glass from the glass carrier with relative ease.

## Van der Waals bonding of glass

It is well-known that clean and hydroxylated surfaces of glass are replete with silanol or hydroxyl groups (number density anywhere between 2-5/nm<sup>2</sup> [1]). These hydroxyl groups are highly polar in nature – the glass surface is essentially an array of permanent dipoles sticking out of the surface – twisting, turning, and vibrating on account of thermal energy. When clean and smooth ( $R_a < 0.6\text{nm}$ ) glass surfaces are brought into optical contact, the surfaces spontaneously bond (**Figure 2a**). The glass surfaces adhere either by direct hydrogen bonding between the opposing silanol groups, or by mediation through one or two layers of molecular water absorbed on the silanol groups [1]. Either way, these polar interactions lead to a polar bonding energy  $\sim 150\text{mJ/m}^2$ . The attractive force between permanent dipoles is called Keesom force, named after W.H. Keesom who worked out the theoretical details and is one of the three types of van der Waals forces [2]. In addition, all materials have fluctuating instantaneous dipoles distributed in the bulk due to the continuous motion of



**Figure 1:** Schematic showing the process path of bonding thin glass to glass-glass carrier, device fabrication, and de-bonding.



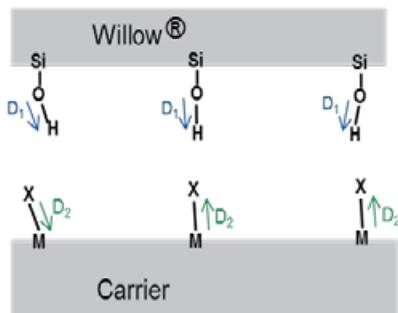
**Figure 2:** a) Van der Waals bonding between a pair of hydroxylated glass substrates, and b) Covalent bonding between the pair due to condensation reaction at high temperature.

the electrons around the protons. The interaction between the fluctuating dipoles of the thin glass and the glass carrier also lead to an attractive energy, which is called the London dispersion energy, named after Fritz London [3]. The London dispersion force is the most ubiquitous type of van der Waals force and its value is generally of  $\sim 10\text{-}50\text{mJ/m}^2$  depending on the nature of the bonding pairs. Overall, total bond energy of  $\sim 200\text{mJ/m}^2$  is achievable in this so-called “water bonded” thin glass-glass carrier pair, which might be sufficient to support the FPD processing. However, at high temperatures, typically above  $200^\circ\text{C}$ , the silanol groups of thin glass and glass carrier react to each other via the silanol condensation reaction:



that leads to covalent Si-O-Si bonding between the thin glass and the glass carrier as shown in **Figure 2b**. Now the bond energy is greater than  $1000\text{mJ/m}^2$  rendering the pair permanently bonded — they are no longer separable.

We realized that special surface treatment was necessary for achieving high van der Waals bonding between the thin glass and glass carrier at room temperature, yet preventing the covalent bond formation at high temperature. The basic physics/chemistry of the challenge was thus formulated as: a) invent a material/process system to replace the silanol groups of glass carrier with other polar groups, say M-X as shown in **Figure 3**. The polar groups must have high enough dipole moments so that the bond energy between the thin glass and glass carrier at room temperature is  $\sim 200\text{-}300\text{mJ/m}^2$ ; b) However, at high temperature, the M-X groups must



**Figure 3:** Schematic of the overall ALOT approach for temporary bonding/de-bonding.

not significantly react with the silanol groups of thin glass leading to strong covalent bonds between the pair; and c) the surface groups M-X should not significantly outgas during the high-temperature thermal processes.

## Results and discussion

The ALOT process and its surface chemistry are discussed in the sections below.

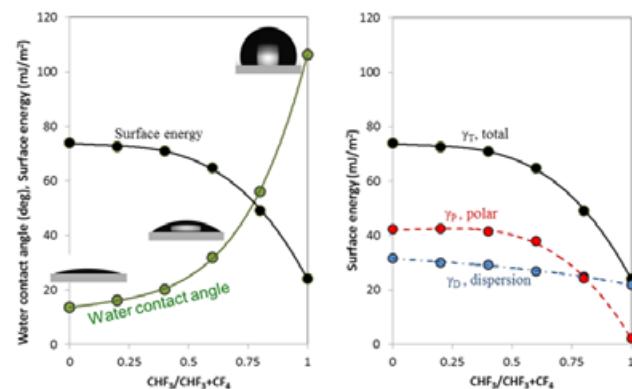
**ALOT process.** The ALOT process involves treating a clean hydroxylated glass carrier surface in low-pressure plasma containing  $\text{CHF}_3$  (or  $\text{C}_4\text{F}_8$ ) and  $\text{CF}_4$  gases (the treatment could also be done on the carrier, thin glass, or on both substrates). The  $\text{CHF}_3$  gas acts as a polymerizing agent and deposits organic fluorocarbon species on the glass carrier while  $\text{CF}_4$  acts as an etchant and tends to etch away both glass and the organic polymer deposited by  $\text{CHF}_3$ . There is, thus, a natural tension between the effects of these two gases on the glass surface chemistry and by changing the relative ratio of the gases, one can modulate the wettability and the surface energy of the treated glass surface. For example, in **Figure 4a**, we plot the water contact angle on the glass-glass carrier and the surface energy of the glass-glass carrier as a function of the  $\text{CHF}_3$  and

$\text{CF}_4$  gas ratio. The surface energy and the polar and dispersion components are measured by fitting the Wu model [4] of solid-liquid interfacial energy to three contact angles of three test liquids: water, diiodomethane, and hexadecane. With only  $\text{CF}_4$  treatment ( $\text{CHF}_3/\text{CHF}_3+\text{CF}_4 = 0$ ), which is the etchant gas, the surface becomes highly hydrophilic as shown by the low water contact angle,  $\sim 10\text{-}12^\circ$ . The corresponding surface energy is very high,  $\gamma_T > 75\text{mJ/m}^2$ , which is close to that of clean glass. On the other hand, when the glass surface is treated with only  $\text{CHF}_3$  ( $\text{CHF}_3/\text{CHF}_3+\text{CF}_4 = 1$ ),

which is the polymerizing agent, the surface becomes highly hydrophobic as shown by the high water contact angle,  $\sim 110^\circ$ . The corresponding surface energy is very low,  $\gamma_T \sim 20\text{mJ/m}^2$ , which is similar to Teflon™ — one of the lowest surface energy materials. In between the two extremes, by changing the gas ratio, we could tune the surface energy and the wettability of the glass substrate on a continuum from a high-energy, clean, “glass-like” surface to a low-energy “Teflon™-like” surface. In **Figure 4b**, we take a closer look at the surface energetics. The total surface energy could be separated into two additive components: the polar and the dispersion components [3,4].

$$\gamma_T = \gamma_P + \gamma_D \quad (2)$$

The dispersion component,  $\gamma_D$ , remains fairly constant between  $\sim 20\text{-}30\text{mJ/m}^2$  due to the fact that the



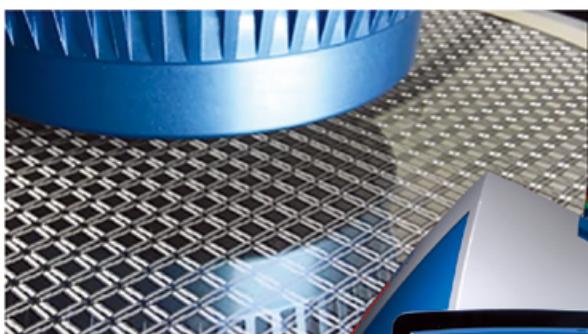
**Figure 4:** Wettability and surface energy modulation of a glass surface as a function of the gas ratio: a) Water contact angle and total surface energy vs. gas ratio, and b) Total surface energy and polar (red) and dispersion (blue) components as a function of the gas ratio.

dispersion interaction is mostly a bulk phenomenon between instantaneous dipoles. On the other hand, the polar component,  $\gamma_P$ , could be varied from  $40\text{mJ/m}^2$  to  $0\text{mJ/m}^2$  by varying the  $\text{CHF}_3/\text{CHF}_3+\text{CF}_4$  ratio, which vindicates that we are mainly affecting the surface of the glass carrier glass and especially its surface polarity.

**Surface chemistry of ALOT.** We now discuss our present state of understanding of how the surface energetics is modulated by the ALOT process. We have analyzed the surface composition of untreated and ALOT treated Corning® Eagle XG® carrier

# XM8000

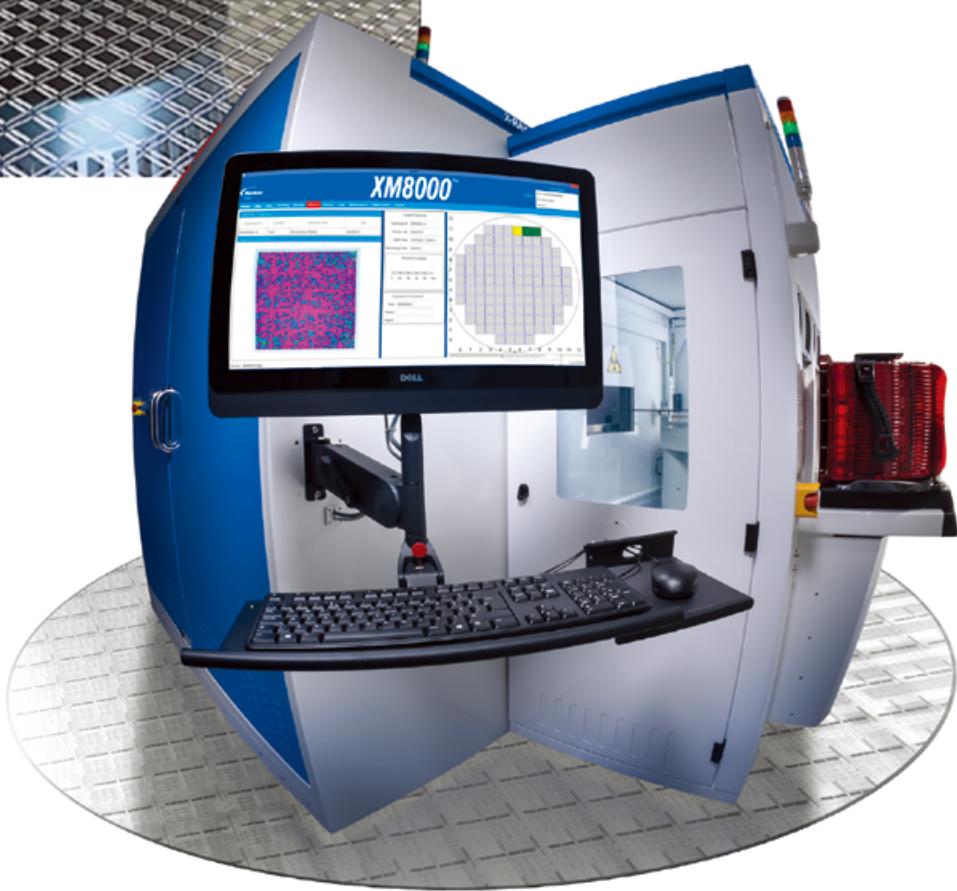
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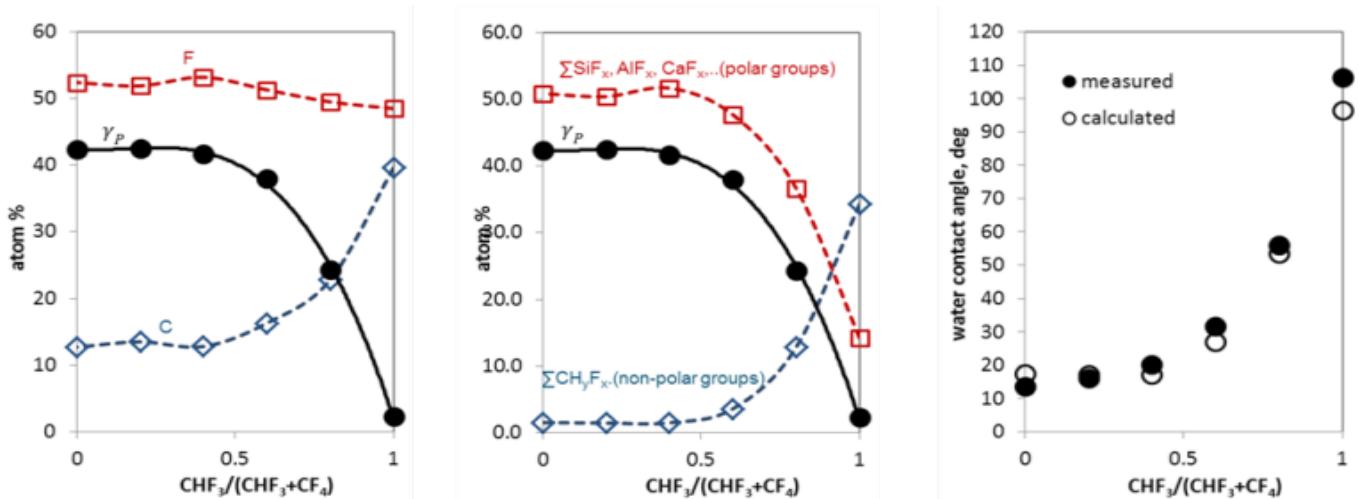


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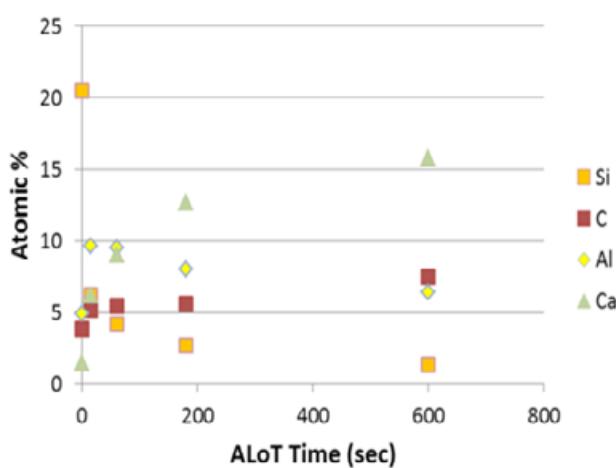


**Figure 5:** Effect of ALot treatment on the surface composition of alkaline earth alumino-silicate carrier glass: a) Polar component of surface energy, fluorine and carbon concentration of surface as a function of the gas ratio; and b) Polar component of surface energy, polar metal-fluorides and non-polar fluorocarbon composition of the surface as a function of the gas ratio; and c) Comparison of the measured water contact angle with the calculated water contact angle based on XPS measurement.

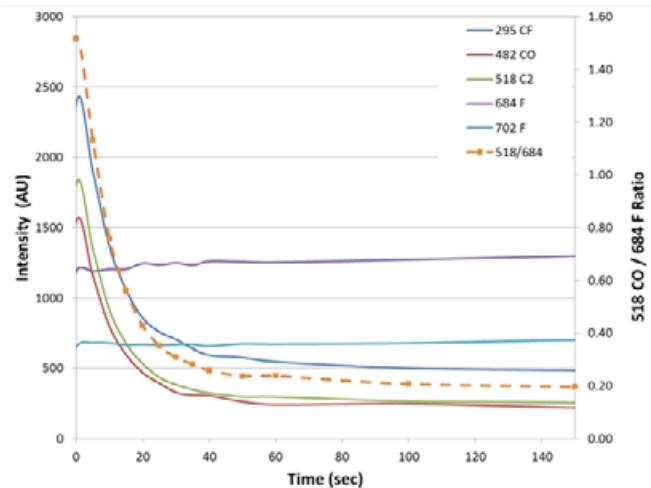
glass as a function of the treatment conditions. This is a fusion drawn alkaline earth alumino-silicate glass well-suited to glass bonding because of its low surface roughness  $<0.3\text{nm}$  Rq. While we have employed various techniques, such as X-ray photoelectron spectroscopy (XPS), Fourier transform infrared spectroscopy (FTIR) and secondary ion mass spectrometry (SIMS), here we discuss only the XPS data. In **Figure 5a**, we plot the concentration of fluorine and carbon incorporated on the glass-glass carrier surface as a function of the  $\text{CHF}_3/\text{CHF}_3+\text{CF}_4$  gas ratio. We found that the fluorine concentration of the surface remains fairly constant while the

amount of carbon incorporated in the glass surface increases with increasing  $\text{CHF}_3$  content in the plasma gas – not a surprising fact as  $\text{CHF}_3$  is the polymerizing agent. We also used XPS fine structure to look at the speciation of the carbon and fluorine and found that fluorine is essentially partitioned into two types of groups: the polar metal-fluoride groups (such as  $\text{Al}-\text{F}_x$ ,  $\text{Ca}-\text{F}_x$ ,  $\text{Si}-\text{F}_x$ , ...) and the non-polar fluorocarbon groups (such as,  $\text{CF}$ ,  $\text{CF}_3$ ,  $\text{CH}_x\text{F}_y$ ...), as shown in **Figure 5b**. As we transition from all- $\text{CF}_4$  to all- $\text{CHF}_3$  gas composition in the plasma chamber, the polar metal fluoride concentration decreases and the non-polar fluorocarbon concentration increases

all the while maintaining a constant amount of total fluorine concentration on the surface. Interestingly enough, the shape of the polar metal-fluoride curve (obtained via XPS) is almost the same as the shape of the polar surface energy curve (obtained via contact angle measurement). The agreement between the different measurement techniques confirms the mechanistic understanding that by changing the relative concentrations of polar and non-polar surface groups we manage to change the surface energy and its wettability. Yet another vindication of this mechanism is found in the contact angle behavior on the ALot-treated surface. Using the relative



**Figure 6:** Plot of surface composition of alkaline earth alumino-silicate carrier glass as measured by XPS vs. ALot process time.



**Figure 7:** Plot of optical emission intensity and 518nm/684nm peak ratio vs. ALot process time for  $\text{CF}_4$  etch of alkaline earth alumino-silicate carrier glass showing end point behavior similar to  $\text{SiO}_2/\text{Si}$ .

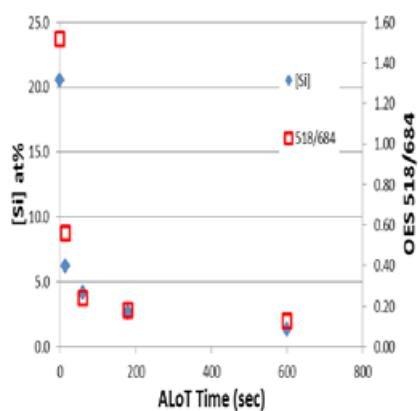
fractions of polar metal-fluorides and the non-polar fluorocarbons measured by XPS, we can approximately calculate the water contact angle on the chemically non-homogeneous surface as [5]:

$$\cos\theta = x \cos\theta_1 + (1 - x) \cos\theta_2 \quad (3)$$

where  $\theta$  is the water contact angle on the non-homogeneous surface,  $x$  is the area-fraction of the metal-fluorides,  $\theta_1$  is the water contact angle on only metal-fluoride, and  $\theta_2$  is the water contact angle on only fluorocarbons. Using,  $\theta_1 \sim 0^\circ$  and  $\theta_2 \sim 110^\circ$ , the water contact angle on the ALOT-treated surface is calculated as a function of the  $\text{CHF}_3/\text{CHF}_3+\text{CF}_4$  ratio and is compared with the measured water contact angle in **Figure 5c**. The reasonably good agreement between them, again, supports the physical mechanism of surface energy modulation via tuning the relative ratio of metal fluorides and fluorocarbons.

In a nutshell: when the alkaline earth alumino-silicate glass is treated with only- $\text{CF}_4$ , the surface is mostly made of metal fluorides, which are highly polar — there is very little fluorocarbon species deposited on the surface. As a result, the surface energy and hydrophilicity are high. On the other hand, when only- $\text{CHF}_3$  is used, the glass surface is coated with a Teflon™-like continuous fluorocarbon film, not much unlike non-stick frying pans found in household kitchens — the surface energy is low, and hydrophobicity is high.

The ALOT process was further explored by comparing the surface composition as measured by XPS,



**Figure 8:** Plot of silicon surface concentration and 518nm/684nm peak ratio vs. ALOT process time.

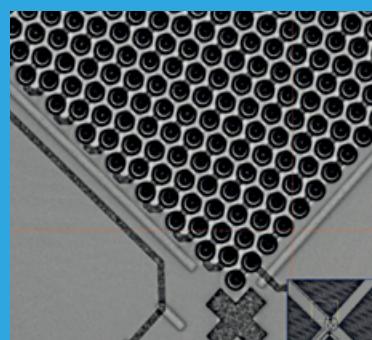
optical emission spectroscopy (OES) of the fluorocarbon plasma, and roughness as measured by atomic force microscopy (AFM) on ALOT-treated alkaline earth alumino-silicate carrier glass as a function of process time. Because a high surface energy is of most interest for strong self-propagating van der Waals bonding, we considered the case of only  $\text{CF}_4$  treatment ( $\text{CHF}_3/\text{CHF}_3+\text{CF}_4 = 0$ ). **Figure 6** shows the surface concentration of silicon, carbon, aluminum, and calcium as a function of  $\text{CF}_4$  plasma treatment time. Concentration of silicon (and boron) is observed to fall quickly with process time, while concentration of alumina, alkaline earths, and carbon increases. Therefore, the ALOT process begins with etching that removes the silicon (and boron), which have volatile metal

$\text{CHF}_3+\text{CF}_4 = 0$ ). **Figure 6** shows the surface concentration of silicon, carbon, aluminum, and calcium as a function of  $\text{CF}_4$  plasma treatment time. Concentration of silicon (and boron) is observed to fall quickly with process time, while concentration of alumina, alkaline earths, and carbon increases. Therefore, the ALOT process begins with etching that removes the silicon (and boron), which have volatile metal



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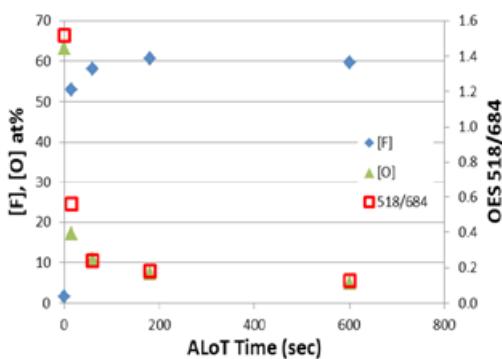
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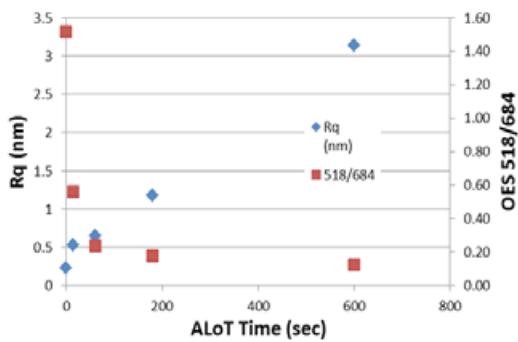
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**Figure 9:** Plot of fluorine and oxygen surface concentration and 518nm/684nm peak ratio vs. ALOT process time showing that OES end point corresponds to silicon depletion and fluorine enrichment of the surface.



**Figure 10:** Plot of surface roughness  $R_q$  ( $\text{\AA}$ ) and 518nm/684nm peak ratio vs. ALOT process time showing an inverse relationship.

fluorides, while enriching the surface in alumina and alkaline earths, which do not form volatile metal fluorides. Carbon concentration increases due to polymer formation after consumption of the etchable species.

The optical emission of  $\text{CF}_4$  plasma treatment of alkaline earth aluminosilicate glass surface as a function of process time resembles that of  $\text{SiO}_2$  on silicon (Figure 7). A clear end point signature is observed by comparing the ratio of a carbon-containing peak, such as a  $\text{C}_2$  at 518nm or CO at 482nm to a strong fluorine emission, such as 684nm. Comparing the silicon concentration as measured by XPS to the OES 518nm/684nm peak intensity ratio as a function of ALOT process time, it is seen that the OES ratio mirrors the silicon surface composition (Figure 8). The OES spectra, therefore, can be used to end point depletion of the  $\text{SiO}_2$  from the alkaline earth aluminosilicate glass surface in a manner similar to end-

pointing a  $\text{SiO}_2$  during a silicon etch process. Furthermore, it is seen that the oxygen depletes with the OES 518nm/684nm ratio as not only is the  $\text{SiO}_2$  etched from the surface, but also the alumina and alkaline earth oxides are fluorinated (Figure 9). This leads to an increase in fluorine concentration, which is inversely related to the oxygen concentration.

Comparing the roughness as measured by AFM to the OES 518nm/684nm ratio as a function of ALOT process time, one observes that roughness increases as the OES ratio decreases (Figure 10). Surface accumulation of the non-volatile metal fluorides as the silicon and boron are removed from the glass surface during the etch process leads to micro-masking, which causes increasing roughness with surface treatment time.

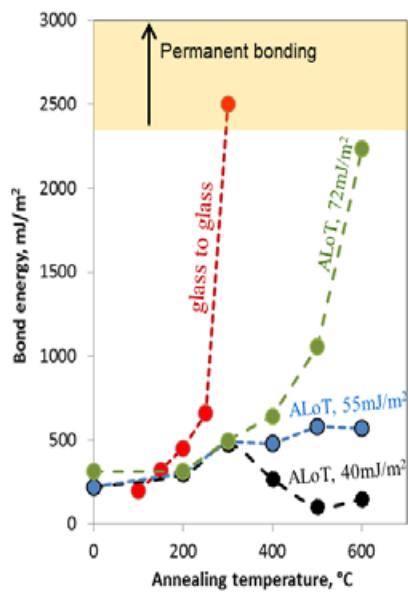
The effects of the etch component ALOT surface treatment on alkaline earth alumino-silicate carrier

glass are depletion of silicon and boron from the glass surface while converting the aluminum, calcium, magnesium, etc., to high surface energy metal fluorides. The polymer forming gas creates a partial surface coverage with polymer, which ranges from a high surface concentration of perfluorinated polymers when  $\text{CHF}_3/(\text{CHF}_3+\text{CF}_4)$  approaches unity, to a low surface concentration of hydrocarbon polymers when  $\text{CHF}_3/(\text{CHF}_3+\text{CF}_4)$  approaches zero. Rapid self-propagating van der Waals bonding is observed when the concentration of metal fluorides is high and coverage of polymer low, providing the required high polar surface energy.

### Compatibility with device fabrication

Now we look at the bond/debond performance of ALOT-bonded fusion formed thin glass-fusion-drawn glass carrier pair (Corning<sup>®</sup>,

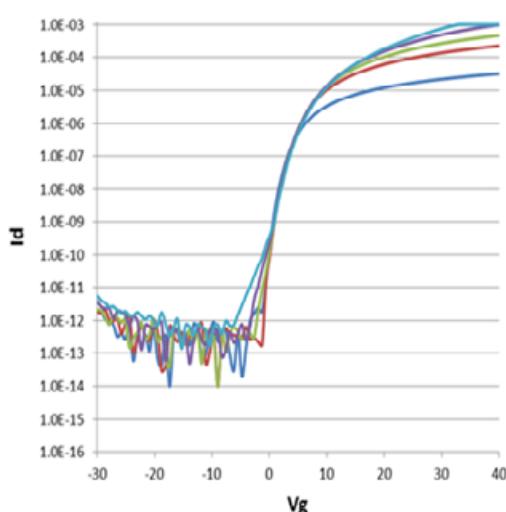
Willow<sup>®</sup>, and Eagle XG<sup>®</sup>). Bond energy (BE) measurements were accomplished using the wedge test method [6]. Bubble or blister area was evaluated using an optical scanner and a macro written in Image J. The bond energy and blister area of the thin glass ALOT bonded to a glass carrier were unchanged after wet or vacuum processing. In Figure 5a, we plot the bond energy as a function of annealing temperature for “water bonded” thin glass to glass carrier without ALOT treatment (marked as “glass on glass” in Figure 11), and for thin glass bonded to an ALOT-treated glass carrier corresponding



**Figure 11:** Bond energy vs. annealing temperature for thin glass bonded to ALOT-treated alkaline earth aluminosilicate carrier glass with ALOT compositions with surface energy ranging from 40 to 72mJ/m<sup>2</sup>.

to three initial surface energies (40mJ/m<sup>2</sup>, 55mJ/m<sup>2</sup>, 72mJ/m<sup>2</sup>). The bond energy of the untreated glass to glass pair increases exponentially after 200°C rendering the pair permanently bonded due to covalent bonding. On the other hand, the bond energy of thin glass and the ALOT-treated glass carrier pair remain fairly constant at a moderate value up to 400°C irrespective of the initial surface energy of the glass carrier.

ALOT surface treatment renders the thin glass-glass carrier pair debondable after a:Si or IGZO TFT

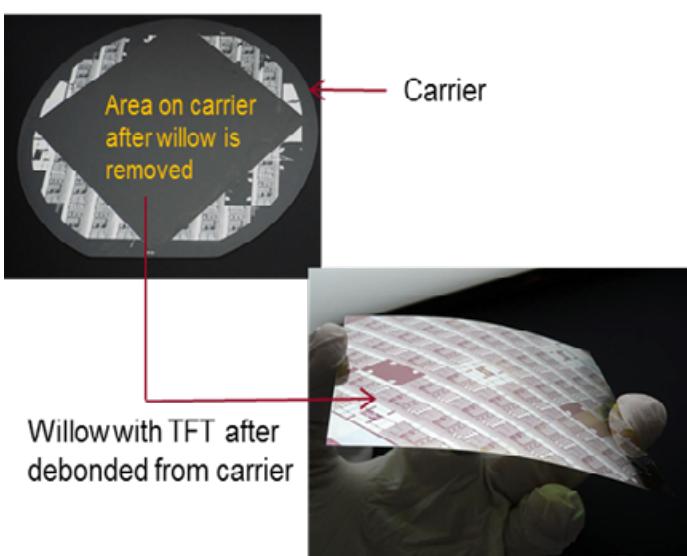


**Figure 12:** Drain current vs. gate voltage for an array of bottom gate IGZO TFTs with a  $75 \times 10\mu\text{m}$  channel.

processing, which experiences a maximum temperature excursion of  $\sim 350\text{-}400^\circ\text{C}$ . **Figure 12** shows the I-V curves for an array of bottom gate IGZO thin-film transistors (TFTs)

fabricated on ALOT-bonded thin glass and successfully de-bonded. Linear mobility was comparable to arrays deposited directly on alkaline earth alumino-silicate carrier glass,

averaging  $7.6\text{ cm}^2/\text{Vs}$ . **Figure 13** shows a TFT array on thin glass and the carrier wafer from which the thin glass was mechanically de-bonded after fabrication.



**Figure 13:** IGZO TFT array on flexible thin glass after debonding from the alkaline earth aluminosilicate carrier wafer.

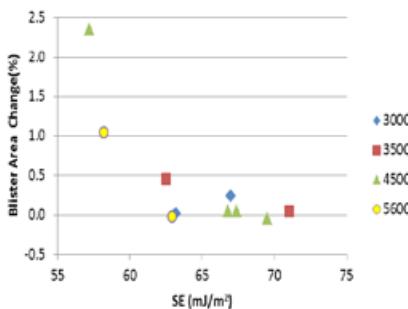
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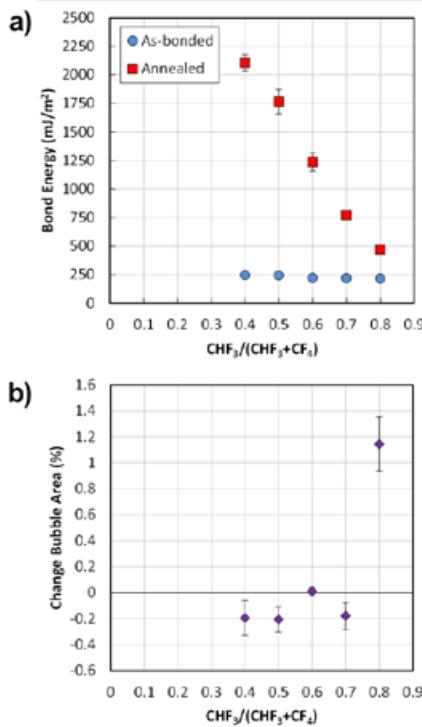
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**Figure 14:** Change in blister area vs. surface energy of ALOT treatment for thin glass bonded to alkaline earth aluminosilicate carrier glass as a function of annealing temperature.



**Figure 15:** a) Bond energy and b) change in bubble area vs.  $\text{CHF}_3/(\text{CHF}_3+\text{CF}_4)$  gas ratio in ALOT treatment after a 580°C thermal process showing the trade-off between lowering the final bond energy vs. bubble formation.

Achieving the optimal bond/de-bond performance compatible with higher temperature processes, such as low-temperature polysilicon (LTPS) (at a temperature as high as 600°C), is more challenging. The bond energy at temperatures much higher than 400°C can increase significantly for high surface energy ALOT treatment (e.g., 72mJ/m<sup>2</sup> sample). While lower surface energy ALOT treatment (high initial fluorocarbon coverage) would reduce the final bond energy

at high temperature, this may lead to decomposition of the fluorocarbon film and formation of bubbles as shown in **Figure 14**. Blistering also causes a decrease in bond energy as observed in the 40mJ/m<sup>2</sup> sample in **Figure 11**. Increased blister area decreases the fraction of bonded area. The process/material challenge, therefore, is to fine-tune the initial surface energy so that the final bond energy at high temperature (~580°C) remains moderate yet no outgassing or bubble formation occurs. **Figure 15** shows de-bondability without blistering after a 580°C process is possible only within a narrow range of  $\text{CHF}_3/(\text{CHF}_3+\text{CF}_4)$  gas ratios. Excess polymer formation results in blistering after a 580°C process, while insufficient polymer formation results in permanent bonding. In one heroic experiment on wafer scale samples, we successfully fabricated an LTPS-TFT device on a thin glass bonded to an ALOT-treated glass carrier (surface energy ~55mJ/m<sup>2</sup>) and fully de-bonded it after it experienced a thermal excursion of 580°C.

### Summary

Temporary glass-to-glass bonding compatible with device processing including thermal steps at temperatures up to 580°C has been demonstrated using ALOT surface modification. This temporary method is suitable for bonding thin glass-to-glass carriers for sheet-to-sheet (S2S) or wafer-scale processing. The ALOT surface modification creates a high surface energy providing for strong van der Waals bonding compatible with mechanical, wet, and vacuum processing. Furthermore, ALOT surface treatment inhibits covalent bonding at temperatures as high as 580°C preventing permanent bonding. ALOT accomplishes temporary bonding by competing etch and deposition processes in a fluorocarbon plasma, which deplete silicon and boron from the carrier glass surface, fluorinate aluminum and alkaline earths, and create partial surface coverage of a polymer. Compatibility with device processing was demonstrated by IGZO and pSi TFT fabrication on

thin glass ALOT-bonded to glass carriers and successfully de-bonding.

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## FormFactor targets the need for faster engineering development data for 5G devices

By Debra Vogler, Sr. Technical Editor

**T**he demand for high-frequency ICs such as devices used for 5G applications is not only driving test requirements for the high-volume manufacturing (HVM) side of the industry, but also for engineering development. Jens Klattenhoff, Sr. Director of Marketing Systems at FormFactor, Inc., told *Chip Scale Review (CSR)* that 5G will dominate RF device growth for applications such as Vehicle to Everything (V2X), the Internet of Everything (IoT), as well as transportation and industrial machine control. Some of the challenges facing the test sector because of these developments include being able to gather data at frequencies that can go up to 70GHz, and even up to 120GHz in some cases, as well as taking more measurements that are sensitive to probe placement errors and calibration drift. Also of significance is the fact that 5G device testing requires measurements over a broader temperature range (-40°C to +175°C), which adds to testing time.

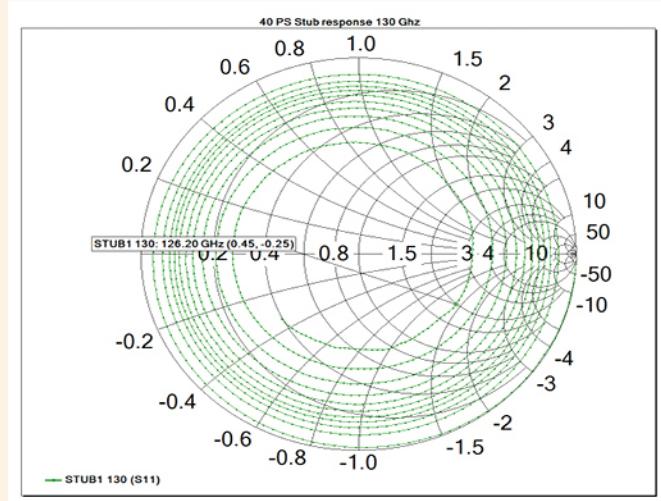
Add to the above considerations the fact that product life cycles are getting shorter, yet the product development cycle requires more testing at multiple frequencies and over a broad temperature range, and the industry clearly needs a way to do more measurements in a shorter period of time. Additionally, Klattenhoff pointed out that, as you go higher in frequency, the whole system and the whole measurement gets much more sensitive to probe placement errors and calibration drift. As a result, the system has to be recalibrated more frequently.

To address the challenges described above, FormFactor extended its Contact Intelligence™ technology and the

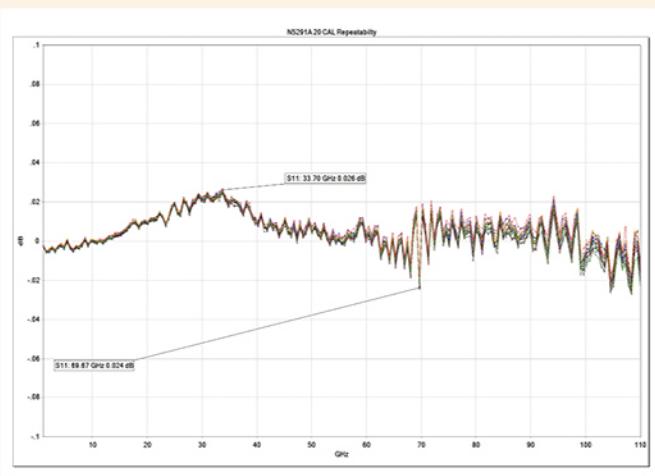
Autonomous RF Measurement Assistant (a new application layer), to its SUMMIT200 system for use in engineering environments. This extension enables those who work in test engineering development labs to complete their work on 5G device testing — with its need for high-volume engineering data — in a shorter period of time, thereby reducing time-to-market. The company refers to this part of the market as “niche production” or “high-volume engineering.”

The Autonomous RF Measurement Assistant encompasses the software algorithms that enable hands-free calibration on impedance standard substrates (ISSs) and is also responsible for monitoring calibration drift and automatic recalibration. The vision system addresses the drift challenges that come with making measurements at higher frequencies for 5G applications (Figure 1). The programmable positioners on the vision system are at 45° angles with respect to the wafer for the shortest possible measurement path. Algorithms check the calibration (probes in air) before testing. Slight mechanical drift in the system is accounted for by using cameras (eVue), which are housed separately from the rest of the system. These cameras, therefore, are not impacted by temperature excursions that would occur in the rest of the system. The motorized positioners are able to compensate and align the probes to the ISS for the most repeatable measurements (Figure 2).

In addition to the above RF testing application, the company has specialized Contact Intelligence™ applications for DC and silicon photonics (SiPh) testing.



**Figure 1:** S-parameter measurements of an open stub verification standard to 130GHz. SOURCE: FormFactor



**Figure 2:** Repeatability of 20 successive calibrations to 110GHz. SOURCE: FormFactor

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Accretech (Tokyo Seimitsu Co., Ltd.) 2968-2, Ishikawa-machi, Hachioji-shi Tokyo 192-8515, Japan Tel: +81 (42) 642-1701 <a href="http://www.accretech.jp">www.accretech.jp</a>	UF2000 _ Automated _ WI, DW, WLP, KGD, DM, MEMS, WP, ET	
Aehr Test Systems 400 Kato Terrace Fremont, CA 94539, USA Tel: +1-510-623-9400 <a href="http://www.aehr.com">www.aehr.com</a>	Fox-1P _ = CM _ = CM  Fox-XP _ = CM _ = CM	
Afore Vakiotie 5 Lieto 21420 Finland Tel: +358 2 274 6040 <a href="http://www.afore.fi">www.afore.fi</a>	Kronos _ = CM _ = CM	
Celadon Systems, Inc. 13795 Frontier Court Burnsville, MN 55337, USA Tel: +1-952-232-1700 <a href="http://www.celadonsystems.com">www.celadonsystems.com</a>		Card Type = C _ = CM _ = CM T = CM P = CM
Chunghwa Precision Test Tech. Co., Ltd No.15, Gongye 3rd Rd. Pingzhen Dist., Taoyuan City 324, Taiwan Tel: +886-3-469-1234 <a href="http://www.cht-pt.com.tw">http://www.cht-pt.com.tw</a>		Card Type = V _ = CM _ = CM T = CM P = CM
Contech Solutions Incorporated 631 Montague Avenue San Leandro, CA 94577 USA Tel: +1-510-357-7900 <a href="http://www.contechsolutions.com">www.contechsolutions.com</a>		Card Type = CM _ = CM _ = CM T = CM P = CM
EG Systems LLC 6200 Village Parkway Dublin, CA 94568 USA Tel: 1-408-528-3000 <a href="http://www.electroglas.com">www.electroglas.com</a>	EG6000 / EG6000e _ = CM _ = CM	
Feinmetall Zeppelinstr. 8, Herenberg 71083, Germany Tel: +49-171-5372072 <a href="http://www.feinmetall.de">www.feinmetall.de</a>		Card Type = C _ = CM _ = CM T = CM P = CM  Card Type = MEMS _ = CM _ = CM T = CM P = CM  Card Type = V _ = CM _ = CM T = CM P = CM

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FormFactor, Inc. 7005 South Front Road Livermore, CA 94551, USA Tel: +1-925-290-4000 www.formfactor.com	<p>MPS150/EPS150 measurement platform  <u>_</u> Manual  <u>_</u> = CM</p> <p>Summit 12000 probe station  with Pureline technology  <u>_</u> = Semi-automatic, automatic  <u>_</u> = CM</p> <p>PM8/EPS200/PA200  <u>_</u> = CM  <u>_</u> = CM</p> <p>PM300/CM300  <u>_</u> = CM  <u>_</u> = CM</p>	
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JEM America Corp. 3000 Laurelview Court Fremont, CA 94538, USA Tel: +1-510-683-9234 www.jemam.com	VS Series C CM <u>_</u> CM <u>_</u> CM T CM P CM	<p>Card Type = C  <u>_</u> = CM  <u>_</u> = CM  T = CM  P = CM</p>
Korea Instrument Co., Ltd. 9-29, Dongtansandan 4-gil, Dongtan-myeon Hwaseong-si, Gyeonggi-do 18487, South Korea, Tel: +82-31-375-5930 www.kicl.co.kr		<p>Card Type = C  <u>_</u> = CM  <u>_</u> = CM  T = CM  P = CM</p> <p>Card Type = V  <u>_</u> = CM  <u>_</u> = CM  T = CM  P = CM</p>

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MarTek, Inc. 112 S Rockford Dr. Ste 103 Tempe, AZ 85281, USA Tel: +1-480-947-5757 <a href="http://www.martekprober.com">www.martekprober.com</a>	4090μ+ <u>_</u> = CM <u>_</u> = CM T = CM P = CM	
Microfriend Inc. 10F Seoul Techno Park #232 Gongneung-ro, Nowon-gu Seoul, South Korea Tel : +02-944-6400		Card Type = MEMS <u>_</u> = CM <u>_</u> = CM T = CM P = CM
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	AP-80 <u>_</u> = CM <u>_</u> = CM T = CM P = CM	Card Type = MEMS <u>_</u> = CM <u>_</u> = CM T = CM P = CM
	708ft <u>_</u> = CM <u>_</u> = CM T = CM P = CM	Card Type = V <u>_</u> = CM <u>_</u> = CM T = CM P = CM
	705A-WG7 <u>_</u> = CM <u>_</u> = CM T = CM P = CM	
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T.I.P.S. Messtechnik GmbH Europastrasse 5, Villach, 9524 Austria Tel: +43-4242-319720 ext.4 <a href="http://www.tips.co.at">www.tips.co.at</a>		Card Type = V <u>_</u> = CM <u>_</u> = CM T = CM P = CM

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TSE Co. Ltd. 78, 4sandan 5-gil, jiksan-eup Cheonan-si, Chumgnam 31040, South Korea Tel: +82 10 8822 5630 <a href="http://www.tse21.com">www.tse21.com</a>		<p>Card Type = V  <u>_</u> = CM  <u>_</u> = CM  T = CM  P = CM</p>
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<b>Yokowo Co. Ltd.</b> 5-11 Takinogawa 7-Chome, Kita-Ku Tokyo 114-8515, Japan Tel: +81-3-3916-3111 <a href="http://www.yokowo.com">www.yokowo.com</a>		Card Type = CM <u>_</u> = CM <u>_</u> = CM T = CM P = CM

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# More than you think: the beauty of coaxial sockets

By Collins Sun, Ryan Chen, Hayden Chen /WinWay Technology/

**R**ecently, there have been significantly increasing demands for high-speed digital applications, such as computing requirements for artificial intelligence (AI), auto-pilot driving, augmented reality (AR), as well as virtual reality (VR). These applications require high-performance edge computing devices and more networking data centers to support the yearly increasing data stream. All those novel applications are coming with new industrial specifications in IC design, like PCIE Gen 4\_16Gbps, HDMI 2.0\_18Gbps, SerDes\_ 56Gbps, and GDDR6\_16Gbps etc., that will build up a fully digitally-connected world. Moreover, booming markets such as radio-frequency (RF) transmission systems, are coming to the fore as part of the mm-wave era, like 5th generation mobile networks (5G), WiGig, and automotive radar. Semiconductor test specifications and the acceptable tolerance are getting tighter, for example, insertion loss (IL), return loss (RL), impedance (Z), near- and far-end crosstalk, as well as jitter, etc., which make the test process more challenging.

Conventional test solutions for high-speed requests, like short probe and elastomer solutions, cannot satisfy all the different kinds of test conditions from characterization to production. Short probes that are <2mm when testing in a plastic socket is the most common solution for production applications. However, the signal integrity of a short probe might not be acceptable for various higher speed (>25Gbps) conditions because the plastic housing can neither shield the electromagnetic interference, nor improve signal integrity when there are less ground pins. Furthermore, the large device size, >55X55mm<sup>2</sup>, will usually have issues with “opens” that are caused by the warpage that can occur during the package assembly process. This warpage has a value of around 0.25mm based on the tolerance of the package outline drawing (POD). It almost

reaches the same level of recommended travel for the short probe. The other solution is an elastomer solution, whose thickness is near 1mm and is accompanied with superior performance and has a signal quality that is almost as good as a device that has been soldered. On the other hand, there is less current carrying capacity, shorter contact travel, and maintenance for the elastomer in production, and these will be the concerns because of its natural limitation in design and material.

Both of the solutions discussed above will not fulfill advanced semiconductor test requirements because the problems that arise from their implementation, as noted above, will lead to low or unstable yield in production.

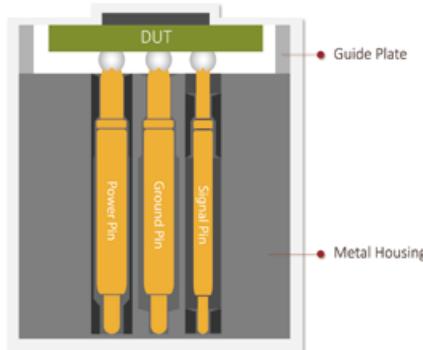
## Socket structure introduction

To satisfy all the requirements for high-bandwidth, low-crosstalk, impedance control, and a wide range of application temperatures, etc., a fully shielded coaxial socket is one of the few solutions that can address the challenges from device characterization to production because of its superior design that covers electrical, mechanical, and thermal considerations.

An intrinsic coaxial socket structure was developed under the brand name “Brownie.” It was based upon the fundamental design of a coaxial cable with a built-in highly reliable insulating composite, which is also suitable for the wide temperature range under a long-term testing environment. A challenge intrinsic to the design of this kind of socket is how to hold the pin without shorting to the metal housing body. Either using a plastic ring on the probe, or inserting it inside the pinhole are the intuitive methods for the coaxial socket design. However, it is very difficult to achieve a fine-pitch design (<P0.65mm) based on the ring structure, the dimension tolerance, and the long-term reliability requirements. There are also concerns with respect to socket maintenance because the ring plays

an important role for the purpose of impedance control.

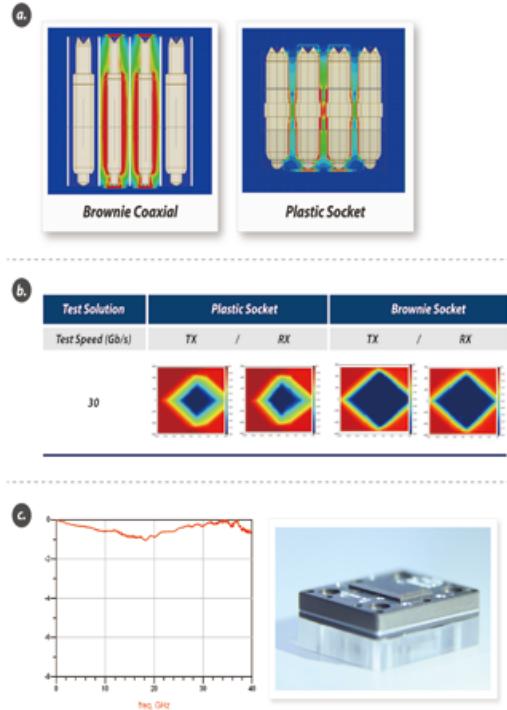
The patented feature of the Brownie coaxial socket is the “through-hole design” for the signal and power pin, which has an embedded insulated composite. The insulating material is like a probe holding mechanism that provides a heterogeneous coaxial structure as shown in **Figure 1**. The through-hole design is achieved by a series of sophisticated manufacturing and machining processes. The



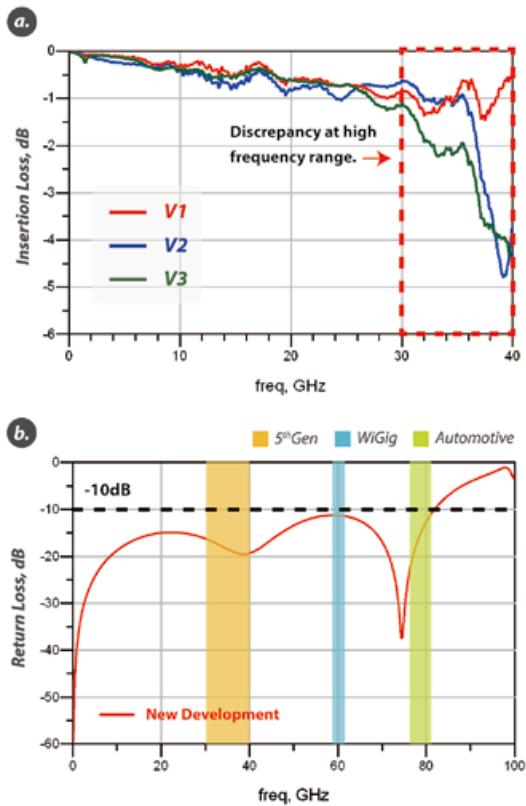
**Figure 1:** Brownie heterogeneous coaxial structure.

through-hole design can minimize the impedance discontinuity because the pin hole in the metal housing has the same diameter. In other words, the pin hole dimension of the metal housing doesn't need to change to fit the probe shape with the plastic ring as the holding mechanism. Therefore, many coaxial socket parameters can be easily adjusted to optimize the impedance value and RF behavior with minimal effort.

In **Figure 1** there are three characteristic types of the pin hole design for signal, power, and ground pin. They are able to optimize the electrical performance, such as power and signal integrity. The Brownie heterogeneous coaxial structure combines two different insulated features: 1) One is an insulated surface to avoid the socket body shorting with the PCB; 2) The other is an insulated composite to hold



**Figure 2:** a) Crosstalk effect between a plastic and a coaxial socket; b) A 30Gbps Eye diagram measurement; c) P0.4 coaxial measurement result and the product.



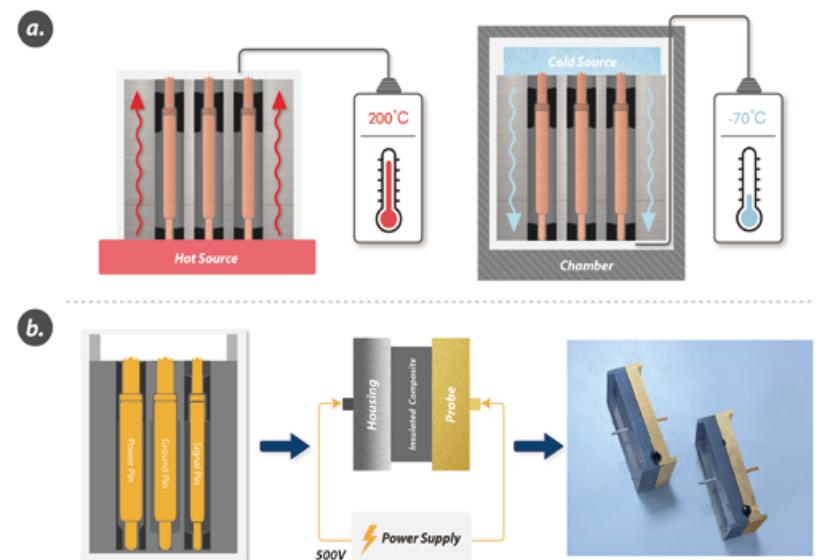
**Figure 3:** a) Co-grounding effect between the ground pin and metal housing; b) Coaxial socket in a millimeter wave (MM wave) application.

the signal and power probe inside the pinhole. The Brownie coaxial socket design along with the manufacturing process, enable multiple parameters to be easily adjusted to achieve the finest pitch testing down to 350 $\mu$ m now, in the -40~150°C testing range, and in the long term having a reliability of up to one million touchdowns.

The well-known benefits of using a coaxial socket are the impedance control and the significant crosstalk reduction. These properties help the signal integrity under high-speed test data transmission without disturbing the eye diagram, even at 30Gbps, (see Figures 2a and 2b). Because of the through-hole design embedded in the insulated composite, the fine-pitch fully-shielded coaxial solution for wafer test becomes real. The P0.4 coaxial solution in Figure 2c has been released to the market for package test with a guide plate, or a floating plate design, as well as for wafer test. It shows good impedance matching even at such small pitches as those used on the fully-shielded coaxial structure. Based on the product development roadmap, the minimum pitch of a Brownie coaxial socket will be targeted at a 200 $\mu$ m pitch.

We further studied the coaxial socket's performance in high-frequency applications, both using the through-hole design and the ground contact design between the ground pin and the pinhole of the metal housing. The impact on high-frequency behavior is shown in Figure 3, where it can be seen that there is a significant insertion loss deviation above 30GHz. The results in Figure 3a show that the ground pin needs to contact the housing in the testing position in order to have a better result in the high-frequency range. Therefore, the socket designer must seriously consider the grounding effect of the coaxial socket, especially in mm-wave applications. Figure 3b shows the return loss vs. frequency for the devices in the next "booming" markets of 5G, WiGig, and automotive radar. The package pitch of those consumable devices is usually less than P0.65mm. Brownie is the only fully-shielded coaxial socket solution for fine-pitch test.

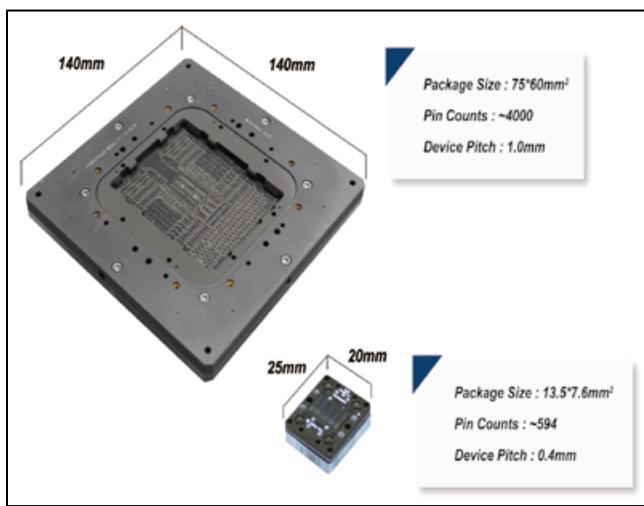
The Brownie coaxial socket was evaluated in various semiconductor test situations. Figure 4a illustrates the Brownie coaxial socket undergoing thermal cycling between -70 to 200°C to check the reliability of the embedded insulating composite material. The automotive test conditions require a wide range of test temperatures. Additionally, isolation under high-voltage conditions must be verified (see Figure 4b). The specification of EIA-



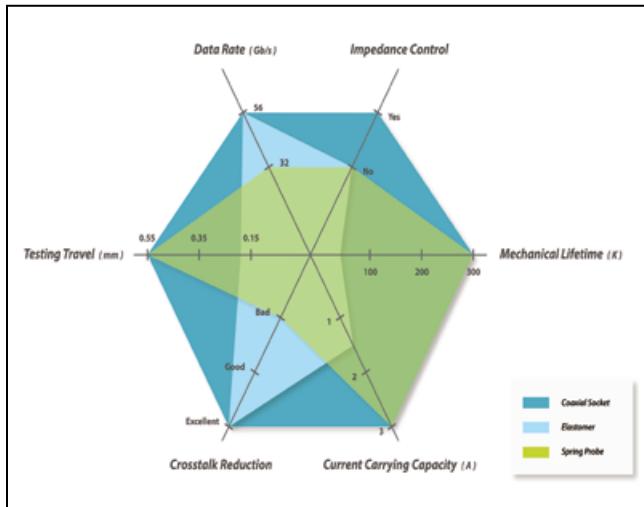
**Figure 4:** The verification of high- and low-temperature environments and the high-voltage test setup.

Laser Clean			
Material	Surface Resistance ( $\Omega$ )	Before Clean	Power : 250mJ Times : 5000
Peek Ceramic	$1.6 * 10^{11}$	$5.5 * 10^3$	$4.9 * 10^3$
PAI	$3.0 * 10^{11}$	$7.5 * 10^3$	$3.9 * 10^3$
PI	$4.5 * 10^{11}$	$2.5 * 10^{11}$	$1.9 * 10^{11}$
Brownie Coaxial	$3.2 * 10^{11}$	$2.2 * 10^{11}$	$2.0 * 10^{11}$

**Table 1:** Surface resistance variation of socket materials using a laser shot test.



**Figure 5:** Examples of a large package and small pitch with a high-speed application.



**Figure 6:** Test solution comparison among a coaxial socket, an elastomer socket, and a spring probe plastic socket.

364-20E (Method D) is used to test the insulated composite of the pin hole. In this case, the composite successfully passed 500V at 60s duration and the leakage current is less than 5mA. On the other hand, following the product maintenance guideline, there is no

With respect to mechanical performance and reliability, a touch down experiment was performed in the lab to check the socket's wear-out characteristics. There was only a few microns worth of damage on the

insulated composite after one million touchdowns. The results indicate the material strength and reliability is sufficient for the production requirement. With the increasing demands placed on high-performance ICs, especially in server applications, larger packages ( $>55 \times 55 \text{ mm}^2$ ) are becoming popular in the semiconductor market. These larger packages can include more and more functions in a single chip with the best cost and performance ratio. The maximum socket outline was  $140 \times 140 \text{ mm}^2$  (Figure 5), which was a manufacturing milestone in the development of the Brownie coaxial socket. The longer contact travel — up to 0.8mm for the probe design — is also considered for package sizes larger than  $65 \times 65 \text{ mm}^2$  to improve the contact coplanarity. For the purpose of package alignment, the guide plate and the floating plate can both be designed as the parts of a coaxial socket to fully protect the signal from the bottom to the top side. In the case of a package-on-package (PoP) application for use in the application processor (AP) of a mobile phone, the low-power DDR4 (LPDDR4\_4.2Gbps) has gradually become mainstream for high-performance mobile devices, but the signal crosstalk issues highly affect test results. It is suitable to use a coaxial socket to solve the crosstalk issue.

The Brownie coaxial socket can be adapted to a broad range of package designs and pitch requirements with well-controlled impedance and significantly reduced crosstalk. It is also a suitable solution for a wide range of temperatures, as well as for different kinds of package types. In summary, the Brownie coaxial socket structure solves many coaxial socket design challenges.

## Summary

In the future, more and more challenges will arise for certain applications of semiconductor testing requirements. Whatever the application might be, the computation capabilities of devices will continue to go much higher. It will therefore be an on-going challenge for socket design. Figure 6 shows a radar chart that illustrates test solution comparisons. The radar chart indicates 6 key factors including

Item	Application Description
1.	Requirement for high-speed testing solution for wafer test is as follows: the minimum pitch is now down to 350µm, but 200µm is the final goal in the product roadmap.
2.	There remains a concern for contact when there is a large package size (more than 55X55mm <sup>2</sup> ) because of warpage.
3.	A few ground pins will cause the high crosstalk effect, especially in memory tests. One example is that of P0.4 LPDDR4 (highest speed is 4.2Gbps) in the memory test of a PoP top socket.
4.	The PoP contact chuck design in automatic test equipment (ATE) is from -40 to 125°C.
5.	The Brownie coaxial socket is a suitable solution from initial device characterization to mass production.
6.	The Brownie coaxial socket is the single solution that can be applied to high-speed and mixed-frequency signals, such as RF analog and digital signals.
7.	High-speed and current carrying capability, >3A @0.8mm.
8.	High-voltage test requirements up to 500V
9.	Bandpass design for specific mm-wave applications, such as 5G networking, WiGig, and automotive radar.

**Table 2:** Summary of various semiconductor test requirements and applications that can be accomplished by using the coaxial socket solution.

impedance control, achievable data rate, testing travel, crosstalk reduction, current carrying capacity, and the mechanical life among coaxial sockets, elastomer sockets, and spring probe plastic sockets.

**Table 2** summarizes the various semiconductor test requirements and

applications that can be accomplished by using the coaxial socket solution.

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# Die-attach materials and LED functional performance

By Gyan Dutt, Nicholas Herrick, Sathish Kumar, Pavan Vishwanath, Ranjit Pandher [Alpha Assembly Solutions]

**D**ie attach materials play a key role in functional performance and reliability of light-emitting diodes (LEDs). Selection of a suitable die-attach material for a particular chip structure and application depends on several considerations. These include performance (light output and thermal dissipation at operating temperature), reliability (lumen maintenance and mitigation of thermo-mechanical stresses over lifetime), packaging process (equipment, throughput and yield) and cost factors. Eutectic gold-tin, silver-filled epoxies, solder, silicones and sintered materials have all been used for LED die attach. Often, use of a particular material technology results in trade-offs between different performance attributes.

In this study we used different die-attach materials (solder, silver epoxy and silicone-based) to package lateral, vertical and flip-chip LEDs. For vertical and flip-chip structures (which require electrically conductive die attach), solder, silver epoxy and silver-filled silicone materials were used. Lateral dies (on nonmetallized sapphire substrates) were bonded with silicones (both conductive and insulated) as well as silver epoxy. The optical and electrical performance of the assembled packages was then characterized by junction temperature, luminous flux and efficacy measurements in an integrating sphere (according to IES LM-79-08).

The paper describes these results and discusses the effect of die-attach material properties and chip structure on LED functional outputs. The results clearly indicate that while optical characteristics of the die-attach material dominate the light output of lateral LEDs, junction temperature management (via die-attach thermal conductivity) is important for achieving optimal functional performance for higher power vertical and flip-chip LEDs.

## Introduction

LED die packaging still accounts for ~1/3 the cost of the packaged LED. The last few years have seen several trends in LED packaging, namely: 1) flip-chip and chip-scale

packaging (CSP) adoption; 2) growth of a packaged mid-power segment (0.2-0.5W) with lateral dies and chip-on-board (COB) modules; and 3) increased focus on infrared (IR) and ultraviolet (UV) LEDs for new applications (with higher power vertical structures). All these trends, with different chip structures, are driven by underlying need for higher efficacy (lm/W), lower cost (lm/\$) and longer lifetime in a smaller form factor.

Die attach is the first layer that comes into contact with the LED die and its thermal performance and stability has a direct impact on LED light output, light extraction and lumen maintenance over time. The die-attach material and (more importantly) the process together have a significant effect on the cost of ownership of the package (and the light engine).

With several material technologies available for die attach (like eutectic gold-tin/Au80Sn20, silver-based conductive adhesives, solder- and silicone-based adhesive), selecting a suitable material for a particular chip structure (lateral, vertical and flip chip) is essentially about making trade-off decisions between different process or performance attributes.

In this study we attached different structure LEDs (lateral, flip chip, and vertical) with different die-attach materials (silver epoxy, solder and silicone). These packages were then subjected to industry standard optical and electrical performance tests.

## Die-attach materials overview

The descriptions below provide an overview of die-attach materials.

**Eutectic gold-tin or AuSn.** Eutectic gold-tin (80/20 Au/Sn by wt) has been the “gold standard” die-attach material for high-reliability applications. For LED die attach it is used either as a pre-coated layer on the LED backside, a preform, or in the form of solder paste. The typical process is flux-less with an automated bonder with scrubbing capability. Lately, AuSn solder paste as well as flux-assisted processes (with pre-coated dies or preforms) have been used for higher throughput. Although the cost of ownership of AuSn die attach is much higher than other materials, it is still the material of

choice for high-power applications due to its high thermal conductivity (57W/mK) and proven reliability (high creep and fatigue resistance with secondary reflow compatibility).

**Conductive adhesives.** Conductive adhesives (mostly silver-filled epoxies) constitute the largest class of thermal die-attach materials (by unit number) for semiconductor power packages. They are compatible with the existing back-end packaging equipment and provide an attractive cost/performance balance (typically up to 50W/mK thermal with secondary reflow compatibility). Because they stick to bare silicon, they are the preferred material of choice for dies without back-side metallization (like GaN on silicon).

**Solder.** Solder (mostly SAC-based) provides exceptional value with low cost and fast assembly process with reasonable thermal performance (50-60W/mK). Lately, there has been a trend to make the flip-chip structure compatible with solder on surface mount technology (SMT) lines. However, because SAC solder melts in the 217-221°C range, its use is limited to applications where either high-temperature stability is not required in operating conditions, or during further processing (like secondary reflow). SnSb-based solder with a melting point range between 245-251°C can survive second reflow below 240°C.

**Silicone-based adhesives.** Silicone-based adhesives (filled with ceramic-based fillers for heat dissipation) have been the die-attach technology of choice for low-mid power sapphire-based lateral LEDs. These materials are transparent, have excellent adhesion and high-temperature stability (resistant to color degradation). The stamping (pin transfer) process has been adopted to achieve very thin bond lines at relatively high throughput for LED die attach.

## LED die structures overview

This section discusses the experimental elements of our study.

**LEDs.** For lateral die structure, green LEDs on a sapphire substrate from III-V semiconductor (TCE13-525, 330x330µm) were bonded on a star-shaped extruded copper pedestal. This design did not include

a dielectric layer between the die and the die-attach layer and allowed for high-sensitivity thermal measurements of the stack. Because a sapphire die bottom does not have any metallization, it requires an adhesive die attach (like silver epoxy and silicones) and solder was not used to bond the lateral dies.

For vertical dies, red LEDs on silicon (TCO40-624) from III-V semiconductor were bonded on the same star-shaped copper pedestal. Because vertical dies have the metallized p-electrode at the bottom, only conductive die-attach materials (like solder, silver epoxy and silicone-filled epoxy) were used.

To evaluate a flip-chip LED, a Luxeon Flip-chip UV (LxF2-U400 from Lumileds) was bonded onto an aluminum core substrate with electroless nickel immersion gold (ENIG) pads. Conductive die-attach materials (solder, silver-filled epoxy and silicone) were used.

**Die-attach materials.** To evaluate non-conductive materials, two silicone-based materials (Silicone A and Silicone B) were used for lateral die bonding. Both these materials are commercially available and mainly differed in their transparency (with transparency of Silicone B being higher than Silicone A).

Among silver-based conductive materials, one material was a high thermal silver-filled epoxy (Silver Epoxy) and the other one was silver-filled silicone (Silver Silicone) with the thermal conductivity of the silver epoxy being much higher than that of the silver-filled silicone (**Table 1**). Finally, fine T6 powder (15-25 $\mu$ m particle size) SAC305-based solder paste (T6 Solder Paste) was used for flip-chip and vertical LED die attach (**Table 2**).

Die Structure	Die Attach Materials
Lateral	Silicone A, Silicone B, Silver Epoxy, Silver Silicone
Vertical	T6 Solder Paste, Silver Epoxy, Silver Silicone
Flip-Chip	T6 Solder Paste, Silver Epoxy, Silver Silicone

**Table 1:** Die-attach materials and the type of dies that were bonded.

Die Attach	Optical Transparency @ 450nm	Bulk Thermal Conductivity (W/mK)
Silicone A	~80% (5 $\mu$ m thick)	0.5
Silicone B	>83% (1mm thick)	0.2
Silicone Epoxy	0	>25
Silver Epoxy	0	60
T6 Solder Paste	0	60

**Table 2:** Die-attach materials properties.

**Die-attach set-up.** Pin transfer (also called stamping) was used to transfer the die-attach material (from a reservoir) onto the substrate. The die was then aligned, placed on the substrate and then reflowed. An ASM pin transfer die bonder (ASMD838L) was used for the pin transfer and die placement. The height of the paste in the reservoir was optimized for full die pad coverage and the desired bond line thickness (BLT). A batch oven was used for curing of silicones (150°C for 1hour) and silver epoxy (175°C for 1 hour). The T6 Solder Paste assembly was reflowed in a 7-stage Heller oven (under a N<sub>2</sub> environment).

**Optical and electrical characterization.** The transient voltage method was used to measure the junction temperature of the LED assemblies. These measurements were based on JEDEC Standard EIA/JESD51-1 and have been described in detail [1-2]. Essentially, the method is based on rapidly switching the LED between high and low currents, so as to utilize them as test devices to measure the junction temperature. If the

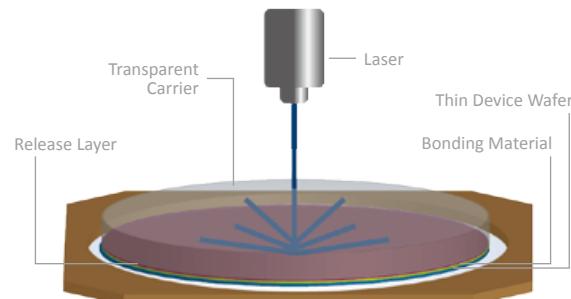


# Creating Safe Environments

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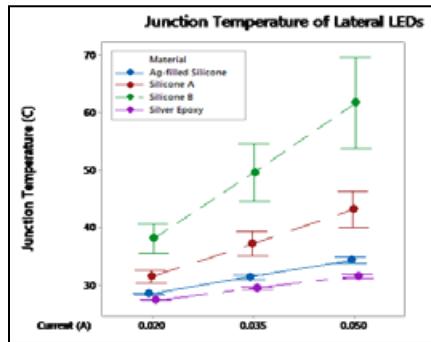


switch between heating and sensing currents happens fast enough, then the sensing current can be used to measure the temperature of the previous heating phase. The thermal resistance of all the layers in the die-attach stack can then be calculated. The relationship between the forward voltage and the junction temperature (also known as the k-factor) was established to calibrate the use of the LED as a temperature sensor.

Measurement of the optical properties of the LED assemblies was done according to IES LM-79-08 [3]. The set-up consisted of placing the LED assemblies in a light integrating sphere with a radiometrically calibrated spectrometer.

## Results and discussion

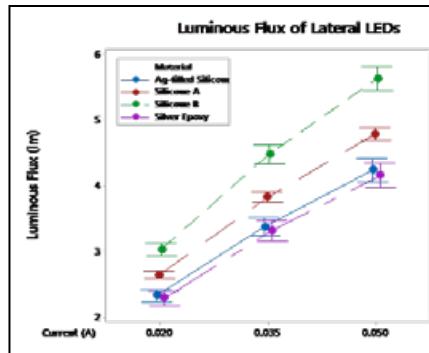
The results of the study fall under three



**Figure 1:** Junction temperature of lateral LEDs assembled with four different die-attach materials vs. the operating current.

main categories, discussed below: 1) Lateral LED; 2) Vertical LED; and 3) Flip-chip LED.

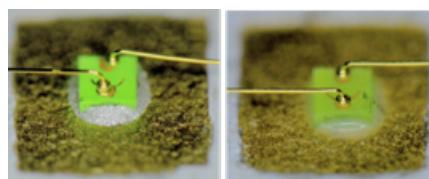
**Lateral LED results.** Figure 1 shows the behavior of the junction temperature of the lateral LEDs with increasing current. Lateral LEDs used here do not have any backside metallization. So the choice of die-attach materials eliminated any material that does not stick to non-metallized surfaces, such as solders. Four materials were tested: a silver-filled conductive epoxy, a silver-filled silicone-based adhesive, and two types of non-conducting silicones. Nonconducting silicones were essentially optically transparent, while silver-filled materials are opaque. Among the materials used, silver-filled epoxy has the highest thermal conductivity followed by silver-filled silicone. Unfilled silicones have the lowest thermal conductivity. At any given current, LEDs with silver-filled epoxy show the lowest junction temperature followed by those assembled with silver-filled silicone. Unfilled silicones have much lower thermal conductivity and result in a much higher



**Figure 2:** Luminous flux of lateral LEDs assembled with four different die-attach materials vs. the operating current.

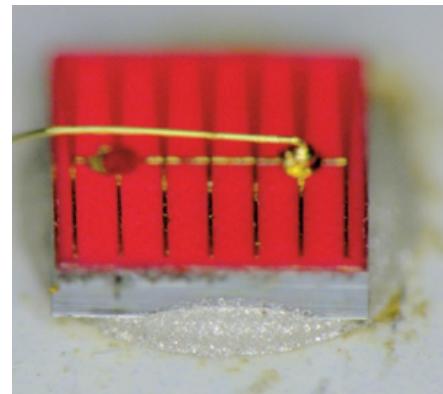
junction temperature of LEDs assembled with those. Between the two silicones tested, Silicone B has a higher junction temperature.

Figure 2 shows a luminous flux of the same lateral LEDs at three different operating currents. At any given current, silver-filled epoxy shows the lowest luminous flux followed by silver-filled silicone, Silicone A and Silicone B. These are interesting results showing how the optical transparency affects the overall optical efficiency of the packaged LED. LED quantum efficiency decreases with increasing junction temperature. However, not all of the photons generated by electron-hole pair recombination are extracted as useful light. This is especially true for lateral LEDs. The PN junction of lateral LEDs is grown on a sapphire substrate. Sapphire is partially optically transparent and light generated at the PN junction travels in all directions. To get the maximum efficiency, all of those photons should be collected. Silver-filled epoxy and silver-filled silicone absorb ultraviolet (UV), visible and near infrared (IR) radiation. Therefore, when these materials are used in die attach, the fraction of light traveling towards the substrate is lost. On the other hand, silicones are transparent, therefore all the light traveling in that direction is ultimately reflected back from the metallized substrates. That is why LEDs assembled with transparent silicones show higher luminous flux (and efficacy) even though those LEDs are operating at higher junction temperature as compared to



**Figure 3:** Pictures of operating LEDs assembled with silver-filled epoxy (opaque) and silver-filled silicone (transparent) die-attach materials.

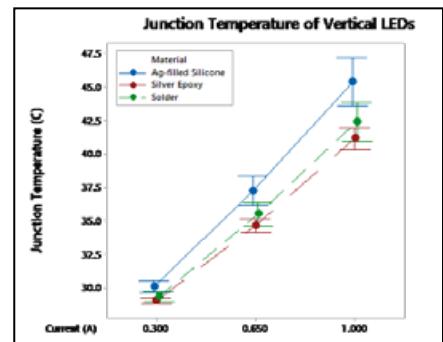
silver-filled opaque die-attach materials. This effect can be seen visually in the pictures of operating LEDs shown in Figure 3. Among the nonconductive silicones as well, die-attach assemblies with higher optical transparency Silicone B had higher light flux (compared to



**Figure 4:** A vertical LED assembled with silver epoxy.

Silicone A, even though Silicone A had higher thermal conductivity).

**Vertical LED results.** Figure 4 shows the vertical LED bonded by silver epoxy. The top side electrode is wire-bonded, while the die bottom serves as the other electrode. Figure 5 shows the junction temperature of

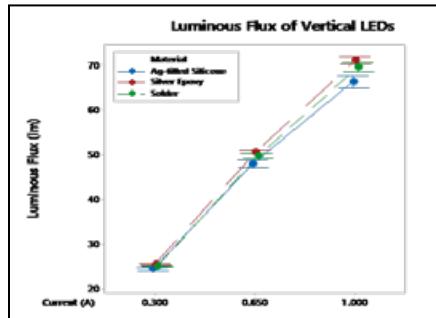


**Figure 5:** Junction temperature of vertical LEDs assembled with three different die-attach materials vs. the operating current.

vertical LEDs assembled with three types of die-attach materials: SAC305 solder paste, a silver-filled epoxy and a silver-filled silicone. The plots show junction temperature at three operating currents. In the vertical LED, the current path is through the die-attach layer, therefore, die-attach material has to be electrically conducting. That is why no silicone is used in this part of the experiment. Not surprisingly, the measured junction temperature of LEDs assembled with these materials is in the reverse order of their thermal conductivities. Silver-filled epoxy with thermal conductivity >60W/mK

mk shows the lowest junction temperature at any current, closely followed by solder. Silver-filled silicone shows the highest junction temperature.

**Figure 6** shows the luminous flux of the same three type of vertical LEDs at three different currents. Not surprisingly, LEDs with the lowest junction temperature (those assembled with silver-filled epoxy) show the

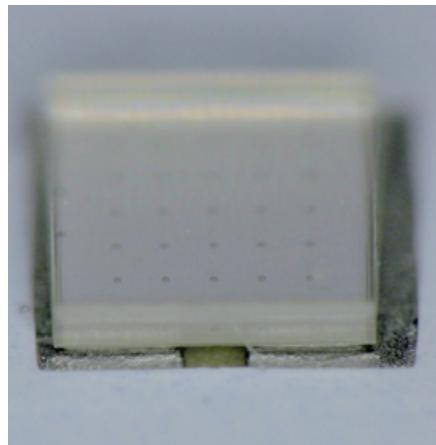


**Figure 6:** Luminous flux of vertical LEDs assembled with three different die-attach materials vs. the operating current.

highest luminous flux, and those with the highest junction temperature (silver-filled silicone die attach) show the lowest luminous flux (and efficacy).

Unlike lateral LEDs, vertical LEDs have a conducting substrate, and that substrate has a backside metallization. This metallization layer reflects back the light going towards the die attach later. Therefore, unlike lateral LEDs, there is no advantage to using a transparent die-attach material. The only properties of the die-attach material that matter are the thermal properties and the electrical conductivity.

**Flip-chip LED results.** Like vertical LEDs, flip-chip LEDs also need an electrical conducting die-attach material to bond the anode and cathode pads (see **Figure 7**). Therefore, silver-filled epoxy, silver-filled



**Figure 7:** A flip-chip LED assembled using solder.

silicone and SAC305 solder paste were used. Most of the LEDs assembled with silver-filled epoxy and silver-filled silicone either demonstrated a shorted P and N terminal, or demonstrated a small leakage current. This situation arises because of the fact that the PN junctions on the flip-chip LED dies are exposed on the side. Any of the die material wicking up on the side is likely to short the PN junction. It is impossible to avoid any fillet on the side of the die when using an epoxy- or silicone-based die-attach material. Solder

does not have that problem, because during the soldering process, the solder always sticks only to metallized surfaces. Even if there is any solder paste outside the die during die placement, all of it pulls back underneath the die, onto the two pads during solder reflow because of the solder surface tension. Therefore, the only good results we obtained on flip-chip LEDs is when solder was used as the die-attach material. This result is consistent with our previous work on flip-chip die attach by solder stamping [4].

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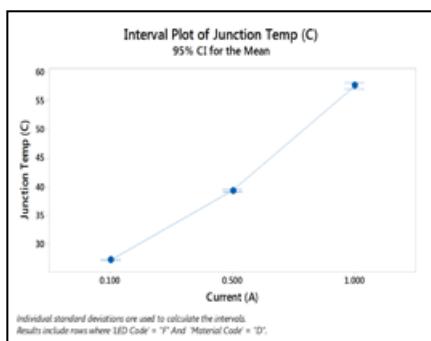
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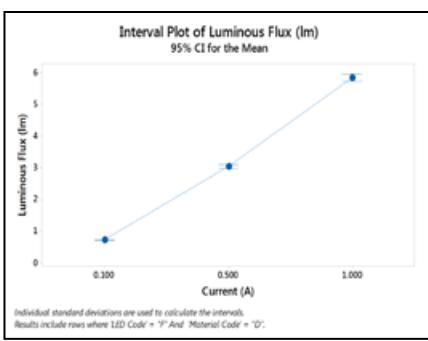
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**Figure 8:** Junction temperature of flip-chip LEDs assembled with SAC305 solder paste die-attach material vs. the operating current.

**Figure 8** shows a plot of the junction temperature of flip-chip LEDs assembled with SAC305 solder paste vs. operating current. Not surprisingly, higher current results in a higher junction temperature. Luminous flux follows the same trend, as shown in **Figure 9**. Just like the vertical LEDs, both die attach pads on the flip-chip LEDs are metallized. Therefore, any light going towards that side is reflected back before reaching the die attach layer. Therefore, there is no advantage to using a transparent conducting die-attach material, even if you could find one.



**Figure 9:** JLuminous flux of flip-chip LEDs assembled with SAC305 solder paste die-attach material vs. the operating current.

## Summary

The study systematically evaluated the effect of thermal and optical properties of die-attach materials on functional performance characteristics of lateral, vertical and flip-chip LEDs (junction temperature, light output and efficacy).

For lateral LEDs, the optical transparency of the die-attach material was found to dominate the extracted light output. Even though high bulk thermal conductivity materials (silver-filled epoxy and silver-filled silicone) enabled lower junction temperatures

(and hence, higher quantum efficiency), the extracted light output (up to the maximum current limit) was much lower than for optically transparent materials (which had much higher junction temperatures).

For vertical LEDs, high bulk thermal conductivity die attach (as expected), resulted in lower junction temperature (higher quantum efficiency), as well as higher light output. Optical transparency of the die-attach material was irrelevant because the light is reflected off the metallized electrode at the bottom and does not come in contact with the die-attach layer.

Finally, functional performance of flip-chip LEDs was found to be strongly

influenced by the fillet around the light-emitting junction. Any conductive material covering the active PN area was found to cause current leakage resulting in dark spots and low light output. Solder (due to its high surface tension) wet-out the metallized substrate pads and did not make the fillets contaminating the PN area. This suggests that solder (other than eutectic AuSn, of course) is a suitable material for flip-chip die-attach for LEDs.

This study clearly suggests that there is no universal die attach for LED packaging and LED die structure must be taken into account to select the optimal suitable die-attach material and/or process.

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Pavan Vishwanath received Diploma in Tool & Die Making from Government Tool Room & Training Center, Mysore (India) and is Senior Engineer for Manufacturing Technology at Alpha Assembly Solutions.

Ranjit Pandher received his PhD in Physics from Indian Institute of Technology (Kanpur) and is Senior R&D Manager at Alpha Assembly Solutions.

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# INDUSTRY NEWS



The 2018 IEEE 68th Electronic Components and Technology Conference

## Report from ECTC 2018

By Sam Karikalan [Broadcom Inc.]

The IEEE Electronic Components and Technology Conference (ECTC) lived up to its reputation as the premier global event of the microelectronics packaging industry, yet again in 2018. The 68th edition of ECTC, held at the Sheraton San Diego Hotel & Marina, May 29 – June 1, 2018, broke several records set in the recent past. Impressive statistics from this year's conference, like the ones listed below, prove again that IC packaging is continuing to gain the attention of the greater semiconductor and electronic systems industry and ECTC's focus on serving the needs of these new attendee demographics is continuing to yield results. Here are a few of this year's statistics:

- 1756 attendees, the highest attendance ever in ECTC history (Figure 1);

- 369 technical papers, presented in 36 oral and five interactive presentation sessions;
- 18 professional development courses

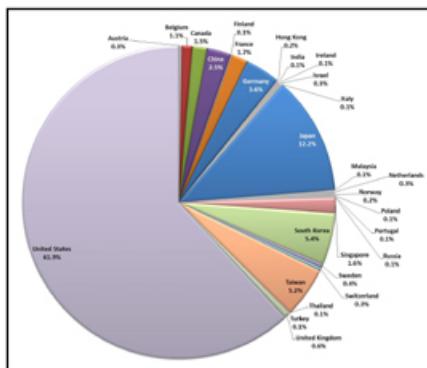


Figure 1: ECTC 2018 attendees came from 28 countries all across the world.

attended by a record number of 480 participants;

- 36 corporate sponsors with a record level of industry support; and
- 106 Technology Corner exhibit booths, with the best exhibitor interest ever to participate.

Speaking as the General Chair of the 68th ECTC, I attribute this success of the conference to all its authors and invited speakers, who brought their world class work on cutting-edge IC packaging technologies for presenting at this conference, the 200+ program subcommittee members who worked very hard throughout the past year to pull together the technical sessions, the highest level of industry interest in exhibiting at the Technology Corner, and the outstanding financial support from the conference sponsors.

The logo for the 15th International Wafer-Level Packaging Conference (WLPC) 2018. It features a stylized globe composed of blue and white squares, with the year '2018' above the letters 'WLPC'. Below the letters, the text '15th International Wafer-Level Packaging Conference' is written.

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Douglas C.H. Yu, Ph.D  
Vice President, Research & Development  
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**Monolithic versus Heterogeneous Packaging: Where Does the Future Lie?**  
Walden Rhines, Ph.D  
President and Chief Executive Officer  
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**Interconnected World and the Automotive Paradigm**  
Veer Dhandapani, Ph.D  
Head of Automotive Packaging  
NXP Semiconductors

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## Fan-out packaging still rules!

Technical sessions (Figure 2) on fan-out wafer/panel-level packaging were the biggest draw, for the fourth year in a row. Many of these sessions saw attendees spilling over into the hallways, with no room to even stand inside, and the organizing team had to scramble for a TV display outside the room for viewing



Figure 2: Packed room for a fan-out packaging session.

the slides. Papers from key players in that industry segment, such as TSMC, Samsung and MediaTek, generated a lot of interest. Sessions on other packaging topics such as 2.5D/3D integration, flip-chip and opto-electronics were also well attended. An interesting observation was that this year's ECTC also attracted some very good signal integrity/power integrity papers as well that took four full sessions.

The five interactive presentations sessions this year were not co-located with the Technology Corner exhibits. In spite of that, one could see that a large number of people stopped by those posters and interacted well with the presenting authors.

## Artificial intelligence at ECTC

ECTC is known for its special sessions, with invited speakers, running very late into the night, and this year was not any different. This is where non-traditional and emerging topics such as artificial intelligence (Figure 3), co-design for heterogeneous integration, soft material-enabled electronics, assembly frontiers, and high-density packaging kept over 100 attendees at any given time engaged with these presentations from industry experts, irrespective of the time of day.



Figure 3: Wednesday evening plenary session on the "Impact of Artificial Intelligence on System Design."

## ECTC luncheon keynote address

Boon Chye (BC) Ooi (Figure 4), Sr. Vice President of Global Operations at Broadcom Inc., was this year's ECTC luncheon keynote speaker. Being a semiconductor industry veteran with over four decades of operations and supply chain



Figure 4: B.C. Ooi of Broadcom Inc. delivered the ECTC luncheon keynote address.

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experience, Mr. Ooi addressed the cost aspect of the advanced 2.5D integration technology that enables artificial intelligence, autonomous cars and wearables, and its implications on the supply chain of the immediate future. Stressing the point that IC packaging technology will be the key enabler of all these new application frontiers with the highest CAGR, Mr. Ooi issued a call-to-action to enable the supply chain of 2022 that included the following:

- Upgrade assembly yield management to fab level, big data;
- Develop µ-bump probe & test technologies for improved yield;
- Develop substrates for low-loss mm-wave channels on large packages;
- Develop low-cost thermal solutions to reduce end-customer's system cost;
- Need multiple suppliers for silicon content, packaging raw material, substrates and assembly, to maintain business continuity.

#### IEEE CPMT Society is now IEEE EPS



The sponsoring organization of ECTC, the IEEE Electronics Packaging Society (formerly Components, Packaging and Manufacturing Technology Society) hosted the Thursday luncheon. Avram Bar-Cohen, IEEE EPS President, presided over this luncheon and said that the IEEE EPS members were at the forefront of the electronic industry's transformation, driving innovation in microsystem packaging in key areas such as heterogeneous integration, 3D packaging and the Internet of Things (IoT). The 2018 IEEE President-Elect, José M. F. Moura, was the invited chief guest at this luncheon. The following industry pioneers and innovators were also honored with various IEEE EPS Field Awards, at the luncheon:



**Figure 5:** William Chen of ASE receives the IEEE Electronics Packaging Award from the 2018 IEEE President-Elect, José M. F. Moura.

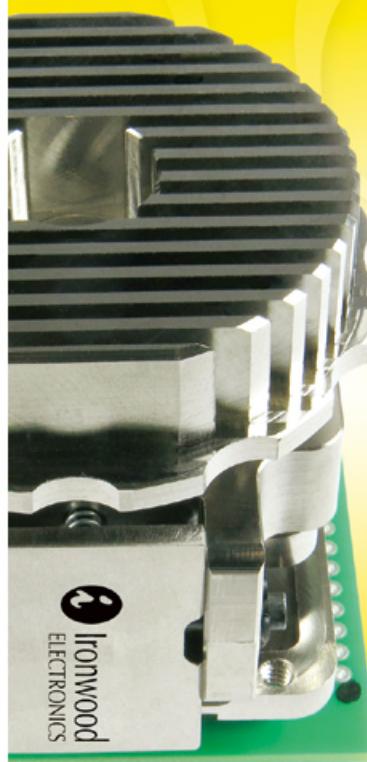
- William Chen, ASE (Figure 5), with the IEEE Electronics Packaging Award for Contributions from R&D through Industrialization and Leadership in Strategic Road-mapping for Heterogeneous Integration.
- Pradeep Lall, Auburn University, with the Outstanding Sustained Technical

Contribution Award.

- Douglas Yu, Taiwan Semiconductor Manufacturing Company, with the Electronics Manufacturing Technology Award.
- Jean Trewella, GLOBALFOUNDRIES, with the David Feldman Outstanding Contribution Award.

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- Muhannad Bakir, Georgia Institute of Technology, Kuan-Neng Chen, National Chiao Tung University in Taiwan, and Katsuyuki Sakuma, IBM T.J. Watson Research Center, with the Exceptional Technical Achievement Awards.
- Annette Teng of Promex Industries Inc., Gilles Poupon of CEA-LETI in France, and Yoshitaka Fukuoka of Worldwide Electronic Integrated Substrate Technology Inc. in Japan, with the 2018 IEEE EPS Regional Contributions Awards.

#### Joint events with ITERM

The 2018 ECTC featured two joint events with its sister conference, ITERM, that was also co-located at the same venue. The Wednesday evening Women's Panel and Reception (Figure 6), co-chaired by Cristina Amon of University of Toronto, and Tanja Braun of Fraunhofer Institute for Reliability and Microintegration (IZM), was one of them. This panel had over 100 attendees listening to the speakers and participating in the discussions on how to enhance women's participation in engineering around the globe.



**Figure 6:** ECTC/ITERM Women's Panel and Reception saw a record attendance this year.

The other joint event, ECTC/ITERM Young Professionals Panel and Reception (Figure 7) that was chaired by Yan Liu of Medtronic had been introduced at ECTC for



**Figure 7:** Young Professionals Panel & Reception was new at ECTC this year.

the first time this year. Career development advice from industry veteran, Steve Bezuk, and Kathleen Kramer of UC San Diego brought together many recent graduates that attended either of the conferences together for an evening of useful introspection.

#### ECTC is outgrowing its traditional venues

As it was evident in San Diego, the record attendance at this year's ECTC – and at one of its smallest venues – pushed the logistics challenges to their limits. Some of the session rooms and the luncheon ballroom were overflowing with attendees, while the organizing team (Figure 8) also had to deal with the loss of an annex tent, previously used for additional exhibit booths in the main Bayview Pavilion tent, to comply with fire code regulations. This caused several unplanned exhibit floor map changes and relocation of IP poster display areas out of their original places among the exhibits.

Finally, ECTC 2018 seems to have emerged unscathed through all these challenges, as proved by its resounding success and the attendee satisfaction rate for the depth of the technical content it offers. The ECTC Executive Committee is reportedly looking into various options that could sustain or even accommodate any anticipated future growth in industry participation!!

There is no doubt that such an energetic and proactive team at the helm and the growing importance of the IC packaging industry as a whole will keep ECTC's flag flying high for a very long time.

Mark your calendar for the 69th ECTC:



**Figure 8:** Some of the ECTC 2018 Organizing Team members (from left to right): Rozalia Beica – Web Admin, Henning Braunisch - Jr. Past General Chair, Alan Huffman - Sr. Past General Chair, Chris Bower - Program Chair, Nancy Stoffel – Asst. Program Chair, Sam Karikalan – General Chair, Mark Poliks – Vice General Chair.

Planning is already underway for the 69th ECTC, which will be held May 28–May 31, 2019, at the Cosmopolitan of Las Vegas, Las Vegas, Nevada, USA. The first call-for-papers has been issued and abstracts must be received by October 8, 2018. For more information, visit [www.ectc.net](http://www.ectc.net).

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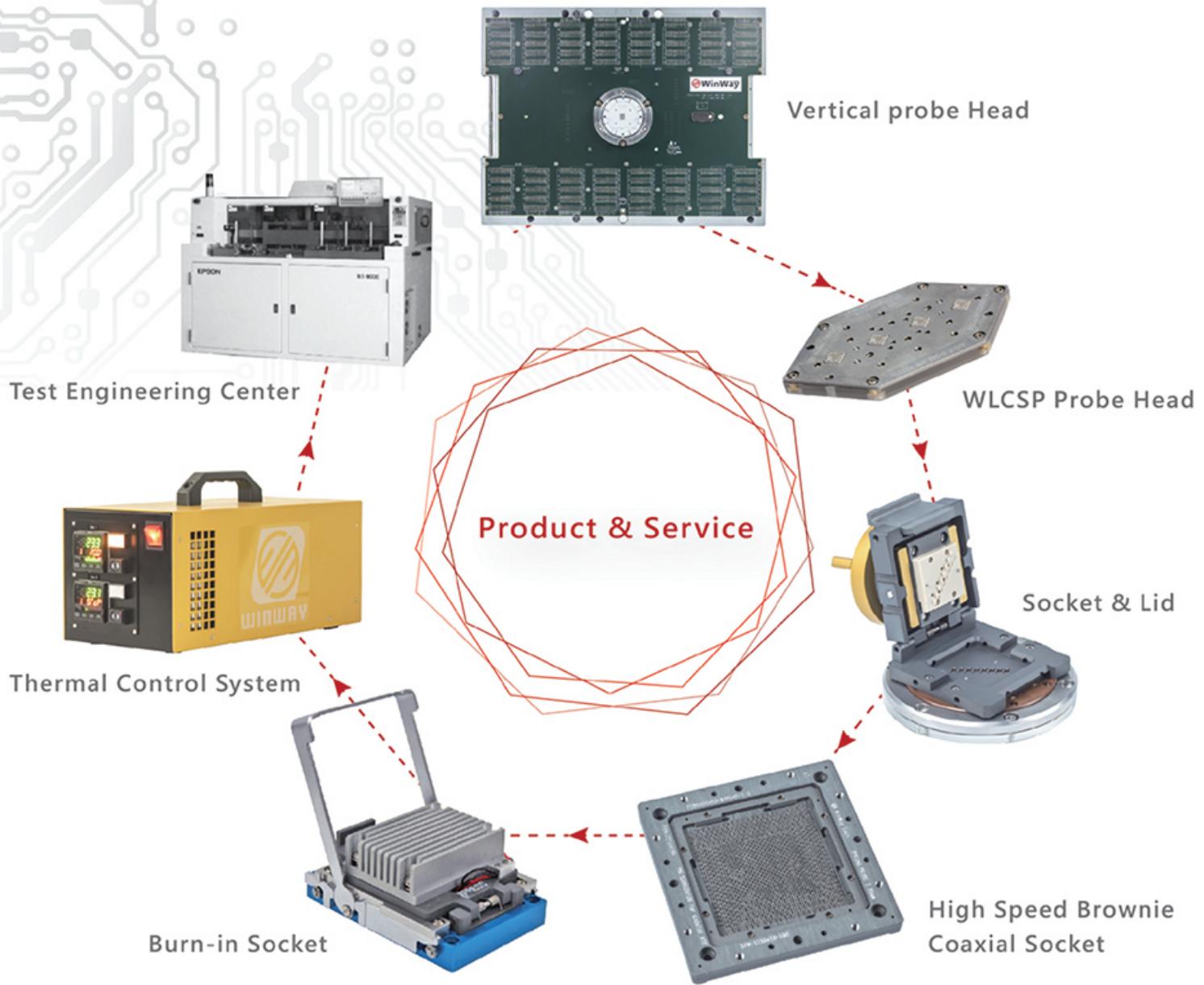
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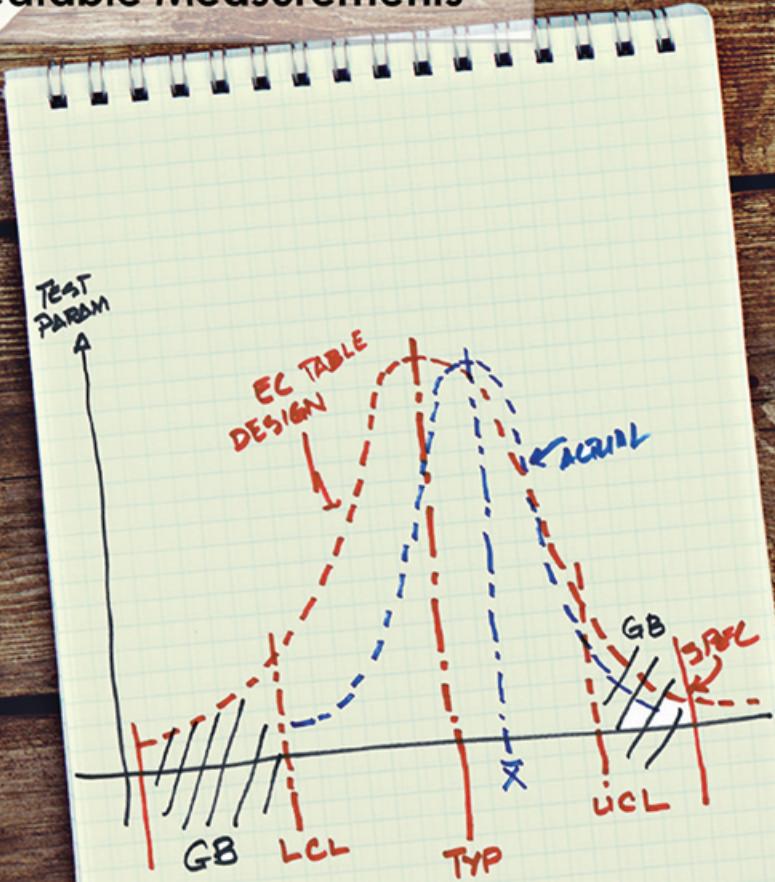
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