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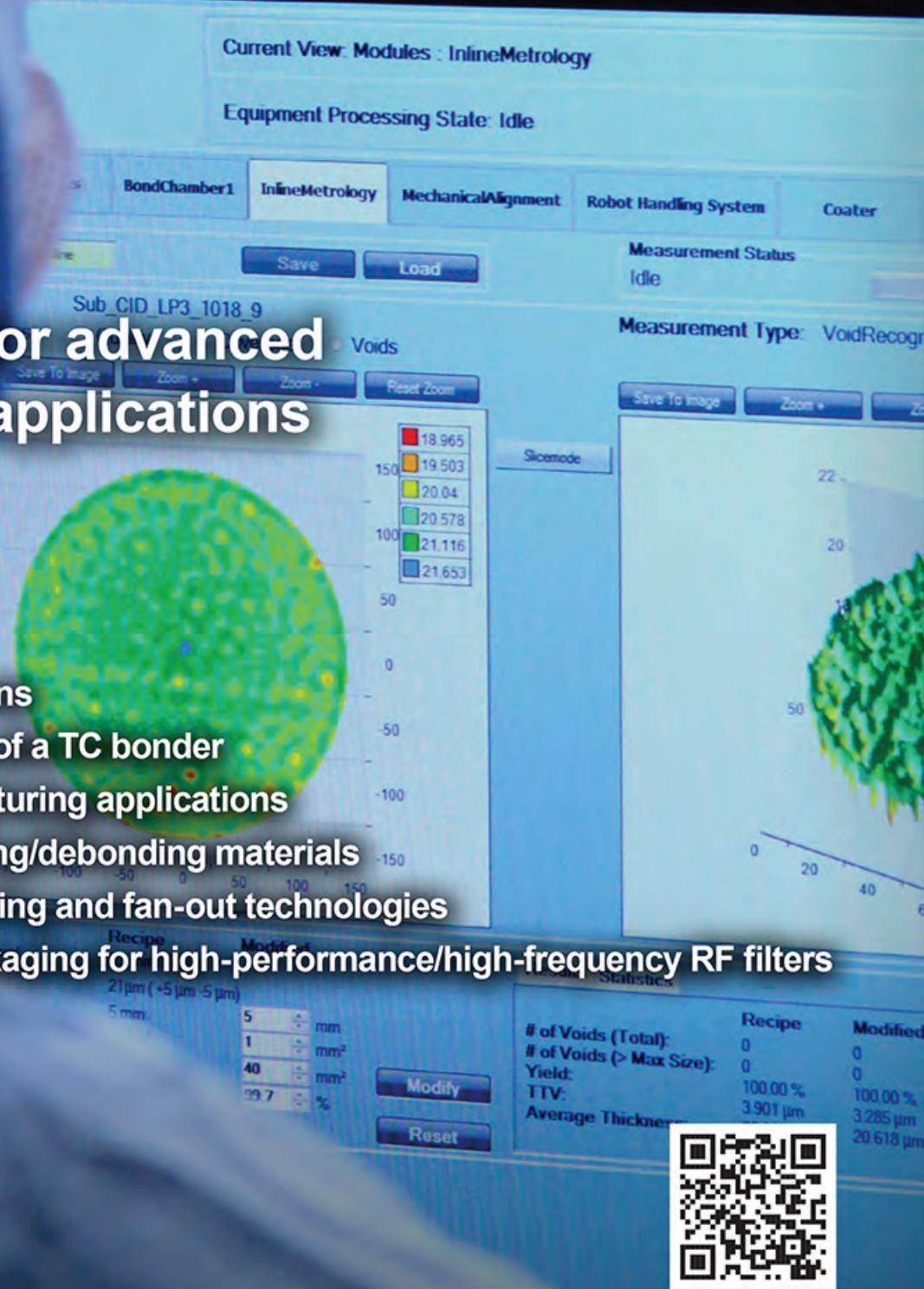
Volume 21, Number 2

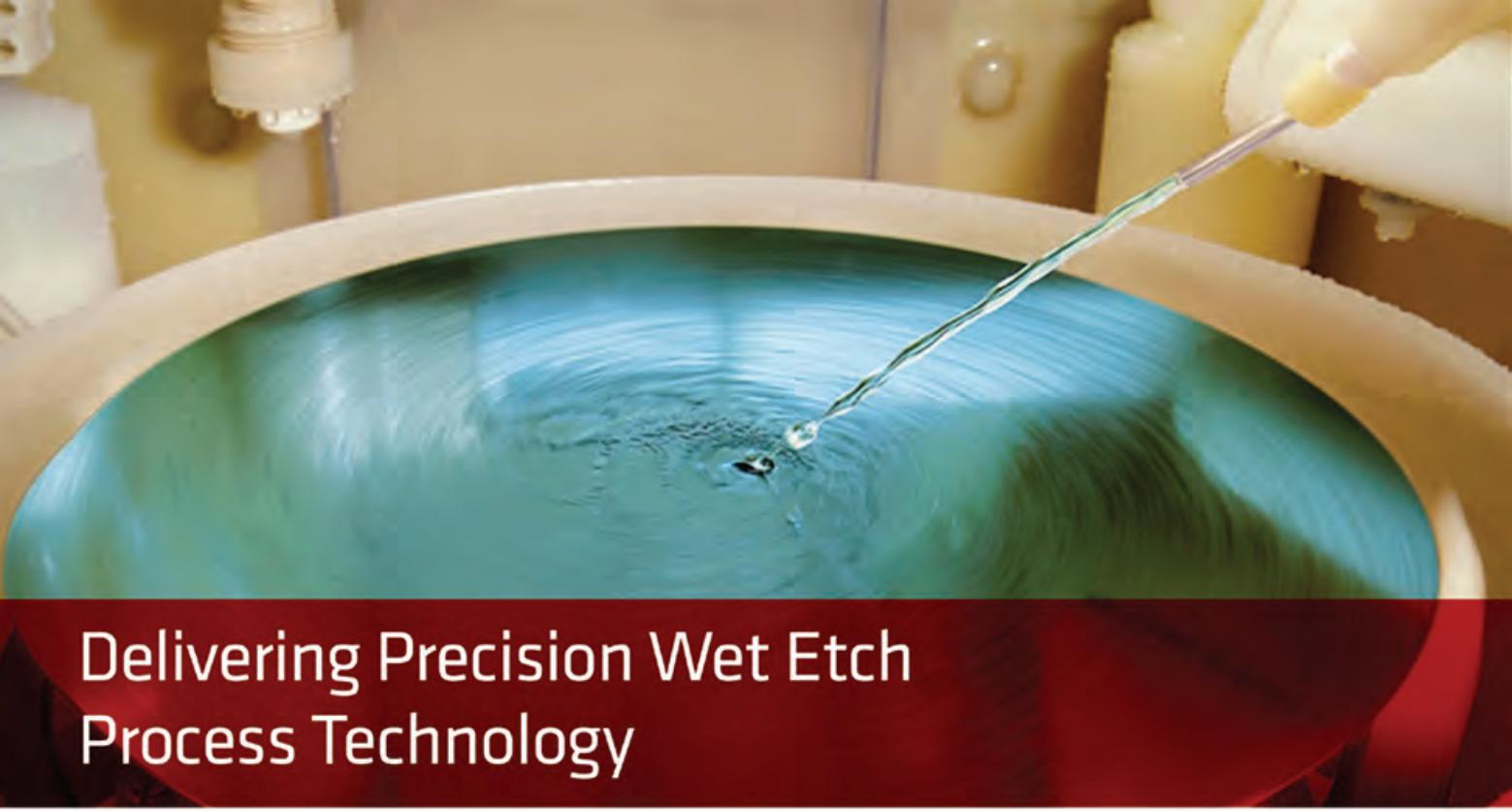
March • April 2017

Metrology for advanced packaging applications

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- Additive manufacturing applications
- Temporary bonding/debonding materials
- Future of embedding and fan-out technologies
- Glass-based packaging for high-performance/high-frequency RF filters





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The cover shows a tool operator measuring the total thickness variation of an adhesive interlayer of a temporary bonded wafer by taking 280,000 measurement points. For thickness measurements, a high number of measurement points is needed to achieve proper accuracy. Local deviations, such as particles within the bond interface, have a significant effect on the subsequent thinning process, which can lead to wafer breakage and tool downtime.

Cover image courtesy of EV Group

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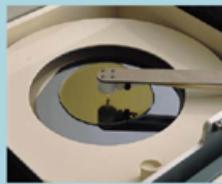
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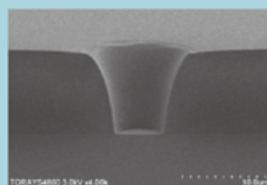
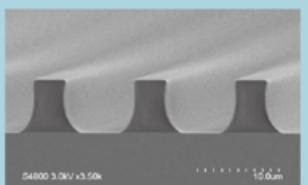
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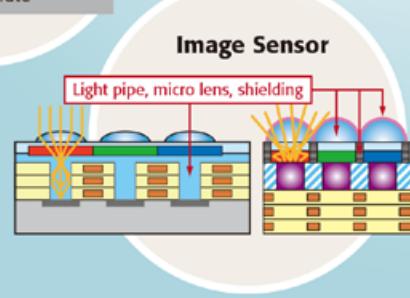
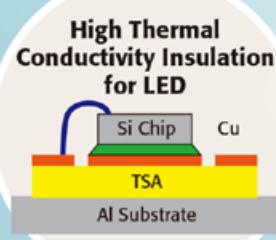
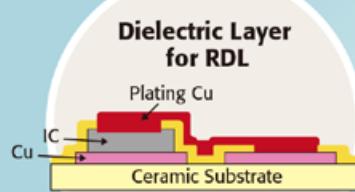
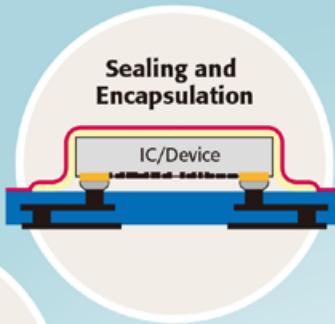
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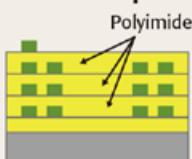
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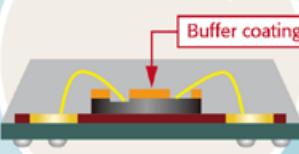
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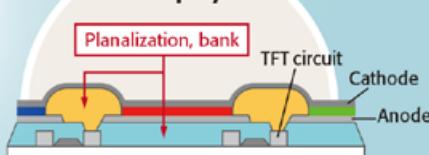
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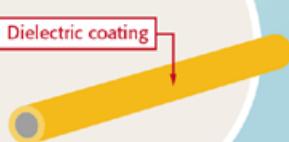
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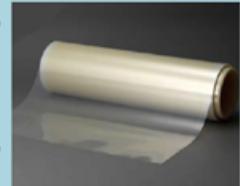
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Challenges and opportunities for OSATS in today's semiconductor market

By Scott Sikorski *[STATS ChipPAC]*

The maturation of the semiconductor industry is evident from its recent anemic growth—averaging 2.1% per year from 2010-2015 and 2016 producing a similar result. While the analyst community is ever optimistic about better growth numbers for 2017 and beyond, there are no major electronics platforms with enough short term growth prospects to really fuel the semiconductor market beyond its recent norms. Semiconductor companies are keenly aware of the stagnant growth environment in which they are operating, and are reacting in two fundamental ways: 1) consolidating and 2) pursuing higher level solutions.

Industry consolidation

Industry consolidation is occurring at a faster pace throughout the semiconductor supply chain and is reshaping the entire landscape. Fabless and integrated device manufacturers (IDMs) alike have utilized mergers and acquisitions (M&A) to strengthen their position in the market. Because by definition they outsource all of their manufacturing needs, fabless semiconductor companies are especially important to the outsourced semiconductor assembly and test suppliers (OSATS). In 2010, the top 10 fabless semiconductor companies represented approximately 61% of the total fabless segment. By 2015, the top 10 accounted for 68% of the total, representing tremendous market concentration for the OSAT community with important ramifications to pricing and technology roadmap – either you're aligned with these top 10 or you're in trouble!

Semiconductor industry consolidation has another impact on the OSATS. Most companies have a well-disciplined strategy involving a

certain diversity of OSAT supplier base that weighs having enough suppliers to ensure vigorous competition on pricing, but not an unmanageable number of suppliers with small volumes and higher pricing. However, through M&A, a company may find that they suddenly have 10-20 OSATS supporting them and the long slow process of streamlining the supply chain to a more optimal number begins, but with important implications for the OSATS. The OSATS best positioned are those with the scale and diversity of capability to service a broad spectrum of the semiconductor company's business. Smaller OSATS with more limited offerings have a tough time creating a value proposition.

Integration trend

Looking at the messaging to Wall Street of many top semiconductor companies, a recurrent theme is providing higher level solutions to their customers. Packaging is a strategic enabler and companies are increasingly looking to their supply chain partners to enable highly heterogeneous and differentiated integrated solutions for their new end products. The Internet of Things (IoT) is an example of a segment many companies are looking to service with more integrated solutions as a way of differentiating their offerings to boost top line revenue, market share and profit margin gain, otherwise difficult to do in a low-growth market environment.

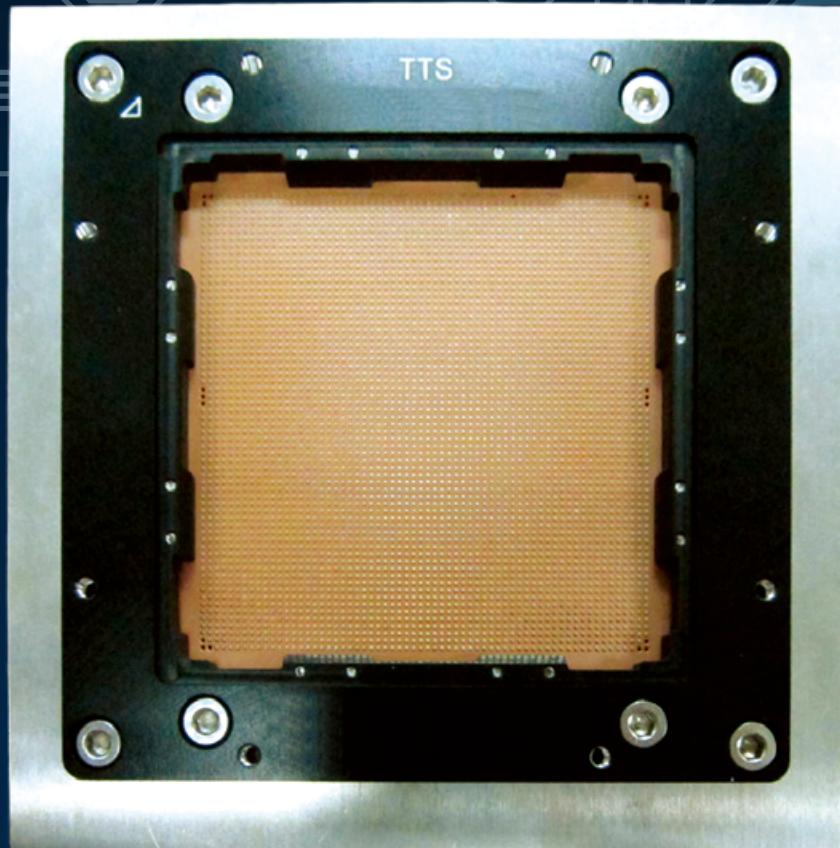
The OSAT implication here is that these higher level solutions often involve multiple heterogeneous devices creating the need for more integrated packaging-level solutions. Because of the diversity of underlying packaging technologies that could

potentially be required, it is the larger OSATS that offer a very broad spectrum of services that are best situated for these semiconductor companies, and so are best positioned for success. With advanced capital intensive technologies such as wafer-level packaging, the barrier to entry becomes very high. Smaller OSATS are not usually in a position to sustain this type of ongoing investment.

While there have been a number of through-silicon via (TSV)-enabled 3D IC approaches designed and discussed by both front- and back-end service providers, it is important to separate the hype from the reality in chip integration in terms of real OSAT revenue impact. The challenge is to provide 2.5D or 3D solutions that can deliver the promised performance at a cost-effective price. Today, there is very little OSAT revenue or high-volume demand for TSV-enabled 2.5D or 3D IC approaches relative to the \$25B OSAT market.

OSATS with the ability to invest in advanced integration technology such as fan-out wafer-level packaging (FOWLP) and other advanced system-in-package (SiP) platforms are able to provide customers with a 2.5D/3D solution that is more cost effective and infrastructure-friendly than specialized TSV approaches. In fact, we see integration platforms like FOWLP and SiP as the new growth engines for the OSAT industry based on three major market drivers: 1) mobile devices (such as power amplifiers, digital baseband, WLAN, GPS modules and Bluetooth®); 2) organic growth in traditional SiP applications such as RF front-end modules; and 3) emerging market segments such as IoT, wearables, MEMS, sensory modules and infotainment.

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FOWLP

FOWLP — also known as embedded wafer-level ball grid array (eWLB) — delivers product advantages to customers in terms of higher reliability, higher performance, better high-frequency performance, higher bandwidth and thinner package profiles. No other integration packaging technology in high-volume production today provides the flexibility and integration density, with die-to-die, die-to-passives, and passives-to-passives placement as eWLB.

Figure 1 shows the flexibility of eWLB as a packaging platform that can extend into 2.5D/3D designs. We have been in high-volume production with eWLB for over 7 years now, delivering over 1.3 billion units to an increasingly diverse customer base. NANIUM S.A. is also in high-volume production of eWLB and Nepes is in production with an ex-Freescale RCP technology. ASE is reported to now be shipping eWLB product too. These are today's main OSAT options and several other companies are now working on various fan-out approaches, but are not in volume production yet.

FOWLP manufacturing lends itself to the use of high-density wafer carriers as well as panel-level processing. Today, all high-volume manufacturing, including the TSMC InFO approach, is on 300mm or greater round carriers, which will likely continue to be the dominant process for the foreseeable future. For applications that would require larger body sizes and/or relaxed ground rules, panel-level processing is an option. There will, however, be a package body size below which the industry will not be able to produce favorable economics for panel-level processing. The cross-over point will be dependent on the specific panel-level technology in question.

Unlike the current round carriers that are the OSAT industry de facto standard, there is no such panel-level processing standard evident on

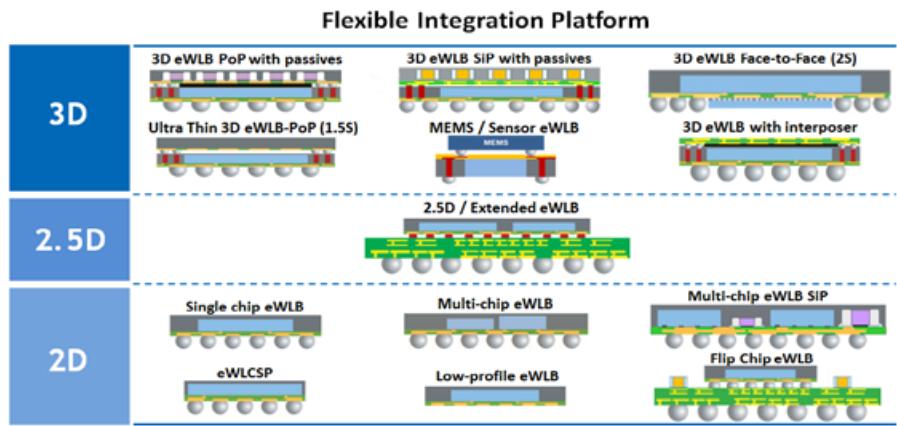


Figure 1: Flexible integration platform.

the horizon. All tier 1 OSATS are working on a panel-based process, although no two are exactly alike. Lack of processing commonality, even down to the lack of a panel size standard, hinders establishment of an equipment supplier base because there will be limited production scale for any given equipment set. For example, while STATS ChipPAC has a proven panel-level process today, we anticipate that the lack of an equipment supplier base, or industry standards in general, will delay panel-level processing from being mainstream for several years.

Investment

FOWLP is a capital-intensive manufacturing process, requiring access to financial resources that are often difficult for smaller OSAT players. We mitigate the typical high costs through our FlexLine™ method where we can produce both fan-out and fan-in wafer-level packages on the same manufacturing line. This loading flexibility is critical to ensuring very high equipment utilization rates—the key to maintaining a cost advantage in the market.

Advanced SiP technology is also capital intensive and requires a highly integrated and automated manufacturing line. Leading OSATS have made significant investments in SiP capability. For example, we

recently opened a dedicated advanced SiP facility in South Korea to exploit the burgeoning market need for such technology. Only OSATS that have strong FOWLP and SiP capabilities can expect robust top line revenue growth given the stagnant underlying semiconductor market. These technology trends may then accelerate the concentration of OSAT revenues in the top three OSATS – Holding Company (ASE/SPIL), AMKOR, and JCET Group – which all have the technology and resources to maintain the pace of capability and capacity expansion demanded by the top semiconductor players.

It is not clear, however, that this will necessarily drive near or even mid-term OSAT consolidation. Most OSATS other than the top three are heavily dependent on wire bond technology and, while not growing much, wire bond remains by far the dominant interconnect technology used and will continue to be so for years, if not decades. Smaller OSATS with modern wire bonder fleets and some wafer-level chip-scale packaging (WLCSP) and test capability may survive, if not thrive, for a long time. Also, there is limited rationale for the Tier 1 OSATS to acquire these smaller players. Whereas, there may be the rare case of a Tier 1 OSAT acquiring a small player for technology access (e.g., Amkor acquiring NANIUM S.A.), it

will mostly not make sense to acquire a smaller competitor with manufacturing sites diverse from the acquirer because it doesn't necessarily help your scale, which is really measured at the site level more than the corporate level. For these reasons, major OSAT consolidation may lag that which we are seeing in the semiconductor space.

China

With the maturation of the semiconductor industry, there has been little growth in the supply chain in most regions. China, however, is the exception and a key market for the vast majority of semiconductor companies. Historically, the Chinese market has required somewhat less complex technologies than some of the established markets. Today, we see Chinese customers driving advanced technology requirements that are similar to other developed geographies. OSATS expecting to see meaningful top line growth need to be well-positioned with strong technology offerings to locally service the Chinese eco-system. A major part of the rationale behind the JCET Group acquisition of STATS ChipPAC was to enable servicing the local Chinese market. The market reaction 1.5 years into the merger has been exceedingly positive, supporting the idea behind the combination.

What does it mean for OSATS?

Industry consolidation will continue to reshape the semiconductor supply chain. OSATS must be able to provide a full range of offerings including the latest advanced integration technology. With increasing demand for integrated packaging solutions, we expect revenue growth in the OSAT industry is likely to exceed the overall semiconductor industry growth for the next several years. This represents a major opportunity for a select few OSATS with FOWLP and SiP capabilities and capacity. The OSAT leaders need to be in a strong financial position to continually invest in R&D and capacity expansion for integration solutions, primarily in SiP and FOWLP, but also for test. From a regional standpoint, they must have a strong strategy in China. Beyond the ASE-SPIL merger, the OSAT industry may see some on-going consolidation but not anything like at the dizzying pace we've seen in the semiconductor industry. However, we anticipate important milestones to be evidenced by STATS ChipPAC as well as other OSAT providers over the coming year.

Biography

Scott Sikorski received his Bachelor of Science degree from Columbia U. and a Master's degree and PhD in Materials Engineering from Massachusetts Institute of Technology; he is VP, Product Technology Marketing at STATS ChipPAC; email scott.sikorski@statschippac.com.



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High-accuracy metrology for advanced packaging applications

By Elisabeth Brandl, Markus Heilig, Thomas Uhrmann, Thomas Wagenleitner [EV Group]

The semiconductor industry is witnessing a trend toward total control and monitoring of all production processes. Mid-end-of-line (MEOL) and back-end packaging processes face tighter process constraints at levels previously seen only in front-end-of-line (FEOL) wafer processing. With every process step there is a risk of error, affecting the whole wafer or individual dies on it. This is creating an urgent need for highly accurate metrology both in stand-alone equipment as well as integrated into process equipment that can provide critical process data quickly and cost-effectively.

For example, before nonreworkable processes, such as wafer thinning after temporary bonding, high-accuracy metrology with a feedback loop leads to an increase in yield through more accurate thinning and process optimization decisions. In this case, non-destructive and high-throughput infrared (IR) metrology integrated into process equipment is ideal for permanent and temporary bonding applications as it offers thickness measurements, verification of homogenous bond lines and void detection. For chip or wafer stacking, as well as for lithography applications, alignment verification implemented in stand-alone equipment is useful in generating correction parameters for the alignment process itself.

Process control

Metrology tools can be versatile and enable inspection both before and after a given process. Therefore, the influence of a given process on the overall production flow can be determined, which leads to a greater understanding of the process and allows improved process control accordingly. Process control is a key criterion for reproducibility, especially for high-volume manufacturing (HVM).

For bonding and lithography in advanced packaging, wafer alignment and thickness uniformity are critical parameters in the production line. Optical inspection methods offer high accuracy and wide measurement range by employing different wavelengths, making it a suitable measurement method for alignment verification and thickness measurements. To enable sufficient verification, the measurement accuracy must be ten times better than the needed accuracy of the parameter. As an example, verification of 100nm alignment accuracy requires a measurement accuracy of 10nm.

Direct feedback loop for process parameter optimization

Process parameter optimization, like alignment improvement, is an effective way to enhance the yield in production lines and can be realized with a direct feedback loop (**Figure 1**). Metrology consisting of a suitable inspection and analysis is done after the production process step. Correction factors are calculated from the metrology output, which improve the process for subsequent wafers. With this method, the process parameters are constantly improved, which leads to an optimized process. This feedback loop is limited by the metrology accuracy and the precision of the process parameter adjustment.

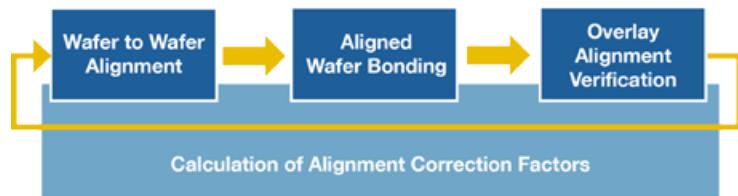


Figure 1: Direct feedback loop for process parameter optimization.

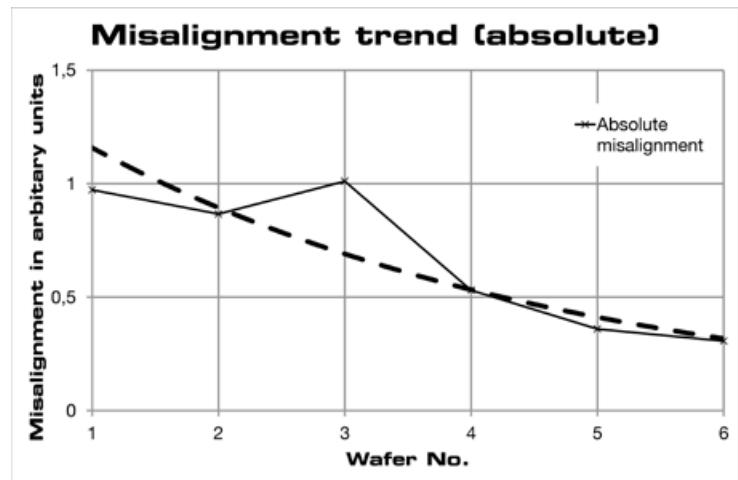


Figure 2: Integrating a direct feedback loop leads to significant alignment improvement within 5 wafers.

One example of a direct feedback loop is using the EVG®40NT metrology tool for alignment verification in combination with the SmartView® bond aligner. The requirement for the alignment in this case is $\pm 100\text{nm}$, which requires a measurement accuracy of 10nm. With the feedback loop from the metrology tool to the aligner, it is possible to achieve significant alignment improvement within five wafers (**Figure 2**).

Another example for this type of feedback loop is spin coating parameter optimization. Some coating materials change their viscosity slowly over time on account of solvent evaporation and other factors. If this solvent evaporation can't be prevented, metrology can help to achieve reproducible coating thicknesses. The thickness of the coated wafers is measured



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and by adjusting the rotation speed of the spin coater accordingly, the next wafer is coated with the optimized rotation speed.

Indirect feedback loop enabling rework

If it is not possible to directly influence the process parameters, or the capability to influence these parameters is not sufficiently precise, there is still an option to avoid unnecessary wafer scrap. Before nonreworkable processes like wafer thinning or etching, a simple pass or fail decision for subsequent process steps can enhance the yield.

In **Figure 3**, an example of an indirect feedback loop for thinning after temporary bonding is described. During temporary bonding, the device wafer is bonded to a handler wafer with the help of an adhesive interlayer. The uniformity of the interlayer has an effect on the thickness uniformity of the device wafer after thinning. This thickness uniformity must be within defined specifications or the wafer ends up in scrap. In this case, a rework process before thinning can be used to enhance the yield for temporary bonding. The value of the total thickness variation (TTV) can be used to make the correct decision. A standalone metrology tool providing multilayer thickness measurement can be programmed to sort the wafers after metrology between wafers that comply with the tight process requirements and those destined for rework.

A different example of an indirect feedback loop is fusion bonding in combination with void detection. Directly after the pre-bond in the fusion bonding process, the bond strength is relatively low, which enables rework by simple mechanical debonding similar to the debonding process for temporary bonding. By inspecting the bond interface for voids, one can determine the need for rework. If no rework is needed, the pre-bonded wafers can stay in the production line and be annealed where the bond strength is drastically increased, thereby preventing further rework.

Influence of the measurement accuracy

Making correct decisions either for process parameter improvement, or for a pass/fail decision with the help of metrology, is the main goal of its implementation into production as well as pilot lines and R&D applications. These decisions are driven by the output

from the metrology and require sufficient metrology accuracy and resolution to keep measurement uncertainties at bay. The required metrology accuracy depends on the parameter specifications needed for a successful process. Higher metrology accuracy is better but often comes with the tradeoff of higher measurement time. This is the reason why HVM metrology

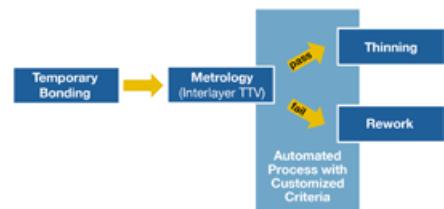


Figure 3: Feedback loop for pass and fail criteria.

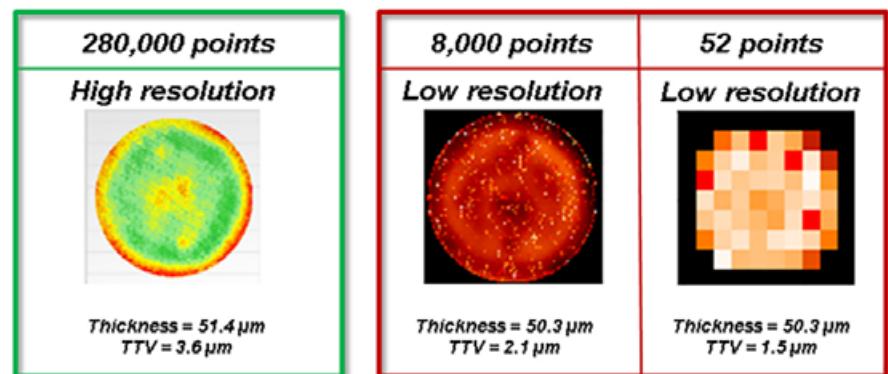


Figure 4: Three TTV measurement systems are pictured. The higher number of measurement points leads to a better picture of the measured wafer, which therefore makes the feedback decision more accurate.

tools have been introduced that offer high accuracy within reasonable times.

In **Figure 4**, the importance of metrology accuracy on making correct decisions is pictured. The TTV of an adhesive interlayer of a temporary bonded wafer was inspected by three different tools that take different amounts of measurement points. The metrology was conducted before thinning, where a strong TTV deviation would lead to wafer breakage. For thickness measurements in particular, it is essential to have a high number of measurement points in order to achieve proper accuracy. Local deviations like particles within the bond interface have a significant effect on the subsequent thinning process, which leads to the worst case of wafer breakage. This not only results in yield loss of the one wafer, but also tool downtime for cleaning. In the example in **Figure 4**, the decision to undergo rework was based on a total thickness variation of at least 3 μ m, because the purpose of the thinning was TSV revelation. The number of measurement points for the three systems was 280,000 points, 8,000 points and 52 points respectively.

When the wafer was measured with 280,000 measurement points on an EVG®50 stand-alone metrology system, a TTV of 3.6 μ m was acquired because

more thickness deviations were observed simply by increasing the measurement point density. Because the TTV was higher than 3 μ m, the wafer was sent for rework. For the measurement systems with 8,000 points the TTV was 2.1 μ m, while for the system with 52 measurement points a TTV of 1.5 μ m was measured. In both cases the measured TTV would have resulted in the decision to further process the temporary bonded wafer, which in this case would be nonreworkable thinning. As the real TTV is higher than what was reported with the low-resolution systems, this decision would have led to wafer breakage. High measurement point density has a higher probability of identifying local deviations like small particles. In wafer thinning, where the trend leads to even thinner wafers, small defects have a particularly strong effect.

Throughput requirements

Because metrology tools help enable cost savings and improve fab profitability by increasing semiconductor yields, the throughput of metrology tools must at least match the throughput of process tools. Metrology cannot be the bottleneck of one's process. The throughput requirement differs depending on whether the metrology step is integrated into the process tool, or implemented in a stand-alone system. If integrated within the production tool, the

metrology throughput should be the same as for the production tool. Putting the metrology outside of the production tool in a stand-alone system provides the opportunity for the metrology tool to monitor several production tools if necessary, and therefore would require higher throughput than the process tool accordingly.

The throughput of the metrology tool comprises the handling time and measurement time, which is usually strongly dependent on the measurement method and resolution. Using nondestructive and non-contact measurement methods is a necessity. Optical inspection systems offer this advantage combined with a high throughput, which is typically only limited by the stage movement. Another advantage of using optical inspection is its versatile nature due to the fact that different wavelengths can measure different material properties. By implementing multiple sensors with different wavelengths, one can enable a highly flexible metrology tool.

Metrology integrated in process tool or as stand alone

Having the metrology integrated within a process tool or as a stand-alone system depends on the manufacturing conditions and requirements. Integrating the metrology tool into the processing equipment has the advantage that the feedback loop has a very small delay, and therefore the corrective actions can immediately affect the next processed wafer. By implementing metrology outside the production tool, the feedback loop is delayed by at least one wafer cassette. These delays have no influence on the process if an indirect feedback loop as previously described is used. The effectiveness of the pass or fail decision does

not rely on process parameter optimization in the upstream processes. For a direct feedback loop, however, it can be important to implement the changes immediately. Besides the delay, the other influencing factor on the choice of integration is the throughput. If the metrology tool is integrated within the production tool, the throughput of the metrology tool is limited by the throughput of the production tool. If the integration is done with stand-alone equipment, one can use the full throughput potential.

Yield enhancement pays off fast

High production yields are already well established in the semiconductor industry. But as the processes become more sophisticated, the value of semiconductor wafers is increasing. This gain in value makes yield loss an even more important topic. As shown in **Figure 5**, annual yield losses are calculated for \$5000 wafers and \$2000 wafers. By enhancing the yield from 99% to 99.9% through metrology at a throughput of 10wph, it is possible to save \$1.3 million annually for a \$2000 wafer. Even this annual saving justifies taking necessary actions toward yield enhancement. For \$5000 wafers this effect is logically even higher leading to annual savings of \$17 million for a throughput of 50wph.

As previously stated, a feedback loop integrated within the process is one way to optimize process parameters. There are basically two options for combining metrology with a feedback loop to enable successful process integration with enhanced yield. One is to have the feedback loop directly influence the process parameters like alignment accuracy or spin coated layer thickness. The other is to create an automatized action that either leads to rework or further processing. By using metrology tools with SECS/GEM interface,

the feedback loop can occur throughout the host's network—making it possible to influence multiple production tools in the same feedback loop.

Conclusion

Successful metrology not only consists of a highly accurate measurement system but also includes a way to influence and improve the process. Today, some processes have been pushed to their limits, making metrology an enabler to achieving high yields. In this article we demonstrated that a yield increase for even already high-yielding processes is a significant cost saver, and introduced two efficient ways to implement metrology within a feedback loop for process improvement. Both the described indirect feedback loop enabling rework and the direct feedback loop for process parameter optimization provide solutions for increasing yields.

Biographies

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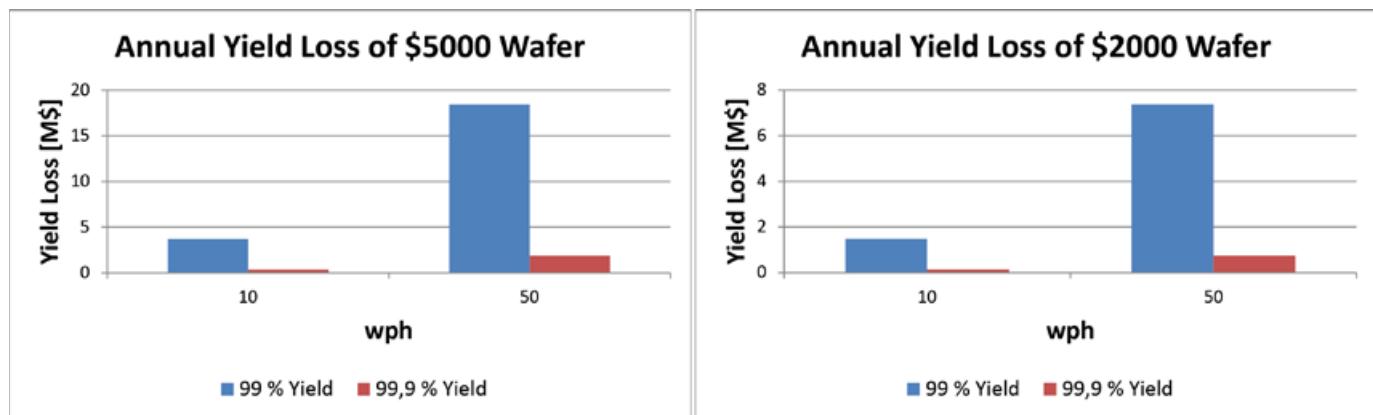


Figure 5: The annual yield loss is pictured for \$5000 and \$2000 wafers calculated for 10 and 50wph manufactured by the monitored process.

Core capabilities of a thermocompression bonder

By Hugo Pristauz, Alastair Attard, Andreas Mayr [Besi Austria GmbH]

Thermocompression bonding (TCB) is now a well-established interconnection technology for 2.5D- and 3D-integrated devices that are built on chip-to-substrate (C2S), chip-to-chip (C2C), or chip-to-wafer (C2W) levels. The maturity of TCB has progressed over recent years, with yield levels greater than 99.8% per attached die. Though industrial interconnect pitches are still found above the 30 μm level, the new paradigms of heterogeneous integration are driving pitches down to 5 μm for stacked ICs (SICs) and down to 1 μm for system-on-chip (SoC) devices. In order to leverage TCB for such advanced interconnection pitches, it is essential to understand the core capabilities of a TCB, which directly contributes to the required high-yield levels. In particular, the complexity of these core capabilities need to be well understood in order to further improve them for high-yield bonding of 2.5D and 3D devices with scaled pitch.

Today, 2.5D and 3D integrated stacked ICs (SICs) are widely adopted, with the main applications being high-performance computing, graphics processors and 3D through-silicon via (TSV) memory [1]. In the case of 3D system-on-chip (SoC) large volumes have been driven in the image sensor area for camera applications [2]. In contrast to 3D-SoCs, where the interconnection is achieved by wafer-to-wafer (W2W) bonding, the assembly of 3D-SICs utilizes C2S, C2C and C2W methods, mostly based on TCB, which enjoys advantages such as known-good-die (KGD) yield benefits as well as enabling greater heterogeneous integration.

TCB process flows

Three process variants of TC bonding have been established for high-volume production. Thermocompression nonconductive paste bonding (TC-NCP) (Figure 1a) is the pioneer of TC bonding [3]. The TC bonder receives a substrate with pre-applied underfill (i.e., the nonconductive paste) that is dispensed upstream of the TC process. The TC bonder picks and flips a die and, after alignment, presses the die into the paste. At this point, the actual thermocompression phase starts. A force ramp is applied in order to squeeze out the

NCP from between the bump's solder caps and the substrate pads, and, furthermore, slightly deforms the bumps to establish good thermal die-substrate contact. In parallel, a temperature profile is applied in order to melt the solder and to cure the NCP.

Initially, the NCP is cured sufficiently before solder reflow, allowing the NCP to provide a sufficient reaction force to prevent a sudden collapse of the die once the solder cap melts. After a certain dwell time, the solder melts and forms the joint to the pad on the substrate side, while the NCP continues to cure completely. At this point, the bond is complete and the bond tool can immediately release the die, cooling down in parallel while fetching and aligning the next die. Throughout the process, the stage heating is controlled to maintain it always at a constant temperature. Keeping these few principles in mind, the bond control for TC-NCP is quite simple. The selection of NCP is critical for the achievement of a reliable interconnect [3]. With long-term availability of suitable NCP materials (more than 6 years), the TC-NCP process is robustly applicable in many areas.

For ultra-thin (e.g., 20-50 μm) die, however, the NCP bleed-out is very hard to control in order to avoid NCP climbing up the die edges and contaminating the bond tool. This is essentially the reason why TC-NCP has not been considered for 3D memory production, besides the lack of available NCP that is compatible with extra low-k (ELK) dielectrics used in advanced CMOS nodes.

These drawbacks of TC-NCP were the main reason why thermocompression capillary underfill (TC-CUF) has been introduced for high-volume TCB production (Figure 1b). With the TC-CUF process, CUF is applied downstream from the TC bonding step, therefore, no underfill is present during bonding. In most cases, flux dipping is applied after die flip, although

other methods such as upstream spray fluxing onto the substrate also exist. After the die is dipped in flux, it is bonded onto the substrate again with the use of force and temperature profiles. The absence of underfill during solder reflow comes with serious challenges for bond control, which will be explained later in detail. It is worth mentioning that TC-CUF is the most widely deployed TC bonding process on the market with an estimated 200 TC bond heads running TC-CUF for high-volume manufacturing of hybrid memory cubes and computing/server logic.

The application space for TC-CUF is considerably wider than that for TC-NCP. TC-CUF is capable of memory cube production, and compatible CUF materials are readily available at high maturity levels. However, TC-CUF has one big disadvantage: it cannot be used as a basis for collective TC bonding processes, which promise a TC bonding cost reduction by a factor of five [4].

The requirements for collective TC bonding are supported by a nonconductive film (TC-NCF) (Figure 1c). In this process, a non-conductive film-based underfill (NCF, sometimes called WLUF, i.e., wafer-level underfill) is applied at wafer level [5].

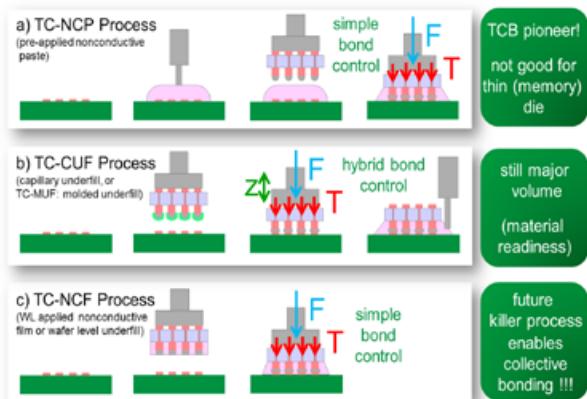


Figure 1: Different TCB process flows.

The basic process runs similar to TC-NCP, although underfill is present on the die side rather than on the substrate side. This means that the NCF is directly exposed to the TC bonder tool temperature, and therefore, die



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fetch and die transport have to happen at a moderate temperature in order to avoid NCF pre-curing. Bond control itself is a simple force control with parallel temperature control, similar to TC-NCP control. Because of its simplicity, detailed TC-NCF bond control is not considered in this context.

Challenges to be mastered

Realizing that the cost of a TC bonder is twice the cost of a mass reflow flip-chip bonder, and TCB throughput is a factor five lower, one might ask in what way a ten times cost increase of TCB is affordable. To understand the justification of TCB, it therefore makes sense to appreciate which kind of packaging challenges are being solved by this bonding method (**Figure 2**).

One of the major strengths of TCB comes into the scene when warped dies or warped substrates are involved, which in both cases are yield killers for mass reflow processes, leaving non-wetted joints in the interface. Clearly the TCB process solves this issue by running a local reflow per bond while clamping the warped substrate flat on the stage and keeping the die by vacuum flat on the bond tool until completion of solidification at the end of the local reflow process. It should be obvious, however, that this process can only work for coplanar bond tool and stage.

The warped die challenge dominates in 3D TSV-memory production: when the hybrid memory cube was introduced the die thickness stood at 50 μm , and roadmaps indicate die thickness scaling down to 20 μm in the short term. The production of mobile application processors, however, are also exhibiting a trend for reducing die thickness. This can be observed through the packaging challenges currently being faced to overcome thickness restrictions of PoP packages, which is partly addressed by thinning down the application processor die.

Another challenge that brings TC bonding into the scene is related to ultra-fine interconnection pitch. Besides the obvious logic that finer pitches require higher placement accuracy, another key challenge is based on the fact that the solder cap volume of a copper pillar bump scales down with the third power of the pitch. As a consequence, the available solder volume to make up for the unevenness of the surfaces due to warpage is greatly reduced and the process windows for co-planarity requirements get drastically smaller (**Figure 3**).

Another effect observed with ultra-fine pitch is solder bridging that occurs when bond control is not capable to keep solder joint thickness reliably above a minimum level. This occurrence is particularly predominant if bond control of a TC-CUF process is not accurate enough. In such a case, upon solder reflow, the bond head is too slow to maintain the correct gap between the die and substrate, resulting in a rapid bump collapse causing bad solder joints, which can be categorized into three types of defect (**Figure 2**):

1. The solder of two neighboring bumps is squeezed out and forms a solder bridge, thereby resulting in a shorted connection.
2. The solder is squeezed out of the joint and climbs up the copper pillar, leading to a lack of solder volume in the joint, which leads to reliability issues.
3. The solder is squished asymmetrically out of the joint, which ends up in a lack of solder volume at one position of the joint, leading again to reliability issues.

A major reason to introduce TC bonding for C2S packaging was to avoid cracking of ELK dielectrics, which are more brittle and less resistant to mechanical stress. For mass reflow processes, such materials are facing two kinds of issues. First, because of the absence of underfill, the whole mechanical stress induced by CTE mismatch during cool down has to be managed by the localized region of ELK dielectric under the bumps. Second, in

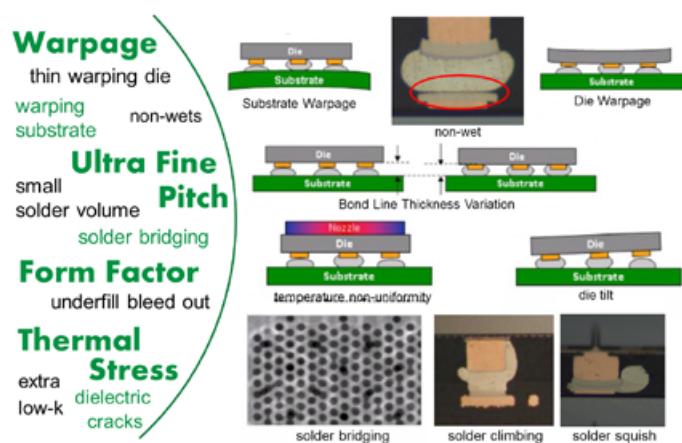


Figure 2: Challenges being mastered by TCB.

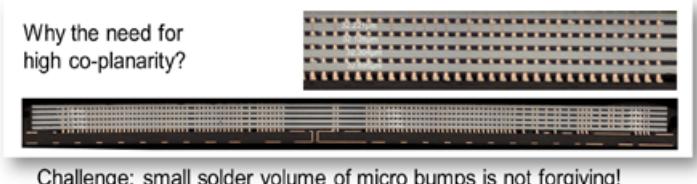


Figure 3: Cross section of an ultra-fine pitch bond.

public source: IMEC	3D stacked IC		3D system-on-chip		True 3D IC	
	wiring level	3D-SIC	Semi-global	Intermediate	Local	FEOL
2-tier stack						
Contact Pitch Relative density:		40 \Rightarrow 20 \Rightarrow 10 \Rightarrow 5 μm $1/16 \Rightarrow 1/4 \Rightarrow 1 \Rightarrow 4$	5 \Rightarrow 1 μm 4 \Rightarrow 100	2 $\mu\text{m} \Rightarrow 0.5 \mu\text{m}$ 50 \Rightarrow 400	200 \Rightarrow 100 nm 5000 \Rightarrow 10000	< 100 nm > 10000
Partitioning		Die	blocks of standard cells		Gates	Transistors

Figure 4: Imec's fine-pitch roadmap.

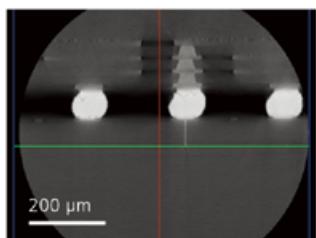
a traditional reflow oven, the same level of temperature is applied to both die and substrate, which results in high stress due to different thermal expansions, i.e., CTE mismatch. TC bonding has two approaches to master thermally-induced stress issues. First, a TC-NCP or TC-NCF process can be selected, which comes with the help of pre-applied underfill (NCP or NCF) that at the end of the reflow phase is sufficiently cured to absorb mechanical stress during solidification and cooling. Second, die and substrate temperatures are set separately in a TC bonding process, which is a means to minimize thermal expansion mismatch-induced stress.

If form factor of a side-by-side multi-chip module (MCM) is of importance, and design rules for flip-chip placement prohibit narrow

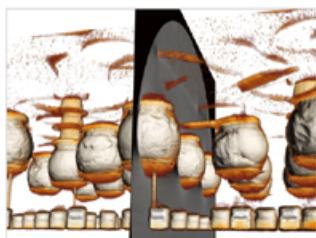
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die-to-die gaps, then with a TC-NCF approach, the gaps can be minimized down to 50 μm because of better bleed-out control of the NCF.

To summarize, there are a couple of challenges mainly driven by warped die/substrate, ultra-fine pitch, brittleness of ELK materials and bleed-out limited form factor, which can be overcome by utilizing TC bonding.

Heterogeneous integration roadmap

To understand future semiconductor requirements, a common roadmap such as the ITRS roadmap would be helpful to provide critical information about the next-generation of semiconductor devices. The ITRS roadmap, however, has been stopped with the final edition published in July 2016, and now we ponder about which key enabling technologies will drive the next wave of semiconductor advancement. Visionaries throughout the whole semiconductor industry agree that new paradigms have to be established where heterogeneous integration based on 2.5D/3D-SIC and 2.5D/3D-SoC technologies will play the key role [6].

One of the key challenges of heterogeneous integration is related to the device interconnection, where ever finer pitches need to be managed. This can be seen in imec's roadmap (**Figure 4**), which is published in the framework of its 3D program [7]. While the industrial pitch is still above the 30 μm level, the imec roadmap for 3D-SICs starts at 40 μm going down to 5 μm . Current TC bonding activities related to imec's 3D program are using test chips supporting 10 μm pitch structures, requiring a placement accuracy of 2 μm at the 3 σ level (**Figure 5**).

The next steps will tackle 5 μm pitch bump structures with a C2W accuracy requirement of 1 μm at 3 σ . For the 3D-SoC roadmap, the challenges are even greater, where pitches start at 5 μm and go down to 1 μm . Current production of heterogeneous integrated SoCs is based on W2W bonding methods, with CMOS image sensors being a good example of where this technology is already applied in mass production based on a W2W oxide bonding process [2]. For yield reasons and known-good-die aspects, the target is to implement SoCs also at the C2W and C2C levels with pitch roadmap targets down to 1 μm .

A means to implement heterogeneous integration is the chiplet- (or dielet-) based approach, which makes extensive use of a C2W-level 2.5D assembly of standardized chiplets on an interposer. CEA-Leti proposed such an approach and claims that for a 20 μm

pitch, TC-NCF is still a feasible technology, however for applications requiring finer bump pitches from 10 μm down to 1 μm , a direct bonding approach is proposed.

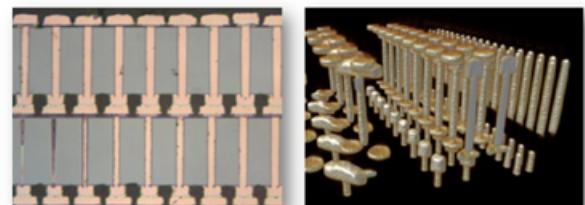
A similar approach is proposed by UCLA without claim of proper interconnection technology, but mentioning that for the pitch range of 2 μm to 10 μm a sweet spot can be expected, further commenting that the interconnection will be the key challenge.

TCB core capabilities

As of yet, it is not entirely clear whether TCB is a suitable bonding method for next-generation pitch targets. A better understanding of the TC process is needed to determine if it can be realistically adopted for high-volume and high-yield C2W- and C2C-based stacking of fine-pitch SICs and SoCs.

Facing such challenges, one is urged to think about the following: 1) What are the core capabilities of a TC bonder, specifically those capabilities that are responsible for creating a high yield process? And 2) What are the approaches, and the associated difficulties, to improve these capabilities in order to be ready for the next step of the pitch scaling roadmap?

Studying the introduction carefully, one comes to the following conclusions: 1) On account of pitch scaling, higher placement accuracy is needed; and 2) On account of the smaller solder volumes (even total absence of solder for direct Cu-Cu bonds), the coplanarity requirements are crucial; and 3) For avoiding solder squeeze-outs, solder climbing and solder squishing, a proper bond control is required. Additionally, an excellent uniformity of the tool temperature distribution is necessary to avoid the possibility that some joints are not formed because of localized cold spots, which therefore meant that solder reflow is not occurring at these locations. In fact, the following four capabilities have been identified to be the core capabilities of a thermocompression bonder: 1) Accuracy; 2) Coplanarity; 3) Bond control; and 4) Temperature uniformity. These are the capabilities that are responsible for maintaining a high yield, which as mentioned earlier, is expected to be greater than 99.8% per TC bond in high-volume production.



10 μm pitch TC-NCF C2W face-up stacked die

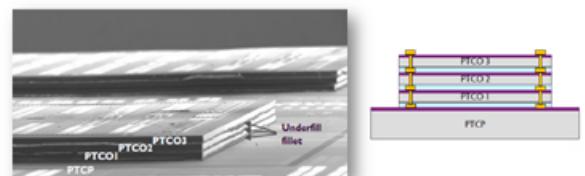


Figure 5: Current imec focus on 3D SICs with 10 μm pitch.

References

1. B. Black, "Die stacking is happening," European 3D TSV Summit, Grenoble 2015; pp.: 1-27.
2. T. Nomoto, "Image sensor technology evolution for sensing era," 3D ASIP Conf., 2016; pp.: 16-23.
3. M. Lee, et al., "Study of interconnection process for fine-pitch flip-chip," 2009 Elect. Comp. and Tech. Conf. pp.: 721-722.
4. A. Attard, "Productivity improvements on thermo-compression bonding," European 3D Summit, Grenoble 2017, pp.: 13-16.
5. T. Wang, et al., "Thermal compression bonding of 20 μm pitch micro bumps with pre-applied underfill — process and reliability," IEEE 17th EPTC Conf. 2015; pp.: 791-796.
6. W. R. Bottoms, (IEEE CPMT): "Innovations in packaging will enable the IoT world of the future," IEEE 18th EPTC Conf. 2016; p. 1.
7. P. Absil, "Overview of the 3D landscape and challenges," Semicon Korea Conf. 2016; p. 23.

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Future of embedding and fan-out technologies

By Rao R. Tummala, Venky Sundaram, P.M. Raj, Vanessa Smet, Tailong Shi [Georgia Institute of Technology]

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Embedding and fan-out are two different technologies, but they can be combined into one at either wafer-level, panel- or board-level. All the packaging technologies can be classified into four types as shown in **Figure 1**: a) wafer-level packaging, b) embedded packaging, c) fan-out packaging, and d) embedded and fan-out packaging.

Embedding and fan-out technologies

Wafer-based packaging is emerging as a strategic and dominant packaging technology because of its many benefits. It started as a wafer-level packaging technology by simply redistributing the back-end-of-line (BEOL) wiring on wafers in the wafer fab and placing solder bumps on the entire wafer, and then singulating the packaged ICs, ready for board assembly. This WLP is a single unit with a continuum of interconnections from transistors to BEOL, to redistribution layer (RDL), and to solder bumps. All WLPs are chip-scale packages with chip and package sizes nearly the same. This is the best package electrically. But it is limited to small ICs and to small packages, typically below 5mm. As such, it is limited in external I/Os to connect to the board, typically at 400 microns in pitch.

To eliminate the board-level I/O limitation of WLPs, wafer fan-out technology was developed. The fan-out means fanning out of I/Os beyond the footprint of the IC in the package. Fan-out technology, by itself, is not new; in fact, most of the billions of packages since the 1970s are manufactured annually as fan-out packages. **Figure 1c**, a ball grid array (BGA) package – one of the more recent packages – is an example of a fan-out package. These are manufactured, however, not as round wafers in the wafer fabs, but as strips, panels or boards, in package and board foundries. The “embedding” technology, as shown in **Figure 1b**, began to emerge as another paradigm in packaging. In this technology, RDL wiring is directly deposited on reconstituted ICs into 200 or

300mm round wafers by molding them with epoxy-based molding compounds. Embedding means the chip is embedded or buried inside the package or board and the interconnections are made to and from these buried ICs using either wafer BEOL tools or package tools. The new trend, often referred to as wafer fan-out (WFO), includes both of these technologies at wafer-level. It should really be called embedded wafer fan-out (eWFO) as is done in this article. Such a concept of a combined fan-out and embedding, as shown in **Figure 1d** was originally developed in the 1980s by GE for military applications, and then followed by many others including Intel as bumpless build-up-layer (BBUL), Freescale as redistributed chip packaging (RCP), and more recently, further developed by Infineon as embedded wafer-level packaging (e-WLP), and manufactured by STATS ChipPAC, NANIUM S.A., and others.

eWFO technology, however, is not wafer-level packaging, as described above. It is packaging of singulated ICs that are reconstituted back into 300mm wafers and addressing the I/O limitation of WLPs at board level. It is also an embedded packaging technology with more benefits than simply fan-out, such as reduced package thickness, and not requiring assembly because the wiring is deposited directly on the surface bond pads of ICs. It has high I/O density at chip level, the shortest interconnections between IC and the RDL wiring, and is an ultra-thin package. eWFO, however, has many challenges in applying it to next-generation needs, as summarized below:

- Die placement accuracy, die shift and die pad coplanarity;
- Molding compound shrinkage and wafer warpage due to molding compounds;
 - Limited RDL scaling in contrast to the potential of BEOL scaling and pitch;
 - High electrical loss of EMC and

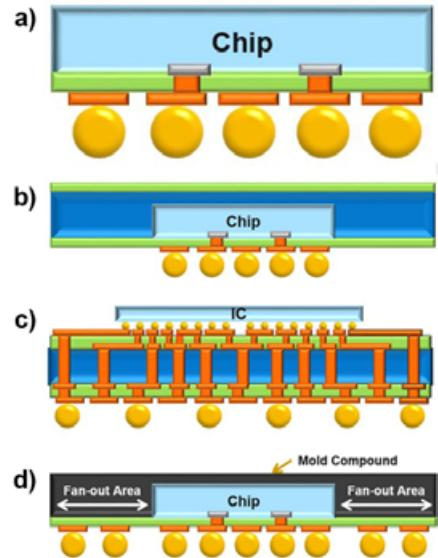


Figure 1: Four types of packages: a) wafer-level package (WLP); b) embedded package; c) fan-out package; and d) embedded and fan-out package.

RDL dielectric loss;

- Outgassing of RDL polymers during sputtering;
- Board-level reliability;
 - Limited to small-to-medium size ICs and packages;
 - Difficulty in IC removal and repairability of high-value single chips or multi-chips; and
 - High cost for large size packages beyond 20mm in size.

The concepts of embedding and fan-out have many applications, as described below. All applications benefit from embedding while fan-out benefits mostly higher I/O applications such as packaging of processors and other logic devices. Independent of eWFO, panel- and board-based embedding is emerging as a very high throughput and lower cost technology that is bound to move up to higher I/O fan-out capabilities, as described in this article.

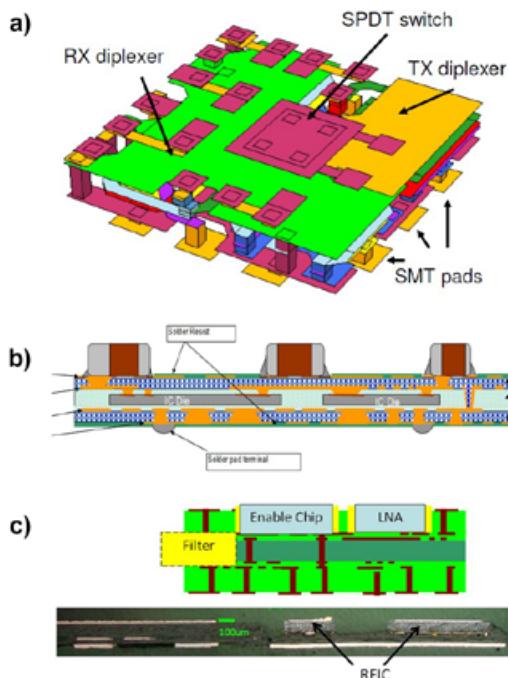


Figure 2: a) LTCC WLAN module (EPCOS); b) embedded actives in TDK's SESUB; and c) Georgia Tech's embedded chip-last actives and passives (EMAP) in an organic package.

Embedding and fan-out of RF and millimeter wave modules

The primary motivation for embedding, fan-out, or both for RF packaging, is to reduce the package footprint, thickness, and shorten the interconnection length for improved electrical performance. Embedding started with low-temperature co-fired ceramic (LTCC) substrates. RF components such as capacitors, inductors, filters, diplexers and impedance matching networks have been embedded into ceramic substrates. EPCOS demonstrated dual-band WLAN front-end modules in LTCC substrates, as shown in **Figure 2a**, with substrate-embedded receiver (Rx) and transmitter (Tx) diplexers. The single-pole double-throw (SPDT) switch in this module was assembled on top of LTCC substrates to reduce package size, and improve loss with high rejection attributes [1].

The second-generation of embedding is with organic laminates. TDK developed a leading-edge module technology called semiconductor embedded in substrate (SESUB), which enabled multi-functional and miniaturized solutions for RF applications [2], as shown in **Figure 2b**. Multiple semiconductor chips are embedded side-by-side in a fully-molded laminate, but with backside device surfaces accessible for cooling.

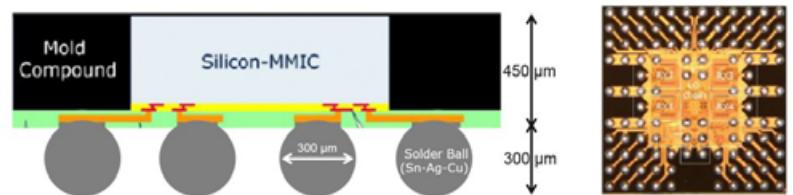


Figure 3: Infineon's eWFO for 77GHz automotive radar.

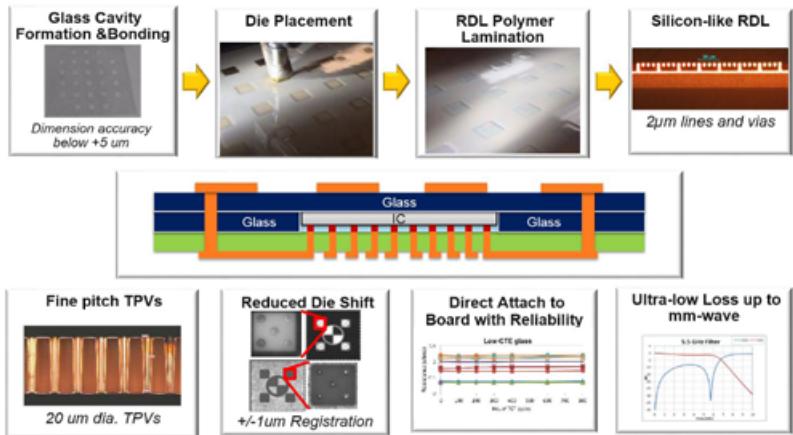


Figure 4: Georgia Tech's approach to embedding and fan-out with glass fan-out (GFO) at wafer- or panel-level.

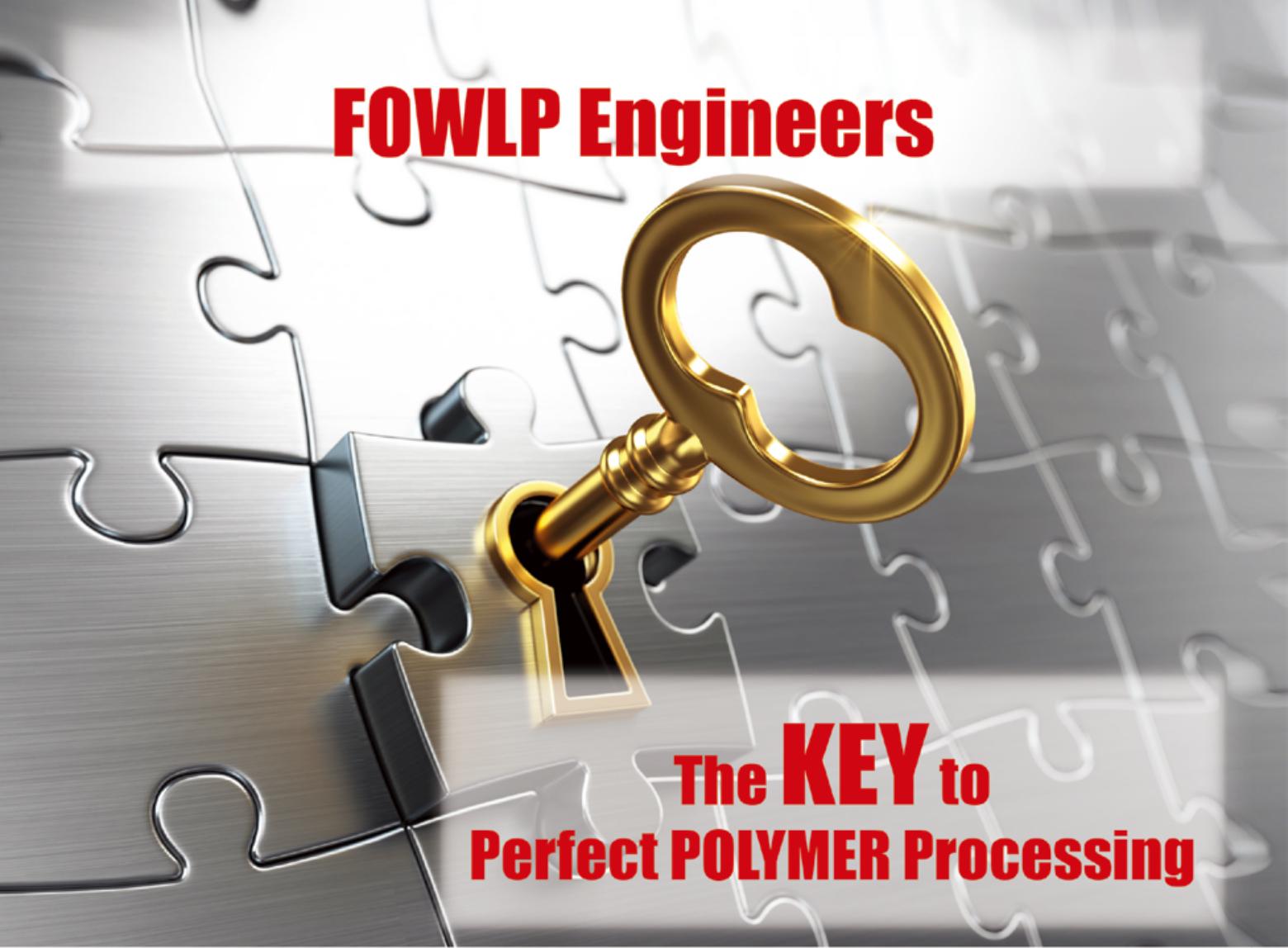
The substrates, with embedded 50μm thin ICs, are as thin as 300μm or less, on top of which discrete components are assembled. Georgia Tech further advanced this concept as shown in **Figure 2c** with chip-last embedded and fan-out for power and RF modules. In this approach, the core and build-up layers of the substrates are also used to embed thin-film passives such as filters, along with RDLs and transmission lines. Build-up layers with laser-ablated cavities are laminated onto these core layers. ICs were assembled into these cavities with low-temperature Cu-to-Cu bonding at a temperature of 160°C with ultra-short copper bumps (<10μm). This is one of the first low-temperature Cu-Cu interconnections and assembly processes in the industry [3]. The low-noise amplifier (LNA), power amplifier (PA) and switch were embedded inside prefabricated cavities in organic substrates [4] to form RF modules and power modules with embedded power management ICs (PMIC), benefiting from the high current handling of copper interconnections without solder. Georgia Tech's embedded active and passive (EMAP) concept of such an embedded RF module is shown in **Figure 2c**.

Millimeter wave applications. Performance requirements and associated substrate design challenges are more

stringent for mm-wave than for RF applications. The primary reason for this is the sensitivity of mm-wave performance to dielectric loss, circuit precision, and substrate parasitics. This situation led to the shift from traditional organic packages to eWFO ball grid array packages to lower the interconnection length and enhance the performance [5]. One such example is Infineon's transceiver bare die for 77GHz automotive radar application [6] as shown in **Figure 3** [5].

Georgia Tech is developing the next-generation of radar with advances in both SiGe devices, by including LNA to improve linearity, and in embedded fan-out by pioneering inorganic fan-out using ultra-thin glass. The glass fan-out (GFO) approach has many superior attributes over current eWFO technologies described above. A schematic of a GFO mm-wave package, shown in **Figure 4**, is a hermetic glass-on-glass structure without molding compound and its problems, listed above. It achieves BEOL-like precision RDL ground rules, currently at 2 microns lithography. **Figure 4** shows other benefits of GFO that include excellent temperature coefficient of expansion (TCE) matching throughout the structure, and therefore, high reliability even with large ICs, low electrical loss, and directly-attachable to the board, without a BGA package. Georgia Tech demonstrated

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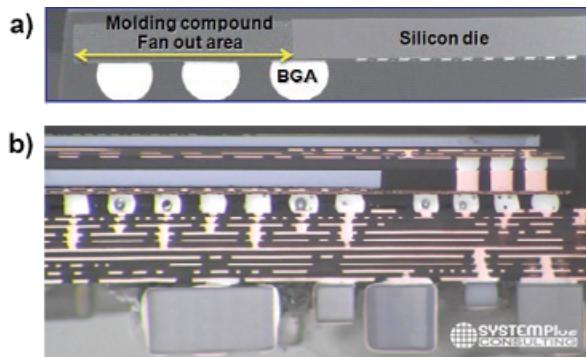


Figure 5: a) TSMC InFO package for processor packaging; b) TSMC processor-memory stacking. SOURCES: System Plus and Yole.

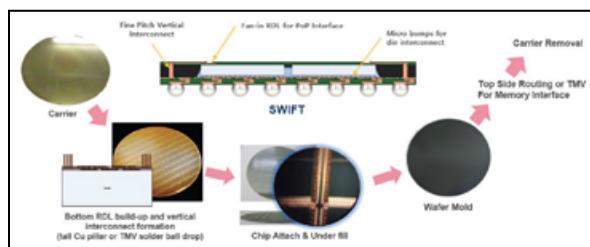


Figure 6: Process for Silicon Wafer Integrated Fan-out Technology (SWIFT™) by Amkor.

the industry's first 20 μm pitch assembly at panel level with GFO. Because the RDL in GFO is made up of ultra-low loss dielectrics, along with through-vias, unique low-loss transmission lines and embedded passives, GFO becomes one of the most leading-edge and thinnest 5G and mm-wave packages in the industry.

Digital applications

Digital applications are driving advances in both embedding and fan-out to benefit from ultra-short interconnections by embedding and highest I/O density, from fan-out at chip level, using BEOL RDL tools. Although the first embedded packages were developed by GE in the 1980s for the military, and Intel in the early 2000s for high-performance computing applications, the first high volume of embedded fan-out packages (eWFO) was not produced until TSMC for the Apple iPhone 7 in 2016, using integrated fan-out (InFO), as shown in **Figure 5**.

eWFO packages have advantages over flip-chip BGA packages due to the elimination of the substrate and the solder-based assembly processes. By eliminating the high-temperature substrate processing and high-temperature assembly processes, the overall warpage of the eWFO package is reduced from over 100 μm to less than 60 μm . Elimination of the substrate also

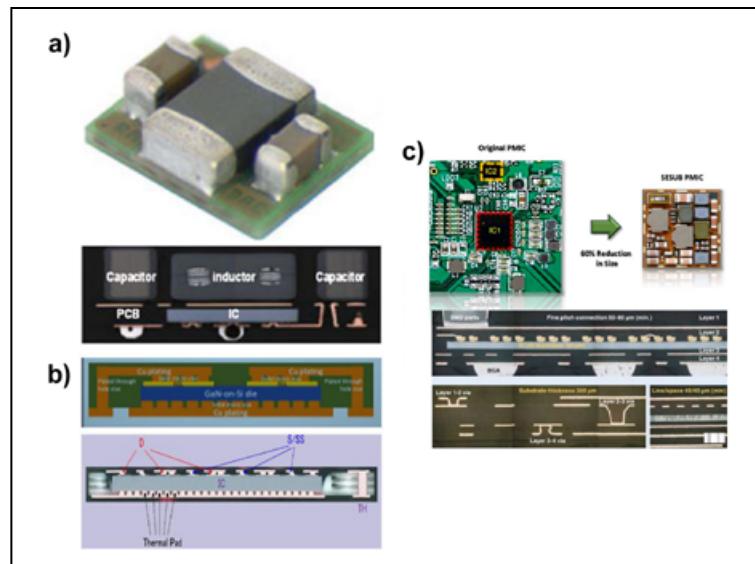


Figure 7: Power embedding of actives in laminate panels: a) TI MicroSiP™ DC-DC converter package with AT&S' ECP® in-PWB embedding process [11, 12]; b) GaN Systems and AT&S 650V/30A GaN-on-Si HEMT transistors package [13]; and c) TDK's SESUB [14].

reduces the package height to less than 0.4mm. The package-on-package (PoP) form factor can be reduced to 0.8mm in thickness.

A major concern of eWFO with chip-first embedding of high value-add and high-I/O CPUs and GPUs is the yield loss of ICs during RDL fabrication. The same concern applies to high-value multi-chip modules that can't be thrown away, if not yielded. Georgia Tech and Amkor addressed this concern by chip-last approaches but with eWFO benefits. Amkor developed Silicon Wafer Integrated Fan-out Technology (SWIFT™) [7], as shown in **Figure 6**, by first depositing RDLs on silicon wafers, followed by IC assembly at fine pitch, followed by molding the entire assembled wafer and releasing the silicon carrier to form the final thin embedded fan-out structure. This method has been demonstrated with RDL lines to 2 μm .

In Georgia Tech's GFO packages – in both chip-last and chip-first configurations – 50 μm thick glass with up to six RDL layers with 2 μm lines and 5 μm vias at 20 μm bump pitch are demonstrated with about 4x reduction in warpage, compared to low CTE organic laminate substrates.

Low- and high-power applications

Embedding of actives and passives is becoming very important in power applications to increase power density and efficiency along with miniaturization of power modules using Si devices for

low power and wide band gap GaN and SiC devices for high power. Among other benefits, embedding of these devices provides the lowest-inductance by elimination of bond wires [8].

The concept of die embedding into laminates was first explored in the “HERMES” EU project for power applications. Texas Instruments (TI) was the first to use this technology in high volume in its MicroSiP™ DC-DC converter package, shown in **Figure 7a**. In this approach, both the power IC switch and the microcontroller IC are embedded in ultra-large boards and then singulated into BGA packages [9], [10] using the Embedded Component Packaging (ECP®) process developed by AT&S. The AT&S ECP® process has also been applied recently by GaN Systems to package its new 650V/30A GaN-on-Si HEMT transistors, as shown in **Figure 7b**. In this process, GaN devices were embedded in laminate boards to eliminate bond wires to create a near chip-scale package with reduced inductance and enhanced heat dissipation.

TDK's SESUB in **Figure 7c** is another panel-based embedded IC-in-laminate technology resulting in ultra-thin packages with surface mount device (SMD) passive components on the top layers and with molding and shielding [8].

Integrated voltage regulators (IVRs) are another example illustrating the benefits of embedding in high-performance processors for improved efficiency, higher

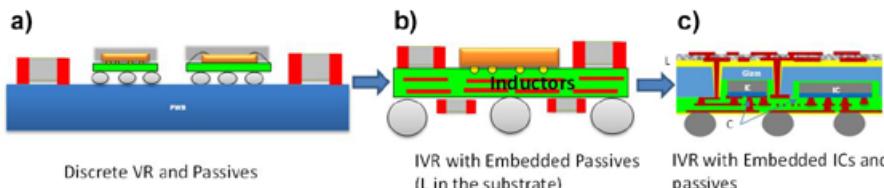


Figure 8: a) Evolution of IVRs from discrete components to b) embedded L, and to c) IVRs with embedded ICs and passives.

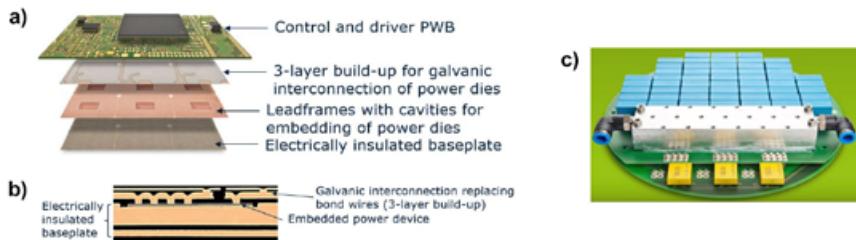


Figure 10: Schweizer Electronics p² Pack power embedding technology: a) process; b) cross section of embedded power die; and c) example of application in a 40kW e-motor with embedded IGBTs and diodes.

switching frequency, lower power losses, increased reliability and even lower cost. **Figure 8** shows how embedding evolved to form IVRs from discrete components to embedded passives and to embedded passives and actives. In IVRs, the focus is on embedding of switches, microcontrollers and passive components for power conversion inside the processor package, as illustrated in **Figure 8**. This leads to better power conversion efficiency and miniaturization. Intel utilized IVRs in its Haswell microprocessor packages where air core inductors are embedded [15]. Similarly, ferrite inductor-embedded power modules are being developed [16].

Virginia Tech recently proposed a new approach to embedding of power inductors in point-of-load (POL) converters using an innovative LTCC process. This new method combines GaN devices for higher switching frequencies and to increase power density up to 1000W/in³ as compared to the typical <300W/in³ achieved for 20A converters [17].

Georgia Tech, in collaboration with its industry partners, is developing IVRs using magnetic composite materials for higher power handling at high efficiency using panel-based embedding for low cost. A new class of layered magnetic composite films with high permeability of up to 900, low coercivity <1 Oe, high saturation magnetization >1 Tesla, and high-frequency stability up to 800MHz are being developed. An example of integrated inductor with such films is shown in **Figure 9a** [18].

These thin-film inductors are now being co-packaged with high-density capacitors using a 3D package architecture being pioneered by Georgia Tech. An example of such a high-density capacitor film on a silicon substrate is shown in **Figure 9b** [19]. Such inductors and capacitors are projected to result in modules with efficiency >90% and power handling above 2A/mm².

Large board-like, panel embedding has gained momentum in mid- to high-power electronics to minimize the package inductance and enable higher switching frequencies at lower cost. High-power modules are traditionally packaged by integrating all power switches on insulated metal-ceramic substrates such as direct bonding to ceramic (DBC), while control and drive systems are generally assembled separately on standard PWBs and connected to the power module using press contacts [20]. Fraunhofer IZM has recently developed a panel-based power die embedding process using panel laminates of 18" x 24" size for low- to medium-power, and 5" x 7" for high power where the base substrate is a DBC. This process was applied to single-chip power MOSFET packages, system-in-packages with MOSFET and driver co-integration, and IGBT high-power modules using multi-level wiring to interconnect power, control and driver.

Schweizer Electronics also pioneered an innovative power embedding concept using large board-like panel embedding involving different substrate technologies for DC-DC and AC-DC converters in the 1-50kW range. In this approach, the power dies are

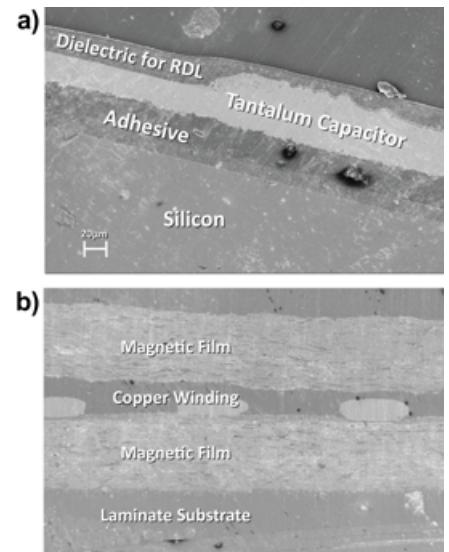


Figure 9: a) Examples of embedded power inductors [18], and b) embedded Ta capacitor on silicon substrates [19].

first assembled on electrically-insulated baseplates, and are then embedded in cavities. A three-layer build-up is then created using standard PWB processing to interconnect the power devices where bond wires are replaced by direct galvanic contacts with Cu-filled vias to minimize the package inductance. This substrate is then further embedded into PWBS of 575mm x 583mm in size for direct integration of drivers and control systems. Schweizer's p² Pack power module is one of the first packages to enable co-integration of power, control and driver ICs in a single package in a thickness of less than 1.4mm. The p² Pack technology as well as its implementation in a 40kW e-motor with embedded IGBTs and diodes is illustrated in **Figure 10**. Other commercial power embedding technologies include Infineon's DrBlade, Siemens' SiPLIT, Schweizer's i2 Board®, and General Electric's Power OverLay (POL) technology.

Development of power embedding technologies at >50kW is expected, with advances in SiC-based power modules. To fully benefit from the performance of SiC devices, operating temperatures of 250°C are highly desirable to minimize the size of the cooling systems. Georgia Tech is developing many new technologies that include: 1) DC-DC converters with GaN; 2) high-temperature hybrid organic-inorganic dielectrics and molding compounds; and 3) low-CTE, high electrical and thermal conductivity conductors for Hi-Rel CTE-matched packaging.

Future of embedding and fan-out technologies

There are four future directions the industry could take in terms of embedding and fan-out technologies. **Figure 11** shows the evolution of embedding and fan-out technologies, starting with WLP, that led to wafer-based embedding and fan-out technologies called eWFO. In this process, embedding by itself became a highly strategic technology, even when fan-out and high I/Os are not needed. It is now becoming clear that there are four strategic directions for embedding and fan-out technologies; two at wafer level and two at panel level. All four require embedding.

eWFO for highest I/O density and small ICs—digital devices. One strategic direction for eWFO is for high chip-level I/O density to package logic devices such as processors. This is best achieved with wafer BEOL tools, materials and processes. So eWFO is best for packaging digital devices such as processor and server ICs and for logic-to-memory interconnections with highest I/Os that can't be produced in any other way. TSMC's InFO is an excellent example. But achieving scaling and high I/O density by eWFO is limited by the process for eWFO with molding compounds. The eWFO is also limited to smaller to medium size ICs and packages because of the high cost of producing small number of larger fan-out packages from 300mm wafers. Application of eWFO for multi-chip heterogeneous packaging presents another major challenge because this technology doesn't provide a path for repairability or reworkability. Georgia Tech is addressing the challenge noted above by its inorganic, mold compound-free GFO in large panel form that is capable of Si-like BEOL dimensions, as described below. This is in development and not manufacturing ready.

eWFO for medium I/O density and small ICs—RF and millimeter wave devices. In contrast to the use of expensive BEOL technologies for the highest density of I/Os, non-wafer fab facilities such as by outsourced semiconductor assembly and test suppliers (OSATS) have been, and continue to be used for embedding and fan-out by interconnecting medium I/O density and small-size ICs. These 300mm facilities are appropriate for packaging small RF, 5G, and millimeter devices.

ePFO for low I/Os and small-to-large packages—power devices. Panel-based embedding has begun to emerge in a

Attributes	WLP	eWFO	ePFO-Organic	ePFO-Inorganic
Substrate	No Substrate	Molding Compound	Laminate	Glass, Poly-Si, Metal
Chip Assembly	None	None	None	None
Chip-level I/O Pitch	Low	Low-Medium	Medium-Large	Large
IC & Pack. Size	Small	Medium	Small-Medium	Medium-Large
Production Size	300mm	300mm	Up to 600mm	Up to 500mm

Figure 11: Evolution of embedding and fan-out packaging from 1st-generation WLP in 1990s to 4th generation inorganic PFO in 2020.

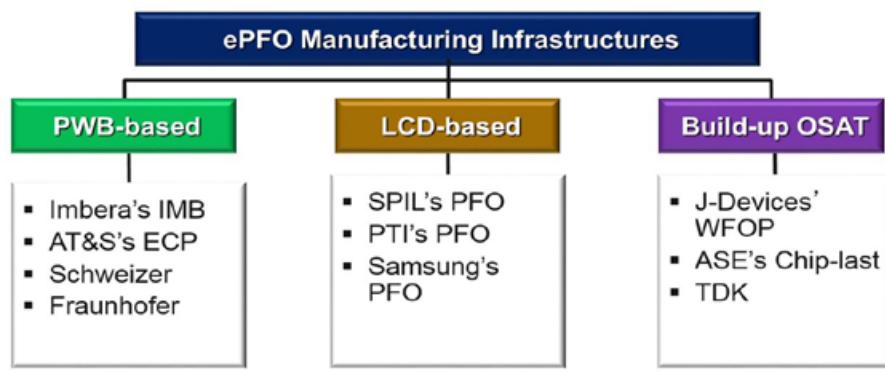


Figure 12: Three types of manufacturing infrastructures for panel embedding.

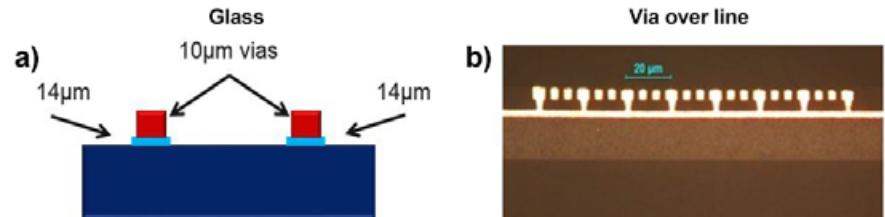


Figure 13: a) Concept of via on line with nearly the same dimensions; and b) Actual via on line enabled by GFO.

big way for analog products, starting with low power, then high power, and in the future many others that include integration of many devices. These panels don't require BEOL tools, materials and processes. The panels can be any and all that are not round wafers and manufactured outside the IC foundry. Embedding by AT&S for low power, and by Schweizer and Fraunhofer for high power, both in board-like large panels, are examples of ePFO. This is referred to as embedded panel fan-out (ePFO-organic) technology in **Figure 11**. **Figure 12** shows three different manufacturing infrastructures to address this market: 1) the traditional PWBs such as those used by AT&S; 2) the new LCD-based ultra-large panel process, such as by Samsung;

and 3) built-up RDL manufacturing infrastructure by OSATS. All these manufacturing infrastructures exist today and with appropriate modifications, they are capable of handling high-volume manufacturing of all embedded and low-to-medium I/O products other than those that require BEOL infrastructure for ultra-high I/O density.

Inorganic panel embedding for very high I/Os and large packages. Georgia Tech and its 50 industry partners are developing the 4th-generation of embedding and fan-out technology, as shown in **Figure 4**, **Figure 11** and **Figure 13**, that is ultra-thin, has very high electrical performance, very high I/O density, and high reliability in both chip-first and chip-last scenarios using ultra-thin and large

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panels of glass for low cost. In contrast to the wafer fan-out that is limited by molding compounds, and laminate-embedding that is limited in I/O density, reliability, and thermal stability, the Georgia Tech approach referred to as embedded glass fan-out (eGFO) has many attributes listed below. **Figure 13** shows Si-like, same via and line dimensions for the first time in the packaging world. Some of the attributes of eGFO are as follows:

- Si-like BEOL to close interconnect gap;
- Ultra-miniaturized;
- High-temperature stability;
- Hermetic reliability;
- Ultra-low loss and ultra-high resistivity;
- Minimum warpage;
- Excellent surface smoothness;
- High moisture resistance; and
- Large panels up to 510mm in size.

The GFO approach addresses the limitations of current embedding and fan-out technologies. It begins to address the interconnect gap that exists between current fan-out and Si BEOL lithographic dimensions, as shown in **Figure 14**.

The silicon-like dimensional stability of glass in large-panel manufacturing enables an unparalleled combination of ultra-high I/O density, high electrical performance, high reliability and low cost, not possible in molding compound-based wafer or laminate-based fan-out technologies. Unlike high-density fan-out packages that require another package such as an organic BGA package to connect to boards for large package sizes, GFO packages are designed to be directly SMT-attachable to the board. Lastly, the ultra-smooth surface and high-dimensional stability of glass enables silicon-like RDL wiring and BEOL-like I/Os but on large panels, for the first time, with less than 2µm critical dimensions (CD) for high-density fan-out applications.

The Georgia Tech team is developing GFO using daisy chain test dies from Intel to emulate an embedded device of 6.469mm x 5.902mm size in 75µm thickness with a pad pitch of 65µm. GFO was fabricated with these devices using 70µm-thick glass panels with through-glass cavities fabricated with dimensional accuracy below ±5µm. This cavity-containing panel is then bonded with an adhesive to a 50µm-thick glass panel and the test dies were then placed in these cavities using a high-speed placement tool from Kulicke and Soffa. The RDL polymers

were then laminated and cured on both sides to minimize the warpage of the ultra-thin package. A surface planar tool by Disco was used to planarize the surface of the panel to expose the copper micro-bumps on the die, followed by a standard semi-additive process (SAP) for the fan-out RDL layer. The die shift and warpage were characterized systematically. Initial modeling and measured results indicated less than 5µm die shift and less than 15µm warpage across a 300mm panel in the Georgia Tech pilot line. The first demonstration of a fully integrated GFO package, the thinnest package at highest I/O pitch to-date of 20µm, is shown in **Figure 15**.

Summary

Embedding is the most important strategic technology that is applicable for all digital, RF and power applications. When combined with fan-out at chip- and board-levels, it enables higher I/O applications. eWFO packaging can be fabricated in either wafer fabs using BEOL tools, materials and processes, or OSATs' built-up fabs and tools. The eWFO technology from 300mm wafer fabs is capable of the ultimate I/O density, but at high cost for large ICs requiring large eWFO packages. This technology is best suited for high-value logic devices requiring very high I/O density. It is currently limited by molding compounds and others, in many ways. The eWFOs from OSATs are capable of handling high I/Os from their 300mm fabs and the technology is extendable to panels. This technology is suitable for small devices such as RF and some logic devices, but as the device size goes up, the cost of packaging this device goes up. Embedding with or without fan-out is most suitable for power devices.

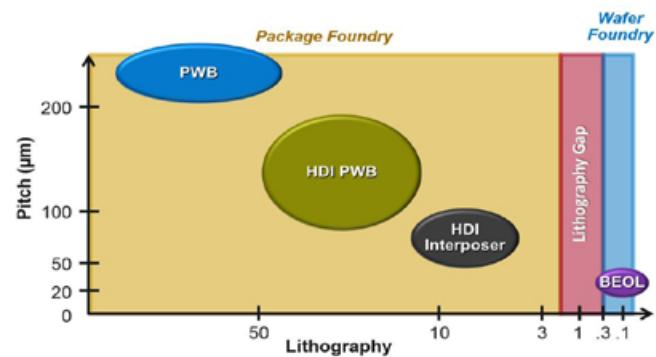


Figure 14: Interconnect gap with current eWFOs.

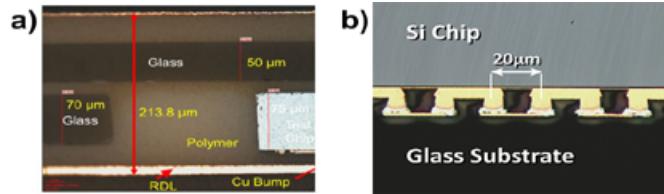


Figure 15: a) Ultra-thin glass fan-out (GFO) package for high I/O digital applications; and b) 20µm pitch assembly on a glass substrate.

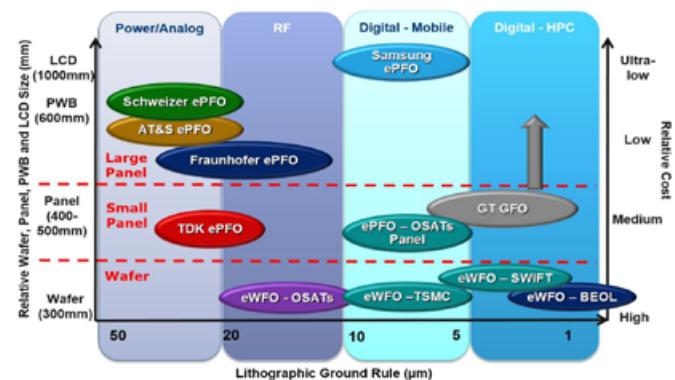


Figure 16: Summary of wafer, panel and board embedding and fan-out technologies as a function of applications and lithographic ground rules.

They don't require high I/Os, but they need to be manufactured at very low cost. Ultra-large panels such as boards from the printed wiring board (PWB) industry or the liquid crystal display (LCD) industry are best suited to embed these devices.

There is a need to couple ultra-high density of interconnections such as from wafer-based foundries with high-throughput panel manufacturing so as to end up with the highest performance at lowest cost, even for larger ICs and packages and with very high I/O density. There are two solutions that are coming to the fore. Panel-based embedded and fan-out manufacturing infrastructure are emerging as described in this article and with advances in lithographic ground rules by new advanced large-area lithographic tools; and in advanced laminates, panel-based embedded fan-out is bound to evolve to serve not only power, but also RF and

mm-wave markets. The second path that is emerging has to do with glass fan-out, such as by Georgia Tech with its GFO, with Si-like ground rules to 2 μ m and below in lithography, leading to 20 μ m bump pitch and below in interconnections and assembly on large panels. This technology is capable of closing the interconnections gap between BEOL and the package foundry, as shown in **Figure 14**. **Figure 16** shows the relative regimes of embedding and fan-out at wafer-, panel- and board-levels for digital, RF and power applications as a function of relative size and cost.

References

1. S. Sakhnenko, D. Orlenko, B. Vorotnikov, O. Aleksieiev, P. Komakha, P. Heide, et al., "Ultra-low-profile small-size LTCC front-end module (FEM) for WLAN applications based on a novel diplexer design approach," 2009 IEEE/Mtt-S International Microwave Symposium, vols. 1-3, pp. 609-612, 2009.
2. SESUB (semiconductor embedded in substrate) module technology Available: <https://en.tdk.eu/tdk-en/374108/tech-library/articles/products---technologies/products---technologies/very-small-and-extremely-flat/171672>.
3. N. Kumbhat, A. Choudhury, G. Mehrotra, P. M. Raj, V. Sundaram, R. Tummala, "Highly reliable and manufacturable ultra-fine pitch Cu-Cu interconnections for chip-last embedding with chip-first benefits," IEEE Trans. on Comp., Packaging and Mfg. Tech., vol. 2, pp. 1434-1441, 2012.
4. S. Sitaraman, Y. Suzuki, C. White, V. Nair, T. Kamgaing, F. Juskey, et al., "Modeling, design and demonstration of multi-die embedded WLAN RF front-end module with ultra-miniaturized and high-performance passives," 2014 IEEE 64th Elect. Comp. and Tech. Conf. (ECTC), pp. 1264-1271, 2014.
5. J. Bock, R. Lachner, "SiGe BiCMOS and eWLB packaging technologies for automotive radar solutions," in Microwaves for Intelligent Mobility (ICMIM), 2015 IEEE MTT-S Inter. Conf., 2015, pp. 1-4.
6. G. Haubner, W. Hartner, S. Pahlke, M. Niessner, "77GHz automotive RADAR in eWLB package: from consumer to automotive packaging," Microelectronics Reliability, vol. 64, pp. 699-704, Sept. 2016.
7. R. Huemoeller, C. Zwenger, "Silicon wafer integrated fan-out technology," *Chip Scale Review*, vol. 19, pp. 10-13, 2015.
8. E. Parker, B. Narveson, A. Alderman, L. Burgyan, "Embedding active and passive components in PCBs and inorganic substrates for power electronics," 2015 IEEE Inter. Workshop on Integrated Power Packaging (IWIPP), pp. 107-110, 2015.
9. J. Moss, U. Chaudhry, S. Kummerl, C. DeVries, "Increase power density and simplify designs with 3D SiP modules," 2016 Inter. Symp. on 3D Power Electronics Integration and Mfg. (3D-PEIM), 2016.
10. L. J. Smith, "3D SiP with embedded chip providing integration solutions for power applications," in 3D Power Electronics Integration and Manufacturing (3D-PEIM), Inter. Symp. on, 2016, pp. 1-17.
11. TI Microsip. Available: https://www.google.com/search?q=TI+MicroSiP%2E2%84%A2+Package&espv=2&b_iw=1130&bih=648&source=lnms&t_bm=isch&sa=X&ved=0ahUKEwit8t-cwKzRAhWMOCYKHVqAO8Q_AUBygC#t_bm=isch&q=TI+MicroSip&imgrc=LwetbDn37-ZVeM%3A
12. Ti Microsip cross section. Available: http://www.systemplus.fr/wp-content/uploads/2013/05/Micronews_2012_03_N125_systemplus.pdf
13. GaN Systems and AT&T GaN Package. Available: <http://www.apec-conf.org/wp-content/uploads/IS-8.5-Maximizing-GaN-Power-Transistor-Performance-with-Embedded-Packaging.pdf> and <http://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is83-significant-developments-and-trends-3d-packaging.pdf>
14. TDK SESUB cross section. Available: <http://www.chipscalereview.com/tb1505-01.html> and <http://www.apec-conf.org/Portals/0/Industry%20Session%20Presentations/1.5/IS1-5-1.pdf>
15. E. A. Burton, G. Schrom, F. Paillet, J. Douglas, W. J. Lambert, K. Radhakrishnan, et al., "FIVR—Fully integrated voltage regulators on 4th generation Intel® Core™ SoCs," in 2014 IEEE Applied Power Elec. Conf. and Exposition-APEC 2014, 2014, pp. 432-439.
16. T. Mikura, K. Nakahara, K. Ikeda, K. Furukawa, K. Onitsuka, "New substrate for micro DC-DC converter," in 56th Elec. Comp. and Tech. Conf. 2006, p. 5.
17. Y. P. Su, Q. Li, F. C. Lee, "Design and evaluation of a high-frequency LTCC inductor substrate for a three-dimensional integrated DC/DC converter," IEEE Trans. on Power Electr., vol. 28, pp. 4354-4364, Sept. 2013.
18. T. Sun, P. M. Raj, J. Min, Z. Wu, H. Sharma, T. Takahashi, et al., "Magnetic materials and design trade-offs for high-inductance density, high-Q and low-cost power and EMI filter inductors," IEEE 66th Elect. Comp. and Tech. Conf. (ECTC), 2016, pp. 374-379.
19. P. Chakraborti, H. Sharma, M. R. Pulugurtha, K.-P. Rataj, C. Schnitter, N. Neuhart, et al., "Ultra-thin, substrate-integrated, and self-healing nanocapacitors with low-leakage currents and high-operating frequencies," 2016.
20. C. Neeb, J. Teichrib, R. W. De Doncker, L. Boettcher, A. Ostmann, "A 50kW IGBT power module for automotive applications with extremely low DC-link inductance," 2014 16th European Conf. on Power Elect. and Applications (Epe'14-Ecce Europe), 2014.

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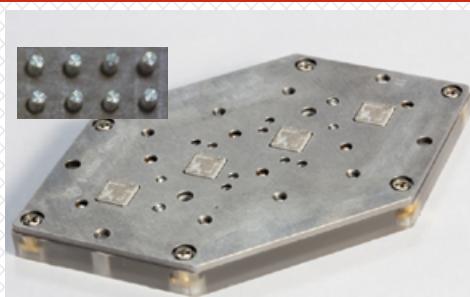
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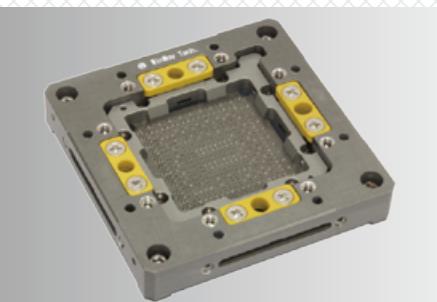
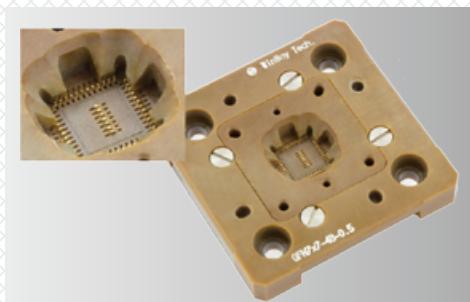
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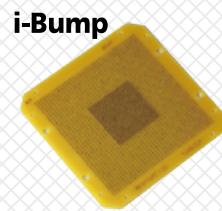
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Temporary bonding material with high sensitivity for laser release in advanced packaging processing

By Kenzo Ohkita, Yooichiro Maruyama, Hikaru Mizuno, Takashi Mori, Hiroyuki Ishii, Koichi Hasegawa [JSR Corporation]

Driven by exponentially increasing demand in big data for the Internet of Things (IoT), powerful and multifunctional devices with low energy consumption have been developed. As Moore's law is reaching its limitations, innovative evolutions of advanced electronic packages are required. Devices that deploy 2.5D/3D integration and fan-out wafer-level packages (FOWLPs) have progressed to satisfy these requirements in the recent decade [1-5]. The 2.5D/3D structures consist of stacked chips with thinned silicon wafers and through-silicon vias (TSVs), while FOWLPs include device chips (dies) embedded in a mold compound. Even though their designs are different, the basic concept for improving device performance tends to be focused on two directions, one is to achieve 3D packaging by stacking thinned wafers, and the other is to increase I/O density by constructing fan-out packaging designs.

In order to handle thin and fragile substrates, temporary bonding/debonding (TBDB) technologies have been utilized. In this technology, the device wafers are rigidly fixed onto a carrier while processing and then released. To release the substrate from the carrier, four predominant debonding systems – thermal slide, mechanical release, solvent release, and laser release – have been reported. Some of the systems have already been put into practical use. However, the requirements for TBDB materials are broad and depend on the target application. This is one of the reasons that development and optimization of each TBDB system is still underway.

Among the options listed above, the laser release system has advantages in very high-throughput debonding specifically with respect to low mechanical and thermal stresses. The temporary bonding layer is designed to absorb the laser beam to be decomposed. As a result, the TB layer loses adhesion immediately and completely thereby allowing the device a force-free release from the carrier. In this paper, we will outline TBDB technology, features of laser TBDB

systems, and the development of TBDB materials for UV laser debonding.

TBDB process flow and system

The process flow of temporary bonding, including the device wafer thinning process followed by backside processing for 3D packages, is shown in **Figure 1a**. Wafer thinning is carried out by grinding until the thickness reaches 100 μm or thinner. On the other hand, FOWLPs, which comprise molded compound embedding dies, also require a wafer support system. As a representative flow of FOWLP, a redistribution layer (RDL)-first process is shown in **Figure 1b**. In this process, a TBDB material is coated on the support wafer first, followed by building up of RDL layers using photoresist, dielectrics, copper plating materials, and epoxy molding compounds (EMCs). It should be noted that the bonded wafer must withstand the high-temperature conditions, chemical exposure and subsequent release without damage to the device.

A laser release system has advantages in terms of debonding temperature, mechanical stress and throughput, compared with the other conventional debonding systems such as thermal slide, mechanical and solvent release. For applications where glass carriers are acceptable, a laser release system is a promising procedure for debonding.

Laser release systems are classified by the laser wavelengths as shown in **Table 1**. These are different in terms of the laser-induced reaction mechanism and debonding equipment cost, while all the systems listed in the table require a glass carrier. Generally, the UV laser debonding system has advantages

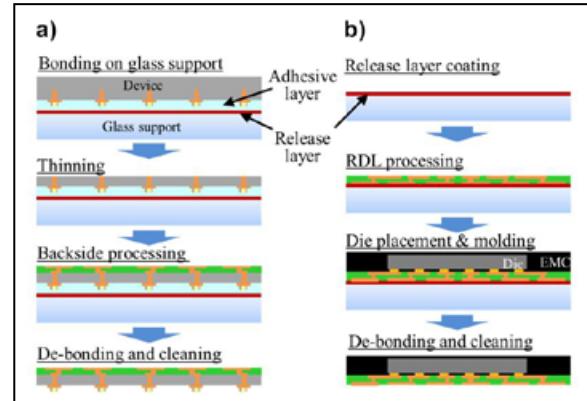


Figure 1: Schematic drawing of the TBDB process: a) Device wafer thinning and backside processing; b) Mold wafer build-up for fan-out packages.

	308nm	355 nm	532 nm	1064 nm
Release Mechanism	Photonic cleavage	Photonic cleavage	Thermal or Photonic	Thermal degradation
Thermal effect	Low	Low	Intermediate	High
Equipment cost	Expensive Excimer	Low Solid state	Low Solid state	Low Solid state
Carrier	Glass	Glass	Glass	Glass

Table 1: Laser release system comparison.

in terms of lower heat generation. The ablation reaction induced by a high energy density ultraviolet (UV) laser is speculated to have photochemical characteristics including a two-photon absorption mechanism. This results in direct activation followed by cleavage of the covalent bonds of the TBDB material. In contrast, an infrared (IR) laser is speculated to have a photothermal mechanism that results only in the thermal decomposition of molecules.

There are several sources for oscillating UV lasers. In this study, we focused on UV laser release systems with 308nm and 355nm wavelengths because there are numerous advanced packaging manufacturers that can handle glass carriers and also because of the trend to decrease operation temperatures to minimize thermal damage to packages.

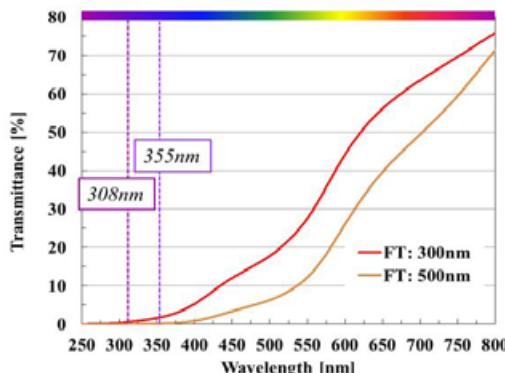


Figure 2: UV-VIS spectra of the release layer material (Release-1) with 300nm and 500nm in thickness.

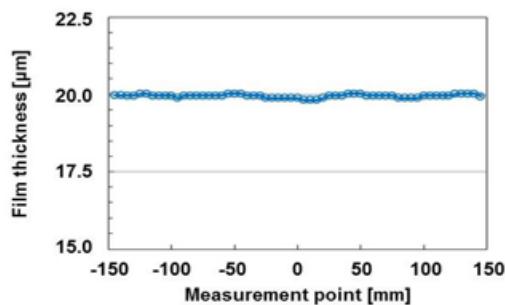


Figure 3: Film thickness uniformity of the 20 μm thick adhesive layer (Adhesive-1) on a 300mm silicon wafer.

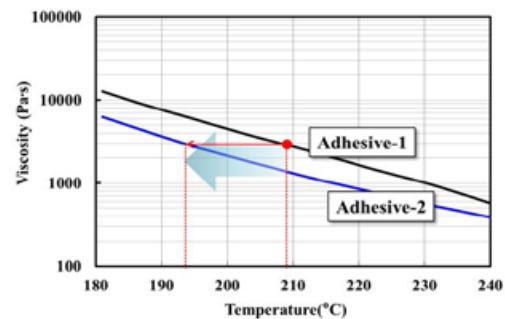


Figure 4: Shear viscosity of adhesive materials against temperature.



Figure 5: Photograph of a bonded glass support wafer and bare silicon wafer with Adhesive-1. The thickness of the adhesive layer is 20 μm . Bonding was carried out by a thermo-compressive procedure under vacuum, 200°C for 5 min, and 0.8MPa compressive pressure.

TBDB materials for laser release

To enable handling, device wafers are bonded onto a glass carrier wafer with TBDB materials that comprise two layers, a release layer and an adhesive layer. The release layer is applied onto the carrier. The device substrate is then bonded with adhesive to the release layer side of the carrier by a thermocompressive procedure. The release layer is designed to have a high absorbance of the UV laser beam to induce ablation selectively through the glass carrier. On the other hand, the role of the adhesive layer is to hold the device wafer on the glass support wafer correctly, without creating any issues such as void generation or delamination during the device fabrication process.

Material design for release layer

In order to achieve optimal sensitivity for UV laser release, the release layer is designed to have high absorbance of UV light to induce photonic cleavage of covalent bonds. The lower absorbance material needs a thicker film, which requires higher energy to release completely. The UV-VIS spectra of the developed release layer material, Release-1, with different film thicknesses, are shown in **Figure 2**. Transmittance of 308nm and 355nm are low enough at both thicknesses. Such optical design enables debonding with minimal laser irradiation, which prevents damage to the device surface.

To get the desired optical properties, a polymer with a specific chromophore in the molecule was used as a main component. This release material does not contain any additional laser-absorbing additives, such as dye or pigment, as components. As a result, this material is free from precipitation in solution or bleeding out of the coated film, which can be caused by the extremely high concentration of additive required to get high absorbance.

The thermoset character of Release-1 gives good chemical resistance. The bonded wafer should be exposed by various chemicals through photolithography, electroplating, and etching processes. The cured release layer exhibits good resistance against any common

organic solvent, acidic plating solution, or alkaline solution such as a TMAH developer.

Material design for adhesive layer

The adhesive material is designed based on an aromatic thermoplastic resin that has hydroxyl groups. From a material point of view, spin coating thickness, uniformity, melt viscosity during temporary bonding, thermal stability, adhesion strength, chemical stability, and wet cleaning properties must be taken into account.

One of the most important requirements of the adhesive layer is good bonding without creating any voids inside the bonded pair. For this purpose, low variation of thickness uniformity and appropriate shear viscosity at the bonding temperature, are quite necessary. Thickness uniformity of the developed adhesive – Adhesive-1 – with 20 μm thickness after coating on a 300mm Si wafer (**Figure 3**) shows that its variation is within 0.2 μm . A peak and a cave at the center of the wafer, or hump at the wafer edge, which sometimes happens in spin-coated films, are acceptable for wafer bonding.

The rheological properties of the adhesives against temperature are shown in **Figure 4**. Optimization of the molecular weight of the base polymer can easily control the shear viscosity to achieve both bonding and thermal stability simultaneously. To achieve good bonding, the shear viscosity is preferably 3,000Pa·s or lower. This indicates that the bonding temperature needed for Adhesive-1 has to be 210°C or higher. However, the maximum process temperature allowed for some next-generation packaging processes, especially for FOWLP applications, is sometimes lower than 200°C to avoid wafer bowing and warping. An adhesive layer material with lower shear viscosity (Adhesive-2) is also shown in **Figure 5**. In this case, shear viscosity of 3,000Pa·s could be achieved at 195°C with a 12% lower molecular weight than Adhesive-1.

Sufficient thermal stability of the adhesive layer helps to ensure void-free adhesion during the entire TBDB process. Thermal degradation of Adhesive-1 was determined by thermogravimetric analysis (TGA) and found that a 1% weight loss temperature in a nitrogen atmosphere was 380°C, which indicates that stable void-free temporary bonding is expected at elevated temperatures. Adhesion strength is determined by the hydroxyl groups in the polymer structure. As a result, sufficient adhesion to various materials such as silicon, dielectric, metals, and EMC were obtained.

Bonding/debonding properties of TBDB materials

A bonding demonstration using a 300mm bare silicon wafer on a glass carrier was carried out with a 20 μm -thick Adhesive-1 as the adhesive layer. Thanks to excellent coating uniformity and appropriate shear viscosity, bonding at 200°C was completed with no remarkable voids or defects (**Figure 5**).

The adhesive strengths of TBDB materials to various surface materials were evaluated by a die shear test with bonded and diced samples. Release-1 was coated onto the glass carriers with a thickness of 0.5 μm . Silicon wafers, which have a surface comprising silicon, silicon oxide, silicon nitride, copper, titanium, and organic insulator, were coated at 20 μm thickness with Adhesive-1, then bonded onto the release layer side of the glass carrier. All die shear strength results of samples diced into 10mm squares are higher than 200N/cm² and are beyond the measurement limit. In most runs, a glass wafer fracture mode was observed. These results imply that Adhesive-1 has excellent adhesion strength against a wide variety of device wafer surface materials.

The chemical resistance of TBDB materials was evaluated by soaking bonded pairs in various chemicals. The bonded pairs of a glass carrier with a release layer (Release-1) and a silicon wafer with an adhesive layer (Adhesive-1) were examined in the evaluation. The results are summarized in **Table 2**. Only the bonded pair soaked in an NMP/EG mixture failed with a slight wrinkling on account of swelling of the adhesive layer. However, the bonded pairs were stable in all other chemicals to indicate that the TBDB materials described in this paper are promising for practical applications.

Chemicals		Condition	Result
Solvent	Acetone	25°C / 10min	Pass
	PGME	25°C / 10min	Pass
	PGMEA	25°C / 10min	Pass
	IPA	25°C / 10min	Pass
	NMP/HG mixture*	60°C / 30min	Fail (wrinkle)
Wet etcher	10% H ₂ SO ₄	25°C / 30min	Pass
	30% H ₂ O ₂	50°C / 30min	Pass
Developer	2.38% TMAH	25°C / 10min	Pass
Cleaner	10% NH ₄ OH / 10% H ₂ O ₂	25°C / 10min	Pass

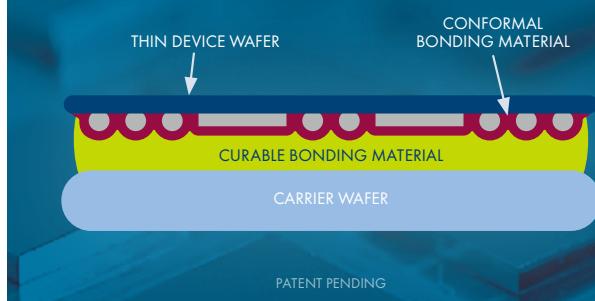
*NMP/Ethylene glycol = 50/50

Table 2: Chemical stability of adhesive layer.

Laser debonding was performed using a bonded pair of a glass support wafer coated with a release layer (Release-1) and a 300mm bare silicon wafer coated with an adhesive layer (Adhesive-1). As a UV laser source, a third harmonic wave of Nd-doped YAG, which emits 355nm light with 50kHz oscillation frequency, and equipped with a galvanic scanner, was used. Debonding was carried out by laser irradiation by scanning with a 50kHz repetition frequency across the entire wafers. The irradiation pitch, which is defined by the frequency and the scan speed, can be appropriately adjusted to not produce any un-irradiated area.

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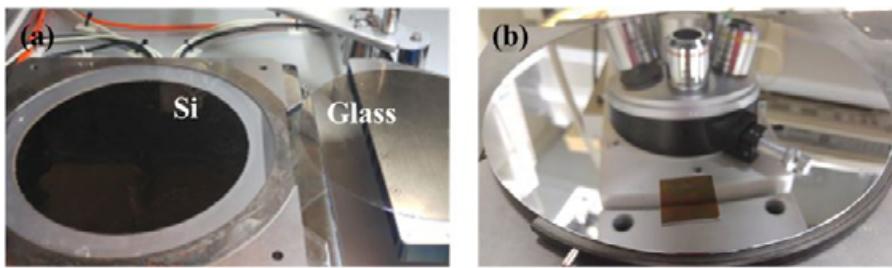


Figure 6: a) A debonded pair of wafers: the left is a silicon wafer thinned down to 50 μm and the right is a glass carrier. b) A silicon wafer after solvent cleaning. The diced wafer on the whole wafer is the corresponding debonded wafer before cleaning.

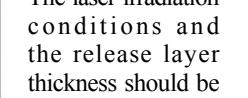
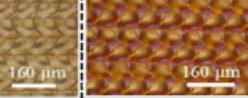
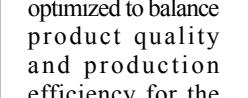
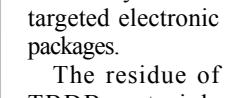
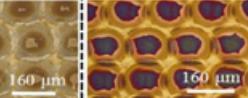
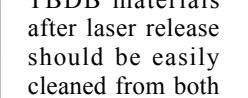
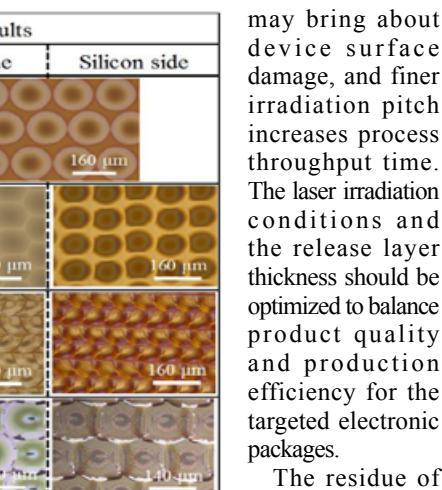
Irradiation		Results		
power	pitch	release	Glass side	Silicon side
2.0W	160 μm	Fail		 160 μm
2.0W	120 μm	Released	 160 μm	 160 μm
2.0W	80 μm	Released	 160 μm	 160 μm
2.5W	140 μm	Released	 140 μm	 140 μm
3.5W	160 μm	Released	 160 μm	 160 μm

Table 3: Optical micrographs of glass and silicon surfaces after 355nm laser debond.

Optical micrographs of the glass and silicon surface after laser irradiation are summarized in **Table 3**. Dots observed in these micrographs are the laser marks that indicate the occurrence of laser ablation. In the case where the laser power is 2.0W and the irradiation pitch is 160 μm , the laser marks are relatively small compared with the other conditions. Also, a large part of the release layer remains un-irradiated. As a result, this bonded sample could not be released from the glass.

To achieve laser release, two methods were attempted: increasing the laser power and decreasing the laser irradiation pitch. Under higher laser power conditions (2.5W or higher), bonded pairs were successfully debonded because the ablated area of each irradiated spot got wider and overlapped adjacent spots. In the same way, decreasing the laser irradiation pitch (120 μm or narrower) was also able to achieve laser release. However, excess laser power and finer irradiation pitch have disadvantages in practical applications. Higher laser power



may bring about device surface damage, and finer irradiation pitch increases process throughput time. The laser irradiation conditions and the release layer thickness should be optimized to balance product quality and production efficiency for the targeted electronic packages.

The residue of TBDB materials after laser release should be easily cleaned from both debonded surfaces. In our material design, the residue

on the device wafer side is removed by wet chemicals, while on the glass support wafer side, it is removed by plasma cleaning. **Figure 6** shows a silicon wafer after laser debonding and cleaning. The small diced piece of wafer on the whole wafer is the reference before cleaning. The residue on both wafers was confirmed to be removed completely.

Summary

Recently developed laser-releasable TBDB materials were described. The laser TBDB materials comprise two parts: adhesive layer materials and release layer materials. Adhesive layer materials, which are required to hold device wafers correctly on rigid support wafers, showed good adhesion properties against each material, such as metals and insulators. Excellent thermal and chemical stability of the materials were also described. Release layer materials, which are essential for the laser TBDB process, were also introduced. They were designed to absorb UV lasers such as 308nm or 355nm wavelengths. The release

layer materials developed have very high UV absorption properties, which help to reduce laser irradiation energy and shorten the laser release process time. Temporary bonding technology is being developed in parallel to packaging structure advancements. Laser debonding systems will drive evolutionary progress in packaging technology for advanced applications.

Biographies

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References

1. G. J. Jung, B. Y. Jeon, I. S. Kang, "Structure and process development of wafer-level embedded SiP (system-in-package) for mobile applications," Proc. EPTC 2009, 191 (2009).
2. Y. Kurita, S. Matsui, N. Takahashi, K. Soejima, M. Komuro, M. Itou, "A 3D stacked memory integrated on a logic device using SMAFTI technology," Proc. ECTC 2007, 821 (2007).
3. M. Santarini, "Stacked and loaded: Xilinx SSI, 28-Gbps I/O yield amazing FPGAs," Xcell Journal, 74, 8 (2011).
4. M. Murugesan, H. Kino, H. Nohira, J. C. Bea, A. Horibe, F. Yamada, "Wafer thinning, bonding, and interconnects induced local strain/stress in 3D-LSIs with fine-pitch high-density micro-bumps and through-Si vias," IEDM Tech. Digest, 30 (2010).
5. C.-F. Tseng, C.-S. Liu, C.-H. Wu, D. Yu, "InFO (wafer-level integrated fan-out) technology," Proc. ECTC 2016, 1 (2016).

Optimization of die attach to surface-enhanced lead frames for MSL-1 performance of QFN packages (part 1)

By Senthil Kanagavel, Dan Hart [MacDermid Performance Solutions]

This article is part 1 of a two-part series. Part 2 focuses on MSL-1 evaluation of the material combination.

Qquad flat no-leads (QFN) semiconductor packages represent one of the steadiest growing types of chip carriers, and they are predicted to continue growing as original equipment manufacturers (OEMs) strive to put more signal handling into a smaller space. Owing to their low-profile, condensed form factor, high I/O and high thermal dissipation, they are popular choices for chip set consolidation, miniaturization, and chips with high power density, especially for the automotive and RF markets. As with any package, reliability is critical, and due to their widespread acceptance, OEMs, integrated device manufacturers (IDMs) and outsourced semiconductor assembly and test suppliers (OSATS) demand continued improvements in the reliability of QFNs.

Chemical processes that treat the surface of copper lead frames to enhance mold compound adhesion and reduce delamination in chip packages deliver improved reliability in QFNs. These chemical processes result in micro-roughening of the copper surfaces, while concurrently depositing a thermally robust film that enhances the chemical bond between the epoxy encapsulants and the lead frame surface. Typically, this type of process can reliably provide JEDEC MSL-1 performance.

While this chemical pretreatment process provides improved performance with respect to delamination, it can create other challenges for the lead frame packager. Increased surface roughness magnifies the tendency for die attach adhesives to bleed (epoxy bleed out, or EBO), causing the silver-filled adhesive to separate and negatively impact package quality and reliability. Additionally, any epoxy resin that bleeds onto the lead frame surface can interfere with other downstream processes, such as down-bonding or mold compound adhesion (**Figure 1**).

Anti-bleed or anti-EBO coatings have been developed to control the amount of bleed, but different adhesives can have different physical

properties (surface tension, percent solids, viscosity, etc.) that impact the interaction with the anti-bleed coatings. Consequently, the selection of die attach adhesive can be critical to package performance. This article examines the appropriate methods for optimizing both die attach adhesive chemistry with state-of-the-art lead frame technology.

Performance attributes for achieving MSL-1

MSL-1 performance is typically attributed to a number of factors in the semiconductor package. The various materials such as epoxy molding compound, die attach material, lead frame alloy type and surface chemistries, as well as the die type and size, all influence the performance of the package as a whole. The performance and interaction of the individual materials is important in preventing delamination in the package during MSL-1 testing. This article focuses on the key material interactions and their effects on MSL-1 performance.

Conductive die attach typically will undergo stress during the MSL-1 exposure and reflow so it is important it maintains its properties and does not initiate delamination with the lead frame surface or die back side (**Figure 1**). The other key factor that contributes to the failures is epoxy bleed out or resin bleed out. The resin from the epoxy will bleed onto the lead frame surface. This can cause loss of adhesion to epoxy molding compound and result in delamination during MSL-1 (**Figure 2**). In addition, as the epoxy bleeds onto the lead frame, the composition of the adhesive under the die changes—less epoxy and more silver. This can impact the adhesion of the die attach to the lead frame or the die, and result in an adhesive failure, as opposed to the desired

cohesive failure mode. So, it is very critical for the die attach to not cause any significant bleed out on the lead frame surface.

With the challenges driven by the move to lead-free electronics components, reflow temperatures have increased significantly. This move triggered a reduction in reliability at MSL-1, specifically delamination of epoxy molding compounds (EMCs) and die attachment from the lead frame surface. To improve MSL performance, many semiconductor packagers have turned to different methods for adhesion improvement. The most popular of these is generically termed “brown oxide” or “alternative oxide,” which roughens the copper lead frame surface while concurrently applying an organometallic coating.

The brown oxide mechanism comprises an intergranular etching process that selectively etches small gaps between copper grains of the lead frame alloy. The etching composition includes organic



Figure 1: Typical construction of a QFN package showing EBO from die attach material.

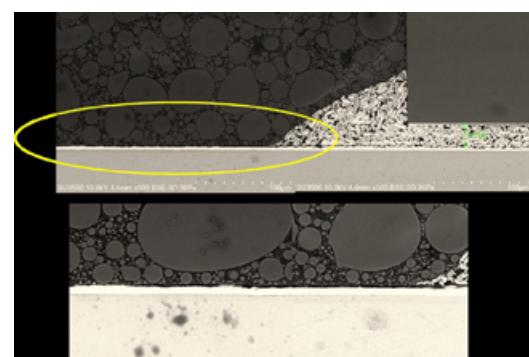


Figure 2: Delamination observed due to EBO from die attach.

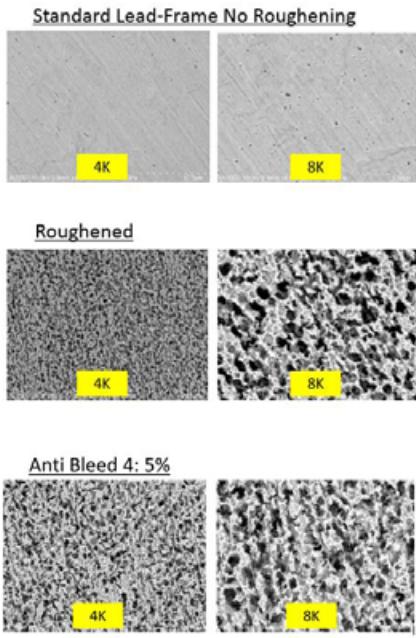


Figure 3: SEM image of a lead frame surface comparison before and after treatment.

additives to help define the surface morphology. During the process, etched copper ions react with organic components to form an organocopper coating that is deposited onto the alloy surface. It has been demonstrated that the roughened surface morphology produces improved adhesion, and that the coating is necessary to minimize loss of adhesion during post-mold heating excursions (e.g., reflow) (**Figure 3**) [1].

A disadvantage of the roughening process is that it leads to an increase in resin bleed out (RBO), sometimes referred to as epoxy bleed out (EBO). The sponge-like morphology of the alloy surface after treatment produces a capillary action that triggers a leaching or bleeding of the fluids in the die attach adhesives away from the adhesive deposit.

Methods to control epoxy bleed out

There are two key methods to control the EBO on a lead frame surface. The first is to tailor the die attach adhesive to the lead frame surface. The die attach formulation has added anti-bleed agents that minimize the flow out of resin and other organics onto lead frame surfaces. Each anti-bleed agent has a different response to the surface chemistry of the individual lead frame surface, thereby necessitating a compatible combination that will have delamination-free performance during MSL-1 testing.

The second method uses compatible anti-bleed coatings on the lead frame to match the chemistry of the die attach and minimize the EBO. From a surface treatment perspective, the key to limiting EBO is to control the surface energy on the lead frame. Application of a coating to the lead frame that reduces the surface energy will reduce the degree of capillary action and reduce/eliminate EBO. Theoretically, this can be seen from Young's contact angle equation (**Eq. 1**; see **Figure 4** for additional details):

$$Y_{SV} - Y_{SL} - Y_{LG} (\cos \theta) = 0 \quad \text{Eq. 1}$$

Where: Y_{SV} = Surface energy
 Y_{SL} = Interfacial energy between surface and liquid
 Y_{LV} = Surface tension of the liquid (droplet), and
 Θ = Contact angle between the liquid and surface

Rearranging the equation, we find the following observations. As the surface energy (Y_{SV}) decreases, the numerator increases and the term $\cos \theta$ decreases. This situation occurs when the contact angle θ increases. So decreasing the surface energy increases the contact angle, thereby decreasing wetting of the surface. This can also be accomplished without adjusting the surface energy by increasing the surface tension (Y_{LV}) of the liquid.

On the contrary, if the surface energy is reduced too much, the resin will resist wetting the surface and can "shrink" away or dewet from the surface. In a worst case, the adhesive will not wet the surface. Therefore, optimization to control EBO while maintaining the enhanced adhesion and thermal resistance properties is critical.

The combination of surface anti-bleed coatings on the lead frame and their compatibility with specific anti-bleed agents in die attach is studied and hereby presented as a compatible combination for delamination-free MSL-1 performance.

Experiments

The alloy surfaces were treated with MacDermid Enthone's standard PackageBond HT process: acid cleaner, mild micro-etch, PackageBond Predip, PackageBond HT coating, and alkaline Postdip. Etch rate was maintained in the 1.50-2.00 $\mu\text{m}/\text{min}$ range in order to maintain a consistent surface morphology. The surfaces were then treated with the

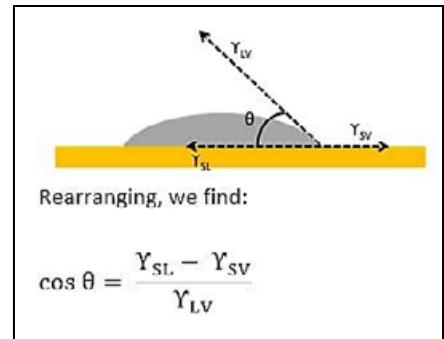


Figure 4: Relationship between the parameters in Young's contact angle equation.

Log#	LeadFrame	Roughening	AntiEBO Concentration (%)	DOE LAYOUT FOR RBO & OBS			Die Attach		
				DA1	DA2	Benchmark	DA1	DA2	Benchmark
1	CuQFN	PackageBond HT	0.50%	X					
2					X				
3						X			
4			0.75%		X				
5						X			
6							X		
7			5%			X			
8							X		
9								X	
10			7.50%		X				
11						X			
12							X		
13								X	
14									X
15									
16			0%	X					
17						X			
18							X		
		Standard - No Roughening							

Table 1: DOE layout for EBO and adhesion testing.

anti-bleed coating as shown in **Table 1**.

Two ATROX epoxy die attach products were evaluated with an external benchmark die attach product. The die attach adhesive was dispensed in a standard asterisk pattern and then staged for four hours before measuring the EBO on the different surfaces (**Figure 5**).

Lead Frame Finish	DA1	DA2	Benchmark
Standard No Roughening			
Anti-Bleed 4 0%			
Anti-Bleed 4 0.5%			
Anti-Bleed 4 0.75%			
Anti-Bleed 4 5%			
Anti Bleed 4 7.5%			

EBO Observed
No EBO observed

Figure 5: EBO results

All die attach products showed EBO on the roughened lead frame surface as expected. The two ATROX die attach products showed minimal epoxy bleed out on the lead frame surfaces treated with an anti-bleed coating, indicating good compatibility with the surfaces. **Table 2** compares the die attach materials in terms of key properties.

Experiment results for adhesion

Different die attach materials are tested on copper lead frames with different coatings to evaluate the adhesion strength and failure modes to determine the most compatible combination. Adhesion strength is measured by die shear at elevated temperature (260°C) (**Figure 6**). The failure mode is evaluated by inspecting both the die and lead frame surfaces after shear. The desired failure mode — cohesive — is indicated by adhesive remaining on both die and lead frame surfaces.

The benchmark product showed significantly lower adhesion on all conditions evaluated, indicating that the material does not possess high adhesion strength at high temperature. However, the samples treated with the brown oxide process exhibited improved adhesion strength for all adhesives, including the benchmark. The other important finding was that the two ATROX die attach products showed a very low drop in adhesion with untreated lead frames while using 5% of PackageBond Anti-Bleed 4. This demonstrates that both improved EBO resistance, in addition to increased adhesion strength at high temperatures, can be achieved with the proper combination of EBO reduction techniques (**Figure 7**).

Summary

The key finding from this study was that the use of roughening processes is critical for enhancing adhesion strength to lead frame surfaces; however, it is also critical to choose a compatible anti-bleed material that reduces/eliminates EBO on the lead frame surface and doesn't interfere with adhesion of die to the lead frame. This combination of treatments maintains the joint integrity during high stress such as MSL1 performance followed by a 260°C reflow process.

The two ATROX die attach materials, although different in properties, are shown to be compatible with the MacDermid

Properties	ATROX® DA1	ATROX® DA2	Benchmark
Chemistry	Non-Epoxy	Non-Epoxy	Epoxy
Weight Loss during cure	0.8%	1.35%	5.3%
Cure profile	175C/60min	175C/60min	175C/60min
Volume Resistance	0.0002 Ohm-cm	0.00008 Ohm-cm	0.0001 Ohm-cm

Table 2: Comparison of die attach materials in terms of key properties.



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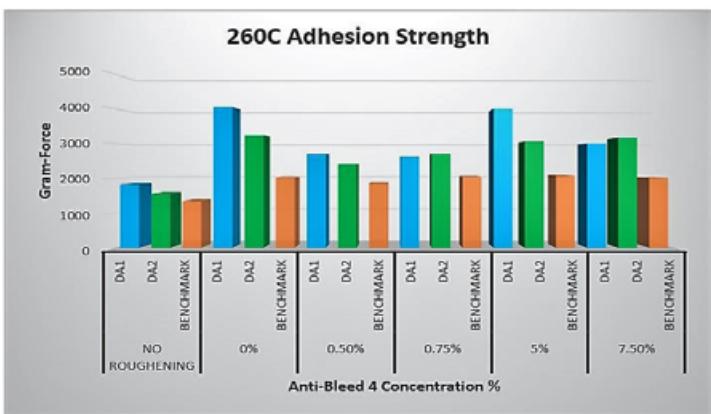


Figure 6: High-temperature adhesion results.

Enthon PackageBond HT roughening and PackageBond Anti-Bleed surface treatments, which lead to high MSL reliability.

Acknowledgment

This study is the result of a collaboration between Alpha Advanced Materials and MacDermid Enthon Electronics Solutions. Both are businesses of MacDermid Performance Solutions, a Platform Specialty Products company.

Reference

- D. Hart, B. Lee, J. Ganjei, "Increasing IC lead frame package reliability," 41st International Symp. on Microelectronics 2008, IMAPS Conf. Proc., 533, 2008.

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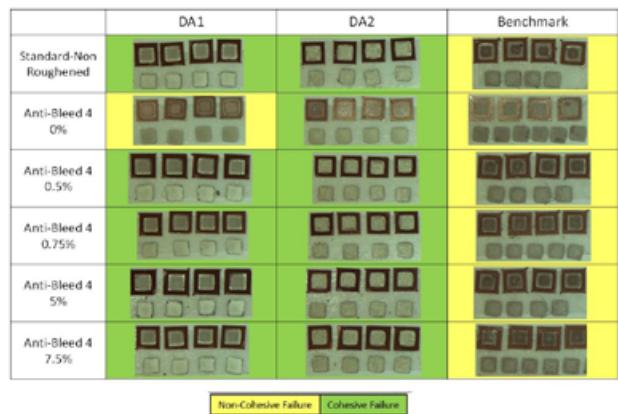


Figure 7: Failure modes of die shear adhesion results.

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3D integration technology for high-density/high-performance ICs

By Séverine Cheramy, Maud Vinet, Olivier Faynot [Leti]

Denser integration techniques have begun attracting more interest following many years during which the evolution of packaging was the main industrial driver for 3D integration. Efforts to maintain Moore's Law while meeting demand for high performance and/or low power consumption – and a combination of performance and small form factor – spurred innovation and alternative solutions to packaging for power-efficient 3D integration.

Additionally, the difficulty of associating in one 2D wafer heterogeneous processes, such as combining CMOS devices with flash memories or with "exotic" materials, including low-temperature dielectric film, also points the way to a 3D approach rather than a 2D sequential one.

For example, back-side-illuminated (BSI) imager vendors and their customers have recently achieved 3D density approaches with pitches in the range of 5 to 10 μm . It is no longer a dream to think about a 3D industrial integration within the range of a few micrometers pitch. This specific application may prompt interest in other architectures, such as memory denser stacking or partitioning of a large system-on-chip (SoC).

This article describes two complementary technologies developed at Leti that address such high density of 3D integration: 1) A back-end-of-line (BEOL)-type technology, based on hybrid bonding in the range of a few micrometers; and 2) A front-end-of-line (FEOL)-type technology, named CoolcubeTM, in the range of a few 100e of nanometers.

3D stacking using hybrid bonding

We begin this section by introducing the back-end-of-line (BEOL)-type 3D technology, based on hybrid bonding.

Principle. The hybrid bonding approach combines the excellent advantages of a room-temperature, no-pressure process that does not require underfill [1]. It consists of planarization in a chemical-mechanical-polishing (CMP) process of damascene

layers, including metal pads (in our integration, copper is used) surrounded by a dielectric layer (SiO_2).

Surface preparation is key to success for this integration: roughness and cleanliness are critical factors for a successful bonding. Here, the chemical mechanical polishing (CMP) process is finely tuned so that the copper pad shows very low dishing (typically a few nanometers). Additionally, to reach finer pitches, an alignment between both prepared surfaces also must be achieved, using EVG tools, for instance. After bonding and final curing, electrical and mechanical links are performed without any additional material, as shown in **Figure 1**.

Integration. Both wafer-to-wafer and die-to-wafer integration flows are possible. The wafer-to-wafer approach has been adopted widely for backside illumination (BSI) imagers for many years, using the top layers for photodiodes and the bottom layers for digital devices. This partitioning is a natural evolution of standard 2D BSI imagers [1,2]. **Figure 2** is a cross section of a 3D BSI imager structure.

The approach described above has proven to be reliable and robust and some products already on the market use a similar approach, which demonstrates that the hybrid bonding concept is compliant with integration of all BEOL layers. A deep morphological characterization plan led to a nearly perfect interface, with no defects or delamination, and with pad integrity similar to what has been shown in the R&D phase. Furthermore, a

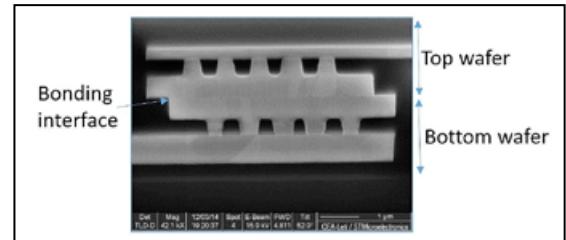


Figure 1: Cross section of a copper pad after bonding.
Courtesy: STMicroelectronics and CEA-LETI

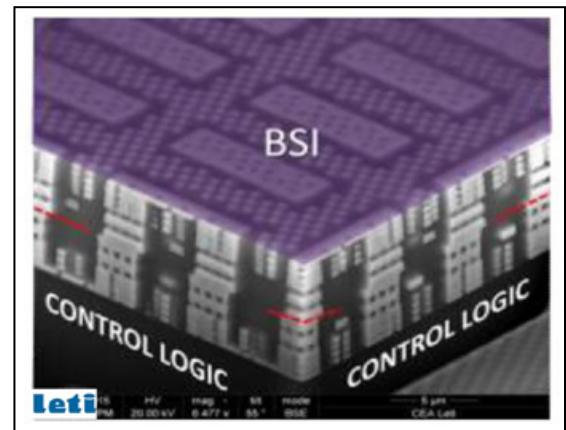


Figure 2: Scanning electron microscopy (SEM) images (3D view) of the 3D assembly including all metal levels of the BSI imager structure.

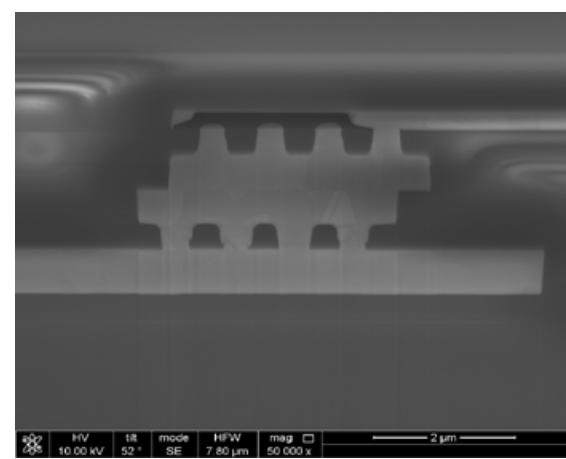


Figure 3: Cross section of the bonding interface after electromigration.
large matrix of electrical data is available: stability of the process is undoubtedly achievable. Finally, reliability tests,

particularly electromigration [3] complete the characterization plan (**Figure 3**).

Electromigration results indeed prove that a hybrid bonding architecture does not induce additional failure in comparison to the usual tests in BEOL layers: voids appear in the last metal level connected to the hybrid bonding interconnect. If, as noted, this wafer-to-wafer integration is near or already in production (3D BSI), it naturally raises some questions about yield. Cross yield loss when stacking two wafers together may erase all possible advantages of the integration, especially when considering insufficient yield from at least one of two stacked wafers. A chip-to-wafer approach is an alternative. The advantage of this approach is stacking known good dies on known good dies. Consequently, a presumed 100% yield wafer may be “rebuilt.”

Nevertheless, additional difficulties of the approach outlined above lead to a less mature integration. For example, proper handling of the dies is necessary, i.e., compatible with further copper-copper bonding: there can be no degradation or contamination of the die surface after dicing. The feasibility of this die handling, which is far more challenging than wafer handling, has nevertheless been proven [4], as shown in **Figure 4**. This feasibility paves the way for a promising industrial chip-to-wafer integration flow.

A pitch of 10 μm has been reached. In addition to proving that the bonding interface is morphologically similar to the one achieved with a wafer-level approach, the measured contact resistance is similar to the one achieved in the wafer-to-wafer approach and consequently, to the monolithic copper pad resistance. Nevertheless, to obtain such results, the pick-and-place equipment must achieve an accuracy of about $\pm 1\mu\text{m}$, and the handling of the die and the bonding itself must not contaminate the surface. SET, a French equipment supplier, is developing such a machine with Leti in an IRT Nanoelec program.

3D monolithic: CoolCube™

This section discusses the principle behind an alternative approach to a 3D integration scheme.

Principle. An alternative approach using high-density 3D integration is to rely on a monolithic 3D integration scheme (3D VLSI). Monolithic technology offers the possibility of stacking devices with a lithographic alignment precision, enabling

the introduction of 3D contact at the device level (up to 100 million vias per mm^2 with 14nm ground rules). 3D VLSI devices can be routed either at the gate or transistor levels. The partitioning at the gate level allows IC performance gain without resorting to scaling, thanks to wire length reduction. Partitioning at the transistor level by stacking NFET over PFET, or vice versa, enables the independent optimization of both types of transistors. This includes customized implementation of performance boosters: channel material/substrate orientation/channel and raised sources and drains strain, etc. [5], with reduced process complexity compared to a planar co-integration.

The ultimate example of high-performance CMOS at low process cost is the stacking of III-V NFETs above SiGe PFETs [6]. These high-mobility transistors are well suited for 3D VLSI because their process temperatures are intrinsically low. 3D VLSI, with its high contact density, can also be seen as a powerful solution for heterogeneous co-integrations requiring high 3D-via densities, such as nanoelectromechanical systems (NEMS) with CMOS for gas sensing applications [7] or highly miniaturized imagers [8].

Integration. By resorting to a unique alignment flow throughout the whole process, layers are stacked on top of each other within a lithographic alignment precision, as shown in **Figure 5**.

The bottom layer is first processed up to a few metal layers (typically two or four depending on the technology) in an almost standard CMOS flow. It can be any CMOS technology, from bulk planar to FinFET or fully-depleted silicon-on-insulator (FDSOI). The process can be tweaked slightly to increase the silicide thermal stability, if needed [9]. A blanket wafer is subsequently transferred at low temperature on top of the bottom layer, using direct bonding either of a silicon-on-insulator (SOI) wafer, or by using

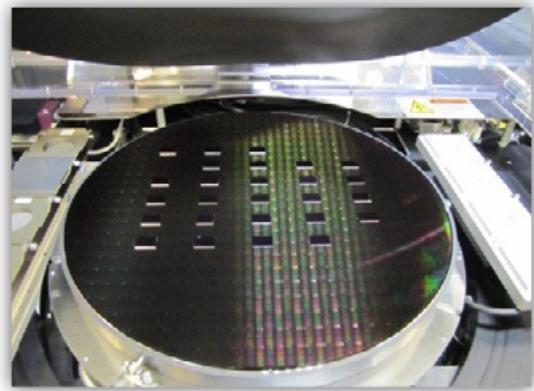


Figure 4: Chip-to-wafer approach using hybrid bonding.



Figure 5: CoolCube™ principle and transverse electromagnetic (TEM) cross section of processed devices.

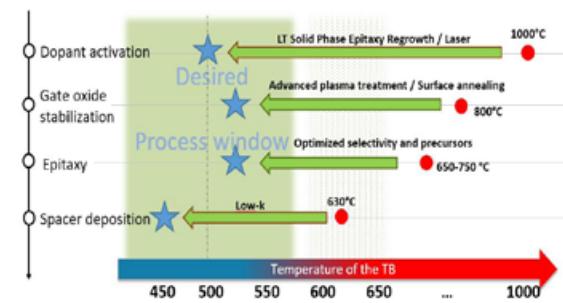


Figure 6: Top thermal budget analysis and solutions to bring the process temperature of the critical thermal steps in the 500°C range.

hydrogen implantation and splitting. Top-layer lithography relies on a single-stream alignment flow, leading to excellent alignment precision between top and bottom transistors. Top devices are subsequently fabricated with a low thermal budget to preserve the bottom layer's metal oxide semiconductor field-effect transistor (MOSFET) performance. **Figure 6** shows how, in order to design the low thermal budget process flow, the hot modules are engineered to lower their thermal budget and match it with the bottom layer thermal stability.

Results. Thanks to solid phase epitaxy, high-performance/low-

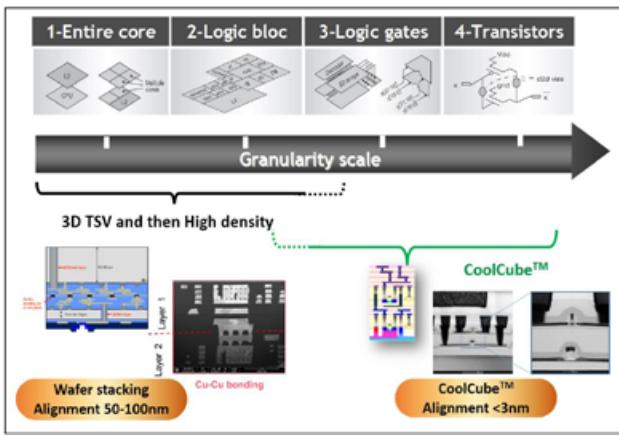


Figure 7: 3D integration pitch roadmap.

temperature junctions have been designed to match standard process flow, where junctions are activated using rapid thermal annealing at 1,050°C. Low-temperature epitaxy has been demonstrated with the use of disilane and Cl₂ as precursor and etching gas. Low-k spacers based on SiCO deposited at 400°C have demonstrated similar DC performance as SiN, but with improved ring oscillator performance [10]. Finally, compatibility with production line environment has been demonstrated, thanks to a dedicated contamination-containment protocol.

Pitch roadmap

As described before, the pitch roadmap of hybrid bonding both at wafer-level and at chip-level strongly depends on equipment accuracy, whereas in the case of monolithic 3D integration it depends only on lithographic alignment precision of the stepper (**Figure 7**). The capability of high throughput is also key at chip level.

So far, wafer-level bonder equipment suppliers have reached alignment of a few hundreds of nanometers. Going further is no longer a pure equipment challenge. A complete process understanding is necessary, including previous steps of the wafers (BEOL). Close collaboration between equipment suppliers and process experts is required to improve final alignment.

In the frame of IRT Nanoelec, and thanks to the collaboration between EVG and Leti, a perspective of a pitch of 1-2µm is scheduled in 2017, and when taking into account perspectives of equipment suppliers (+/-40nm), a pitch of 500nm or less could be reachable in the very near future. For a chip-to-wafer process, a target of +/-1µm is scheduled in the

common work of the IRT Nanoelec program, with SET's new equipment platform SET1. This target, scheduled by 2018, could open the door for a chip-to-wafer integration with a pitch of a few micrometers.

CoolCube™ allows the same range of 3D-contact density, i.e., in between the layers of devices, as planar-contact density. This high via density is needed for two reasons. First, because lithography

strategy relies on a single-stream alignment flow, the alignment precision between the layers only depends on the lithographic alignment capability of the stepper, and for state-of-the-art lithographic tools it is in the 5nm range. Second, the 3D contact process is close to a standard 2D tungsten contact plug: the 3D contact is a simple contact in an oxide and its aspect ratio is kept very similar to the one in a 2D integration; as an additional consequence, there is no keep-out zone.

Summary

This paper describes the process flows for very high 3D integration: 3D stacking, (wafer-to-wafer and chip-to-wafer), as well as 3D monolithic CoolCube™ technologies are considered as complementary approaches to produce high-performance devices. CoolCube™ and 3D stacking are considered for performance, cost and form factor reduction. The promising results reached for both integrations give high confidence for their use in fabricating products in the near future for a wide range of applications.

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References

1. S. Lhostis et al., "Reliable 300mm wafer-level hybrid bonding for 3D stacked CMOS image sensors," 2016 IEEE 66th Elect. Comp. and Tech.

Conf. (ECTC), 31 May–5 June 2016, Las Vegas, NV USA.

2. L. Benissa, et al., "Next-generation image sensor via direct hybrid bonding," 2015 IEEE 17th EPTC Dec. 2–4 2015, Singapore.
3. S. Moreau et al., "Mass transport-induced failure of hybrid bonding-based integration for advanced image sensor applications," 2016 IEEE 66th ECTC, May 31 – June 5, 2016, Las Vegas, NV USA.
4. Y. Beillard et al., "Chip to wafer copper direct bonding electrical characterization and thermal cycling," IEEE International Conference on 3D System Integration (3D IC), 2013.
5. P. Batude, et al., "GeOI and SOI 3D monolithic cell integrations for high-density applications," Symp. on VLSI Technology Digest of Technical Papers, A9-1, p.166-167, VLSI 2009.
6. T. Irisawa, et al., "Demonstration of InGaAs/Ge dual-channel CMOS inverters with high electron and hole mobility using stacked 3D integration," IEEE VLSI (2013).
7. I. Ouerghi, et al., "High-performance polysilicon nanowire NEMS for CMOS embedded nanosensors," Sect. 22.4, pp. 1-4, IEDM 2014.
8. P. Coudrain, et al., "Setting up 3D sequential integration for back-illuminated CMOS image sensors with highly miniaturized pixels with low-temperature fully-depleted SOI transistors," IEDM 2008.
9. L. Brunet, et al., "Direct bonding: a key enabler for 3D monolithic integration," Electrochemical Soc. ECS, 2014.
10. L. Pasini, "High-performance CMOS FDSOI devices activated at low temperature," VLSI 2016.

Biographies

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Inkjet-based additive manufacturing addresses challenges in semiconductor packaging

By Wouter Brok, Henk Goossens, Klaus Ruhmer [Meyer Burger]

Growing demand for semiconductors in wearable electronics, automotive and Internet of Things (IoT) applications, drive the development of miniaturized and lower cost semiconductor devices. Additive manufacturing and printed electronics technologies like inkjet printing of functional materials have a number of unique benefits over traditional semiconductor technologies that enable further miniaturization and process cost reduction.

Just like traditional dispense technology, inkjet printing deposits small droplets of functional liquid materials onto a substrate. What makes inkjet unique is that droplets are much smaller (picoliter volume), are jetted by thousands of individually addressable nozzles at the same time, and are deposited in a non-contact manner. With this technique, patterned and homogeneous layers can be produced, also on 3D surfaces. Even 3D structures can be printed directly. These benefits are recognized in many industries such as printed circuit board, photovoltaics, display, 3D printing, and even pharmaceuticals where inkjet technology finds its way into industrial manufacturing.

Where the feature size of inkjet printing is not compatible with most semiconductor front-end processes because sub-micron patterning is required, many wafer-based back-end-of-line (BEOL) and strip-based packaging process steps need features of tens of microns up to millimeters, and can benefit from inkjet technology. Therefore, inkjet printing is being adopted by some of the largest semiconductor producers in the world. In this article we will review the advantages of inkjet printing in comparison to traditional technologies, give an overview of inkjet-compatible

materials and highlight two application examples of the technology.

Basics of functional inkjet printing

Today, everybody is familiar with inkjet printing because it is widely used for graphics printing in home and office printers, in large-scale production of magazines, bill boards, and even for applying a design onto ceramic tiles. That said, it is important to highlight some basics of the technology and the differences between graphics printing and functional inkjet printing as applied in electronics and semiconductor manufacturing. All inkjet print heads are based on the principle of pushing a low viscosity liquid out of a number of individually addressable tiny channels, or nozzles. The very small droplets that are created in this way eventually form the pattern on the substrate. In home and office printers, a thermal pulse is used to invoke a droplet. However, for the application of printing electronic materials, a much higher accuracy and reliability is needed, which therefore restricts the choice of print heads to piezo-driven high-quality heads as used in industrial, large-scale graphics printers. **Figure 1** provides an illustration of a droplet in flight.

Although they share the basic print head technology, it should be noted, that printing equipment for graphical and for functional applications (such as the example shown in **Figure 2**) also have a lot of differences. The accuracy and reliability requirements and the

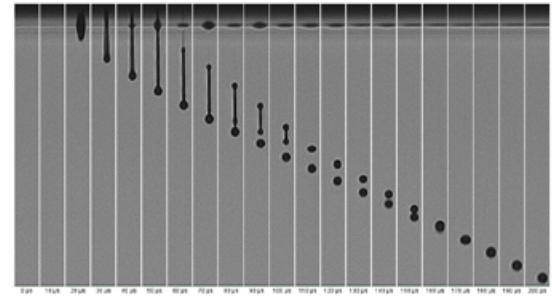


Figure 1: An inkjet droplet in flight in the first 200μs after the piezoelectric excitation of a nozzle.

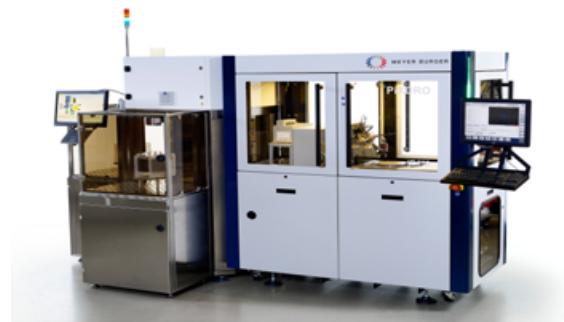


Figure 2: Example of a functional inkjet printer for semiconductor fabrication.

diversity of applications and inks to be processed have a large impact on the machine design of a functional printer. These specifications ask for a high-precision motion platform, precise pattern rendering, modular design, adequate head inspection and maintenance functionality, as well as substrate handling.

Comparison between inkjet and traditional technologies

The cost reduction potential of inkjet printing becomes apparent when comparing it to lithography. The ability of inkjet printing to directly produce patterned layers from a digital file avoids the need for expensive lithography tools and associated processes such as resist coating, mask production, development and etching. All these steps are typically



Figure 3: Example of precise inkjet printed dams for dam-and-fill applications.

	Inkjet	Lithography	Screen printing	Spin/spray coating	Dispense
Low process cost	+	--	-	-	+
Feature size	+	++	-	--	-
Throughput	++	+	+	-	+
3D capability	++	-	-	-	-
Flexibility	++	-	-	+	++
Large area	+	+	-	--	+

Table 1: Characteristics of the inkjet process compared to other methods.

replaced by only two steps: printing and curing. This not only saves cost, it also adds flexibility. Avoiding a mask enables a fast changeover between different products. The additional benefit of inkjet printing is the efficient use of material. Spin coating and spray coating technologies waste between 70% and 90% of the applied material, compared to virtually no waste for inkjet printing. Overall cost savings as high as 90% for certain process steps have been reported.

As will be explained in the next section, inkjet printing can also be applied to produce a direct printed mask. With such a process, the production of a hard mask, lithography and development are avoided and a digitally printed mask is directly used in a subsequent etching or metallization step. Although not fully additive,

this approach has many advantages too: a high level of compatibility with existing circuit etching and plating technology, quick product changeover with digital printing, and still a significant cost reduction.

The small drop volume (down to 1 picoliter) and accurate drop placement (down to a few microns) gives inkjet printing a miniaturization benefit over dispense technology. It especially offers the possibility to reduce keep-out zones, for example by printing dam structures for dam-and-fill applications (as demonstrated in **Figure 3**) or dispensing adhesives. Moreover, thousands of parallel nozzles in an inkjet printer yield a throughput advantage over single-nozzle dispense.

Compared to the more well-known screen printing technology, inkjet avoids the cost of screens by directly printing from a digital layout, it improves on feature size and especially enhances registration on large substrates. In general, inkjet is well suited for large rectangular substrates (for example in panel-based packaging),

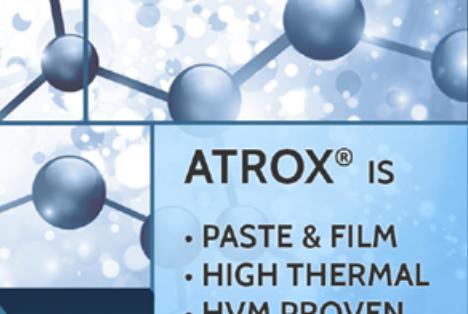


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also for blanket coatings. Both spin and spray coating technologies struggle to create homogeneous layers on such large substrates.

It is worth highlighting the 3D capability of inkjet printing. With a typical jetting distance of 0.5 to 1mm, inkjet is a contactless manufacturing technology. Therefore, it is better suited to deal with 3D topology than other coating and printing technologies. One can jet material into vias, cavities and trenches, cover heights of 100s of microns and even print onto the edges of wafers or dies. Furthermore, fast curing (e.g., UV curing) materials can be used for 3D printing applications. Although the third dimension in most semiconductor applications is limited to hundreds of microns, such features need 3D printing capability, which includes multi-layer printing of slices with good layer-to-layer overlay accuracy. **Table 1** provides an overview of characteristics of inkjet printing in comparison to other manufacturing methods.

Inkjet materials

For a reliable and high quality inkjet process, materials need to be specifically formulated for inkjet applications. First of all, the viscosity needs to be in the range of 2–20 centiPoise (cP). Additionally, aspects like surface tension, particle size and particle loading have to be optimized. A growing number of chemical suppliers, both large companies like Dow, Dupont, Taiyo, and JNC, to name a few, and specialized start-ups, are commercializing inkjet formulations and have a range of appealing new and advanced materials under development, often based on a reformulation of spin or spray coating versions of well-known semiconductor materials.

Commercially available dielectric materials include polyimides and polyimide-like materials, epoxy and epoxy-acrylates. These polymers can be applied with layer thicknesses of several microns up to hundreds of microns. Even at low layer thicknesses, polyimides offer a very high electrical resistivity, opening opportunities of using inkjet application even in power device manufacturing. Polymer materials are typically cured by UV photo-polymerization or thermal

baking, and UV sources and hotplates are often included in printing equipment in order to minimize operator handling.

Another important class of materials is the group of resists. As explained above, these can be used for direct printing of etch or plating masks. Hot melt or wax-based materials have a high chemical resistance against wet chemical etching and metallization baths. For a large thermal window, they are especially formulated in a mixture with UV curing components. Such inks also have high mechanical resistance, thermal stability, and very good adhesion properties. Their excellent printing properties make them very suitable for etching copper circuits and plated interconnects. Glass and silicon have also been successfully etched using such printed resists. Furthermore, traditional acrylate-based photoresists and imprint resists can be printed. Some spin coating formulations can be made jettable with minimal modifications. Both hot melt and photoresist materials can be stripped with well-known low concentration hydroxide or amine-based chemicals. However, some applications require a more permanent resist. For such cases, epoxy-based SU-8 resist or polyimide can be used.

Conductive inks are a third class of important materials. A mainstream material for printed electronics is silver nanoparticle ink. Sub-micron silver nanoparticles are suspended in a solvent and upon printing can be sintered at low temperatures (<150°C) reaching up to 40–50% of bulk silver conductivity. A number of ink suppliers have made significant advances in copper nanoparticle inks as well. For advanced applications, transparent conductor materials based on either organic PEDOT or silver nanowires are available, and even semiconducting materials for completely printed transistors have been developed.

Next to the commercially available materials noted above, there is a large selection of advanced materials under development, such as specialized adhesives, graphene and quantum dot inks, sensor materials for gas detection, optical sensors and biomaterials, materials for passive components such as resistor material.

More generally, the ongoing innovation in nanoparticle, nanowire, and polymer science will yield many more interesting inkjet materials.

Examples of inkjet applications

A typical example of inkjet enabled miniaturization is routed quad flat no-leads (QFN) packaging. Routed-QFN combines the advantages of traditional QFN with those of organic substrates. By applying a copper lead frame with an advanced fan-out structure, it offers higher I/O pin counts with respect to traditional QFN, combined with excellent thermal and electrical properties. Because the more complicated fan-out structure would lead to free-standing lead fingers, the manufacturing process for routed-QFN lead frames involves a dual-etch procedure as shown in **Figure 4**.

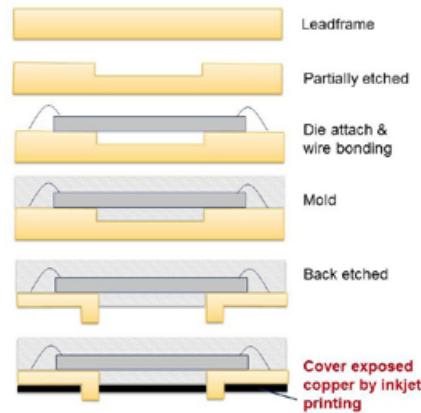


Figure 4: Manufacturing procedure of a routed-QFN package.

First, the lead fingers are etched halfway through the lead frame. After die attach, wire bonding and molding, the lead frame is etched back from the bottom side yielding the final structure of free-standing lead fingers (now supported by molding compound) and protruding solder contacts. The challenge, however, is that after back etching of the lead frame, the exposed copper is to be encapsulated without contaminating the contacts and leaving enough stand-off for reliable soldering. **Figure 5a** illustrates an example of a routed-QFN device. Encapsulating the exposed copper is a difficult task for molding, dispense or screen printing technology.

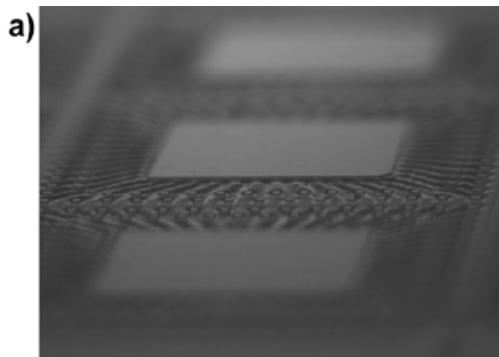


Figure 5: a) (left) An example of a routed-QFN package; b) (right) Close-up image of a routed-QFN package.

The required layer thickness is in the tens of microns range—too thin for molding. For dispense and screen printing technology, the feature sizes are a challenge and they easily contaminate the contact points due to overfilling by dispense or contact with a screen. Inkjet technology, however, precisely prints small droplets of dielectric material in a thin layer around the contacts and has no problems with the 3D topology of the lead frames. In **Figure 5b** the close-up picture demonstrates how the inkjetted material creates a closed layer, contamination-free contacts, and nice fillets around the contact point for reliable soldering. Inkjet-printable solder mask offers the right specifications in terms of layer thickness, resistivity and adequate reliability in terms of adhesion and solder resistance.

As discussed above, creating patterned dielectric layers is an important process in semiconductor packaging. Often, lithography and photo-imageable materials are used. Inkjet offers the possibility to directly print such layers with all the benefits associated with additive manufacturing. A field that offers great opportunities is the application of the outer repassivation layer on wafer-level packages. This layer provides extra protection to the die and mechanical support for the solder joints for board-level reliability. Typical bump pitches are 500 μ m and smaller with bump pad openings of 300 μ m and smaller. Such structures can be printed directly using polyimide or other polymeric dielectric materials. **Figure 6** shows a range of patches with openings compatible with typical wafer-level package (WLP) solder ball dimensions.

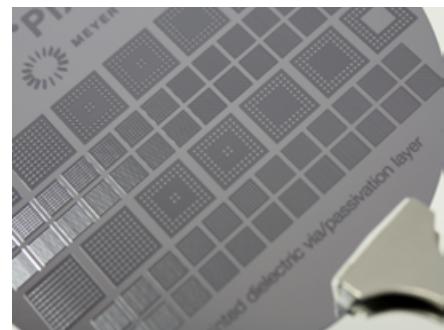
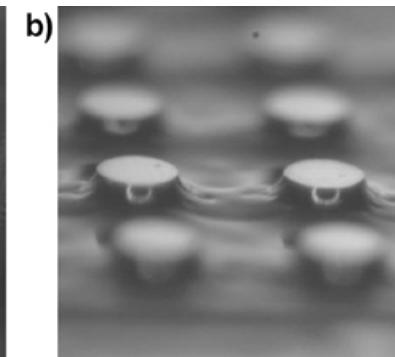


Figure 6: Printed dielectric patches for wafer-level packaging.

Flexible hybrid electronics

Endless opportunities for truly flexible and wearable electronics that are conformable, lightweight and low cost are driving a new trend in electronics packaging: flexible hybrid electronics (FHE). In hybrid electronics, the advantages of printed electronics and silicon technology are combined. The weight and flexibility of such very-thin FHE devices allows them to be even worn directly on the body, opening up all kinds of applications in medical, consumer, and military spaces. Printed electronics offers low-cost, lightweight substrates with (digitally) printed circuitry on polyethylene terephthalate (PET) or polyethylene naphthalate (PEN) foils. Although nowadays, complete transistors can also be printed and will appear in products for simple logic and amplification functionality, silicon integrated circuits are still the preferred solution when it comes to implementing digital intelligence. When applying bare and thinned dies to the PET or PEN foil, a fully flexible piece of electronics is created. In this cross-over area between IC packaging and electronics assembly industries, a number of proven packaging technologies are no longer applicable. For example, wire bonding on printed circuitry on a polymer foil meets huge difficulties—the high-temperature ultrasonic welding process is simply not compatible with thin conductor layers on top of a plastic film. Also, die bonding will have to be approached in a different way in order to prevent breakage or overfilling of fragile thin dies. Inkjet technology is offering great opportunities in this area—not only for digitally printing multi-layer circuitry, but also for printed interconnects

and precise dispensing of die attach material. Under the umbrella of the San Jose-based NextFlex consortium, a large number of equipment suppliers, material suppliers, electronic manufacturing (EMS) companies, universities and research institutes are teaming up to solve the challenges of this next-generation electronics.

Adding up the opportunities in both IC manufacturing and new fields like FHE, recent material developments and advances such as those in print head technology, we expect a broad increase in functional inkjet printing as an additional manufacturing technology in semiconductor packaging.

Biographies

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Chip over-test: are ICs tested too much?

By Dale Ohmart [Texas Instruments]

It can be difficult to understand the trends of test cost in the IC industry. One common metric is to measure the capital spent on test systems against the revenue produced by chip makers (Figure 1). When evaluated that way, it appears that there is a long-term trend in the downward direction. Over the last five years, this downward trend has slowed significantly. As the average selling price of automatic test equipment (ATE) systems has come down over the last several years, the cost of handling equipment and infrastructure has grown to roughly 50% of test cell capital price. The total capital investment for test is currently around 2% of semiconductor revenue.

Industry growth over the next few years is forecast to be in the industrial and automotive markets. Industrial and automotive applications generally demand more complex and expensive test flows. It seems safe to conclude that there will be upward pressure on test costs over the next few years. Test professionals should see this as a challenge. More specifically, the following issues should be considered: 1) How can test cost reduction be accelerated?; and 2) More testing, and consequently higher test cost, is perceived as a path to better quality (e.g., automotive, industrial applications). Is more test the best way to achieve better quality?

IC manufacturing test and quality

The primary purpose of testing ICs as part of the manufacturing process is to identify defective units and remove them from the population of units delivered to customers. The test process is required due to the fact that IC manufacturing produces a mix of units, some that conform to the product specifications and some that do not conform. Conforming units will be called “good” units, and nonconforming units will be called “rejects.”

In IC manufacturing, rejects can generally be classified as being produced in one of two ways.

1. Defects: Defects are inherent in the IC manufacturing process. The geometries are very small. There are a large number of process steps. Particle defects, setup errors, and

machine failures are a few examples of special causes that can cause defects to be introduced into some of the manufactured units.

2. Parametric: Many terms are used to describe these failures, but it all comes down to cases where the desired product characteristics cannot be consistently achieved with the available manufacturing process. The part will generally function correctly, but will not meet some expected performance characteristic. These rejects are caused by common causes.

Common cause (parametric) rejects are a result of product requirements (specifications) that are less than the distribution of the manufacturing process. Test engineers will describe this as a requirement to “truncate the distribution to meet spec.” In a normal distribution, if the specification accepts ± 3 sigma of the manufacturing distribution, then 0.27% (2700DPPM) of the product will be nonconforming. If the specification accepts ± 6 sigma, then 0.006% (60DPPM) will be nonconforming.

When test is used to truncate the manufacturing distribution this way, the result will be that some nonconforming product will be shipped. This is a result of the simple fact that all test measurements have uncertainty (i.e., common cause measurement variation). Any tested product parameter that is close to the product spec limit will have some probability of resulting in an incorrect pass/fail result for that



Figure 1: Capital spent on test systems vs. revenue produced by chip makers. SOURCES: Gartner, iSuppli

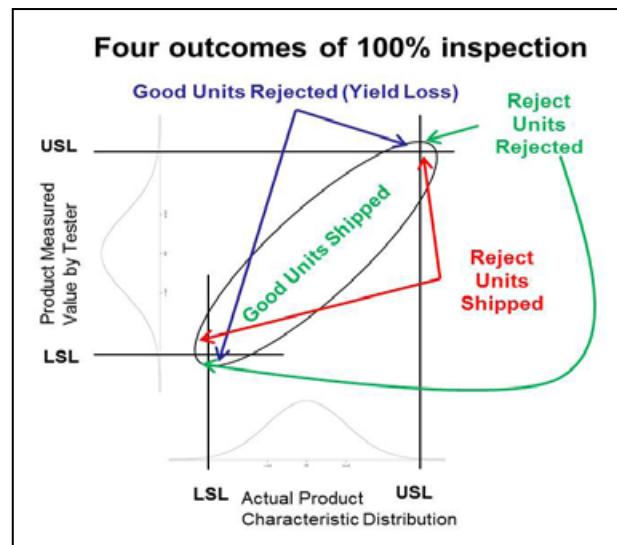


Figure 2: Four outcomes of 100% inspection.

parameter on account of test measurement variability (Figure 2).

The number of reject units shipped is some fraction of the actual rejects manufactured. The size of that fraction is related to the measurement accuracy of the test. For this discussion, it is sufficient to point out that for parameters with a ± 6 -sigma spec limit, the fraction is multiplied by a 60DPPM population of nonconforming units. For products with a ± 3 -sigma spec limit, that same fraction is multiplied by a 2700DPPM population of nonconforming units. Everything else being equal, the 3-sigma spec limit

causes 45 times the probability of shipping a nonconforming unit.

Note also that there is a result of good units rejected. Test introduces scrap of good units when test spec limits are set to truncate distributions. The typical response by the test industry to this loss is to reduce the Y-axis distribution by providing more accurate (and generally more expensive) instrumentation.

Test achieves much better results in sorting special causes of rejects. Special causes will produce units that are clearly distinguishable from the population. There is no requirement to sort units based on performance that is very near the specification limit. Many of these units will simply not operate at all.

In summary, IC testing will undoubtedly pass rejects to customers in the case of truncated distributions or common causes of nonconformance to spec. On the other hand, special causes should always be detectable by testing, so none of this type of unit should escape to a customer. It is instructive to review actual manufacturing data on reject units identified by customers. **Figure 3** is an example of customer identified units that did not conform to customer expectations. The categories of failures identified by customers are all related to manufacturing defects (special causes), not to product performance characteristics. If these types of defects are easy to detect, then why do customers see these types of rejects?

The answer to the above question lies in recognizing that test itself is a manufacturing process. It has both common cause variation and special cause variation. Common cause variation in test results causes test pass/fail results to be grouped into the four outcomes discussed above. Special cause variations in test results are caused by errors in the test manufacturing process. A test cell is a complex of tester, handling equipment, device interface board (DIB), contactor, and some communication link between the tester and handler. Many manufacturing process errors are possible, a few examples are: 1) Tester related: failed hardware, wrong test program, test program error; 2) Handler related: wrong

temperature, jam recovery errors, sort errors; 3) Device under test (DUT) interface-related: failed component, incorrect calibration, wrong component; and 4) Tester/handler communication errors. Finally, where are the customer returns from the common cause outcome “reject units shipped?” It seems that there is a low probability of such devices being returned.

A common approach to the “reject units shipped” issue is to test to tighter than spec limits, by applying what are known as guard bands to the test limits. This changes the relative size of the “reject units shipped” and “good units rejected” categories, essentially increasing the false yield reject losses to eliminate the performance quality escapes. This is one possible reason that customer returns rarely include close-to-the-limit parametric rejects. Another possibility is margin in the customer system. Well-designed systems have margin tolerance. It is possible that customer manufacturing processes are not as sensitive to functional units with small margin failures as they are to non-functional gross test escape-type (GTE) units.

It is easy for a test engineer to move from the logic of: 1) Sort out defective units, to 2) Verify every unit shipped is good; to 3) Test every spec on every unit. The data show consistently that the “test every spec” approach to manufacturing test is not required, and in fact, leads to yield loss, as well as increased test time and cost.

Returning to the question of the purpose of manufacturing test and summarizing, the following are key considerations: 1) Managing test cost is a key requirement of all manufacturing test; 2) The objective of manufacturing test is to sort out the defective units; 3) Appropriate test requires understanding sources of variation in the product being tested and in the test process; and 4) Using test to truncate distributions introduces test-related scrap (yield loss) and still allows some rejects to ship. Shipping rejects can only be avoided by accepting greater test-related scrap of good units due to use of guard bands. The conclusion one comes to given the above discussion is

this: avoid the “test every spec” trap in IC manufacturing test.

Understanding test cost

The effort to reduce the cost-of-test (CoT) starts with understanding the underlying sources. Conceptually, test cost/unit is very simple. It boils down to the cost of owning and running the test cell (often called cost-of-ownership or CoO) divided by the number of units the test cell can produce. Looked at on an hourly basis, the following equation applies:

$$\text{CoO-per-Hour/PPH}, \text{ where PPH is the tested parts per hour.}$$

CoO is a function of the test equipment purchase price and the cost to operate the equipment. Most of this cost is driven by the initial capital investment decision. Depreciation is fixed based on the original investment, of course. Facilities and repair and maintenance are also largely driven by the requirements of the equipment purchased.

The initial capital decision is critical in managing CoO. This decision must be made with full knowledge of the facilities requirements of the equipment, the reliability of the equipment, and the required configuration for the target products.

A common approach to managing CoO is to improve CoO per test socket. Recent innovations in IC test have led to an explosion in multi-site test. In the past, very high multi-site testing was largely confined to memory test. In the current environment, it is being applied to system-on-chip (SoC), microcontroller, and analog devices with great effectiveness. The hourly CoO of the test cell goes up when supporting higher site counts, but the cost per test site can go down dramatically (**Figure 4**).

The concept of CoO per test socket is powerful, but the corollary is that it can lead to fragmentation of configurations in a test factory in the attempt to achieve maximum site count for many different products. This makes the challenge of good initial capital decisions more difficult, but even more important.

The benefit of spreading CoO across multiple test sockets also provides the opportunity to reduce the effective test time per unit (TTeff) through performing parallel test of some or all of the tests. This can be a somewhat expensive strategy. It requires testers with more instrumentation, handlers with more sites, and DUT interface hardware of higher complexity. It is necessary to balance the higher capital investment and support costs against the benefit of CoO/site and test time/unit reduction.

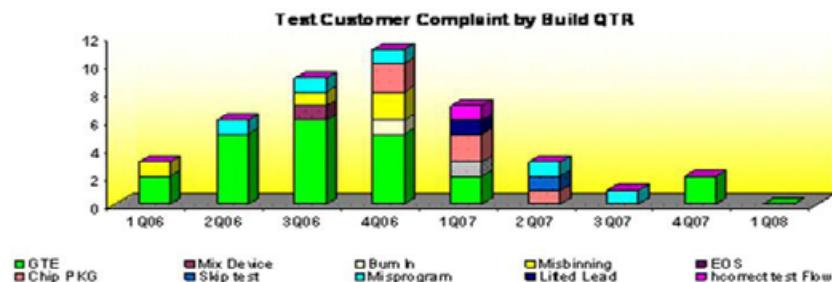


Figure 3: Test customer complaint by build quarter.

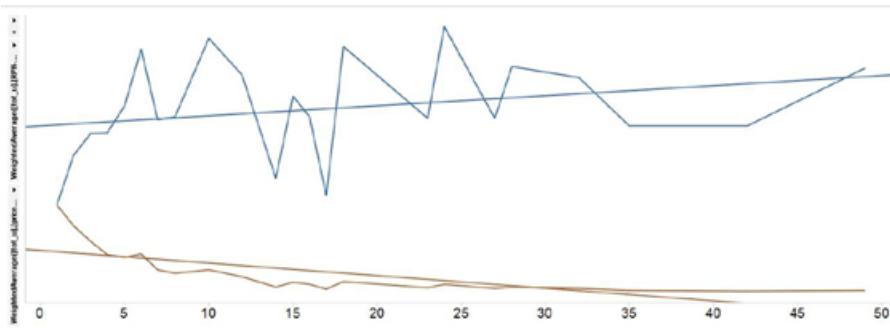


Figure 4: Final test cost-of-ownership (CoO) vs. multi-site. Note: y-axes is WeightedAverage

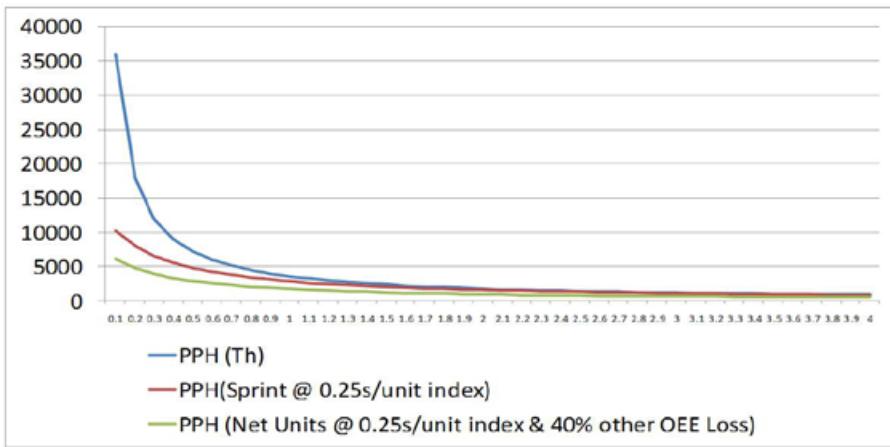


Figure 5: Simple models of PPH vs. unit test time.

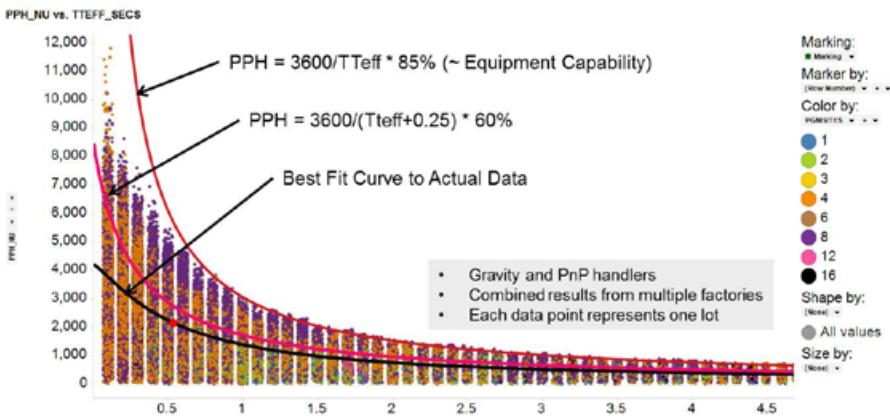


Figure 6: Net PPH vs. test time (measured data by lot).

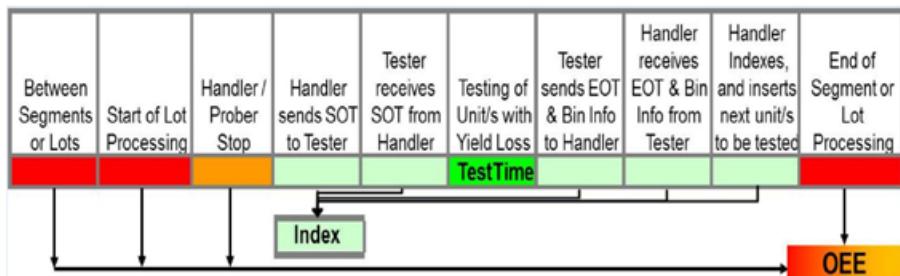


Figure 7: A (not to scale) concept graphic of the typical manufacturing test cycle.

The other approach that can be used to reduce test cost is improving throughput, or PPH. This is often considered equivalent to reducing test time, or reducing test time/unit. Test time/unit can be reduced by reducing test time or increasing site count. Certainly, test time reduction is a big factor in PPH improvement. In its simplest form,

$$PPH = 3600 \text{sec-per-hr/test time-per-unit.}$$

However, test time is not the whole story. This is especially true as test time approaches 0s. At low test time per unit, other factors, such as handler index time and factory overhead, begin to significantly limit PPH. A slightly better, but still simple, model is

$$PPH = 3600 \text{sec-per-hr}/(\text{test time-per-unit} + \text{index time-per-unit}) * \text{OEE}$$

where OEE (overall equipment efficiency) is a measure of the effective utilization of the test cell (**Figure 5**). As test time falls below about 1.5s/unit, the predictions of output diverge significantly.

Models are interesting, but it is always useful to verify the model against real-world data. The simple model above, using 60% OEE and 0.25s/unit index time predicts a maximum output around 5,000PPH to 6,000PPH. Recent data using traditional test approaches (gravity and pick-and-place handlers, maximizing multi-site, and test time reduction) show that aggregate factory performance does not quite match this model. The divergence at low test time is quite large (**Figure 6**).

It is clear that the traditional approaches noted above have a point of diminishing PPH returns for the effort and expense involved in driving down the test time curve. The typical factory performance maximizes at around 3,600PPH. This is not precisely a limitation of the equipment capability. The equipment capability can be visualized by tracing a curve along the top of the curve, which reflects the best performing lots. This view makes it clear that the equipment is capable of achieving two to three times the actual factory performance. It is when the aggregate average performance is measured that the productivity limitations become apparent. A (not to scale) concept graphic of the typical manufacturing test cycle helps to explain what is happening (**Figure 7**).

The time shown in dark green is the actual time the DUT is in the test socket being evaluated by the tester. The time shown in light green is the “index time” overhead of sorting tested units, then inserting untested units into

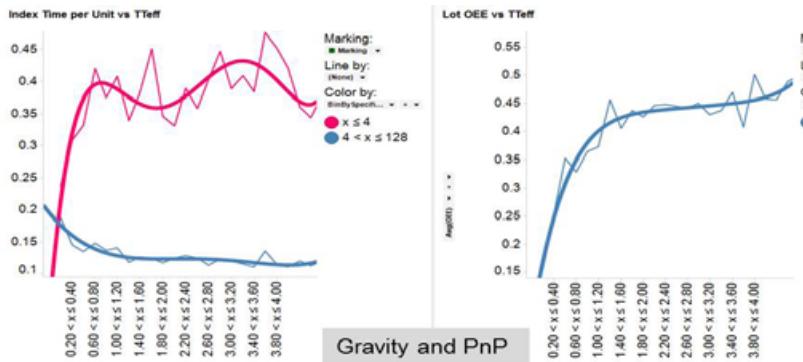


Figure 8: Test time dependency of index time and OEE. Note: In this view, “Index time” means the total time to cycle tested units out and insert untested units. This may be limited by handler input load time, handler soak time, handler sort time, or other variables.

the test socket. The time shown in orange is the time when the handling equipment stops for an equipment-related reason, such as a jam, waiting for new parts, no more material to test, or other stops during testing the lot. Finally, the time shown in red is the factory overhead of moving from one lot to the next lot. The in-lot stops and the between-lot processing are grouped into an overall OEE loss.

With the right tools, it is possible to measure both index time and OEE performance on a lot-by-lot basis. From the same aggregated data used in **Figure 6** is a view of the test time dependency of index time and OEE (**Figure 8**).

The results shown in **Figure 8** lead to a few conclusions: 1) At higher multi-site counts, index time goes up in a nonlinear fashion at low test time per unit (<1s); 2) OEE never gets above 50% (half the time, the test cell is waiting to test units); and 3) OEE drops in a nonlinear fashion at low test time per unit (<1s). Handling equipment manufacturers can explain the throughput limits of each handler type at low test time. This explanation is generally available in the documentation.

The OEE loss at short test time is significant, and perhaps more difficult to understand. The calculation used for OEE here is:

$$OEE = \frac{\text{LotTestTime}}{\text{AllTime}}$$

where

$\text{LotTestTime} = (\text{TestTime-per-unit} + \text{IndexTime-per-unit}) * \text{UnitsTested}$ and AllTime can be thought of as

$$\text{AllTime} = \text{LotTestTime} + \text{AllManufacturingOverhead}.$$

Then

$$OEE = \frac{\text{LotTestTime}}{\text{LotTestTime} + \text{AllManufacturingOverhead}}.$$

Consider that LotTestTime is
 $(\text{Test Time}/\text{unit} + \text{Index Time}/\text{unit}) * \text{Tested Units}$.

reduces yield while not necessarily improving the quality of product shipped. The current industry response to this trap is more accurate instrumentation and higher multi-site counts. The improved instrumentation tends to cost more, which is more than balanced by the COOP-er-site reduction of higher multi-site counts and lower test time/unit.

There is a point of diminishing returns on lower test time/unit. At low test time, handler limitations and factory operations begin to limit the actual output of the test process. The diminishing returns curve on traditional handling equipment begins to come into play at about 0.5 seconds unit test time. Test time reduction below that value will not provide significantly greater output. Improvements in handling technology and factory operational efficiency are required.

Biography

Dale Ohmart received his BS degree in Engineering Physics from the U. of Kansas and is a Distinguished Member of the Technical Staff at Texas Instruments; email d-ohmart@ti.com

When considered this way, it is clear that as Test Time/unit approaches 0, LotTestTime goes down. And as LotTestTime approaches 0, OEE also approaches 0.

Summary

There is upward pressure on test costs as IC customers demand higher quality. However, achieving higher quality simply through additional testing is a trap that increases cost and

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MEMS sensor testing challenges and requirements

By Andreas Bursian [Xcerra]

Industry 4.0 and the Internet of Things (IoT) may be the most utilized expressions currently being used to describe the change going on in the world. But Industry 4.0 and IoT are small components of a rapid global change that experts tend to call the 4th Industrial Revolution. This revolution will change all aspects of today's living, such as cash flow, data handling, job structure, and the political and social structures of society and the industrial production of goods.

Before answering the question of what the test requirements for MEMS sensor devices will be in the future, you have to answer the question of what our world will look like in the future. Such a discussion can give a rough indication on how the semiconductor industry has to evolve to keep pace with this revolution. Some aspects of MEMS sensors need to be examined first before you can start to think about how the requirements for MEMS sensors will change in the future.

If you take a look at today's market size, the annual volume of MEMS sensors can be roughly estimated to be 14 billion devices per year. Some forecasts have the annual growth rate estimated to be up to 20% until 2020. This would translate to 30 billion MEMS sensor devices. Scientists, however, expect, that the number of connected devices will go up to 1 trillion in 2025, which suggests an even larger growth rate than we are experiencing today. Whichever projections are proven out, they tell us that we will see a large trend in smaller and cheaper devices. This trend in turn will lead to advanced packaging and production technologies that will enable the industry to stay on trend.

Taking a look at sensor functions today, we see a large number of inertial sensors being used in mobile applications. The market is saturated and the main goal is to make these sensors cheaper and less power consuming. Nevertheless, there is a growth potential, because the mobile market is still growing and the lifetime of mobile devices is limited.

New trends for MEMS sensors can be observed in environmental sensing, such as barometric pressure, humidity, gas and sound. Sensor abilities and technology are driven by an army of engineers and obey

the rules of the 4th Industrial Revolution. New technologies may be disruptive, e.g., replacing existing technology in a very short period of time. More than that, there will be new requirements for testing, which cannot be achieved with test equipment that is available today. This disruptiveness may find its path into final test as well.

Quality has always been an important factor, but there is a trend to 0ppm test quality requirements that have only been seen so far in automotive applications. There are a couple of reasons for this. On the consumer side, there is the pure cost factor and the fact that one bad device on a board can only be detected on a system-level test. Once detected, the whole board will be scrapped, no repair is possible. For industrial, medical and automotive applications, quality is determined by safe operation. Many of the sensors are used to maintain lifesaving systems or systems for human interaction, where a fail function of a sensor can cause serious injuries to human beings.

The market for MEMS sensors is becoming more and more volatile and disruptive. Large global manufacturers in the sensor market acquire smaller companies, or mergers create new super companies with new portfolios. Even larger companies disappear or give up on MEMS product. Demanding product ramps require a fast time-to-market and the ability to ramp production from zero to ultra-high volumes, maintaining this volume for a couple of months, and then running the same cycle for different product with potential different test requirements. Suppliers that cannot keep track with the demanding market requirements may disappear in a very short period of time.

MEMS test equipment requirements

Keeping the above outlook on the MEMS sensor market in the 4th Industrial Revolution in mind, there are a few key factors that MEMS test equipment has to fulfill: 1) fast time-to-production; 2) highly parallel; and 3) modular, scalable, and easily convertible.

Fast time-to-production has become a key factor over the past several years with consumer applications having been the main driver. The product cycle for consumer

products is no longer than one year. It can be observed that the ramp-up and qualification period of a new MEMS sensor can be down to three months. A typical test setup for a MEMS device comprises a handler, tester, test program, a stimulus, a contactor solution, and last, but not least, the integration of everything. In a classical test environment, the integrated device manufacturer (IDM) or outsourced semiconductor assembly and test supplier (OSAT) would select all parts and drive the integration on site. There is a big risk that parts may not fit, or you may see interfacing problems due to the fact that every piece was built by a different supplier. This is unavoidable and you can account for it, if time margins are large enough. Besides timing issues, incompatibilities produce costs that usually do not appear in any planning.

A very convenient way for the customer to overcome such issues is to push the integration part of the job out to the vendor. If the vendor acts like the customer, there will be no big improvement on the whole process. If the vendor, however, can supply all parts from its own portfolio, the process becomes lean and safe. The vendor typically can build and integrate the whole system in its factory. Once the vendor produces all parts and sub-systems on its own, there is a seamless communication and knowledge of every little piece under the umbrella of one company. In such an environment, the customer's duty is limited to a requirement list. Pre-qualification can be done at the supplier and final qualification can be done on site. The customer saves cost in terms of work that has to be done in engineering and development and can focus on the core competency, which is production. Following this model, there is a huge cost saving potential in supply chain management and spare parts management.

Test parallelism is a key factor for volume production, ramp capability and cost-of-test. There are two very specific constraints for MEMS sensor testing: 1) The major fraction of these devices are being tested after saw and packaging. The silicon sensors are extremely sensitive to mechanical force, which can influence the calibration of the sensors. And 2) The test times are short, but the calibration

process usually lasts for seconds. Supplying the stimulus at a high accurate level may also significantly contribute to the process time.

The ability to test singulated devices in a highly parallel manner is the basis for running in high-volume with a reasonable amount of equipment. Test parallelism of 144 devices under test (DUTs) is widespread in the market, going up to by 256 DUTs. Such equipment can run millions of devices per month and enable ramp ups from engineering to production lost within days.

Systems that can test millions of devices per month used to be dedicated in the early days of the semiconductor industry. They were built to run one product for one life cycle, which had been acceptable because the depreciation period was shorter than the life cycle. This is no longer acceptable because MEMS test systems have to be able to test many different generations of sensor types. The nature of such systems is the ability to be converted easily. This goes beyond the simple change of some mechanical parts, but requires the ability of the base system to handle a large variety of different package types and sizes. Starting with classical molded devices, going to automotive packages, metal cap, and finally, chip-scale packaged devices, all package types have to be handled in a reliable way, guaranteeing the highest QA standards and fulfilling all relevant safety standards.

The discussion above aside, not only packages are changing. Stimuli change completely or develop over time. A good example is the environmental combo sensor that started with the requirement for obtaining a highly accurate temperature. The requirements for barometric pressure, relative humidity and gas tests were added step-by-step, now being able to provide only one port hole for four different kinds of sensing. So it can be seen that just as packaging technologies develop, so must test requirements (i.e., stimuli). Being modular means that handling and MEMS testing must be separated, so that you can keep the handler as a base system and exchange the MEMS module if required. The same is true for the tester: it has to be flexible to support all MEMS applications. Having this flexibility in place, it is possible to assign test cells to special production processes that can be limited to a short period of time and may change in test requirements. The modularity enables the customer to keep most of the equipment and adjust the test cell to the new requirements by simply using a new conversion kit and, if required, exchanging the MEMS test module. After an initial investment, the customer can react to

changing production requirements in terms of volume and MEMS stimulus by a resource management of existing production resources. Additional investment is limited to new or improved MEMS stimuli.

There is another aspect of scalability that is often not considered. Coming out of standard singulated test handling, loading of devices, testing and unloading of devices are part of one single handling system. This is the classic pick-and-place (P&P), or gravity handler. Taking a look at the large and rapidly changing number of device types, the pure handling process becomes challenging. Devices become smaller and smaller, not being able to be handled on a gravity system. Chip-scale devices finding their way into MEMS applications may even exclude P&P handlers as appropriate handling systems. Every jam that occurs in such a combined handling system will impact the load of the tester and the output of the system. Furthermore, long test times may cause the loading and unloading areas of these handlers to be idle. Therefore, it can be an advantage to separate loading and unloading from the test process. If, for example, the test process is very long, one loading and unloading unit can serve more than one test unit or vice versa.

Such an arrangement makes best use of the handling system units and enables the customer to add capacity to its fleet of handlers by adding the required units only, instead of adding systems, thereby delivering the entire loading and testing capability. Such a production environment can be optimized by planning and needs less investment once it is established.

The 4th Industrial Revolution will dramatically change our lives. The changes take place everywhere and will affect our private lives as well as our professional lives. It will make our lives better, it will increase the health

and living standard for billions of people, but it will also make our lives more volatile, demanding more flexibility from everybody.

The 4th Industrial Revolution with Industry 4.0 and IoT will also dramatically change the MEMS sensor testing requirements. A static production environment cannot fulfill the requirements of the MEMS sensor market. The production process will have to provide flexible answers to the marked requirements. Traditional test handling systems may not be able to provide the required solutions. New MEMS sensor handling systems need to provide good ramp capability, high test parallelism and modularity to be able to react flexibly to these market requirements. We have described a number of paths on how such test systems can look and which preconditions have to be fulfilled to be successful.

Biography

Andreas Bursian received his Masters degree in Electrical Engineering at the U. of Applied Sciences and Arts, Dortmund and is a Director of InStrip and InMEMS products at Xcerra. He started his career as a pioneer in SPICE and FEM simulation; email andreas.bursian@xcerra.com

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INDUSTRY EVENTS

**SEMICON®
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Packaging news from SEMICON Korea

By Steffen Kroehnert [NANIUM S.A]

The biggest event for the semiconductor industry in Korea — SEMICON Korea — celebrated its 30th anniversary this year. The event took place February 8-10, 2017, at COEX in Seoul. It featured approximately 600 exhibiting companies and 40,000 attendees along with keynote speeches, the SEMI Technology Symposium (STS), Test Forum, Market Seminar, Smart Manufacturing Forum, System LSI Forum, Metrology Inspection Forum, and the Supplier Search Program.

In his keynote address, Sungjoo Hong, Executive VP and Head of R&D at SK hynix, talked about the increasing difficulties of scaling, and the alternative technologies developed to manage the move from “happy scaling” to “hard scaling.” Luc Van den hove, President & CEO of imec, said, “Moore’s legacy will be the heartbeat of the semiconductor industry for many more decades, enabled by 3D constructions with nanowire as vertical interconnects inside the die, but also by heterogeneous integration and fan-out wafer-level packaging (FOWLP).” Jan Vardaman, Founder and CEO of TechSearch International, said in her Market Briefing presentation (“The Future of Fan-Out Wafer-Level Packaging”), that by removing the substrate from the package, we are facing a new level of chip-package interaction (CPI) challenges, and need to factor this in for next technology nodes.

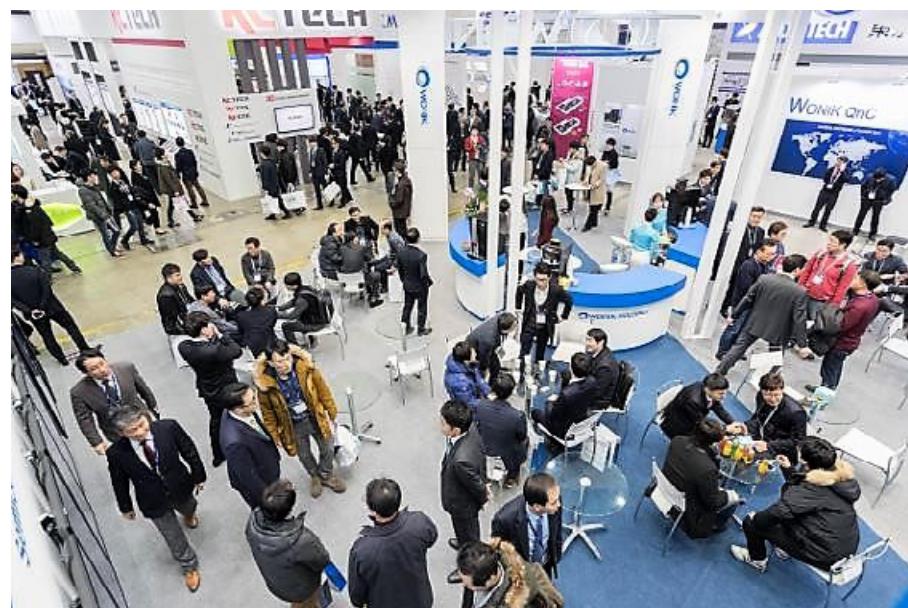
Session 6 of the STS – with its theme “Electropackage System and Interconnect Product” – has been the most interesting with respect to packaging. The organizing committee of that session noted that, “As customers demand new electronic devices and performance enhancement, high-tech technology is required for package processes, which had been treated as simple manufacturing in the past. In the meantime, advanced wafer-level packaging is attracting attention as a future technology. This is due to its high cost competitiveness compared

to existing packaging processes and the ability to package system-in-packages (SIPs).” As the first invited speaker of this session (“Where Is the Destination of the Packaging Technology”), Dr. Choon Heung Lee, Global CTO of Lam

Research, said that in terms of FOWLP, it is all about manufacturing capacity. The technology is available and mature, and he observed that embedded multi-chip fan-out modules with optimized system design will be the future.



Luc Van den hove, President & CEO of imec



SEMICON Korea Exposition Hall



22nd Annual SMTA Pan Pacific Microelectronics Symposium

By Tanya Martin [\[SMTA\]](#)

The 2017 SMTA Pan Pacific Symposium (held at Sheraton Kauai Resort in Koloa, HI, USA) included over 50 presentations on new technology trends in the electronics manufacturing industry. The intimate setting of the symposium provided ample opportunity for attendees to make quality professional connections during a variety of social activities such as the golf tournament, welcome reception, and private luau.

The four-day event kicked off Monday, February 6, 2017 with a Plenary Session that included insightful

presentations by three respected experts. Dwight Howard (Delphi) presented Rapid Electronics Design with Advanced Tools and Optimized Workflow. Matthew Hudes (bdllBiologx) spoke on the topic of Fostering Innovation in Digital Health. Horatio Quinones, PhD, (FDCS) presented Intelligent Manufacturing Automation.

The technical sessions and panel focused on topics including Materials & Reliability, Nanotechnology, Design & Manufacturing Strategies, Packaging Solutions, Advanced Packaging, Roadmaps, Test, and Embedding &

Fan-Out Packaging. An expert panel discussion on Ionic Test Methods closed out the day on Tuesday. Chuck Bauer, PhD, (TechLead Corp.) moderated the panel featuring technical experts from Celestica Inc., Foresite Inc., Indium Corporation, and KYZEN Corporation.

The program featured two keynote speakers, Kyung Paik, PhD (KAIST) and Thomas Brunschwiler, PhD, (IBM Research – Zurich). On Tuesday, February 7, Dr. Paik gave an interesting keynote presentation on “Fabric-Based Fine Pitch Interconnect Technology Using Anisotropic Conductive Films (ACFs).”



14th International Wafer-Level Packaging Conference www.iwlpc.com

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- Advanced Integrated Systems and Devices
- Advanced Wafer-Level Manufacturing and Test

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Contact Jenny Ng at jenny@smta.org or 952-920-7682



Kyung Paik, PhD (KAIST)

The presentation outlined a major technological advancement in the area of flexible wearable electronics. Dr. Brunschwiler shared his expertise in



Steering Committee and Session Chairs

3D heterogeneous integration in his Wednesday morning keynote presentation on "Multi-Functional Packaging Technologies Supporting Performance and Efficiency Scaling Beyond Exa-Scale Systems." He touched on nanotech applications for assembly, orthogonal scaling and neuromorphic computing in achieving true artificial intelligence and big data handling capabilities for real world applications.

The 2018 symposium will be held February 5-8 at the Hapuna Beach Prince Resort on the Big Island of Hawaii. Abstracts can be submitted online at www.smta.org/panpac/call_for_papers.cfm. For more information on the Pan Pacific Microelectronics Symposium, contact Tanya Martin at 952-920-7682 or tanya@smta.org.



ECTC preview

By Mark Poliks *[Binghamton University]*

IEEE's 67th Electronic Components and Technology Conference (ECTC) will be held at the Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida, from May 30 to June 2, 2017. This premier international annual conference, sponsored by the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society, brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1,400 people attended the 66th ECTC in Las Vegas, Nevada, in May 2016.

At this year's ECTC, more than 360 technical papers are scheduled to be presented in 36 oral sessions and five interactive presentation sessions. The oral sessions will feature selected papers on



67th ECTC Location: Walt Disney World Swan and Dolphin Resort at Lake Buena Vista, Florida.

key topics such as flip-chip packaging, 3D/TSV technologies, wafer-level packaging, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, and materials and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion

and interaction with authors about their work. Authors from 22 countries are expected to be presenters.

The ECTC will also feature panel and special sessions with industry experts covering a number of important and



67th ECTC ExComm (from left to right): Christopher Bower, Assistant Program Chair, X-Celeprint Inc.; Mark Poliks, Program Chair, Binghamton University; Henning Braunisch, General Chair, Intel Corporation; Sam Karikalan, Vice-General Chair, Broadcom Limited.

emerging topic areas. On Tuesday, May 30 at 10:00AM, Vikas Gupta and Pradeep



Materials and Process Subcommittee: one of ten subcommittees at the ECTC Dallas Abstract Selection meeting.

Lall will chair a session on “Material and Package Reliability Needs/Challenges for Harsh Environments.” Then at 2:00PM, Bing Dang will chair a panel session on “Flexible Hybrid Electronics – Electronics Outside the Box,” where a panel of experts will discuss how innovation in device integration and packaging are adapted to the shape of the human body and vehicles. Tuesday evening will also include the ECTC Panel Session at 7:30PM on “Panel Fan-Out Manufacturing: Why, When, and How?” chaired by CPMT President Jean Trewella and Young Gon Kim. The ECTC Luncheon Keynote Speaker on Wednesday will be Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation. His talk is entitled “Advanced Packaging Opportunities and Challenges.”

The CPMT Women’s Panel chaired by Kitty Pearsall on Wednesday, May 31, at 6:30PM will discuss “Emotional Intelligence (EI) – Link to Successful Leadership.” Also on Wednesday at 7:30PM, Luke England will chair the ECTC Plenary Session entitled “Packaging for Autonomous Vehicle Electronics;” the session will feature key technologists sharing their views on the electronics challenges needed to support widespread implementation of driver-less vehicles on the road. On Thursday, June 1 at 8:00PM, the CPMT Seminar “3D Printing Tools, Technologies and Applications,” will be moderated by Venkatesh Sundaram and Yasumitsu Orii.

Supplementing the technical program, ECTC also offers several Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference this year, the 67th ECTC will offer 18 PDCs, organized by the PDC Committee chaired

by Kitty Pearsall. The PDCs will take place on Tuesday, May 30th, and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by more than 100 leading companies in the electronic components, materials,

packaging and services fields. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions. Don’t miss out on the industry’s premier event!

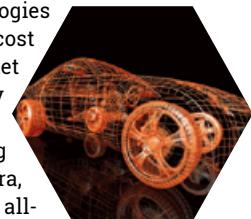
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PACKAGING RESEARCH CENTER GEORGIA TECH LAUNCHES INDUSTRY CONSORTIUM IN NEW ERA OF SELF-DRIVING AND ELECTRIC CARS

NEW ERA OF SELF-DRIVING AND ELECTRIC CARS

New Era of Self-driving and Electric (NESE) car technologies is expected to account for about a third of the total cost of each car, about \$10,000, potentially creating a market of \$1T within a decade. Such an emerging industry requires many new IC, package and 3D architectures in computing and communications for self-driving sensor technologies such as RADAR, LiDAR and camera, and high-power and high-temperature technologies for all-electric cars.



The Southeast USA, with Atlanta as a global hub for European, Japanese, Korean and US car and Tier 1 and 2 companies, presents Georgia Tech, as the top-tier university in this region, with a unique opportunity to contribute to the NESE. The challenges in addressing these needs are more complex than any electronic product to date and include both hardware and software.

Georgia Tech is launching the NESE industry consortium with focus on:

- » Device and package technologies leading to highly integrated, miniaturized, low cost and highly-reliable autonomous and all-electric automotive systems
- » Partnership with Tier 1 and Tier 2 global supply chain companies for R&D in integrated components and with car makers to develop road maps, supply chain management and standards
- » Education of large number of highly-interdisciplinary engineers who are well prepared for the NESE industry.

Georgia Tech has world-class faculty expertise and R&D and prototype infrastructure for the most leading-edge:

- » Devices such as SiGe, GaN, photonic, and image sensors
- » Highly integrated, high-performance, high-temperature glass-based packaging; 2.5D and 3D glass interposers; 5G and 3D glass photonics; high-power and high-temperature materials; cameras, RADAR and LiDAR.

For more information, contact Center Director, rao.tummala@ece.gatech.edu

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INDUSTRY NEWS



Tessera Holding Corporation announced name change to Xperi Corporation

Tessera Holding Corporation (Nasdaq: TSRA) announced that it changed its name to Xperi Corporation ("Xperi") and its Nasdaq ticker symbol to XPER, effective February 23. The change also included a new corporate logo and brand platform to reflect the company's expanded capabilities, continued technological innovation and refined vision. Xperi and its wholly owned subsidiaries, DTS, FotoNation, Invensas and Tessera, will continue to create and deliver audio and broadcast solutions, computational imaging technology, semiconductor packaging, and intellectual property licensing.

"Changing our name to Xperi is an incredible moment in our history," said Tom Lacey, CEO of Tessera Holding Corporation. "Xperi represents the combination of DTS, FotoNation, Invensas and Tessera - world-class companies dedicated to creating solutions that enable extraordinary experiences for people around the world. Our new logo and brand identity convey the unlimited possibilities of what our team of approximately 700 employees can create to truly impact the human experience. We are constantly inspired by how people use our technologies in their lives, and that drives us to continue generating ideas and innovation. We cannot wait to show the world what's next."

Since 1993, DTS has been dedicated to making the world sound better. Through its audio solutions for mobile devices, home theater systems, cinema, automotive and beyond, DTS provides immersive and engaging audio experiences to listeners everywhere.

FotoNation, founded in 1997, provides computational imaging and computer vision solutions. Its technologies and solutions enhance the digital imaging capabilities in billions of smartphones, digital cameras, drones, activity cameras, tablets, surveillance systems, access control systems and more.

Since its founding in 2011, Invensas has been a provider of advanced semiconductor packaging and interconnect technologies that enable the next-generation of electronics products to be smaller, faster,

consume less power and deliver higher levels of functionality.

Founded in 1990, Tessera originally focused on the research and development of semiconductor packaging technology and has been a leader in innovating and licensing technology and intellectual property. Tessera's customers include many of the world's leading semiconductor, smartphone and digital imaging manufacturers.

smiths interconnect bringing technology to life

Smiths Interconnect launches brand transition to simplify customer access to technologies

Smiths Interconnect, a division of Smiths Group plc, recently announced it is unifying its technology brands of EMC Technology, Hypertac, IDI, Lorch, Millitech, RF Labs, Sabritec, TECOM, and TRAK under the single brand identity of "Smiths Interconnect."

According to the company, the brand transition supports a recent strategic reorganization focused on creating a more agile structure that can better anticipate and respond to customers' evolving needs. Individually, the technology brands represent state-of-the-art solutions across the connectors, microwave components and microwave subsystems markets. Providing a strong umbrella brand that supports the breadth of these products and technologies will make Smiths Interconnect a more comprehensive solutions provider, improving the customer experience by streamlining access and interactions across multiple applications.

"Over time, interactions among our brands have increased across many of our markets," said Roland Carter, President of Smiths Interconnect. "Aligning all this activity under the Smiths Interconnect name will make us a more streamlined partner, enhancing our customers' access to the combined strength of our products, expertise and application knowledge."

The individual technology brands will continue to be visible in association with the Smiths Interconnect brand during the transition period.



GE Ventures and Samsung Electro-Mechanics (SEMCO) recently announced a multi-year, worldwide patent license agreement

With this partnership, SEMCO will license GE's microelectronics packaging patent portfolio, covering the fabrication of substrates embedded with electronic circuits.

Developed by GE Global Research and Imbera Electronics Oy (now GE Embedded Electronics Oy) as part of a major GE focus in power electronics research over the last decade, the patent portfolio is of particular value for high-performance communication and mobility products.

"GE is extremely pleased that SEMCO has recognized the significance of GE's IP in this space," said Lawrence Davis, VP and MicroElectronics Packaging Program Director at GE Ventures. "As the demand for increased power efficiency and higher performance in mobility products continues to expand, GE is positioned to be a strong partner for embedded electronics technology in the power and consumer electronics space. GE Ventures accelerates innovation and growth for partners by providing access to GE technologies through licensing and joint development partnerships. This advanced microelectronics packaging technology is being licensed to leading global manufacturing partners to provide advanced solutions to businesses worldwide."



Amkor Technology to acquire NANIUM S.A.

Amkor Technology, Inc. (Nasdaq: AMKR) and NANIUM S.A. have announced that they have entered into a definitive agreement for Amkor to acquire NANIUM. Terms of the transaction were not disclosed at the time of the announcement.

According to Amkor, the acquisition of NANIUM will strengthen its position in the fast growing market of

wafer-level packaging for smartphones, tablets and other applications. NANUM has developed a high-yielding, reliable WLFO technology, and has successfully ramped that technology to high-volume production. NANUM has shipped nearly one billion WLFO packages to date utilizing a state-of-the-art 300mm wafer-level packaging (WLP) production line.

"This strategic acquisition will enhance Amkor's position as one of the leading providers of WLP and WLFO packaging solutions," said Steve Kelley, Amkor's President and Chief Executive Officer. "Building on NANUM's proven technologies, we can expand the manufacturing scale and broaden the customer base for this technology."

"The Amkor transaction is a great fit for us and provides NANUM and its employees with a strong platform for future growth," said Armando Tavares, President of NANUM's Executive Board. "Amkor's technology leadership, substantial resources and global presence coupled with NANUM's best-in-class WLFO packaging solutions will accelerate global acceptance and growth of this technology worldwide."

NANUM is based in Porto, Portugal, employs approximately 550 people and had annual sales of approximately \$40 million for its fiscal year that ended September 30, 2016. The transaction is expected to close in the first quarter of 2017, subject to customary closing conditions and regulatory approvals.



InvenSense and GLOBALFOUNDRIES collaborate on ultrasonic fingerprint imaging technology

InvenSense, Inc. (NYSE: INVN), and GLOBALFOUNDRIES have announced their collaboration on an ultrasonic fingerprint imaging technology for InvenSense UltraPrint Ultrasound Fingerprint Touch Sensor Solution. InvenSense and GF are enabling, for the first time, commercial manufacturing of aluminum nitride-

based piezoelectric Micromachined Ultrasonic Transducers (pMUT). As a result of the close technological collaboration between InvenSense and GF, InvenSense's CMOS-MEMS Platform can now be extended to pMUT devices and enable a biometric authentication solution for mobile and IoT products.

Mobile OEMs are looking for highly durable, button-free solutions that require fingerprint sensors to be placed behind the cover glass or under metal on the back of the phone. Capacitive sensors, incapable of sensing through metal, can only sense through roughly 0.3mm of glass, which creates durability concerns. InvenSense's UltraPrint technology enables the use of thicker glass or metal materials without compromising biometric authentication performance. Moreover, the technology enhances fingerprint imaging, enabling the reader to scan even when the user's skin contains common contaminants such as oils, lotion, or perspiration. These critical factors combined with GF's aluminum-nitride-based manufacturing technology ensure consistent quality for higher-performance devices and can be extended to a secure identification for smartphones, home automation, payment or health-related interactions with wearables.

"We are pleased to have collaborated closely with GF on the proprietary InvenSense CMOS-MEMS platform (ICMP)," said Mo Maghsoudnia, VP of Technology and Worldwide Manufacturing at InvenSense. "This close technology collaboration has enabled us to advance the manufacturing of ultrasonic imaging technology, resulting in production of our fingerprint authentication solution for a myriad of applications. We look forward to expanding our collaboration into multiple pMUT devices and the delivery of best-in-class products to our customers."

"InvenSense's entry into pMUT provides testimony to our differentiated capabilities on aluminum nitride-based piezoelectric MEMS fabrication technology," said Gregg Bartlett, SVP, CMOS Business

Unit of GF. "This is particularly notable as we broaden the relationship to now include InvenSense's ultrasonic fingerprint and other process technologies."



imec and EVG demonstrate for the first time 1.8µm pitch overlay accuracy for wafer bonding

At the 2017 European 3D Summit in Grenoble (France, Jan 23-25) imec and EV Group (EVG) announced an extension to their collaboration, achieving excellent wafer-to-wafer overlay accuracy results in both hybrid bonding and dielectric bonding. Expanding this collaboration, EVG will become a partner in imec's 3D integration program through a joint development agreement to further improve overlay accuracy in wafer-to-wafer bonding.

Wafer-to-wafer bonding is a promising technique for enabling high-density integration of future ICs through three-dimensional (3D) integration. This is achieved by aligning top and bottom wafers that are then bonded, thereby creating a stacked IC. An important advantage is that wafers/ICs with different technologies can be stacked, e.g., memory and processor ICs.

The companies provided additional background information about their work with the news release. Many of the alignment techniques and bonding methods for 3D integration have evolved from microelectromechanical system (MEMS) fabrication methods. The fundamental difference between MEMS and 3D integration is that the alignment or overlay accuracy has to be improved by 5–10 times. Accurate overlay is needed to align the bonding pads of the stacked wafers and it is essential to achieving a high yield with wafer-to-wafer bonding.

imec and EVG released results they achieved with respect to overlay accuracy. First, the hybrid (via-middle) wafer-to-wafer bonding technique was improved by using EVG's bonding system that resulted in a high-yield and a 1.8µm pitch (see **Figure 1**), which is significantly better compared to recently published results at

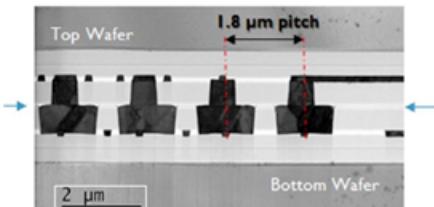


Figure 1: Results of the hybrid (via-middle) wafer-to-wafer bonding achieved by EVG and imec's collaboration achieving a 1.8μm pitch.

recognized conferences such as ECTC and 3DIC reporting 3.6μm pad size.

Second, the dielectric (via-last) wafer-to-wafer bonding technique was tackled by the collaborators. This technique requires extremely good overlay accuracy to align the copper pads from both wafers, which are then contacted by through-silicon vias (TSVs). In this case, 300nm overlay across the wafer was achieved.

"By joining forces, we achieved these excellent results on overlay accuracy," explained Eric Beyne, Fellow at imec. "We are excited that we can expand our collaboration with EVG with a JDP and the installation of EVG's GEMINI FB XT wafer bonder in our cleanroom. The GEMINI FB XT has the potential to further reduce the wafer-to-wafer overlay errors and therefore allow for the development of sub-micron wafer-to-wafer interconnects technologies."

"Further improving the overlay accuracy for wafer-to-wafer bonding into the sub-200nm range requires optimization of the interaction between the wafer bonding tool and processes as well as pre-and post-processing and the wafer material," noted Markus Wimplinger, Corporate Technology Development & IP Director at EVG. "We are excited to partner with imec in an effort to advance overlay accuracies for wafer-to-wafer bonding to meet the needs of future 3D IC designs that rely on high density interconnects"

Imec's 3D integration program explores technology options to define innovative solutions for cost-effective realization of 3D interconnect with TSVs. Imec's 3D integration processes are completely executed on 300mm. Imec also explores 3D design to propose methodologies for critical design issues, enabling effective use of 3D interconnection at the system level.



CORWIL Technology invests in portable clean environment for wafer sort

To satisfy demand for ultra-clean environments for wafer sort, CORWIL Technology (CORWIL) has added a Portable Clean Environment for wafer sort that is good to Class 1000. This is a one-stop solution from wafer sort, die prep, assembly, package test and reliability that provides the ability to understand how different pieces of the backend process affect each other in terms of yield.



Joe Foerstel, VP of Test for CORWIL said, "Customers have found that wafer sort in a very clean environment improves yield, especially when using certain RF probe technologies or probing devices with sensitive surface structures, particularly for our customers in the communications and medical industries."

"We have seen dramatic improvement of yields at Second Optical when customer's wafers arrive from a cleaner environment, especially when back grind is one of the steps in the process," added Jonny Corrao, CORWIL's Director of Die Prep.

smartphone manufacturers and designers effectively manage heat dissipation in their phones. Honeywell pointed out that the worldwide smartphone market is expected to reach more than 1.9 billion units by 2020, according to a study from IDC Research. In addition, data needs are growing at unprecedented rates. To meet this challenge, the smartphone industry is leveraging technology that enables phones to provide optimal processing performance without overheating.

Honeywell's TIM technology is based on phase change materials (PCMs). The technology transfers thermal energy from phone chips to a heat sink or spreader, where it is dissipated into the surrounding environment. This functionality keeps the chips cool, so the phone can perform reliably even during the most data-intense processes or during heat spikes. According to the company, Honeywell's solution is available worldwide and is already being used by some of the largest smartphone makers to upgrade the thermal designs of its latest phone models.

"Honeywell's innovative TIM technology provides customers with the ideal solution to optimize their phones' performances," said Olivier Biebuyck, VP and GM of Honeywell Electronic Materials. "As demand for smartphones grows around the world, these breakthrough designs help provide optimal user experience throughout the entire lifecycle of their devices."

The company's PCM series of thermal management materials are based on sophisticated phase-change chemistry and advanced filler technology that was developed specifically for high-performing electronic devices. TIM products are designed to optimize thermal impedance across the entire thermal path, providing an end-to-end solution for best-in-class thermal performance. The PCM design can be customized to fit diverse product applications and end uses.

Honeywell | Electronic Materials

Honeywell technology: keeping smartphones cool

Honeywell (NYSE: HON) has announced the availability of a thermal interface materials (TIM) solution to help

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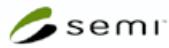
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Glass-based SiP solutions for high-performance/high-frequency RF filters

By Jeb Flemming, Roger Cook, Tim Mezel, Kyle McWethy [3D Glass Solutions]

High-Q RF filters in a small cost-effective form factor are a key enabler for today's mobile electronic devices. For applications above 3GHz, traditional RF filter materials such as piezoelectrics and ceramics fail to provide the necessary performance metrics to enable compact, low-power devices. Therefore, new materials are being pursued to meet the market demand for the production of smaller high-performance integrated passive device (IPD) RF filters including bandpass filters, diplexers, and duplexers among others.

Due to the ever-increasing demand for wireless data access and mobile devices performance, the FCC has recently designated three new frequency bands for 5G applications: 4.9-5.8GHz, 27.5-29.5GHz, and 37-40GHz [1]. At these frequencies, acceptable material choices are reduced further, and by default, impose stricter requirements on manufacturing options to meet the required performance.

Glass has been touted as a very good substrate for RF applications including 5G frequencies by a number of authors, including multiple articles from the Georgia Tech Packaging Research Center [2-5], which has done extensive research on glass substrates for electronic applications. The main attributes of using glass for an RF substrate are: 1) better material properties at RF frequencies; 2) decreased surface roughness for fine line redistributions; and 3) ability to manufacture in large formats (wafer and panel) to meet industry cost targets.

Photosensitive glass-ceramic (PSG) materials are a class of materials that offers all of the benefits of glass but have some additional beneficial attributes that regular glasses do not offer. These benefits include: 1) the ability to transfer patterns directly to glass with a standard photolithography step; 2) the ability to create small, precise, features at high densities; and 3) the opportunity to integrate IPDs such as high-Q inductors and capacitors into a single substrate.

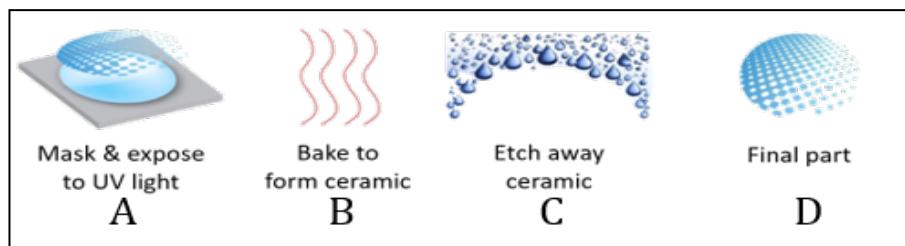


Figure 1: APEX® glass processing steps.

Furthermore, these IPDs can also be directly integrated into higher functioning RF systems-in-package (SiP) devices, leading to smaller packaging, lower power consumption, and increased bandwidth.

In this article we will present an overview of PSGs for the electronics packaging industry with a focus on the integration of integrated passive devices (IPDs) for the RF industry. We will present on our recent advances in the monolithic integration of high-Q inductors and capacitors and several IPDs that have target performance up to 20GHz. We will present both modeling and measurement data for several devices.

What are photosensitive glasses?

Photosensitive glass ceramics (PSGs) were first identified and explored in the 1950s and were initially discovered by Dr. Stanley Donald Stookey at Corning. Corning first commercialized photosensitive glass ceramic products under the trade name CorningWare in the 1950s. The initial products focused on high-temperature stability materials for household cooking and included dishes and stovetops.

Photosensitive glasses belong to the lithium-aluminum-silicate family [6] with impurities of metal oxides that greatly contribute to the photostructurability of these glasses. This class of materials is capable of existing in both an amorphous glassy state and a crystallized ceramic state (crystalline-phase lithium metasilicate) within the same substrate. PSGs are characterized by their ability to selectively pattern ceramic features in the bulk glassy material through lithography.

In recent years, PSGs, with their unique 3D structuring ability, have been explored for a variety of technical applications [7] including microfluidics, optoelectronics, and more recently, led by 3D Glass Solutions, RF IPDs and systems-in-packages (SiPs). The primary PSG that we use is APEX® Glass.

Process approach

The manufacturing of 3D structures in PSGs is accomplished through a patented 3-step manufacturing process. The first step in processing an IPD wafer is to expose the glass using a lithography mask to create through-glass features (e.g., through-glass vias (TGVs) and through-glass capacitor plates). This is accomplished using a chrome-on-glass mask placed directly onto the glass wafer, without photoresist, and exposed to 310nm UV light (Figure 1a). During this step, photo-sensitizers in the glass undergo a redox exchange initiated by the UV light.

In the second step, the glass is baked above its glass transition temperature (Figure 1b), where mobile ions surround the exposed regions, converting the previously exposed glass into a nano-crystalline ceramic phase. After the bake step, the exposed pattern has been converted into ceramic, going all the way through the glass wafer. Unexposed regions of the wafer remain in the original glassy state.

In the third processing step, the wafer is etched in a diluted acid (Figure 1c), preferentially etching the

ceramic regions 60 times faster than the surrounding glass regions. In this manner, the through-glass ceramic patterns can be completely removed leaving a glass wafer with the desired through-wafer pattern of TGVs and through-glass capacitor plates. Using this same process, a wide variety of additional features not commonly associated with glass processing such as posts, wells, trenches, blind vias, and air bridges may be produced.

The fourth step is to fill the through features with copper. There are a number of possible methods for achieving this depending on the dimensions and aspect ratio of the structures. 3D Glass Solutions uses a couple of methods currently including a proprietary metal filling approach that

Young's Modulus	81GPa
Electrical Resistivity	$10^{12}\Omega$
Coefficient of Thermal Expansion	10ppm/K
Loss Tangent (3.3GHz)	0.0086
Loss Tangent (10.2GHz)	0.0106
Dielectric Constant (3.3GHz)	6.58
Dielectric Constant (10.2GHz)	6.575

Table 1: Summary of APEX® Glass' relevant RF material constants.

completely fills the through-structures with copper.

The final process steps are similar to semiconductor processing for patterning conductive layers on one or both sides of the glass wafer. Utilizing the process flow described above

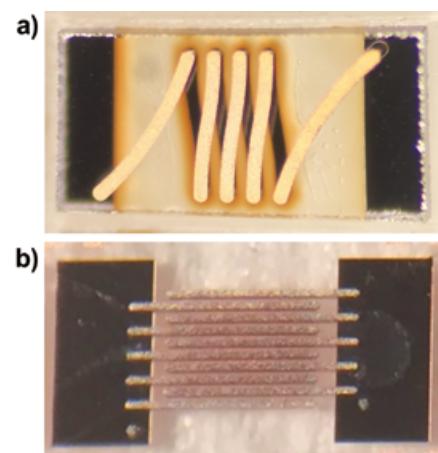


Figure 2: A = high-Q inductor; B = parallel-plate in-glass capacitor.

allows us to create inductors, capacitors and IPDs in a wide variety of custom designs with values targeted at the RF market. This gives microwave and RF designers a very flexible toolkit to utilize in creating products to meet their unique requirements. **Table 1** outlines several physical and electrical material constants. Further processing details have been published by independent researchers [8].

The building blocks

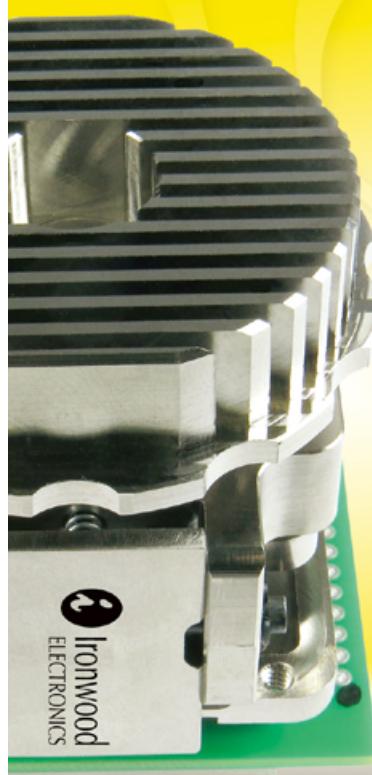
The basic building blocks of IPD filters (e.g., band pass filters) are inductors and capacitors. **Figure 2** shows some examples of individual components that are representative of the 3D structures that are possible to build with the PSG process outlined above.

Figure 2a shows a 3-turn high-Q inductor. This particular design is called an in-glass stitched inductor. It utilizes

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copper traces on the top and bottom of the wafer connected with copper-filled TGVs to build the entire device. High-Q inductor values currently range from 0.5–30nH. High-Q capacitors are produced by etching openings through the glass in the shape of the parallel plates and then filling these with copper. Figure 2b shows an example of a parallel-plate in-glass capacitor. Capacitance values currently range from 0.5–10pF.

Simulation and testing approach

Initial component designs, as well as more complex filter designs, are developed using a methodical geometric incrementation of key features. This process enables fine control over the final part geometry and accommodates some of the more unique features that can be produced with the manufacturing process. All designs were developed and simulated using National Instruments AWR software.

Component measurements are measured using a 0.1-40GHz test setup. A 0-67GHz 2-port PNA-X is used in conjunction with a pair of matched length cables and 250 μ m pitch probes. The measurement reference plane is located at the end of the probes for all of the data outlined in this paper. The device under test (DUT) therefore includes the probe launch structure that converts the probe pads to the transmission line of the filter. Due to the length and quality of the cables, measurements have a reduced dynamic range between 10-30GHz resulting in a slight increase of measurement noise between 10-30GHz most evident on S11 and S22 measurements.

Device testing

By putting the building blocks described above together in the proper order, we can create a wide variety of filter designs including low-pass, high-pass, band-pass, baluns, bias tees, diplexers and duplexers. All of the devices come in a small footprint and a small z-height (0.3 mm). Furthermore, all of these products are intended to be flip-chip bonded to save additional package space and improve performance by the elimination of wire bonding.

Example RF IPD filter #1: 1GHz diplexer. The first proof-of-concept

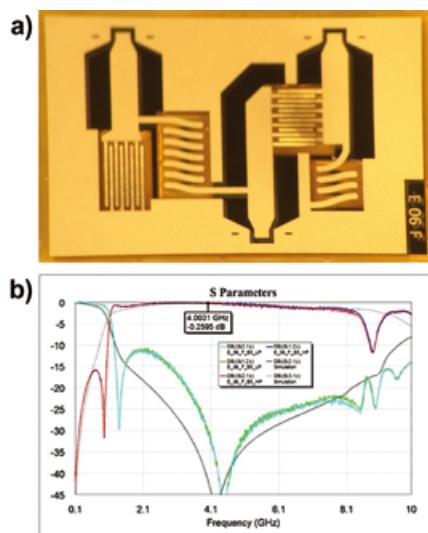


Figure 3: a) 1GHz diplexer IPD filter; b) Measured S-parameter data (solid lines) overlaid on top of simulation data (dotted line).

example of an IPD designed with a combination of the building blocks shown above is a 1GHz diplexer as shown in **Figure 3a**. The footprint of this device is 3.8 x 5.8mm. It is made up of two high-Q stitched inductors and two high-Q parallel-plate in-glass capacitors that utilize the full thickness of the glass substrate. The individual components are connected with metal traces on both sides of the glass substrate. This particular design was intended for testing purposes and has 3 G-S-G (ground-signal-ground) pads for isolating the individual S-parameters using two separate 2-port measurements. This initial device focused on the baseline demonstration that software simulations with NI's AWR software matched reasonably close to the measured device performance. Although this device was not optimized for its performance, it closely matched the simulated design (see **Figure 3b**) and produced insertion losses better than that of the simulation with a demonstrated insertion loss at 4GHz of -0.26dB. The values for the 1GHz diplexer design are $L_1 = 7.0\text{nH}$, $L_2 = 3.4\text{nH}$, $C_1 = 3.2\text{pF}$ and $C_2 = 3.0\text{pF}$.

**Example RF IPD filter #2:
5-9GHz GHZ bandpass filter.**
Beyond the initial proof-of-concept production of an integrated passive device shown above, a 5-9GHz bandpass lumped element filter is

shown in **Figure 4a**. The footprint of this device is 3.8 x 2.7mm, with a thickness of 300 microns. This filter is made up of two high-Q surface inductors, two shunt-to-ground vias, and capacitively-coupled center plates that utilize two in-glass parallel plates that are the full thickness of the glass to create a high-density capacitive coupling between the two sections of the filter. This filter shows a smooth response with a high correlation to simulation with improved insertion loss in the second band pass. **Figure**

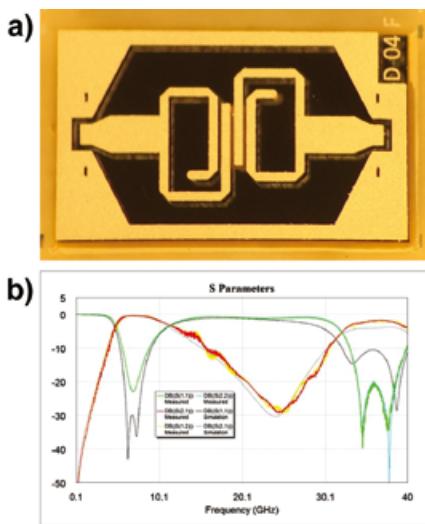


Figure 4: a) 5-9GHz bandpass IPD filter; and b) Measured S-parameter data (solid lines) overlaid on top of simulation data (dotted line).

4b shows the measured vs. modeled S-parameters of the 5-9GHz diplexer, showing a 0.4dB insertion loss at 8GHz.

Example RF IPD filter #3: 20GHz GHz bandpass filter. Finally, a picture of a 20GHz bandpass filter, along with the S-parameter data is shown in **Figures 5a** and **5b**. The footprint of this device is 3.8 x 5.8mm, with a thickness of 300 microns. This filter design also utilizes a lumped element approach to electrically couple the individual passive devices. This particular design shows great roll off before and after the pass band with less insertion loss and more reflection in the pass band than the simulation.

Reliability testing

We have started collecting reliability data on multiple RF filter designs. Complete reliability testing

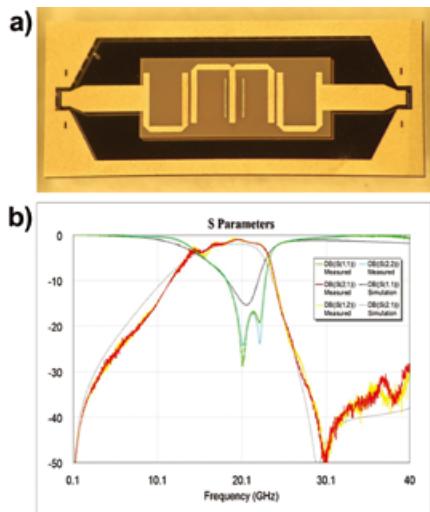


Figure 5: a) A 20GHz band pass IPD filter; and b) Measured S-parameter data (solid lines) overlaid on top of simulation data (dotted line).

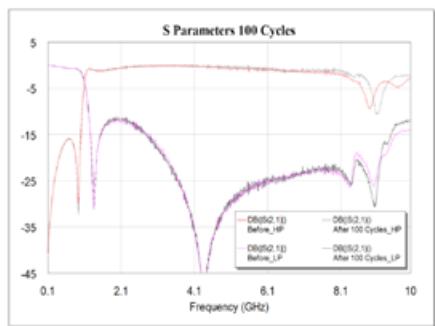


Figure 6: 1 GHz diplexer S-parameters before and after 100 thermal cycles.

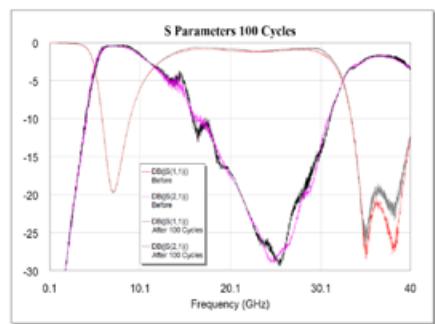


Figure 7: 5-9GHz band-pass filter S-parameters before and after 100 thermal cycles.

is ongoing, but early devices have been thermal-cycled over 1,000 times without mechanical failure. Furthermore, RF testing of pre- and post- thermocycled IPD filters is shown in **Figure 6**. Here S-parameter data for the 1GHz diplexer after 100 temperature cycles from -40°C to +125°C is shown. There is excellent correlation between the pre- and post-

thermocycled test data, with less than a 0.05dB difference.

Figure 7 shows the before and after S-parameter data for the 5-9GHz bandpass filter after 100 temperature cycles from -40°C to +125°C. Again, there is very good correlation between the curves showing less than 0.1dB change in the device performance due to the temperature cycling. Temperature cycling of these parts to a minimum of 1000 cycles is ongoing.

Summary

RF solutions for 3GHz or greater are in high demand, especially solutions that have a small footprint and z-height. Legacy substrate materials are unable to meet the size and performance requirements at these higher frequencies requiring the need for alternative substrates. Photosensitive glasses enable advanced unique RF architectures over traditional glasses and have been shown to produce extremely low-loss RF IPD filters.

The presented glass ceramic and processing approach has been shown to be extremely flexible in its ability to produce a wide variety of RF designs, targeted at different frequencies on the exact same process. This platform gives RF engineers a very flexible toolkit for creating designs to meet their precise needs in a small footprint device today and tomorrow. Because all filter designs are built with the same manufacturing process, this opens up the possibility of integrating multiple filters and/or other RF devices on the same chip, eliminating the need for expensive processing to populate boards with multiple discrete components.

Insertion loss has been measured at extremely low values. Overall filter performances are quite competitive compared to other published results. These products demonstrate a capability that has not been possible to date in this compact size.

References

1. <https://www.fcc.gov/document/fcc-adopts-rules-facilitate-next-generation-wireless-technologies>, July 14th, 2016, FCC.com
2. A. Polyakov, P.M. Mendes, S.M. Sinaga, M. Bartek, B. Rejaei,

J.H. Correia, J.N. Burghartz, "Processability and electrical characteristics of glass substrates for RF wafer-level chip-scale packages," 2003 ECTC Conf.

3. V. Sridharan, S. Min, V. Sundaram, V. Sukumaran, S. Hwang, H. Chan, et al., "Design and fabrication of bandpass filters in glass interposers with through-package vias (TPV)," 2010 ECTC Conf.
4. A.B. Shorey, R. Lu, "Progress and application of through-glass via (TGV) technology," 2016 iMAPS Conf.
5. J. Flemming, R. Cook, S. Sibbett, C.F. Schmitt, K. Dunn, J. Gouker, "Cost-effective 3D glass microfabrication for advanced RF packages," Microwave Jour., Apr., 2014.
6. T. Dietrich, W. Ehrfeld, M. Lacher, M. Kramer, B. Speit (1996), "Microelectron Eng." 30:497.
7. <https://www.crcpress.com/Photosensitive-Glass-and-Glass-Ceramics/Borrelli/p/book/9781498745697>
8. K. Tantawi, J. Oates, R. Kamali-Sarvestani, N. Bergquist, J.D. Williams, "Processing of photosensitive APEX™ glass structures with smooth and transparent sidewalls," Jour. of Micromechanical Microengineering 21 (2011).

Biographies

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Kyle McWethy is finishing a BS in Mechanical Engineering at the U. of New Mexico and is a Systems Designer at 3D Glass Solutions.

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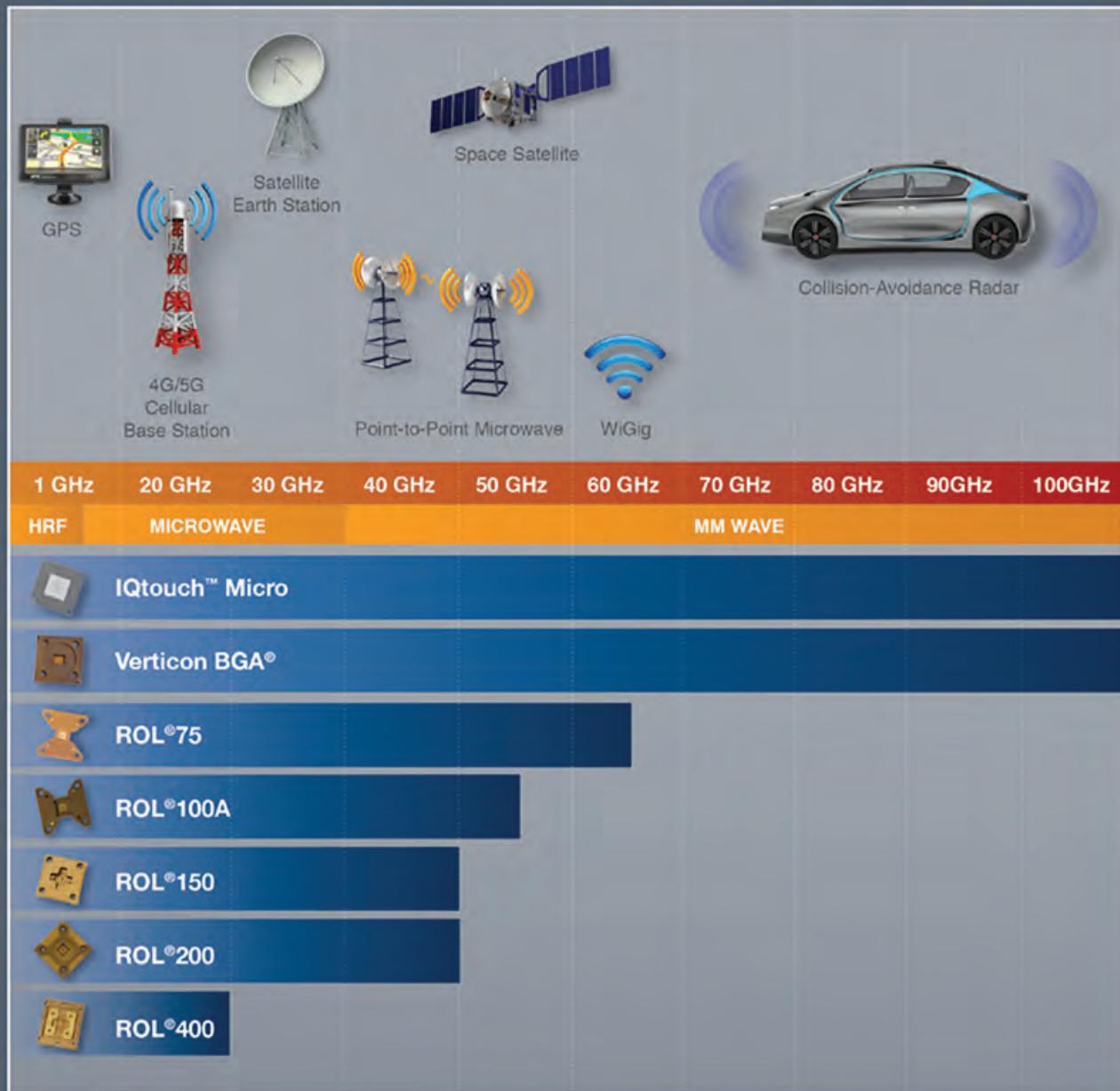
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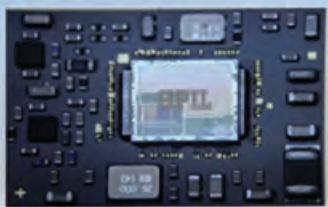
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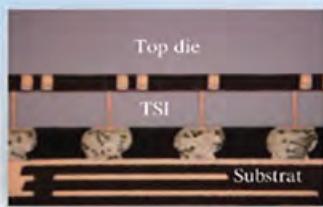
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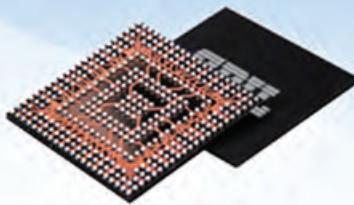
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