

Chip Scale Review®

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The Future of Semiconductor Packaging

Volume 20, Number 6

November • December 2016

Interconnects for MEMS & sensors

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- SiC wafer dicing
- 2.5D/3D TSV trade-offs
- Advances in photoresist stripping
- Multi-beam full cut of a mWLCSP
- Implementing FOWLP in the foundry
- Chip/package co-analysis of thermal-induced stress for FOWLP





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i innovate

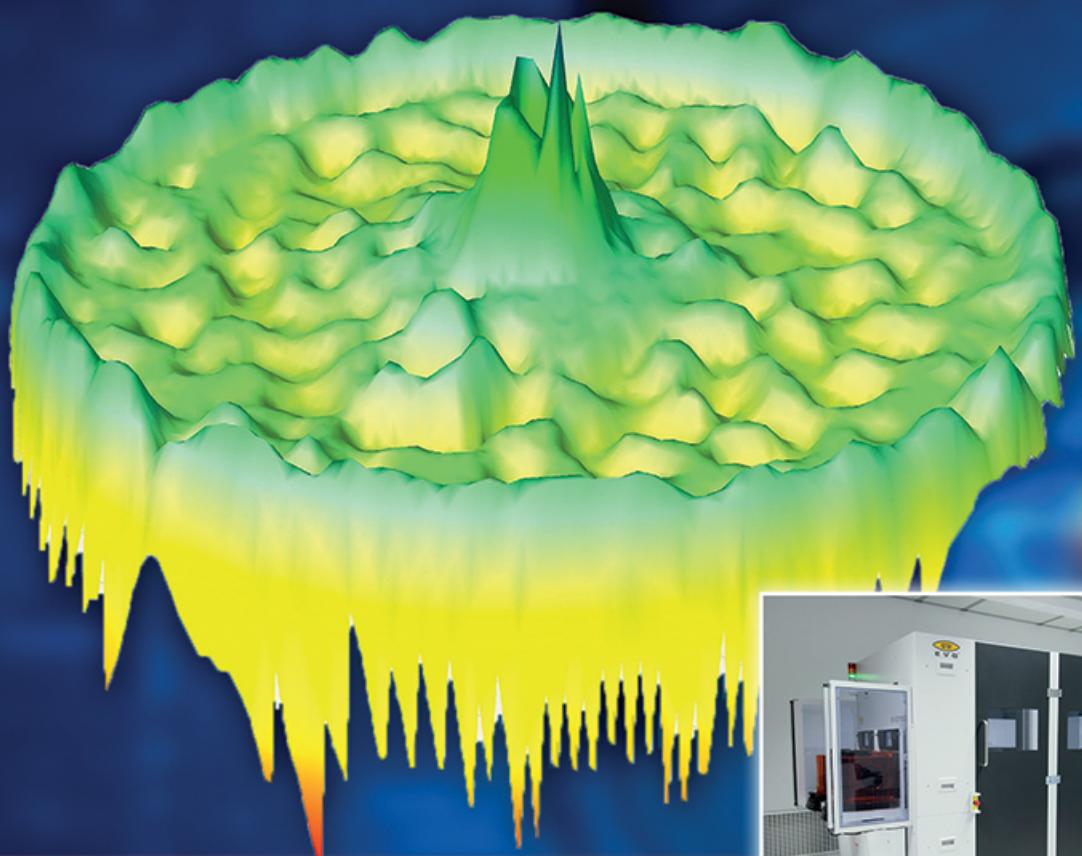
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The semiconductor and MEMS sensor industry is rapidly growing. Everyday, new applications, next-generation materials, and state-of-the-art information gathering sensors are being created. Each new device must be packaged and electrically connected to the outside world. A robust and reliable interconnect is critical to the success and function of every integrated circuit, sensor and device. Advanced technologies, new manufacturing technologies and novel materials come with unique challenges when it comes to making robust and reliable interconnects.

Cover image courtesy of SMART Microsystems Ltd.

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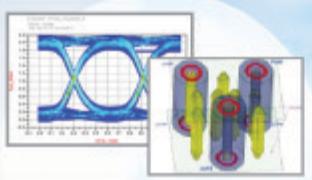
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GUEST EDITORIAL



Implementing FOWLP in the foundry

By John Ferguson *[Mentor Graphics]*

The technical challenges of implementing fan-out wafer-level packaging (FOWLP) are well known by now [1]. The interplay between system-on-chip (SoC) technologies and packaging requirements requires co-validation between integrated circuit (IC) and package design environments. The choice of operating system, IC or packaging technology, manufacturing output format, netlist format—these considerations, among others, can make the decision to adopt FOWLP a difficult choice to justify. However, the very difficulty of that decision has provided a new opportunity in the FOWLP marketplace.

Foundries are now developing their own integrated offerings for FOWLP. With a dedicated process flow and certified tools, design companies can realize the benefits of FOWLP technology without the worry, time, and expense of assembling design, layout, and verification flows from many disparate components and tools. Additionally, the foundry can provide dedicated packaging lines for these flows, ensuring availability and consistent, uniform processing. Electronic design automation (EDA) companies are also stepping up to deliver design and verification tools that support these solutions. Mutual customers can take advantage of these offerings to design and deploy FOWLP products using proven design methodology and certified EDA tools.

Comparing a foundry FOWLP process to that available from an outsourced assembly and test (OSAT) company illustrates some of the advantages and disadvantages of each approach, as shown in **Table 1**. The most obvious advantage for design companies is the option to work

with a single point of contact and a single process flow. Foundries have extensive expertise in generating process design kits (PDKs) for advanced IC processes. Now they are bringing that knowledge and expertise into the package co-design world. Not only do they have the advantage of significant experience and long, historic relationships with the EDA companies, they also control both the package and the die process details. This control enables them to more readily access information across the IC and package domains than might be possible when working with multiple parties.

With respect to the above discussion, for example, it would be difficult for an outsourced semiconductor and test (OSAT) supplier to put together a generic solution to solve parasitic extraction issues where die signals and package signals affect each other, because the OSAT only has detailed

knowledge about the package. Not only does it have little insight as to what might be in the dies, it may also have various legal restrictions as to what it is allowed to divulge to other IC suppliers.

By unifying the IC and package design and process flow, the foundry can ensure uniformity and consistency across designs. Troublesome features or packaging issues can be resolved more quickly, and the solutions can be implemented across all future designs. EDA tools can be enhanced or modified to address design and verification issues specific to that foundry. What that means to the designers is the ability to find and fix potential design issues earlier in the process, saving costly iterations and time-to-market.

On the other hand, having a single foundry control the FOWLP process means design companies will most likely be restricted to using dies produced by that foundry. If the goal

Foundry	OSAT
<ul style="list-style-type: none">• Single-source process<ul style="list-style-type: none">◦ All die tied to single foundry◦ Faster throughput time◦ Single point of communication• Dedicated FOWLP packaging process design kit and design methodology<ul style="list-style-type: none">◦ Certified EDA tools and flows• Controls manufacturing capacity and cost	<ul style="list-style-type: none">• Multi-party chain<ul style="list-style-type: none">◦ Can combine die from multiple foundries and processes◦ May incur transition delays◦ Multiple points of communication◦ Who owns yield issues?• Historically, no rigorously supported PDK support• Typically compete on lowest price

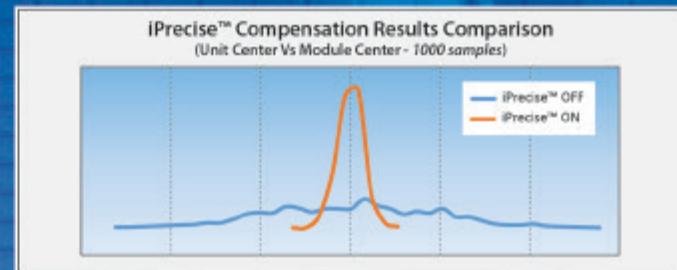
Table 1: Comparison of a foundry FOWLP process to that of an OSAT.

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is to unify and streamline the process, limiting die to those produced in-house is a logical choice. While this may not be an issue for some design companies, others may find it constricts their design and product options, limiting their available market opportunities. Those companies may choose to pursue or continue using an OSAT to ensure they can select from a full range of die options for their package offerings.

The availability of a dedicated PDK will be attractive to design companies, given the increased complexity associated with FOWLP design and verification. Manual control and checking of these designs is no longer practical from either a time or accuracy standpoint. In fact, some OSATS are now looking to implement their own PDKs to reduce the risk of these package designs [2].

The potentially faster throughput and availability of dedicated packaging lines may prove to be irresistible to companies for whom time-to-market is the predominant success factor. On the one hand, foundries may be incentivized to provide manufacturing capacity to customers using their internal FOWLP process, but on the other hand, they have full control of that capacity and the associated cost. OSATS traditionally compete on lowest cost, making them an attractive choice for design companies looking to control expenses. However, the overt financial costs belie many of the hidden costs discussed above, so companies must carefully consider all of their resources and options when choosing which path to pursue.

One of the first foundries to announce an in-house FOWLP process was TSMC, with its integrated fan-out (InFO) wafer-level packaging process that eliminates silicon, through-silicon vias (TSVs) and silicon interposers. The InFO process flow enables TSMC customers to deploy the unique fan-out layer structures and interconnects in the InFO technology, targeting cost-sensitive applications such as mobile and consumer products.

To ensure InFO design support, TSMC worked with EDA companies such as Mentor Graphics [3] to develop EDA solutions for IC and package design, including packaging design and layout, as well as physical verification. This congruency ensures that InFO designs are fully compliant with TSMC's packaging design rules and sign-off requirements to ensure adequate yield and reliability, and enables the foundry to provide a complete InFO design flow for its customers. Through its Open Integration Platform (OIP), TSMC has already established rule deck support for co-validation between IC and package design environments, including design rule checking (DRC) verification, layout vs. schematic (LVS) comparison, and inter-die DRC/LVS. The company is currently expanding InFO tool support into electrical analysis and sign-off, including parasitic extraction (to enable designers to analyze the parasitic impacts from InFO and its neighboring layers) and multi-die reliability analysis (analysis of electromigration (EM) and IR drop). In addition, TSMC and its ecosystem partners are extending the physical implementation with inter-die connections, and physical sign-off with inter-die DRC and LVS solutions.

Intel Custom Foundry recently introduced its embedded multi-die interconnect bridge (EMIB) as a cost-effective approach to in-package high-density interconnect of heterogeneous chips [4]. While not a true FOWLP design, it is a package option that eliminates the need for through-silicon vias and replaces large silicon interposers with small die-to-die silicon bridges. They are also rumored to be working on a true fan-out wafer-level packaging process, but no details have yet been made public.

As more foundries look to implement proprietary FOWLP flows, how will this affect the FOWLP market? Where will design companies go? While design strategies may drive decisions at first, the market

is new enough to entice companies to reexamine their package design flows and possibly move to foundry-provided programs. On the other hand, OSATS may take their cue from these foundries and accelerate the development of their own standardized FOWLP flows to retain and expand their customer base. It will be interesting to watch the market dynamics as this technology becomes more widely used.

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Biography

John Ferguson holds a BS degree in Physics from McGill U., an MS in Applied Physics from the U. of Massachusetts, and a PhD in Electrical Engineering from the Oregon Graduate Institute of Science and Technology. He is the Director of Marketing for Calibre DRC Applications at Mentor Graphics; email john_ferguson@mentor.com

Ball Placement System (Micro Solder Ball Mount Technology)



BPS-8200
Ball Placement System

System Performance

Cycle Time : 12~14 Sec (Normal Package(1 Dotting/Strip))

25~30 Sec (Fine Pitch Package(2 Dotting/Strip))

40~45 Sec (Fine Pitch Package(2 Dotting/Half Strip))

YIELD PERFORMANCE : 99.98%

Placement Accuracy : +/- 0.02mm

Fine Pitch Capability : 0.100mm_Ball size / 0.180mm_Ball pitch

Strip Handling Capacity : 50 ~ 95mm

Width x 180~260mm Length

Product Flexibility : All kinds of laminated Substrate BGA Package series

Quick Conversion Time : Ball tool, Flux tool, Lift Block

Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)

Foot Weight : 3,000kg

BPS-8200 Process (Stand-alone type : Magazine input)

MOLD MARKING SOLDER BALL ATTACH REFLOW



BPS-8200S
Ball Placement System

Cycle Time : 12~14 Sec (Normal Package(1 Dotting/Strip))

25~30 Sec (Fine Pitch Package(2 Dotting/Strip))

40~45 Sec (Fine Pitch Package(2 Dotting/Half Strip))

YIELD PERFORMANCE : 99.98%

Placement Accuracy : +/- 0.03mm

Fine Pitch Capability :

0.100mm_Ball size / 0.180mm_Ball pitch

Strip Handling Capacity :

50 ~ 95mm Width x 180~260mm Length

Product Flexibility :

All kinds of BGA Package series

Quick Conversion Time :

Ball tool, Flux tool, Lift Block, Stripper(Optional)

Foot Print & Weight : 2,300(L) x 1,350(W) x 1,820(H)

Foot Weight : 3,000kg

BPS-8200S Process (In-line type: Substrate Input)

MOLD MARKING SMT SOLDER BALL ATTACH REFLOW



BPS-7200FC
Ball Placement System
for Flip Chip

Cycle Time : 12~14 Sec (Single Boat without Flipper)

22~25 Sec (Matrix Boat without Flipper)

27~30 Sec (Matrix Boat with Flipper)

YIELD PERFORMANCE : 99.98%

Placement Accuracy : +/- 0.03mm

Fine Pitch Capability :

Min. 0.20mm Ball size & 0.40mm Pitch

Product Flexibility :

All kinds of Flip chip BGA on boat

Quick Conversion Time :

Ball tool, Flux tool, Vacuum Block, Pre-aligner, Flipper(Optional)

Foot Print & Weight : 2,800(L) x 1,800(W) x 1,870(H)

Foot Weight : 3,500kg

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wBPS-2000
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Ball Placement System

Cycle Time : 120sec/wafer(12'wafer - 880,000 Ball)

High Capability : +/- 0.02mm

Fine Pitch Capability : 0.050mm

Ball size & 0.120mm mm Pitch

Target Device : 8,12inchwafer

High Productivity : Max. 30WPH

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PRS vision - Look up type

Stencil, Wafer Vacuum Chuck

Lm Guide + Ball Screw

Wafer LoadingLinear motion

Vacuum ejector

Inlet PRS Vision

Flux Y axis servo motion

Flux Squeegee Blade

ABL™ (Air floating Ball Loading unit)

Foot Print : 2900(L) x 1300(W) x 2100(H)

Package EMI Shielding System

H-VAM Application



PSS-8000SL
Package Sorting System

System Performance

UPH : 13,000

Yield Performance : 99.9%

Placement Accuracy : +/- 0.15mm

Picker : 14 Pickers x 2 Head

Package Type : 3x3 mm ~ 20x20 mm LGA, BGA

Product Flexibility : LGA, BGA PKG Applicable

Quick Conversion Time :

Detach tool, Picker pad, Precise tool

Foot Print : 3,460(L) x 2,090(W) x 1,760(H)

Foot Weight : 3,500kg



PSS-8000SUV
Package Sorter System with Vision

PI-TAPE Application



PSS-7000SL
Auto Package Loading
P&P System

System Performance

UPH : 13,000

Yield Performance : 99.99%

Placement Accuracy : +/- 0.02mm

Picker : 14 Pickers x 2 Heads

Package Type : 3x3 mm ~ 20x20 mm LGA

Quick Conversion Time :

3x3 mm ~ 20x20 mm LGA, BGA

Product Flexibility : LGA, BGA PKG

Applicable Quick Conversion Time :



PSS-7000SUV
Auto Package Loading
P&P System

System Performance

UPH : 10~12K (Based on 860Unit/ Frame)

Placement Accuracy : +/- 0.05mm with Theta axis

Product Flexibility : 3x3 mm ~ 20x20 mm

LGA, BGA PKG Applicable

Quick Conversion Time : Picker Pad: Less than 20Min

Reject sorting : Rework Tray

Vision System : Top Frame Align - 1.4K (FOV 20.0x15.0, Resolution 14um)

Top Picker Align - 5M (FOV 22.0x16.0, Resolution 9um)

Bottom Align - 4M (FOV 20.5x20.5, Resolution 10um)

Motion Picker : 10ex x 2set (Individual Z, T Motion)

Detach Picker x 2set

Foot Print & Weight :

2,050(L) x 2,000(W) x 1,800(H) / 2,500kg

Developing robust interconnects for MEMS and sensors

By Mara Rice [SMART Microsystems Ltd.]

The semiconductor and MEMS sensor industry is rapidly growing. Every day new applications, next-generation materials, and state-of-the-art information gathering sensors are being created. Each new device must be packaged and electrically connected to the outside world. A robust and reliable interconnect is critical to the success and function of every integrated circuit, sensor, and device. Advanced technologies, new manufacturing techniques, and novel materials come with unique challenges when it comes to making robust and reliable interconnects. Custom packaging, unusual part geometry, and unconventional material limitations can make a usually reliable interconnect process difficult to develop. Despite these obstacles, well understood processes like gold ball bonding and aluminum wedge bonding, as well as emerging technologies like isotropic and anisotropic conductive adhesives can be successfully implemented with extensive process development.

More than 90% of the 15 trillion interconnects are manufactured by wire bonding, and ball bonding is the predominant method of making these interconnects. A combination of heat, ultrasonic energy, and force is used to form a cold fusion weld between the gold wire and the material of the desired bond location. Gold is preferred for its mechanical thermal properties and low chemical reactivity. Gold wires can be easily bonded to many materials and will not likely corrode in harsh environments. Gold will not oxidize at high temperatures and has a lower thermal coefficient of expansion than copper and aluminum. Gold ball bonding is frequently the interconnect method of choice for many sensors, including photodiodes. Some photodiodes are used in high-temperature applications and may be required to sustain temperatures as high as 200°C during operation. Because of this, gold ball bonding is often used in photodiodes.

The photodiode application, like many others, presents many unique wire

bonding process challenges owing to the unique application of the device. The first challenge is fixturing. Before wire bonding development can begin, a custom fixture must be designed to securely hold the parts and maintain temperature during thermosonic bonding. Gold ball bonding requires that parts be held in a stationary position, with a fixed orientation, perpendicular to the bonding tool. The fixture must be able to withstand elevated bonding temperatures, hold the part securely, not add any unintended stress to the part, and not interfere with bond head movement. In some cases, the photodiode has a unique package designed so that the die is thermally insulated. This presents further challenges when designing a fixture. To ensure the part is fully heated to the desired temperature, a fixture is designed to conduct heat and maintain the desired temperature through the package and to the wire bond pads.

Once fixturing has been resolved, wire bond development can begin. This involves development of a robust weld through a design-of-experiments (DOE) for critical bond parameter selection and optimization while meeting the package limitation for wire loop geometry. The photodiode can contain some unique geometry that can present product limitations over life. If wires are too long or tall they can interfere with the package, become deformed with heat or vibration, or become shorted. By understanding loop geometry and bond head movement, proper looping can be determined.

Loop geometry is not the only challenge presented by a photodiode's unique package design. The machined surfaces on the pins are not always an entirely favorable bonding surface. These surfaces can be coarser and less planar than a typical semiconductor finish on account of previous processes upstream in the assembly. The machined surfaces are where the wire bonds terminate. The termination end of

the gold ball bond is called the stitch (also referred to as the crescent) bond. Just like the ball, the stitch bond requires a thick, even, and smooth plating to make a reliable bond. To overcome the surface defects a stand-off stitch bond (SSB) is used instead of a standard stitch bond (see **Figure 1** for a comparison). To make a SSB, a gold ball is first bonded to the pins or leads, where the bond will terminate. This gold ball has a larger surface area and contains more gold than a standard stitch bond. Because of this, the gold ball bonds more readily and more securely to the imperfect surfaces. Once the gold balls have been placed, the gold wire bond is made as usual, with the stitch bond welding to the top of the gold ball rather than directly to the pins or leads. The ball

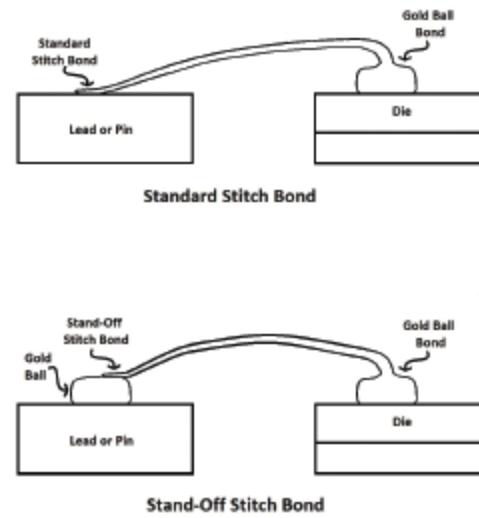


Figure 1: Diagram showing the difference between a SSB and a standard stitch bond.

offers a large, thick, and smooth surface to which the stitch bond can be welded. This is a more reliable and robust bond for non-semiconductor grade surfaces, which can be used in high-reliability applications.

Aluminum wedge bonding is another popular interconnect technique. Unlike gold wire, aluminum does not need to be bonded

at an elevated temperature. With the use of force and ultrasonic energy, aluminum can be welded to Al or some dissimilar metals at room temperature (see **Figure 2** for an image of the bond head and work surface). This method is especially useful for temperature-

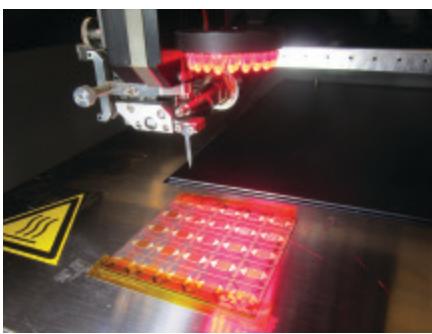


Figure 2: Aluminum wedge bond head with a test coupon on the work surface.

sensitive parts. Because of the low-temperature capabilities of aluminum wedge bonding, it is selected as the interconnect method for many applications, such as MEMS optical sensors. MEMS optical sensors are sometimes connected to a flex circuit and they can be extremely sensitive to both heat and electrostatic discharge (ESD). These unique characteristics present another set of challenges.

Once again, fixturing is always critical. Much like with gold ball bonding, the parts need to be secured in a fixed location, in an established orientation, and on a plane perpendicular to the bond tool. A common obstacle with a flex circuit is that it does not tend to lie perfectly flat. This creates undesired opportunity for the flex to shift during bonding. This movement can put an unwanted force on the die creating either die movement, die tilt, or die cracking while the part is in the fixture. A combination of set screws to secure the die and vacuum to secure the flex circuit can achieve necessary part perpendicularity and stability during bonding while removing the threat of unnecessary stress on the die. A slight variation between die attach and bond line thickness on each part can allow for some die movement in the fixture. This movement can disrupt wire bonding. The problem can be solved by placing a thin compliant support material beneath the die during bonding. This compliant material supports the die and reduces movement during wire bonding. Fixtures are initially designed on a solid modeling computer program. They are then rapid prototyped in

SLA plastic to check fit, form, and function. Once the design has been verified, the fixture is approved and precision-machined out of aluminum.

MEMS optical sensors can be extremely ESD sensitive (e.g., <100V). Often times these are devices designed to be actuated electrostatically. As a result, every step of the process must be ESD-compliant. Special caution is taken during process development, handling, storage, and shipping. Every surface these parts touch must be checked and grounded before coming in contact with the parts. This requires careful consideration when developing the handling system used for the parts—for example, the fixtures used on the wire bonding equipment, trays used at inspection stations, and the protocol for how the parts get transferred during the process. Because of the extreme sensitivity of the parts, great caution must be used at all times when dealing with ESD-sensitive parts in order to avoid unwanted yield loss.

Once fixturing has been verified and ESD sensitivity has been guarded against, wire bonding development can begin. It is common that wire bond process development is not straight forward. With the increased demand for more interconnects in a smaller space, leads and bond pads on the PCB can become extremely dense. Depositing metallization with small and dense features can result in non-ideal surfaces. Sometimes leads can be tilted non-planar to the fixture. Often when this occurs, no two parts are the same, with each lead tilted to a varying degree with metallization deposited to varying thicknesses. This makes developing a reliable and repeatable bond process difficult. By increasing the search height and decreasing the touchdown speed, the wire bonder can compensate for the varying heights of the leads. Utilizing a combination of angled bonding and s-curves, lead tilt is accounted for and a robust aluminum wedge bonding process can be developed (see **Figures 3 and 4**).

The increasing demand for advanced applications of sensors has led to a surge in new technologies. Often times these new technologies use novel materials—sometimes referred to as next-generation materials. Novel materials that are used to functionalize next-generation MEMS sensors need to be integrated with semiconductor and microelectronic manufacturing processes. These novel materials can have unique material properties that are extremely useful in the sensor, but often come with strict process limitations. For example, a sensor

used in new medical imaging technology may use a die made out of one such next-generation material. Next-generation materials typically require extensive development and can become very costly. These materials can also be extremely brittle (more brittle than Si), temperature sensitive, and sensitive to chemical exposure. Some materials cannot withstand the force needed for wedge bonding or the heat (and force) needed for ball bonding. These sensors need to connect to a PCB, but wire bond interconnects often can damage the sensor.

Because wire bonding is often not a viable option, bond pads can be engineered to be on the backside of the die to allow for a direct attach to the PCB. More stable materials can then undergo a flip-chip thermal compression process. Unfortunately, thermal compression requires both heat and force that may damage novel materials that are too brittle. Temperature-resistant and less costly materials could be interconnected using a solder reflow process. The heat of a reflow process can damage the heat-sensitive

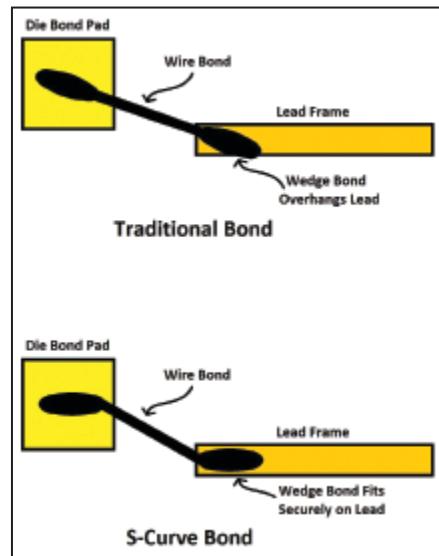


Figure 3: Diagram showing an S-curve bond shape.

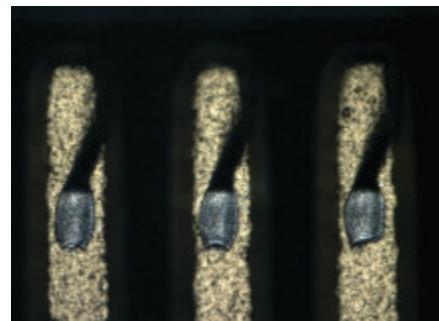


Figure 4: Image of S-curve wire bonds with 125µm pitch.



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- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

materials and does not allow for rework. To protect the novel material from heat and stress, a new flip-chip interconnect method can be developed. The pads on the PCB can be bumped with gold balls. Each ball is then coined to increase surface area and create bump height consistency (**Figures 5** and **6**). An isotropic conductive adhesive (ICA) can be dispensed on top of each coin. The adhesive can run over the sides of the coins

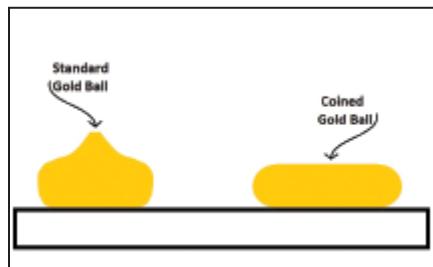


Figure 5: Diagram showing the difference in geometry between a coined and an un-coined bump.

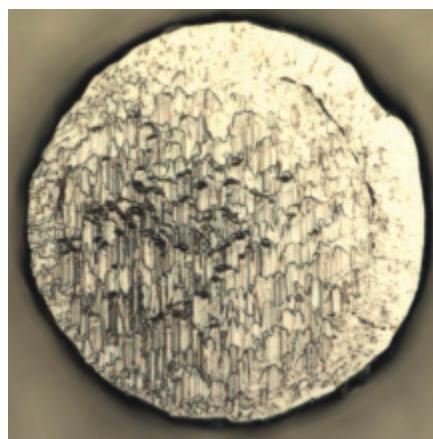


Figure 6: Photo of a coined gold bump.

as needed, but should not come in contact with any other adhesive covered coin. The die can be placed on the adhesive covered coins. It is aligned so that the adhesive covered coins contact the bond pads on the die and establish interconnects between the die and the PCB. The PCB provides passivation between each pad, coin, and adhesive "glob." Insulated interconnects are formed as a result.

The ICA has a low-temperature cure (less than 80°C) so heat is never applied to the next-generation material. Only a slight force is required to attach the die to the conductive adhesive, which protects a brittle die from compression forces and stress damage. The adhesive acts as a semi-compliant material and compensates for any non-planarity between the coins and the die. It also

compensates for any coefficient of thermal expansion mismatch between the PCB and novel material, further protecting the brittle material from stress.

The novel material and die itself are very expensive, therefore it is crucial that rework is possible. Because of the high-value added nature of the components, scraping a working die as a result of a misalignment, electrical short, or other interconnect failure is not an option. The conductive adhesive allows for the die to be repositioned or removed after it has been attached without sustaining damage. This is an important cost-saving process element. It allows for the new interconnect process to be fully developed at the lowest cost possible. Additionally, this method provides working prototypes without sacrificing thorough and deliberate testing and development.

Summary

These exciting advancements in the semiconductor industry are not without challenges. New applications and next-generation materials provide vast new opportunities for integrated circuits, MEMS sensors, and state-of-the-art manufacturing techniques. Creating robust and reliable interconnects for these new technologies presents a series of new obstacles. Despite this, problems encountered as a result of custom packaging, unique geometry, and unusual material limitations can be overcome. Using a combination of well understood processes (such as wire bonding), emerging technologies (such as isotropic conductive adhesive), and creative thinking, reliable interconnect processes can be developed for any new technology. Robust interconnects are crucial for the function and success of all new semiconductor and sensor technologies. Interconnect methods are adapting and advancing with the changing market. The cutting edge breakthroughs in the semiconductor market, combined with advanced interconnects processes, will continue to fuel growth and expand the semiconductor and MEMS sensor landscape.

Biography

Mara Rice received her Associate's Degree in Mechatronics from Lorain County Community College and is in her final year at Cleveland State U., working to receive a BS in Mechanical Engineering. She is a lead Engineering Technician at SMART Microsystems; email mara@smartmicrosystems.com



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Chip/package co-analysis of thermal-induced stress for fan-out wafer-level packaging

By Stephen Pan, Zhigang Feng, Norman Chang [ANSYS, Inc.]

This paper presents an innovative co-analysis solution for thermal-induced stress of fan-out wafer-level packaging (FOWLP). The reliability of FOWLP on either the fan-out package region or in the chip inter-dielectric layers (IDLs) are of concern for loadings from large differential thermal expansions at Si chip and package/printed circuit board (PCB) interfaces and the glass transition temperature (T_g) effects in the dielectric materials. The dielectric layers in a wafer-level package (WLP) and the IDL of a chip have weak, extreme low-k (ELK) materials that are easy to develop cracks at relatively low stress levels. The drastic property changes, for example, a 30x change in the coefficient of thermal expansion (CTE) at T_g , aggravates the development of micro-flaws that coalesce into long cracks leading to eminent failure of the FOWLP. The approach in thermal-induced stress analysis includes the generation of thermal-aware chip power maps for multiple dies in FOWLP, the conversion of converged thermal profiles in FOWLP to thermal loadings for stress analysis, efficient model generation and analysis for T_g effect of nonlinear material properties, and detailed sub-modeling of on-chip structures for thermal-induced stresses. Discussions of innovative thermal-induced stress modeling process and results extraction for a FOWLP test case are demonstrated.

Introduction

FOWLP is known for its low cost and high performance. **Figure 1** is the cross-section view of a FOWLP with redistribution layer (RDL) fan-out layers, which is thin with respect to its thickness. Like FCBGA, there could be multiple dies in FOWLP, either side-by-side or stacked. The dies could be flushed with the mold and exposed to air for better heat dissipation. The fan-out area could have copper pillars up to the top to connect to a top package and form a package-on-package (PoP) configuration. Removing the need for a package substrate reduces the cost

and makes the FOWLP a popular choice in low-power high-performance industry such as for mobile devices.

The electrical and thermal performance of FOWLP was discussed in [1] that it has superior form factor, pin count, and thermal performance to flip-chip ball grid array (FCBGA) and it paves the way to the solution from foundry today. The mechanical reliability of the dielectric layer of the bond-on-lead (BOL), which has similar structure as FOWLP was reviewed [2]. This shows the efforts of a packaging house to provide a solution. This paper is from the perspective of electronic design automation (EDA) tool development to demonstrate what can be done for FOWLP in terms of thermal and stress analyses.

In the following sections, a FOWLP package with two side-by-side chips was analyzed for thermal and stress responses and checked for reliability-related issues in the chip-package-system (CPS) environment. One of the chips in this FOWLP was reviewed for thermal stresses in the IDL, which is known to be weak and has reliability concerns at higher stresses. The focus of this paper is on the modeling and simulation capability developed for FOWLP and the SoC chips. The theory involved in the thermal-stress analyses are described first. Then the important modeling methods in creating thermal and stress models are discussed with sample case results presented.

Theory

Heat flow. The governing equations of the heat conduction are:

For anisotropic and transient,

$$\frac{\partial}{\partial x} \left(K_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(K_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(K_z \frac{\partial T}{\partial z} \right) - \rho c \frac{\partial T}{\partial t}$$

$T = T(x, y, z, t)$ = Temperature distribution

K_x = Thermal conductivity in the x-direction

K_y = Thermal conductivity in the y-direction

K_z = Thermal conductivity in the z-direction

ρ = Mass density

c = Heat capacity

For isotropic steady state condition, the governing equation is the following:

$$K \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) = 0$$

where $K_x = K_y = K_z = K$

The boundary conditions are for a known temperature at specific locations:

$$T(x_o, y_o, z_o; t) = F(t)$$

For heat flux/power generation,

$$Q = -KA \frac{\partial T}{\partial n}$$

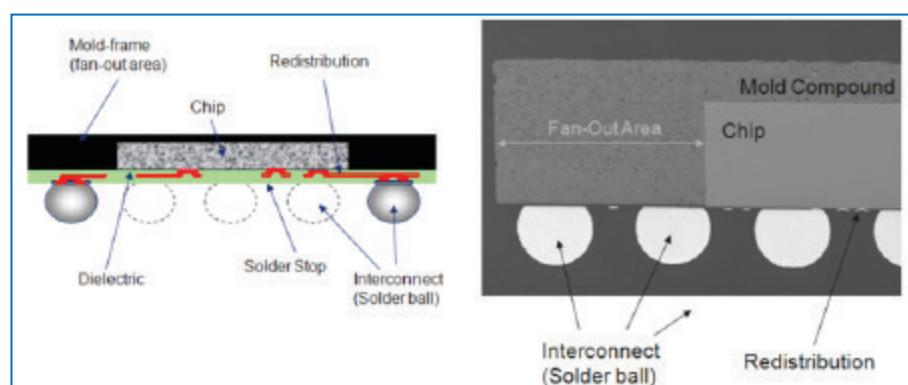


Figure 1: Structure of a modern FOWLP.

where

Q = Heat flux in Watts

A = Surface area in mm²

n = Outer normal of the surface area

For heat convection and radiation,

$$q = -K \frac{\partial T}{\partial n} = (h + h_r)(T - T_\infty)$$

where

n = outer normal of the surface

T = package surface temperature

T_∞ = ambient temperature

h = heat convection coefficient due to convection

h_r = effective heat convection coefficient due to radiation

q = surface heat flux

Use the equation above for heat loss to the ambient.

Thermal-elasticity. The stress (**Figure 2**) is related to the strains by:

$$\{\sigma\} = [D]\{\varepsilon^{el}\}$$

where:

$\{\sigma\}$ = stress vector

$[D]$ = elasticity or elastic stiffness matrix or stress-strain matrix

$\{\varepsilon^{el}\} = \{\varepsilon\} - \{\varepsilon^th\}$ = elastic strain vector

$\{\varepsilon\}$ = total strain vector

$\{\varepsilon^th\}$ = thermal strain vector

$$\{\varepsilon\} = \{\varepsilon^th\} + [D]^{-1}\{\sigma\}$$

The stress vector definition is shown in **Figure 2** and with the following expressions:

$$\{\varepsilon\} = \{\varepsilon^th\} + [D]^{-1}\{\sigma\}$$

$$\{\varepsilon^th\} = \Delta T^T [\alpha_x^{se} \alpha_y^{se} \alpha_z^{se} 0 0 0]^T$$

α_x^{se} = secant coefficient of thermal expansion in the x direction

$$\Delta T = T - T_{ref}$$

T = current temperature at the point in question

T_{ref} = reference (strain-free) temperature

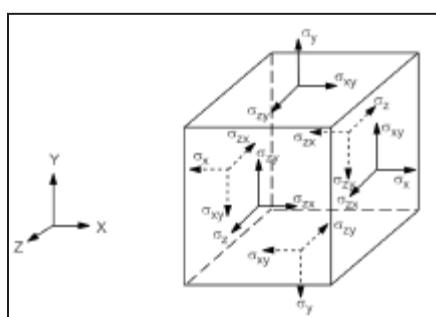


Figure 2: Stress vector definition.

The flexibility or compliance matrix, $[D]^{-1}$ is:

$$[D]^{-1} = \begin{bmatrix} 1/E_x & -v_{xy}/E_x & -v_{xz}/E_x & 0 & 0 & 0 \\ -v_{yx}/E_y & 1/E_y & -v_{yz}/E_y & 0 & 0 & 0 \\ -v_{zx}/E_z & -v_{zy}/E_z & 1/E_z & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/G_{xy} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/G_{yz} & 0 \\ 0 & 0 & 0 & 0 & 0 & 1/G_{xz} \end{bmatrix}$$

where typical terms are:

E_x = Young's modulus in the x direction

v_{xy} = major Poisson's ratio

v_{yx} = minor Poisson's ratio

G_{xy} = shear modulus in the xy plane

For isotropic materials ($E_x = E_y = E_z$ and $v_{xy} = v_{yz} = v_{xz}$) the $[D]^{-1}$ matrix is symmetric.

The governing equation of thermal-elasticity is given by the strain-displacement relationship:

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{xy} \\ \gamma_{yz} \\ \gamma_{zx} \end{bmatrix} = \begin{bmatrix} \frac{\partial}{\partial x} & 0 & 0 \\ 0 & \frac{\partial}{\partial y} & 0 \\ 0 & 0 & \frac{\partial}{\partial z} \\ \frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \\ 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ 0 & 0 & \frac{\partial}{\partial x} \end{bmatrix} \begin{bmatrix} u \\ v \\ w \end{bmatrix}$$

The equilibrium equations in terms of displacements for isotropic materials are:

$$(1-2v)\nabla^2 u + \frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial x \partial y} + \frac{\partial^2 u}{\partial x \partial z} = 2\alpha(1+v)\frac{\partial T}{\partial x}$$

$$(1-2v)\nabla^2 v + \frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 v}{\partial x \partial y} + \frac{\partial^2 v}{\partial y \partial z} = 2\alpha(1+v)\frac{\partial T}{\partial y}$$

$$(1-2v)\nabla^2 w + \frac{\partial^2 w}{\partial z^2} + \frac{\partial^2 w}{\partial z \partial y} + \frac{\partial^2 w}{\partial z^2} = 2\alpha(1+v)\frac{\partial T}{\partial z}$$

The finite element method (FEM) is used by reducing the equilibrium equations into the matrix with the displacement vector as unknowns. Once the displacements are solved, strain and stress can be calculated.

The material properties of E and α could be temperature-dependent as used in the FOWLP thermal-stress study. The boundary conditions in the thermal-stress problem are the displacement constraints

at a local area to avoid rigid body motion, and the temperature distribution of FOWLP on the board. For warpage analysis, environment temperature change is used for differential thermal expansion of the FOWLP.

Modeling of FOWLP for analysis of ECAD-based FOWLP

The structure of the FOWLP with two chips is similar to that of a FCBGA with molding compound, except that the package substrate layers are replaced with the redistribution layers (RDLs), which are much thinner in thickness. The total thickness of the RDL layers is around 60 μ m vs. ~300 μ m for a typical FCBGA package. The mold material is placed around the dies as structural support to avoid excessive warpage on account of the use of RDL layers, which are thin in the fan-out zone. The configurations of the FOWLP are listed in **Table 1**.

Attribute	Specifications
FOWLP size	8x8mm
Chips	2x3x0.3mm with 450 Cu pillars
RDL thickness	0.06mm
Mold	7x6x0.3mm
2 nd level joints	270 Cu pillars with solder paste

Table 1: Configurations of the FOWLP device used in the study.

Figure 3 is the 3D geometry of the FOWLP as imported from ECAD in a chip-package thermal analyzer [6] and the placement of the two chips with the molding flush on the die top so that

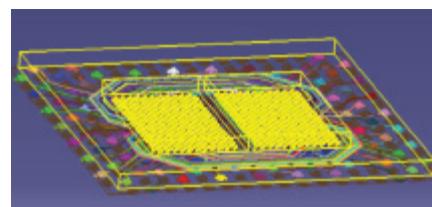


Figure 3: Geometry configuration of the FOWLP in this study through ECAD import.

the dies are exposed for better heat dissipation. The yellow pattern under the dies are the pins/pillars under the dies in contact with the RDL. **Figure 4** is the zoom-in view of the traces, via, and pins. The target analysis model using finite element analysis (FEA) should include the geometry details for the most accurate solutions.

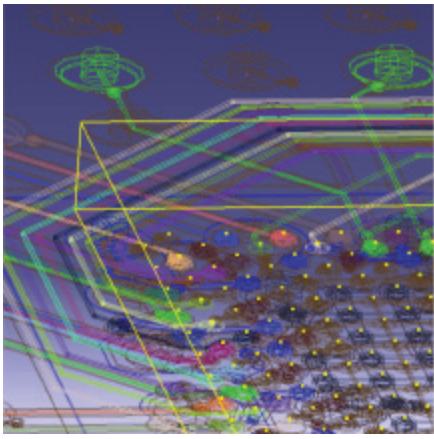


Figure 4: Zoom-in view showing the details of trace, via, and pins/Cu pillars under the die.

The thermal-stress task flow (Figure 5) for FOWLP starts with a chip power map generated from a chip power calculation tool [6]. The chip power map is in the form of the chip thermal model (CTM) to be described in the next section. The FOWLP on-board geometry was then modeled using the FE method with CTM as the power input and still air at 20°C ambient. Empirically-based equivalent heat transfer coefficients on exposed surfaces are used in this study. For a more complicated environment, such as multiple packages/boards and fans in a box, the moving air environment can only be simulated by computational fluid dynamic (CFD) type simulators [8]. The resulting thermal boundary conditions for FOWLP can be extracted from the CFD solutions and used in the conduction-based thermal analysis model in this study.

After the thermal analysis of FOWLP in a system, the analysis model can be converted for stress analysis using a structural analysis tool [7] to review the deformation and stress states on Cu traces/vias or dielectric, which could be of weak extreme low-k (ELK) or ultra low-k (ULK) material.

Chip power generation

Chip power arises mostly from transistors. Figure 6 shows the schematic of current flow in a CMOS device and its switching power due to the charging and discharging of output capacitances, i.e., power $\sim C_L \times V_{dd}^2 \times f$ where f is the switching frequency.

For system-on-chip (SoC) or gate-level chip design, the instances or the standard cells that provide the Boolean logic functions are composed of transistors

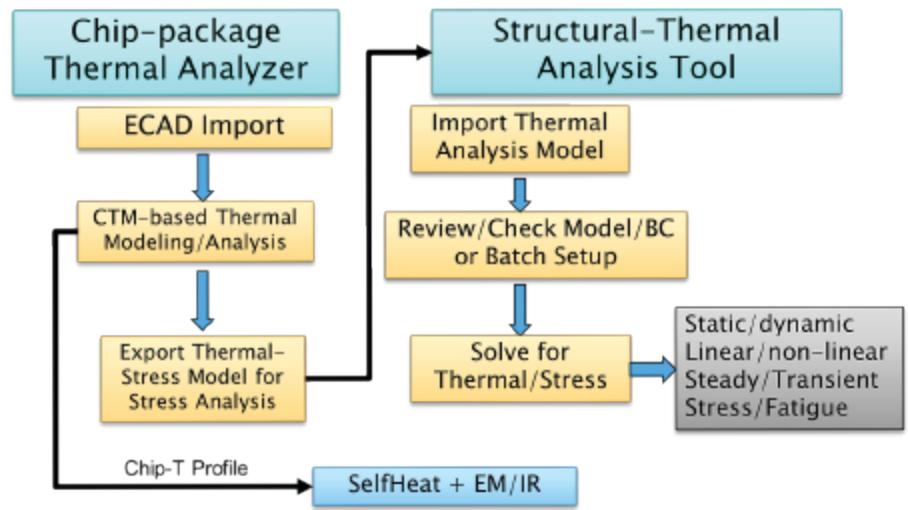


Figure 5: Task flow for thermal-stress in FOWLP and thermal-aware EM/IR of an SoC design.

and power calculations are done for the different cells or instances. There are more than 8 million instances in an area of 6mm² for each of the two chips in this FOWLP under consideration. If each instance is a heating object, the thermal modeling efforts will be overwhelming in current FEM technology. The current approach is to lump them into a smaller number of heat sources. A tile-based mapping from the different instances/elements was performed and the resulting power map based on 10x10µm tiles had – in total – about 120 thousand tiles or heat sources in the resulting power map for the thermal analysis. Figure 7 is the contour display of the power map at a uniform temperature condition. The total power in this power map is about 1.5W. The transistor or instance/element power is typically temperature-dependent due to the leakage current component. The total power in a device includes the dynamic switching power in Figure 6 and the leakage power. From the chip power integrity tool, a collection of the power map calculated at several temperature points was generated in CTM, which is a temperature-dependent power map library for the chip. The generation of CTM was from either vector-less or event-driven power scenarios. It is the power on the chip at a specific operating mode averaged over a period of time. The on/off of the CTM operating modes can be assembled into transient scenarios for analysis [5].

The CTM was rotated when applied to the chips in the analysis. In this FOWLP as defined in ECAD, viewing from the top, the left chip CTM was rotated 90°

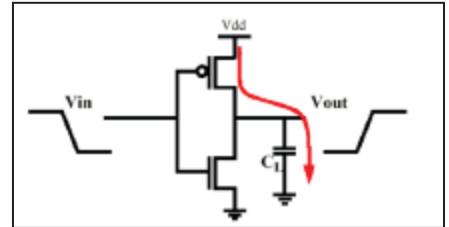


Figure 6: Transistor power $\sim C_L \times V_{dd}^2 \times f$.

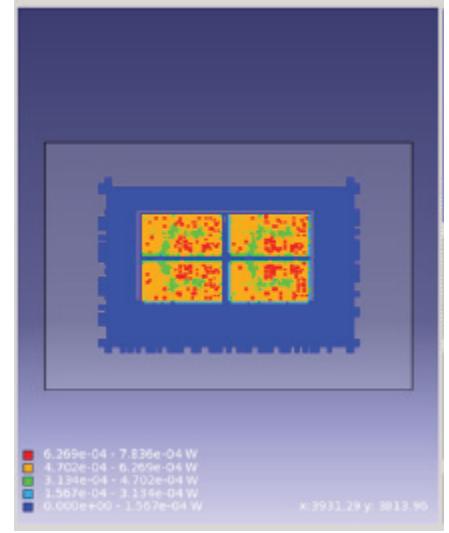


Figure 7: Chip power map in CTM.

and the right chip CTM was rotated 270° before flipping for final placement on the FOWLP. When using CTM in thermal analysis, the power on the tiles can be updated with the resulting temperature for the next power-thermal iteration. Typically, only 2-3 iterations are needed for the converged solution in the CPS environment.

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CPS thermal modeling

Analysis model using FEM was generated in the chip thermal analyzer with the CTM power applied to the chips in a FOWLP. The analyzer ran through thermal/power iterations until the temperature profile and power map were consistent, i.e., at a converged state. **Figure 8** is the converged thermal profile on top of the FOWLP. In this FOWLP study, the materials used were defaults from the chip thermal analyzer for a

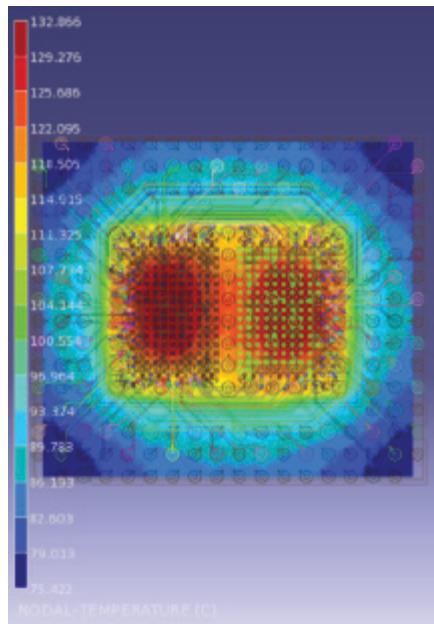


Figure 8: Thermal response on top of an FOWLP device, calculated in RH-CTA with a Tmax on the chip of 132.866°C.

typical ball-grid array (BGA) package. However, this will not affect our goal of demonstrating the thermal-induced stress flow. The same FE model is used in the subsequent thermal stress analysis. In this FOWLP case, the FE model has 1.8M nodes, 3.3M elements, and the model details can be reviewed in the structural analysis software [7] (**Figure 9**).

Figure 10 shows the FE details of the traces and vias in the RDL of the FOWLP. The details of the geometry in the analysis model is critical to the thermal response accuracy, and is especially sensitive for smaller packages [4] like the one in this example. If smeared properties are used on RDL layers, the Tmax will be underestimated by 14% and the Theta_{ja} of this FOWLP will be reduced from 37°C/W to 31°C/W. The observation is that there are many heat flow paths through the narrow

vias from layer to layer in the detailed model. In the smeared model, however, the layers are shorted by the material of equivalent conductivity in a much larger region near each via. Heat is easier to spread out through “shorted” conductive materials, even if they are less conductive than the copper vias. On the other hand, stress analyses of traces and vias are not possible in a model using simplified and smeared properties. The smeared model is only good in estimating overall warpage, die stress, and solder joint reliability, not for prediction of failures in the RDLs of the FOWLP.

One of the issues in detailed trace outline modeling by FE modeling is the existence of degassing holes on the power/ground (PG) nets in RDLs with large metal pieces. While degassing holes are necessary in the formation of the RDL in the FOWLP, it makes the mesh generation much more difficult (**Figure 11**). Comparison of results of the thermal models with and without degassing holes using FE modeling showed negligible differences in the temperature distribution and maximum temperature on the chips. This is probably due to the very low heat flux on the PG layers so that the existence of the degassing holes has minimal impact on the overall heat dissipation path. For stress analysis, warpage results were compared and negligible impacts from the degassing holes were observed, possibly due to the small contribution of the thin RDL layers to the stiffness of the whole FOWLP

structure. A function in the chip thermal analyzer was created to identify and remove the degassing holes automatically for simulation purposes. The number of degrees of freedom in this FOWLP model is about 1.8M and the structural tool [7] took about 14min and 7.3GB of peak memory to solve with a single core in a Linux server with 256GB of memory.

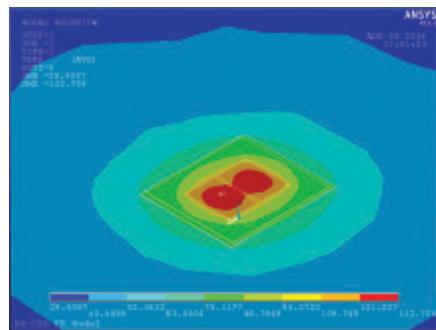


Figure 9: Thermal response in the neighborhood of an FOWLP device on the board (4L JEDEC board) with a Tmax on the chip of 132.895°C.

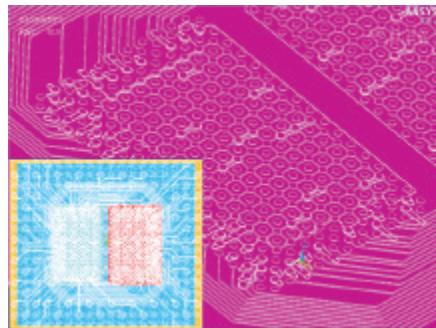


Figure 10: FE model with geometry outlines from ECAD.

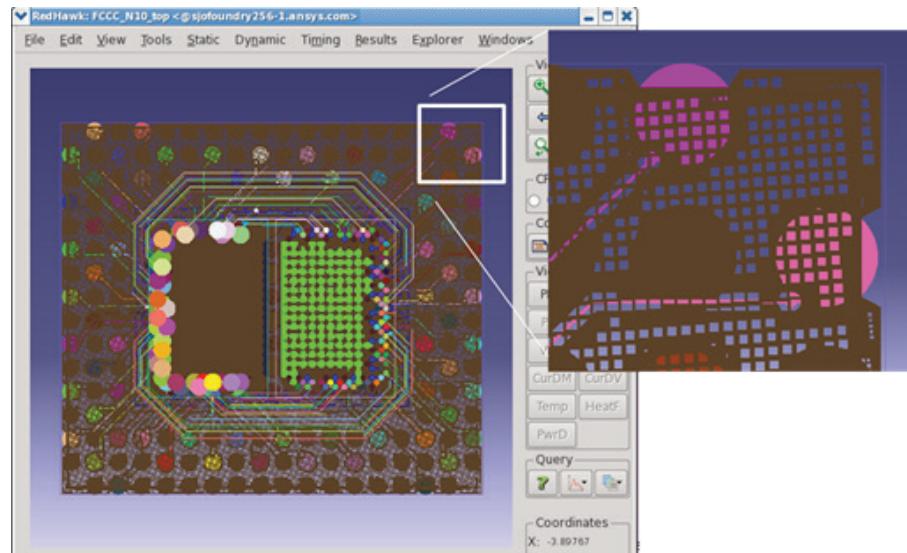
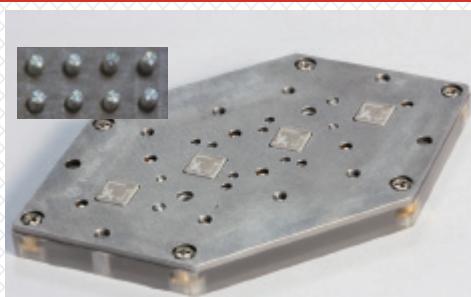


Figure 11: Degassing holes on PG nets.

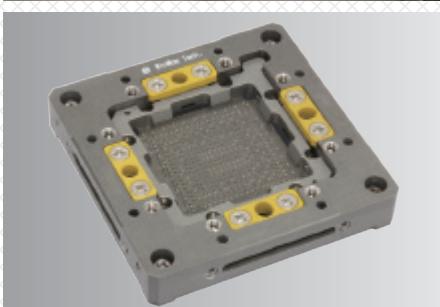
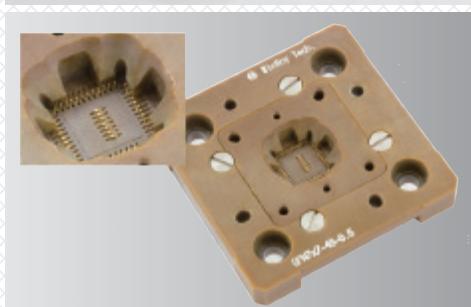
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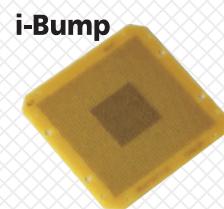


Figure 12 is the temperature profile on the top metal traces of the RDL, which

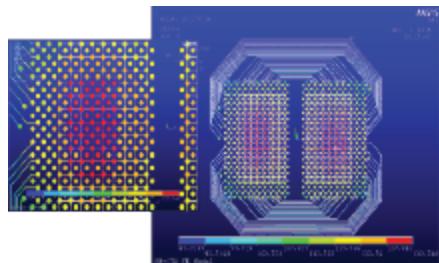


Figure 12: Temperature on the top metal layer and Cu contacts.

is connected to dies by Cu pillar contacts (small squares with equivalent areas to the contacts) at the center of the circular pads. The heat flux vector display in **Figure 13** shows the critical path in

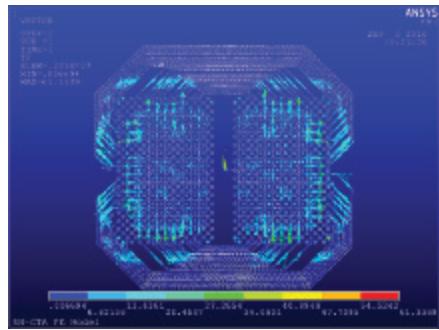


Figure 13: Heat flux on the top metal traces.

heat dissipation near the die. **Figure 14** shows the heat flux vector on Cu pads, which connects the dies to the RDL. It

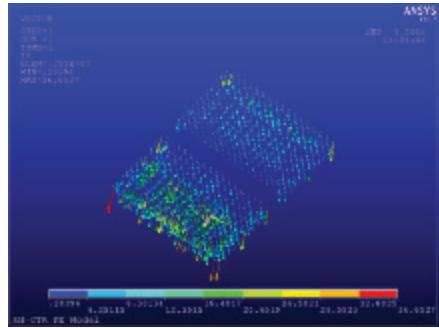


Figure 14: Heat flux vectors on Cu pads showing the heat flow distribution directly from the die to the RDL.

seems that the right die in **Figure 8** has a higher heat flux on the Cu contacts and the temperature is a little lower than the other one. This was unexpected as the design is in general symmetric. A review

of the model found that the materials filling the spaces under the two dies were not the same, which leads to the minor asymmetry for the thermal and stress results as discussed below. In FOWLP production, the filling material should be the molding compound. **Figure 15** is the heat flux vector plot of Cu pillars under the RDL into the thermal board underneath. Most of the heat dissipations are under the die footprints through the board, i.e., about 95% of all the power (~3W) from the chips.

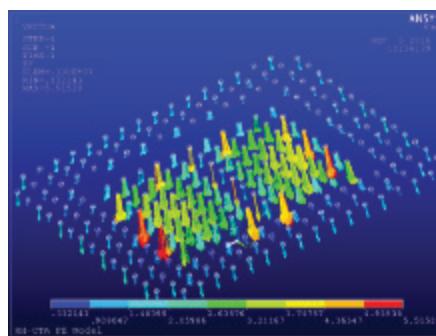


Figure 15: Heat flux on a Cu pillar under the RDL into the thermal board.

CPS thermal-stress modeling

The Tmax values on the chip are almost the same when solved in the chip-package thermal analysis (**Figure 8**) and in the structural analysis tool [7], which is also a thermal solver (**Figure 9**); only a negligible 0.022% difference was observed in this case. The temperature loading for the thermal-stress analysis can be either from the chip-package thermal analysis run or regenerated in the structural analysis software in the coupled thermal-stress analysis. When exporting to the thermal model from the thermal analysis, converged power maps were on the chips already—they were ready to rerun the thermal analysis in the structural tool. When exporting as a structural model from the chip-package thermal analysis tool, the existing thermal profile was automatically applied to all the FE nodes as thermal loads, ready to run the thermal-stress analysis.

For a thermal-stress analysis, the element type needs to be changed from thermal, e.g., SOLID70, to structural e.g., SOLID185. The material properties should be reviewed to include mechanical properties, e.g., E, v, and α (CTE). The typical structural boundary conditions are the nodal constraints to avoid rigid body

motion, i.e., large translation and rotation of the FOWLP+board structure. A script was generated to hold the top center of the molding between the dies against the rigid body motions.

Linear elastic properties are used in the thermal-stress analysis, assuming that the FOWLP on board is stress-free at room temperature of 20°C. The stress due to differential thermal expansion will build up in all components of FOWLP+board when the dies were powered with CTM at about 3W total.

Figure 16 is the warpage or Uz (Z displacement) contour of the FOWLP structure due to the power on. Again, the asymmetry of Uz was due to different α

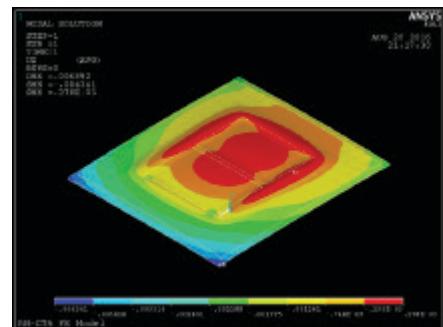


Figure 16: Warpage or Uz on top of the FOWLP device due to die power up.

and E in the underfill material surrounding the Cu contacts directly under the dies. There was about a 2.4x difference in α and a 2.35x difference in E. **Figure 17** is the Seqv (equivalent stress) on the top metal traces. The Seqv is mostly at an ~200MPa level and it could be acceptable given the

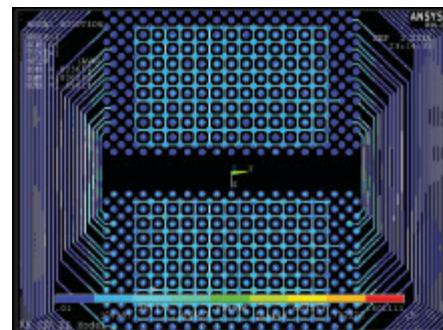


Figure 17: Seqv on the top metal mostly at ~200MPa level.

ultimate stress of copper wire at around 323MPa. For dielectric materials in the RDL, we could check on S1, the first principal stresses as the dielectric material

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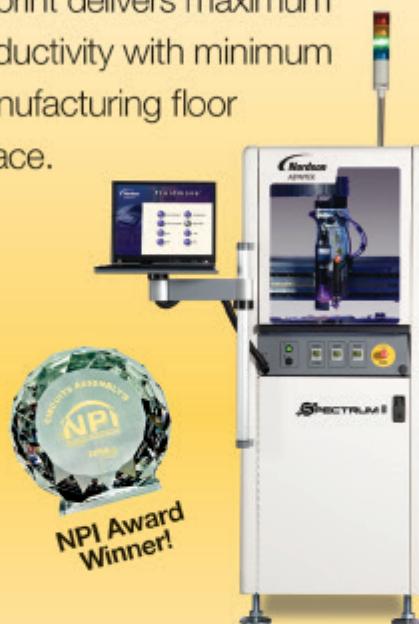
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could be brittle and fragile at a high tensile stress state. **Figure 18** is the S1 (tensile) contour of the dielectric material. The FE model for thermal stress has about 5.5M

α , of the dielectric material was smaller (12ppm/ $^{\circ}$ C) below a T_g of 100 $^{\circ}$ C and jumped to 30x above T_g (**Figure 20**). This analysis of FOWLP was using assumed material properties and only T_g in dielectric material is included and there were no changes in Young's modulus at T_g . For this nonlinear material property, multiple load steps were set up to monitor the development

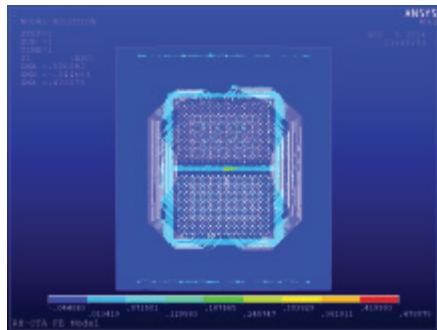


Figure 18: S1 in the dielectric materials in the RDL layers.

degrees of freedom (displacements on nodes) in the solution. The linear model took about 10min from matrix formulation to solution, using the same Linux server.

Warpage of FOWLP at reflow

When mounting an FOWLP device on a board at an elevated temperature ($>200^{\circ}$ C) to melt the solder material in a reflow oven, the FOWLP must remain flat so that all the connections by solder materials are in good condition. Assuming that the package is perfectly flat at room temperature (20 $^{\circ}$ C), when the temperature rises in the reflow oven, the FOWLP will deform on account of the differential thermal expansion of the molding, chips, RDL metal, and dielectric materials. One issue for temperature changes over a large range like reflow is the existence of the glass transition temperature (T_g) (**Figure 19**) in organic materials like molding and the dielectric in the RDL. For example, the thermal expansion coefficient,

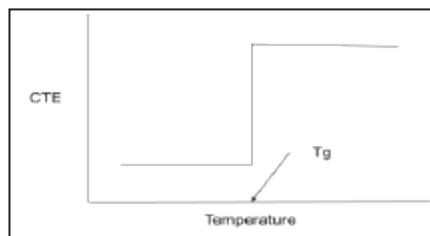


Figure 20: The significant CTE change at T_g used in the FOWLP study.

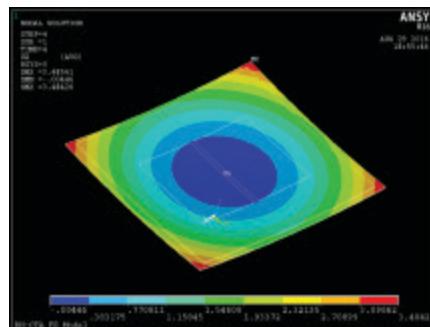


Figure 21: Warpage of the FOWLP and the contours of U_z .

of displacements and stresses as the temperature rises from 20 $^{\circ}$ C to 200 $^{\circ}$ C with $T_g=100^{\circ}$ C for the dielectric in the RDL.

Figure 21 is the warped FOWLP at 200 $^{\circ}$ C with contours of displacement in the Z direction showing significant uplift at the corners (3.48mm). The copper pillars under the RDL move 2.94mm vertically (**Figure 22**), which will fail the coplanarity check at reflow as the solder paste cannot fill the large gap at the corner joints. Further review of the materials used are needed by selecting the proper CTE and E. **Figure 23** shows that the glass transition effect shown at the end of step 2, which corresponds to $T_g=100^{\circ}$ C, and the significant rise of U_z from 100 $^{\circ}$ C to 200 $^{\circ}$ C, is due to high α in the material. The FE model (FOWLP package only) for

warpage with the T_g effect has about 3.3M degrees of freedom to solve. It took about 45 minutes to go through the four steps to the reflow temperature.

Chip Joule and self-heat modeling

In the area of chip design, the term of Joule heating is typically used for wires and self-heating is used for devices, especially for FinFET devices. The chips used in modern FOWLPs could be FinFET chips for increased device density and performance. The thermal approach used to analyze FinFETs will be discussed below.

The thermal analysis at the CPS level includes chips in FOWLPs as silicon blocks with a chip power map of the CTM. Though the tile size at 10 μ m in the CTM is already too fine for the CPS model, the power in each tile is still lumped from many front-end-of-line (FEOL) devices. For the previous nodes before FinFET devices, planar CMOS is relatively conductive compared to FinFET. A FinFET device has a 3D structure and is less conductive. Heat from a planar CMOS device is easier to spread out into the neighboring areas and dissipates away through the IDL and the silicon substrate to the FOWLP, i.e., the RDL, the molding, and the board, and eventually escapes into the air through thermal convection and radiation. The CPS thermal solution provides a good

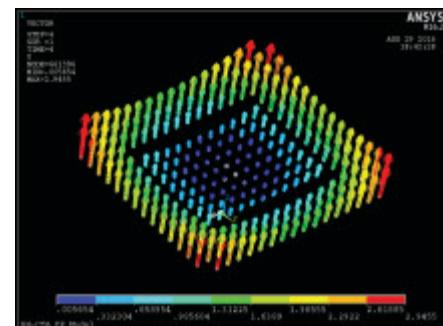


Figure 22: Displacements of copper pillars in FOWLP.

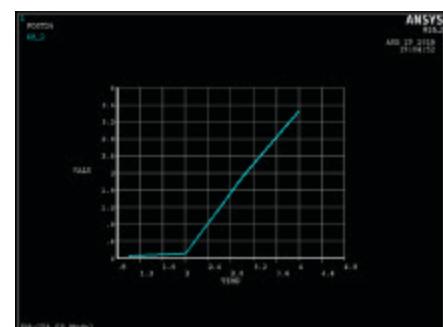


Figure 23: The U_z history plot showing the significant effect of high CTE change at $T_g = 100^{\circ}$ C.

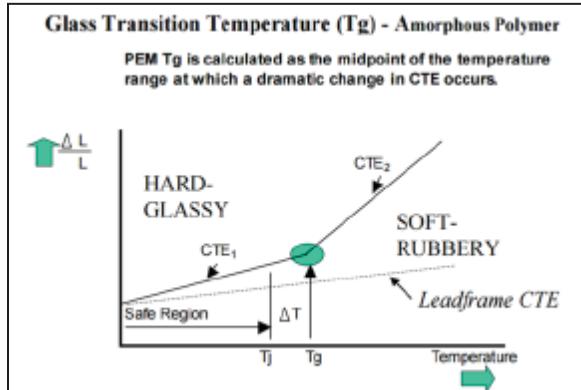
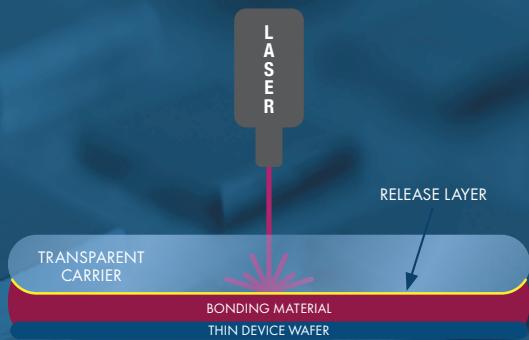


Figure 19: Sudden material CTE changes at T_g from hard glassy to soft rubbery.

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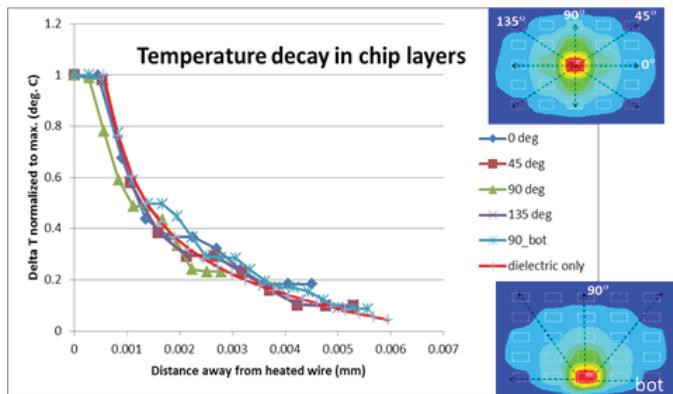


Figure 24: Wire temperature decay behavior [3].

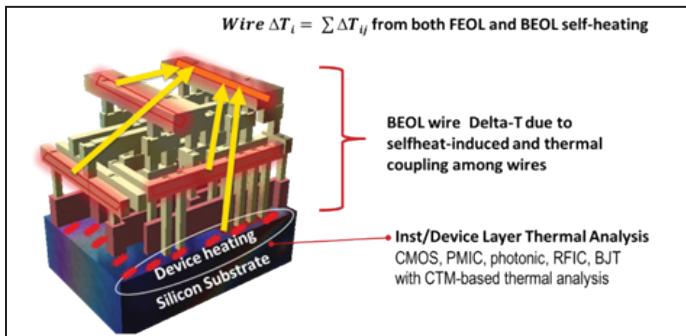


Figure 25: Thermal coupling due to self-heating on devices and wires [3].

approximation for Tmax – considering the overall power dissipation – and provides the operating temperature profile to all devices on the chip. The local heating effect inside the FinFET, however, cannot be covered by the macro-level modeling at the CPS level.

For chip designers, the high thermal resistance of a FinFET device is difficult to model and simulate using a field solution such as FEM because the details of the FinFET geometry, the fin/finger configurations and materials are determined by semiconductor foundries. Many foundries are now providing thermal resistance of standard cells or delta T of the FinFET devices based on measurements and/or simulations [9].

Temperature rises on wires embedded in IDLs in modern chip designs are expected to be higher than before because the wires are narrower in width and thinner in thickness, which makes the Joule heating effect more severe, in addition to the higher temperature impact from the FinFET architecture. Because the dielectric material surrounding the wires is of low thermal conductivity, e.g., typically 1W/mC as compared to ~130 of silicon, even with low Joule heating power, the delta T of the wire still will be significant, e.g., 3.3°C from 0.002mW on a wire segment of 22nm in width. While some foundries provided empirical formulas, this delta T on the wire can be simulated accurately using an FE sub-modeling technique. The influence of the Joule heating on a wire dies out over distance quickly. There is no need to consider the thermal coupling for wires more than 5μm away from the previous study (Figure 24) [3].

The thermal coupling from FEOL structures and neighboring wires will add to the delta T from the Joule heating of the wire and push the final wire temperature higher (Figure 25). Note that the final wire temperature could be calculated as the sum of the CPS temperature near the location on the chip and the delta T for the wire/device as described above.

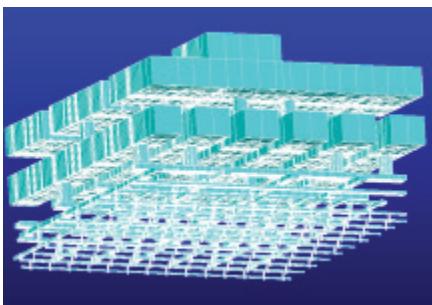


Figure 26: A sub-model with wires from the first metal layer to the 12th metal layer.

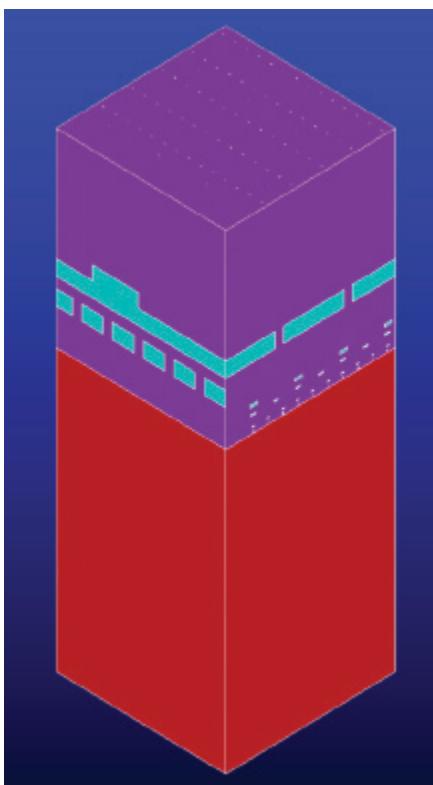


Figure 27: The complete chip sub-model including dielectric layers and silicon substrate.

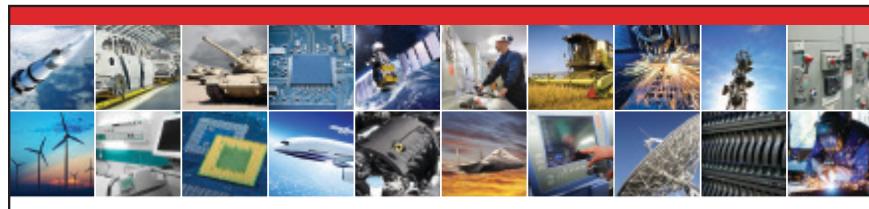
Chip sub-modeling for thermal and stress

While the full chip modeling with detailed wire layout is difficult to analyze by FEM, a smaller piece of the chip, such as the geometry in [Figure 25](#), can be modeled by FEM in an automated way. [Figure 26](#) shows the FE model of wires in a $10 \times 10 \mu\text{m}$ region of a chip in the FOWLP. In [Figure 27](#), the wires are embedded in low-k dielectric material (purple) and with the silicon substrate (red) at the bottom. From the previous study of delta T decay behavior, the range extending beyond the target wire of interest does not need to be much greater

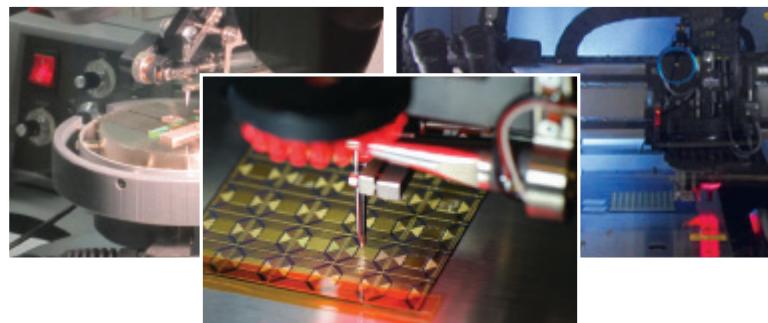
than $5 \mu\text{m}$ if the purpose of the analysis is to determine the thermal influence of the target wire to the neighboring wires. This FE model ([Figure 27](#)) has 368K nodes and 702K elements—not a very large model. For either thermal or structural analysis, the modeling range could still be extended and see good performance in the analysis.

The model was also used to test the capability of thermal stress on

the wires. The analysis was used to examine free thermal expansion with an environmental temperature rise of 120°C , e.g., from the CPS T profile. The model was held fixed at the top center to avoid rigid body motion. [Figure 28](#) is the resulting deformed shape and displacement contours that show more thermal expansion in the interconnection layers than in the silicon substrate. [Figure 29](#) shows the von



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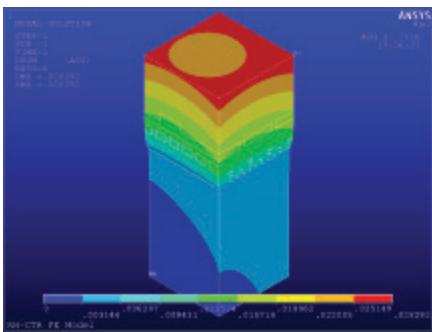


Figure 28: The deformed shape of free expansion with a temperature rise of 120°C.

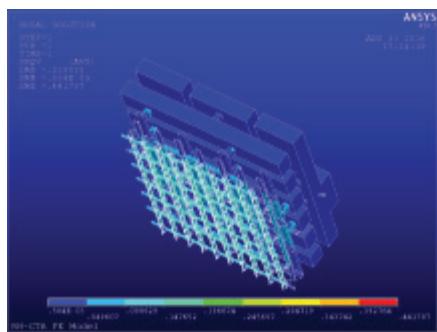


Figure 29: Equivalent stress on wires.

Mises equivalent stress on the wires. A zoom-in view (**Figure 30**) identifies that the higher stress is caused by shearing/bending on the vias of the bottom layers caused by differential thermal expansion. The

For thermal sub-modeling, the wire Joule heating power can be allocated to all the wires in the selected region (**Figure 31**). The power on the devices was based on chip power calculations

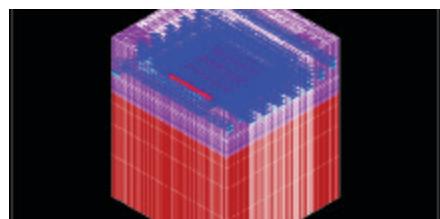


Figure 31: Joule heating power distribution on wires in the chip sub-model.

using chip power integrity tools [6] and was applied to the device areas. Alternatively, if the delta T of devices was available from the foundry, equivalent temperature loading could be used on devices in the sub-model. Then after analysis, the resulting thermal responses on wires can be retrieved (**Figure 32**) and back-annotated in the thermal-aware EM/IR analysis in the chip power integrity tools. As mentioned in the previous section, the Joule and self-heating effects with full BEOL/FEOL coupling are possible using the sub-modeling capability in the chip-package thermal analysis tool and the structural analysis tools.

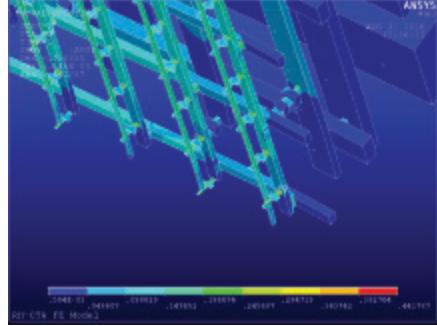


Figure 30: Zoomed-in view to show shear and bending stress on vias at the bottom layers caused by expansion relative to the silicon substrate.

maximum stress of 441MPa seems at the same level of the yielding or tensile strength of some copper alloys. The boundary condition of this stress sub-model, which allows free expansion, is not real as there are still adjacent structures to support it. The better solution is to use a cut-boundary in the CPS or warpage model to extract the boundary displacements surrounding the sub-model in FE tools in future studies.

modeling can help in verifying the Joule heating on wires, and the self-heating in FinFET structures, and therefore improve the reliability of chip designs.

Acknowledgments

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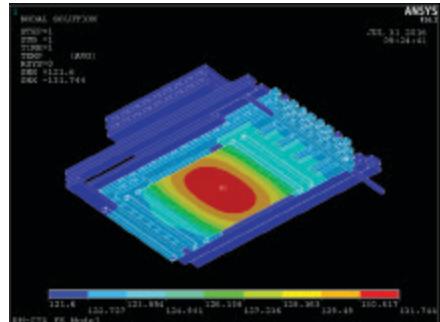


Figure 32: Temperature response in chip wires.

Summary

The methods of thermal-induced stress analysis of FOWLP structures were discussed using a sample case from the perspective of EDA tool calculations. Automation and ease-of-use is the top consideration in the flow development. Detailed outline modeling of FOWLP structures is emphasized as that would be the key to accurate thermal and stress results. Recent development of chip sub-

Multi-beam full cut of a molded wafer-level chip-scale package

By Richard Boulanger, Jeroen van Borkulo, Eric Tan [ASMPT Laser Separation International B.V.]

The introduction of chip-scale packaging (CSP) has recently become one of the key packaging solutions in the semiconductor industry. With the advantages of reducing the package size and stacking capability for higher interconnects, CSPs are continuously evolving into many different types of CSP packages. One of the key package solutions is the molded wafer-level CSP (mWLCSP) [1,2] that uses the robust 5-sided or 6-sided protection of the devices with epoxy mold compound (EMC). The advantages of this application include prevention of chipping and handling damage, sort screening capability because of its form factor at the wafer level, and the enhancement in board-level reliability [3]. The current singulation method – the mechanical blade dicing process – is encountering many challenges including yield loss, blade lifetime, productivity limitations, as well as its limitation to achieve a narrow kerf width. We report in this article on the multi-beam technology that addresses all the issues of blade dicing and, more importantly, enables a narrow dicing width while maintaining very good yield, reliability, and high productivity.

Introduction

The current standard separation technique used in the semiconductor industry is the blade dicing that has increased in complexity to fulfill the die separation requirements and specification of molded wafers. The demand for mWLCSP has experienced a significant growth because of the large demand in the advanced mobile phones and tablets technologies, wearable technology, and automotive markets. However, it has become clear that the requirements of these technology segments and the pressure of cost reduction have pushed the limits of the

capabilities of the current blade dicing technique until it is no longer able to meet the demands.

The challenging demands of mWLCSP technology require for it to have more dies per wafer and a smaller foot print of dies for higher integration. As a result, scribe lane design has to be narrower, and therefore, the blade dicing process no longer can achieve a narrow dicing width that allows a sufficient amount of mold compound to remain on the sidewall of the devices. In addition to these issues, blade dicing also encountered major issues with frequent exchange of narrow blade and re-alignment of wafers on account of the shortened life span of these blades. This shortened life span has been attributed to the blade that has lost its sharpness more frequently and the ability to prevent blade swing during the dicing process, especially for a very thin blade. The combination of these issues have led to yield loss during the singulation process and the complexity of realigning the wafer for every blade change. As the capabilities of conventional blade dicing have reached their limits of meeting mWLCSP specifications, the semiconductor industry is therefore looking into other solutions. Here we are introducing the laser dicing technology that breaks the limit of blade dicing while providing high yield and productivity [4]. Figure 1 illustrates the mWLCSP wafer and the position of the molded area that

the laser technique and the mechanical blade technique have to cut.

Multi-beam laser dicing solution

Our laser dicing technology utilizes the patented multi-beam technology that has been proven in various dicing applications and at various leaders of assembly and packaging companies to achieve high yield and reliability, high productivity, narrow kerf width, and a cost-effective dicing solution. All of these criteria are advantages over the traditional separation technique—the blade dicing technique that is currently used in the industry. Multi-beam laser dicing technology allows the distribution of the average laser power into uniform low-spot energy that can be used efficiently to achieve a narrow dicing width and for a mold compound thickness of up to 700 μm . This technique has an advantage over the standard single-beam laser dicing process in which the heat-affected zone (HAZ) that is usually attributed to a large amount of pulse energy being used is reduced, although the main contribution of HAZ is inherently attributed to the pulse duration [5,6]. The laser dicing system combines many specific process details that are crucial for the success of mWLCSP dicing.

Coating development for mWLCSP

The success behind the mWLCSP multi-beam laser dicing process is derived from overcoming several challenges that include meeting the dicing quality, the coating requirement, and the alignment requirement. Coating plays a significant role in the laser dicing process to protect the wafer from debris generated during the dicing process and it must be able to be washed away easily. The combination of mold compound surface and different types of bumps poses a challenge on the coating due to their different surface characteristics, including their surface tension parameters. These characteristics have contributed to the adhesion problem of a typical coating

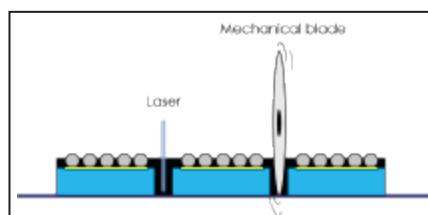


Figure 1: Illustration of laser and mechanical blade dicing of a 5-sided mWLCSP wafer.

formulation that resulted in inadequate coverage of coating across the wafer, and therefore, contamination occurs along the dicing lane that cannot be washed away as shown in **Figures 2a–b**.

Significant improvement has been made to incorporate an effective coating that is able to protect both the wafers and the bumps from debris. Different coatings have been tested, and in-house formulation process developments resulted in a coating that is capable of providing a homogeneous film across the wafers. The formulated coating improves the adhesion of the coating onto the molded wafer by resolving the competing surface energies between the coating and the substrate. The new coating, therefore, adheres very well to the surface of the molded wafer. This coating has been observed to be effective on several types of molded wafers that have been molded by different EMC suppliers. As a result, the diced mWLCSP wafer is free from contamination attributed to its robustness—it not only has full coating coverage across the wafer, but it also has resistance to heat and prevents coating delamination. The advantages of the coating on mWLCSP are shown in **Figures 2c–d**.

Alignment capability for mWLCSP

The choice of device protection with EMC can be either the 5-sided or the 6-sided EMC encapsulation as shown in

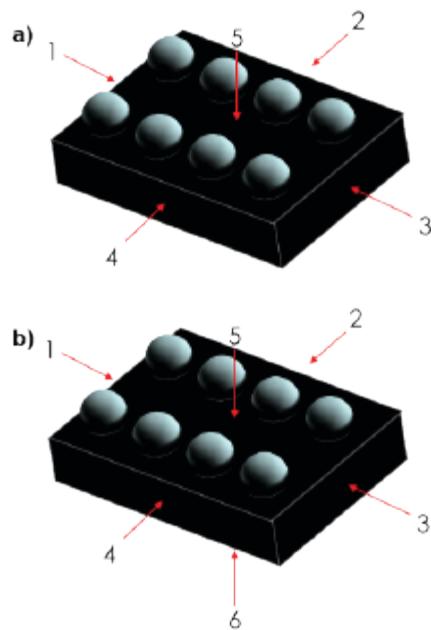


Figure 3: a) A drawing to show 5-sided EMC encapsulation on a die; and b) A drawing to show 6-sided EMC encapsulation on a die.

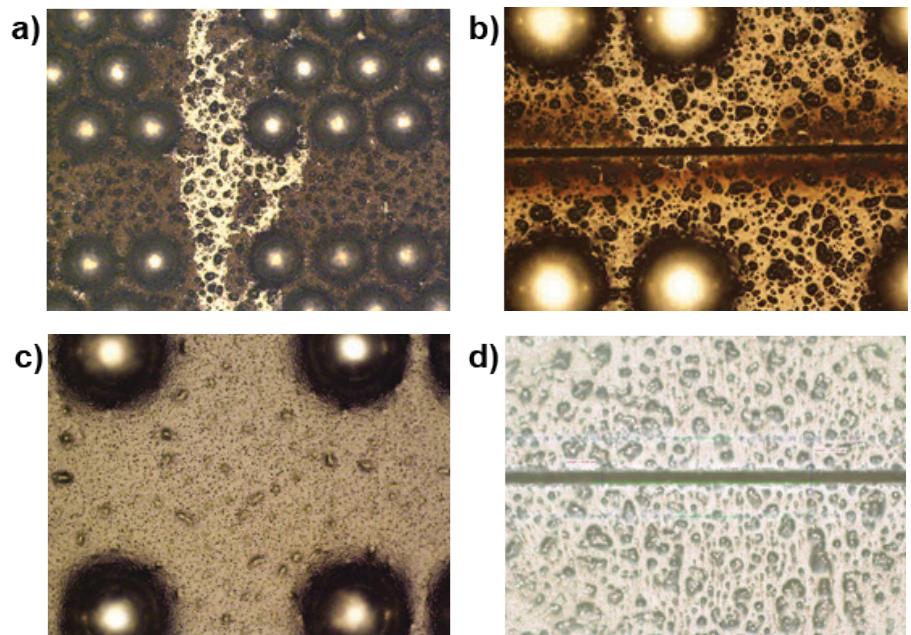


Figure 2: a-b) The disadvantages observed from an uncoated mWLCSP wafer; and c-d) The advantages observed from a coated mWLCSP wafer.

Figures 3a and 3b. It is dependent on the requirements of the device to endure handling damage during the assembly process. This design and process of the mWLCSP has raised a crucial need for developing a new alignment capability to enable accurate positioning of the laser beam position for the cutting process. It is clear that the alignment based on the bumps positions is not accurate for the laser beam to cut in the center of the half-cut as the half-cut made prior to the molding process has at least a $\geq 4\mu\text{m}$ positioning error relative to the bumps placement. The consequences of this error are large and can contribute to off-centered dicing, which eventually results in delamination of the mold compound from the sidewall of the silicon. This inherent inaccuracy of the half-cut made has to be resolved with exposure of the edges of the mWLCSP to allow for inspection of every half-cut lane.

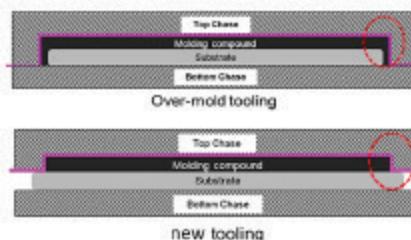


Figure 4: Drawings to show the difference between the over-mold tooling and the new tooling.

The exposure of the edges of the molded wafer can be done with two methods. The first method can be performed by using the unique compression molding process with our molding tool to free up the edge depending on the desired width as shown in **Figure 4**. Instead of applying an over-molding process that covers the whole wafer up to the wafer edge [7], the new tooling is capable of restricting the EMC to reach the edge of the wafer. The second method is to perform mechanical trimming on the edge of the wafer that has been over-molded with the standard molding process. Therefore, in both of these methods, the half-cut lanes are exposed for the alignment prior to the dicing process. In comparing the two methods, the advantage of having the first method is to reduce the additional process step and cost of mechanical trimming around the edge that can induce stress on the wafer because of its mechanical pressure. This situation, however, is typically undesirable for very sensitive and brittle devices.

Edge alignment for the mWLCSP dicing process

The multi-beam laser dicing machine is able to support either of the two methods described above by incorporating a patented alignment methodology to

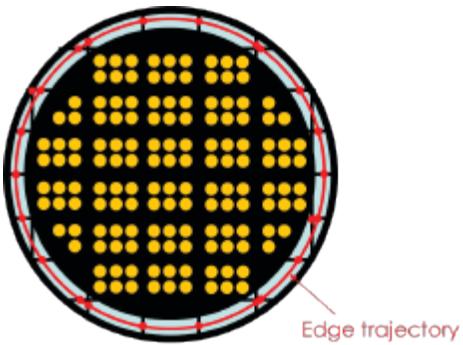


Figure 5: A schematic illustrating the wafer edge circular trajectory to align on all exposed critical lanes.

achieve the high accuracy required for dicing. This methodology makes a circular trajectory around the wafer edge to inspect and to align on all exposed critical lanes as shown in **Figure 5**. Every lane is inspected to determine the position where the laser beam has to be placed.

The inspections are done with very complex and accurate algorithms while maintaining a high overall throughput. Inspection of the lane is followed by a decorated image of the half-cut lane as shown in **Figure 6**. These images of all lanes are stored for tracking and analysis for manufacturing traceability. In addition, re-checking of the lanes can be triggered to validate the accuracy of the lane alignment prior to the dicing process, thereby ensuring a full-proof solution to prevent inaccurate dicing. Many of the functionalities of the edge alignment rely on very specific hardware configurations and software complexity to support the dicing system to seamlessly handle and align many types of wafers.

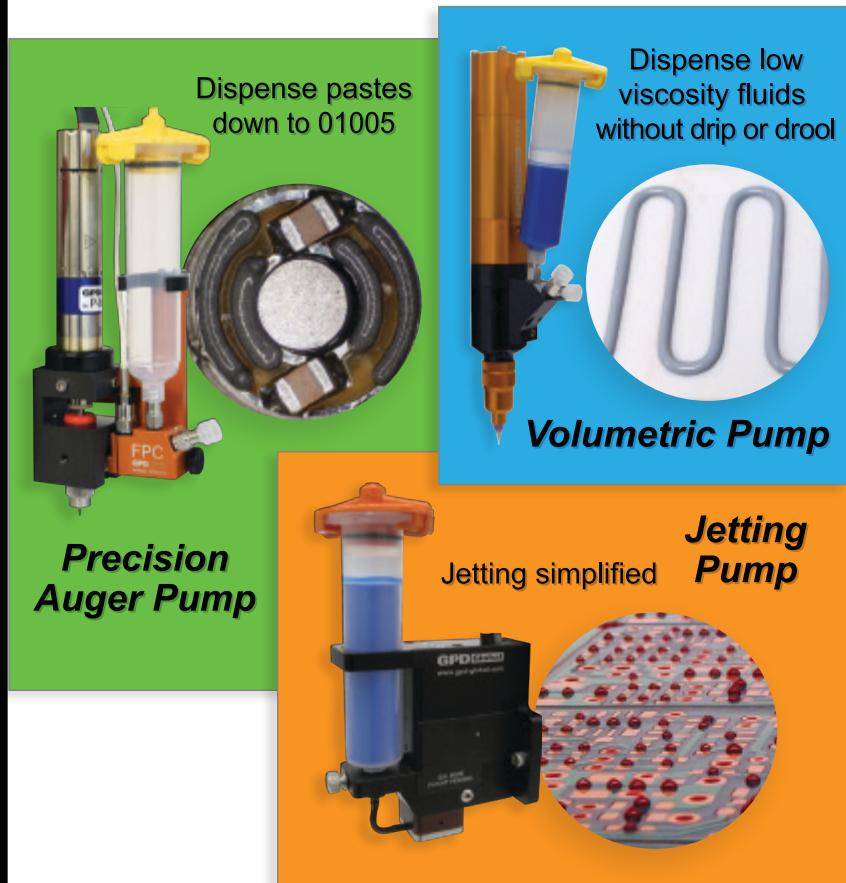
Results of the evaluation

A number of results came out of the evaluation of mWLCSP as described below.

Top dicing width and bottom dicing width. The multi-beam laser dicing technology has demonstrated the capability of dicing several applications with thickness between 180 μm up to a 700 μm thick mold compound. This technology is the current enabler for the mWLCSP application, which has set many stringent requirements that are difficult for some standard dicing methods to achieve. The multi-beam dicing technology has achieved very good dicing qualities that can be assessed in several assessments that will be described in this paper. Several typical assessments include the top dicing width, back dicing width, productivity,

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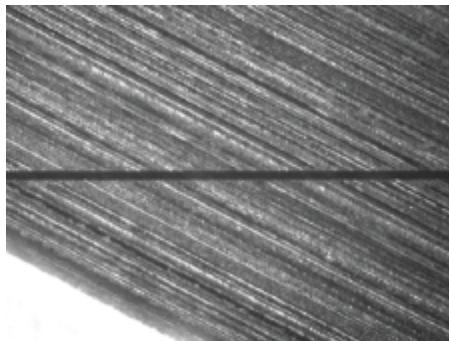


Figure 6: Example of an edge lane detection with a complex and accurate algorithm.

smoothness of sidewall, dicing profile, and accuracy of beam positioning.

Figure 7 shows the top dicing width of a fully separated 380 μm -thick mold compound wafer. This is a significant improvement over the blade dicing that can only achieve a dicing width of 25 μm . In this application, burr that is typically generated during dicing is not detectable and the debris due to the dicing process can be easily washed away together with the coating that was spin-casted prior to dicing. The achieved results of a narrow dicing width and reduced HAZ with the multi-beam technology, therefore, allows

for the reduction of the scribe lane design from a width of 80 μm to 65 μm in order to achieve more dies per wafer. In particular, a greater advantage can be observed especially for very small dies that primarily dominate the discrete devices segment.

The other critical criteria for assessing good dicing quality is determined by the bottom dicing width for a 5-sided mWLCSP wafer. **Figure 8** shows the remaining mold compound material along the edges of the silicon that is up to 14 μm on each sidewall of the silicon. The width of the remaining mold compound is at least 3 times more

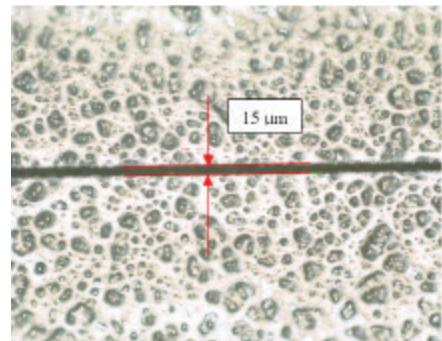
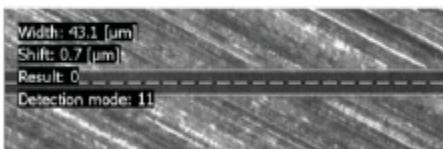


Figure 7: Top dicing width of the mold compound wafer.

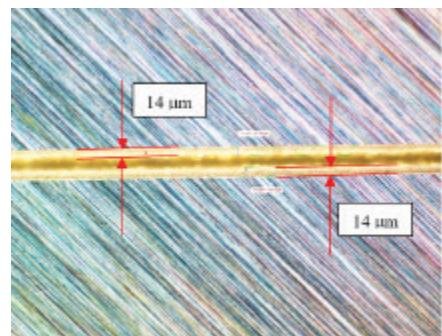


Figure 8: Dicing width of the mold compound wafer observed from the back of the 5-sided mWLCSP wafer.

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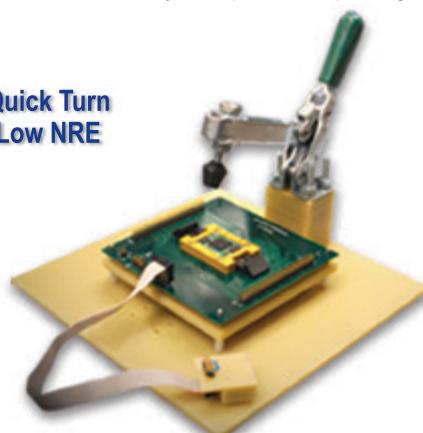
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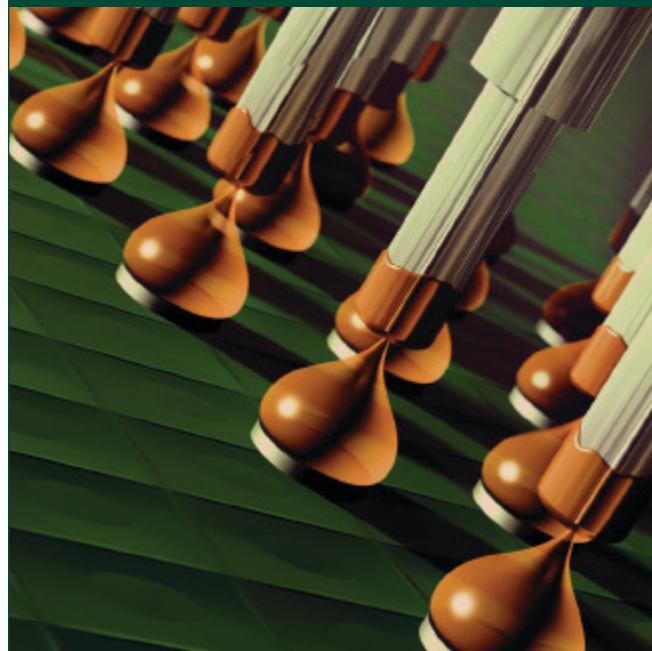


Figure 9: Mold compound remaining around the silicon as shown at the corner of a singulated die.

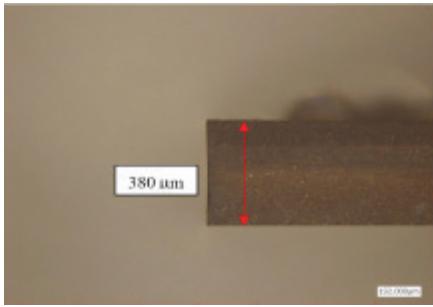


Figure 10: Sidewall of the remaining mold compound and dicing profile at the edge.

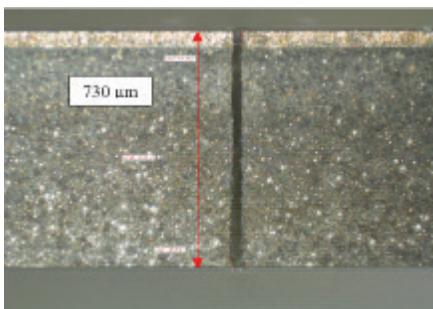


Figure 11: Sidewall of the cut and the dicing profile.

wafer has to rely entirely on the exposure of the trimmed edge and the accurate edge alignment method prior to the dicing process.

Sidewall surface roughness and cut profile. Inspection of the sidewall with an optical microscope as shown in **Figure 10** and **Figure 11** revealed the dicing quality, especially the smoothness of the sidewall and close to zero taper for the cut profile. The zero taper that is observed for the cut profile is definitely a huge improvement on quality because it is hugely dependent on the thickness of the material. **Figure 11** illustrates the capability of the multi-beam dicing process to achieve a close to zero taper for a 730µm-thick mWLCSP material. The confocal microscope image shown in **Figure 12** demonstrates an average smoothness of the sidewall of $\leq 2-3\mu\text{m}$ that is important for space-constrained integration typically required in mobile devices.

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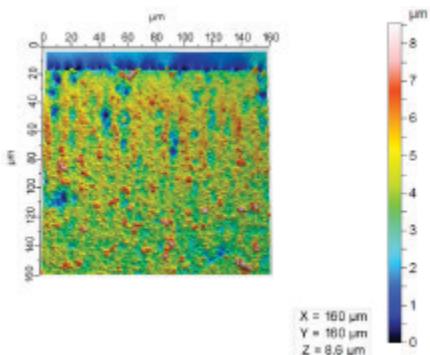


Figure 12: Confocal image of the sidewall.

More importantly, the straightness of the cut is significantly better than the profile of the cut made by a mechanical blade, which can typically produce a slant cut on account of the wear and tear of the diamond blade.

Multi-beam dicing productivity. It has been validated that the productivity of the multi-beam technology is up to 2.5 wafers per hour. That is a 5x increase in productivity compared to conventional blade dicing. **Figure 13** shows the comparison of the calculated productivity for a 300mm wafer with a die pitch of 2500 μm x 2500 μm . The significant gain in productivity lies on the multi-beam technology that allows the user to fully utilize the potential of the average laser power and to achieve high quality and reduced HAZ. Besides, the configuration of the slider technology incorporates an efficient acceleration and speed that outperforms many sliders in its category.

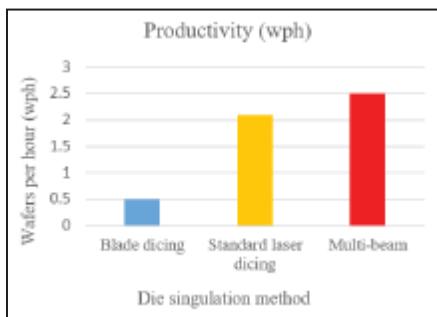


Figure 13: A comparison of productivity between conventional blade dicing, standard laser dicing, and the multi-beam dicing technology.

Summary

With great demand from mWLCSP in various sectors of the semiconductor and electronics industry, especially the mobile segment, the multi-beam laser dicing technology is the solution for the die separation process because blade dicing technology no longer can meet the critical requirements of singulation of

mWLCSP materials. Multi-beam laser dicing technology can achieve a dicing width of $\leq 15\mu\text{m}$ for a 380 μm -thick wafer and a dicing width of $\leq 40\mu\text{m}$ for a 730 μm -thick wafer. The combined patented multi-beam dicing technology and patented alignment methodology not only ensure a narrow dicing width, but also ensures that a substantial equal amount of mold compound remains, which is essential to achieve higher yield and package reliability. The mold compound remaining for a 5-sided mWLCSP is at least 14 μm , which is a factor of 3 times more than the standard mechanical blade dicing process. The result of a narrow dicing width with an equal amount of mold remaining on each sidewall can only be reconciled with the new dicing and alignment methodology we have described that ensures an accuracy of up to 1.5 μm . This patented alignment methodology is capable of providing the solution for the 5-sided encapsulation and can also be extended to the more stringent 6-sided encapsulation. The dicing quality of the multi-beam method is further substantiated by the inspection on the sidewall of the diced material. Essentially, the cut profile has close to a zero taper that is typically hard to achieve for a thick material, while the average smoothness of the sidewall is $\leq 3\mu\text{m}$. This value is typically dependent on the size of the fillers that comprise the EMC material. The benefit of the multi-beam dicing system is highly suitable for the manufacturing environment as the system excels in both quality and productivity. The productivity of the system is at least 5 times more than the standard blade dicing system and with huge improvement on the dicing quality. The combined advantages can justify the effective cost-of-ownership for part of the mWLCSP manufacturing. The advantages of multi-beam dicing can be extended with the in-house formulated coating that also ensures that the wafers and bumps will be free of contamination from the debris generated in the dicing process.

Acknowledgements

The authors would like to thank each of the ASMPT members who were involved in the mWLCSP dicing project—in particular, Dr. Guido Knippels, Geert Ubink, Kees-Jan Leliveld, Dr. Jian-Fei Yang, Ralf Noijen, Albert Koeling, and Alexander de Groot, for the edge alignment software and system support. The authors would also like to acknowledge Martien Kok, Peter Dijkstra and Dr. Eric Kuah for the various technical inputs and supports throughout the project. In addition, we would also like to acknowledge Dr. Rogier Evertsen, Mark Mueller, and Won-Chul Jung for the coating

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TSV package architectures and trade-offs

By Paul Silvestri, Rama Alapati, Mike Kelly [Amkor Technology, Inc.]

The proliferation of connected devices is driving system requirements for smaller form factor, higher data transfer rates, improved signal integrity, higher memory bandwidth, and/or increased thermal performance. The problem is technology scaling limitations present a cost barrier to traditional semiconductor die shrinks and device integration using 2D packaging techniques. Through-silicon via (TSV) packaging technology provides a solution and enables homogenous and heterogeneous integration of logic and memory co-located closely together in a small form factor assembly. Concurrently, high-density signal routing and very high bump counts are driving line and space widths with very fine-pitch interconnects using copper pillar technology on interposers.

Choices for TSV

Combined with the appropriate wafer bumping technology and advanced packaging, TSV interconnects enable very high-density I/O so application-specific integrated circuits (ASIC) and memory die can be located near each other on a TSV silicon interposer. This integration scheme is called 2.5D TSV. Additionally, silicon layers can be stacked tier-to-tier on top of each other, which reduces the physical area allocated for each component. This tier-to-tier stacking is called 3D TSV technology. In the dynamic random access memory (DRAM) space, 3D TSV has been deployed in both high-bandwidth memory (HBM) and 3DS-DDR 4. By combining the two TSV technologies into a flip-chip ball grid array (FCBGA) assembly, systems with high-bandwidth and low-power per bit transferred and high memory density are realized.

A 2.5D assembly process can be achieved through either wafer-level or substrate-level integration. The decision to use one method or the other requires a comparison of the process flow. In general, architects should trade off test coverage vs. repair capability at the ASIC design level. Because automated test equipment (ATE) platforms are much more flexible for substrate technology rather

than wafer technology, assembly integration that starts at the substrate level (chip-on-substrate, or CoS) will readily enable flexible test solutions early in the assembly flow.

In contrast, an assembly methodology that begins with a wafer (chip-on-wafer, or CoW) will require full population of top die and completion of the wafer processing plus assembly to a printed circuit board (PCB) before suitable testing can begin. This “dies first” strategy of placing the top die (logic + logic or logic + memory) to the interposer while in wafer form (CoW) can become a very high-cost process if redundancy methods and post-assembly die repair schemes are not deployed in the architecture to manage yield loss. Assembly methods such as chip-on-substrate and hybrid forms of CoW + CoS (partial chip-on-wafer flows) are very attractive solutions where die yield, cost, and test strategy are crucial to a device’s economic viability.

TSV assembly technologies

To address the changing market requirements, multiple 2.5D TSV

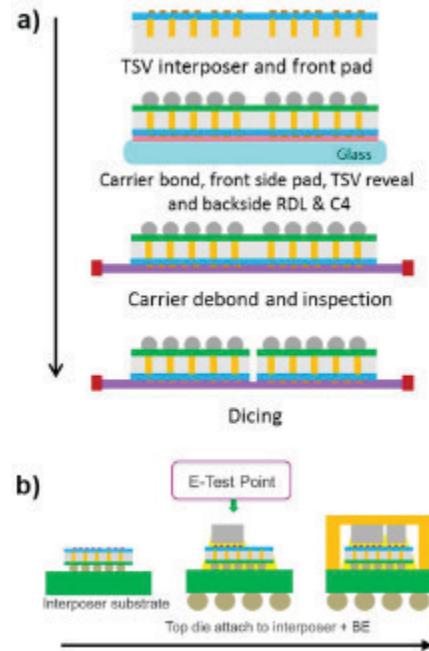


Figure 1: a) The MEOL process flow; and b) assembly process flow with interim test for CoS packaging.

technologies have been developed and commercialized. At Amkor, a 2.5D TSV CoS process has been in production for several years and the CoW process is being qualified in 2016. The process flow details of each of these approaches are shown in **Figure 1** and **Figure 2**. The TSV process flow starts with middle-end-of-line (MEOL) processing to expose the TSVs and metallize the front and back of the wafers to form the interconnects.

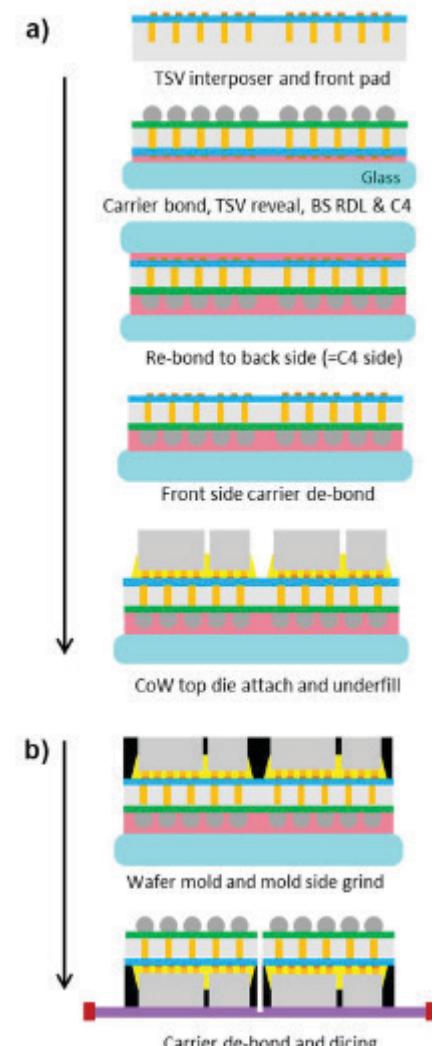


Figure 2: a) MEOL process flow and die attach; and b) wafer finish option of molded wafer format for CoW packaging.

Figure 1, 2 and **3** show three major assembly techniques. The choice of the appropriate TSV technology to use depends on the size of the interposer and number of component dies attached to it. Designers need to understand the nuances between these approaches including the advantages and disadvantages of each. In most cases, TSV processing whether it is CoS, CoW or even 3D TSV for memory has essentially the same basic approach on the wafer side: the foundry processes the TSVs that do not go all the way

through. The outsourced semiconductor and test supplier (OSAT) receives the wafer with the TSVs and then processes both the front and back side to expose the TSVs and bump the wafers. **Figure 1a** and **Figure 2a** show the MEOL processing. The CoW approach adds a carrier flip (**Figure 2b**) to present the interposer front-side for top die assembly.

Interposers for 2.5D are designed to enable side-by-side die interconnects. As a result, interposer die sizes are large, sometimes larger than the reticle size. As such, 2.5D TSVs are

deeper in the silicon, generally 100 μm deep. During the MEOL process, more bulk silicon will remain, which increases the die resistance to warpage.

In contrast, 3D TSV integration is generally integrated in DRAM with small die area. The 3D TSVs are integrated at 50 μm deep, making the die more sensitive to warpage. HBM is built using CoW molded style assembly

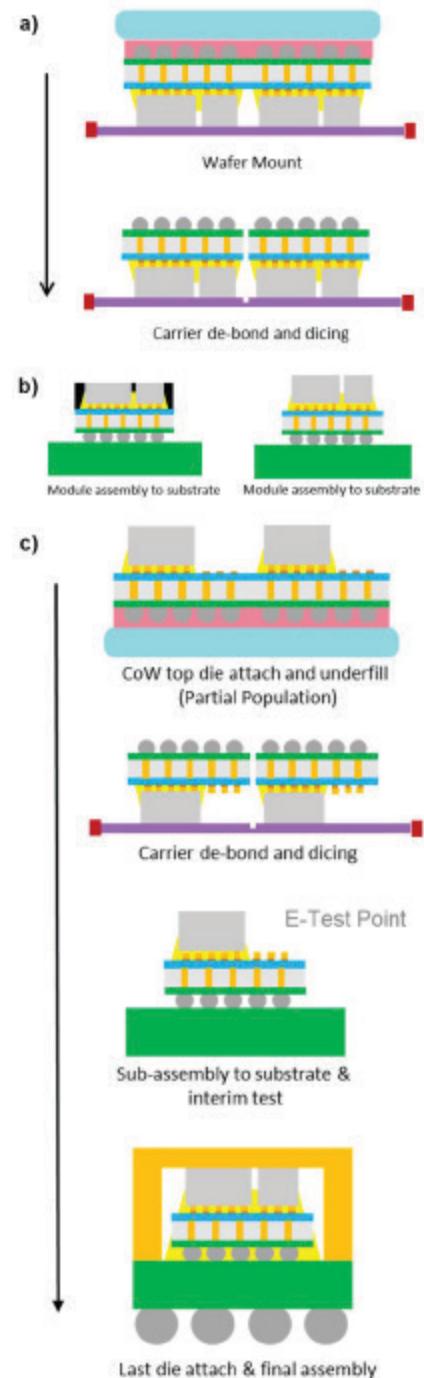


Figure 3: a) Wafer finish option of no-mold wafer for CoW; b) CoW module assembly – molded and no-mold module; c) CoW + CoS hybrid flow with eTest.

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technology, which does limit the test coverage available because the memory cube can only be tested while in wafer form. Because HBM test coverage is reduced, it is desirable for 2.5D assembly integration to consider assembly methods that can enable test before HBM cubes are committed to the assembly.

With a CoW molded style assembly, all interposer die sites must be populated before wafer molding. The problem with wafer-level testing is it can only be performed at wafer test sites that are typically limited to how fast the vectors can be run, and parallelism, and even temperature can be problematic. In contrast, on a substrate using a handler and some form of automation, much higher volume testing can occur with much better test vectors, more I/O on the test board, and more. This provides much more efficient testing at the substrate level. For many customers, this is the right approach today.

The flow that is the most flexible and low cost is CoS because the location in assembly where the top die has to be committed is late in the flow. **Figure 1b** shows the E test point where acceptable or unacceptable product is identified. A multiple die design frequently has two, three, four, or five dice that sit on top of a very large interposer. The die can be very expensive if it uses 7 or even 14 or 16nm technology, or even the HBM device itself. If there is an issue with the assembly, committing the die in a CoW process without testing them can potentially result in the loss of many other die. This is where the avoidable expense occurs.

CoS allows an OSAT supplier to perform interim tests prior to committing the other top die that could be a logic layer or memory. With the current cost of HBM, there is a lot of interest in placing die on a tested substrate. However, the thinned interposer will assume the substrate warpage characteristics once assembly to the PCB is completed, making assembly of the top die to the interposer difficult if warpage is not managed. CoS assembly can be a suitable solution for interposer designs up to the reticle size. Because of the coupling of the interposer and PCB, the PCB design and materials selection must be carefully selected.

In other cases, CoW can offer a desirable solution. Again, there are advantages and disadvantages. In the Cow approach shown in **Figures 2a** and **2b**, the difference occurs when the wafer is flipped (**Figure 2b** bottom) to expose the front side of the interposer to place the die. Because the wafer warpage is managed by the carrier, the front side of the interposer wafer remains flat and subsequent die placement is not sensitive to warpage. This enables very large interposer designs with

fewer constraints on PCB selection. During wafer assembly, all top die must be populated before wafer molding starts.

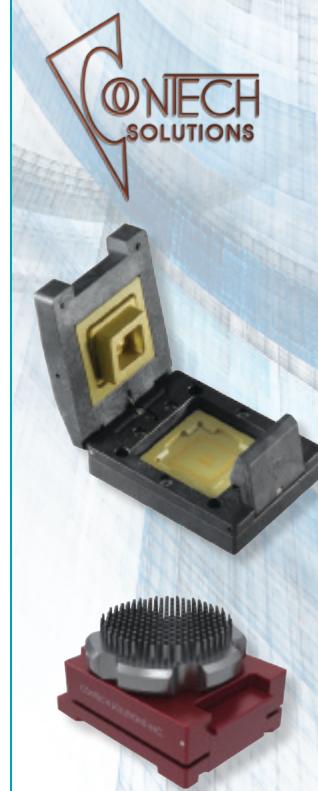
CoW process flexibility is shown in **Figure 2b** with a mold and **Figure 3a** with a non-mold process flow. **Figure 3b** shows a side-by-side comparison of the module assemblies. Typically, the industry is pursuing the molded process flow. In the over-mold flow, everything is locked in place after molding. After assembly and wafer molding, the module is mechanically diced from the interposer wafer and placed on the PCB. Test can then be performed at that point to check functionality and perform any post-package repair. A defect that is not repairable or recoverable through design redundancy (redundant TSVs) or other external means (such as remapping I/O) is lost and a very large and expensive top die (ASIC and HBM) is scrapped.

The mold compound's mechanical properties dictate the use of less mold material to reduce stresses on the interposer die and the adjacent top die. This is accomplished by keeping the die-to-die spacing very tight (<100µm) and minimizing all unused interposer die area that would be exposed to the mold compound. The resulting design rule requires any top die (ASIC and/or memory) to be similar in size such that the interposer floor plan to minimize the interposer size. CoW molded is a good platform for logic + logic integration where the logic dies are the same size. Additionally, the wafer dicing step must use mechanical dicing methodology in order to accurately dice through the mold and silicon interposer. This requires a sufficiently large dicing lane to allow for singulation. FPGAs are an excellent example of CoW-molded integration.

In the CoW no-mold path, an interim test flow (**Figure 3c**, middle) is supported. Die size alignment is not design rule-limited because mold compound is not used in this platform. Furthermore, stealth dicing of the interposer is possible, which could reduce the interposer dicing street width. Because the wafer will not be over-molded, every die site on the interposer does not need to be populated. This feature allows for interim test options, either at the wafer level or at substrate level. In this process, the partially populated wafer is put onto a substrate so it can be tested similar to a CoS and then the remaining dice are added later. This hybrid chip-on-wafer process is an attractive flow for heterogeneous 2.5D top die integration that does not limit the top die size synchronization. It is a combination of CoW and CoS.

With the variations discussed above, there are interesting tradeoffs. CoS provides the most flexibility. The CoW molded flow has the least flexibility. However, there are two process flows between these extremes. One is the CoW no mold. While it is not as aggressive, it can be modified to perform the hybrid process that combines the best of CoS and CoW.

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Table 1 shows a quick high-level summary of several high-level design considerations. There are more criteria depending on the application and specific customer constraints, such as improved system performance, or high performance at relatively low energy dissipation as measured by bandwidth per unit of energy expended, thermal performance, or others.

TSV solutions

With TSVs commonly accepted as a solution for advanced IC packaging and several TSV processes available, today's design decisions focus on identifying the right implementation for specific applications. To make the correct choice, there are several design considerations and tradeoffs. Today's 2.5D TSV solutions enable new power and form factor efficient systems. As a result, many leading original equipment manufacturers (OEM) of semiconductors have taken advantage of their flexibility and ability to achieve performance and cost goals. While 2.5D technology has matured, significant effort is underway to scale the technology to enable faster and more efficient systems. At the same time,

TSV Assembly Process	Interim Test	Interposer Size Support	Die to Die Spacing	Interposer Whitespace	Interposer Dicing	Application
Chip on Substrate [CoS]	Yes	< Reticle Size	Largest for Interim Test; Variable OK Otherwise	Top Die can be any size	Stealth	Logic + Logic; Logic + Memory
Chip on Wafer [CoW] Molded	No	> Reticle Size	Minimum required	Top Die should be balanced	Mechanical	Logic + Logic
Chip on Wafer [CoW] Non Molded	No	> Reticle Size	Variable	Top Die can be any size	Stealth	Logic + Logic; Logic + Memory
Chip on Wafer [CoW] Hybrid	Yes	> Reticle Size	Largest for Interim Test; Variable OK Otherwise	Top Die can be any size	Stealth	Logic + Logic; Logic + Memory

Table 1: TSV processes and attributes comparison.

much of the effort for 2.5D is applicable to 3D packages that will provide even further performance and system advantages. With these and other process variations, different customers have the flexibility to choose the process that meets their specific needs.

Biographies

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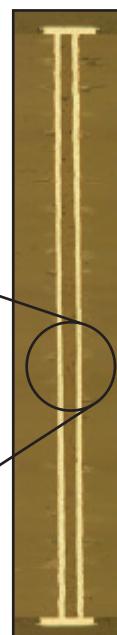
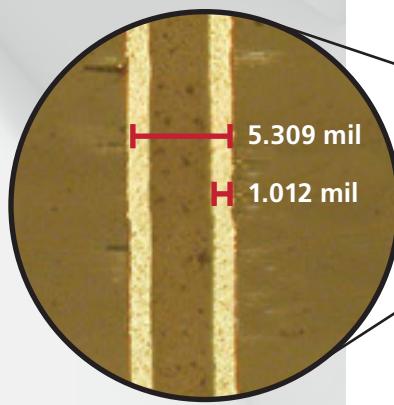
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Photoresist strip using advanced single-wafer process technology

By Laura Mauer, Scott Kroeger [Veeco Precision Surface Processing], and Amy Lujan [SavanSys Solutions]

Photoresist strip is a key lithography step in many electronics packaging process flows. There are a variety of photoresists and processes available depending on the lithography requirements. In addition, there are different methods for stripping the negative dry film photoresist that is typically used for advanced packaging applications.

The focus of this analysis is the Veeco Precision Surface Processing WaferStorm® tool featuring ImmJET™ high-performance immersion and single-wafer spray process technology. The tool and chemistry are introduced, along with a cost analysis of the key variables of the strip process. The cost modeling portion, conducted by SavanSys Solutions LLC, includes a comparison of the Veeco tool to other available processes, such as batch immersion and spray tools.

The approach to understanding the cost elements associated with each technology is activity-based cost modeling. In this methodology, a process flow is broken down into activities, and the cost components of each activity—including labor, material, capital, tooling, and yield—are analyzed. The goal of this analysis is to evaluate the ImmJET technology, and to understand the key cost drivers associated with photoresist strip.

Background

A thick photoresist pattern is required for the formation of tall bump structures, shown in **Figure 1**. Dry film resist provides the advantage of uniform resist thickness across the entire wafer, eliminating the need to do multiple coatings and edge bead removal. However, since these are negative working polymers, they are highly cross-linked and more challenging to remove. The complete removal of the film and cleaning of the surface is critical to the yield of the next step, which is etching of the underlying metal seed layers.

A successful process results from the proper choice of tool technology, solvent, and process to completely remove the dry film without any residuals that would block subsequent etching. Wet benches are commonly used for photoresist stripping

processes. A batch of wafers is loaded into an immersion station with heated chemistry for a long soak. Typical wet-bench configurations include multiple soak tanks. The first immersion station is the “dirty” tank where the bulk of the resist saturates the solvent. The second tank typically involves a “cleaner” solvent process after which the

wafers are transferred to a final rinse tank before drying. Single-wafer spray systems have also been used as an alternative to batch processes. However, the length of time for the spray process is quite long for these highly cross-linked dry film resists and, though this process can be effective at removing the resists, the cost-of-ownership is too high to be feasible in a high-volume manufacturing process. Here, we present a new high-performance immersion and spray process technology, called ImmJET, which combines an optimized immersion step and single-wafer spray process to produce high-yield results at a low cost-of-ownership.

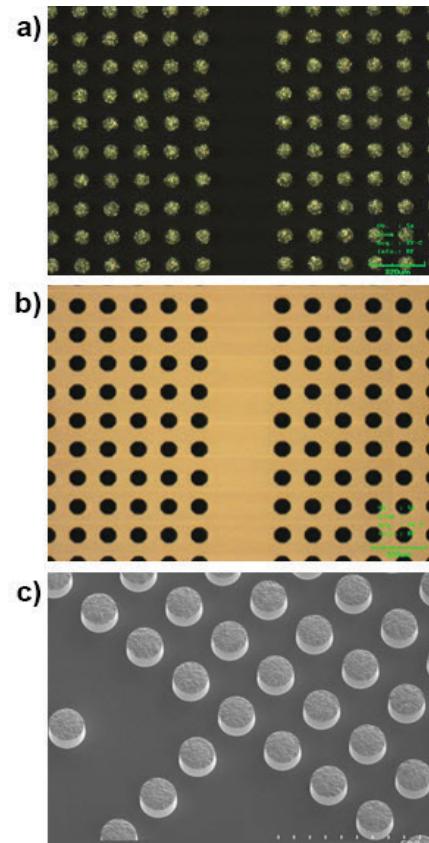


Figure 1: Optical images a) Pre-dry film resist strip; b) Post-DFR strip; c) SEM image post-DFR strip.

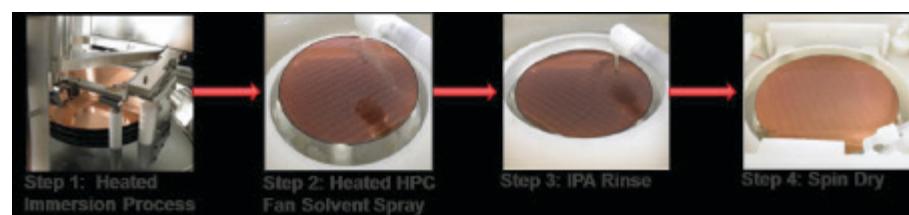


Figure 2: Dry film strip process sequence.

spin-rinse-dry station where the surface is completely cleaned and becomes particle-free using an IPA rinse.

Because there are numerous types of dry film resists, the selection of a solvent appropriate for the film being dissolved is important. For the work reported in this paper, a Dynastrip™ solvent technology was selected given its compatibility with all advanced packaging applications, such as plated bumps and redistribution line metallurgies. This family of chemistries

has excellent performance with dry film resists, as well as wet spin-on resists. The Dynastrip solvent is compatible with copper, all solder types, and with the underlying passivation layers. Because it can be recirculated within the equipment, and has a high bath loading capability, it contributes to a low cost-of-ownership, as is demonstrated in the cost analysis section of this paper. It should be noted that other chemistries have been used successfully. However, there

are differences in the chemical costs, chemical life, and process parameters.

One of the significant operational cost drivers using a wet bench or traditional single-wafer process is the frequency of filter changes caused by the significant buildup of partially dissolved resist material in the system. To address this, ImmJET technology includes a Triple Strainer that collects this material. The Triple Strainer is automatically flushed with solvent to clear the buildup of residuals. With two strainers in tandem, one strainer can be actively processing while the other is self-cleaning, thereby enhancing process efficiency and eliminating the cost for filter replacements.

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Cost-of-ownership

Activity-based cost modeling is a detailed, bottom-up approach to understanding cost. A process flow is broken down into individual activities, and the cost considerations for every activity are analyzed. These considerations include the time required for the activity, labor dedicated to the activity, material costs (both consumable and permanent), tooling costs, all capital-related costs, and yield loss.

The goal of the study was to compare ImmJET to three industry standard methods: wet bench, batch spray, and single-wafer strip equipment. A summary of the initial analysis is shown in **Figure 3**. Because the wet bench is the most commonly used of the three alternatives, the scope of the cost analysis presented in this study compares the new solution versus a traditional wet bench strip approach (**Figure 3**). This analysis focuses on a single-step in a process flow, so rather than adding or removing steps, as often happens when two technologies are compared, all of the adjustments are within the parameters of a single step. Industry data was used to determine the parameters for the current industry method, such as equipment price, bath refresh rate, and throughput. However, because every factory is different, in addition to selecting baseline assumptions for the industry method, a sensitivity analysis was

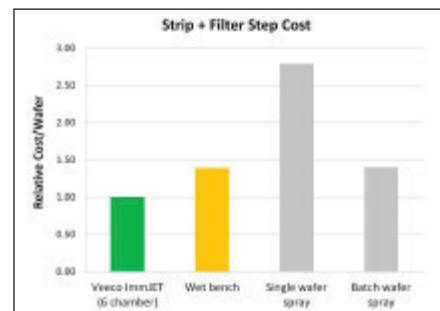


Figure 3: Cost-of-ownership comparison.

carried out on key variables to understand their impact on cost (**Table 1**).

Cost model assumptions include the following: 1) Direct costs only—no overhead or pricing margins; and 2) Factories are assumed to be well-balanced and fully utilized. **Table 2** shows the cost breakdown of wet bench technology relative to the ImmJET 6-chamber tool, which is the more cost-effective of the two. The type of contributing cost is also included. Note that the percentage of cost for the new technology is split almost evenly between material and capital. This is because the equipment price is more expensive than a traditional wet bench, but less material is required to clean the same number of wafers. The wet bench is a more material-heavy process, not only due to the larger bath, but due to the filter requiring continual replacement – and the filter represents a material cost.

Sensitivity analysis

The analysis of baseline assumptions revealed that the wet bench is more expensive than the 6-chamber ImmJET tool. To verify these findings, material costs (related to both the bath and the filter) were analyzed for sensitivity. There are multiple ways to look at chemical costs with regard to a process that uses a substantial volume of chemical as a consumable. This analysis looks at the trade-offs from the perspective of the

number of wafers cleaned by a set number of gallons, and also by the refresh rate of a bath for a set number of wafers. It should be noted that the yield for both processes was assumed to be the same. Because the use of single-wafer processing typically results in higher yield than a batch process, the results in this analysis are conservative.

The two charts in **Figure 4** show the cost of the strip step for the 6-chamber tool compared to a wet bench, at different refresh rates. The blue circle indicates the baseline assumptions. These charts make it clear that even if the 10-gallon refresh rate is a high assumption and fewer gallons can be used to completely clean 500 wafers, the

	Relative Throughput (wph)	Relative Equipment Cost	Relative Chemical Cost	Bath Loading	Other
ImmJET 6 chamber	1.00	1.00	1.00	500 wafers in 6.2 gal of material at \$80/gal	Triple strainer with self-cleaning capability
Wet bench	0.32	0.33	1.61	500 wafers in 10 gal of material at \$80/gal	Filter changed every 1000 wafers at \$100 per filter

Table 1: Cost model assumptions (ImmJET vs. wet bench).

Breakdown of Strip + Filter Steps	Labor	Material	Capital	Strip + Filter
ImmJET (6 chamber)	1%	49%	50%	1.00
Wet bench	2%	60%	38%	1.39

Table 2: Strip + filter costs by activity.

ImmJET 6-chamber tool
Sensitivity to # of gallons per refresh

Cost of strip step

of gallons

Wet bench
Sensitivity to # of gallons per refresh

Cost of strip step

of gallons

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Figure 4: Cost sensitivity to chemical usage. (Note: y-axis scale is the same for both charts.)

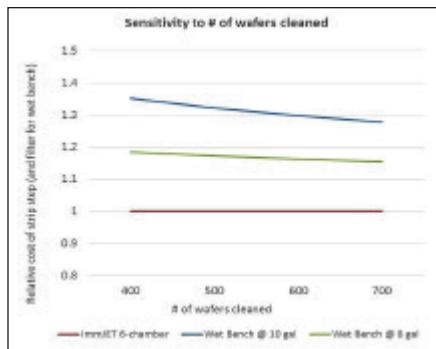


Figure 5: Cost sensitivity to number of wafers cleaned.

wet bench is not cost-effective at even 8 or 7 gallons.

Figure 5 assumes a baseline chemical amount and varies the number of wafers cleaned. Our solution is proven to clean 500 wafers in 6.2 gallons of material. This chart indicates how the cost would further be affected by an increase or decrease in the number of wafers. The new immersion and spray process technology shows a clear cost advantage. A lower cost wet bench at 10 gallons may only compete in long-term cost-of-ownership if a bath refresh of 8 gallons is able to successfully clean more than 700 wafers.

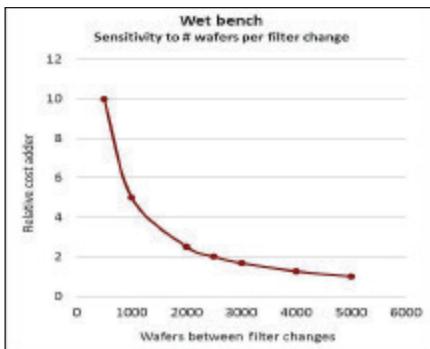


Figure 6: Cost sensitivity to filter change frequency.

Figure 6 indicates the contribution to cost when having to replace a filter regularly for a typical wet bench. The cost adder indicates how much of a \$100 filter is amortized over the cost of each individual wafer, depending on the number of wafers cleaned between filter replacement.

Summary

The new immersion and single-wafer spray process technology evaluated combines the advantages of sequenced immersion and single-wafer spray within one tool. This enables a cost-effective method for stripping

of dry film resists. Activity-based cost analysis conducted by SavanSys Solutions LLC, confirms the use of this technology to be less costly than the conventional batch wet bench. Improved bath life, efficient chemical usage, and significant reduction in filter changes provide the cost savings.

Acknowledgment

ImmJET and WaferStorm are registered trademarks of Veeco.

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Dicing silicon carbide power devices using thermal laser separation

By Hans-Ulrich Zuehlke, Mandy Gebhardt [3D-Micromac AG]

This paper will give an overview of the potential of a laser dicing approach, called TLS-Dicing™, for SiC-based semiconductor products. In the described case study, a typical power device wafer with full backside metallization, polyimide and metal structures in the dicing streets was separated by using this new technology. A high yield count in combination with very high edge quality was demonstrated. The dicing cost per wafer was significantly reduced.

Challenges with dicing SiC power devices

Silicon carbide (SiC) is a crystalline compound of silicon and carbon. It possesses certain qualities such as high charge carrier mobility, high strength, hardness, and high thermal conductivity. Due to these characteristics, SiC is considered a replacement material for silicon (Si)-based semiconductors in the electronics industry in certain applications, including power devices, light emitting diodes (LEDs), and sensors for harsh environments. Cost, quality and throughput are all major factors in achieving successful manufacturing of SiC-based devices. Wafer dicing is evolving as a critical value-add process step that not only ensures, but further enhances, SiC device yields.

The traditional technique for separating SiC devices from wafer form is mechanical blade sawing. This method involves a very fast rotating foil with abrasive particles to remove the wafer material. Because of the hardness of SiC (Mohs scale 9.2), blade sawing suffers from low feed rate and high wear of the diamond-coated dicing blade, resulting in the risk of uncontrolled tool breakage during the dicing process. In addition, blade sawing can result in chipping and delamination at the edge of the die (**Figure 1**). An advanced version of this approach is ultrasonic vibration-

supported mechanical sawing, which provides slightly higher dicing speed (10-20mm/s), but in principle has the same limitations. With the upcoming transition of SiC wafer sizes from 4-inch to 6-inch diameters, mechanical blade dicing will reach its limit because the cumulated street length more than doubles and is beyond the ability of one saw blade to completely cut. In this situation, the blade would either have to be changed while the wafer is in work-position or, in the worst case scenario, the blade will break during the middle of the dicing process and damage the wafer. Laser ablation is an alternative approach to wafer dicing, but when applied to SiC wafers it can result in micro cracks, significant heat affected zones, and metal debris in the streets, all of which can impact die yields.

Thermal laser separation overview

Thermal laser separation (TLS-Dicing) is a fast, clean and cost-effective alternative to separating SiC-based semiconductor products. It has many advantages compared to competing technologies such as blade sawing and laser ablation:

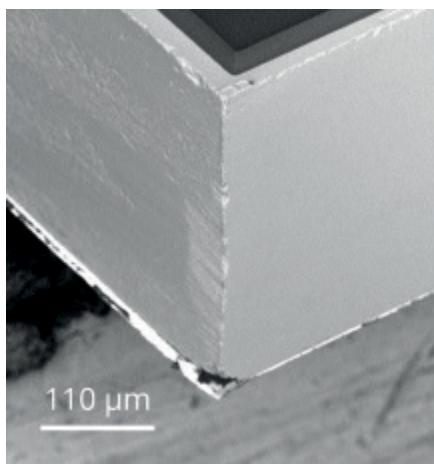


Figure 1: SiC die edge after mechanical dicing shows chipping and delamination defects [1].

- High separation speed (up to 300mm/s for SiC) resulting in a throughput of 10 wafers per hour (assuming a 4-inch wafer with 2mm die size);
- Very smooth edges (avoids increased leakage current of vertical diodes by leaving the p/n-junction undamaged);
- Nearly no chipping and micro cracks for less breakage;
- Thin backside metal on the chip is separated without damage;
- No tool wear;
- Low cost-of-ownership due to no tool wear and nearly no consumables; and
- Zero kerf cleaving for reduced street width.

The new thermal laser separation process uses thermally-induced mechanical stress to cleave brittle semiconductor materials such as SiC, Si, germanium (Ge) and gallium arsenide (GaAs). A laser heats up the solid, brittle material and generates a zone of compressive stress, surrounded by a zone of tangential tensile stress pattern. Next, a jet of extremely small amounts of deionized (DI) water spray is applied that creates a second cooled zone with a minimum distance to the first one—inducing a tangential tensile stress pattern. The resulting tensile stress in the overlaying region of both stress patterns has a local maximum that is sharply focused and has a clear orientation (perpendicular to the street), and is therefore able to open and guide the crack tip through the material.

The new process is always a one-pass process that separates the whole thickness of the wafer at once. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. The local scribe is preferred to ensure the highest bending strength and least particle generation. On the other hand, the continuous scribe offers best results for products with metal in the street and improves the straightness of the cleaving process.

Because thermal laser separation is a cleaving process, the die edges are smooth and free of remaining stress or micro cracks and chipping zone (**Figure 2**). Any reduction in bending strength as a result of the dicing process is significantly lower compared to ablative laser technologies. In addition, the backside metal is separated with no delamination or heat affects.

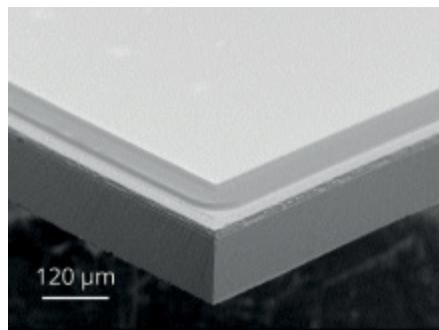


Figure 2: SiC die edge after the TLS-Dicing process shows smooth edges and no micro cracks or chipping.

Experimental set-up

An experiment was conducted to evaluate the impact of thermal laser separation on SiC device yields. The wafer separation was done with a microDICE™ system using thermal laser separation technology. The processed 4-inch wafer had a thickness of 110 μm and a thin silver-type backside metal stack. The streets were covered with several metal test structures. The active zone of the dies was protected by a polyimide coating. On the frontside of the wafer, the outer part of the edge exclusion zone was covered by a ring of metallization and polyimide coating. On account of customer requirements, larger dies were simulated by building 3 by 3 die-clusters of smaller dies. For this reason, only every third street was diced (**Figure 3**).

As described earlier, each cleave needs a defined starting point in the form of a local initial scribe. To remove the reflecting metal structures in the street, a shallow continuous soft scribe along the entire street length was applied. The scribing laser is a 532nm short-pulsed laser with a Gaussian beam profile. Scribing speeds of 50mm/s up to 200mm/s were achieved. The lower the scribing speed, the smaller the heat affected zone of the

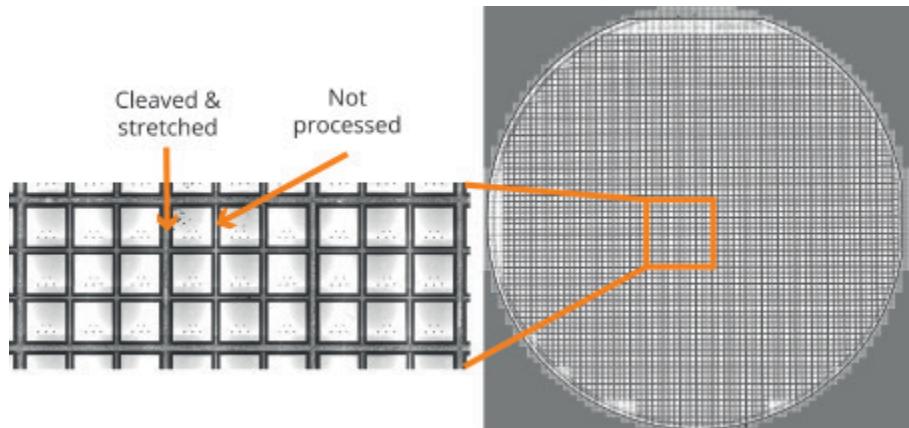


Figure 3: The whole wafer was diced; and target die size was simulated by 3 by 3 clusters of smaller dies.

polyimide cover layer and the particle pollution. Further investigations have shown that comparable scribing results can be achieved with less expensive near infrared (NIR) laser sources. A z-axis autofocus was used to obtain a smooth scribing line. The cleaving itself was realized by a 200W continuous wave (cw) laser with NIR wavelength. The consumption of cooling liquid (DI-water) was below 10ml/min.

Experimental results

The new dicing method was able to separate all chips without chipping and micro cracks (**Figure 2**). There is nearly no thermal impact of laser machining to the polyimide cover layer. No washing or cleaning and no protective coating was applied – a significant advantage in terms of operation costs. The separation of the backside metal was very smooth and without any delamination (**Figure 4**). This is important for minimizing problems during die mounting on the heat sink. The applied continuous scribe was used to open the metal structures without any impact on the bulk material after cleaving (**Figure 5**).

Yield impact

The processed wafer was analyzed for defects and yield using a high-resolution optical inspection tool. This inspection method was adopted from a best practice of an industrial SiC device manufacturer. Yield consideration only includes dies inside the edge exclusion zone. The average yield value for this application is more than 98.9%. The observed defects and deviations have

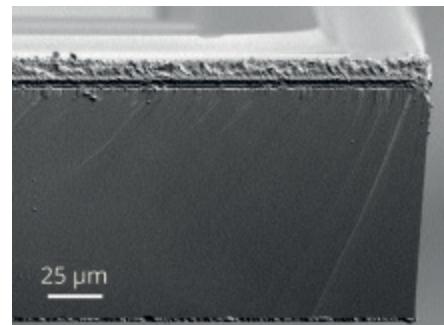


Figure 4: Smooth separation of backside metal, with the typical 4-degree off orientation visible.

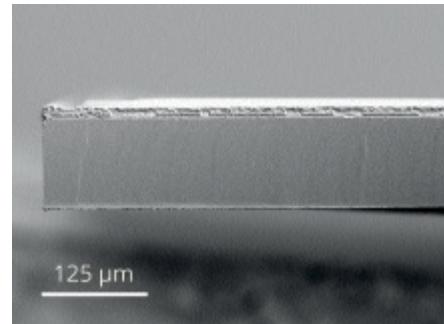


Figure 5: The photo shows the effect of metal in the dicing street. Separation is successful with minor impact on straightness as noted by the Wallner lines.

been categorized (**Table 1**). Nearly all of the defects are located in the edge exclusion region.

A noted characteristic pattern of the cleaving process was a short, local cleave dislocation, perpendicular to the edge of the wafer. In all cases, this deviation was limited to the edge exclusion region (**Figure 6**) and can be ignored for yield calculation. For a few chips, the cleave was not perfectly straight, but the deviation never reached the active area of any

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die (see “minor straightness deviation” in **Table 1**, **Figure 7**). In an even rarer occurrence, the cleave touched the active die area (see “major straightness deviation” in **Table 1**). A potential source of this is an overlaying internal stress pattern.

In this case study, the wafer had a massive metal and polyimide ring in the edge exclusion area on the top side of the wafer, which was built into the design rules by the manufacturer. The influence of this ring was visible and caused damage to a few die behind the edge exclusion (see “cleave failure by outer metal ring” in **Table 1**). This error pattern can easily be avoided by implementing a laser

clearing step comparable to the metal pattern opening in the dicing streets. Alternatively, this clearing step can be avoided by modifying the design rules to exclude any outer metal rings.

As an outcome of this case study, it is suggested to either avoid designing in the metal ring, or take a less restrictive approach and remove the metal ring by implementing an additional laser clearing step. In both cases, the expected yield will increase an additional 0.8% (to a total yield count of 99.74%). Dies from a comparable wafer have been packaged, and after thermo-cycling only one out of 106 dies failed the leakage current test. The cause of this defect is believed to be unrelated to the new process.

Additional implications

In addition to yield improvement, the new process has demonstrated a significant improvement in terms of cost per wafer. A typical mechanical sawing process wears one saw blade per wafer due to the enormous hardness of SiC. As noted earlier, this problem is compounded on larger diameter wafers, and is likely to result in requiring an additional blade to completely cut a 6-inch wafer. To match the throughput of the TLS process, an investment in nine times more mechanical sawing tools is required. Taking this and additional factors into consideration such as cost of consumables, projected tool depreciation and footprint (one microDICE system using TLS-Dicing technology versus nine blade saws), the overall cost per wafer is projected to reach up to \$41.69 per 6-inch wafer for mechanical sawing, but only \$2.70 per 6-inch wafer for the microDICE/TLS system. This does not factor in additional cost considerations such as reduced tool operator costs by

using a single microDICE system compared to the significantly greater number of mechanical blade dicing tools, nor the increased yield enabled by the new dicing process.

Summary

Thermal laser separation is a new approach to separating brittle materials at high throughput, low cost, and with high separation quality. The cleaving principle shows unique advantages for SiC-based products with backside metallization, such as power devices. The case study highlighted in this white paper demonstrated a very high separation yield of 98.9%. This is an average value for a small batch of 4-inch SiC product wafers with backside metal, metal structures in the street on the front side, and polyimide on the dies.

The new process has demonstrated unique advantages for SiC-based power devices. Investigations and developments for other applications and materials (including silicon) are in preparation. For example, the ability to cleave without any particle generation could be an interesting option for flip-chip applications, such as MEMS and 3D-packaged wafers with solder bumps. At the same time, the ability to provide zero kerf cleaving could have a noticeable impact on die yields where smaller die sizes are involved and reduced street widths could enable more die per wafer.

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Acknowledgements

TLS-Dicing and microDICE are trademarks of 3D-Micromac AG.

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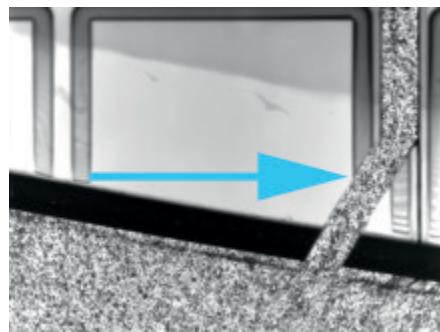


Figure 6: This photo shows the perpendicular cleave exit at the wafer’s edge, which is not yield-relevant due to residing in the in-edge exclusion zone.

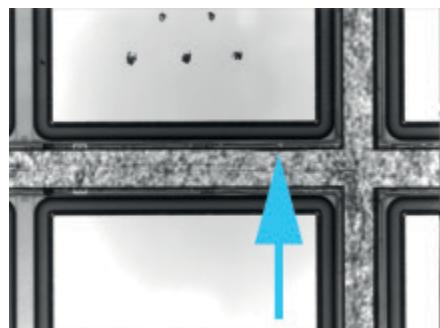


Figure 7: Example of minor deviation with no influence on the electrical function.

Defect Category	Yield %
Perfect	97.97
Minor straightness deviation	0.94
Major straightness deviation	0.23
Cleave failure by outer metal ring	0.83
Total Yield (all usable dies)	98.91

Table 1: Resulting average yield and yield losses by categories.

INDUSTRY NEWS



Reflections on IWLPC 2016

By Louis Burgyan *[LTEC Corporation]*

The 13th International Wafer-Level Packaging Conference (IWLPC) and Exhibition, held in Silicon Valley on October 18-20, offered an excellent



insight into current issues and future challenges in advanced packaging technologies. An impressive array of 48 presentations, five interactive presentations (poster sessions), and four workshops covered a wide array of topics with focus on various aspects of



fan-out wafer-level packaging (FOWLP), 3D packaging and manufacturing, and microelectromechanical systems (MEMS). Overall, attendance was higher than what I've seen in past years, and the expo hall was sold out completely. Table-top exhibitors, who couldn't get space inside the main exhibition hall, lined up their display items along the walkways in front of the main exhibit area. Quite fittingly, the main theme

of the conference was "Bridging the Interconnect Gap," thus highlighting one of the major challenges our industry is facing as "big data" seeps into our daily lives in multiple forms at the workplace, home, and in between.



Cognitive computing, mobile communication, connected vehicles, cloud-connected Internet of Things (IoT) devices—all require fast processing locally and through the cloud with access to massive amounts of data, regardless of its location. The brick and mortar of the underlying hardware environment is advanced packaging technology that needs to facilitate interconnectivity among often heterogeneous systems within a package. Processors, memories, and logic devices need to interact at multi-gigabit per second data rates. Those vastly improved latencies attained by 3D NAND flash memory stacks must not get compromised by data paths within various building blocks assembled in 2.5D or 3D systems in a package. Similarly, data and information generated by sensors need to be processed, interpreted, and transmitted through communication systems with high signal and power integrity.

The focus of this event was wafer-level packaging (WLP) and FOWLP technology. With the evolution of semiconductor manufacturing processes, minimum feature size decreases and functionality built into the die increases along with I/O count, and heat generation within the die often increases. FOWLP technology offers a practical and cost-effective solution by creating additional surface area around the semiconductor die where I/O terminals can be placed. Outward routing from the die is facilitated by adding a redistribution layer (RDL) structure having one or more routing layers.

Implementation of the systems noted above, often in application-driven form factors, presents formidable challenges to outsourced semiconductor and test suppliers (OSATS) and circuit and

systems designers alike. Circuit and system performance can no longer be separated from the packaging technology deployed. As noted by several presenters at the conference, the new paradigm is a collaborative approach between circuit/system and package design teams. One of the speakers at a panel discussion cited an example of the exemplary collaboration between Apple's design teams and TSMC's developers of the highly advanced Integrated Fan-Out Wafer-Level Packaging (InFO-WLP) technology deployed in the A10 processor of the iPhone7.

Given this backdrop, in his keynote address, Prof. Rao R. Tummala of Georgia Institute of Technology discussed the future of fan-out wafer-level technologies and active/passive component embedding. In another keynote presentation, Prof. Klaus-



Dieter Lang, Director of Fraunhofer IZM, outlined his vision of advanced manufacturing technology platforms required to serve the needs of a diverse field of cyber-physical systems. Dr. Lang highlighted an existing gap between wafer-panel and rectangular PCB-panel infrastructures in the 2-20µm L/S range and stressed the need to find reliable, low-cost solutions.



Panel discussions

Large-area rectangular panel processing. Participants of a panel discussion, moderated by Jan Vardaman of TechSearch International, examined the potential cost savings and existing barriers that large-area rectangular panel processing needs to overcome before 2.5D and 3D FOWLP system-in-package (SiP) structures having less than 20µm L/S could be fabricated in a high-volume manufacturing environment. Per estimates, most cost benefits stemming from increased throughput can be attained at a roughly 600mm x 600mm panel size. The larger the individual package size, the larger the saving. For example, at a 10mm x 10mm package size, a 25-30% cost reduction is realizable; however, at a 4mm x 4mm or smaller package size, there is no cost saving.

The need for optical systems having higher accuracy and depth of focus to accommodate processing of large warped wafers with high yield and reliability was discussed. The lack of standards and requirement for die-shift error correction were also highlighted. Panel processing plant tooling costs were estimated to be over \$150 million. Panelists suggested that IoT and the requirement for processing massive amounts of data in the coming years ahead are likely to be the market driver that finally ushers fine-pitch fan-out panel-level packaging (FO-P LP) into mass production.

Chip-package interaction. Dr. Urmie Ray of Qualcomm moderated another panel discussion on chip-package interaction (CPI) and its impact on products fabricated for the commercial, automotive, and defense sectors. The discussion followed two paths: mechanical CPI (mCPI) and electrical



The advertisement features the SEMI logo at the top left. To the right, the text 'www.semi.org/European3DSummit' is displayed. The main title 'EUROPEAN 3D SUMMIT' is prominently shown in large white letters. Below it, the subtitle 'CREATING HIGH DENSITY SYSTEMS' is written. To the right of the subtitle, the words 'Conference', 'Exhibition', and 'Networking' are listed vertically. At the bottom left, a circular graphic contains the text '23-25 JAN 2017' and 'GRENOBLE, FRANCE'. On the right side, there is a detailed description of the summit's focus: 'A cutting-edge conference and exhibition that brings together the entire 3D supply chain and focuses on the technologies that enable higher density products.' At the very bottom, the phrase 'Attend to Connect!' is written in bold.



CPI (eCPI). Many attendees asked specific questions concerning back-end-of-line (BEOL) separation, metal line breakage, warpage, die thinning, issues related to thick Cu RDL, advanced process nodes using ultra low-k materials, and new failure mechanisms. The long list of concerns underscored the need for consistent process control, predictive modeling, and tracking and understanding failure mechanisms.

Session highlights

Concerning session highlights, it is impossible to offer a comprehensive overview of so many excellent presentations in a short article, however a few are highlighted below.

Dr. Habib Hichri of SUSS MicroTec described a full-field scanning exposure system with a 1:1 projection lens suitable for high-resolution patterning and large depth of focus. These features

and the 30x30mm field size are essential for working with thick photoresist and warped 300mm wafers or large rectangular panels. The system has closed-loop projection mask temperature control to facilitate use of low-cost soda lime masks. The system has software to correct for die placement errors, and it is capable of supporting <3µm L/S at 50% lower cost-of-ownership relative to UV steppers.

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Eoin O' Toole of NANIUM S.A. addressed an emerging thermal challenge: as FOWLP is moving towards accommodating multiple dies in 2.5D and 3D package-on-package (PoP) forms, the dissipated power within the die increases. Consequently, thermal resistance of the new structure requires enhancement. The company addressed this issue in the form of a demonstrator project. The key point is the need to address this issue proactively.

Dr. Bora Baloglu of Amkor described the company's multi-die capable and 3D PoP compatible high-density polymer-based chip last fan-out process that is expected to deliver lower cost and reduced z-height. This technology has a maximum of three layers of RDL with a 2-10 μ m L/S range. The target markets are multi-die SoCs, high-bandwidth memories (HBM), mobile applications, and networking.

Eight presentations were devoted to manufacturing issues: Dr. Guilian Gao of Invensas disclosed a room-

temperature Cu-Cu direct bond method initially developed for wafer-to-wafer (W2W) bonding that is already in high-volume production for image sensors. The technology was recently further developed for die-to-wafer (D2W) and die-to-die (D2D) stacking, positioned as a simpler alternative to thermal compression bonding of microbumps. Per Dr. Gao, this technique uses a unique grid-contact pattern that is more tolerant to D2D and D2W misalignment—an important consideration impacting both cost of production and cost-of-ownership. While the technique requires a <1nm surface roughness, this is within the capabilities of today's chemical mechanical polishing (CMP) technology she noted.

Four of the eight MEMS presentations described various low-temperature bonding methods to create a hermetic seal between a MEMS device wafer (DW), and a cap wafer (CW) using wafer-level bonding (WLB) process. The key requirements of

this process are hermeticity sustained over time, a narrower bond-seal footprint, low peak process temperature, low bonding pressure, and a <2 μ m alignment capability. Eutectic and diffusion bonding techniques are the leading candidates.

Advances in various gold electroplating applications were described by **Dr. Lynne Michaelson** of Technic Inc., a provider of advanced plating equipment and specialty chemicals. The author presented images of remarkably outstanding results attributed to a proprietary additive.

Summary

IWLPC 2016 turned out to be a very well-attended three-day event. Conference organizers, invited speakers, authors of papers, and exhibitors all contributed to creating this lively, inspiring event, facilitating an informal exchange of ideas for learning and collaboration, all to the good of package engineering—a key enabling technology of our times.



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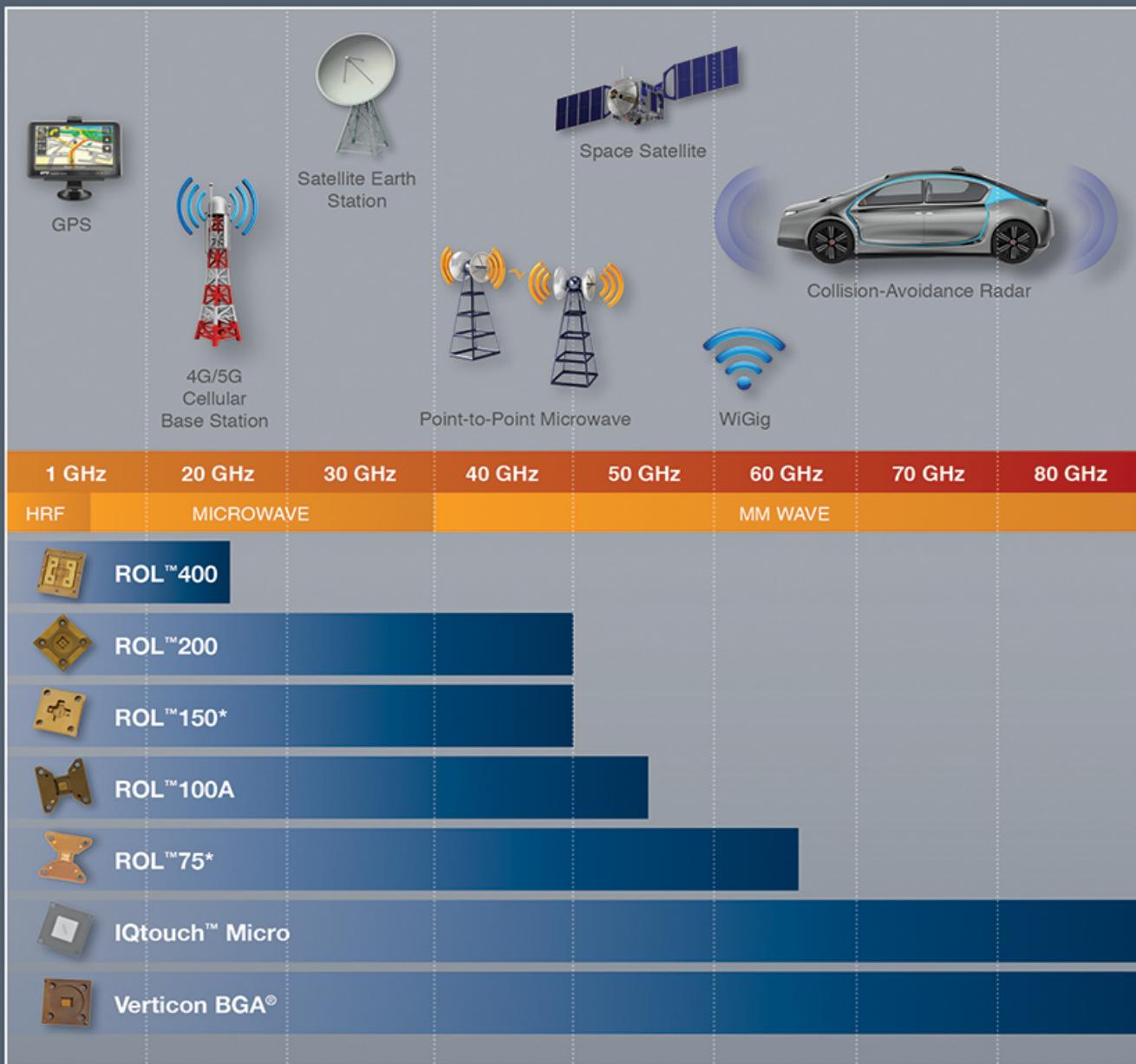
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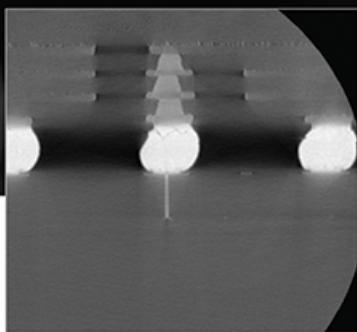
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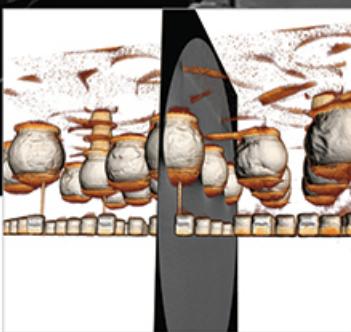


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