

Chip Scale Review®

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Volume 20, Number 3

The Future of Semiconductor Packaging

May • June 2016

3D backside processing

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- Plasma dicing
- FOWLP advances
- Packaging trends & update
- Emerging automotive applications
- Improving yield and reliability in AOI
- Impact of wafer-based packaging on the supply chain





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A plasma etch module that provides high-rate, low non-uniformity Si via reveal etch is important to one of the final and critical steps in the 3D wafer stacking process flow (see cover article on p.45). Combining a high-throughput Si thinning process with high selectivity to the oxide liners delivers the smooth wafer surface needed for the subsequent steps to complete the 3D process flow.

Photo courtesy of SPTS Technologies

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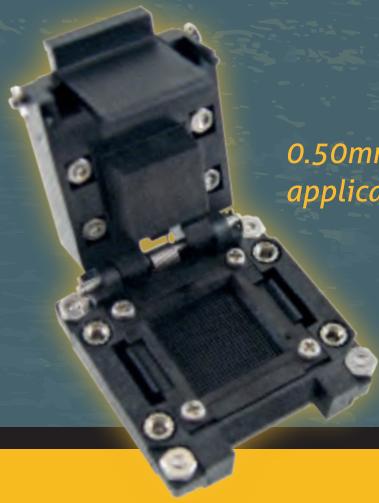
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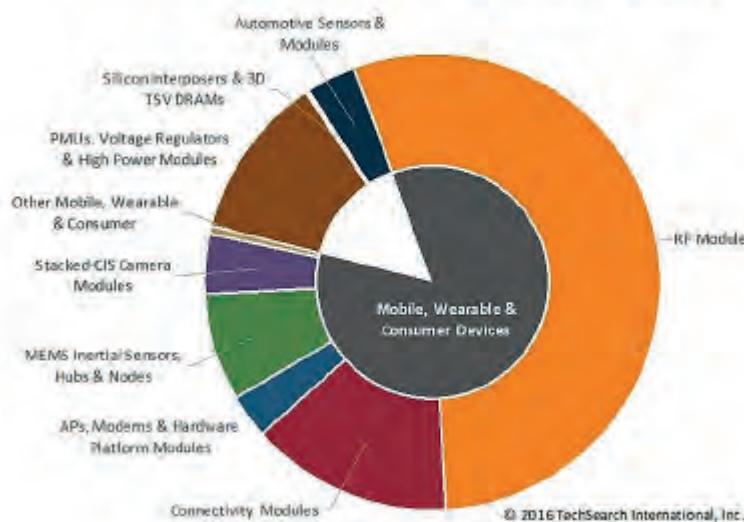
MARKET UPDATE

Major OSATs positioned for growth opportunities in SiP

By TechSearch International and Chip Scale Review staff

In a series of interviews, *Chip Scale Review* and TechSearch International asked several major outsourced semiconductor assembly and test companies (OSATs) to comment on their view of system-in-package (SiP) technology and how they are positioned to meet the growing demand. In today's world of mobile product introductions that must ramp in four to five months and may only have a lifetime of a year, SiP is essential to the success of new products in this space. The physical form of a SiP is a module that often includes mechanical features such as shielding, heat sinks, antennas, and/or connectors. There are many different configurations of SiP modules (2D/2.5D/3D) that are customized for specific end applications to leverage a variety of potential benefits offered by SiP, including performance, cost, form factor, and time-to-market. SiP solutions may require multiple packaging technologies such as fine-pitch flip-chip, wire bonding, wafer-level packaging (WLP) and fan-out WLP (FOWLP), integrated passive devices, and embedded die, as well as advanced substrates, high-density surface mount technology (SMT), enhanced molding processes, shielding, and system-level design and test. In addition to multi-die flip-chip packages, hybrid package designs with stacked wire bonding die on FC die, or in side-by-side configurations, integrated with a number of passives, are examples of 2D SiP package technologies in use today. A recent report from TechSearch International shows a compound annual growth rate of slightly more than 13% in the areas of mobile, wearable, consumer, and select computing, communication, and automotive electronics (**Figure 1**). Several major OSATs are targeting this market with varying capabilities. Below is a summary of the responses to interview questions posed to several OSATs.

**2015 SiP Market by Device Type
(shares of packages shipped)**



- Almost 70% of the units were RF and connectivity modules

Figure 1: 2015 SiP market by device type (shares of packages shipped). SOURCE: TechSearch International

Q: How do you define SiP?

Amkor: Amkor defines advanced SiPs as multi-component, multi-function in an IC package. SiP integrates more than one semiconductor component of different functionalities into a single package form.

ASE: ASE defines an SiP module as a package or module that contains a functional electronic system or subsystem that is integrated and miniaturized through IC assembly technologies. It is important to note that the module is a "system or subsystem." There are many multi-die packages with surface mount technology (SMT) components being manufactured, but they may not perform system-level functionality. If a system-level test were performed on the module, then it would fit into this SiP definition. It is also important to highlight the achievement of miniaturization using IC assembly technologies. There are many

small modules fabricated using traditional SMT methods. If an IC process such as die attach, wire bonding, transfer molding or any other process common to IC assembly is used, then it would fall into this definition.

STATS ChipPAC: SiP is a functional electronic system or sub-system that includes two or more heterogeneous semiconductor die (often from different technology nodes optimized for their individual functionalities), usually with passive components.

SPIL: SiP is a hybrid solution for system integration.

UTAC: SiP is a heterogeneous integration into a standard package format such as ball grid array (BGA), land grid array (LGA), and lead-less or leaded lead frame. SiPs typically contain multiple ICs with diverse device functions such as logic and memory, RF or analog plus digital

controllers, and sensors. Often passive components are included. SiP uses a mixed assembly of technologies including SMT, wire bond, flip chip and may feature the using of embedding or redistribution layer (RDL) in wafer or panel format.

Q: What advantages does your company offer the SiP market?

Amkor: SiP requires high-precision assembly technology that leverages Amkor's strengths in design—especially for RF and mm-wave designs where understanding the impact of noise on the performance is critical. A complete SiP solution is offered with passive components in the form of integrated passive devices or embedded components to provide a small form factor, embedded and conformal shields, and antenna design in an external, side-by-side, or antenna on package/mold solution. We offer conformal metal shielding and emphasize its EMC design on copper-supporting shielding technology with good adhesion of the shield to EMI/ground and minimum leakage through the bottom layer of the substrate.

Amkor highlights its time-to-market enabling development cycles of less than six months with rapid production ramps of millions of units per week. Also highlighted is cost reduction by the use of bill-of-material optimization through co-design and bill of materials (BOM) purchasing management and scale, as well as high-yielding assembly.

ASE: To address ongoing trends within the electronics market, such as increasingly smaller devices packaged with higher functionality, ASE is building its SiP business upon a strong foundation that leverages established core strengths and large infrastructure of IC assembly capabilities with factories across the world. ASE is the only OSAT with internal substrate manufacturing, semiconductor assembly and test, as well as EMS capabilities. We can offer customers a complete solution, based on our system-level design, manufacturing expertise, and build-of-materials logistics management supported by our USI division.

STATS ChipPAC: STATS ChipPAC has developed comprehensive capabilities, including design, advanced packaging technologies, high-density SMT component placement, advanced molding for complex topographies, conformal shielding, and system-level test, for a wide variety of SiP and modules in multiple market segments. Various SiP configurations have been deployed ranging from conventional 2D modules with multiple active and passive components, interconnected through flip chip, wire bonding, and SMT, to more complex modules such as package-in-package (PiP), package-on-package (PoP), 2.5D and 3D integrated solutions.

An experienced R&D and engineering team supports customers faced with complex SiP integration requirements. SMT design rules are being advanced through refinements in process technologies to enable tighter component-to-component placement and new material and molding technologies to enable lower mold cap profiles and smaller dimensions. We work with advanced substrate materials with fine line and space (L/S), reduced dielectric thickness, and coreless design to address the reduced form factor requirements of next-generation applications, while enabling lower cost.

SPIL: SPIL has developed an antenna-in-package design using an inverted-F antenna in the molding compound to provide size reduction, greater antenna efficiency, the ability to support high-density components in the package, and easier customer layout designs. We also offer a package with a printed antenna in the substrate or an antenna-on-package design using a thin sputtered coating layer.

UTAC: UTAC has recently teamed with AT&S to offer a 3D SiP collaboration that allows the co-design of substrate and assembly in an embedded chip configuration. Components can be mounted on top of the package with SMT or flip chip, enabling a 3D structure.

Common themes

While there are different views of SiP, there are some common themes. TechSearch International has developed the following definition of SiP:

- SiP is a functional system or subsystem assembled into a standard footprint package such as an LGA, BGA, quad flat no lead (QFN), or FOWLP.
- It contains two or more dissimilar die, typically combined with other components such as passives, filters, MEMS, sensors, and/or antennas.
- The components are mounted together on a substrate to create a customized, highly integrated product for a given application.

Regardless of the definition used, SiP is driven by the need for miniaturization and is only adopted when form factor and performance requirements are met.

A common theme that runs through the OSATs is the importance of design in the SiP process. Die and package traditionally have been treated as two separate designs. The package engineering is considered a backend effort. With SiP, co-design is essential for success, which becomes especially important in the example of RF products where antenna design and EMI shielding are required. In many cases, reducing the cost of SiP depends on reducing the BOM, which can be accomplished with careful design.

Success in SiP will require a business model that combines the strengths of the electronics manufacturing services (EMS) providers with those of the semiconductor assembly and test providers. For this reason, additional partnerships are expected to emerge. As noted by STATS ChipPAC, existing package technologies and processes are used to enable various SiP solutions. The challenge is the integration of these processes, and the incorporation of new process technologies such as EMI shielding, and yield management.

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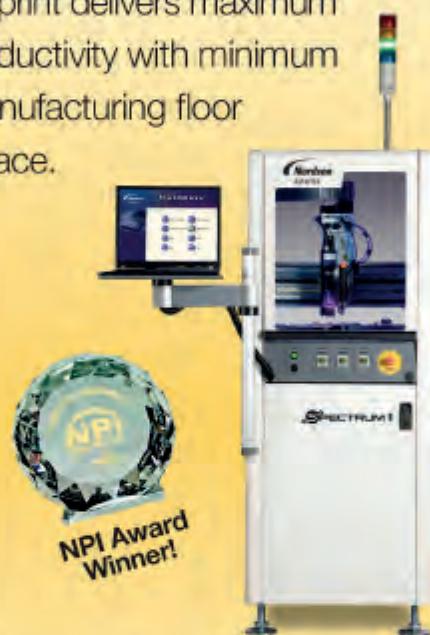
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MARKET UPDATE



Impact of wafer-based packaging on the supply chain

By Brandon Prior *[Prismark Partners LLC]*

The past twenty years have seen an enormous shift in packaging approaches used for integrated circuits (ICs). In that time, we have moved from over 95% of die going in to lead frame packages to about 60% of units today. From a revenue perspective, 85% of all package assembly is into package types that did not exist 20 years ago.

The shift to customizable substrate-based array packages was one of many key factors contributing to the growth of the outsourced semiconductor assembly and test (OSAT) market. Though many OSATs started with quad flat package (QFP) and other lead frame packaging, today, a significant portion of their revenues come from substrate-based array packages. Substrate-based packages first emerged twenty years ago as an alternative to lead frame packages, and since that time have grown to represent 16% of IC package units, but closer to 68% of all IC package value. We will continue to see improvements and evolution in substrate-based packages, and they will remain the packages of choice for most all advanced requirements. More recently, the growth of packaging solutions completed in wafer format, including WLCSP, FO-WLP and 2.5/3D TSV, has prompted both OSATs and wafer foundries to address this growing opportunity.

Although many captive semiconductor operations are building WLCSP internally, OSATs and increasingly, foundries, continue to represent the fastest growth of capacity to serve both fabless and IDM customers. We are also seeing WLCSP commonly adopted in other segments beyond smartphones and

tablets. These segments include wearables/Internet of Things (oT)/medical, ultra-mobile PC and automotive applications. Though some concerns remain in terms of cost, reliability and ease of assembly, improved versions of WLCSP have allowed adoption for increasing complexity devices (**Figure 1**).

This adoption of WLCSP in new segments will be enabled by the second-generation of WLCSP package approaches, including, but not limited to:

- Protected or enhanced WLCSP: These offer protection on five sides of the die, which should enable improved package reliability and easier handling for surface mount technology (SMT) assembly. This technology is being explored for small die sizes.
- WLCSP without RDL: Die designed for flip-chip attach without RDL keep the cost of WLCSP low. Many companies have been using this “bump on pad” approach for years.
- Fan-out wafer-level package (FO-WLP): These offer significantly added flexibility with multi-chip, package-on-package (PoP), and broader final pitch configurations that can be built. While no longer a die size package, the RDL processing is still wafer-based, and already offers thinner packages and finer routing capabilities than substrate-based solutions of today.

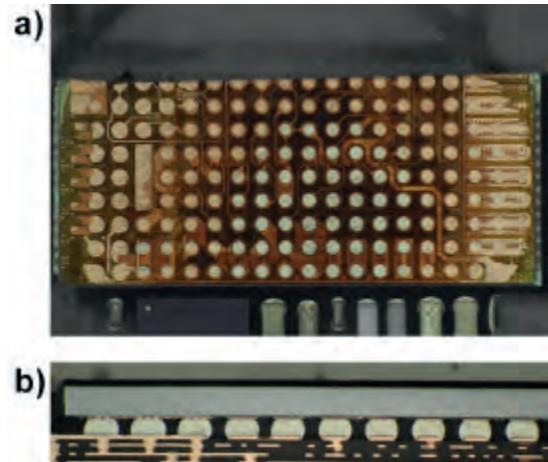


Figure 1: A Dialog PMIC. a) (top) The Dialog PMIC device found in the iPhone 6S measures 7.2 x 7.5mm, with a thickness of less than 0.4mm. b) (bottom) It has 380 I/Os, and utilizes a fan-in WLCSP structure with 1 metal layer RDL at 15µm line/space. The large die size requires underfill on this main board assembly. SOURCE: Prismark Partners LLC / Binghamton University

FO-WLP has been an available solution for over five years, and is now getting increased attention. Leading OSATs such as STATS ChipPAC (a JCET company), ASE, SPIL, Amkor, and NANUM S.A. have seen a significant uptick in interest for products over the past 12 months. No fewer than 12 fabless and IDM companies are in the process of qualifying dozens of design wins using this approach. Most of the FO-WLPs to date focus on smaller die/packages up to 8x8mm. Over the course of 2016, we expect to see 1-2 die packages with up to 500 I/O for multiple applications and companies. Most production of FO-WLP so far is focused on 1-2 layer RDLs at 10-15µm L/S.

As the shift from lead frame to substrate to wafer-based packaging evolves, Prismark expects the supply

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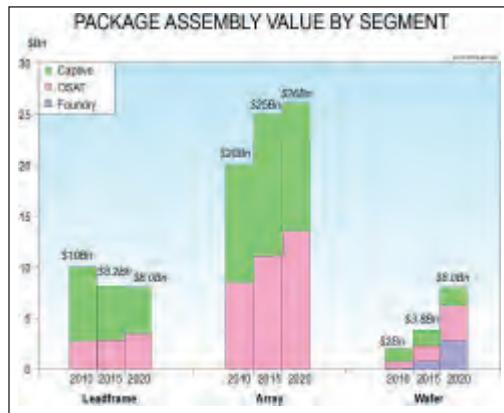


Table 1: Package assembly value by segment.

SOURCE: Prismark Partners LLC

chain to change as well. **Table 1** highlights the significance of OSATs in the substrate/array-based packages, and the importance of both the OSATs and the wafer foundries in forecasting wafer-based packaging.

Wafer foundries entering advanced packaging

The major story in the FO-WLP segment is the ongoing investment by TSMC with its integrated fan-out (InFO) package. It is now widely presumed that the Apple A10 processor will be the first large die adoption of FO-WLP technology. This may be a notable turning point for wafer foundries to enter the packaging domain. While speculations mount on whether second location/source will be required, TSMC appears committed to growing its back-end business.

From a business perspective, the entrance of wafer foundries and “mid-end” service providers may change the landscape for packaging. TSMC has aggressive growth targeted for back-end processing. The company is currently investing more in FO-WLP than all other OSATs combined. Meanwhile, other foundries are considering joint ventures and developments in this sector.

The offering of post-fab processing of semiconductors is logical for wafer foundries, especially while still in wafer format. For years, TSMC and GLOBALFOUNDRIES have been offering wafer bumping services.

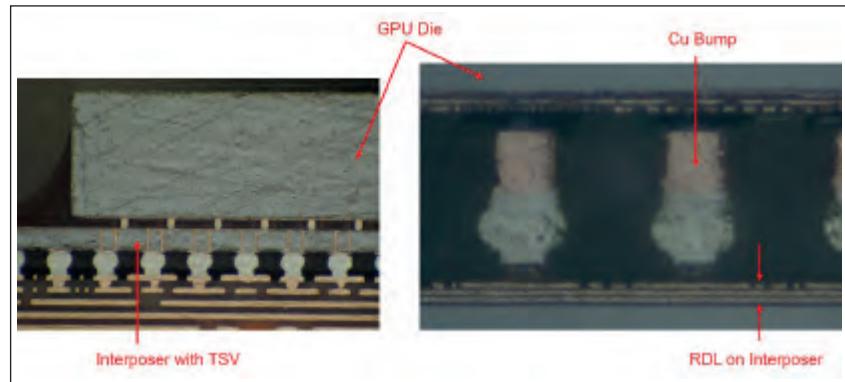


Figure 2: An AMD Fury X graphics processor comprising the following: a) (left) A 28x 35mm Si interposer from UMC that connects the GPU die to high-bandwidth memory stacks; and b) (right) The interposer has 3RDLs at 2.5µm line/space with 10µm diameter TSVs. SOURCE: Prismark Partners LLC / Binghamton University

Standard fan-in WLCSP has also been offered by TSMC, but was not necessarily a major focus. In addition, pure play foundries see legitimate threat from vertically integrated players such as Samsung and Intel that offer turn-key foundry and package solutions. At the heart of the TSMC InFO development justification would be the success at capturing 100% of the Apple A10 foundry business.

Other wafer foundries such as SMIC and UMC are involved in wafer bumping partnerships as well, getting some wins in the Si Interposer domain. Meanwhile, TSMC has continued to increase its presence in back-end processing including: 1) Wafer bump and test business; 2) Chip-on-wafer-on-substrate (CoWoS) technology for 2.5D interposers; 3) Integrated fan-out wafer-level package (InFO-WLP); and 4) Expansion of WLCSP and wafer bumping.

Similar to the early days of flip-chip with stand-alone wafer bumpers, WLCSP, fan-out WLCSP, 2.5D and 3D has spurred a few companies to emerge. Most of these companies offer (or are preparing to offer) wafer-based package assembly services: DECA Technologies, ALLVIA, TEZZARON/Novati, ANCSi, Tessera/Ziptronix. There are also a couple emerging WLCSP players in China that focus on image sensor and other specialty wafer-based package solutions.

Going forward, we expect wafer foundries and other wafer-based package

solution providers to continue to target the mid-end segment. Some customers may see value in a turnkey/integrated offering from a wafer foundry, but more critically, the emerging of WLCSP and 2.5/3D segments in high volume will eventually lead to additional mid-end offerings by foundries. However, OSATs have a significant head start, and by 2020, will likely capture 45-50% of the wafer-based packaging business, compared to about 35% today. The heavily cited AMD Graphics card comprising 3D TSV and silicon interposer, utilized wafer and back-end packaging solutions at captive, OSAT, and wafer foundry locations (**Figure 2**).

Investment and consolidation

TSMC's 2016 capital spending plan of \$9-10Bn is ten times that of even the largest OSATs. The company expects that about 10% will be for the back-end, most of which is for the InFO package. This scale of investment for wafer-based packaging at TSMC is unprecedented. In the past, perhaps only Intel would have had such large investments within packaging. To keep up with these investment levels, we may see more consolidation of OSATs to compete in this domain. There has already been a major wave of consolidation with both fabless and IDM semiconductor companies.

Typically, as industries mature, participants consolidate to gain market share advantages. Within the electronics industry supply chain, there has been an

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unprecedented wave of consolidation over the past three years, fueled both by lower industry growth, but also by the reserves of cash that companies accumulated coming out of the great recession.

Within the packaging domain, JCET buying STATS ChipPAC is the most notable completed transaction. However, Amkor also completed 100% acquisition of J-Devices, and ASE continues its path toward increasing its share of SPIL. Investment scale for new technology at the fab and now packaging levels will continue to increase in order for companies to remain competitive.

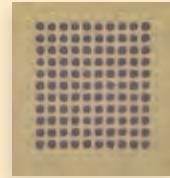
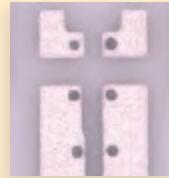
Today, there are two key areas of focus for companies in the packaging world:

1. System-in-package (SiP): This includes a wide range of solutions incorporating multiple die and/or passives into a single package. Most SiPs will continue to be served by the existing OSAT supply base.
2. FO-WLP and WLCSP: These wafer-based processes have opened the door for wafer foundries, and other players to investigate opportunities in package assembly services. In some cases, different processes and or investment levels are required. OSATs still dominate this space as of Q2 2016, but TSMC is investing nearly \$1Bn to make its position clear.

Meanwhile, 3D-TSV and silicon interposer technologies continue to gain selective design wins. The most notable developments have been in the DRAM sector, where Samsung, SKHynix and Micron are all offering 3D stacks of DRAM, often incorporated with a GPU/CPU on a silicon interposer. Much of the DRAM wafer and assembly processes remain captive. However, for most other applications, Prismark expects both IDM and fabless semiconductor companies to look to OSATs and wafer foundries to support this technology evolution.

Biography

Brandon Prior received his BA and BE degrees from Dartmouth College and the Thayer School of Engineering, Hanover, NH, respectively. He is a senior consultant at Prismark Partners LLC; email bprior@prismark.com



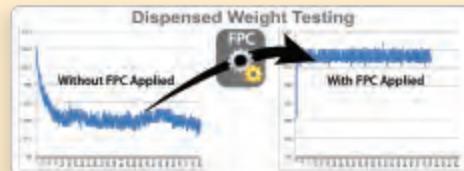
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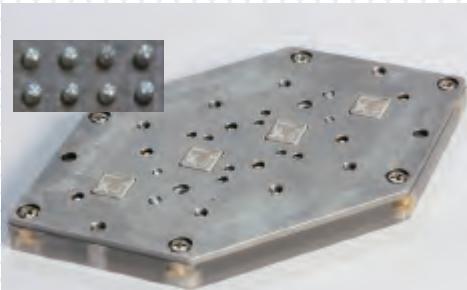
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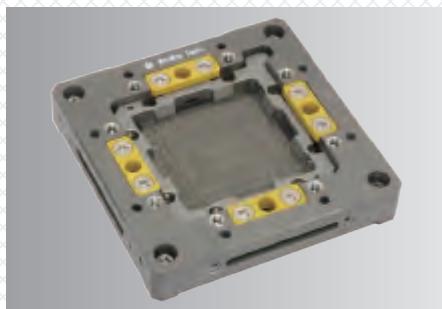
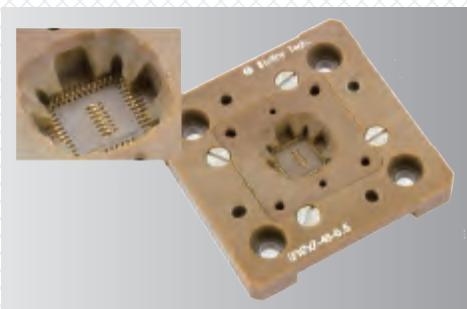
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GUEST EDITORIAL



Not yet a fan of fan-out? Why you should be!

By John Ferguson *[Mentor Graphics]*

Fan-out wafer-level packaging (FO-WLP) is the latest buzz in the semiconductor industry.

Since the announcement [1] in 2014 that TSMC was getting into the FO-WLP game with its InFO process [2], and the news [3] that the company plans to use it this year in production, multi-die assembled packages finally seem to be entering the mainstream with their promise of low cost, small form factors, and low power with high performance. But what exactly is FO-WLP? How do we take advantage of it? What limitations still need to be overcome?

In its simplest form, FO-WLP is a new method for combining multiple die from heterogeneous processes into a compact package (**Figure 1**). It differs from the traditional silicon interposer approach in several key factors:

- While FO-WLP typically requires a silicon wafer as a carrier, it does not remain in the package. Die-to-die and die-to-ball grid array (BGA) connectivity are established through the package redistribution layers (RDL) directly.
- Because FO-WLP doesn't require an interposer, or insertion of through-silicon vias (TSVs), costs come down. You also don't have to worry about the unintended effects of the TSVs on electrical behavior.
- FO-WLP allows a substrate-less package, which provides a smaller vertical footprint. The shorter path to a heat sink also reduces concerns about thermal impacts.
- Thanks to the reduced vertical height gained by eliminating the substrate and the interposer, FO-WLP opens up real estate to place even more components vertically on top. This is achieved with the use of through-package vias (TPVs), which allow

for package-on-package (POP) design. Unlike TSVs, TPVs act much more like the traditional vias you are used to, reducing concerns about yields and reliability. This approach is especially useful for including third-party DRAMs in the package.

Given the above points however, this is not to say that FO-WLP design doesn't present its own set of unique challenges. Historically, package design and integrated circuit (IC) design have been isolated processes. ICs are designed primarily in a Linux operating environment, using electronic design automation (EDA) tools certified by a target foundry or fab and associated with a specific process design kit. System-on-chip (SoC) designs are typically built using primarily Manhattan geometries, and represented in gridded formats like GDSII or OASIS. When finalized, a die abstract (indicating the die's size and the individual pin locations) is passed to a package design team using any one of several formats (LEF, AIF, etc.).

When the IC design is sign-off ready, it is taped out to the foundry for manufacture. The package design community predominantly works with EDA tools designed to run on a Microsoft Windows operating system. Packaging design uses non-Manhattan geometries extensively, and does not often map

nicely to the gridded formats of the IC world. In fact, the two worlds share very few standards in terms of data representation. Package designs, along with the physical die, are historically transferred to a package house or outsourced assembly and test (OSAT) facility using a number of formats, including AIF, MCM, ODB++, and even Gerber. There is typically very little in the form of formal sign-off requirements that accompany the package design, other than a textual document describing the intended design rules.

The introduction of the FO-WLP design approach requires the communication between the IC design world and the package design world to expand beyond the limited interchange described above. To optimize the entire package design, IC designers must know more about the intended package, and package designers must know more about the ICs included in the package. For instance, if you want to optimize the package design for size and/or performance, then you

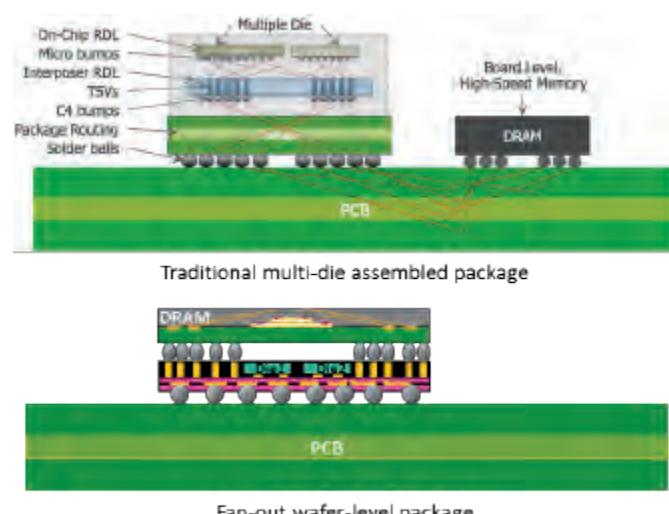


Figure 1: Fan-out wafer-level packaging can significantly reduce the package footprint.

must optimize the whole system, not just the individual elements. An IC designer might be able to design a really small IC, but in doing so, it might be more difficult to connect that die into the package, expanding the package footprint. Similarly, a package designer

providers. Of course, the cost of the license has to be incorporated into the product, something OSATs must consider in their pricing strategy. However, it is very difficult for the OSATs to compete if they all use the exact same recipe.

As a result, all of the major OSATs are developing their own flavors of the FO-WLP process. Add to this the fact that TSMC has entered the game with its own InFO process, and package design companies now have a plethora of production options from which to choose. Determining which offering is best for a given design requirement can be complex. In general, beyond price, product offerings are typically measured by what they can provide in terms of package footprint. Footprint is determined by the minimum vertical height that can be delivered, the minimum horizontal coverage as dictated by the minimum spacing allowed between die,

and the minimum line width and space of the interconnecting redistribution layer (RDL) and BGA pitch.

With the inclusion of TSMC into the market, package designers also have a new wrinkle to configure: OSAT vs. foundry. The primary benefits touted by the foundries are 1) faster turn times due to the ability to share manufacturing lines, 2) single point-of-contact and one-stop shopping, and 3) decades worth of experience in delivering full design kits together with qualified design tools. For example, TSMC is reportedly [4] employing the InFO technology in production this year, meaning they are building and validating InFO design flows, complete with required sign-off requirements, providing designers confidence that the final taped-out package will work with reasonable yields. It is likely that the OSATs will ultimately be required to follow suit in this area, putting more resources into quantifying and validating their manufacturing tolerances.

What is not likely available through TSMC or another pure play foundry

would be the ability to build an assembly based on die produced by multiple foundries. It's not likely, for example, that one would send a die manufactured at Samsung to TSMC to incorporate into an InFO package. On the one hand, using a single foundry eliminates the need to transfer die from a foundry to an OSAT, saving time and ensuring that all the information stays together from start to finish. On the other hand, choosing an OSAT places the burden of ensuring all the components work together (and debugging in the case of errors) on the package designer, to work out through multiple third-party partners. This choice may materially impact pricing of a full FO-WLP package, depending on a foundry's die manufacturing offerings.

What we can say is that it appears whether you target a foundry or OSAT offering, FO-WLP is here to stay. While it does not replace all cases where a silicon interposer is required, it enables a new design methodology with several key advantages of which package designers will likely want to take advantage. You can expect FO-WLP to be a continued area of growth over the next several years, as 3D IC technologies continue to expand.

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Biography

John Ferguson received his BS in Physics from McGill U., and MS in Applied Physics from the U. of Massachusetts, and a PhD in Electrical Engineering from the Oregon Graduate Institute of Science and Technology; he is the Director of Marketing for Calibre DRC Applications at Mentor Graphics; email john_ferguson@mentor.com

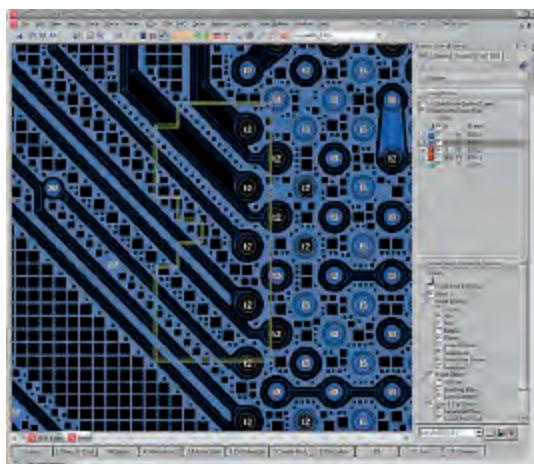


Figure 2: Package integrator tools smooth the lines of communication and enable co-design optimization.

might be able to design a clean and tight package, while making it impossible for the IC designers to get their die I/Os to match specific locations. This is where package integrator tools can be useful (**Figure 2**). These types of tools allow for design co-optimization and help communicate opportunities to both sides.

Fortunately, even though there are few common standards between the two worlds, it does not appear that new standards are required to bridge this gap. Instead, it appears that conversion between data formats may be suitable to meet the needs of all the parties involved, although we will also need tool-to-tool interfaces and communication protocols. While communicating between Microsoft Windows and Linux can be tricky, experience has shown it can be readily achieved using a virtual network connection (VNC).

The first commercially viable FO-WLP methodology is the embedded wafer-level ball grid array (eWLB) approach invented by Infineon. Infineon chose to license its approach, so it is now readily available from most of the leading OSAT

Fresh from the Oven

A black and white photograph of a woman in a kitchen. She is wearing a light-colored short-sleeved shirt and a checkered apron. She is leaning over a white oven, holding a large metal tray filled with numerous small, square, blue-coated items that look like circuit boards or components. She is looking down at the tray. In the background, there is a white stovetop with a pot on it.

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INDUSTRY NEWS

10 BEST semiconductor equipment supplier rankings for 2016

VLSIresearch Customer Satisfaction Survey announces 10 best semiconductor equipment supplier rankings for 2016. Teradyne, Advantest, Advanced Dicing Technologies, Plasma-Therm, and Axicelis achieve ratings above 9.0 in the 2016 10 BEST.

19 of the 20 10 BEST suppliers have achieved greater than an 8.0 rating this year. Large Suppliers increased ratings in nine categories. This resulted in two suppliers having achieved ratings at 9.0 and above. Focused Suppliers made great strides with improvements in twelve categories, an increase from nine last year. Two of these were in usable performance and quality of

results, areas where Large Suppliers fell behind. Congratulations to the 2016 10 BEST winners!

About the 2016 VLSIresearch Customer Satisfaction Survey

VLSIresearch received feedback from more than 95% of the chip market and 80% of subsystems customers for this year's survey. The survey spans two and half months and covers five languages. Worldwide participants were asked to rate equipment suppliers among fifteen categories based on three key factors: supplier performance, customer service, and product performance. 3,619 surveys were returned, resulting in 54,282 total responses.

The VLSIresearch annual Customer Satisfaction Survey is the only publicly available opportunity since 1988 for customers to provide feedback for suppliers of semiconductor equipment and subsystems. The 10 BEST, THE BEST, and RANKED 1st awards provide special recognition to suppliers that are rated highest by their customers.

10 BEST awards recognize each chip making equipment supplier as a whole, regardless of product type:

- Fab, Test, and Assembly equipment ratings are grouped together for an overall rating for each supplier
- Each supplier is then listed in one of

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 <p>10 BEST Equipment Suppliers 2016</p>			
10 BEST Segment	Rank	10 BEST CHIP MAKING EQUIPMENT SUPPLIERS OF 2016	10 BEST Rating
L A R G E	1	Teradyne	9.26
	2	Advantest	9.12
	3	ASML	8.93
	4	Hitachi Kokusai Electric	8.80
	5	ASM Pacific Technology	8.56
	6	Tokyo Electron	8.51
	7	Hitachi High Technologies	8.13
	8	Applied Materials	8.12
	9	Lam Research	8.09
	10	KLA-Tencor	7.91
F O C U S E D	1	Advanced Dicing Technologies	9.25
	2	Plasma-Therm	9.13
	3	Axcelis Technologies	9.11
	4	F&K Delvotec	8.95
	5	Evatec	8.76
	6	Xcerra	8.70
	7	SPTS Technologies, an Orbotech Company	8.53
	8	EV Group	8.31
	9	HANMI Semiconductor	8.10
	10	ACCRETECH - Tokyo Seimitsu	8.01

SOURCE: VLSIresearch's 2016 Customer Satisfaction Survey. Copyright © 2016 VLSI Research Inc. All rights reserved.

two categories based on a three-year average of total revenues for all its market segments: **Large** and **Focused**

THE BEST awards recognize the more detailed markets:

- Fab, Test, Assembly equipment, and Subsystems

RANKED 1st awards place special distinction on suppliers that achieve the highest rating from customers in any survey category, including:

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Advanced testing technology for emerging automotive applications

By Dan Stillman [[Texas Instruments](#)] and Amy Leong, Ashish Bhardwaj [[FormFactor, Inc.](#)]

The IC content in automobiles has been steadily increasing for the last twenty years. Emerging automotive applications in the areas of mobile connectivity, automotive safety and electrically powered vehicles are expected to drive that content well beyond its current historic level. Many of these new applications, especially those in the area of automotive safety and electrical power will require extremely high levels of performance and reliability in harsh operating environments. FormFactor and Texas Instruments recently collaborated in a study designed to address some of the testing challenges presented by these new applications. This paper discusses select results from the study.

Automotive semiconductor growth

The automotive sector is one of the fastest growing segments in the semiconductor industry. According to an IC Insights report [1], the ICs used by the automotive industry are expected to expand at a compounded annual growth rate of 6.7% from 2014 to 2019. As shown in [Figure 1](#), the automotive segment is predicted to grow faster than any other semiconductor market segment during that time period, such as communication, computer and consumer end-applications.

One of the main reasons for this notable automotive segment growth is that the automotive industry, worldwide, is undergoing some profound changes that are driving an increased dependence on semiconductors. The demand for increasingly versatile electronic systems listed below is believed to be a key driver behind this growing use. These include:

Automobiles with mobile connectivity. Consumers are demanding expanded access to mobile digital content while driving. This trend has required the development of application-specific ICs that can provide a safe and secure merger of the two sectors.

Environmentally friendly cars. The slow, but steady growth of the electric

car market is also helping to drive increased semiconductor demand from the automotive industry. Application-specific semiconductors play a critical role in delivering the high energy requirements needed to make electric vehicles a practical and environmentally friendly alternative to those powered by internal combustion engines.

Increased automotive safety. The trend of including advanced driver assistance systems (ADAS) in automobiles, which provides automated driving assistance in difficult conditions, has also helped drive automotive IC content specifically designed to provide the high reliability sensing and reaction capabilities required by ADAS systems.

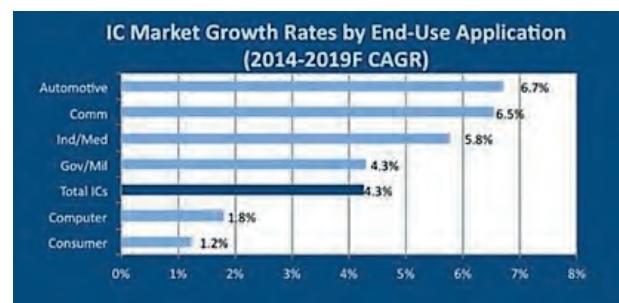
Gartner projects [2] that the increasing semiconductor content in automobiles will drive the worldwide automotive semiconductor market from its all-time high of \$30 billion in 2014 to \$40 billion by 2019. This level of growth makes the automotive market highly attractive to many semiconductor manufacturers, because it is seen as being steadier and less cyclical than the consumer and mobile semiconductor markets. This highly positive growth outlook is, in part, predicated on the assumption that the future vision of driverless and fully automated cars will soon become reality.

Emerging auto IC test applications

These new automotive electronic systems will require specialized ICs that have been tested to guarantee the highest levels of performance and reliability [3]. These various applications will require a range of ICs including these examples:

Advanced driver assistance systems (ADAS). This application provides the latest technology advancements for driver awareness and safety. It requires processors with digital signal processing (DSP) capabilities to enable multiple vision and radar systems for applications like lane departure warning, rearview and surround view camera systems, collision warning and avoidance, as well as blind spot detection. It also requires a fully integrated system-on-chip (SoC) for ultrasonic parking assistance, FPD-Link connecting standard cameras and megapixel cameras via thin, as well as light and cost-optimized cables, which can reduce the weight and complexity of the wiring harness without sacrificing performance.

[Figure 2](#) highlights some of the ADAS



[Figure 1](#): IC Market growth rates by segment, 2014-2019. SOURCE: IC Insights, Inc.



[Figure 2](#): Some of the latest automotive applications requiring leading-edge IC technology.



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Typical Applications

Semiconductor Packaging

- Medical Imaging
- Multichip Modules
- 3D / 2.5D Packaging
- Wafer Scale Packaging
- RF / Microwave Modules

Photonic Packaging

- Optical Engines
- LED Assemblies
- Laser Diode Bonding
- Active Optical Cables
- Silicon Photonic Packaging

MEMS Assembly

- IR Sensors
- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

functions currently being produced for that sector by Texas Instruments [3].

Body electronics and lighting. The central body controller supervises and controls the functions related to the car body, such as lights, windows and door locks. It also serves as a gateway for controller area network (CAN) and local interconnect network (LIN). TI's portfolio of products includes solutions for power management, signal-chain, interfacing, load drivers, RFID functions, and DSP/microcontrollers. **Figure 3** shows ICs designed to address some of these applications [3].

Hybrid/electric power train systems. ICs also provide analog and embedded processing solutions for improved performance and safety throughout the hybrid/electric power train systems. Solutions include battery management and charging systems, fully integrated plug-in electric vehicle management systems, and start/stop functionality. **Figure 4** highlights a TI ASIC designed for such applications [3].

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Figure 3: TI provides a range of ASICs to meet body electronics and lighting needs.

Automotive 60W Brushless DC Motor Drive Reference Design

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- Drives 3-phase Brushless DC (BLDC) motors up to 60W with no position sensors required
- Easy to get started with MotorWare software

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Figure 4: TI's 60W brushless DC motor drive.

Infotainment and cluster. Applications are widely used in designing cluster, head unit, human-machine interface (HMI) display or other infotainment system components [3].

Safety. ICs are now being used in a wide range of automotive safety applications that include stability control and anti-lock braking systems; electric power steering systems; airbag, occupant detection and alarm systems; and ADAS [3].

Stringent automotive IC test requirements

ICs used in automotive applications must adhere to the highest performance and quality standards to ensure the safety of both the driver and passengers. As a result, ICs used in these applications must be tested more rigorously and under more extreme conditions than ICs used in most mobile and consumer applications as noted in the following paragraphs.

Harsh outdoor environment. The electronics incorporated into an automobile, or one of its subsystems, will be expected

Automotive Rear Lamp EMC Reference Design

- Three TPS92630 connected together by FAULT bus to drive 9 LED strings with 100mA current each string
- Car battery directly connected and full test in Qualified Automotive EMC Lab
- Ideal results for Tail Light, Stop Light and Turn Light

TI Designs

the electronics it deploys, the automotive industry expects zero defects, both for safety and economic reasons. IC manufacturers participating in that sector are expected to use a defective parts per million (DPPM) design methodology and manufacture their products using a zero-defect process technology that minimizes early life failures and ensures long mean-time-between-failure (MTBF). Even a 1ppm IC failure rate can translate to a 1.5% or 15,000ppm failure rate at the automotive level—a rate that can result in a massive recall and serious economic distress for an automotive manufacturer. As a result, automotive IC suppliers are strongly motivated to achieve a goal of zero defects if they want to maintain or grow their share of the automotive IC market.

Automotive probe card requirements

The need for zero defects and the harsh automotive environment create certain challenges for back-end wafer test probing. FormFactor and TI have worked together to address some of these challenges by leveraging FormFactor's latest vertical MEMS probe card product Katana™. The two biggest issues concern maintaining thermal agility for wide temperature range probing, and ensuring minimum pad damage with no dielectric punch-through. This section will discuss those challenges and how they were addressed.

Thermal agility for wide temperature probing. The various effects of wide temperature probing are summarized below. This study shows that the new probe card can achieve stable electrical and mechanical performance at both cold and hot temperatures. This allows customers to use the same probe card design over a wide temperature range, resulting in a significant reduction in cost-of-test.

1) X,Y and Z movement of probes: Because of the safety nature of many of the semiconductor applications used by the automotive industry, the industry demands that the ICs intended for its use are broadly tested over a wide temperature range (-40 to 140°C) to ensure reliable performance. Thermal stresses due to high temperature (140°C) not only cause the wafer pads to shrink, but also add to the testing complexity by affecting the X, Y and Z position of the probes testing the wafer [4,5].

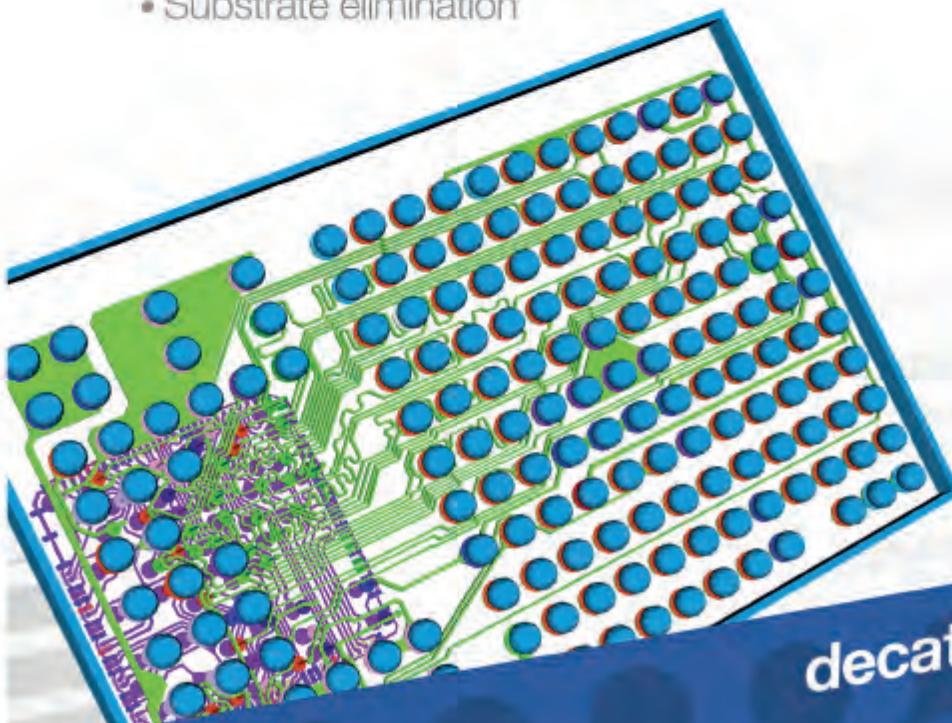


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Thermal stress acts on various components of a probe card including printed circuit boards (PCBs), mechanical hardware and probe head components (such as guide plates, metal stiffeners and probes). As a result, the probe position can change, negatively affecting test accuracy [4,5].

It was found that the most effective way to minimize the effects of high temperature in wafer testing is to modify probe card construction. The necessary modifications include, selecting MEMS probe materials that are minimally affected by temperature change, as well as implementing scaling in the probe head design that negates temperature effects on the other probe card components. Various steps taken during IC production, including introduction of soak times (placing the probe card near the wafer for a short period prior to testing to attain thermal equilibrium), realignment of the probe card, changing the distance between chuck and the probe card, and changes in the stepping pattern, can all reduce the effect temperature has on probing accuracy [4, 5].

It was found that it was possible to control the movement of probes by introducing effective scaling in the probe head design to compensate for heat-induced PCB stiffness and the thermal expansion of the mechanical hardware. **Figure 5** highlights the production data showing the X, Y and Z movements at a temperature range of -40°C and 140°C. It also shows the relative chuck height. The correction in X, Y and Z (Cx, Cy and Cz) are relative to the scale on the left side of the graph (in μm). The absolute planarity (Z) and auto Z are relative to the scale on the right side of **Figure 5** (chuck height in μm). The black dotted lines represent a new wafer and the green dots (INDEX) represent a new die. During the initial setup, the Auto Z (electrical contact) shown by the red dotted line is attained and the relative chuck height value is stored. Temperature causes X, Y and Z movements on the probe card and the prober performs the optical alignment to change the value of the absolute chuck height (Z) with respect to corrections [6].

The soak process is not used in the process described above to compensate for the effects of temperature—instead, the optical alignment method is used

to provide correction to the movement. Optical alignment by the prober is done every 6 minutes in the first hour and every 15 minutes after the first hour. This schedule accounts for the fact that in the first hour, the movement in the Z direction is tremendous and therefore, the correction Cz is of higher magnitude. Therefore, the frequency of the alignments is more in the first hour until the probe card attains thermal equilibrium and has stable movements. As shown in **Figure 5** at 140°C, the correction Cz is about 60 μm until the thermal equilibrium is achieved.

Figure 5 also shows that X, Y and Z optical movement is under 10 μm for the data collected across 35 wafers at -40°C, and that the X, Y and Z optical movement is under 20 μm for the data collected across 9 wafers at 140°C. This demonstrates that only a minimal correction is needed in all directions to compensate for the thermal effect. As a result, once the vertical MEMS Katana probe card achieves thermal equilibrium, probe movement is minimal for both cold and hot temperature.

2) Stable CRES with increase in temperature. The other major challenge to probing with a wide temperature range (especially at high temperatures) is maintaining stable contact resistance (CRES). Generally, an increase in temperature will cause the aluminum pad to soften and oxidize, resulting in an aluminum oxide formation on the pads, which degrades probe tip contact performance. This situation requires aggressive cleaning and, in turn, reduces the lifetime of the probe card. The new product provides a unique anti-wear probe tip material (PA2 material) to extend product lifetime, while achieving stable CRES by gently scrubbing through aluminum oxide.

Minimum pad damage/no dielectric punch-through. Probe-induced dielectric cracking or punch-through is an ongoing test industry issue. Damage to Cu/low-k devices during fabrication, wafer probe, and assembly is a long-term reliability concern. Current leading-edge process

technologies are using low-k materials, which tend to have a lower modulus of elasticity and easily fracture, resulting in a greater probability of cracking.

In automotive applications, it is common to rate wafer probe cards according to a certain number of probe tip touchdowns on wire bonding pads. The tests conducted at TI used an 11-touchdown standard to ensure the highest reliability and to confirm that no dielectric cracking or punch-throughs occurred during probing.

When it comes to vertical probe technologies, two key factors — probe contact force and scrub mark size — have been shown to significantly affect pad cracking.

1. Desired probe force: FormFactor's Katana pointed tip probe, used in the study, delivered a probe force ranging between 1.8 grams and 2 grams at a production overdrive of 75 μm . The graph in **Figure 6** shows 1.9 grams of probe force measured for the data collected for 1.5M touchdowns for 6 probes.

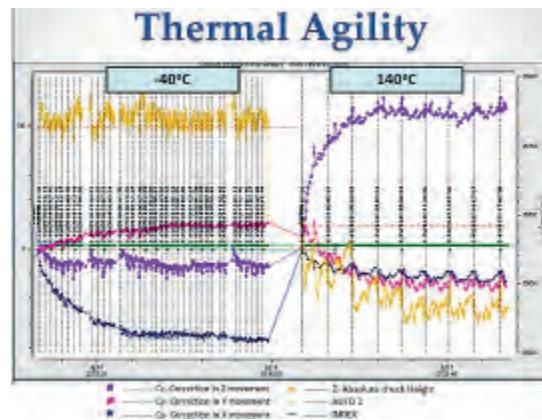


Figure 5: X, Y, Z movements at a wide temperature and relative chuck height.

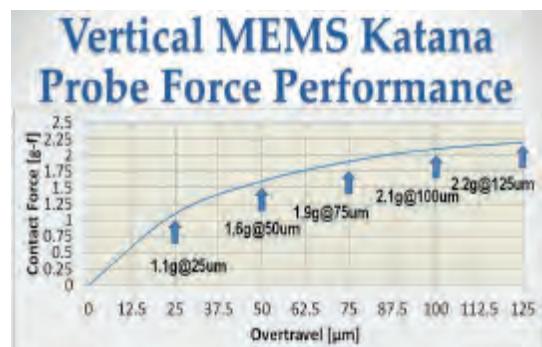


Figure 6: Probe force performance of FFI's Katana Vertical MEMS probe after 1.5M cycles.

	TD1	TD2	TD3	TD4	TD5	TD6	TD7	TD8	TD9	TD10	TD11
FormFactor Katana Technology	No	No	No	No	No	No	No	No	No	No	No
Other vertical pointed tip technology	No	No	No	Yes, under pads cracked							

Table 1: A comparison of FFI under-pad cracking results with that of alternative vertical pointed tip probe technology.

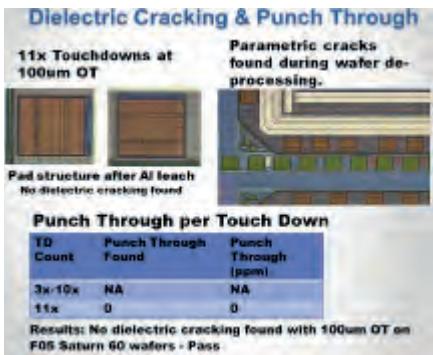


Figure 7: The illustration highlights the FFI probe's ability to test even highly sensitive dielectric materials without damaging the dielectric layers.



Figure 8: FFI's Katana vertical MEMS probes demonstrate small probe mark size at production overdrive.

2. Consistent probe mark size: The new MEMS fabricated pointed tip probe card used in the study provides a consistent $13\mu\text{m}$ probe tip size. In contrast, a typically mechanically-shaped pointed tip probe card can have tip size variations from $10\mu\text{m}$ to $20\mu\text{m}$ throughout the usage and on-line cleaning cycles. Such probe tip size variations impose a difficult balancing act to minimize pad cracking, while maintaining adequate probing pressure to ensure contact stability. Additionally, frequent and

laborious offline tip-reshaping is also required to maintain tip size in the range, adding further maintenance cost.

FormFactor's Katana MEMS pointed tip probe, by contrast, has a constant probing pressure on the pads. This allows the wafer probing process to operate in the normal prober mode, while the other mechanically-shaped pointed tip products would require a 5SVC (5 speed variable control) prober mode to minimize impacts of high probing pressure variation. The 5SVC mode reduces the speed and acceleration of the prober chuck movement to minimize pads damage at the expense of increased test time. Therefore, the low constant pressure advantage of the Katana MEMS fabricated pointed tip probe minimizes pad cracking, while also reducing the test time and frequent offline maintenance required to reduce cost of test.

Table 1 and **Figures 7** and **8** show the results from a study conducted on a TI test chip that is highly susceptible to dielectric pad cracking. The study found no dielectric punch-throughs after 11 touchdowns using FormFactor's MEMS pointed tip product, while the mechanically shaped pointed tip product showed cracking after 3TDs even with 5SVC prober mode.

Summary

Emerging automotive applications in the areas of safety, connectivity and electrical power are likely to be the next big area of growth for the semiconductor industry. Many of these new applications, however, present unique challenges for wafer probing, due to formidable

dynamics like wide temperature ranges and stringent under-pad cracking requirements to ensure "zero defect" IC performance goals. This study — a collaboration between Texas Instruments and Form Factor — found that low-force vertical MEMS probe technology and advanced probe card construction design techniques can help to overcome the challenges, while improving production flexibility and uptime.

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Chips “face-up” panelization approach for fan-out packaging

By Boyd Rogers, Debbie Sanchez, Craig Bishop, Cliff Sandstrom, Chris Scanlan, Tim Olson *[Deca Technologies, Inc.]*

This paper describes a chips “face-up” approach to panelization, the process in which die are embedded in mold compound to effectively grow the die surface and to create a panel for supporting redistribution layer (RDL) buildup. In this approach, die with preformed Cu studs are placed face-up on a carrier, using a high-speed pick-and-place tool to achieve high throughput and low cost. The front and sides of the die are then covered with mold compound using compression molding. The molded panel is debonded from the carrier, and the front surface is ground to reveal the Cu studs, which provide current pathways from the chip I/Os to the mold compound surface. A high-speed optical scanner is used to inspect the Cu studs protruding through the mold compound, to determine the actual position of every die on the panel. This information is fed into a proprietary Adaptive Patterning™ design tool, which adjusts the fan-out unit design for each package on the panel to match actual die locations. Finally, the design files for each panel are imported to a lithography machine that uses the design data to dynamically apply a custom, Adaptive Pattern to each panel during the fan-out build-up process. The result is a panelization process that can deliver high yielding panels with high throughput and low cost and with a planar surface capable of supporting high-density RDL wiring.

This paper details challenges and benefits of this chips face-up approach and describes these new patterning strategies used to compensate for die displacement in the molded panel and thereby achieve high panel yield.

Introduction

The handheld consumer electronics space, where portability and increasing functionality are strong drivers, continues to motivate the transition to packaging approaches that provide small size, high performance, and low cost. Wafer-level chip-scale packaging (WLCSP), which offers the smallest packaging form factor, has

often been a preferred option for addressing the handheld market. In WLCSP, chip I/Os are generally fanned-in across the die surface using polymer and redistribution line (RDL) buildup layers to produce an area array, and large solder bumps are formed at the terminals by ball drop or plating. These additive processes allow the chip to be attached directly to a PCB with high reliability. However, two progressions in front-end chip manufacturing bring challenges to packaging in a WLCSP format: 1) die shrink, enabled by advancing semiconductor technology nodes, makes it increasingly difficult to fit all of the large solder ball I/Os on the die surface; and 2) increasing chip functionality produces a need for more I/Os, also making WLCSP packaging more difficult. One approach to extending WLCSP is to shrink the size of the I/Os or solder bumps on the chip surface so that more can fit within the chip area. However, this approach is generally limited by a lack of assembly infrastructure, design rule limitations in end application PCBs, and higher assembly costs with the smaller, tighter pitch I/Os [1].

Fan-out, or FOWLP has been offered for a number of years as an alternative for addressing constraints to WLCSP [2,3]. In this technology, chips are singulated and then embedded in a molded panel, a process referred to here as panelization. A common method for forming this panel is to place the chips face-down on a carrier at a desired pitch and then mold over them using compression or print molding. The molded panel is subsequently separated from the carrier. The panel is often formed in the shape of a wafer, so that standard wafer processing techniques can be used to create buildup layers on the panel surface. The extra panel surface around the chip allows I/Os to be both fanned in over the chip and fanned out across the mold compound, thus accommodating a larger number of I/Os. After buildup layer processing and solder ball attachment, the packages undergo backgrinding, laser marking, and singulation,

just like WLCSPs. The resulting package is often just slightly larger than the chip and just large enough to accommodate the I/Os. Like WLCSPs, the package is ready to be mounted directly to an end application PCB.

The potential benefits of FOWLP are numerous. This technology provides the smallest possible form factor for packaging small, high I/O chips that cannot be packaged as WLCSPs. As with WLCSPs, the device-to-board connections through thick copper routing layers and large solder balls offer excellent electrical properties and performance. When hitting acceptable cost and yield targets, FOWLP can potentially displace other forms of packaging, such as flip-chip or wirebond ball grid arrays (BGAs). In those cases, it generally brings a size advantage and eliminates the need for custom substrates, significantly simplifying the supply chain. Finally, FOWLP enables the connection of two or more chips in the fan-out routing layer, facilitating multi-chip and system-in-package (SIP) applications [4-7].

Cost, yield and reliability issues have effectively limited the widespread adoption of FOWLP despite its promise. Placing singulated chips on the carrier to form the molded panel requires high placement accuracy. Any misplacements can lead to pattern overlay difficulties in the buildup process on the reconstituted panel. The requirement for high placement accuracy restricts throughput at the pick-and-place operation, leading to high process costs. During the molding operation and mold cure, die drift or movement can occur. This die drift can further complicate pattern overlay matching in the buildup process on the panel and can result in yield loss when the drift is excessive. Addressing or overcoming die offset and resulting overlay issues is one of the keys to making FOWLP competitive with other package formats.

Other challenges are posed by performing the fan-out routing over a surface that is partially composed of silicon and partially of mold compound. These challenges are

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illustrated in **Figure 1** for a conventional FOWLP structure. To avoid potential mold flash on the active surface during molding, the die are compressed into the release tape on the temporary carrier. The

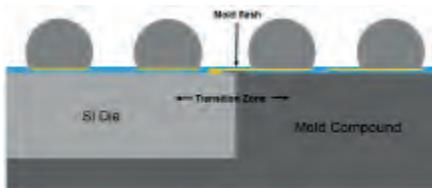


Figure 1: Illustration of a conventional FOWLP structure, showing the transition zone between silicon and mold compound on the package front surface.

discontinuity posed by the transition between the silicon chip and the mold compound at the die surface can result in a topography step that is difficult to route over with the RDL, even with substantial smoothing of a base polymer layer. Laser grooving and sawing of the native silicon die can result in upwardly protruding metal that can short to the RDL routed over the die edge. Finally, the coefficient of thermal expansion (CTE) mismatch between the silicon and the mold compound can result in stress in the fanout RDL structure and potential fracture of the RDL during reliability stressing.

Chips face-up panelization approach

This paper describes a chips face-up approach to panelization that addresses many of the key issues associated with conventional FOWLP technology [8]. The chips face-up FOWLP structure is illustrated in **Figure 2**. In this approach, the front surface of the die is fully protected by a thin layer of mold compound, eliminating issues associated with the silicon/mold transition and resulting in a more robust package. Pre-formed Cu studs provide current pathways from the chip I/Os to the mold compound

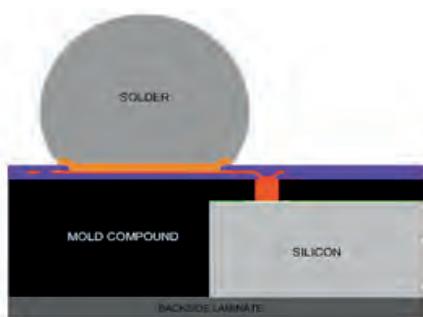


Figure 2: Illustration of the chips face-up FOWLP structure.

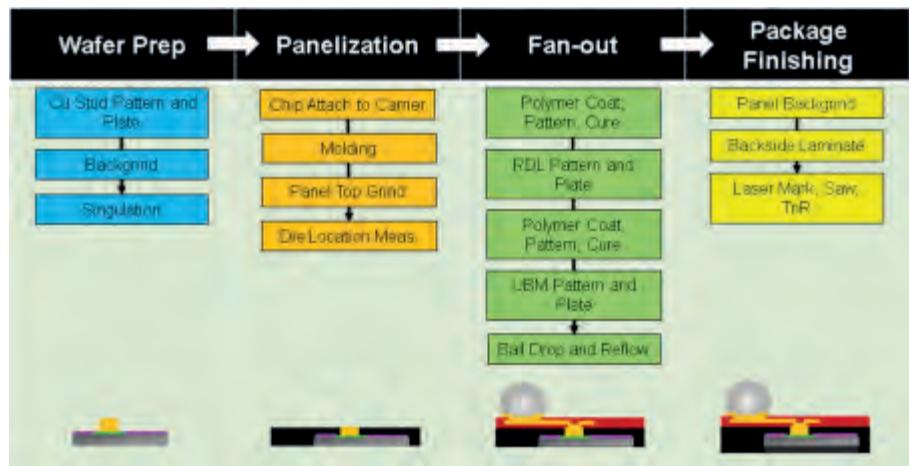


Figure 3: Process flow for chips face-up approach.

surface. A technology called Adaptive Patterning allows routing of the fan-out layers to the Cu stud locations, even with substantial die shifts. This new patterning technology can facilitate tighter ground rules, higher yield, and lower overall costs.

The process flow for the chips face-up FOWLP is shown in **Figure 3**. In the first segment of processing, termed “wafer prep,” Cu studs are fabricated on the native wafer by sputter-depositing seed layers, patterning a thick photoresist, plating Cu studs, and then performing strip and etch of the photoresist and seed layers. In the second “panelization” segment, the chips are singulated and attached to a carrier face up. Overmolding is applied, and the newly formed panel containing the chips is debonded from the carrier. The panel is then top ground to reveal the Cu studs. Finally, an optical scanner is used to measure the location of each die on the panel to enable the new patterning technique described later. Following panelization, fan-out processing is performed on the molded panel. This includes patterning and curing a polymer layer, patterning and plating Cu RDL, processing a second polymer layer, and, optionally, patterning and plating under bump metallization (UBM) pads. Ball drop and reflow are then performed. Finally, panel backgrind is performed and a backside laminate is applied, followed by laser mark, package saw, and tape and reel.

A cross section of the chips face-up FOWLP structure is shown in **Figure 4**. With the addition of the backside laminate, the chip has been completely encased in epoxy, forming a robust package, and the discontinuity at the die edge, which exists on conventional FOWLP structures, has been eliminated.

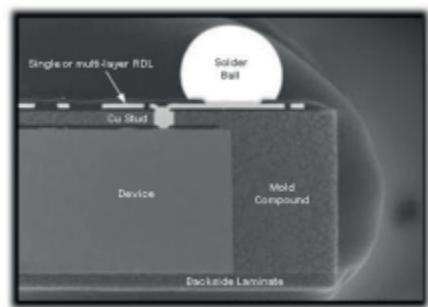


Figure 4: Cross section of a fully fabricated structure.

Wafer prep

The face-up panelization approach starts with Cu stud fabrication on the native wafer. Because this is an added process in the face-up flow, requirements include yields approaching 100% and low cost of fabrication. Key to obtaining high yields are good photoresist patterning integrity and advanced wetting techniques at Cu plating to insure good plated deposits in all photoresist template openings. Low cost is enabled by the use of dry film for photoresist patterning. An approximately 2:1 aspect ratio in resist thickness to Cu stud diameter can be achieved with the dry-film patterning process.

Additional cost reductions can be realized by utilizing high-speed Cu stud plating and by minimizing the required Cu plating height. The target plating height for the Cu studs must be safely above the height in the final structure, which is equal to the frontside mold thickness. Overplating is required to take into account three tolerances: 1) Cu stud plating nonuniformity; 2) silicon backgrind tolerance; and 3) tolerance of the top grind step used to reveal the Cu studs. Assuming these are all independent factors, the required target plating height is approximated by:

$$CSH \approx \frac{2MT + \text{Sqrt}((2MT)^2 - 4(1 - CSU^2)(MT^2 - BGT^2 - TGT^2))}{2(1 - CSU^2)}$$

where CSH = Cu stud as-plated height

MT = Final mold thickness target

BGT = Backgrind tolerance

TGT = Panel top grind tolerance

CSU = Cu stud plating uniformity

Minimizing the grind tolerances and the Cu stud plating nonuniformity are keys to reducing the Cu stud plating height and minimizing costs. A Cu stud in the final molded structure is shown in **Figure 5**. After Cu stud fabrication, the wafers undergo backgrind and singulation in preparation for the panelization process.

Panelization

Panelization starts with chip attach of the singulated die onto release tape on a temporary carrier. In the face-up approach, chips are placed on the release tape with the Cu studs facing up. Because chip attach is a serial process, it can constitute a significant percentage of the total costs associated with fan-out technology. The interplay between placement speed, placement equipment type and cost is illustrated in **Figure 6**. For traditional fan-out technologies, high yield often requires high placement accuracy, which in turn requires slow and relatively expensive high-accuracy die bonders. In this example, the chip shooter represents a typical surface mount technology (SMT) placement machine with a wafer feeder for die pick and place. Such tools may be configured with different placement heads, with the lower speed heads placing at higher accuracy and higher speed heads at lower accuracy. Placement accuracy on such tools ranges from $\pm 8\mu\text{m}$ to $\pm 25\mu\text{m}$ at 3σ . A typical flip-chip bonder is assumed to cost 28% more than the chip shooter, with placement accuracy ranging from about $\pm 5\mu\text{m}$ to $\pm 10\mu\text{m}$. The high accuracy bonder represents a class of equipment with lower throughput, but with placement accuracy of $\pm 2\mu\text{m}$ or less at 3σ and equipment cost 2.8 times higher than the chip shooter. All tools are assumed to occupy similar floor space and consume similar labor and facilities resources.

The requirement for higher placement accuracy to achieve high-yield results in a precipitous increase in the cost per unit. On the other hand, relaxing placement accuracy to facilitate higher placement speeds can significantly reduce part costs. Adaptive Patterning can be used to ease placement accuracy requirements at chip attach by up to an order of magnitude, allowing for higher placement speeds and lower costs, while at the same time improving overall fan-out yield.

After chip attach to the carrier, compression molding is used to form the fan-out panel. An epoxy molding compound with a high silica filler content is used, to closely match the thermal expansion coefficient of the silicon chips. Molding parameters must be optimized to eliminate surface voids and incomplete molding, as well as to minimize die shift. Keys to controlling die shift include optimizing the adhesion of the die to the release tape and optimizing the mold dispense pattern.

During the molding process and post mold cure, some die shift is generally unavoidable due to mold flow and mold shrinkage [9]. Die shifts from these sources are often predictable and can be compensated for at chip attach. To compensate for linear shifts with a single-die package, the placement pitch at chip attach can be adjusted such that:

$$\text{Placement pitch} = \text{nominal pitch X (1 + comp factor)}$$

where “comp factor” is the mold shrinkage compensation factor. For the mold compound used in this study, the mold shrinkage compensation factor has been measured for various single chip packages as a function of the fan-out ratio, defined as the total package area divided by the silicon chip area. **Figure 7** shows a plot of this dependency. For low

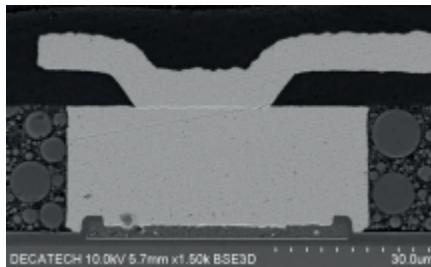


Figure 5: Cross section of a Cu stud in the final molded structure.

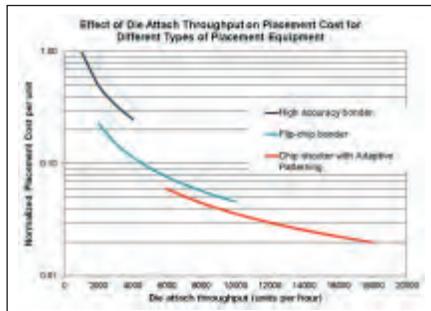


Figure 6: Approximate normalized placement cost as a function of placement rate and equipment type.

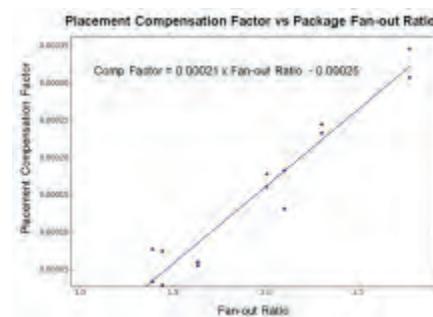


Figure 7: Mold shrinkage placement compensation factor as a function of the fan-out ratio for various single-chip packages.

fan-out ratios, the compensation factor is small and almost negligible, while at higher fan-out ratios, the larger amount of mold compound causes die shift to become significant. By effectively compensating for mold-induced die shift at chip attach, improvements in post-mold yield can be achieved.

Once molding is complete, the molded panel is separated from the temporary carrier. A top grind process is used to reveal the Cu studs and to set the final front side mold thickness. Control of the grind tolerance is important at this step, as well as producing a good finish on the molded top surface to accommodate fan-out processing.

Finally, to prepare the panel for the Adaptive Patterning process, an optical scanner is used to inspect the Cu studs protruding through the mold compound for each die, to determine the actual position and rotation of every die on the panel with respect to the ideal design frame of reference. Summary data from this type of measurement for a 3mm X 3mm package is shown in **Figure 8**. In this example, X and Y shifts have been controlled through the chip attach and molding processes to approximately $\pm 20\mu\text{m}$ and angular rotations to ± 0.2 degrees. Shifts such as these can be readily compensated for with this new patterning process.

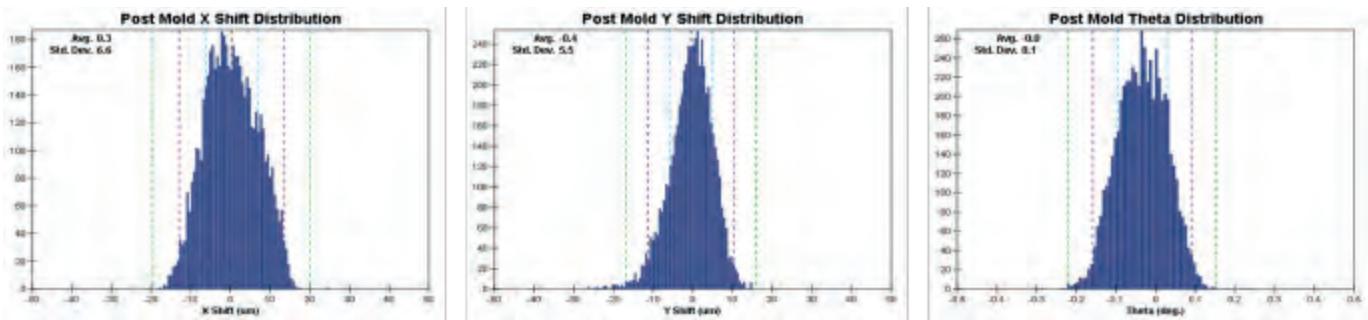


Figure 8: Measured X, Y, and angle shifts from chip attach and molding for a 3mm X 3mm package on a 300mm panel.

Correcting for die shifts

Adaptive Patterning has been developed to correct for die shifts inherent in fan-out processing [10]. This new patterning process works by dynamically adjusting one or more build-up layers to accurately connect to the Cu studs protruding through the mold compound for each individual die in the molded panel. The flow for this new process is summarized in **Figure 9**. The measurements of each die location

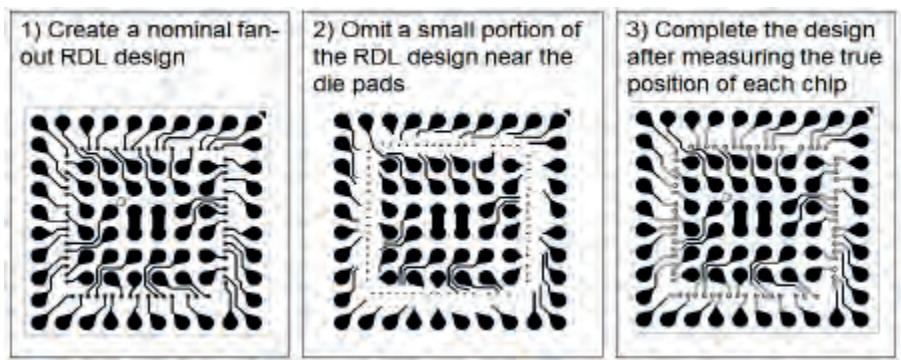


Figure 10: Process for creating Adaptively Routed via1 and RDL fan-out layers.

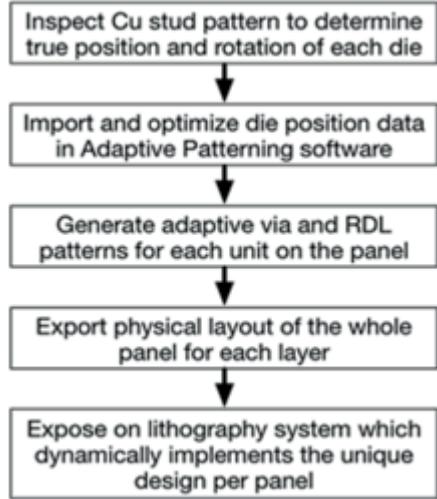


Figure 9: Adaptive Patterning flow.

and orientation on each panel are fed into a proprietary software system. This system adjusts the fan-out unit design for each package on the panel so that the first via layer and fan-out RDL pattern are properly aligned to the studs on the die. The design files for each panel are imported to a lithography machine that uses the design data to dynamically apply a custom pattern to each panel.

Two types of new patterning strategies are currently deployed. One, called Adaptive Routing, is illustrated in **Figure 10**. For this type of routing, a nominal fan-out RDL design is created. Then, a partially routed RDL layer called a prestratum is formed by omitting

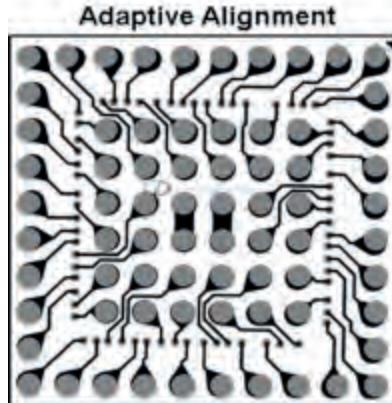


Figure 11: Process for creating Adaptively Aligned via1 and fan-out RDL layers.

a small portion of the RDL layer in close proximity to the Cu studs. After scanning the panel to measure the actual position and orientation of each unit, the design of each unit on the panel is completed to connect the prestratum pattern to the Cu stud pads and their corresponding dielectric vias. The adaptive region in which the RDL traces are allowed to dynamically change is typically on the order of 100 μ m to 200 μ m.

A second type of patterning referred to above, called Adaptive Alignment, is illustrated in **Figure 11**. In this approach, the whole RDL pattern and via1 layers are shifted to account for the actual die position and rotation. The via2 and ball locations remain on a fixed BGA

grid. To compensate for the shifting RDL pattern, the RDL BGA pad is oversized or the via2 under the bumps is undersized.

The two types of Adaptive Patterning can also be used in concert, when appropriate. **Figure 12** shows a two die package, in which Adaptive Alignment has been used to compensate for each die position separately, while Adaptive Routing has been used to complete traces between the two die.

Figure 13 shows the yield map corresponding to the shift data for the 3mm X 3mm package in **Figure 8**. In this case, Adaptive Alignment has been used to fully compensate for the measured die shifts, resulting in almost 100% post-mold yield.



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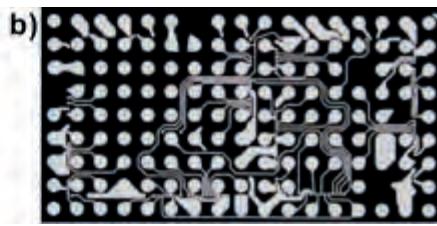
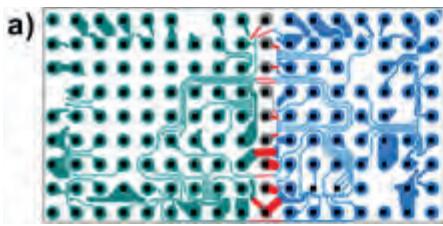


Figure 12: A two-die package utilizing two types of Adaptive Patterning. In image a), green and blue RDL areas over the die are aligned using Adaptive Alignment, while traces are adjusted in the red area of routing between the two die by Adaptive Routing; grey areas are non-adaptive. Actual RDL layers are shown in image b).

Fan-out processing

After the Adaptive Patterning design files are created, fan-out processing can commence. The build-up proceeds through polymer 1, RDL, polymer 2 and UBM layers, with the lithography system implementing unique designs at the polymer 1 and RDL layers on a per panel basis. Finally, ball attach and package finishing are performed to produce singulated fan-out packages.

A cross section of the chips face-up FOWLP package mounted to a printed circuit board is shown in **Figure 14**. The device chip is completely encased, forming a robust package, and the discontinuity at the die edge that exists on conventional FOWLP structures has been eliminated. An added benefit is that the frontside mold compound provides a very planar surface capable of supporting high-density RDL wiring.

The board-level reliability of the chips face-up fan-out package has been tested using an 8mm X 8mm package with 324 I/Os on a 0.4mm pitch. The packages were mounted to 1mm thick printed circuit boards (PCBs) with non-solder mask defined PCB pads. Standard JEDEC conditions were used for temperature cycling and for drop [11,12]. Cycling results are shown in **Figure 15**. The part performed well, with a first cycling failure at 665 cycles and with no failures up to 250 drops.

Summary

A chips face-up approach to fan-out packaging has been described, in which Cu studs provide current pathways through mold compound covering the front die surfaces. Low cost at chip attach and high yields are enabled by an Adaptive Patterning technique, which compensates for die shifts inherent in fan-out technology. The frontside mold provides a planar surface capable of supporting high-density RDL wiring and creates a robust package structure that exhibits good performance in board-level reliability tests.

Acknowledgements

Adaptive Patterning™ is a registered trademark by Deca Technologies, Inc. Multiple structures and methods described within this paper are protected by US and foreign patents.

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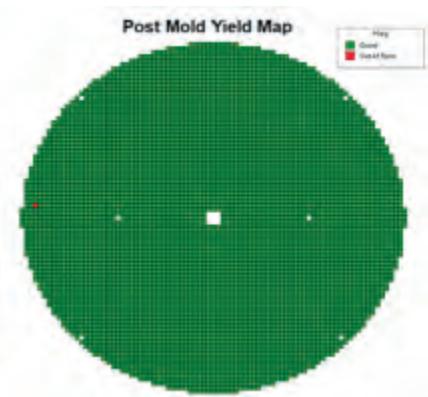


Figure 13: Yield map corresponding to shift data shown in **Figure 8** for a 3mm X 3mm package. Adaptive Alignment has been used to compensate for die shift, resulting in successful overlay to 99.98% of the die on the 300mm panel.

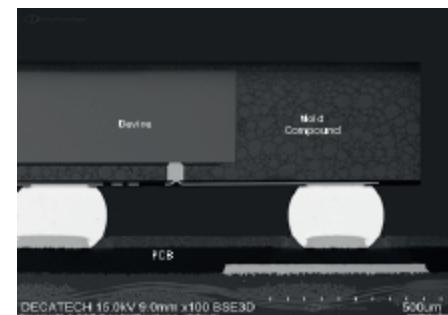


Figure 14: Chips face-up fan-out package, mounted to a printed circuit board.

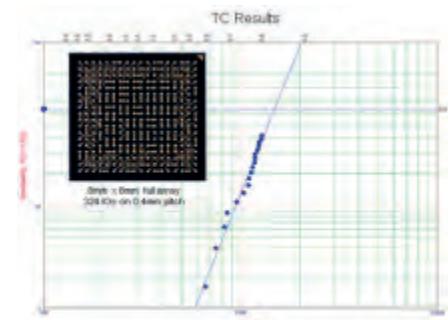


Figure 15: Thermal cycling tests on an 8mm x 8mm chips face-up test vehicle. The first failure occurred at 665 cycles.

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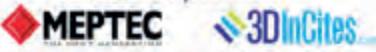


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What is driving advanced packaging platforms development?

By Thibault Buisson, Santosh Kumar [*Yole Développement*] and Ron Huemoeller [*Amkor Technology*]

The semiconductor industry is driven by the miniaturization of transistors and scaling CMOS technology to smaller and more advanced technology nodes, while at the same time reducing the cost. To overcome these limitations, new advanced packaging technologies have been developed, enabling more functionality to be integrated along with various types of devices in the same package. A significant level of activity is currently underway within the advanced packaging industry. Research, development, innovation, industrialization and mass market are the advanced packaging industry's key words. The spotlight is shifting towards advanced packaging. This article details the status of advanced packages and reviews some of the most innovative ones.

Which packaging platforms will take the lead?

While technology nodes continue to be developed and innovative solutions are being proposed, the investments required to bring such technologies to production are increasing significantly. The advanced packaging industry is doing well, with solid growth expected and a market value reaching US\$30 billion by 2020. Overall, the main advanced packaging market is the mobile sector, with end products such as smartphones and tablets. Other high-volume applications include servers, PCs, game stations, external HDD/USBs, and more [1].

At Yole Développement (Yole), we observed several different packaging approaches available on the market. These solutions clearly depend on the final product and application needs that are of great interest to the industry today. These advanced packaging technologies have increased in complexity over the years, transitioning from single to multi-die packaging, enabled by 3-dimensional integration. They include system-in-package (SiP), wafer-level packaging (WLP) (such as fan-in and fan-out, flip-

chip technologies), 2.5D/3D technologies, and embedded dies.

Which packaging platforms will take the lead or garner more interest from the industry? This is the big question that all advanced packaging companies would like to answer.

At Yole, we continue to see a very dynamic ecosystem, a lot of valuable companies and great interest in all of these innovative platforms. Because of the growth of the consumer market, as well as the need for higher performance products (i.e., 4K gaming, networking) both packaging platforms, fan-out and 2.5D/3D TSV, are being used for these applications. Below we provide an overview of the status of these two current package types.

Fan-out packages. Fan-out is in the spotlight since TSMC, the Taiwanese foundry leader, will be producing this type of package for the application processor of the Apple smartphone. Fan-out technology works by embedding a die into a molding compound and redistributing the I/Os to the outside of the die. Initially, this technology was adopted by STATS ChipPAC and NANIUM S.A. with their own proprietary solutions. With the entrance of players such as ASE, SPIL, Amkor Technology and Deca Technologies, and much more, the competitive landscape of this market is

intensifying—each player brings different techniques and integration schemes to the table. The advantages and challenges are different for each approach. These include warpage concerns, die shift, and issues with increasing yield and I/O counts, all of which are especially difficult for higher-end, complex applications.

TSMC's preparation for mass production, with its own technology called InFO, will increase the pressure; according to Yole, the market was initially estimated to reach only US\$174 million, prior to TSMC's adoption of the fan-out platform [2]. Today, the fan-out market is expected to have the highest growth of all, exceeding US\$2 billion by 2020, all platforms included (**Figure 1**). Fan-out technology will not only bring value to several players; the innovative approach could also significantly impact the substrate and flip-chip markets and become a disruptive technology within the entire advanced packaging market. The strategic choice made by TSMC confirms this revolution. It will be very exciting to follow up on the advanced packaging industry landscape to see how the market evolves and see which players will be part of the new ecosystem.

So, is it possible to predict what 2016 will be like? Of course, 2016 will



Figure 1: FOWLP activity market forecast with Apple entry. SOURCE: [2]

see much broader fan-out usage and therefore more investment in equipment to address that demand, including outsourced semiconductor assembly and test (OSAT) companies, integrated device manufacturers (IDMs) and foundries. The complete advanced packaging supply chain is now getting ready to ramp up production to larger volumes.

2.5D/3D with TSVs. Another emerging advanced packaging platform is 3D integration. This solution allows devices to be stacked vertically using through-silicon vias (TSVs) and interconnects for both mechanical and electrical connections. The two major architectures using 3D integration with TSV technology are 2.5D and 3D IC. 3D integration can enable higher memory bandwidth, lower power consumption, and reduced form factor and cost, compared with traditional packaging technologies.

TSV technology was first adopted in production for CMOS image sensors (CIS) and microelectromechanical systems (MEMS) markets and was used for several years. CIS devices continue to be the main application using 3D stacking and TSVs. New sensors such as the ambient light sensor (ALS) and fingerprint sensor have also adopted these technologies. Such technology is not limited to CMOS scaling in itself; rather, it adds functionality by stacking different types of devices, such as X-PUs, together with memory stacks. For the memory segment, the main market is for high-performance computers, networking, gaming and servers. This functional diversification is known as the More-than-Moore concept.

One of the latest products, such as AMD Radeon R9 Fury with its 2.5D configuration, high-bandwidth memory (HBM) stacks, and Samsung 3D TSV stacked dynamic random access memory (DRAM) released in 2015, highlight the added-value of 3D integration platforms. AMD's 3D and 2.5D components integrate HBM-based DRAM dies connected with via-middle TSVs and micro-bumps, as well as a GPU stacked onto a silicon interposer, that also incorporates via-middle TSVs. The graphics market is driven by the need for high performance. The HBM component delivers 60% more memory bandwidth and 3x the performance per watt and consumes 94% less PCB area than GDDR5 [3]. Furthermore, Samsung is an active player in this domain and is entering mass

production, driven by the need for higher bandwidth performance. Its new DRAM package, named 4GB HBM2, features 256Gbps of bandwidth, doubling the current HBM1 DRAM package. This year, Samsung is also planning to produce an 8GB HBM2 DRAM package; this second DRAM generation clearly paves the way for wider adoption of 3D TSV stacked memories in lower-end applications within the next three years. As volumes go up

and price goes down, Yole's analysts are expecting more announcements from Samsung of course, and also its main competitors [4].

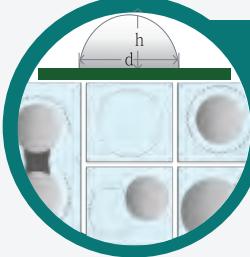
Market status of the 3D integration platform

MEMS and CIS markets are expected to exhibit continuous growth over the next several years, fueled by consumer applications such as smartphones, tablets, wearable products,

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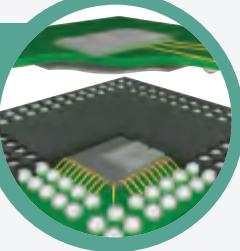


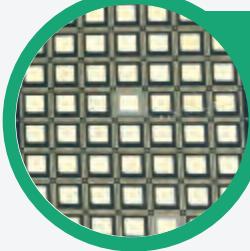
Inspection Items

Bump Types	BGA
- Paste Print	Bump Metrology
- μ Ball	Height: 1um
- Cu Pillar	Diameter: 2um
	Bump Offset: 2um
	(Single Sigma)

Applicable Packaging

SiP	3D	WL CSP	MCM
2.5D	3D WLP	FO WLP	FC BGA





Handling Media

- Laminate Substrate
- Metal Carrier
- Strip on Boat
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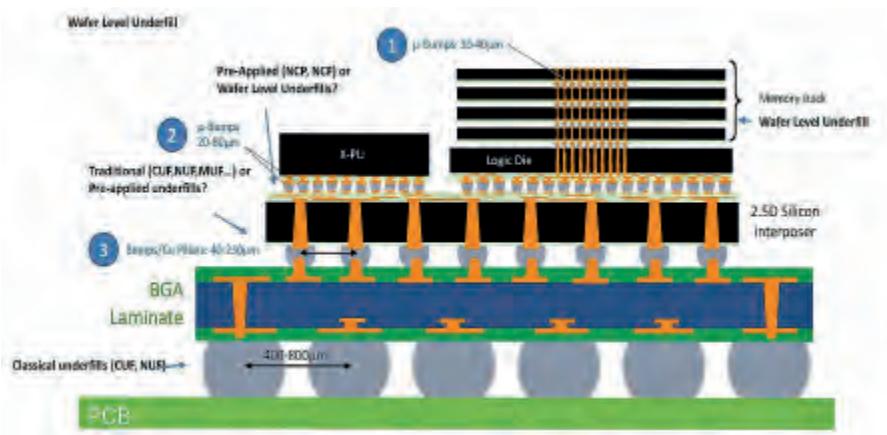


Figure 2: Underfill materials opportunities: flip-chip and 3D packaging solutions. SOURCE: [6]

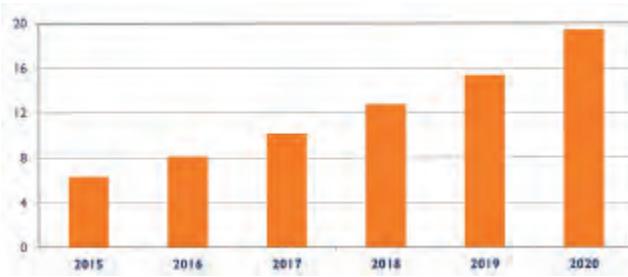


Figure 3: TB/DB material is mainly used for the 2.5D/3D TSV packaging platforms; from 2015 to 2020 – in M\$. SOURCE: [7]

and more. Indeed, the mobile phone industry has grown, producing more than 1.1 billion devices in 2014 [5]. On the high-end market, driven by the need for further performance increases, volatile memory and especially DRAM are clearly opening the doors to the commercial adoption of 2.5D/3D ICs. Original equipment manufacturers (OEMs) are also planning to release products using memory stacks around 2016-2017. These companies are targeting networking applications, routers and switches.

A large range of packaging platforms is available today. All are expected to continue their growth. Fan-out and 3D IC could stand out with the strongest growth rates: 3D integration is now available on the market across a wide range of devices, especially in the consumer market segment. As for fan-out, it has seen the largest growth and a potential move to panel manufacturing in the future.

On the advanced materials side, a lot of incredible innovations have been developed by advanced packaging players. For example, fan-out and 2.5D/3D platforms require creative materials that will provide the most robust manufacturing processes, as well as the lowest cost and most reliable final packaging products (**Figure 2**). Key materials include the items described below:

Dielectrics for redistribution layers (RDLs). Such materials are mostly polyimide/polybenzoxazole (PI/PBO) based. The key technical requirements in fan-out and 2.5D/3D packaging platforms are a low dielectric constant and low dielectric loss, high thermal stability, low-temperature cure

processing, fine geometry patterning, process flexibility (coating, patterning, development), low moisture uptake, robust mechanical properties and chemical stability, tunable viscoelastic properties for planarization and gap filling, and high reliability.

Temporary bonding and debonding (TB/DB) materials for further thinning and handling of thin wafers. TB/DB is one such key to technology for handling and double-sided processing of extremely thin TSV wafers for 2.5D/3D platforms [7]. The requirements of temporary bonding materials are numerous. First, they must be compatible with a vacuum process. They must also be stable up to 200°C in order to resist the plasma-enhanced chemical vapor deposition (PECVD) process at 200°C and bump reflow at 260°C. The bonding temperature must be lower than the reflow temperature.

TB/DB materials must also be chemically compatible, meaning they must be resistant to chemicals used during the processing steps, such as chemical mechanical polishing (CMP), and be easy to clean and debond without chemical and thermal stresses. Additionally, such advanced materials must have superior mechanical properties to withstand the wafer thinning process and provide strength to hold the

temporary carrier-to-device wafer during high-temperature process steps.

TB/DB materials can be developed using different chemical processes: Brewer Science, JSR Micro, and Dupont focus their materials development on a thermoplastic approach. Thin Materials/Nissan Chemical Industries and Dow propose TB/DB materials using thermosetting technology, while materials from 3M and TOK are part of the photoset type. Shin Etsu, meanwhile, has developed a specific combination of thermoplastic and thermoset composites.

Currently, TB/DB material is mainly used for 2.5D/3D TSV packaging platforms. Related markets are not as significant. At Yole, we estimate these markets to have reached about US\$6.3 million in 2015. A 25% CAGR is expected between 2015 and 2020, allowing the market to reach about US\$19 million in 2020 (**Figure 3**) [7].

Fan-out platforms could be another potential application, especially when the thickness of reconstituted wafers falls below 400µm. Certain OSATs are currently studying the feasibility of such technology.

Wafer-level underfills (NCP/NCF). NCP/NCF for smaller pitches are one of the key materials used in 2.5D/3D packaging platforms. Capillary underfill (CUF) is probably the most mature and widely used underfill technology. Underfill technology is mainly suited to large interconnection pitches and die-to-die gaps (up to 50µm). In advanced packaging applications (e.g., 2.5D and 3D), the technical challenges are numerous. At Yole, we have identified some of these as high interconnect density, adequate bonding pitch, small die-to-die/substrate gap size, and CUF application. Some of the issues include the cleaning of flux residue, voiding due to difficulty in filling the narrow gap, and longer underfilling times. To overcome these challenges, in CUF applications for example, alternative underfill methods, such as NCP and NCF, have been developed. NCP is better for Cu pillar-thermocompression bonding (TCB) applications, whereas NCF is mainly used for TSV memory dies. The market for NCF is currently small but expected to reach about US\$13 million by 2020.

Molding compound is one of the most critical materials in the fan-out platform. It can have a significant impact on performance, cost and reliability in the fan-out advanced package. Such materials are produced by industrial players in various forms, including liquid, granular and film/sheet. Almost all of the fan-out market currently uses a liquid mold compound. Key suppliers are Nagase

Ultra-Low Residue No-Clean Flip-Chip Fluxes

ChemX, Hitachi Chemical, and Panasonic. Materials suppliers are also promoting other options, such as granular and film forms, with different characteristics in terms of cost, thickness control and compatibility with panel formats.

Emerging packages and materials aim to bridge the gap by reviving the cost and performance curve while adding more and more functionality. 3D technology and fan-out WLP combined with innovative materials are undeniably part of these new package types as previously described.

The added value of SiP

In parallel with the efforts noted above, another type of architecture has also shown added-value in the advanced packaging industry: the system-in-package (SiP). Particularly driven by the Internet of Things (IoT), SiP is a high-interest packaging approach, as it enables the integration of heterogeneous technology (separating ICs with functional blocks) and reduces cost and form. According to Yole's analysis, the market drivers are numerous and comprise the mobile market, including smartphones and tablet applications, radio-frequency (RF) applications and connectivity modules.

Within the context of the above, industrial players are more and more looking for disruptive platforms and therefore pushing the limits of innovation. The SiP advanced packaging platform could be an answer as well. Indeed, substantial effort has been made at the substrate level, especially with coreless SiP penetration. Latest high/mid-band filters, TQF6405 from Qorvo and AFEM8030 from Avago Technologies, both embedded in iPhone 6s™, point up the added-value of SiP technologies [8,9].

Keys to advanced packaging: miniaturization and modularization

The trends for miniaturization and modularization continue to cause disruption at the system level. The drive for modularization pushes both the foundry (at one end) and electronic manufacturing service (EMS) providers (at the other) to offer services beyond their core capabilities. With advanced silicon nodes continuing to increase in cost, packaging has emerged as a key competitive differentiator—necessitating consideration earlier in the design process.

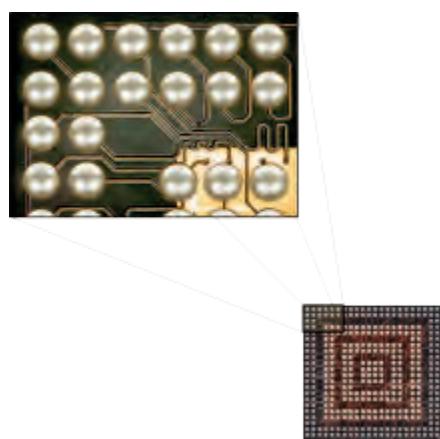
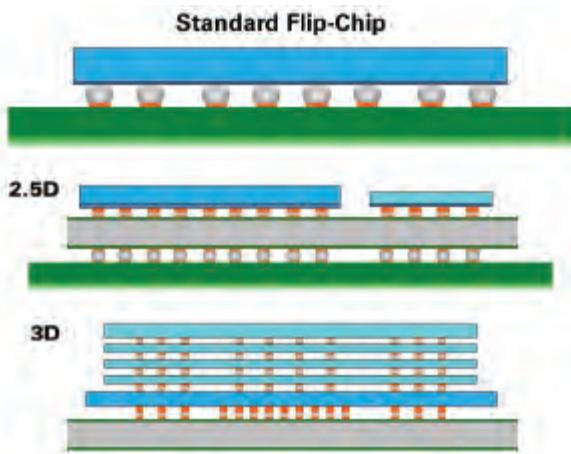


Figure 4: Amkor Technology WLF0.



Figure 5: Amkor Technology Avatar TSV progress.

Advanced packages such as fan-out (**Figure 4**) and those implementing through-silicon vias (TSVs) (**Figure 5**) have become key packaging platforms that effectively address the more recent trends noted above. These two types of advanced packaging technologies provide the modularization and integration required to enable higher levels of system-level performance, delivering higher bandwidth and affording more efficient power management. The use of these latest platform technologies can be found in new



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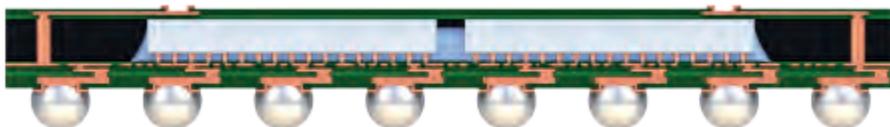


Figure 6: Amkor Technology SWIFT™ top RDL.



Figure 7: Amkor Technology SLIM™ cross section.

product releases spanning the mobile arena to high-end networking, as well as processing. To enable all these newer technologies, closer collaboration between the packaging houses and their customers, as well as additional end-to-end support is essential, including electrical design, characterization and testing. Only the most advanced assembly houses have adequate funding and are able to make these investments. That said, for the leading OSATS, the investment has been made and is now paying dividends with the release and designed-in use of both of these packaging technologies. As a result, advanced packaging is clearly one of the key enablers for the next-generation of sophisticated electronic devices, simultaneously enabling miniaturization and performance optimization.

An example is in SiP technology, which requires the ability to handle multiple process technologies and die for the different functional blocks (analog, mixed-signal, digital), thereby increasing the requirement for state-of-the-art packaging solutions. Fan-out wafer-level package technologies, even at the rudimentary level, enable the most complex SiP solutions, such as mobile RF front-end or MEMS technologies. In addition, by utilizing a yield-conscious “die-last” technology approach (**Figure 6**), package technologies now found in advanced wafer-level fan-out packages such as silicon wafer integrated fan-out technology (SWIFT™), allow for the integration of even higher value die by reducing the risk of die loss due to packaging yield issues typically found in the traditional fan-out approaches. The more sophisticated dies-last approach enables the use of very fine-line lithography down to 2µm line/space and multi-die integration by virtue of a process flow that isolates the high-value die from the difficulty in routing multiple layers at these very fine trace pitches. Ultimately, the dies-last approach removes the crippling effects of losing die due to the intimate tie to fine-line lithography yield loss in the dies-first approach, providing a package technology that is unmatched in value. An example of a package utilizing the dies-last configuration is shown in **Figure 7**, where the integration of memory and high-powered processing is illustrated.

TSV technology is now gaining traction in the semiconductor industry, providing the

preferred platform for advanced networking devices as well as the most advanced graphic devices. One strategy for TSV today is the partitioning and use of die at the best technology node where the best price and performance exist. This approach helps to keep foundry costs down by making use of system optimization for memory, analog, performance and power management. In this manner, die costs are correctly relegated to the appropriate node, allowing maximum yield and reducing the overall die size. Another strategy is to place HBM onto a silicon interposer very near the processor to reduce the typical parasitics and inductance issues encountered with on-board memory. This technique specifically addresses the growing need for increased memory integration and provides clear downstream benefits in both power and performance, by serving as a replacement for eDRAM/eFlash. This is the primary attraction to 2.5D TSV today, where a side-by-side format is used to allow reduction in both die size and motherboard size (including layer count).

Acknowledgments

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Design, material, process, and equipment of embedded fan-out wafer/panel-level packaging

By John H. Lau, Nelson Fan, Li Ming [ASM Pacific Technology Ltd.]

The design, materials, process, and equipment of embedded fan-out wafer/panel-level packaging (FOW/PLP, or simply FOWLP) are the focus for this article. Emphasis is placed on various FOWLP formation methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). As redistribution layers (RDLs) play an integral part of FOWLP technology, various RDL fabrication methods such as Cu damascene, polymer, and printed circuit board (PCB) will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, molding materials, and equipment for pick-and-place, RDLs, molding, solder ball mounting, and inspection, test, and marking will be provided. Embedded chips will be briefly mentioned first.

Embedded chips

Basically, there are two groups of embedded chips in semiconductor packaging. One is embedded chip in laminate substrate and the other, embedded chip in epoxy mold compound (EMC).

Embedded chip in laminate substrate. TI's MicroSiP [1] manufactured by AT&T is a classic example of embedded chip in rigid laminate substrate. It is a DC/DC convertor with an IC chip (PicoStar™) face-down embedded in the laminate substrate with solder balls to be attached onto PCB. Smaller form factor, lower profile, lesser weight, and better electrical performance have been achieved.

Fujikura's wafer-and board-level embedded package (WABE) technology demonstrated that by embedding an application-specific IC (ASIC) in a flexible laminate substrate, the package size can be reduced by 50% [2]. They also showed that a multilayer flexible substrate can embed two chips in a stacked configuration [3].

The advantages of embedding chips in rigid and flexible laminate substrates are [4] a) low profile, b) low cost with a large panel, c) better electrical performance with

low inductances, and d) easy to extend to 3D chip stacking. The disadvantages are a) cannot rework, b) infrastructure, and c) supply chain. Using an embedded chip in rigid and flexible laminates has a great potential in portable, mobile, and wearable applications, but are out of the scope of this study.

Embedded chip in EMC. Since the embedded fan-out patent [5], which was filed in 2001, and the technical paper [6] that was published in 2006 by Infineon [7], the embedded chip in EMC, also called fan-out wafer-level packaging (FOWLP), has been used in various products such as baseband, RF (radio frequency) transceiver, and PMICs (power management ICs) by companies such as Infineon, Intel, Marvell, Spreadtrum, Samsung, LG, Huawei, Motorola, and Nokia, among others. Many outsourced semiconductor assembly and test services (OSATS) and foundries are developing their own embedded FOWLP for the forecasted explosive growth of this market in the next few years. FOWLP will be the focus of this study.

Formation of FOWLP

Basically, there are two methods to form (build) the FOWLP. One is chip-first and the other is chip-last. For the chip-first method, there are two options: face-down (die-down) and face-up (die-up). On the other hand, there is only one option for the chip-last method (also called RDL-first): is face down.

Chip-first with face-down (die-down). This is the most conventional method to form FOWLPs, and most FOWLP products

being manufactured today are using this method [6, 8, 9]. **Figure 1** shows the process flow of chip-first with die-down FOWLP. First, the device wafer is tested for known-good dies (KGDs) and then singulated into individual dies. This is followed by picking up the KGDs and placing them face-down on a temporary carrier that can be round (wafer) or rectangular (panel) with a double-sided thermal release tape. Then, the reconfigured carrier is overmolded using the compression molding method with EMC before removing the carrier and the double-sided tape and

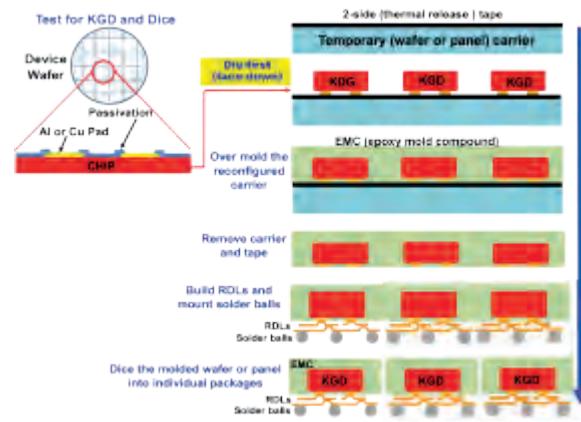


Figure 1: Process flow of chip-first (die-down).

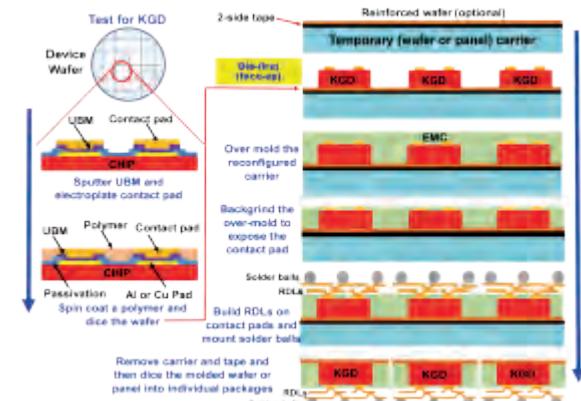


Figure 2: Process flow of chip-first (die-up).

turning the whole molding (with KGDs) around. Next comes building the RDLs for signals, power, and grounds from the Al or Cu pads. Finally, solder balls are mounted and the whole molding (with KGDs, RDLs, and solder balls) is diced into individual packages (**Figure 1**).

Chip-first with face-up (die-up). **Figure 2** shows the process flow of chip-first with die-up FOWLP. TSMC's famous integrated fan-out wafer-level packaging (InFO-WLP) [7, 10] is an example. It can be seen that after the test of KGDs from the device wafer, a Ti/Cu under bump metallurgy (UBM) is sputtered using physical vapor deposition (PVD) on the Al or Cu pad, and a Cu contact pad (or stud) is electroplated on the UBM (this is for building the RDLs later). It is followed by spin coating a polymer, e.g., PI (polyimide), BCB (benzocyclobutene), or PBO (polybenzobisoxazole), on the whole wafer. The wafer is then diced into individual dies. The KGDs are then picked and placed face-up (die-up) on a double-sided thermal release tape, which is on a temporary carrier. (An optional wafer can be attached on top of the double-sided tape and its top-side is laminated with a die-attach adhesive for the back-side of the KGDs. This wafer can be used as a reinforcement to increase the bending stiffness so as to resist the warpage of the reconfigured molding when the carrier and double-sided tape are removed.) These steps are followed by compression molding with EMC on the reconfigured (wafer or panel) carrier, and then backgrinding the over-mold to expose the contact pad of the KGDs. The next step is to build up the RDLs from the contact pads and then mount the solder balls. Next comes the removal of the carrier and tape, and then the dicing of the whole molding into individual packages. For high-performance applications, the material of the optional reinforced wafer can be made of a metal to enable it to be used as a heat spreader.

Chip-last with face-down (RDL-first). Since 2006, NEC Electronics Corporation (now Renesas Electronics Corporation) has been developing a novel SMAFTI (SMArt chip connection with feedthrough interposer) packaging technology for inter-chip wide-band data transfer [11-12], 3D stacked memory integrated on logic devices [13-17], system in wafer-level package (SiWLP) [18], and "RDL-first" fan-out wafer-level packaging [19]. The feedthrough interposer (FTI) used in SMAFTI is a film with ultra-fine linewidth and spacing RDLs. The dielectric of the FTI is usually SiO₂ or a polymer, and the conductor wiring of the RDLs is Cu. The FTI not only supports the RDLs underneath within the chip,

it also provides support beyond the edges of the chip. Area array solder balls are mounted at the bottom-side of the FTI, which are to be connected to the PCB. EMC is used to embed the chip and support the RDLs and solder balls. In 2015, Amkor announced a very similar technology called SWIFT™ (silicon wafer integrated fan-out technology) [20].

Figure 3 shows the process flow of the chip-last with face-down (die-down) or "RDL-first" FOWLP. This is very different from the

chip-first FOWLP. First of all, this only works on a wafer carrier. Also, RDL-first FOWLP requires: 1) building up the RDLs on a bare silicon wafer (the FTI), 2) performing the wafer bumping, 3) performing the fluxing, chip-to-wafer bonding, and cleaning, and 4) performing the underfill dispensing and curing. How to build up RDLs on a silicon wafer will be discussed later. As to wafer bumping, chip-to-wafer bonding and underfilling, please see our previous study [21]. Each of these tasks is



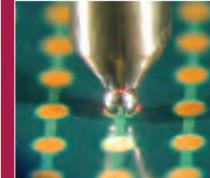
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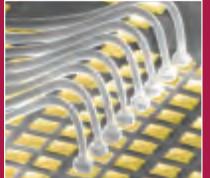
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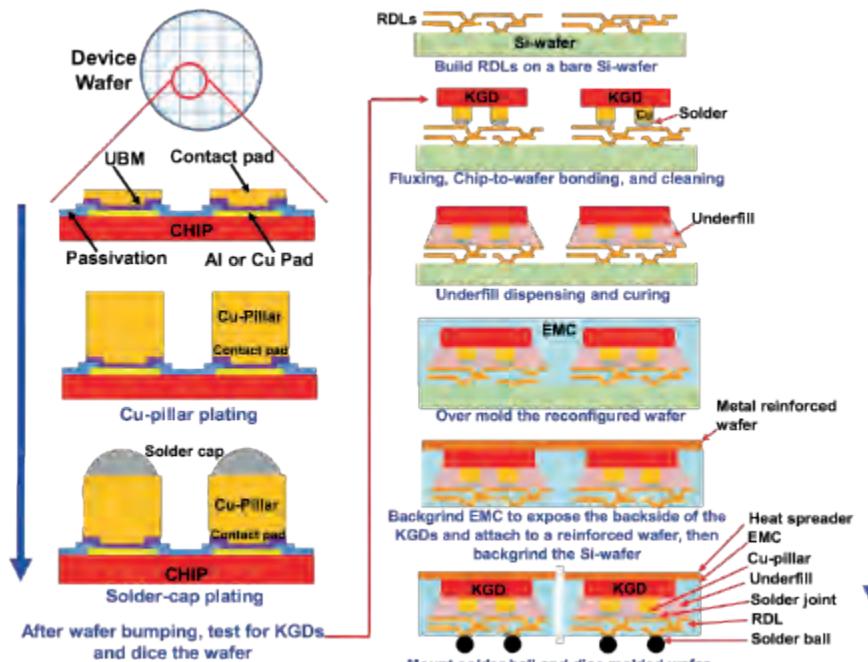


Figure 3: Process flow of chip-last (RDL-first).

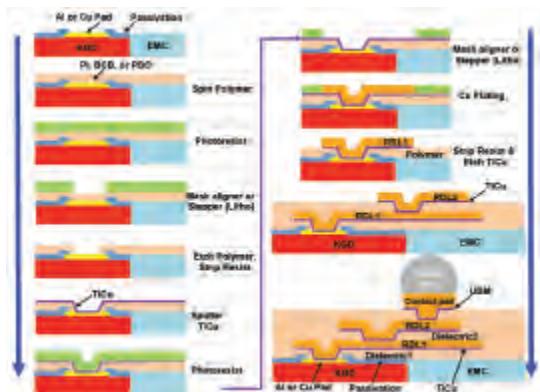


Figure 4: Process flow of RDLs with a polymer as the dielectric layer.

a major undertaking and requires additional materials, process, equipment, manufacturing floor space, and personal effort. Therefore, compared to chip-first FOWLP, chip-last (RDL-first) FOWLP incurs very high cost and has a higher probability of greater yield losses. It can only be afforded by very-high density and performance applications such as high-end servers and computers.

According to [18-19], the challenges of chip-first FOWLP (the key reasons for them to introduce the chip-last FOWLP) are as follows: 1) The production yield during the RDL process is low because the KGDs are already embedded (this is true only if the chip-last (RDL-first) FTI is fully functionally tested before the chip-to-wafer bonding, otherwise the KGDs still have to be thrown away for the case of a FTI with bad RDLs

after a system test); 2) The I/O pitch of a chip must be large enough to allow alignment error between the chip and RDL layer, on account of thermal expansion and warpage of the molding, and also the error in chip displacement during the process. (This does not apply to chip-first FOWLP for portable, mobile, and wearable applications, because their smallest pitch of chips, using the latest Apple AP (application processor A9) as an example, is 150 μ m staggered.); and 3) The RDL requires a low-cure temperature dielectric that may negatively affect the package reliability. (This situation does not apply to chip-first FOWLP for portable, mobile, and wearable applications as reliability is not a critical issue of these products owing to their short life cycle.)

After wafer bumping of the device wafer, the next step is to test for KGDs and then dice the wafer into individual dies. Next, the KGDs are picked up, flux is applied, and then the KGDs are placed face down on the contact pad (which is on top of the RDLs) of the full-thickness silicon wafer prior to performing chip-to-wafer bonding. That step is followed by cleaning the flux residue and then dispensing the underfill and curing. Next comes over molding the whole reconfigured wafer carrier using the compression method with EMC. Then, backgrinding is done to remove the silicon carrier. (Another way is to

backgrind the over mold to expose the backside of the KGDs, which are attached to a metal reinforced wafer, and then backgrinding is done to remove the silicon carrier as shown in Figure 3.) Finally, the solder balls are mounted on the bottom RDL (which will be discussed in detail later) and the molded wafer is diced into individual packages.

In 2012, GIT [22] published a paper on chip-last fan-out (CLFO) packaging with embedded PMIC in ultra-thin laminate substrates. In 2015, ASE [23] proposed a low-cost fan-out chip-last package (FOCLP) using a coreless panel substrate for low-end and low pin count applications. Strictly speaking, because they used the substrates and area-array solder balls to fan-out the circuitry from the chip to the PCB [7], this cannot be considered an FOWLP structure.

RDL processes

Basically, there are at least three different methods used in fabricating the RDLs, namely the polymer, Cu damascene, and PCB. The method used will depend on the linewidth/spacing of the conductor wiring of the RDLs. For example, for high-performance applications, the linewidth/spacing and thickness are <5 μ m and 2 μ m, respectively, at this juncture (but very soon they will go down to \leq 2 μ m and 1 μ m); the lithography process is accomplished using a stepper and they are fabricated by the Cu damascene method. If the dielectric layer (most likely it is SiO₂) is about 1 μ m thick, then it should be fabricated by the plasma-enhanced chemical vapor deposition (PECVD) method. For mid-performance applications, the Cu linewidth/spacing and thickness are 5-10 μ m and 3 μ m, respectively, and the lithography is accomplished using a mask aligner, they should be fabricated by the electrochemical deposition (ECD) method. (However, because of the die drift and warpage of the molding, and in order to lower the yield loss caused by the mask aligner, sometimes a stepper is used.) The dielectric layer comprises polymers (e.g., PI, BCB, and PBO) that are about 4-8 μ m thick and fabricated by spin coating and curing. For low-performance applications, the Cu linewidth/spacing and thickness of the RDLs are >10-20 μ m and 5 μ m, respectively, they are fabricated by the resin-coated copper (RCC) with PCB technology and laser direct imaging (LDI) [24].

RDL by polymer method

Figure 4 shows the process flow of fabricating the RDLs with polymer such as

the PI, BCB, and PBO method. First, spin coat a polymer on the whole wafer. That step is followed by spin coating a photoresist. Then the photoresist is opened with a mask aligner or stepper. The polymer is then etched and the resist is stripped off. Next, the adhesive/seed layer (Ti/Cu) is sputtered using PVD; the photoresist is then spin coated, and then the photoresist is opened with a mask aligner or stepper. Next comes electroplating the Cu. After the resist is stripped off and the TiCu is etched off, we have the first RDL1. If one repeats the processes, you get the second RDL2, the third RDL3, and so forth [25-26]. Finally, on top of the RDL, one needs to fabricate a UBM and a Cu contact pad for mounting the solder balls. This method is very suitable for chip-first with die-down or die-up FOWLP. For the latter case, the UBM and contact pad on the device wafer have to be fabricated first. This method can also be used for RDL-first FOWLP if the linewidth/spacing is not very fine (e.g., $\geq 5\mu\text{m}$).

RDL by Cu damascene method

Figure 5 shows the process flow of fabricating very fine linewidth/spacing ($<5\mu\text{m}$) RDLs for chip-last with die-down (RDL-first) FOWLP. First, use PECVD to form a thin layer of SiO_2 on a full-thickness bare silicon wafer and then use a spin coater to laminate the photoresist. These steps are followed by using a stepper to open up the resist and a reactive ion etch (RIE) to remove the SiO_2 . Then, a stepper is used to open the resist wider and RIE to etch more of the SiO_2 . Next, strip off the resist, sputter the TiCu, and electroplate the Cu on the whole wafer. These steps are followed by chemical mechanical polishing (CMP) to remove the overburden Cu and the TiCu, and then we have the first RDL1 and V01 (the via connecting the Si and RDL1) as shown in **Figure 5**. This is called the dual Cu damascene method [25,26]. Repeat all the processes to get the second RDL2, the third RDL3, and so forth. V12 is the via connecting RDL1 and RDL2. **Figure 6** shows an example of fabricated RDLs by the dual Cu damascene method [25,26]. It can be seen that there are three RDLs and on top of RDL3, there are a UBM and a Cu contact pad; the contact pad is to be connected to the microbump for chip-to-wafer bonding. If the linewidth and spacing of the RDL's conductor wiring is not very fine (e.g., $\geq 5\mu\text{m}$), then instead of the Cu damascene method, a polymer method could work for fabricating the RDLs for chip-last (RDL-first) FOWLP. On the other hand, for chip-first FOWLP, if the linewidth/spacing is $<5\mu\text{m}$, then the

Cu damascene method is recommended.

After fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing, and molding, it is time to remove the silicon wafer and attach the solder balls. The remaining parts of **Figure 5** show the process flow. The steps are as follows: 1) Backgrind the silicon wafer to a few microns from the via (V01), 2) then use CMP on the silicon wafer, and then 3) TiCu and passivation to expose the Cu of V01. These steps are followed by 4) PECVD to form a SiO_2 layer and then 5) spin coating a photoresist. Then, 6) use a stepper to open the resist and a RIE to remove the SiO_2 ; 7) use another stepper to open the resist wider and a 8) RIE to etch the SiO_2 further, and then 9) strip off the resist. It is followed by sputtering the Ti/Cu and electroplating the Cu. Then, 10) CMP on the overburden Cu and the TiCu and obtain the UBM

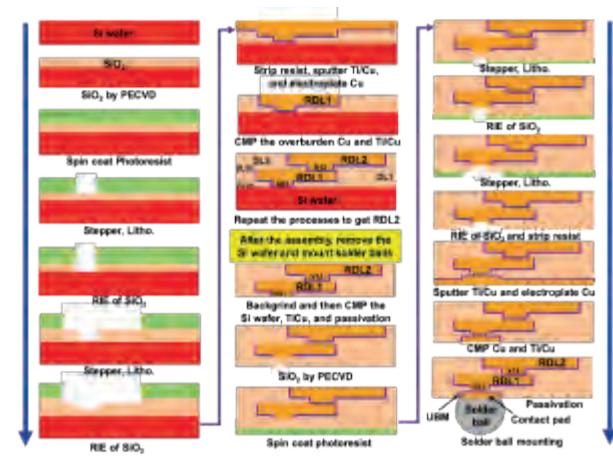


Figure 5: Process flow of RDLs fabricated using the Cu damascene method.

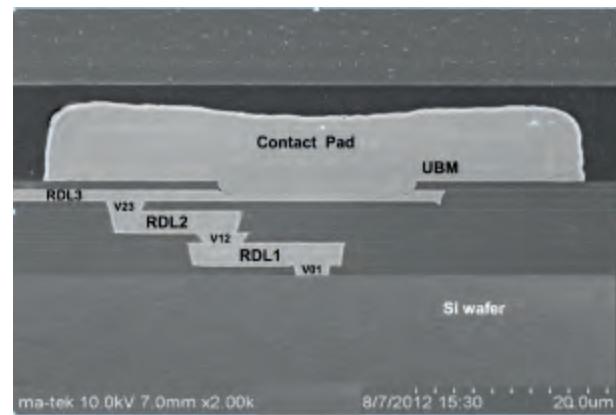


Figure 6: Typical SEM image of RDLs fabricated using the Cu damascene method.

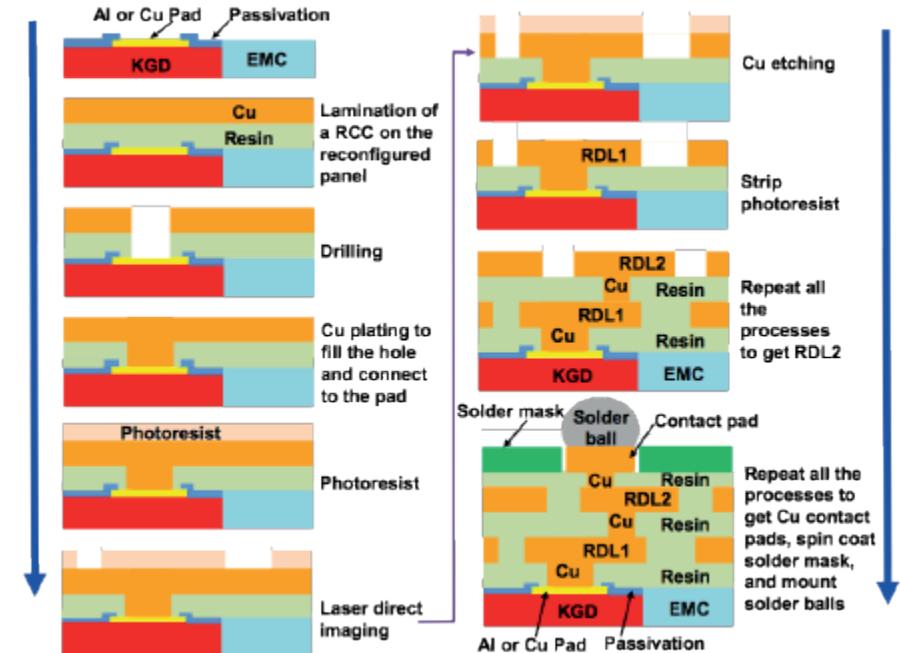


Figure 7: Process flow of RDLs fabricated using the PCB/LDI method.

and Cu contact pad. Finally, 11) mount the solder balls on the Cu contact pads as shown in **Figure 5**. In this case, the dielectric layer, UBM, and contact pad can be fabricated by the polymer method, regardless of the linewidth/spacing of the conductor wirings of the RDLs.

RDL by PCB/LDI method

Figure 7 shows the process flow of fabricating the large conductor linewidth/spacing ($>10\mu\text{m}$) RDLs for chip-first with die-down FOPLP (fan-out panel-level packaging). First, laminate an RCC on the reconfigured panel. Then, use a mechanical or laser drill to make holes into the RCC. It is followed by PCB Cu plating to fill the holes and connect to the Al or Cu pads. Laminate a dry-film photoresist and use an LDI to remove the resist. Perform the Cu etching and strip off the resist. We then have the first RDL1 and can repeat all the processes to get the other RDLs. The final RDL can be used as a contact pad. Next, we laminate, photolithograph, and cure the solder mask (in either a solder mask defined or a non-solder mask defined formats) before mounting the solder balls. For this process,

no material and equipment are needed from the semiconductor arena except a PCB shop. If the RDLs are earmarked for chip-first with die-up FOPLP devices, then the UBM and contact pad on the device wafer have to be fabricated first.

Round or rectangular reconfigured carriers

As shown in the studies [7,24] with a standard size PCB large panel (610mm x 457mm) for reconfigured carriers, surface mount technology (SMT) equipment for picking and placing the KGDs and passive components, and PCB technology equipment, as well as LDI for making the RDLs, it is able to fabricate FOPLP at a very low cost for low-end, low-pin count, small chip sizes, and high-volume applications. The choice of wafer or panel reconfigured carriers depends on the linewidth/spacing of the conductor wiring of RDLs. Usually, if it is $>10\mu\text{m}$, then the panel carrier method could work, otherwise the wafer carrier method is recommended.

Notes on dielectric materials

For RDLs used in chip-first FOWLP structures with very fine linewidth/spacing, the dielectric layer (SiO_2) is fabricated by either low-temperature PECVD ($<200^\circ\text{C}$) or sub-atmosphere chemical vapor deposition (SACVD) (170°C); either of these processes are accomplished at temperatures less than the critical temperature (230°C) of the compression molded EMC. However, for the polymer dielectric layer, low curing temperature polymers such as BCB and PBO are required. For example, the curing temperature of Dow's BCB is 200°C , and for Sumitomo's PBO, 220°C .

For low warpage and high-reliability chip-first and chip-last FOWLP, the Young's modulus and elongation of the dielectric materials must be, respectively, low and high. For example, the Young's modulus and elongation of Dow's BCB are 2GPa and 28, while Sumitomo's PBO, are 2.7GPa and 55.

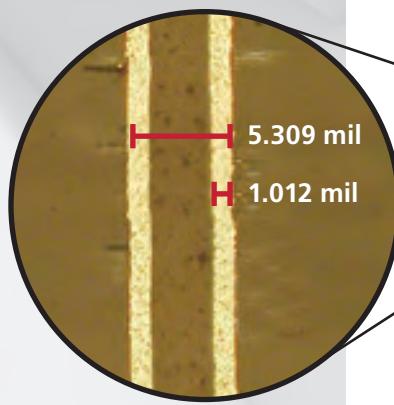
Notes on molding materials

The molding of FOWLP is by the compression method with EMC. For chip-first FOWLP, the curing temperature of

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the EMC must be lower than the release temperature of the double-sided tape. For chip-last FOWLP, the curing temperature of the EMC must be lower than the critical temperature of the dielectric material.

For chip-first and chip-last FOWLP, there are at least two forms of EMC, namely liquid and solid. The advantages of liquid EMC are better handling, good flowability, less voids, better fill, and less flow marks. The advantages of solid EMC are less cure shrinkage, better stand-off, and less die drift.

For chip-first and chip-last FOWLP, high filler content (>85%) [6] EMC will shorten the time in mold, lower the mold shrinkage, and reduce the mold warpage. Uniform filler distribution and filler size of the EMC will reduce flow marks/fill and enhance flowability. For example, the filler content (wt%), maximum filler size, mold condition, post cure, T_g, and bending stiffness of EMC by Sumitomo (solid) are 90, 55μm, 7m/125°C, 1h/150°C, 170°C, and 30GPa, respectively, and by Nagase (liquid), 89, 75μm, 10m/125°C, 1h/150°C, 165°C, and 22GPa, respectively.

Notes on equipment

The key sets of equipment in making FOWLP are pick-and-place, RDLs, molding, solder ball mounting, and packaging handling, as discussed below.

Pick-and-place (P&P). There are at least two groups of P&P machines. One is SMT P&P for large-pitch KGDs and therefore, large linewidth/spacing RDLs supplied by, e.g., Universal, Panasonic, and ASM, and the other is high precision P&P for fine-pitch KGDs and therefore, fine linewidth/spacing RDLs supplied by e.g., Toray, Datacon, and ASM.

ASM's SIPLACE CA [27] is an SMT machine intended for high-speed large FOPLP, which delivers maximum performance and capability. When equipped with the SIPLACE Speedstar CP20 head, the SIPLACE CA is able to place up to 42,000 flip-chips or 28,000 die-attach components per hour in sizes ranging from 03015 (0.3mm x 0.15mm) up to 6mm x 6mm with an accuracy of ±10μm/3σ, and a package up to 27mm x 27mm with an accuracy of ±25μm/3σ.

ASM's NUCLEUS [27] is a high-precision P&P machine, which is designed to address die-up or die-down with local and/or global alignment modes. Apart from high-throughput, this P&P machine also provides high bonding accuracy with an XY placement accuracy of <2.5μm/3σ. The

system comes with an optional feature that provides an additional processing capability for high bond force and bond temperature catering to a specific process requirement of very high-end device application.

RDL fabrication. There are at least three key tasks in fabricating RDLs, namely, the seed/adhesion layer by PVD, the dielectric layer by PECVD, and the conductor wiring by ECD. The PVD machines are provided by companies such as Applied Materials, SPTS (which is now part of Orbotech) and NEXX, and the PECVD machines are provided by companies such as Applied Materials, Lam Research, and Tokyo Electron. The ECD machines, provided by companies such as Semitool (which is now part of Applied Materials), Novellus (which is now part of Lam Research), and NEXX can do the job.

Molding. Compression with EMC is the key method to mold the reconfigured carriers; the machines' suppliers are Yamada, TOWA, and ASM, among others. ASM's ORCAS [27] is an encapsulation system with configurable molding direction and pressing capabilities that performs well on wafer and panel carriers. It can also encapsulate different sizes of carrier as well as handles both liquid and solid EMCs. The tool delivers a high co-planarity accuracy of ±20μm with its robotic handler providing the required stability. It can be configured for multiple press usage.

Solder ball mounting There are at least two methods to perform the ball mounting, namely, stencil print on the solder paste and reflow, and stencil or screen print on the flux, drop (mount) the solder spheres, and reflow. Examples of equipment suppliers are Shibuya, Pac Tech, and ASM. ASM's DEK Galaxy [27] is high-throughput with a minimum alignment capability of 2Cpk @±12.5μm system and with an in-line capability for the highest automation. It allows placement of solder balls as small as 200μm and up to 1.2mm on the same machine, meeting the industry's speed and accuracy requirements (i.e., delivering greater than 99.99% placement yield at a high throughput). It also provides an intelligent detection system for assurance of process.

Packaging handling The equipment suppliers on inspection, test, and laser marking are DISCO, Rudolph Technologies, and ASM, among others. ASM's SUNBIRD [27] provides a solution on sorting and flexibility for an individual unit testing and laser marking. The system is equipped with iTechnology features to provide the user an intelligent machine for fan-out

wafer/panel-level packaging handling at high speed.

Summary

The design, materials, process, and equipment used for FOWLP have been investigated in this study. Some important results and recommendations are as follows:

- Out of the three methods used to form FOWLP structures, chip-first with die-down is the most simple and low cost, while chip-last (RDL-first) is the most complex and high cost. Chip-first with die-up requires slightly more process steps (and therefore slightly more costly) than chip-first with die-down.
- Chip-first FOWLP can perform more than what fan-in wafer-level packaging (WLP) can do. However, some of the things that plastic ball grid array (PBGA) package can do, but chip-first FOWLP cannot are: 1) larger die size ($\geq 12\text{mm} \times 12\text{mm}$), and 2) larger package size ($\geq 25\text{mm} \times 25\text{mm}$). This is due to the thermal expansion mismatch and warpage limitations of the chip-first FOWLP. In this case, chip-last (RDL-first) FOWLP can extend the application boundary to a die size with the range of $\leq 15\text{mm} \times 15\text{mm}$ and a fan-out package size of $\leq 32\text{mm} \times 32\text{mm}$. With the heat spreader wafer option, the boundary can even be stretched to a die size of $<20\text{mm} \times 20\text{mm}$ and a fan-out package size of $<42\text{mm} \times 42\text{mm}$.
- Chip-first FOWLP is a good choice for packaging semiconductor ICs such as baseband, RF/analog, PMIC, AP, low-end ASIC, CPUs (central processing units) and GPUs (graphics processing units) for portable, mobile, and wearable products. While chip-last (RDL-first) FOWLP is suitable for packaging IC devices such as high-end CPUs, GPUs, ASICs, and FPGAs (field programmable grid arrays) for servers, networking, and telecommunication products.
- Of the three methods for fabricating RDLs, PCB technology with LDI is the cheapest, while Cu damascene is the most expensive. The method used will depend on the Cu linewidth/spacing and thickness of the RDLs. Usually, if the linewidth/spacing and thickness are $<5\mu\text{m}$ and $<2\mu\text{m}$ respectively, then Cu damascene is the preferred option; if they are $\geq 5\mu\text{m}$ and $\geq 3\mu\text{m}$, respectively, then polymer with ECD is the better choice; and for $>10\mu\text{m}$ and $\geq 5\mu\text{m}$, PCB with

- LDI can be used.
- For chip-first FOWLP, the choice of whether to use a reconfigured wafer or panel depends on the Cu linewidth/spacing of the RDLs. If it is >10µm, then use a large (610mm x 457mm) panel combined with PCB/LDI and SMT to increase manufacturing throughput and to save cost.
 - For chip-first FOWLP, the curing temperature of polymers for the RDL's dielectric layer should be less than the critical temperature (230°C) of the compression molded EMC.
 - For chip-first FOWLP, the curing temperature of the EMC must be lower than the release temperature of the double-sided tape.
 - For chip-first and chip-last FOWLP, high filler content EMC will shorten the time in mold, lower the mold shrinkage, and reduce the mold warpage. Uniform filler distribution and filler size of the EMC will reduce flow marks/fill and enhance flowability.
 - The equipment for P&P, RDLs, compression molding, solder ball mounting, and packaging handling for fan-out wafer/panel-level packaging have also been mentioned.

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Comparison between wet and dry silicon via reveal in 3D backside processing

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Wafer backside processing is critical for 3D-IC wafer stacking. Through-silicon vias (TSVs) typically formed using via-middle processing, are usually exposed from the backside of 300mm device wafers by the combination of mechanical grinding and wet or dry etch processes. A fast via reveal etch is required to have a productive etch rate, but also to have the precision necessary to control within wafer uniformity, selectivity to thin TSV liners and smoothness of post-etch surfaces. This makes in situ end point detection essential for controlled processing, especially as the target tip height is reduced to minimize cost. This paper compares imec's current wet chemical process of record with SPTS's dry etch approach. With the dry technique, 1 μm nail heights can be controlled within 300nm in order to minimize the overall cost per wafer by eliminating the need for rework steps. The applicability of such a process to extreme wafer thinning to 5 μm final Si thickness is also demonstrated.

3D technologies hold the promise to further enable system performance increase in a time where device scaling has become increasingly challenging. Among the many 3D options that are being explored and developed today, the 3D-stacked IC (or 3D-SiC) approach has become a mature and economically viable technology and provides the highest density for 3D interconnects to date [1]. 3D stacking and interconnecting components through TSVs is intrinsically limited to the stacking of thin dies or wafers, typically ranging from 100 μm down to 10 μm or lower. The most commonly used approach nowadays is via-middle where the TSVs are made after completion of the front-end-of-line (FEOL) and before the back-end-

of-line (BEOL). The formation of TSVs is not the only crucial element of 3D chip stacking. Backside processing, including wafer thinning and TSV reveal, is essential to access the TSVs from the wafer backside in order to make the required electrical connections during the 3D assembly process. Thinning of the device wafer uses a carrier wafer system to provide mechanical support. Achieving precise thickness control of the thinned wafer on carrier is critical for successful subsequent TSV reveal, passivation layer deposition, metal redistribution and bumping. In this via-middle approach, the starting residual silicon thickness above the via tips (also called TSV nails) can vary within a few microns, because of incoming accumulating nonuniformities from the TSV frontside etching, wafer bonding and wafer thinning processes, as shown in **Figure 1**. This makes in situ end point detection essential for controlled processing, especially as the target nail height is reduced to minimize the cost.

Options for TSV reveal processing

In the via-middle integration scheme, the main purpose of backside processing

is to expose the buried TSVs in order to make the future inter-die connections. Two approaches can be used for the via reveal processing.

One approach ("flat reveal") consists of grinding the Si bulk until the TSVs are reached. In this case Cu within the TSVs comes into contact and contaminates the Si wafer backside. This may be a risk for Si die <50 μm thick. The approach is useful when depth variations of the Cu TSVs are large (multiple microns of within-wafer variation) and/or the thin wafer thickness variation (TTV) is large (>4 μm).

The second approach ("soft reveal") is preferred because it prevents backside Cu contamination issues. Here the mechanical grinding is stopped before the first Cu TSVs are reached. Some silicon remains between the wafer backside and the tip of the TSVs, the so-called residual silicon thickness (RST). When the frontside TSV depth is controlled within tight tolerances (below 1 μm within-wafer variation) and the wafer thinning on carrier results in a low TTV, the resulting variation of the RST can be very small, in the range of a few μm . The remaining Si etch to expose the TSVs has to be

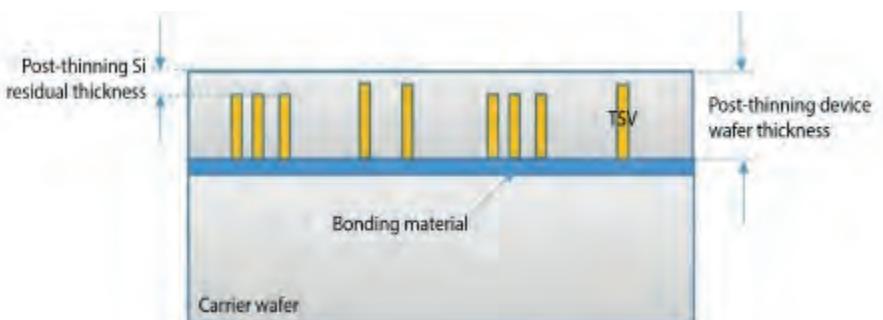


Figure 1: Illustration of a TSV device wafer on carrier after thinning. The residual Si thickness above the TSVs is the sum of all process contributors (TSV depth variation, bonding and thinning process variation).

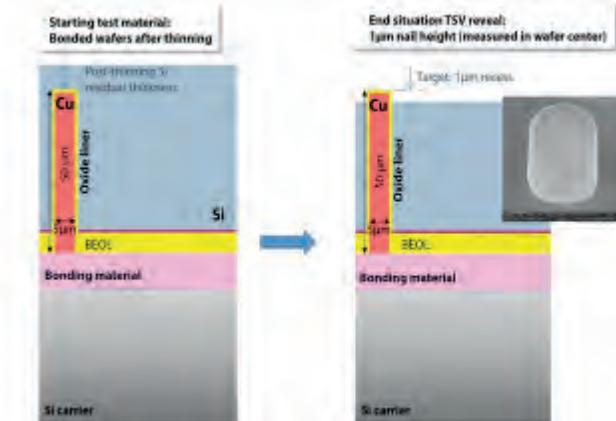


Figure 2: Illustration of the soft via reveal process.

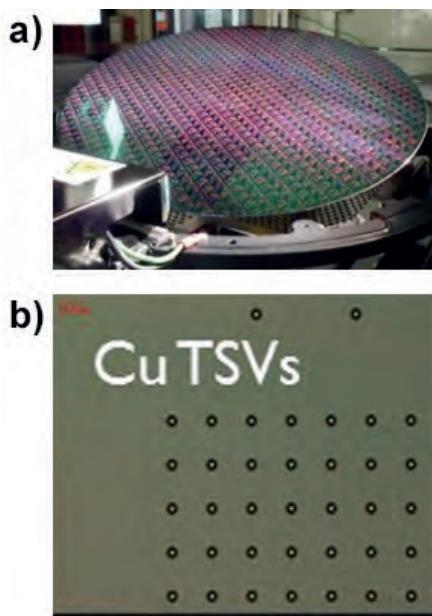


Figure 3: Photo of a 300mm wafer after TSV wet reveal a) and microscope picture of revealed TSVs b).

done selectively to the oxide liner. The TSV is passivated with dielectric and subsequently etched or CMP'd to expose the Cu [2]. Soft reveal etching can either be done using a wet or a dry process. An illustration of the soft via reveal process is shown in **Figure 2**.

This paper compares imec's current wet chemical via reveal process of record,

based on the selective TMAH chemistry, with SPTS's dry etch via reveal, based on an SF₆ plasma. State-of-the-art metrology has been used to image large arrays of revealed TSVs. Data on nail height control and uniformity, liner selectivity and surface roughness are presented and discussed.

Experimental

The imec process of reference (POR) is wet and uses TMAH solution with a center dispense as shown in **Figure 3**. Although this process has a good uniformity (<±3% variation across a 300mm wafer) and a high selectivity to oxide (>1000:1), the etch rate is low (about 1µm/min), and the current set-up does not offer end point detection. This makes the process difficult to control as multiple reworks are very often required to achieve the target TSV nail height.

Imec has also investigated a second option of a fast dry Si etch that offers a similar uniformity (<±3%) and a

high selectivity to oxide (180:1). This process, based on an SF₆ plasma, can deliver an etch rate >9µm/min and is offered together with an in situ end point detection system capable of detecting the presence of the Cu TSVs. This means that the reveal etching is fast and controlled and no longer requires any rework.

A 300mm SPTS Rapier system was used for the dry via reveal. The process combines high RF source power (~4kW) with a high gas flow to maximize etch rate. Uniformity is controlled by separating the RF powers and gas inlets into primary and secondary locations—referred to as dual-source design [3]. A uniform, highly dissociated plasma (with a high neutral F reactant density) is thereby exposed to the wafer. The temperature of the wafer is controlled using an electrostatic chuck. RF bias power is minimized in order to maximize selectivity to the liner oxide. This makes the etching mechanism highly chemical in nature with the final etch product being SiF₄. **Figure 4** is a schematic of the Rapier plasma chamber.

More recent wafers have been run on an SPTS Rapier XE module. This includes productivity enhancements to the Rapier design that increases the source power to ~8kW and increases the available gas flows. The result is a significant increase in etch rate (by a factor of ~2). Both plasma chambers include an in situ end point detection system known as ReVia®.

Prior to reveal etching, the wafers are thinned down on carriers by standard rough and fine grinding [2]. The

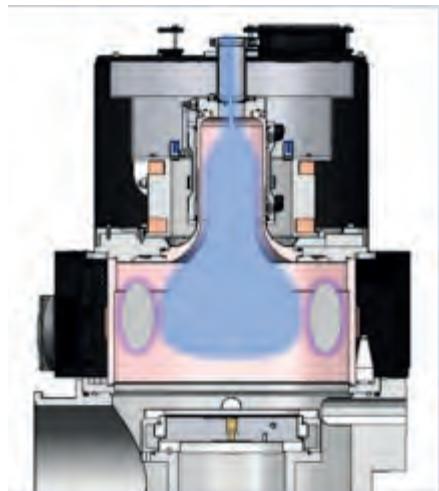


Figure 4: Rapier process module used for dry via reveal etching in an SF₆ plasma.

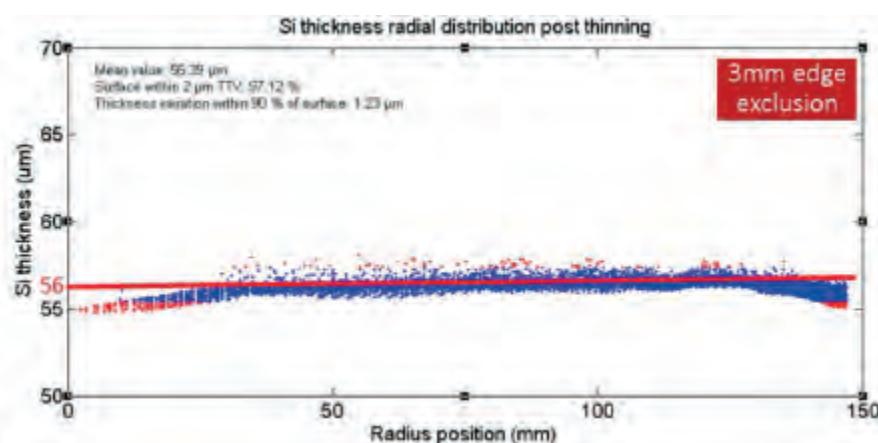


Figure 5: Top Si thickness variation across a 300mm wafer after thinning to a target value of 56µm.

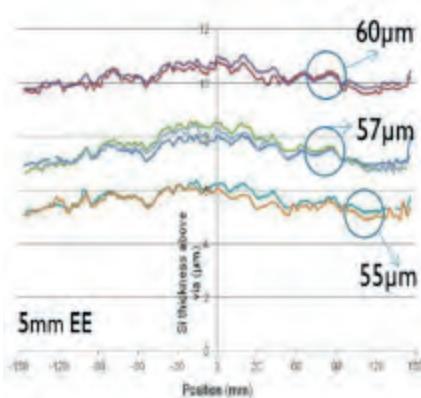


Figure 6: Thickness variation of incoming test wafers before dry TSV reveal (full wafer range <1.5μm).

grinding stops above the TSVs: 56μm thinning for 50μm deep TSVs, leaving about 6μm RST above the TSVs. The TTV of the wafer after thinning stays below 1.5μm as shown in **Figure 5**.

In order to challenge the dry etcher end point capability, three post-grinding thicknesses have been used as incoming test material: 55μm, 57μm, and 60μm, respectively, as shown in **Figure 6**. Two wafers of each thickness were dry etched. The TSVs were 50μm deep, similar to the wafers used for the wet PoR.

Results

Table 1 shows the main process characteristics of the wet and dry reveal approaches used in this work.

Wet etching results. A top SEM inspection of the TSV nails after wet reveal in **Figure 7** shows a center-to-edge variation in the 400nm range for a target TSV height around 2μm. This variation is the sum of all contributions from the TSV etch process to the TSV reveal process including wafer thinning.

Dry etching results. Etch rate and uniformity data for the Rapier & Rapier XE dry etching are shown in **Figures 8** and **9**. One of the 55μm wafers was used for process set-up. The remaining five wafers were etched using the automatic end point control to target 1μm nail height in the wafer center. The end point signals as a function of etch time are shown in **Figure 10** for the various incoming wafer thicknesses.

The ReVia® traces are grouped together based on the initial Si thickness. The data clearly shows the reproducibility of the process in terms of thinning control and dry etch rate. As expected, a longer process

time is observed for thicker Si wafers. **Figure 11** shows a top scanning electron microscopy (SEM) inspection of the TSV nails after soft reveal using the ReVia® end point detection system. Nail height in the wafer center is extremely reproducible, independently from the incoming residual Si thickness. **Figure 12** is a summary of the TSV nail height variations. A center-to-edge variation between 600nm and 800nm is measured. This variation is a combination of all process nonuniformities, including TSV frontside etch (in the 1μm range), the grinding process (1.5μm) and dry etch process (in the 0.4μm range).

Table 2 is a summary of the two process performances and compares the imec wet via reveal process and the SPTS dry etch process in terms of process uniformity and post-etch surface roughness. The wet imec process-of-record (POR) process slightly increases the incoming surface roughness from 9nm to 12nm, while the SPTS dry etch process smooths the surface from 9nm to 4nm as seen in **Figure 13**.

Note that the etch processes were performed without any post-grinding CMP step. The post-etch roughness could be further improved if a short Si chemical mechanical polishing (CMP) step is used before the TSV reveal.

But in the case of the dry etch, it may not be necessary to do this.

Extreme wafer thinning process

Another application of blanket Si etching is extreme wafer thinning for via-last processing. Here, controlling the final thickness of the top device wafer is critical [4]. Multiple challenges are seen in this

	Wet TSV reveal imec POR	Dry TSV reveal SPTS approach
Based chemistry	TMAH	SF ₆ plasma
Tool set-up	Chemical dispense, single-wafer etch	Rapier Rapier XE
Process uniformity	±2.4%	±3.2% (Rapier) ±1.9% (XE)
Selectivity to oxide liner	>1000:1	180:1 (Rapier) 170:1 (XE)
Etch rate	1μm/min	4.8μm/min (Rapier) 9.4μm/min (XE)
End point detection	Time based process	ReVia in situ

Table 1: Wet and dry TSV reveal process characteristics as used for process demonstration.

	imec wet TSV reveal	SPTS dry etch TSV reveal
Base chemistry	TMAH	SF ₆ plasma
Etch rate	1μm/min	4.8-9.4μm/min
Within-wafer uniformity	±3%	±1.9-3.2%
Oxide liner selectivity	> 1000:1	170-180:1
End point detection	Time-based process	ReVia system
Post-grinding surface roughness	R _a = 9nm (before via reveal)	
Post-etching surface roughness	R _a = 12nm	R _a = 4nm

Table 2: Process performance summary comparing the imec POR wet reveal and the SPTS dry etch via reveal.

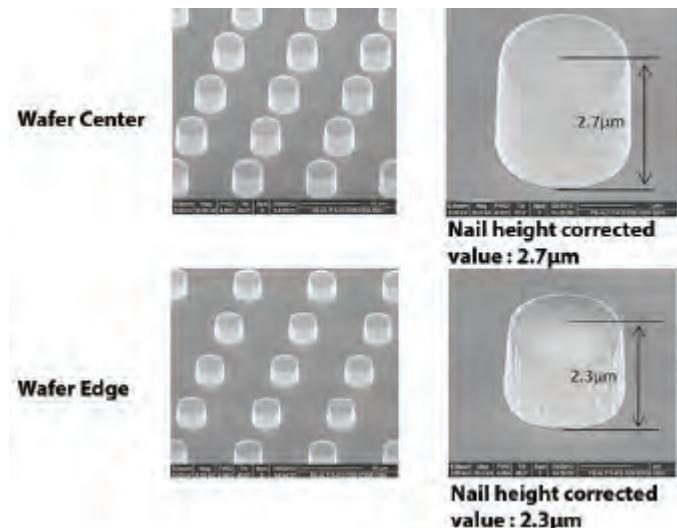


Figure 7: Top SEM inspection of TSV nails after wet reveal in TMAH (imec POR).

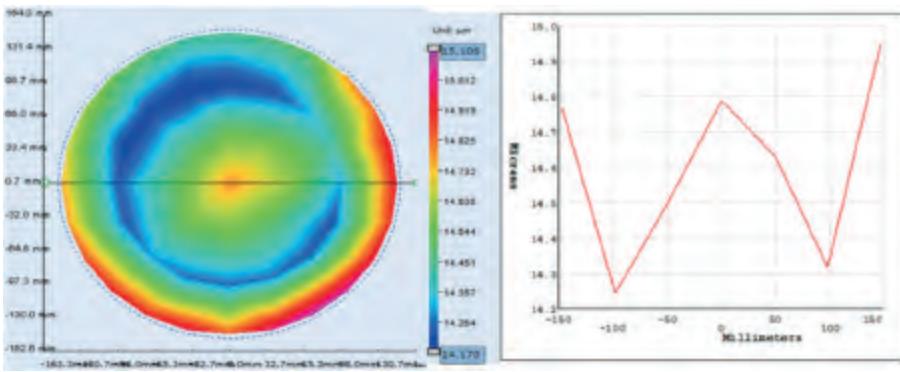


Figure 8: Rapier dry etch rate and uniformity for a bulk wafer. The etch rate is $4.8\mu\text{m}/\text{min}$, and the uniformity is $\pm 3.2\%$ (3mm EE).

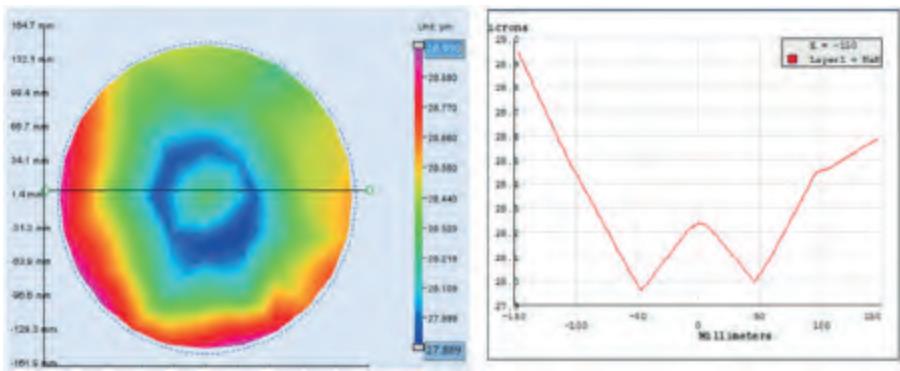


Figure 9: Rapier XE dry etch rate and uniformity for a bulk wafer. Etch rate $9.4\mu\text{m}/\text{min}$, uniformity $\pm 1.9\%$ (3mm EE).

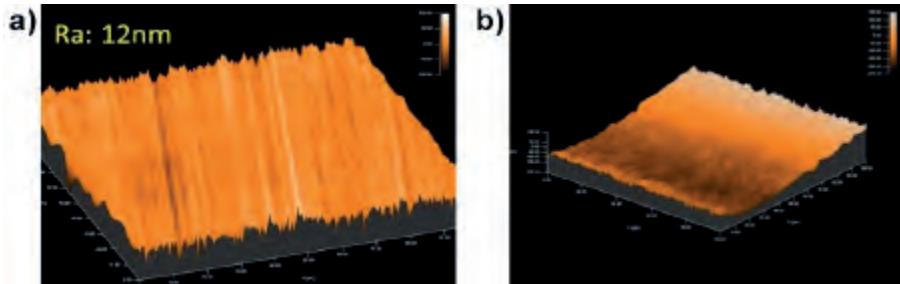


Figure 13: Surface roughness measured by AFM after wet TSV reveal a) and after SPTS dry etch b).

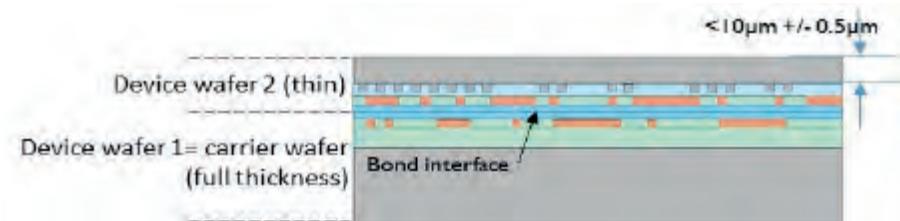


Figure 14: Illustration of the extreme wafer thinning concept.

application, such as optimizing the thinning to $10\mu\text{m}$ and below, delivering a good TTV of the bonded wafer to minimize the impact of the via-last over-etch process on the BEOL, and minimizing any plasma-induced damage to the FEOL device. An illustration of such an application is shown in **Figure 14**.

Wet etching lacks the precision required for this application. The same dry etching approach has been used based on the same Rapier XE process module. However, the ReVia® end point detection system is replaced in this instance by a near infra-red (NIR) interferometer (Verity Instruments model SD512NIR). The semi-

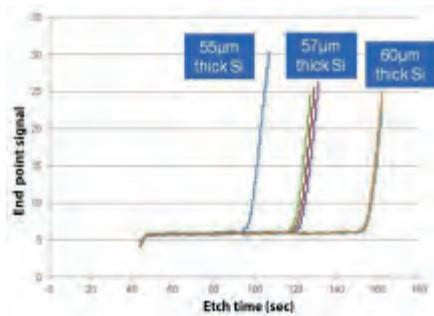


Figure 10: ReVia® end point detection traces for different incoming wafer thicknesses. The target is $1\mu\text{m}$ TSV nail height in the wafer center.

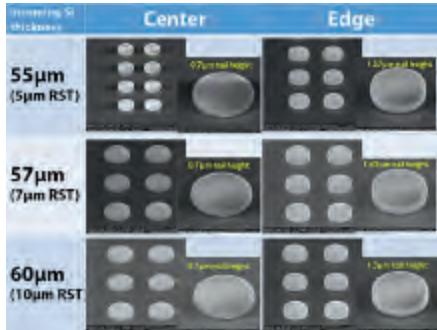


Figure 11: Top SEM inspection after TSV dry reveal using the ReVia® end point detection system.

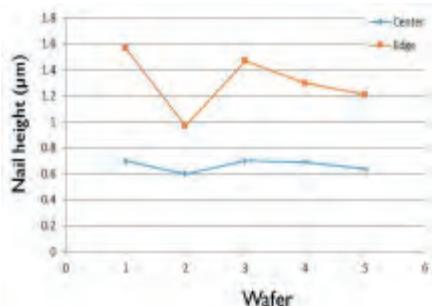


Figure 12: Overview of TSV nail height variation for the different processed wafers.

transparency of Si at the NIR wavelengths allows the NIR unit to continuously monitor reflections from the etching and back surfaces of the thinning wafer (together with any reflections coming from the bonding layer and the combined device circuitry). The system is able to output the top wafer thickness in real time as dry thinning proceeds.

A process demonstration has been done on permanently bonded wafers. The incoming top device wafer thickness was $52\mu\text{m}$ after fine grinding. The total thickness variation was measured to be in the $2\mu\text{m}$ range for all processed wafers. The same high Si etch rate (in this case $9.4\mu\text{m}/\text{min}$) plasma etch process



conditions have been used as for the via reveal application (except that the etch time was higher by a factor of ~6.7). The NIR end-point was set up to stop etching when the wafer was thinned to a maximum of 5 μ m. **Figures 15 and 16** show the total thickness variations before and after dry etching.

It is extremely encouraging that the TTV before and after etching is maintained, even despite the very high etch rate conditions. This is due to a combination of the dry etch uniformity and the precision of the NIR end-point method. Another important point is that the thickness variation post-etch is radially symmetric. The dual-source nature of the Rapier XE plasma chamber allows for recipe tuning to enhance either the etching at the wafer center or at the wafer edges. An example of the impact of recipe tuning is shown in **Figure 17**.

In the case of the extreme wafer thinning of **Figure 15**, enhanced etching at the wafer edges could result in a significant flattening of the final TTV distribution. In turn, this would mean that the post-thinning TSVs would have more consistent depths across the wafer. In the next phase of this work, recipe tuning will be implemented to improve the final thinned wafer TTV and broaden the process window for this device integration scheme.

Summary

Imec's wet-etch via reveal PoR has been compared to SPTS's dry via reveal. The dry option offers a range of technical and productivity (cost) benefits. Etch rates

above 9 μ m/min can be achieved while maintaining uniformity below $\pm 3\%$ and oxide selectivity at 170:1. In situ end point detection is key in reducing and controlling the TSV reveal height. Tip heights of 1 μ m are possible when end point detection is employed. The dry process also smooths out grinding marks in the Si and has the potential for eliminating a costly CMP step. Finally, a new integration scheme for 3D ICs

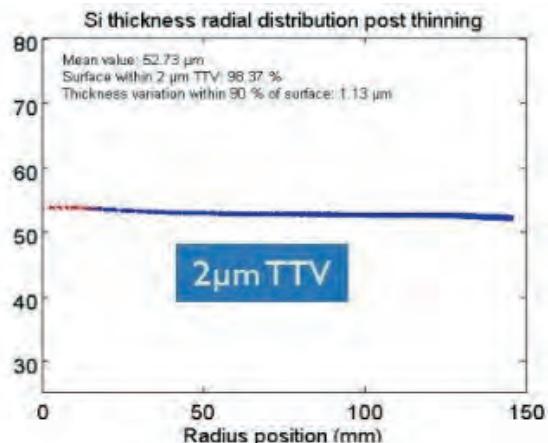


Figure 15: Top wafer TTV before dry etching. The wafer thickness is 52 μ m after grinding.

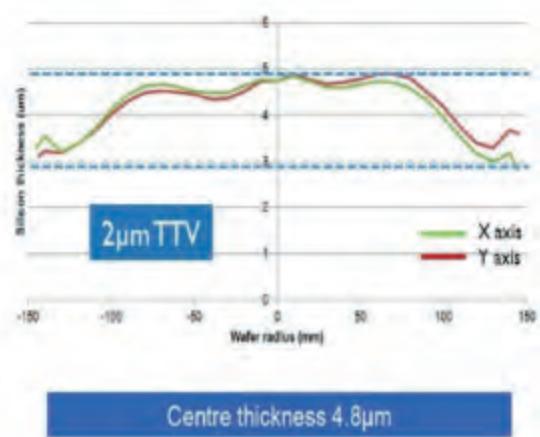


Figure 16: Top wafer TTV after dry etching. The target thickness is 5 μ m at the wafer center.

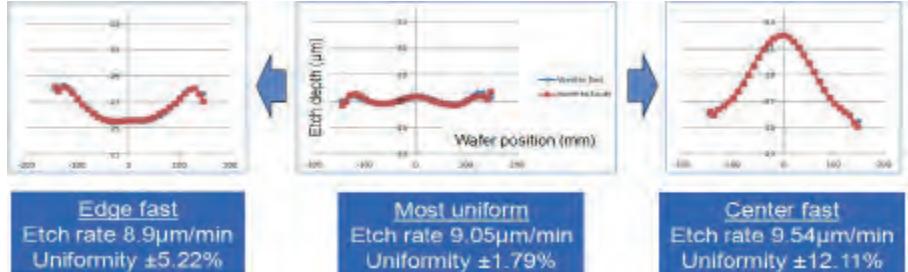


Figure 17: Example of recipe tuning for the Rapier XE to create edge fast or center fast etch uniformities.



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involving extreme wafer thinning to 5 μm has been realized by combining the high-rate dry etch process with a NIR end point detection system. The TTV of the incoming wafer is preserved at ~2 μm and the radial distribution of the dry etch uniformity could potentially be improved to further flatten the final thinned wafer. This would broaden the process window for the subsequent shallow Si TSV etching.

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Current state and evolving trends in MEMS packaging

By Mehran Mehregany [Case Western Reserve University]

Microelectromechanical systems (MEMS)—comprising sensors and actuators—augment the computational ability of microelectronics to perceive (i.e., sensing) and control (i.e., actuation) our world. MEMS sensors and actuators have been commercialized in a wide range of applications since the 1970s, including pressure measurements, motion sensing, optical projection, and fluid flow control to name a few. To do their work, sensors and actuators require a transduction mechanism, e.g., realized by a mechanical element in physical sensors. Generally stated, sensor transduction mechanisms convert nonelectrical parameters to electrical ones in a calibrated way, while the reverse is the case for actuators.

Compared to electronic chips, packaging of MEMS devices is more challenging. The goal in the former is to seal the chip from the environment. However, MEMS devices have to be protected from the environment, while also exposed to it for perception (i.e., sensing) and control (i.e., actuation). These two requirements are often contradictory. It is not surprising that pressure and motion sensors were first to be commercialized. In the former, the sensing chip can be isolated from the environment through a media-compatible means that seals the sensor while transmitting pressure. In the latter, the sensor chip can be sealed from the environment because inertial forces travel through the package.

Commercial evolution of MEMS actuators has evolved similarly to the evolution of sensors. MEMS optical displays and switches benefit from the fact that the MEMS chips can be sealed from the environment using a window material through which light travels (e.g., glass). Therefore, they have gained volume, including in consumer applications. MEMS resonators—used in timing and filter applications—also need not be exposed to the environment and are presently gaining momentum.

Most generally, the MEMS chip and its package have to be co-designed to ensure that

the device will meet the expected function, form and cost. **Table 1** outlines the evolution of MEMS technology, in the context of which, the packaging technology has evolved and continues to do so. As volume has grown and price eroded, packaging has moved from a low-volume, custom to a high-volume, standardized domain. In specialty applications, the chip cost is often far less significant than the packaging and testing cost. Examples of these are pressure sensors for aerospace, media-compatible and medical applications. In fact, the pressure sensor chip may be essentially the same in each case, while the packaging is custom to the application.

Figure 1 presents examples of MEMS sensor packaging in specialty applications. It would not be uncommon for these packages to include an application-specific integrated circuit (ASIC) for local signal conditioning and processing, particularly for capacitive sensors. The non-medical

with stress isolation, i.e., stresses that result from attachment interfaces and thermal mismatch of the materials in the package. These measures usually lead to larger and more expensive metal or ceramic packages.

Some industrial/chemical pressure sensing applications require packaging that is inert to the media of measurement. These media may be corrosive in nature—examples abound in semiconductor gas processing. Providing such media compatibility often requires using stainless steel packages and taking strong measures to seal the inside of the package from the media, for example, by using a thin stainless steel diaphragm—through which the pressure is transmitted—welded to the stainless steel body of the package.

Packaging of medical pressure sensors shares many of the same attributes, but must additionally conform to biocompatibility requirements. Package materials are usually metal (stainless steel or titanium) and glass.

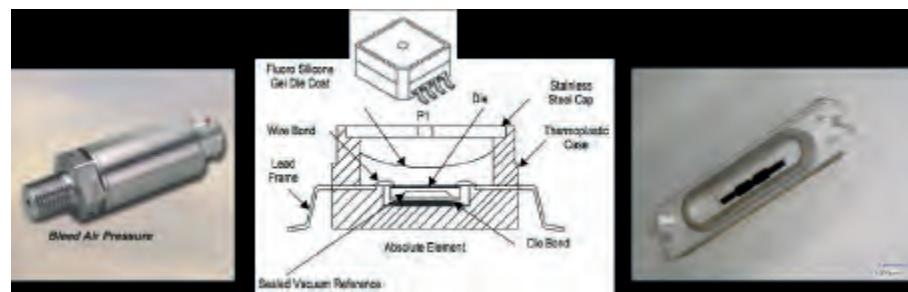


Figure 1: Specialty application packaging of a pressure sensor: a) Aerospace in stainless steel package (image courtesy of GE Measurement and Control); b) A media-resistant in thermoplastic package with a stainless steel cap (image courtesy of NXP Semiconductors N.V.); and c) Self-packaged implantable in glass, delivered by a guide wire (image courtesy of Mark Allen, U. of Pennsylvania).

packages are usually threaded so that they can be screwed in for installation; a 2000mm³ package volume would not be unusual in these cases. Specialty pressure sensors can range in price from about a few tens to several hundreds of dollars.

Some aerospace applications require high-accuracy, resolution and sensitivity pressure and inertial measurements, with extremely low long-term drift. In these applications, much of the packaging emphasis is on dealing

Package size is more restricted, particularly when the sensor has to be delivered by guide wire in minimally invasive applications.

In sum, the cost and size of the sensor in specialty applications are usually driven by packaging and testing, not that of the MEMS chip. In fact, there is an old saying in the MEMS community about startup product strategy: “When in doubt, do pressure sensors!” In other words, there are always specialty applications that can be

commercialized by custom packaging of commodity pressure sensing chips to build for small sustainable income.

The contrast in MEMS packaging is like night-and-day on the consumer end. Many component application opportunities are standardized to allow interchangeability. Today's high-volume MEMS components use packaging forms and processes of their integrated circuit (IC) cousins; surface-mount, and tape and reel assembly is essential. **Figure 2** presents examples of sensor packaging in consumer applications.

Devices such as inertial sensors and resonators, wherein direct exposure to the environment is not necessary, come (most commonly) in plastic land grid array (LGA) packages. Sensors that require access to the environment (e.g., pressure, humidity and gas) are packaged similarly, but incorporate a small top or bottom hole in the package (HLGA). The hole is located strategically for such environmental access, e.g., directly over/under the sensing diaphragm of the MEMS chip in pressure sensors and microphones. The hole may be in the top or bottom surface of the package. Use of a metal cap in such packages is not uncommon, particularly for shielding against electromagnetic interference when capacitive sensing is used.

Packaging and test cost considerations

Packaging and test are currently ~30% of the cost of the sensor in consumer applications. Footprints are generally less than 10mm² and heights less than ~1mm, resulting in a package volume less than ~10mm³. In sum, the trend is to have the package add minimally to the size of the MEMS chip. The footprint does not just accommodate the MEMS sensors, but also the accompanying ASIC, since most of these sensors are capacitive. In some cases, more than one sensor chip is included, e.g., six- (i.e., acceleration and rotation) or nine-(acceleration, rotation and heading) axes motion measurement. A consumer-volume pricing of ~\$1 for a single sensor solution is a good rule of thumb, though it can be much less in cases like microphones or more in cases of multi-chip package (MCP) multi-sensor solutions such as a nine-axes motion sensor.

Packaging of automotive sensors is generally similar to consumer applications, but size and cost are not as pressured. Automotive sensors often come in quad flat no-lead (QFN) packages. Package heights are near 1mm. Footprints are ~10mm² to ~50mm² and prices a few to several dollars

depending on the type and number of chips in the package.

Compared to the specialty application examples, the effects of packaging stresses on the sensor chip become less pronounced in automotive, and even less in consumer applications. There are two reasons for this. On the one hand, performance specifications like accuracy, sensitivity and resolution become less demanding. On the other hand, the effect of packaging stress on the sensor chip is less pronounced (**Figure 3**).

For specialty pressure sensor applications, the sensor chip is usually bulk micromachined to form the pressure sensitive diaphragm. As a result, the diaphragm is supported around its edges by the substrate frame. Any stress on the substrate from the package is directly transmitted to the diaphragm. In comparison, in sensors fabricated by polysilicon or silicon-on-insulator (SOI) surface micromachining, the sensitive elements are less affected by stresses on the substrate (i.e., from the package). Comparatively, the substrate is a uniformly thick support platform.

It would not be lost on the reader that another important difference in packaging of MEMS vs. ICs is that the MEMS chips usually have dynamic or static micromechanical elements, as well as treated surfaces. This situation is rather clear to envision for devices with moving parts. An example of a sensor

with static micromechanical elements is that of **Figure 3a**, wherein there are no moving parts. The flow is sensed by comparing the temperature difference between upstream and downstream thermopiles suspended over the cavity, wherein heating is from a resistive heater located midway between the two. The cavity is used for thermal efficiency. Other examples are humidity and gas sensors. In these devices, a thin-film catalyst is used; its electrical property (e.g., resistivity) changes when exposed to the intended stimulant. In order to increase the speed of response (humidity) and/or tune selectivity (gas) of the sensor, a resistive heater is incorporated under the thin-film catalyst. To reduce power consumption associated with the requisite heating, the combination is fabricated on a suspended micromechanical bridge.

Once the MEMS device wafers come out of the fab, they are singulated into dies. Various steps are needed to protect the micromechanical elements and the treated surfaces during singulation and further backend processing. In addition, at some point in the wafer processing, the micromechanical elements must be released to perform their intended function. Furthermore, there is a surface treatment step after the release in cases when the sensor has moving parts. Without surface treatment, these elements may stick to other surfaces that they contact as they

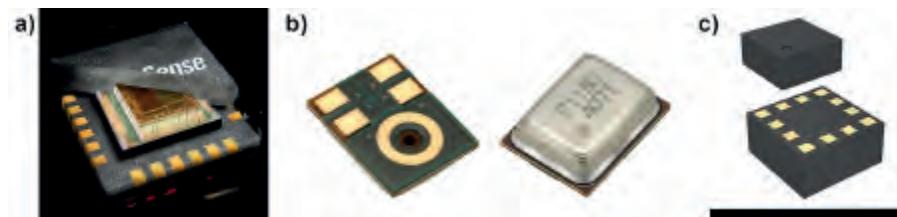


Figure 2: Consumer application packaging of sensors: a) A nine-axes motion sensor cutaway (image courtesy of InvenSense, Inc.); b) Top and bottom sides of a microphone package (image courtesy of Knowles Corporation); and c) Top and bottom sides of a combined humidity and temperature sensor package (image courtesy of STMicroelectronics).

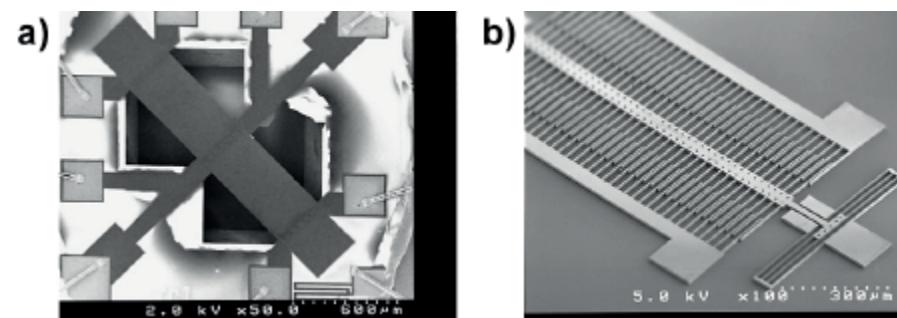


Figure 3: Effect of packaging stresses on the sensor chip: a) A bulk micromachined air flow sensor, wherein the sensing elements are suspended over a cavity bulk micromachined in the silicon substrate; and b) A surface micromachined accelerometer, wherein the sensing element is supported on the silicon substrate. SOURCE: Mehran Mehregany, Case Western Reserve University

Application	Material	Process	Inflection Point	Volume
Specialty	Silicon	Bulk/Bonding	1980s	Thousands
Automotive	Polysilicon	Surface	1990s	Millions
Consumer	SOI	DRIE	2010s	Billions
IoT	Flex?	Printing?	2020s	Trillions

Table 1: Evolution of MEMS technology.

move, failing to operate after backend process steps or in the field. This release step and surface treatment is usually near, or at the end, of the wafer fabrication process. Different companies do these provisions differently, often holding them as trade secret.

IoT considerations

The emergence of Internet of Things (IoT) will indeed force further evolution of MEMS packaging. Flex may become the newly added materials technology and printing the additional fabrication technology, while volume grows toward trillions. Together, they will create the need for new packaging techniques. A new paradigm is likely, one in which the chips are fabricated self-packaged, i.e., integrating the chip and package into a seamless design and fabrication process. In fact, we have been consistently moving toward this new paradigm as MEMS packaging has evolved per the evolution outlined in **Table 1**.

Wearables are a first step in evolution of IoT and a new application domain for MEMS sensors, with momentum rooted in activity monitors—initially standalone devices, and now transitioning to smart watches. Activity monitors leverage the size, performance and volume pricing of MEMS accelerometers. These products began in form factors that were compatible with printed circuit board (PCB) assembly, using MEMS devices packaged for consumer applications. Wearables are now evolving into products that leverage thin, flexible PCBs for a better form factor. These conformal form factors can still use consumer MEMS devices, though pressure will continue to build for further reductions in sensor package height and footprint to allow better product look and feel, as well as to pack more functionality. A corollary to this point is the likely trend that multi-sensor solutions will be packed into MCPS.

One can certainly envision a wide range of new sensors coming—including chemical and biological. Many such

sensors are undergoing research and development, and many have not yet been identified. Most will likely be challenged by the MEMS packaging contradiction, i.e., how to expose the sensor to the desired stimulant while protecting it from the environment. It is not hard to see that this contradiction becomes more challenging as we move into biological and chemical sensors, which is why gas sensors for air quality monitoring are being pursued as a much lower hanging fruit of this direction. The package can be HLGA, following in the footsteps of the examples above.

Smart watches are moving rapidly to integrate new sensors for monitoring additional vitals, motivated by displacing pure activity bracelets. For example, current smart watches are integrating sensors for pulse and blood oxygen. For now, the sensors are packaged into the watches' housing, but as the housing disappears into a flexible, conformal wearable, the sensor packaging approach must evolve as well.

Everything else being equal, wearables will likely be the key IoT driver of MEMS packaging changes than other applications (e.g., industrial, agricultural, environment, food, etc.). These other applications do not seem to present similar packaging miniaturization pressures. Nevertheless, volume growth toward trillions

will necessitate new material and process technologies to reduce sensor cost substantially. Without self-packaging (i.e., fabricating the sensor and its package in an integrated process), the packaging and test component of the sensor cost would be a barrier.

Finally, conformality is an enabler of many new applications, for example smart labels. Printing is a high-throughput, low-cost process. The combination of flexible substrates and printed electronics and sensors will perhaps provide a new pathway for realizing the trillion-sensor volume driven by IoT. The packaging requirements and strategies to support these developments are yet to be developed.

Biography

Mehran Mehregany received his Masters and PhD in Electrical Engineering from Massachusetts Institute of Technology and is the Veale Professor of Wireless Health Innovation at Case Western Reserve U. and Director of the Case School of Engineering San Diego; email mxm31@case.edu



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Plasma dicing methods for thin wafers

By Christopher Johnston [Plasma-Therm LLC]

The concept of employing deep silicon etch technology to dice wafers is called plasma dicing. The technology delivers very high dicing quality results and design flexibility. As a parallel process, it dices the entire wafer at the same time without die size sensitivity. From a cost perspective, plasma dicing is very attractive for thin and small devices. Larger products benefit from the higher dicing quality attained and limitless wafer layout designs. Several methods for plasma dicing are offered today to address risks with thin wafers and overcome integration challenges for various devices. As a consequence of product diversity, plasma dicing processes have various levels of complexity, costs and limitations. Upon exploring the various process options, key factors to consider are wafer preparation and support, dicing process and post-processes.

Today, semiconductor devices performance, packaging and cost requirements are demanding higher wafer dicing quality, flexibility and speed. Thinner and smaller packaging trends are limited by blade and laser dicing methods due to the mechanical and thermal stress and longer process times for smaller devices. Plasma dicing is a chemical process that offers significant advantages as described in **Figure 1**. This article will examine the different approaches to perform plasma dicing: plasma dicing before grind (DBG), plasma dicing after grind (DAG), laser grooving for plasma dicing, and plasma dicing on tape (PDOT).

As the need to increase the number of die per wafer continues to grow with each product generation, the spacing between die is limited by the precision and dicing quality of mechanical dicing systems. Such systems have numerous dynamic forces that are very difficult to control in addition to the variation from system to system and processing materials. As a result, the variation in die size and defect control area limit wafer layout designs. Squeezing accuracy performance from mechanical systems can be an expensive battle. However, the yield risk

may be so high that extensive process control systems and metrologies must be employed. Plasma dicing offers an opportunity to regain process margins with near perfect dicing accuracy (**Figure 2**). It may be possible that delivering ultra-low variation products to downstream processes could have a positive “snowballing” effect with alignment, placement, bonding, dispensing errors, and defects as a secondary benefit.

Plasma dicing methods

There are four main approaches that have been developed to perform plasma dicing. The process flows for each method are explained in **Table 1**:

- DBG with and without additional mask
- DAG w/ additional mask
- Laser grooving followed by plasma dicing
- PDOT

DAG and DBG differences

In standard dicing process flows, dicing occurs after the wafer grinding or thinning step (i.e., DAG). DAG processes are used for >35 μm thick wafers, as shown in **Table 2**. Ultra-thin wafer DAG may require trimming the wafer edge

bevel to reduce risk of wafer edge damage. To achieve wafer thicknesses <50 μm [1], the DBG process is more common. DBG

Lower Cost of Ownership for small die and thin wafers	+ Thinner wafers = faster dicing time. (i.e. 50 μm thick wafer < 3 minutes for dicing)
Maximized die per wafer or additional functionality per area	+ Optimized die placement: non-orthogonal streets. + Less wafer starts, more capacity
No shape, size or layout constraints	+ Freedom to dice any shape, multi-product wafers. + Reuse/move/relocate tool alignment areas
Higher die strength	+ No chipping or micro-cracking + No mechanical or thermal stress
Highest accuracy	+ Die size variation determined by the mask

Figure 1: Benefits of plasma dicing.

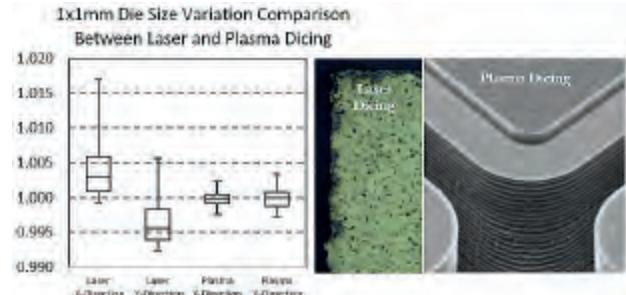


Figure 2: Die size variation between laser and plasma dicing. SOURCE: ON Semiconductor, Arizona, 2014

Thin Wafer Plasma Dicing Process	Thinning			Dicing				Thinning					
	BG Tape Lamination	Wafer Thinning	Wafer Mounting	Laser Grooving	Wafer Ablation	Wafer Cleaning	Litho Mask	Mask Exposure	Etching	Ashing	DBC Tape Lamination	Wafer Thinning	Wafer Mounting
Plasma DBG										*			
Plasma DBG*										*	*	*	*
Plasma DAG*	*	*	*					*		*	*	*	*
Grooving + Plasma DAG	*	*	*	*	*	*				*	*		
PDOT	*	*	*							*			

*Requires an additional mask

Table 1: Plasma dicing process flows.

Process	Dicing Process Per Wafer Thickness	
	Wafer Thickness	Kerf Width
DAG	>35 μm	>4 μm *
DBG	<50 μm	>30 μm **

*Achieved with Plasma Dicing on Tape Process

**Achieved with special Backside Grind Tape

Table 2: Dicing process per wafer thickness.



Figure 3: 1000 to 1, SiO₂ mask-to-silicon selectivity with the PDOT process.

Plasma Dicing Cost and Quality Comparison					
Plasma Dicing Process	Setup Costs	Dicing Costs	Cleaning Costs	Dicing Quality	Kerf Width
Plasma DBG w/o Additional Mask	None	Special Materials	In-situ	Competitive	>300μm
Plasma DBG w/ Additional Mask	High	Special Materials	Separate System	Competitive	>300μm
Plasma DAG w/ Additional Mask	High	Special Materials	In-situ	Competitive	>300μm
Laser Grooving + Plasma DAG	Medium	Multiple steps	Separate System	Laser (optional)	<300μm
Plasma Dicing on Tape (PDOT)	None	Low	In-situ	Competitive	>4 μm

Table 3: Plasma dicing process cost and quality comparison.

reduces some of the damage risks with mounting ultra-thin wafer on tape frames. In the DBG process, wafer dicing occurs during the wafer grind process exposing the partial kerf or blind etch done during the dicing step.

Successful plasma dicing requires proper support and wafer preparation. In the plasma DBG process, the full thickness wafers are partially diced and maintain enough rigidity for the next process steps without any additional support. Partially etched wafers require wide kerfs for the special backside grind tape adhesive to penetrate into the kerf to reduce damage during the wafer separation in the grind and mounting process. DAG process wafer support is required to hold the die together after dicing. The plasma etching process occurs in a vacuum environment and at temperatures that may cause problems for standard dicing tapes. Some of the problems that arise are wafer and chamber contamination, tape damage, or residue. Systems not compatible with standard dicing tapes may require special vacuum and high-temperature compatible tapes or other forms of tape protection.

Wafer preparation for plasma dicing

The areas that are not to be etched by the dicing process may need to be protected or covered by a mask [2]. Depending on the aggressiveness of the etching system, bumps, pads, any metals or materials prone to damage or contamination may need protection. For most dry etch applications, the areas left unmasked, such as the spacing between die, will be attacked by the plasma. The mask thickness is determined by the selectivity, etch rate of the mask material versus the silicon, and the silicon amount to be diced. The costs

to prepare wafers for plasma dicing can be overwhelming for some processes. It is important to note that some or all of the setup costs for plasma dicing can be eliminated with a high-selectivity dicing system used in the PDOT process. The plasma Singulator™ system by Plasma-Therm is a high-selectivity plasma dicing system requiring no additional mask protection. The PDOT process employs the passivation layer [3] as the mask (example shown in **Figure 3**) to dice the wafer.

The dry etch process requires direct access to open the silicon in the streets for the plasma to dice the wafer. This access may include opening the mask through exposure or a laser ablation process. Non-silicon structures in the streets, test element groups (TEGs), alignment features, or process control monitoring (PCM) structures [4] interfere with the plasma reaching the bulk silicon underneath. Street structures are commonly

removed via blade dicing or laser grooving processes that increase yield risks caused by the mechanical and thermal damage that was induced. The street structures take up valuable wafer real estate, which could be used for more devices. The capability of plasma to dice any shape and extreme narrow features is enabling more and more efficient wafer designs.

Plasma dicing process

Process gases, SF₆ and C₄F₈ are used in the time-multiplex alternating etching/deposition cycles to etch the exposed silicon and to control the vertical anisotropic profile. For the DBG process, partial etching is completed when a predetermined number of cycles reaches the desired depth. In the DAG process, the completion of the dicing process is determined once all exposed silicon is etched. The etched silicon byproduct emission is monitored by an optical emission endpoint control system. Once the byproduct signal disappears, the street silicon has been etched and the dicing process stops. Endpoint detection becomes very challenging for wafers with small amounts of exposed silicon area and may require more sophisticated detection systems.

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Post-dicing cleaning

Once the etching process ends, there may be residue materials that require stripping or cleaning. The deposited polymers that control the etch profile, may cause corrosion or affect downstream processes and require stripping. Some plasma dicing systems include an in situ polymer stripping in the same process chamber. Other processes require external cleaning systems to remove left-over mask materials, as well as etching polymers (see **Table 3**).

Summary

Advanced packaging trends are becoming so diverse that not one dicing solution can solve all challenges. Wafer layouts and die designs are formed around manufacturing capabilities. These design rules will continue to evolve as new manufacturing capabilities are qualified. The wafer preparation steps have the biggest cost impact and the point of definition in the process flow are device-specific. Materials such as oxides, photoresist polyimides, photosensitive polyimides, metals,

metal oxides and water- soluble protective materials have been used with success. To open the silicon for plasma dicing, a number of strategies can be used. The lowest cost option technique is to remove the non-etchable material as part of the process flow or redesign the test structures to eliminate the problem. The ability of plasma dicing to etch very fine features, high-aspect ratios and any shape will enable creative solutions around test structures. This design approach is already implemented in small die products such as RFIDs, LEDs and power devices employing plasma dicing techniques to solve quality/reliability issues, reduce dicing cost-of-ownership (CoO), and improve die per wafer outputs. Plasma dicing is a competitive advantage that is soon to spread to more applications as the first 300mm wafer production systems are delivered in 2016.

Acknowledgements

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Biography

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Automated inspection between the die improves yield and reliability

By Scott Balak *[Rudolph Technologies, Inc.]*

As back-end assembly and packaging processes become more complex, manufacturers are finding an increasing need for automated optical inspection (AOI) to detect defects. Until now, most AOI has been focused on the active area of the die while the “streets” that separate the die have been largely neglected by the user because, in theory, they have little to do with the functioning of the integrated circuit. As is often the case, problems develop where you are not looking. In this situation, problems arise during the die singulation process where multiple types of defects can occur (i.e., chips, cracks, delamination, etc.) If severe enough, the defects will propagate into the active area. Even more problematic is the potential for chip-related defects, such as delamination, to cause device failure after the die has been packaged and is in the field. Chip inspection poses a number of challenges to conventional AOI methods. A new approach addresses many of these challenges and provides an automated go/no go inspection capability that can be tuned to accommodate the acceptable risk profile for the inspected product.

Final package quality is really a combination of yield – determined by the ratio of good devices to bad at the completion of the manufacturing process – and reliability, determined by the number of devices that fail at some later time in the field. Any product loss at the assembly phase of the manufacturing process is expensive because the devices are nearly finished and most of the manufacturing costs have already been sunk. Yield problems at this stage are bad enough, but at least they occur while the product is still at the manufacturer, and manufacturers have become very good at detecting and correcting problems that cause yield excursions. Reliability issues can be much more challenging and costly. They occur once the device is in the field and can result in much greater damage to the customer and to the supplier. Moreover, their causes are often much more difficult to diagnose.

Historically, yield levels have been high at assembly because geometries were large (relative to front-end processes). However, this picture is changing significantly as packaging and assembly processes become more complex and geometries become smaller. As further advances in the front-end have become more

difficult and more costly, emphasis has shifted to the back-end to continue the industry’s progress toward more power and functionality in smaller devices – a trend sometimes referred to as “More than Moore.” Advanced packages now have multiple redistribution layers (RDL) and conductors that are smaller and closer together. With more layers come more thermal processing cycles, which introduce more mechanical stress among the layers. Ultrathin substrates, which result in highly warped wafers and die, also pose a challenge to advanced packaging and inspection processes.

Changes in front-end processes are also causing problems that often do not become apparent until assembly, or worse, as reliability problems in the field. The impact of their changes on the back-end are often not the first priority for front-end engineers wrestling with design and yield problems of their own. Perhaps the best known of issues in this category is the propensity of low-k dielectric layers to delaminate after dicing. This is representative of a class of problems that result from the mismatch of stress between layers caused by differences in their thermal expansion coefficients. Front-end process engineers are careful to manage these stresses during the wafer fabrication process, and increasingly back-end process engineers are as well, but the balance of stresses changes dramatically when the large, round wafer is cut into small, rectangular die using a rough mechanical process – sawing.

The dicing process is further complicated by the constant pressure to make devices smaller, which results unavoidably in narrower streets, less distance between the saw kerf and the die and tighter process windows for controlling the path of the blade and the roughness of the sawn edge. The final ingredient in this troublesome mix is the presence of test structures in the streets. These structures, composed of materials with entirely different mechanical properties than the silicon substrate, can cause significant deviations in the cutting process when they are encountered by the saw blade.

Excursions in the singulation process can cause yield problems, but the more troublesome issues are those that result in reliability failures in the field. A chip that occurs during the sawing operation may not extend into the active area of the die and may have no immediate

effect on die performance that can be detected during testing. However, it may serve as the locus for delamination that continues over time, exacerbated by the thermal cycling that occurs during normal use, and ultimately results in failure in the field. Traditionally, AOI has focused on the active area of the die and excluded areas outside, including the space between the circuit and the edge of the die. In fact, conventional AOI is difficult to perform in this area and prone to overkill, false positives that result in very expensive and unnecessary product loss. One problem is that the size of typical chips at the edge of the singulated die can be quite large relative to the nanometer scale of variability seen for defects in the active area. Another issue is that the test structures in the streets may or may not be visible after singulation because of variations in the kerf location. Moreover, these structures repeat with the reticle, not the die, and so are not incorporated in the model pattern to which the inspection data are compared. As a result, they often appear as false positive nuisance defects that should be ignored.

For these reasons and more, dicing inspection has traditionally been limited to human operators using optical microscopes. This approach has its own problems, most notably, variability among operators or by the same operator over time, limits on the inspection area imposed by the inherently slow speed of the inspection process, and the lack of automated reporting procedures that are possible with AOI.

Manufacturers have tried a number of methods to improve the dicing process. Among the most promising is the combination of automated fault detection and classification (FDC) methods with kerf line metrology to improve control of the dicing process. Another approach has been the addition of infrared (IR) microscopes to the visual inspection process. The ability of IR to see through silicon allows the operator to better evaluate the extent of the chipping, but it does not get away from the shortcomings of human-based visual inspection. Finally, there are six-sided AOI tools that actually pick up the die to inspect top and bottom surfaces as well as all four sides/edges. Unfortunately, these tools are prohibitively slow and expensive and, therefore, used only when they are absolutely necessary.

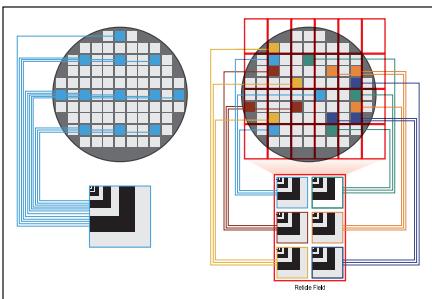


Figure 1: Reticle based training–test structures in the streets between die repeat with the reticle not the die. They are not included in the gold standard model used in traditional pattern-based inspection (left) and, therefore, typically appear as nuisance false positives unless the area outside the die is excluded. The new algorithm builds a reticle-based model (right) that does include the test structures, permitting them to be treated appropriately by the inspection system.

A new approach

Rudolph has developed a new solution based on standard AOI technology. It is intended to be used for simple go/no go inspection, as opposed to process control/process improvement. It can effectively detect dicer chipping excursions that are likely to lead to reliability problems. The system inspects the active area and edges simultaneously so there is essentially no penalty in throughput. The solution begins with a modified inspection algorithm that recognizes the die seal ring at the border of the active area and can measure the distance between the ring and a chip at the edge of the die. The algorithm permits the user to specify a minimum acceptable distance and, thus, adjust the risk profile to an appropriate level for each product. It is also aware of the reticle-based location of test structures and incorporates these structures into the inspection model (Figures 1 and 2). Finally, it classifies detected defects as kerf defects, corner defects or active area defects to assist in defect review and automated sorting decisions (Figure 3). The system's pattern-based inspection technology delivers high-sensitivity and low-noise performance that is essential in assembly applications where the cost of false positives is so high.

The inspection is also capable of wafer-level die quality judgements based on a comparison of expected and actual die location or on die rotation. When a wafer is singulated normal relaxation of stress in the wafer results in a slight increase in the distance between die after the cutting operation. If the actual distance is less than expected, it suggests that the separation is not complete, due perhaps to insufficient depth of cut that leaves silicon connecting the die. If the separation is larger than expected, the cut may have been uneven or misplaced, or there may have been an excess of local wafer stress. Rotated die may result from kickback of the saw blade and is often associated with large chips at the die edge. Changes in the position

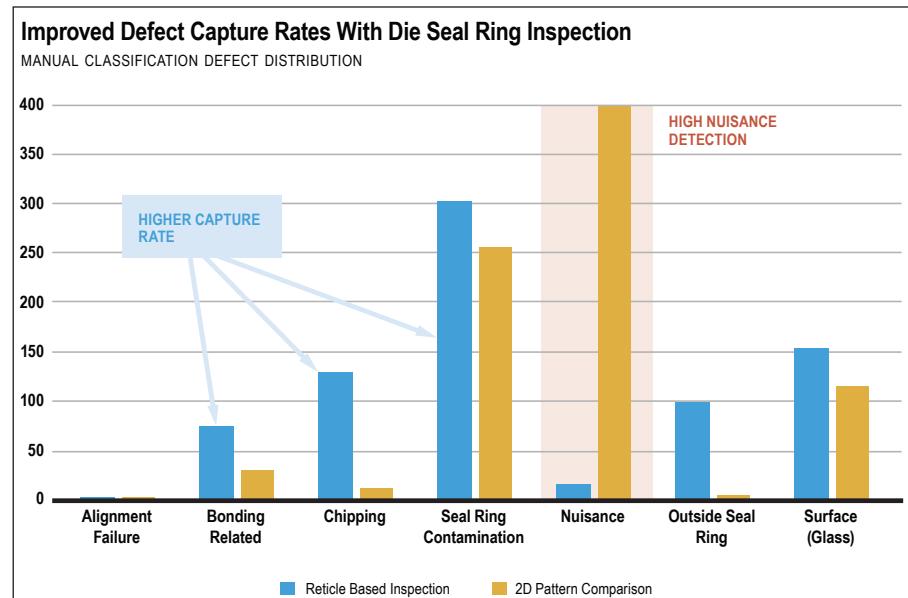


Figure 2: This chart compares results of AOI using a conventional 2D algorithm (gold) and the new reticle-based algorithm (blue). All detected defects were classified manually for this comparison. In all cases the new algorithm demonstrated excellent sensitivity, capturing more defects in each category except the nuisance category. In the nuisance category it showed excellent ability to eliminate false positives caused by test structures.

or rotation distribution across the wafer also indicate problems with the dicing operation.

Finally, the inspection system offers IR microscopy during defect review (Figure 4). As described above, IR's ability to see through the substrate can help the reviewing operator make a better evaluation of the true extent of the chip, though this evaluation may be challenged by non-transparent metal often used in the die seal ring. As an automated inspection technique, the system can automatically send alarms, analyze and report data and transmit data to yield analysis software programs.

Summary

Defects at the edge of a singulated die often result from the sawing process used to separate the die and have, until now, been difficult to detect using conventional AOI techniques. These defects often escape detection during final test yet lead to failures in the field, frequently from delamination. A new approach uses pattern-based inspection that is aware of reticle-based test structures located between die, which often appear as nuisance defects. The new approach has demonstrated excellent sensitivity to defects outside the active area of the die while at the same time reducing the number of false positive nuisance defects caused by test structures. The system includes a simple binning capability that can classify defects on the basis of user defined criteria, such as the distance between a chip and the die ring exclusion, defect size, area, color, and many more, thus enabling efficient defect review and go/no go sorting decisions.

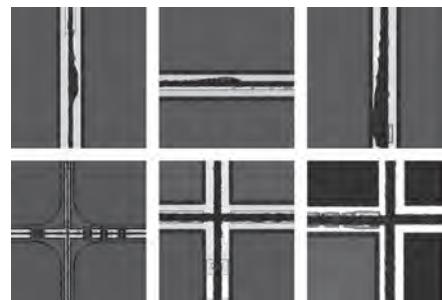


Figure 3: Several examples of defects. Bins may be defined based on a number of criteria, including: the distance between the chip and the die seal ring, defect size, defect area, color, and many more.



Figure 4: The figure on the left was taken using visual optics, on the right using IR optics. The extent of the chip on the backside of the substrate is apparent in the IR image.

Biography

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Final test solution for WLCSP devices

By Andy Nagy *[Xcerra]*

Wafer-level chip-scale package (WLCSP) devices are widely used because they offer low cost, small height and small footprint packages to be directly mounted into smartphones, tablet PCs, and other mobile devices. WLCSP devices are even being used in some automotive applications. The manufacturers of these mobility and automotive products are demanding very low defect parts per million (DPPM) from their suppliers of WLCSP devices. Today's back end process for WLCSP is not satisfying this low DPPM quality requirement sufficiently and reliably. This is because there is no final test after singulation—a process that can damage a die and result in defective devices getting shipped to the field.

The established back end process flow for WLCSP devices is a single insertion test only at wafer probe. After device singulation by wafer saw, with the wafer mounted on a film frame carrier, the devices will proceed directly to final packaging without an additional final test step. The only quality measure to identify defects from sawing is a 5S vision inspection right at the tape and reel equipment. Functional defects that cannot be detected from visual inspection will escape and reach the final customer. The reason for this flow is because there has not been a cost-effective way to handle, and final test, singulated WLCSP devices in a high-volume manufacturing environment.

To reduce the risk of quality escapes, the defect levels of the 5S inspection are down to 10 and 20 μm levels. At this defect size, the vision system will require more often than not the final judgement of a human operator to decide if the identified issues are really defects or only cosmetic marks. This is driving an increasing number of operator assists and as a result, the cost-of-test is increasing dramatically, as the inspection at low defect levels is much more time consuming, thereby significantly slowing down the taping speed.

Another shortcoming of the probe test process is the lack of direct support of the retest of returned materials authorization

(RMA) devices. After singulation, the device cannot get retested on a prober with the same tooling setup. It requires the redistribution of the devices on a film frame at a different device to device pitch. Hence, the test parallelism is typically down to only one site to avoid expensive investment in new contactors and probe cards.

Xcerra has developed a solution using InCarrier™ device carrier technology to address the high-volume manufacturing challenges for the final test of WLCSP devices. The new technology was designed to hold up to hundreds of singulated devices in an array looking similar in format to a device strip (**Figure 1**). By placing the singulated devices into an InCarrier, a strip test handler can then be used to provide true final tri-temp testing of WLCSP devices. The same carrier and strip test handler can also be used to retest RMA devices with the original test setup at any time.

The carrier technology has been in volume production for more than 5 years with billions of devices tested. The cost-effective and robust architecture of the carrier has several layers of edged sheet metals that are welded together (**Figure 2**). The basic configuration comes with a bottom and top layer that sandwiches a layer with a precision pocket matrix where each pocket contains two springs to hold the singulated die in place.

The device is automatically loaded into one of the carrier pockets, while the two springs are biased to the side to enlarge the pocket size and to insure an interference-free placement. When the springs are relaxing, they will bias the device into a precision corner to clamp and register it precisely in the carrier matrix. The precision is good enough to support highly parallel contact pitch testing down to 0.3mm, with a roadmap to 0.2mm. The precision pocket contour is curved to stay away from the sensitive device edges and corners. The spring layer is shimmed with a distance layer to touch the device only in the center of its side wall.

The clamping spring forces are comparable to a typical contact pogo pin force. The



Figure 1: Handling singulated WLCSP in strip format with InCarrier.

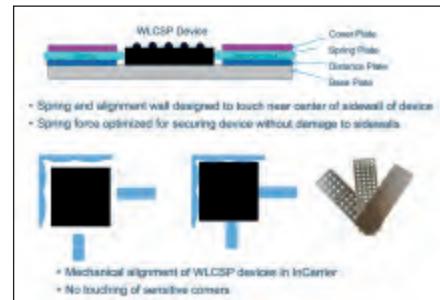


Figure 2: Basic InCarrier architecture for WLCSP.

resulting stress on the silicon die is only 5MPa, a factor 100 times less than the critical failure stress for brittle silicon, and therefore does not cause any harm to the die.

Xcerra has proven damage-free handling of WLCSP devices with its technology during several evaluations for very large mobile chip manufacturers. The evaluations included intense stress tests such as repeatable positioning and clamping of devices and handling of several wafers with final 5S vision inspection (**Figure 3**).

After successful proof-of-concept and feasibility, the total cost-of-test, including handling, is becoming a relevant concern that requires thorough analysis. One of the main contributors to this equation is the cost of bad quality. The cost of a defective device that escapes and reaches the final product has to be quantified by each customer and application. It is the main justification to look for a lower DPPM process and its associated cost.

The redistribution of a device after sawing to a new kind of carrier is characteristic for the final test requirement. Final test on a

Die Stress Analysis

5 MPa max. stress on the silicon die
→ 100x lower than maximum failure stress of die

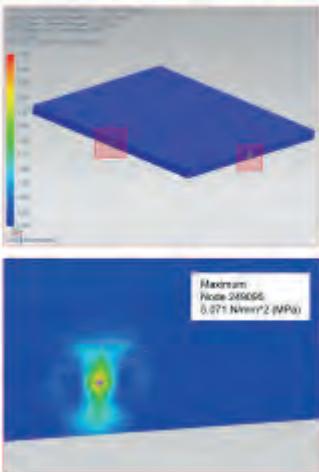


Figure 3: Die stress analysis with FEM.

and overall temperatures. Another positive throughput contributor is the 100% touch efficiency. While a wafer touch efficiency can be down to only 80% on account of its round-shaped device arrangement that should be contacted with a linear, diagonal or matrix contactor. This results in a higher throughput.

At first glance, the metal InCarrier seems to be more costly but because of its 10,000 cycle lifetime capability, the cost-per-cycle is 500 times less expensive than the disposable film frame carrier. Blue tape is not inexpensive. Depending on the type of tape, the cost-per-wafer ring handling cycle varies from 30 cents to \$1.00. In addition, the standardization of the new carrier technology helps to drive cost down further. Important for WLCSP technology, which does not offer standard devices sizes, the new technology is able to accommodate a range of device sizes, which minimizes the number of carriers required and supports faster time-to-market.

The spacing between DUTs for easier load board/probe design, and the use of a strip test

handler versus a prober, typically offers the capability for higher parallel testing at a lower tooling cost. The load board footprint of a strip handler typically offers more real estate for component placement compared to a probe card solution. The strip contactor technology offers lower cost contact solutions, all the way down to a 0.3mm pitch.

While all the arguments noted above are supporting InCarrier for final test, there is still the general concern that a second test insertion could neglect the WLCSP cost advantage versus the fan-out WLP types. A key question to address is if WLCSP final test could completely substitute for probe test. The answer is yes. The technical enabler is the virtual reconstitution of the wafer map using final test data. The tracing of the InCarrier test results back to the original wafer position is supported by simple device mapping during the device loading step (**Figure 4**). Certainly, the quality relevant probe data would only be available after singulation and final test, but the cost of

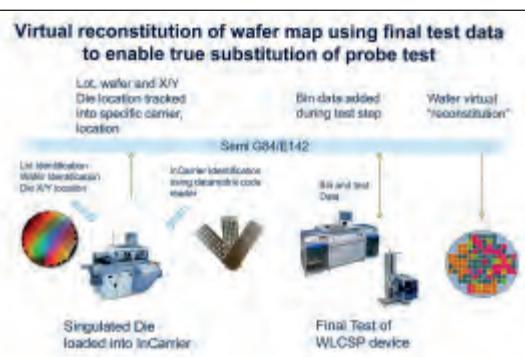


Figure 4: Wafer data back-tracking from final test. film frame carrier immediately after dicing is not recommended because it introduces additional risk for chipping. The gap from sawing between the devices is so small, that the sensitive device edges and corners will likely randomly touch each other and break off during handling and test. Therefore, the process step to load singulated dies to a new single device carrier seems to be a given, regardless if an InCarrier, a film frame carrier, or any other type of carrier is used.

The InCarrier supports faster test throughput and higher contact yield than a film frame test because of its more precise device registration with mechanical alignment. The film frame process relies strictly on the positioning tolerances of the loading tool and has to deal with nonlinear creeping behavior of the film, which is especially compromised at temperature test. The new carrier technology, therefore, supports higher parallel test setups even at smaller device pitch

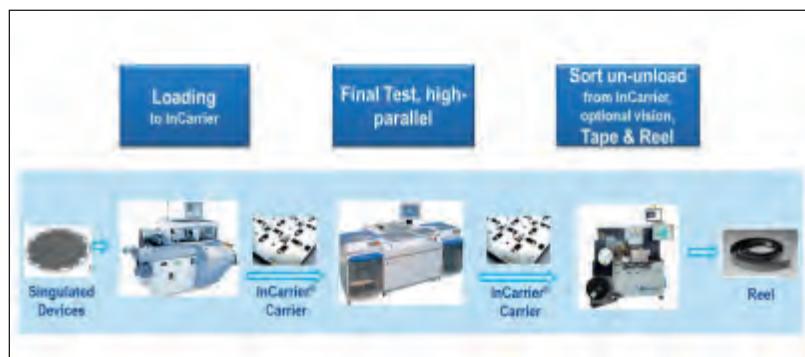


Figure 5: Final test for WLCSP, RCP, eWLB, LGA and BGA.



Figure 6: InStrip and InCarrier cassette as the FOUP of the back end.

probing will be eliminated and the WLCSP final test process would be similar to the cost structure of the current WLCSP process.

If final test of WLCSP with the new technology will enable the elimination of wafer probe testing, the remaining process steps of the WLCSP back end process flow are wafer saw, device loading from blue tape carrier to InCarrier, highly parallel final test on a strip test handler, and the sort-unloading from InCarrier to tape and reel. The 5S vision inspection prior to taping may remain as an optional test, but certainly not at the same defect size requirements required for probe test, and therefore it will be a lot faster and need reduced operator assistance.

The flexible off-line flow of the new carrier technology process with its individual machines for the different process steps offers the most cost-effective solution. In the early days of strip test, integrated lines were dominating the test floors of the early strip test adopters. Fifteen years later, most of these lines have been eliminated and replaced by flexible off-line setups. Why? Because of the line effect: the total overall equipment effectiveness (OEE) of an integrated line is the product of all client OEEs, which will significantly decrease the effective output. Flexible off-line setups are dominating the test floors.

The effect of flexible off-line setups is also relevant for InCarrier test. The flexible off-line setup of the individual clients will insure that each client will be able to run at its optimum OEE and therefore contribute at its optimized application specific cost (**Figure 5**). This also helps to minimize the machines required for the specific application. A high-volume tri-temp test setup requires much less loading and unloading capacity than an ambient flow, which might require higher loading and unloading capacity. Optimized flow balancing is the key terminology for cost advantage. Certainly, there is a higher number of carriers required than in an integrated line, but the cost for these carriers is manageable with the help of the standardization of carriers, which was described earlier, and the long depreciation time over 10,000 cycles.

Unlike the semiconductor front end, there is still very little process automation in the back end. One of the reasons might be the different transport media that are in use, with different form factors and handling concepts involved. The most common transport means are JEDEC tray, tube, metal magazine, and wafer ring. Front end automation basically deals with only one form factor—the wafer and its standardized transport container, the so-called

wafer front opening unified pod (FOUP).

The transport media between loading, test and tape of the new WLCSP final test are slotted cassettes, which provide the same form factor for all packages. This standard cartridge could support automation requirements of the standard back end final test process similar to the wafer FOUP at the front end (**Figure 6**). This is certainly a forward-looking question that will get answered over time by our industry's sensitivity to cost.

But ultimately, the final test of WLCSP with the new carrier technology will address the shortcomings of today's probe test flow and enable the replacement of probe test.

Biography

Andy Nagy received his Masters degree in Mechanical Engineering at the Technical U. of Munich and is a Sr. Director of the Marketing Handler Group at Xcerra; email andreas.nagy@xcerra.com

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STATS ChipPAC's Fan-out Wafer Level Packaging Shipments Exceed 1 Billion Units

STATS ChipPAC announced that it has shipped over one billion fan-out wafer level packages (FOWLP), also known in the industry as embedded Wafer Level Ball Grid Array (eWLB). FOWLP or eWLB is an advanced packaging technology platform that provides ultra-high density interconnection, superior electrical performance and the ability to integrate multiple heterogeneous dies in a cost effective, low-profile semiconductor package.

As the industry was beginning to learn about eWLB in 2008, STATS ChipPAC immediately recognized the significant potential, value and scalability of eWLB and designated it as a key technology for the company. Within a year, STATS ChipPAC had ramped eWLB to high volume production and was driving a number of technology and manufacturing initiatives in this new packaging approach. STATS ChipPAC has led the industry in eWLB manufacturing capabilities, capacity and technology innovations, particularly in 2.5D and 3D package designs. STATS ChipPAC became the first company in the semiconductor industry to implement significantly larger than 300mm eWLB wafer manufacturing capabilities and has a strong portfolio of innovative eWLB packages, including small die, large die, multi-die, multi-layer, Package-on-Package (PoP) and System-in-Package (SiP) architectures.

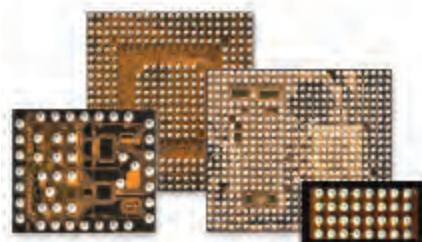
"We differentiated STATS ChipPAC by our unwavering commitment to eWLB technology over the years, beginning with our vision of how this scalable packaging platform can be leveraged to drive performance and size advantages for our customers' applications. Over the years we have made significant capital investments and process enhancements to fulfill our vision and raise the bar on manufacturing efficiency and productivity in the industry, adding further value for our customers," said Dr. Han Byung Joon, President and Chief Executive Officer, STATS ChipPAC. "Although we have achieved multiple milestones with eWLB through the years, shipping over one billion eWLB packages is a testament to the ever expanding customer adoption in the industry and success which we knew was possible with this game changing technology."

The exceptional success of eWLB in the mobile market, particularly in baseband processors, connectivity devices, Codec devices, RF transceivers and power management integrated circuits (PMICs), is a reflection of the ongoing pressure semiconductor companies face in cost effectively achieving higher input/output (I/O), higher bandwidths and lower power

consumption in the smallest possible form factor. STATS ChipPAC has driven a number of eWLB technology achievements such as dense vertical interconnections as high as 500 – 1,000 I/O, very fine line width and spacing down to 2um/2um and ultra-thin package profiles below 0.3mm (including solderball) for single packages and below 0.6mm for a stacked PoP with proven warpage control.

With the ability to partition silicon and embed passive devices and vertical interconnects (known as eBar) into a design, eWLB is a powerful integration technology for 2.5D and 3D PoP or SiP solutions for a wide range of new and emerging applications. The compelling performance, size and cost advantages of eWLB are accelerating the adoption of this advanced technology into new markets such as the Internet of Things (IoT) and wearable electronics,

Micro-Electro-Mechanical Systems (MEMS) and automotive applications. Examples of new eWLB applications are Advanced Driver Assistance Systems (ADAS) in automobiles and bio-processors in the wearables market.



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BiTS is coming to Suzhou!

The Burn-in and Test Strategy (BiTS) China Workshop will be held on **September 13, 2016 in Suzhou**. Over the course of its seventeen-year history, BiTS has established itself as the preeminent event for test and burn-in consumables, test cell integration, and test operations. BiTS China will highlight what is *Now & Next* in the test and burn-in of semiconductors.

"After an extremely successful inaugural event last year with over 300 attendees, there is a great deal of excitement for BiTS China 2016. BiTS has always been a very international event with > 40% of the recent attendees from overseas demonstrating that the overall value of the event is not unique to the local test community. The strong interest from China reinforces this further," said Ira Feldman, BiTS Workshop General Chair.

The full-day program will feature world-class technical presentations including a prominent keynote speaker and award-winning presenters from BiTS as well locally submitted content. A BiTS EXPO will facilitate networking and meeting with various international and regional suppliers and supply chain partners to the industry.

BiTS Shanghai will be held at the **DoubleTree by Hilton Hotel Suzhou**. "This is a brand new facility which is conveniently located. With nearby access to the Metro and expressways, it will be easy for local and international attendees alike," said Steven Zheng, BiTS China Chair.

For full details on participating please see www.bitsworkshop.org. "There are a limited number of BiTS EXPO spaces and sponsorships still available. But we expect to sell out quickly," continued Steven.



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