Chip Scale REVIEW®

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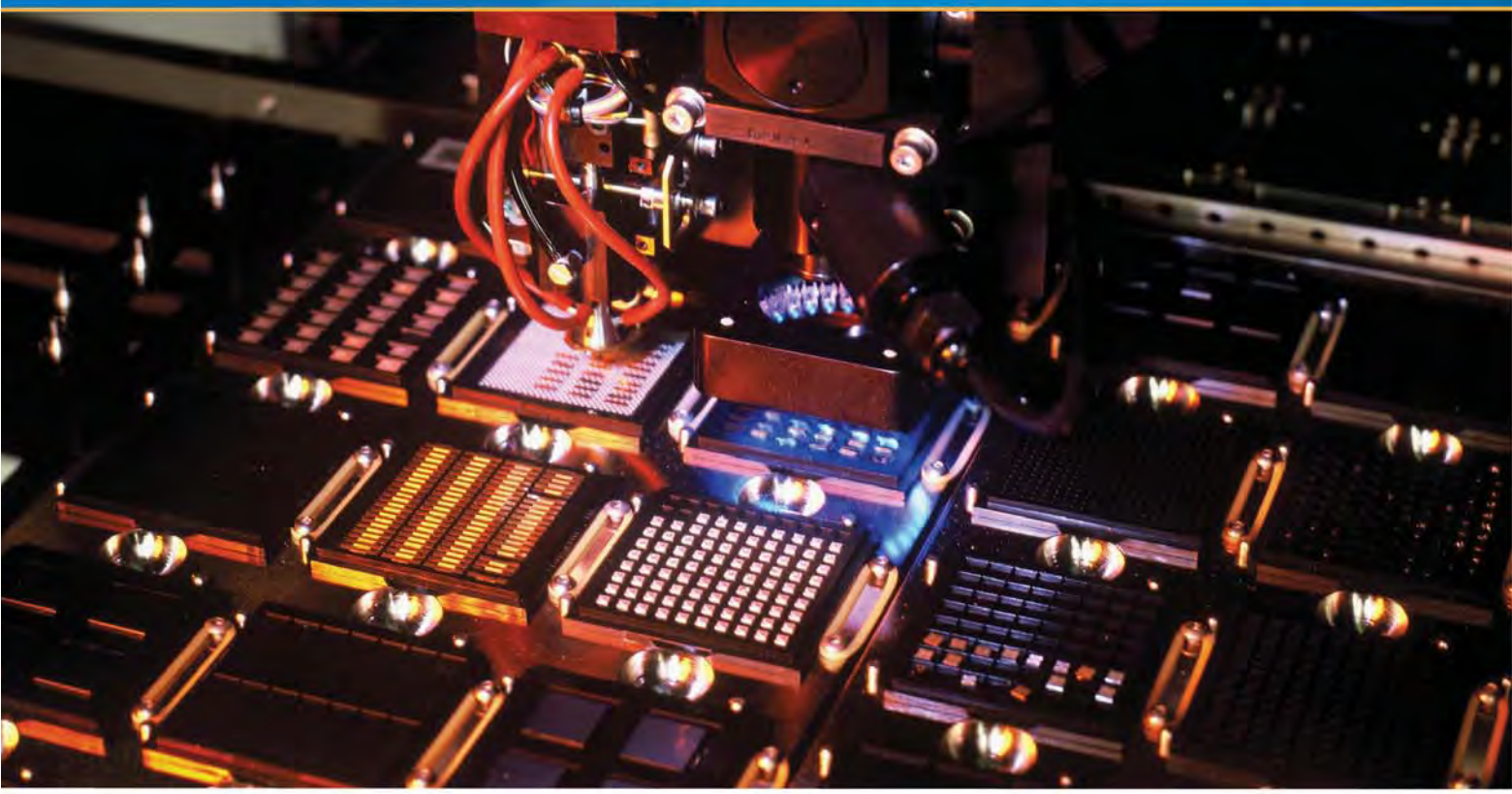
Volume 14, Number 3 May-June 2010

- Defect Inspection Systems
- New Realities for TSV Processing
- Advanced Chip-to-Wafer Bonding
- Die-attach and Flip-chip Bonders / Aligners



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May-June 2010

Volume 14, Number 3

Chip Scale REVIEW

The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/ Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

Photograph by Jeff Maloney: This edition's cover depicts a technician inspecting a wafer through a defect inspection system in a clean room environment. Chip Scale Review brings to readers The International Directory of Defect Inspection Systems which provides the most comprehensive listing of Acoustic, Optical & XRay Systems.

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VOLUME 14, NUMBER 3

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FROM THE PUBLISHER

Oh the Cycles . . . Time to Spring Ahead!

By Kim Newman

The seasonal weather cycles of summer, fall, winter, and spring are known globally and can have significant impacts on business as related to product purchasing cycles and the bottom line of your company. Those of us in the electronics industry are all too familiar with the impact of cycles on revenue, and although not as predictable as annual weather temperature, our industry continues to cycle through the highs, lows (or very low as in 2009) and then back to the high, with many attempting to predict a cycle. I can predict the seasons: fall – leaves will *fall* from the trees, spring – flowers will appear to *spring* up from the ground. But the prediction of electronics cycles . . . well, I prefer to leave it to the experts.

Interesting as well is a practice here in the US (excluding Hawaii and Arizona, although I am not sure why) of changing the time on a clock back 1 hour (falling back) in the fall month of November and then ahead for 1 hour (springing ahead) in the spring month of March, to take full advantage of daylight hours, termed Daylight Savings Time. The saying I have heard for years, spring has sprung, has even more significance this year as I see a dynamic spring rebound and growth in the electronics industry. These are positive industry trends at a very critical time for many companies that strategized and sacrificed throughout 2009 and are now poised for the opportunity to expand their industry position and presence.

The majority of companies in the electronics industry are now taking aggressive strategic advantage of the current positive business trends and increases in revenue to spring ahead. There are several indicators that are tracked by the CSR staff showing the positive continuing momentum. The increased number of technical articles submitted for publication can be linked to available corporate resources and new product developments. Approvals on corporate marketing funds have led the way to increases in numbers of exhibitors and attendees at recent CSR-sponsored events. The funding has also increased advertising budgets, as companies capitalize on revenue growth, with visibility on existing and new products and services.

Companies positioned to spring ahead are leading those companies that are somehow stuck in the cycle of falling behind, specifically in the area of new product development and technical marketing. CSR sees the focus to expand the technical scope of our annual CSR/SMTA – IWLPC event, with many areas of interest in assembly and test, including bonded wafers, chip scale packages, stacked die and through-via technology, and flip-chip and/or wire-bonded configurations. Review the many updated and expanded supplier directories in CSR. They list sources for the following: sockets and connectors, subcontract assembly, wafer bumping, die attach/flip-chip bonders, and defect inspection equipment, with more to follow through the year.

The key objectives of CSR are to bring our loyal readers the latest in technical innovations and business trends, and to give global visibility to our advertisers, working together to continue to *spring ahead in 2010*!

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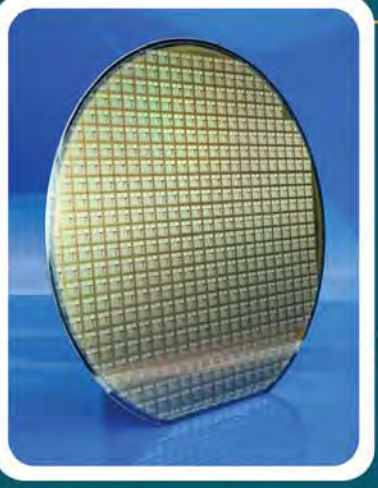

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EDITOR'S OUTLOOK

Keeping Your Cool in an Overheated World

By Ron Edgar [redgar@chipscalereview.com]

A few years back I was involved with a PCB design that required putting a dozen DSP chips on a very small circuit board. It quickly became apparent that the biggest problem we had was keeping the board cool in spite of considerable airflow. One of my coworkers composed a picture of a hot dog sitting on top of one of the DSP chips, sizzling strongly! He posted this on the corridor wall of his cube. The reaction was humorous but the problem was serious. It cost the company huge bucks to solve the excess heat problem.

The IC heat problem has plagued designers since the beginning. Heat can destroy chips and, at best, slow down their function. Cool chips work faster. Modern processors can easily generate 100 watts or more. Look inside your desktop and you will see that metal sculpture rising with crazed fingers, grimly grasping a hard-working fan. So how do we keep our cool in an overheated world?

The most common solution today is, of course, a heat sink like the one described above, and many variations thereof. While effective but inefficient, they fail to attack the problem at the source and are further impeded by the package. Some chips expose the silicon through the package and this helps. But the real problem is getting as close to the source as possible. Usually there are hot-spots on chips and it would be good to pay special attention to these. While not new in concept, developments like thermal Through-Silicon Vias (TSVs) are helping to focus on the trouble spots and wick heat away from the inside of the silicon. While close to the source it is, like the heat sink, purely passive.

Much research has been done, and continues to be done, in the field of active cooling, that is, using electronics as a means of cooling. Thermoelectric cooling devices using the Peltier effect have been around a long time, but due to their inefficiency they have only found limited application. Research into another thermoelectric effect at the chip-scale level was announced in Nature Nanotechnology, published online, January 25, 2009. Titled *On-chip cooling by superlattice-based thin-film thermoelectrics* it reports in the abstract, "… we show the integration of thermoelectric coolers fabricated from nanostructured Bi_2Te_3-based thin-film superlattices into state-of-the-art electronic packages. We report cooling of as much as 15 °C at the targeted region on a silicon chip with a high (~1,300 W cm^{-2}) heat flux. This is the first demonstration of viable chip-scale refrigeration technology and has the potential to enable a wide range of currently thermally limited applications." The joint team from Intel, Arizona State University, Nextreme, RTI International, and NMB Technologies sadly also report, "However, fully functional practical thermoelectric coolers have not been made from these nanomaterials due to the enormous difficulties in integrating nanoscale materials into microscale devices and packaged macroscale systems." The technology has a way to go. However, I am hopeful that we will see the commercialization of this and other research in the not too distant future.

Continuing our thermal theme, in their article Zane Johnson and Nathan Schneck of the Center for Nanoscale Science and Engineering, North Dakota State University, wonder about *High Thermal Conductivity Underfills—How Much Do They Help?* In our inspection article from David Richard of Vi Technology, *Improving CMOS Camera Module Manufacturing Costs in Back End Of Line (BEOL) Environments*, he explores potential yield and cost advantages. While he focuses on a CMOS camera module, much of what he says has wider application. Our major article this edition is *Advanced Chip-to-Wafer Bonding Enabling Silicon-in-Package (SiP) Production with Low Cost of Ownership*. Written by a team from the EV Group (EVG) and Datacon Technology GmBH, both in Austria, they provide a detailed look at new chip-to-wafer bonding techniques and processes. AZ Tech Direct, LLC, has prepared two directories for us, *International Directory of Failure Analysis/Defect Inspection System Suppliers* and *International Directory of Die Attach & Flip-Chip Bonders/Aligners*, both exhaustive and very useful.

New for this edition is a business focus section. Penned by Liz Richards of Richards and Lord, her article on outsourcing office management answers the question *When to Call In the Cavalry—or at Least Get a Faster Horse*. Sandra Winkler in her regular Emerging Trends space takes a look at *The State of the Industry*. We have our usual sections on Industry News and What's New, with the latest announcements and new products. Keeping you well informed and mentally stimulated within the pages of our magazine is our goal and our way of helping you keep *your* cool in an overheated world.

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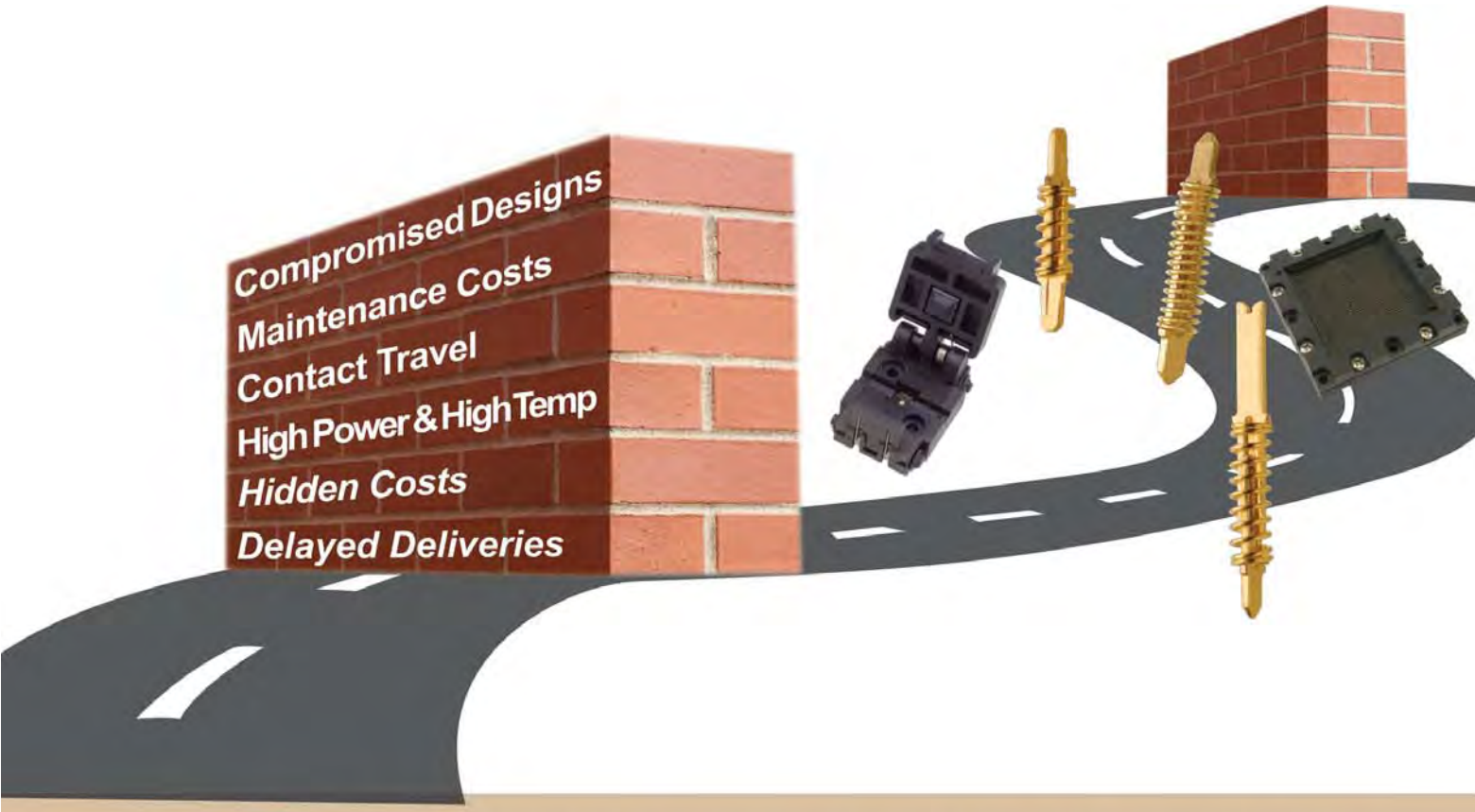

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The State of the Industry

By Sandra Winkler, Contributing Editor [slwinkler@newventureresearch.com]

The Great Recession that began in the fourth quarter of 2008 had an enormous effect on world economies in 2009. The bursting of the housing market bubble in the U.S. resulted in the meltdown of financial institutions around the world. Electronic Trend Publications (ETP, now New Venture Research) predicted 2009 to be a year in which the industry would dovetail a bit due to normal cycles in the industry, but the depth of the downturn in world economies was certainly not predicted. ETP had also predicted a downturn in 2001, likewise due to normal industry cycles, but again had not predicted the depth, as the bursting of the dot-com industry had not been predicted.

However, the semiconductor industry fared better than many this time around, pulling back up in the second half of 2009. The following table compares the two downturns.

Year	2001	2009
Revenue($M)	118,490	190,341
Rev Change	-33.0%	-8.8%
Units(M)	68,550	144,630
Unit Change	-20.8%	-6.9%
ASP($)	1.73	1.32
ASP Change	-15.5%	-2.1%

First of all, semiconductors recovered with both revenue and units considerably higher in 2009 when compared with 2001, but ASPs were lower. But the turnaround came back up considerably faster in the 2008/2009 downturn than in the 2000/2001 downturn. Why?

Inventories

Inventories were considerably higher in 2000 than in 2008. Prior to the downturn at the end of 2000 there had been a massive build up of inventories of lesser-priced parts. These parts had to be burned off or discarded due to obsolescence before new purchases would be made. Inventories have been leaner since, so there were no inventories to be burned off in 2009 before new purchases of semiconductors would take place.

Consumer Spending

Consumer spending turned downwards in 2009, as many people in all industries found themselves unemployed. Even for those who kept their jobs, uncertainty in continued employment kept wallets from freely opening. To combat this, all leading world governments put forth stimulus packages to step up consumer spending. It did get the money to start flowing again, and U.S. consumer spending rose twice as fast as income in March of 2010 (Source: News Alert, The Wall Street Journal, May 3, 2010).

While the downturn reduced spending on larger computer products, the invention and sale of smaller, less expensive computers such as netbooks and notebooks did well. Tablets such as e-readers and the iPad have become instant successes due to their low price. Products under only a few hundred dollars seem to do well, even in a downturn.

Further Influences

Fluctuating oil prices and the value of the Euro are need-to-watch items. The higher the price of oil, the higher the price for all goods that require transportation, plus more money is spent at the pump. This results in less money left over for other items such as computers, televisions, and other luxury consumer items. The economies of Spain and Greece are threatening the stability of the Euro, and Greece was recently bailed out by European partners. The net effects of these on global spending and economic health are yet to be seen.

Unemployment rates remain high, but with new inventions and new employment opportunities, more people will enter or re-enter the work force, boosting spending on products that undoubtedly will contain semiconductors. Indeed, semiconductors are prevalent in products sold around the world, touching the lives of even remote peoples on this planet.

The explosion of products demanded in every day lives is actually quite impressive. One generation ago a home with a single television was the norm, and automobiles quite simple with engines with catalytic converters and a radio with both AM and FM stations a luxury. Today's automobiles are laden with ICs, and incorporate creature comforts and safety features not heard of a generation ago. Nearly everyone carries around a cell phone. Most homes have not only at least one television set, but also a minimum of one PC as well, and likely one PC per family member! Digital cameras have largely replaced film, and to get the best in print quality of those pictures, an upgraded printer is necessary as well. Indeed, the demand for ICs has continued to climb upwards, despite the occasional downturn. With world economies continuing to gain steam, so will the IC industry continue to gain momentum, for an even brighter future in the years ahead.

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- Stacking Processes
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- SIP/SOP vs. SOC
- MEMS Processes and Materials
- Quality, Reliability, and COO

"The IWLPC was excellent in 2008, spectacular in 2009 and I expect it to be just as good in 2010. We have already opened dialog with four major semiconductor manufacturers and three equipment manufacturers interested in partnering with us from IWLPC. We are seeing an increase in new customers for our technologies even in the first week after the show."
– 2009 EXHIBITOR

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INDUSTRY NEWS

Endicott Honors Employees

At an awards dinner and ceremony held Friday, April 16th at The McKinley in Endicott, N.Y. Endicott Interconnect Technologies, Inc. (EI) honored 36 employees for patent applications filed, U.S. patents issued and trade secrets received in 2009. "I am very proud of these individuals whose bold invention, creativity and technology innovation has contributed to the success of EI, ensuring our technical vitality and allowing us to compete aggressively in the open market," commented James McNamara, President and CEO at EI. "This seventh annual ceremony signifies how firmly and decisively EI's corporate leadership encourages innovation as the corner stone for the future of the company's progression," affirmed Voya Markovich, Senior VP of R&D and CTO at EI. "I am honored to be working with this team of inventors," he continued. EI has 145 filed applications and has been awarded 103 U.S. patents to date, including 25 new patents issued and 7 trade secrets in 2009. [www.endicottinterconnect.com]

Even NASA Gets Duped

In 2009, a NASA probe project was delayed nine months and exceeded its budget by more than 20 percent, partly because of a counterfeit part. According to BrandWatch Technologies, a developer and implementer of brand security and product authentication solutions, the problem extends beyond NASA's dollars and timelines, risking personal safety, diminishing confidence in U.S. aerospace programs, and impacting the businesses of legitimate component manufacturers. "The effort it takes to get astronauts one step further into space is immense, so the fact that counterfeiters have penetrated our space exploration and defense programs is a shock and certainly raises concerns," said Phil Huff, chief executive officer of BrandWatch Technologies. "Unfortunately, globalization has made it more difficult than ever to control the millions of parts and sources within supply chains, including those that support NASA. The only way to truly protect legitimate companies and the integrity of their parts, and enforce NASA's compliance and safety standards is through proactive product authentication." In response to its counterfeit problems, NASA adopted SAE AS5553, an aerospace parts standard issued in 2009. [www.brandwatchtech.com]

Imec Successfully Concludes 2009

At a meeting on April 30, 2010, the imec board announced its results for 2009. Despite the severe economic downturn, they reported that 2009 was a satisfying year. Using EUV lithography, imec claims fabrication of the world's first functional 22nm SRAM cell, an extremely small memory cell representing a huge technical and logistical challenge. They developed a micro-nail chip enabling intimate contact with neurons. The chip can stimulate neurons and read their signals. It will be used in the Neuroelectronics Research Flanders initiative to unravel the human brain. NERF was founded by imec, VIB, and K.U.Leuven and is supported by the Flemish Government. 2009 was also marked by the successful kick-off of imec's solar cell research program, endorsed with collaborations with important players such as Schott Solar, Total, GDF Suez, and Photovoltech.

Said Luc Van den hove, President and CEO at imec, "This is our way to prepare for the future, to tackle the technological and the economical challenges ahead. Because we are convinced that open innovation and global collaborations are the key to progress." [www.imec.be]


Luc Van den hove

IWLPC 2010 Gains Momentum—Three Gold Sponsors

The International Wafer Level Packaging Conference is delighted to announce the 2010 gold sponsors. Gold sponsors have a special relationship with the conference and get their company logos, with links, put on the conference web site front page. The 2010 sponsors are Amkor Technology, Pac Tech USA, and NEXX Systems.

Amkor is one of the world's largest providers of contract semiconductor assembly and test services and a long-time supporter and sponsor of the IWLPC conference.

Pac Tech has also been a sponsor in the past and IWLPC is pleased to have them again. Pac Tech is a provider of advanced wafer bumping, packaging, and solder-ball placement equipment and contract services.

Also a former sponsor, NEXX Systems, Inc. is a semiconductor equipment company specializing in wafer level packaging processing for the semiconductor packaging industry.

IWLPC attracts a large international attendance. If your company is interested in sponsorship or exhibit opportunities please visit www.iwlpc.com or contact Leslee Johns [leslee@smta.org]. The IWLPC is sponsored jointly by the SMTA [www.smta.org] and Chip Scale Review magazine [www.chipscalereview.com]

3D Process Advances

Experts from SEMATECH's 3D interconnect program based at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex outlined new developments in wafer bonding, copper removal, and wafer thinning at the 2010 Materials Research Society (MRS) Spring Meeting on April 5-9 in San Francisco, CA. Process advances aimed at improving 3D performance include:

- A practical approach to copper overburden removal by chemical mechanical polishing (CMP), using high removal rate slurry screening and achieving good planarization

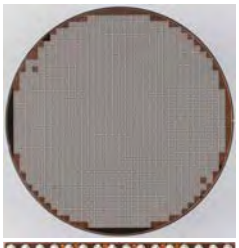
results, with low polish defects, at a rate suitable for emerging 3D TSV copper applications.

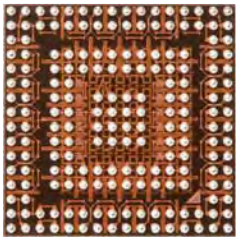
- The process development and associated metrology necessary in thinning bonded 300mm TSV and non-TSV bonded wafers, leaving a defect-free surface which meets the requirements for subsequent processing.
- An array of metrology techniques used in characterizing a manufacturable wafer bond process to deliver a void and dendrite-free bond for handle wafers.

To accelerate progress, the program's engineers have been working jointly with chipmakers, equipment and materials suppliers, and assembly and packaging service companies from around the world on early development challenges, including cost modeling, technology option narrowing, and technology development and benchmarking. [www.sematech.org]

STATS ChipPAC Transitions to 300mm

Claiming to be the first in the semiconductor industry to introduce 300mm embedded Wafer-Level Ball Grid Array (eWLB) wafer manufacturing capabilities, STATS ChipPAC, headquartered in Singapore, recently announced the expansion of its eWLB technology to reconstituted 300mm wafers. By adding capacity through 300mm wafer manufacturing, STATS ChipPAC expects its customers to benefit from the cost and productivity advantages of eWLB technology on the larger 300mm format.





"The 300mm eWLB wafer manufacturing accomplishment is a milestone for the industry and is the result of leveraging the strengths of STATS ChipPAC and its manufacturing partner, Infineon Technologies," said Dr. Han Byung Joon, Executive Vice President and Chief Technology Officer, STATS ChipPAC. The company continues its development work on the eWLB evolution to enable larger package sizes, higher Input/Output (I/O) density, and 3D Package-on-Package (PoP) solutions to address a wider application market. [www.statschippac.com]

Advanced Chip-to-Wafer Bonding Enabling Silicon-in-Package (SiP) Production with Low Cost of Ownership

As geometries get smaller, new approaches hold promise

By Alfred Sigl, Garrett Oakes and Paul Kettner [EV Group, St. Florian/Inn, Austria]
and *Christian Pichler and Christoph Scheiring [Datacon Technology GmbH, Radfeld, Austria]*

The shrinkage and integration of various functionalities into electrical devices such as computers or mobile phones has lead to an ongoing need for shrinkage of the integrated semiconductor units as well. One possibility for manufacturing highly integrated electrical devices is the System-in-Package (SiP) approach where various semiconductor chips with different functionalities are stacked and electrically connected to each other. The shrinkage of features, for example transistor size, die thickness, height of the die stack, and the dimension and shape of interconnects between the dice, affects all aspects of the SiP. Smaller die interconnects can cause difficulties to widely used joint technologies such as solder bumping, because of the small amount of solder involved, to the point that the assembly yields drop and the reliability of the interconnects decrease.

The Advanced Chip-to-Wafer (AC2W) bonding approach is a two-step process for stacking and bonding dice on wafers. All dice are aligned and tacked on the wafer first and, in the second step, these dice are bonded simultaneously and permanently to the wafer. This process allows the use of force while bonding the dice on the wafer. In this way, low solder volume interconnects can be formed at the wafer level with high assembly yield and throughput. The cost of ownership (CoO) combined with the throughput of the AC2W process can be an order of magnitude smaller than for comparable chip-to-wafer bonding processes. While there are some issues concerning die joint shrinkage, AC2W offers a low cost chip-to-wafer bonding process for high volume production.

Introduction

Collapsible solder-bump interconnects are widely used for flip-chip connections. However, as structure size on semiconductor devices decreases to follow Moore's Law, the dimensions of the interconnects also have to shrink. In turn, the solder volume at the individual interconnects must decrease. Amongst other influences, the solder also functions as a compensator for height variations of the substrates and functional layers or variations due to warp and bow. Decreasing the solder volume decreases the ability to compensate for height variation, and only with the application of force during bonding can sufficiently high manufacturing yield be guaranteed.

During the formation of solder interconnects the selected metals diffuse into each other and usually convert to intermetallic compounds (IMC) at the interface. In most solder connections utilized to date, this undesirable effect occurs with a known growth rate that depends on temperature and metallurgy. The thickness of this layer depends on physics and for low solder volume interconnects (**Figure 1**) IMC thickness is nearly that of the joint thickness. Therefore, as the connection size shrinks, the ratio of

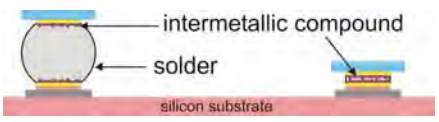


Figure 1. Comparison between C4 solder interconnect and low volume solder interconnect

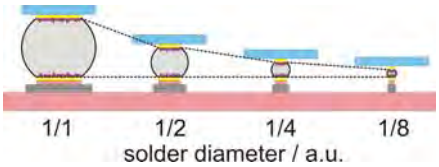


Figure 2. The ratio of IMC to solder increases as interconnect size decreases

IMC to solder rises (**Figure 2**). Furthermore the growth of IMC does not stop after the heat cycle for forming the connection. At room temperature the conversion continues, albeit with a very long time constant, due to its thermodynamic instability. One possible solution is to bring the connection into a thermodynamically stable state, which means converting the metals completely to IMC and using them directly as the material for the interconnection. In this case, the volumes of the metal components are adjusted to each other in such a way that all material can convert to IMC while bonding. This approach is similar to the well-known eutectic bonding. Additionally, the density of the IMC is usually higher than the densities of the parent metal components leading to volume shrinkage while forming the connection. To guarantee a good contact and allow a sufficiently high metal-diffusion rate, application of force is necessary for bonding.

A more sophisticated approach for making small metal interconnects is thermocompression bonding, which is well known from wafer-to-wafer bonding. It is well suited for making very small interconnects with dimensions in the single digit micrometer range. In this approach, force is required during bonding to

overcome the microroughness and bring the two metal surfaces proximal so that the diffusion of the metal atoms can occur to form a metal bond.

Several major semiconductor manufacturers have evaluated or employed these types of interconnect formations for volume production[1-7]. In all approaches for small interconnects, the application of force is necessary to form a proper bond. For the application of force for chip-to-wafer bonding, the sophisticated AC2W bonding process, designed specifically for high volume production, is available.

Advanced Chip-to-Wafer Bonding

The AC2W bonding process is a process flow for chip-to-wafer bonding specifically designed for the application of force while forming the bond at a throughput appropriate for volume production[9]. The concept of separately aligning substrates and then bonding them to each other is well known and widely used for wafer-to-wafer bonding. In the AC2W bonding process the same concept is adapted to chip-to-wafer bonding. AC2W is a two-step process (**Figure 3**). First, all chips are aligned and prebonded to the wafer. Second, all chips are bonded in parallel simultaneously and permanently to the wafer.

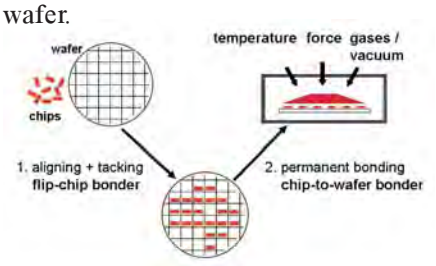


Figure 3. The AC2W process flow

In the first step of the AC2W bonding process the dice are aligned to the wafer and then the alignment is fixed by prebonding the chips to the wafer. Three different methods are commonly available for the prebonding, each having a distinct application:

1) Using a prebonding adhesive[9]: a prebonding adhesive, for example bibenzyl, can be used. This material has the properties that it is a solid below 48° C, a liquid above that temperature and it evaporates without residues in the temperature range of 250 – 280° C. The dice and the adhesive are heated above 53° C for aligning, applying the adhesive, and placing the dice on the wafer. Then the stack is cooled to solidify the adhesive, thus fixing the die. The adhesive completely evaporates during the permanent bonding step.

2) Using a preapplied underfill[10]: preapplied underfill can also be utilized for die-to-substrate prebonding. There are various methods to apply underfill either to the target wafer or to the dice prior to bonding. During prebonding the underfill has to have, either on its own or via special treatment, enough tack to fix the dice to the wafer and secure the alignment. The usage of preapplied underfill for prebonding has a large advantage in that underfill typically has to be applied at stacked substrates. Therefore, it covers two functions simultaneously, saving additional cost.

3) Using ultrasonics[11]: ultrasonic prebonding can be used for metals with low melting points. In this case a fragile connection between the surfaces of the metal pads is formed by ultrasonic energy. This method is preferable for MEMS fabrication because no organic materials are involved. Furthermore, no consumables are used.

All of these methods fix the dice and thereby the alignment of the dice while the populated wafer is transported from a flip-chip bonder to a permanent bonder (**Figure 7**). All methods can be performed at high speed, which means that the flip-chip bonder can operate in a production mode in the range of the highest specified throughput for the equipment. The permanent bonder requires the following features for the chip-to-wafer bonding: (1) a closed chamber for vacuum encapsulation or process gases, (2) a pressure plate and force application system, (3) a point of application of force movement system and (4) a compliant layer. Therefore, it enables the permanent bond process at high temperature (up to 550° C) with application of force and with vacuum (down to $1x10^{-5}$mbar) or process gases.

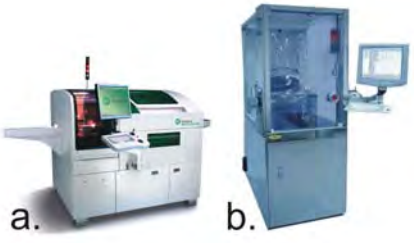


Figure 7. AC2W equipment. Step 1: (a) flip-chip bonder, Step 2: (b) permanent bonder

1) The closed chamber for vacuum encapsulation or process gases allows having a specific controlled atmosphere while the bond is formed. In that way gases or vacuum can be encapsulated in semiconductor devices such as pressure sensors, or bonding-improving gases can by used.

2) The pressure plate allows the application of force simultaneously on all dice on the wafer during the whole process of forming the bond as this is necessary to have a high process yield for small interconnects.

3) The point of application of force movement allows the usage of Known Good Dice (KGDs) only, which is a large cost saving. In KGD bonding, the target wafer is partially populated. Tested chips are only placed on yielding dice on the target wafers. To guarantee the same force on each die, the point of application of force has to be at the center of gravity of the die population (**Figure 4**) and is achieved by the point of force application movement system.

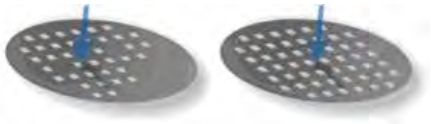


Figure 4. The point of application of force has to be at the center of gravity of the die population

4) The compliant layer compensates for thickness variations of the dice which occur when the dice originate from different source wafers. The variations are usually in the range of tens of micrometers or less. With the compliant layer, yield issues caused by small interconnects can be overcome as shown in **Figure 5**.

While the permanent bonding process force is applied to the dice on the wafer, the stack is heated up to the

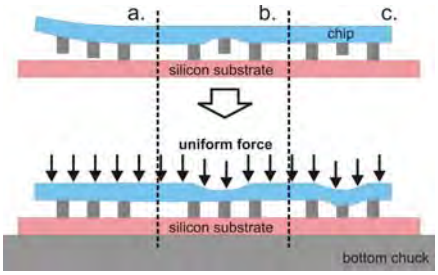


Figure 5. Open contacts can occur by (a) bow or warpage, (b) unevenness of the substrates, (c) height variation of the interconnects (top). These issues can be overcome by uniform application of force on the backside of the die by the usage of a compliant layer while bonding (bottom)

bonding temperature under vacuum or certain process gases and the bond is formed for all dice simultaneously. At this time the prebonding adhesive either evaporates or cures depending on the prebonding method that is used. The bonded stack is then cooled down and can be unloaded from the chamber.

The AC2W bonding concept is a new concept compared to the well-known Controlled Collapse Chip Connection (C4) for flip chip, wafer-to-wafer bonding, and chip-to-wafer bonding by only using a flip-chip bonder. All of these concepts have their advantages, but there are application spaces where the AC2W bonding approach is the best suited and, in terms of cost of ownership, the cheapest process.

Comparison of C4 to AC2W Process

The most popular process for making collapsible interconnections is the Controlled Collapse Chip Connection (C4) process[8]. It mainly consists of four steps (**Figure 6**, top): (1) application of under-bump metallization (UBM), (2) application of solder with ball forming reflow, (3) fluxing and placing the chip on the substrate, and (4) assembly reflow. The process flow of AC2W is quite similar to C4 (**Figure 6**, bottom): (1) application of under-bump metallization, (2) application of solder without ball forming reflow, (3) aligning and prebonding on substrate by prebonding adhesive, (4) assembly reflow with force.

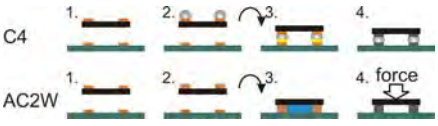


Figure 6. C4 and AC2W (for Cu-Sn-Cu eutectic bond) process flow comparison

In principle the concept of the two process flows are the same. In both cases, the chips are fixed by an adhesive for the last step (flux for C4, prebonding adhesive for AC2W). The difference is when and how the alignment is performed. In the C4 process, the chips undergo a self-alignment when the solder melts during the final assembly reflow. At that time, the surface tension of the solder pulls the chips to the correct position. This concept only works when the amount of solder is large enough so that the droplet of solder has a high enough surface tension to move the chip. For small solder volume interconnects, the floating resistance is too high, and this concept fails since the process yield drops rapidly due to open contacts.

In the AC2W process, the chip-to-wafer alignment is already completed during the placement of the chip on the wafer and secured by the prebonding adhesive and by the application of force during the final bonding step. The alignment is completely done by the flip-chip bonder and not dependant on the properties of the interconnection material. Therefore, higher accuracies with smaller interconnects can be achieved as compared to the C4 process, and open contacts are avoided by the application of force during bonding. Therefore the C4 process is well suited and offers high throughput for larger size solder interconnects but for smaller size solder interconnects the AC2W process is favored.

Comparison of AC2W to Wafer-to-Wafer Bonding Process

Wafer-to-wafer (W2W) bonding is a well known and widely used process approach for connecting and stacking devices at the wafer level. The main advantage of W2W bonding is the very high achievable alignment accuracy in the submicrometer range with high throughput.

For flip-chip bonders, the throughput depends strongly on the targeted alignment accuracy. Therefore, the throughput in the first step of the AC2W drops when accuracies below two micrometers are targeted while for W2W it stays nearly constant for all required accuracies. In the second step of the AC2W bonding, high throughput is achievable since it is very comparable to W2W bonding as there are multiple dice bonded to the target wafer at once. Also the process time and process recipe are quite similar.

In contrast to W2W, in AC2W bonding only known good dice are used. This offers a large cost savings. When stacking multiple dice, the W2W yield can decrease dramatically (**Table 1**). Here, a hypothetical yield of 90 % of the devices on the processed wafers is taken into account. It is assumed that all stacked wafers have the same yield. The yields for all other yield detractors, such as bonding, testing, and chip yield, are assumed to be a 100 %, since they are usually very high. For W2W the yield decreases exponentially while for AC2W it stays constant at the starting level of 90 %.

# of stacked dies	W2W yield/ %	AC2W yield/%
0	90	90
1	81	90
2	73	90
3	66	90
4	59	90
5	53	90
6	48	90
7	43	90
8	39	90

Table 1. Yield advantage of AC2W over W2W

When dice with different sizes have to be stacked on each other, additional losses occur in the W2W approach because the patterns on the different wafers have to match regardless of the chip size on the wafer. For example, assume that two dice are to be stacked and one die is a quarter of the size of the other, and the two source wafers cost the same to process. When stacking the devices with the W2W approach, three-quarters of one wafer has to be without devices since the dice on the both wafers have to be at a

certain position to mate with each other while bonding. Therefore, on one wafer, only one-quarter of the wafer area is covered with chips. When looking at the process cost, the wafers cost the same, so each are 50 % of total costs. In the W2W process, 75% of the wafer area from one wafer is unused and possible dice are lost that would be used in the AC2W process. In this example the costs for using the W2W process as compared to the AC2W process are 37% higher caused by the choice of bonding process.

The W2W approach is the method of choice for applications where alignment accuracy in the submicrometer range is necessary. AC2W bonding offers an equivalent throughput simultaneously with higher yield and is therefore cheaper for stacking multiple or different sized dice.

Comparison of Flip-Chip Bonder Only to AC2W Process

The flip-chip bonder only process flow does both the alignment and the bonding steps directly after each other for each individual die so all the dice are bonded in serial to the wafer. Die interconnects (eutectic bond, thermocompression bond) form by diffusion processes that need a certain amount of time, usually in the range of tens of seconds. In the flip-chip bonder only process, this time is needed to bond each and every individual die and therefore lowers the throughput dramatically. In contrast, for the first step of the AC2W process, the flip-chip bonder can operate with very high throughput. The time needed for diffusion contributes to the second step of the AC2W process, but since all dice are bonded in parallel the overall time contribution, in the range of tens of seconds for all the dice, is negligible.

For better understanding, here is an example. Assume that 2,641 chips with a size of 5x5mm^2 are bonded to a 300mm wafer. The type of interconnection is CuSnAg which usually requires 20 seconds for bonding. The alignment time of a flip chip is about 0.5 seconds. This means that in the flip-chip bonder only process each individual die needs (20 seconds + 0.5 seconds =) 20.5 seconds to be bonded to the wafer which results in a throughput of about 175 dice per hour or 0.066 wafers per hour. In the AC2W process, the throughput of the two steps has to be evaluated separately. During the first AC2W step, the throughput is determined by the flip-chip bonder alignment and placement time (0.5 seconds) and therefore about 7,200 dice per hour or 2.73 wafers per hour can be processed. The throughput of the second step is mainly determined by equipment restrictions and is in the range of about 20 minutes per wafer or three wafers per hour. The 20 seconds diffusion time to form the interconnection, contributed at the second bonding step, has therefore no negative effect on throughput of the AC2W process.

Besides the throughput, there are several other variables that affect the cost of ownership of the AC2W process, such as die size, wafer size, bonding process, and alignment accuracy. For the given example the cost of ownership (CoO) was calculated and it shows a cost advantage of one order of magnitude (**Figure 8**).

Comparison of Capillary to Preapplied Underfill Usage

For nearly every manufactured die stack there is a filler material, called the underfill, applied between a die and the target

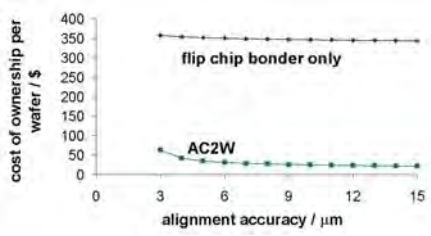


Figure 8. Cost of Ownership comparison of flip-chip bonder only and AC2W bonding processes

substrate for mechanical stabilization of the electrical interconnection. The underfill is required to achieve a sufficiently long lifetime of the device, as the device has to withstand detractors to longevity such as thermal cycles, humidity, and corrosion.

Available underfill materials can be divided into two main categories: capillary underfill and preapplied underfill. Capillary underfill is the most widely used and a well-known technology in various fields of stacking applications, like die to wafer, die to lead frame, and many other packing methods. The underfill is applied to the die stack after bonding by needle or droplet dispensing. The underfill may be applied to the package at one edge, a few edges, or in more complex patterns. The liquid underfill material then wicks into the gap between the dice due to the capillary effect, which means it maximizes the wetted area to minimize its energy. Additionally, there are some ceramic filler particles with a diameter down in the single digit micrometer range mixed into the polymer base material to lower the coefficient of thermal expansion (CTE) to a value near the CTE of the semiconductor material. The filling of the die gap with capillary underfill is a separate process that occurs after the stacking. Therefore it can be used in all die-to-substrate bonding approaches and is state of the art of die stacking with the C4 process. Usage of capillary underfill for die gaps below thirty micrometers in high volume production is economically unattractive because the filling time rises with decreasing gap height and a void-free filling cannot be guaranteed.

The usage of preapplied underfill is an alternative method to apply underfill material to these kinds of small die gaps. Therefore this underfill technique allows for smaller overall stack height with a cost structure appropriate for high volume production. As the name suggests, preapplied underfill is applied before the bonding of the dice either on the die or onto the target substrate. It may be a liquid, paste, or a foil depending on the supplier and application. For solder interconnects the preapplied underfill has to have some special properties:

1) The preapplied underfill should allow prebonding of the die to the target substrate. This can be by an inherent level of tack or via a bistage property, which means that the viscosity is lowered and thereby the tackiness is increased for prebonding by heat.

2) The preapplied underfill has to allow for void-free prebonding and permanent bonding which means that it should not demonstrate any outgasing or shrinkage during heating or final curing.

3) The preapplied underfill has to allow for proper solder bond formation. Because the bumps are usually not in full contact after prebonding it must be possible to squeeze out the underfill between the bumps while permanent bonding takes place. Usually underfill material is a bistage material. It is very stringy at room temperature. Upon heating, the viscosity decreases. This allows the underfill to squeeze out. Above a certain temperature the material migrates to its final stage and it cures into a solid material.

4) The preapplied underfill has to have fluxing properties to guarantee sufficient wetting of the solder to the bumps. These fluxing components should not influence the mechanical or electrical properties of the final package since they cannot be removed from the die stack.

5) The preapplied underfill has to cure without shrinking since that would lead to stress on the dice or voids in the stack. The underfill is usually cured by heat.

6) The preapplied underfill should have a temperature behavior of its bistage properties which fits to the needed final metal bond temperature and the temperature gradient.

These are very difficult restrictions which demand very special materials for this application. After applying the preapplied underfill, the die can be bonded to the target substrate by C4, flip-chip bonder only, or by the AC2W process. For the C4 and AC2W process, a placing or prebonding of the die to the target substrate is necessary (**Figure 6**, step 3). For making the permanent metal connection the prebonded die stack has to be heated to the bonding temperature. This temperature rise results in a thermal expansion or a viscosity reduction of the underfill material. Decreasing the viscosity of the underfill can lead to a shape change caused by the surface tension. These effects can lead to a lifting up or shifting of the die in relation to the target substrate. Again, this can cause open contacts or misalignment. Therefore, to avoid these effects, preapplied underfill can only be used for a sufficiently high manufacturing yield with the application of force while permanent bonding. The preapplied underfill can either be fully cured in the permanent bonder by tempering for a longer period of time or at an elevated temperature. It can also be final cured in an external process.

Conclusions

For die-to-wafer interconnects, the application of force is necessary while forming the connection. The advanced chip-to-wafer bonding process is a sophisticated approach with the application of force while bonding. Compared to other approaches like flip-chip bonder only or wafer-to-wafer bonding, it offers a much higher yield and throughput and therefore a lower cost of ownership. Additionally, preapplied underfill, the gap-filling material of choice for high-volume production of smaller devices, can only be economically used with application of force while bonding. These are the reasons why AC2W is best suited for high volume chip-to-wafer stacking production.

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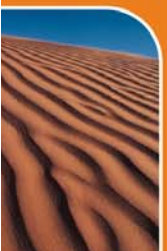

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New Realities for TSV Processing

CoO: Variation on Theme

By Steve Lerner, CEO [Alchimer, Massy, France]

3-D integration and More-than-Moore are popular topics in the semiconductor industry, with high expectations for eventual wide use of 3D-IC technologies. But the pace and scale of adoption is largely dependent on long-term cost of ownership (CoO). This article presents an alternate perspective from those through-silicon-via (TSV) consortia oriented around adaptation of front-end processing, examining all aspects from design to factory-floor deployment.

What is a TSV? A real reference for cost

It's important to keep in mind that TSVs are not sensitive transistors with complex switching characteristics. They are, in fact, merely dumb wires, and should be treated as such. So in the Pareto chart of TSV-manufacturing concerns, the top three items would be cost, cost, and cost (assuming reliability and process control are in place for the given application). Although each application will have different priorities (parasitics, mechanical and thermal compliance, etc.), at the end of the day we are still dealing with a wire.

In the semiconductor industry, most experience with dumb wires has been in the back end, where wire bonds, package pins, and bumps have gone through an extraordinary evolution of reliability improvement and cost reduction. There was a time when wire-bond yield and reliability were in the 97% range. Now we talk of parts per million (ppm). Outsourced assembly and test services (OSATs) were once challenged by a package price of 1 cent per pin. Now they deliver products at a small fraction of a penny per I/O. 10 years ago, bumped 200mm wafers cost nearly $500. Today, 300mm wafers go for less than $50 with redistribution layer (RDL).

TSVs are on a similar trajectory. In fact, an interposer wafer has much more in common with a bumped RDL wafer or a printed circuit board than it does with a typical CMOS wafer. Therefore, the infrastructure to process such an interconnect vehicle can and should be radically different from CMOS infrastructure. It is commendable that some front-end consortia have modeled TSV wafer processing at below $200, but if TSVs are to realize their true potential, initial cost must be less than $50 — with a target of $25 within the next five years. Given the typical five-year depreciation of those front-end machines, it is no wonder that sticker shock is widespread, especially among companies that are not the most dominant and integrated semiconductor players. But there is hope.

It starts with design

Unfortunately, designers have been conspicuously absent from many discussions regarding the formation of the TSV infrastructure, and run the risk of missing out on the greatest potential benefits of 3-D integration. The most strategic question from the design perspective is about aspect ratio. The ability to decrease TSV diameter has huge implications for how much die space is available for working circuitry, and for the overall cost impact of TSV adoption.

Parameter	Value	Unit	Notes
Thickness	50 - 500	nm	
Thickness uniformity	5	%	3 σ
Adhesion	All layers pass 16-square scribe tape test		
Via diameter	1 - 200	µm	
Via aspect ratio	2:1 - 20:1		
Step coverage	Up to 90%		bottom/field thickness

Table 1. Common film properties for eG/eC films

And this is where the necessity to reconsider adoption of dry, vacuum-based front-end processes becomes most apparent. The most notable design rule differences between wet and dry TSV film deposition are in via aspect ratio. Most front-end tooling groups currently model around a 6:1 aspect ratio for cost purposes, but state capability up to 10:1. Why such a modest starting point? Simply because most dry tools — with the exception of expensive low-throughput techniques such as ALD — simply can't deliver the aspect ratios most beneficial to designers.

Current wet processing can easily deliver 20:1 aspect ratio and higher at a significantly reduced cost. **Figure 1** demonstrates the impact of TSV aspect ratio on silicon real estate.[1] TSV aspect ratios of more than 10:1 can cut the area needed for vias to <1% of the wafer surface, and keep costs under $100/wafer. This model assumes 10 x 10mm dice on a 300mm wafer, with 10,000 TSVs of 50nm depth and total wafer cost of $6,359.

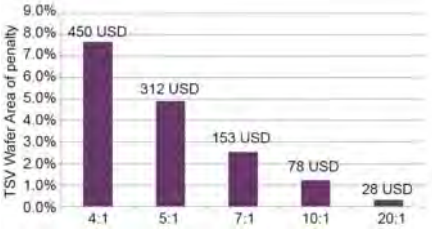

Figure 1. TSV wafer area penalty, as a function of aspect ratio, with calculated cost/wafer

Further, designers have been bombarded with dry film properties as the only electrical parameters available, when in fact better-performing materials can be attained through wet processing. **Table 1** illustrates common deposition properties and process capabilities associated with a novel family of

(continued on Page 33)

High Thermal Conductivity Underfills—How Much Do They Help?

Some, but underfills are only part of the story

By Zane Johnson and Nathan Schneck [Center for Nanoscale Science and Engineering, North Dakota State University]

A half century has passed since underfill was first applied to flip-chip ICs. In that time, much effort has been directed toward optimizing thermo-mechanical properties such as viscosity, stiffness, thermal expansion, and adhesion in order to make the underfill process as cheap, effective, and factory-friendly as possible. In recent years, attention has turned to increasing the thermal conductivity as a means of reducing IC temperatures in high-power devices.

Underfills

Most commercially-available underfills are composed of an organic resin (typically epoxy or silicone) to which filler particles (often alumina, silica, or aluminum) are added to increase stiffness and reduce thermal expansion. The resin alone has a low thermal conductivity (0.1-0.3 W/mK), but the addition of high-conductivity particles can easily double that value, and through careful control of particle size and shape raise it to 1.5W/mK or more. Employing more exotic fillers made from carbon fiber, boron nitride, or various nanoparticles and nanotubes can result in composite conductivities as high as 30W/mK, though manufacturability can be a concern. This one to two orders of magnitude improvement in thermal conductivity is impressive, but the underfill is only one factor in an overall thermal management scheme. So, to place these material developments in perspective, it is necessary to examine their impact at the electronic package or module level.

The study

The range of package and module designs in use today varies widely. For an initial study on the benefit of high-conductivity underfill, a flip-chip Silicon-on-Sapphire (SoS) device was chosen. SoS is a member of the silicon-on-insulator family of CMOS technologies, and due to sapphire's intrinsic radiation resistance shows distinct benefits in aerospace and satellite applications. To simulate the thermal performance of the SoS flip-chip, a Finite-Element (FE) model was constructed. The configuration is that of a 2 X 2mm die mounted directly to a 25 X 25mm PWB in the chip-on-board style. The die has twenty eutectic tin-lead solder bumps spaced equally around its periphery on a 333µm pitch. Void-free underfill is used to bridge the 55µm gap between the die face and the PWB. No heat sink or heat spreading feature is present. The meshed FE model is shown in **Figure 1**.

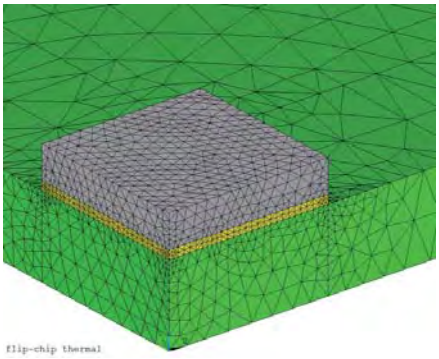

Figure 1. FE model of a chip-on-board configuration. The IC is shown in gray, the underfill in yellow, and the PWB in green. The full extent of the PWB is not shown and the flip-chip solder joints are hidden from view. Quarter-symmetry is assumed to reduce the size of the model

The FE model dissipates a steady and uniform 100mW at the die-underfill interface, and natural convection and radiation boundary conditions are applied to the die and PWB surfaces to represent heat loss to a still air environment at 298K (25°C). As is typical with very small devices and ICs, almost all of the power generated in the device flows downward into the PWB where it spreads laterally and is eventually released to the environment. As a consequence, the composite conductivity of the PWB is a critical factor in the thermal performance of a chip-on-board IC. Peak temperature occurs at the center of the die, with PWB temperatures dropping with increasing distance from the IC. Temperature contours from a typical simulation are shown in **Figure 2**.

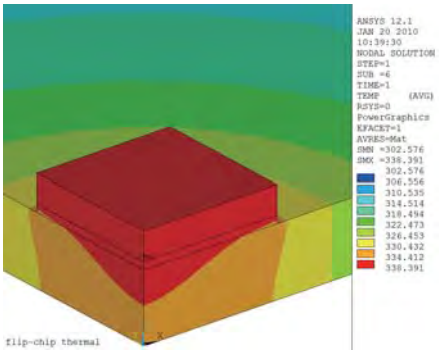

Figure 2. Typical temperature contours resulting from a 100mW power dissipation

To gauge the effectiveness of enhanced-conductivity underfill, the conductivities of the underfill and the PWB were varied over a realistic range of values. A full-factorial study was performed with underfill conductivity values that ranged from 0.027W/mK (representing air, or no underfill) to 2.0W/mK (a highly filled resin). The PWB conductivity values were varied from 0.2W/mK to 30W/mK. PWB construction varies widely, but the range chosen captures many board and module designs of practical interest. Forty-nine FE simulations were performed. The simulation results are

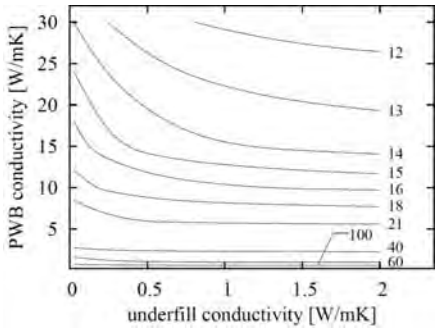

Figure 3. Die temperature rise over ambient as a function of underfill and PWB thermal conductivity. Contour values are in °C

presented as maximum die temperature rise over ambient. The results are summarized as contours in a PWB/underfill conductivity plot (**Figure 3**).

Analysis

Note that the contours and contour labels are not evenly spaced. Overall, the contour pattern of nearly parallel lines shows that increasing PWB conductivity yields a much greater benefit (lower die temperature) than increasing underfill conductivity. For example, for a PWB conductivity of 15W/mK and an underfill conductivity of 0.2W/mK, the model predicts a die temperature rise of 15.4°C. Increasing the underfill conductivity to 2.0W/mK yields a die temperature rise of 13.6°C, an improvement of only 1.8 degrees Celsius (12%) at this 100mW power level.

Notably, die temperatures rise sharply when PWB conductivity drops below 5W/mK, but in practice few PWB designs exhibit composite conductivities lower than that. The contours show that for most PWBs of interest, little benefit is seen by increasing the underfill conductivity beyond 0.5W/mK. This contour pattern may change, perhaps significantly, for other chip-on-board designs or other packaging technologies.

Conclusions

For this chip-on-board configuration, only minimal thermal benefit was seen for underfill conductivity values beyond 0.5W/mK. This study does illustrate the importance of PWB conductivity in IC thermal management, and that a designer would be wise to incorporate numerous thermal vias into IC substrate and module designs. New "high conductivity" underfills do not change this basic design imperative.

Acknowledgement and disclaimer

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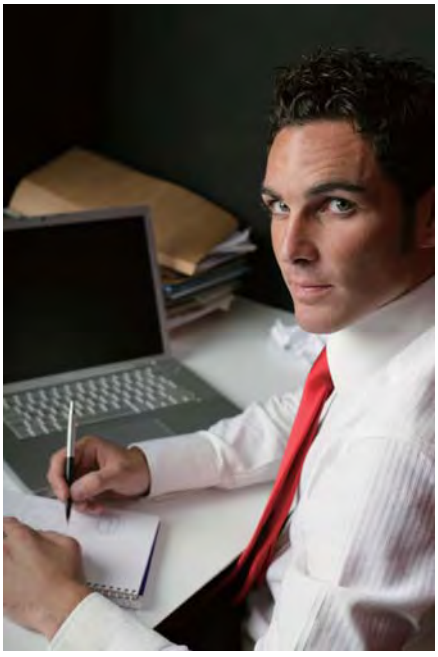
When to Call In the Cavalry—or at Least Get a Faster Horse

By Liz Richards [Richards & Lord]

If you are a smaller OEM, EMS, or supplier that is running lean, how much is too much involvement in back-office administration? Would you be better off spending your time exclusively on growing your business through sales and engineering tasks per se, leaving the back office to someone else? If you have all the time in the world and love what you're doing, I say have at it, but that is not the typical scenario. Usually CEOs and Engineering Management wind up wearing many hats. So how do you know when that last hat was one too many and it's time to bring in the cavalry: hiring or outsourcing?

The Signs Are There

Let's define back office as any of the approximately 80% of the business tasks that do not impact on the customer's client experience with your company. Those front-office tasks that do impact the customer, such as sales, follow up, and customer service should remain firmly in your hands as your core business, and not be outsourced. My rule of thumb is that if you can make more money doing your core business than you would lose by paying someone else to do the data entry, accounting, or whatever else from the back office, then pay someone else to do it. You still come out ahead, and if you are losing money because you are not only neglecting your core, but doing the "whatever" poorly, then definitely hire someone else to do it.



The CEO of any small business is what Elizabeth Marasco of Bookkeepers Plus calls a causative being, a hands-on person whose ability to make things happen is one of his or her most valuable assets. But eventually, as the successful executive grows the business, there is just too much administrative work for one person, or even several, to handle. Soon that typical 80% administrative end of the business begins to eat into the remaining 20% needed to continue generating the revenue. When that happens, it becomes critical decision time. Let us assume you have seen the signs and decided that you are at the point where you need administrative help. What are your options as a small-to-medium sized business? There are three main ones.

Option 1—the Employee

The first would be to hire employees either part or full time. But then, ironically, you take even more back-office responsibility and cost. You also find that for every employee hired, you will be robbed of part of your own dedicated time as you train, mentor, and answer questions. If you have built up enough reserves to take on this additional cost and time and feel it will help your company grow, it may well be the way to go, and you will have hired people to both handle the tasks and grow with your company. But not everyone has that option.

What if you're not at the point where you have any reserves or any extra time to train and mentor? It's a conundrum because you still have to free yourself to bring in more revenue. What now? Perhaps a skilled virtual assistant or other expert could help.

Option 2—the Virtual Assistant

Enter the next player, the virtual assistant. What exactly is a virtual assistant (VA)? According to Anne Wanchic, a VA based in Florida who writes about the subject online, she/he is someone you work with but may never meet because they accomplish the assigned tasks from their offices, often in their home, and email, fax, or in some other way delivers the results to you. The VA may visit with you through virtual meeting sites such as Go-To-Meeting or on Skype, but as an independent contractor they set up and maintain their own office, pay their own insurance, and pay and file their own taxes. Note that you will, however, need to keep track of how much you spend on an independent contractor. If it is over one thousand dollars in a calendar year, you will need to issue them a Form 1099. They use that to declare income and pay taxes.

Wanchic feels your business needs might be handled by a VA in less time than by a part-time employee, since a good VA may be able to take as much as thirty hours per week and turn it into only thirty hours per month. Many VAs have years of executive administrative

experience from the brick and mortar world, are already skilled in multi-tasking, and take less time to produce high quality work. VAs usually work on retainer for ten to thirty hours per month and are your best bet versus a part-time employee if the amount and type of tasks you delegate is consistent and the cost is less than a part-time employee. A good resource to find a VA with the right skill set for your needs is to visit the International Virtual Assistants Association's site www.ivaa.org or simply do a search for Virtual Assistants.

Option 3 – Full-Service Partner

If you like the idea of a company which handles all your back office needs, then a full-service partner is for you. This is the option of choice for many small companies that simply do not have the time or the background to figure out why their computer went down when they are on a deadline. They just want it fixed. They find it very desirable to have one point of contact to provide their internet, phone service, host their website, and do their accounting.

I spoke with Pete Calderaro, V.P. of Business Development for INT, a company that takes care of many back-office needs. "The thing is, once you see how much time it gives you to succeed at what you really love doing, it's hard to go back to the old way of doing everything yourself," he said. He cited the example of one company who was spending five hours per day on lengthy spreadsheets. INT looked at the end result that the company was aiming for and developed a template for them that included calculation formulas. With the new formulas in place, those five hours spent per day dropped to forty-five minutes. "Utilizing our experienced people makes all the difference to a small company," Calderaro concluded.

For a brand new startup, a full-service partner can arrange to lease you office furniture and computers so you need not invest in that during your critical first year. For a lot of busy people, that's perfect.

How Do You Select a Service Provider?

Let's assume that you are convinced that outsourcing is for you. How do you protect yourself, and what are the basic steps you need to take? Figure out what you want to outsource. Good candidates are data entry, blog and website maintenance, accounting, payroll, secretarial, and research reports. Categorize them as one-off or ongoing tasks, and estimate how many hours you think each will entail. Then, interview both Virtual Assistants and Full Service Agencies to see which fits you better. Be sure to include the following in your interview process:

- Availability — do you need them to work the same hours as you do, for example?
- Resumé —ask about their experience, get references, and check them.
- Obtain samples of their work
- Security — (sometimes the bigger firms have the advantage here) specifically:
  - Do they permanently delete your data, post task?
  - Do they back up data, and how often? Do they store it securely offsite?
  - Do they have a secure facility? (especially applicable for any offshore outsourcing)
- Non-disclosure agreements should be signed by any VA or firm, and should also be signed by any employees they may have.
- Make sure that payroll services also include filing payroll taxes and making sure employees get end of year forms, etc.
- Ensure you communicate well with each other, or you will be spending too much valuable time explaining and reinforcing.
- Clarify terms — they get paid for performance, not for effort. If it requires outside labor to complete the agreed-upon task, or more hours than they anticipated, that is their responsibility, not yours.
- Clarify type of agreement/payment, for example per project or per hour. Depending on the type of work, the rates could be anywhere from ten to fifteen dollars per hour to over eighty dollars per hour. It all depends on skill level, specialist designation, and various other factors. Be sure to get several quotes for comparison. And remember, the higher fee of a specialist who can do something in an hour may be no more expensive than explaining the task to someone who then takes three hours to do it.
- Document the terms in a simple contract: the provider may even have a standard one they use. If not, you can find templates for one online, but do have one, and make sure it says what you want it to say. This is a pure business transaction.

So there you have a brief overview of the various ways to decrease your frustration and increase your revenue. There's a faster horse out there. Just remember to get out the legal pad, figure out what you need and for about how many hours, pick what works best for you, and tend to the details that clarify the agreement. You might even get the fun back into your day and some extra money on your bottom line.

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Aceris, Inc. (Acquired byTopcon in JP) 19501 Clark Graham, Ste. 300 Montreal, Quebec, Canada H9X 3T1 Tel: +1-514-695-0112 www.aceris-3d.ca	2D, 3D PR MP - 300 mm WFR, PKG		
Advanced Metrology Systems 12 Michigan Drive Natick, MA 01760 Tel: +1-866-367-8334 www.advancedmetrologysystems.com	3D PR MP - 300 mm WFR		
AkroMetrix LLC 2700 NE Epressway, Bldg. B, Ste. 500 Atlanta, GA 30345 Tel: +1-404-486-0880 www.akrometrix.com	3D (TherMoire) PR MP - 600+ mm WFR, PKG, SUB, PCB		
ASC International Inc. 1799 County Road 90, Suite 9 Maple Plain, MN 55359 Tel: +1-763-478-6200 www.ascinternational.com	3D PR, NP MP - 450+ mm SDP, SUB, PCB		
Camtek Ltd. P.O. Box 544 Migdal Haemek, Israel 23150 Tel: +972-4-604-8100 www.camtek.co.il	2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB		
Creative Electron, Inc. 310 Via Vera Cruz, Suite 107 San Marcos, CA 92078 Tel +1-760-752-1192 www.creativeelectron.com		2D NP MP - 300+ mm PKG, SUB, PCB	
CyberOptics Corporation 5900 Golden Hills Drive Minneapolis, MN 55416 Tel: +1-763-542-5000 www.cyberoptics.com	3D PR MP - 450+ mm SDP, SUB, PCB		
Dage Precision Ind, (Nordson) 48065 Fremont Blvd. Fremont, CA 94538 Tel: +1-510-683-3930 www.dage-group.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Digiray Corporation 317 Hartford Road Danville, CA 94526 Tel: +1-925-838-1510 www.digiray.com		3D NP MP - 300+ mm PKG, SUB, PCB	
EV Group Europe & Asia/Pacific GmbH DI Erich Thallner Strasse 1 St. Florian am Inn A-4782, Austria Tel: +43-771-253110 www.evgroup.com	(X,Y,Z) - CM PR, NP MP - 300 mm WFR (BONDED)		

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FocalSpot Inc. 9915 Businesspark Avenue, Ste. A San Diego, CA 92131 Tel: +1-858-536-5050 www.focalspot.com	2D PR MP - 480+ mm PKG, SUB, PCB	2D, 3D PR, NP MP - 500+ mm PKG, SUB, PCB	
GE Inspection Technologies 50 Industrial Park Road Lewistown, PA 17044 Tel: +1-866-243-2638 www.gesensinginspection.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Glenbrook Technologies, Inc. 11 Emery Avenue Randolph, NJ 07869 Tel +1-973-361-8866 www.glenbrooktech.com		2D NP MP - 600+ mm PKG, SUB, PCB	
Göpel Electronic GmbH Göschwitzer Strasse 58/60 Jena D-07745, Germany Tel: +49-0-36-416896-0 www.goepel.com	3D PR MP - CM PKG, SUB, PCB	2D PR MP - CM PKG, SUB, PCB	
Hitachi Engineering & Services Co., Ltd. 3-2-2, Saiwai-cho, Hitachi-shi Ibaraki 317-0073, Japan Tel: +81-294-22-7111 www.hitachi-hes.com			2D, 3D PR, NP MP - 300+ mm WFR, PKG, SUB, PCB
Hyphenated Systems LLC 1826 Rollins Road Burlingame, CA 94010 Tel: +1-650-651-3000 www.hyphenated-systems.com	3D NP MP - 300 mm WFR, Other		
ICOS Vision (acquired by KLA Tencor) One Technology Drive Milpitas, CA 95035 USA 1-408-875-3000 www.icos.be	2D, 3D PR, NP MP - CM PKG		
Jordan Valley Semiconductors Zone 6, Ramat Gavriel Industrial Zone Migdal Haemek, Israel 23100 Tel: +972-4-654-3666 www.jvsemi.com	2D, 3D PR MP 300+ mm WFR, PKG		
Lloyd Doyle Ltd. Molesey Road, Walton on Thames Surrey KT12 3PI, England Tel: +44-1932-245000 www.lloyd-doyle.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Machvision 3F, No 15, Industry East Road, IX Hsinchu Science Park Hsinchu, 30077, Taiwan Tel: +866-3-563-8599 www.machvision.com.tw	2D, 3D PR, NP MP - 600+ mm SUB, PCB		

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Machine Vision Products Inc. 5940 Darwin Court Carlsbad, CA 92008 Tel: +1-760-438-1138 www.visionpro.com	3D PR MP - 600+ mm PKG, SDP, SUB, PCB		
MIRTEC Corporation 103-803 SK Ventium Bldg 522 Dangjeong-Dong, Gunpo Kyunggi-Do, 435-776 Korea Tel: +82-31-202-5999 www.mirtec.com	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB		
Nikon Metrology, NV Geldenaaksebaan 329 3001 Leuven, Belgium Tel +32-16-74-0100 www.nikonmetrology.com	2D, 3D PR, NP MP - 600+ mm WFR, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
North Star Imaging, Inc. 19875 S. Diamond Lake Road # 10 Rogers, Minnesota 55374 Tel +1-763-463-5650 www.4nsi.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Panasonic Factory Solutions Company of America 909 Asbury Drive Buffalo Grove, IL 60089 Tel: +1-847-495-6100 www.panasonicfa.com	CM CM CM CM		
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Rudolph Technologies Inc. One Ruldolph Road Flanders, NJ 07836 Tel: +1-952-820-0080 www.rudolphtech.com	3D PR MP 300 mm WFR		
ScanCAD International 12779 West Belleview Avenue Littleton, CO 80127 Tel: +1-303-697-8888 www.scancad.com	2D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB		
Sonix Inc. 8700 Morrissette Drive Springfield, VA 22152 Tel: +1-703-440-0222 www.sonix.com			2D, 3D PR, NP MP - 300+ mm WFR, PKG, SUB, PCB
Sonoscan Inc. 2149 E. Pratt Blvd. Elk Grove Village, IL 60007 Tel: +1-847-437-6400 www.sonoscan.com			2D, 3D PR, NP MP - 600 mm WFR, PKG, SUB, PCB
SUSS MicroTec Inc. 228 Suss Drive Waterbury Center, VT 05677 Tel: +1-802-244-5181 www.suss.com	(X,Y,Z) - CM PR, NP MP - 300 mm WFR (BONDED)		

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Teradyne, Assembly Test Division 700 Riverpark Drive North Reading, MA 01864 Tel: +1-978-370-2700 www.teradyne.com/atd		2D, 3D PR, NP MP - 450+ mm PKG, SUB, PCB	
Test Research 7F No 45 Dexing W Road, Shilin District Taipei City 11158 Taiwan Tel: +886-2-2832-8918 www.tri.com.tw	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
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VJ Electronix Inc. 234 Taylor Street Littleton, MA 01460 Tel: +1-978-486-4777 www.vjt.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
Xradia Inc. 5052 Commercial Circle Concord, CA 94520 Tel: +1-925-288-1228 www.xradia.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
YESTech (Nordson) 1317 Calle Avanzado San Clemente, CA 92673 Tel: +1-949-361-2714 www.yestechinc.com	2D, 3D PR, NP MP - 600+ mm SDP, PKG, SUB, PCB	2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
YXLON Int'l Inc. (COMET Group) 3400 Gilchrest Road Akron, OH 44260 Tel: +1-330-798-4800 www.yxlon.com		2D, 3D PR, NP MP - 600+ mm PKG, SUB, PCB	
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Improving CMOS Camera Module Manufacturing Costs in Back End Of Line (BEOL) Environments

Automated Optical Inspection (AOI) provides yield enhancement and cost savings

By David Richard [Vi Technology, Saint-Egrève, France]

New packaging technologies feed the buzz and have never been as promising as in the last few months. The latest technologies, for example Back-Side Illuminated (BSI) sensors; Wafer-Level Cameras (WLC); new advances in packaging, assembly and test; and new techniques such as 3D TSV interconnects, are already in use in camera module manufacturing processes. In parallel, high-end lens module components such as auto-focus and MEMS-based lenses are now being introduced to increase the final product feature set and value. The assembly of the complete module (including the lens) at the wafer level still only represents a minor part of the production of CMOS camera modules today. While this is bound to become a mainstream assembly process in the next couple of years, most of the market still relies on the traditional assembly of the sensor and lens modules in BEOL environments. At the same time this assembly process becomes even more critical since the components are more sophisticated and more expensive. The latest lens modules now include, for instance, auto-focus functionality and high-end sensors (5, 8, and 12 megapixels), the attachment of which also drives up the module cost. Both of these components can cost up to a few dollars each.

Figure 1. Foreign materials on CMOS Image sensors

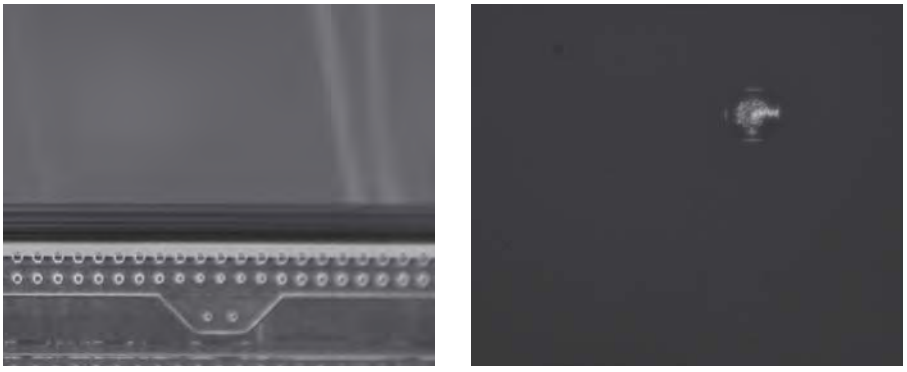


Figure 2. Striation and stain defects

BEOL gaining attention

As a consequence we can see a paradigm shift, with BEOL gaining more and more attention in the camera module assembly market until all or most of the production for wafer-level cameras is made in front-end mode. Conventional front-end scaling is no longer the only way to improve device performance. BEOL packaging technology plays a greater role in improving system-level performance since this technology is not easy to apply to complex lenses. As manufacturers continue to struggle with efficiency to reduce costs and be more attractive in this low-cost high-volume market, some new inspection processes must be implemented in this environment. This will ensure only know-good sensors are assembled to increase the yield and reach the desired cost efficiency. BEOL environments are not as clean and automated as Front End Of Line (FEOL). Clean rooms are usually "only" class 1000 to 10000 which implies a higher level of possible contamination. This is not much of a problem for molded components like BGA but can become a killer for naked CMOS sensors. The assembly of CMOS sensors is also usually carried out on diced products placed onto supports like stiffeners or boards. Those can be used either on in-line processes where the assembly process is continuous from die placement to lens attach and test, or on off-line process islands. In the second case, the units are carried from one island to the next in magazines or boxes which can lead to additional accidental contamination.

Camera modules defects

The most common defects found in BEOL environments are Foreign

Materials (FM) (**Figure 1**). They can be linked to human manipulation (skin), surrounding environment particles, or even the manufacturing process itself (wafer dicing residues for example).

Defect characteristics may vary in size and appearance. From less than a micron to a few microns in size, their impact is related to the sensor pixel size. The rule here is usually to detect defects that cover two consecutive pixels and above, meaning in the range of 2-3µm for most current production. The FM appearance will differ depending on whether they reflect or absorb light. On a sensor, dark and light particles can be found on the pixel array and both need to be detected. Additional defects (**Figure 2**) on the pixel array include scratches, striations, stain, passivation, or watermarks traces, which can have a significant impact on the final image quality. These defects can have a much lower contrast difference with the pixel array and are usually larger. That implies that a different detection algorithm is required in automated systems.

The above defects lie on the pixel plain surface but some sensors come capped with a glass before lens assembly. This produces additional defects that can reside on the top or even the bottom surface of the glass. In this case, the detection becomes more difficult as the reflection/refraction of the glass must be taken into account and the focus correctly done onto the inspection plain (**Figure 3** and **Figure 4**).

Other types of defects or issues result from ensuring the proper alignment (X, Y, Theta, and Tilt) of the lens module with the pixel array as well as an inspection of the lens itself.

Inspection processes and options

Most of the time, inspection is carried out by operators looking into a microscope to find tiny particles. This process is the least expensive upfront and allows some kind of manual cleaning. Yet it shows several drawbacks and can become more costly in the end.

The shrink of the pixel size, down to 1.1µm in mass production and soon even smaller, leads to great difficulty for the operator to accurately detect very small defects in the range of 1µm. Also, visual inspection is not a repeatable process since different people with different experience will output different results. The last issue with operators' inspection is the requirement for a big number of inspection desks which can consume space and imply a lot of manual handling. In the end, manual inspection usually leads to unknown high escape rates resulting in scrap costs at the end of the process. There is also a costly requirement in terms of clean-room space.

The other common inspection process today is the incoming automated inspection of the sensors in wafer format, before sensor placement, wire bonding, and lens attach processes. This process is mature and quite efficient; however, it has the drawback of being held too far upstream of the lens-attach process step which has to be applied on

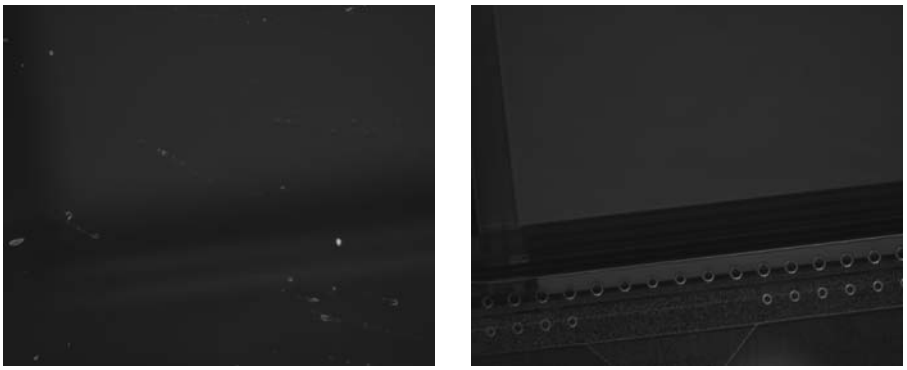


Figure 3. Scratch defect at the glass (left) and pixel array (right) levels

Figure 4. Foreign material located on glass at the glass (left) and pixel array (right) levels

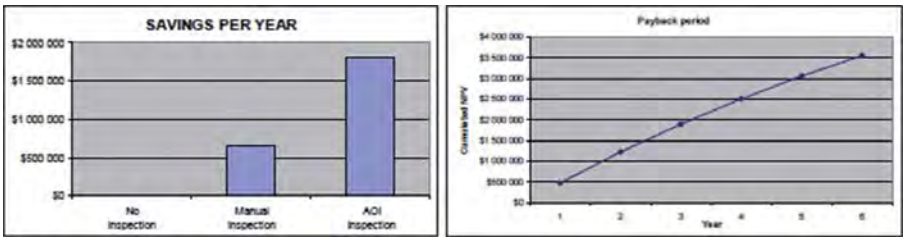


Figure 5. Conservative estimation of savings/year and payback period of inspection solutions

perfectly clean sensors. It is therefore quite common to see good dice from previously inspected wafers be contaminated just before lens assembly. The end result is a lower yield and additional scrap costs.

Both the above inspection processes can only be carried out off-line. The consequence is manual handling to and from these machines with a risk of adding some FM in the process. In-line solutions are still relatively rare since they require a very flexible solution and the combination of high throughput and detection accuracy. Sensor supports are different from customer to customer. Up-stream and down-stream systems communicate with different mapping formats. Although more difficult to implement today due to the lack of adapted equipment, this is the target to aim at in order to optimize the yield of the process.

Automated Optical Inspection (AOI)

New AOI systems, more optimized for the BEOL environment, can help solve these issues. They bring the same kind of benefits of all automated systems, namely, better repeatability and accuracy than with manual inspection, a faster throughput, and the traceability of the defects to enable further process improvements. However, unlike FEOL systems, they are built to ensure a great flexibility to adapt to each customer environment. The whole optical acquisition chain can be optimized easily, algorithms can be tuned according to the kind of defects, and products can be inspected in wafer, JEDEC trays, stiffeners, or board supports, depending on the process.

A Strong Return on Investment

Inspection processes are not productive processes per second, so the question related to their implementation is always the Return On Investment (ROI). What is the benefit of including an AOI in a camera module manufacturing line? A quick calculation results in significant savings with an ROI between 1 and 6 months. For a conservative 1 million units production per month of $1 sensors assembled with a $3 lens module, the materials related scrap costs (lenses attached to defective sensors) are worth more than $2.3M a year versus a process with no inspection, and in the range of $0.5M a year versus a manual inspection process. This takes into account a few hundred thousand dollars CAPEX cost for the AOI system. On top of the material cost savings, the inspection process cost of ownership per year is lower for an automated process than for manual inspection. The low cost of the workforce is balanced by the high number of operators required to ensure the whole production inspection.

Lastly the quality of the production is enhanced. This leads to better end-customer satisfaction, lower field returns costs, and can become a strong competitive advantage for the camera module manufacturer.

Conclusion

Although less visible than the latest innovations in terms of packaging or processes, the current and mainstream assembly processes for CMOS camera modules include significant saving opportunities. Current inspection processes can be greatly improved just before the lens attach-process stage. New BEOL-optimized AOI equipments can enable a higher yield in production and drive materials and process savings. The results obtained in recent trials at customer factories have demonstrated the financial and quality impact of these systems. This translates to a competitive advantage for the manufacturer through cost savings, higher productivity, and higher quality products for the camera module integrator.


Product Patent Notices

Mark or not, but don't mismark: that can be costly!

By Contributing Legal Editors, Jason Mirabito and Carol Peters
[Mintz, Levin, Cohn, Ferris, Glovsky and Popeo P.C.]

Many readers have undoubtedly seen an affixed plate or label on a product that identifies the manufacturer's name, serial number, and one or more U.S. patent numbers. Why are patent numbers displayed? Because, under U.S. patent law, a patent owner can recover damages from infringement of the identified patents from the time the patent owner gives an alleged infringer actual notice of infringement (either by filing a law suit or by sending a letter) or gives constructive notice of infringement.

Constructive notice of infringement is provided for in the patent marking statute, if the patent owner puts the relevant U.S. patent number(s) on the product. This constitutes notice to the world. The patent owner can collect damages from an infringer from the time the notice is applied to the product, rather than later when the patent owner either sends a letter accusing an alleged infringer of infringement and/or files a law suit against the alleged infringer.

Under the patent marking statute, the patent owner is only required to place "patent" or the abbreviation "pat" together with the patent number(s) on a product. Nothing else is required. Obviously, where the size of the product does not lend itself to such marking, such as a pin, the notice can be placed on the container or packaging. Also, if the patent has only method or process claims, then no patent marking is required to be displayed.

However, it is not mandatory to mark the patent number(s) on a patented product in order to recover damages for infringement. Patent marking simply affects the time from which damages begin to accrue. The marking statute provides that, in the event of the failure to mark a patented product, no damages can be recovered by the patent owner from an infringement action except on proof that the infringer was notified of the infringement and continued to infringe thereafter, in which event damages may be recovered only for infringement occurring after such notice (see Patent Statute § 287(a)).

It is necessary for a patent owner to review, on a regular basis, the patents identified in any patent notice on any product plate or label to insure that all the patents that are marked on the product are, in fact, still in force and have not expired. Often no active program exists for a patent owner to review and remove notices of expired patents from a product and to add notices of new patents that cover the product. Failure in updating patent notices can cause legal problems.

Patent Statute § 292 governs "false marking" which prohibits marking a product with a number of a patent that does not cover the product or has expired. The statute provides that a patent owner shall "be fined not more than $500.00 for every such event" of false marking. Until recently, courts have interpreted the provision as composing a single fine for marking multiple products erroneously. For example, if the product is a shoe and the patent number marked on the shoe has expired, whether the company sells one pair of shoes or 1,000 pairs of shoes, the fine would be "up to" $500.00. However, at the end of 2009, the Court of Appeals for the Federal Circuit issued a decision that changed case law. The Court found that the proper penalty for false marking should be "up to" $500.00 for *each* individual product that is falsely marked. False marking, therefore, can truly be a very costly action. In 2010 alone, a large number of suits have been brought against companies that have either marked their products with expired patent numbers or patent numbers that do not cover the product. Section 292 authorizes individuals to go after companies that engage in false marking. If successful, such individuals are entitled to one half of the penalty awarded with the other half going to the U.S. government.

The false marking statute is not a "no fault" statute. A finding of good faith by the patent owner can negate any penalty if the expired patent marking notice was not done with an intent to deceive the public to believe that the product was patented.

The lesson learned is patent marking can be good for you and allow you damages against infringers well before a suit is filed. Yet, patent owners must be vigilant in ensuring patent markings are current and accurate.

WHAT'S NEW!

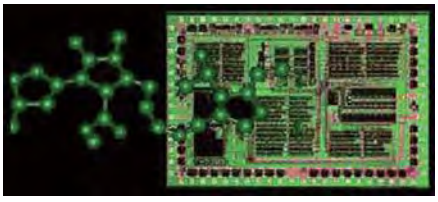
New Test Socket for 0.50mm Pitch BGAs

For testing BGA packages up to 12mm² (22x22 rows), with larger sizes available upon request, Advanced Interconnects Corporation of West Warwick, RI, USA have released a new Mod5 series Flip-Top BGA socket designed for test, debug, and validation. The compact, surface mount design (20x27mm) requires no tooling or

mounting holes in the target PC board and requires only a small keepout zone. The precision machined spring probes offer high bandwidth with very low insertion loss. Advance claim, "Metallic probes offer proven reliability over elastomeric sockets and long-life (spring probe contact system life is 200,000 cycles minimum)." The test socket assembles using a simple reflow process like a BGA. [www.advanced.com]

Electro–chemical Residue Sensor

After more than seven years of commercial development and testing, Tucson-based Environmental Metrology Corporation (EMC) is putting up for sale its electro-chemical residue sensor (ECRS) for semiconductor manufacturing, along with associated intellectual property that includes three issued patents and another that is pending. The technology is based on science developed at the University of



Arizona. Testing has proven that the ECRS can detect very small quantities of impurity left after an incomplete cleaning procedure. "We've invested heavily and worked hand-in-hand with semiconductor manufacturing customers to prove the efficacy of the technology and quantify its benefits," says Doug Goodman, Chairman of EMC. "You can't optimize what you can't measure, and ECRS is the first tool the industry can use that performs in situ and real-time measurement of cleanliness inside high-aspect-ratio features while the wafer is being cleaned, rinsed or dried," says Goodman. "This leads to significant savings in water and energy usage, while increasing manufacturing throughput and yield." [env-metrology.com]

Printable Thermal Management Material

Addressing the challenges posed by traditional greases and phase-change thermal interface materials, Henkel has developed and commercialized Loctite

PowerstrateXtreme Printable (PSX-P), a new thermal management product. Loctite PSX-P allows for thermal management materials to be deposited using traditional screen and stencil printing methodologies and is offered in both medium dry and extended dry versions to accommodate varying manufacturing conditions and requirements. The reliability and performance of PSX-P is consistent with that of Loctite PowerstrateXtreme phase-change films but its paste format enables the material thickness to be adjusted as required.

"Traditionally, phase-change materials have been supplied in film formats," explains Henkel's Jason Brandi, Global Product Manager for TIM Films and Advanced Materials. "And, while films do come in a variety of thicknesses, thinner films are difficult to manufacture and even more problematic from a handling point of view. Loctite PSX-P resolves these issues." Other advantages of PSX-P are its adaptability to deviations in surface flatness and the ability to fill any voids with varying thicknesses. [www.henkel.com/electronics]

Kelvin Connection Contactor

Developed for power management and other precision analog applications that require very tight test guard bands, the Pad ROL 200K from Johnstech International provides improved performance and flexibility. The design is a combination of their traditional high current solid Pad ROL 200 contact (the force) and a dual touch, flexible sense contact that surrounds the force contact on both sides. Two self-cleaning features help ensure the Pad ROL 200K delivers a low and repeatable Kelvin contact resistance. The force contacts include a wipe action that automatically prevents surface debris build-up on the contact tip. In addition, the contactor's force and sense contacts work in combination to remove debris from between the two contacts. These inherent wipe functions are claimed to lower cost of test by extending Mean Time Between Assists (MTBA) and contact life. It is possible to configure and reconfigure the contactor for standard contacting, selective Kelvin (mixed mode applications), or full Kelvin testing. [www.johnstech.com]

(continued from Page 19)

products using electrografting (eG) and chemical grafting (cG).

Isolation

The isolation layer traditionally provides a wire electrical isolation from the semiconducting bulk material, but in the case of TSVs, it should also provide a compliant layer. SiO_2 is the industry's de-facto standard isolation layer, but its mechanical properties cause serious limitations. The following equation[2], illustrates the benefits of a compliant layer in a typical Cu TSV system:

$$Stress\ (Si) = f(E - modulus, R^2),\ where\ R = TSV\ radius$$

Alchimer scientists have been able to demonstrate orders of magnitude less stress through the use of small-diameter vias in conjunction with an elastomeric polymer layer described in **Table 2**. A recent patent from Intel[3] also supports efforts in seeking compliancy in TSVs.

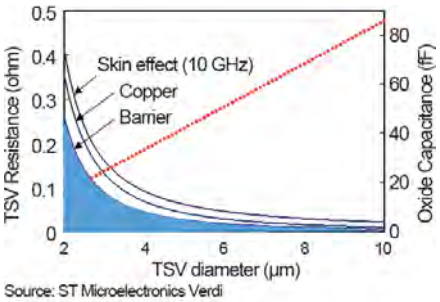
Parameter	Value	Unit	Notes
CTE	30	ppm/°C	
Dielectric constant	3		SiO_2 = 4.2
Breakdown voltage	28	MV/cm	SiO_2 = 10
Capacitance density	0.13	fF/µm²	
Leakage current	15	nA/cm²	SiO_2 = 10-20
Surface finish	1.6	nm	SiO_2 = 2nm
Substrate compatibility	< 200	Ohm.cm	Silicon substrate resistivity
Young modulus	3.4	GPa	SiO_2 = 107
Stress	10	MPa	SiO_2 = 100

Table 2. Film properties for eG isolation layer

Barrier

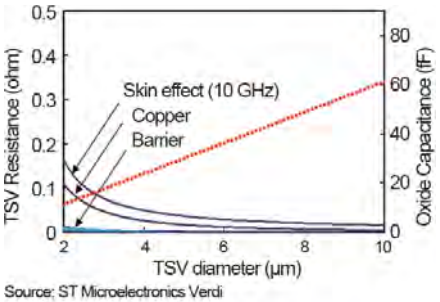
The barrier layer prevents Cu diffusion into the bulk substrate, and has typically been a dry-deposited TiN or TaN material. Although these materials have provided adequate barrier performance when deposited on nearly planar surfaces, they are relatively brittle and can only be conformally deposited on high aspect ratio (HAR) TSVs (3-D structures) with slow and expensive ALD-type equipment. Additionally, the aforementioned films are highly resistive, contributing to unnecessarily high TSV series resistance and the misconception that large vias are required to maintain signal integrity. A simple and inexpensive NiB barrier is available that allows for excellent electrical performance in very small via diameters. **Figures 2a** and **2b** summarize recent work done by STMicroelectronics and the Verdi Project.[4] In **Figure 2a**, the data assumes the use of a 300nm SiO_2 dielectric layer with permittivity of 4.2, and a 30nm TiN barrier layer with resistivity of 2,000 µΩ/cm. **Figure 2b** assumes the use of a 300nm electrografted isolation layer with permittivity of 3, and a 100nm chemicalgrafted barrier layer with resistivity of 20 µΩ/cm.

This data should come as no surprise, since Ni-based alloys have been successfully used as a barrier material outside front-end lines for decades. NiB deposition is, however, a wet process.



Source: ST Microelectronics Verdi

Figure 2a. TSV resistance and oxide capacitance for nominal (dry deposition) case, 15 µm TSV depth



Source: ST Microelectronics Verdi

Figure 2b. TSV resistance and oxide capacitance for electrografted (wet deposition) case, 15 µm TSV depth

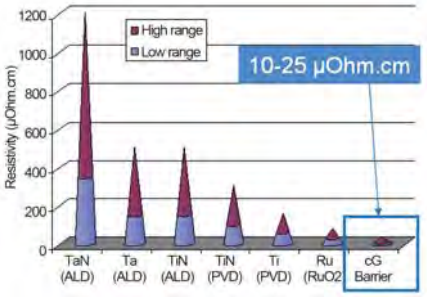


Figure 3. Resistivities for various barrier layers materials and deposition methods

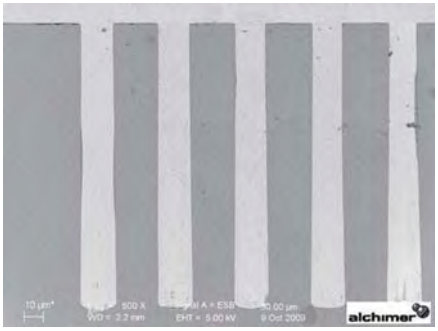


Figure 4. Void-free copper fill, directly on NiB barrier layer

Cu seed layer

Adding to its advantages, the NiB approach eliminates the need for a seed layer. A seed layer is required when the barrier is too resistive to accept normal electrochemical deposition, as in the case of dry-deposited Ti, TiN, Ta, etc. But with a NiB barrier, one can fill directly with either Ni or Cu. **Figure 3** shows the resistance of various materials including NiB cG barrier. Only Ruthenium offers a similar possibility, but at what cost? **Figure 4** shows a scanning electron microscope (SEM) image of a TSV with void-free fill directly on a NiB barrier.

Now comes the fun part

We've briefly outlined the beneficial performance characteristics of alternative film materials available through wet processing. These materials allow enhanced design features and electrical performance at reduced cost, but to bring costs fully in line with demand, capital costs must also be slashed. For the purposes of this article, let's examine only the isolation, barrier, and seed capital-equipment costs attributed to 10:1 and 20:1 aspect ratio vias — something the consortia have not offered us thus far, and we'll see why.

Today, dry 10:1 aspect ratio vias are obtainable with expensive iPVD-type tools, but 20:1 aspect ratio vias can only be deposited conformally by even more expensive ALD processes. These methods work from a technical perspective, but from a production and ROI standpoint, one needs to use extreme cost accounting techniques to make the argument. Data taken from Yole Développement's TSV cost model[5] are shown in **Tables 3a** and **3b**. The capital equipment cost (CapEx) multiplier for dry 10:1 and 20:1 aspect ratio designs is 3x and 5x, respectively, compared to the wet equivalent. Clearly, the basic transition from dry to wet has tremendous potential as a first step in lowering CapEx. The second step would be an evolution of the wet tools themselves. More affinity with productivity and ROI metrics of EMS manufacturers rather than 45nm CMOS manufacturers would be a good start.

	Dry Investment			
	Tool	10:1 AR	20:1 AR	Tool
Isolation	PECVD	3	3	MOCVD
Barrier	iPVD	21	40	ALD
Seed				

Wet Investment (1 Tool)			
Tool	10:1 AR	20:1 AR	*No Seed*
AquiVia XS enabled	8	8	Isolation
			Barrier

Fill (Via Size Dependent)

Source: Yole Développement

Tables 3a and 3b. Capital equipment investment for TSV processes, in millions of US dollars (for 30k 300mm wafers/month)

Users can't afford not to get wet

Substituting wet thin-film deposition for dry deposition runs contrary to what the community has been conditioned to accept for decades, but remember, we live in the age of nanotechnology. With self-assembled nanometric layers, molecules are custom-built layer upon layer in solution. The chemistry and process are the value proposition, not the delivery mechanism. So vacuum-heavy superstructures that occupy a whole room are no longer necessary and can be replaced by simple, inexpensive plating tanks.

To sum up: the industry is faced with a rare opportunity in which a promising technology is actually an easier engagement than its existing competition. Moreover, the up-front investments in wet bench feasibility and productivity are miniscule by industry standards. Prices on TSV processes have nowhere to go but down, and it seems certain that as Chinese vendors add TSVs to their bumping infrastructure, they will utilize manual or semiautomatic tools. This approach will set the price for these TSV commodities.

Side benefits of wet processing:

Via Etching - DRIE, or the Bosch process, is the predominant technique used for etching TSVs, and the depreciation costs associated with it are simply a function of throughput. That throughput is generally compromised in order to minimize the inherent scalloping effect to accommodate the limitations of dry processing. Typical etch rates being used today are in the range of 10 µm/minute. Some users who have recognized the attributes of wet processing are increasing those etch rates by a factor of 4 and living happily with scallops of up to 2µm. **Figure 5** illustrates the AquiVia stack with perfectly conformal coverage of highly scalloped vias.

Fill

One of the biggest questions in the debate about why small-diameter HAR vias are the best approach to low-cost TSVs is fill time and material expense. One could easily dedicate several papers to this subject, but if the expense of large via fill is not apparent to the average reader, just ask your favorite fill provider what the difference in time is to fill a 5x50µm versus a 50x200 µm TSV. Most newcomers to TSV technology will be astonished by the number of hours of equipment depreciation and materials expense required for the larger TSV at little to no value for the end user. From a practical perspective, the only advantage of large-diameter shallow vias, other than power, is their access to current tool and deposition techniques.

Handle wafers

Debate concerning handle wafers is in full swing. Where do they apply, for what process flow, and what are the minimum wafer thicknesses? No doubt this additional manufacturing step will find its place among the many TSV product-and-process variations. But if we can drill and fill deep vias, then we create one or two positive outcomes:

- Possible elimination of the handle wafer if minimum wafer thickness can be preserved
- Reduced real estate allocated to TSVs by virtue of HAR, narrow-diameter vias. A 3 µm diameter via through a 60 µm wafer supported by a handle wafer is still a 20:1 aspect ratio TSV.

Vias with aspect ratios of 40:1 are being designed for MEMS applications today without handle wafers, why not for others?

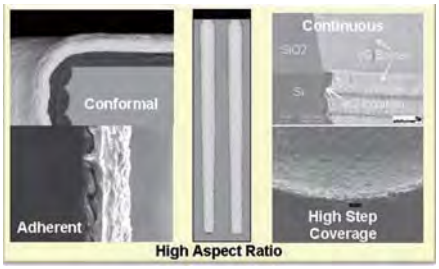


Figure 5. AquiVia film stack showing conformal coverage of scalloped vias and varied substrate material

Vacuum Tool Learning Curve

Most via-last users, particularly the OSATs, do not have the requisite breadth of vacuum-based tool experience, and will need to add that learning curve to the daunting prospect of much higher CapEx. Wet processing is something they have done for decades, and offers a much easier entry point.

Conclusions

Although dry processing can clearly get the job done by brute force, the effort and expense will only be adopted by those who can afford the luxury or are obliged to carry that weight for other front-end processes like high-end via-first and via-middle. The rest of us will require more cost-effective manufacturing alternatives that allow TSVs to become the ubiquitous commodity, giving designers power to revolutionize systems-level integration. Today, the only alternative to expensive and cumbersome dry processing is electrografted and chemically grafted wet film deposition, coming soon to a fab near you, or maybe not so near you if you live in the West. Let the games begin.

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COMPANY HEADQUARTERS	DIE BONDER CAPABILITY	DIE BONDER SPECIFICATIONS	FLIP CHIP BONDER CAPABILITY	FLIP CHIP BONDER SPECIFICATIONS
Company Street Address City, State, Country Telephone Website CM = Contact Manufacturer	Productivity FA = Fully Automatic SA = Semi Automatic Bond Method A = Adhesive E = Eutectic G = Glass, Silver S = Soft Solder O = Other	WD = Wafer Diameter DS = Die Size Placement Accuracy XY (µm) @ 3σ θ (°) @ 3σ CT = Cycle Time	Productivity FA = Fully Automatic SA = Semi Automatic Bond Method A = Adhesive/Bump S = Solder/Flux U = Ultrasonic O = Other	WD = Wafer Diameter DS = Die Size Placement Accuracy XY (µm) @ 3σ θ (°) @ 3σ CT = Cycle Time
Amicra Microtechnologies GmbH Wernerwerkstrasse 4 Regensburg D-93049, Germany Tel: +49-941-208-2090 www.amicra.com	FA A, S	WD: CM DS: CM XY: ± 0.5 - 3.0 µm θ: CM CT: 1.0 - 60 sec	FA A, S	WD: CM DS: CM XY: ± 0.5 - 3.0 µm θ: CM CT: 1.0 - 60 sec
ASM Assembly Automation 4/F Watson Centre, 16 Kung Yip Street Kwai Chung, Hong Kong, China Tel: +852-2619-2000 www.asmpacific.com	FA A, E, O	WD: up to 300 mm DS: 0.15 - 25.4 mm XY: ± 25.4 - 38.1 µm θ: ± 0.5 - 5° CT: 0.18 - 0.42 sec	FA A, S, U	WD: up to 300 mm DS: 0.25 - 25.4 mm XY: ± 10 - 15 µm θ: ± 0.05 - 0.5° CT: 0.7 sec
Canon Machinery Inc. 85 Minami Yamada-cho, Kusatsu-shi Shiga 525-8511, Japan Tel: +81-77-563-8511 www.canon-machinery.co.jp	FA A, E, S	WD: up to 300 mm DS: 0.15 - 20 mm XY: ± 25 - 100 µm θ: ± 0.5 - 3° CT: 0.19 - 0.65 sec	FA U, O	WD: up to 200 mm DS: 0.3 - 1.5 mm XY: ± 5 µm θ: CM CT: 1.4 sec
Datacon Technology GmbH Subsidiary of BE Semiconductor Industries N.V. Innstrasse 16 Radfeld A-6240, Austria Tel: +43-5-337-6000 www.datacon.at	FA A, O	WD: up to 300 mm DS: 0.17 - 50.0 mm XY: ± 7 µm θ: CM CT: 0.51 sec	FA A, S	WD: CM DS: CM XY: ± 10 µm θ: CM CT: 0.36 sec
Dr. Tresky AG Boehnirainstrasse 13 Thalwil CH-8800, Switzerland Tel: +41-44-772-1941 www.tresky.com	SA A, E, G	WD: up to 200 mm DS: 0.15 - 50.0 mm XY: ± 1 - 10 µm θ: CM CT: CM	SA A, S, U	WD: up to 200 mm DS: 0.15 - 50.0 mm XY: ± 1 - 10 µm θ: CM CT: CM
Esec AG Subsidiary of BE Semiconductor Industries N.V. Hinterbergstrasse 32 Cham 6330, Switzerland Tel: +41-41-749-5111 www.esec.com	FA A, S	WD: up to 300 mm DS: 0.25 - 25.4 mm XY: ± 15 - 80 µm θ: CM CT: 0.17 - 0.60 sec	FA CM	WD: up to 300 mm DS: 0.5 - 25 mm XY: ± 12 µm θ: ± 0.1 - 1.0° CT: 0.4 sec
Finetech GmbH & Co. KG Wolfener Strasse 32-34 Berlin 12681, Germany Tel: +49-30-936-6810 www.finetech.de	FA, SA A, E, O	WD: up to 300 mm DS: 0.07 - 100 mm XY: ± 0.5 - 5 µm θ: CM CT: CM	FA, SA A, S, U, O	WD: up to 300 mm DS: 0.07 - 100 mm XY: ± 0.5 - 5 µm θ: CM CT: CM
F&K Delvotec Semiconductor GmbH Industriezeile 49a Braunau A-5280, Austria Tel: +43-7722-67052-8270 www.fkdelvotec.at	FA A	WD: up to 300 mm DS: 0.25 - 40 mm XY: ± 10 µm θ: CM CT: 3.6 se		
Grohmann Engineering GmbH Rudolf-Diesel-Strasse 14 Pruem 54595, Germany Tel: +49-6551-680 www.grohmann.com			FA A, S, O	WD: up to 450 mm DS: 0.5 - 35 mm XY: ± 10 µm θ: CM CT: 0.8 - 1.0 sec
Hesse & Knipps GmbH Vattmannstrasse 6 Paderborn D-33100, Germany Tel: +49-5251-1560-0 www.hesse-knipps.com			FA U	WD: up to 300 mm DS: 0.2 - 12 mm XY: ± 5 µm θ: CM CT: CM

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Company Street Address City, State, Country Telephone Website CM = Contact Manufacturer	Productivity FA = Fully Automatic SA = Semi Automatic Bond Method A = Adhesive E = Eutectic G = Glass, Silver S = Soft Solder O = Other	WD = Wafer Diameter DS = Die Size Placement Accuracy XY (µm) @ 3σ θ (°) @ 3σ CT = Cycle Time	Productivity FA = Fully Automatic SA = Semi Automatic Bond Method A = Adhesive/Bump S = Solder/Flux U = Ultrasonic O = Other	WD = Wafer Diameter DS = Die Size Placement Accuracy XY (µm) @ 3σ θ (°) @ 3σ CT = Cycle Time
Hybond 330 State Place Escondido, CA 92029 Tel: +1-760-746-7105 www.hybond.com	SA A, G	WD: CM DS: 0.1 - 25.4 mm XY: ± 25.4 µm θ: CM CT: 4 - 40 sec		
Kosaka Laboratory Ltd. Mikuni East Building 2F 6-13-10 Sotokanda, Chiyoda-ku Tokyo 101-0021, Japan Tel: +81-3-5812-2081 www.kosakalab.co.jp	FA CM	WD: CM DS: CM XY: ± 30 - 50 µm θ: ± 3 - 5° CT: CM		
Kulicke & Soffa Industries Corp. 1005 Virginia Drive Ft. Washington, PA 19034 Tel: +1-215-784-6000 www.kns.com	FA A	WD: up to 300 mm DS: 1.0 - 25.4 mm XY: ± 12 µm θ: ± 0.1° CT: CM		
Mühlbauer Inc. Josef-Mühlbauer-Platz 1 Roding 93426, Germany Tel: +49-9461-952-1653 www.muhlbauer.com	FA A	WD: up to 200 mm DS: CM XY: ± 30 µm θ: CM CT: 0.36 sec	FA CM	WD: 300 mm DS: CM XY: ± 25 µm θ: CM CT: 0.18 - 0.36 sec
Newport Corporation 1791 Deere Avenue Irvine, CA 92606 Tel: +1-949-863-3144 www.newport.com	FA A, E	WD: up to 200 mm DS: 0.2 mm Min. XY: ± 5 - 10 µm θ: CM CT: CM	FA A, S	WD: up to 200 mm DS: 0.2 mm Min. XY: ± 5 - 10 µm θ: CM CT: CM
NPOS Technologies Inc. 1922 Santa Rosa Avenue Pasadena, CA 91104 Tel: +1-626-398-0327 www.npos-usa.com	SA A, E	WD: CM DS: 0.1 - 20 mm XY: ± 2 µm θ: CM CT: CM	SA A, S, U	WD: CM DS: 0.2 mm Min. XY: ± 3 µm θ: CM CT: CM
Pac Tech GmbH Am Schlangenhorst 15-17 Nauen 14641, Germany Tel: +49-3321-4495-100 www.pactech.com			FA A, S	WD: up to 300 mm DS: 0.25 - 25 mm XY: ± 2.5 - 25 µm θ: CM CT: 1.2 sec
Palomar Technologies, Inc. 2728 Loker Avenue West Carlsbad, CA 92010 Tel: +1-760-931-3600 www.palomartechnologies.com	FA A, E	WD: up to 200 mm DS: 0.18 - 50.8 mm XY: ± 1.5 - 12.7 µm θ: CM CT: 1.8 - 35 sec	FA A, S	WD: up to 200 mm DS: 0.18 - 50.8 mm XY: ± 1.5 - 12.7 µm θ: CM CT: 1.8 - 35 sec
Panasonic Factory Solutions Company of America 909 Asbury Drive Buffalo Grove, IL 60089 Tel: +1-847-495-6100 www.panasonicfa.com	FA A	WD: up to 300 mm DS: 0.25 - 25.4 mm XY: ± 15 - 25 µm θ: ± 0.3° CT: 0.45 - 0.56 sec	FA A, S, U	WD: up to 300 mm DS: 0.3 - 20 mm XY: ± 3 - 10 µm θ: CM CT: 1.0 - 1.8 sec
Semiconductor Equipment Corporation 5154 Goldman Avenue Moorpark, CA 93021 Tel: +1-805-529-2293 www.semicorp.com	SA A, E	WD: CM DS: 0.15 - 25.4 mm XY: ± 5 - 25.4 µm θ: CM CT: 18 sec Min.	SA A, S, U	WD: CM DS: 0.15 - 25.4 mm XY: ± 5 - 25.4 µm θ: CM CT: 18 sec Min.

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Shibaura Mechatronics Corporation 2-5-1, Kasama, Sakae-ku, Yokohama Kanagawa Prefecture 247-8610, Japan Tel: +81-45-897-2421 www.shibaura.co.jp	FA A	WD: up to 300 mm DS: CM XY: CM θ: CM CT: 0.2 sec	FA A, S, U	WD: up to 300 mm DS: 2 - 6 mm XY: ± 2.5 - 15 µm θ: CM CT: 1.0 - 2.5 sec
Shibuya Kogyo Co. Ltd. Mameda-Honmachi, Kanazawa Kanazawa 920-8681, Japan Tel: +81-76-262-1200 www.shibuya.co.jp	FA A	WD: up to 300 mm DS: 2 - 6 mm XY: ± 2.5 µm θ: CM CT: 3.0 sec	FA A, S, U	WD: up to 300 mm DS: 0.25 - 20 mm XY: ± 1.0 - 15 µm θ: CM CT: 1.6 - 60 sec
Shinkawa Ltd. 2-51-1 Inadaira, Musashimurayama-shi Tokyo 208-8585, Japan Tel: +81-42-560-1231 www.shinkawa.com	FA A, E	WD: up to 300 mm DS: 0.18 - 25 mm XY: ± 20 - 30 µm θ: ± 0.5 - 3° CT: 0.15 - 0.35 sec	FA U, O	WD: up to 200 mm DS: 0.3 - 25 mm XY: ± 2 - 5 µm θ: CM CT: 0.8 - 1.4 sec
Smart Equipment Technology SAS 131, Impasse Barteudet, BP 24 Saint Jeoire 74490, France Tel: +33-450-358392 www.set-sas.fr	FA A	WD: up to 300 mm DS: 0.2 - 100 mm XY: ± 0.5 - 3.0 µm θ: CM CT: CM	FA, SA A, S, U, O	WD: up to 300 mm DS: 0.2 - 100 mm XY: ± 0.5 - 3.0 µm θ: CM CT: CM
TDK Electronics Europe GmbH Wanheimer Strasse 57 Dusseldorf D-40472, Germany Tel: +49-211-90770 www.tdk-components.de			FA A, S, U	WD: up to 200 mm DS: 0.3 - 30 mm XY: ± 3 - 8 µm θ: CM CT: 0.8 - 5.3 sec
Toray Engineering Co. Ltd. Nihonbashi Muromachi Building 3-16, Nihonbashi-Hongokucho 3-chome, Chuo-ku Tokyo 103-0021, Japan Tel: +81-3-3241-1543 www.toray-eng.com			FA, SA A, S, U, O	WD: up to 300 mm DS: 0.2 - 20 mm XY: ± 0.5 - 5 µm θ: ± 0.2° CT: 1.7 - 30 sec
Ultron Systems, Inc. 5105 Maureen Lane Moorpark, CA 93021 Tel: +1-805-529-1485 www.ultronsystems.com	SA A, E	WD: CM DS: CM XY: ± 25.4 µm θ: CM CT: CM		
Unovis-Solutions 147 Industrial Park Drive Binghampton, NY 13904 Tel: +1-607-779-3800 www.unovis-solutions.com			FA S	WD: CM DS: CM XY: CM θ: CM CT: CM
West-Bond Inc. 1551 S. Harris Court Anaheim, CA 92806 Tel: +1-714-978-1551 www.westbond.com	SA A, E	WD: CM DS: CM XY: CM θ: CM CT: CM		

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July 11-13, 2010
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www.semi.org/cms/groups/public/documents/web_content/ctr_036516.pdf

June 14-16, 2010
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Moscow, Russia
www.semiconrussia.org/SCRUSSIA-EN/index.htm

July 13-15, 2010
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San Francisco, California, USA
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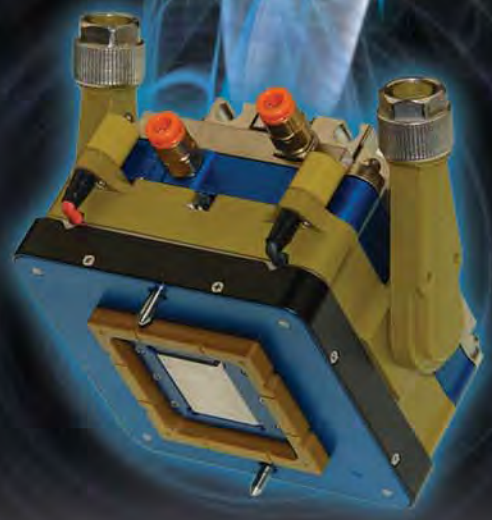

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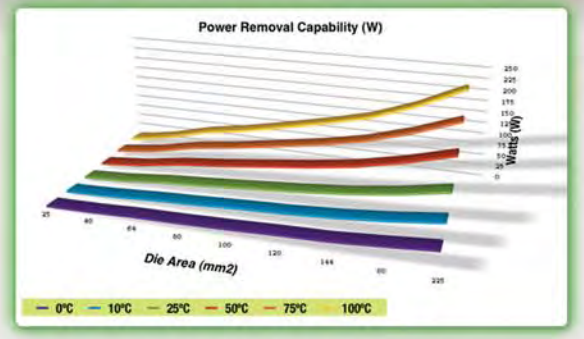

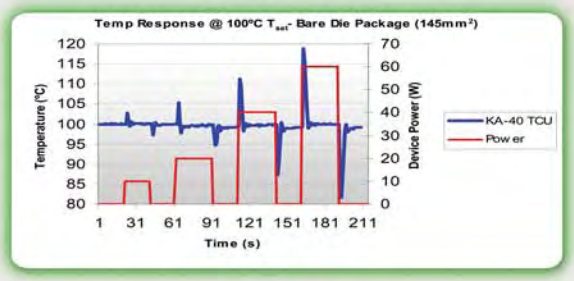

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