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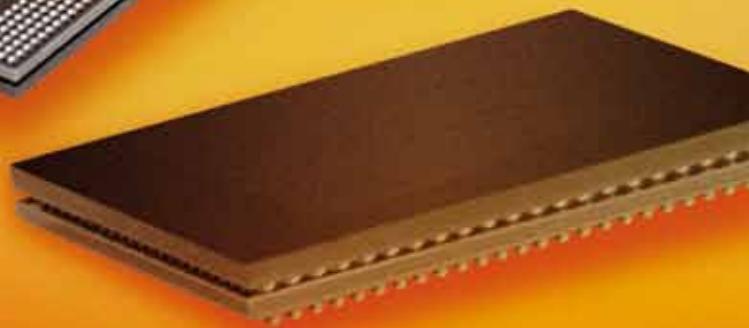
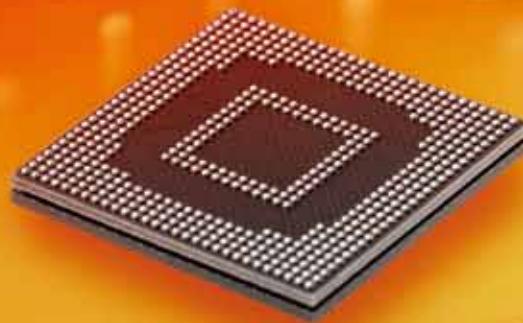
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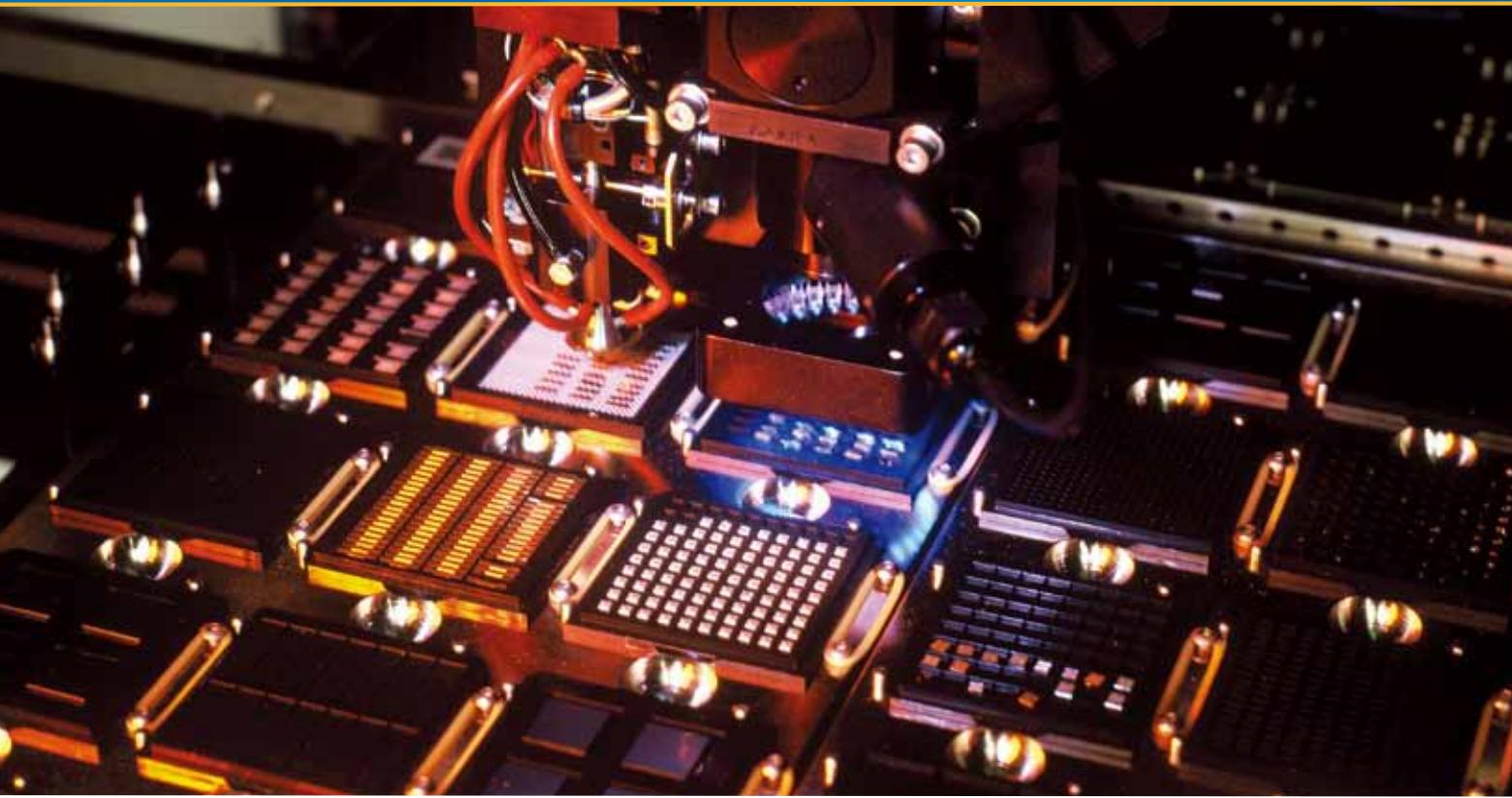
*The International Magazine for the Semiconductor Packaging Industry*

Volume 16, Number 4

July - August 2012

- Final Test
- Copper Pillar Bumping
- Memory Market Trends
- Metrology Processes for 3D IC
- TSV MEOL: End of the Middle or Middle of the End?





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# CONTENTS

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## FEATURE ARTICLES

### TSV MEOL: End of the Middle, or Middle of the End?

Scott Jewler *Powertech Technology Inc.*

**23**

### Sub-surface Microscopies for 3D Interconnect Process and Characterization Metrology

Lay Wai Kong, Victor Vartanian, Andy C. Rudack, Klaus Hummler, and Alain C. Diebold *SEMATECH, GlobalFoundries, and CNSE*

**27**

### Getting Your New IC to Market Faster

Joe Holt *Integra Technologies*

**32**

### Considering Electronic Product's Quality Specifications by Application(s)

Ephraim Suhir *Bell Labs Research*

**34**

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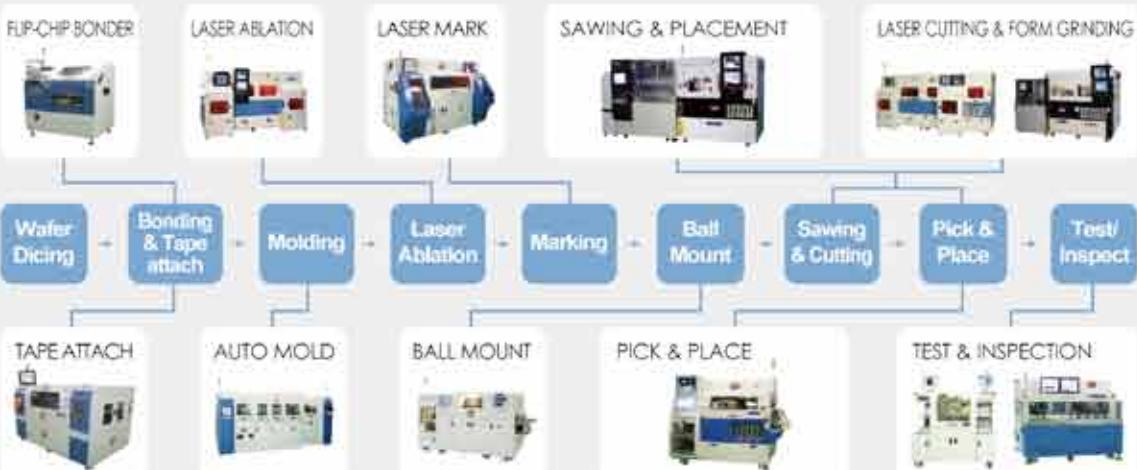




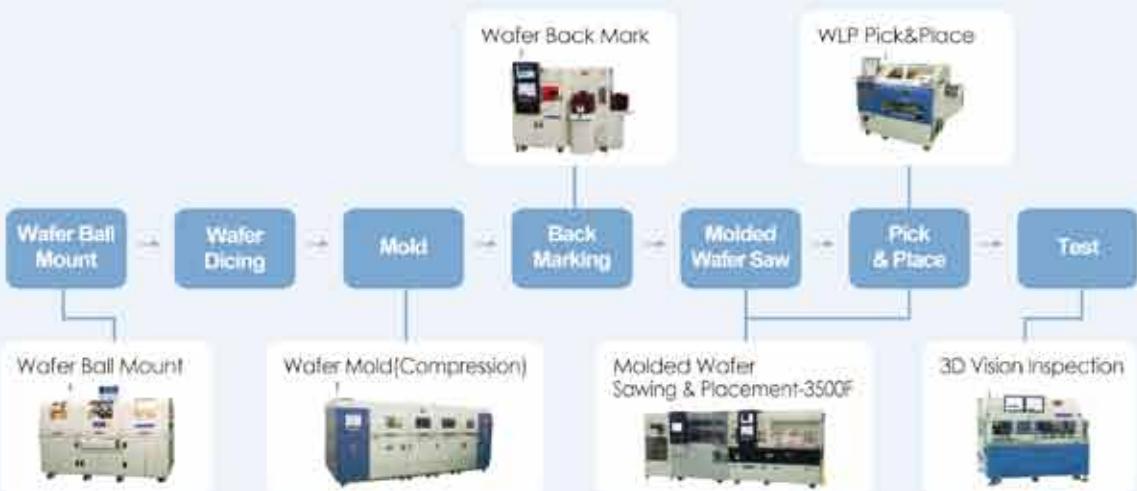
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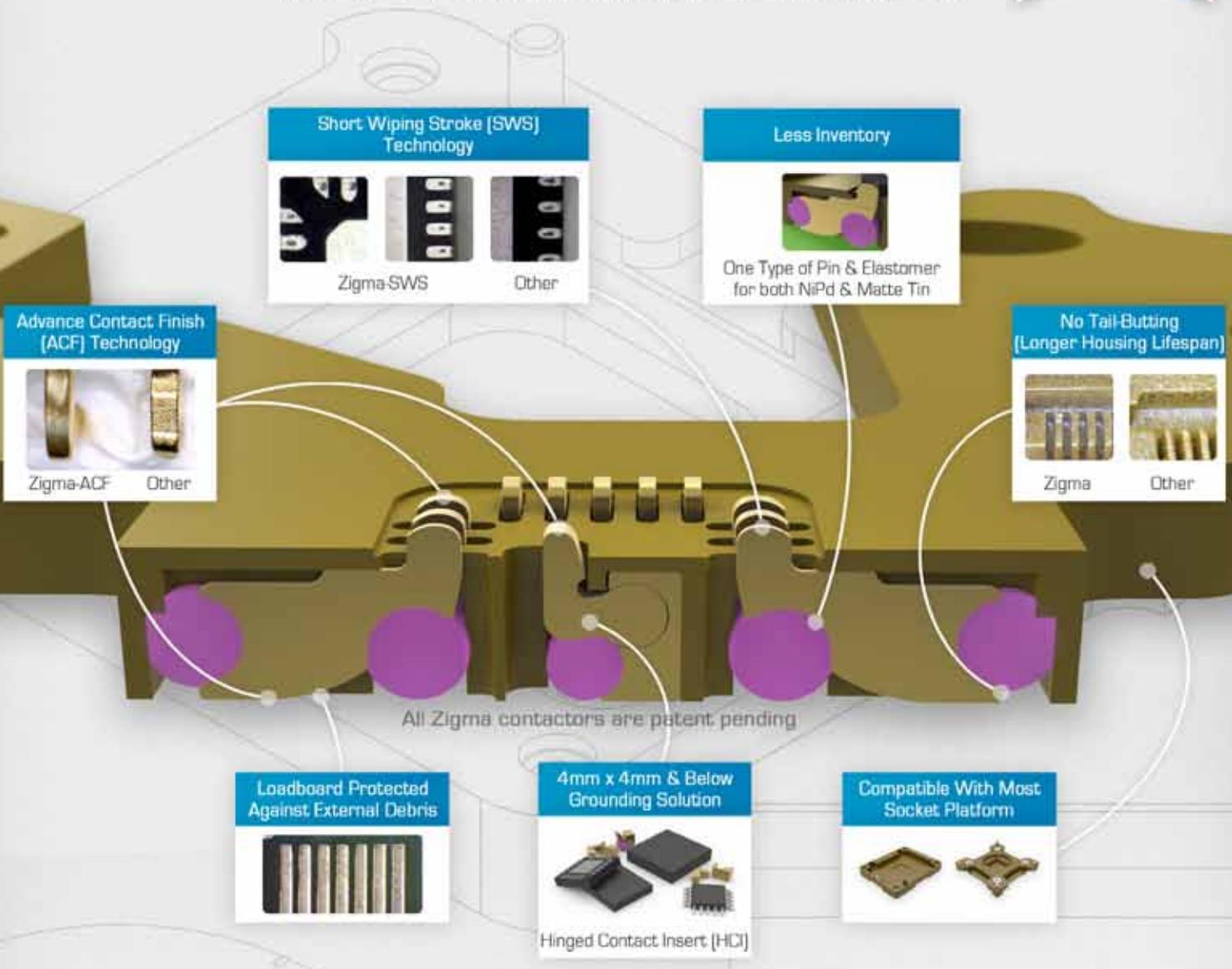
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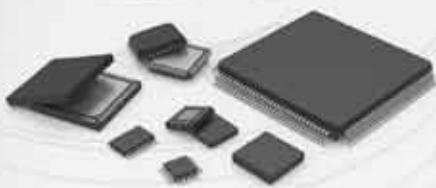
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## FEATURE ARTICLES

<b>Advanced Flip Chip Packaging Platform for Fine Pitch, High Performance and Low Cost Applications</b>	<b>38</b>
Raj Pendse, Ph.D. and Mukul Joshi, <i>STATS ChipPAC Inc.</i>	
<b>Finding Failures in Novel Memory Devices and Modules</b>	<b>44</b>
Paul Sakamoto, <i>DCG Systems Corp.</i>	
<b>An Innovative Approach to Achieving the Best Cost Structure for Semiconductor Companies</b>	<b>48</b>
Bharat Desai, <i>Contributing Editor</i>	

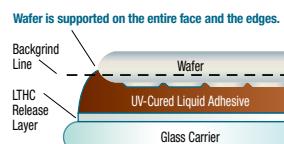
## DEPARTMENTS

<b>From the Publisher</b> Kim Newman, <i>Chip Scale Review</i>	<b>6</b>
<b>Guest Editorial SEMI 3D IC Standardization 2012 Update</b> James Amano, <i>SEMI</i>	<b>8</b>
<b>Business Trends Designing from the Outside In: Ultrabook™ Form Factor Drives Innovation</b> Simon McElrea, <i>Invensas Corporation</i>	<b>12</b>
<b>Market Trends Memory Market Update</b> Adrienne Downey and Jim Feldhan <i>Semico Research</i>	<b>16</b>
<b>Industry News</b> <i>Chip Scale Review Staff</i>	<b>18</b>
<b>What's New</b> <i>Chip Scale Review Staff</i>	<b>22</b>
<b>Guest Editorial The Back End's Back Ache</b> Lee J. Smith, <i>Microelectronic Industry Experts</i>	<b>52</b>
<b>Advertiser Index, Advertising Sales</b>	<b>56</b>

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## STAFF

**Kim Newman** Publisher  
[knewman@chipscalereview.com](mailto:knewman@chipscalereview.com)  
**Françoise von Trapp** Senior Technical Editor  
[fvontrapp@chipscalereview.com](mailto:fvontrapp@chipscalereview.com)  
**Sandra Winkler** Contributing Editor  
[slwinkler@newventureresearch.com](mailto:slwinkler@newventureresearch.com)  
**Dr. Thomas Di Stefano** Contributing Editor  
[tom@centipedesystems.com](mailto:tom@centipedesystems.com)  
**Paul M. Sakamoto** Contributing Editor Test  
[paul.sakamoto@comcast.net](mailto:paul.sakamoto@comcast.net)  
**Jason Mirabito** Contributing Legal Editor  
[mirabito@mintz.com](mailto:mirabito@mintz.com)

## SUBSCRIPTION INQUIRIES

Chip Scale Review  
T 408-429-8585  
F 408-429-8605  
[subs@chipscalereview.com](mailto:subs@chipscalereview.com)

Advertising Production Inquiries:  
**Kim Newman**  
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# FROM THE PUBLISHER



## Economy, Ecology & Events

The global economy, arguably the most significant and complex topic in the upcoming U.S. presidential election will have a direct impact on the developing trends in the semiconductor industry. Although issues exist within the national and global economic systems, our industry has seen solid first half results for 2012, noting analysts are watching vigilantly for yearend forecasting indicators. For most businesses, a mid-year financial review may be the most important of any quarterly review, as the time to make the necessary adjustments to company business plans leading to reportable and demonstrative successes for 2012.

Clearly the current conditions of the European economy persist. We see the European semiconductor industry continue to show relative stability as a result of the overall global demand for electronic components and equipment. Going forward for the next several quarters we may see additional stress points to the general economic condition of the European market that could have a direct cause and effect on it and the various collateral downstream activities. These "steady" business conditions are allowing companies to continue "offensive" strategies in both technology and marketing, versus defensive strategies associated with a downturn or those skeptical decisions that come with any dramatic increases. We must stay attentive on developments to this changing environment.

Publishing the premier semiconductor industry "print publication" has many economic challenges and I would like to take this opportunity to comment on two of these. The leading question is "why should we hard copy print" continues to have a relatively easy answer; because our advertisers, advisors and subscribers continue to remind us that this is a "value" we bring the industry. Conservationism and the use of paper, as well as costs of mailing, was another challenge that has been addressed. Our magazine is now lighter as a result of a more cost effective paper stock. Fear not as this new "look and feel" has the same average number of pages per issue based on the time tested format of CSR, related to editorial content and advertising space.

Last in the list is Events, noting there are several to mention.

CSR was pleased to again be the Official Media Sponsor for ECTC 2012. CSR staff exhibited and met with the organizing committee to review media coverage and strategies for the upcoming year. Read the highlights of the event covering the many technical sessions and exhibition further in this issue.

Semicon West 2012 is coming up on July 10-12 in San Francisco, CA, with CSR a Media Sponsor as well as an exhibitor. Our staff anticipates many of the "mid-year" strategic planning discussions as well.

Planning for the International Wafer Level Packaging Conference (IWLPC) continues. Contact your CSR representative for sponsorship and print ads. IWLPC technical sessions and exhibition are held in San Jose, November 5 – 8.

Go on the "E"ffensive and enhance your company's market presence by submitting abstracts, advertising, sponsoring, exhibiting and attend industry events!

*Kim Newman*  
Publisher

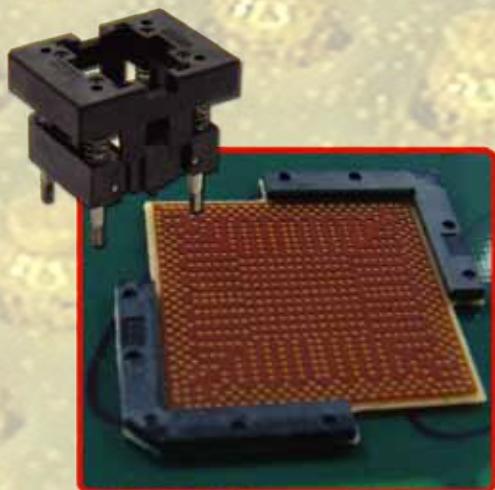
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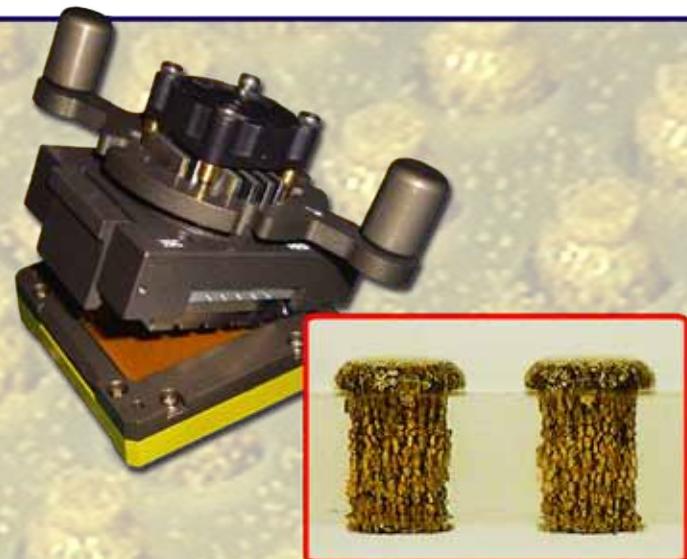
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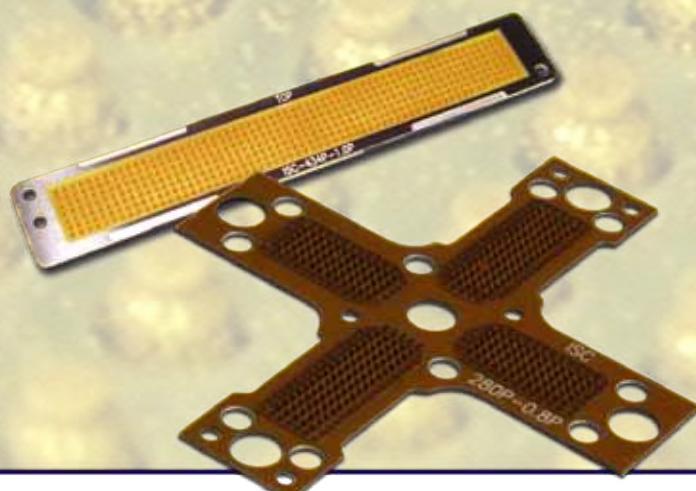
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# GUEST EDITORIAL



## SEMI 3D IC Standardization 2012 Update

By James Amano [SEMI]

**G**iven their potential for increased performance, smaller footprints, and reduced cost and power consumption, 3D IC technologies are now on the leading edge of innovation, with the industry poised to jump from concept to commercialization. However, multiple manufacturing challenges must first be solved, as 3D ICs' increased design and mechanical complexity can lead to increased manufacturing defects, as well as thermal management issues and signal interference. While 3D integration using through silicon vias (TSVs) promise a fundamental shift for current multi-chip integration and packaging approaches, cost-effective, high-volume manufacturing will be difficult to achieve without standardized equipment, materials, and processes.

The needs and opportunities for 3D IC manufacturing Standards were first explored at SEMICON West in 2010, and the first 3DS-IC SEMI Standards Committee was formed in North America in late 2010, with activities initially organized into three task forces (TFs): Thin Wafer Handling, Bonded Wafer Stacks, and Inspection and Metrology. Formation of a counterpart committee in Taiwan followed at SEMICON West 2011, and work is now underway in a 3DS-IC Testing TF and a Middle-End Process TF (Figure 1).

### Thin Wafer Handling TF

The Thin Wafer Handling TF aims to develop standards for reliable handling and shipping of thin wafers and dies (e.g., micro-pillar grid arrays, or MPGA) used in high-volume manufacturing

(HVM). As part of this effort, the TF will define thin wafer handling requirements including physical interfaces used in 3DS-IC manufacturing, as well as shipping requirements, including packaging, reliability, and other relevant criteria for both thin wafers and MPGAs.

The TF's first effort is SEMI Draft Document 5175, New Standard: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers. Current standards for shipping boxes, FOUPs, and FOSBs are not well-suited for the reliable storage and transportation of thin wafers and dice on tape frames used in 3DS-IC manufacturing. Wafer thicknesses of 30-200 $\mu\text{m}$  will need significant changes to the current design criteria of current wafer transport and storage containers. Draft Document 5175 aims to address the robust handling and shipping of thin wafers, including changes in securing the wafers (i.e., transportation/vibration and mechanical shock requirements).

### Inspection and Metrology TF

The Inspection and Metrology TF is working on standards to be used for measuring the properties of TSVs, bonded wafer stacks, and dies used in 3D IC manufacturing. Different technologies can measure various geometrical parameters of an individual TSV, or of an array of TSVs, such as pitch, top CD, top diameter, top area, depth, taper (or sidewall angle), bottom area, bottom CD, bottom diameter, and possibly others. However, it is currently difficult to compare and/or correlate results from the various measurement technologies for various TSV dimensions. In some cases, certain parameters may be described by similar names, but are actually different aspects of the TSV geometry. Clear and commonly accepted definitions are needed for efficient communication and to prevent misunderstanding between buyers and vendors of metrology equipment and manufacturing services. The goal of SEMI



Figure 1: SEMI 3DS-IC Standards organizational chart.



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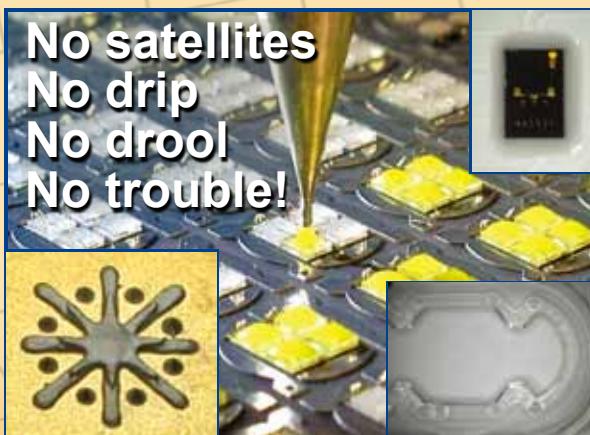
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Draft Document 5269, New Standard: Terminology for Through Silicon Via Metrology, is to provide a consistent terminology for the understanding and discussion of metrology issues important to TSVs. Additional standards under development include:

- SEMI Draft Document 5270: New Standard: Guide for Measuring Voids in Bonded Wafer Stacks,
- SEMI Draft Document 5409, New Standard: Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks, and
- SEMI Draft Document 5410, New Standard: Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures.

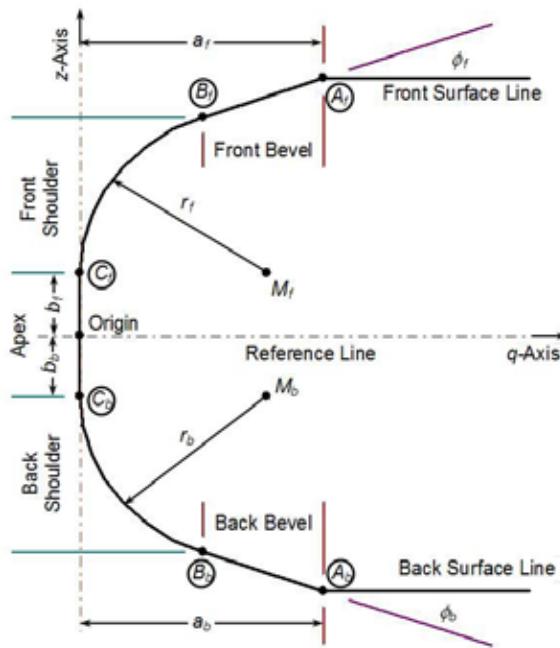
## Bonded Wafer Stacks TF

The Bonded Wafer Stacks TF is nearing completion in its development of SEMI Draft Document 5173, Guide for Describing Materials Properties and Test Methods for a 300 mm 3DS-IC Wafer Stack. Current wafer standards (e.g. SEMI M1) do not adequately address the needs of wafers used in 3D bonded wafer stacks for stacked integrated circuits (3DS-ICs). 3DS-IC processes may require starting materials — silicon and glass wafers — with different tolerances for dimension and material than those specified in SEMI M1 and SEMI M24. Further, in each step of a 3DS-IC process, the incoming material must be specified in terms of wafer dimension and materials present. Wafer thickness, edge bevel, notch, mass, bow/warp and diameters change when

wafer stacks are bonded, debonded, and when wafers incorporated into stacks are thinned. Further, these parameters will change for a single wafer stack during the process. This document provides the required properties of both silicon (“device”) wafers and glass (“carrier”) wafers to be used in 3DS-IC applications (**Figure 2**). Templates for describing bonded wafer stacks and processed wafers to be used in the bonding flow would be provided as well.

## Taiwan 3DS-IC Committee

Since its formation at SEMICON West in July 2011, the Taiwan 3DS-IC Committee has held three committee meetings to refine its discussions on testing and the middle-end process. Two TFs have now been officially chartered: The 3DS-IC Testing Task Force and the Middle-End TF. The 3DS-IC Testing Task Force was chartered to develop standards, guidelines, and/or specifications for electrical testing related activities used in 3DS-IC manufacturing for the ultimate goal of yield enhancement, with future activities



**Figure 2:** From SEMI Draft Document 5173: schematic drawing of a model edge profile illustrating the terms, symbols, and reference points used to describe the profile

planned for:

- Design for Test (DfT) such as test structures and placement;
- Test methodologies such as contact method and test procedures;
- Test fixtures such as probe card and probe interfaces, and
- Data mining test results

The Middle-End TF is looking at processes involving shared activities between wafer foundries and OSATs, including embedded via protrusion and vialed wafer thinning. Current work is focused on the middle-end process on wafers with or without TSVs including post-final metal temporary bonding, wafer thinning, TSV formation and reveal, micro-bumping, redistributed line formation and carrier de-bond.

Ballots for the above activities will be issued throughout 2012, and are just the beginning of this global, industry-wide effort. Over 160 technologists from industry, research institutes, and academia around the world have already joined the SEMI 3DS-IC Standards Committee and are at work on these critical standards. The committee and task forces will next be meeting at SEMICON West 2012 in July. If your company isn't involved yet, now's the time - participation in the SEMI Standards Program is free, but requires registration. If you are not yet a member, please register at: [www.semi.org/standardsmembership](http://www.semi.org/standardsmembership).

## About 3D IC Activities at SEMICON West

3D IC technology is in the spotlight at SEMICON West 2012, with technical sessions, keynote presentations, and exhibitors all dedicated to products, technologies, and solutions for 3DIC, including design, device fabrication, packaging, and test. For more information, visit: <http://semiconwest.org/Segments/3DIC>

*James Amano, Director, International Standards, SEMI, may be contacted at [jaman@semi.org](mailto:jaman@semi.org)*

# BUSINESS TRENDS



## Designing from the Outside In: Ultrabook™ Form Factor Drives Innovation

By Simon McElrea, *[Invensas Corporation]*

In the second half of the 1990s, the Internet and associated technologies started to seriously shape the way we communicate, both on a personal and professional level. In tandem with this, advances in mobile communications networks, devices, and signal robustness inexorably pushed us toward the ‘always on,’ high speed, instantaneous communication we take for granted today.

The past decade has seen a convergence of wireless connectivity and increasingly ubiquitous high-speed data technology that has spawned personalized content, opt-in applications and media-rich environments. Devices continue to get smaller, smarter, faster, and highly functional on multiple levels, which includes being fully portable, with access to content wherever we are through a multitude of devices.

### The rise of the Ultrabook™

Ultrabooks are the latest series of devices enabled by innovations in chip design, power management and connectivity; and combine high-end performance, instant connectivity and power-up, and rich feature sets in an ultra-thin, lightweight notebook format.

“Think of a Macbook Air that runs Windows” writes *Wall Street Journal* San Francisco Bureau Chief Don Clark in his April 4 blog entry titled *Intel Spares No Expense In New Ultrabook Ads.*<sup>1</sup> That, in a nutshell, is what the Ultrabook represents.

Championed by Intel, which last year made \$300M available to fund startups “working on technologies in line with the Ultrabook concept,” the Silicon Valley giant sees such potential for these

powerful yet lightweight devices that it has trademarked the name ‘Ultrabook’ and is putting additional resources behind promoting it in the company’s biggest campaign since Centrino in 2003.

In the PC domain, where Intel leads, manufacturers generally follow, and there has been no shortage of entrants to the Ultrabook market including HP, Dell, Lenovo, Asus, Samsung and Toshiba, and others. On April 17, 2012 Intel president and CEO Paul Otellini commented to analysts that he expects Ultrabooks — which currently range in price from \$1000 to just over \$2000 depending on specifications, and weigh an average 3lbs — to hit more mainstream pricing,

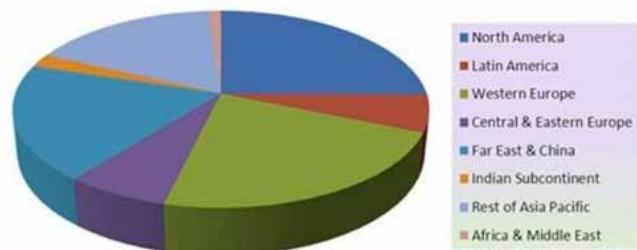
rumored to be <\$1000, by the summer. Otellini also stated that there are approximately 20 designs currently being shipped; a number Intel expects to rise to over 100 in the second half of 2012.

In an April 2012 editorial, *Ultrabooks to Hit 'Mainstream' Price Points*, EE Times’ Dylan McGrath reported that Beau Skonieczny, a computing analyst at Technology Business Research Inc. (TBR), said all major PC vendors are adopting the Ultrabook form factor without hesitation.<sup>2</sup>

According to www.ultrabooknews.com. Juniper Research predicts that 178M Ultrabooks will ship in 2016.<sup>3</sup> North American and Western Europe are expected to account for 90M units, and

sales are expected to really take off in 2014. At \$500/unit, that’s an \$89B market (**Figure 1**).

Looking ahead, the introduction of touchscreen technology into the Ultrabook market to offer tablet-style functionality will only increase the number of options available to consumers.



Source: Juniper Research

**Figure 1:** Worldwide annual Ultrabook shipments (m) split by 8 key regions in 2016.

### Technology Behind the Technology

Ultra responsive, ultra sleek, long lasting – these are the attributes that Intel is pushing on its website to promote Ultrabook. Specifically, Intel is actively marketing technologies such as Intel® Rapid Start Technology, which when used with an SSD drive, uses Flash storage to make the Ultrabook operational within seconds. Ultra-low power consumption in standby mode that extends battery life is another key feature, as is seamless connectivity to other devices through Intel® My WiFi technology.

Of course, these features are underpinned by advances at the component and printed circuit board (PCB) levels, so



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in looking at the ‘technology behind the technology,’ the design rules governing Ultrabook developments are necessitating advances in key performance areas that maintain the performance required, but do so in a suitable format and at a cost-effective price point.

One area that Intel has publicly discussed regarding Ultrabook design the adoption of standards for thinner, lighter batteries. This would accommodate both form factor considerations, as well as potentially drive down costs. “What are the advantages of adopting a thinner battery standard?” asks Edwin Kee at Ubergizmo, “For one, costs can be lowered due to an increase in the supply of batteries, which will end up as suitable for use in Ultrabooks, and computer manufacturers can just use off-the-shelf models. Intel’s ideal size for an Ultrabook battery would measure 60mm x 80mm as a standard, and (the company) hopes to see a diameter of just 16mm, which is 2mm thinner compared to what is normally used in notebooks.”<sup>4</sup>

While not as ‘visible’ a component as a battery, form factor considerations are driving innovation in memory packaging as well. A key design consideration for Ultrabook is the way in which memory is used in portable clients. The inch-thick Ultrabook cannot accommodate the small outline dual in-line memory module (SODIMM) DRAM that is standard in conventional notebooks, so memory is being soldered to the motherboard directly. Due to severe limitations on available space for the PCB, high density interconnect (HDI) technology was used for the PCBs in first generation devices. However, the need for HDI was primarily driven by layout considerations for the memory channel and overall form factor.

What became evident is the need for a multi-die DRAM packaging technology that can accommodate PCB design while miniaturizing the memory footprint.

So what would this optimized memory package look like? Multi-die face-down wirebond package technology is one solution that would achieve premium functionality in the smallest form factor at the lowest cost point for Ultrabooks and tablet computers (**Figure 2**). When compared to standard single die DRAM packages soldered to the motherboard, a multi-die face-down approach allows for:

- Smaller PCB area for memory
- Simple low-cost PCB: plated through hole standard process PCB vs. costly HDI build-up
- Co-support LPDDR3, DDR3x, DDR4, GDDR5: same PCB for either type of memory
- Lowest manufacturing cost/ die for multi-die DRAM packages

Enabling multi-chip scaling in a chip-scale package form factor offers a low-risk and low-cost technology platform. The package concept offers better electrical and thermal performance using standard wire bond process with fewer process steps, compared to conventional dual-die package technology. This approach delivers this memory capacity and performance in a miniature, soldered-down, ball grid array (BGA) package. Coupled with a versatile and efficient ballout, this package drives greatly simplified PCB designs while achieving



**Figure 2:** DIMM-in-a-package incorporating one typical product, the Quad Face Down (QFD™) package, can replace a single-sided SODIMM in a 16 x 16 x 1.0mm form factor, making it ideal for today's ultra-thin electronics.

a common test infrastructure for several DRAM technologies used in multi-die wide-word applications including DDR3, DDR4, LPDDR3 and GDDR5; a significant benefit to the memory maker.

A further benefit of optimizing memory packaging is that by moving to a simpler, non-HDI implementation, manufacturers have the potential to achieve BOM savings typically between \$10 and \$15 in PCB costs per system while reducing PCB prototyping time to five days from three weeks. Assuming typical PC product volumes, this represents several million dollars per year of savings.

## Conclusion

Clearly, the solutions to the design challenges faced by the proliferation of Ultrabooks are being addressed through inventive solutions. The bottom line for IDMs is that the aggressive portable electronics roadmaps demand not just evolutionary products to reduce size and increase performance, but revolutionary solutions that provide a radical simplification of the product design and the supply chain. The memory challenge goes well beyond providing the required capacity. It’s about creating solutions that significantly reduce motherboard size and complexity, while increasing battery size (and hence life), and then dealing with all the heat.

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*Simon McElrea, President and CEO, Invensas, may be contacted at smcelrea@invensas.com*

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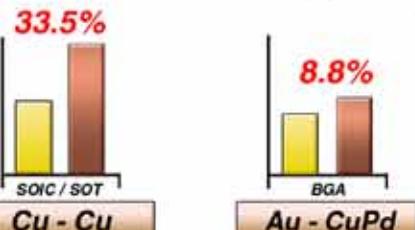
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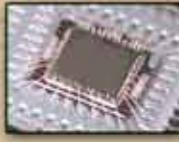
PBGA



QFP

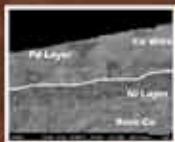
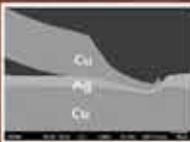


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# MARKET TRENDS

## Memory Market Update

By Adrienne Downey and Jim Feldhan [Semico Research]

The memory market is a tale of two products. In 2012, the DRAM manufacturers are facing another difficult year. DRAM revenues will increase by only 1.4% while DRAM units will grow by 11%. On the other hand, the NAND market, driven by the expanding mobile markets, will experience a good year. NAND revenue growth will increase 23.6% and units will expand by 33.5%.

Total memory industry capex will reach \$15.4B this year, or 25% of the total spending for the entire semiconductor industry. **Figure 1** shows memory spending by company and by memory type. Samsung is planning to spend a solid \$2B more than its next closest competitor, which is Hynix. Toshiba and SanDisk have placed the expansion of Fab 5 on hold through at least the remainder of 2012, so their capex will be at the low end of their targets. Semico believes improved conditions in the second half of the year could change their plans.

The DRAM market has been in trouble for some time. Companies have been reducing their exposure in the commodity PC DRAM market by moving into mobile, consumer, and server specialty DRAM, and by taking on foundry business to diversify their fabs. The DRAM makers in Taiwan are not profitable and are lagging in terms of process technology to Samsung, Hynix, Micron, and Elpida. Consolidation has been occurring over the years as the list of DRAM makers shrink, and the Taiwanese are ripe for consolidation.

The DRAM industry has been rocked by news of Elpida's bankruptcy. Serious bidders for all or portions of

Elpida included Micron, SK Hynix, Hony Capital and TPG (a Chinese and a US investment firm, respectively), and Toshiba, among others. Toshiba and SK Hynix are no longer in the running. Micron announced that Elpida has picked Micron to sponsor Elpida through its reorganization and to acquire the company. The deal is not done, but it seems to be moving along in that direction. Semico believes that this will benefit both companies because they serve some different customer segments, especially Elpida's mobile memory segment. Elpida and Micron currently rank third (12%) and fourth (10%) in terms of worldwide DRAM capacity. With Micron purchasing Elpida, and including Rexchip's output and Micron's share of Inotera's output, the combined company would control 38% of the total capacity, well in advance of Samsung at 26%.

**Figure 2** shows DRAM capacity by company. **Figure 3** depicts the relationships in the DRAM industry today. This will change with Micron's purchase

of Elpida. Currently Micron and Nanya have a 50/50 share of the capacity in their Inotera joint venture, which has 130K total wafers per month (WPM) capacity. DRAM from Inotera accounted for 43% of Micron's total gigabit production in 1QFY12, up from 25% in the 1QFY11. Inotera primarily provides DDR3 for the PC market to Micron.

Powerchip gave 9.3% share in Rexchip to Powertech in exchange for some debt relief, who in turn sold it to Kingston.

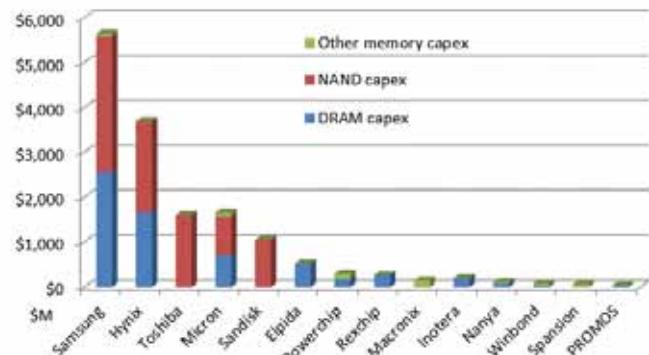


Figure 1. Memory Industry Capex (Source: Semico Research Corp.)

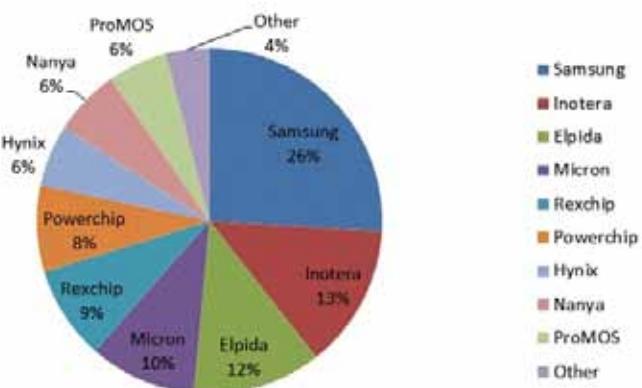


Figure 2. DRAM capacity by company. (Source: Semico Research Corp.)



Powerchip Technology and ProMOS Technologies are both among Elpida's DRAM manufacturing partners. Elpida and Promos had a DRAM foundry agreement where Elpida supplied process technology to ProMOS and ProMOS provided capacity at its 300mm fab.

In terms of NAND capacity, Samsung, Toshiba and Hynix make up 3/4 of the market with IMFlash adding another 14%. This is depicted in [Figure 4](#).

SanDisk and Toshiba see improving yields on 19nm NAND production, as

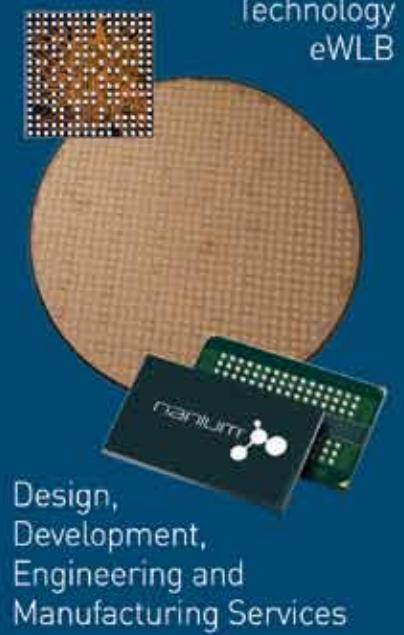
well as no spikes in consumer demand later this year. However, they do think that the second half will show improved demand and growth, especially for SSDs. The earliest that the expansion ramp of Fab 5 will restart is the beginning of 2013, with the decision on that to be made in the third quarter in time for equipment purchases to be made.

Samsung has some new NAND capacity coming online in the next two years, provided its project comes to fruition. The company has received permission to

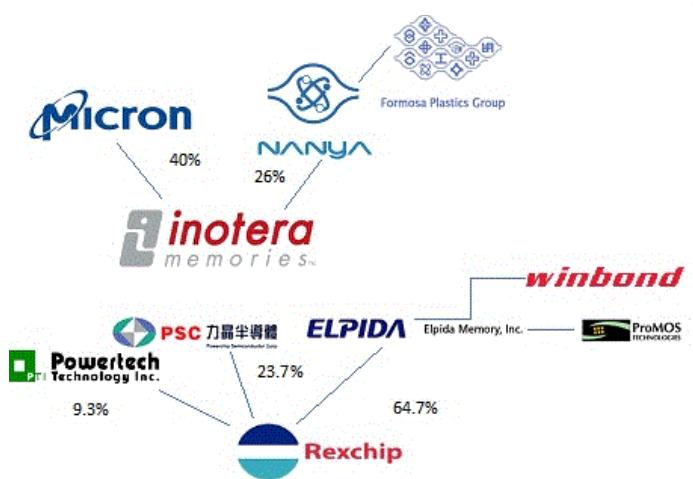
build a NAND fab in China. No location has been announced, but it is supposed to be in production by 2H2013, starting at 20nm, with a 100,000 wafer sorts per month (WSPM). Samsung's main concern with this project is preventing technology leaks, and it has been getting help from the Korean government with that. Samsung wants to build the NAND flash chip factory to be near the contract electronics manufacturers that make the world's smart phones and tablet computers.

## Semiconductor Packaging, Assembly and Test

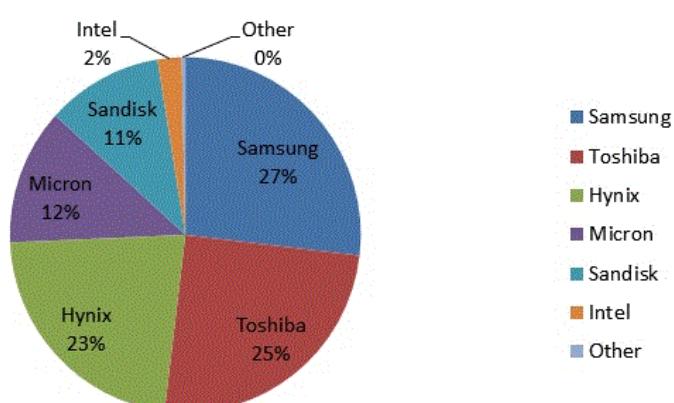
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**Figure 3.** DRAM industry tie-ups. (Source: Semico Research Corp.)



**Figure 4.** NAND Capacity. (Source: Semico Research Corp.)

*Adrienne Downey, Director of Manufacturing Research, Semico Research, may be contacted at [adrienned@semico.com](mailto:adrienned@semico.com); Jim Feldhan, CEO, Semico Research, may be contacted at [jimf@semico.com](mailto:jimf@semico.com).*

# INDUSTRY NEWS

## 3-D Integration and Technology Gathers Momentum at ECTC 2012

By Ronald J. Molnar [Az Tech Direct, LLC]

The 62nd annual Electronic Components and Technology Conference (ECTC) convened at the Sheraton San Diego Hotel and Marina on May 29 – June 1, 2012. By all measures, the event, considered by many to be the premier international conference on IC packaging, components, and microelectronic systems technology, was an outstanding success and lived up to its stellar reputation.

Although highly acclaimed for the quality of its nearly 350 technical presentations, the event has steadily increased the size of its exhibition area as well. The Technology Corner exhibition area was “sold out” this year as it grew to 81 exhibitors from 60 last year (a 35% increase)!

As a sign that the semiconductor market segment has recovered from the 2009 economic downturn, the conference has grown from 550 attendees in 2009 to 1,225 attendees in 2012 representing 26 countries. In fact, attendance grew more than 20% over last year alone – 2nd only to the 50th anniversary event held in 2000.

### Comments from Dave McCann, 2012 General Chair

“We had near-record attendance at

the 62nd Electronic Components and Technology Conference (ECTC). Our focus on cross-committee 3D/TSV MEMS sessions was very well timed to meet the need of our attendees, many of whom are looking at the barriers their companies are facing either in supplying products to their customers that continue to scale and provide memory bandwidth they need, or in the supply chain to deliver materials, tools, or assembly/test services for 3D/TSV products. Our attendees came to ECTC this year from 26 countries to learn the latest on all packaging-related technologies and to network with their colleagues. I think the attendance speaks for itself in measuring the effectiveness of the conference this year in delivering the content that our customers needed. We also had focused sessions on Interposers (2.5D) and MEMS, panel sessions on the role of the Packaging Foundry, on the Photonics Markets

and Technologies, Power Electronics, and Coreless Substrates, in addition to the sessions on new technology from Advanced Packaging, Interconnections, Emerging Technologies, Assembly & Manufacturing Technology, Electronic Components & RF,



S. W. Ricky Lee, President of IEEE CPMT Society, addresses the annual CPMT Luncheon

Materials & Processing, Modeling and Simulation, Applied Reliability, and Optoelectronics fields. Next year we are looking forward to how to integrate additional leading edge cross-committee technologies such as Optical Interconnect.”

### Highlights of the Conference

Nearly 360 registrants attended 16 Professional Development Courses to kick-off the conference. The PDC program included six new courses this year.

One-fourth of the 36 technical sessions dealt with various aspects



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Wolfgang Sauter



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of 3D packaging technology. The most popular session by far was Session 1 titled “3D Interconnect: Bonding and Assembly”. More than 200 people attended each of the 7 presentations in this session.

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ECTC 2012 Outdoor Gala Reception

Two other well-attended presentations were “Coreless Substrate Technology Investigation for Ultra-Thin CPU BGA Packaging” by Intel Corporation in Session 21: Flip Chip Technologies, and “2.5D and 3D Technology Challenges and Test Vehicle Demonstrations” by IBM Corporation in Session 25: 3D Integration.

The annual ECTC Luncheon featured a stimulating keynote speech by Gregg Bartlett, CTO of GLOBALFOUNDRIES, on “Bridging the Gap between Silicon and Packaging.” He described several system-level performance and bandwidth challenges and called for a new collaborative model for silicon and package co-design as we move beyond the 28 nm node.

Five poster sessions held in the Technology Corner exhibit area, including one student poster session, covered 95 different interactive presentations.

Four panelist discussions addressed (1) the role of packaging foundries with respect to next generation packaging and integration, (2) expanding markets and emerging technologies in the area of photonics, (3) the booming market for power electronics, and (4) advanced coreless package substrate and material technologies.

A number of ECTC and CPMT awards were presented for best 2011 session, poster, and transactions papers. In addition, a number of individuals were honored by the IEEE CPMT Society for their service to the industry. Receiving the highest honor, the 2012 Technology Award, was Mauro J. Walker for advancing electronic manufacturing technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia and professional organization.

## Mark your Calendar for ECTC 2013

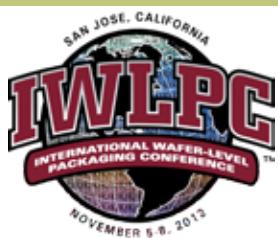
Planning is already underway for ECTC 2013 which will be held May 28 – 31, 2013 at the Cosmopolitan Hotel in Las Vegas, NV. The first Call-for-Papers has been issued and abstracts must be received by October 8, 2012.

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## Final Platinum Sponsor and Program Announced for IWLPC 2012

The SMTA and Chip Scale Review, co-sponsors of the 9th Annual International Wafer-Level Packaging Conference and Tabletop Exhibition, scheduled to take place November 5-8 2012, in San Jose CA, are pleased to announce that Invensas

Corporation has joined the distinguished list of Platinum Sponsors.

Invensas Corporation enables tomorrow's semiconductor technologies by inventing, productizing and acquiring

strategic intellectual property (IP) to solve critical roadmap problems. Focus areas include circuitry design, memory modules, packaging, 3-D systems, and advanced interconnect technologies, targeting the mobile, storage and consumer electronics sectors.

In addition to Platinum, Gold and Silver sponsorship opportunities, there are many ways to show your support for IWLPC while providing your company with creative ways to promote your brand. For example, sponsor lunch, a refreshment break or a reception or be the company to thank for free WiFi access.

The possibilities are almost endless.

### Program Announced

The conference will include three tracks with two days of technical paper presentations covering: Wafer Level Packaging; 3-D (Stacked) Packaging; and MEMS Packaging. Attendees will gain the latest knowledge with eight application-oriented tutorials, 10 technical sessions, two expert panel discussions, and a keynote presentation from John Ellis, bestselling author of 'Dormant Curse,' titled "A Trojan Chip in Your Smartphone? It's Coming..."

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# What's New

## Invensas PoP Technology offers a Bridge to Wide I/O

In an effort to bridge the gap between high performance, low power needs of today's consumer electronics and the availability of a Wide I/O TSV solution, Invensas Corp, a wholly-owned subsidiary of Tessera Technologies, has introduced the bond via array package on package (or BVA PoP), which reportedly "delivers performance required by mobile OEMs while preserving the proven infrastructure and business model of traditional package-on-package (PoP)." According to company CEO and president, Simon McElrea, BVA is a technology that can be used "right now" to achieve performance benefits that otherwise will have to wait until 2016 when wide I/O TSV will be ready.

BVA is an ultra-high I/O packaging alternative to wide-I/O through silicon via (TSV) that delivers the performance required by mobile OEMs while preserving the proven infrastructure and business

model of traditional package-on-package (PoP). The technology features a novel method of interconnect that replaces either solder ball stacking or solder filled laser vias as the method of connecting the top memory package to the bottom logic package. Instead, copper wire bonding processes are used to create free standing pins that are then overmolded for stability, with the ends exposed to create the interconnect to the top package. A dimple in the mold surrounding the exposed pin helps the solder ball from the top package stay in place. The result is a PoP configuration that is 0.300.2mm pitch with 432-1512 interconnects vs. 0.65-0.5mm pitch and 168 interconnects of a traditional solder ball stacked PoP or the 0.5-0.4mm pitch and 240 interconnects achievable in a solder filled via PoP (based on a 14x14mm package). Because BVA PoP utilizes the existing package assembly and surface mount technology (SMT) infrastructure, it does not require a large capital investment

and can be quickly adopted to provide increased bandwidth at low cost.

"With this new approach we're taking PoP from 240 pins to 1,200 pins. In doing so, BVA significantly pushes out the need for 3D-TSV. At the same time, it renders solder via obsolete as it is able to cost-effectively scale to ultra-high I/O," continued McElrea.

BVA PoP is ideally suited for applications processor plus memory PoP stacks. By increasing processor to memory bandwidth, BVA PoP enables higher resolution, faster frame rate video streaming, faster search, higher resolution multi-screen, multi-application operation, more life-like gaming and a whole new generation of high-resolution 3D applications.

## Ziptronix Pursues Lower-Cost 3D Memory With Wafer Bonding and Interconnect

A new customer collaboration at Ziptronix Inc., developer of direct

(continued on Page 55)

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# TSV MEOL: End of the Middle, or Middle of the End?

By Scott Jewler [Powertech Technology, Inc]

The term TSV ‘middle-end-of-line’ (MEOL) has come into wide usage in the semiconductor industry and like ‘3DIC’ it is an acronym that has different interpretations under various circumstances and usages. Across the industry, TSV MEOL flows are being widely developed and industrialized for volume production. However, for the most part these flows are composed of unit processes and tools that are relatively mature. As questions about feasibility and reliability of TSV-based interconnect give way to pressures for wider market adoption by driving down costs, industry focus will intensify on these unit processes and innovators will introduce new methods and tools to form the necessary structures more efficiently. This article will define the term ‘MEOL’ as used in relation to TSV and introduce several of the most common flows. It will highlight some of the key unit processes and raise some of the more significant technical and cost challenges associated with these.

## The Hierarchy of Ends

Figure 1 provides a simple hierarchy of ends as it relates to TSV MEOL. In the most general case (I), a semiconductor product is said to have been fabricated in a front-end wafer fab that outputs a multitude of circuits in the form of a wafer, which are then probed, assembled, and tested in a back-end assembly and test factory that outputs a finished component. In this case the ‘front-end’ and the ‘back-end’ are clearly differentiated, and this model of thinking as well as organizing resources was efficient and effective through about the 130nm node. Front-end and back-end engineers and factories were physically and organizationally disparate and interaction was limited.

Isolated in their own industry segments, the second level (II) of the hierarchy of naming came into common use. Since there was limited interaction between front-end and back-end people at this time the similarities in naming did not lead to much confusion or concern.

The introduction of copper metallization and low- $k$  dielectrics in the front-end (wafer fab) back-end-of-line (BEOL) at the 130nm node led to the recognition that the back-end (assembly process) front-of-line (FOL) (pre-encapsulation processes) needed to be co-engineered with the front-end to provide reliable interconnect as dimensional scaling of devices continued to progress.

At this point someone must have realized that naming conventions in the industry were headed down a dark and confusing path but probably decided that it was too late to do anything about.

Now enter TSV which enables the third (III) level of the hierarchy. Luckily via-first is being widely abandoned by the industry leaving behind only via middle (VM) and Via last (VL) to further

complicate this naming structure. As demonstrated in level (II), the wafer fabrication process is often segregated into three areas. In front-end-of-line (FEOL), silicon substrates are input into the line. Trench isolation is typically formed and then dopants implanted and annealed to form junction. Gate material is added to form transistors. In the wafer fab MEOL, contact metal is formed on the gate, source, and drain of the transistors to enable reliable and low resistance connections to metal lines that will be fabricated in the BEOL.

In VM process flows, TSV’s formation typically begins in the front-end (wafer fab) MEOL process. Via holes are formed from the top side of the wafer typically by deep reactive ion etching (DRIE). Laser drilling may also be utilized in some cases. The dimensions of these holes (perhaps 2-10µm in diameter and 40µm or more in depth) are very large relative to the minimum feature size of the FEOL features at 28nm and below. The via holes are typically then lined with an insulating material using chemical vapor deposition (CVD). Seed

## The Hierarchy of Ends

I	Wafer Fabrication Semiconductor Front End				Packaging and Test Semiconductor Back End			
II	Transistors FEOL	Contact MEOL	Metal Layers BEOL	Circuit Probe	Assembly FOL	Assembly EOL	Final Test	
III (VM)	Transistors FEOL	Contact & TSV MEOL	Metal Layers BEOL	Circuit Probe	TSV(VM) MEOL	Ass'y FOL	Ass'y EOL	Final Test
III (VL)	Transistors FEOL	Contact MEOL	Metal Layers BEOL	Circuit Probe	TSV(VL) MEOL	Ass'y FOL	Ass'y EOL	Final Test

Figure 1: The hierarchy of ends

metal is sputtered into the hole and it is then filled by electrochemical deposition (ECD) or electroplating.

These via middle structures remain embedded in the devices as wafers continue through front-end BEOL or BEOL processing to add metal interconnect layers. Finished wafers ship out of the wafer fab and typically the circuits are electrically probed to identify some reject units. These wafers next enter the back-end MEOL.

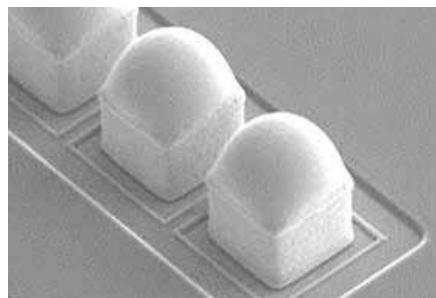
The attractiveness of VL is that the front-end wafer fabrication generally remains unchanged by the adoption of TSV. From a design standpoint, via last requires a target pad on which the via will terminate, typically either in contact or metal layer one. VL may also require specific alignment targets to enable alignment between the structures on the top side of the wafer and the positioning of vias formed from the back side. Wafers intended for VL typically exit the wafer fab and move to a back-end MEOL process line.

## MEOL Processes

**Front Side Bump Formation:** Regardless of VL or VM, the first set of MEOL process steps usually relate to forming bumps on the top side of the wafer. This process is similar to conventional wafer bumping. The wafer is inspected and cleaned and then coated with photo resist material. The pattern for bumping is typically exposed using I-line photolithography and then the resist material is developed and cleaned. Layers of under bump metal (UBM) are sputtered onto the surface of the wafer using physical vapor deposition (PVD). The UBM structure typically includes at least a barrier metal to prevent migration between the pad metal on the wafer and the bump itself. It also typically includes a seed layer that is used as a conductor for subsequent electrochemical deposition (ECD) or plating processes.

After depositing the seed metal, bumps are usually formed by ECD. Bumps may be composed entirely of solderable material, however smaller diameter bumps with higher standoff are typically achieved through a stack of a metal such

as copper with a solder-able cap on top. Some processes used techniques other than solder interconnect for chip-to-chip stacking, in which case a non-oxidizing cap such as gold may be applied. **Figure 2** shows a typical top side bump.



**Figure 2:** Fine pitch copper pillar bumps of wafer top side

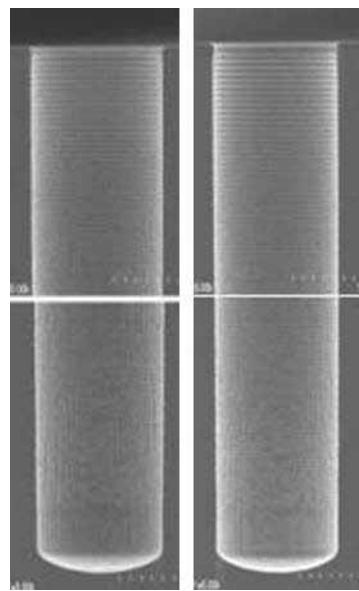
**Wafer Support System:** The next process steps in MEOL relate to mounting the wafer onto a support substrate to allow thinning and further processing. There are a number of variations to this set of processes. Both glass and silicon substrates are utilized. In some cases, the substrate size is that of a standard 300mm wafer, in which case the actual process wafer may be slightly trimmed to make sure that the stack does not exceed the target diameter. In some cases, substrates slightly larger than 300mm are applied and wafer handling on subsequent processes is adjusted to accommodate these larger size wafer stacks.

The wafer is mounted onto the substrate using an adhesive. The adhesive and base material must have sufficient thickness and appropriate mechanical properties to firmly attach to the bumped surface of the wafer. The adhesive needs to have release properties that can be activated by heat or light so that the thinned wafer can be removed during later processing without damage. Most critically, the stack of substrate, adhesive, and wafer need to exhibit a minimal amount of warpage. Since the ultimate goal of this series of processes is to prepare planer bumps for die stacking, any warpage at this point makes the later challenges significantly more difficult.

**TSV Formation (VL) or Reveal (VM):** At this point in the MEOL flow, the processes for VL and VM diverge. In

both cases, the first step is wafer thinning. Thinning is typically accomplished by a combination of mechanical grinding with some form of polishing. In the VL case, the wafer is thinned to the final thickness. In VM, mechanical thinning typically stops prior to reaching the embedded vias inside the wafer.

For VL, via holes are typically formed by etching using DRIE or by laser drilling. An insulation layer is formed inside the via hole most commonly using chemical vapor deposition (CVD). The quality of this insulation layer is of significant importance. The quality of the insulation material and its thickness must be tightly controlled. At the bottom of the via, the insulation must be opened to allow the conductive via fill material to contact the underlying metal. **Figure 3** shows a typical via hole prior to insulation deposition.



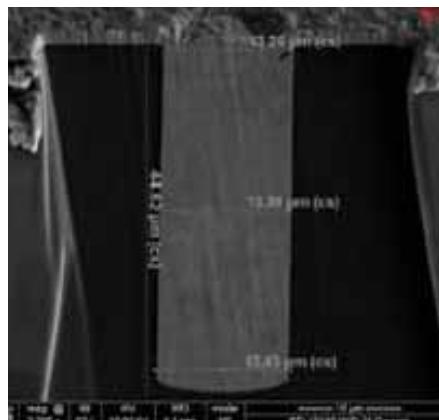
**Figure 3:** Via last holes formed by DRIE

Once the barrier has been deposited, a seed metal is deposited into the hole to enable subsequent filling of the via using ECD. PVD is typically utilized to deposit the seed metal, however since the surface is not planer in this case, chamber design and process conditions must be optimized to deposit a complete and even layer of seed metal.

Vias are then typically filled with metal using ECD. For larger diameter vias, such as those used in image sensors, conformal

coating of the via side walls is applied rather than completely filling. Smaller vias are typically filled. Plating chemistry and fill speed are big contributors to MEOL costs and are an area that will see continuous focus on improvements for some time. **Figure 4** shows a completed filled via using VL technology.

For VM, after preliminary wafer thinning, the via tips (often called ‘nail heads’) are exposed by chemical etching.



**Figure 4:** A filled TSV

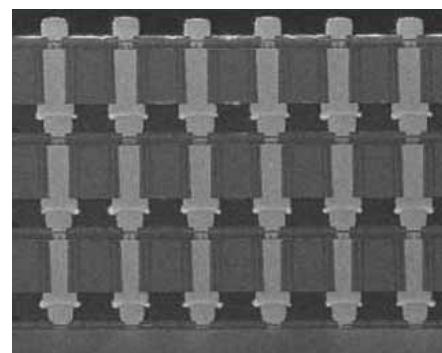
Here the planarity of the wafer and the via depth control from the front end formation process are critical. Although a process to directly make the surface planer is desirable, concerns about via fill material contaminating the back side of the wafer are significant. For this reason, a protective material may be deposited over the wafer surface and nail heads prior to making the surface planer using chemical mechanical planarization (CMP) or an alternate process. The process of exposing the via tips and making the wafer surface planer is a significant MEOL cost driver for VM. A variety of alternate techniques to accomplish the required structure are being studied.

At this point, the process flow for VM and VL again converge. Wafer bumps on the wafer backside are formed in a similar manner to the bumps formed at the beginning of the MEOL flow on the top side of the wafer. Compatibility between the top side bump metallurgy and the bottom side metallurgy must be

considered especially in the case where wafers from different MEOL sources will be later stacked into 3DICs. A 3DIC stack example is shown in **Figure 5**.

### Back-End MEOL – Fab or Assembly?

One of the most contentious topics at industry meetings recently has been whether or not TSV MEOL belongs inside the wafer fab or assembly factories. The arguments for putting back-end MEOL in the wafer fab tend to be that the processes are more



**Figure 5:** Stacked die with TSV interconnect

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similar to traditional fab processes than assembly processes, that the technology and investment is too difficult for the outsourced semiconductor assembly and test service providers (OSATs), and that only through engineering collaboration between the front-end and back-end MEOL can 3DIC integration be successful.

Most of the OSATs, with a fairly short target cycle between capability development and production have been relatively silent on this topic. They argue that integration of chips from different suppliers will continue to be accomplished in the OSAT industry and that the technical capability and financial resources exist to make this a reality.

Like the polarization of many topics in the world these days, there are elements of truth in both arguments. While tools like CMP and CVD are more typically found in wafer fabs than assembly factories, the actual process chambers used for silicon processing and TSV MEOL can differ significantly.

Front end engineers visiting a back end MEOL will see a lot of familiar equipment handling units and may assume that they are looking at front end fab tools. The reality is that TSV structures, accuracies, and cost targets are significantly different from front end requirements. As a result, the process parts of the tool, typically the chambers, are rapidly diverging between traditional fab and TSV MEOL equipment.

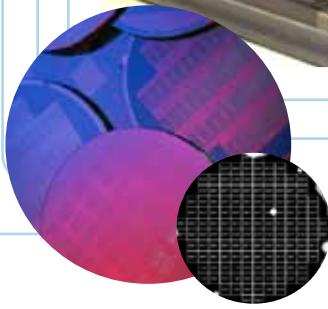
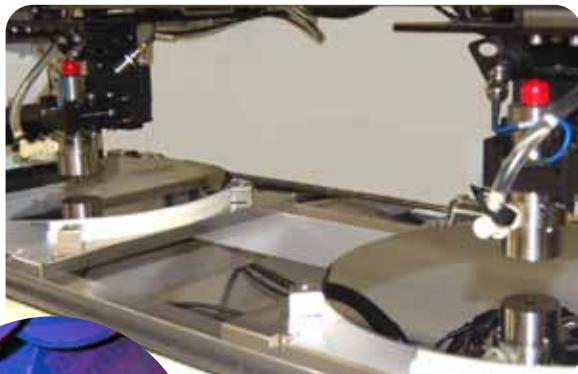
Collaboration between front-end and back-end process engineers is certainly a requirement to enable successful deployment of 3DIC, but so is the ability to have true pure play integration of devices from different fabs. Proponents of both fab and assembly TSV MEOL both raise valid points, however they generally fail to address how they will overcome their disadvantages. The OSATs need to figure out how to have effective engineering collaboration with the front-end fabs and the foundries need to find a way to get competitors to ship them wafers for integration into 3DICs.

Both problems are formidable but achievable.

The last issue is cost and here I have some specific bias. If you assume that both the OSATs and foundries will build similar factories in similar regions with similar tools, you can argue that the direct manufacturing cost or cost of goods sold will be the same regardless of which entity does the work. The difference is overhead and shareholders tolerance for gross margins and earnings. Here I think that the OSATs have a distinct advantage. With their overhead structure and R&D budgets, they will likely make an acceptable return on investment (ROI) in this business at gross margins 20% less than what the foundries will require to have acceptable results. Although this may not drive the early adoption of this technology, it will certainly be a factor once the volume begins to expand. 

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# Sub-surface Microscopies for 3D Interconnect Process and Characterization Metrology

By Lay Wai Kong, Victor Vartanian, Andy C. Rudack, Klaus Hummler, and Alain C. Diebold  
[SEMATECH, GlobalFoundries, and CNSE]

The rapid development of 3D IC stacking technology is driving advances in microscopy methods. Overlay alignment measurements before wafer bonding, defect inspection after wafer bonding, and void inspection after copper plating are challenging due to the need to image through silicon or copper. Since conventional microscopy of 3D IC structures is challenged by the opaque nature of silicon in the visible portion of the electromagnetic spectrum, sub-surface imaging techniques are needed.

**Figure 1** illustrates the abilities of different wavelengths in the electromagnetic and acoustic spectra to penetrate bonded wafers with TSVs. Scanning acoustic microscopy (SAM) and infrared microscopy (IR) provide a means of “looking through” silicon when other microscopy techniques based on visible wavelengths fail. IR and acoustic microscopes are not only used by material

science researchers, but also as in-line metrology tools for defect and overlay inspection at the bonded wafer interface, while high resolution lab-based X-ray computed tomography (XCT) is used to detect voids in metal TSVs. This article covers several analytical techniques using electromagnetic and acoustic sub-surface imaging for process and quality control. The current status of SAM, IR microscopy, and X-ray microscopy, complemented by techniques for microstructure characterization, is discussed in terms of their application to process metrology and failure analysis in 3D IC integration.

## Acoustic and IR Microscopy of Bonded Wafers Interface Inspection

**Acoustic Microscopy:** Improper bonding can leave a trapped pocket or void of highly reflective material that SAM can easily detect with its ultrasonic transducer. The void does not transmit any ultrasound, and the reflected peak

is easily distinguished as a defect at the interface of bonded wafer pairs. SAM is somewhat limited by its resolution as a patterned wafer defect detection tool; its transducer with frequency at 110MHz can achieve only  $\sim 60\mu\text{m}$  resolution. However, it is particularly useful when examining bonded blanket wafers.

A SAM works on the principle of propagation and reflection of ultrasonic waves at interfaces where acoustic impedance changes.<sup>1,2</sup> An acoustic impedance mismatch at the boundary between two materials causes a portion of a sound wave to reflect. The intensity of the reflected wave increases as the mismatch in acoustic impedance increases. A coupling medium is needed to facilitate the transmission of ultrasonic energy from the transducer into the specimen. Compared to air, a coupling medium like water transmits more sound energy into the specimen so that a usable ultrasonic signal can be obtained.

**Figure 2** shows an elastic material (specimen) that is immersed in a coupling medium (water) and a SAM piezoelectric transducer, which transmits and receives longitudinal waves. As the transducer directs the initial ultrasound wave

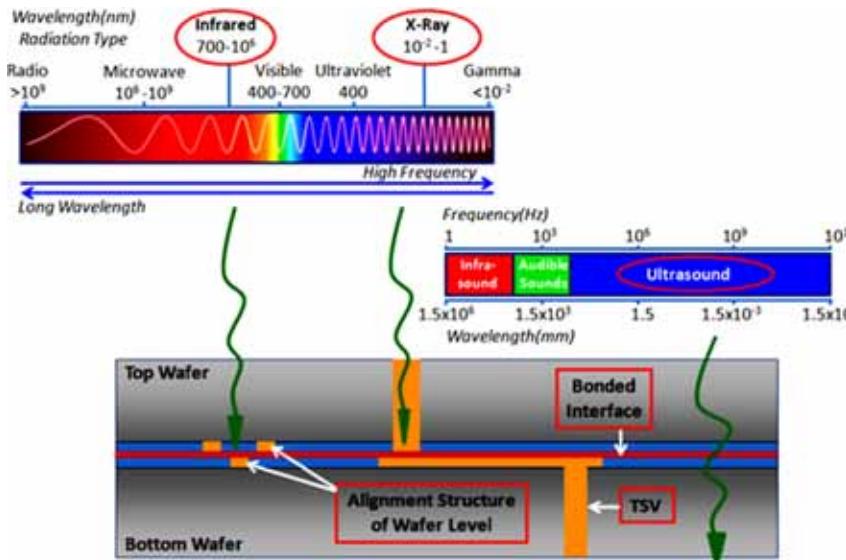


Figure 1: Sub-surface imaging techniques at various wavelengths.

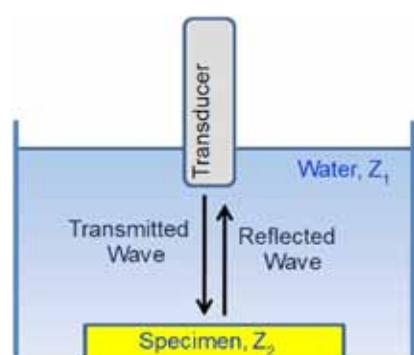
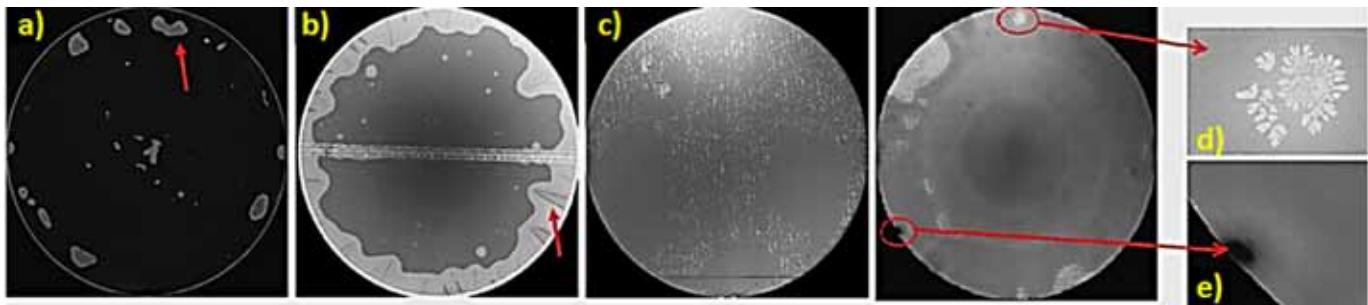


Figure 2: Transmission and reflection wave from transducer.



**Figure 3a-e:** Different blanket bonded wafers defects inspected by SAM.

towards the specimen, ultrasound travels in water as a longitudinal wave before being refracted by the lens. This initial ultrasound wave carries the maximum wave energy generated by the transducer and propagates until it reaches the boundary between the water and specimen. At this boundary, the acoustic impedance of water,  $Z_1$ , is different from the acoustic impedance of specimen,  $Z_2$ , due to the change in material density and the velocity of sound in different materials. Part of this initial wave is reflected from the boundary and received by the transducer, while part of it continues to propagate through the specimen until it reaches another boundary where acoustic impedance once again changes. By thinning the top wafer in a bonded wafer pair, higher frequency with shorter focal length transducers can be used to improve the resolution.

Many different defects can be formed during the wafer bonding process. **Figure 3a** shows the interface of copper-bonded wafer pairs where voids are shown in bright contrast. SAM can determine whether a coating defect due to insufficient bonding adhesive created the pie-slice defect shown in **Figure 3b**. A wafer pair bonded by BCB adhesive is also shown in **Figure 3c** and **Figure 3d**. In **Figure 3c**, small voids can be seen over the entire bonded wafer pair interface, which are attributed to bubbles outgassing

during the adhesive curing process. The bonded wafer pair shown in **Figure 3d** also exhibits dendrite defects, which are formed during the heating and cooling steps of the BCB adhesive process. These crystalline dendrite formations clearly point to problems during bonding. Finally, a “kissing” bond defect as shown in **Figure 3e** occurs when the bonded wafers are physically touching, without bonding material between them.

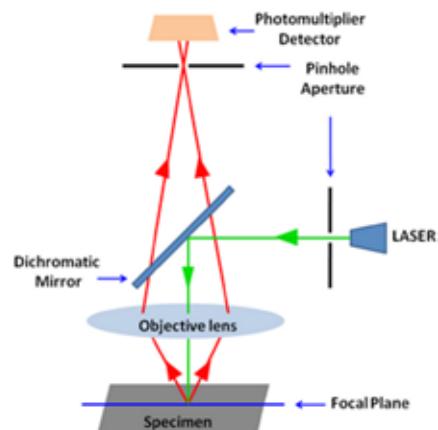
### IR Microscopy

A simplified optical system for a confocal infrared (IR) laser scanning microscope is shown in **Figure 4**. The laser provides intense excitation light, which passes through a pinhole aperture and reaches the dichromatic mirror. The dichromatic mirror functions as a beamsplitter, reflecting excited light toward the specimen and allowing the light emitted from the specimen to pass through it before reaching the detector.

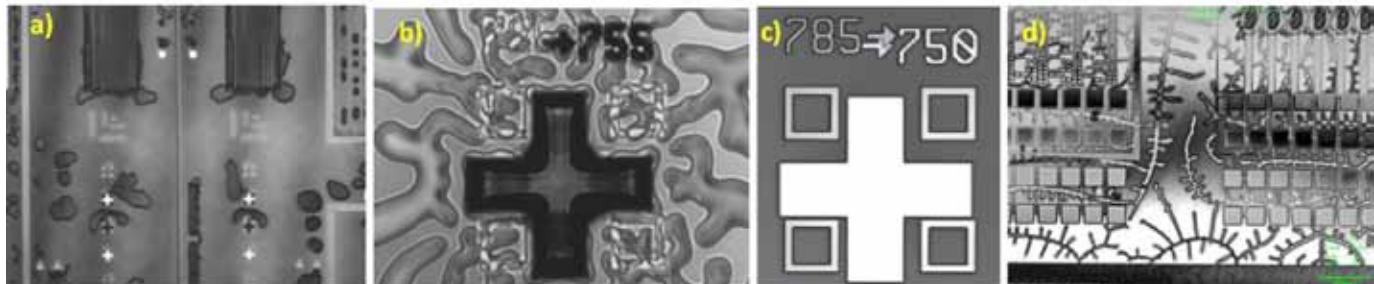
In conventional IR microscopy, all the light is emitted from the specimen into a photomultiplier, while in a confocal microscope only in-focus emitted light is collected by the detector. Another pinhole placed in front of the detector, which is conjugate to the focal point of the lens, blocks most of the out-of-focus light allowing the in-focus light to pass through and be collected by the detector. The

resulting image formed by the out-of-focus light is significantly more attenuated than the image formed by the in-focus light.<sup>3</sup>

Infrared is useful for “looking through” silicon at the interface of the bonded wafer pairs, as silicon is transparent to 1310nm IR light. The IR micrographs in **Figure 5a** show incomplete bonding material coverage over the wafer topography. In **Figure 5b**, bonding material flowing into an over-etched alignment structure causes the defect pattern around the structure. Misalignment of the bonded wafers can be measured using overlay structures of the top (cross) and bottom (box) wafers, shown in **Figure 5c**. Dendritic structures as seen by IR are displayed in **Figure 5d**. All of these defects can be attributed to



**Figure 4:** A simplified diagram showing a confocal IR laser scanning microscope.



**Figure 5a-d:** Different patterned bonded wafer defects inspected by an IR microscope.

an out-of-control process. IR microscopy provides feedback on actions needed to correct the process tool.

### X-ray Microscopy for TSV Void Inspection

Achieving nanoscale resolution with transmission X-rays in a laboratory source through conventional X-ray point projection is not very practical. X-rays with a refractive index close to 1 are weakly refracted by optical lenses. Thus, a different technique is required to focus the X-ray to achieve high-resolution images. A Fresnel zone plate is implemented that uses diffraction rather than refraction to focus the X-rays so that the propagated rays are not altered at the boundary between media of different densities, but are instead bent around the corners of the zone ring. By far the most common imaging lenses in industrial XCT systems and synchrotron TXM are micro-Fresnel zone plates ( $\mu$ FZP), so named because their overall dimensions typically do not exceed 1 mm.<sup>4</sup>

The beamline of a X-ray tomography microscope (nanoXCT) system is illustrated in Figure 6.<sup>5</sup> Incident X-rays at 8 keV are initially focused by a reflective capillary optic or condenser zone plate, designed to condense X-rays to a small spot on the sample.<sup>6</sup> The lens is often made with a blocking ring in the center, which illuminates the sample with a partially coherent hollow cone beam. After transmission through the sample, the rays begin to diverge. A diffractive focusing optic (i.e., a Fresnel zone plate) is located about 20mm past the sample, capturing the diverging rays and focusing the transmitted image of the sample several hundred millimeters downstream.<sup>7</sup> The X-rays are then converted to a visible light image by a scintillating crystal and finally captured by a high resolution charge-coupled device (CCD) detector.<sup>8</sup>

The TSVs shown in Figure 7 are focused ion beam (FIB) cross sections of (a)  $\sim 4 \times 26\mu\text{m}$  and (b)  $\sim 5 \times 27\mu\text{m}$  TSV arrays with intentional voids. The TSV arrays underwent reactive ion etching (RIE) followed by liner and barrier deposition using plasma-enhanced chemical vapor deposition (PECVD)

and physical vapor deposition (PVD), respectively. Finally, the  $4\mu\text{m}$  TSVs were electrochemically deposited with copper so that Cu did not completely fill the bottom of the TSVs. The TSVs were filled from top

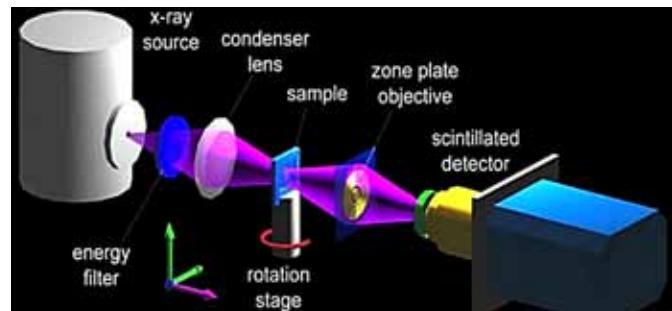


Figure 6: NanoXCT beamline.

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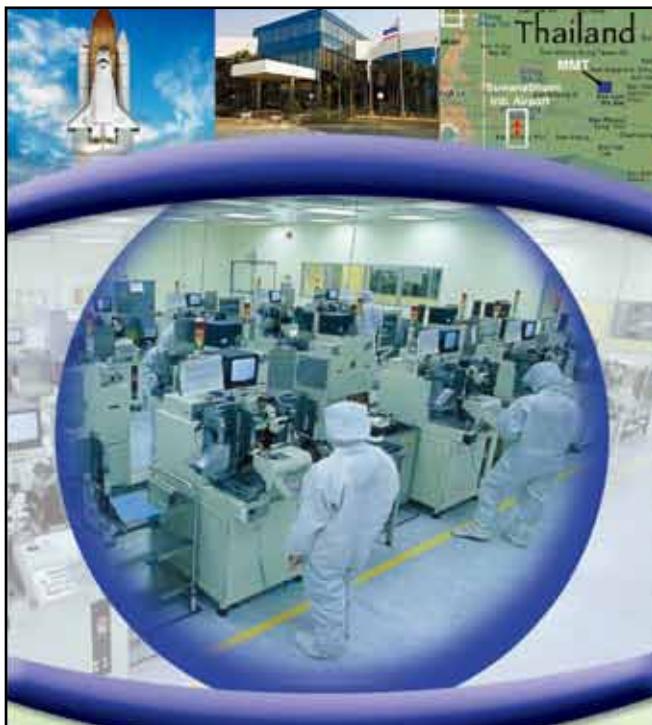
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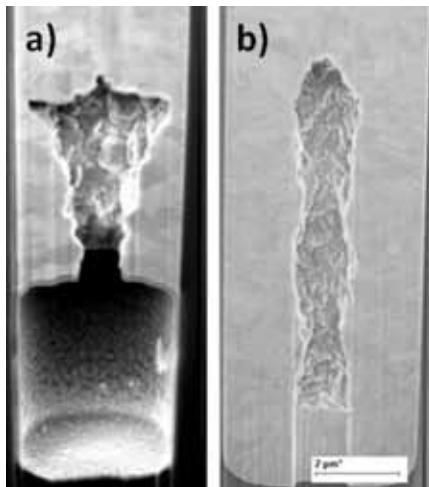
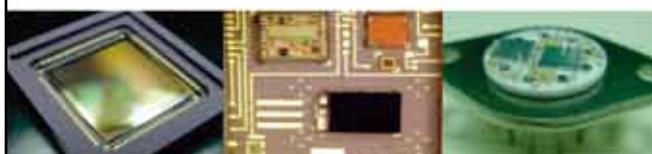
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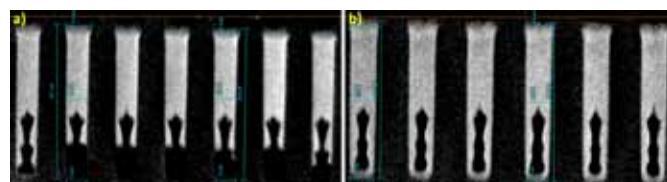
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**Figure 7:** SEM images of 4µm (a) and 5µm (b) TSV arrays with intentional voids.

polishing method, the back of the wafer was polished manually on diamond sandpaper 77µm to ~100µm thick. Finally, the wafer was polished to ~50µm thick using a dimple grinder with SiC diamond paste (particle size: 1µm) applied to the dimpling wheel. The entire TSV array remained in the piece of ~50µm thick wafer after non-destructive preparation.

Shown in **Figure 8** are the X-ray micrographs generated by nanoXCT from two TSV arrays embedded in pieces of ~50µm wafers. These ~4 x 26µm and ~5 x 27µm TSV arrays were fabricated with intentional defects as previously described. The piece of wafer was attached to a rotating sample stage. The 8keV X-ray was condensed before being focused on the sample. The sample was continuously exposed to the X-ray for 20 hours, during which time the sample was rotated from -70° to +70° with 0.44° angle steps. A total of 321 images were collected at an average of ~3.7 minutes per exposure for each projection. Subsequent image reconstruction generated 3D structural information, allowing multi-directional visualization of TSVs in the XY, YZ, and XZ planes. The defects observed in these TSVs are shown to be (a) incomplete filling at the bottom of the 4µm TSV array and (b) large voids at the bottom of the 5µm TSV array, which correspond to the FIB images in **Figure 7**.



**Figure 8:** (a) Incomplete filling at the bottom of 4µm TSVs and (b) voids found at the center of 5µm TSVs, respectively.

### Summary

SAM is found to be most useful as a bonded wafers interface defect detection tool. Thinning the top wafer is expected to improve resolution because higher frequency, shorter focal length transducers can be used. However, SAM does not have the

necessary resolution to be useful for overlay metrology. Overlay metrology can be easily done by confocal IR microscopy. The confocal IR microscope is also useful for inspecting defects within bonded wafer pairs. We have also shown the usefulness of lab-based X-ray microscopy for detecting voids in copper-filled TSVs. Although X-ray microscopy and tomography, and particularly the nanoXCT technique, are able to visualize sub-100nm voids without physically cross sectioning the TSV, they are limited to small sample sizes and sample preparation is required. Further development of the X-ray microscopy, however, should improve its applicability to TSV metrology with the ultimate goal of an in-line inspection tool. <sup>8</sup>

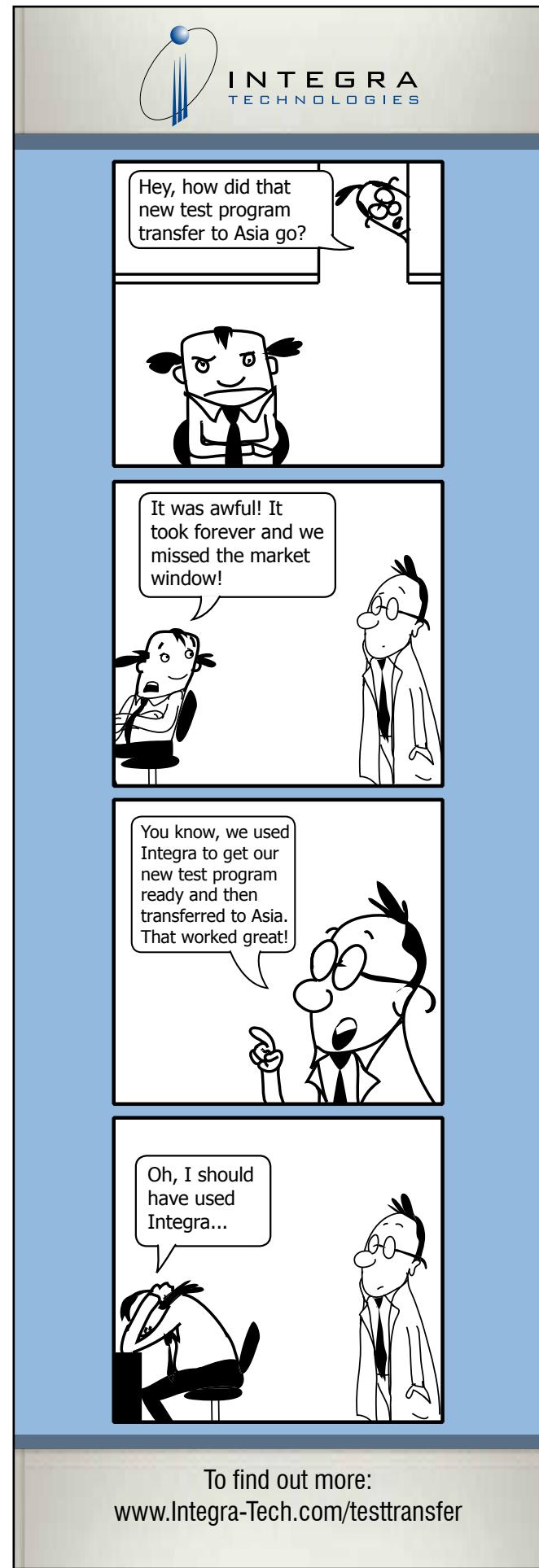
### Acknowledgements

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*Lay Wai Kong, GLOBALFOUNDRIES Assignee, SEMATECH, may be contacted at LayWai.Kong@sematech.org; Victor Vartanian, Member Technical Staff, 3D Enablement Center, SEMATECH, may be contacted at Victor.Vartanian@sematech.org; Andy C. Rudack, Standards and Metrology, 3D Enablement Center, SEMATECH, may be contacted at andy.rudack@sematech.org.; Klaus Hummler, Senior Principal Engineer, 3D Interconnect, SEMATECH, may be contacted at Klaus.hummler@sematech.org; and Alain C. Diebold, Executive Director, Center for Nanoscale Metrology, CNSE*



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# Getting Your New IC to Market Faster

By Joe Holt [*Integra Technologies*]

**G**etting a new Integrated Circuit (IC) to market almost always takes longer than anticipated and developing an effective test process is frequently a meaningful contributor to that problem. This article will discuss ways to improve time to market by making the test development process more efficient. So what is the test development process? Test development is defined as “that process whereby you reconcile the chip you set out to make with the one you actually fabricated.” Test company experience shows that ~80% of new IC designs do not meet one or more of the major original design goals. As implied in this definition, during the test process is when a company finds out exactly what device they will actually take to market. The natural consequence of this “reconciliation” process is that the time it takes to get the new IC to market will vary proportionately to the number and severity of the differences between the IC’s intended design and reality.

A review of the test process helps to explain why that is. **Figure 1** shows the test process as most IC development schedules show it – a linear process that is not overly long or complex. In contrast, **Figure 2** shows the way the process works in the real world.

The real process is an iterative, indeterminate, back and forth dialog between the test engineer and the design engineer. The process follows the above loop for every function and parameter that is not meeting the original design spec. Sometimes the design is robust and only runs through the loop approximately 30 times. But sometimes the issues are more numerous and the number of iterations through the loop can go into the hundreds. Clearly, reducing the number of iterations

– and the length of time each iteration takes – will decrease the time it takes to get the IC into the customer’s hands.

The goal of this iterative loop is achieving something called “Correlation”. Again, a definition may be helpful: “Correlation is when the test engineer and the design engineer agree that the test process is satisfactorily assessing the performance and functionality of the new device.”

As data is examined, and test approaches debated and experiments run, the number of iterations through the loop, shown in **Figure 2**, continues to add up – frequently causing significant delays in getting the IC to market.

Even after correlation is initially achieved, the test development loop may need to be reentered. Correlation is initially achieved based on a set of tests that is a subset of all the possible combinations of the way a device can be used. Different customers in different markets supporting different applications can all use the device differently. Even the biggest semiconductor manufacturers can’t test for all the possible combinations of conditions that the device may see in the myriad of applications in which it may end up. Thus, as new failure mechanisms are discovered by end-customers, the test development and correlation “loop” is often reentered.

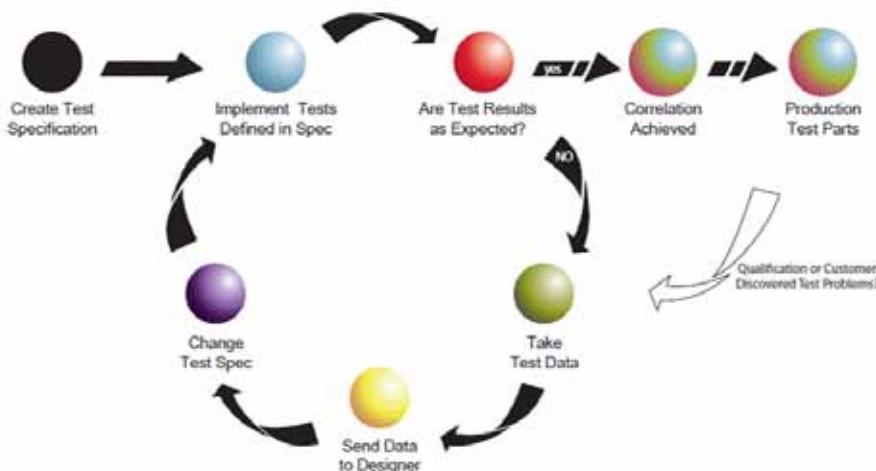
So how can we shorten this iterative test development and correlation loop? The

answer to this question has been analyzed, researched, and reported in countless papers presented throughout the history of the semiconductor industry. However, one of the often-overlooked ways to make the test development process more efficient is to physically locate the test engineer and the design engineer as close as possible. The faster the inevitable iterations through the test development loop can occur, the faster correlation will be achieved and the faster the new device can be shipped in high volume. This physical co-location is not a new idea, but it is one that is more and more difficult to achieve with the migration of much of the silicon processing to Asia. While this migration has contributed to lower overall costs, it has also forced people farther apart physically – and for the highly interactive test development process, this can significantly delay time-to-market.

One alternative that can notably improve time-to-market is to do the test development, qualification, and initial production at a supplier that is physically located near your development team. In particular, if you are a US based design team, working with a US based backend service provider to achieve initial (and post-initial) production correlation can save valuable time. Once the product is correlated and stable, let the Asian suppliers do what they do best – manufacture and ship high volume



**Figure 1:** Ideal development test flow.



**Figure 2:** Real world development test flow.

production at low costs. This solution can be particularly appealing to the 1200 or so small to medium-sized fabless semiconductor companies located across the globe that don't command the same level of attention at Asian suppliers as the top semiconductor companies.

The increase in time-to-market resulting from this iterative reality isn't difficult to compute. Take the number

of times that the loop in **Figure 2** is circumnavigated and multiply by the extra time it takes to communicate over 8-12 time zones to Asia versus the time it takes to communicate 0-3 time zones in the US. Experience shows that the same amount of data that can traverse the test development loop in 24 hours between the US and Asia can speed by in the US in as little as 3 hours.

Add to that the potential for language-related delays, where the question being asked by the designer or the reply from the Asian test engineer is not clearly understood, and the additional time to iterate with Asia can easily double.

What does that mean for time to market? Let's take two examples: one at 30 iterations through the "loop" in **Figure 2** (probably the best that can be hoped for even with a simple device) and one at 150 iterations through the loop (probably towards the high end of the iterative spectrum). Let's also assume that we are only working Monday through Friday from 8:00 AM to 8:00 PM.

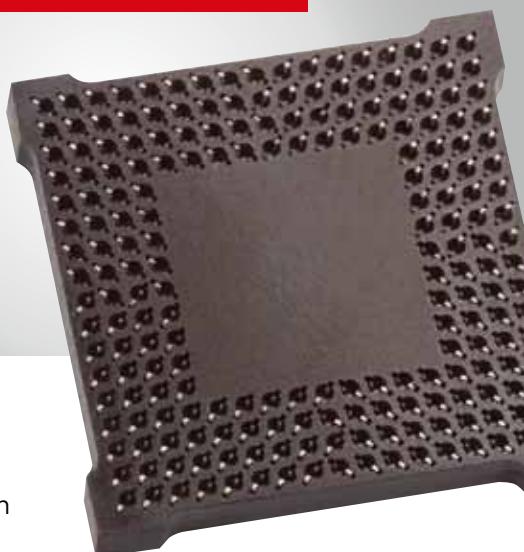
In the US, 30 needed iterations divided by a conservative three iterations per day is 10 working days or two 5-day work weeks. In Asia it will be 30 needed iterations divided by one iteration per day equals 30 working days or six 5-day work weeks. What would typically take two weeks in the US just took six weeks

(continued on Page 55)

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# Considering Electronic Product's Quality Specifications by Application(s)

By Ephraim Suhir [Bell Labs Research]

Qualification specs and testing (QT) is the major means that electronics industries use to make their devices into products. It is highly desirable, of course, that QT specs consider, to whatever extent possible, the most likely application(s) of a particular electronic product and take into account the physics of its possible failure, time in service, loading (demand) conditions and consequences of failure. While reliability level cannot be low, it does not have to be higher than necessary, but has to be adequate. The best way to assure adequate reliability is to understand the reliability physics underlying a particular anticipated or detected mode of failure, and to develop and implement on this basis, effective and consistent ways to quantify reliability. This approach would assure satisfactory performance of the product in the field, while also optimizing its reliability, i.e., to determine if a well-understood and substantiated reduction in its reliability level could be translated into considerable cost savings, so that the best compromise between reliability, cost-effectiveness and time-to-market is established and implemented for a particular product, considering its most likely application(s). However, this is not the case with today's practice. Electronic devices and systems that passed the existing qualification specs often fail in the field. There is a general consensus in the electronics community that today's industries need new approaches to qualify their products.<sup>1</sup> The author is convinced that the existing QT practices and specs should be improved to an extent that if an item passed these tests, there should be a quantifiable way to assure that it will satisfactorily perform in the field in the most cost-effective fashion considering, for a particular application or a mission, the most likely

operation conditions, time in operation and consequences of failure. Secondly, the application of the probabilistic risk management (PRM) approach can improve dramatically the state-of-the-art in the field and that the probabilistic-design-for-reliability (PDfR) concept should be considered as the first and crucial step of such an approach; and that lastly, the most adequate QT methodologies, procedures and specifications could be developed on this basis.

## Probabilistic-design-for-reliability (PDfR) Concept

In today's electronics manufacturing world, devices are typically designed, fabricated, and shipped to customers regardless of the particular anticipated use, i.e., are essentially the same for quite different applications. As a result, when reliability is imperative and consequences of failure might be disastrous, the devices (systems) have to be re-qualified, so that, as a minimum, their mean-time-to-failure (MTTF) is assessed. In such a situation it is too late, of course, to improve the design or to change materials. The only effective way to build a sufficiently reliable system out of insufficiently reliable devices is to use redundancy on the system level and to employ, if possible, technical diagnostics, prognostics and health monitoring (PHM)

during the product's operation.

The PDfR approach (**Figure 1**)<sup>2-9</sup> proceeds from the concept that reliability cannot be left to the operation stage of the product's life, i.e., that reliability evaluations and assurances cannot be delayed until the product is fabricated, installed, and put into operation. The reliability should be controlled and its assessments should be carried out, to a greater or lesser extent, at all the stages in the product's life. One should have in mind that reliability is conceived at the early stages of the product's design; implemented during its manufacturing; evaluated — considering customer and QT requirements — by electrical, optical and mechanical measurements and testing; checked during fabrication; and, if necessary and appropriate, could/should be maintained and managed in the field by using methods, techniques, instrumentation of diagnostics, and PHM engineering. It is certainly desirable and advisable to create a healthy, "genetically" adequate, product and to consider that at the time of the product's conception (design); to maintain its health, if possible, by regular checkups (technical diagnostics) and, if necessary, also by the PHM effort. Since nothing and nobody is perfect, predictive modeling techniques based on applied probability and probabilistic risk management (PRM)



Figure 1: PDfR is the answer.

should be widely applied at all stages of the product's life. The difference between a highly robust and an insufficiently robust product is, in effect, "just" the level of the probability of failure at a certain stage of the product's lifetime. The predicted probability of operational failure (or non-failure) is the most logical, the most natural and should be employed as the ultimate criterion of product's robustness. The complete, comprehensive and effective PDfR effort should include:

- Failure-oriented-accelerated-testing (FOAT), often referred to as highly-accelerated-life-testing (HALT)
- Simple and physically meaningful predictive modeling, both analytical ("mathematical") and computer-aided (simulations)
- Development of adequate QT specifications, methodologies and procedures, and algorithms suitable for conducting sensitivity evaluations
- Technical diagnostics and PHM algorithms, instrumentations and techniques,
- Methods for understanding the role of the human factor in the product's (system's) overall (end-to-end) performance, such as, say, likelihood of a particular mission success (assurance) and safety.<sup>10</sup>

### Three Classes of Products

The following three classes of electronics products could be distinguished from the standpoint of their most likely applications, consequences of failure, cost considerations, need for adequate qualification specifications and best practices and, hence, from the viewpoint of the product's short- and long-term operational reliability expectations and requirements (**Figure 2**).

**Class I** examples include some highly important warfare, military aircraft, battle-ships, spacecraft. The product (object) has to be made as reliable as possible. Failure is viewed as a catastrophe and should not be permitted. The consequences of failure are significant and could be associated with loss of human lives, bad publicity, major legal actions and even with the national security and prestige. Cost is an

important, but not a dominating factor. Products are typically not manufactured in large quantities and usually have a single customer, such as the government or a big firm. Reliability requirements are defined in the form of government standards, such as, e.g., US Military Standards (MIL-STDs). These standards not only formulate the reliability requirements for the product, but also specify the methods to be used to demonstrate the reliability, and often

even prescribe how the system should be manufactured, tested, and screened. It is the customer, not the manufacturer that sets the reliability standards. In the author's opinion, the PDfR approach should be a must for this class of products.

**Class II** examples include telecommunication networks; civil engineering structures (bridges, tunnels, towers, passenger elevators, etc); ocean-going ships and offshore structures;



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### Particular PDfR approach should be different for different classes of engineering products

- **Class I.** The product has to be made as reliable as possible. Failure should not be permitted. Examples are some military or space objects
- **Class II.** The product has to be made as reliable as possible, but only for a certain level of demand (stress, loading). Failure is a catastrophe. Examples are civil engineering structures, bridges, ships, aircraft, railroad vehicles, cars
- **Class III.** The reliability does not have to be very high. Failures are permitted, but should be restricted. Examples are consumer products, commercial electronics, agricultural equipment



**Figure 2:** Three classes of products from the reliability assurance standpoint

commercial aircraft; railroad carriages; cars; some medical equipment; some military and aerospace electronics. The product (object, system, structure) has to be made as reliable as possible, but only for certain anticipated level of demand. Failure might be a catastrophe, and could be associated with loss of human lives and with significant economic losses. If the actual loading (waves, winds, earthquakes, temperatures, shocks and vibrations, or any other off-normal environmental conditions) happens to be larger than the anticipated (specified) level (demand), the product might fail, although the probability of failure (PoF) is determined and specified beforehand and should/could be sufficiently low. Products are highly expensive, but, because they are produced in large quantities, they have to be cost effective. The products are typically intended for industrial markets, rather than for the government or for individual consumers. These markets are characterized by high volume production, but also by fewer and more sophisticated customers than in the case of Class I products (commercial market). The reliability standards/specifications come as industrial standards (JEDEC, Telcordia, ASTM, etc) that often include some MIL-STDs or MIL-STDs requirements.

The vendor and the customer usually negotiate some form of a reliability-and-quality contract. This contract might include both the appropriate industrial specification requirements and the

requirements of a particular customer. For some products (e.g., cars), a low number of field failures are considered acceptable, and could be even specified beforehand. It is typically the customer, rather than the manufacturer, who sets the reliability standards. The PDfR approach might be used in one form or another, if there is a wish/need to minimize the product's cost and shorten the time-to-completion without compromising the acceptable reliability level. It is highly desirable that the PDfR approach is also applied to military and aerospace electronics, with consideration of the specifics of this field, to come up with the best compromise between reliability, cost-effectiveness and time-to-completion.

**Class III** examples include household items, household and commercial electronics, consumer products, agricultural equipment. Reliability does not have to be high. A reasonable level of failures is acceptable, as long as the product is sellable, and the failure rate is within the expected range. The demand for the product is driven primarily by its cost and time-to-market, and not by its reliability. The latter should only be adequate for customer acceptance and reasonable satisfaction. Simple and innovative products that have a high degree of customer appeal and are in considerable demand are able to prosper, even if they are not very reliable. The typical market is the consumer market. An

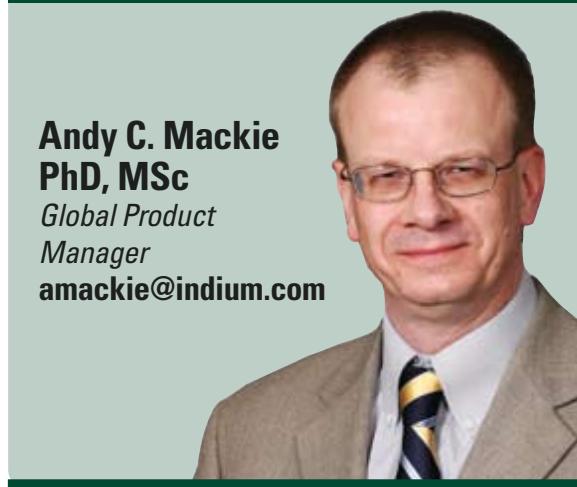
individual consumer is a small part of the total consumer base. The product is inexpensive, and manufactured in mass quantities. The reliability testing is limited, and the improvements, if any, are implemented based on the field feedback, which, however, might not be easy to collect and analyze. No special reliability standards might be needed and followed. It is the customer satisfaction on the statistical basis that is the ultimate criterion of the product's viability and quality. It is the manufacturer, not the consumer, who sets the reliability standards, if any. Probabilistic design for reliability (PDfR) approach might be used, if there is a wish to minimize the product's cost and shorten the time-to-market without compromising the adequate (not very high though) reliability level.

### Novel QT Should Consider Most Likely Application(s) of an Electronic Product

The novel QT, when PDfR and FOAT (which is an important constituent of the PDfR) are implemented, could be viewed as a “quasi-FOAT,” “mini-FOAT”, a sort-of the “initial stage of the actual, full-length, FOAT”. Such a “mini-FOAT” could be perceived as an effort that more or less adequately replicates the initial non-destructive, yet full-scale, stage of the regular FOAT. The duration and conditions of such a “mini-FOAT” QT should/could be established based on the observed and recorded results of the actual FOAT, and should be limited to the stage when no failures, or a limited and a “prescribed” (anticipated) number of failures, are observed, and that “what one sees” during such a “mini-FOAT” is in accordance with “what one got (observed)” in the actual full-scale FOAT. PHM technologies could be of a significant help in this effort. PHM “canaries” could be concurrently tested to make sure that the safe limit is not exceeded. It is noteworthy that “burn-in” is needed regardless of a particular design-for-reliability approach and can be interpreted as a special type of a “mini-FOAT”.

# Semiconductor Assembly

**Andy C. Mackie**  
**PhD, MSc**  
*Global Product Manager*  
[amackie@indium.com](mailto:amackie@indium.com)



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## Conclusion

When reliability is imperative, the ability to quantify it is a must. PDfR concept enables one to improve dramatically the existing practice for qualifying electronic and photonic products when high reliability is imperative. The suggested PDfR approach complements the existing system-related and human-psychology-related efforts, and, most importantly, bridges the gap between the three critical areas responsible for the system and/or mission performance – electronics-and-photonics reliability engineering, vehicular technologies and human factor. Although the approach is highly promising and fruitful, further research, refinement, and validation efforts will be needed before the suggested approach becomes practical. ☺

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Ephraim Suhir, Bell Labs Research, may be contacted at [Suhire@aol.com](mailto:Suhire@aol.com)

# Advanced Flip Chip Packaging Platform for Fine Pitch, High Performance and Low Cost Applications

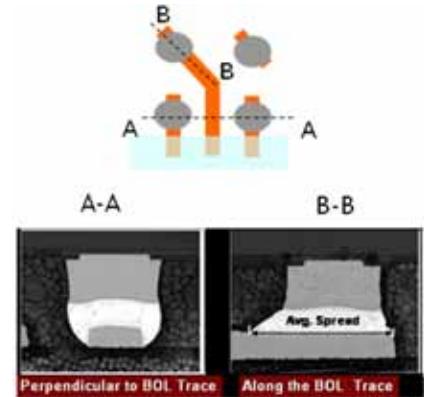
By Raj Pendse, Ph.D. and Mukul Joshi, *[STATS ChipPAC Inc.]*

**A**s the adoption of flip chip technology for semiconductor IC packaging continues its rapid growth trend, there is a new level of interest and demand for greater device performance, superior reliability and lower cost to meet the rigorous requirements of today's advanced electronic devices. A novel advanced flip chip packaging\* technology enables such a paradigm shift where conventional flip chip technology faces stiff manufacturing challenges in scaling to very fine bump pitches, ultra-high densities and advanced wafer technology nodes while achieving superior performance and long term reliability at a price point that is below other packaging solutions available today. **Figure 1** describes the basic building blocks of this technology, which features flip chip interconnect, copper (Cu) column bump with Pb-free solder cap and bond-on-lead (BOL) substrate pad design with an open solder resist (Open SR) scheme. The package is assembled with either capillary or mold underfill for a conventional mass reflow (MR) process

or a thermo-compression bonding (TCB) process.

A key attribute of this technology is its inherent scalability to progressively finer pitches and higher escape routing densities that is in line with the requirements of increasing input/output (I/O) densities of newer silicon (Si) nodes and the emergence of 3D through silicon via (TSV) interconnection. The BOL pad with Open SR together with very fine pitch Cu bump interconnects offers superior electrical performance due to increased I/O density. With flexibility in supporting both conventional MR and TCB interconnect techniques, fcCuBE technology addresses a wide spectrum of bump pitch range from > 200 $\mu$ m to below 80 $\mu$ m.

A subtle but crucial feature is the ability to utilize MR despite the Open SR design. This is made possible by the unique phenomenon of "self confinement" as shown in **Figure 2**. An optimal design of the bump diameter and solder cap size in the Cu column bump in conjunction with the geometric dimensions of the substrate pad promotes a condition wherein the

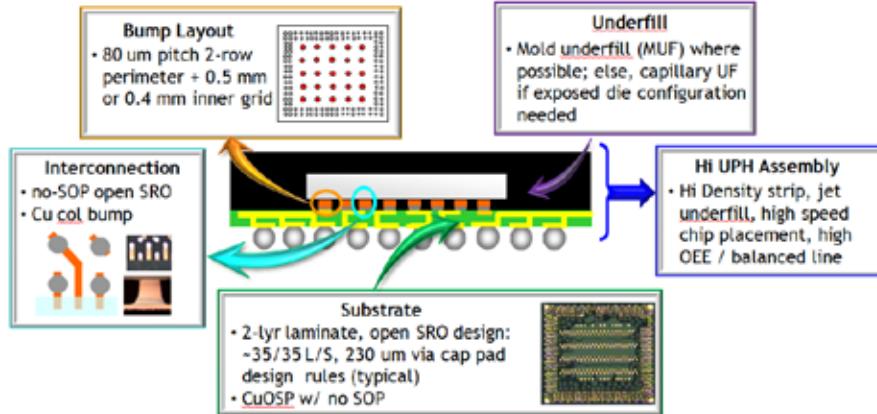


**Figure 2:** Illustration of "solder self confinement". molten solder is retained or confined within the space between the non-fusible portion of the bump and the substrate pad by virtue of the surface tension forces. As such, the solder "self-fillets" to form a natural solder joint without the need of a solder mask to confine its flow.

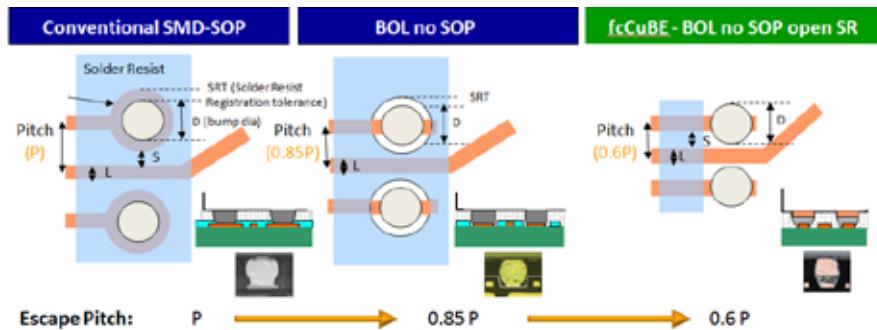
Recent customer case studies have shown that this technology not only has the capability of very fine bump pitches, but also offers superior assembly and thermo-mechanical reliability performance in advanced Si nodes. The extreme low- $k$  or ultra low- $k$  (ELK/ULK) interlayer dielectric (ILD) materials used in conjunction with advanced Si nodes are more fragile and are therefore more susceptible to cracking or delamination during flip chip assembly, or subsequent package reliability stress. The uniquely robust interconnect formed using Cu column with BOL helps alleviate thermo-mechanical stress, thus offering better compatibility with the latest Si nodes (40N/28N/20N).

## Achieving High Density at Low Cost

The BOL interconnection comprises



**Figure 1:** Key Elements of fcCuBE – Cu bump, BOL pad and Open SR design.



**Figure 3:** fcCuBE helps improve escape routing efficiency.

a composite Cu column bump (Cu column + solder cap) bonded directly to a narrow trace with open SR design as illustrated in **Figure 3**. This structure enables a significantly finer routing density and escape pitch with relatively coarse substrate design rules. As such, this technology may be viewed as a means to achieve lower cost through relaxed design rules for a given density, or conversely, as a means to achieve a higher density for a given set of design rules and cost.

The realization of lower cost by

virtue of the more routing-efficient BOL interconnection is further quantified in **Table 1**. Typical substrate design rules and escape densities for conventional build-

Standard flip chip 1-2-1 Build Up Solder Mask Defined - Solder on Pad	fcCuBE 2 Layer Laminate Cu column, no Solder on Pad (nSOP), BOL / Open SRO
20/20 um Line / Spacing 80 um SRO +/- 25 um SR registration 120 um via cap pad	35/40 um Line / Spacing open SR 350 um via cap pad
Bump Pitch (um)	190 um
I/O Density	Effective pitch
	95 um
	# Routable I/O*
	481
% of real IC designs that "fit" in stated des rules	40%
Cost Impact	Substrate
	1.0 X
	Package
	1.0 X
	0.71 X
	0.9 X

**Table 1:** Quantification of routing efficiency and cost benefits based on a presumed 8x8 mm die.

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in routing density/cost is evident. Based on the two cases illustrated, it is clear that the new interconnect structure can be employed to either achieve higher routing densities with relaxed substrate design rules compared to a conventional 1-2-1 BU substrate, or conversely, significantly higher routing densities for a given set of design rules.

A cost reduction in the range of 15-55% is achieved for the substrate, which translates to ~10-30% cost reduction for the package. Analysis of I/O densities of actual devices shows that >60% of IC designs spanning the gamut from GPU, chipset, application processor, baseband and RF/Analog can be routed in 2-layer laminate substrates from a point-to-point escape routing perspective based on the design rules illustrated in **Table 1**. Additional layers may be required for power/ground and signal integrity management based on the design and application.

The package interconnection can be implemented with either the MR technique by taking advantage of the unique “solder self confinement” phenomenon, or TCB at very fine pitches below 60 $\mu\text{m}$  or so. MR is the preferred approach due to its lower assembly cost compared to TCB. In our estimation, the pitch and I/O density range covered by MR captures a large majority of the design population for flip chip packages down through the 20nm Si node. The Open SR feature essentially obviates the use of a solder mask for confining solder flow thereby eliminating the routing space otherwise consumed for tolerances in solder mask opening size and its registration to the metal pattern.

## Cost Benefit

For a traditional Au wire bond package, the substrate and the wire bonding each comprise approximately 40% of the total cost (for a total of 80%) with other elements representing ~20%. The cost for a traditional flip chip package for the same

application increases by ~35% as a result of the premium for the build-up substrate required to achieve the escape routing in a flip chip area array configuration. In contrast, this advanced flip chip packaging solution enables the use of low cost substrates, which takes away the substrate premium as a major impact factor. With concomitant improvements like MUF for further reductions, it can achieve a cost point below that of the Au wire bond solution and in the same range as the Cu wire bond case, but significantly lower than the traditional flip chip case. **Figure 4** illustrates these points.

## Scalability to Fine Bump Pitches

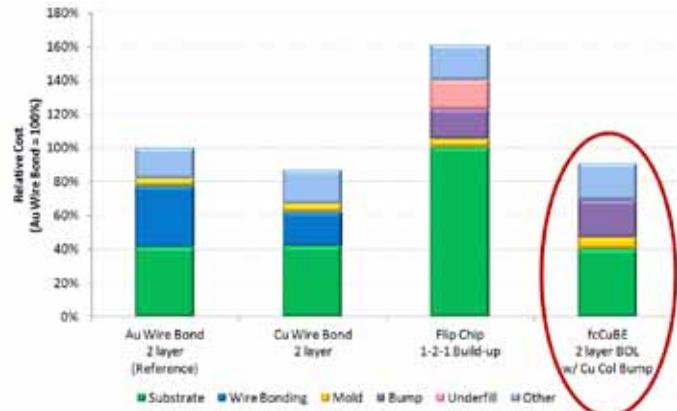
Conventional flip chip packages using SnPb or SnAg alloy bumps face significant manufacturability challenges as the bump pitches go below the 140 $\mu\text{m}$  mark, resulting in small stand-off heights and reduced spacing between the bumps. Significant yield challenges are imposed on substrate suppliers due to reduced solder mask registration targets and tighter tolerances at the finer pitch. This advanced flip chip technology provides a wider process window due to the inherently columnar interconnect shape of the bumps. In addition, the BOL/no SOP/open SR combination makes it more conducive to underfilling without compromising the process window.

A test vehicle (TV) comprising a 12 x 12 mm mfcFBGA package

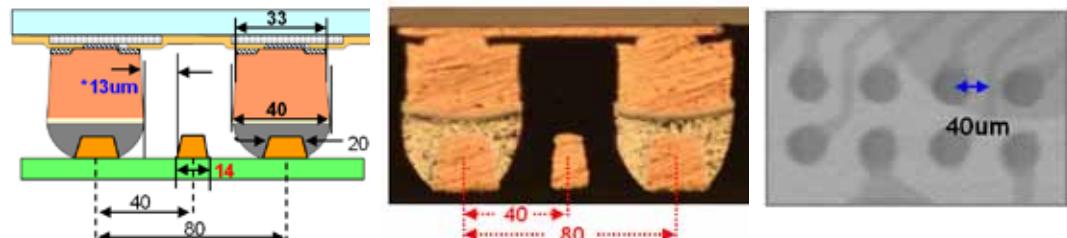
and 80 $\mu\text{m}$  bump pitch flip chip was used to verify assembly and reliability robustness of this new technology at fine pitches using both MR and TCB assembly methodologies. An escape trace between the 80 $\mu\text{m}$  pitch BOL pads was used to represent an effective pitch of 40 $\mu\text{m}$ . A 40 $\mu\text{m}$  bump diameter used in conjunction with a 20 $\mu\text{m}$  BOL pad width enabled the very fine bump pitch structure shown in **Figure 5**. This level of dense routing would not be feasible with a conventional flip chip package architecture using an alloy bump and standard SMD+SOP pad.

The TV described above passed JEDEC standard reliability tests including moisture preconditioning, unbiased HAST, temperature cycle condition “B” and high temperature storage (at 150°C). Prior reliability studies have confirmed robust reliability margins passing up to 3000 TCB cycles and 3000 hours of HTS testing with no evidence of intermetallic degradation or Cu consumption.<sup>1</sup>

The same TV was also qualified using TCB with equally successful assembly and reliability results. **Figure 6** shows the novel flip chip package



**Figure 4:** Relative package costs and cost reduction achieved through use of this technology.



**Figure 5:** 80 $\mu\text{m}$  BP fcCuBE TV design, with optical & X-ray photo of the interconnect structure



**Figure 6:** fCuBE interconnect of 80um/40um pitch TV using a Thermo Compression Bonding (TCB) process.

interconnect structure qualified for the same 80 $\mu\text{m}$ /40 $\mu\text{m}$  bump pitch TV using the TCB process.

### Scalability for Advance Si Node Applications

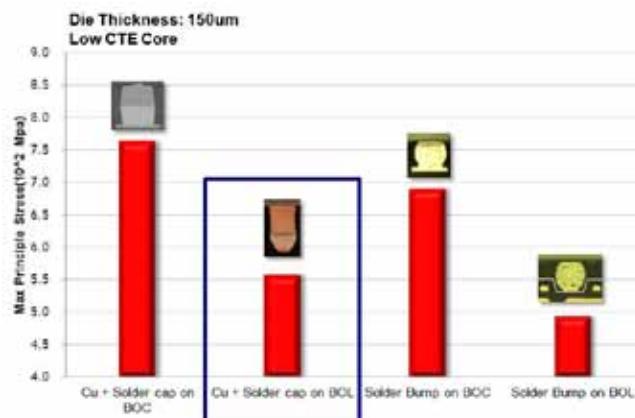
The transition to advanced Si nodes is an inevitable trend. The advanced nodes tend to utilize more fragile ELK/ULK dielectrics, which are potentially more susceptible to interlayer dielectric delamination or cracking during assembly or reliability stress. This is exacerbated by the need for "green" or Pb-free solder interconnect materials that tend to be mechanically stiffer and induce higher

stress on these more fragile ELK layers. Considerable development work and improvements have been directed in this area by device makers, foundries, assembly service providers as well as equipment and metrology tool providers to ensure assembly process and materials compatibility.

The BOL interconnect structure of this advanced flip chip technology offers yet another benefit

in significant relief of this stress on the bump UBM and ELK layers due to the more compliant geometry of the resulting interconnect. Thermo mechanical stress simulation along with empirical data gathered on multiple 40nm and 28nm Si test vehicles and live products have confirmed this benefit convincingly as published in prior literature.<sup>2,3,4,5</sup>

**Figure 7** shows comparative



**Figure 7:** Thermo-mechanical stress simulation results.

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analyses of the BOL interconnect structure and the conventional bump on capture pad (BOC) structure for the cases of Cu bump and Pb-free alloy bump. A global model was applied to the corner most bump region and a local model used to extract the maximum principal stress in the UBM and ELK layers.

The BOL pad structure significantly reduces the stress irrespective of the bump type. This technology offers lower stress compared to conventional flip chip with Pb-free bump, thus proving to be a superior solution for advanced Si node devices. While the leg with Pb-free bump and BOL pad shows the lowest stress, it is not a practical option since it is typically incompatible with fine pitch and open solder mask designs.

Empirical data was generated using a 14x14mm fcFBGA daisy chain TV with a 28nm 10x10mm<sup>2</sup> silicon die with full stack of ELK dielectric that was packaged using this advanced flip chip technology and Pb-free alloy bump with SMD+SOP substrate pad. Comparative analysis of the two technologies was completed using multiple reflow test without using any underfill material (Hammer test). Acoustic microscopy analysis was done at multiple read points to check for ELK crack signature and compare the onset of the same as well as failure rate between the two.

**Table 2** summarizes the hammer test results showing superior overall performance of the advanced flip chip packaging structure, confirming its higher robustness and better compatibility with advance Si nodes and ELK dielectrics.

## Summary

An innovative flip chip packaging platform provides the following compelling advantages over traditional flip chip technology:

- dramatically improved combination of I/O routing density and cost;
- seamless scalability to fine pitches (sub-80µm), advanced Si nodes (sub 20nm) and new package configurations (3D TSV);
- inherent compliancy and reduction of mechanical stresses within the interconnect structure including fragile Si inner layers.

These attributes were made possible by unique structural and process features comprising a “composite” Cu column bump structure with solder cap, BOL pad and open SR design with no SOP on substrate, and the flexibility of applying MR assembly with mold underfilling or TCB for first-level interconnection with a common substrate design. Long-term reliability on live product devices notably including 28nm and 20nm Si nodes was demonstrated. The cost reduction benefits were quantified and case studies on actual product applications were shared.

The result is a powerful, flexible and cost-effective flip chip technology platform that will broaden the application space for flip chip and allow more control in design cost and performance optimization. With successful deployment into multiple customer products and applications, this technology is positioned to meet the evolving product needs across a wide range of end-applications

including mobile processors, network ASICs, consumer ICs and other high-performance applications. 

\* fcCuBE™

## Acknowledgments

The authors would like to extend their sincere thanks to YC Kim, and the entire Flip Chip Engineering team at STATS ChipPAC Korea for the underlying development work on fcCuBE technology and successfully enabling multiple customer product designs to date.

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Raj Pendse, Ph.D, Chief Marketing Officer, STATS ChipPAC, may be contacted at [Raj.Pendse@Statschippac.com](mailto:Raj.Pendse@Statschippac.com); Mukul Joshi, Director, Product Technology Marketing – Advanced Technology, STATS ChipPAC, may be contacted at [mukul.joshi@statschippac.com](mailto:mukul.joshi@statschippac.com).

Run	Input Factor				Output				
	Cu / Ni / Solder Height	Solder comp.	Substrate	Reflow Peak Temp	EOL (C-SAM)	10x (C-SAM)	20x (C-SAM)	30x (C-SAM)	40x (C-SAM)
1	/60 um	Sn 1.8Ag	SOP Sub	255 +/-3°C	Passed (0/30)	Passed (0/30)	ELK crack (10/30)	N/A	N/A
2	A/B/C	Sn 1.8Ag			Passed (0/30)	Passed (0/30)	Passed (0/30)	Passed (0/30)	ELK crack (12/30)
3	A/B/C	Sn 1.8Ag	BOL Sub		Passed (0/30)	Passed (0/30)	Passed (0/30)	Passed (0/30)	Passed (0/10)

Cu column height: A, Ni thickness: B, Solder cap height: C

**Table 2:** Hammer test results data on 28N full metal stack test vehicle.

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# Finding Failures in Novel Memory Devices and Modules

By Paul Sakamoto, [DCG Systems Corp.]

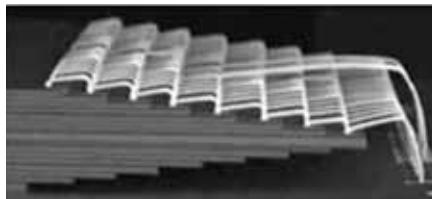
T

he latest memory designs offer failure sources that are difficult to find and debug using traditional bitmap, automatic test equipment (ATE) and lab bench tools. Shrinking geometries in all products, stacked die modules, and the insertion of increasingly complex logic in Flash devices are all pushing debug, failure analysis (FA), low yield analysis (LYA) and product engineers to look for new tools. Not only is the bad bit “needle” lost in a multi-billion transistor “haystack,” these days the stacks are stacked! This article highlights a few tools and methods that go beyond the bitmap and use frequency, time, and temperature to help find and diagnose memory component failures.

## Finding the Failed Chip in the Stack

For most memory devices, regardless of technology, finding a failing bit is usually pretty straightforward given that most of the chip is functioning. This is why SRAMs have been used to help debug new fab processes and manufacturing lines for many years even if the company has no intention to market them. The classic memory device structure of X and Y addressing enables failed bit isolation from which a physical failure analysis (PFA) can be specified to find the root cause. Although different in detail, the single chip flash memory also allows for rapid and precise bit failure location in the array. However, the rise of super stacked die packages benefits from a new diagnostic approach. Some highly stacked die in a single package are pictured in **Figure 1**.

These multi-chip NAND stacks have become relatively commonplace with eight high modules in volume shipment and sixteen just around the corner. As shown in the X-ray photo, wire bonding



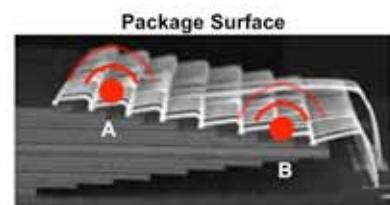
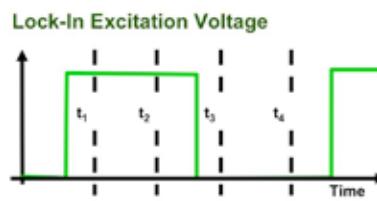
**Figure 1:** Flash memories are being stacked up to 16 die deep. (Source: Toshiba)

is still prevalent and brings with it the possibility of shorts and other failures induced during the encapsulation process. TSV connections will eliminate some of these issues, but will bring on failure risks of its own. In all cases, high-density stacking limits the usefulness of traditional X-ray due to the complexity and three-dimensional nature of the resulting composite device. A practical failure analysis must narrow the search area before going to X-ray.

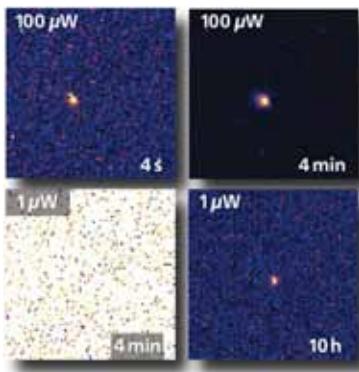
A relatively new method to answer this challenge is called lock in thermography (LIT)<sup>1</sup>. This technique combines an advanced thermal emission camera, high resolution optics, timed device heat stimulus and timed thermal data capture at the surface of the package to provide depth of defect information – the physical “Z” axis (**Figure 2**). In practice, profile data for material properties of the die, encapsulation material, and other packaging elements are gathered

from samples and this information is then used to interpret the data from the failed devices. When the correct depth and relatively precise planar location of a failure is known, more traditional high magnification X-ray or invasive PFA can be focused on that area for further investigation. All of this is done in a non-invasive and non-destructive manner that does not destroy the evidence.

In addition to the revolutionary capability of 3D analysis, LIT provides very high contrast, low noise evaluation of point heat sources from an individual die. Static thermal analysis tends to “lose” small heat sources (< a few mW) in the background noise. This is caused by increasing the image exposure time to capture small heat sources. Using static measurements, the device and the camera are left on for enough time to sense the small heat emitting failure. Unfortunately, the rest of the die is heating during this time, so the contrast will not increase and the image will not improve. LIT increases signal to noise ratio (SNR) and highlights the failure location by eliminating static thermal radiation. Operating at high LI frequency (e.g. >20Hz) further reduces heat spreading and improves localization accuracy. Therefore the longer the image acquisition period, the more accurate and sensitive the results (**Figure 3**).



**Figure 2:** The Excitation Voltage waveform is applied to the module power pins. Defects located at point A will emit heat that will be sensed faster and with higher amplitude than emission from point B. This data is converted to depth information. (Source: DCG Systems, Toshiba)

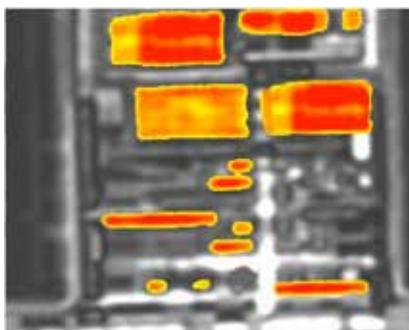


**Figure 3:** LIT allows acquisition to be as long as needed. The result is nearly complete control over noise, contrast and image resolution, as shown above. (Source: DCG Systems)

microprocessors from five or six years ago. As a result, logic circuits have become a significant portion of the NAND component failure distribution.

Laser voltage imaging (LVI) is a valuable tool that has been used in advanced logic debug for over a year and is gaining traction in the memory realm. An advanced unit will have a laser scanning microscope (LSM), laser source, detector and a frequency analyzer. This enables mapping of the chip areas showing activity at a particular frequency of interest. When overlaid with computer-aided design (CAD) data, the overall circuit functionality can be known. The search can then be further narrowed using other techniques such as laser voltage probing (LVP), which allows actual signal capture from a circuit node.

When combined with scan-based testing, LVI usually narrows a failure investigation down to the point that LVP can be used to narrow the failure source down to the gate level. Using a CAD layout overlay on top of the LVI image, the engineer can decide what circuit nodes to check for proper waveform activity (**Figure 4**).



**Figure 4:** LVI highlights areas of frequency activity to help isolate failures. The color is proportional to amplitude. (Source: DCG Systems)

Then, LVP can be focused on a particular circuit node to show the actual waveform. The device is not harmed because LVP is non-contact and uses a laser beam that is modulated by the signal passing through a node.

An even deeper level of precision analysis can be applied to all memory technologies. This is the nanoprobe (**Figure 5**). Although partial de-layering is often required to expose the metal contacts, nanoprobe is a powerful tool to measure transistor and gate characteristics. The smallest geometries can be analyzed using nanoprobe. A typical measurement of an SRAM cell is shown in **Figure 6**.

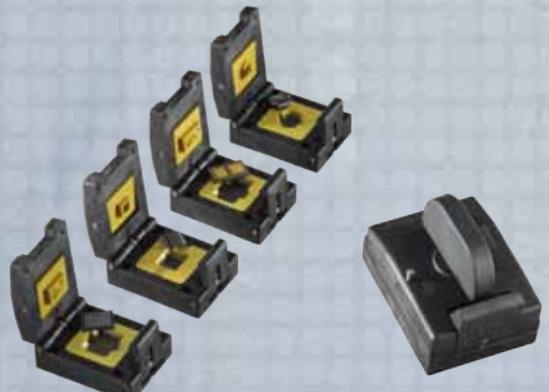
## Embedded Logic Challenge

Modern flash memories use a larger than ever amount of embedded logic for tighter control of the device access, speed, and programming algorithms. There are also fault tolerance circuits that include on-the-fly error detection and correction. These blocks of logic now occupy as much as 20% of the area in a NAND chip and have the complexity of mainstream

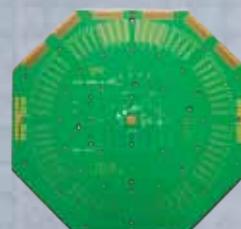
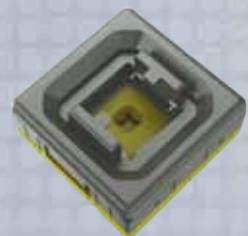
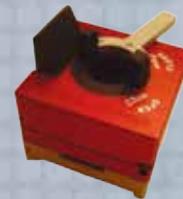


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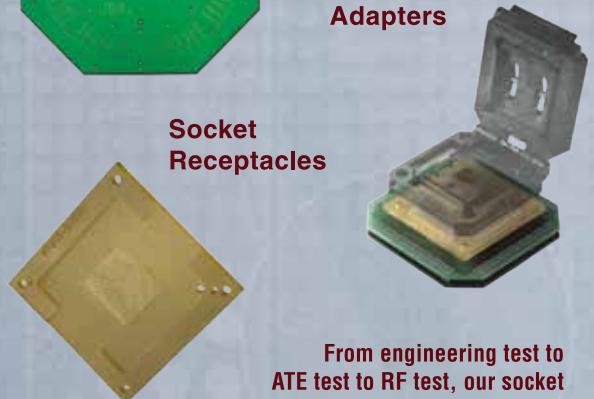
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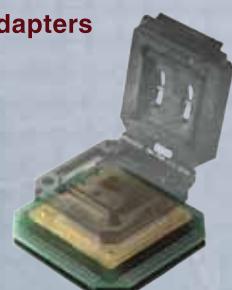


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Nanoprobing is useful for measuring transistor characteristic curves as well as helping isolate non-visual defects or parametric defects. Since the scale of the contacts is so small, the imaging is provided by a scanning electron microscope (SEM), which is used to target the probes as well as house them in its vacuum chamber. The probes are operated via extremely precise positioners that not only need to get the probe on the contact,

but keep it there long enough to make a measurement. This is very difficult, but modern machines can maintain contact with the most advanced processes available today.

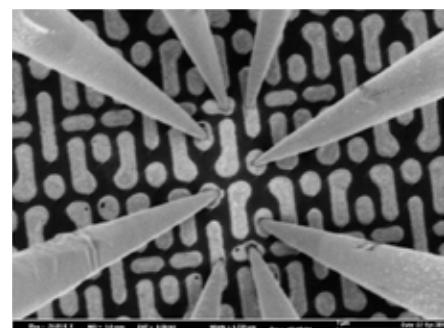
### Conclusion

Although new FA problems continually arise, new tools are constantly rising to the challenge. These are just a few of the new technologies that are being applied to



**Figure 5:** This system contains both LVI and LVP capabilities as well as other active and passive emission instrumentation. (Source: DCG Systems)

all levels of memory diagnosis from the multi-chip package down to the transistor level. The capabilities would have defied belief just a few years ago, but are now becoming necessary to producing both three-d and sub 28nm semiconductor products.



**Figure 6:** 35nm probe tips touching metal contacts for SRAM analysis. (Source: DCG Systems)

### Acknowledgements

The author would like to thank Dr. Rudolf Schangen and Dr. Christopher Nemirow of DCG Systems for their help in gathering material for this article.

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# An Innovative Approach to Achieving the Best Cost Structure for Semiconductor Companies

By Bharat Desai, Contributing Editor

**P**roducing a given product cost-effectively and continuously comprehending how to reduce product cost faster than falling average selling prices (ASP's) for achieving the desired gross profit margin are perhaps the two major cost challenges faced by semiconductor companies. This article discusses how to set up an organization to meet these challenges, day in and day out, i.e., what strategies, systems, processes, tools, and techniques a small or midsize company needs to put in place and employ. The methodology discussed here is based on the idea that if you seek excellence, success will follow.

"The vendor with the best cost structure sets the rules", noted Bob Johnson of Gartner, Inc., in his Semiconductor Industry briefing on June 11, 2009. Johnson cited this as his number one future financial viability strategy for the semiconductor industry.

The question then becomes, how do you achieve the best cost structure for your company?

Achieving "the best cost structure" means achieving the lowest possible cost. In other words, minimize the total cost of doing business and consequently increase profitability, day in and day out.

This innovative approach is about setting a mind-set: "reducing cost continuously" a way of life. It addresses both how to improve short-term performance and at the same time set up the organization for long-term gains. In addition to solving two major business problems, as discussed in the next section, one more way the approach minimizes the total cost is by offering a path of how major business functions can be performed significantly better. For example:

One of the best ways to control and manage inventory is to take a system approach instead of focusing only on a few traditional approaches like reduce cycle times, forecast planning, etc. The system approach should include how to establish "processes/systems" to control and manage "monitor" inventory, etc. The innovative approach includes nineteen "how to" approaches.

## Taking an Innovative Approach

Taking the approach described here will effectively minimize the total cost of doing business. It does so by solving two major business problems: execution and cost structure.

## Improving Execution

As Larry Bossidy, Ram Charan, and Charles Burck say in their book, *Execution: The Discipline of Getting Things Done* "Execution is not just tactics; it's discipline and systems. Execution is a specific set of behaviors and techniques that companies need to master in order to have a competitive advantage."

Execution can be improved by attaining operations excellence, by improving operational efficiency, by creating a well-oiled organization and by coming up with related strategies, systems, processes, tools, and techniques for establishing the discipline to get things done.

Operations excellence is achieved by applying best business practices and by improving operational efficiency. In this context, best business practices means understanding your operations and costs thoroughly, getting the best return on investment (ROI), satisfying internal and external customers, and knowing that you are never done with the job. "Never done

with the job" means understanding the importance of continuous improvement which in turn means you will always have to raise the improvement bar in every aspect of the company's operations. The company needs to come up with a corporate continuous improvement process that demonstrates how to make improvements in people, product, productivity, and process.

Improving operational efficiency means developing systems and processes for talent retention and management to save time and resources and ultimately save on the cost of labor.

A well-oiled organization is one that makes "eliminating unnecessary costs" a way of life; a strategic rather than tactical imperative. In other words, a well-oiled organization is one that consistently operates at minimum cost and is created by optimizing human interactions, continuously improving man, machine, and method productivity, and by putting in place cost control and reduction measures.

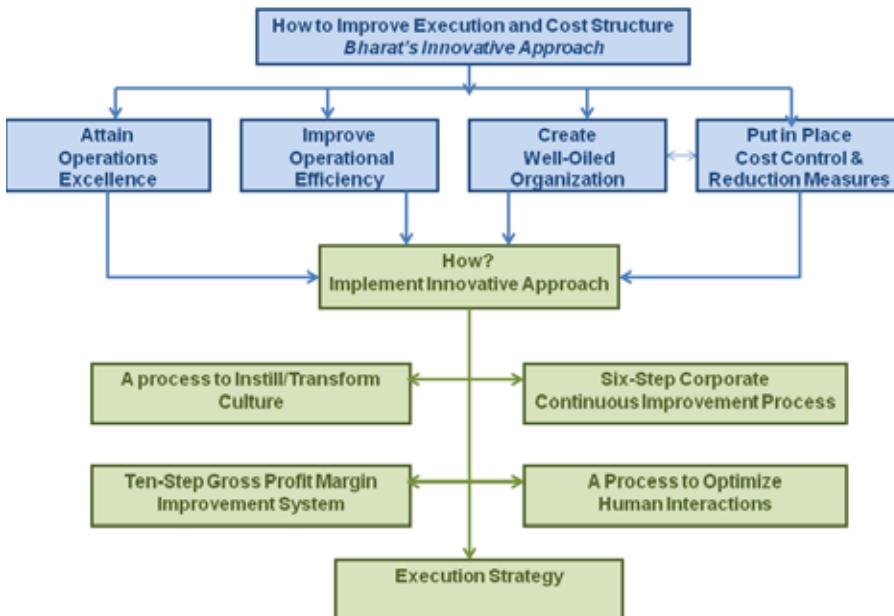
In order to achieve operations excellence, to improve operational efficiency, and to create a well-oiled organization, the company needs to set and accomplish two goals:

1. Define and transform the company culture
2. Establish a company-wide continuous improvement process.

As shown in **Figure 1**, an eight-step process to instill and transform the company culture and a six-step corporate continuous improvement process can help realize these two goals.

## Improving Cost Structure

One of the best ways to improve cost structure is to improve the gross profit



**Figure 1:** An innovative approach for creating a well-oiled machine.

margin (GPM) of products. The GPM can be increased by taking a step-by-step systematic approach that includes all short-

term and long-term cost control and reduction measures. For example, the first step of the system should be to

generate an accurate standard cost. This is a very important step because the accurate standard cost drives desired behaviors and actions.

In summary, the major elements of the approach to improve execution and cost structure are:

1. A ten-step gross profit margin improvement system
2. A six-step corporate continuous improvement process for people, product, process, productivity
3. An eight-step process to instill and transform the company culture
4. A process to optimize human interactions
5. An execution strategy

### Optimizing Human Interactions

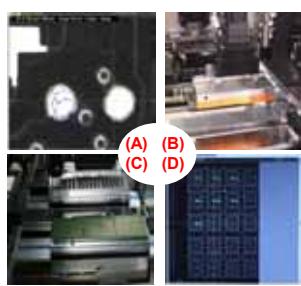
Organizational dynamics is a system of internal customer/supplier relationships. If these relationships are in alignment (i.e. the need of the customer is met by the supplier), the effectiveness of the organization can be optimized. A process

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Tuesday, July 10—

Contemporary Packaging: Achieving Cost Advantage through Innovation  
10:30am–12:30pm, TechXPOT North

IEEE/CPMT Workshop:

“THIN IS IN”: Thin Chip and Packaging Technologies as Enabler for Innovative Mobile Devices

1:00pm–4:30pm, SF Marriott Marquis

Wednesday, July 11—

The 2.5 and 3D Packaging Landscape for 2015 and Beyond  
1:00pm–3:30pm, TechXPOT North

Thursday, July 12—

MEMS and Sensor Packaging  
10:30am–12:30pm, TechXPOT North

ITRS Back End of Line Technologies

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has been discussed to improve the customer/supplier relationships.

The Execution Strategy should include corporate and ground level implementation plans. Why don't most organizations follow such a powerful and practical methodology? There are several possible reasons that could become potential obstacles, such as:

- Too much focus on New Product Development
- Too much focus on demand generation
- No expertise on how to achieve the best possible cost structure
- Cost is an afterthought – treated as tactical issue rather than strategic
- Top executive background – Most have Sales/Marketing/Technical
- Unavailability of step-by-step guide/reference book
- Myth: Not enough bandwidth (resources) to make process improvements

However, in order to improve short-

term performance and at the same time set up the organization for long-term gains, a company can convert these potential obstacles into future opportunities.

### Conclusion:

This innovative approach offers a methodology for small and mid-size organizations to become multi-million dollar companies. It will produce successful outcomes, even under the most difficult of circumstances because it is an old school approach that focuses on the fundamentals. It can help small companies become multi-million dollar companies by following the step-by-step guidelines discussed in the approach. Mid-size companies can also benefit by performing gap analysis: Determining what they have and what they need to implement to work their way up towards becoming a multi-million dollar company.

Practical solutions (strategies, systems, processes, tools, and techniques) are available to meet an organization's

execution and cost structure challenges and consequently help increase its profitability and revenue growth potential. ■

*Bharat Desai, contributing editor, may be contacted at bharat@shalshiv.com.*

*Bharat is writing a book about his methodology. The book will discuss how to attain a competitively-advantaged cost structure by achieving operations excellence and creating a well-oiled organization that consistently operates at minimum cost. A fact of doing a business is that companies need a competitively-advantaged cost structure in addition to competitively-advantaged products in order to survive and prosper.*

*The book is a guide for small to midsize hi-tech companies on becoming a company worth multimillions. The guidelines are in the form of strategies, systems, processes, tools, and techniques. Whenever possible, a checklist format is used for ease of understanding, training, tracking, and execution.*

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# GUEST EDITORIAL

## The Back End's Back Ache

By Lee J. Smith, [Microelectronic Industry Experts]

**A**re you concerned that your back end microelectronic assembly and test supplier, customer or position is sustainable in today's macro-economic morass?

First let's look at the recent financial trends for the publically-traded, broad-based Tier 1 advanced semiconductor assembly and test suppliers (SATS), which highlights a number of pain points. As shown in **Figure 1**; ASE, Amkor, SPIL and STATS ChipPAC had a combined \$10.8Bn in 2011 revenues (a paltry 1% gain vs. 2010), combining to control 45% share of the total SATS market. (Note: Powertech is excluded as they primarily supply memory assembly and test services, but when counted these top 5 hold a 50% share, whereas the next 15 SATS combine to hold only a 17% share). The pain point is what investments they made to realize this 1% gain in revenue. Over the past 2 years, these Tier 1 SATS invested on average 17.6% of their annual sales into new capital equipment, from a low of \$250M estimated for STATS ChipPAC in 2011 to a high of \$951M for ASE in 2010. Combined the top 4 invested \$3,755M in new capital equipment over the last 2 years - to realize a revenue gain of only \$135M for 2011. (Note: we are not looking at 2009 which was a horrible year for the SATS industry due to the world-wide recession). Now this is painful enough, but when also evaluating their gross margin trends; the question of sustainability begins to shout. As illustrated in **Figure 2**, in 2007 the gross margins for these Tier 1 SATS were in the 20 – 30% range, but by 2011 their margins had steadily eroded (despite major investments in advanced technologies), into the 15 - 23% range. Factors like, turnkey wafer bump, assembly and test raise

margins; while rising material costs and excess capacity depress margins. Factors aside, anyway you slice it this data is painful, and to answer the question of sustainability, a close look at the technology requirements and competitive landscape of the SATS industry going forward is warranted.

The second pain point is the technology requirements of the SATS industry going forward. Wirebond interconnected package assemblies are rapidly moving to either copper-based wires or small diameter fine-pitch precision gold wire bond assemblies. Both areas require development of new bond profiles and material sets as well as investment in the latest wirebonders. Flip chip interconnection is rapidly moving to lead-free and copper pillar bumping, along with development /

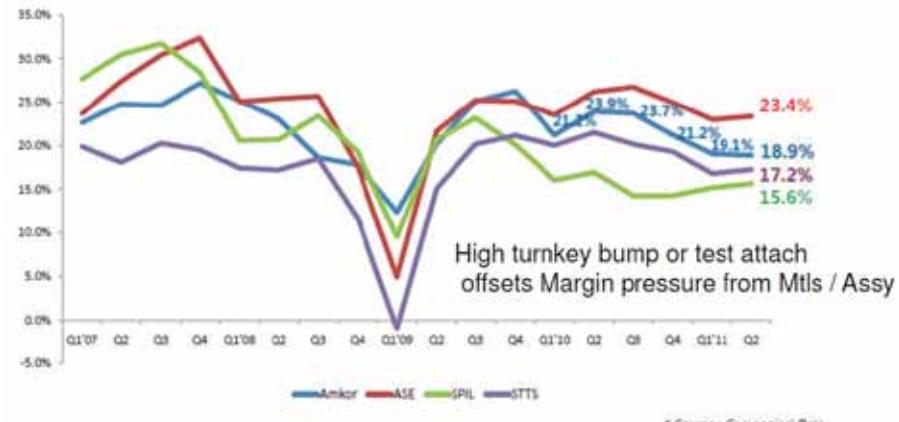
capacity investments for the new wafer bump and assembly processes required for these stiffer bumps on top of fragile ultra-low-k inner layer dielectric based ICs. But the biggest technology factors that are changing the SATS R&D investment levels and competitive landscape are the major transitions to wafer level packaging and 2.5 to 3D IC architectures with through silicon via (TSV) interconnects.

Over the past few years the top 4 SATS invested 2 – 4% of sales in R&D, when coupled with their Capex investments (described earlier), their investment intensity approached or exceeded 20% of sales; sadly the same level as their gross margins - are you feeling their pain now? If you are a major customer of the Tier 1 SATS requiring advanced package assembly

2011 Rank	2010 Rank	Company	Region	2010 Revenue	2011 Revenue	2010 Market Share (%)	2011 Market Share	Change 2010-2011
1	1	ASE	Taiwan	3,903	4,252	16.5%	17.7%	9.0%
2	2	Amkor Technology	USA	2,939	2,776	12.5%	11.6%	-5.5%
3	3	SPIL	Taiwan	2,104	2,024	8.9%	8.4%	-3.8%
4	4	STATS ChipPAC	Singapore	1,678	1,707	7.1%	7.1%	1.7%
5	5	PTI Tech	Taiwan	1,173	1,252	5.0%	5.2%	6.7%
Top 20 Total				18,139	18,493	76.9%	77.0%	2.0%
Other Companies				5,454	5,531	23.1%	23.0%	1.4%
Total Market				23,593	24,024	100.0%	100.0%	1.8%

Source: Gartner (April 2012)

**Figure 1:** SATS Revenue Table



\* Source : Companies' Data

**Figure 2:** Tier 1 Gross Margin Trends (company reported data)

and test solutions, the data points shown in **Figure 3**, should alert you that their pain may soon be yours, as SATS control today's key package platforms (share in unit terms except total available market (TAM)), which is based on Gartner data and forecast in SATS revenues vs. the TAM [note: Intel CPU in organic LGAs or BGAs and a good portion of the DRAM market are captive and not available to SATS.]

Now some can argue and I won't disagree, that the overall investment requirements and competitive landscape of the semiconductor industry is under severe pressure and significant changes are occurring and expected. As IC Insights has well documented, the capital intensity of the semiconductor industry has been declining each of the last three decades

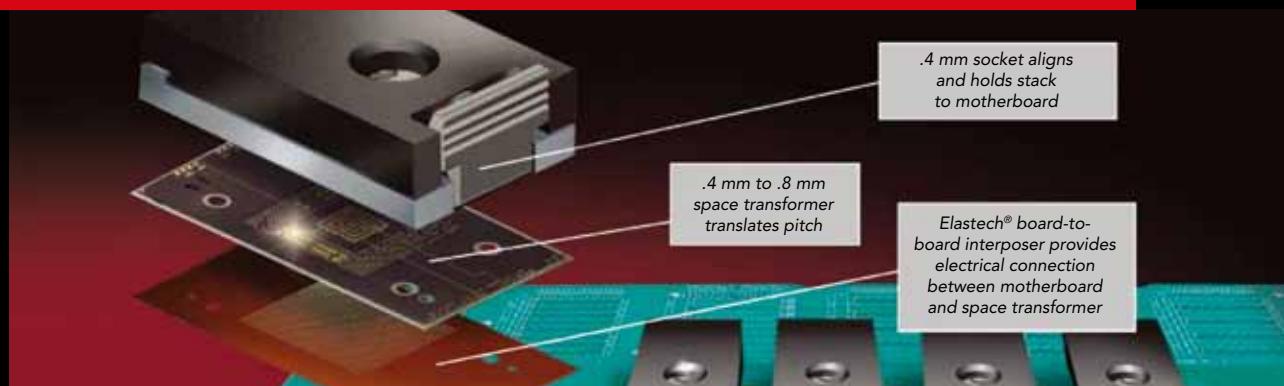
Pkg Type	Share 2010	Comments (Captive)
TAM	51% (of \$)	58% Frcst 2015
BGA	74%	On > 3Bn units (Intel)
CSP	64%	>49Bn units (FBGA)
Stack CSP (W/Bond)	61%	>2.3Bn units (Memory)
QFN	83%	>17Bn units

**Figure 3:** SATS Share of Overall Total and Advanced Packaging

from 26% in the 1990's to 17% forecasted over the next 5 years. Over this same time, the semiconductor industry invests ~16% of sales into R&D to achieve gross margins in the 40 – 60% range for an industry that tops \$300B in annual sales. However, no one argues that the transition to 450mm wafers will severely limit the number of suppliers that can afford to invest in their own mega-fab. What is debated is whether you will need 2

hands to count the number of 450mm suppliers and whether the equipment suppliers can afford to develop these advanced tools for such a small customer base. What is clear is that very little if any attention is being given to the 450mm tools required for the back-end, including who can afford to develop and procure tools for probe, bump, wafer level packaging (WLP), wafer thinning, wafer support systems for TSV back-end, dicing and

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die attach systems, to name some key current processes.

450mm fabrication (projected for the end of the decade) will clearly change the competitive landscape, but prior to that, the wafer level packaging and TSV process requirements are rapidly bringing the foundry suppliers into the back-end services segment. TSMC has been widely projecting their chip on wafer on substrate (CoWoS) 3D packaging solutions for 2013 applications. The capabilities and availability of TSV-bearing high-density silicon or glass-based interposers is a serious supply concern for those planning to procure or produce 2.5D IC architectures. The performance advantages of 3D IC architectures like wide I/O for mobile multimedia applications is currently offset by the lack of production

capability and competitive business models to integrate multi-cell TSV-bearing mobile processors with wide I/O lower power DDR memory. Samsung is currently the only supplier capable of turnkey delivery of the wide I/O 3D IC components demanded by next-generation smartphone and tablets to stream video and run advanced graphics processing without sacrificing battery life. Samsung is already a major turnkey 3D packaged component supplier to Apple for iPod, iPhone and iPad devices. TSMC is already a major supplier of wafer bumping, wafer probe, and wafer level packaging services to their fabless customers. The capital investment levels that these Tier 1 foundry suppliers including Global Foundries range from \$2.8 to \$7.3Bn over the past 2 years. Also their R&D levels dwarf the \$40 to \$100M level

the SATS can invest annually as the foundries enjoy gross margins in the 40 – 50% range.

### Conclusion

So clearly the SATS competitive landscape is changing significantly and they will have to make significant changes in their financial performance in order to effectively compete in the WLP and 3D IC eras. The SATS and foundry suppliers must develop innovative business models that enable them to collaborate and compete concurrently. If the SATS can't reverse their financial trends, they are at risk of losing significance in this next era of advanced packaging. ■

*Lee J. Smith, President, Microelectronic Industry Experts, may be contacted at leejsmith@q.com*

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(continued from Page 22)

bonding technology for advanced semiconductor applications, is showing strong potential for major cost savings in 3D memory applications by replacing standard die-stacking methods with the company's proprietary DBI® wafer-stacking technology.

Memory stacking is one of the most intriguing applications of 3D integrated circuit technology, as it has the potential to enable much higher memory density in a given footprint. But to date, process costs have been high, driven by the challenges of die thinning, handling of the thinned dies, and development of reliable interconnect processes.

Ziptronix DBI combines proprietary wafer-level low-temperature oxide bonding and interconnection reportedly resulting in substantial cost reductions in customer-driven development work focused on server and portable memory applications. That work is now moving into the prototype evaluation stage. DBI® has been proven in the backside imaging (BSI) sensor marketplace, another cost-sensitive sector, and can reportedly deliver cost savings of up to 80% compared to copper thermo-compression bonding. Because the process creates extremely strong low-stress bonds, it allows wafers to be processed and thinned after bonding, greatly simplifying process requirements by eliminating the need to handle thinned wafers and/or dies. In addition, DBI® offers high interconnect density and alignment accuracy and is fully compatible with damascene interconnect processing, opening new avenues for foundry-based through-silicon via process flows. Additionally, the resulting uniform, high hybrid bond strength is said to enable the highest vertical stacking density and the thinnest overall height of finished 3D devices. It also supports a range of post-bonding test and repair strategies.

"This new collaboration shows that silicon supply chain companies have taken notice of how well our bonding and interconnect technologies are performing in the image sensor space, and that they are eager to utilize Ziptronix processes in other applications," said

Ziptronix CEO Dan Donabedian. "We see great potential for DBI® across the board in 3D, and plan to announce licensing agreements outside the image sensor space later this year."

### VTI Technologies is now Murata Electronics Oy

Following the acquisition of VTI Technologies Oy, by the Japanese company Murata Manufacturing, VTI has recently changed its company name. The new company name is Murata Electronics Oy. At the same time, the company has adopted Murata's visual identity with the Murata logo.

"Today is a memorable day: VTI Technologies Oy has become Murata Electronics Oy. The change of company name and visual identity clearly and strongly highlights the fact that this company is now an integral part of Murata," says Mr. Tsuneo Murata, President of Murata Manufacturing. "Our aim is to strengthen the Murata brand worldwide, and this change supports our strategy. VTI has been recognized as a pioneer in MEMS technology, and now we want Murata to be the top-of-mind name also for high-quality MEMS sensors, in addition to other Murata products."

Mr. Shinji Ushiro, the new CEO and President of Murata Electronics Oy as of 1 June says Murata's objective is to become one of the main global MEMS companies. "By exploring the market needs and by developing competitive MEMS products,

we believe that we can reach this objective", he says. With the new company name, a new website has also been launched for Murata MEMS sensors: [www.muratamems.fi](http://www.muratamems.fi). The website presents MEMS accelerometers, inclinometers and gyroscopes, as well as MEMS sensor

elements (dies) manufactured by Murata Electronics Oy – the former VTI. sp

### Getting Your New IC to Market Faster (continued from Page 33)

in Asia – and if the language issue multiplier is present it could make the delay 9 to 12 weeks.

If the same figure is run for the 150-iteration loop, the result is a US time of 10 weeks and an Asian time of 30 weeks plus any language multipliers. And this doesn't include additional correlation iterations due to qualification failure reconciliation or iterations due to initial customer failures. These are meaningful differences in time-to-market for any company.

### Conclusion

While there are good suppliers in Asia that are competent at test development and qualification, it's critical to know who they are and that their "A-Team" will be working on your project throughout its introduction and initial production. Even then the time zone and language barriers will cause a certain amount of additional delay – it is nearly unavoidable. Rest assured, there are several US-based test suppliers available to US based fabless semiconductor companies interested in getting to market faster rather than slower. sp

*Joe Holt, VP of Business Development, Integra, may be contacted at Joe.Holt@Integra-Tech.com*

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<b>HanMi Semiconductor</b> <a href="http://www.hanmisemi.com">www.hanmisemi.com</a> .....	2&3
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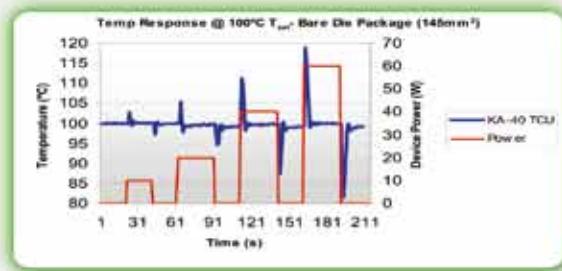
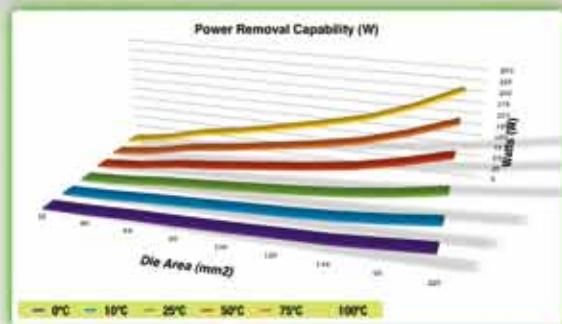
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